

Metal Silicides in CMOS Technology: Past, Present, and Future Trends

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ABSTRACT: Metal silicides have played an indispensable role in the rapid developments of microelectronics since PtSi was first used to improve the rectifying characteristics of diodes in early 1960s. This work first provides a brief historical overview of the many different silicides, and, correspondingly, the different processing methodologies used in the past. With regard to the present use of silicides in CMOS technologies, a convergence becomes clear with the self-aligned technology using only a limited number of silicides, namely, TiSi_2 , CoSi_2 , and NiSi . A section on fundamental aspects is included to cover thermodynamics and kinetics, which are essential for understanding the silicide formation processes. The advantages and disadvantages of TiSi_2 , CoSi_2 , and NiSi are analyzed with the development trend of CMOS technologies as a measure. Specifically, the reactive diffusion and phase formation of these silicides in the three terminals of a metal-oxide-semiconductor device, that is, gate, source, and drain, are scrutinized. The review ends with an extended discussion about future trends of metal silicides in micro/nanoelectronics, with reference to the potential material aspects and device structures outlined in the International Technology Roadmap for Semiconductors.

I. INTRODUCTION

The rapid advancement in microelectronics during the last 40 years has been realized through miniaturization and integration of the electronic devices. Advances in miniaturization and very-large-scale integration (VLSI) allow for computer intelligence to be built into products that are smaller, integrate more complex functions, consume less power, and cost less. According to the 2002 update of the International Technology Roadmap for Semiconductors (ITRS),¹ this rapid pace of development will continue well into the next decade. It is known that metal-oxide-semiconductor field-effect-transistor (MOSFET) is the basic building block for the absolute majority of today's electronic systems. Therefore, the focus is placed on the use of metal silicides for MOS devices in the present article. A cross section of two modern MOSFETs placed side-by-side is shown schematically in Figure 1, with a metal silicide layer present in the three electrode termi-

nals, gate, source, and drain for both transistors. The silicide layer is usually formed simultaneously in all six electrode areas. The two transistors are of opposite polarity, one n-channel MOSFET (nMOSFET) built directly on the p-type substrate and one p-channel MOSFET (pMOSFET) built inside the n-well, that is, in turn first formed on the same p-type substrate as shown. Constructed simultaneously on the same substrate, the two transistors are usually connected in series between the power supply terminals in an electronic circuit to minimize standby power dissipation, that is, the complementary MOS (CMOS) technology. Among many technical parameters, the gate length of a MOSFET, which is one of the most critical indicators of the integration technology, will decrease below 10 nm by year 2016, in order to attain the desired technological gain and economical profit. The predicted development trend in downscaling of the gate length from ITRS is shown in Figure 2 along with the past success in keeping up with the trend first predicted by Moore

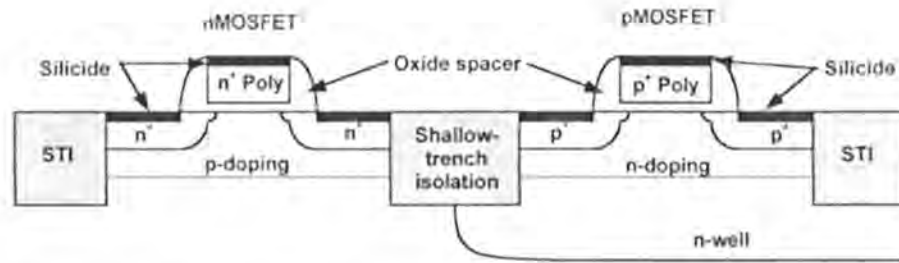


FIGURE 1. Cross section of modern CMOS transistors with an n-channel MOSFET (nMOSFET) and a p-channel MOSFET (pMOSFET).

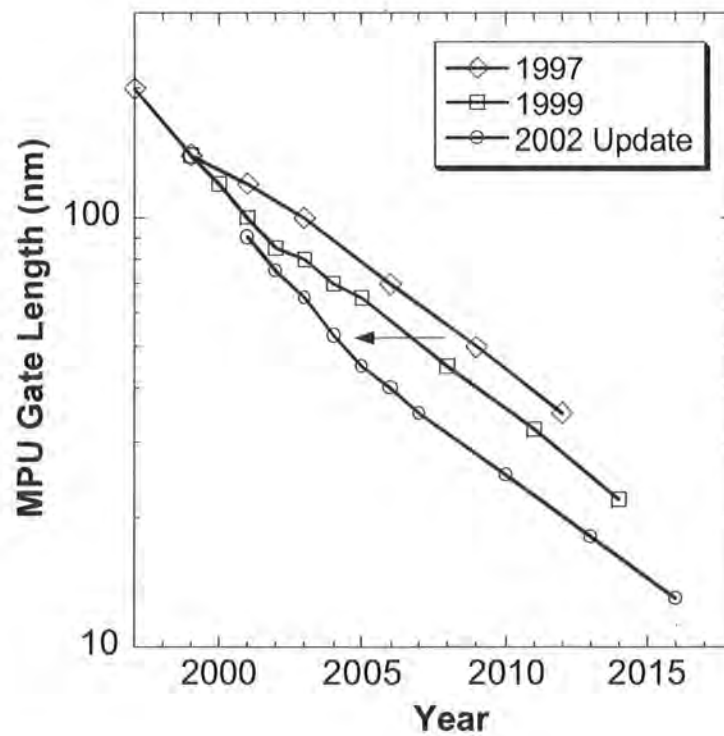


FIGURE 2. MPU printed gate length as predicted in ITRS 1997, 1999 and 2002 update. The arrow points to a more and more aggressive scaling.

in the 1960s.² As can be seen, the development pace has, in fact, experienced acceleration during the latest decennium, reflected as a downward bending of the curves in Figure 2. This experience has also encouraged scientists and engineers to take even more aggressive and daring approaches in order to speed up the developments.

In the large vocabulary of solid-state electronic devices,³ metals often constitute one of the key components rather than merely act as external electrical contacting. Examples of such devices are numerous, here just to mention a few frequently encountered ones such as MOSFETs, Schottky diodes, metal-insulator-semiconductor switches (MISS), and metal-base transistors (MBT). As the electrical contact between metal and semiconductor is directly relevant to the present review, how the electrical contact resistivity should be scaled according to ITRS in order to deliver MOSFETs with the desired performance is shown in Figure 3. The demand on low-resis-

tivity contacts has clearly been lessened when comparing the specifications in the two editions of ITRS in 1999 and 2002. Depicted in Figure 4 is the ITRS prediction for how the junction depth (a), silicide thickness (b), and sheet resistance (c) in the source/drain regions of a MOSFET should scale. The requirements for a decreasing source/drain series resistance and contact resistivity in smaller MOSFETs are well treated by Ng and Lynch,⁴ and interested readers are also directed to two more recent articles.^{5,6}

The main driver for the continuous advancement in VLSI has been the search for electronic circuits of higher performance and lower cost. In particular, the speed of an electronic circuit is one of the major concerns. To enhance the speed, parasitic capacitance and series resistance should both be minimized to reduce the RC (resistance-capacitance) time delay and increase the clock frequency.⁷ For this purpose of reaching higher speed, metal silicides have been utilized for con-

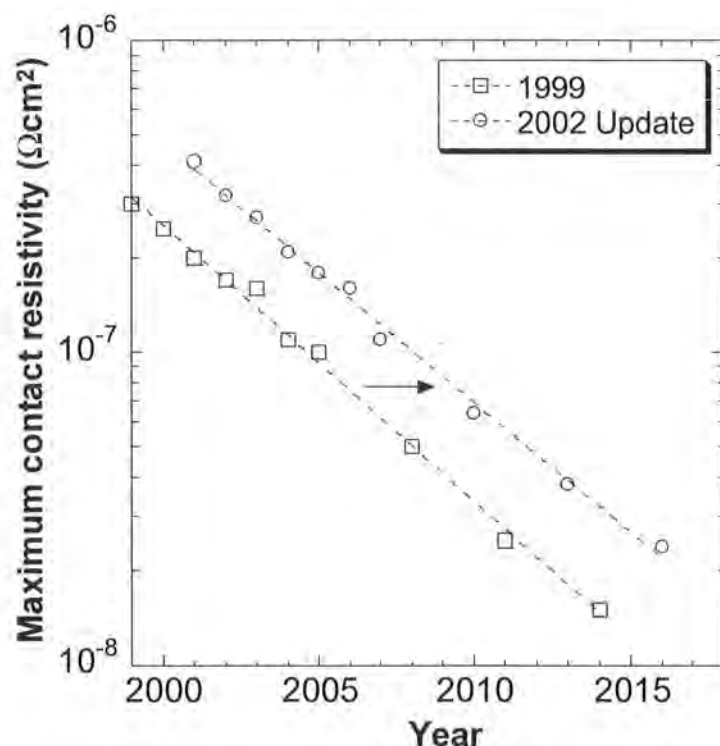


FIGURE 3. Maximum contact resistivity as predicted in ITRS 1999 and 2002 update. Note that the requirements have been relaxed in the 2002 update.

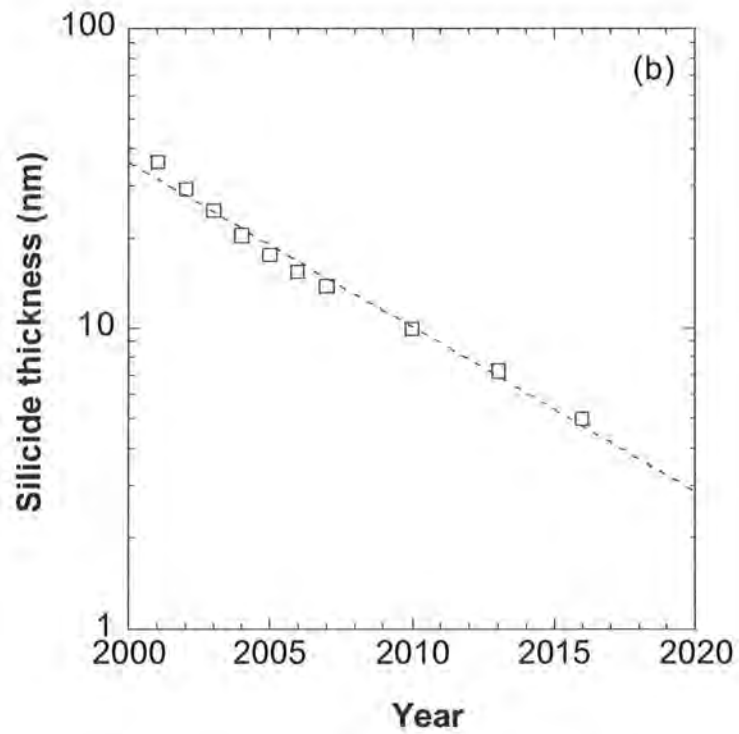
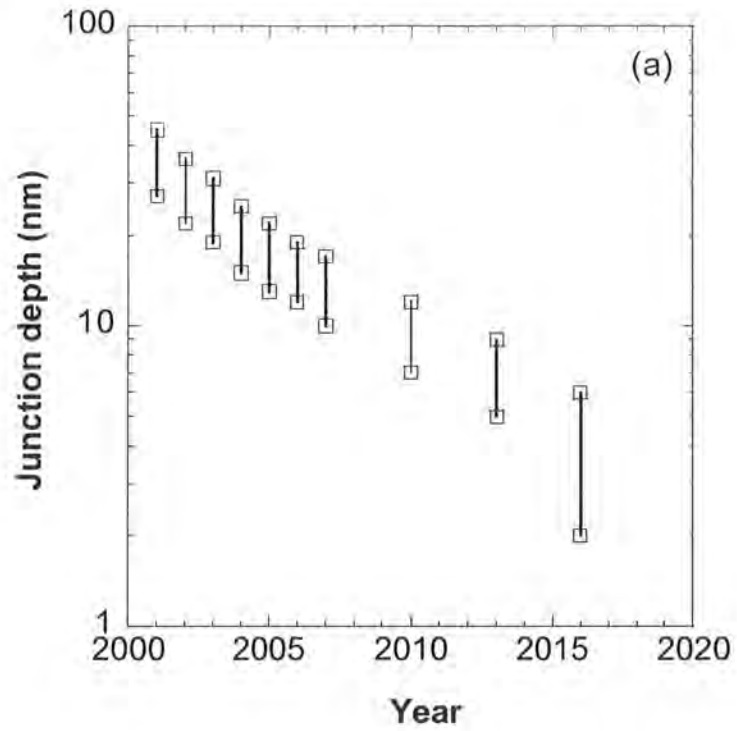


FIGURE 4. ITRS 2002 update predictions on (a) S/D extension junction depth, (b) silicide thickness, and (c) S/D extension sheet resistance.

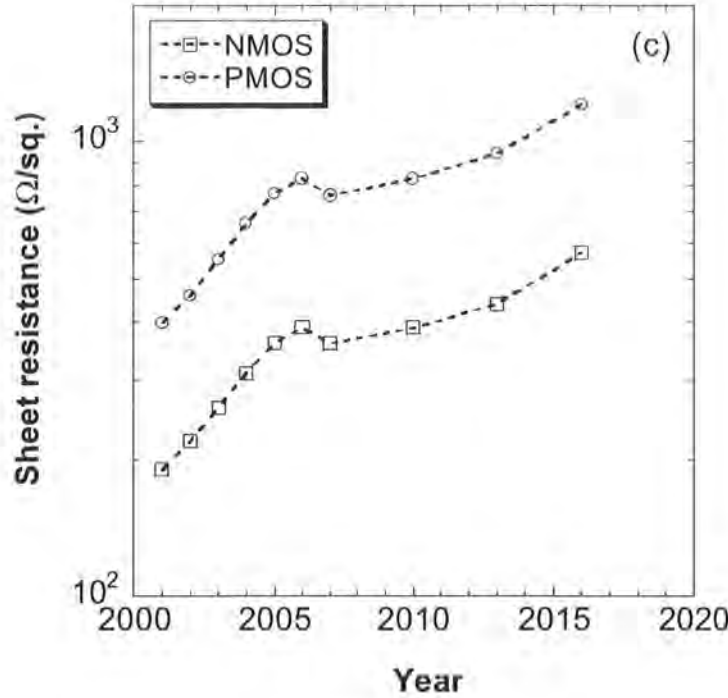


FIGURE 4. (continued)

tact metallization and local wiring.^{5,6} The choice of metal silicides in Si technology is quite natural, because they meet the basic requirements: low specific resistivity, low contact resistivity to both types of Si, high thermal stability, good processability, and excellent process compatibility with standard Si technology. Today, metal silicides are an inseparable part of an electronic device.⁵

The use of metal silicides in electronic devices can be traced back by almost four decennia when Pt,⁸ Cu,⁸ Mo,⁸ and W⁹ silicides were used for manufacturing planar Schottky diodes with enhanced rectifying characteristics. The thermal stability of the Schottky diodes was also greatly improved when using a metal silicide as metal contact, when compared with Al contact.¹⁰ PtSi¹¹ or Pd₂Si¹² were also used as contact layer between Al and Si to reduce the contact resistance, partly by preventing Al doping of n-type Si and partly by ensuring a good surface coverage of contacts by the metal electrode. Such efforts aiming at improving the contact reliability have been nicely summarized in Ref. 13, as schematically shown in Figure 5. Later, metal silicides found important

applications as current shunt to reduce the series resistance of local metallization usually made of heavily doped polycrystalline Si (poly-Si).^{14,15} To practically fabricate the current shunt, a metal silicide layer is deposited on top of a poly-Si substrate. Patterning of the silicide/poly-Si stack with the assistance of photolithography is used to define various desired features. This process is now often termed as POLYCIDE.¹⁶ Such a structure of silicide/poly-Si has an important position as the gate electrode of a MOSFET. The silicides used in the POLYCIDE technology are usually of the high thermal stability type, first with MoSi₂¹⁷ and then with WSi₂.^{16,18} Two other refractory metal silicides, TaSi₂^{19,20} and TiSi₂,²⁰ were also considered.

Because the POLYCIDE technique only addresses the high-resistance problem in the gate electrode, a limitation with the POLYCIDE concept is therefore the high series resistance retaining in the source/drain regions. Referring to Figure 6, reproduced from Ng and Lynch,⁴ the series resistance in the source/drain regions is composed of a contact resistance between metal and Si in the contact window of width l , R_{co} , a diffusion resis-

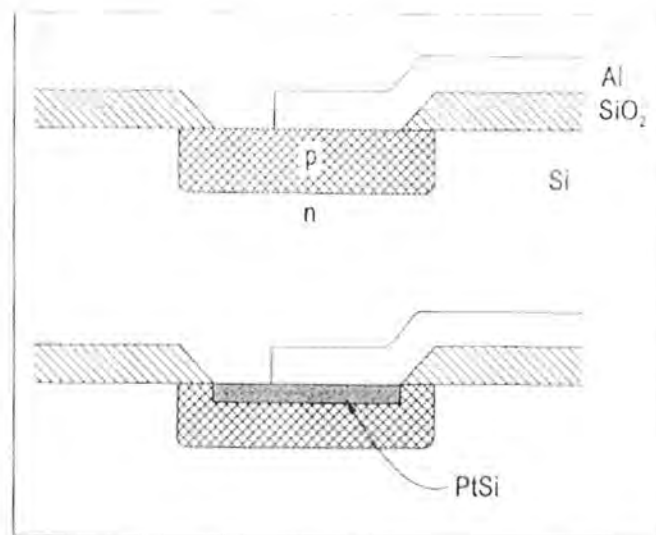


FIGURE 5. On top, a misaligned aluminum metallization causes an increase in contact resistance. This is not so in the case illustrated at the bottom, where a sufficiently thick PtSi contact reduces the formation of aluminum spikes and provides a constant contact resistance. (Taken from Ref. 13. With permission.)

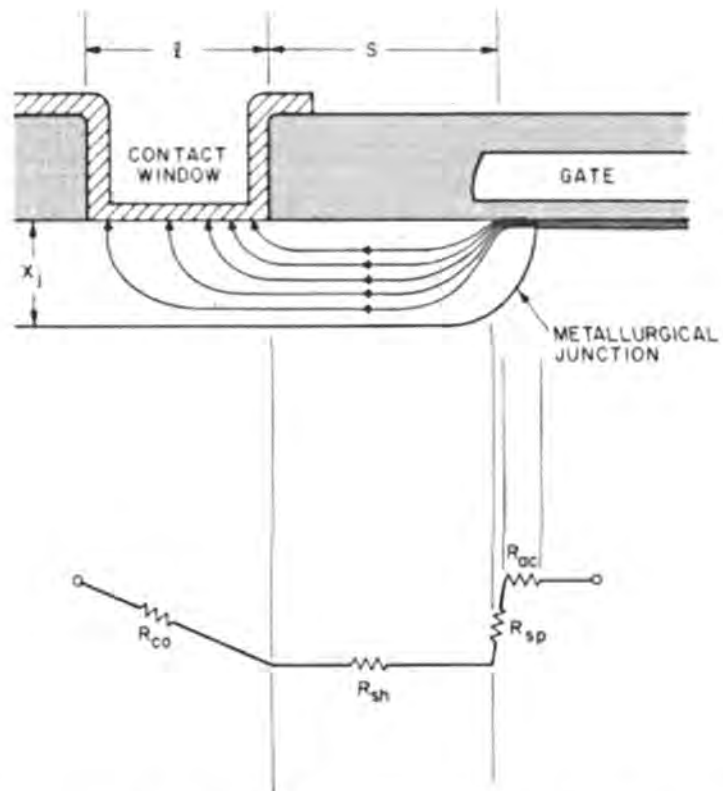


FIGURE 6. Resistance components for the series resistance from the source/drain region to the channel. (Taken from Ref. 4. With permission.)

tance in the heavily doped region of length S below the isolation between the contact window and the gate edge, R_{sh} , a spreading resistance at the junction edge, R_{sp} , and an accumulation resistance toward the channel, R_{ac} . Without a metal silicide in the source/drain regions, the value of R_{co} can be high, as described above.¹³ More seriously, the presence of the parasitic resistance R_{sh} can become a limiting problem for high-speed operations of the device. Comparing the structure in Figure 6 to that in Figure 1, one sees immediately that R_{sh} can be shunted by the silicide layer in the source/drain regions included in Figure 1. Hence, a solution was proposed to use a second silicide in the source/drain regions.²¹ In such a double silicide process, the first silicide used for the POLYCID gate is of high-temperature stable type, for example, $TiSi_2$, while the second silicide used for the source/drain should be formed at relatively low temperatures (*e.g.*, $PtSi$). As the second silicide layer can be made very close to the channel by engineering on the thickness of the two sidewall spacers of the poly-Si gate (Figure 1), the source/drain series resistance can be reduced greatly.

The POLYCID structure needs to be patterned to form the gate electrode. Patterning the silicide films to narrow lines of 500 nm width or below is, however, not trivial. When the gate length is shrunk following the scaling rule, so are the other physical dimensions, including the thickness of the gate oxide SiO_2 , in order to attain the desired device performance.²² To make device

processing controllable, the thickness of a POLYCID gate electrode, in particular, also needs to be reduced so as to make patterning of the POLYCID by dry etching able to fully stop at the underlying SiO_2 . This consideration results in a decreased height of the gate electrode. Because the chemistry for dry etching of metal silicides is generally different from that for poly-Si, dry etching in reactive plasma of such a POLYCID gate stack on top of the delicate SiO_2 of 100 Å thickness or below can cause severe reliability problems. The reduction of the POLYCID thickness also leads to an increase in resistance of the gate electrode, which can become too high to be tolerable. A further problem may arise when a patterned POLYCID gate structure is thermally oxidized for the improvement of device reliability. Successful oxidation of a large number of silicides formed on Si substrates (single crystal or polycrystalline) has been demonstrated with blanket, one-dimensional planar structures.^{23–25} The growth of a protective surface layer of SiO_2 over those silicide/Si structure, due to a sustained Si supply from the Si substrate, makes the oxidation process liable; details about the underlying physics for oxidation of the silicide/Si structure are available in the literature.^{25–28} However, for a patterned POLYCID gate structure, the side walls are also exposed to the oxidizing atmosphere (O_2 or H_2O) (see a schematic structure in Figure 7). Now, the two-dimensional oxidation of the silicide around the upper corners requires a larger Si supply than for the one-dimensional blanket struc-

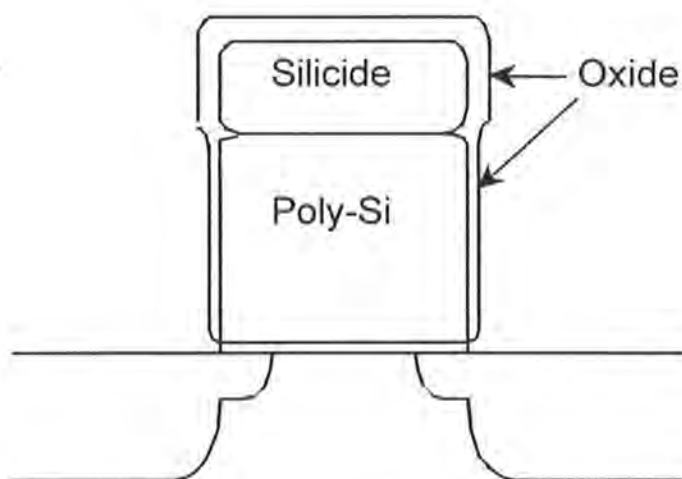


FIGURE 7. A Schematic patterned POLYCID structure under oxidation.

ture in order to grow the protective SiO_2 . The rapid oxidation at the silicide/Si interface can, however, cut off this needed supply of Si. As a result, the metal in the silicide is also oxidized leading to the "pest phenomenon" that is known for intermetallic compounds used as structural parts at high temperatures. Indeed, severe reliability problems with the formation of porous SiO_2 or mixed metal-Si oxides over the patterned POLYCIDE structure have been reported in the literature.²⁹ It is expected that the problem with oxidation of a POLYCIDE gate structure becomes even more serious for smaller gate lengths if no measure is taken.^{30,31} Thus, a more robust process technology has emerged:³²⁻³⁴ self-aligned silicide, SALICIDE, that forms the same kind of metal silicide simultaneously in the gate and source/drain regions.

A general SALICIDE process is summarized graphically in Figure 8, using the formation of TiSi_2 as an example for illustration. The two disilicides of Ti, C49 and C54 TiSi_2 , are structurally and electrically different. Their physical properties are given later when the Ti-SALICIDE process is analyzed in great detail in Section IV. It begins with a metal layer deposited over the entire surface of a wafer substrate where various structures are already defined and different materials, including Si and SiO_2 , are present. After a controlled heat treatment, that is, annealing, the deposited metal only reacts with Si in the areas where Si is in direct contact with the metal. The metal does not react, or reacts very slowly, with the surrounding dielectric materials such as SiO_2 . Selective removal of the unreacted metal on top of SiO_2 can be realized using wet chemicals. It is

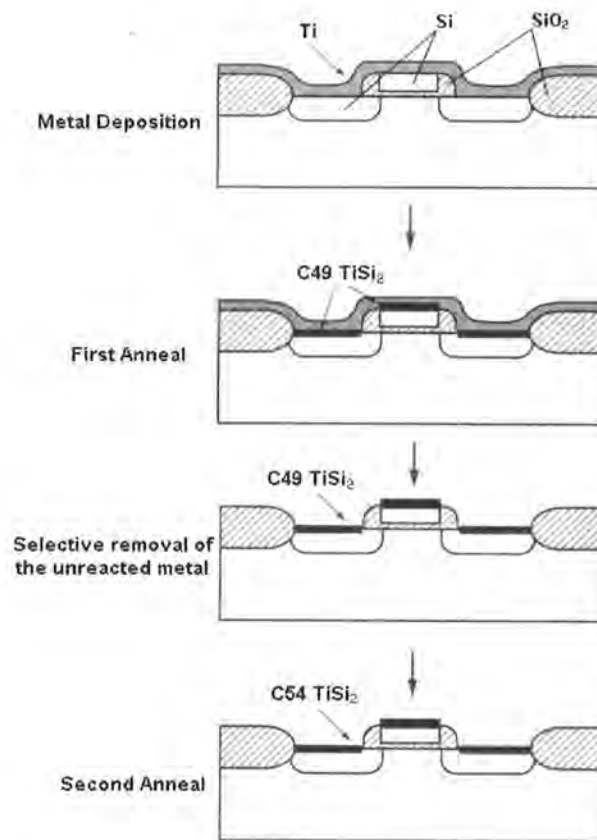


FIGURE 8. A schematic SALICIDE process exemplified with the TiSi_2 formation.

the selective reaction that forms the basis of the SALICIDE technology. As a matter of fact, selective reaction of metal with Si in comparison with SiO_2 was known long⁷ before the widespread use of the SALICIDE technology in the industry after the first demonstration by Shibata *et al.*³² in MOSFETs. The SALICIDE process has been very successful owing to its great simplicity of processing. The main players in this field have been PtSi,^{8,32,35} TiSi₂,³³ and CoSi₂.³⁵ More recently, NiSi has attracted a great deal of attention.^{36,37} The latest developments point to a converging effort to incorporate NiSi in future MOS devices. The process sequence depicted in Figure 8 is most suitable for Ti- and Co-based SALICIDE. The first annealing at a relatively low temperature is necessary to avoid formation of a silicide bridge over the SiO_2 spacers. Such a silicide bridge causes electrical shorts between the electrodes, gate and source/drain. The silicide formation over the SiO_2 spacers is a result of the predominant Si diffusion during the high-resistivity C49-TiSi₂ and CoSi formation.³⁸ The second annealing at a higher temperature is important for the formation of the low-resistivity silicide phase, C54-TiSi₂ in one case and CoSi₂ in the other. For the Pt- and Ni-based SALICIDE, the scheme in Figure 8 is considerably simplified with the second high-temperature annealing completely omitted, because both PtSi and NiSi grow via metal diffusion at low temperatures. These issues are explored in more detail later, along with other topics with the SALICIDE processing. The implementation of the SALICIDE technology has not only led to greatly simplified device processing, but has also remarkably improved the process reliability by, for instance, avoiding direct patterning the silicide/poly-Si stack. It has indeed resulted in significant advancements in the use of metal silicides in microelectronic industry. In short, the SALICIDE technology has found a very special position in present state-of-the-art electronic device technology.

The use of metal silicides has brought about two major beneficial effects for a MOSFET: as a current shunt to reduce the series resistance of the poly-Si gate electrode and as a contact to decrease the series and contact resistances in the source/drain regions. The role of silicides in electronic

devices has evolved strongly over the last decennium. Nonetheless, the time evolution of various metal silicides used in Si technology briefly reviewed above is summarized graphically in Figure 9, a reproduction from a recent publication of Iwai *et al.*³⁹ As a part of the down-scaling scheme, the device isolation technology has evolved from local oxidation of Si (LOCOS) to shallow trench isolation (STI) (see Figure 10). One concern with such isolations is mechanical stress developed during local⁴⁰ or trench isolation,⁴¹ and a more general analysis of implications of mechanical stress in Si technology is given by Hu.⁴² There are at least two additional reviews on the mechanical stresses in thin films used for microelectronics.^{43,44} As the silicide formation is generally accompanied with volume expansion,⁴⁵ it can also lead to build-up of mechanical stresses in the system. A combined effect of isolation and silicidation on device performance has recently received a very thorough treatment⁴⁶ and therefore is not discussed in this context. For the mechanical and thermal properties of various metal silicides, the readers are directed to a comprehensive summary by Östling and Zaring.⁴⁷

Metal silicides in microelectronics have been the subject of many reviews in recent years.⁴⁸⁻⁵³ The reviews by Osburn,⁴⁸ by Gambino and Colgan,⁶ and by Maex⁴⁹ all cover a broad scope of metal silicides in MOS technologies. Other reviews are more dedicated to specific topics such as technological issues with silicide films formed on poly-Si substrates for the gate electrode,⁵⁰ electrical and optical properties of silicides⁵² and crystallographic relations between silicides and Si substrates.⁵³ Recently, an international school on silicides in Erice, Sicily, June 1999, gathered leading experts to deliver more than 20 lectures on silicides that resulted in a unique volume⁵⁴ comprising extensive reviews and articles that entail balanced treatments of fundamental aspects and practical applications of various metal silicides. The intensive research on metal silicides over the years has also resulted in a comprehensive handbook,⁵⁵ updating an earlier work³⁸ by Nicolet and Lau, that recently has become available. The handbook provides a wide range of physical, chemical, electrical, optical, thermal, and mechanical properties of various metal silicides. In order to

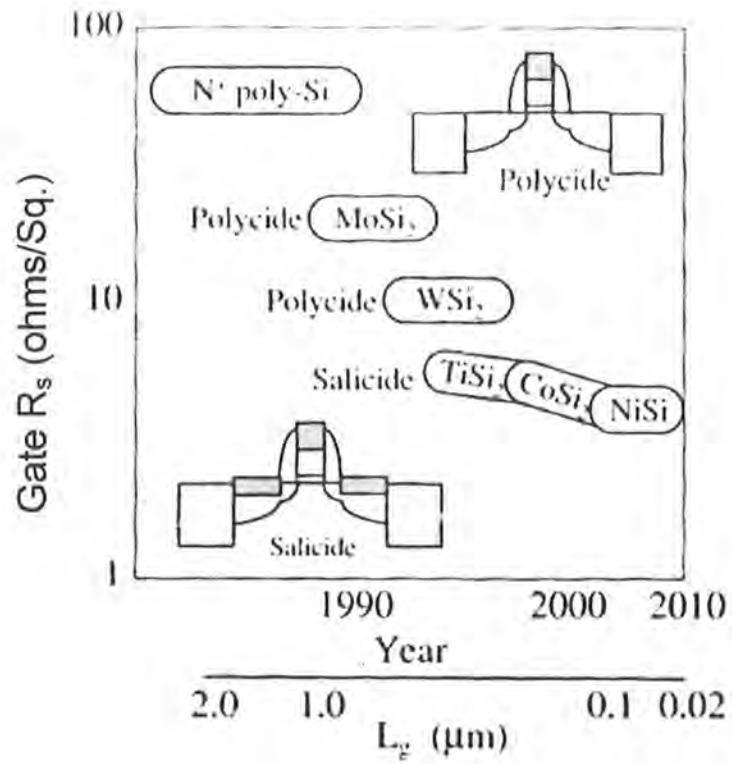


FIGURE 9. Evolution of gate sheet resistance with gate technology over time. (Taken from Ref. 39. With permission.)

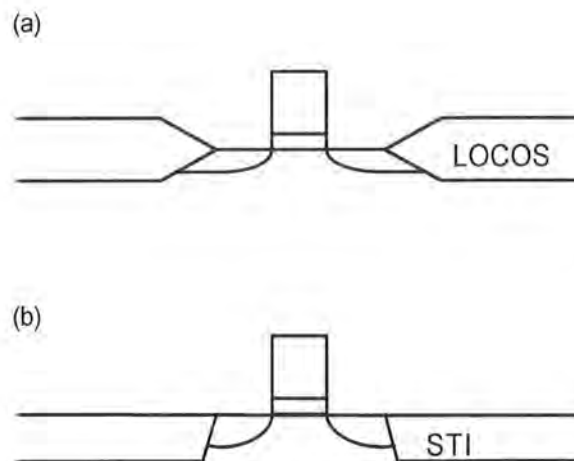


FIGURE 10. Schematic LOCOS (a) and STI (b) for modern device isolation.

cope with the rapid progress in microelectronics, the present review is intended to provide the readers with the latest developments of metal silicides in the MOS applications. Specifically, TiSi_2 , CoSi_2 , and NiSi are the focuses of the following discussions.

This review is structured as follows. First, a brief overview of the fundamental aspects directly relevant to the silicide formation is presented Section II. It presents the basic thermodynamic properties for some selected binary and ternary systems. It covers a short description of the classic nucleation theory that includes both thermodynamic and kinetic terms for growth of nuclei. The section ends with a discussion of differences between bulk and thin-film systems. These fundamental concepts are of important use for later analyses of the silicide formation in different metal-Si systems. The more technology-related aspects are treated in Section III, where different techniques used for metal/metal silicide deposition/formation are discussed, with the consideration of technological limitations and constraints. The discussion is then focused on the most frequently used SALICIDE technology with rapid thermal processing (RTP). The commonly employed physical analysis and electrical characterization methods for quantifying the silicide formation are presented briefly. Test circuits or structures for electrical evaluation of the SALICIDE processing are introduced as suggestions for potential users to consider. The focus of Section IV is placed on the most frequently used/studied silicides of today. The gradual migration from TiSi_2 to CoSi_2 and NiSi is discussed on the basis of the materials properties of the silicides as well as the circuit/system requirements from the device performance perspective. The different issues encountered with the use of a specific silicide are discussed within the framework of the fundamentals covered in Section II. Finally, in Section V future trends of metal silicides in MOS technologies are discussed. Driven by the requirements for enhanced device performance in future MOSFETs of sub-30-nm gate-length, the fundamental structure of such a MOSFET is expected to change, so are the materials used, including metal silicides. The inclusion of new materials puts great challenges on integration as well as on fundamental understanding.

II. FUNDAMENTALS

The focus of this review is placed on solid-state interactions between thin films of Ti, Co, or Ni and (bulk) Si substrates. The approach taken here, however, proceeds from general thermodynamics and kinetics for bulk materials. The differences in phase formation between thin-film and bulk cases are discussed once the fundamental basics are briefly overviewed.

Phase formation during SALICIDE processing is a thermally activated process occurring at elevated temperatures. The formation and growth of silicide phases therefore should follow the well-established laws of thermodynamics and kinetics. To begin with, the phases formed should in general be those found in the corresponding phase diagrams. The discussions below are meant to provide some general guidelines for phase formation and growth with silicides as the emphasis. For more complete treatments see two extensive reviews^{56,57} and several invited lectures⁵⁸⁻⁶⁵ by d'Heurle and co-workers.

Our attempt here is to go through those points important for the remainder of the review, rather than repeating what can be found in the literature references. Several recent books are available for a more general reading about thermodynamics and kinetics of solid-state interactions and inter-metallic compounds.⁶⁶⁻⁶⁸

A. Phase Diagram

In this section, only binary and ternary phase diagrams are presented for some typical systems. In reality, the systems in question can be much more complex simultaneously involving more than three species. For instance, during metal (species 1) interaction with a doped Si substrate (species 2 and 3), oxygen (species 4) originating from native oxide or entering the system from annealing atmosphere also participates in the reaction. Furthermore, the heat treatments for silicide formation are often deliberately conducted in a reactive atmosphere containing N_2 (species 5). It is anticipated that many key properties for such complex systems can be derived on the basis of our understanding of the binary and ternary systems.

For the binary systems there exists established, reliable sources⁶⁹ to use for their phase diagrams. There is also a large compilation of ternary phase diagrams,⁷⁰ but it is not yet complete. A difficulty in constructing phase diagrams for ternary or higher systems is the insufficient source of reliable thermochemical data for the involved, or potentially involved, intermetallic compounds, binary or ternary. Hence, it has often become necessary to carefully evaluate the thermochemical data first when examining the relative phase stability and constructing phase diagrams.⁷¹⁻⁷³ A handy example is the uncertainties in the enthalpy values for the silicides of titanium.⁷⁴⁻⁷⁶ For thermochemical data, there are additional sources besides the often-referred thick volumes in Refs. 74 to 76. One of such that is especially important for intermetallic compounds, including metal silicides, is by Deboer *et al.*⁷⁷

1. Binary Systems

The silicide phases that may form during solid-state interactions between Ti, Co, or Ni thin films

and Si substrates can be found in Figures 11 through 13 that show, respectively, the phase diagrams for the Ti-Si, Co-Si, and Ni-Si binary systems.⁶⁹ Stable phases are presented with their composition domains (*i.e.*, with finite solubility of metal or Si) varying with temperature at standard atmospheric pressure. In the Ti-Si system, the solid solubility of Si in Ti amounts to a few atomic percents above 870°C. At the temperatures typically used for silicide formation below 800°C, the solubility value is lower than 1 at. %. The solubility of Ti in Si is negligible. While Ti_3Si , Ti_5Si_4 , TiSi , and TiSi_2 have a negligibly small composition domain, that is, the so-called "line compound", the atomic composition in Ti_3Si_3 can vary up to 3 at. %. Certain similarities can be found between the Co-Si and Ni-Si systems in terms of the atomic composition (stoichiometry) of the equilibrium phases formed, although there are more phases in the Ni-Si system. When the crystallographic structures^{78,79} are compared in Table 1, Co_2Si and Ni_2Si as well as CoSi_2 and NiSi_2 share not only the same crystallographic structures but also very close lattice dimensions.

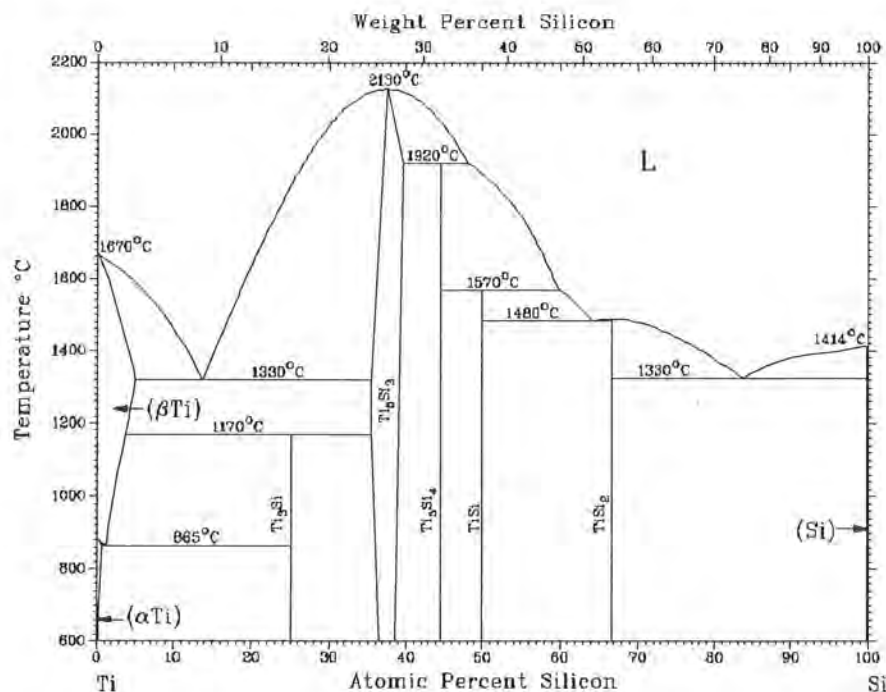


FIGURE 11. Binary phase diagram for Ti-Si. (Taken from Ref. 69. With permission.)

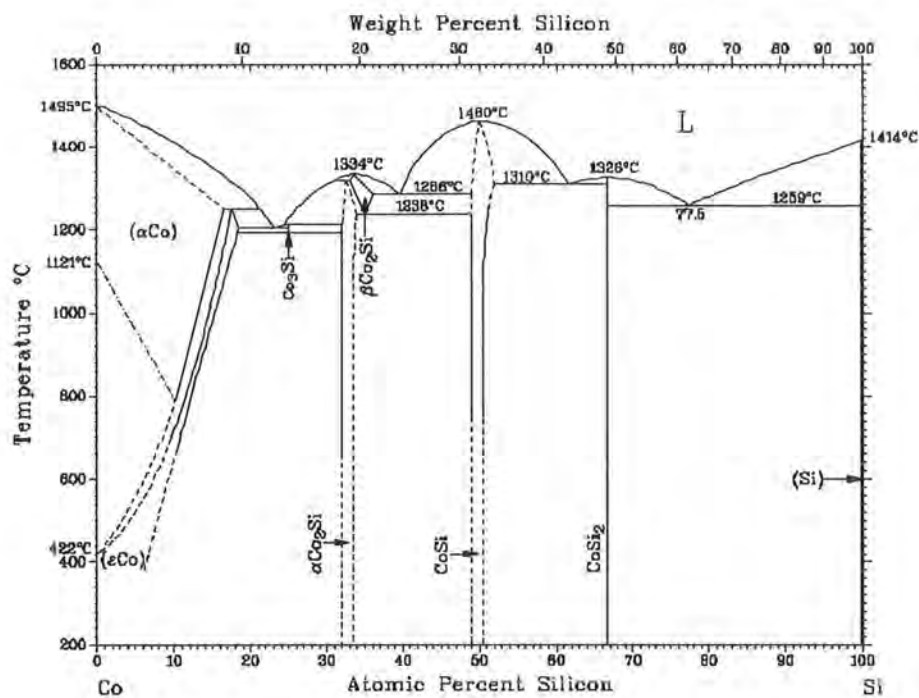


FIGURE 12. Binary phase diagram for Co-Si. (Taken from Ref. 69. With permission.)

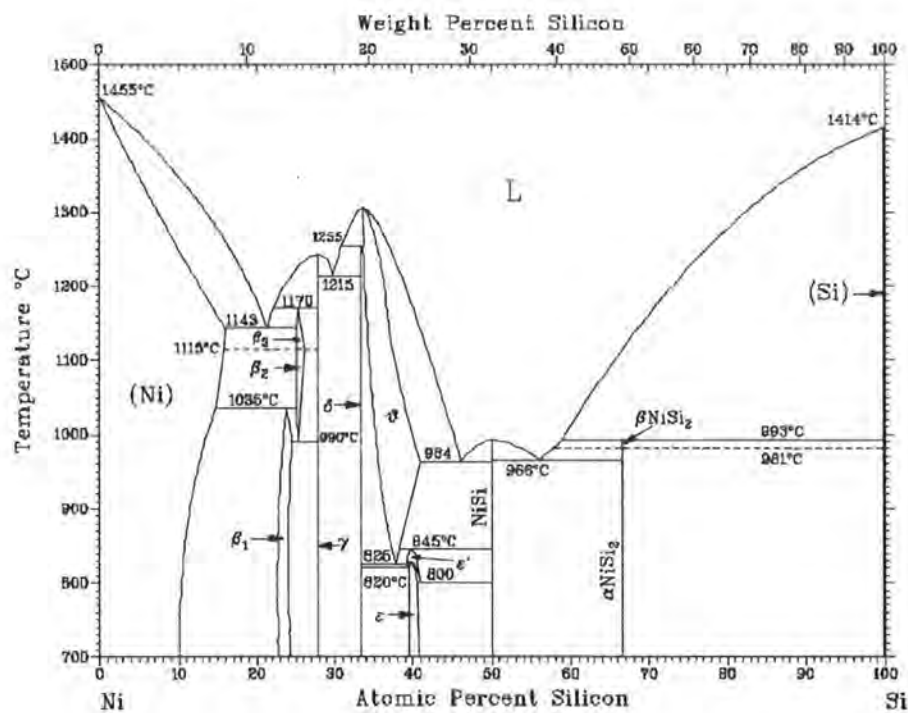


FIGURE 13. Binary phase diagram for Ni-Si. (Taken from Ref. 69. With permission.)

TABLE 1
Some Physical Properties of Ti, Co, Ni Silicides^{47,69,78,79}

Metal	Silicide phase	Crystal structure	T _m (K)	Lattice constant (Å)		
				A	b	c
Ti	Ti ₃ Si	Tetragonal	1440	10.196	-	5.097
	Ti ₅ Si ₃	Hexagonal	2400	7.429	-	5.139
	Ti ₅ Si ₄	Tetragonal	2190	6.702	-	12.174
	TiSi	Orthorhombic	1840	3.618	6.492	4.973
	C49 TiSi ₂ ^{a)}	Base-centered orthorhombic	?	3.562	13.531	3.550
	C54 TiSi ₂	Face-centered orthorhombic	1750	8.2687	8.5534	4.7983
Co	Co ₃ Si	Hexagonal	1480	4.976	-	4.069
	Co ₂ Si	Orthorhombic	1600	4.918	3.738	7.109
	CoSi	Cubic	1700	4.4443	-	-
	CoSi ₂	Cubic	1600	5.365	-	-
Ni	Ni ₃ Si	Cubic	1440	3.504	-	-
	Ni ₂ Si	Orthorhombic	1580	5.00	3.73	7.04
	NiSi	Cubic	?	4.446	-	-
	NiSi	Orthorhombic	1265	5.18	3.34	5.62
	NiSi ₂	Cubic	1298	5.406	-	-
Si	Si	Cubic	1683	5.4306	-	-

a) Dimensions for TiSi_{1.9}Cu_{0.1}, according to Ref. 80.

Also included in Table 1 are the corresponding parameters for Si for reference. Similar to Ti-Si, the solid solubility of Ni and Co in Si is negligible. The solubility of Si in the metals can, on the other hand, amount to more than 10 at. %. As one only finds the thermodynamically stable phases, that is, those with the lowest free energies at a specific atomic composition, in phase diagrams, the TiSi₂ in Figure 11 refers to the disilicide phase with the face-centered orthorhombic C54 crystallographic structure. The metastable, base-centered orthorhombic⁸⁰⁻⁸² C49 TiSi₂ is not shown here but is discussed in detail in Section IV. Similarly, the NiSi in Figure 13 refers to the phase with the orthorhombic structure.

2. Ternary Systems

When a third element is present, intentionally such as doping in Si (*i.e.*, with B, P, or As) or

unintentionally such as oxygen contaminates, one has to consider the related ternary phase diagrams in order to understand the phase formation. While such attempts for the former cases have been pursued by Maex and Probst *et al.*⁸³⁻⁸⁶ for a number of silicides, good examples for the latter cases can be found in the work of Beyers *et al.*^{87,88} for refractory metal silicides. The readers are also referred to Refs. 70, 89, and 90 for a more complete compilation of such ternary phase diagrams.

Ternary phase diagrams are often presented at constant pressure and temperature. They are shown as equilateral triangles, with each of the three corners presenting one pure element (*i.e.*, 100 at. %). Moving away from a corner for a specific element corresponds to a linear reduction of the atomic concentration of that particular element and simultaneously linear increases in atomic concentrations of the other two elements. Shown in Figures 14 and 15 are such ternary phase diagrams for Ti-Si-As and Ti-Si-B, and Co-Si-As

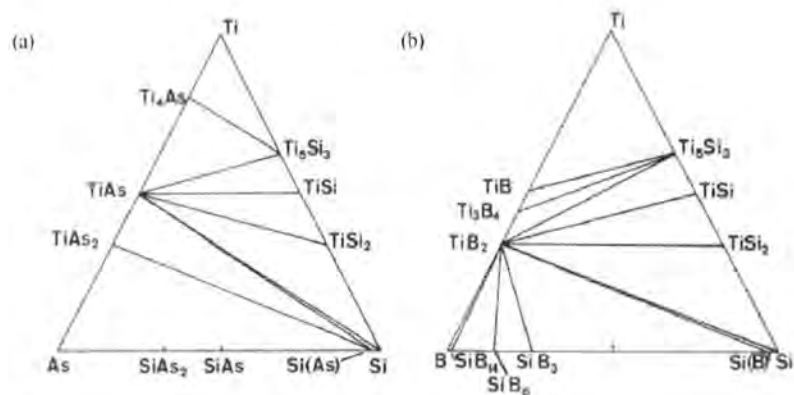


FIGURE 14. Ternary phase diagrams for (a) Ti-Si-As and (b) Ti-Si-B. (Taken from Ref. 83. With permission.)

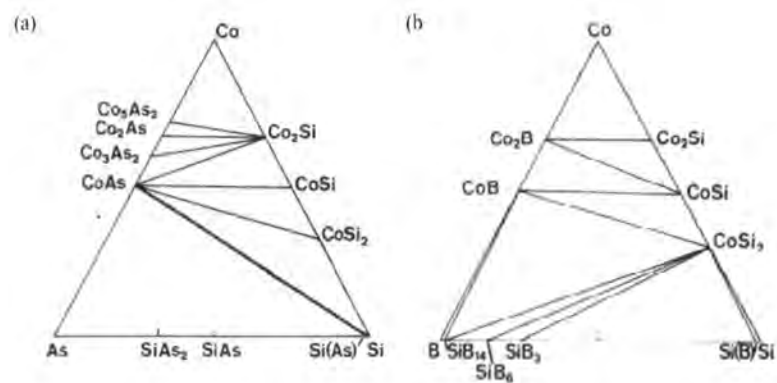


FIGURE 15. Ternary phase diagrams for (a) Co-Si-As and (b) Co-Si-B. (Taken from Ref. 83. With permission.)

and Co-Si-B, respectively.^{49,83} Similar phase diagrams for Ni are not found, but it is anticipated that they would assemble Co more than Ti, because of a closer chemical behavior of Ni to Co.

Phase diagrams can show the possibilities of dopant-metal phase formation in the presence of Si, as well as the probable consequences for the silicide/Si contacts in question. When a line is drawn connecting two phases, sometime called a "tie-line", the phases can co-exist in equilibrium. The lack of a tie-line between two phases is an indication of potential chemical interaction between them. Specifically for the Ti case, both TiAs_2 (Figure 14a) and TiB_2 (Figure 14b) are thermodynamically stable in contact with Si, indicating the possibility of formation of TiAs_2 and TiB_2 precipitates, during interaction between Ti and heavily doped Si with As or B. Such phase formation can be detrimental because they consume the dopants and Ti. Consequently, it modifies the interfacial properties of the silicide/Si as well as influences the silicide formation. The potential formation of CoAs in the presence of Si is also found (Figure 15a), while the formation of CoB is unlikely (Figure 15b).

In Figures 16 through 18, ternary phase diagrams are shown for Ti-Si-O,^{87,88} Co-Si-O,⁴⁹ and

Ni-Si-O, respectively. It should be noted that the diagram in Figure 18 for the Ni-Si-O system is an approximation with dashed lines representing the likely tie-lines. It was constructed based on the thermochemical data in Refs. 74 to 77 as well as on the great similarities in chemical behaviors between Co and Ni. It is clear in Figure 16 that Ti can readily react with SiO_2 forming Ti-oxides and silicides, which has been repeatedly confirmed experimentally⁹¹⁻⁹⁵ and presents a technological challenge for the Ti-based SALICIDE process, as discussed later. The silicides are, however, stable with SiO_2 . With Co, the situation is more complex. While the silicides are also stable with SiO_2 , there is a possibility that Co can interact with SiO_2 , forming a ternary compound Co_2SiO_4 , cf. Figure 17. Such a reaction may also introduce reliability problems when using Co-based SALICIDE process.

Dictated by Gibbs' phase rule, the phase diagrams in Figures 14 to 18 are each sectioned into many triangles in various shapes. Each triangle represents a phase domain consisting of the three stable phases present at the three corners. The amounts of the phases can be determined using the lever-rule that can be found in physical chemistry textbooks.

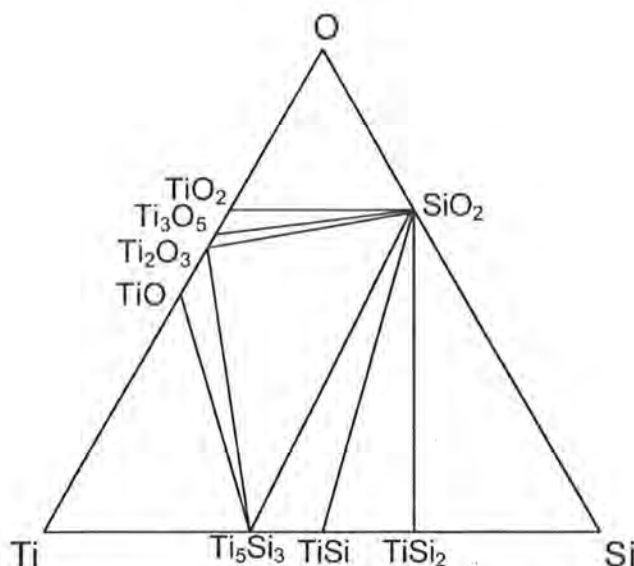


FIGURE 16. Ternary phase diagram for Ti-Si-O ($T=700-1000$ C), redrawn according to Ref. 87.

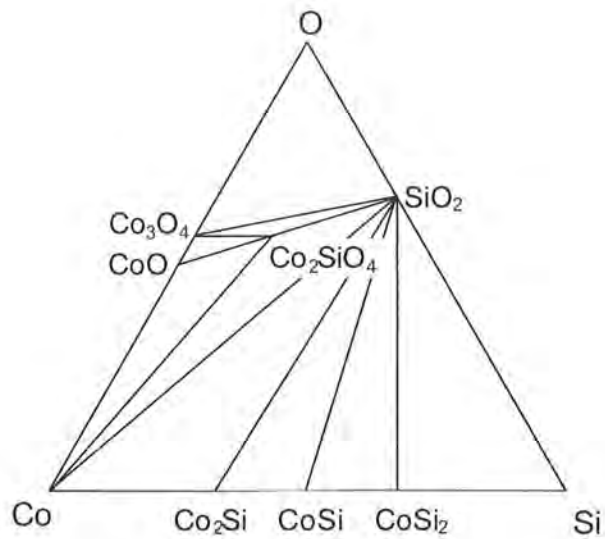


FIGURE 17. Ternary phase diagram for Co-Si-O, redrawn according to Ref. 49.

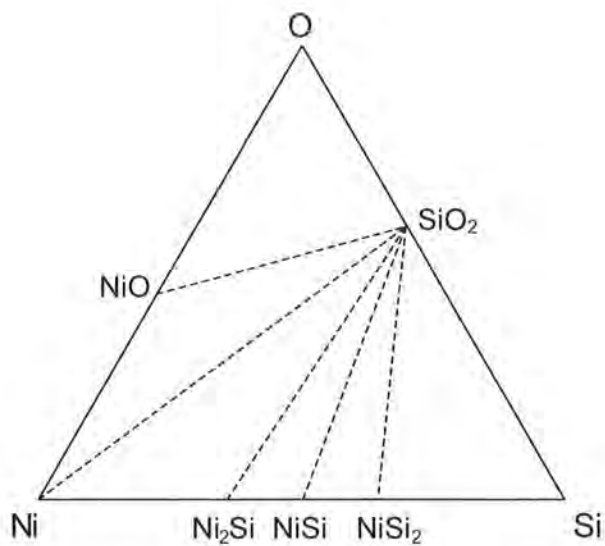


FIGURE 18. Probable ternary phase diagram for Ni-Si-O.

B. Nucleation of a New Phase

The classic nucleation theory provides a powerful means in analyzing the phase formation in silicides.⁵⁷ In nucleating a new silicide phase by solid-state interaction at the interface between two adjacent parent phases that can be metal, silicide, or Si, the Gibbs free energy gain due to the creation of a nucleus of the new phase is the driving force for the nucleation process. This process is, however, necessarily accompanied with the formation of the surface of the nucleus, which requires certain work to do and thus constitutes a hindrance force to the nucleation process. These changes are schematically shown in the two subdiagrams of Figure 19, before (left) and after (right) the nucleation of "MSi" (phase 3) between "M" (phase 1) and "Si" (phase 2). As seen, the surface of the nucleus is present in the form of inter-phase boundaries to the two parent phases. Whether the nucleus survives and grows depends on a dynamic balance of these two forces. Mathematically, what is being said can be expressed by the following energy equation describing the total free energy change, ΔG , for the nucleation:

$$\Delta G = ar^3 \Delta g_v + br^2 \Delta \sigma \quad (1)$$

where ar^3 and br^2 are, respectively, the volume and surface area of the nucleus with r being a

typical dimension (*e.g.*, radius) and a and b two geometrical constants determined by the detailed shape of the nucleus. Δg_v and $\Delta \sigma$ represent, respectively, the Gibbs free energy per unit volume of the new phase and the surface energy change per unit area associated with the creation of the nucleus. $\Delta \sigma = \sigma_{31} + \sigma_{32} - \sigma_{12}$, with σ_{12} , σ_{31} and σ_{32} denoting, referring to Figure 19, the surface energies at interfaces between parent phases 1 and 2, the newly formed phase 3 and parent phase 1, and the newly formed phase 3 and parent phase 2, respectively. The difference in surface areas corresponding to σ_{12} , σ_{31} , and σ_{32} is neglected for simplicity.

For the formation of a stable compound phase, Δg_v is always a negative quantity. $\Delta \sigma$, on the other hand, is generally a positive one. Their contributions to ΔG are different through their respective dependencies on r . In Figure 20, a schematic diagram is shown for the evolution of these two terms on the right-hand side of Eq. 1 as well as their sum, ΔG with r . A maximum in ΔG , denoted as ΔG^* , is found, which corresponds to letting the first derivative of Eq. 1 with respect to r equal to zero. Physically, ΔG^* represents the energy barrier height to overcome in order for the nucleus to grow spontaneously. This behavior is seen as ΔG decreases monotonically once r is greater than the corresponding critical dimension of the nucleus, r^* . These two critical quantities are given by:

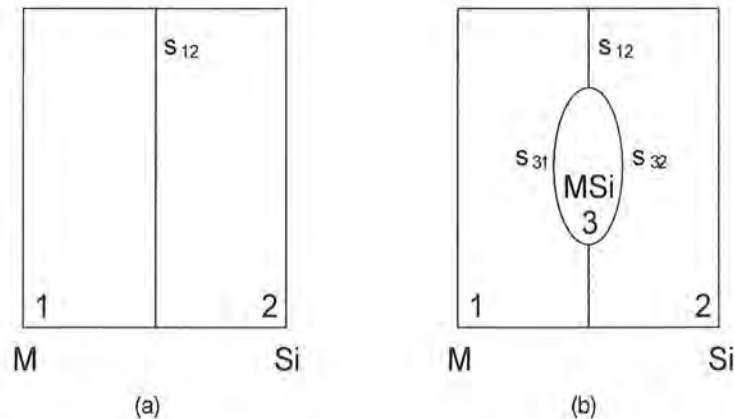


FIGURE 19. A new phase MSi, 3, forms between parent phases M, 1, and Si, 2, with the various interface energies indicated.

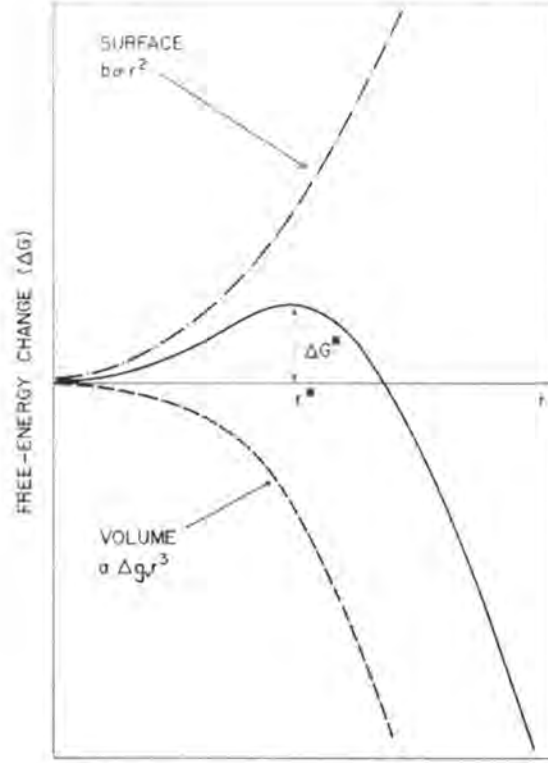


FIGURE 20. Energy curves for the nucleation of a new phase. (Taken from Ref. 57, With permission.)

$$\Delta G^* = \frac{4}{27} \frac{b^3}{a^2} \frac{\Delta \sigma^3}{\Delta g_v^2} \quad (2)$$

and

$$r^* = -\frac{2b}{3a} \frac{\Delta \sigma}{\Delta g_v} \quad (3)$$

A point to make here⁵⁷ is that surface energies, σ , do not vary significantly from one substance to the other for solid materials; they approach zero for epitaxial interfaces and amount to maximum values of 2000 ergs per centimeter square (ergs/cm²).^{96,97} Δg_v in the denominators of Eqs. 2 and 3 is the algebra sum of enthalpy change, Δh_v , and entropy change, Δs_v , for the nucleation,

$$\Delta g_v = \Delta h_v - T\Delta s_v \quad (4)$$

Since the entropy values for most solids are comparable, Δg_v for the nucleation of the first silicide phase from metal and Si can sometimes be approximated by the enthalpy change as:

$$\Delta g_v \approx \Delta h_v \quad (4a)$$

However, for cases where Δh_v itself is small, the entropy term can become dominantly important and therefore not negligible.⁹⁸

The rate of growth, GR , for the nucleus will follow an Arrhenius behavior proportional to ΔG^* and absolute temperature T in the form of:

$$GR \propto \exp\left(-\frac{\Delta G^*}{R_B T}\right) \times \exp\left(-\frac{Q}{R_B T}\right) \quad (5)$$

where R_B is the Boltzmann constant. The first exponential term on the right-hand side related to thermodynamic quantities derived above only

represents the probability of nucleation or the density of nuclei. Atomic diffusion is essential for growth. Hence, the second exponential term represents a kinetic term with Q as the activation energy for diffusion.⁵⁷

From Eq. 5, for nucleation processes whose Δg_v values are small and thus giving rise to large ΔG^* , nucleation becomes difficult and rate-limiting. This is so because very low densities of nucleation sites are found with large ΔG^* , although the diffusion could be significant with small values of Q . Since $\Delta\sigma$ is more or less temperature-independent and Δg_v is largely a linear function of temperature, ΔG^* then becomes inversely proportional to T^2 . Hence, for processes whose nucleation presents the rate-limiting step, their growth rate becomes strongly temperature sensitive,⁵⁷ that is, $GR \propto \exp(-1/T^3)$. In practice, a

critical temperature is found below which nothing seems to happen. However, above this critical temperature, the growth of a new phase becomes extremely rapid. An important consequence of the nucleation-controlled growth is the formation of a rough interface between the layer of new phase and the layers (substrates) of its parent phases due to a low starting density of nuclei.

If, on the other hand, ΔG^* is small due to a considerably large Δg_v for the phase formation, nucleation does not impose constraints on the growth and the density of nuclei becomes large. For such cases, the resulting interface is often smooth. The thickening, that is, growth of the layer of the new phase, will then be limited by atomic transportation of the reacting species across the growing layer. Such growth behaviors are termed diffusion controlled. Note that the diffusion across the growing layer in this case is characterized mostly with a different activation energy from Q in Eq. 5.

C. Formation of the First Phase — The Ordered Cu₃Au Rule

The different silicide phases shown in a phase diagram cannot simultaneously nucleate and grow. The selection and growth of a particular phase are mainly governed by kinetics, not by thermodynamics. This important finding is attributed to

d'Heurle, who has condensed it as the ordered Cu₃Au rule, see the extensive analyses in Refs. 56, 60 to 64. The ordered Cu₃Au rule applies with great success and satisfactory accuracy not only for metal silicides, but also for other intermetallic compounds. In short, the ordered Cu₃Au rule states that the first phase formed should be that rich in the most mobile species, for example, Cu₃Au when Cu is more mobile than Au. Similarly, if Au would be more mobile than Cu, the first phase to form should be CuAu₃. Again a good example is found in the Ni-Si binary system:^{56,57} Ni₂Si, not NiSi₂, forms first as a result of a higher mobility of Ni than Si during the formation of all Ni-silicides.⁹⁹⁻¹⁰³

Once a new phase nucleates and grows, the interfaces (cf. Figure 19) and therefore the energetics are altered for the next new phase. This change in interface conditions leads to changes not only in $\Delta\sigma$ but also in Δg_v . The latter change can be understood by referring to Figure 21 where the free energy variations, per atom, is shown for a system with A and B as the two parent phases and A₂B, AB, and AB₂ as the intermediate compound phases to nucleate and grow.⁵⁷ For the sake of simplicity, A and B are considered as two pure elements, and the solubility limits of A in B and B in A are assumed to be zero. In this system, it is assumed that A is the dominant diffusion species and it follows from the above discussions that A₂B will be the first phase to nucleate and grow. The driving force (energy) for the formation of A₂B is proportional to the vertical bar marked "X1" in Figure 21. Now, the next phase to nucleate would be AB at the interface between A₂B and B, with a driving force proportional to "X2" much smaller than "X3" that is related to the driving force for direct nucleation of AB from A and B.

D. Growth and Stability — Multiple Phase Growth; Thin-Film vs. Bulk

It is important to note that not all the phases listed in the phase diagrams will appear during solid-state interactions between metal thin films and Si substrates (thick). This situation is very different from that found in reactions between two "infinitely" thick (bulk) materials of metal

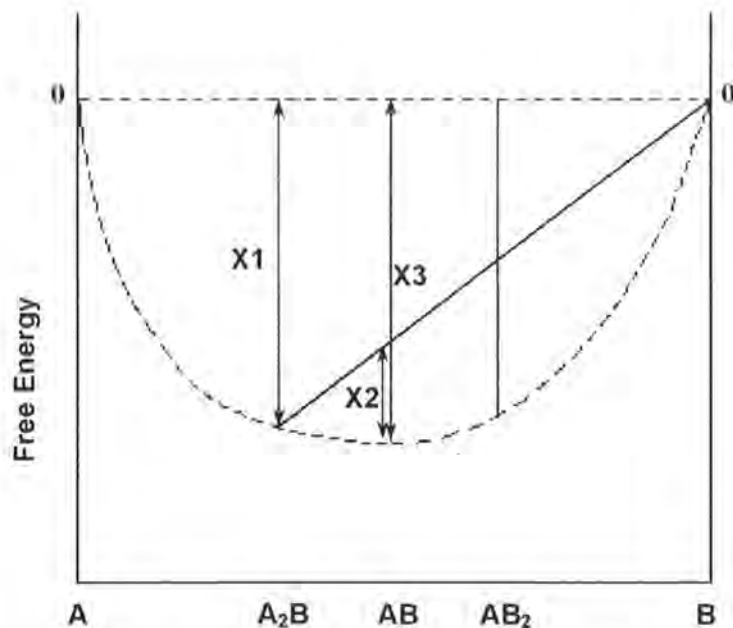


FIGURE 21. Free energy vs. atomic composition for A, A_2B , AB, AB_2 , and B.

and Si. In these latter cases with infinitely thick diffusion couples, the listed phases in phase diagrams may all form, although not always appearing simultaneously. One such example is found in the Ni-Si diffusion couples studied by Gülpén *et al.*,¹⁰⁴ who has shown co-existence of several Ni-silicide phases. In thin-film cases with films typically 1000 Å thick or below that are directly relevant to today's electronic device applications, only a few phases can appear. Further, they appear in sequence and simultaneous growth of two or more phases common in bulk cases is hardly seen.

That multiple phases cannot grow simultaneously in thin-film cases is again related to kinetics and not to thermodynamics. A mathematical treatment by Gösele and Tu¹⁰⁵ reveals that once the first phase forms and grows, the second phase will not appear until the first phase grows to a critical thickness typically on the order of several micrometers, exceeding the thickness of thin films that we are dealing with. This mathematical model was experimentally confirmed with reactive diffusion studies of the Al-Pd diffusion couple.¹⁰⁶ In this particular system, Al_3Pd was found to appear and grow simultaneously

with Al_3Pd_2 at 386°C after the Al_3Pd_2 layer reached its critical thickness of 5 to 6 μm . A slightly later analysis by Johnson and Martin¹⁰⁷ further points to the possibility of one of two simultaneously growing phases disappearing if the atomic transport necessary for the growth of that particular phase is too small. The different aspects influencing the phase formation and growth, including stress and crystallographic orientation, can be found in Refs. 57, 107, and 108. Similar mathematical analysis has also been applied to simultaneous growth of more than two phases.^{109,110}

A brief mathematical treatment is given for the growth of two layers to clarify what are summarized above for the simultaneous growth of multiple layers.¹¹⁰ For growth of more than two layers, the principles remain the same, although one has to consider more interfaces and consequently more terms in the corresponding growth equations. For this purpose, a simple sketch is shown in Figure 22 for the growth of two intermediate layers A_2B (1) and AB (2) between A and B via the diffusion of A. At the interface A_2B/AB , the diffusion of one atom of A through layer 1 of A_2B leads to the formation of one molecule of A_2B according to the reaction:

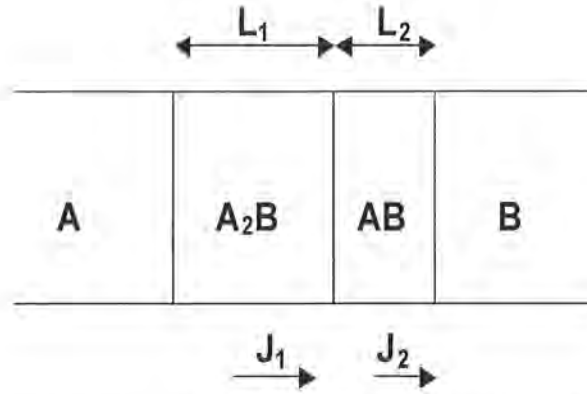


FIGURE 22. Schematic simultaneous growth of A_2B and AB between A and B . (Taken from Ref. 110. With permission.)



with a change in free energy per moving A atom of δg_1 . According to the Nernst-Einstein equation,⁵⁶ the flux of A atoms through layer 1, J_1 is given by:

$$J_1 = c_1 \times \frac{D_1}{k_B T} \times \frac{\delta g_1}{L_1} \quad (6)$$

where D_1 is the diffusion coefficient of A through A_2B and L_1 the thickness of layer 1 (Figure 22). The first term c_1 is the concentration of A atoms in A_2B , $2N_1/3$, with N_1 being the total number of atoms in A_2B per unit volume. In Eq. 6, the force term, $\delta g_1/L_1$, is the usual gradient of chemical potential $d\mu/dx$ integrated between the two extreme limits of the growing phase 1. If D_1 is constant, that is, not a function of μ (or of the concentration), it is equal to the tracer diffusion coefficient. Otherwise, it represents some average from one interface to the other. The diffusion of one atom of A through layer 2 leads to the formation of one molecule of AB at the interface A_2B/AB (through the destruction of one molecule of A_2B) and to the formation of a second molecule of AB at the interface AB/B . The overall process corresponds to the formation of AB from the reaction of A_2B with B according to:



with a free energy change, again per moving A atom, of δg_2 . The flux, J_2 now is given by:

$$J_2 = \frac{1}{2} \times N_2 \times \frac{D_2}{k_B T} \times \frac{\delta g_2}{L_2} \quad (7)$$

Here, D_2 , L_2 , and N_2 assume their corresponding meanings as their respective counterparts D_1 , L_1 , and N_1 . The factor of $1/2$ is obtained with obvious reason. Initially, the rates of growth are most likely not limited by diffusion of A through the two growing layers (D_1 and D_2) but by some form of interface reactions defined by some rate constants, which as a first-order approximation, are validated by experimental observations.¹¹¹ With the rate constants denoted as K_1 and K_2 , proportionality between the rate of layer growth and flux it gives rise to the following relations:

$$\frac{dL_1}{dt} = 2 \times \frac{\alpha}{L_1 + \frac{\alpha}{K_1}} - \frac{\Omega_1}{\Omega_2} \times \frac{\beta}{L_2 + \frac{\beta}{K_2}} \quad (8)$$

and

$$\frac{dL_2}{dt} = 2 \times \frac{\beta}{L_2 + \frac{\beta}{K_2}} - 2 \frac{\Omega_2}{\Omega_1} \times \frac{\alpha}{L_1 + \frac{\alpha}{K_1}} \quad (9)$$

as a result of competition in growth of the two layers due to Reactions (R1) and (R2). Here, the

two intermediate parameters, α and β , are defined as:

$$\alpha = D_1 \times \frac{\delta g_1}{k_B T} \quad (10)$$

and

$$\beta = D_2 \times \frac{\delta g_2}{k_B T} \quad (11)$$

In Eqs. 8 and 9, two new quantities Ω_1 and Ω_2 are introduced. They represent, respectively, the molecular volumes for A_2B and AB equal to $3/N_1$ and $2/N_2$.

If A_2B and AB are the only two phases that grow between infinitely thick A and B, Eqs. 8 and 9 define the conditions of L_1 and L_2 for which dL_1/dt and dL_2/dt would be zero or even negative, which can be schematically shown in Figure 23.¹¹⁰ With an arbitrary sample defined by point P, dL_1/dt being negative and dL_2/dt positive, the two phases would follow the trajectory described by the curved line with arrows; A_2B would first decrease in thickness until the curved line crosses the straight line numbered "2", while AB would continue to

grow. Under certain conditions in a sample with arbitrary layer thicknesses as indicated by the cross-hatched area about part "R", some phases may disappear. One important implication of Eqs. 8 and 9 is the necessary sequential growth of the phases. This point can be highlighted by setting $L_2=0$ and $dL_2/dt=0$ and then evaluating the value of L_1 , which gives:

$$L_{1c} = \frac{\Omega_2}{\Omega_1} \times \frac{\alpha}{K_2} - \frac{\alpha}{K_1} \quad (12)$$

Here, L_{1c} denotes a critical thickness of layer 1 below which phase 2 cannot grow. If K_1 is sufficiently large, L_{1c} becomes

$$L_{1c} = \frac{\Omega_2}{\Omega_1} \times \frac{\alpha}{K_2} \quad (12a)$$

A distinct difference between thin-film and "bulk" cases can now be made. For "bulk" cases, the amounts of A and B are infinite. Therefore, one could see the simultaneous growth of both phases A_2B (assumed to appear first) and AB (assumed to appear second). Although they may appear one after the other, they eventually coexist

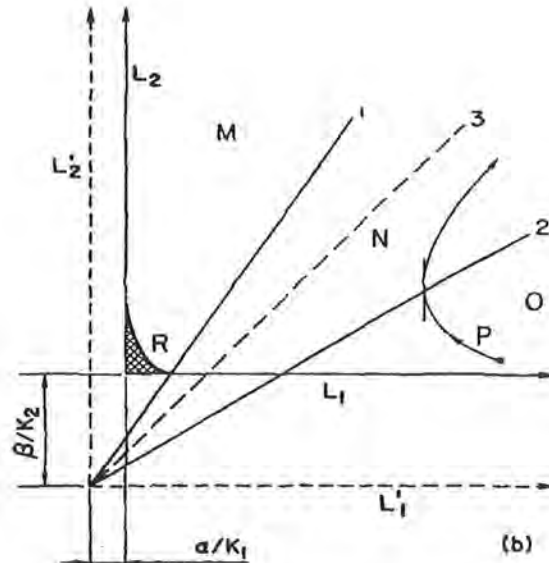


FIGURE 23. Regions for growth of phase 1 (A_2B) and phase 2 (AB) as well as simultaneous growth of them between A and B. (Taken from Ref. 110. With permission.)

with both A and B.^{104,106,112,113} For thin-film cases, however, at least one of the parent phases A and B has a very limited amount. Here, let us assume A being below 1000 Å thickness for the sake of discussion. Therefore, it is highly likely that full consumption of A occurs prior to L_1 reaching L_{1c} . It is then often observed experimentally that AB only appears when A is exhausted. Now, the growth of AB is on the consumption of A_2B , as there is no pure A left in the diffusion couple.

The values of K_1 and K_2 can mostly be seen as corresponding to the maximum possible values for J_1 and J_2 when the corresponding L_1 and L_2 tend toward zero (for instance, at the initial stage of growth). When the above considerations of interfacial reactions are simplified to assume that the growths of both layers follow a pure diffusion-controlled process, the graphical presentation of the results refers to the broken coordinate axes L'_1 and L'_2 in Figure 23. The two sets of coordinates, that is, L_1 and L_2 vs. L'_1 and L'_2 , only differ by a shift in the origin.^{107,110} Now the two solid straight lines "1" and "2" begin from the origin of the new coordinates. However, this assumption of pure diffusion-control implies infinite rates at the beginning of growth, clearly a physical impossibility.

Mathematically, the presence of K_1 and K_2 terms in Eqs. 8 and 9 yields an initial growth region where a linear time-dependent thickening of the layers is found. Therefore, it is, tempting to make an analogy to the well-known growth model for thermal oxidation of Si,¹¹⁴ where the two regions of growth as well as their kinetic parameters, *i.e.*, linear and parabolic rate constants, are well defined with clear physical meanings. It should, however, be noted that the origin of such rate-limiting interface reactions defined by constants K_1 and K_2 is often unclear for metal silicide growths.⁶² Stress has been discussed as a possible cause.^{57,107,108} A special case with a clear physical interpretation of the linear dependence of layer thickening on time, that is, linear growth, can be found for growths controlled by diffusion through an interfacial layer (membrane) of constant thickness and constant composition.⁵⁸ Such a behavior has been shown in mathematics for oxidation of a silicide layer on the Si substrate, with the linear rate-constant equal to the ratio of the diffusion

coefficient through the silicide to the silicide thickness.²⁶ For a different system of Ti-silicide formation, an initial linear growth of C54 TiSi₂ has been found experimentally¹¹⁵ when an interfacial layer of C40 (Ti,Mo)Si₂ of constant thickness and constant composition is present. The structural properties of C40 (Ti,Mo)Si₂ are described in detail when discussing the importance of Mo in the formation of TiSi₂ in Section IV.

For the reason of an unspecified physical origin for the so-called interfacial-reaction controlled growths, the discussions only focus on two distinct growth behaviors: nucleation-controlled and diffusion-controlled growth processes.^{56,57} A short summary of these two growth kinetics is repeated here for thin-film cases. For the former of a nucleation-controlled growth, there exists a critical temperature below which practically nothing happens. Above this temperature, the growth of a new phase is explosive and its growth kinetics are difficult to determine. The resulting interface is often rough. For the latter of a diffusion-controlled growth, one phase grows at a time following the well-defined diffusion kinetics with an activation energy characteristic of atomic transport through the growing phase mostly along the grain boundaries (see below). When the thickness-square of the growing phase is plotted against time, a linear relationship is found. In addition, the resultant interface is smooth.

Now returning to the comparison between "bulk" and thin-film cases, the dominant diffusion mechanisms are generally different as well.^{56,58,59,103,116,117} In "bulk" samples, lattice diffusion is often the major path. In thin-film samples, grain boundary diffusion governs. A comparison is shown by Barge *et al.* for the two different types of diffusion behaviors in Co-silicides formed from both "bulk" and thin-film samples.¹¹⁶ In Ref. 117, as well as in Ref. 103, a comprehensive summary is presented to compare these two cases in a large number of silicides. A rule of thumb is that the activation energy for the grain boundary diffusion is about 0.7 to 0.8 times that for the lattice diffusion.^{103,117} In general, the latter, the activation energy for lattice diffusion, in turn scales with the melting point of the silicide.¹⁰³ Consequently, the diffusion, and then growth, in thin films occurs more rapidly than that in their "bulk" counterparts at low temperatures.

E. Growth of the Second Phase in Thin-film Cases — Further Analysis

In the above analysis according to Eqs. 8 and 9, it is made clear that the second phase AB will not appear until the first phase A_2B grows beyond its critical thickness L_{lc} defined by Eq. (12). This phenomenon, confirmed experimentally,^{106,112,113} can be explained with an interfacial reaction barrier to AB,¹⁰⁵ (Such a barrier is also responsible for the absence of phases predicted by the equilibrium phase diagrams for thin-film cases.) On the other hand, experimental results with thin films indicate that AB immediately nucleates and grows once A is exhausted; here A is the thin film (say, below 1000 Å), and B the substrate as assumed earlier. Here, “immediately” refers to the time scale on the order of seconds that is beyond the experimentally resolvable limit during typical silicidation studies. The immediate nucleation of AB under such conditions is, however, difficult to predict from a kinetic point of view based on Eqs. 8 and 9. Let us examine the schematic diagrams for the growth of A_2B between A and B in Figure 24 and the corresponding free energies in Figure 25. (Although concentrations and concentration gradients are used in Figure 24, one should remember that the more rigorous presentation should be based on free energies and free energy changes as in Ref. 62, simply because they are the true driving forces for the diffusion and growth.)

When A_2B grows between A and B via the diffusion and on the expenses of A, the concentration gradient of A in A_2B is represented by the solid straight line in Figure 24 with two end concentration values C_{A0} and C_{A1} at the two interfaces toward A and B, respectively. When the solubility limits are assumed to be zero for simplicity as indicated in Figure 25, C_{A0} is simply equal to the equilibrium value of A in A_2B in contact with A, i.e., $C_{A0} = C_{A0}^e$. At the other interface, it is necessary that C_{A1} be greater than the equilibrium value of A in A_2B in contact with B, C_{A1}^e , in order for the growth to proceed. These various values of C_{A0} , C_{A1} , C_{A0}^e , and C_{A1}^e are shown in Figure 25. Mentioned earlier was that the driving force for the growth of A_2B is proportional to the vertical bar of length “X1”. For thin A_2B , C_{A1} is close to C_{A0} and far above C_{A1}^e . The tangent passing the

energy curve of A_2B at C_{A1} would give a negative driving force for the formation of AB, since its energy at the composition AB would be below (i.e., more negative) the minimum of the energy curve of AB, as indicated by “X2” in Figure 25. This “X2” corresponds in some manner to a positive value of ΔG , to be entered in Eq. 1. Thus, the possibility of nucleating AB is ruled out. When A_2B thickens, the growth necessarily slows down as a result of reduced diffusion through the growing A_2B . This process is accompanied with a decreasing value of C_{A1} approaching C_{A1}^e , as indicated by the vertical arrow in the top diagram of Figure 24. This behavior can also be seen by moving C_{A1} towards C_{A1}^e , as indicated by the horizontal arrow at the top in Figure 25. If A is rather abundant as in “bulk” cases, C_{A1} will continue to approach C_{A1}^e (upper diagram of the left column in Figure 24). Now the tangent passing the energy curve of A_2B at C_{A1} can yield a positive driving force for the nucleation of AB, proportional to “X3” in Figure 25. At this point, simultaneous growth of A_2B and AB becomes possible (lower diagram of the left column in Figure 24).

The discussion in the preceding paragraph provides a complementary interpretation, from the thermodynamic viewpoint, for the delayed nucleation of AB in “bulk” samples. If, however, A is very limited as in thin-film samples and is completely depleted far before C_{A1} reaches a value allowing the nucleation of AB, that is, “X2” still remains, equivalent to L_l being smaller than L_{lc} as discussed earlier, the situation is altered. Once A is exhausted, the equilibrium concentration of A throughout A_2B rapidly approaches C_{A1}^e as a result of B diffusing into A_2B (upper diagram of the right column in Figure 24). Now, A_2B is in equilibrium with B. Under this condition, the tangent passing the energy curve of A_2B at C_{A1}^e clearly yields a positive driving force for the nucleation of AB, proportional to the vertical bar “X4” in Figure 25. Now AB can nucleate and grow if the surface energy term, $\Delta\sigma$, also allows.⁵⁷

The analysis above naturally also applies for the nucleation and growth of the next phase in sequence, AB_2 , at the interface AB/B. Now the parent phases are A_2B and B when AB is grow-

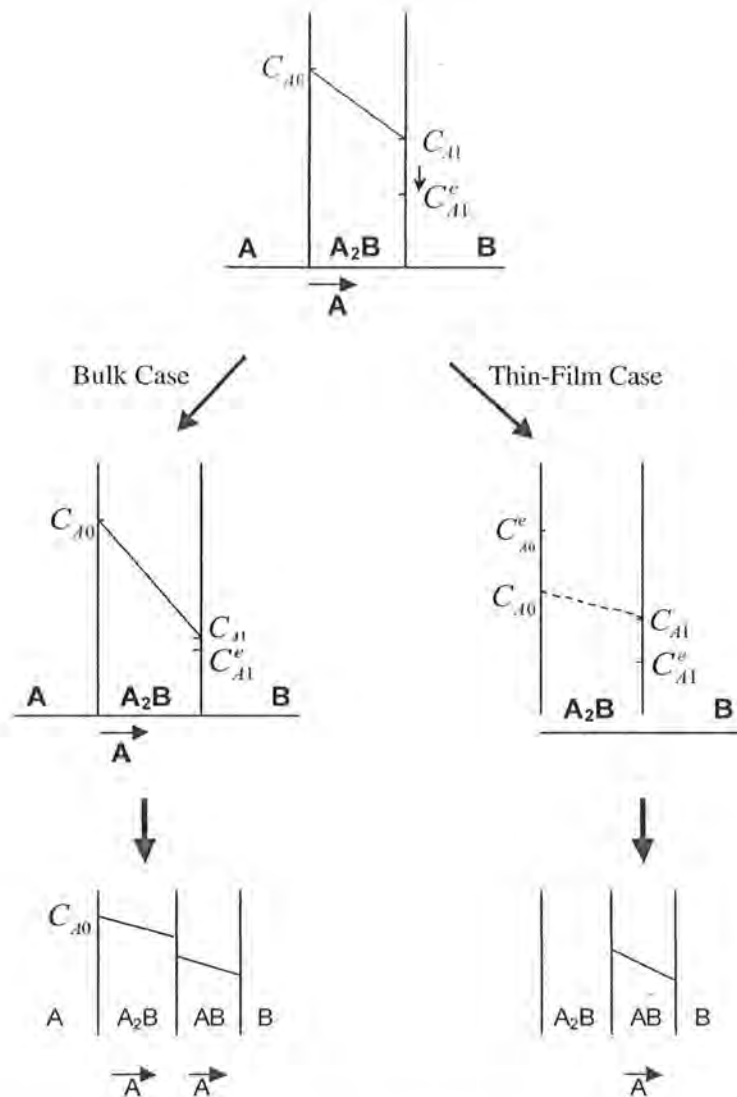


FIGURE 24. Growth of A_2B and AB between A and B , with concentration values indicated, for bulk and thin-film cases.

ing, AB_2 cannot nucleate and grow until A_2B is completely consumed.

F. Dominant Diffusion Species — Marker Experiments

To study atomic transport mechanisms as well as to identify the dominant diffusion species (DDS)

for the growth of a specific silicide phase, marker experiments are often employed. Four different groups of marker experiments have been used in the literature. They are (1) ion implantation of noble gas atoms, such as Xe ,^{101,118-120} (2) deposition or implantation of small islands of refractory metals, such as tungsten,¹²⁰⁻¹²² (3) deposition of pairs of metals with properties so similar that they act almost like true isotopes, typically of the type

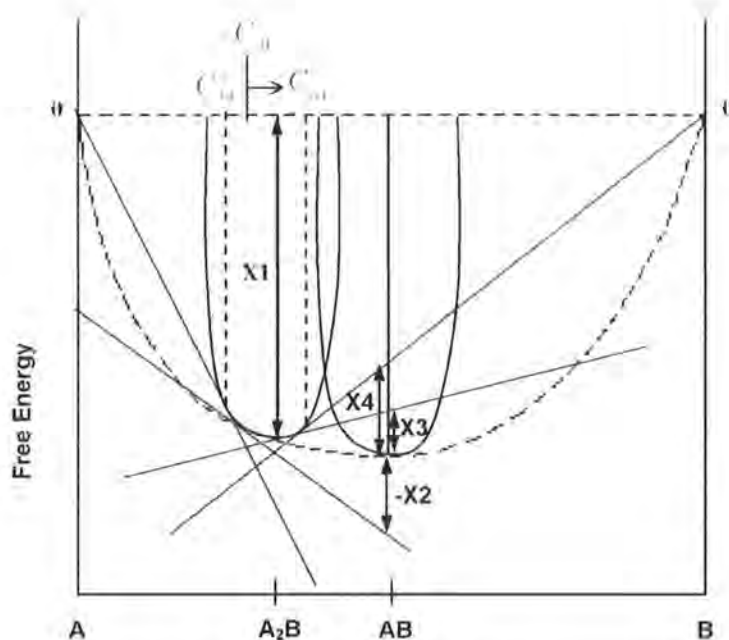


FIGURE 25. Free energy vs. atomic composition for A, A₂B, AB, and B, with the same concentration values as shown in Figure 24, and driving forces indicated (X1, X2, X3, X4).

of Mo and W^{123–125} or of Si and Ge,¹²⁶ and (4) use of some tracer isotope,^{127–129} often radioactive, for example, ³¹Si with a lifetime of 2.62 h.^{128–133} For details of the four commonly used marker experiments see discussions and summaries in Refs. 38 and 56.

Special comments are given here to the use of ³¹Si or other types of radioactive tracer. This method provides the best information when the tracer belongs to the least mobile species.^{56,135} Then, the degree of mixing (of normal Si and ³¹Si or of metal and its isotope) during reaction indicates that the reaction proceeds by motion of the other species in the diffusion couple (*e.g.*, metal when reacting with ³¹Si/Si bilayers). Further heating after reaction causing mixing provides precise information about the mobility of the least mobile species. Unfortunately, this method generally has been used with the tracer belonging to the most mobile species. Then, its usefulness becomes very limited. At low temperatures, it can show if a reaction occurs by grain boundary diffusion; confirmed aspects of such observations are few, if any. The first systematic mathematical analysis

of such experiments is provided in Ref. 135, showing that the results cannot provide any information about vacancy or interstitial diffusion processes (except in the very unusual case of ¹⁸O used to investigate¹³⁶ the formation of SiO₂).

G. Morphological Instability

The morphological stability of silicide thin films on Si substrates is a main concern for device performance and reliability. Numerous studies can be found in the literature regarding the evolution of morphology for silicide thin films on single-crystal and/or polycrystalline Si, and only a few references are mentioned here for TiSi₂,^{137–145} CoSi₂,^{145–152} and NiSi.^{139,145,151,153} In general, thin silicide films exhibit a much better morphological stability on single-crystal substrates than on polycrystalline ones. Nygren and d'Heurle^{150,151} have identified two distinctly different mechanisms that are behind the instability of thin films on the single-crystal and polycrystalline substrates. Both mechanisms are governed by the same physical

origin — minimization of the total energy of the system in question, as expected. On single-crystal substrates, two parallel processes drive the morphological change and cause the agglomeration of the silicide films: reduction of the density of grain boundary interfaces in the silicide films and elimination of the high-energy interface(s) between the silicide and Si. Grooving at grain boundaries and even coarsening of silicide grains can then be observed. An equilibrium model schematically shown in Figure 26 was proposed by Nolan *et al.*¹⁴² to account for the evolution of the morphology for a silicide thin film. The initial film is composed of equal-sized silicide grains with flat interface and surface (a). Grain grooving along with grain growth occurs uniformly to all grains (b) and (c). When the grains grow beyond a critical size of L_c (d), the initially continuous film would break into discrete grains of much greater size than the original. Greatly improved morphological stability of CoSi_2 thin films thus is achieved when such grain boundary interfaces in the silicide films are removed in epitaxial CoSi_2 .^{154,155}

On polycrystalline substrates, it is mainly the grain growth in the underlying poly-Si that induces the morphological change and leads to the disintegration of the silicide films. The grain

growth, driven by a reduction of the density of grain boundary interfaces in the poly-Si, is enhanced by the presence of metals, here silicides.^{139,150,151} The temperature for grain growth in poly-Si (*i.e.*, degradation temperature) is found by Zheng *et al.*¹³⁹ to scale with the melting temperature of the top silicide, with an approximate relation as $T_{\text{grain-growth}}^{\text{poly-Si}} = 0.6 \times T_{\text{melting}}^{\text{silicide}}$. Although the degradation temperature might also be represented as to scale with the formation temperature of silicides, a much better correlation is found by Hong *et al.*¹⁴⁵ based on a study on Ni-, Pd-, Pt-, Co-, Ti-, and Cr-silicides: it is related to the plastic deformation temperature of silicides by $T_{\text{grain-growth}}^{\text{poly-Si}} = T_{\text{deformation}}^{\text{silicide}} + 100$.

When the metal atoms are more mobile during the silicide formation, as in the case for the formation of Ni-silicides, the agglomeration of the silicide films would sequentially undergo coarsening, inversion, and mixing, as depicted schematically with the left-column diagrams in Figure 27 from Gambino and Colgan.⁶ When instead the Si atoms are more mobile, as for the formation of Ti-silicides, the agglomeration of the silicide films would follow a different path of roughening, deformation, and mixing, see the right-column diagrams in Figure 27.

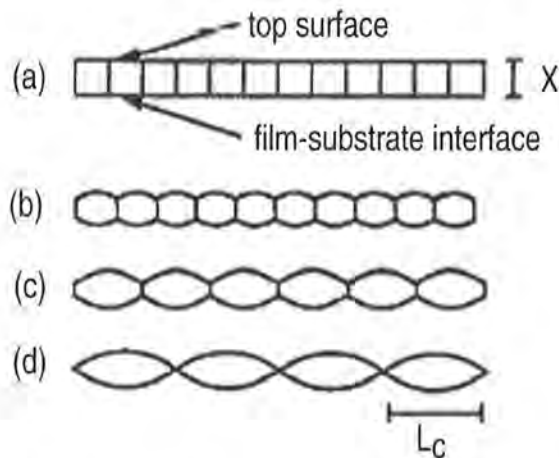


FIGURE 26. Morphological evolution of a silicide film on single-crystal Si, with X indicating the thickness of the silicide and L_c as the critical silicide grain size prior to agglomeration. (Taken from Ref. 142. With permission.)

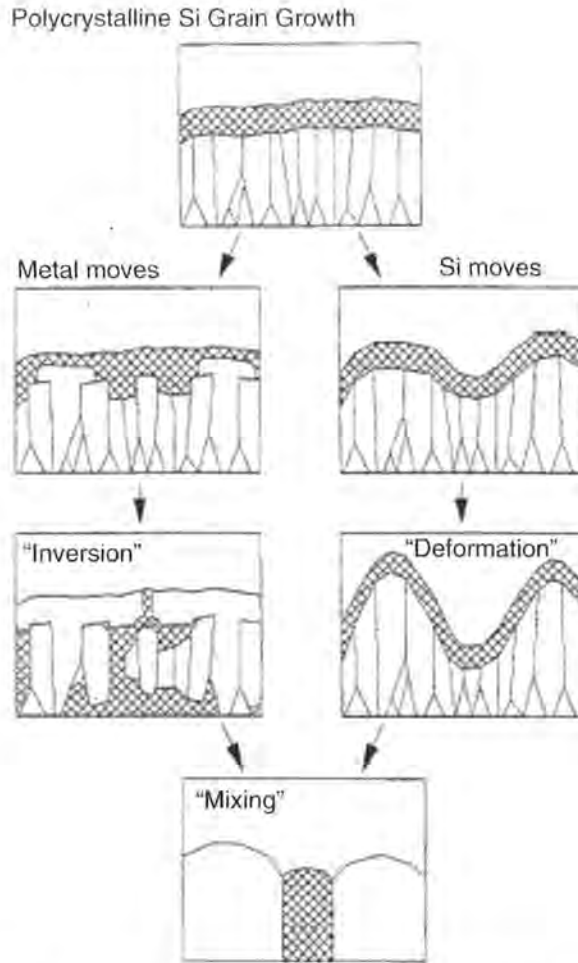


FIGURE 27. Morphological evolution of a silicide film on polycrystalline Si for two cases with different dominant diffusing species (left: metal, right: Si). (Taken from Ref. 6. With permission.)

Calculations of the balance of surface and interface energies indicate^{142,156} that thin films on single-crystal substrates could be more resistant to agglomeration if they are thicker, of finer grains, or with higher surface and interface energies. The fact is¹⁵⁷ that the equilibrium models derived in Refs. 142 and 156 actually provide kinetic predictions, while minimization of the total energy that requires the opposite, that is low surface and interface energies or large grains, is a thermodynamic forecast.

III. FORMATION AND CHARACTERIZATION

In this section, the focus is first directed to the most frequently employed deposition and forma-

tion techniques, that is, sputter deposition and rapid thermal processing (RTP) for the SALICIDE process, as shown in Figure 8. Oxygen contamination is especially addressed because the silicide formation is affected. An overview is then given to other techniques than SALICIDE used for the formation of silicides. Physical analyses and electrical characterizations utilized for quantification of the silicide formation process are presented at the end.

A. SALICIDE Processing

The SALICIDE technology has become an industry standard, where the metal silicide is

formed by solid-state reacting a metal film with the Si substrate in a self-aligned manner. (Co-deposition of Si and metal that is often used for POLYCIDe processes is, however, not suitable for the SALICIDE technology due to formation of silicide films over the isolation and thus shortage between the electrode terminals.) The metal film can be deposited by a variety of techniques. Most commonly used is sputter-deposition from an appropriate (solid) target. Electron-beam evaporation is another physical vapor deposition (PVD) technique that is often used for metal deposition. However, evaporation is useful mainly for fundamental investigations of metal-Si interactions but less common in production lines, because of its low throughput, poor topological conformality of deposition, and high price when compared with sputter-deposition. The usual SALICIDE process relying on sputter-deposition of metal films followed by annealing is discussed in the following. As described earlier, it can require two separate annealing steps for a complete SALICIDE process, cf. Figure 8. It will be made obvious below that the temperature control during the annealing steps is of critical importance for the success of the SALICIDE processing; poor control of wafer temperature can lead to formation of undesired silicide phases and/or electrical shorts between the gate and source/drain regions over the SiO_2 spacers. Also covered in this section are impurity control and selective etching. The selective removal of unreacted metal films on the SiO_2 isola-

tion, against the silicide formed in the Si areas, using wet chemistry is an important component of the SALICIDE technology.

1. Furnace Annealing vs. RTP

The annealing is today most often carried out in a single-wafer, rapid thermal processing (RTP) chamber. In an RTP chamber, see Figure 28 for the schematic cross section for the interior of a most common RTP unit, a Si wafer is placed in the middle of the chamber surrounded by quartz walls. The wafer is horizontally seated on three tiny quartz pins sticking up from a quartz wafer susceptor to minimize the physical contact between the wafer and the susceptor in order to achieve a uniform heat (energy) distribution when the wafer is being heated up. Two lamp banks each with a set of linear lamps, one above and one below the wafer, are utilized for wafer heating. To improve the heating efficiency, reflectors are placed outside the quartz chamber. Quartz parts are used in order to minimize the total mass for heating, because quartz poorly absorbs radiated energies coming from the lamps. Hence, rapid heating and cooling can be realized. The wafer temperature is read contactless with a pyrometer situated beneath the wafer. By comparing the setpoint temperature and the pyrometer readout, the electrical power to the heating lamps is regulated to yield the desired wafer temperature. Be-

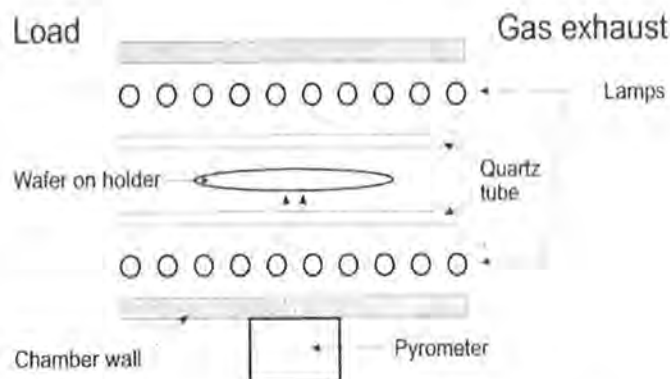


FIGURE 28. Schematic cross-section of a RTP chamber used for silicide formation.

cause the pyrometer readout depends strongly on the emissivity of the wafer surface, it is common practice to etch off all surface layers from the wafer back in order to expose the Si surface to the pyrometer for more accurate and/or reproducible temperature measurement and control.

For wafer temperature control in an RTP chamber, it is crucial to analyze wafer-heating mechanisms as well as to identify factors that affect the heating process. There are at least three devoted literature issues or volumes that deal specifically with the issues of wafer heating using radiating sources.¹⁵⁸⁻¹⁶⁰ Modeling of wafer temperature variations can be found in many specialized papers included in these volumes. Lord¹⁶¹ takes into consideration thermal radiation, conduction, and convection. It gives a complete account of temperature uniformity over a wafer during the heating and cooling processes, with and without a heat-compensation ring around the substrate wafer. It further calculates the developments, as well as the consequences, of thermal momentum across a substrate wafer as a result of temperature nonuniformity. As an example, severe dislocations and even slip lines can form in a substrate wafer as a result of the large thermal momentum build-up during the heating-up cycle. Accurate modeling and precise control of the wafer temperature are in general challenging tasks¹⁶² because of the fact that the emissivity of Si is not only wavelength and temperature dependent,^{163,164} but also sensitive to surface roughness¹⁶² and doping concentration.^{165,166} For substrate wafers with patterned structures on the front surface, the presence of different layers and different materials inherently yields local differences in emissivity. Temperature nonuniformity across the wafer can then build up due to the local differences in heat absorption as well as finite thermal conduction within the substrate.¹⁶⁷ All these issues leave us with a very demanding proposition regarding the modeling and control of wafer temperature in an RTP chamber. For instance, the optimal machine parameters (*e.g.*, power distribution and algorithm) for uniform wafer temperature at the setpoint temperature may not be the optimal ones during the ramping-up process.¹⁶¹

Despite all these difficulties in wafer temperature control, RTP offers a superior means for

silicide formation when compared with the traditional furnace annealing.⁴⁸ Practically, only the wafer substrate itself constitutes the entire mass and allows rapid temperature rising and falling. Consequently, a much better control of annealing temperature, annealing time, and temperature ramping (up and down) is realized using RTP. Because the chamber is relatively small, a good control of impurities is also realistic with RTP. Because it also offers other features that are desirable for processing CMOS devices of deep sub-micron dimensions,¹⁶⁸ such as a much reduced dopant diffusion and redistribution at a given activation efficiency of dopants, RTP has become an industrial standard for a number of important processing steps.

2. Oxygen Contamination

Unless elaborated means such as ultrahigh vacuum and *in situ* surface cleaning are employed, oxygen contamination is a fact. The presence of native oxide on the surface of a Si substrate can lead to failure of silicide formation. A detailed analysis of how the presence of interfacial oxygen reduces the TiSi_2 formed can be found in Ref. 169. A discontinuous layer of TiSi_2 is formed on the poly-Si gate when excessive interfacial oxygen is present, as revealed by a transmission electron microscopy (TEM) study.⁷

During sputter-deposition of metals, impurities such as O and Ar can be incorporated in the metal films. Other impurity sources could be C and N. During the transportation of wafers from the metal deposition chamber to the annealing chamber, air exposure can also lead to incorporation of O in the metal, especially Ti, films. Wafer wet-cleaning prior to metal deposition can be critical as well. Because O, N, and C may participate in or interfere with the silicide formation process, it is highly desirable to reduce their amounts in order to achieve a controllable silicide formation. The great importance of controlling the oxygen contaminates for successful silicide formation is illustrated in Refs. 170 and 171.

Maex *et al.*¹⁷⁰ show that water molecules, H_2O , dissolved in the surrounding SiO_2 isolation can be released during the temperature ramping-

up period of RTP at about 200 to 400°C. In Figure 29,¹⁷⁰ the H₂O concentration (in ppm diluted in large flows of N₂ - 10 liters per minute, slm) is shown to increase rapidly around 200°C when heating up the substrate wafers with TEOS-oxide or Co-covered TEOS-oxide deposited on the wafer surface. When a Ti layer is also added on top of the Co/TEOS, the H₂O concentration is greatly reduced. The H₂O released diffuse toward the reaction interface between the Co film and the Si substrate. As a result, the formed CoSi₂ is very nonuniform in thickness; it is substantially thinner along the boundary between the active Si area and the SiO₂ isolation than in the active area further away from the boundary (cf. Figure 30a). The solubility of O in Co is practically negligible.⁶⁹ In the presence of Si, SiO₂ should preferably form by H₂O-oxidation according to Figure 17, thus presumably leaving Co in contact with a partially oxidized Si surface. Hence, the Co-Si interaction is much more disturbed along the boundary between the active Si area and the SiO₂ isolation than in the active area away from the boundary. By adding a Ti cap layer on top of the Co film, a uniform CoSi₂ layer is formed as shown in Figure 30b. Oxygen-gettering by the Ti apparently helps suppress the influence of H₂O on the Co-Si reaction.

The oxygen can influence the formation of Ti-silicides in a different way. Interfacial oxygen present

at the interface between Ti and Si can in principle be dissolved by Ti according to Figure 16. However, the ability of Ti oxygen-gettering can readily lead to a high concentration of oxygen in Ti films, if not carefully controlled. Titanium can dissolve up to 32 at. % oxygen.⁶⁹ Thus, in a sample with a 10-nm-thick sputter-deposited Ti film, oxygen concentration up to 33 at. % was found in the film after air exposure.¹⁷¹ An *in situ* transmission electron microscopy (TEM) study in ultra-high vacuum by Ross¹⁷¹ of such a sample shows that the phase transformation in TiSi₂ from the C49 to the C54 structure (see also Section IV about this transformation) is not smooth in the sample. The reaction front moves in a jerky manner; it "moves slowly at first, then suddenly covers a large area almost instantaneously", as described by Ross. In a control sample with the Ti film deposited in ultra-high vacuum without air exposure, the movement of the reaction front is smooth. The formation of C54 TiSi₂ also occurs at a lower temperature.

3. Etching and Cleaning

As an integral part of the SALICIDE technology, selective removal of metal with respect to silicide after the first annealing (Figure 8) is crucial and deserves separate treatment. The

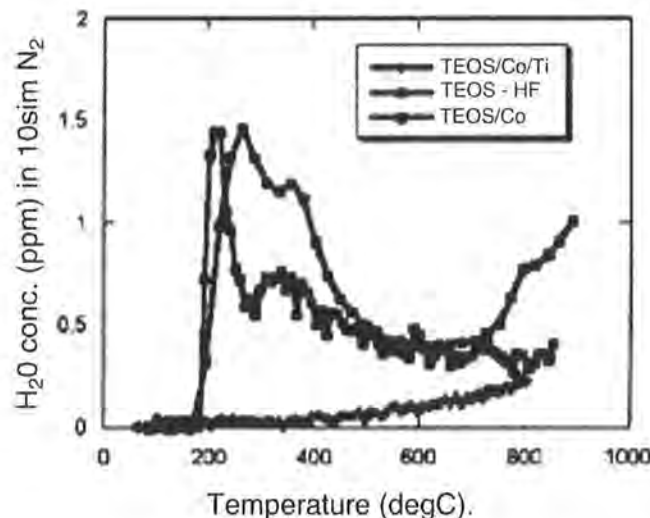


FIGURE 29. Detection of H₂O molecules released during RTP, from the wafer substrate with different surface layers. (Taken from Ref. 170. With permission.)

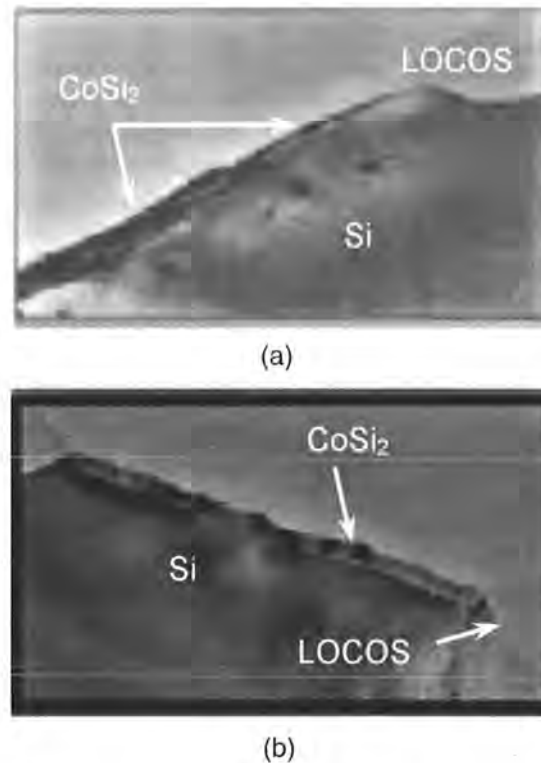


FIGURE 30. (a) Non-uniform and (b) uniform formation of CoSi_2 . (Taken from Ref. 170. With permission.)

SALICIDE processes are, with reference to Figure 8, illustrated in Table 2 for the formation of the three different low-resistivity silicides: C54 TiSi_2 , CoSi_2 , and NiSi . For Ni-SALICIDE, the process is simpler with only one annealing step needed, when compared with the Ti- and Co-SALICIDE processes. It also requires a considerably lower temperature. Because most of the metal-rich silicide phases shown in Table 1 do not directly participate in the SALICIDE processes, physical properties of TiSi_2 , CoSi , CoSi_2 , and NiSi extracted from Refs. 38, 52, 103, 172, and 173 are shown in Table 3. For comparison, the corresponding NiSi_2 properties are also included.

During MOS processing, the silicide films can be in contact with other chemicals usually used for surface cleaning. They can also be exposed to plasma for dry etching. Examples are dilute HF solution for the former and $\text{CHF}_3\text{-O}_2$ plasma for the latter. While the former is a routinely used surface etching/cleaning agent, the latter is often used for opening contact windows in the SiO_2 isolation. As a comparison, etching of

(a) C54 TiSi_2 ¹⁷⁴ and (b) NiSi in dilute HF (1 vol. % in H_2O) is shown in Figure 31 by monitoring the variation of sheet resistance of the silicide films vs. the time used for etching. The thickness of the etched-off silicides was converted from the sheet resistance data using the respective film resistivity values for C54 TiSi_2 and NiSi in Table 3. Clearly, NiSi is superior to TiSi_2 in terms of the resistant to the HF etching, since the sheet resistance of the NiSi film increases much more slowly than that of TiSi_2 . The results for TiSi_2 are comparable to those in Ref. 49.

When opening contact windows in the SiO_2 isolation, a slight over-etch is required to ensure the complete removal of SiO_2 in the windows. Thus, a comparison is shown in Figure 32 for dry etching of C54 TiSi_2 (a) and NiSi (b) using the $\text{CHF}_3\text{-O}_2$ plasma, since a silicide layer is present at the bottom of the contact windows. The different symbols in Figure 32a represent different test runs conducted under the same etching conditions. Again, NiSi shows a more resistant behavior.

TABLE 2
Parameters for SALICIDE Processing Using Ti, Co, or Ni^{6,49}

Metal	Temperature 1 st RTP (°C)	Phase to form after 1 st RTP	Wet selective etching	Temperature 2 nd RTP (°C)	Phase to form after 2 nd RTP
Ti	650-730	C49 TiSi ₂	H ₂ SO ₄ :H ₂ O ₂ + NH ₄ OH:H ₂ O ₂ :H ₂ O	>850	C54 TiSi ₂
Co	400-600	CoSi	H ₂ SO ₄ :H ₂ O ₂	>700	CoSi ₂
Ni	400-550	NiSi	H ₂ SO ₄ :H ₂ O ₂	-	-

TABLE 3
Properties^{38,52,103,172,173} of the Silicide Phases Directly Involved in SALICIDE Processes

Silicide	T _f (°C)	ρ (μΩcm)	Φ _{Bn} (eV) ^{d)}	DDS ^{e)}
C49 TiSi ₂	350-700 ^{a)}	60-80	?	Si
C54 TiSi ₂	750 ^{b)}	15-20	0.60	Si
Co ₂ Si	350	110	?	Co
CoSi	375	147	0.68	Si
CoSi ₂	500	15-20	0.64	Co
NiSi	250-400	10.5-15	0.65	Ni
NiSi ₂	700-800 ^{c)}	34	0.66	Ni

a) Upper limit depending on thickness, feature size and doping level.

b) Depending on thickness, feature size and doping level.

c) When formed from NiSi through a nucleation controlled process.

d) Φ_{Bn}: Schottky barrier height to n-type Si.

e) DDS – Dominant diffusion species during formation.

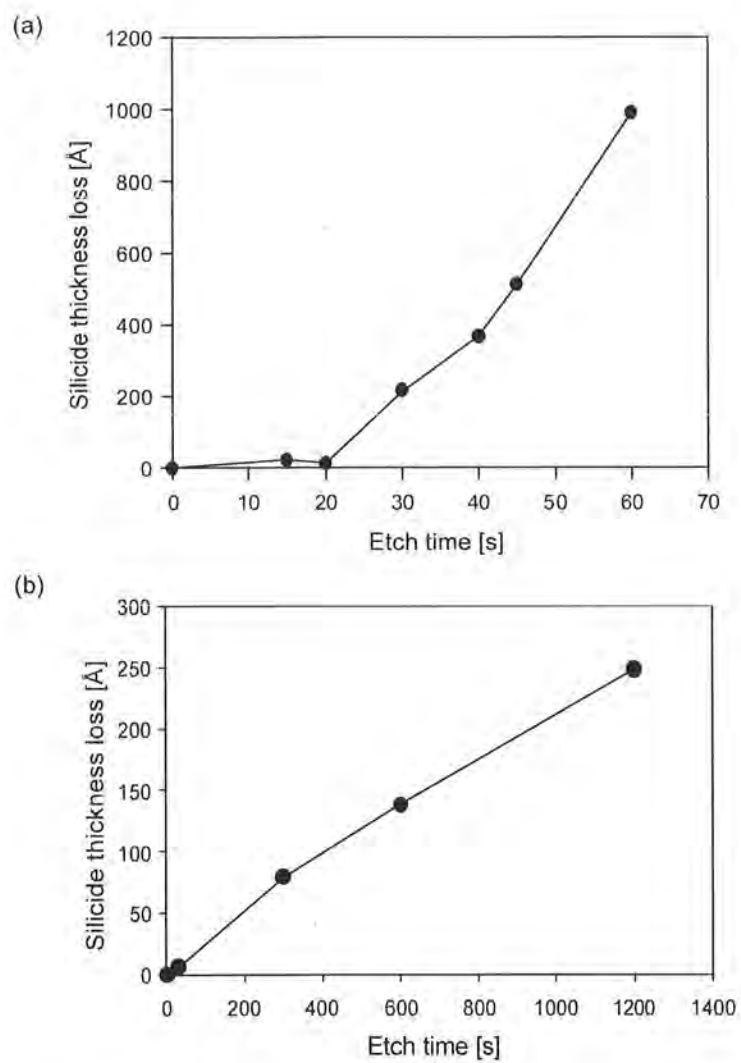


FIGURE 31. Thickness loss vs. time in 1% HF for (a) TiSi_2 and (b) NiSi .

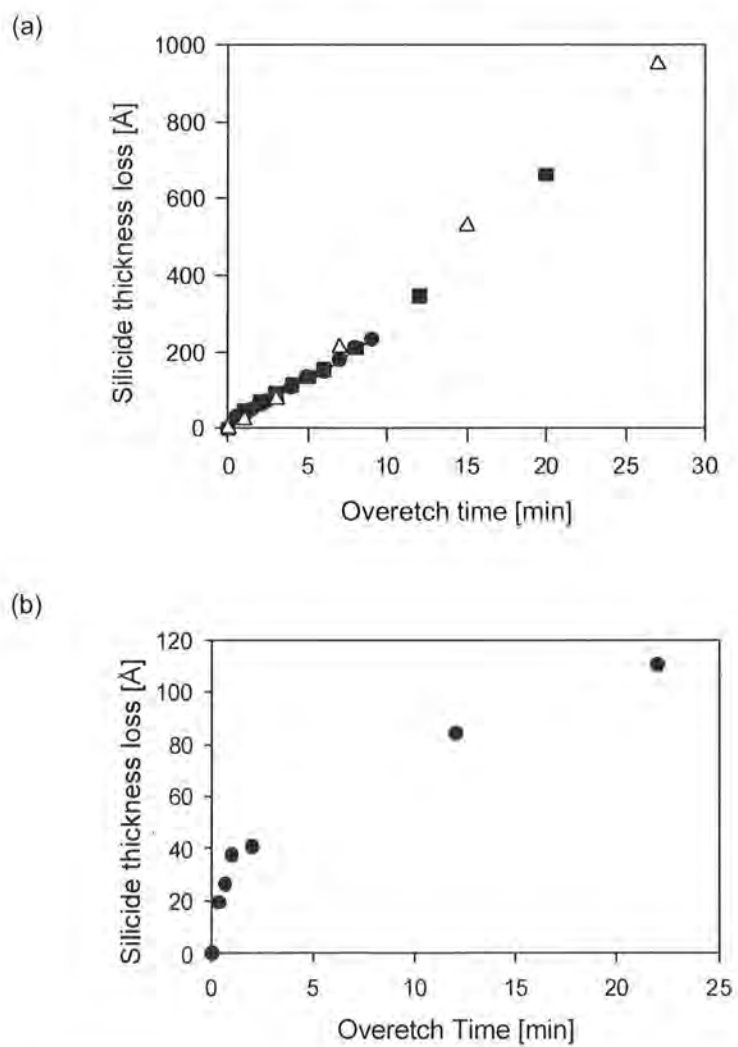


FIGURE 32. Thickness loss vs. time in $\text{CHF}_3\text{-O}_2$ plasma for (a) TiSi_2 and (b) NiSi .

B. Other Techniques for Silicide Formation

Before proceeding to discussions of the SALICIDE technology, a brief overview of other techniques useful for metal silicide formation or deposition is given below. It will be made clear that for various reasons the elaborated formation methods discussed below are not ideally suitable for contact metallization in CMOS technology.

1. Molecular Beam Epitaxy and Ion Implantation

Molecular beam epitaxy (MBE), largely a research-oriented tool, has also been utilized. With a template layer, epitaxial growth¹⁷⁵⁻¹⁷⁸ of metal silicides such as CoSi_2 and NiSi_2 that share with Si not only of the same crystallographic structure but also of an almost identical lattice parameter has been demonstrated. The fabrication procedure using this technique is shown schematically in Figure 33, with two slightly different ways to

grow the template layer. It is important to note that the high-quality epitaxial NiSi_2 and CoSi_2 layers grown by MBE provide a model system for understanding the physics of Schottky barriers.¹⁷⁹⁻¹⁸³ In general, inhomogeneities exist at the metal-semiconductor interfaces due to the anisotropic properties of crystalline solids that lead to appreciable work-function variations at the interfaces between polycrystalline materials, in particular. Hence, "abnormal" behaviors of Schottky barriers are observed if the interfaces are not understood.¹⁸³ Although the MBE technique¹⁷⁵⁻¹⁷⁸ described in Figure 33 could be used for producing good Ohmic contacts in the source/drain regions, the complexity (e.g., with ultrahigh vacuum) makes it unsuitable for large-scale device production.

Ion implantation of metal atoms into Si followed by appropriate heat treatments, named "mesotaxy", can also lead to the formation of epitaxially aligned silicide films.¹⁸⁴ The selection of metals for ion implantation is mainly based on the consideration of their silicides matching with the Si lattice of diamond structure, since the epi-

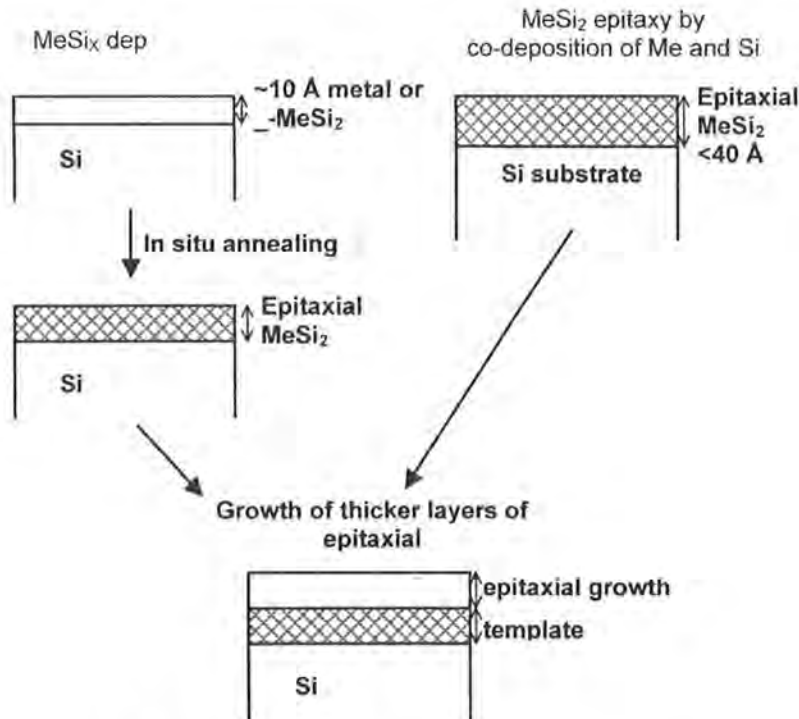


FIGURE 33. Template method for epitaxy of silicides by MBE.

taxy quality of the silicides is sensitive to such lattice matching. For this reason, Co and Ni are the most studied cases.¹⁸⁴⁻¹⁹² The rather flexible mesotaxy technique has also been used for the formation of a variety of other buried silicides such as CrSi_2 ,¹⁹³ FeSi_2 ,^{194,195} $\text{ErSi}_{1.7}$,¹⁹⁶ $\text{YSi}_{1.7}$,¹⁹⁷ and $\text{GdSi}_{1.7}$.¹⁹⁸ Even bi-metal silicide systems with Nd-Y,¹⁹⁹ Co-Y,²⁰⁰ Co-Fe,²⁰¹ and Ni-Fe²⁰¹ have been demonstrated. The silicide films formed by mesotaxy are often buried under a thin surface Si layer. See Figure 34 for the procedure with CoSi_2 as an example. Another method for such buried structures is "allotaxy",²⁰² shown schematically in Figure 35. Here, the metal atoms are grown into the structure instead of being implanted. Similarly, use of appropriate subsequent heat treatments is crucial for the allotaxy technique.

The main application of buried epitaxial silicides is, however, for other types of devices, for example, metal-base transistors (MBT) or permeable-base transistors (PBT).^{203,204} Their fabrication procedure is not entirely compatible with the standard CMOS process, thus not suitable for contact metallization of the ultrashallow junctions in small MOSFETs. Therefore, no further discussion of MBE, mesotaxy, or allotaxy is cov-

ered in the present work, and interested readers are referred to three dedicated reviews of von Känel,²⁰⁵ Mantl,²⁰⁶ and Bulle-Lieuwma.²⁰⁷

2. Chemical Vapor Deposition

Having a long tradition in the microelectronics industry, chemical vapor deposition (CVD) offers a number of unique features that are difficult to realize with PVD. Those include conformal deposition with excellent step coverage²⁰⁸ and selective deposition on areas of specific surface properties.²⁰⁹ The deposition of metals by CVD has been studied for more than 30 years.²¹⁰⁻²¹⁴ The deposition of metal silicides attracted great attention about 25 years ago when IBM first showed the success in deposition of WSi_x .²¹⁵ It was demonstrated that the CVD WSi_x could be used not only as a current shunt for the gate electrode but also for local interconnections.²¹⁶ Similar attempts were then quickly investigated for the depositions of TiSi_x ,²¹⁷ MoSi_x ,²¹⁸ TaSi_x ,²¹⁹ and CoSi_x .²²⁰

While the stoichiometry of the silicides, that is x in MeSi_x with "Me" denoting the metals, is

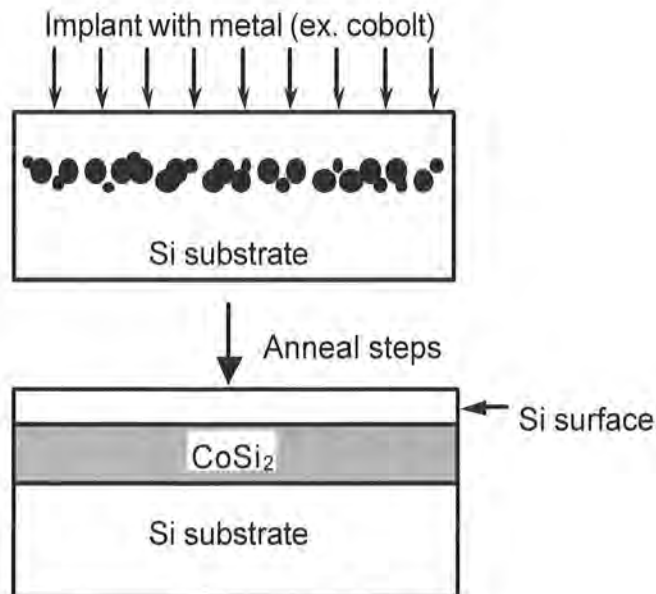


FIGURE 34. Mesotaxy method for buried epitaxial silicides.

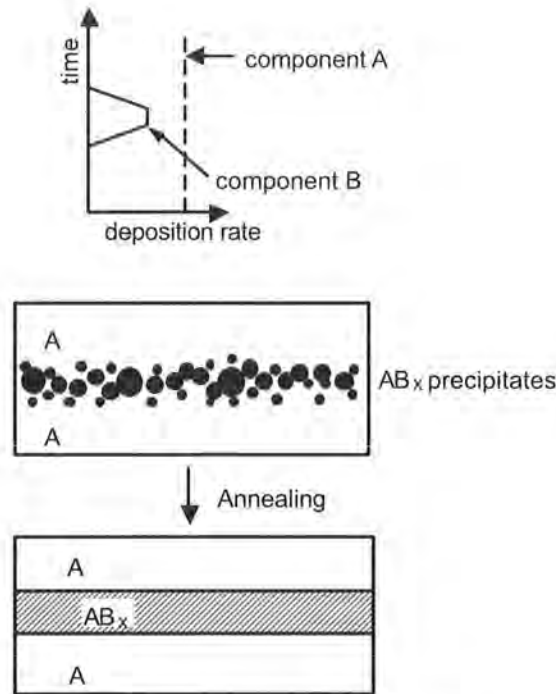


FIGURE 35. Allotaxy method for buried epitaxial silicides.

determined by the temperature and/or time used for the silicide formation in the case of solid-state reaction of metal and Si, it is determined by the ratio of the partial pressures of the precursors being fed in a CVD reactor. Other parameters such as substrate temperature also affect the stoichiometry of the CVD metal silicides. Very often, the deposited films are off from equilibrium stoichiometries. For the deposition of WSi_x , for instance, a detailed discussion based on thermodynamic equilibrium calculations can be found in Ref. 221. Different composition domains, each with up to two phases (W, silicides — W_5Si_3 and WSi_2 , and Si), are defined. The theoretically predicted atomic composition (x) of the WSi_x films deposited under different conditions agreed well with the experimentally found results.²²² One can find similar thermodynamic considerations in Refs. 223 and 224 for the deposition of other refractory metals and silicides, that is, TaSi_x and TiSi_x . For these refractory metal silicides, the deposition of silicide films off-stoichiometric can either lead to precipitation of Si (with $x > 2$) or result in consumption of Si substrate (with $x < 2$) during subsequent annealing at high temperatures.

The deposition of silicide films is, however, mainly interesting for the POLYCID structure. Therefore, it is generally not attractive for small-dimension MOS devices as discussed earlier, unless the selective deposition feature of CVD could be utilized. Selective depositions of stoichiometric TaSi_2 ,²²⁵ WSi_2 ,²²⁶ and TiSi_2 ,^{217,227} onto Si with respect to the surrounding SiO_2 isolation have been demonstrated. The selective deposition of TiSi_2 using TiCl_4 and SiH_4 became very attractive,^{217,227-241} due to the low specific resistivity as well as the widespread use of TiSi_2 in the SALICIDE process. However, as with other selective processes, the selective deposition of TiSi_2 is a surface sensitive process. Slight surface contamination with oxygen or carbon could jeopardize the deposition leaving poor deposition in the desired areas, that is, gate and source/drain.^{217,238} Because Si substrate consumption due to etching by TiCl_4 is an important concern for MOS devices, efforts have been focused on carefully tuning the deposition parameters in order to minimize or eliminate the consumption (see Figure 36 for the concept).²²⁹⁻²³² Substrate consumption also leads to the loss of As dopants from the Si sub-

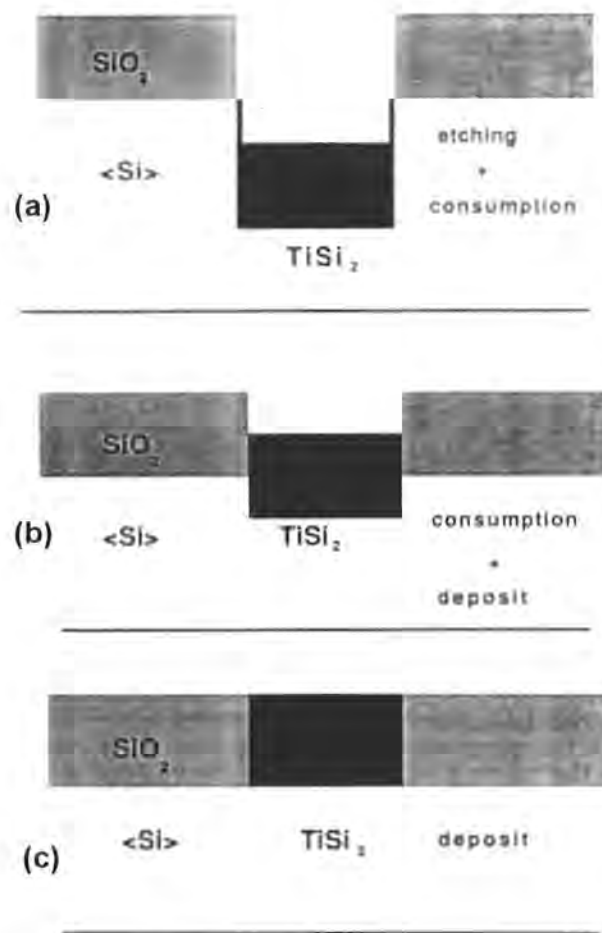


FIGURE 36. Selective deposition of TiSi_2 (a) with etching and consumption of Si (b) with consumption of Si and (c) without consumption of Si. (Taken from Ref. 231. With permission.)

strates.²⁴² The deposition of a sacrificial Si layer prior to the interaction of TiCl_4 with Si or SiH_4 could be viable for control of the substrate consumption.^{228–233} However, detailed local surface chemistry with heavily doped Si regions (with p-type vs. n-type dopants) could alter the deposition properties,²⁴¹ which imposes a tough challenge for the successful selective deposition of TiSi_2 . Indeed, the selective deposition of Si, which has an important bearing on the deposition of TiSi_2 , is a sensitive process to the substrate doping.^{243,244} Additionally, the selective deposition of TiSi_2 by CVD does not seem to yield the expected superiority to the SALICIDE process in terms of phase formation in TiSi_2 in narrow lines.²⁴⁵

A major concern with CVD of metals and metal silicides is the search for appropriate reaction precursors.²²⁴ For silicide deposition, a metal-carrying precursor and a Si-bearing precursor are needed. One may also find a precursor that contains both Si and the desired metal.²⁴⁶ While there is a relatively rich number of Si-bearing precursors among which one can choose from depending on applications, the metal-carrying precursors are, however, not always available for the desired metal silicide depositions. The rather limited number of inorganic precursors has forced the users to explore organic precursors. While the inorganic precursors are often corrosive, explosive, and toxic, the metal-organic ones are extremely un-

stable and flammable. Therefore, the safe handling of such precursors can impose constraints on their industrial use. One added problem with metal-organic precursors is that the deposits often contain a large quantity of carbon atoms. The presence of carbon usually gives rise to an undesired high specific resistivity of the deposited metal silicide films.

The selective deposition of metal silicide films is a very demanding process, because two precursor source gases, one for Si often SiH_4 and another for metal usually a halogenide, are involved. As in the TiSi_2 deposition, the deposition process requires a delicate balance among good selectivity, minimal substrate consumption and desired stoichiometry. The process certainly becomes much simpler if only metal is deposited. The selective deposition of metals on the Si surfaces could be attractive for the SALICIDE technology, because it would in principle eliminate the risk of electrical shorts between the gate and source/drain regions over the SiO_2 spacer isolations in Figure 1. However, caution must be exercised with the processes of metal deposition. For W deposition using H_2 reduction of WF_6 that is a gas at room temperature, difficult issues such as the formation of encroachment, voids and microchannels (wormholes), incorporation of fluorine and oxygen at the W/Si interface, and rough interface and surface can lead to severe reliability problems.²⁴⁷⁻²⁵⁸ The aggressive nature of WF_6 and the subfluorides of tungsten (WF_5 and WF_4) coupled with local oxygen contaminations has been identified as the cause for the formation of such defects.²⁵⁹ Therefore, it is advisable not to make W deposition directly onto Si surfaces. Using SiH_4 or Si_2H_6 reduction of WF_6 for deposition of W^{260} might lessen the problems, but it requires fine-tuning for selective deposition and, simultaneously, the suppression of defect formation. The use of SiH_2Cl_2 ,²⁶¹ instead, would further complicate the process since one has to handle two halogens (F and Cl) simultaneously.

Although selective deposition of W, Mo, Ta, and Ti using their respective halogenides WCl_6 (solid), MoF_6 (gaseous), TaCl_5 (liquid), and TiCl_4 (liquid) has been much less studied, it is expected that one is to encounter similar issues found in the W deposition using WF_6 . One further complica-

tion with TiCl_4 is the impossibility to obtain Ti by H_2 reduction. When Si is also available during the deposition, Si reduction of TiCl_4 leads to the growth of TiSi_x on the expenses of Si substrates.^{217,227-242} In all processes discussed, halogen contamination can be a concern. The minimization of halogen contents can at least lead to a decreased film resistivity. Chemical vapor deposition of Co using $\text{Co}(\text{CO})_3\text{NO}$, an organic precursor, has been shown recently.^{262,263} Because it is a nonselective process potentially contaminated with appreciable amounts of C and O, whether it is advantageous to use such Co layers instead of the sputter-deposited Co films for SALICIDE awaits further investigation.

C. Characterization

An efficient characterization methodology is crucial for the diagnosis of the formation of silicide films. There are numerous analysis techniques available for the analysis of the silicide films. A list of all those techniques can become several pages long.²⁶⁴⁻²⁶⁷ It is, however, beyond the scope of this review to go through each of them. Instead, the goal of this section is to review the basic features of a handful of techniques that are most commonly used for silicide studies. These analysis techniques are most suitable for blanket samples without any pattern or structure. To qualify the silicide formation in actual devices, some useful test structures and circuits are shown. Several of the analysis techniques are often combined in order to obtain the most precise information of silicide formation.

1. Physical Analysis and Electrical Characterization²⁶⁴⁻²⁶⁷

Phase identification. Phase formation in silicide thin-films is usually identified using X-ray diffraction (XRD)²⁶⁸ with Cu K_α radiation that has an average wavelength (1.5418 Å) comparable to the atomic interplanar spacings of the silicide phases of interest. A rich databank comprising thousands of the diffraction patterns obtained from powder standards is commercially

available.⁷⁹ As X-ray beams usually have a rectangular shape of millimeters by millimeters size, average information is extracted. Because the depth of penetration of X-rays into the silicide films can be up to several micrometers, depending on the material properties of the silicide, normally no depth resolution is possible.

Depth profiling of atomic composition. Depth resolution of film stoichiometry can be obtained with Rutherford backscattering spectrometry (RBS)²⁶⁹ typically using He⁺ ions accelerated at about 2 MeV. For ultrathin films of a few hundred Å's thickness, appropriate sample tilting can significantly improve the depth resolution. Although RBS also gives average information of a sample film because its beam size is typically millimeters in diameter, a combined use of XRD and RBS can often lead to conclusive information of the silicide phase(s) formed. To the extent that the depth resolution is satisfactory, reliable information about surface or interface morphology can be gained using RBS.

Similar information can also be extracted by combining the use of Auger electron spectroscopy (AES) or X-ray photoelectron spectroscopy with sputter-etching. Even information about electron bonding can be acquired simultaneously. Calibrated standards are necessary for quantification of atomic composition using AES or XPS.

Dopant distribution. With a typical sensitivity of 1 to 5 at. %, RBS and AES cannot provide useful information about the dopant distribution in silicide as well as in underlying Si, as dopant concentrations are typically below 1 at. %. Such information can be readily extracted using secondary ion mass spectrometry (SIMS) that has a large dynamic range up to 8 orders of magnitude. SIMS technique also requires reference samples for quantification purposes.

Surface morphology. Much more accurate information about the surface/interface morphology can be obtained using atomic force microscope (AFM). The quantification of surface roughness is possible with AFM, but great caution should be exercised when attempting to correlate the roughness data to the size of silicide grains.²⁷⁰

Information at micrometer/nanometer scales. Local information about phase formation, atomic composition, and morphology can be gained us-

ing scanning electron microscopy (SEM) in combination with energy-dispersive spectroscopy (EDS). The relatively poor resolution with SEM has led to the more frequent use of the more elaborated method TEM, especially for identification of phase(s) formed in small features such as contact window structures. Several examples of the use of TEM combined with EDS are shown in Section IV.

Conductivity of thin films. Sheet resistance measurement using a four-point probe²⁷¹ is perhaps the most convenient and rapid means used for monitoring the solid-state interaction. This convenience is based on the fact that the silicides of a specific metal have distinctly different specific resistivity values.^{38,52,173} Because two factors, thickness and specific resistivity, contribute to the sheet resistance values measured, it is important that phase identification based on resistance measurements take probable thickness variations into consideration.

Studies using blanket substrates are, however, insufficient for actual devices made in or with small-geometry features. The example in Ref. 170 shows a disturbed formation of CoSi₂ due to oxygen contamination coming from the surrounding SiO₂. Another well-known example is the difficult C49-C54 phase transformation in TiSi₂ that is mainly observed in narrow Si lines of 0.5 μm and below²⁷² or small Si features of 100 μm² or below.²⁷³ Obviously, there is a need for proof-of-concept studies on patterned structures in order to qualify a SALICIDE process.

2. Test Structures and Circuits

Electrical shorts due to silicide formation over the SiO₂ spacer. Successful SALICIDE processing requires that the gate and source/drain regions be electrically isolated after the silicide formation. Three efficient test structures for evaluating whether these two regions are linked electrically are shown in Figure 37.²⁷⁴ The structures principally consist of a SiO₂ spacer (cf. Figure 1) between the two regions deliberately made over different surface topographies to emulate the surface of a practical device. Currents are monitored using a high-sensitivity current meter when a bias

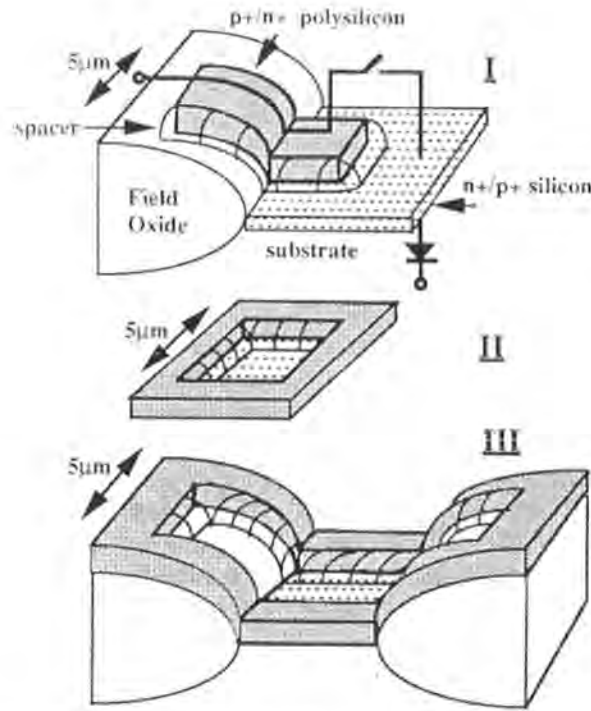


FIGURE 37. Bridging test circuits. (Taken from Ref. 274. With permission.)

potential is applied between the two regions. Since the SiO_2 spacer is usually made millimeters to centimeters long, it is a highly sensitive bridging-monitor.

Electrical properties of a silicide/Si contact. As metal-semiconductor interfaces constitute an indispensable part of a MOSFET, as shown in Figures 1 and 6, a relatively extensive description of electrical characterization of the interfaces is given below. An electrical contact between a metal and a semiconductor can be either Schottky or Ohmic mainly dependent on substrate doping concentration and Schottky barrier height.^{275,276} For contact metallization in MOSFETs, it is the latter type usually with heavy doping in the semiconductor that is of major interest. Studies of Schottky contacts are, however, implicative for studies of Ohmic contacts, because the Schottky barrier height, Φ_{Bn} , of a specific metal-semiconductor interface appears in the theoretical formula for the specific contact resistivity, ρ_c .²⁷⁵⁻²⁷⁷

$$\rho_c \propto \exp\left(\frac{2\Phi_{Bn}}{qh} \sqrt{\frac{m^* \epsilon_r}{N_D}}\right) \quad (13)$$

where Φ_{Bn} denotes the Schottky barrier height of metal to n-type semiconductor, q electronic charge, h Planck's constant, N_D n-type doping concentration in the semiconductor, m^* effective mass of electrons in the semiconductor, and ϵ_r the relative permittivity of the semiconductor. The values of Φ_{Bn} for the silicides of interest are given in Table 3. For details about Schottky contacts, the readers are referred to Refs. 275-277. The focus here is placed on Ohmic contacts that are usually obtained when a metal is in contact with the heavily doped Si. The ITRS requirements for contact resistivity for future generations of CMOS technologies are shown in Figure 3. In practice, the contact resistivity is obtained by measuring the current density J (in A cm^{-2}) at infinitesimal potentials (V) across a contact, i.e.,

$$\rho_c = \frac{1}{\left(\frac{\partial I}{\partial V} \right) \Big|_{V=0}} \quad (14)$$

Characterization of Ohmic contacts has attracted intensive attention for the last four decades since Shockley outlined a scheme employing the transmission-line model to analyze the contacts.²⁷⁸ Examples of the efforts on constructing test circuits and analyzing measurement results are given in several early publications²⁷⁹⁻²⁸⁴ and in a special issue of *IEEE Transaction on Electron Devices* in 1987.²⁸⁵ Over the years, numerous methods and structures have been utilized for measurement of ρ_c .^{286,287} Only two of them, transfer-length method or transmission-line method (TLM) and cross-bridge Kelvin structure (CBK), are discussed here, because they resemble the geometrical and electrical feature of a practical contact in the source/drain of a MOSFET, that is, the current enters the contact laterally from its side.

TLM

The work of Berger^{287,288} lays the foundation for modern contact characterization techniques including TLM and CBK. In Figure 38, the one-dimensional (1D) transmission-line model used by Berger for characterizing a contact is shown. The structure is composed of three layers—semiconductor, interface, and metal. While the semi-

conductor and metal layers act as two transmission lines, the interface layer defines the electrical communications between them resistively (through G') and capacitively (through C'). By analyzing the current and voltage components at the entrance and exit of the contact, denoted as i_1 , i_2 , v_1 , and v_2 , mathematical relations leading to the extraction of ρ_c can be obtained.²⁸⁸ Therefore, the model leads directly to one of the most frequently used structures/methods today. The method, TLM, relies on the use of a number (greater than 3) of identical contacts on a resistor bar of the semiconductor (*i.e.*, diffusion layer). The contacts are linearly arranged but separated to different distances, see Figure 39 for a schematic presentation. In the sketch, heavily doped poly-Si with SiO_2 beneath for isolation is used as an example for the “Diffusion layer” to illustrate how a TLM structure can be made using three levels of photolithography. The poly-Si can, of course, be replaced with a single-crystal Si on insulator, for example, using an SOI (silicon-on-insulator) substrate. Traditionally, it is heavily doped single-crystal Si with a p-n isolation beneath that is referred to as the “Diffusion layer”. The measurements of the potential difference between two adjacent contacts while passing a known current yield a total resistance expressed as,

$$R = 2R_c + \frac{d}{W} R_s. \quad (15)$$

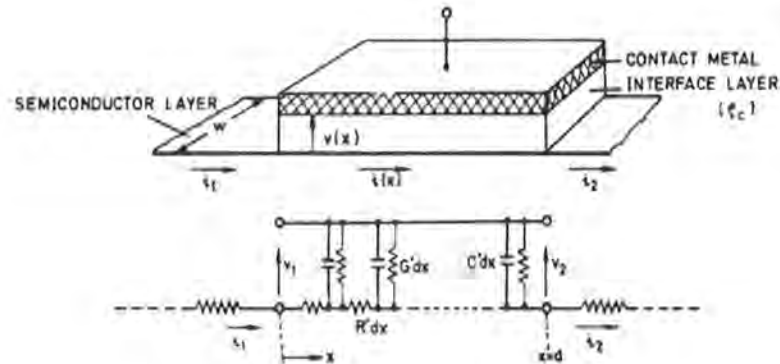


FIGURE 38. Schematic view of a metal/semiconductor contact system (top) with a 1D transmission-line model to describe the current and voltage distributions (bottom). (Taken from Ref. 288. With permission.)

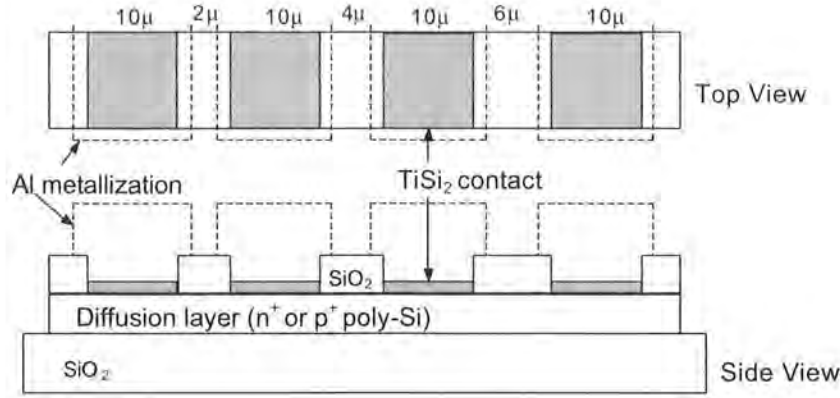


FIGURE 39. Schematic view of a TLM structure.

Here, R_c represents the contact resistance between the metal and semiconductor, R_s the sheet resistance in the semiconductor between the two contacts, d the distance between the two contacts and W the width of the resistor bar. In writing Eq. 15, the series resistance of the metal is neglected; this is a valid assumption for most cases of interest. Also assumed is an equi-potential condition at the metal contacts, a condition that unfortunately is not always met in the published work. Repeating the measurement on another pair of contacts with a different d leads to elimination of R_s and direct calculation of R_c as,

$$R_c = \frac{d_2 R_1 - d_1 R_2}{2(d_2 - d_1)}. \quad (16)$$

To minimize the influence of measurement uncertainties on the accuracy of R_c , it is common practice to make similar measurements on several pairs.^{278,282,284,287,288} When the contacts are made sufficiently long, a plot of R vs. d yields a straight line with three important parameters [cf. Eq. 15]: the slope corresponds to R_s , the intercept on the y-axis (R) to $2R_c$ and the intercept on the x-axis (d) to an important parameter named transfer-length²⁸⁴ L_T that is in turn determined by,

$$L_T = \sqrt{\frac{\rho_c}{R_s}} \quad (17)$$

Thus, a "simple" set of measurements using TLM can readily yield ρ_c , R_s , and R_c . It is ρ_c , not R_c , that is characteristic of a contact.

To calculate R_c for a practical contact of length L_c in the source/drain regions (Figure 40), the following is derived based on the transmission-line model:²⁸⁸

$$R_c = \frac{\sqrt{\rho_c R_s}}{W} \coth\left(\frac{L_c}{L_T}\right). \quad (18)$$

For a long contact with $L_c \gg L_T$, $\coth\left(\frac{L_c}{L_T}\right) \approx 1$

and Eq. 18 is reduced to:

$$R_c = \frac{\rho_c}{L_T W}. \quad (18a)$$

For a short contact with $L_c \ll L_T$, $\coth\left(\frac{L_c}{L_T}\right) \approx \frac{L_T}{L_c}$

and Eq. 18 is simplified to:

$$R_c = \frac{\rho_c}{L_c W}. \quad (18b)$$

Large errors in the so-determined values of ρ_c and R_s can arise because of geometrical or material modifications around the contacts. Three major error sources are identified, cf. Figure 41.

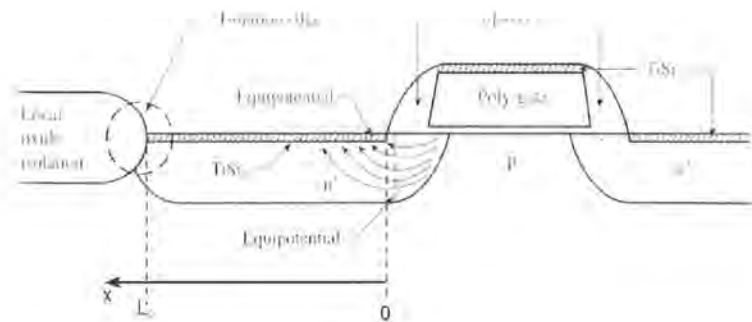


FIGURE 40. Schematic cross-section of a MOSFET with silicided gate, source and drain contact. (Taken from Ref. 667. With permission.)

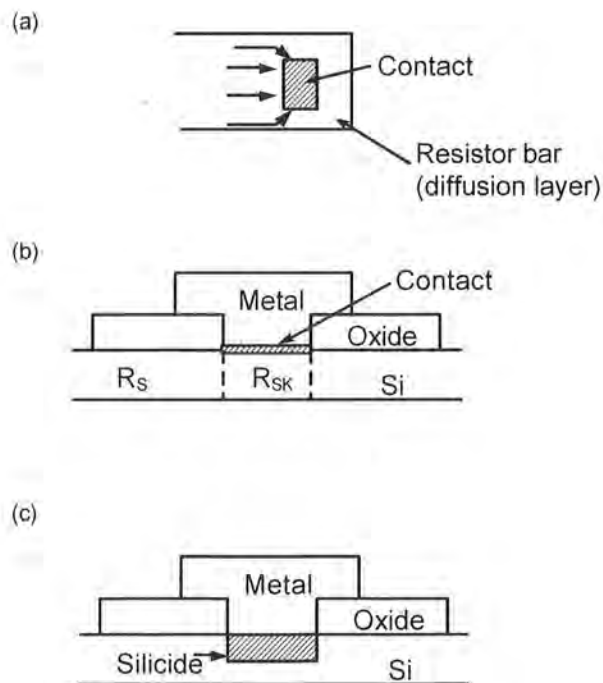


FIGURE 41. Three potential error sources in TLM contact resistivity extraction: (a) 2D current crowding, (b) variations in sheet resistance of the Si under the contact (R_{sk} different from R_s), and (c) considerable silicide step into the Si.

(1) Berger²⁸⁷ and later Loh *et al.*^{289,290} pointed out that the width of the contacts are usually different from that of the resistor bar due to contact fabrication details. Two-dimensional (2D) effects, that is, “current crowding” — current flowing around the contacts (Figure 41a for a top view), that are neglected in the 1D model above can result in a considerable deviation of ρ_c from its true value. The degree of deviation, either overestimation or underestimation, not only depends on the value of ρ_c and R_s , but also on the size of the “overlap”, that is, the distance from the contact edge to the resistor edge relative to the contact width.²⁹⁰ (The overlap is, of course, determined by the lithography capability.)

(2) During contact formation, it is likely that the material properties of the semiconductor part directly beneath the contacts are modified because of dopant redistribution and/or surface interaction. Thus, the sheet resistance in these areas can depart from R_s (Figure 41b for a side view), one of the important parameters in the 1D model. Reeves and Harrison²⁹¹ proposed a simple remedy with an additional measurement to obtain the so-called contact-end resistance. Such a measurement is made using a third contact: the potential difference is measured between the third contact and the closer one of the pair-contacts under current stress.

(3) For silicide formation in particular, the planar feature assumed in the 1D model, that is, the contact lies at the same level as the rest of the resistor as shown in Figure 39, is no longer valid. (The silicide step is negligible for the contact structure in Figure 40.) Silicon consumption during silicide formation⁴⁷ leads to the presence of the silicide layer in the recessed Si areas in the contact windows as shown in Figure 41c for a side view, precisely as is indicated in Figures 1, 8, and 9 as well. The presence of such a silicide step calls for 2D models if the above-mentioned overlap can still be neglected. A numerical calculation based on 2D modeling²⁹² shows an appreciable underestimation of ρ_c amounting to 20 to 50 % with the 1D model. The degree of underestimation not only depends on the values of ρ_c and R_s , but also on the size of the step relative to the

entire thickness of the resistor (diffusion layer). Therefore, it is anticipated that the influence of the silicide step on the accuracy of the extracted ρ_c becomes more problematic for contacts in smaller MOSFETs, because the silicide layer is expected to become a greater part of the shallower junctions in the source/drain regions according to ITRS.

CBK

The extraction of ρ_c using TLM is indirect because it is relying on the measurement of two or several resistor circuits, each comprising not only the contact resistance but also the series resistance in the semiconductor resistor. Hence, the CBK technique, aiming at direct measurement of ρ_c emerged.^{293,294} In detail, two different CBK structures can be constructed: the L type vs. the D type. Both structures are shown in Figure 42 where physical dimensions, measurement arrangements, and the fabrication procedure using three levels of photolithography are also given. A 1D analysis by Proctor *et al.*^{293,294} reveals that ρ_c can be obtained by measuring R_c of a contact with known area A on a CBK structure, *i.e.*,

$$\rho_c = A \times R_c. \quad (19)$$

In practice, a series of contacts of different dimensions should be made and measured. When the log-log plot of R_c vs. A yields a straight line of slope -1 , any measurement data point gives ρ_c through Eq. 19.^{293,294} As an overlap around the contact is always present due to process details, similar to the TLM structure in Figure 41a, the 2D current crowding effects are also present in the L-type CBK structures. Such effects lead to a downward bending of the line in the log-log plot of R_c vs. A ,^{293,294} that is, the line is no longer straight with a single slope and a 2D model becomes a necessity. In the 2D models, ρ_c and R_s are extracted simultaneously. Through the thorough mathematical treatments of Loh *et al.*,^{289,290} it is made clear how and why the 1D model fails. The use of the 1D model without taking into consideration current crowding effects tends to give rise to overestimate values of ρ_c . The degree of overestimation not only depends on the size of the overlap relative to the contact width, but also is

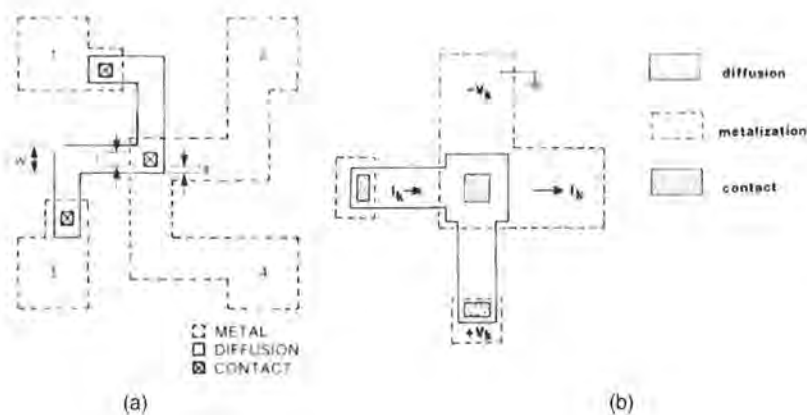


FIGURE 42. Top view of CBK structures: (a) L-type and (b) D-type. (Taken from Ref. 285. With permission.)

affected by the values of ρ_c and R_s . In Figure 43, the important difference between the 1D and 2D models in terms of the potential distribution in the semiconductor along the contact is depicted.²⁹⁰ In short, the 2D effects with current flowing around the contact make the voltage decrease along the direction of current flow strongly deviate from the exponential behavior predicted by the 1D model.

The design of the D-type CBK structure, with the two resistor arms being trimmed and aligned to the contact size, is an attempt to minimize such 2D effects.^{293,294} When the dimension of the contact windows is reduced following the downscaling trend of the MOS devices, the overlap becomes an increasingly significant part of a contact if not being scaled down in the same proportion. For such small devices, the current crowding is nonnegligible even for the D-type structure. Gillenwater *et al.*^{295,296} conducted a study of the D-type CBK structure also using a 2D model and explored potential effects of different imperfections due to poor process control. The misalignment of the contact relative to the resistor arms and overetching or underetching of the contact are two readily encountered technological difficulties.

In general, CBK yields a better accuracy than TLM.²⁸⁶ The implementation of 2D models has greatly advanced the art of contact resistivity assessments. However, for contact resistivity below $10^{-7} \Omega\text{cm}^2$, necessary for CMOS technologies

beyond 2007 with the 65-nm technology node, the extraction of accurate values of ρ_c can become problematic because the resistance curves generated by means of 2D models begin to become close-packed and therefore difficult to resolve (see Figure 9 Ref. 290). For such low-resistivity contacts, the contact geometry as well as the semiconductor resistor should be carefully examined for designing functioning CBK structures. The presence of a silicide step in the contact window,²⁹⁷ as depicted in Figure 41c, further complicates the problem, and a three-dimensional modeling is necessary for the reliable extraction of ρ_c .

3. In Situ Real-Time Characterization

In situ characterization has become increasingly attractive because it helps visualize the problems encountered in thin-film interactions in real-time. An example is resistance measurements during temperature up-ramping, a simple yet very informative technique that has been used by many to monitor the phase formation in silicide films often with the attempt to study the kinetics as well.^{298–306} Because the resistance value of a thin film is also strongly correlated to the morphology of the film, both *in situ* and *ex situ* resistance measurements are often used for monitoring the morphological developments after annealing. In combination with *in situ* stress measurements, the kinetics of silicide formation as well as poly-Si

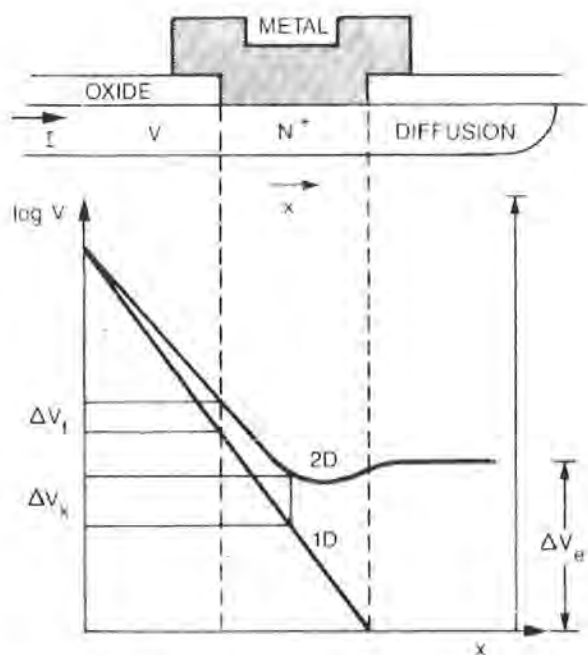


FIGURE 43. 2D vs. 1D analysis of the potential distribution around a CBK contact. (Taken from Ref. 290. With permission.)

degradation were studied by Hong *et al.*¹⁴⁵ for a number of silicides. One should, however, be cautious in interpreting the results from such resistance measurements. Zhang and d'Heurle^{307,308} studied two different thin-film morphologies corresponding to the two different modes of phase formation: nucleation controlled or diffusion controlled. Mathematical analysis shows^{307,308} that the Kissinger plot:^{309,310} $\ln(m/T^2)$ vs. $1/T$ with m as the linear rate of heating and T the transformation temperature, originally derived based on differential thermal analysis, can indeed be adopted to yield the so-called activation energy for phase formation or transformation using *in situ* resistance measurements.

In situ TEM studies of the influence of oxygen on the C49–C54 phase transformation in TiSi_2 by Ross¹⁷¹ convincingly shows the usefulness and importance of such kinds of analyses. Gignac *et al.*³¹¹ used *in situ* TEM to study the motion of the C49–C54 transformation front and determined the velocity of the moving front in blanket substrates as well as in narrow lines down to $0.13\text{-}\mu\text{m}$ width. When XRD is used, specially designed structures with an immensely large number of narrow lines

densely placed are suitable for *in situ* characterization.^{311–313}

Correlation to the results of *ex situ* XRD analysis on similarly arranged narrow lines can be revealing.³¹⁴ IBM Watson Research Lab has over the years built a powerful *in situ* analysis apparatus that is capable of carrying out real-time structural (by diffraction), electrical (by resistance measurement), and morphological (by surface light scattering) analyses simultaneously.^{315–318} A schematic view of the IBM set up is shown in Figure 44.³¹⁷ For diffraction studies, the apparatus uses X-rays at Beamline X20C of the National Synchrotron Light Source (NSLS), Brookhaven National Laboratory, New York. An X-ray linear detector is used for rapid and effective recording. For morphology studies, an He:Ne laser beam is focused on the sample surface, and the scattered photons are monitored by two optical detectors at different wavelengths. The *in situ* resistance measurement details are omitted in the figure for clarity. Such *in situ* analysis capabilities have also opened ample opportunities for materials research. One example is an ingenious combination of *in situ* XRD with *in situ* surface light scattering by

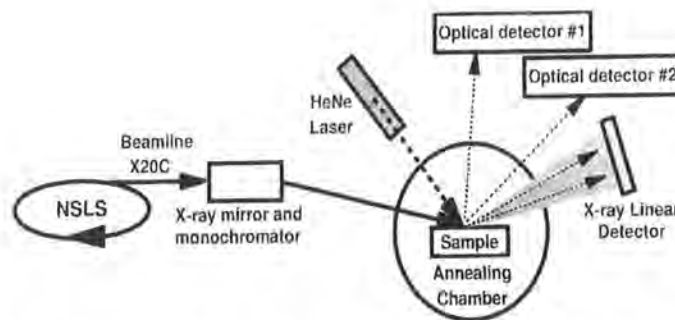


FIGURE 44. Schematic picture of the IBM setup for *in situ*, real time, x-ray diffraction and surface light scattering measurements. (Taken from Ref. 317. With permission.)

Lavoie *et al.*³¹⁸ recently that yields extremely important information about the mechanisms of silicide formation in Ti-Si, Co-Si, and Ni-Si systems with crucial implications for device applications, as seen later. Another example is the search for performance improvement of the CoSi₂ formation by sorting out those of the most effective from 23 different Co-alloys.³¹⁹

IV. CHALLENGES AND POTENTIAL SOLUTIONS

The convergence of the technologies for contact metallization and local interconnection to SALICIDE with a small group of metals, that is, Ti, Co, and Ni, is a response to the increasing demands set by the projected system/circuit performances that are anticipated from and driven by MOSFETs of decreasing dimensions. To make such modern MOSFETs typically of 100-nm gate length or below, it is essential to minimize the parasitic contact and series resistances in the gate and source/drain regions. It is also critical that the SALICIDE process does not lead to modifications of the defined device structure, including doping profiles. Hence, a set of general criteria for selection of a metal for silicide formation in these regions is given below:

- High conductivity
- Low contact resistivity to both types (n and p) of heavily doped Si
- Good chemical stability in contact with Si

- Satisfactory thermal and mechanical properties with reference to Si
- Satisfactory thermal stability that leads to good morphological stability on Si
- Compatibility with standard Si processing technology, including cleaning and etching
- No requirements for excessive thermal treatments
- No detrimental contaminations that affect device performance

Further, yet more specific, requirements will be added to this list when discussing the increasingly stringent demands as a consequence of the continual developments of CMOS technologies. They are brought up in this section in conjunction with the introduction of Ti, Co, and Ni as well as their silicides. It is, in fact, these specific requirements that dominate the selection of a metal and its silicide(s) for contact metallization in CMOS technologies.

Because the demands for the gate are not necessarily identical for those for the source/drain, separate discussions specific for each of the regions are necessary. In Figure 45, several key issues to deal with for a SALICIDE process are identified. They can be grouped into three main subject matters to consider with respect to their geometrical locations, *i.e.*,

1. *For the gate:* phase formation in small-dimension features such as narrow stripes of poly-Si gate and small areas of single-Si source/drain regions; morphological stabil-

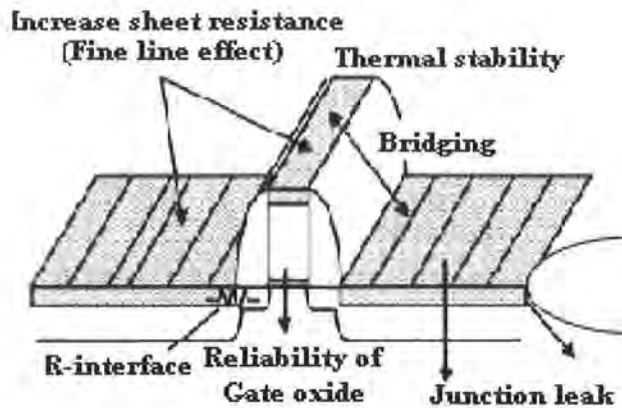


FIGURE 45. Main issues for a SALICIDE process. (Taken from Ref. 39. With permission.)

- ity of the silicide/poly-Si gate electrode stack; integrity of the SiO_2 gate dielectric beneath;
2. *For the source/drain:* contact resistance between the silicide and the source/drain terminals and junction integrity of the source/drain regions; and
3. *Between the gate and source/drain:* electrical shorts (bridging) between the gate and source/drain regions.

In the following, these various issues are addressed with respect to the different silicides used. The discussions of the material requirements from the device-performance perspective refers to Figures 1 and 45. Solutions pursued are discussed on the basis of thermodynamics and kinetics outlined in Chapter II. A unified approach satisfying the demands for both regions is crucial for the success of the SALICIDE technology. As silicon-germanium with different atomic compositions, that is, $\text{Si}_{1-x}\text{Ge}_x$ with different values of x , has emerged as a key technology for significant enhancements of Si device performance,^{320–322} solid-state interactions of Ti, Co, and Ni with $\text{Si}_{1-x}\text{Ge}_x$ will also be discussed, in a separate section at the end of this section. Particularly in a MOSFET, the $\text{Si}_{1-x}\text{Ge}_x$ can be present in the channel to enhance carrier (hole) mobility,^{323–327} in the gate as an extra means to control the threshold voltage,^{328–338} or in the source/drain to combat the high-resistivity issue.³³⁹

Among the three silicides discussed below, TiSi_2 is the most studied because it has been used widely for contact metallization in CMOS technologies. CoSi_2 begins to replace TiSi_2 in MOS devices of $0.25\text{-}\mu\text{m}$ gate length or below, due to the difficult formation of the low-resistivity C54 TiSi_2 in small features. Consequently, the number of publications on CoSi_2 has lately increased substantially. As the research around the formation of CoSi_2 deepens, more technological issues are revealed. Although great progresses have been made in the formation of CoSi_2 ,^{170,340} it is anticipated that NiSi will eventually take over for CMOS technologies with 100-nm gate length and below where the formation of CoSi_2 could become problematic. Because the actual gate lengths begin to deviate from (*i.e.*, become smaller) the corresponding CMOS technology nodes below, say, $0.25\text{ }\mu\text{m}$, the “gate lengths” cited here should rather refer to the technology nodes with the specified dimensions.

A. Gate Integrity

The various issues associated with the silicide formation on the poly-Si gate are discussed below. As the fine-line effect is one of the most serious concerns in the SALICIDE process, a detailed discussion about it is first presented. Agglomeration of the silicide/poly-Si layer stack,

and its influence on the integrity of the underlying ultrathin SiO₂ gate dielectric are then addressed.

1. Fine-Line Effect

“Fine-line” here refers to those small-dimension features, including narrow lines and small areas of Si. The three different silicides, TiSi₂, CoSi₂, and NiSi, are treated separately.

TiSi₂

The formation of TiSi₂ has been an important subject attracting a great deal of attention over the last 2 decennia, because of its wide use for contact metallization.⁴⁹ Therefore, studying its phase transformation from C49 to C54 bears both scientific importance and practical implications. The term “fine-line effect” is, in fact, mostly associated with the great difficulties encountered with the phase transformation in TiSi₂ in narrow lines or small-dimension features.^{272,273} The effect arises due to the facts that TiSi₂ may exist in two different phases,^{80,81} that is, C49 and C54, and that the growth of TiSi₂ usually begins with the formation of the metastable C49 phase and eventually ends with the formation of the stable C54 phase. In the SALICIDE process using Ti, a two-step annealing therefore is required as summarized in Table 2. After the first-step annealing at about 700°C, the C49 TiSi₂ forms in the three terminal regions gate, source, and grain. The second-step annealing at 850°C or above is an attempt to transform the high-resistivity C49 to the low-resistivity C54 TiSi₂. The C49–C54 phase transformation becomes increasingly difficult when the geometrical dimensions of narrow poly-Si lines in the gate and small single-crystal Si areas in source/drain decrease below 0.5 μm and 10 to 100 μm², respectively.^{272,273} Consequently, a significant increase in resistance with decreasing line/area dimensions is observed.^{36,39,272,273,311–314} Higher temperatures exceeding 900°C are then needed in order to fully convert the C49 to the C54 phases in the smaller-dimension features, which, however, can cause other problems as discussed later in this section.

It remains unclear why the formation of the C49 phase is favored compared with that of the

C54 phase. It has been suggested^{341,342} that the base-centered orthorhombic C49 structure has lower surface/interface energies than the face-centered orthorhombic C54 structure. The lower surface/interface energies can lead to an appreciably smaller $\Delta\sigma$ for the former, although the latter is thermally more stable with a slightly greater absolute value of Δg_v (see more below). As a result, the energy barrier for nucleation, ΔG^* in Eq. 2 becomes smaller for the C49 structure, according to the analysis in Section II.B. It has also been found³⁴³ that the mobility of Si, the DDS during the TiSi₂ formation (Table 3), is higher in the C49 structure than in the C54 one. Thus, the formation of the C49 phase should be favored according to the ordered-Cu₃Au rule discussed earlier in Section II.C. Theoretical calculations indicate³⁴⁴ that the C49 TiSi₂ displays a similar atomic structure to amorphous TiSi₂, compared with C54 TiSi₂. The measurements and calculations of the stiffness of TiSi₂ show³⁴⁵ that the C49 phase is much softer than the C54. These factors could also favor^{344,345} the nucleation of the C49 phase. The lattice of the two TiSi₂ phases is shown in Figure 46, while their physical properties are found in Tables 1 and 3. The two Ti-disilicides display different stacking sequences along their respective stacking directions: ABA along $\langle 001 \rangle$ for C49 and ABCDA along $\langle 010 \rangle$ for C54. In thin films, the C54 phase has the cell dimensions that are identical to those of the C54 TiSi₂ powder standard.³⁴⁶ However, the thin-film C49 TiSi₂ displays different cell dimensions from those tabulated in the JCPDS file for the C49 TiSi₂ powder standard.³⁴⁷ Rather, they assume those for TiSi_{1.9}Cu_{0.1}³⁴⁸ that are cited in Table 3, according to d’Heurle *et al.*⁸⁰ For information about the C49 structure in detail, the readers are referred to a thorough microscopic study on C49 ZrSi₂.³⁴⁹

The formation of the high-resistivity C49 phase of TiSi₂ usually occurs at about 300 to 600°C. The low-resistivity C54 phase forms as a result of polymorphic phase transformation at higher temperatures, typically around 700°C,^{49,350} on blanket substrates or in wide lines far exceeding 1 μm width and large areas far greater than 100 μm² dimension. The transformation (from C49 to C54) is, however, driven by a very small

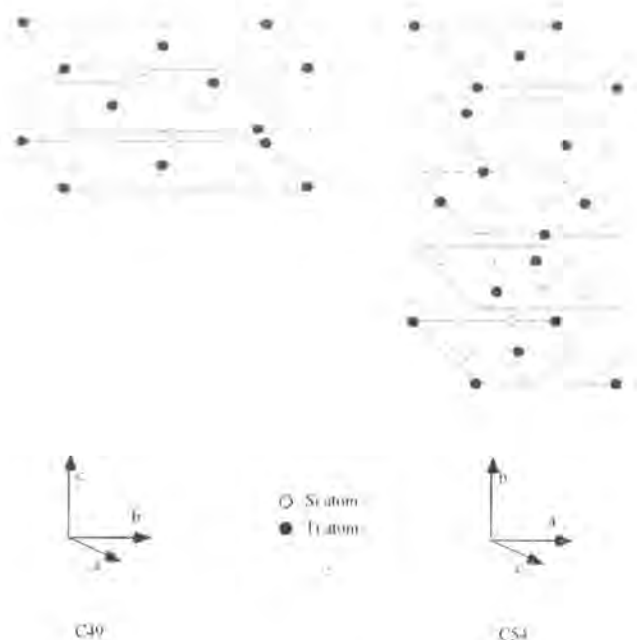


FIGURE 46. Crystal lattices for C49 and C54 TiSi_2 .

Δg amounting to 0.48 kJ/g atom.³⁵¹ (Note: Δg_v and Δg are not equal but closely related by a constant conversion factor.) Hence, ΔG^* becomes high and the transformation process is nucleation-controlled occurring in a very narrow temperature span. This behavior explains the existence of a critical temperature about 700°C for the formation of C54 TiSi_2 . Such a nucleation-controlled phase transformation therefore would preferably initiate at grain boundaries and/or grain junctions in the C49 TiSi_2 film at which the driving force for nucleating the C54 phase is maximized. Experimental evidence of the preferred nucleation of C54 TiSi_2 at the grain boundaries and/or grain junctions in the C49 TiSi_2 film has been provided by Ma *et al.*^{352–354} Hence, fine grain-size in the C49 film corresponding to a high density of grain boundaries and/or grain junctions should increase the probability of the nucleation of the C54 phase (see the schematic presentation of the process in Figure 47 beginning with two C49 TiSi_2 films with initially differently sized grains). While disconnected C54 TiSi_2 grains form in the C49 background for the case with larger C49 grains (left of Figure 47), a continuous conduction path through the C54 TiSi_2 grains is established for the case

with smaller C49 grains (right of Figure 47). This hypothesis is verified experimentally by Houtum *et al.*³⁵⁵ who have shown a lowered transformation temperature in C49 films of finer grain size, a phenomenon often referred to as a grain-size effect mechanism. Additionally, increasing thickness of the Ti layer, or rather of the C49 TiSi_2 film, has been found to lower the formation temperature for the C54 TiSi_2 ,^{341,352} which is suggested to result from a higher density of C54 nucleation centers in thicker films of C49 TiSi_2 .

Because the TiSi_2 films are usually thinner than 500 Å and the density of C54 TiSi_2 nuclei much smaller than $1/\mu\text{m}^2$,^{352–354,356} the C54 TiSi_2 crystals grown quickly extend through the film thickness and the growth of C54 TiSi_2 subsequently becomes lateral and two-dimensional. The observation of a difficult C49–C54 transformation in narrow Si lines^{272,311–314,357–359} is attributed to the low probability, and thus low density, of the C54 nucleation sites, and consequently to a change of the growth from two-dimensional to one-dimensional.^{272,358,359} A recent micro-Raman spectroscopy study reveals³⁶⁰ that the density of C54 nuclei in narrow lines only amounts to 0.03/cm². As schematically depicted in Figure 48, such a

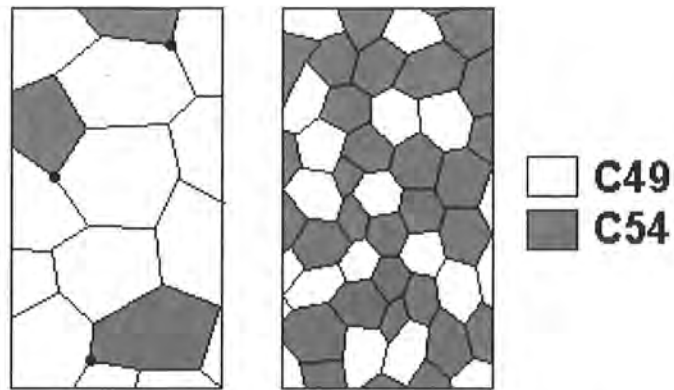


FIGURE 47. Schematic presentation of grain-size effects on the C49-C54 transformation.

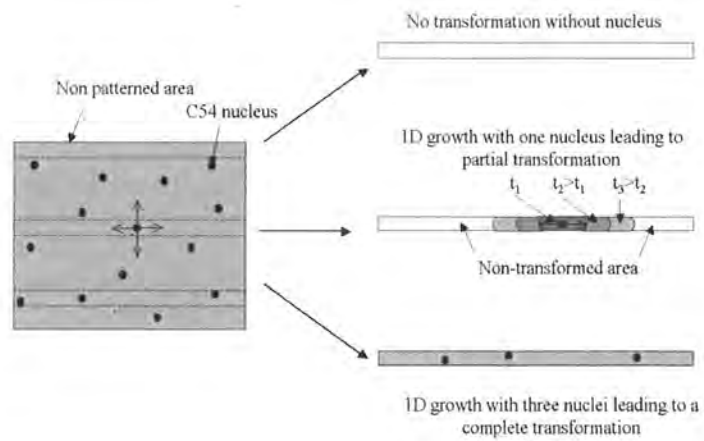


FIGURE 48. 2D vs. 1D growth of C54 TiSi_2 in a C49 background.

change in growth mode leads to a nonuniform transformation over different lines: the TiSi_2 remains in the C49 phase in one line (uppermost in the right column), is fully converted to the C54 phase in another line (lowest in the right column) and only partly transforms in yet a further line (middle in the right column). In a large-area C49 TiSi_2 film, the two-dimensional growth could lead to full transformation to the C54 phase (left). This nonuniformity has a serious consequence to the performance of a circuit because the RC time-constant varies from device to device. The ever-increasing difficulty in transforming TiSi_2 from the C49 to C54 phase in shrinking Si features, either by decreasing line width^{272,311–314,357–359} or by contracting area size,²⁷³ can be well accounted for with the grain-size effect mechanism discussed above. Because the low-resistivity C54 phase is desired in device applications, numerous means have been sought for to enhance the formation of C54 TiSi_2 by reducing its formation temperature. These methods include ion implantation or ion mixing,^{39,361–371} change of Ti sputter-deposition conditions,^{372–375} deposition of an ultrathin TiN interlayer between Ti and Si,³⁷⁶ and introduction of Ge into Si.³⁷⁷ While the first two methods are used aiming at reducing the grain size in the (precursor) C49 film in order to increase the density of grain boundaries and/or grain junctions, the last method with Ge incorporation is based on the work of Thomas *et al.*^{378–380} with a low formation temperature for C54 $\text{Ti}(\text{Si},\text{Ge})_2$ when compared with that for C54 TiSi_2 . Ion-implantation to amorphize the Si surface prior to Ti deposition is often referred to as preamorphization implantation, PAI. It has been found that ion-implantation into Si prior to Ti deposition gives rise to an appreciable effect in enhancing the C49–C54 transformation,^{361–371} while ion-implantation into deposited Ti is also effective but that into formed C49 TiSi_2 leads to no noticeable effect.³⁶⁵ PAI has been shown^{361–371} to enhance the formation of C54 TiSi_2 even in narrow lines down to 0.1 to 0.2 μm width. However, a worse agglomeration of the TiSi_2 formed in such narrow lines has been reported and seems to be closely related to the use of PAI.³⁷¹

It remains to be confirmed why preamorphization of Si can lead to an enhanced formation of C54

TiSi_2 . An amorphous layer mainly consisting of Si and Ti has been found at the interface between as-deposited Ti films and Si substrates using high-resolution TEM.³⁸¹ This amorphous layer thickens with increasing temperature up to 400 to 450°C without the crystallization of a silicide phase.^{140,381,382} It has been suggested³⁸³ that a thicker interfacial amorphous layer favors the formation of C54 TiSi_2 . It is, however, unclear how the temperature of C54 TiSi_2 formation can be lowered when a thicker interfacial amorphous layer is present, although it has been postulated³⁷² that in this case the precursor C49 TiSi_2 film would have finer grains leading to a higher density of nucleation sites for the C54 TiSi_2 . Experimental results show indeed that crystallization of the first Ti-silicide phase becomes easier with a thicker interfacial amorphous layer.³⁸² Apparently, the argument of smaller grains of the C49 TiSi_2 in thicker amorphous layers may only be valid when this particular structure indeed is the first crystalline phase to form. However, controversial results have been reported in the literature with respect to what is the first Ti-silicide phase to crystallize at the interface between Ti and Si (100): Ti_5Si_3 (or Ti_5Si_4) in Ref. 384, TiSi in Ref. 382 and C49 TiSi_2 in Ref. 381. Even more complex is that almost all the phases in the Ti-Si binary system (Figure 11) except C54 TiSi_2 were reported to simultaneously appear together with C49 TiSi_2 within the amorphous layer after annealing at 400 to 500°C.^{372,385} Thus, it is unlikely that the grain size of the C49 TiSi_2 is the only factor affecting the C49–C54 transformation, although a recent work reports that the grain-size in the C49 TiSi_2 film is smaller when it is formed on amorphous Si than on crystalline Si.³⁸⁶

Although appreciable improvements in enhancing the C49–C54 transformation have been shown with the PAI technique, a true breakthrough did not occur until Mann *et al.*³⁸⁷ used ion implantation of Mo and W into Si prior to Ti deposition. A high-temperature annealing was subsequently performed after the ion implantation. The temperature for the C49–C54 phase transformation is reduced by 100 to 150°C with ion-implantation of Mo into Si to a dose of 10^{13} to 10^{14} cm^{-2} , and it is especially effective for the C54 formation in Si narrow lines. Mouroux *et al.*^{388,389} used a different approach by depositing a 0.5- to 2-nm-thick Mo

at the Ti and Si interface. The formation of C54 TiSi₂ also occurs at a temperature 100 to 150°C lower than that needed for the usual C49–C54 transformation, and it is particularly effective for the formation of C54 TiSi₂ in narrow lines.³⁹⁰ A further approach was later demonstrated by Cabral *et al.*³⁹¹ in using Ti-alloys with Mo, Nb, and Ta. Once again, the C49–C54 phase transformation is substantially enhanced with a reduced temperature, especially in Si narrow lines. The three different approaches used to introduce the refractory metals into the Ti–Si system are summarized in Figure 49,¹¹⁵ where the schematic depth profiling of atomic concentration of the refractory metals is depicted. From a process point of view, ion implantation of refractory metals requires special arrangements of an implanter and standardization of such practice. In addition, the metal atoms are also implanted into the source/drain regions because the implantation is done after the gate stack is defined and the doping in the three electrode regions is made. Thus, there is a risk of the introduction of deep levels in the source/drain junctions that can lead to an increased junction leakage. On the other hand, reproducibly depositing a thin film of the order of 1–nm thickness is a demanding technological challenge to the day-to-day industrial production. Too thick a refractory-metal layer can lead to a much-reduced growth of C54 TiSi₂ via the diffusion of Si atoms through the interfacial layer containing refractory metals. Raising the formation temperature to promote the growth can cause other problems, which are discussed later. Therefore, the most practical method is that using Ti alloys. The fabrication of a standard sputtering target containing a few percents of the alloying metals has been a common practice for decennia, for example, Al with 0.5 at. % Cu and/or 1 at. % Si. However, the enhancement effects begin to fade away for the formation in narrow lines below 0.2 μm width when Ti–Ta alloys with up to 5.5 at. % Ta are used.³⁹¹ Adding more Ta (or Nb) may help enhance the formation of C54 TiSi₂ in narrower lines, but the cost of that is a substantial increase in resistivity of the silicide layer.³⁹¹

Finally, a thorough discussion of the mechanism(s) behind the enhanced formation of C54 TiSi₂ by the presence of refractory metals is

necessary. For ion-implantation, the enhancement effect was first attributed to pinning of the C49 TiSi₂ grains by Mo-bearing precipitates, thereby reducing the grain-size in the precursor C49 TiSi₂ film.³⁸⁷ For interposition, Mouroux *et al.* suggested^{388,389} a template mechanism for the enhancement effects. The template mechanism is described as follows. After annealing, an ultrathin layer of (Ti,Mo)Si₂ of the C40 structure readily forms at the Ti/Si interface. Direct growth of the C54 TiSi₂ on the C40 (Ti,Mo)Si₂, bypassing the C49 TiSi₂, can occur due to two facts: (1) the C40 (Ti,Mo)Si₂ and the C54 TiSi₂ share the same atomic arrangement and only differ in plane stacking, ABCA vs. ABCDA,^{115,392–394} and (2) the in-plane lattice mismatch between the stacking planes, *i.e.* the basal <001> planes of the C40 (Ti,Mo)Si₂ phase³⁹⁵ and the <010> planes of the C54 phase,³⁴⁶ is within 3%. For alloying, both mechanisms, that is, grain-size reduction due to pinning by refractory-metal-bearing precipitates and template phenomenon due to the formation of C40 crystals, could be at work simultaneously.³⁹¹ The epitaxial growth of C54 TiSi₂ on C40 (Ti,Mo)Si₂ has been confirmed using TEM.³⁹⁶ A cross-sectional TEM micrograph in Figure 50a reveals a layered structure with different phases and atomic compositions, after annealing a 440–Å Ti / 9–Å Mo bi-layer structure deposited on a Si(100) substrate. The electron diffraction pattern in Figure 50b shows the formation of C40 (Ti,Mo)Si₂ in the region marked “A” (Figure 50a). Analysis using EDS along this interfacial region gave (Ti+Mo)/Si=0.29–0.37 and Mo/Ti=0.04–0.23. In the region between “A” and “B”, the C54 TiSi₂ is found according to the diffraction pattern in Figure 50c, with Ti/Si=0.29–0.45 using EDS.

The reports of the substantial enhancement effects for the formation of C54 TiSi₂ have induced a large interest in the community aiming at further improvements and confirmation of the discussed mechanisms. It has been reported,³⁹⁷ based on a high-resolution TEM study, that MoSi₂ and an unknown silicide phase were present at the interface between C54 TiSi₂ and Si substrate when ion implantation was used. A good lattice match between both phases and the C54 TiSi₂ was shown to provide evidence of the operation of the template mechanism even for the ion-implantation

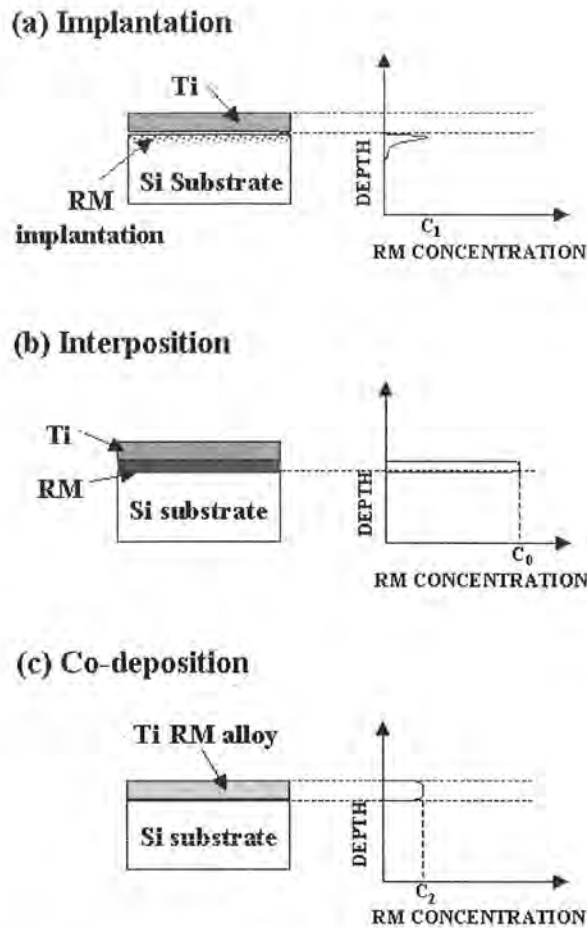
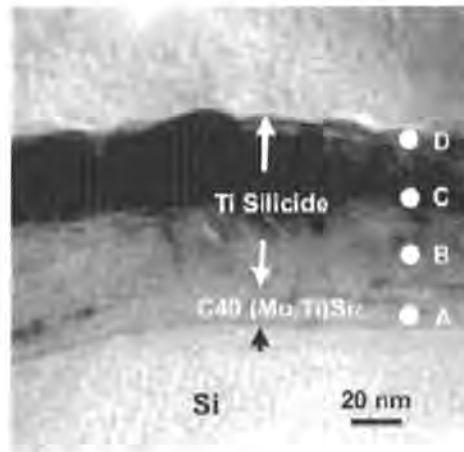


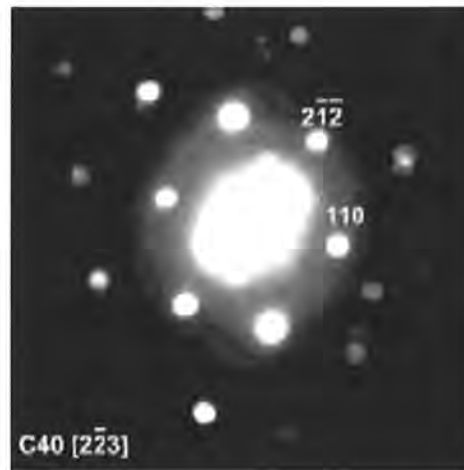
FIGURE 49. Three different ways to introduce refractory metal into the Ti-Si system.¹¹⁵

case. Indeed, one curiosity with the grain-size effect has been its preference in hindering the growth of one phase (C49) and promoting that of the other (C54); if the Mo-bearing precipitates at the interface would hinder the growth of the C49 phase, why did not they do the same to slow down the C54 TiSi_2 growth? This question is perhaps even more relevant for the alloying case where the concentration of refractory metals is much higher. In the alloying case, the enhanced formation of C54 TiSi_2 has been confirmed using Ti-Nb alloys with Nb up to 10 at. %^{398,399} or Ti-Ta alloy with 4 at. % Ta.⁴⁰⁰ (Because Ta, Nb, and Mo are quite identical for our discussions here, they are treated as one same metal.) Also, the temperature for the formation of C54 TiSi_2 decreases monotonically with increasing Nb concentration.^{391,399}

Further, the C49 TiSi_2 has also been consistently found prior to the formation of C54 TiSi_2 in samples with Nb up to 10 at. %.^{398,399} Based on these observations, it is tempting to conclude the grain-size effect as the major mechanism behind the enhancement effects and rule out the possible effect of template phenomenon. Why would just these few refractory metals and not any other additives promote the C54 TiSi_2 formation by pinning the C49 grains?³⁹⁹ Whether the template mechanism with the formation of C40 $(\text{Ti,Nb})\text{Si}_2$ is also at work in the Ti-alloys needs further investigation. There is, in fact, a different variant of the template mechanism suggested, which invokes the formation of $(\text{Ti,Ta})_5\text{Si}_3$ as the template for the C54 TiSi_2 in the alloying case.⁴⁰¹



(a)

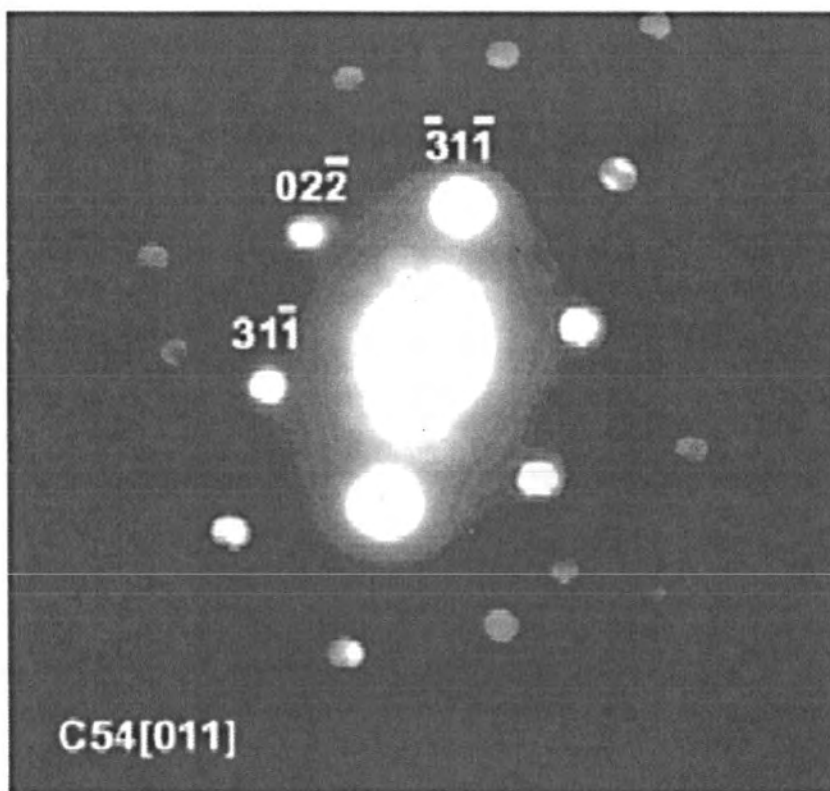


(b)

FIGURE 50. Cross-sectional TEM results showing (a) the layered structure, (b) a diffraction pattern for the C40 phase at region "A", and (c) a diffraction pattern for the C54 phase between region "A" and region "B", for a Ti/Mo/Si(100) sample annealed at 550°C for 30 minutes. (Taken from Ref. 396. With permission.)

A third mechanism for the enhanced formation of C54 TiSi_2 in the alloying case can be proposed, based on quantum mechanical calculations of how the electron-to-atom (e/a) ratio affects the relative stability in different TiSi_2 phases. The calculations indicate⁴⁰² that the stability of the C49 phase of TiSi_2 with respect to C54 is enhanced by a decrease in the e/a ratio. When this e/a ratio increases, the phase stability successively moves from C49 to C54, and then to C40 and finally to C11b structures. In Figure 51, the calcu-

lated energy curves⁴⁰² for the C49 and C40, with reference to the C54, are shown as a function of the e/a ratio (top). Also shown in Figure 51 is the relative (to C54) Fermi level for C49 and C40 (bottom). Experimental evidence for the shift of phase stability in TiSi_2 can also be found in several other Ti-Si systems with the addition of Al,⁴⁰³ Sc,⁴⁰⁴ or Sb,⁴⁰⁵ to yield $\text{Ti}(\text{Si},\text{Al})_2$, $(\text{Ti},\text{Sc})\text{Si}_2$ or $\text{Ti}(\text{Si},\text{Sb})_2$, respectively. For $\text{Ti}(\text{Si},\text{Al})_2$ with certain Al replacing Si and $(\text{Ti},\text{Sc})\text{Si}_2$ with certain Sc in place of Ti, a decrease in e/a results in a stabi-



(c)

FIGURE 50. (continued)

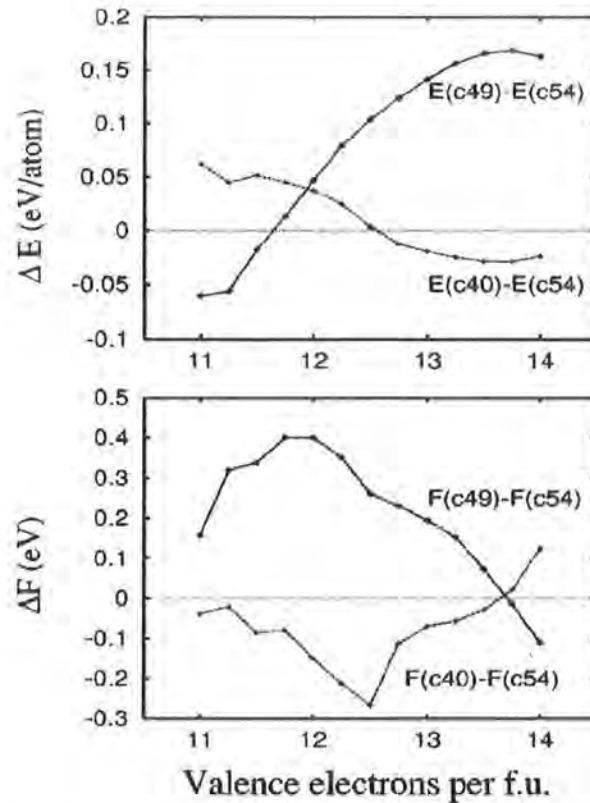


FIGURE 51. Top panel: differences in total energy between competing phases C49 and C40 both relative to C54 for increasing number of valence electrons. Bottom panel: corresponding variations in the relative positions of the Fermi-level F . (Taken from Ref. 402. With permission.)

lized C49 phase.^{403,404} For $\text{Ti}(\text{Si},\text{Sb})_2$ with certain Sb substituting Si, an increase in e/a gives rise to an enhanced formation of the C54 phase by reducing the formation temperature.⁴⁰⁵ Now, a plausible explanation for the enhanced formation of C54 TiSi_2 in Ti alloys is described as follows. After annealing, C49 TiSi_2 forms with the Nb dissolved on the metal site, that is, C49 $(\text{Ti},\text{Nb})\text{Si}_2$. The presence of the C49 structure has been revealed using *in situ* XRD.^{391,398,399} This C49 $(\text{Ti},\text{Nb})\text{Si}_2$ is, of course, unstable, precisely as C49 TiSi_2 . Its formation with a relatively low concentration of Nb can invoke a similar argument³⁴¹ of C49 $(\text{Ti},\text{Nb})\text{Si}_2$ having a lower surface/interface energy than C54, C40, or C11b $(\text{Ti},\text{Nb})\text{Si}_2$. Since Δg is greater between C49 and C54 $(\text{Ti},\text{Nb})\text{Si}_2$ than between C49 and C54 TiSi_2 according to the energy calculations in Figure 51, ΔG^* in Eq. 2 is reduced in the presence of Nb as the variation in $\Delta\sigma$ due to Nb should be negligible. Hence, the

formation temperature for C54 TiSi_2 (it should rather be C54 $(\text{Ti},\text{Nb})\text{Si}_2$ because C54 TiSi_2 can dissolve up to 10 at. % Nb on the metal site³⁹⁸) decreases.

An extended discussion of these different mechanisms can also be found in a recent review by Harper *et al.*⁴⁰⁶ However, a few words need be added about the template mechanism. It is known^{115,392-394,406} that in addition to the C40 (*i.e.*, NbSi_2 , TaSi_2 , VSi_2 , and CrSi_2 as well as ternary alloys $(\text{Ti},\text{Nb})\text{Si}_2$ ($\text{Ti},\text{Ta})\text{Si}_2$, $(\text{Ti},\text{Mo})\text{Si}_2$ and $(\text{Ti},\text{W})\text{Si}_2$ ⁴⁰⁷ with certain Ti/refractory-metal ratios) and C54 (*i.e.*, TiSi_2) structures, the C11b structure (*i.e.*, MoSi_2 and WSi_2) also shares the same atomic arrangement but differs in the plane stacking sequence, that is, ABA for C11b, ABCA for C40, and ABCDA for C54. Such great structural similarities among these three different phases are depicted schematically in Figure 52 and summarized in Table 4. In the top diagram of Figure 52, the in-plane lattice is shown

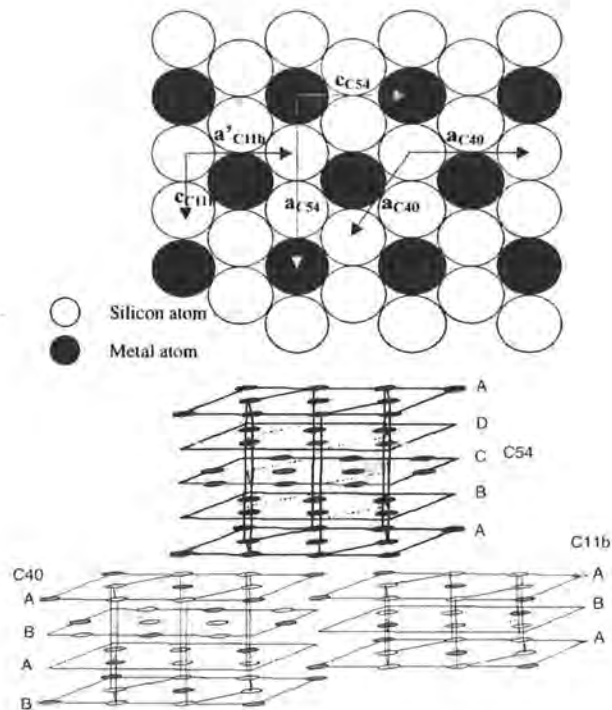


FIGURE 52. Top panel: two-dimensional atomic arrangements in the stacking plane for the C54, C40 and C11b. Bottom panel: corresponding layer stacking in three dimensions.

TABLE 4
Crystallographic Properties of the Refractory-Metal (RM) Silicides¹¹⁵

Silicide	Crystallographic structure	Angle between hexagonal axes in the stacking plane	Inter-atomic distance in the stacking plane (Å)	Distance between the stacking planes (Å)	Solubility limit of Ti in RMSi_2 at 1300 °C (at. %)
TiSi_2	C54	121°	2.76	2.138	-
VSi_2	C40	120°	2.64	2.124	85
NbSi_2	C40	120°	2.77	2.197	>75
TaSi_2	C40	120°	2.76	2.188	50
CrSi_2	C40	120°	2.56	2.121	88
MoSi_2 (metastable)	C40	120°	2.66	2.1416	80
MoSi_2	C11b	120°	2.61	2.27	0
WSi_2 (metastable)	C40	120°	2.66	2.138	60
WSi_2	C11b	120°	2.62	2.28	0

with the two-dimensional unit cells for the three structures. In the bottom diagram of Figure 52, the different stacking sequences are depicted for the structures. In Table 4, the three-dimensional cell dimensions are given for all C40, C54, and C11b disilicides, including those in discussion.¹¹⁵ To verify this mechanism, Ta⁴⁰⁸ or Nb⁴⁰⁹ were used in place of Mo as the interposed layer between Ti and Si. The consideration of Ta and Nb was based on the fact^{115,393} that both C40 TaSi₂⁴¹⁰ and C40 NbSi₂⁴¹¹ have an excellent in-plane lattice match to C54 TiSi₂ within 0.3 %, that is, 10 times better than C40 (Ti,Mo)Si₂. Experimental results indeed show^{408,409} an equivalent enhancement effect with a reduced formation temperature of the C54 TiSi₂ by about 100°C. A high-resolution TEM study⁴¹² not only confirmed the template effect induced by a Ta interlayer but further revealed for the first time an epitaxial growth of C40 TiSi₂ on C40 (Ti,Ta)Si₂ as well as the formation of C54 (Ti_{0.86}Ta_{0.14})Si₂. While C40 TiSi₂ had never been reported earlier, C54 (Ti_{0.86}Ta_{0.14})Si₂ with the specified atomic composition was not a stable phase. Their appearance was a result of epitaxial growth at low temperatures dictated by kinetics not thermal equilibrium.⁴¹² In addition to blanket films with Ti/Nb,²⁹⁷ high-resolution TEM has also been used to study the influence of an Nb interlayer on the silicide formation in small contact windows.⁴¹³ Only C40 (Ti,Nb)Si₂ is found in all contacts down to 0.5 μm by 0.5 μm size. Without Nb, only C54 TiSi₂ is found in blanket samples, both C54 and C49 are present in contacts of 5 μm by 5 μm size, and only C49 TiSi₂ is detected in contacts of 0.5 μm by 0.5 μm size. While the enhanced formation of C54 TiSi₂ in the presence of an interlayer of Mo,^{408,414-419} Ta,^{420,421} or Nb²⁹⁷ has been repeatedly confirmed, the validity of the template mechanism is still under debate. Ohmi and Tung⁴²² showed with an ultrathin layer of Mo disposed at different depth within the Ti film that the enhancement effect was at the maximum when the Mo was present at the interface between Ti and Si. It decreased when the Mo was placed away from the interface and became almost negligible when the Mo was on top of Ti. Zhang *et al.*^{396,423,424} later confirmed those observations. However, a detailed TEM study also reveals³⁹⁶ that the template

mechanism is still operative even with a surface Mo layer. A number of factors contribute to the difference in the enhancement effects, with the most important one being that the precursor phases for the C54 TiSi₂ are different. See Figure 53 for the summary of the TEM observations³⁹⁶ presented in a schematic form. Without Mo in the system, the formation Ti-silicides follows the usual phase sequence with Ti₅Si₃ as the first silicide product.^{384,416} The formation of C49 TiSi₂ occurs on the expenses of Ti₅Si₃, followed by the C49–C54 phase transformation. Typical temperature ranges for these phase formation steps are marked below each subdiagram. With an interposed layer of Mo (Figure 53b), C40 (Ti,Mo)Si₂ forms readily at the interface after annealing at relatively low temperatures. Then C54 TiSi₂ directly grows upward on the C40 layer due to the template phenomenon, on the expenses of Ti₅Si₃. With a surface Mo (Figure 53c), the entire Ti is first converted to C49 TiSi₂ preceded by the formation of Ti₅Si₃. Phase transformation in TiSi₂ does not occur until the surface layer containing Mo becomes C54 (Ti,Mo)Si₂. Apparently, the C54 (Ti,Mo)Si₂ forms at a lower temperature than needed for the usual C49–C54 phase transformation in pure TiSi₂ due to an increased driving force as discussed slightly earlier for the alloy case. Now, the C54 TiSi₂ grows downward on the expenses of C49 TiSi₂, at the same temperature as for the formation of C54 (Ti,Mo)Si₂.

A final, brief overview can now be given to the latest efforts with laser annealing to induce TiSi₂ formation. Chen *et al.* have reported⁴²⁵⁻⁴²⁸ that using excimer laser annealing with a laser beam of up to 5 mm by 10 mm size, C40 TiSi₂ can form directly without the addition of refractory metals, according to careful TEM and micro-Raman studies. Phase identification was made using convergent beam electron diffraction in combination with EDS. A typical diffraction pattern for C40 TiSi₂ induced by laser annealing is reproduced in Figure 54a, along with simulated patterns (along the C40 [0 to 1 0] zone axis) in 54b and 54c as well as the indexing results in 54d.⁴²⁶ Chen *et al.* have further shown⁴²⁶⁻⁴²⁸ the formation of C54 TiSi₂ at 600°C, 100 to 150°C below the temperature for C49–C54 transformation. Such an enhanced formation of C54 TiSi₂ is revealed by means of micro-Raman in Figure 55.^{426,427}

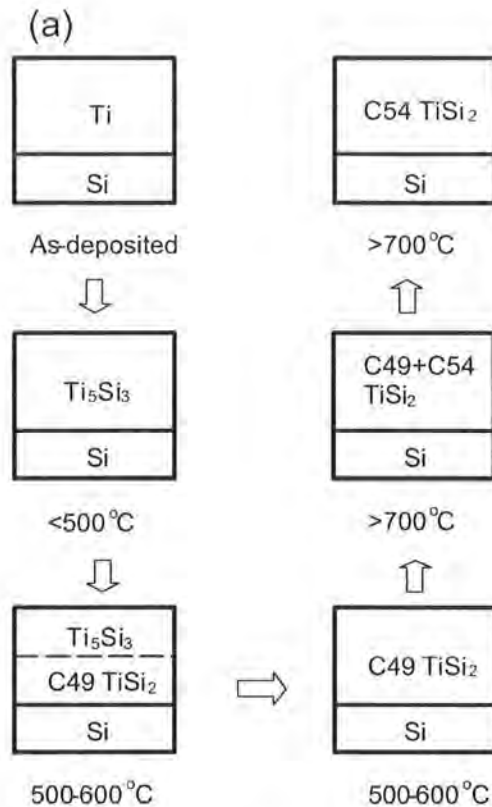


FIGURE 53. Schematic phase formation sequence to the formation of C54 TiSi_2 in samples (a) without Mo, (b) with an interfacial Mo layer, and (c) with a surface Mo layer. (Taken from Ref. 396. With permission.)

The enhanced formation of C54 TiSi_2 in narrow lines down to $0.25\ \mu\text{m}$ seems to outperform⁴²⁸ that obtained using Ti alloys.³⁹¹ Similar results of line-width independent TiSi_2 formation in narrow lines down to $0.18\ \mu\text{m}$ width, due to the use of laser-annealing, have also been reported by Verma *et al.*⁴²⁹ While the results of Chen *et al.* are implicative for device applications, one question arises: How does the rate of heating (orders of magnitude higher in laser-annealing than in ordinary RTP) influence the formation of the first phase in TiSi_2 , C49 vs. C40? Clearly, further studies are required to satisfy this academic curiosity. For practical device applications, laser systems capable of scanning over wafers of 300 mm in diameter are desirable.

CoSi_2

In the SALICIDE process using Co, a two-step annealing is also required,^{430,431} as shown in Table 2.

After the first step annealing at about 500°C , CoSi forms in the three terminal regions—gate, source, and drain. The second-step annealing above 700°C aims at transforming the high-resistivity CoSi to the low-resistivity CoSi_2 . The formation of CoSi_2 from interaction between CoSi and Si is, in general, much less problematic than the C49–C54 phase transformation in TiSi_2 , because no fine-line effect seems to be present for the CoSi_2 formation in narrow lines down to 100 nm width with careful control.^{39,340} Of more concern right now could be contaminations from gaseous impurities released during the temperature up-ramping in an RTP chamber.^{170,432} Therefore, the integration of the Co SALICIDE process in transistor fabrications could still be troubled with an unacceptably high sheet resistance in narrow gates below $0.2\text{-}\mu\text{m}$ width,^{433,434} and more elaborated means such as elevated gates need be sought.⁴³⁵

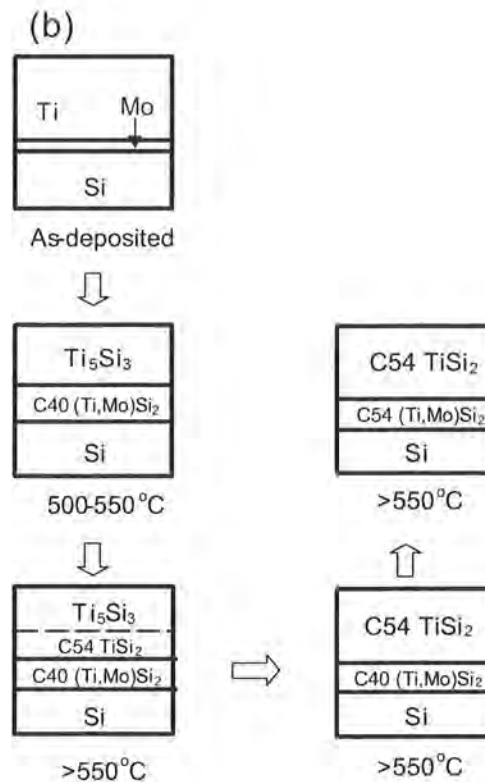


FIGURE 53. (continued)

From an academic viewpoint, the growth of CoSi_2 is characterized with a mixed kinetics and both nucleation and diffusion seem to affect the process.⁴³⁶ For this reason, the process is labeled “ill-behaving” because it lacks a clear kinetic behavior. The value of Δg for the formation of CoSi_2 from CoSi only amounts to about 1 kJ/g atom.⁴³⁷ Because this difference is within the limits of accuracy of any such thermodynamic values, it is not really known for certain what is its size. Nonetheless, a practical consequence of this academic inquiry is the following: while other factors such as the phase stability⁴³⁶ may cause CoSi_2 to nucleate relatively easily even in 100-nm-wide lines, as shown in Refs. 39 and 340, the extremely small driving force for the change from CoSi to CoSi_2 can eventually impose constraints, leading to a low density of CoSi_2 nuclei. Hence, the formation of CoSi_2 also becomes line-width dependent.

Recently, there has been intensive work aiming at improvements of the formation of CoSi_2 by

adding another metal in the Co-Si system; there exist at least two earlier articles about the interaction between Ni-Co and Si.^{438,439} Detavernier *et al.*⁴⁴⁰ and Lavoie *et al.*³¹⁹ show that adding Ni gives the desired benefits in reducing the formation temperature of CoSi_2 , or rather $(\text{Co,Ni})\text{Si}_2$ now. This effect is easily accounted for by considering the nucleation kinetics discussed in Section II.B. Sharing the same CaF_2 structure and almost the same lattice parameter, CoSi_2 and NiSi_2 are mutually completely soluble.^{57,441} At the same time, the monosilicides of Co and Ni have different crystallographic structures (Table 1), that is, cubic CoSi vs. orthorhombic NiSi , and are not miscible (at least not completely).⁴⁴² Hence, the formation of $(\text{Co,Ni})\text{Si}_2$ is now driven by a greater Δg with the entropy of mixing for the disilicides being added up, and thus a decreased ΔG^* in Eq. 2. Line-width independent formation of the $(\text{Co,Ni})\text{Si}_2$ has been demonstrated in narrow stripes down to 100 nm width, presumably with a re-

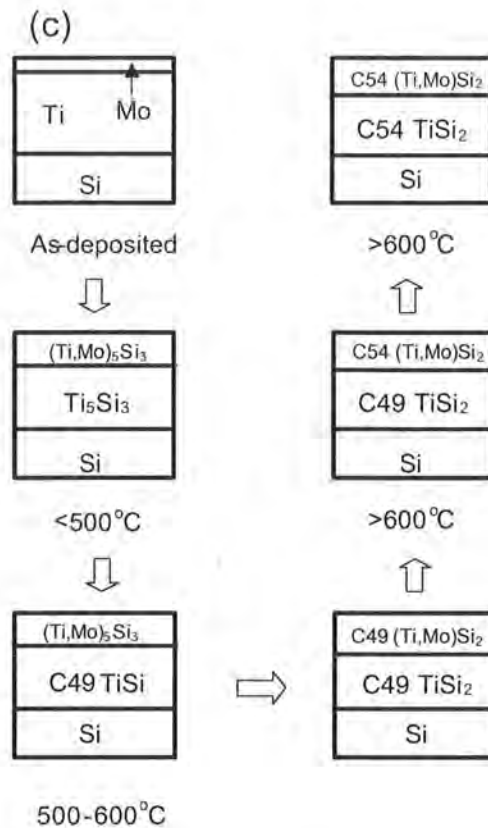


FIGURE 53. (continued)

duced temperature compared with that used for the CoSi_2 formation in similar stripes.³⁴⁰ Whether this decrease in ΔG^* also leads to a change in the kinetics of $(\text{Co,Ni})\text{Si}_2$ formation, for example, becoming more of a diffusion-controlled type, awaits experimental proof, but a very smooth interface has indeed been found between the $(\text{Co,Ni})\text{Si}_2$ and Si.^{340,443}

NiSi

The formation of NiSi in narrow lines is quite straightforward and independent of the line width^{36,39,340,444,445} because the growth of NiSi is diffusion controlled.^{57,101-103} The growth of NiSi occurs at rather low temperatures between 250 to 500°C , with a small activation energy of about 1.5 eV^{306,446-448} for the diffusion of Ni through NiSi. Even in narrow Si lines down to a 100 nm width, an annealing at 400°C for typically 30 seconds could complete the NiSi formation.⁴⁴⁴

Therefore, there is no need for a second step annealing as for the formation of C54 TiSi₂ or CoSi_2 (see Table 2). The fact that Ni is more mobile than Si during the formation of Ni-silicides⁹⁹⁻¹⁰³ even leads to a decrease in sheet resistance for narrow lines.^{39,340,444,445} In fact, similar observations of lower resistance in narrow lines have also been found for the CoSi_2 formation.^{39,340} The reproduction of such resistance results from Ref. 39 is shown in Figure 56 where the line-width dependence of gate sheet resistance for the three SALICIDE processes is given for comparison. Also shown are the results for Ti-SALICIDE with PAI as well as the PAI process (right sketch). The reason for such a "reversed" fine-line effect is simply the formation of thicker NiSi toward the two edges of a line than that in the middle, as revealed by TEM.^{39,444,445} In Figure 57, the influence of the DDS (upper diagrams) on the silicide formation in narrow Si lines is illustrated with a

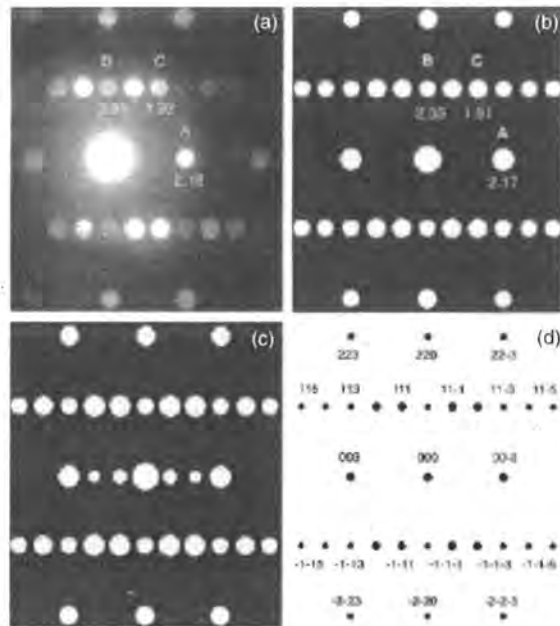


FIGURE 54. Formation of C40 TiSi_2 induced by laser annealing: (a) diffraction pattern, (b) and (c) simulated patterns along different zone axes of the C40 structure, and (d) corresponding indexing results. (Taken from Ref. 426. With permission.)

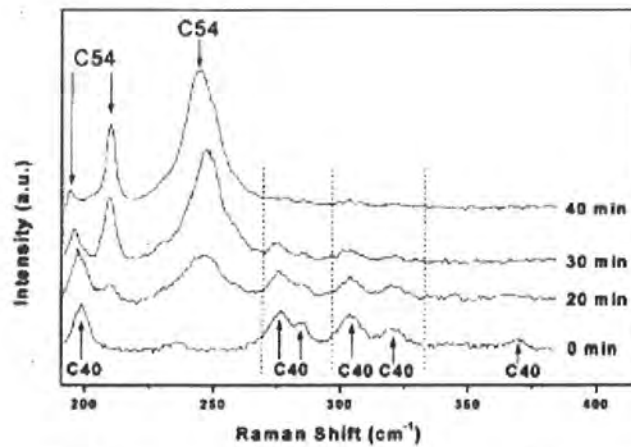


FIGURE 55. Micro-Raman data showing an enhanced formation of C54 TiSi_2 by C40 TiSi_2 induced by laser annealing. (Taken from Ref. 426. With permission.)

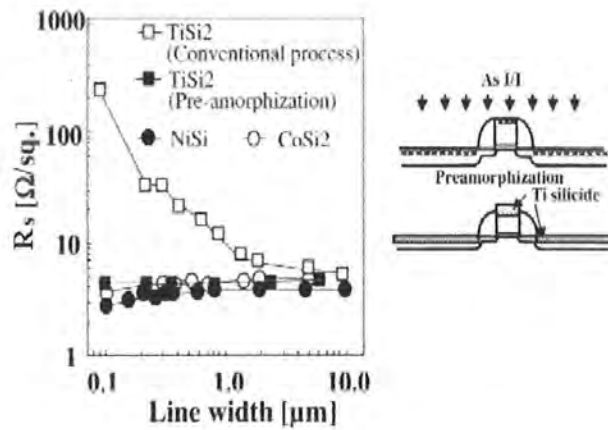


FIGURE 56. Dependence of sheet resistance on line width (left) for various silicide materials and processes. Preamorphization (right) is mainly for Ti-silicide process. (Taken from Ref. 39. With permission.)

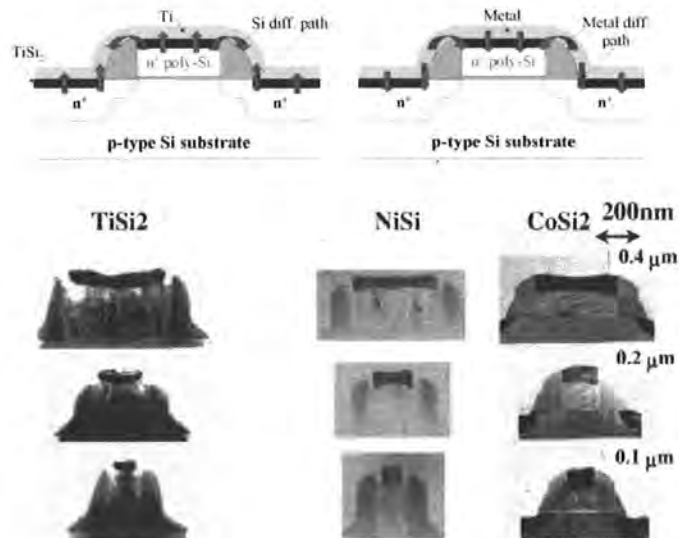


FIGURE 57. Illustration (top) of how the dominant diffusion species (DDS) affects silicide formation in narrow lines (bottom). (Taken from Ref. 39. With permission.)

comparison among the formation of TiSi_2 , CoSi_2 , and NiSi (lower diagrams).

Nucleation and growth of NiSi_2 is not desirable in the Ni-SALICIDE process, simply due to a threefold increase in specific resistivity when changing from NiSi to NiSi_2 (Table 3). (The change in sheet resistance of the silicide films is smaller as a result of a 1.7 times volume expansion from NiSi to NiSi_2 .⁴⁷) In addition, the growth of NiSi_2 from NiSi is nucleation-controlled typically yielding rough surface and interface,⁵⁷ which is detrimental to the junction integrity that is discussed later. The roughened surface/interface due to the nucleation-controlled formation of NiSi_2 recently has been nicely confirmed by combining *in situ* surface light scattering with *in situ* XRD.³¹⁸ The nucleation of NiSi_2 is also driven by an extremely small Δg of about 3 kJ/g atom.⁵⁷ Consequently, it does not occur below 700°C, leaving a relatively large temperature window for NiSi that already forms at 400°C by RTP.⁴⁴⁴ The difficulties with the NiSi_2 nucleation, as a result of a very low density of nuclei due to the small Δg , could also lead to the fine-line effect discussed extensively earlier for the phase transformation in TiSi_2 . Now, this fine-line effect should work *for* the phase stability of NiSi because it should push the formation of NiSi_2 to higher temperatures in narrower lines or smaller-dimension openings, precisely as in the case of the nucleation of C54 TiSi_2 . Such a positive effect has indeed been observed recently experimentally,⁴⁴⁹ although mechanical stress was discussed as the possible cause for the improved phase stability of the NiSi formed in narrow lines of 0.25- μm width. Usually agglomeration of NiSi films and layer-inversion already take place at 550 to 600°C, a temperature considerably lower than that for the formation of NiSi_2 .^{145,151,152,450} Hence, such a possible benefit due to the fine-line effect can be difficult to utilize unless the agglomeration issues are resolved.

2. Morphological Stability and Integrity of SiO_2 Gate Dielectric

Since the morphological stability of a silicide/poly-Si gate electrode stack has direct implications for the integrity of the underlying SiO_2

gate dielectric, these two issues are closely associated. The fundamental aspects of morphological stability are discussed in detail in Section II.G. An immediate concern is if the inversion of the silicide/poly-Si layer-stack occurs with the silicide in direct contact with the SiO_2 , the work function of the gate electrode can deviate from that of the heavily poly-Si. Work-function fluctuation was shown when an Al/poly-Si layer-stack was annealed.⁴⁵¹ The work function of the silicides is generally different from that of Si (Table 3). As a result, the precise work function of the gate electrode becomes dependent on the process details, including annealing temperature and time that in turn determine the degree of physical contact between silicide and SiO_2 (Figure 27). Although a direct contact between silicide and SiO_2 may not generate other reliability issues, mechanical stress induced by grain-growth in poly-Si as well as silicide can impose on the delicate SiO_2 layer that is becoming 2 nm thick in today's advanced devices.¹ Consequently, a breakdown of the SiO_2 occurs, which has actually been demonstrated by Karlin *et al.*¹⁴⁹ to take place in the CoSi_2 /poly-Si system on a 23-nm-thick SiO_2 . It has been reported that the crystallization of amorphous Si could induce a change in film stress from a relatively small compressive stress (200 MPa) to a large tensile stress (1000 MPa).^{452,453}

As mentioned earlier in Section II.G, the thermal stability of a silicide/poly-Si stack is mainly determined by the grain growth in the poly-Si, which in turn, is enhanced by the presence of the top silicide layer.^{150,151} A reproduction of the results of Hong *et al.*¹⁴⁵ is shown in Figure 58 to illustrate how the degradation of TiSi_2 , CoSi_2 , and NiSi , along with other silicides, on poly-Si substrates is varied with (a) the formation temperature and (b) the plastic deformation temperature of the silicides. It is clearly seen that the TiSi_2 /poly-Si is the most stable system among those studied. In Si narrow lines down to a 0.5 μm width, the edge-pinning of TiSi_2 to the sidewall of the SiO_2 spacers, as revealed by Norström *et al.*,⁴⁵⁴⁻⁴⁵⁷ occurs, making the TiSi_2 layer severely bow downward in the middle of the TiSi_2 /poly-Si gate, which could impose a high mechanical force on the underlying gate oxide and therefore affect its integrity. A thicker TiSi_2 layer on heavily P-doped poly-Si displays a

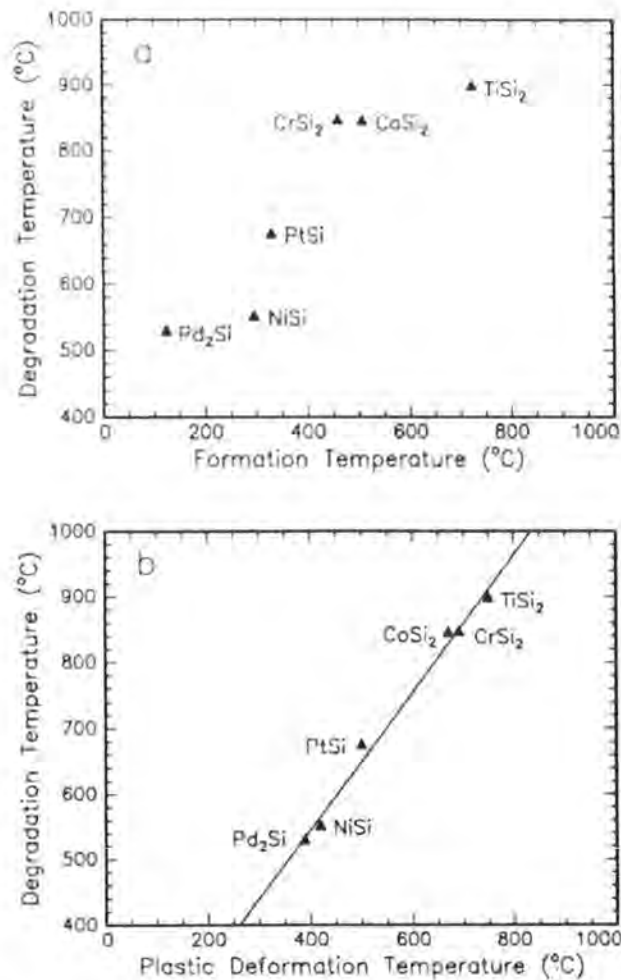


FIGURE 58. Silicide degradation temperature vs. (a) silicide formation temperature and (b) deformation temperature for six silicides. (Taken from Ref. 145. With permission.)

better morphological stability, while doubling the thickness of TiSi₂ on undoped poly-Si substrates shows no improvement.¹⁴³ The reason for this difference could be, as suggested by Karlin *et al.*,¹⁴³ due to a subtle difference in detailed mechanisms for the grain-growth in poly-Si; P is known to enhance the grain growth in poly-Si by increasing the Si self-diffusivity as a function of dopant concentration.⁴⁵⁸ With a sufficiently high P concentration in the poly-Si, the Si atoms no longer diffuse through the TiSi₂ layer but through the poly-Si for grain growth, thereby leaving the morphology of the TiSi₂/poly-Si layer-stack intact. Without P doping, the grain-growth in poly-Si necessarily pro-

ceeds via Si diffusion through the TiSi₂, hence causing the morphology to change (*i.e.*, deteriorate). In narrower lines, because the TiSi₂ formed becomes so thin, it is a barely continuous layer to begin with. A slight annealing can then cause the layer to agglomerate due to the capillary effect for coarsening of TiSi₂ thin films on single-crystal Si (Section II.G). Therefore, the difficult phase formation of TiSi₂ in narrow lines leads to^{39,272,311,444} a quickly worsened morphological stability and agglomeration of TiSi₂ occurs at a substantially reduced temperature.

Edge-pinning is also evident for CoSi₂ formed in Si lines down to 0.5 μm width.⁴⁵⁷ Now, the

pinning results in a CoSi_2 layer considerably thicker in the middle of the gate than toward the two edges, in addition to a downward bowing. This nonuniformity in CoSi_2 thickness not only leads to an increase in sheet resistance of narrow gates but also can become a factor deteriorating the morphological stability. In narrower lines, such a pinning phenomenon seems to be absent. Quite the contrary, a thicker CoSi_2 is shown toward the edge,³⁹ giving rise to the “reversed” fine-line effect as discussed earlier. A schematic presentation for such a reversed fine-line effect is shown in Figure 59; for the formation of CoSi_2 it actually originates from the dominant diffusion of Co during the formation of Co_2Si . As regard to the morphological stability for CoSi_2 /poly-Si layers, it is comparable to that for TiSi_2 /poly-Si as shown in Figure 58. In narrow Si lines, it is suggested⁴⁴⁹ that the grain growth in poly-Si should also become one-dimensional, thus much constrained when compared with that in blanket films, similar to the growth of C54 TiSi_2 in narrow lines, as depicted in Figure 48. Should this happen, the morphological stability for CoSi_2 /poly-Si layers would improve in narrow lines.

NiSi presents the poorest morphological stability among the silicides shown in Figure 58. However, if the grain growth in poly-Si is indeed much constrained in narrow lines, it should benefit the stability of NiSi/poly-Si layer-stacks. This improvement has been reported recently by Lee *et al.*⁴⁴⁹ with a continuous NiSi layer in 0.25- μm wide poly-Si lines up to 750°C. Working directly on the poly-Si films prior to the NiSi formation is an alternative approach for the improvement of the morphological stability. In the presence of NiSi precipitates, the rate of crystallization and epitaxial

regrowth of amorphous Si is increased by more than 300 times at 425°C.⁴⁵⁹ Making use of this phenomenon, Lee *et al.*⁴⁶⁰ recently show an improvement of the morphological stability of Ni(Pt)Si on poly-Si using NiSi₂ precipitates to first mediate and enhance the grain-growth in poly-Si. Using a stacked Si structure with various combinations of polycrystalline and amorphous Si layers, a stable NiSi up to 800°C has been reported.⁴⁶¹

The influence of silicide formation on dopant redistribution in the underlying Si will be discussed later when treating the junction and contact integrity. Observations of nano-scale voids at the silicide/poly-Si interface have been reported during the formation of TiSi_2 ⁴⁶² and CoSi_2 ⁴⁶³ in narrow poly-Si lines down to 0.13- μm width. As the voids are present only in the Si doped by ion implantation of BF_2 , their formation is clearly associated with fluorine or rather fluoride(s), although other potential causes such as mechanical stress have also been suggested.

The overall “thermal budget”, that is, temperature and time for thermal processing steps, for device fabrication has been greatly reduced in recent years,⁴⁶⁴ and is a result of technological advancements using, for instance, chemical-mechanical polishing instead of the traditional high-temperature reflow to planarize the wafer surface for the back-end processing such as inter-metal isolation. A low thermal budget relieves the pressure on the morphological stability issue.

B. Contact and Junction Integrity

The p-n junctions in the source/drain regions become more shallow in order to control short-



FIGURE 59. Schematics of the reversed fine-line effect for CoSi_2 (due to Co diffusion in Co_2Si) and NiSi formation.

channel effect (SCE) for MOSFETs with shorter gate-length.¹ In response to the dimensional down-scaling, a decreasing thermal budget is then required in order to minimize dopant diffusion in the source/drain regions.⁴⁶⁴ If not controlled, the doping profile in these regions can be modified thereby deteriorating the contact and junction integrity.

The two most influential parameters that determine the contact resistivity, ρ_c , are the surface (rather the interface) concentration of substrate doping, N_D , and the Schottky barrier height, Φ_{bs} , cf. Eq. 13. The ITRS prediction for maximum ρ_c in Figure 3 points to the requirement for contacts with a decreasing contact resistivity over time in an exponential manner. Such contacts are to be made in shallower junctions with higher doping concentrations in the source/drain regions, as inferred from Figure 4. To illustrate what these demands actually mean for the formation of contacting silicide films, two contact structures with simple rectangular geometries are shown in Figure 60. The technical parameters required for the 100-nm technology node¹ are given below as reference for further discussions:

- $R_{SD} = 180 \text{ } \Omega\text{-}\mu\text{m}$, parasitic source/drain resistance including R_{co} , R_{sh} , R_{sp} and R_{ac} (see Figure 6)
- $\rho_c = 2 \times 10^{-7} \text{ } \Omega\text{cm}^2$, contact resistivity between the silicide film and the source/drain regions
- $R_{silicide} = 6 \text{ } \Omega$ per square, silicide sheet resistance

- $t_{silicide} = 25 \text{ nm}$, for a maximum Si consumption of 24-nm thickness
- $x_{SD} = 50 \text{ nm}$, junction depth in the deep source/drain regions
- $x_{ext} = 30 \text{ nm}$, junction depth in the extension.

This set of data places clear quantitative demands on the properties of the silicide used, the interface morphology, and the electrical properties of the substrate.

1. Interface Roughness and Si Consumption

The structure with a planar contact in the left diagram of Figure 60 can be conceived using, for instance, the so-called elevated (or raised) source/drain technique⁵ that is discussed later in this section. Selective growth technique can be employed to deposit a sacrificial layer of Si in the source/drain regions prior to silicide formation. The structure in the right diagram of Figure 60 with a recessed silicide contact results from the ordinary SALICIDE process applied immediately after the gate definition. Now the formation of the silicide film consumes a considerable fraction of the Si in the junctions, making these junctions thinner and more vulnerable to any irregularity during silicide formation. For instance, junction leakage, detrimental to the device performance, may occur if silicide protrusions or spikes form penetrating through the junctions. High junction-

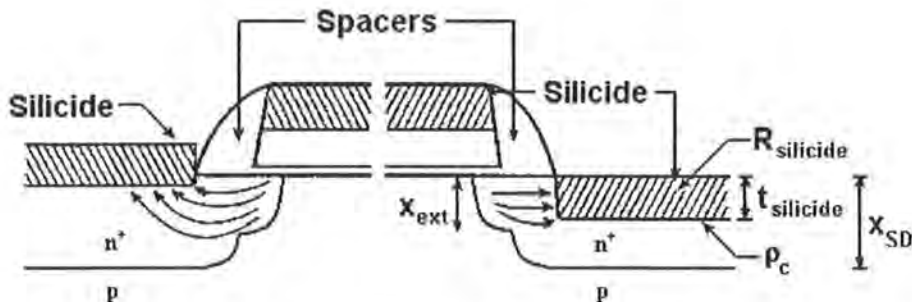


FIGURE 60. An ultra-scaled source/drain region with a planar silicide contact (left) and a recessed silicide with a step about half the junction depth (right).

leakage has been reported for CoSi_2 ^{465–468} or NiSi ^{469,470} contacted junctions. For the former contacts using Co-SALICIDE, CoSi_x ^{467,468} or CoSi_2 ⁴⁷¹ spikes penetrating through the junctions have indeed been identified. Thus, a flat interface between silicide and Si free from such irregularities is crucial for ultra-shallow junctions. From the viewpoint of silicide growth kinetics (Section II.B), the growth of both NiSi and its preceding Ni_2Si follows a diffusion controlled mechanism.^{57,101–103} The resultant surface and interface are smooth.^{57,318} The “ill-behaving” nature with the growth⁴³⁶ of CoSi_2 can lead to problematic, rough CoSi_2 surface, and/or CoSi_2/Si interface.³¹⁸ When Co-Ni alloys are used, a very smooth interface has been shown by Lauwers *et al.*,^{340,443} possibly resulting from a change in growth kinetics from the mixed nucleation-diffusion⁴³⁶ to a diffusion-controlled one. A recent study by Lavoie *et al.* reveals³¹⁸ that the formation of C54 TiSi_2 is also characterized with a rough surface/interface, most likely caused by the formation of C49 TiSi_2 from its precursor phase (TiSi_x) instead of during the C49–C54 phase transformation. The exact cause for the surface/interface roughening during the TiSi_2 formation remains to be confirmed, but the conclusion from the above analysis is quite clear: NiSi and $(\text{Co,Ni})\text{Si}_2$ are promising candidates for contacting ultra-shallow junctions in future generations of devices.

All the three silicides in discussion, that is, C54 TiSi_2 , CoSi_2 , and NiSi , are in possession of a specific resistivity (Table 3) that meets the above-listed requirements on sheet resistance and silicide thickness intended for the source/drain regions for the 100-nm technology node. As regards the Si consumption, the thickness of a silicide film formed and the corresponding Si consumption, normalized to the initial thickness of the metal films, are depicted in Figure 61 for Ti-, Co-, and Ni-silicides.⁴⁷ Arrows are shown below the desired silicide phases for electrical contact purposes. The graphical presentations in Figure 61 clearly indicate an added advantage with NiSi with its least Si consumption for a given silicide thickness. On the contrary, an obvious drawback with the formation of CoSi_2 is that the Si consumed is thicker than the silicide formed. A serious consequence of this excessive Si consump-

tion can be anticipated when CoSi_2 contacts are to form on even shallower junctions or on substrates where the Si supply is limited (*e.g.*, SOI).

For future CMOS technologies beyond the 100-nm node, the Si consumption due to silicide formation should be minimized further. Then, a silicide of lower specific resistivity is highly desirable because it is equivalent to a thinner film and thus a lower Si consumption at a given sheet resistance. It is apparent from the values in Table 3 that NiSi is the most attractive material with the lowest achievable thin-film resistivity ($10.5 \mu\Omega\text{cm}$) among the three silicides in question. Thus, the formation of NiSi should consume 30% less Si when compared with the formation of CoSi_2 and TiSi_2 for the same silicide sheet resistance.

2. Phase Formation and Morphological Stability

As shown above, as well as much more below, metal alloys as well as metal interlayers or capping layers are often used today to enhance the formation as well as the phase stability. The systems in question then become more complex because there are more species involved. It is important that the role of the metals used for alloying, interposition, or capping be analyzed as a part of the systems, not as separate elements. For ternary metal-metal-Si systems, a systematic discussion by Setton is available.⁴⁴¹ One can also find important information about such systems in Nicolet and Lau.³⁸

TiSi_2

The formation of TiSi_2 is strongly affected by the substrate doping, especially on n-type substrates usually caused by the presence of a thicker interfacial oxide because the dopants are known^{472,473} to enhance the oxidation rate of Si. The tendency of formation of Ti-dopant compounds^{83–85,169} at the TiSi_2/Si interface (Figure 14) is likely to contribute to the observed retardation of TiSi_2 formation. On heavily doped n-type Si substrates, thinner silicide films than on undoped Si have been obtained along with out-diffusion of dopants.^{169,474–480} Although a relatively less reduction in the TiSi_2 thickness is found on p-type

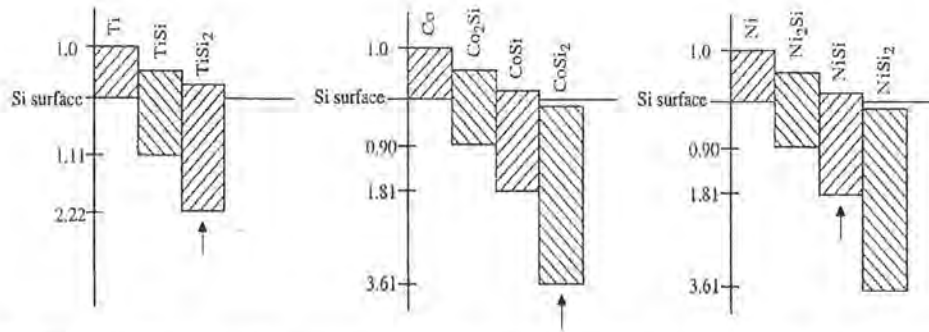


FIGURE 61. Silicide formation and Si consumption, normalized to the initial metal thickness, for the various silicide phases of Ti, Co and Ni, with the arrows pointing to the desired low-resistivity phase. (Taken from Ref. 47. With permission.)

substrates,⁴⁸¹ a different problem can arise for the substrates doped by ion implantation of BF_2 . Lur and Chen¹⁴⁰ have found cavities or voids at the TiSi_2/Si interface after TiSi_2 formation by reacting Ti films with BF_2 -implanted Si substrates. These cavities or voids are likely due to the formation of solid TiO_xF_y or SiO_xF_y that precipitate at the TiSi_2/Si interface at low formation temperatures. For instance, although TiF_3 remains as a solid up to 1300 K, its vapor pressure is high at considerably lower temperatures.⁷⁴⁻⁷⁶ Thus, when the temperature is raised, such compounds become volatile. Decomposition and out-diffusion of TiO_xF_y or SiO_xF_y leave behind cavities or voids at the interface. Poor electrical contacts with an increased contact resistivity are anticipated for the contact with such cavities and voids.

The formation of C54 TiSi_2 becomes difficult in source/drain regions of $100\text{-}\mu\text{m}^2$ area or below,²⁷³ as discussed extensively in Section IV.A, although the electrical contacts formed have been reported to be stable up to 1200°C .⁴⁸³ The introduction of refractory metals Mo, Nb, or Ta, through ion-implantation,³⁸⁷ alloying,³⁹¹ or thin-film interposition,^{388,408,409} or amorphization of Si prior to metal deposition, PAI,³⁶⁷ may provide a means to overcome this difficulty. With the interposition of Mo or Ta, a reduction of the interface roughness as well as an improvement of the morphological stability of C54 TiSi_2 layers have been found, at least on blanket Si (100) substrates.⁴¹⁵ The physical and chemical properties of Ta and Nb as well as their disilicides are, respectively, quite similar to those of Ti as well as TiSi_2 . As a result, when an Nb interlayer was used, no change in contact resistivity was

found on n-type substrates while a 2-4-fold lower contact resistivity than using pure TiSi_2 was obtained on p-type substrates.²⁹⁷

CoSi₂

A recent study indicates that the morphological stability is worse for the CoSi_2 formed in narrow lines when compared with that formed on blanket Si (100) substrates.⁴⁸⁴ The CoSi_2 films grown, via solid-state interaction between Co films and Si substrates, are polycrystalline. However, while the CoSi_2 grains are randomly oriented in the middle of the lines, they tend to grow epitaxially toward the edge of the narrow lines.⁴⁸⁵ Similar observations were found in another work;⁴⁸⁶ however, much thinner CoSi_2 layers were found toward the edge than in the middle of the narrow lines, similar to the observation in Ref. 170 (Figure 30). When properly controlled, larger CoSi_2 crystal grains are found in narrow lines of, for instance, $0.6\text{ }\mu\text{m}$ width than on blanket substrates. Consequently, the surface is rougher for the CoSi_2 layer formed in the narrow lines. Presumably, the interface roughness is also worse for the former case, but it could be difficult to quantify because in extreme cases single CoSi_2 grains extend transversely across the narrow lines. The interface is then primarily defined by the grain surfaces and edges of the CoSi_2 that are actually also present in wider lines. That a film with greater grains is less stable is actually consistent with the model of Nolan *et al.*¹⁴² and Miller *et al.*¹⁵⁶ In addition, the CoSi_2 formed in narrow lines are under a higher compressive mechanical stress than those formed on blanket substrates.^{46,487}

When a CoSi_2 film grows epitaxially on Si substrates, its morphological stability improves.^{154,155} Because it is epitaxially grown, the CoSi_2/Si interface is sharp. The epitaxy of CoSi_2 was achieved using a thin Ti interlayer deposited between Co and Si (100), a technique that was first reported by Yang and Bene.⁴⁸⁸ However, it was Wei *et al.*^{489,490} that pointed out the potential technical importance of the Ti-interlayer mediated epitaxy (TIME), which immediately sparked a great deal of interest both within and beyond the academic community. It was later shown that replacing Ti with Ta⁴⁹¹ or Zr⁴⁹² leads to CoSi_2 epitaxy as well. Alloying Co with W⁴⁹³ or C⁴⁹⁴ also induces the epitaxy of CoSi_2 . Later, a study of Tung⁴⁹⁵ reports that CoSi_2 can grow epitaxially when a deliberately grown SiO_x is present at the interface between Co and Si (100). Because this SiO_x layer can be grown using the standard chemical solutions for wafer cleaning, that is, $\text{HCl}:\text{H}_2\text{O}_2:\text{H}_2\text{O}$ or $\text{NH}_4\text{OH}:\text{H}_2\text{O}_2:\text{H}_2\text{O}$, the process of oxide-mediated epitaxy (OME) is technologically robust and thus has attracted a great deal of attention in the community. In view of the structural and geometrical similarities between CoSi_2 and Si, the epitaxial growth of CoSi_2 on Si is expected to be easy because $\Delta\sigma$ in Eq. 2 should be the minimum compared with any other configuration of the CoSi_2/Si interface. Unfortunately, however, this is not the case on Si (100) at least. Instead, polycrystalline CoSi_2 , dominated by components with (111) and (220) orientations, is grown when reacting Co films deposited on Si (100). The expected (200) and (400) reflections, characteristic of epitaxial alignment on Si(100), are almost invisible.⁴⁹⁶ Why should the presence of a Ti (or Ta or Zr) or SiO_x interlayer enhance the epitaxy of CoSi_2 on Si(100)? Numerous work^{154,155,491-524} have been devoted to studying the mechanism(s) of the epitaxy of CoSi_2 , using a Ti (or the like) interlayer, a SiO_x interlayer or a combination of a Ti-capping layer with a SiO_x interlayer. An analysis of the different mechanisms can be found in Ref. 525, where the effect of lattice-mismatch-induced strain on the nucleation of CoSi_2 is also discussed. As the strain energy amounts to less than 10% of Δg for the change from CoSi to CoSi_2 , the effect of lattice-mismatch strain is negligible. By successively reducing the rate of Co

deposition while holding the substrate temperature constant, Vantomme *et al.*^{526,527} show that the quality of CoSi_2 epitaxy steadily improves. A recent study of Detavernier *et al.*⁵²³ shows that in the presence of an inert Mo interlayer CoSi_2 can also grow epitaxially, similarly to the CoSi_2 epitaxy in the presence of a reactive Ti (or Ta, Nb, or Zr) interlayer. These observations, along with the success of OME as well as the detection of ternary Co-Ti-Si^{510,512} or quaternary Co-Ti-Si-O⁵⁰⁹ compounds, seem to suggest the reduction of Co flux as the prevailing factor that leads to the epitaxy of CoSi_2 .

A Ti capping-layer has been shown¹⁷⁰ to be effective in suppressing the detrimental influence of the impurities released from the surrounding SiO_2 isolation during annealing. The Ti capping layer has also been demonstrated^{514-516,520-522} to dissolve the interfacial SiO_2 between Co and Si and thus promote the CoSi_2 formation. The formation of CoSi_2 is generally less affected by the substrate doping compared with TiSi_2 , because Co is rather "inert" and the Co-dopant compound formation is less likely⁸³⁻⁸⁶ than the Ti-dopant compound formation (Figure 15 vs. Figure 14). However, the junction integrity is damaged resulting in a high junction leakage due to the formation of CoSi_x or CoSi_2 spikes.^{467,468,471} Although an epitaxial CoSi_2 layer presents attractive properties with an enhanced morphological stability and an improved CoSi_2/Si interface, voids have been found^{528,529} to form at the corner of a CoSi_2/Si contact in the vicinity of a SiO_2 or Si_3N_4 spacer leading to the channel of a MOSFET. Figure 62 shows TEM pictures of such a void formed after annealing at 850°C for 60 (a) and 90 min (b),⁵²⁹ which caused a drastically decreased drain current due to a substantial increase in source/drain series resistance. The void formation seems to be independent of how the Ti layer is disposed, at the interface between Co⁵²⁸ or on top of Co.⁵²⁹ Because voids of 100-nm size can form at typical RTP conditions, 900°C for 20 sec,⁵²⁸ adequate measures should be taken to suppress their formation.

It is anticipated that the approach with Co-Ni alloying^{319,340,440,443} to lower the formation temperature of CoSi_2 should also lead to an improved interface as a result of the change in growth kinet-

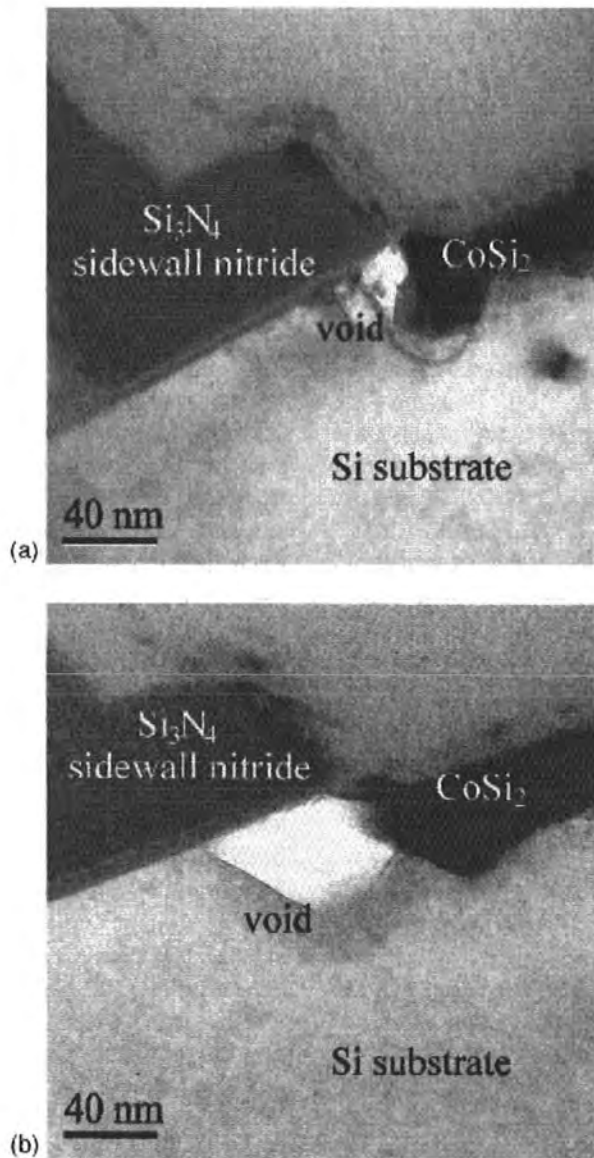


FIGURE 62. Cross-sectional TEM images taken along the $[110]$ direction showing voids generated at the edge of the sidewall spacer when the CoSi_2 formation is performed at 850°C for (a) 60 min and (b) 90 min. (Taken from Ref. 529. With permission.)

ics (see Section IV.A). That $(\text{Co,Ni})\text{Si}_2$ is more stable than CoSi_2 should also be beneficial to the morphological stability of the disilicide thin films on single-crystal Si. It is, however, expected that the specific resistivity of $(\text{Co,Ni})\text{Si}_2$ is higher than that of CoSi_2 due to two reasons: (1) alloy scattering and (2) the 2- to 3-fold higher specific resistivity of NiSi_2 than that of CoSi_2 (Table 3). The Si consumption for the formation of $(\text{Co,Ni})\text{Si}_2$ remains quite the same as that due to CoSi_2 (Figure 61).

NiSi

The use of NiSi for contact metallization shows a number of technological advantages among the three silicides of interest, that is, (1) its very low formation temperature, (2) its possession of the lowest achievable specific resistivity, (3) its smooth silicide/Si interface, and (4) its least Si consumption. Similar to CoSi_2 , the formation of NiSi is also rather insensitive to the substrate doping.⁴⁴⁵ However, NiSi has not been considered a serious candidate until recent, mainly due to its low morphological stability and the risk of the formation of the high-resistivity NiSi_2 .

A greatly enhanced phase stability of NiSi by alloying Ni with Pt has been reported by Mangelinck *et al.*^{449,460,530-536} The reasons behind the choice of the Ni-Pt alloy are twofold: (1) there is no disilicide of Pt,^{69,78,79} and (2) NiSi ⁵³⁷ and PtSi ⁵³⁸ share the same crystallographic structure and have rather close lattice parameters. Hence, a ternary alloy $(\text{Ni,Pt})\text{Si}$ with certain atomic compositions can form after annealing.^{449,460,531-536} This ternary phase obviously has a better phase stability than NiSi (or PtSi) due to the entropy of mixing between Ni and Pt, similar to the formation of $(\text{Co,Ni})\text{Si}_2$ with Co-Ni alloys, as discussed earlier.⁴⁴⁰ Because the solubility of Pt in NiSi_2 is low,⁵³⁰ the driving force for the formation of NiSi_2 from $(\text{Ni,Pt})\text{Si}$, that is, ΔG , in Eq. 2, is reduced, which results in an increased formation temperature for NiSi_2 . Note that the difference between the Ni-Pt alloying for the formation of Ni-silicides and the Co-Ni alloying for the formation of Co-silicides is that the entropy of mixing enhances the stability of the monosilicide in the former case, while it promotes the formation of the disilicide in the latter. Motivated by the success

with Ni-Pt alloys, Liu *et al.*⁵³⁹⁻⁵⁴¹ show that a Pt interlayer between Ni and Si yields similar effect in enhancing the phase stability of NiSi against the formation of NiSi_2 . An improved morphology stability has also been found,⁵³⁹ as expected.

It can certainly be expected adding Pd that sits in the same column as Ni and Pt in the periodic table should lead to similar beneficial effects in enhancing the phase and morphology stabilities of NiSi films. Here, no disilicide of Pd exists.^{69,78,79} PdSi ⁵⁴² also shares the same crystallographic structure and has close lattice parameters as NiSi. For more information about the Ni-Pd-Si ternary system, a phase diagram at 800°C is actually available.⁷⁰

Similar to the earlier discussions about Ti-alloying, it is more practical to employ a Ni-Pt or Ni-Pd alloy than to use an interlayer of Pt or Pd. Alloying with Pt or Pd can lead to an increase in specific resistivity due to alloy scattering and the variation of Schottky barrier heights due to different values¹⁷² of Φ_{bn} for PtSi (0.88 eV) and NiSi (0.65 eV). A change in Φ_{bn} changes the contact resistivity according to Eq. 13. Because the amounts of Pt or Pd needed are only about 5 at. % for appreciable beneficial effects,^{449,460,530-536} the changes in specific resistivity and Φ_{bn} are expected to be small.

With the consideration of potential difficulties in forming NiSi on patterned substrates, the use of a Ti capping-layer has been reported to yield a low leakage current.⁴⁷⁰ Such a capping layer has also been shown to reduce the interfacial oxide between Ni and Si⁵⁴³ in the same manner as for the Co-Si interaction under the influence of a Ti cap.^{514-516,520-522} For the metallurgical aspects of Ti on the Ni-Si interactions, one is referred to the work by Setton *et al.*^{441,544}

Three serious issues may arise with NiSi contacts:

1. Reliability of Ni-silicide contacted shallow junctions. With Ni or Ni_2Si contacts, Huang *et al.* have shown⁵⁴⁵ a strong polarity effect on failure at such contacts under high stress. In a pair of cathod and anode contacts, the Ni/ n^+ -Si contact pair failed at the anode and the Ni/ p^+ -Si pairs failed at the cathod. The Ni/ $\text{Ni}_2\text{Si}/n^+$ -Si and Ni/ $\text{Ni}_2\text{Si}/p^+$ -Si failed prefer-

entially at the cathod. Three different mechanisms were discussed as the likely causes for such failures: wear-out, electromigration enhanced silicide formation, and electron-hole recombination. For NiSi contacts, similar failures have not yet been reported.

2. Effect of contact size on phase formation. It was reported⁵⁴⁶ when the size of square contacts on Si (111) substrates decreased from 1.8 to 1 and then to 0.8 μm , the temperature for the formation of (epitaxial) NiSi₂ increased from 550 to 800 and then to 850°C. The results seem to indicate the operation of the fine-line effect discussed earlier in Section IV.A. However, a more recent publication of the same group showed⁵⁴⁷ when the contact size was further decreased below 0.6 μm , epitaxial NiSi₂ was found already at 400°C. The enhanced formation of epitaxial NiSi₂ at such a low temperature was attributed to the stress build-up around the contacts. The results in Refs. 546 and 547 suggest a risk of nonuniform phase formation in contacts of different sizes: NiSi in large openings and NiSi₂ in ultrasmall ones.
3. Effect of initial Ni film thickness on phase formation. With a starting Ni film thickness of 12-nm, NiSi₂ was found as the first silicide phase to form at 300 to 400°C according to *in situ* TEM.⁵⁴⁸ Hence, it did not follow the usual sequence of phase formation, Ni₂Si $\rightarrow$ NiSi $\rightarrow$ NiSi₂, with thicker Ni films. Furthermore, NiSi_x pretrusions in the form of upside-down pyramids of up to 30-nm height were found to penetrate into the patterned Si substrate after annealing at 150°C. The silicide protrusions were identified as NiSi₂.⁵⁴⁸ Figure 63a shows a cross-sectional TEM picture of such pyramids formed after annealing the Ni/patterned-Si structure at 150°C for 1 h. An interfacial oxide is clearly observable as a bright horizontal line immediately above the pyramids. Without the annealing, no NiSi₂ pretrusion is found in Figure 63b. The formation of NiSi₂ pyramids at such a low temperature seems to be related to the presence of the interfacial oxide as well as to the thickness of the Ni film.⁵⁴⁸ Similar observations of

CoSi₂ pyramids at 400°C skipping the formation of Co₂Si and CoSi have also been reported in the Co-Si system with a Ti interlayer.⁵⁴⁹ A risk with such pyramids if not suppressed is the formation of leaky junctions. Indeed, a higher density of leakage currents is found for both p⁺-n (marked "p-type") and n⁺-p diodes (marked "n-type") in Figure 64 for those formed with a 10-nm-thick Ni than with a 40-nm Ni. Apparently, adequate steps should be taken to suppress the formation of such pretrusions in order to eliminate the thus-caused junction leakage.

3. Dopant Diffusion and Use of Silicides for Dopant Incorporation

After the gate definition by dry etching, the conventional process sequence for fabricating MOSFETs is to first dope the source/drain regions along with the gate by ion implantation. When a high-temperature annealing is carried out for removal of implantation-induced damage, dopant activation and diffusion, the device structure looks like that in Figure 8a without the Ti layer. The SALICIDE process is then performed as depicted in Figures 8b through 8d. This process sequence is now detailed in Figure 65 for Ti- or Co-SALICIDE. A low thermal budget for the dopant activation and SALICIDE processing is crucial for retaining the device structure, including dopant profiles in the source/drains regions.⁵⁵⁰ Any excessive heat treatment or surface reaction can lead to undesirable dopant diffusion and redistribution. An important physical phenomenon associated with silicide formation is that the diffusion of dopants in the Si substrates can be affected. The diffusion of dopants is mediated by two kinds of point defects in Si: interstitials and vacancies.⁵⁵¹ The diffusion of B and P is mainly mediated by interstitials, while that of As and Sb by vacancies. Several studies show⁵⁵²⁻⁵⁵⁸ that the formation of silicide at the Si surface injects point defects and thereby influence the behavior of dopant diffusion. The latest results confirm^{557,558} that the point defects injected are mainly vacancies, giving rise to vacancy supersaturation and interstitial depletion. As a result, the diffusion of

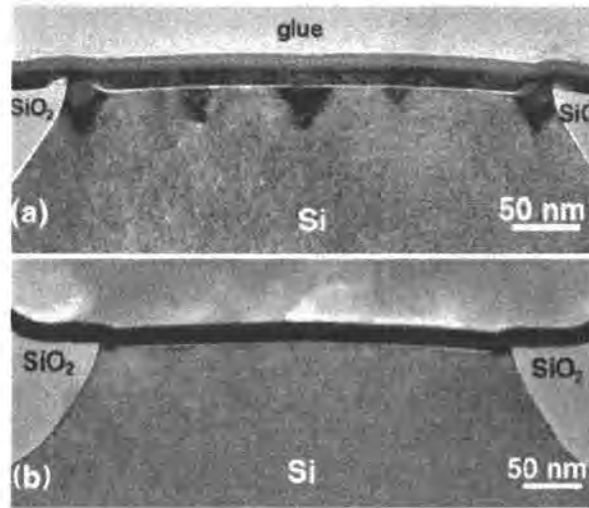


FIGURE 63. Formation of NiSi_2 pretrusions in Si (100) upon annealing at 150°C for 1 hour of 12 nm thick Ni layer (a), and similar interface area free of such pretrusions without heating (b). (Taken from Ref. 548. With permission.)

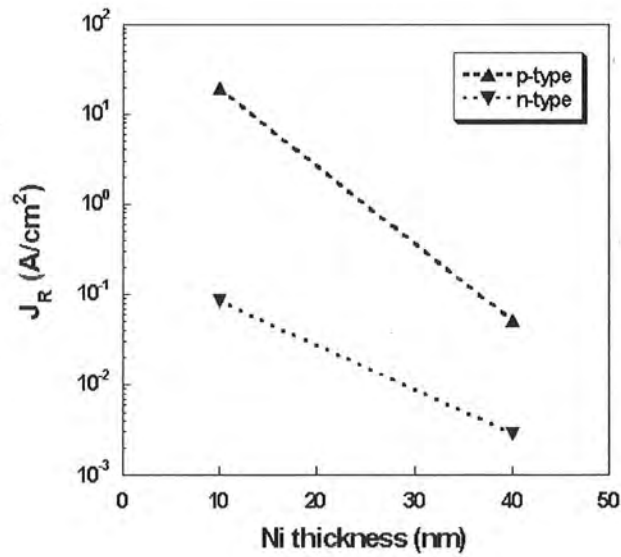


FIGURE 64. Leakage current density for diodes contacted with NiSi of different Ni thicknesses. In the figure, p-type means p^+ -n diodes and n-type n^+ -p diodes.

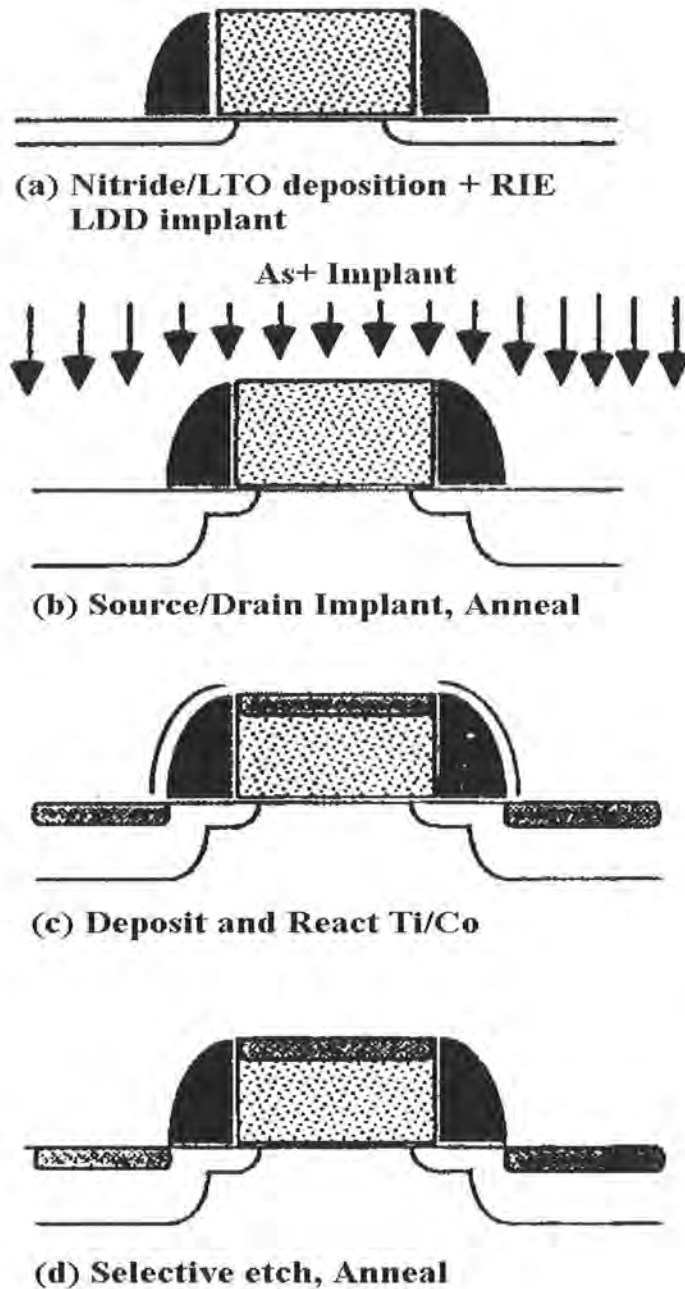


FIGURE 65. Conventional SALICED process for an nMOSFET. (Taken from Ref. 5. With permission.)

B and P is retarded and that of As and Sb enhanced. Therefore, it is necessary to be aware of the potential effects of silicide formation on dopant diffusion and redistribution in the ultrashallow junctions in the source/drain regions when the SALICIDE process is implemented.

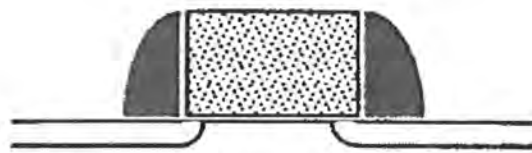
An alternative process to the conventional one is to reverse the procedure by first applying the SALICIDE process. Dopants are then implanted into the silicide layers without damaging the Si substrate. An appropriate annealing step is employed to drive the dopants out of the silicide layers into the underlying Si.⁵⁵⁰ This process, called "Silicide As Diffusion Sources" — SADS and depicted in Figure 66 — presents a number of attractive features such as the formation of ultrashallow junctions that follow the silicide/Si interface morphology, thereby reducing the junction leakage.^{546,560} Choosing an appropriate silicide can lead to a reduced thermal budget compared with that for the conventional process. A very detailed, systematic investigation of SADS with all the silicides of current interest, PtSi, NiSi, CoSi₂, and TiSi₂, has been carried out by Jiang *et al.*^{561–563} Similar information can also be found in Ref. 564. Examples of a more recent attempt with the SADS concept can be found in Refs. 565 and 566.

As shown in Figure 14, phase formation between the dopants and Ti can occur;^{83–85} hence, TiSi₂ may not be an efficient doping source for the SADS process and limitations of diffusing B and As from TiSi₂ have indeed been shown.⁵⁶⁷ More focus of the SADS process therefore has been placed on CoSi₂. Information about the dopant (B, P, and As) diffusion in implanted TiSi₂ thin films can be found in two studies by Gas *et al.*⁵⁶⁸ and Probst *et al.*,⁸⁵ while similar information but about B, Ga, Ge, P, As, and Sb in CoSi₂ thin films is available in two other diffusion studies by Thomas *et al.*⁵⁶⁹ and Probst *et al.*⁸⁶ Grain boundary diffusion predominates the redistribution of the dopants after annealing.^{568,569} These results are also summarized along with other diffusion data in the two lengthy compilations of Gas and d'Heurle.^{103,117} There is certainly more recent work on dopant diffusion, activation, and redistribution during silicide formation (for instance, Ref. 570).

The diffusion of dopants along the grain boundaries, vertical as well as lateral ones,⁵⁶⁸ in silicide thin films of polycrystalline nature is very rapid, which can be helpful for the SADS process to yield a uniform doping of the Si substrate. In CMOS technology using dual gates, that is, n⁺ poly-Si gate for the n-channel MOS device and p⁺ poly-Si gate for the p-channel MOS device (Figure 1), the two poly-Si gates are interconnected using the same silicide film for current shunt. This rapid dopant diffusion inside polycrystalline silicide films thus can lead to a serious problem of counterdoping in the gates and thus instability of the work function of the gates.⁵⁷¹ For the lateral diffusion of B, P, and As in WSi₂, TiSi₂, and CoSi₂ thin films, kinetic parameters for diffusion as well as important guidelines for layout design of CMOS devices, in terms of the minimum distance between the two types of gates, are available in the literature.^{572–574}

When epitaxial CoSi₂ films are used for the SADS process,⁵ lattice diffusion of dopants in single-crystal CoSi₂ should be considered. Information about the lattice diffusion as well as the solid solubility of B in CoSi₂ can be found in Zaring *et al.*^{575–577} The results of lattice diffusion and solid solubility of As in CoSi₂ are found in Cardenas *et al.*^{578–580} and Mangelinck *et al.*⁵⁸¹ They are also available in Refs. 103 and 117.

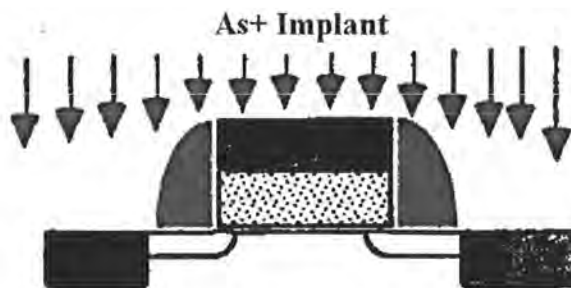
The electrical activation of a dopant is generally limited by its solid solubility in Si. Within the temperature range usually used for dopant activation, that is, below 1000°C, the solubility increases with increasing temperature.⁵⁸² (A retrograde temperature behavior of the solubility is evident at high temperatures.) Thus, a relatively high temperature is required to achieve a high level of dopant activation in Si in order to minimize R_{co} and R_{sh} in Figure 6. The low-temperature formation and morphology stabilities of NiSi can then prevent it from being considered a viable candidate for the SADS process. Whether the enhanced stability of NiSi by Pt addition could pave the way for the NiSi SADS process remains to be confirmed. This leaves CoSi₂ as the most promising candidate.



(a) Nitride/LTO deposition + RIE
LDD implant



(b) Deposit and React Ti/Co



(c) Selective etch, Anneal
As+ Implant



(d) Dopant drive-in anneal

FIGURE 66. Silicide as a diffusion source (SADS) process for an nMOSFET. (Taken from Ref. 5. With permission.)

4. Control of Contact Resistivity

For TiSi_2 and CoSi_2 contacts formed using SALICIDE or SADS, Probst *et al.*⁸⁵ have shown a strong concentration-dependent behavior of the contact resistivity. The minimum value obtained was slightly above $10^{-7} \Omega\text{cm}^2$ on the Si doped by B to $1.8 \times 10^{20} \text{ cm}^{-3}$ and by As to $3 \times 10^{20} \text{ cm}^{-3}$. These concentration values of B and As refer to the interface region as determined by SIMS. For TiSi_2 contacts formed using SALICIDE, Åberg *et al.*²⁹⁷ have also revealed a strong concentration-dependency on uniformly doped poly-Si layers. They obtained $3 \times 10^{-8} \Omega\text{cm}^2$ on the Si doped by As to $5 \times 10^{20} \text{ cm}^{-3}$ and $0.9\text{--}1.5 \times 10^{-6} \Omega\text{cm}^2$ by B to $1\text{--}5 \times 10^{20} \text{ cm}^{-3}$. These concentration values were chemical ones determined with information about the poly-Si film thickness and implantation dose. Also a strong function of doping concentration, a somewhat lower contact resistance was shown for NiSi contacts than TiSi_2 ones to both n- and p-type poly-Si.⁵⁸³ Recently, Tsuchiya *et al.* have reported⁵⁸⁴ low values of 4.2×10^{-8} and $7.0 \times 10^{-8} \Omega\text{cm}^2$ for NiSi contacts on n- and p-type Si, respectively, both formed at 350°C .

With the conventional device-making procedure using ion implantation followed by dopant

activation with furnace annealing or RTP, the substrate doping concentration usually displays a graded depth profile, that is, the concentration is the highest at the Si surface and decreases when advancing into the interior of the Si substrate, see Figure 67a for a schematic depth profile of a very graded junction beside a MOSFET structure. The SALICIDE process results in silicide contacts with a recessed feature, as shown in the right diagram of Figure 60, due to Si consumption and silicide growth. Consequently, an increase in contact resistivity can occur for a silicide contact on such a graded junction in the source/drain regions, because the contact resistivity is determined by the actual doping concentration at the silicide/Si interface (Figure 67a). An ideal box-shaped doping profile as schematically depicted in Figure 67b therefore is desired to avoid contact resistivity degradation. A recent theoretical study of Kim *et al.*^{585–587} shows a great advantage of using such a box-shaped doping profile for the reduction of the various resistance components as well as the overall parasitic source/drain resistance.

Inasmuch as the doping concentration at the silicide/Si interface plays a vital role in determining the contact resistivity, raising the doping concentration in combination with controlling the

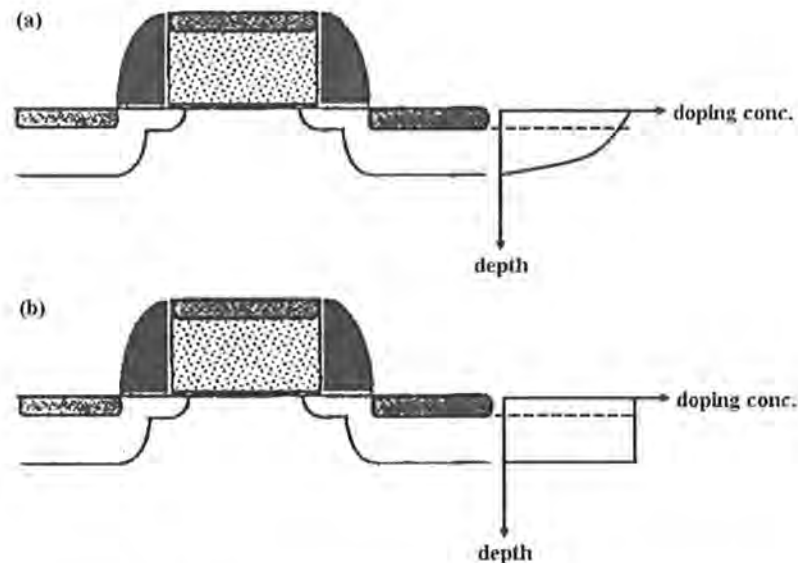


FIGURE 67. A very graded doping profile (a) and an ideal box-shaped doping (b), with a silicide layer placed to show how the actual interface concentration changes.

doping profile⁵⁸⁵⁻⁵⁸⁷ presents a viable solution for the reduction of contact resistivity. The idea of doping profile engineering has now been implemented by Kim *et al.*⁵⁸⁸ using the emerging laser-annealing technique; a nearly ideal box-shaped doping profile within 30 to 40 nm depth is obtained for both As and B doped junctions. Preamorphization using Ge implantation seems to be crucial for achieving the desired box-shaped junctions. Success with laser annealing for the fabrication of ultrashallow junctions has also been reported by Yu *et al.*⁵⁸⁹ In addition to the progress in forming the low-resistivity C54 TiSi₂ using laser-annealing,^{475-479,590} an extremely low contact resistivity of $4 \times 10^{-8} \Omega\text{cm}^2$ on B doped single-crystal Si has been shown by Goto *et al.*⁵⁹¹ with an unspecified silicide. Such a low contact resistivity is mainly due to the result of a supersaturation doping: the activated doping concentration was reported to be 10^{21} cm^{-3} , almost 10 times the highest solubility value of B in Si.⁵⁸² A rough estimate of the Si layer of Goto *et al.* gave a specific resistivity value of 0.1 to 0.2 m Ωcm , corresponding quite well with what one could extrapolate from the standard resistivity-concentration curve for p-type Si.⁵⁹² What one is concerned with laser annealing are the consequences of an inherently inhomogeneous processing within one microsecond, such as distortion and degradation of ultrafine structures like the gate.

Simultaneous supersaturation doping and ideal box-shaped doping profile can also be achieved using selective growth by means of CVD. This approach has been validated recently and demonstrated by Gannavaram and Öztürk.³³⁹ Because it also involves SiGe alloys, more discussion of the work in Ref. 339 is given in next section when the interaction between SiGe alloys and metals is presented.

How the silicide thickness and the junction depth in the source/drain regions should simultaneously scale along with the gate-length has been outlined in ITRS¹ (see Figure 4). Such scaling trends place high demands on the control of silicide formation, interface morphology, morphological stability of the silicide film, influence of the silicide formation on dopant diffusion, etc. By elevating the source/drain regions through selective deposition techniques such as CVD,^{593,594} the

demand for decreasing the junction depth can be separated from that for forming a uniform, low-resistivity silicide film in order to maintain the contact and junction integrity. Now, the formation of silicide consumes the sacrificial Si layer grown by selective CVD instead of the precious Si in the original Si source/drain regions. However, use of the elevated source/drain scheme is not entirely problem free. An immediate concern with the elevated source/drain scheme is the risk of forming a silicide bridge over the two spacers on the two sides of the poly-Si gate, because the physical distance between the gate and source/drain regions is reduced by the source/drain elevation. This point is clarified later when discussing issues for electrical short between the gate and source/drain electrodes. What is to be assessed below is how elevating the source/drain could influence the value of R_{co} in Figure 6. With reference to the list of technical data for the 100-nm technology node at the beginning of this section as well as to the simple contact structures in Figure 60, we further assume $\rho_{SD}=10^{-3} \Omega\text{cm}$ as the specific resistivity of the Si in the source/drain regions. This value for ρ_{SD} is chosen because it coincides almost perfectly with the resistivity for a p-type single-crystal Si⁵⁹² doped to 10^{20} cm^{-3} , that is, the solid solubility of B in Si.⁵⁸²

A comparison between the two idealized contact structures with rectangular geometries in Figure 60 indicates that the assumption of a planar contact for Eq. 18 based on the contact geometry in the left diagram of Figure 60 is no longer valid for the recessed contact in the right diagram of Figure 60. Hence, different equations are used for the estimations. For the contact in the right diagram of Figure 60, if the current is assumed to uniformly flow into the contact from its vertical side, $R_{co} = \frac{\rho_c}{t_{\text{silicide}} W} = 800 \Omega$ for a 1- μm -wide

contact ($W=1 \mu\text{m}$), *i.e.*, $R_{co}=800 \Omega\text{-}\mu\text{m}$ far exceeding the allowed limit of $R_{SD}=180 \Omega\text{-}\mu\text{m}$. Of course, this simple estimate gives the result for the most severe case, and the current flowing into the bottom of the silicide/Si contact certainly reduces the value of R_{co} substantially. Nonetheless, a change of the contact geometry to the planar type in the left diagram of Figure 60, by depositing the sacrificial Si layer to the desired

thickness for silicide formation, can lead to a much-reduced contact resistance. Using Eq. 18a

$$\text{for } L_c \gg L_T = 0.32 \mu\text{m}, R_{co} = \frac{\rho_c}{L_T W} = 63 \Omega \text{ for } W = 1$$

μm . For the last calculation, Eq. 17, $L_T = \sqrt{\frac{\rho_c}{R_s}}$,

was used with $R_s = \frac{\rho_{SD}}{x_{SD}} = 200 \Omega$. Now, a decrease

in x_{SD} is possible to make even shallower junctions. If it is reduced from 50 to 25 nm,

$$R_{co} = \frac{\rho_c}{L_T W} = 90 \Omega, \text{ when other parameters remain}$$

unchanged. However, one should bear in mind that R_{SD} represents the total sum of R_{co} , R_{sh} , R_{sp} and R_{ac} in Figure 6. Thus, even the value of 63 Ω is an appreciable part of the total allowable parasitic series resistance of $R_{SD} = 180 \Omega\text{-}\mu\text{m}$ because there are, in fact, two such contacts from the source end to the drain end. A further reduction of ρ_c is the most effective means to bring R_{co} down and therefore desired.

As shown above, supersaturation doping can lead to an extremely low ρ_c in the low- $10^{-8} \Omega\text{cm}^2$. A 10-fold reduction of ρ_c directly leads to a 10-fold decrease in R_{co} , to 80 $\Omega\text{-}\mu\text{m}$ for the recessed contact and 6.3 $\Omega\text{-}\mu\text{m}$ for the planar one if R_s is also reduced by a factor of 10 due to supersaturation doping. From the viewpoint of achieving a supersaturation doping, the SADS process may not be viable because the active doping concentration at the silicide/Si interface is now limited by the solid solubility at the annealing temperature. For the p-type doping using B, this limit is low, only amounting to 10^{20} cm^{-3} . The SIMS results in Refs. 85, 86, and 561–564 for the SADS processes indeed show an interfacial concentration of B around this level. Hence, using SALICIDE on preformed supersaturation doped Si can be more practical and attractive for contact metallization. However, it should be remembered that supersaturation doped Si presents a nonequilibrium condition. Any thermal processing thereafter, including SALICIDE, tends to force it to resume the equilibrium state with the concentration of the electrically active dopants approaching the solid solubility limit. For this reason, a low thermal budget SALICIDE process is highly preferred, and that with NiSi is certainly the most promising candidate for this aspect.

C. Bridging between Gate and Source/Drain Over the Gate Spacers

Electrical short between the gate and source/drain regions, that is, bridging, is a serious reliability issue. As the gate-length becomes shorter, it is necessary, following the scaling rule, that the junctions in the source/drain areas become shallower for SCE control. Because the ion implantation into the gate and source/drain regions is carried out simultaneously for CMOS processing, the height of the poly-Si gate needs to be reduced to allow the incorporation of dopants at the poly-Si/SiO₂ interface. Otherwise, a serious gate depletion will occur, hence degrading the current drivability, unless other measures are taken to resolve the gate depletion issue. However, a reduced height of the poly-Si gate is also necessary for process control in particular for dry-etching to define the poly-Si gate on an extremely thin SiO₂ gate dielectric, as mentioned earlier for the POLYCID structure. Furthermore, the width of the SiO₂ (or Si₃N₄) spacers on the two sides of the poly-Si gate (Figure 1) should also be down-scaled to reduce the source/drain series resistances. Such geometrical changes in the gate structure result in a very short physical distance between the gate and source/drain regions. Thus, the control of bridging over the spacers becomes an increasingly important issue for the SALICIDE processing.

Bridging problems for the Ti-based SALICIDE have been studied in numerous publications. Severe bridging occurs mainly because of (1) lateral diffusion of Si and (2) Ti-spacer interaction. During the formation of Ti-silicides, Si is the DDS (Table 3). Lateral diffusion of Si atoms can lead to the growth of Ti-silicide over the spacers forming electrical paths between the gate and source/drain. The Ti-SiO₂ (or Ti-Si₃N₄) interactions^{91–95,595} also lead to the Ti-silicide formation on the spacers (Figure 16). A two-step annealing with the first step at relatively low temperatures, thus Table 2 is used to overcome the problem. In addition, silicide formation in N₂ has been found to be an effective means to suppress both processes (lateral diffusion of Si and Ti-spacer interaction).^{49,95,274,596} The yield of bridging free test structures increases when N₂ is used, compared with that when using Ar.^{597–599} However, two reactions in competition are taking

place when annealed in N_2 : silicide formation at the Ti/Si interface and nitridation of Ti at the Ti surface. High-temperature anneals promote the formation of $TiSi_2$, while low-temperature ones favor the formation of TiN .⁹² It then becomes rather trivial to fine-tune the process parameters, including the thickness of the initial Ti film and the annealing details in order to grow a sufficiently thick $TiSi_2$. When the distance between the gate and source/drain is shorter, such a fine-tuning becomes a more demanding proposition.

The bridging is generally less severe in the Co-based SALICIDE process, with a larger process window for high yield and low sheet resistance than for the Ti-base SALICIDE.⁴⁹ The main reason for bridging to occur in the Co-based SALICIDE process as well is that Si is the DDS during the $CoSi$ formation (Table 3). Thus, similar to the Ti-SALICIDE process, lateral diffusion of Si atoms can lead to the growth of Co-silicide over the spacers. As the formation of $CoSi$ occurs at a considerably lower temperature than $C49 TiSi_2$, the Si diffusion causing lateral silicide growth is much less pronounced. A further decrease in formation temperature of the first-step annealing below $500^\circ C$ can lead to an elimination of bridging.⁴³⁰ However, interaction between Co and the spacer materials, either SiO_2 or Si_3N_4 , could be a concern. In accordance to the phase diagram in Figure 17, a severe reaction between Co and SiO_2 has been clearly demonstrated to occur during RTP at $800^\circ C$ in N_2 leaving behind Co_3O_4 in SiO_2 grooves.⁶⁰⁰ An interaction between Co and Si_3N_4 already occurs $600^\circ C$ and the formation of $CoSi_2$ and CoN becomes evident at $800^\circ C$.⁶⁰¹ At an even higher temperature of $1050^\circ C$, epitaxially grown $CoSi_2$ spikes are detected under a 100-nm-thick Si_3N_4 .⁶⁰² Although the temperatures at which such severe interactions occur are typically much higher than that used for the first-step RTP (Table 2), less pronounced effects could become more important for smaller devices with thinner spacers. In the presence of a Ti capping layer on Co to improve the $CoSi_2$ formation, the SiO_2 spacers can be affected due to the interaction between Ti and SiO_2 .^{514-516,520-522} When Si_3N_4 is used as the spacer isolation, it can be attacked by the metal layers forming a complex layered structure TiO_2/TiO /

unreacted $Co/(Ti,Co)_2N/Co_2Si/Si_3N_4$ after annealing at a quite low temperature of $660^\circ C$ for 120 sec.⁶⁰³

Because Ni is the DDS during the formation of all Ni-silicides,^{99-103,117} bridging is not an issue in the Ni-based SALICIDE process. This special feature makes the Ni-based SALICIDE process especially attractive for future devices with an extremely short distance between the gate and source/drain regions. In particular, when the elevated source/drain scheme is implemented to combat SCE as well as to improve the contact and junction integrity of ultrashallow junctions in the source/drain regions, the Ni-based SALICIDE process is, among the three silicides in discussion, the most promising contact formation technique. A summary of how the DDS influences the bridging is schematically shown in Figure 68; bridging can take place during the formation of $TiSi_2$ and $CoSi$ (a) and it is much less likely during the formation of Co_2Si and Ni-silicides (b). Inasmuch as the formation of $CoSi_2$ usually necessarily proceeds after $CoSi$ is formed, bridging is determined by the Si diffusion during the $CoSi$ formation. It should be noted that the Ti atoms are also mobile during the formation of Ti-silicides, although much less so than the Si atoms. Similarly, the Si atoms also move during the formation of Ni-silicides, but less rapidly than the Ni atoms.

Finally, an attempt is shown in Table 5 to summarize how the various physical, geometrical, and processing parameters influence the process temperature-window for the three different SALICIDE processes. A process temperature-window is defined as the temperature interval from the temperature for silicide formation to the highest allowable temperature for the integrity of junctions and/or silicide morphology. In combination with the processing data in Table 2, one sees a clear trend of the shift from $TiSi_2$ to $CoSi_2$ and to $NiSi$ for the SALICIDE process as the integration technology evolves with the availability of a decreasing thermal budget processing.

D. Incorporation of $Si_{1-x}Ge_x$

Silicon and Ge form nearly ideal binary solid solutions.^{604,605} The binary solution $Si_{1-x}Ge_x$ is

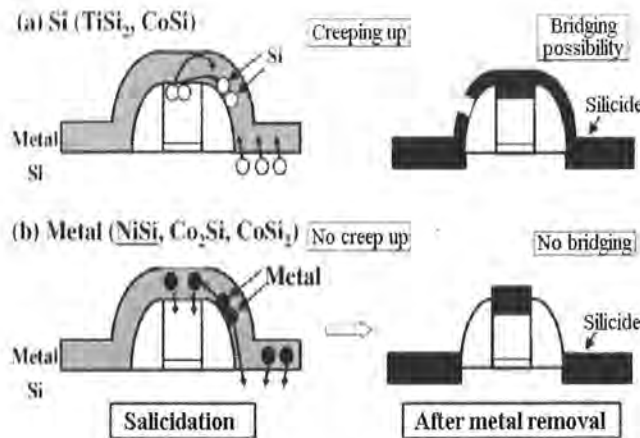


FIGURE 68. Illustration of how DDS affects bridging in different SALICIDE processes, (a) Si diffusion and (b) metal diffusion. (Taken from Ref. 39. With permission.)

TABLE 5

Variation of the Minimum Temperature for the Formation of Silicides and the Upper Temperature Limit for the Integrity of Junction and Morphology Due to Technology Developments (i.e., Smaller Geometrical Dimensions and Lower Processing Temperature). “+” and “-” in Parentheses Under the Last Three Columns Indicate Advantages and Drawbacks, Respectively, Associated with the Indicated Changes

Issues	C54 TiSi ₂	CoSi ₂	NiSi
Overall formation temperature	High (-)	Medium (-)	Low (+)
Formation temperature due to decrease in line-width and/area size	Increase (-)	Little effect (+)	No effect (+)
Formation temperature due to increase in doping-level in Si	Increase (-)	No effect (+)	No effect (+)
Risk of bridging due to decrease in gate-to-source/drain distance	Increase (-)	Increase (-)	No effect (+)
Risk of agglomeration due to increased formation temperature	Increase (-)	Irrelevant (+)	Irrelevant (+)
Degradation of shallow junction due to increased formation temperature	Yes (-)	Irrelevant (+)	Irrelevant (+)
Dopant deactivation and redistribution in Si upon silicide formation	Most likely (-)	Possible (-)	Least probable (+)
Temperature for agglomeration of silicide film	High (+)	High (+)	Low (-)
Formation temperature due to alloying with appropriate metal(s)	Decrease (+)	Decrease (+)	Little effect?
Risk of agglomeration on single-crystal Si due to alloying	Decrease (+)	Decrease (+)	Decrease (+)
Use in contact metallization scheme for future generations of devices	Poor candidate	Fair candidate	Good candidate

single-crystal in the channel^{323–327} and polycrystalline on the gate^{328–338} of a MOSFET, precisely the same as Si. Although single-crystal $\text{Si}_{1-x}\text{Ge}_x$ is preferred in the source/drain for its high conductivity,³³⁹ polycrystalline $\text{Si}_{1-x}\text{Ge}_x$ can in principle also be used as well as long as it yields the needed electrical properties for desired transistor performance. The fabrication of $\text{Si}_{1-x}\text{Ge}_x$ -channel MOSFETs always leads to the presence of $\text{Si}_{1-x}\text{Ge}_x$ in the source/drain regions even if a $\text{Si}_{1-x}\text{Ge}_x$ -source/drain is not originally intended. This picture is made clear in Figure 69, where the schematic cross section of a $\text{Si}_{1-x}\text{Ge}_x$ -channel MOSFET is shown. The discussions below therefore also consider the probable effects of the crystallinity of $\text{Si}_{1-x}\text{Ge}_x$, mainly on the morphological instability of germanosilicide/ $\text{Si}_{1-x}\text{Ge}_x$ layer stacks.

It should be noted first that the solid solubility of the most common dopants, that is, B, As, P, is much higher in Si than in Ge.⁶⁰⁶ When poly- $\text{Si}_{1-x}\text{Ge}_x$ films are doped with P, a considerable increase in sheet resistance with increasing Ge fraction is observed,⁶⁰⁷ as a result of a sharply decreasing electron concentration. When the films are doped with B, a substantial decrease in sheet resistance with increasing Ge fraction is evi-

dent.^{607–609} However, the solubility of B in $\text{Si}_{1-x}\text{Ge}_x$ is found to drop when increasing the Ge fraction.⁶⁰⁹ Supersaturation doping of $\text{Si}_{1-x}\text{Ge}_x$ with B is possible with the *in situ* doping technique using Si-, Ge-, and B-source gases simultaneously.^{608,609} For single-crystal $\text{Si}_{1-x}\text{Ge}_x$, alloying with B up to 10 at. %, due to strain compensation effect,^{610,611} has been demonstrated by Gannavaram and Öztürk to yield extremely low specific resistivity and contact resistivity values^{339,611} of 0.2 mΩcm and 1.5×10^{-8} cm², respectively.

To study the solid-state interactions between Ti, Co, or Ni and $\text{Si}_{1-x}\text{Ge}_x$, the relevant ternary phase diagrams are important and are presented during the course of further discussion. A comparison is first made between the respective binary phase diagrams for Ti-Ge (Figure 70), Co-Ge (Figure 71), and Ni-Ge (Figure 72) and those for Ti-Si (Figure 11), Co-Si (Figure 12) and Ni-Si (Figure 13). Although certain similarities remain, overall the melting points for the germanide phases are lower than those for their silicide counterparts. The available thermochemical data^{74–77} indicate that the germanides are less stable than their corresponding silicides with the same atomic composition but by replacing Ge with Si, as the

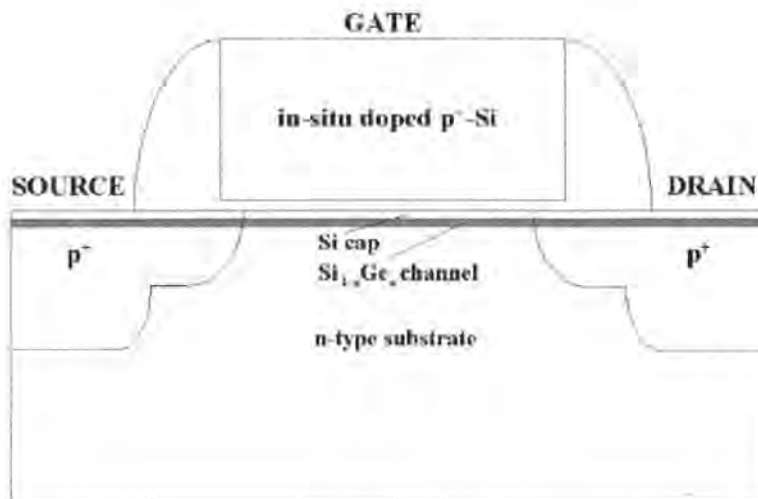


FIGURE 69. Schematic cross-section of a buried $\text{Si}_{1-x}\text{Ge}_x$ -channel MOSFET with the $\text{Si}_{1-x}\text{Ge}_x$ channel highlighted in gray.

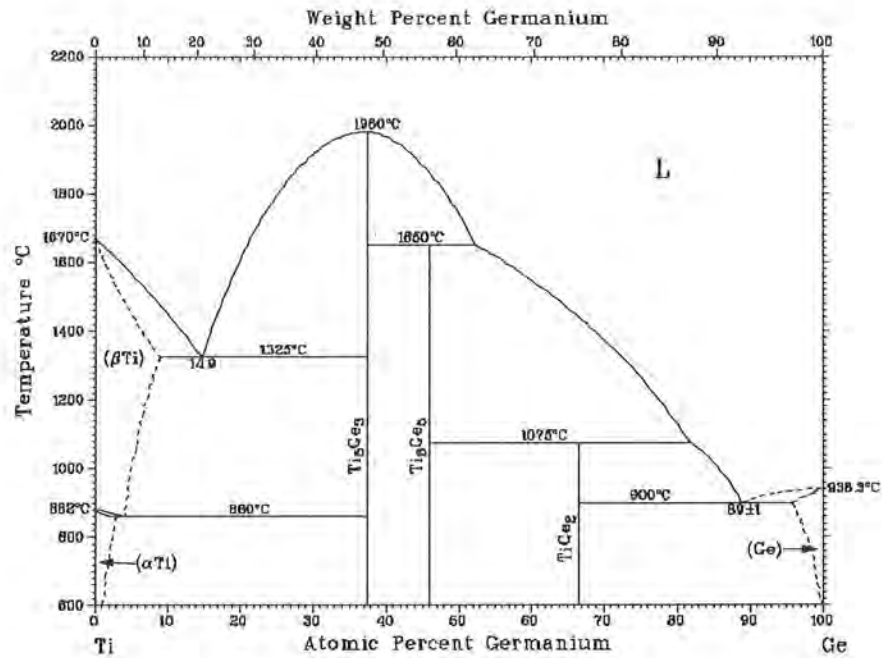


FIGURE 70. Binary phase diagram for Ti-Ge. (Taken from Ref. 69. With permission.)

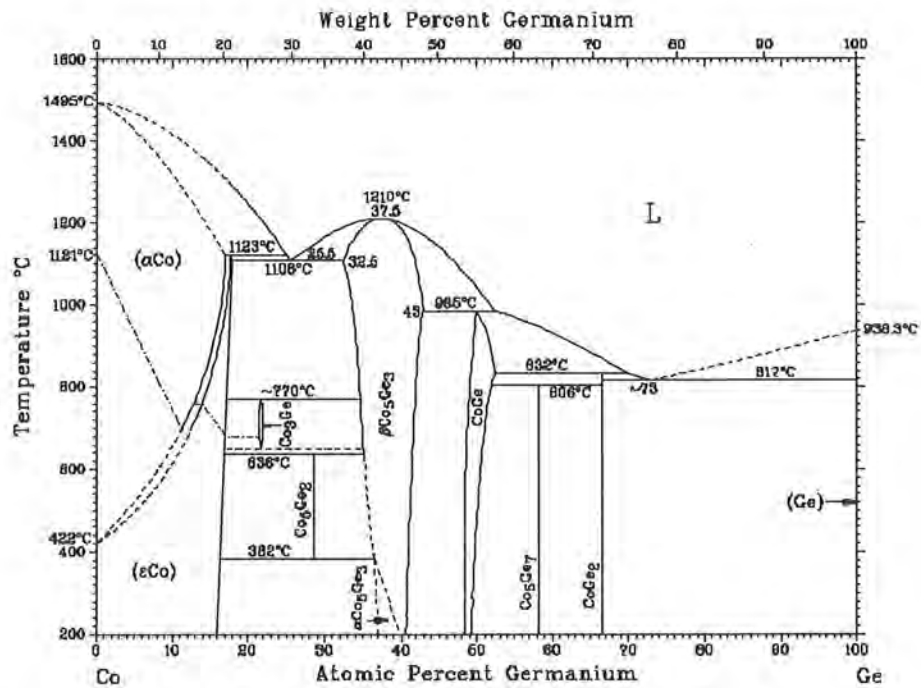


FIGURE 71. Binary phase diagram for Co-Ge. (Taken from Ref. 69. With permission.)

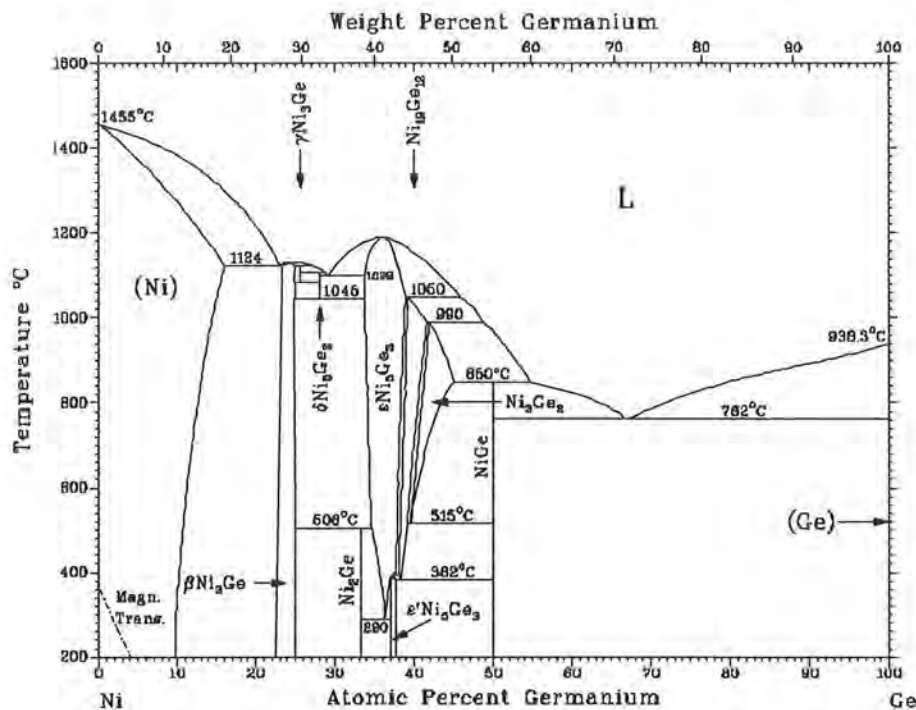


FIGURE 72. Binary phase diagram for Ni-Ge. (Taken from Ref. 69. With permission.)

heats of formation (enthalpy) or Gibbs' free energies are lower (less negative) for the germanides. The physical properties of the silicides and germanides of Ti, Co, and Ni are summarized in Table 6. There are two major aspects to consider, one related to the kinetics and the other to the thermodynamics that are important for the phase formation of the silicides and germanides. First, the relatively low melting points of the germanide phases indicate a relatively high reactive diffusion in them, when compared with the similar diffusion in the corresponding silicide phases.^{103,117} Consequently, the formation of germanides tends to occur at lower temperatures than the formation of the silicides. Second, the relatively large Gibbs' energies for the silicide phases indicate their relatively high phase stability, when compared with the phase stability of the corresponding germanides. As a result, a germanide can be transformed into a silicide by Si replacing Ge in the compound lattice if Si is available, which has indeed been observed experimentally.

Studies of interaction between $\text{Si}_{1-x}\text{Ge}_x$ and other transition-metals than Ti, Co, and Ni, as well as the

formation of their germanosilicides are also found in the literature. Some examples are given for Pd,^{612,613} Pt,⁶¹⁴ Fe,⁶¹⁵ W,⁶¹⁶ and Zr⁶¹⁷ in the reference list, but they are excluded from this discussion in order to keep our focus on contact metallization using the SALICIDE technique.

1. Ti

The majority of the Ti-silicides share the same crystallographic structures and display close lattice dimensions as the corresponding Ti-germanides (see Table 6). One would then expect that ternary solutions or alloys, corresponding to the pairs $\text{Ti}_3\text{Si}-\text{Ti}_3\text{Ge}$, $\text{Ti}_5\text{Si}_3-\text{Ti}_5\text{Ge}_3$, $\text{TiSi}-\text{TiGe}$, $\text{C49 TiSi}_2-\text{C49 TiGe}_2$, and $\text{C54 TiSi}_2-\text{C54 TiGe}_2$, should form after the annealing of Ti films deposited on $\text{Si}_{1-x}\text{Ge}_x$ substrates. Then, one would think that the phase formation sequence should remain the same as that observed in the Ti-Si reaction, but likely with the various ternary alloys found at decreased temperatures. However, what has been obtained experimentally appears to be quite dif-

TABLE 6

Physical and Thermochemical Properties of the Silicides and Germanides of Ti, Co, and Ni.^{38,47,69,74-79} Δh Represents the Room-Temperature Heat of Formation (Enthalpy) of a Compound in Eq. 4

Metal	Phase	Crystal structure	Lattice constant (Å)			T_m (K)	ρ ($\mu\Omega\text{cm}$)	Δh (kJ/g-atom)	DDS
			a	b	c				
Ti	Ti ₃ Si	Tetragonal	10.196	-	5.097	1440			Si
	Ti ₃ Ge	Tetragonal	10.29	-	5.14	?			Ge?
	Ti ₅ Si ₃	Hexagonal	7.429	-	5.139	2400		-72	Si
	Ti ₅ Ge ₃	Hexagonal	7.537	-	5.223	?			Ge?
	Ti ₅ Si ₄	Tetragonal	6.702	-	12.174	2190			Si
	Ti ₆ Ge ₅	Orthorhombic	16.915	7.954	5.233	?	150		Ge
	TiSi	Orthorhombic	3.618	6.492	4.973	1840		-65	Si
	TiGe	Orthorhombic	3.809	6.834	5.235	?			Ge?
	C49TiSi ₂	Orthorhombic	3.562	13.531	3.550	?	60-80	-43(???)	Si
	C49GeSi ₂	Orthorhombic	3.68	14.24	3.704	?	146		Ge
	C54TiSi ₂	Orthorhombic	8.252	4.783	8.540	1750	15	-45	Si
	C54TiGe ₂	Orthorhombic	8.594	5.030	8.864	?	22	-37	Ge
Co	Co ₃ Si	Hexagonal	4.976	-	4.069	1480			Co
	Co ₃ Ge ₂	Hexagonal	3.933	-	5.014	?			Co?
	Co ₂ Si	Orthorhombic	4.918	3.738	7.109	1600	110	-38	Co
	Co ₂ Ge	Orthorhombic	5.02	3.82	7.26	1470		-15	Co?
	CoSi	Cubic	4.4443	-	-	1700	147	-48	Si
	CoGe	Cubic	4.4637	-	-	1250		-16	Ge?
	CoGe	Orthorhombic	11.648	3.807	4.945	?			Ge?
	Co ₅ Ge ₇	Tetragonal	7.64	-	5.81	?			Co
	CoSi ₂	Cubic	5.365	-	-	1600	15	-33	Co
	CoGe ₂	Orthorhombic	5.681	5.681	10.818	1110	35	-12	Co
Ni	Ni ₃ Si	Cubic	3.504	-	-	1440		-26	Ni
	Ni ₃ Ge	Cubic	3.566	-	-	1400		-25	Ni
	Ni ₂ Si	Orthorhombic	5.00	3.73	7.04	1580	24	-48	Ni
	Ni ₂ Ge	Orthorhombic	5.113	3.830	7.264	780		-37	Ni
	NiSi	Orthorhombic	5.18	3.34	5.62	1265	10.5	-45	Ni
	NiGe	Orthorhombic	5.389	3.438	5.82	1123		-32	Ni
	NiSi ₂	Cubic	5.406	-	-	1298	34	-31	Ni
	NiGe ₂	No existence	-	-	-	-	-	-	-

ferent. Thomas *et al.* have shown,³⁷⁸⁻³⁸⁰ and confirmed by others,^{618,619} that C49 TiGe₂ does not form and that Ti₆Ge₅ is the phase preceding the formation of C54 TiGe₂ during the solid-state interaction between Ti films and Si_{1-x}Ge_x substrates, including pure Ge. The nucleation of TiGe₂ apparently becomes difficult once Ti₆Ge₅ is formed.³⁷⁸⁻³⁸⁰ (The C49 TiGe₂ was found in a separate study⁶²⁰ by annealing a co-deposited Ti-Ge film with the correct stoichiometry Ti:Ge=1:2.) As a result, phase separation was found with the

co-existence of C49 TiSi₂ and Ti₆Ge₅ prior to the formation of the ternary alloy C54 Ti(Si_{1-y}Ge_y)₂, where y is generally different from x in Si_{1-x}Ge_x. The entropy of mixing due to Si-Ge in the C54 Ti(Si_{1-y}Ge_y)₂ gives rise to an increase in Δg , and then a decrease in ΔG^* , cf. Eq. 2, for the formation of the C54 phase on the expenses of C49 TiSi₂ and Ti₆Ge₅. This effect, together with a lower formation temperature for C54 TiGe₂ than for TiSi₂,^{379,380,621} lead to a continuously decreasing temperature for the formation of C54 Ti(Si_{1-y}Ge_y)₂.

with increasing the atomic fraction of Ge, as can be inferred from a successive decrease in temperature for the formation of the low-resistivity germanosilicide film.^{379,380,618,619,621} Such examples are shown in Figure 73 for Ti-silicide formation on heavily B-doped poly-Si, $\text{Si}_{0.75}\text{Ge}_{0.25}$ and $\text{Si}_{0.5}\text{Ge}_{0.5}$ films, at various RTP temperatures. Many more studies than just discussed on the Ti-Si_{1-x}Ge_x interaction are found in the literature.⁶²²⁻⁶³⁰

The specific resistivity of C54 TiGe₂ is higher than that of C54 TiSi₂.^{379,380,621} Because there also exists alloy scattering in the ternary solution $\text{Ti}(\text{Si}_{1-y}\text{Ge}_y)_2$, a higher specific resistivity is obtained for the C54 $\text{Ti}(\text{Si}_{1-y}\text{Ge}_y)_2$ than for the C54 TiSi₂.^{379,380,621} For device processing, the etching rate of the $\text{Ti}(\text{Si}_{1-y}\text{Ge}_y)_2$ films in the standard solutions $\text{H}_2\text{SO}_4\text{:H}_2\text{O}_2$ ⁶³¹ or $\text{NH}_4\text{OH}\text{:H}_2\text{O}_2\text{:H}_2\text{O}$ ^{619,622} is fairly low, thus they can be cleaned in such solutions.

Although it enhances the formation of the C54 phase even in narrow lines down to 0.3- μm width,³⁷⁷ the morphological stability of the $\text{Ti}(\text{Si}_{1-y}\text{Ge}_y)_2/\text{Si}_{1-x}\text{Ge}_x$ layer structure remains an important issue to resolve. Agglomeration of a C54 $\text{Ti}(\text{Si}_{1-y}\text{Ge}_y)_2$ layer on top of heavily B-doped

poly-Si_{0.5}Ge_{0.5} already occurs when it is annealed at 750°C for 30 sec (see Figure 74 for a cross-sectional TEM picture). Careful examinations by Aldrich *et al.* show^{618,623} that out-diffusion of Ge from the $\text{Ti}(\text{Si}_{1-y}\text{Ge}_y)_2$ crystal grains results in the formation of Ge-rich $\text{Si}_{1-z}\text{Ge}_z$ (*i.e.* $z > x$) precipitates segregating at the grain boundaries of $\text{Ti}(\text{Si}_{1-y}\text{Ge}_y)_2$. The SEM results in Figure 75 clearly indicate that the presence of a high density of such $\text{Si}_{1-z}\text{Ge}_z$ precipitates can interrupt the electrical network of a continuous C54 $\text{Ti}(\text{Si}_{1-y}\text{Ge}_y)_2$ film at their grain boundaries. Hence, an increase in sheet resistance of the C54 $\text{Ti}(\text{Si}_{1-y}\text{Ge}_y)_2$ /poly-Si_{1-x}Ge_x bilayer structures can occur, as seen in Figure 73 for the resistance values at 800°C. Aldrich and d'Heurle later presented a thermodynamic model showing⁶³² that the difference in Gibbs' free energy between TiSi₂ and TiGe₂ is the driving force for the out-diffusion and segregation of Ge. The ternary phase diagram at 700°C based on their equilibrium calculations taking into consideration the entropy of mixing is reproduced in Figure 76 showing the composition domain directly concerning the formation of $\text{Ti}(\text{Si}_{1-y}\text{Ge}_y)_2$

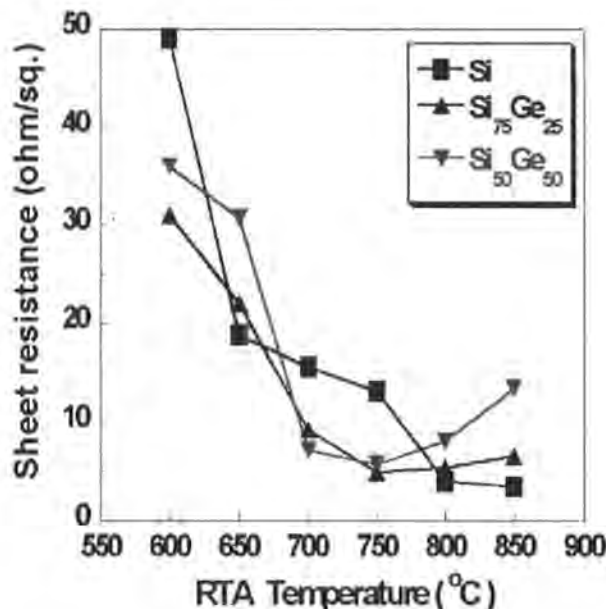


FIGURE 73. Sheet resistance vs. RTP temperature for Ti-Si_xGe_{1-x} interaction for 30 s.

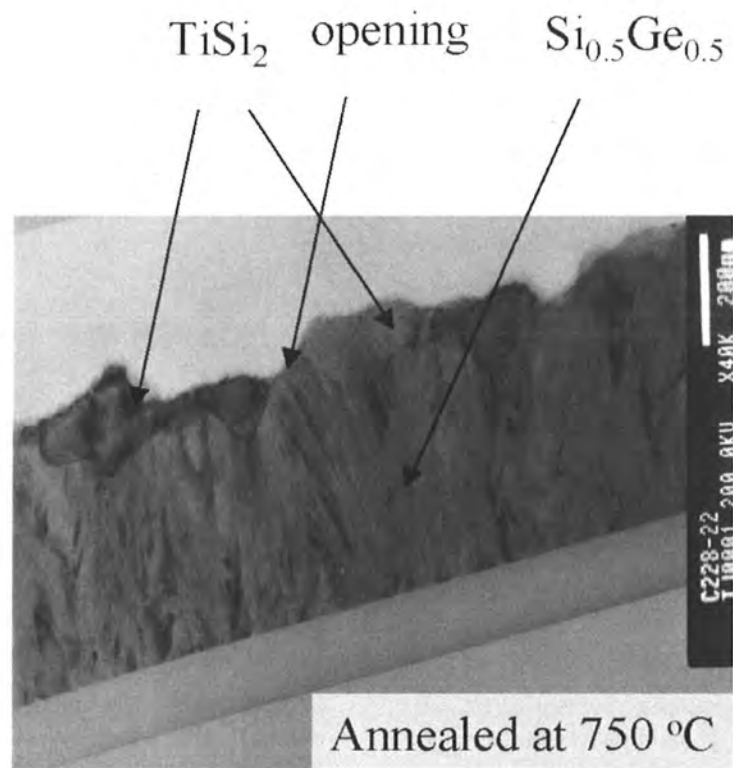


FIGURE 74. XTEM of a broken C54 Ti(Si,Ge)₂ layer (marked as TiSi₂) on p⁺ poly-Si_{0.5}Ge_{0.5}.

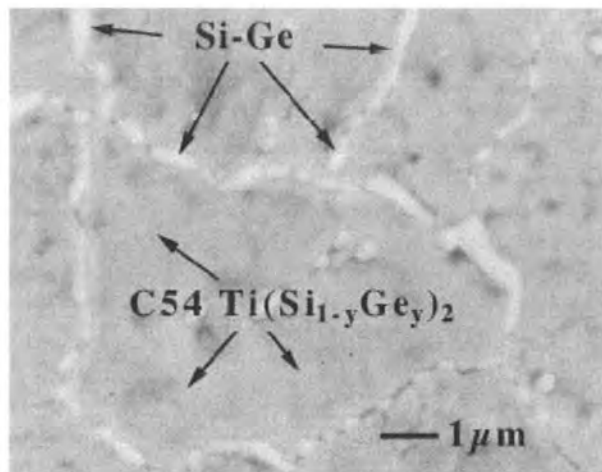


FIGURE 75. SEM top view of Ge-rich precipitates around C54 Ti(Si_{1-y}Ge_y)₂ grains. (Taken from Ref. 632. With permission.)

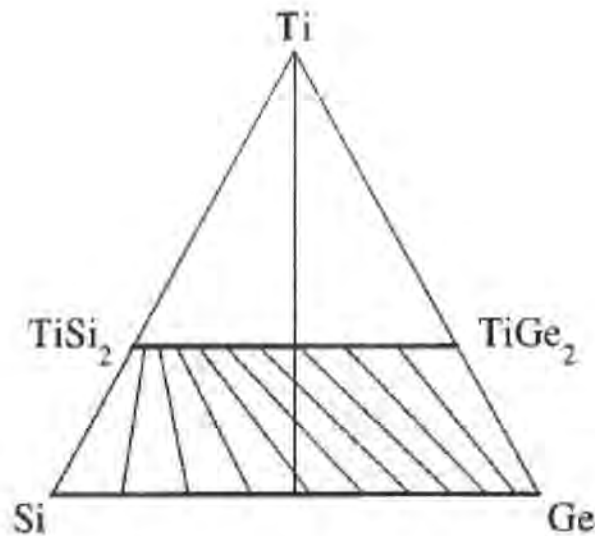


FIGURE 76. Ternary phase diagrams at 700°C for Ti-Si-Ge. (Taken from Ref. 632. With permission.)

as well as the interaction between $\text{Ti}(\text{Si}_{1-y}\text{Ge}_y)_2$ and $\text{Si}_{1-x}\text{Ge}_x$. The calculation results agree very well with the experimental data.^{618,623}

The process of out-diffusion and segregation of Ge is driven⁶³² by the difference in thermochemical properties of the two C54 phases of TiSi_2 and TiGe_2 . The degree of out-diffusion depends on a number of factors, both thermodynamic and kinetic, including the value of x in $\text{Si}_{1-x}\text{Ge}_x$, the total amounts of Si, Ge, and Ti available in the system, and the annealing temperature. Usually, the $\text{Si}_{1-x}\text{Ge}_x$ layer is much thicker than the Ti. The value of x sets the initial points on the two horizontal lines Si-Ge, $\text{Si}_{1-x}\text{Ge}_x$, and TiSi_2 - TiGe_2 , $\text{Ti}(\text{Si}_{1-x}\text{Ge}_x)_2$, and these points are connected by a straight line originating from the upper corner Ti (see the vertical straight line in Figure 76). There are numerous possible tie-lines intersecting this straight line. Each of the tie-lines defines a specific set of equilibrium compositions, that is, y in the final $\text{Ti}(\text{Si}_{1-y}\text{Ge}_y)_2$ and z in the precipitates $\text{Si}_{1-z}\text{Ge}_z$ around. The annealing temperature determines how much Si and Ge would inter-diffuse within a certain period of time between the precipitates $\text{Si}_{1-z}\text{Ge}_z$ and the unreacted $\text{Si}_{1-x}\text{Ge}_x$ beneath. If the inter-diffusion of Si and Ge inside SiGe is rapid, one should pick one of the tie-lines whose intersection with the vertical line in Figure 76 is closer

to the bottom Si-Ge line because there would be more $\text{Si}_{1-x}\text{Ge}_x$ joining the interaction. The removal of Ge from the $\text{Si}_{1-z}\text{Ge}_z$ precipitates due to inter-diffusion will allow further out-diffusion of Ge from $\text{Ti}(\text{Si}_{1-y}\text{Ge}_y)_2$. This process continues until the system approaches the equilibrium conditions determined by the given tie-line, provided that the annealing time is sufficiently long. The diffusion coefficients of Si and Ge are dependent on the crystallinity of $\text{Si}_{1-x}\text{Ge}_x$. Because the inter-diffusion of Si and Ge in SiGe is generally very slow at the temperatures typically used for silicide formation ($<900^\circ\text{C}$), it is much less influenced by the crystallinity than the composition of the $\text{Si}_{1-x}\text{Ge}_x$.⁶³³⁻⁶³⁶

The degree of Ge out-diffusion could be reduced if the formation temperature for the C54 phase could be reduced, according to the analysis above. Further lowering the formation temperature is, however, not practically viable due to the requirement for the formation of the low-resistivity C54 TiSi_2 or $\text{Ti}(\text{Si}_{1-y}\text{Ge}_y)_2$ in all three regions of gate and source/drain. The phase sequence, that is, C49-first and C54-later, is not altered in the presence of Ge; the C49 TiSi_2 or $\text{Ti}(\text{Si}_{1-y}\text{Ge}_y)_2$ always forms prior to the C54 ones.^{378-380,618,619,621-631} even when a Ge interlayer is used.⁶³⁷ Hence, the formation of the C54 phase necessarily undergoes the usual route of C49-C54

phase transformation that is driven by a small value of ΔG_v and thus requires a relatively high temperature. Because the temperature at which agglomeration of C54 the $\text{Ti}(\text{Si}_{1-y}\text{Ge}_y)_2/\text{poly-Si}_{1-x}\text{Ge}_x$ structure occurs is rather low compared with that needed for the formation of C54 TiSi_2 or $\text{Ti}(\text{Si}_{1-y}\text{Ge}_y)_2$ in the narrow-line gate or small-dimension source/drain, there is hardly any temperature window left for the SALICIDE process using Ti on $\text{Si}_{1-x}\text{Ge}_x$.

2. Co

Although the majority of the Co-silicides also share the same crystallographic structures and exhibit close lattice dimensions as the corresponding Co-germanides (Table 6), the most desired phases CoSi_2 and CoGe_2 do not follow this pattern. Consequently, CoSi and CoGe form a ternary solution, while phase separation is expected for CoSi_2 and CoGe_2 . On $\text{Si}_{1-x}\text{Ge}_x$ substrates, the formation of silicides-germanides or germanosilicides usually begins with the metal-rich phases and ends with the Si/Ge-rich ones. For Co reacting with $\text{Si}_{1-x}\text{Ge}_x$, the formation of $\text{CoSi}_{1-y}\text{Ge}_y$ precedes that of CoSi_2 and CoGe_2 . Thus, the formation tempera-

ture for the latter phases is expected to increase. Experimental results indeed show a substantially increased temperature for forming CoSi_2 to yield a low-resistance film;^{319,624,625,638-645} some results are shown in Figure 77 depicting the low-resistivity phase formed at 650°C in the Co/SiGe case but at 850°C in the Co/case of SiGe. Although the available ternary phase diagram for Co-Si-Ge is calculated for the system reaching equilibrium above 760°C,⁶⁴⁶ it provides useful information about the phase formation and is reproduced in Figure 78. A recent study by Detavernier *et al.*⁶⁴⁵ shows that the increased difficulty with the formation of CoSi_2 and CoGe_2 is simply due to a decrease in ΔG_v and then an increase in ΔG^* in Eq. 2, caused by the entropy of mixing due to Si-Ge in the $\text{CoSi}_{1-y}\text{Ge}_y$, as expected. It is precisely the opposite to the formation of C54 $\text{Ti}(\text{Si}_{1-y}\text{Ge}_y)_2$ from C49 TiSi_2 and Ti_6Ge_5 discussed slightly earlier. During the Co- $\text{Si}_{1-x}\text{Ge}_x$ interaction, the Co-Si bonding is preferred compared to the Co-Ge.⁶⁴⁷ Studies of solid-state interactions between Co films and Ge substrates can be found in the literature.⁶⁴⁸⁻⁶⁵⁰ It is apparent from the analysis above, as well as the results in the literature,^{319,624,625,638-646} that the fundamental differences between the disilicide and digermanide of Co make the Co-based SALICIDE process unat-

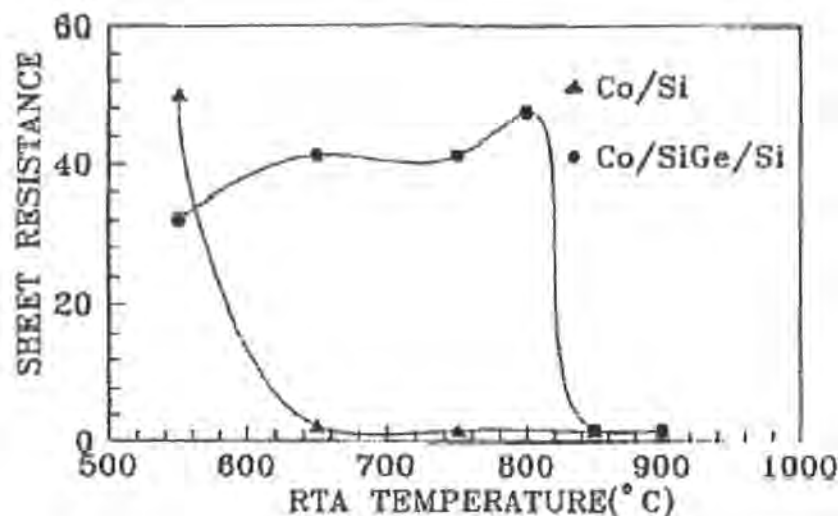


FIGURE 77. Temperature dependence of sheet resistance for $\text{Co}(350 \text{ \AA})/\text{Si}_{0.8}\text{Ge}_{0.2}(1000 \text{ \AA})/\text{Si}$ and Co/Si samples. (Taken from Ref. 624. With permission.)

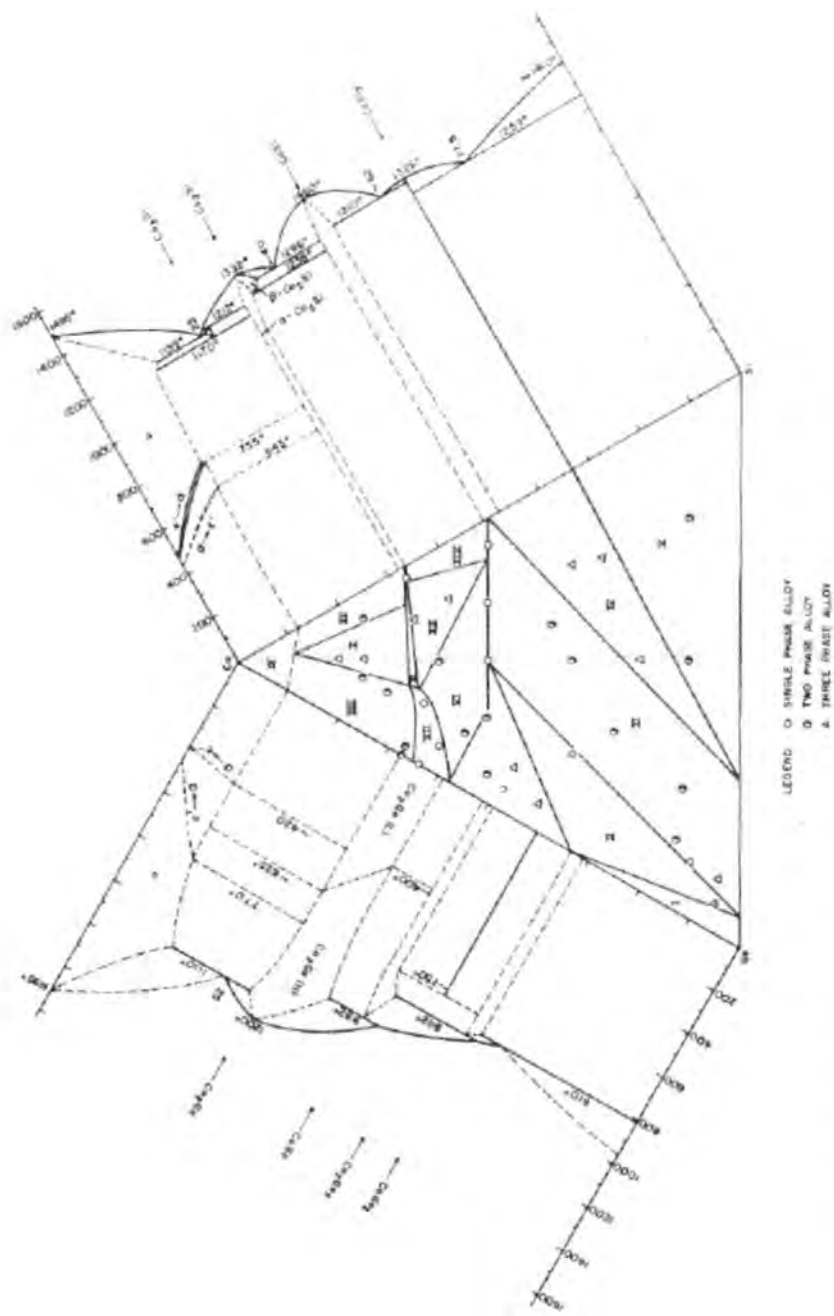


FIGURE 78. Ternary phase diagram for Co-Si-Ge. (Taken from Ref. 646. With permission.)

tractive for contact metallization of SiGe devices, if no improvements are made to lower the formation temperature for CoSi_2 .

3. Ni

Studies on the solid-state interaction between Ni and $\text{Si}_{1-x}\text{Ge}_x$ have been relatively few compared with those on Ti and Co, but recently an increased interest is being observed.^{450,651-655} The formation of ternary solid solutions is expected between the silicide-germanide pairs Ni_3Si - Ni_3Ge , Ni_2Si - Ni_2Ge , and NiSi - NiGe (see Table 6). The formation of ternary solid solution $\text{NiSi}_{1-x}\text{Ge}_x$ of the MnP structure has now been confirmed and the lattice parameters a , b , c vary linearly with x ⁶⁵⁵ following Vegard's law. The facts that NiGe_2 does not seem to exist and that the ternary solution $\text{NiSi}_{1-x}\text{Ge}_x$ does form have been shown to hinder the nucleation of NiSi_2 .^{450,655} The fundamental causes for this observed retardation of the NiSi_2 formation are identical to the earlier discussed ones for the enhanced formation of the ternary solution $\text{C54 Ti}(\text{Si}_{1-y}\text{Ge}_y)_2$ from C49 TiSi_2 and Ti_6Ge_5 or the increased difficulties for the formation of CoSi_2 and CoGe_2 from the ternary

solution $\text{CoSi}_{1-x}\text{Ge}_x$, that is, Gibb's free energy gain for the ternary alloys due to the entropy of mixing. An approximate ternary phase diagram depicting the composition domains directly concerning the formation of $\text{NiSi}_{1-x}\text{Ge}_x$ as well as its interaction with $\text{Si}_{1-x}\text{Ge}_x$ is shown in Figure 79. Four composition domains are found: (1) two-phase domain $\text{Si}_{1-x}\text{Ge}_x$ - NiSi_2 , (2) two-phase domain $\text{Si}_{1-x}\text{Ge}_x$ - $\text{NiSi}_{1-u}\text{Ge}_u$, (3) three-phase domain $\text{Si}_{0.53}\text{Ge}_{0.47}$ - $\text{NiSi}_{0.95}\text{Ge}_{0.05}$ - NiSi_2 , and (4) two-phase domain $\text{NiSi}_{1-u}\text{Ge}_u$ - NiSi_2 , when counting counterclockwise from the lower-left corner. Experimental results showed^{450,655} that after annealing of Ni on poly- $\text{Si}_{1-x}\text{Ge}_x$ ($x=0.29, 0.58$), $\text{NiSi}_{1-x}\text{Ge}_x$ formed at 450°C and above. However, severe out-diffusion and segregation of Ge forming Ge-rich $\text{Si}_{1-z}\text{Ge}_z$ ($z>x$) precipitates and simultaneous Si-enrichment in the ternary solution $\text{NiSi}_{1-y}\text{Ge}_y$ ($y<x$) were found between 600 and 650°C RTP for 30 sec. As a result, drastic increases in sheet resistance at these temperatures were found, as shown in Figure 80, indicating the occurrence of agglomeration of the $\text{NiSi}_{1-x}\text{Ge}_x$ /poly- $\text{Si}_{1-x}\text{Ge}_x$ structure. Also shown in Figure 80 are the results for Ni reacting with poly-Si for comparison. The compositional changes vs. annealing temperature for these samples, determined by means of XRD

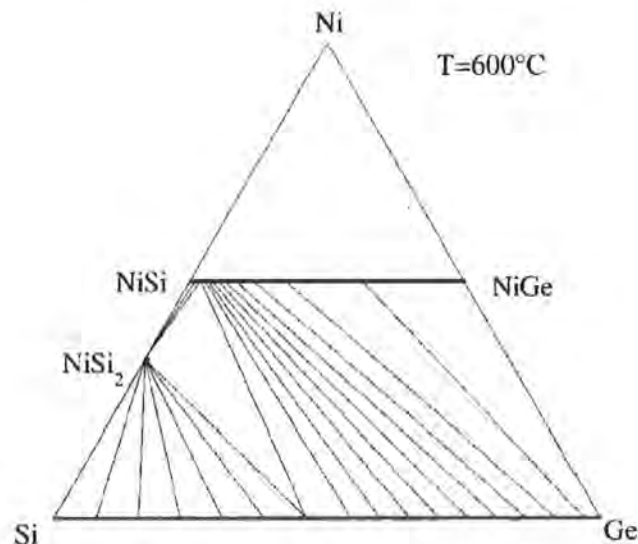


FIGURE 79. Ternary phase diagram at 600°C for Ni-Si-Ge. (Taken from Ref. 450. With permission.)

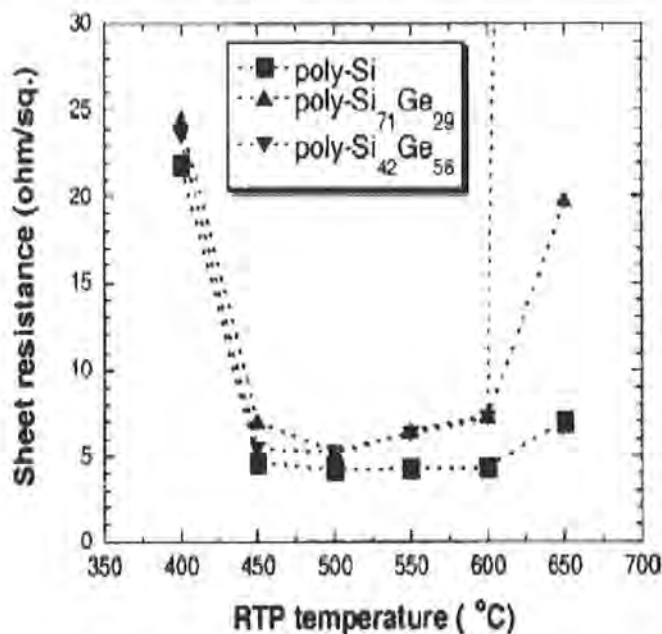


FIGURE 80. Variation of sheet resistance with RTP temperature for Ni(200 Å) on Si, Si_{0.71}Ge_{0.29} and Si_{0.42}Ge_{0.58}. (Taken from Ref. 655. With permission.)

and EDS in Refs. 450 and 655, are reproduced in Figure 81. In the figure, the changes are quantified with u in NiSi_{1-u}Ge_u and z in Si_{1-z}Ge_z. Agglomeration of the NiSi_{1-u}Ge_u layer and diffusion of the NiSi_{1-u}Ge_u grains along the grain boundaries within the Si_{1-x}Ge_x matrix are identified as the cause for such rapid changes in the compositions (see Figure 82 for a cross-sectional TEM picture taken at 650°C).⁴⁵⁰ And all experimental observations in Refs. 450 and 655 can be quantitatively accounted for based on the calculated phase diagrams.

As it is NiSi or NiSi_{1-x}Ge_x that is wanted for the device contact formation due to its low resistivity, this retarded formation of NiSi₂ is actually an observation favoring its practical device applications. This situation is entirely different from the Co-Si-Ge system, where the disilicide or digermanosilicide is desired. Although the morphological instability with the NiSi_{1-x}Ge_x continues to pose a challenge, the comparable formation temperatures for both NiSi and NiSi_{1-x}Ge_x, in fact, leave a practical process temperature window for the integration of the Ni-based SALICIDE process with the Si_{1-x}Ge_x electrodes.⁶⁵⁵ On compressively strained, heavily B-doped single-crystal

Si_{0.8}Ge_{0.2}, it has been found^{656,657} that the morphological stability of the NiSi_{0.8}Ge_{0.2}/Si_{0.8}Ge_{0.2}/Si(100) structure greatly improves when compared with that of the NiSi_{1-x}Ge_x/poly-Si_{1-x}Ge_x structure (see Figure 83 for the sheet resistance results vs. RTP temperature). Also shown in Figure 83 are the results for Ni reacting with Si(100). A recent comparative study on Ni and Co reacting with single-crystal Si_{0.3}Ge_{0.7} also shows a clear advantage with Ni because a continuous NiSi_{1-x}Ge_x layer was found yielding the desired low-resistivity contact material.⁶⁵⁴ With Co, annealing at low temperatures yielded a very high sheet resistance, presumably due to the formation of CoSi_{1-y}Ge_y and the retarded formation of the low-resistivity CoSi₂. At high temperatures at which CoSi₂ would form, for example, 900°C, the germanosilicide layer became severely agglomerated.

V. FUTURE TRENDS

The down-scaling trend of device dimensions will continue well into the next decade.¹ New elements and therefore materials are incorporated

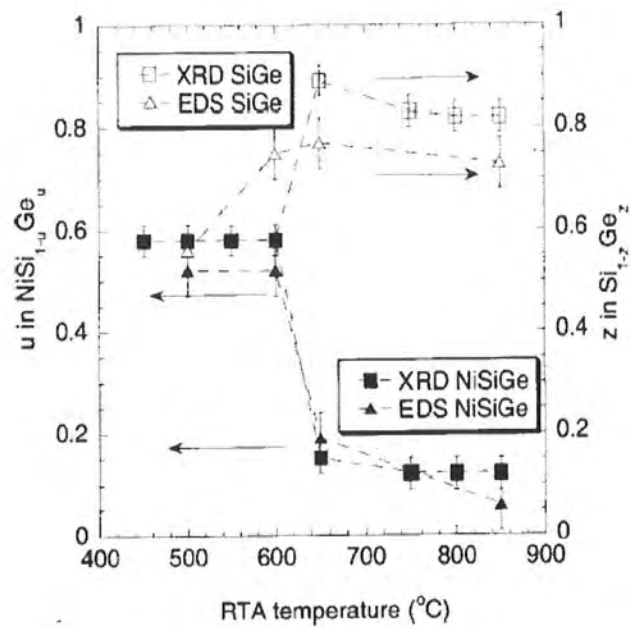


FIGURE 81. Comparison between XRD and EDS data for the atomic composition of $\text{NiSi}_{1-u}\text{Ge}_u$ as well as $\text{Si}_{1-x}\text{Ge}_x$ and Ge-rich $\text{Si}_{1-z}\text{Ge}_z$ for the annealed $\text{Ni/poly-Si}_{0.42}\text{Ge}_{0.58}$ samples. (Taken from Ref. 450. With permission.)

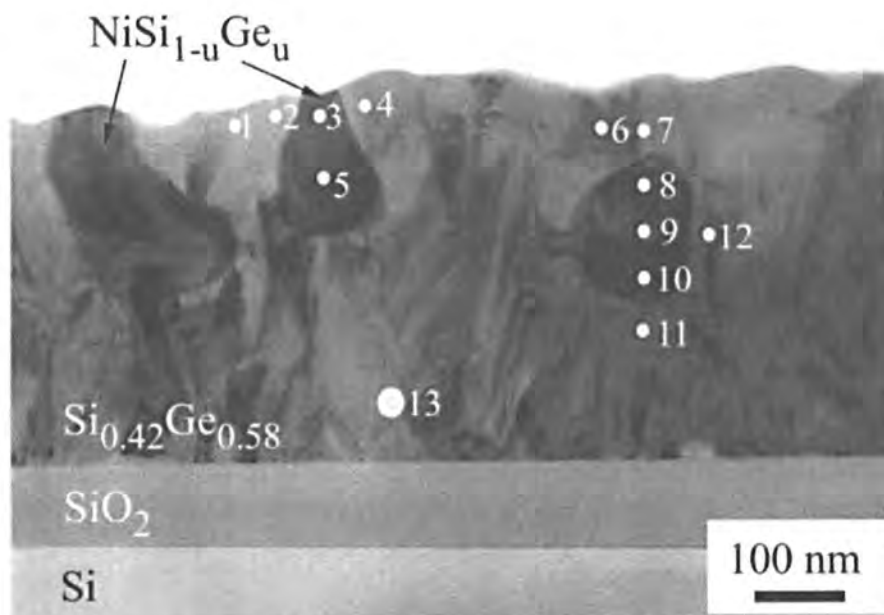


FIGURE 82. XTEM of the $\text{Ni/poly-Si}_{0.42}\text{Ge}_{0.58}$ sample at 650°C. (Taken from Ref. 450. With permission.)

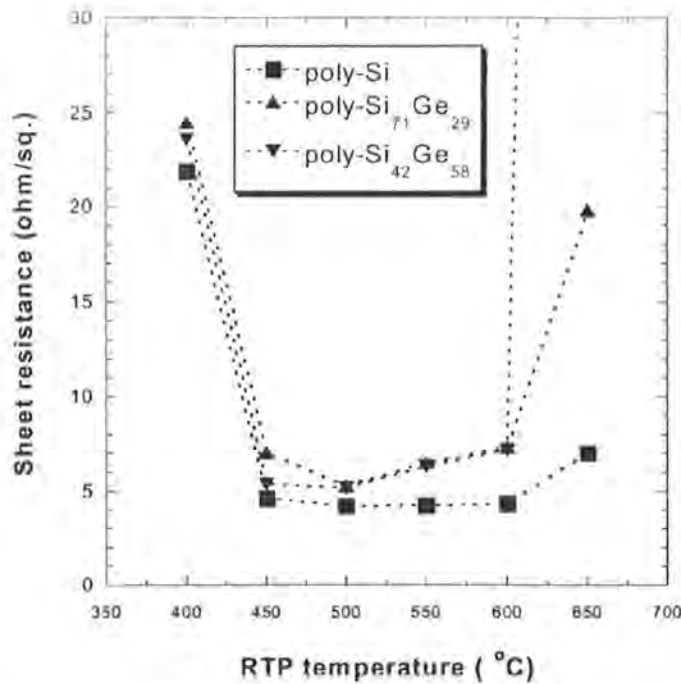


FIGURE 83. Sheet resistance vs. RTP temperature for Ni/epi-Si_{0.8}Ge_{0.2}(B)/Si(100) and Ni/Si(100). (Taken from Ref. 656. With permission.)

in each coming generation of devices in order to help realize the dimensional down-scaling. This action is also referred as “material-scaling”. The demand for device performance improvements has not only revived some old ideas with new approaches but more importantly motivated search for non-classical MOSFETs that provide a path to scaling CMOS to the end of the Roadmap using innovative device structures and architectures. Some scenarios of how metal silicides could find their positions in coping with such developments are discussed in this final section.

A. Mechanical and Metallurgical Aspects

As shown by Steegen and Maex,⁴⁶ mechanical stress can become increasingly important in devices of decreasing dimensions. Silicide formation induced stress may influence the electrical characteristics as well as reliability of MOS devices. Inversely, stress may affect the silicide formation in terms of the formation temperature, morphology, and phase.^{525,656–658} Examples have been shown for an increased drain current due to the silicide-induced stress in the channel.⁴⁶ On the other hand, detrimental effects of stress on device

performance that can be anticipated are the generation of undesirable defects that can trap carriers, decrease carrier mobility and cause current leakage. Hence, stress management is crucial for desired device performance. The systematic study of Steegen and Maex provides a useful guide toward modeling and understanding how and where stress is built up during silicide formation as well as how it affects the electrical characteristics of devices. Refinements of the existing models are, however, anticipated for effective stress management for future generations of devices with even more demanding material and dimensional requirements. These include, of course, the stress induced by silicide formation.

Acceptance of a new element in the established CMOS technology requires the full understanding of its consequences based on intensive fundamental research. To begin with, the metallurgical aspects should be investigated in order to interpret and even predict the silicide phase formation. As shown earlier, intended alloying can be a useful solution to overcome silicide formation difficulties, for example, Ti alloys for C54 TiSi₂,^{391,398–401} Mo-, Ta-, or Nb-interlayer for C54 TiSi₂,^{115,388–390,396,408,409,412–424} Co-Ni alloys for CoSi₂,^{340,440,443} and Ni-Pt alloys for NiSi.^{449,460,530–536}

Search for such alloys can be purposeful under the supervision of thermodynamics. Unintended alloying encountered during silicide formation, for example, during contact metallization to SiGe alloys that are, however, vital for improvements of device performance, could impose on the existing silicide system(s) for contact integrity. For the three silicides in question, TiSi_2 , CoSi_2 , and NiSi , our understanding of the Ge incorporation has greatly improved through thermodynamic approaches.^{50,632,645} The quest of higher performance for future generations of devices may lead to the incorporation of C in Si along with Ge.⁶⁵⁹ The amounts of C incorporated are usually rather low, on the same order of magnitude for an ordinary dopant such as P, As, and B, that is, around 1 at. %. Yet, its influence on the formation of silicides/germanosilicides can in some cases be significant, according to a few recent studies of Ti,^{660,661} Zr,⁶⁶¹ Co,⁶⁴⁴ and Ni^{662,663} interacting with $\text{Si}_{1-x-y}\text{Ge}_x\text{C}_y$, where y is typically around 0.01. For this particular case with C incorporation in SiGe alloys, previous knowledge from related studies on metal-SiC interactions^{104,664,665} can be especially useful. Of particular concern here are how C behaves during annealing and how it affects the contact integrity in terms of interface morphology and contact resistivity. The phase formation and therefore the electrical properties can be modified if C also becomes part of the formed silicides or germanosilicides. If C tends to become graphite precipitates dispersed in the silicide or germanosilicide films, the sheet resistivity of the films is expected to increase. If segregation of C occurs preferentially at the interface between the silicide/germanosilicide and Si/SiGe, an increase in contact resistivity is also anticipated. Whether these increases can be tolerated depends on the relative importance of the contact resistivity compared with the overall source/drain series resistance as an example.

In order to choose a metal for eventual contact formation with its silicide or germanosilicide in the presence of a fourth element (*e.g.*, C, B, As, etc.), one should begin by consulting relevant equilibrium phase diagrams, if available. Now it involves at least four different elements. Phase diagrams are few or incomplete for ternary systems⁷⁰ and rarely available for quaternary ones. One such quaternary phase diagram is shown in

Figure 84 for Al-Ni-Si-C⁶⁶⁶ to show the complexity of the problem. When the corresponding quaternary phase diagrams are unavailable, a look at the related binary and/or ternary diagrams can be very helpful.

B. Metal Gates and Schottky Source/Drain

The poly-Si gate-depletion poses a serious performance limitation for small devices with an ultrathin gate dielectric of about 2 nm SiO_2 . It arises from the use of a poly-Si gate. If the poly-Si region immediately above the gate dielectric is not sufficiently doped due to a too shallow ion implantation and/or too low activation/diffusion annealing, it becomes depleted under the influence of a gate potential for normal transistor operation. The depleted region then acts like a parasitic dielectric being added to the gate dielectric, resulting in a thickening of the overall gate dielectric. Thus, it weakens the control of the gate over the channel as it adds a parasitic capacitance in series with the gate capacitance due to the gate dielectric.⁶⁶⁷ Figure 85 illustrates (a) the electrical gate-dielectric thickening (shown as $t_{\text{poly-dep}}$) and (b) the gate-capacitance lowering (depicted by $C_{\text{poly-dep}}$ in series with C_{ox}), as a result of the gate-depletion effect. Replacing the poly-Si gate with a metal gate can lead to elimination of the gate-depletion effect, provided that the technological challenges with the introduction of metal gates in CMOS technology are overcome. These challenges include the physical properties of the metals chosen as well as their integration into device processing. For the former, a low specific resistivity and an appropriate work function are two major concerns. In addition, two metals are necessary to replace n^+ and p^+ poly-Si for CMOS devices (Figure 1), that is, the so-called dual metal-gate technique.^{1,668-670} For the latter, the chemical, thermal, and mechanical stability of the metals in contact with the underlying gate dielectric, deposition, and etching of the metals, etc. are all important integration questions. Additionally, the gate dielectric is to be changed from the traditional SiO_2 to a high- κ dielectric material, for example, HfO_2 , in order to suppress the tunneling (leakage)

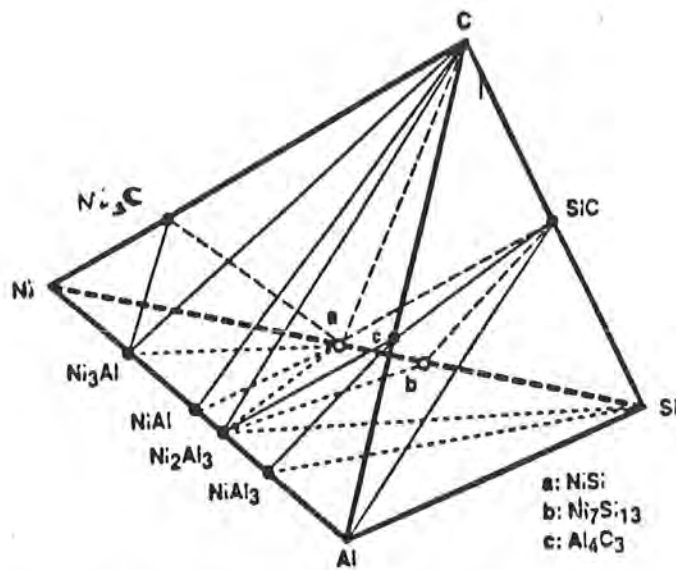


FIGURE 84. Quaternary phase diagram for Al-Ni-Si-C. (Taken from Ref. 666. With permission.)

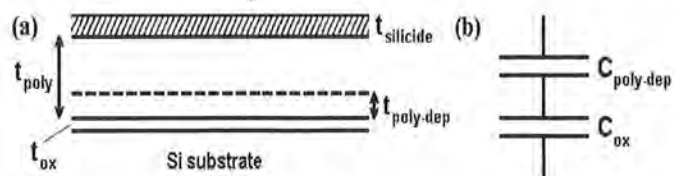


FIGURE 85. Schematic pictures showing gate-depletion (a) and its contribution as a series capacitance (b) in a gate structure.

current through the gate dielectric, thereby keeping pace with the down-scaling.^{1,671} The consideration of a metal silicide in place of poly-Si as the gate electrode material has to take all these issues into account.

For Ohmic contacts to the p-n junctions in the source/drain regions, metal silicides are likely to remain as the main player when the poly-Si gates are being replaced with metal gates. Low specific resistivity and low contact resistivity are still valid requirements for the contact materials; see the discussions above in Section IV.B. The choice of metal silicide for source/drain contact metallization can be dependent on the detailed device-making procedure. Now there exist two alternatives for the fabrication of future MOS devices. One alternative is the traditional “gate-first” route to have the gate first defined (Figure 86a) followed by the source/drain regions. The other alternative reverses the procedure by having a dummy gate first in order to retain the self-alignment processing.⁶⁷² After the source/drain regions are defined, the dummy gate is replaced with the actual one at the end, that is, “gate-last” (Figure 86b). Obviously, a metal with its silicide formed at low temperature, for example, NiSi, is desirable in the traditional “gate-first” approach, with the consideration of retaining the integrity of the metal-gate/high- κ gate structure. For the other alternative “gate-last”, a silicide of high-temperature stability, for example, TiSi₂ or CoSi₂, may become more interesting unless all the processing steps

thereafter are executed at temperatures well below that causing agglomeration of the silicide thin films in the source/drain regions.

The intensive research on transition-metal silicides over the years has also led to revisits of an “old” idea of using Schottky junctions instead of p-n junctions in the source/drain regions.⁶⁷³ Shallow junctions and low parasitic source/drain resistances can be achieved with the silicide source/drain. Using metal silicide(s) for Schottky source/drain is also attractive for the integration of metal-gate and high- κ dielectric, because there will be no dopants in the source/drain regions so that the high-temperature step for dopant activation is eliminated. The silicide formation can be realized using a low thermal budget processing with, for example, NiSi or PtSi. An extension of the use of PtSi as the source/drain terminals for p-channel MOSFETs has been implemented on SOI substrates yielding 35-nm gate-length devices.⁶⁷⁴ A different approach is to use the allotaxy technique (Figure 35) to grown high-quality epitaxial CoSi₂.^{675,676} Making use of the facts that a high stress is present at the edge of isolation^{40–42,46} and that high-temperature thermal oxidation of CoSi₂/Si yields a protective SiO₂,^{23–28,677} Schottky source/drain MOSFETs of down to 40-nm gate-length could be made.^{675,676} A more exciting device concept is the use of two different silicides as the Schottky contacts to the channels of CMOS devices.⁶⁷⁸ On a 14-nm-thick SOI material,

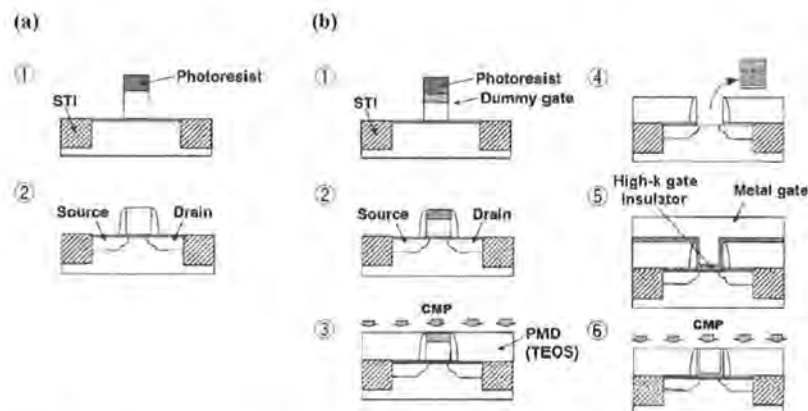


FIGURE 86. Schematic process sequence for gate-first (a) and gate-last (b) approaches for future device making. (Taken from Ref. 672. With permission.)

MOSFETs of 15 to 20 nm gate-length were fabricated using $\text{ErSi}_{1.7}$ and PtSi for the n-channel and p-channel devices, respectively. These two silicides were chosen with the consideration that $\text{ErSi}_{1.7}$ has a low barrier height^{678,679} of around 0.3 eV to n-type Si (for the p-channel MOSFET) and PtSi a low barrier height¹⁷² of 0.21 eV to p-type Si (for the n-channel MOSFET). Note the difference between the traditional approach with the use of *high-barrier* metals or silicides⁶⁷³ and the present ingenious approach with the use of *dual low-barrier* silicides⁶⁷⁸ to boost the drain current for both types of MOSFETs.

C. New Device Structures

With the conventional planar MOSFET structure built on bulk Si substrates, SCEs is severe and difficult to control for transistors of 20-nm gate-length and below. To effectively combat the SCEs, several new device structures have been studied, especially those made on SOI substrates. A comparison has been done by Wann *et al.*⁶⁸⁰ Both planar⁶⁸¹ and vertical⁶⁸² MOSFETs with surrounding-gate have been demonstrated. Intensive research on different device structures has gradually led to a focus on two major kinds of innovative devices that attract most attention today: double-gate (DG) with a thin Si body (channel) mostly built on SOI^{683,684} and FinFet.^{685,686} There are three different solutions to realizing the DG structure with respect to the direction drain current, as summarized in a schematic form in Figure 87.⁶⁸³ The concept and fabrication sequence of a FinFet are shown in Figure 88.⁶⁸⁶ A FinFet actually has a three-side gate from the top and the two sides but not from the bottom of the “Fins”. The fabrication of FinFets completely relies on the established planar technology. Using the conventional spacer technique, the FinFet concept allows for devices of very thin body, much below 100 nm, to be fabricated without recourse to elaborated lithography means.⁶⁸⁶

Low-temperature processing is crucial for both DG and FinFet because they are extremely small with the gate-length as well as the source-to-drain distance much below 100 nm. Making good Ohmic contacts to the source/drain regions can be de-

manding for the DG structures. For the Type-III DG structure shown in Figure 87, it would also need conformal deposition of metal films on the vertical sidewalls if the established SALICIDE technology is to be directly applied. For the FinFet, fine-lines are present not only in the gate but also in the source/drain areas. Therefore, NiSi that can be formed at low temperatures, free from fine-line effect and free from bridging, is a serious candidate for contact metallization for these new MOSFET structures.

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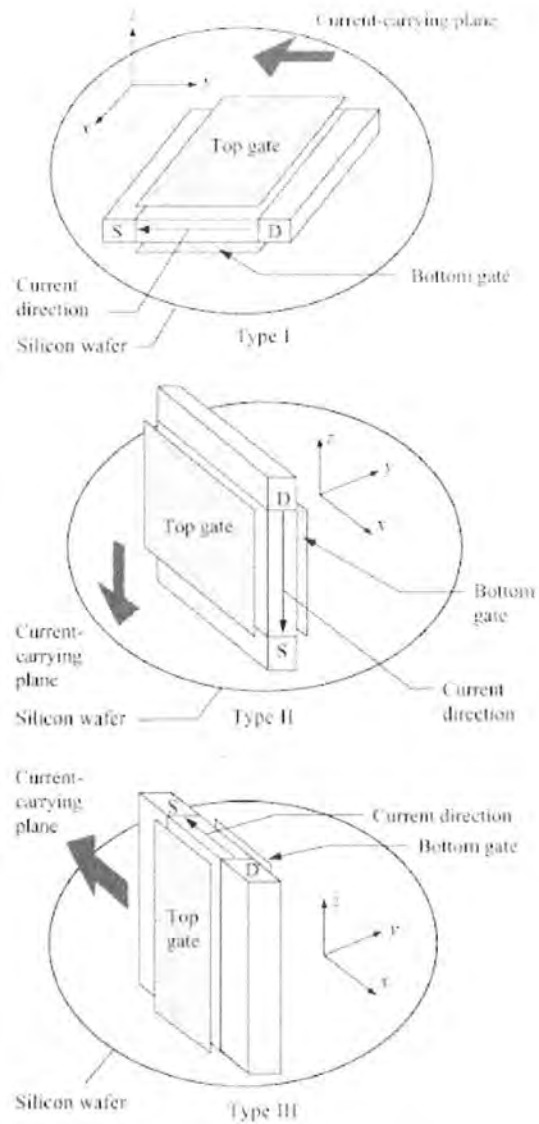


FIGURE 87. Schematic diagrams of three different double-gate structures. (Taken from Ref. 683. With permission.)

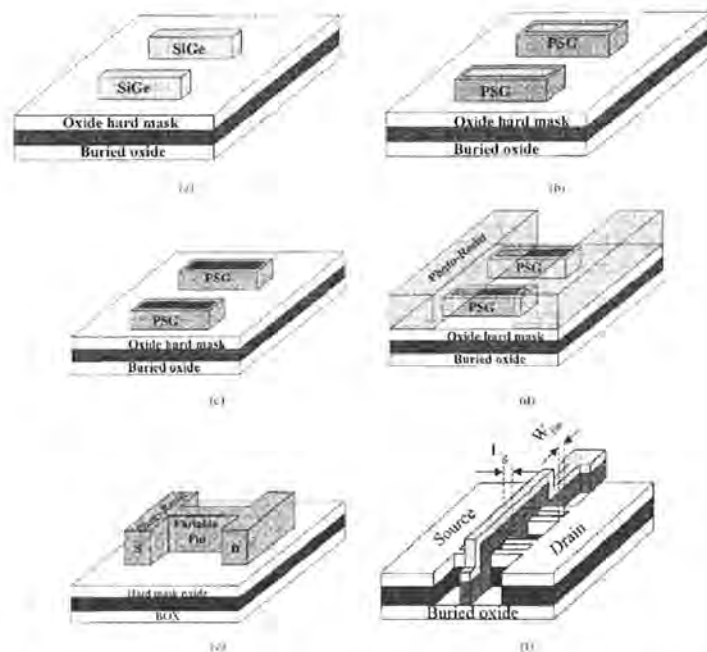


FIGURE 88. Schematic diagrams of FinFet fabrication. (Taken from Ref. 686. With permission.)

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