

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Taiwan Semiconductor Manufacturing Company Ltd.,
Petitioner,

v.

Marlin Semiconductor Limited,
Patent Owner.

Case No. IPR2026-00058

U.S. Patent No. 7,288,822

**DECLARATION OF DR. JACK LEE REGARDING
CLAIMS 1-14 OF U.S. PATENT NO. 7,288,822**

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I, Jack Lee, declare as follows:

I. INTRODUCTION

1. My name is Jack Lee.

2. I am making this declaration at the request of Taiwan Semiconductor Manufacturing Company Ltd. (“TSMC” or “Petitioner”) as an independent expert consultant in this proceeding before the United States Patent and Trademark Office and to provide testimony pertinent to TSMC’s Petition for *Inter Partes* Review of U.S. Patent No. 7,288,822 (“’822 patent”). I understand that Petitioner is challenging the patentability of claims 1-14 of the ’822 patent (“Challenged Claims”).

II. QUALIFICATIONS AND EXPERIENCE

1. My qualifications generally are set forth in my *curriculum vitae*, which is submitted as **Appendix A**.

2. I am an expert in the field of semiconductor design and process technology and have over forty years of first-hand experience as a researcher, educator, and consultant in this field.

3. I received a B.S. degree in Electrical Engineering, with highest honors, in 1980, and an M.S. degree in Electrical Engineering in 1981, both from University of California, Los Angeles. I received a Ph.D. degree in Electrical Engineering in 1988 from University of California, Berkeley (“UC Berkeley”).

4. From 1979 to 1984, I was a Member of Technical Staff at the TRW Microelectronics Center, in the High-Speed Bipolar Device Program. I worked on bipolar device/circuit design, fabrication, and testing. I was promoted to Engineering Group Leader level in 1983.

5. I received several academic honors while at UC Berkeley. For example, I won the Best Paper Award from the Institute of Electrical and Electronics Engineers (“IEEE”) International Reliability Physics Symposium in 1988. I was also awarded a Lectureship with my own teaching assistant from UC Berkeley.

6. After receiving my Ph.D. in August 1988, I joined the faculty at The University of Texas at Austin (“UT Austin”). As a faculty member, I have taught numerous courses in semiconductor device fabrication and design, at both the undergraduate and graduate levels. I have supervised over 40 students who received their doctoral degrees under my guidance. Since September 2000, I have held the Cullen Trust for Higher Education Endowed Professor in Engineering in the Department of Electrical and Computer Engineering at UT Austin. In September 2023, I was promoted to the Professor Emeritus level.

7. My current research and teaching interests encompass semiconductor devices and technologies including strained silicon metal-oxide-semiconductor field effect transistor (“MOSFET”) technologies, 3D structures such as FinFETs or tri-gate

MOSFETs, ultra-thin insulating layers, high-K gate dielectrics and gate electrodes, fabrication processes, electrical and material characterization, reliability and modeling, packaging technologies, dielectric and passivation processes, display technologies, photovoltaic and solar cell technologies, semiconductor memory applications, and alternative channel materials.

8. I have been invited to give talks, teach short courses and participate in panel discussions at numerous conferences specifically on the topic of fabrication processes for nanoscale devices such as strained silicon MOSFETs, FinFETs and gate-all-around MOSFETs, ultra-thin insulating layers, high-K gate dielectrics, gate electrodes, device reliability and semiconductor memory devices. This includes prestigious conferences such as the Symposium on VLSI Technology, the IEEE International Electron Devices Meeting, and other global forums. My research group at The University of Texas at Austin is recognized as a pioneer in developing strained silicon, high-K gate dielectric metal-gate processes for nanoscale MOSFETs including FinFETs. I have extensive experience in this field, with numerous publications in journals and conference proceedings on the topics of nanoscale MOSFETs and FinFETs, fabrication processes, characterization, and device reliability.

9. My research has been partially supported by grants from the National Science Foundation, the Texas Advanced Research Program, the Semiconductor Research Corporation (SRC), SEMATECH, Texas Emerging Technology Funds, and others. I have authored over 600 journal publications and conference proceeding papers and have coauthored 8 book and book chapters on semiconductor technologies. I am a named inventor of 9 U.S. patents. I have also received numerous teaching and research awards, e.g., inventor recognition and best paper awards.

10. In 2002, I became an IEEE fellow for my “contributions to the understanding and development of ultra-thin dielectrics and their application to silicon devices.” I was also an IEEE Electron Devices Society Distinguished Lecturer from 2004 to 2016.

11. I have served in various technology consulting and business advisor roles. For example, I have been teaching short courses on semiconductor device physics and technologies at various semiconductor companies and consortiums (e.g., SEMATECH). I have also organized several international conferences and have given lectures at numerous conferences and symposia, including the International Symposium on VLSI Technologies, the IEEE Symposia on VLSI Technology, and the IEEE International Electron Devices Meeting. These conferences are some of the most prestigious in the field.

3. Taken as a whole, my academic and practical experience has provided me a substantial basis upon which to evaluate the technology that is in question in the claims of the '822 patent. Based on my experience and education, and the acceptance of my publications and professional recognition by peers in my field, I believe that I am qualified to opine as to the knowledge and level of skill of one of ordinary skill in the art at the time of the alleged invention of the '822 patent (which I further describe below) and what such a person would have understood at that time, and the state of the art during that time.

III. LEGAL PRINCIPLES

4. I am not an attorney. For the purposes of this declaration, I have been informed about certain aspects of the law that are relevant to my opinions. My understanding of the law was provided to me by Petitioner's attorneys.

A. Scope of Opinion

5. I have been informed and understand that the petitioner in an *inter partes* review may request cancellation of claims as unpatentable only on grounds that such claims are anticipated or would have been obvious to a person of ordinary skill in the art at the time of the purported invention, and only on the basis of prior art consisting of patents and/or printed publications. My opinions in this matter address only such grounds.

B. Anticipation

6. I have been informed that a patent claim is anticipated and therefore unpatentable if every element of the claim is present in a single prior art reference.

C. Obviousness

7. I understand that a claim is unpatentable if, at the time the alleged invention was made, it would have been obvious to a person of ordinary skill in the art. I understand that a claim can be obvious based on the teachings or suggestions of either a single prior art reference or a combination of two or more prior art references. I understand that the obviousness analysis requires an understanding of the scope and content of the prior art, any differences between the prior art and the alleged invention, and the level of ordinary skill in evaluating the pertinent art.

8. I understand that in order to be considered for obviousness, prior art must be analogous to the patent at issue. I further understand that art is analogous if it either pertains to the same field of endeavor as the patent at issue or, alternatively, if it is reasonably related to the problem faced by the inventor(s) of the patent at issue.

9. I understand that a claim would have been obvious if it unites old elements with no change to their functions or alters prior art by mere substitution of one element for another known in the field such that the combination yields

predictable results. Also, I understand that obviousness does not require a physical combination or example, but rather is concerned with what the combined teachings would have taught or suggested to persons of ordinary skill in the art at the time of the alleged invention.

10. In connection with obviousness, I have been informed that there must have been some reason or motivation for a person of ordinary skill in the art to have combined or modified the relevant teachings in the prior art to obtain the claimed invention, and one of ordinary skill in the art must have had a reasonable expectation of success making the combination or modification.

11. I understand that a claim would have been obvious if a person of ordinary skill in the art would have had reason to combine multiple prior art references or add missing features to reproduce the alleged invention recited in the claims. I further understand that there is no rigid requirement of finding an express teaching, suggestion, or motivation to combine within the references, although such an express teaching or suggestion may be helpful in identifying a reason for the combination.

12. If a person of ordinary skill in the art can implement a predictable variation, that variation is likely unpatentable as obvious. For the same reason, if a technique has been used to improve one device and a person of ordinary skill in the

art would have recognized that it would improve similar devices in the same way, using the technique to make such an improvement would have been obvious.

13. I understand that when considering obviousness, it is important not to use the benefit of hindsight derived from the patent being considered. I also understand that one of ordinary skill in the art has ordinary creativity (i.e., is not a mindless automaton).

14. In sum, I understand that a determination of whether a claim would have been obvious is based upon the following non-exclusive considerations:

- whether prior art references teach or disclose known concepts combined in familiar ways, such that when combined they would yield predictable results;
- whether a person having ordinary skill in the art could implement a predictable variation, and would see the benefit of doing so;
- whether the claimed elements represent one of a limited number of known design choices, where those skilled in the art would have had a reasonable expectation of success in implementing that design choice;
- whether a person having ordinary skill would have been motivated based on the prior art to combine known elements in the manner described in the claim;

- whether there is a teaching or suggestion in the prior art to make the modification or combination of elements claimed in the patent; and
- whether the alleged invention applies a known technique that had been used to improve at least one similar device or method in a similar way.

15. I further understand that certain additional factors, commonly referred to as secondary considerations or objective indicia, may support or rebut the obviousness of a claim. I understand that secondary considerations include, among other things, commercial success of the patented invention, skepticism of those having ordinary skill in the art at the time of invention, unexpected results of the invention, any long-felt but unsolved need in the art that was satisfied by the alleged invention, the failure of others to make the alleged invention, praise of the alleged invention by those having ordinary skill in the art, copying of the alleged invention by others in the field, and contemporaneous and independent invention by others. I understand that there must be a nexus (i.e., a connection) between any such secondary considerations and the alleged invention. I also understand that secondary considerations cannot be used to overcome anticipation. I further understand that contemporaneous and independent invention by others is a secondary consideration tending to show obviousness.

16. I reserve the right to respond to any allegations that Patent Owner may put forth in this proceeding suggesting that secondary considerations tend to rebut the obviousness of any claim of the '822 patent as discussed in this declaration.

D. Claim Dependency

17. I understand patents may include two types of claims: independent claims and dependent claims. An independent claim stands alone and simply recites the limitations it covers. In contrast, a dependent claim depends from either an independent claim or another dependent claim, and incorporates all the limitations recited in the claim or claims from which it depends along with the limitations it recites itself.

* * *

18. The analysis that follows in this declaration is in accordance with the above-stated legal principles.

IV. MATERIALS CONSIDERED

19. In forming my opinions, in addition to my knowledge and experience, I have considered the materials cited herein and listed in **Appendix B**.

V. PRIORITY DATE

20. I have been informed that the '822 patent was filed on April 7, 2006. I have also been informed that the '822 patent does not claim the benefit of an earlier filing date. I have formed my opinions in reference to this filing date. Should Patent

Owner suggest a different priority date, I reserve the right to revise my opinions accordingly.

VI. LEVEL OF ORDINARY SKILL IN THE ART

21. I understand that when considering the claims of the '822 patent and the prior art, I must do so from the perspective of one of ordinary skill in the art as of the patent's effective priority date.

22. I have been informed and I understand the factors to be considered in determining who would be a person of ordinary skill in the art include: (1) the types of problems encountered in the art; (2) the prior art solutions to those problems; (3) the rapidity with which innovations are made; (4) the sophistication of the technology; and (5) the educational level of active workers in the field.

23. Based on these factors as well as my experience and expertise, a person of ordinary skill in the art as of the claimed priority date of the '822 patent (also called a "POSITA") would have had a master's degree in electrical engineering, physics, chemistry, materials science, or a related field and three years of work experience in semiconductor manufacturing, such as, for example, in integrated circuit device (or transistor) design and/or manufacturing. Additional relevant education could substitute for professional experience, and significant work experience or training could substitute for formal education.

24. My analysis and opinions herein regarding the '822 patent have been based on the perspective of a person of ordinary skill in the art as of the priority date for the '822 patent (i.e., April 7, 2006).

25. I have the qualifications and experience necessary to assess the '822 patent based on the perspective of a person of ordinary skill in the art, including as of the priority date for the '822 patent. *See* Section II.

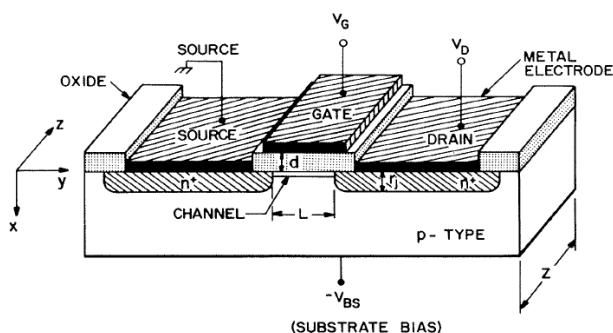
VII. TECHNOLOGY BACKGROUND

A. Metal-Oxide-Semiconductor Field Effect Transistors (“MOSFETs”)

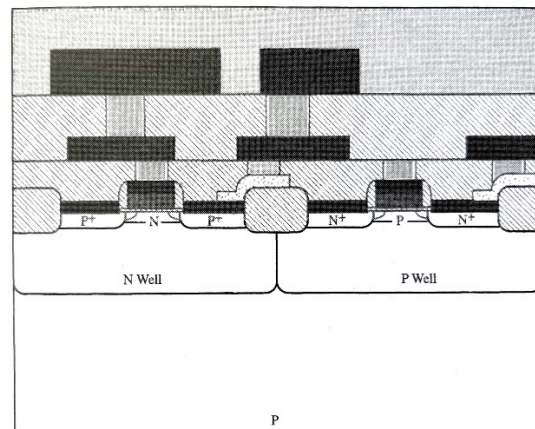
26. A transistor is an electronic device used to control the flow of electrical current, i.e. the flow of charge, in electronic circuits. To control the flow of electrical current, transistors operate like a “switch” that can be turned ON or OFF. On the one hand, when the transistor is OFF, it blocks the flow of electrical current. On the other hand, when the transistor is ON, it allows current to flow through it.

27. One type of transistor that is commonly used in electronic circuits is the Metal-Oxide-Semiconductor Field-Effect-Transistor (“MOSFET” or “MOS transistor”). MOSFETs have a current input (called source) and a current output (called drain). EX1008-Sze, 433-34, Figs. 3, 6; EX1009-Plummer, 76-90. Electrodes formed on the source/drain regions allow current to flow into and out of the MOSFET. *Id.* MOSFETs also have a channel region between the source and

drain regions and a gate over the channel region. *Id.* A gate dielectric (also called gate “oxide” or gate “insulator”) separates the gate of a MOSFET from the channel region. *Id.* Applying an appropriate voltage to the gate electrode causes a conductive channel to form in the channel region, electrically connecting the source and drain. When the conductive channel is formed, the MOSFET is turned ON and current can flow between the source and the drain. When the conductive channel is not present, the MOSFET is OFF and the flow of electrical current between the source and the drain is blocked. The voltage applied to the gate controls the conductivity (i.e., the ability to conduct electric current) of the conductive channel, thereby controlling the source-drain current. *Id.*



EX1008-Sze, Fig. 3



EX1009-Plummer, Fig. 1-11

B. Semiconductor Materials

28. Transistors, such as MOSFETs, in integrated circuits are formed from semiconductor materials. EX1008-Sze, 431-32; EX1009-Plummer, 7-8, 13. Semiconductors are materials with a conductance (i.e., how easy it is for a charge to flow) somewhere in between a conductor (a material having high conductance) and an insulator (a material having low conductance). *Id.* Most modern microelectronic circuits use silicon (“Si”) as the semiconductor material to form transistors in integrated circuits. *Id.*

29. Impurities can be added to a semiconductor material to alter its electrical and physical properties. Impurities called “dopants” are those that introduce extra charge carriers – called electrons or holes (which represent the absence of an electron in a semiconductor lattice) – into the semiconductor material. Phosphorous (“P”), arsenic (“As”) and antimony (“Sb”) are common examples of “n-type” impurities that introduce extra electrons into a semiconductor material. Boron (“B”), gallium (“Ga”) and indium (“In”) are common examples of “p-type” impurities that introduce extra holes into a semiconductor material.

30. Semiconductor devices (such as transistors) and integrated circuits are fabricated on a semiconductor substrate, typically a large circular piece of silicon called a “wafer.” Subsequent fabrication steps include etching and depositing

structures on the semiconductor substrate and cutting the wafer into smaller pieces called “dies” that can be incorporated into electronic devices. *See, e.g.*, EX1008-Sze, 433-434, Fig. 3.

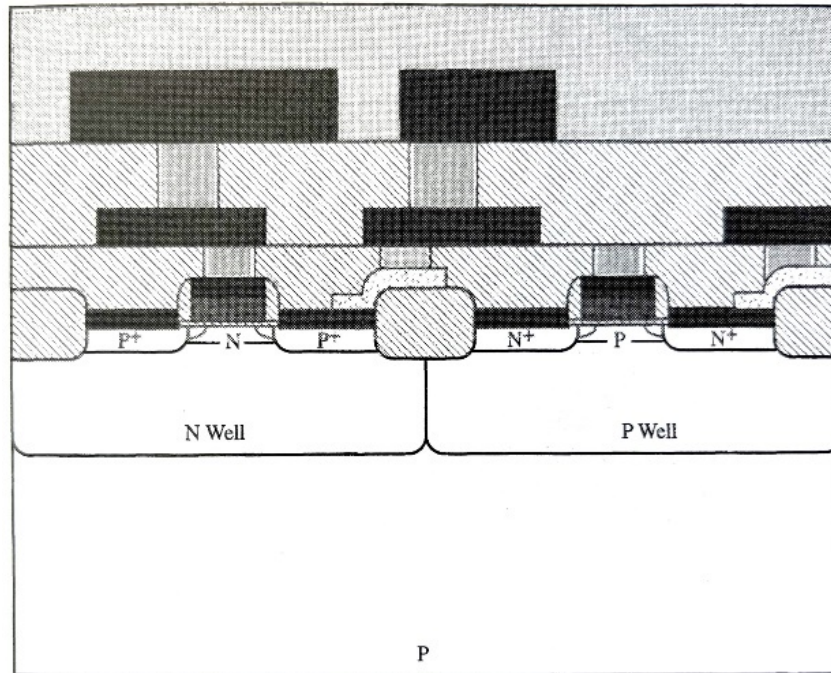
C. MOSFET Fabrication

31. MOSFET fabrication includes selectively doping portions of the substrate to define the source, drain, and channel regions. *See* EX1008-Sze, 433-34; EX1009-Plummer, 76-82. For example, a PMOS transistor has n-type well (or substrate) regions with p-type source and drain regions, and a conductive p-type channel forms when the gate voltage is appropriately negative. An NMOS transistor has p-type well (or substrate) regions with n-type source and drain regions, and a conductive n-type channel forms when the gate voltage is appropriately positive. EX1009-Plummer, 12-13, 50-51, Figs. 1-11, 2-2.

32. Both NMOS and PMOS transistors are often integrated on the same chip to form a complementary MOS (CMOS) circuit, enabling efficient logic design with low power consumption. *Id.*

33. As shown in the figure below, CMOS circuits generally include MOSFET transistors that are formed in respective “well regions.” An n-type well region (“N-well”) is used for PMOS transistor and a p-type well region (“P-well”) is used for NMOS transistors. *See id.*, 51-52, Figs. 1-11, 2-2. The use of N-wells

and P-wells to form MOSFET transistors in CMOS integrated circuits is called a twin-well process and is known to help control the characteristics of the MOSFET transistors during manufacturing. *Id.*, 52; *see also* EX1010-Quirk, 205-07, Figs. 9.8, 9.9; EX1004-Koontz ¶[0041], ¶[0053], Figs. 3, 4A-4N; EX1011-Murthy, 3:14-4:6, Fig. 4; EX1012-Kim, ¶[0054]; EX1009-Plummer, Fig. 2-29; EX1013-Cook, ¶¶[0022]-[0023], Figs. 1-11.



EX1009-Plummer, Fig. 1-11

D. Strained Silicon Technology

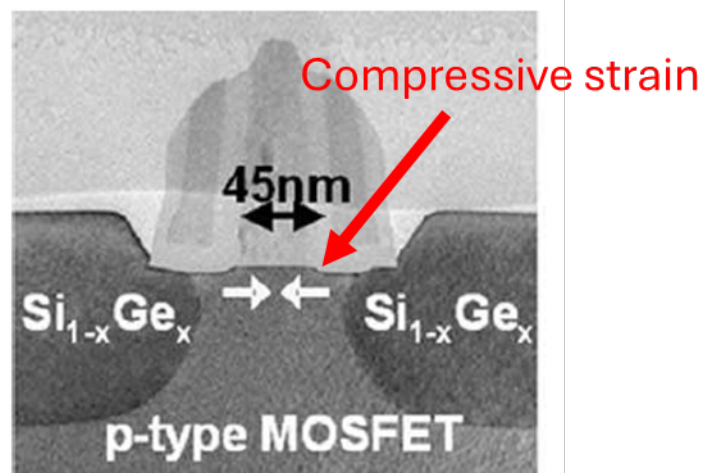
34. Strained silicon technology is a technique for applying physical strain (i.e., either tensile strain or compressive strain) to the channel regions of a MOSFET. Doing so can increase the mobility of charge carriers (electrons or holes) in the

channel regions. The increased mobility reduces the channel's electrical resistance, allowing current to flow faster, thereby improving operating speed. EX1014-Thompson, 191-93; EX1015-Sun, 2.

35. Physical strain can be introduced in the channel region by adjusting the lattice parameter (which measures the spacing between neighboring atoms in the material) of a semiconductor material surrounding the channel region. For example, the lattice parameter of a layer of silicon can be increased by mixing the silicon with a larger element such as germanium (forming silicon-germanium or "SiGe") or decreased by mixing the layer of silicon with a smaller element such as carbon (forming silicon-carbon or "SiC"). When silicon-germanium or silicon-carbon are epitaxially grown on or next to a silicon channel region, they introduce strain within the channel region. Whether the strain is tensile or compressive depends on whether the surrounding material has a smaller or larger lattice parameter than silicon. Thus, silicon-germanium (with a larger lattice parameter) introduces compressive strain while silicon-carbon (with a smaller lattice parameter) introduces tensile strain. The percentage of silicon in the mixture relative to the other elements (e.g., germanium or carbon) in the mixture determines how small or large the difference is between the lattice parameter of the silicon mixture and the lattice parameter of pure silicon.

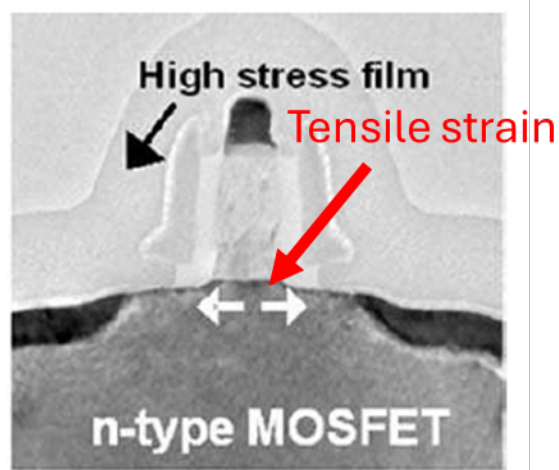
EX1017-Murthy482, 1:45-48; EX1018-Richter, 41, 46; EX1027-Dismukes, Fig. 3, Tbl. IV.

36. The performance of PMOS transistors improves when compressive strain (forces pushing or compressing the channel region) in the direction of current flow is applied to the channel region of the transistor. To apply compressive strain to the channel region, silicon-germanium can be used in the source/drain regions of a PMOS transistor. As illustrated below, the larger lattice parameter of silicon-germanium in the source/drain regions of the PMOS transistor relative to pure silicon in the channel region creates compressive strain in the direction of current flow. By 2005, the use of silicon-germanium in the source/drain regions of PMOS transistors had doubled PMOS operating speeds.



EX1014-Thompson, Fig. 1 (excerpt).

37. Similarly, the performance of NMOS transistors improves when tensile strain (forces pulling or stretching the channel region) in the direction of current flow is applied to the channel region. To apply tensile strain to the channel region, silicon-carbon can be used in the source/drain regions of an NMOS transistor. *See* EX1006-Orlowski, 1:15-23.



EX1014-Thompson, Fig. 1 (excerpt).

The smaller lattice parameter of silicon-carbon in the source/drain regions of the NMOS transistor relative to pure silicon in the channel region creates tensile strain in the direction of current flow. *See* EX1006-Orlowski, 6:15-28; EX1004-Koontz ¶[0047], ¶¶[0059]-[0060]; EX1005-Samoilov, ¶[0009], ¶[0068]. The use of silicon-carbon in the source/drain regions were also well-known by 2006.

38. Strained silicon technology has a long history, *see* EX1015-Sun, 1-2, and was well-known by April 2006, *see* EX1001-USP'822, 1:17-27, 1:40-42, Fig.

1B. For example, two generations of high-volume commercial devices, including Intel's 90 nm technology and Intel's 65 nm technology, already used this technique by then. *See* EX1014-Thompson, 191 (describing Intel's 90 nm devices); EX1016-Bai, 1 (describing Intel's 65 nm devices). Moreover, because smaller transistors experience less strain for a given germanium or carbon concentration in the source/drain regions, germanium and carbon concentrations in the source/drain regions increased as transistors shrank. *See* EX1016-Bai, 28.2.1 (noting Intel "increase[ed] Ge content in the SiGe film" when scaling to 65 nm).

E. Silicon-Germanium and Silicon-Carbon Source/Drain Regions with a Non-Uniform Lattice Parameter

39. To form a MOSFET with a strained silicon channel, during manufacturing, an opening is formed in the substrate where the source/drain region is located, and the opening is filled in with silicon-germanium or silicon-carbon. However, because silicon-germanium and silicon-carbon have a different lattice parameter than the silicon substrate, strain accumulates in the material as it grows, which may cause dislocations. EX1017-Murthy482, 1:49-56; 46-47; EX1020-Zhu, 5:11-13. Essentially, the material being grown cracks due to stress.

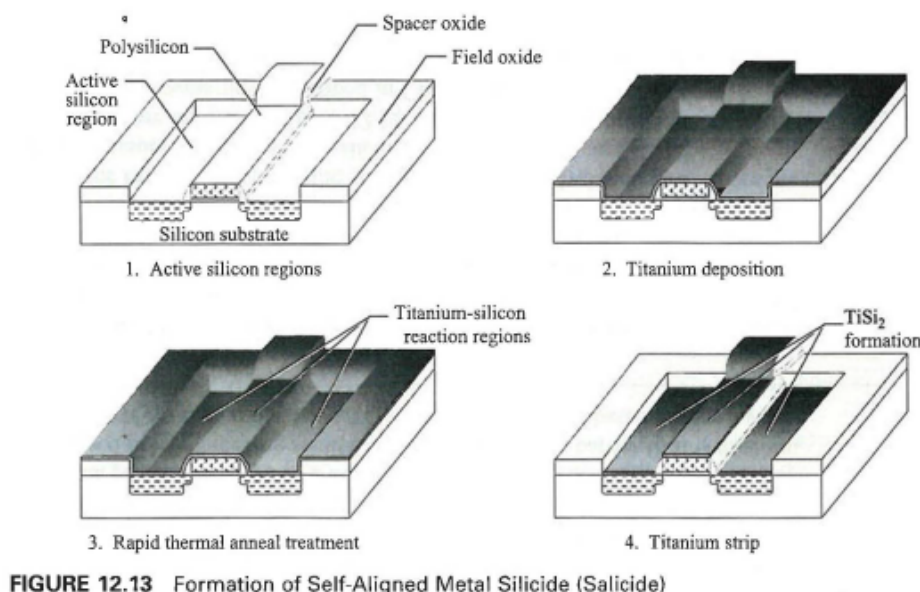
40. It was well-known to suppress dislocations by gradually increasing the concentration of germanium or carbon, thereby gradually adjusting the lattice parameter, as the source/drain region is formed, resulting in a graded source/drain

region. *See* EX1020-Zhu, 1:56-64, 5:26-35; EX1006-Orlowski, 5:15-29; EX1005-Samoilov ¶[0030], ¶[0072], ¶[0074]; EX1004-Koontz ¶[0034], ¶¶[0038]-[0039], Fig. 2C; EX1021-Lochtefeld, ¶[0003]. For example, in the case of a graded silicon-germanium source/drain region, the ratio between silicon and germanium is changed as the silicon-germanium material is grown. Since a graded source/drain region “does not have a sharp interface (where the dislocations are generated) between SiGe [silicon-germanium] [or silicon-carbon] and Si, dislocations are not easily produced.” EX1020-Zhu, 1:59-64. As an added benefit, this technique also “provide[s] a method to optimize stress in order to enhance device performance.” EX1020-Zhu, 1:59-64.

F. Silicidation

41. Electrical contacts on the top surface of the source/drain regions MOSFET allow current to flow through the MOSFET. A conductive metal-silicon compound called a silicide is typically used to form the contacts by providing an interface between the semiconductor source/drain regions and the metal interconnects. *See, e.g.,* EX1009-Plummer, 82-84, 699-702, Fig. 11-14; EX1010-Quirk, 214, 309-12, Figs. 9.19, 12.9-13.

42. Silicides are typically formed by self-aligned silicidation, called a salicide process, illustrated below.



EX1010, Fig. 12.13

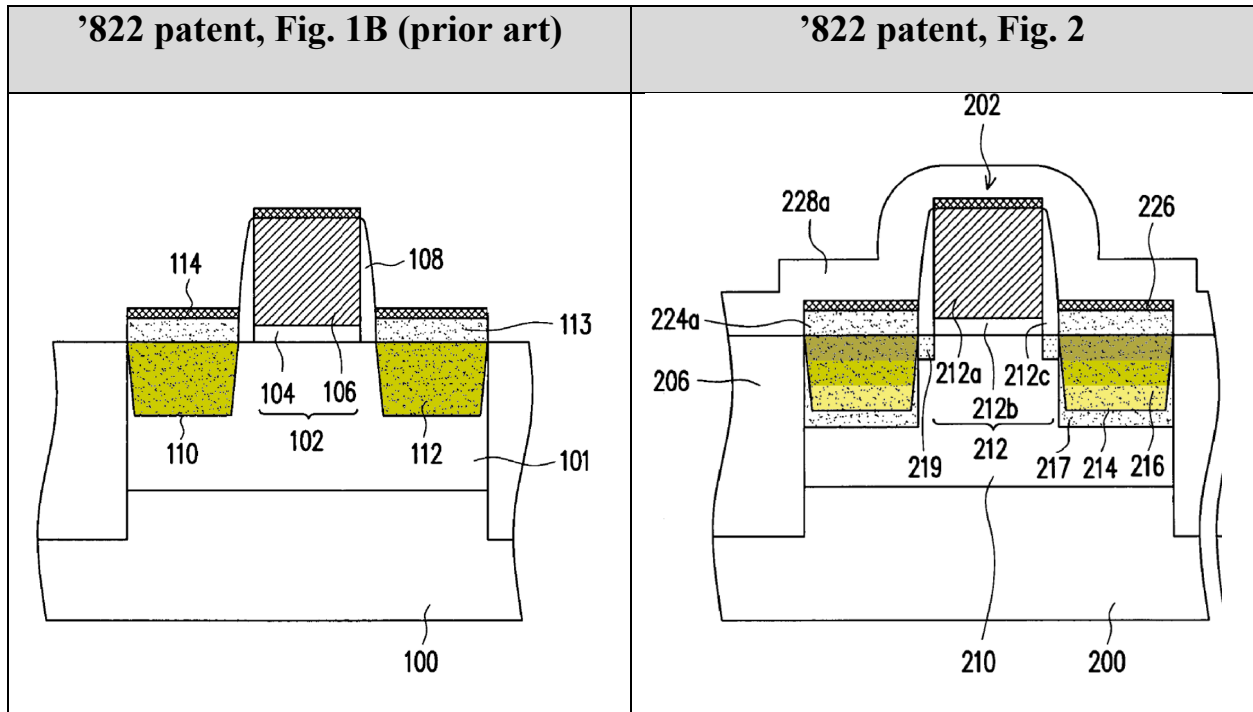
In the salicide process, a metal (e.g., titanium) deposited over the wafer is heated (i.e., annealed) to cause a reaction between the metal and any silicon material in contact with it. EX1009-Plummer, 82-84; EX1010-Quirk, 214, 311-12, Fig. 12.13; EX1023-Zhang, 9-12, Fig. 8. The metal does not react with insulators like SiO_2 or Si_3N_4 , so the unreacted metal in contact with other parts of the wafer can be selectively removed, leaving behind only the silicide regions.

VIII. OVERVIEW OF THE '822 PATENT

A. Summary of the '822 Patent

43. The specification of the '822 patent describes MOSFET devices with silicon-germanium or silicon-carbon source/drain regions that induce strain in the silicon channel region. EX1001-USP'822, 1:6-11; *see also id.*, 1:37-44, 7:23-33.

According to the '822 patent, “defects easily occur at the interface of the [silicon germanium (or silicon-carbon)] layer and the substrate lowering the device performance.” *Id.*, 1:45-51. The '822 patent states that the occurrence of defects can be reduced by using source/drain regions “with a non-uniform lattice parameter distribution ... for decreasing the difference between the lattice parameters of the [source/drain] region and the substrate....” *Id.*, 1:57-62. The '822 patent’s approach (shown on the right) compared to a prior art approach (shown on the left) is illustrated below.



44. The MOSFET devices depicted in prior art Figure 1B (left) and Figure 2 (right) are similar, and both devices have respective source/drain regions (e.g., source/drain region 112 in Figure 1B and source/drain region 216 in figure 2).

However, the '822 patent states that in Figure 2(right), the silicon-germanium or silicon-carbon source/drain regions 216 have a non-uniform distribution, such as a “gradient distribution.” The inventors believed that this approach would reduce the likelihood of defects because the lattice parameter near the bottom of the source/drain region is closer to that of the substrate than the lattice parameter towards the top of the source/drain region. *Id.*, 1:31-34, 4:65-5:19, 5:61-6:2.

45. In addition to its disclosure of a non-uniform lattice parameter, the '822 patent describes features of the silicide contacts on the source/drain regions and the dopants implanted “around and under” the source/drain regions. *Id.*, 1:51-53, 4:20-24, 5:19-24, 5:55-60, 6:54-62, 7:1-13.

B. Prosecution History

46. The claims of the '822 patent did not receive any prior art rejections and the reason for allowance stated by the patent examiner were vague and non-specific. *See* EX1002, 40-52, 61-65. The Examiner’s statement of reasons for allowance suggests the claims were allowed because the strain-inducing source/drain layers have a graded composition:

The prior art of record does not disclose, make obvious, or otherwise suggest the structure of the applicant's together with the other limitations of the independent claims, such as “a first strained layer of the first conductivity type in a first opening in

the second well beside the first gate structure, wherein a difference between a cell parameter of a portion of the first strained layer near a bottom of the first opening and a cell parameter of the substrate is smaller than a difference between a cell parameter of a portion of the first strained layer apart from the bottom of the first opening and the cell parameter of the substrate.” *Id.*, 63.

47. Notably, the Applicant did not submit any prior art references to the USPTO with the filing or during the brief prosecution of the ’822 patent. Each of the references on the face of the ’822 patent was cited by the examiner. EX1001-USP’822 (“References Cited” all “cited by examiner”).

IX. CLAIM CONSTRUCTION

48. For purposes of my opinions, I applied each claim term’s ordinary and customary meaning to a person of ordinary skill in the art read in light of the specification and prosecution history, unless otherwise specified.

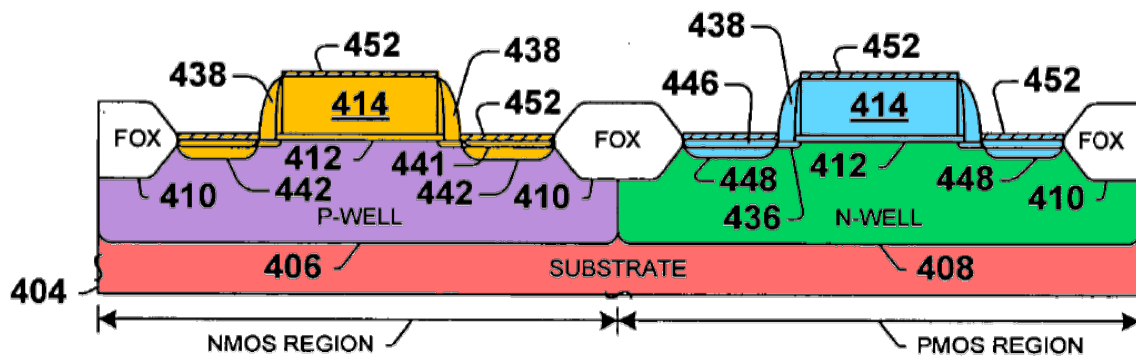
X. OVERVIEW OF THE PRIOR ART

49. Before discussing the specific grounds, I provide below a brief overview of the references in the grounds.

A. Koontz

50. Koontz (U.S. Patent Appl. Pub. No. 2006/0134873) is titled “Tailoring channel strain profile by recessed material composition control” and was filed on December 22, 2004.

51. Like the '822 patent, Koontz teaches strained-channel MOSFETs with silicon-carbon and silicon-germanium source/drain regions 441 and 446, respectively. The strained channel MOSFETs include PMOS transistors (blue) formed on N-well regions (green) and NMOS transistors (orange) formed on P-well regions (purple). The N-well and P-well regions are formed on a substrate 404 (red).



EX1004-Koontz, Fig. 4N (annotated)

52. The silicon-carbon and silicon-germanium source/drain regions 441 and 446 (which Koontz also calls “composition controlled filled recess structures”) have a non-uniform or graded composition. For example, Koontz explains that the silicon-carbon and silicon-germanium source/drain regions 441 and 446 can have a

linear strain profile (dashed line 252 below), “which can generally be obtained by linearly adjusting” the concentration of the silicon-carbon and silicon-germanium source/drain regions 441 and 446. EX1004-Koontz, Fig. 2C, ¶¶[0038]-[0039]. Alternatively, Koontz explains that these regions can exhibit a non-linear strain profile (dash-dotted curve line 253 below), obtained by “non-linearly adjusting” the composition during deposition. *Id.*

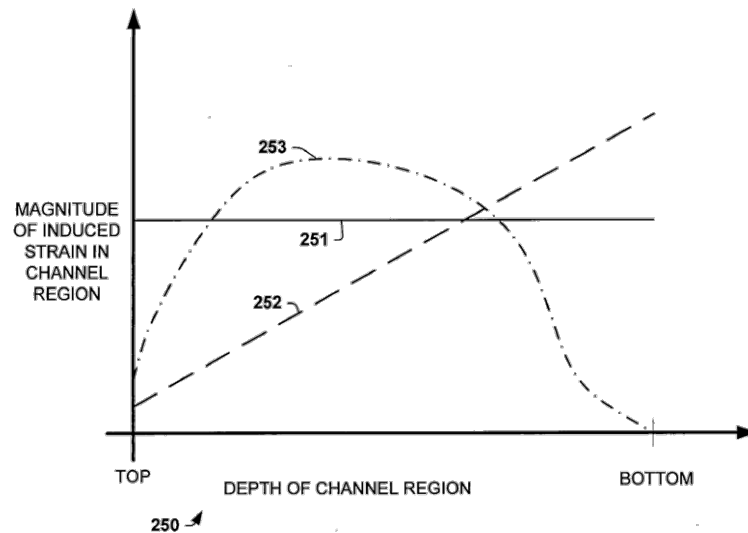


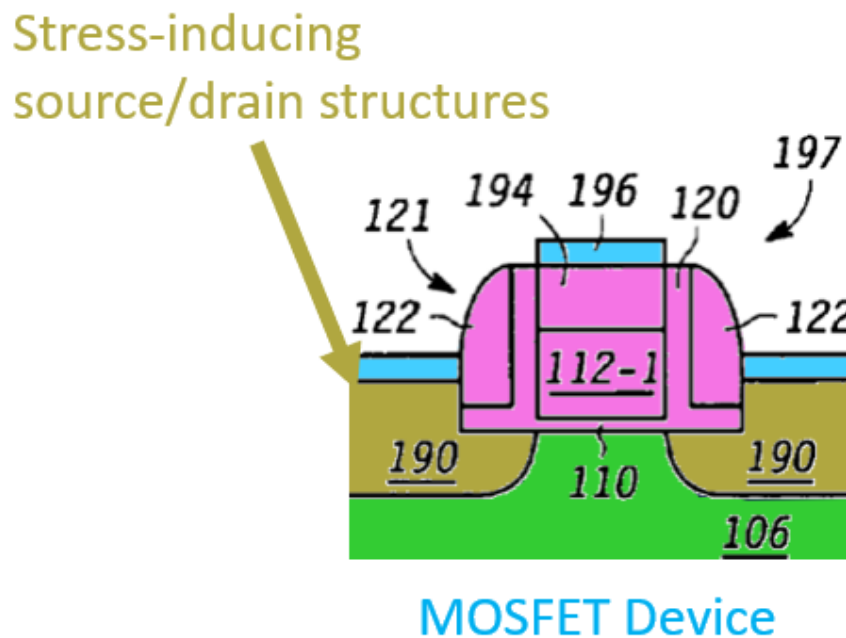
FIG. 2C

EX1004-Koontz, Fig. 2C

B. Orlowski

53. Orlowski (U.S. Patent No. 7,238,580) is titled “Semiconductor Fabrication Process Employing Stress Inducing Source Drain Structures With Graded Impurity Concentration” and was filed on January 26, 2005.

54. Like the '822 patent, as shown in Figure 13 of Orlowski below, Orlowski teaches strained-channel MOSFET devices with silicon-germanium or silicon-carbon source/drain regions 190 (which it calls “stress-inducing source/drain (SISD) structures”). EX1006-Orlowski, 2:34-37.

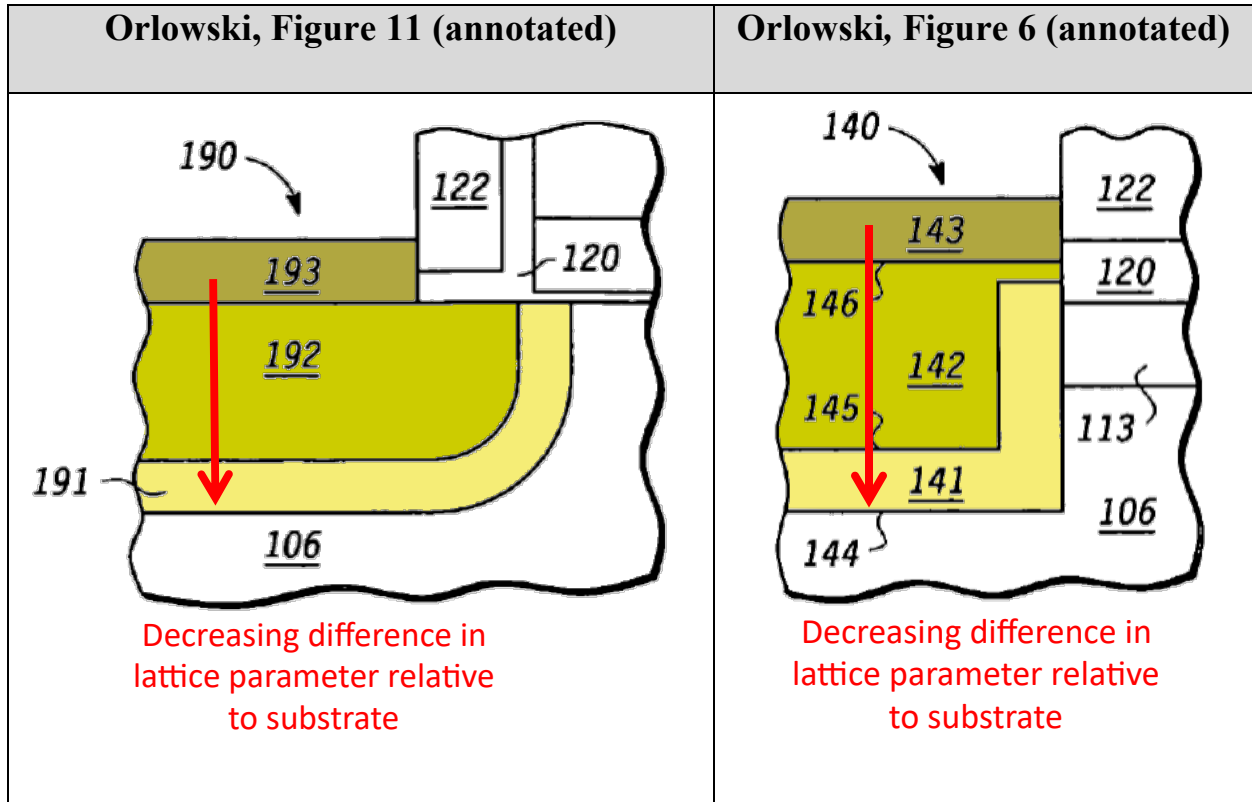


EX1006-Orlowski, Fig. 13 (annotated).

55. “The SISD structures are semiconductor structures having a lattice constant that differs from a lattice constant of the semiconductor substrate....” EX1006-Orlowski, 2:37-40. The SISD structures comprise a semiconductor compound with a “first element (e.g., silicon) and a second element (e.g., germanium, carbon, et al.)” such that “[t]he percentage of the second element varies from the upper surface of the source/drain structure to a lower surface of the SISD

structure.” *Id.*, 2:40-45. For example, PMOS devices employ silicon-germanium SISD structures to apply compressive strain to the channel, whereas NMOS devices employ silicon-carbon SISD structures to apply tensile strain to the channel. *Id.*, 1:16-23, 6:15-28. Although Figure 13 above only illustrates SISD structures in the PMOS region, Orlowski explains that “[e]xtending the depicted processing sequence to encompass the case of two types of SISD structures would be obvious to one skilled in the art....” *Id.*, 4:1-10; *see also id.*, 7:40-47.

56. Orlowski further teaches silicon-germanium or silicon-carbon source/drain structures with a non-uniform lattice parameter, e.g., a lattice parameter with a gradient distribution. EX1006-Orlowski, 1:24-43, 2:34-55. For example, source/drain structures with a graded composition are illustrated in Figures 11 (left) and 6 (right). In both cases, the lattice parameter of the source/drain structures 190 and 140 (brown/yellow) approaches the lattice parameter of the substrate 106 in the regions that are closer to the substrate. EX1006-Orlowski, 8:17-21.



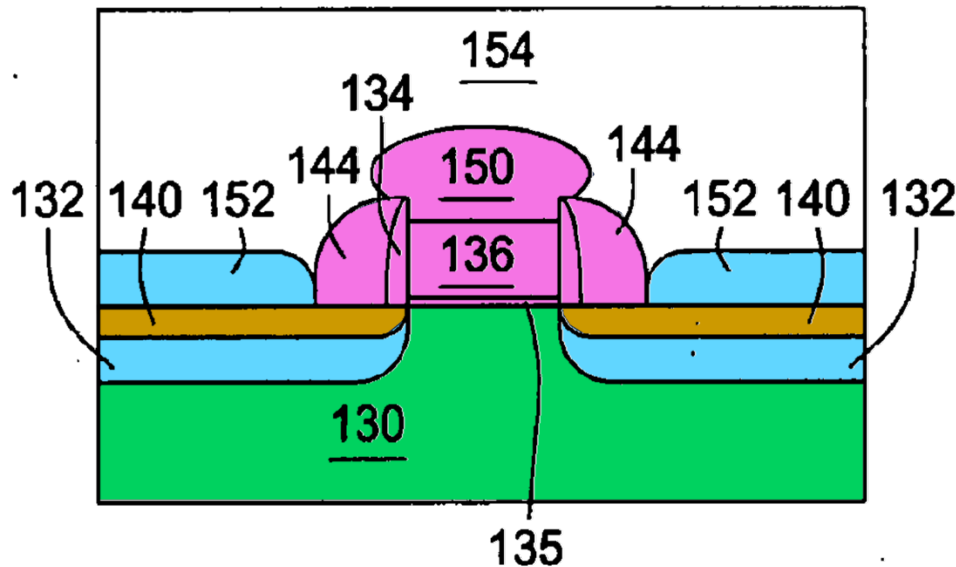
EX1006-Orlowski, Figs. 6, 11 (annotated).

57. For example, Orlowski explains that SISD structures 190 (brown) may comprise “a third layer 193 overlying a second layer 192 overlying a first layer 191” such that “the silicon percentage of SISD structure 190 [(brown)] is greater in first layer 191 than in second layer 192 and the silicon percentage in second layer 192 is greater than the silicon layer in third layer 193.” *Id.*, 8:10-21.

C. Samoilov

58. Samoilov (U.S. Patent Appl. Pub. No. 2005/0090082) is titled “Methods to Fabricate MOSFET Devices Using Selective Deposition Process” and was filed on May 14, 2004.

59. Like the '822 patent, as shown in Figure 2F of Samoilo below, Samoilo teaches a strained-channel MOSFET device with strain-inducing silicon-germanium or silicon-carbon layers 140 (brown).



EX1005-Samoilo, Fig. 2F (annotated)

60. In Samoilo, the “MOSFET devices may contain a PMOS or a NMOS component” and may be used “for CMOS device fabrication.” *Id.*, ¶[0009], ¶[0038]. To strain the channel region, these MOSFETs include a “silicon-containing compound deposited as a recessed source/drain...” *Id.*, ¶[0026]; *see also id.*, ¶[0005], ¶[0021], ¶[0039], Figs. 1A, 1B, 2B-2C. Specifically, Samoilo teaches a doped silicon-containing layer 140 for this purpose, which may comprise silicon-germanium (compressive strain for PMOS) or silicon-carbon (tensile strain for

NMOS). *See id.*, ¶¶[0005]-[0006], ¶¶[0008]-[0009], ¶[0021], ¶¶[0030]-[0032], ¶[0039], ¶[0072], ¶[0074], Figs. 2B-2C.

61. According to Samoilov, silicon-containing layer 140 may comprise multiple sub-layers having non-uniform concentrations of germanium or carbon in the silicon-germanium or silicon-carbon mixtures. For example, Samoilov teaches that the silicon germanium or silicon carbon layers 140 should be graded: “Multiple layers containing Si, SiGe, SiC or SiGeC may be deposited in varying order to form graded elemental concentrations of silicon-containing layer 140.” *Id.*, ¶[0032]; *see also id.*, ¶[0030] (describing a PMOS with a first SiGe layer with a concentration of 15 at % to 25 at % followed by a second SiGe layer with a concentration of 25 at % to 35 at %), ¶[0072], ¶[0074] (describing an NMOS with a first SiC layer with a concentration of 1.25 at % followed by a second SiC layer with a concentration of 1.75 at %), claim 1.

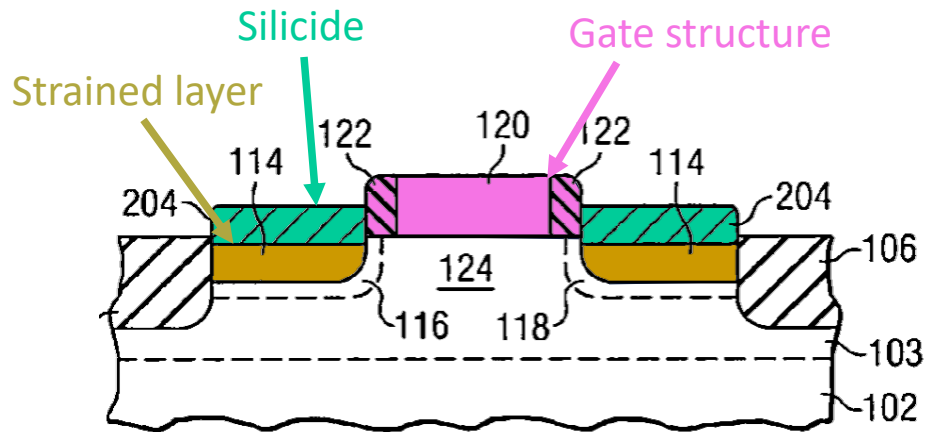
62. To form electrical contact to the silicon-germanium source/drain regions, Samoilov teaches a silicidation process that employs a silicon capping layer. First, “[s]ilicon-containing layer 148 is deposited on layer 140 (e.g., doped-SiGe). . . .” EX1005-Samoilov, ¶[0035]; *see also id.*, Fig. 2E. Silicon-containing layer 148 is a silicon capping layer, as it “contain[s] little or no germanium or carbon.” *Id.*, ¶[0036]. After forming this silicon capping layer, “a metal layer 154

is deposited over the features and the device is annealed.” *Id.*, ¶[0037]. As a result, the silicon capping layer 148 is “converted to metal silicide” layer 152. *Id.*; *see also id.*, Fig. 2F.

D. Sridhar

63. Sridhar (U.S. Patent Appl. Pub. No. 2005/0090082) is titled “Method and System for Improving Performance of MOSFETs” and was filed on October 28, 2003.

64. Like Koontz, Samoilov, and Orlowski, Sridhar teaches strained-channel MOSFETs with source/drain regions having a lattice parameter that differs from that of silicon. EX1007-Sridhar, ¶¶[0003]-[0004], [0014]. For example, Sridhar teaches strained-channel MOSFETs with silicon-germanium source/drain regions 11, explaining that “[o]ne way to increase drive current in MOSFETs is to utilize Silicon-Germanium (SiGe) epitaxial layers in the source and drain regions to introduce compressive stress in the channel.” EX1007-Sridhar, ¶[0003]; *see also id.*, ¶[0010]. As Figure 1D illustrates, source/drain regions 116 and 118 “include SiGe layers 114 that are formed within substrate 102....” *Id.*, ¶[0012].



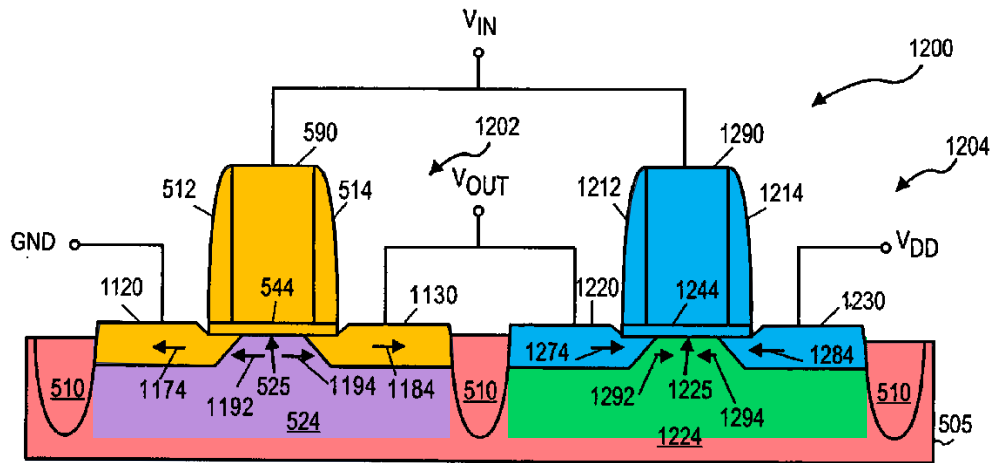
EX1007-Sridhar, Fig. 1D

65. Sridhar notes, however, that the process of forming silicide contacts on the strain-inducing source/drain regions “may counteract the benefits by increasing source/drain resistances.” *Id.*, ¶¶[0003], ¶[0014]. To address this issue, Sridhar proposes capping the source/drain regions with a “thin layer of silicon” and then forming a silicide contact layer using the thin layer of silicon. *Id.*, ¶¶[0004]-[0005], ¶¶[0014]-[0017].

E. Murthy

66. Murthy (U.S. Patent No. 7,195,985) is titled “CMOS Transistor Junction Regions Formed By a CVD Etching And Deposition Sequence” and was filed on January 4, 2005.

67. Like the '822 patent, as shown in Figure 12 of Murthy below, Murthy teaches a substrate 505 (red) suitable for forming PMOS transistors (blue) on N-type wells 1224 (green) and NMOS transistors (orange) on P-type wells 524 (purple).



EX1011-Murthy, Fig. 12 (annotated)

XI. GROUNDS FOR FINDING THE CHALLENGED CLAIMS INVALID

68. It is my opinion that the Challenged Claims are unpatentable on the following grounds.

- **Ground 1A:** Claims 1-7, 9 and 11-13 are invalid as obvious over Koontz.
- **Ground 1B:** Claims 8, 10, and 14 are invalid as obvious over Koontz and Sridhar.
- **Ground 2:** Claims 1-4 are invalid as anticipated by Orłowski.
- **Ground 3A:** Claims 1-7, 9, and 11-13 are invalid as obvious over Samoilov and Murthy.
- **Ground 3B:** Claims 8, 10, and 14 are invalid as obvious over Samoilov, Murthy, and Sridhar.

The below discussion demonstrates in detail that claims 1-14 of the '822 patent are unpatentable. A copy of the Challenged Claims is attached as **Appendix C**.

A. GROUNDS 1A: Claims 1-7, 9 and 11-13 Are Invalid as Obvious Over Koontz

69. As detailed below, Koontz renders obvious claims 1-7, 9 and 11-13 of the '822 patent.

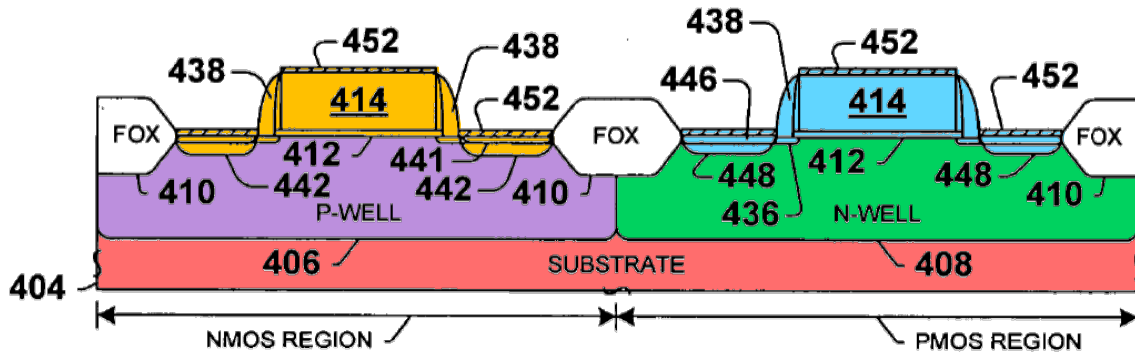
1. Claim 1

a. Element [1Pre]: “A semiconductor structure”

70. I have been informed and understand that, in general, there are circumstances where the preamble of a claim does not limit the scope of the claim, and there are circumstances where the preamble does limit the scope of the claim. In any event, even if the preamble of claim 1 is limiting, Koontz discloses the claimed semiconductor structure.

71. Koontz discloses “a semiconductor structure.” Specifically, Koontz discloses a semiconductor structure, such as a CMOS integrated circuit, having transistors with “improved mobility due to channel strain.” EX1004-Koontz, ¶[0001].

72. Figure 4N of Koontz is reproduced below.



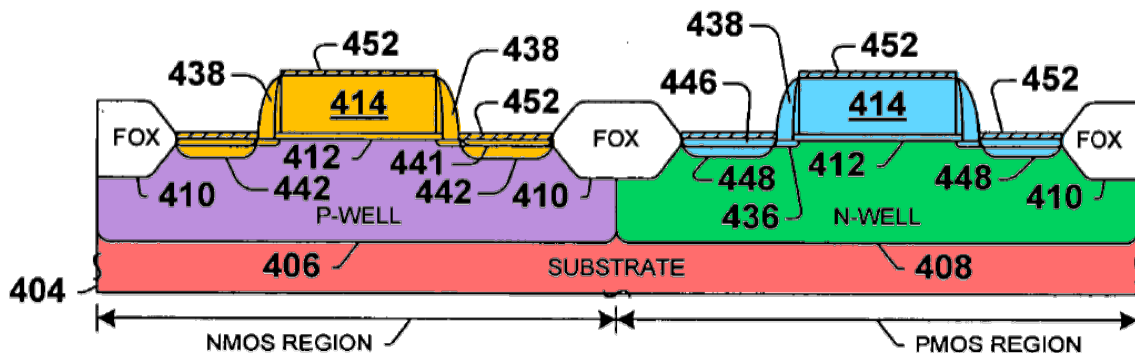
EX1004-Koontz, Fig. 4N (annotated)

As shown above, the semiconductor structure includes a substrate 404 (red), an NMOS transistor (orange) in a P-well 406 (purple) and a PMOS transistor (blue) in an N-well 408 (green). EX1004-Koontz, Fig. 4N, ¶[0041] (“The method 300 begins at 302, wherein transistor fabrication is initiated, and transistor well formation and isolation processing is performed at 304 thereby defining NMOS and PMOS regions, wherein NMOS regions comprise a P-well in which n-type source/drain regions will later be formed, and PMOS regions comprise an N-well in which p-type source/drain regions will later be formed, respectively.”); *see also id.*, ¶[0015]-[0016], ¶[0040]-[0066], Figs. 3, 4A-4N. A POSITA would recognize this as a typical CMOS configuration involving complementary wells formed in a common substrate.

b. Element [1A]: “a substrate, having therein a first well of a first conductivity type and a second well of a second conductivity type”

73. Koontz discloses “a substrate, having therein a first well of a first conductivity type and a second well of a second conductivity type.”

74. Figure 4N of Koontz is reproduced below.



EX1004-Koontz, Fig. 4N (annotated)

Figure 4N depicts a substrate 404 (red) that “has a number of wells formed therein, such as a P-well 406 [(purple)] to define an NMOS transistor device region and an N-well 408 [(green)] to define a PMOS transistor device region, respectively.”

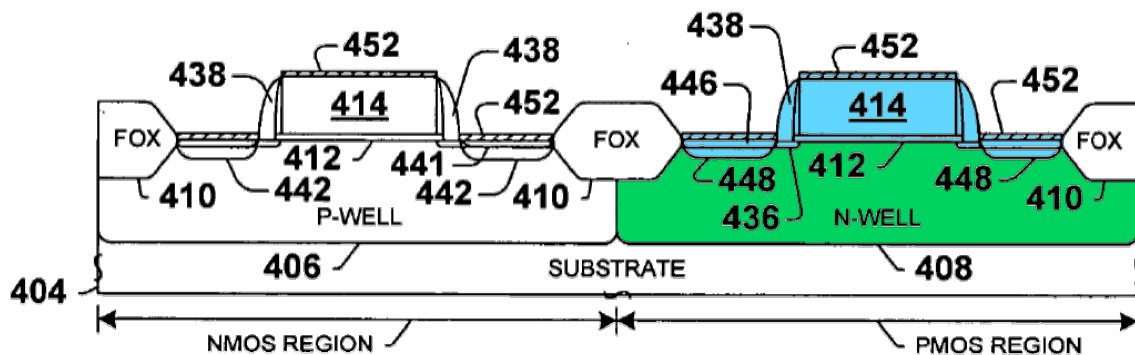
EX1004-Koontz, ¶[0053]; *see also id.*, ¶[0041], Figs. 3, 4A-4N. N-well 408 is n-doped (i.e., n-type) and P-well 406 is p-doped (i.e., p-type). Thus, the P-well 406 is of a first conductivity type (i.e., p-type) and N-well 408 is of a second conductivity type (i.e., n-type). Accordingly, P-well 406 of Koontz corresponds to the first well of claim 1 and N-well 408 corresponds to the second well of claim 1. Additionally,

and alternatively, these teachings equally satisfy the challenged claims when the conductivity types are reversed, i.e., when the “first conductivity type” is n-type and the “second conductivity type” is p-type, since the claim language permits such symmetry.

c. Element [1B]: “a first MOS transistor of the first conductivity type on the second well, comprising:”

75. Koontz discloses “a first MOS transistor of the first conductivity type on the second well.”

76. Figure 4N of Koontz is reproduced below.



EX1004-Koontz, Fig. 4N (annotated)

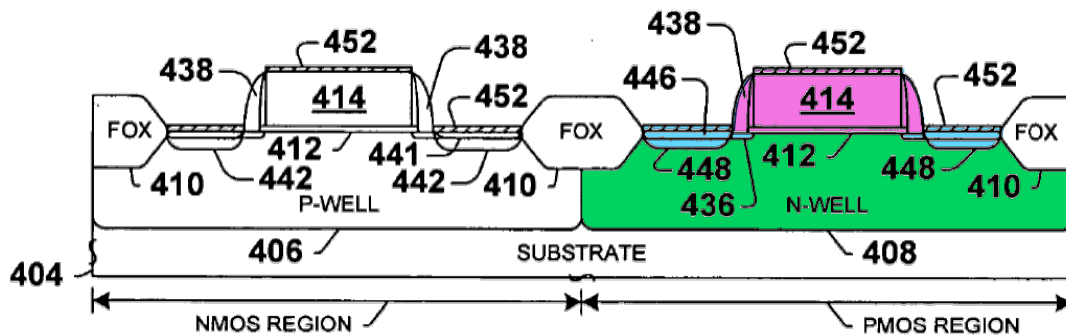
As I explained above in Section XI.A.1.b for Element [1A], Koontz discloses a P-well 406 (purple) (i.e., a “first well” of a “first conductivity type”) on which NMOS transistors (orange) (i.e., a “second MOS transistor” of a “second conductivity type”) are formed and an N-well 408 (green) (i.e., a “second well” of the “second conductivity type”) on which PMOS transistors (blue) (i.e., a “first MOS transistor”

of the “first conductivity type”) are formed. EX1004-Koontz, Fig. 4N, ¶[0053]. Accordingly, the PMOS transistors of Koontz correspond to the first MOS transistor of the first conductivity type of claim 1. Additionally, and alternatively, these teachings equally satisfy the challenged claims when the conductivity types are reversed, i.e., when the “first conductivity type” is n-type and the “second conductivity type” is p-type, since the claim language permits such symmetry.

d. Element [1C]: “a first MOS transistor... comprising: a first gate structure on the second well”

77. Koontz discloses “a first gate structure on the second well.”

78. Figure 4N of Koontz is reproduced below.



EX1004-Koontz, Fig. 4N (annotated)

79. As explained above in Section XI.A.1.c for Element [1B], Koontz discloses an N-well 408 (green) (i.e., a “second well”) on which PMOS transistors (blue) (i.e., a “first MOS transistor”) are formed. Figure 4N additionally depicts a gate structure (including gate electrode 414, gate oxide 412, and sidewall spacers

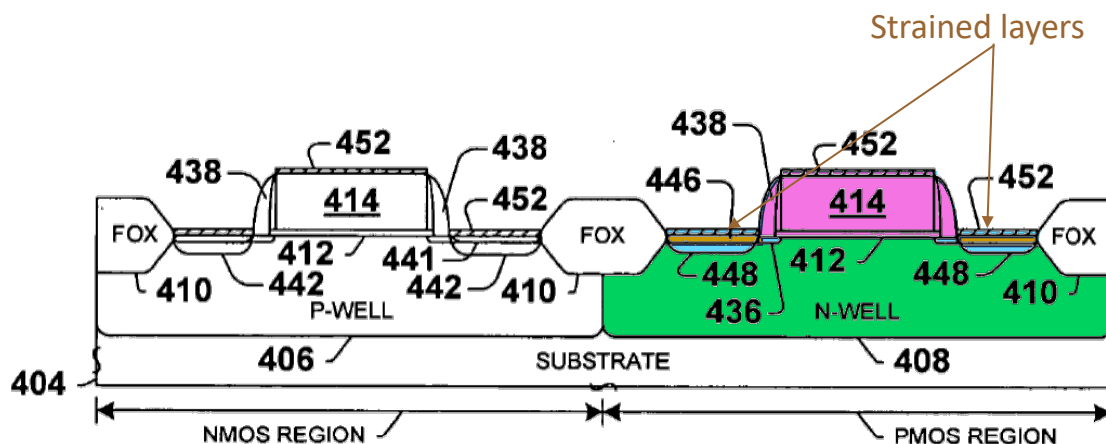
438) (magenta) of the PMOS transistor (blue) on N-well 408 (green). EX1004-Koontz, Fig. 4F, ¶¶[0053]-[0066]. Accordingly, the gate structure (including gate electrode 414, gate oxide 412, and sidewall spacers 438) of Koontz correspond to the first gate structure of claim 1. Additionally, and alternatively, these teachings equally satisfy the challenged claims when the conductivity types are reversed, i.e., when the “first conductivity type” is n-type and the “second conductivity type” is p-type, since the claim language permits such symmetry.

- e. **Element [1D]: “a first MOS transistor ... comprising: ... a first strained layer of the first conductivity type in a first opening in the second well beside the first gate structure, wherein a difference between a lattice parameter of a portion of the first strained layer near a bottom of the first opening and a lattice parameter of the substrate is smaller than a difference between a lattice parameter of a portion of the first strained layer apart from the bottom of the first opening and the lattice parameter of the substrate”**

80. Koontz discloses “a first strained layer of the first conductivity type in a first opening in the second well beside the first gate structure, wherein a difference between a lattice parameter of a portion of the first strained layer near a bottom of the first opening and a lattice parameter of the substrate is smaller than a difference between a lattice parameter of a portion of the first strained layer apart from the bottom of the first opening and the lattice parameter of the substrate.”

81. I will first address the portion of Element [1D] reciting “a first strained layer of the first conductivity type in a first opening in the second well beside the first gate structure.”

82. As explained above in Section XI.A.1.d for Element [1C], Koontz discloses a gate structure (including gate electrode 414, gate oxide 412, and sidewall spacers 438) (magenta) of the PMOS transistor (blue) on N-well 408 (green). Figure 4N of Koontz additionally discloses that PMOS transistor (blue) includes a filled recess structures 446 (brown) (which are comprised of a “strain producing material”) on a N-well 408 (green) beside the gate structure (magenta). EX1004-Koontz, Fig. 4F (annotated); *see also id.*, ¶¶[0005]-[0006], ¶[0025], ¶[0027], ¶[0050], ¶[0063].

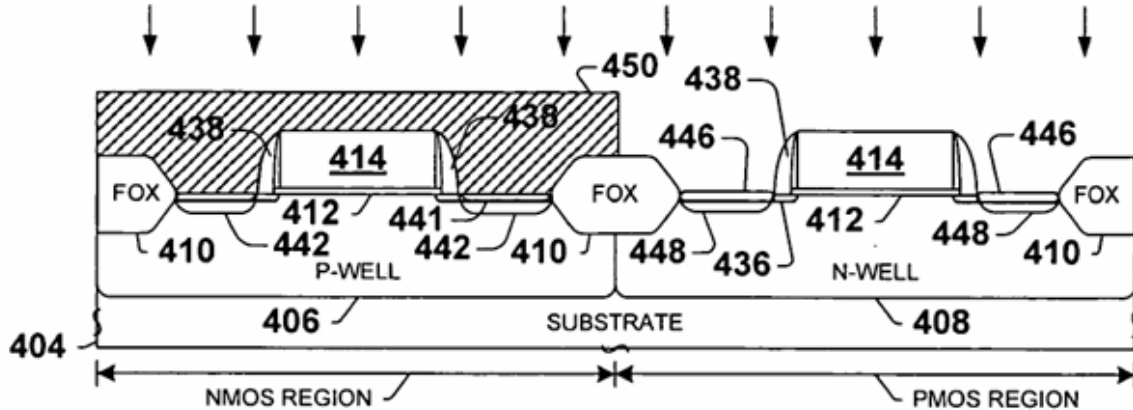


EX1004-Koontz, Fig. 4F (annotated)

83. I note that Koontz’s recess structures 446 have the same role as the “strained layer” in the ’822 patent. As explained in the ’822 patent, a strained layer

“serv[es] as part of the S/D region of the MOS transistor” and creates a compressive or tensile stress to improve the performance of the MOS transistor. EX1001-USP’822, 3:19-29, 4:65-5:19. Koontz, like the ’822 patent, teaches that the recess structures 446 are “comprised of a compressive strain producing material....” EX1004-Koontz, ¶[0063]. Specifically, Koontz teaches that “[t]he composition of the filled recess structures 446 is controlled and can vary in composition vertically from bottom to top of the structures 446. As a result, the resulting compressive strain can be increased or decreased by correspondingly increasing or decreasing one or more components of the tensile strain producing material. Thus, a vertical strain profile ... can be obtained.” EX1004-Koontz, ¶[0063]; *see also id.*, ¶¶[0006], [0026].

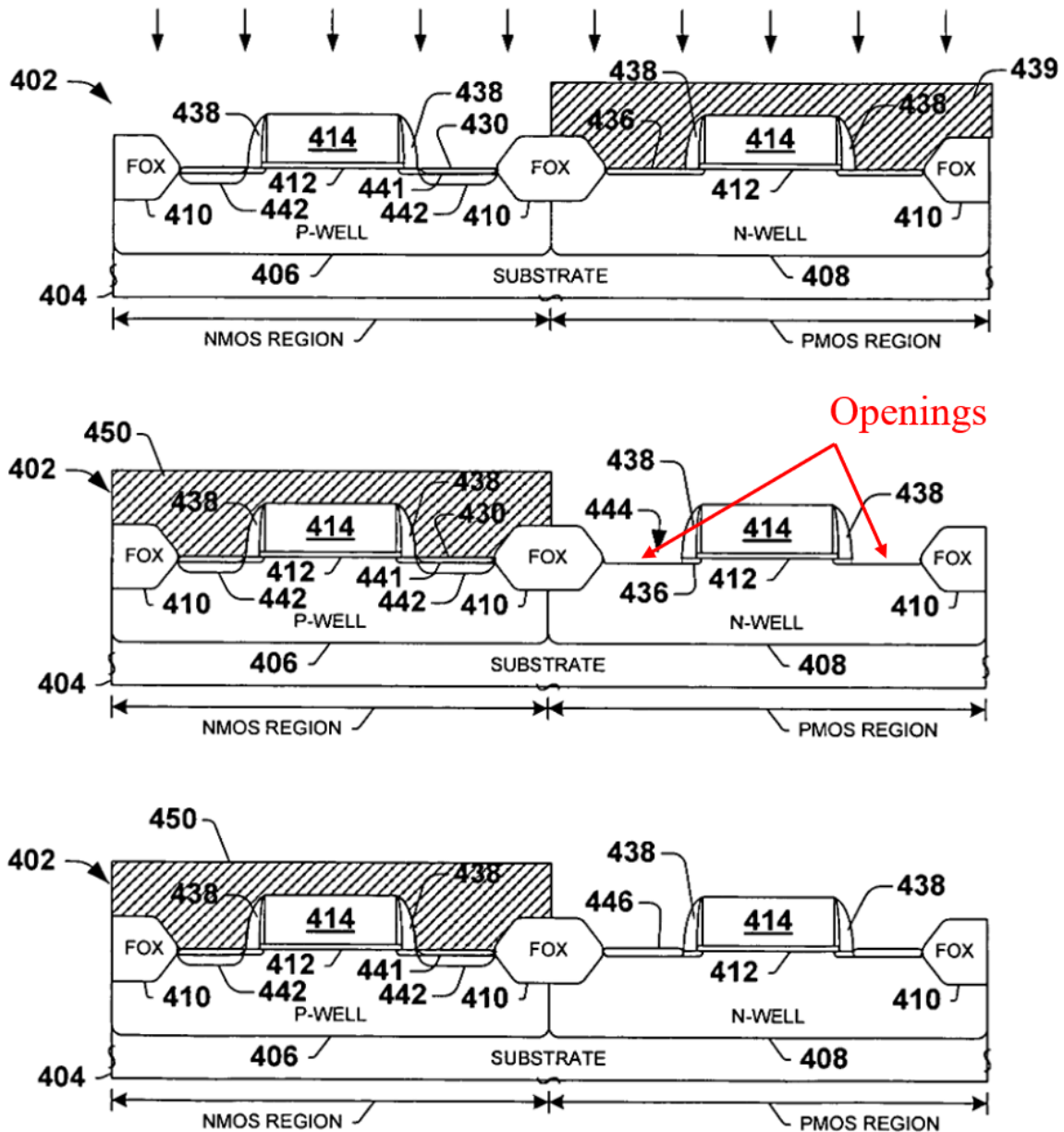
84. Moreover, Koontz teaches that the recess structures 446 are of a first conductivity type (i.e., p-type). Specifically, as shown in Figure 4M of Koontz, Koontz discloses that recess structures 446 are “formed in the PMOS region” by implanting boron, which a POSITA would understand is a p-type dopant. EX1004-Koontz, ¶[0051], Fig. 4M.



EX1004-Koontz, Fig. 4M

85. Furthermore, Koontz teaches that the recess structures 446 are formed “in a first opening in the second well beside the first gate structure.” Figures 4K through 4M of Koontz depicts the process for forming the recess structures 446. As shown in Figures 4M through 4L of Koontz, the recess structures 446 are formed by “remov[ing] a selected amount of material from a surface portion of the active regions and subsequently re-depositing and forming recess structures in the active regions comprised of a compressive strain producing material, such as silicon-germanium.” EX1004-Koontz, Figs. 4J-4L, ¶[0025]. Specifically, recess structures 446 are formed in recessed regions 444 (i.e., a first opening in the second well) that are created by removing extension region 436, which in turn is formed by “a recess etch” “that removes a selected amount of material from a surface portion of the active regions ... within the PMOS region.” As shown in Figure 4K of Koontz, the recessed regions 444 are in the N-well 408 (i.e., the second well) and besides the

first gate structure (i.e., gate electrode 414, gate oxide 412, and sidewall spacers 438).



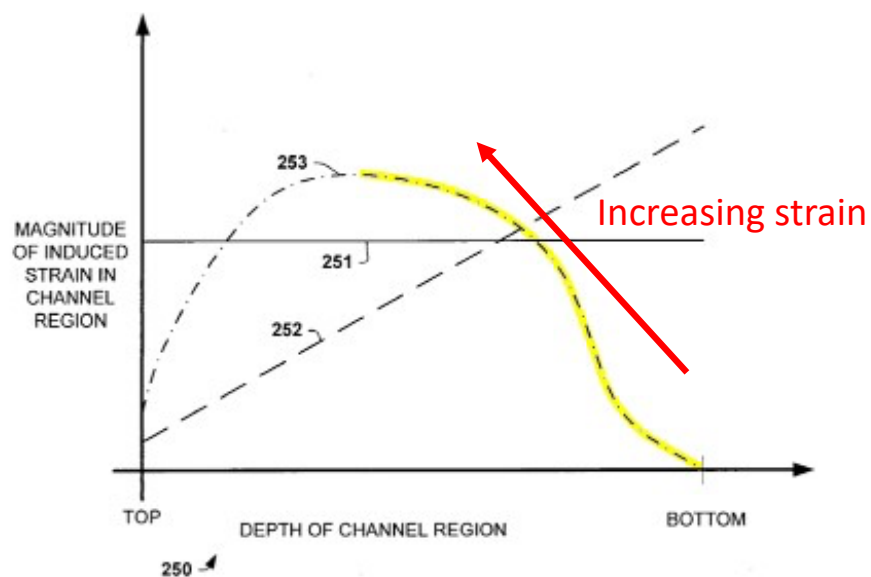
EX1004-Koontz, Fig. 4J-4M (annotated)

86. Next, I will address the portion of Element [1D] reciting that “a difference between a lattice parameter of a portion of the first strained layer near a bottom of the first opening and a lattice parameter of the substrate is smaller than a difference between a lattice parameter of a portion of the first strained layer apart from the bottom of the first opening and the lattice parameter of the substrate.”

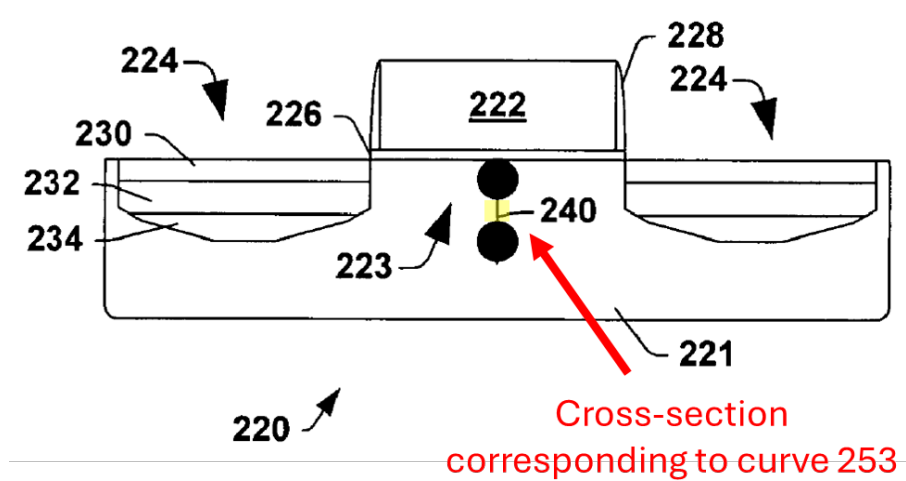
87. This portion of Element [1D] recites that the lattice parameter of the first strained layer is not uniform across the vertical direction. As I explained above, the lattice parameter of a crystalline structure measures the spacing between neighboring atoms in the material. *See supra* Section VII.D. As such, this portion of Element [1D] requires the spacing between neighboring atoms to vary in the vertical direction across the first strained layer.

88. Koontz discloses that “[t]he composition of the filled recess structures 446 is controlled and can vary in composition vertically from bottom to top of the structures 446.” EX1004-Koontz, [0063]. A POSITA would have understood that changing the composition of the recess structures 446 would directly influence their lattice parameter, resulting in a corresponding variation in the lattice parameter of the recess structures 446. *See* EX1017-Murthy482, 1:45-48 (difference between lattice constant of SiGe and that of Si varies depending on the Ge percentage); EX1027-Dismukes, Fig. 3 (plotting this relationship).

89. In particular, Koontz discloses that the composition of the recess structures 446 can be controlled to produce a “linearly changing channel strain profile” by, for example, “linearly adjusting concentration of one or more components of material comprising recess structures at various depths during formation thereof.” EX1004-Koontz, ¶[0038]. Similarly, the composition of the recess structures 446 can be controlled to produce a “non-linearly changing channel strain profile” by, for example, “non-linearly adjusting concentration of one or more components of material comprising recess structures during formation thereof.” EX1004-Koontz, ¶[0038]. Figure 2 of Koontz plots the “linearly changing channel strain profile” (line 252) and the “non-linearly changing channel strain profile” (curve line 253) across cross-section 240 (as shown in Figure 2B of Koontz).



EX1004-Koontz, Fig. 2C (annotated)



EX1004-Koontz, Fig. 2B (annotated)

90. Even though Koontz does not provide a description of the lattice parameter that would result in the “linearly changing channel strain profile” and the “non-linearly changing channel strain profile,” a POSITA would have understood that the increasing strain in the channel region in the vertical direction arises from a corresponding increase in the lattice parameter mismatch between the strain-inducing regions adjacent to the gate and the underlying substrate. In fact, Koontz itself teaches that “the resulting compressive strain [produced by recess structures 446] can be increased or decreased by correspondingly increasing or decreasing one or more components of the tensile strain producing material.” EX1004-Koontz, ¶[0063]; *see also id.*, ¶[0033], [0034]-[0036], [0059]. In other words, Koontz teaches that *increasing* the concentration of germanium atoms in a silicon-germanium recess structure would result in a corresponding *increase* in the

compressive strain produced by recess structures 446. Similarly, Koontz teaches that *decreasing* the concentration of germanium atoms in a silicon-germanium recess structure would result in a corresponding *decrease* in the compressive strain produced by recess structures 446.

91. Accordingly, Koontz teaches that, as illustrated in FIG. 2C (curve line 253), the strain in the channel region increases progressively from the bottom toward the top of the recess, consistent with a vertical compositional variation in the adjacent SiGe stressor layer. As Koontz explains (§ [0063]), the composition of the filled recess structures 446 can vary vertically from bottom to top, and the resulting compressive strain can be increased or decreased by correspondingly adjusting the composition of the strain-producing material. A POSITA would have understood that this vertical compositional variation, e.g., increasing the Ge concentration toward the top of the recess to enhance compressive strain, corresponds to a graded lattice parameter: the lattice parameter near the bottom of the recess (adjacent to the silicon substrate) is closer to that of the substrate, while the lattice parameter farther from the bottom (closer to the channel) is larger due to the higher Ge content. Accordingly, the difference between the lattice parameter near the bottom of the first opening and that of the substrate is smaller than the difference between the lattice parameter farther from the bottom and that of the substrate, as recited in claim 1.

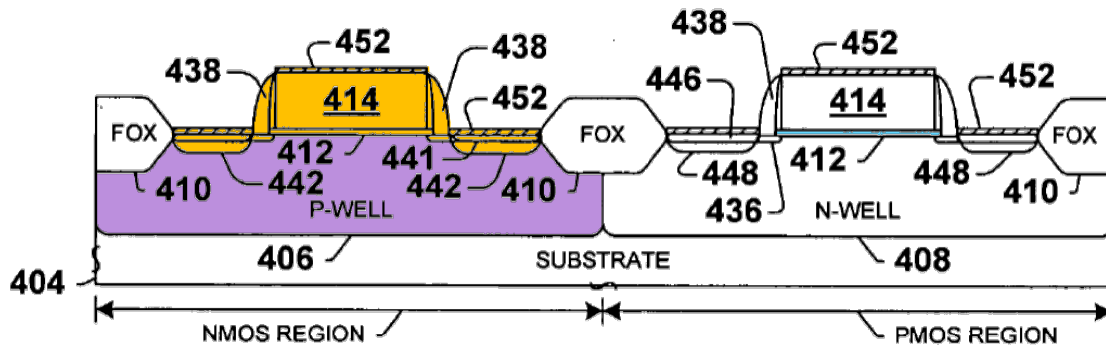
92. Moreover, in light of Koontz’s teachings, it would have been obvious to a POSITA to vary the lattice parameter of the recess structures 446 of Koontz (corresponding to the “first strained layer” of claim 1) along the vertical direction to achieve the strain distribution depicted in Figure 2C. A POSITA would have recognized that varying the lattice parameter of the recess structures 446 across the vertical direction offers multiple advantages (*see supra* Section VII.E). For instance, this design mitigates the formation of a sharp interface between the silicon-germanium strained layer and the silicon substrate, reducing the risk of dislocation defects. *See* EX1020-Zhu, 1:56–64, 3:18–25. Accordingly, a POSITA would have been motivated to vary the lattice parameter of the recess structures 446 in Koontz’s across the vertical direction and would have had a reasonable expectation of success in doing so.

93. Additionally, and alternatively, these teachings equally satisfy the challenged claims when the conductivity types are reversed, i.e., when the “first conductivity type” is n-type and the “second conductivity type” is p-type, since the claim language permits such symmetry. In that situation, the recess structures are formed using silicon-carbon instead of silicon-germanium to induce a tensile strain rather than a compressive strain. EX1004-Koontz, ¶¶[0008], [0025], [0027], [0047], [0059], Figs. 3, 4N.

f. Element [1E]: “a second MOS transistor of the second conductivity type on the first well”

94. Koontz discloses “a second MOS transistor of the second conductivity type (e.g., n-type) on the first well.”

95. Figure 4N of Koontz is reproduced below.



EX1004-Koontz, Fig. 4N (annotated)

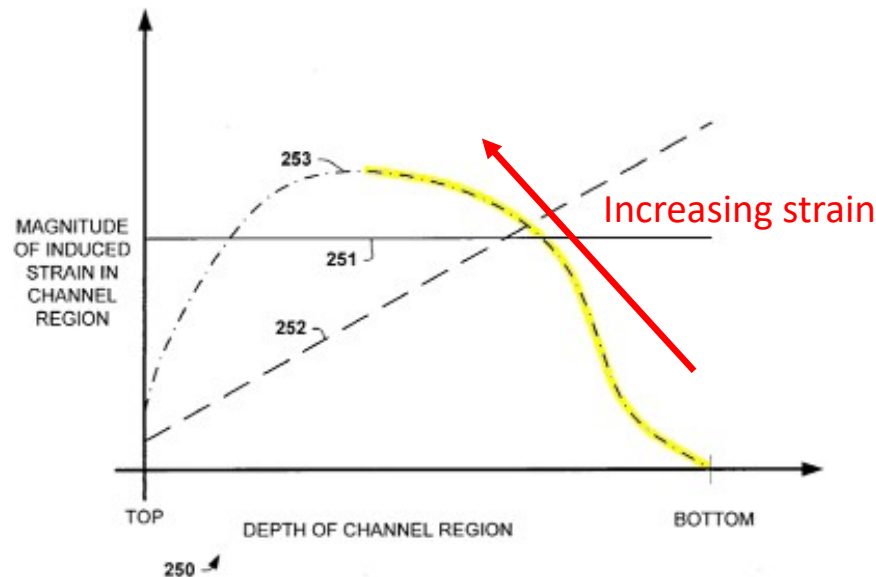
As I explained above in Section XI.A.1.b for Element [1A], Koontz discloses a P-well 406 (purple) (i.e., a “first well” of a “first conductivity type”) on which NMOS transistors (orange) (i.e., a “second MOS transistor” of a “second conductivity type”) are formed and an N-well 408 (i.e., a “second well” of the “second conductivity type”) on which PMOS transistors (i.e., a “first MOS transistor” of the “first conductivity type”) are formed. EX1004-Koontz, Fig. 4N, ¶[0053]. Accordingly, the NMOS transistors of Koontz correspond to the second MOS transistor of the second conductivity type of claim 1. Additionally, and alternatively, these teachings equally satisfy the challenged claims when the conductivity types are reversed, i.e.,

when the “first conductivity type” is n-type and the “second conductivity type” is p-type, since the claim language permits such symmetry.

2. **Claim 2: “The semiconductor structure of claim 1, wherein the lattice parameter of the first strained layer has a gradient distribution”**

96. Claim 2 depends from claim 1, which, as I explained above, is obvious over Koontz. *Supra* §XI.A.1. Moreover, as I explain above in section XI.A.1.e, as shown in Figure 2C of Koontz, the lattice parameter of the first strained layer (e.g., recess structures 446) has a gradient distribution from bottom to top. EX1004-Koontz, Fig. 2C; *see also id.*, ¶¶[0022] (“[T]he amount or magnitude of strain can be constant or vary linearly or non-linearly across the profile.”), [0034] (“The strain composition of the filled structures 224 can vary according to individual layers, vary linearly, or vary non-linearly. The resulting strain profile 240 can thus be controlled to be constant or non-constant, throughout a depth of the channel and, if non-constant, vary linearly or non-linearly.”), [0038] (“Line 252 depicts a linearly changing channel strain profile, which can generally be obtained by linearly adjusting concentration of one or more components of material comprising recess structures at various depths during formation thereof.... Line 253 illustrates a non-linearly changing channel strain profile, which can be obtained by non-linearly

adjusting concentration of one or more components of material comprising recess structures during formation thereof.”).

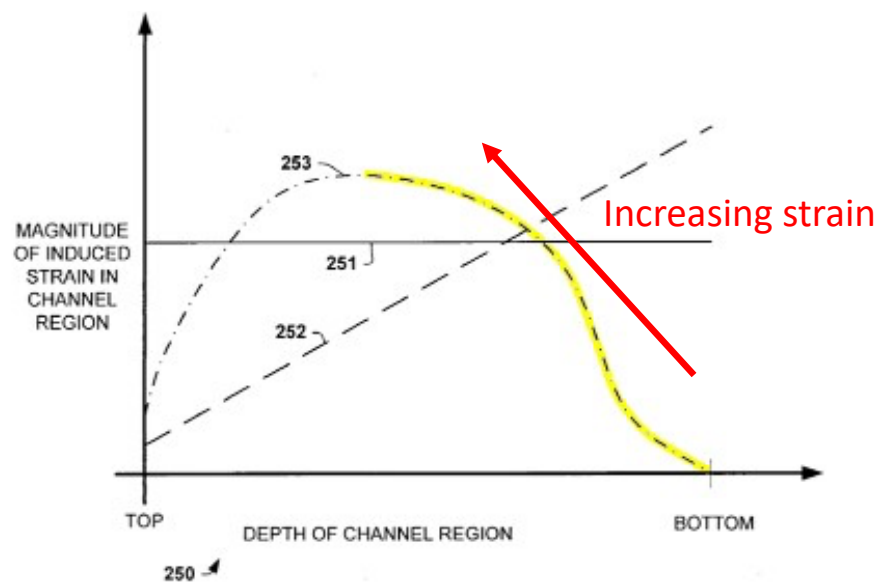


EX1004-Koontz, Fig. 4N (annotated)

3. **Claim 3: “The semiconductor structure of claim 1, wherein the first conductivity type is P-type, and the lattice parameter of a portion of the first strained layer near the bottom of the first opening is smaller than the lattice parameter of a portion of the first strained layer apart from the bottom of the first opening”**

97. Claim 3 depends from claim 1, which, as I explained above, is obvious over Koontz. *Supra* §XI.A.1. Moreover, as I explain above in section XI.A.1.e, for p-type MOS transistors (i.e., when the first conductivity type is p-type), the recess structures 446 are formed using silicon-germanium. EX1004-Koontz, ¶[0063]. Moreover, as I explained above in section XI.A.1.e, a POSITA would have understood that, to obtain profile depicted in the curve line 253, the concentration of

germanium at the bottom of the recess structures 446 is lower than the concentration of germanium of a portion apart from the bottom of the recess structures 446. Thus, a POSITA would have understood that, to achieve the strain profile of the curve line 253, the lattice parameter of the silicon-germanium recess structures 446 becomes smaller near the bottom of the recess structures 446. *See* Section VII.D; EX1017-Murthy482, 1:46 48 (difference between lattice constant of SiGe and that of Si varies depending on the Ge percentage); EX1027-Dismukes, Fig. 3 (plotting this relationship).



EX1004-Koontz, Fig. 4N (annotated)

4. **Claim 4: “The semiconductor structure of claim 3, wherein the first strained layer comprises SiGe”**

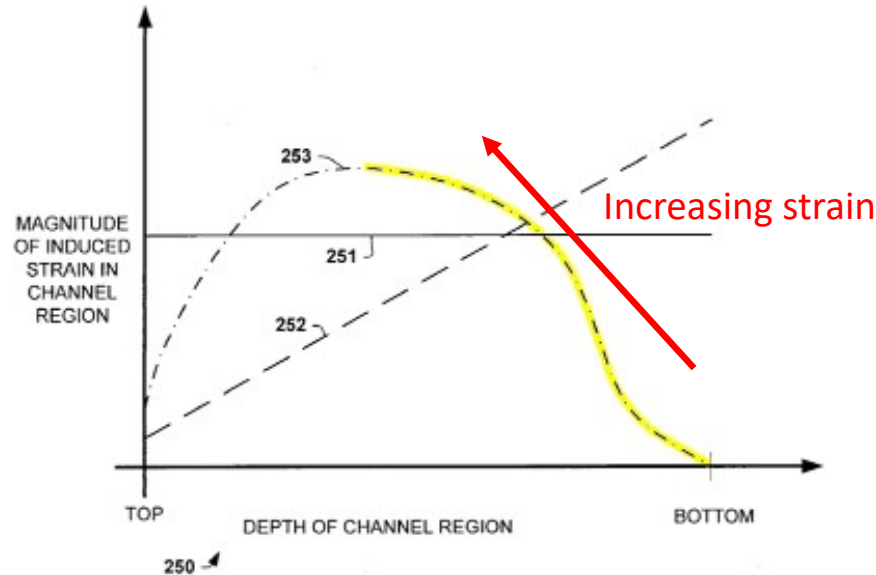
98. Koontz satisfies claim 4 for the reasons in Section XI.A.4 (Claim 3) and XI.A.1.e (Element [1D]). For example, Koontz discloses that in the case of PMOS

transistors, the recess structures (which, as I explained above, correspond to the first strained layer”) are “comprised of a compressive strain producing material, such as silicon-germanium....” EX1004-Koontz, ¶[0063].

5. **Claim 5: “The semiconductor structure of claim 1, wherein the first conductivity type is N-type, and the lattice parameter of a portion of the first strained layer near the bottom of the first opening is larger than the lattice parameter of a portion of the first strained layer apart from the bottom of the first opening”**

99. Claim 5 depends from claim 1, which, as I explained above, is obvious over Koontz. *Supra* §XI.A.1.

100. Moreover, as I explain above in section XI.A.1.e, for n-type MOS transistors (i.e., when the first conductivity type is n-type), the recess structures 441 are formed using silicon-carbon. EX1004-Koontz, ¶[0059]. Moreover, as I explained above in section XI.A.1.e, a POSITA would have understood that, to obtain profile depicted in the curve line 253, the concentration of carbon at the bottom of the recess structures 441 is lower than the concentration of carbon of a portion apart from the bottom of the recess structures 446. Thus, a POSITA would have understood that, to achieve the strain profile of the curve line 253, the lattice parameter of the silicon-carbon recess structures 441 becomes larger near the bottom of the recess structures 441. *See* Section VII.D; EX1017-Murthy482, 1:46 48; EX1027-Dismukes, Fig. 3, Tbl. IV.



EX1004-Koontz, Fig. 4N (annotated)

6. **Claim 6: “The semiconductor structure of claim 5, wherein the first strained layer comprises SiC”**

101. Koontz satisfies claim 6 for the reasons in Section XI.A.1.e (Element [1D]). For example, Koontz discloses that in the case of NMOS transistors, the recess structures (which, as I explained above, correspond to the “first strained layer”) are “comprised of a tensile strain producing material, such as silicon-carbon....” EX1004-Koontz, ¶[0059].

7. **Claim 7**

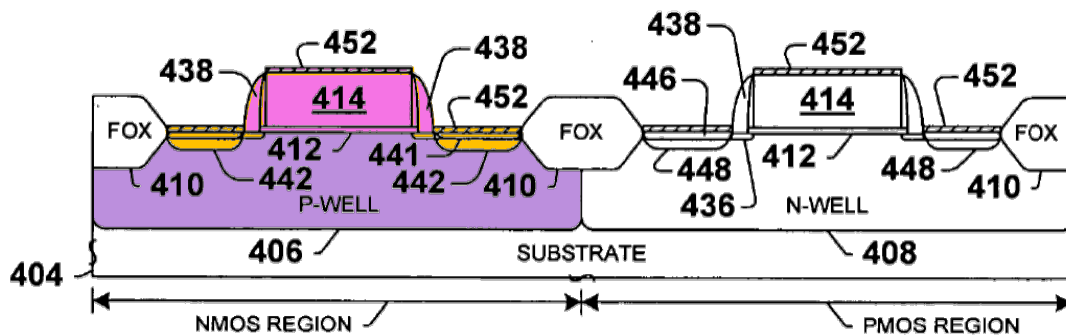
a. **Element [7Pre]: “The semiconductor structure of claim 1”**

102. Claim 7 depends from claim 1, which, as I explained above, Koontz satisfies. *Supra* §XI.A.1.

**b. Element [7A]: “the second MOS transistor comprises:
a second gate structure on the first well”**

103. Koontz discloses “the second MOS transistor comprises: a second gate structure on the first well.”

104. Figure 4N of Koontz is reproduced below.



EX1004-Koontz, Fig. 4N (annotated)

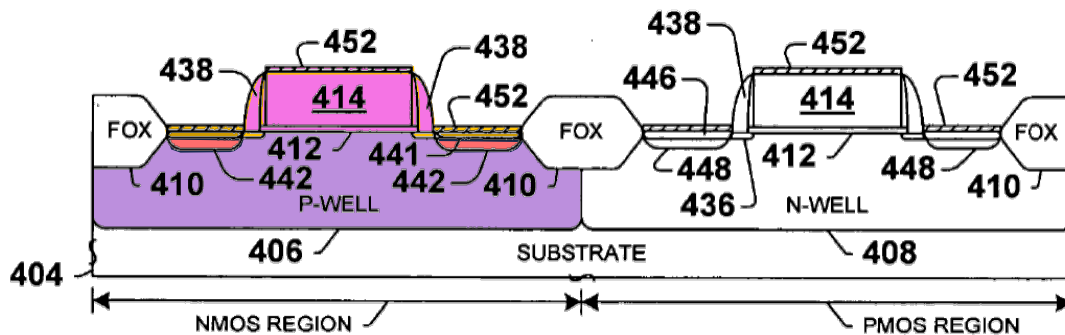
As explained above in Section XI.A.1.e for Element [1E], Koontz discloses a P-well 406 (purple) (i.e., a “first well” of a “first conductivity type”) on which NMOS transistors (orange) (i.e., a “second MOS transistor” of a “second conductivity type”) are formed. EX1004-Koontz, Fig. 4N, ¶[0053]. Figure 4N additionally depicts a gate structure (including gate electrode 414, gate oxide 412, and sidewall spacers 438) (magenta) of the NMOS transistor (orange) on P-well 406 (purple). EX1004-Koontz, Fig. 4N, ¶[0053]-[0066]. Accordingly, the gate structure (including gate electrode 414, gate oxide 412, and sidewall spacers 438) of Koontz correspond to the second gate structure of claim 7. Additionally, and alternatively, these teachings

equally satisfy the challenged claims when the conductivity types are reversed, i.e., when the “first conductivity type” is n-type and the “second conductivity type” is p-type, since the claim language permits such symmetry.

c. Element [7B]: “the second MOS transistor comprises: ... a source/drain region of the second conductivity type in the first well beside the second gate structure”

105. Koontz discloses “the second MOS transistor comprises: ... a source/drain region of the second conductivity type in the first well beside the second gate structure.”

106. Figure 4N of Koontz is reproduced below.



EX1004-Koontz, Fig. 4N (annotated)

As explained above in Section XI.A.7.b for Element [7A], Koontz discloses a gate structure (including gate electrode 414, gate oxide 412, and sidewall spacers 438) (magenta) of the NMOS transistor (orange) on P-well 406 (purple). Figure 4N of Koontz additionally discloses that NMOS transistor (orange) additionally comprises

source and drain regions 442. EX1004-Koontz, Fig. 4N, ¶[0061]. The source and drain regions 442 “are formed in the NMOS region by implanting a suitable n-type dopant...” Accordingly, a POSITA would understand that source and drain regions 442 of Koontz are n-type, which I explained above corresponds to the second conductivity type. Moreover, as shown in Figure 4N of Koontz, source and drain regions 442 are besides the second gate structure (including gate electrode 414, gate oxide 412, and sidewall spacers 438) (magenta). Additionally, and alternatively, these teachings equally satisfy the challenged claims when the conductivity types are reversed, i.e., when the “first conductivity type” is n-type and the “second conductivity type” is p-type, since the claim language permits such symmetry.

8. Claim 9

a. Element [9Pre]: “The semiconductor structure of claim 1”

107. Claim 9 depends from claim 1, which, as I explained above, Koontz satisfies. *Supra* §XI.A.1.

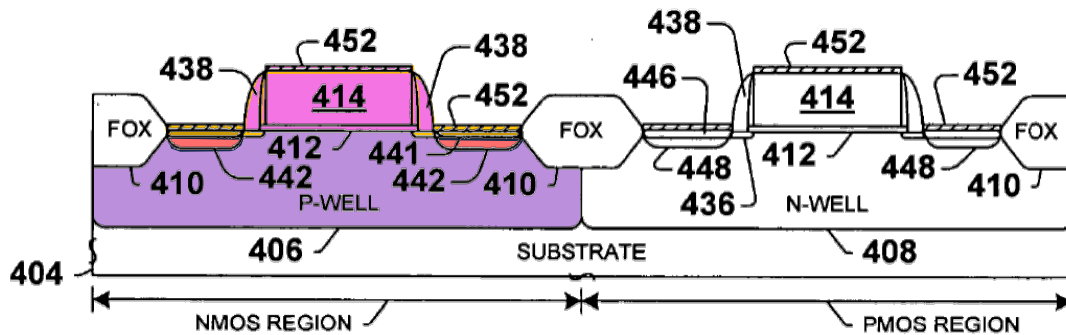
b. Element [9A]: “the second MOS transistor comprises: a second gate structure on the first well”

108. Element [9A] recites the same subject matter as Element [7A], which I addressed above. Namely, Element [9A] recites that “the second MOS transistor comprises: a second gate structure on the first well,” which is identical to Element

[7A]. As such, my analysis above regarding Element [7A] (Section XI.A.7.b) equally applies here. Therefore, Koontz discloses this limitation.

c. Element [9B]: “the second MOS transistor comprises: ... a source/drain region of the second conductivity type around and under a second opening in the first well beside the second gate structure”

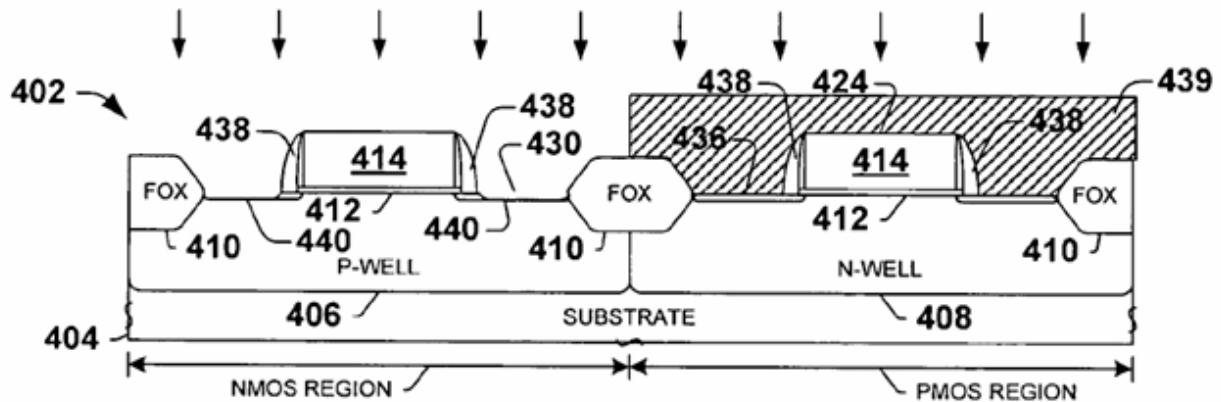
109. As I explained above in Section XI.A.7.c for Element [7B], Koontz discloses source and drain regions (red) of the second conductivity type (e.g., n-type) besides the second gate structure (magenta). Figure 4N of Koontz is reproduced below.



EX1004-Koontz, Fig. 4N (annotated)

110. In addition, as shown in Figure 4N of Koontz, the source and drain regions 442 are around and under the recess structures 441, which as I explained above are formed in recesses regions 440. As shown in Figure 4H, the recess regions 440 are a second opening in the P-well 406 (i.e., the first well) beside the second gate structure (including gate electrode 414, gate oxide 412, and sidewall spacers

438). Accordingly, a POSITA would understand that the source and drain regions 442 are around and under a second opening in the first well beside the second gate structure.



EX1004-Koontz, Fig. 4H

9. **Claim 11**

- a. **Element [11Pre]: “The semiconductor structure of claim 1”**

111. Claim 11 depends from claim 1, which, as I explained above, Koontz satisfies. *Supra* §XI.A.1.

- b. **Element [11A]: “the second MOS transistor comprises: a second gate structure on the first well”**

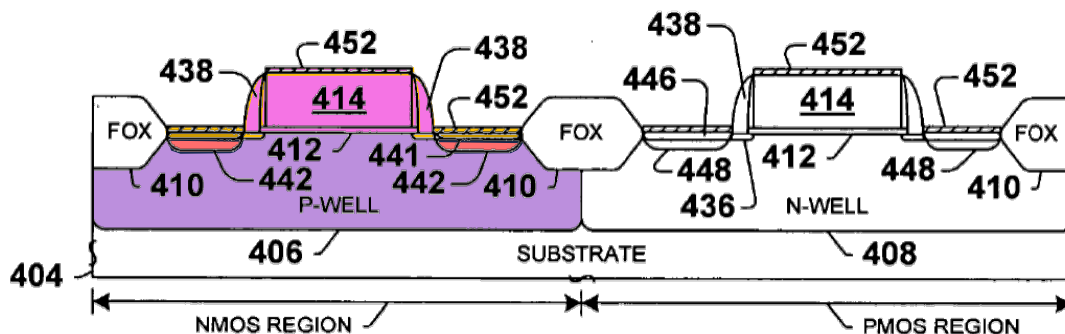
112. Element [11A] recites the same subject matter as Element [7A], which I addressed above. Namely, Element [11A] recites that “the second MOS transistor comprises: a second gate structure on the first well,” which is identical to Element

[7A]. As such, my analysis above regarding Element [7A] (Section XI.A.7.b) equally applies here. Therefore, Koontz discloses this limitation.

c. Element [11B]: “the second MOS transistor comprises: ... a second strained layer of the second conductivity type in a second opening in the first well beside the second gate structure”

113. Koontz discloses “the second MOS transistor comprises: ... a second strained layer of the second conductivity type in a second opening in the first well beside the second gate structure.”

114. Figure 4N of Koontz is reproduced below.



EX1004-Koontz, Fig. 4N (annotated)

115. As shown in Figure 4N, Koontz discloses a gate structure (including gate electrode 414, gate oxide 412, and sidewall spacers 438) (magenta) of the NMOS transistor (orange) on P-well 406 (purple). Koontz further teaches recess structures 441 are “comprised of a tensile strain producing material” and are “formed in the NMOS recessed region” within P-Well 406. Accordingly, a POSITA would

have understood that these recess structures 441—together with the adjacent source and drain regions 442—constitute strained layers of the second conductivity type (n-type), as the NMOS device uses n-type dopants. The recess structures are formed in openings in the first well (P-well 406) and positioned beside the second gate structure (including gate electrode 414, gate oxide 412, and sidewall spacers 438) (magenta), satisfying the spatial relationship required by Element [11B]. Accordingly, Koontz teaches a second MOS transistor that includes a second strained layer of the second conductivity type in a second opening in the first well beside the second gate structure. Additionally, and alternatively, these teachings equally satisfy the challenged claims when the conductivity types are reversed, i.e., when the “first conductivity type” is n-type and the “second conductivity type” is p-type, since the claim language is symmetric to polarity.

10. Claim 12

a. Element [12Pre]: “The semiconductor structure of claim 11”

116. Claim 12 depends from claim 11, which, as I explained above, Koontz satisfies. *Supra* §XI.A.9.

b. Element [12A]: “a difference between a lattice parameter of a portion of the second strained layer near a bottom of the second opening and the lattice parameter of the substrate is smaller than a difference between a lattice parameter of a portion of the second

strained layer apart from the bottom of the second opening and the lattice parameter of the substrate”

117. Limitation [12A] requires that the second strained layer described in Limitation [11B] (*see* Section XI.A.9.b) exhibits the same vertical lattice-parameter gradient specified in Limitation [1D]—that is, the lattice parameter of the strained layer changes along the vertical direction such that the mismatch with the substrate is smaller near the bottom of the recess and larger toward the top. As explained above for Limitation [1D] (*see* Section XI.A.1.e), Koontz discloses that its strained source/drain epitaxial layers are formed with a vertical compositional variation, for example by gradually altering the Ge or C content during deposition, which produces a corresponding increase in lattice mismatch and channel strain moving upward from the interface with the substrate. A POSITA would have understood that this same compositional-grading approach applies to both the compressive SiGe layers used in PMOS transistors and the tensile SiC layers used in NMOS transistors. Accordingly, Koontz teaches the required relationship in which the lattice parameter of the strained layer near the bottom of the recess is closer to that of the substrate, while the lattice parameter farther from the bottom differs more from the substrate, satisfying Limitation [12A].

- c. **Element [12B]: “when the first conductivity type is P-type and the second conductivity type is N-type, the lattice parameter of a portion of the first strained layer**

near the bottom of the first opening is smaller than the lattice parameter of a portion of the first strained layer apart from the bottom of the first opening, but the lattice parameter of a portion of the second strained layer near the bottom of the second opening is larger than the lattice parameter of a portion of the second strained layer apart from the bottom of the second opening”

118. Element [12B] recites the same subject matter as Claims 3 and 5, which I addressed above. Namely, the portion of Element [12B] reciting that “the lattice parameter of a portion of the first strained layer near the bottom of the first opening is smaller than the lattice parameter of a portion of the first strained layer apart from the bottom of the first opening,” as applied to a PMOS transistor, is identical to Claim 3. Similarly, the portion of Element [12B] reciting that “the lattice parameter of a portion of the second strained layer near the bottom of the second opening is smaller than the lattice parameter of a portion of the second strained layer apart from the bottom of the second opening,” as applied to an NMOS transistors, is substantively the same as Claim 5. The only difference is the change between the word “first” and “second,” but as I explained above for Element [1D] (Section XI.A.1.e) and Element [11B] (Section XI.A.9.c), the claims are symmetric to polarity. As such, my analysis above regarding Claim 3 (Section XI.A.3) and Claim 5 (Section XI.A.5) equally applies here. Therefore, Koontz discloses this limitation.

- d. Element [12C]: “when the first conductivity type is N-type and the second conductivity type is P-type, the lattice parameter of a portion of the first strained layer near the bottom of the first opening is larger than the lattice parameter of a portion of the first strained layer apart from the bottom of the first opening, but the lattice parameter of a portion of the second strained layer near the bottom of the second opening is smaller than the lattice parameter of a portion of the second strained layer apart from the bottom of the second opening”**

119. Element [12C] recites the same subject matter as Claims 3 and 5, which I addressed above. Namely, the portion of Element [12C] reciting that “the lattice parameter of a portion of the first strained layer near the bottom of the first opening is larger than the lattice parameter of a portion of the first strained layer apart from the bottom of the first opening,” as applied to an NMOS transistors, is identical to Claim 5. Similarly, the portion of Element [12C] reciting that “the lattice parameter of a portion of the first strained layer near the bottom of the first opening is smaller than the lattice parameter of a portion of the first strained layer apart from the bottom of the first opening,” as applied to a PMOS transistor, is substantively the same as Claim 3. The only difference is the change between the word “first” and “second,” but as I explained above for Element [1D] (Section XI.A.1.e) and Element [11B] (Section XI.A.9.c), the claims are symmetric to polarity. As such, my analysis above

regarding Claim 3 (Section XI.A.3) and Claim 5 (Section XI.A.5) equally applies here. Therefore, Koontz discloses this limitation.

11. **Claim 13: “The semiconductor structure of claim 12, wherein the lattice parameter of the second strained layer has a gradient distribution”**

120. Claim 13 depends from claim 12, which, as I explained above, Koontz satisfies. *Supra* §XI.A.10.

121. Claim 13 further requires that the second strained layer described in Limitation [11B] (*see* Section XI.A.9.b) exhibits a lattice-parameter gradient distribution— i.e., a continuous variation in lattice parameter with depth, such that the mismatch with the substrate is smaller near the bottom of the recess and larger toward the top. As discussed above with respect to Limitation [1D] (*see* Section XI.A.1.e) and Claim 2 (*see* Section XI.A.2), Koontz expressly teaches vertically graded strain-inducing layers whose composition, and thus lattice parameter, changes from the substrate interface upward. In particular, Koontz explains that the composition of the filled recess structures (e.g., SiGe or SiC) can be varied during deposition to control the strain profile across the vertical direction (¶ [0063]). A person of ordinary skill in the art would have understood that this compositional grading directly results in a lattice-parameter gradient within both the compressive SiGe stressors of the PMOS device and the tensile SiC stressors of the NMOS device.

Accordingly, Koontz teaches that the second strained layer possesses a vertical lattice-parameter gradient distribution, satisfying the requirements of Claim 13.

B. GROUNDS 1B: Claims 8, 10 and 14 Are Invalid as Obvious Over Koontz In View Of Sridhar

1. Claim 8

a. Element [8Pre]: “The semiconductor structure of claim 7”

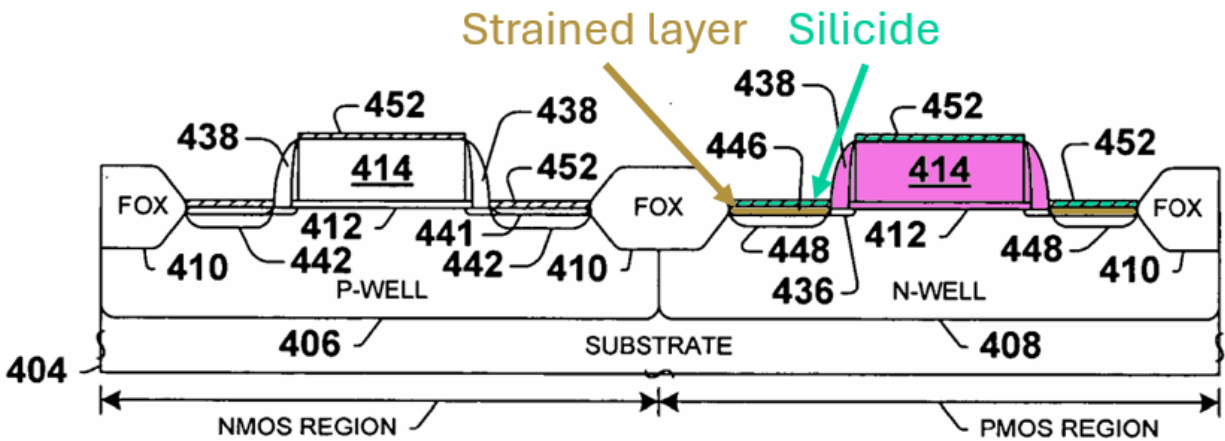
122. Claim 8 depends from claim 7, which, as I explained above, the Koontz satisfies. *Supra* §XI.A.7.

b. Element [8A]: “a silicon layer on the first strained layer”

123. Koontz in view of Sridhar discloses “a silicon layer on the first strained layer.”

i. Koontz

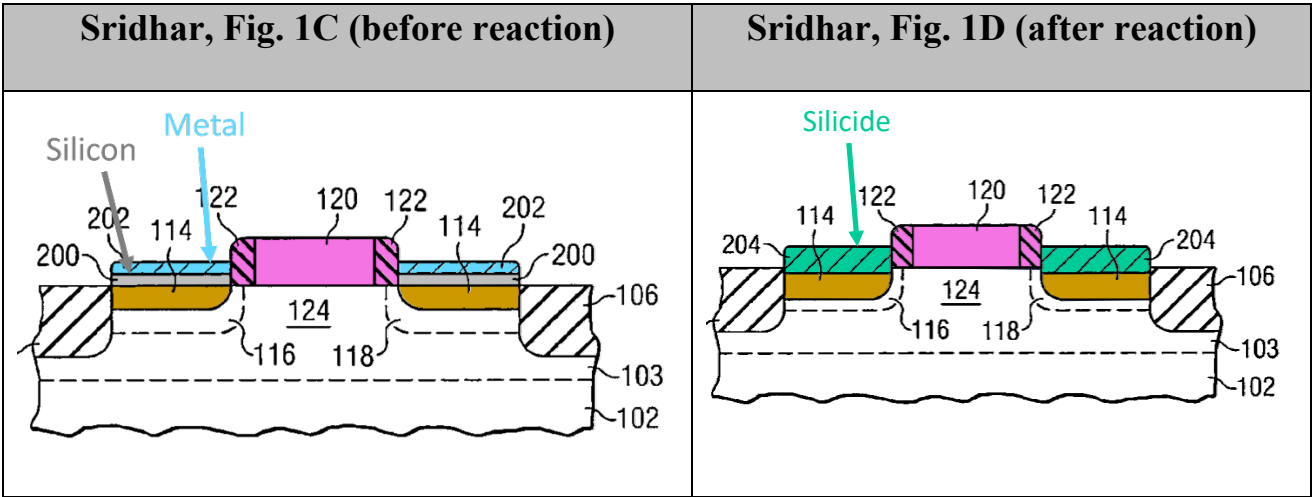
124. Figure 4N of Koontz is reproduced below.



EX1004-Koontz, Fig. 4N (annotated)

As shown above, silicide region 452 (teal) (the claimed “silicide layer”) is formed on recess structures 446 (brown) (the claimed “first strained layer”). EX1004-Koontz, Fig. 4N, ¶[0066]. For example, Koontz discloses that silicide regions 452 “are formed on active regions and gate electrodes 414,” including recess structures 446. Koontz, ¶[0066], Fig. 4N. Koontz teaches that silicide 196 “are formed ... by a suitable silicidation process.” Koontz, ¶[0066]. For example, Koontz discloses that silicide regions 452 may be formed “by depositing a refractory metal (e.g., nickel, cobalt, titanium, alloys thereof, and the like) over the device and inducing (e.g., by annealing) the deposited refractory metal to react with underlying silicon forming silicide regions that reduce contact resistance between active regions and electrodes with contacts, interconnects, and the like.” Koontz, ¶[0066].

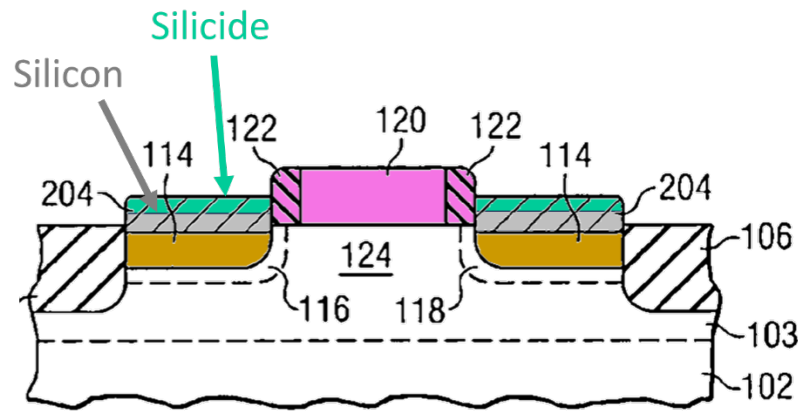
126. Koontz discloses using a “suitable silicidation process” to form silicide regions 452, and Sridhar provides examples of such processes for forming these silicide regions. EX1004-Koontz, ¶[0052]. An example of such a technique is illustrated below.



In the example above, a silicon capping layer 200 is formed on source/drain regions 114. EX1007-Sridhar, ¶[0015] (“In one embodiment, a thickness of silicon layer 200 is between approximately 25 angstroms and 150 angstroms.”), Fig. 1B. Then, a metal layer 202 is deposited on and reacted with silicon capping layer 200 to form a silicide layer 204. *Id.*, ¶[0016] (“[A] reactive metal layer 202 is disposed outwardly from silicon layer 200 for the salicidation process.”), Figs. 1C, 1D.

127. Although Sridhar’s Figure 1D shows a process in which salicide layer 204 has reacted with “all of silicon layer 200,” Sridhar teaches that “[d]epending on the thicknesses of SiGe layer 114, silicon layer 200, reactive metal 204, and the

process conditions within the processing chamber, silicide layer 204 may react with *only a portion* of silicon layer 200....” *Id.*, ¶[0017] (emphasis added). As the annotated figure below illustrates, when the silicide layer 204 only reacts with a portion of silicon layer 200, a portion of silicon layer 200 would remain over the silicon-germanium source/drain region after the reaction is complete.



EX1007-Sridhar, Fig. 1D.

iii. Motivation to combine

128. In my opinion, it would have been obvious to a person of ordinary skill in the art to combine the teachings of Sridhar with the semiconductor structure of Koontz. As explained above, Koontz teaches forming a silicide region 452 (the claimed “silicide layer”) on recess structures 446 (the claimed “strained layer”). EX1004-Koontz, ¶[0066], Fig. 4N. Sridhar teaches that certain advantageous techniques for forming a silicide layer result in a residual silicon layer remaining on the strained layer after formation of the silicide layer is complete. Moreover, a

person of ordinary skill in the art would have had a reasonable expectation of success in combining the teachings of Koontz and Sridhar in the proposed manner.

129. As I explained above, Koontz itself teaches that silicide region 452 is formed “by a suitable silicidation process.” EX1004-Koontz, ¶[0066]. Thus, Koontz expressly encourages a person of ordinary skill in the art to seek out external sources that disclose the details regarding the formation of Koontz’s silicide layer.

130. A person of ordinary skill in the art at the time—circa the early to mid-2000s—would have been well aware of standard fabrication practices for forming silicide layers over strained source/drain structures. These practices were extensively discussed in technical literature and reflected in industry roadmaps such as the International Technology Roadmap for Semiconductors (ITRS). *See 2005 ITRS Roadmap – Front End Processes* (<https://www.semiconductors.org/wp-content/uploads/2018/08/2005FEP.pdf>) at 38. Widely known textbooks like Wolf & Tauber, *Silicon Processing for the VLSI Era*, Vol. 2 (1990) also detailed the growing use of strained silicon, SiGe and SiC layers, and the widespread implementation of ion implantation and silicidation techniques for performance enhancement. These resources confirmed that a thin silicon cap over strained layers—whether for dopant activation, silicidation uniformity, or electrical tuning—was already a well-known optimization strategy. Thus, the combination of Sridhar’s

approach with Koontz's structure would have been viewed by a POSITA as a routine refinement aligned with industry expectations and the trajectory of scaling-era process development.

131. A person of ordinary skill in the art also would have been motivated to turn to the teachings of Sridhar to provide additional details for the regions layer of Koontz because Sridhar specifically discloses that its techniques for forming a silicon layer on the strained layer are beneficial. For instance, Sridhar discloses that electrical performance of the transistor may be degraded if the silicide layer is formed directly on the strained layer (i.e., with no silicon layer in between). EX1007-Sridhar ¶[0003] (explaining that forming the silicide layer directly on the strained layer “may counteract the benefits [of a strained channel] by increasing source/drain resistances”). To address this issue, Sridhar teaches that it would be beneficial to add a thin silicon layer between the strained layer and the silicide layer. *Id.*, ¶¶[0005], [0015]. Sridhar teaches that using its technique “decreases the source/drain resistances that would have occurred if [the silicide layer had been formed] directly over [the strained] layers....” *Id.*, ¶[0015]; *see also id.*, ¶[0005]. Koontz itself identifies “reduc[ing] contact resistance between active regions and electrodes” to be a desirable objective. EX1004-Koontz, ¶[0066].

132. Moreover, while Sridhar explicitly teaches this silicon cap configuration, even if not expressly stated in every reference, a person of ordinary skill in the art would have inferred the inclusion of such a cap as a logical design optimization. By 2005, a person of ordinary skill in the art would have been familiar with using thin silicon layers to improve silicide uniformity, minimize interfacial defects, and preserve strain. Techniques such as selective epitaxial growth and solid-phase epitaxy were routinely used to deposit conformal, low-defect silicon layers over SiGe or SiC structures prior to silicidation. These methods were known to enhance both manufacturability and device performance, and were supported by widespread industry adoption and discussion in technical literature (e.g., Sze & Ng; Wolf & Tauber). Accordingly, a person of ordinary skill in the art would have viewed the presence of a silicon cap as a known solution aligned with established process flows.

133. Notably, Sridhar explicitly teaches preserving a silicon layer above the strained region after silicidation to achieve improved device characteristics. Therefore, a person of ordinary skill in the art would have been motivated to preserve a silicon layer between Koontz's recess structures and silicide layer to obtain known benefits, including improved electrical performance of the transistor (e.g., reduced source/drain resistances).

134. A person of ordinary skill in the art would have recognized that leaving a residual silicon capping layer after the silicidation reaction offers several advantages over fully consuming the silicon layer. First, the residual layer provides a buffer that increases robustness to process variations, such as unintentional overreaction due to thermal fluctuations or extended annealing times. This buffer helps ensure that the silicidation reaction does not consume or damage the underlying strained silicon-germanium or silicon-carbon source/drain regions, helping to maintain the desired stress profile and associated mobility enhancements in the transistor channel. Second, preserving a thin layer of unreacted silicon protects the structural integrity of the junction, helping to prevent strain relaxation, dislocation generation, or silicide encroachment into sensitive regions. Third, the residual cap layer contributes to more uniform silicide formation and reduces the likelihood of agglomeration, particularly in scaled devices where silicide stability is more difficult to control. These benefits are reflected in prior art, including Sridhar itself, which teaches that its silicon capping approach is compatible with conventional process flows and may be “dropped in” to existing structures, such as those disclosed in Koontz and Samoilov.

135. A person of ordinary skill in the art also would find the proposed combination of Koontz and Sridhar to be consistent with the objectives of material

compatibility and strain integrity. For example, as noted above, Sridhar describes its process “as a drop-in” to conventional flows that can be integrated without degrading device performance. At that time, it was common practice to optimize interface quality and stress preservation through techniques like low-temperature epitaxial growth and pre-clean steps. Accordingly, a person of ordinary skill in the art would have reasonably expected the benefits of Sridhar’s approach to translate directly to the Koontz structure without introducing new compatibility risks.

136. Additionally, the combination of Koontz and Sridhar would have yielded predictable results because Koontz and Sridhar each describe similar semiconductor structures and similar techniques for forming such structures. For instance, Koontz teaches a “semiconductor device fabrication by tailoring a vertical channel strain profile by selecting and controlling composition of strain inducing materials... such as silicon-carbon and silicon-germanium....” EX1004-Koontz, ¶[0018]. The process of Koontz is “can be applied to NMOS and/or PMOS devices.” *Id.*, ¶[0029]. Like Koontz, Sridhar discloses fabrication techniques for NMOS and PMOS transistors that include “forming a silicon-germanium layer in each of the source and drain regions....” EX1007-Sridhar, ¶[0004]; *see also id.*, ¶¶[0001], [0010]. Indeed, Sridhar expressly states that its technique for forming a silicon layer

on the strained layer may be integrated into existing processing technologies like those used by Koontz “as a drop-in” solution. *Id.*, ¶[0017]; *see also id.*, ¶[0005].

137. Both references disclose MOSFET transistors with strained source/drain regions formed using silicon-germanium or silicon-carbon, and both describe forming silicide layers over these regions to enhance performance. Their process steps and resulting structures are materially similar, enabling straightforward integration. For example, notable similarities between the Koontz’s and Sridhar’s semiconductor structures include:

- Koontz and Sridhar both disclose MOSFET transistors, including NMOS and PMOS transistors, with source/drain regions and gate structures. EX1004-Koontz, ¶¶[0053]-[0054], [0057], [0061], [0065], Fig. 4N; EX1007-Sridhar, ¶¶[0010]-[0013], Fig. 1D.
- Koontz and Sridhar both disclose improving the performance of the transistor by using a strained layer in the source/drain regions. EX1004-Koontz, ¶¶[0017], [0026]; EX1007-Sridhar, ¶¶[0003], [0014].
- Koontz and Sridhar both disclose forming the strained layer using silicon germanium or other types of stress-inducing materials. EX1004-Koontz, ¶¶[0008], [0018], [0025]-[0027], [0034], [0047], [0050], [0059]-[0060], [0063]-[0064]; EX1007-Sridhar, ¶¶[0003], [0012], [0014].

known semiconductor structures and processing techniques would have been used to improve similar semiconductor structures described in Koontz in a similar manner. For instance, Koontz discloses a semiconductor structure having a strained layer with a silicide layer. EX1004-Koontz, ¶¶[0052], [0066], Fig. 4N. Sridhar discloses a technique to form the silicide layer in a way that improves its electrical characteristics (e.g., by forming a silicon layer on the strained layer that is only partially consumed when forming the silicide layer). Thus, the teachings of Sridhar would have been applied to the structure disclosed in Koontz in the same manner as they are used in Sridhar itself.

139. I note that it would have been obvious to apply the teachings of Sridhar as I described above to either (or both) the PMOS and NMOS transistors described in Koontz. Sridhar expressly discloses that its teachings are equally applicable to “NMOS, PMOS, CMOS, or other suitable semiconductor device.” EX1007-Sridhar, ¶[0010]. A person of ordinary skill in the art would have understood this to mean that the silicon capping layer described in Sridhar is formed on either (or both) silicon-germanium (for PMOS) or silicon-carbon (for NMOS) strained layers.

140. With respect to silicon-germanium, Sridhar expressly teaches embodiments where a silicon layer is formed over a silicon-germanium strained

layer. *Id.* This embodiment is applicable to the PMOS transistor described in Koontz. EX1004-Koontz, ¶¶[0041], [0053].

141. With respect to silicon-carbon, the application of the Sridhar's silicon capping layer to a silicon-carbon strained layer would have been obvious. As I explained above, Sridhar itself discloses that its teachings are equally applicable to PMOS and NMOS transistors. EX1007-Sridhar, ¶[0010]. Like Sridhar, Koontz teaches that the same process for forming a silicide layer is applicable to both the PMOS and NMOS transistors. EX1004-Koontz, Fig. 4N (showing silicide regions 425 overlying the source and drain regions of both the PMOS and NMOS transistors). Other prior art references confirm that it would have been obvious to a person of ordinary skill in the art to form silicon layer on a strained layer composed of silicon-carbon when applying the teachings of Sridhar to the NMOS transistors of Koontz. *See* EX1005-Samoilov, ¶¶[0035]-[0036] (describing a process for forming a silicide layer on a strained layer composed of either silicon germanium or silicon-carbon, where the process includes first forming a "silicon-containing layer 148" on the strained layer that has, and where silicon-containing layer 148 contains "little or no germanium or carbon").

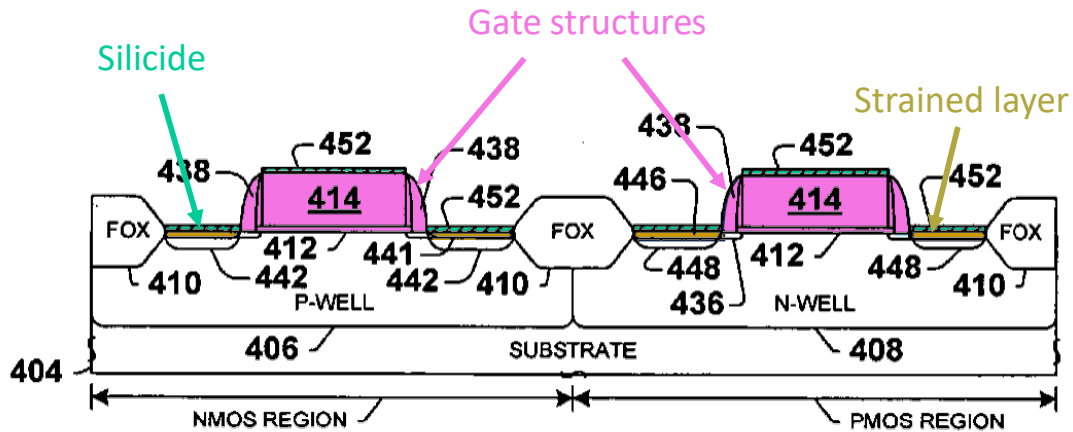
142. A person of ordinary skill in the art would have reasonably expected success in forming a thin silicon cap on a silicon-carbon layer, given widespread use

of silicon passivation and the availability of deposition techniques such as selective epitaxy, which are compatible with both SiGe and SiC alloys. Accordingly, applying the teachings Sridhar to the NMOS transistors of Koontz with silicon-carbon strained layers would have been a straightforward application of known techniques.

c. Element [8B]: “a metal silicide layer on the silicon layer, the source/drain region and the first and the second gate structures”

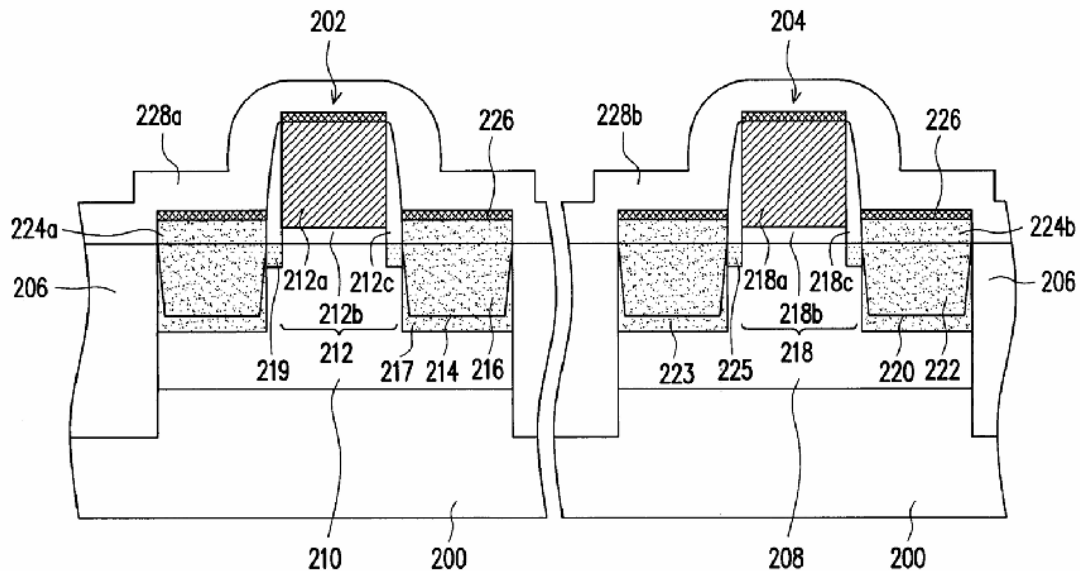
143. As I explained above in Section XI.B.1.b for Element [8A], the combination of Koontz and Sridhar teaches a metal silicide layer (e.g., Koontz’s silicide regions 452) on a silicon layer (e.g., Koontz’s recess structures 446, where the recess structures are only partially consumed during the silicide formation process, as taught by Sridhar).

144. Figure 4N of Koontz is reproduced below.



EX1004-Koontz, Fig. 4N (annotated)

As shown above, Koontz further teaches that silicide regions 452 (teal) are on source/drain region 446 (brown) and on the gate structures (including gate electrode 414, gate oxide 412, and sidewall spacers 438) (magenta). EX1004-Koontz, Fig. 4N, ¶[0066]. This is consistent with embodiments of the '822 patent, such as Figure 2, which shows a silicide layer 226 that is located directly on top of silicon layers 224a and 224b and gate structures 212 and 218, and is further located on strained layers 216 and 222 via intervening silicon layers 224a and 224b. EX1001-USP'822, 5:61-6:7.



EX1001-USP'822, Fig. 2

2. Claim 10

145. Claim 10 recites the same limitations as claim 8, except it depends from claim 9 rather than claim 7. Thus, as I explained above, the Koontz-Sridhar combination satisfies claim 10 for the reasons I described in Sections XI.A.8 (Claim 9) and XI.B.1 (Claim 8).

3. Claim 14

a. **Element [14Pre]: “The semiconductor structure of claim 11”**

146. Claim 14 depends from claim 11, which, as I explained above, Koontz satisfies. *Supra* §XI.A.9.

b. Element [14A]: “a silicon layer on the first strained layer and the second strained layer”

147. As I explained above in Sections XI.A.1.e and XI.A.9.c for Elements [1D] and [11B], Koontz discloses a first strained layer and a second strained layer. Moreover, as I explained above in Section XI.B.1.b for Element [8A], Koontz in view of Sridhar renders obvious the formation of a silicon layer on the strained layers.

c. Element [14B]: “a metal silicide layer on the silicon layer and the first and second gate structures”

148. Element [14B] recites the same subject matter as Element [8B], which I addressed above. Namely, Element [14B] recites that “a metal silicide layer on the silicon layer and the first and second gate structures,” which substantively the same as Element [8B]. The only difference is that Element [8B] additionally requires the metal silicide layer to be on the source/drain region. As such, my analysis above regarding Element [8B] (Section XI.B.1.c) equally applies here. Therefore, Koontz in view of Sridhar discloses this limitation.

C. GROUND 2: Claims 1-4 Are Invalid as Anticipated by Orlowski.

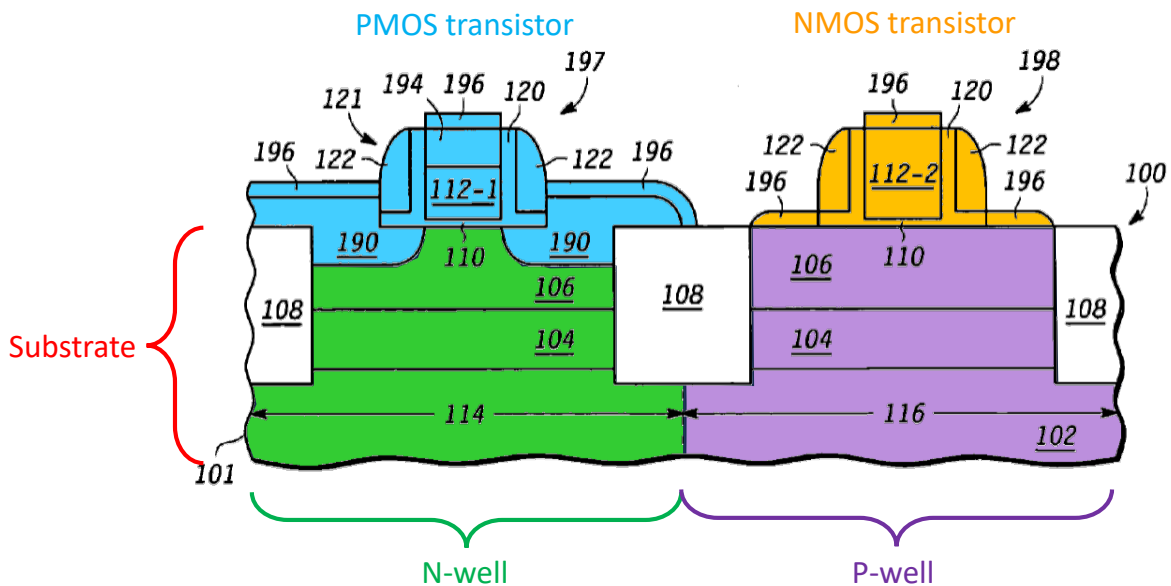
149. As detailed below, Orlowski anticipates claims 1-4 of the '822 patent.

1. **Claim 1**

a. **Element [1Pre]: “A semiconductor structure, comprising:”**

150. To the extent the preamble is limiting, Orlowski discloses “a semiconductor structure.” For example, Orlowski discloses a semiconductor structure, such as a CMOS integrated circuit, “having [stress-inducing source/drain] structures characterized by a composition gradient.” EX1006-Orlowski, 2:62-65; *see also id.*, Abstract, 1:35-44, 2:34-61, 3:64-4:10, 7:48-51.

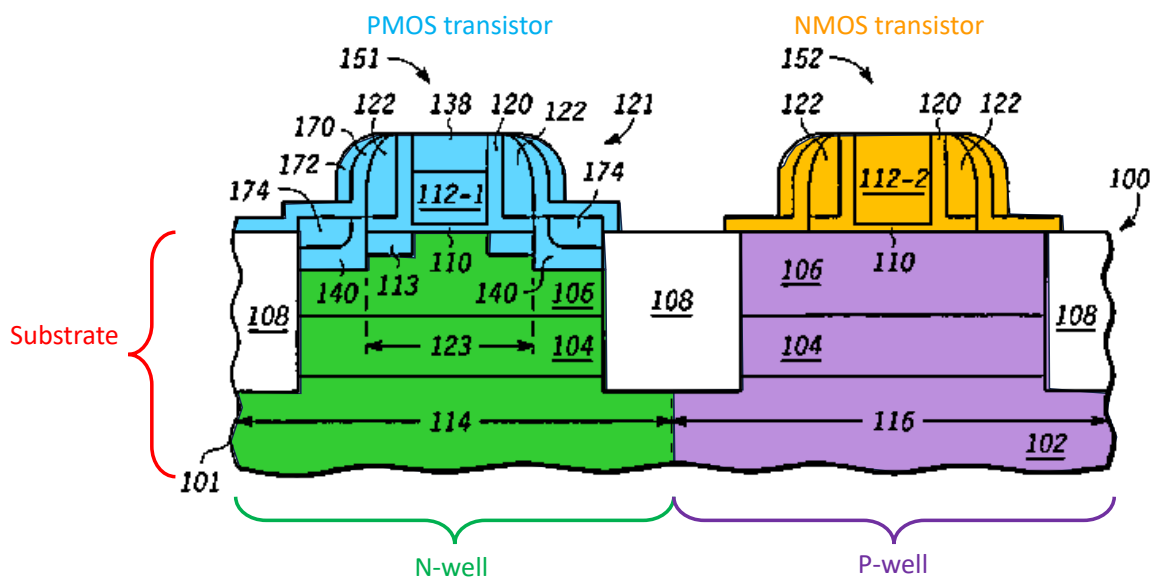
151. One embodiment of Orlowski’s semiconductor structure is shown in Figure 13, reproduced below.



EX1006-Orlowski, Fig. 13 (annotated)

As shown in Figure 13 above, the semiconductor structure of Orlowski includes a substrate 101 with a PMOS transistor 197 (blue) on an N-well 114 (green) and an NMOS transistor 198 (orange) on a P-well 116 (purple).

152. A second embodiment of Orlowski's semiconductor structure is shown in Figure 13, reproduced below.



EX1006-Orlowski, Fig. 8 (annotated)

Like Figure 13, Figure 8 shows semiconductor structure that includes a substrate 101 with a PMOS transistor 151 (blue) on an N-well 114 (green) and an NMOS transistor 152 (orange) on a P-well 116 (purple). EX1006-Orlowski, 7:15-16.

153. Orlowski expressly analogizes between the semiconductor structure depicted in Figure 8 and the semiconductor structure depicted in Figure 13, and the applicability of Orlowski's disclosures to either or both of these structures is readily

ascertainable. Solely to avoid duplicative analysis, I focus my analysis below on the embodiment depicted in Figure 13 (unless otherwise noted). However, as my analysis below makes clear, it is my opinion that the embodiments shown in Figures 8 and 13 each independently satisfy the challenged claims for similar reasons.

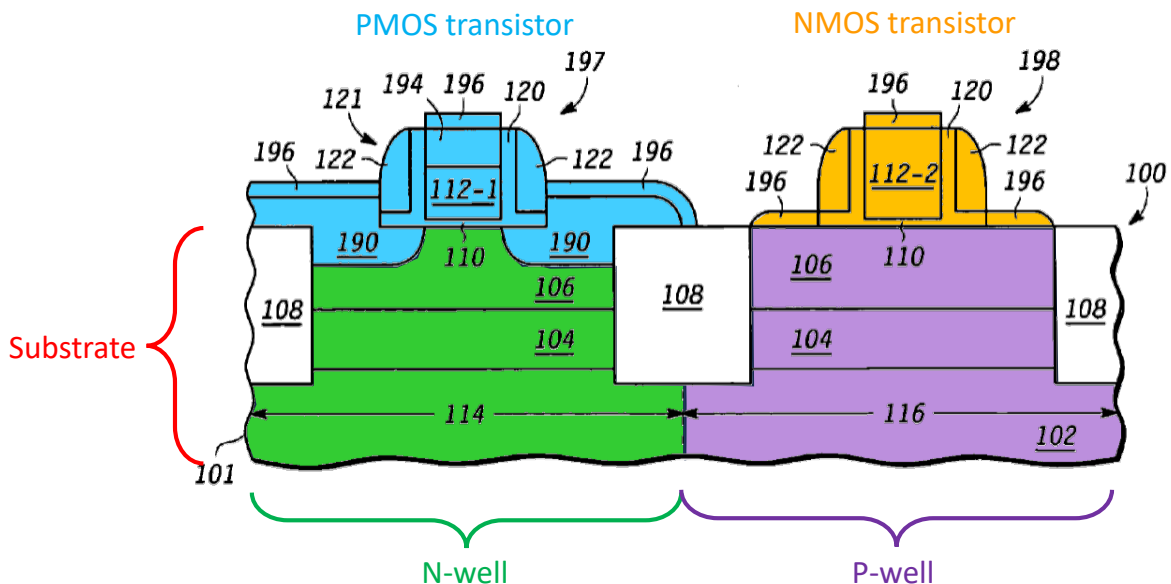
b. Element [1A]: “a substrate, having therein a first well of a first conductivity type and a second well of a second conductivity type”

154. Orlowski discloses “a substrate, having therein a first well of a first conductivity type and a second well of a second conductivity type.” A person of ordinary skill in the art would have understood that the Element [1A] encompasses arrangements where “first conductivity type” is p-type and the “second conductivity type” is n-type, or the reverse – the “first conductivity type” is n-type and the “second conductivity type” is p-type. In either case, Orlowski discloses these limitations.

155. Orlowski identifies the substrate for its semiconductor structure as “wafer 101.” EX1006-Orlowski, 3:9-20 (“The depicted embodiment of wafer 101 is a silicon-on-insulator (SOI) wafer in which a semiconductor layer 106 overlies a buried oxide (BOX) layer 104. BOX layer 104 overlies a substrate bulk 102.... In other embodiments (not depicted), wafer 101 is a ‘bulk’ wafer that does not include a BOX layer 104.”). Orlowski further teaches that wafer 101 comprises single

crystal silicon. *Id.* (“In one embodiment, substrate bulk 102 comprises single crystal silicon, BOX layer 104 is a silicon dioxide layer, and semiconductor layer 106 is another crystalline silicon layer.”). A person of ordinary skill in the art would have understood that wafer 101 corresponds to the claimed “substrate.”

156. Wafer 101 (the claimed “substrate”) includes multiple wells (N-well) and (P-well), as illustrated below.



EX1006-Orlowski, Fig. 13 (annotated)

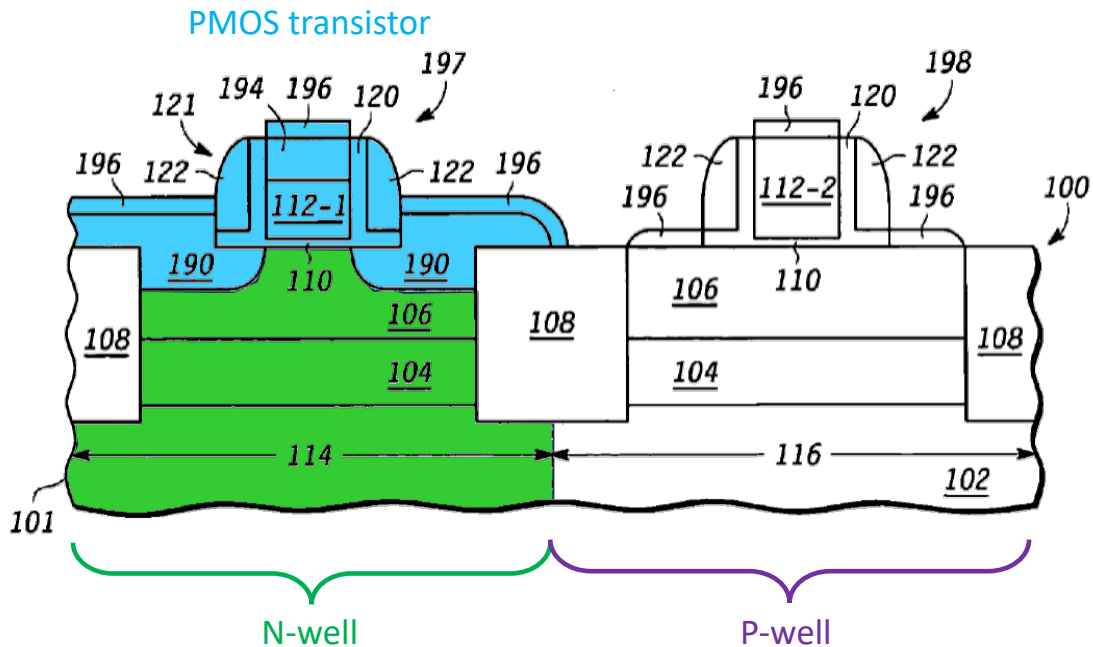
Orlowski teaches that N-well 114 (“first well region 114”) (green) and P-well 116 (“second well region 116”) (purple) are formed on the substrate 101. EX1006-Orlowski, 3:21-25 (“In the depicted embodiment, two gate electrodes 112 are shown where first gate electrode 112-1 overlies a first region (referred to herein as the first well region) 114 of substrate 102 and a second gate electrode 112-2 overlies a second

well region 116.”). N-well 114 (green) is n-doped and P-well 116 (purple) is p-doped. EX1006-Orlowski, 3:25-32 (“In one embodiment, semiconductor layer 106 in first well region 114 is n-doped (thereby making it suitable for forming PMOS transistors) while semiconductor layer 106 in second well region 116 is p-doped (thereby making it suitable for forming NMOS transistors). In this embodiment, first well region 114 may be referred to as PMOS region 114 and second well region 116 may be referred to as NMOS region.”).

c. Element [1B]: “a first MOS transistor of the first conductivity type on the second well, comprising:”

157. Orlowski discloses “a first MOS transistor of the first conductivity type on the second well.”

158. Figure 13 of Orlowski is reproduced below:



EX1006-Orlowski, Fig. 13 (annotated)

As shown in Figure 13 above, PMOS transistor 197 (blue) is located on N-well 114 (green). EX1006-Orlowski, Fig. 13, 8:32-36 (“FIG. 13 depicts an integrated circuit 100 including a first transistor 197 and a second transistor 198. First transistor 197 includes a gate structure 121 overlying a semiconductor layer 104 in a first well region 114 of wafer 101.”). For example, Orlowski discloses that N-well 114 is “suitable for forming PMOS transistors” and that portions of PMOS transistor 197 (blue) “overl[ie]” N-well 114. EX1006-Orlowski, 3:21-31 (“In one embodiment, semiconductor layer 106 in first well region 114 is n-doped (thereby making it suitable for forming PMOS transistors) while semiconductor layer 106 in second well region 116 is p-doped (thereby making it suitable for forming NMOS

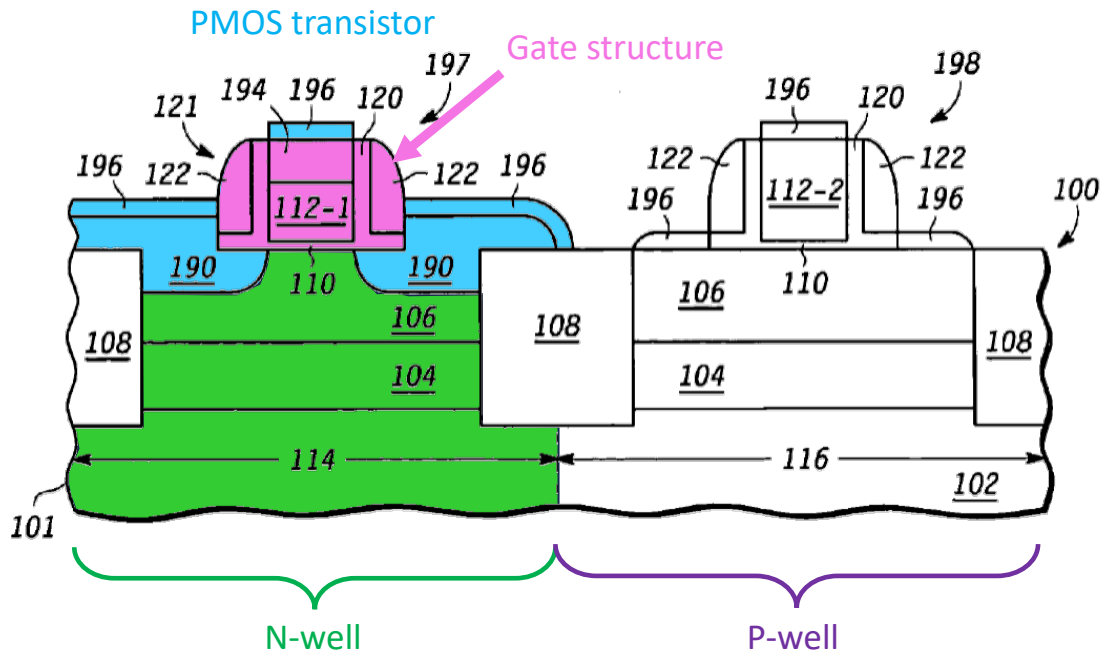
transistors).”), 8:32-36, Fig. 13. Thus, a person of ordinary skill in the art would have understood that PMOS transistor 197 is a “first MOS transistor of the first conductivity type” (e.g., p-type).

159. Moreover, Orłowski analogizes PMOS transistor 197 in Figure 13 to PMOS transistor 151 in Figure 8. Like PMOS transistor 197 in Figure 13, PMOS transistor 151 in Figure 8 overlies N-well 114 (green). *Id.*, 7:15-19, 7:35-37, 8:32-36.

d. Element [1C]: “first MOS transistor...comprising: a first gate structure on the second well”

160. Orłowski discloses “a first gate structure on the second well.”

161. Figure 13 of Orłowski is reproduced below.



EX1006-Orlowski, Fig. 13 (annotated)

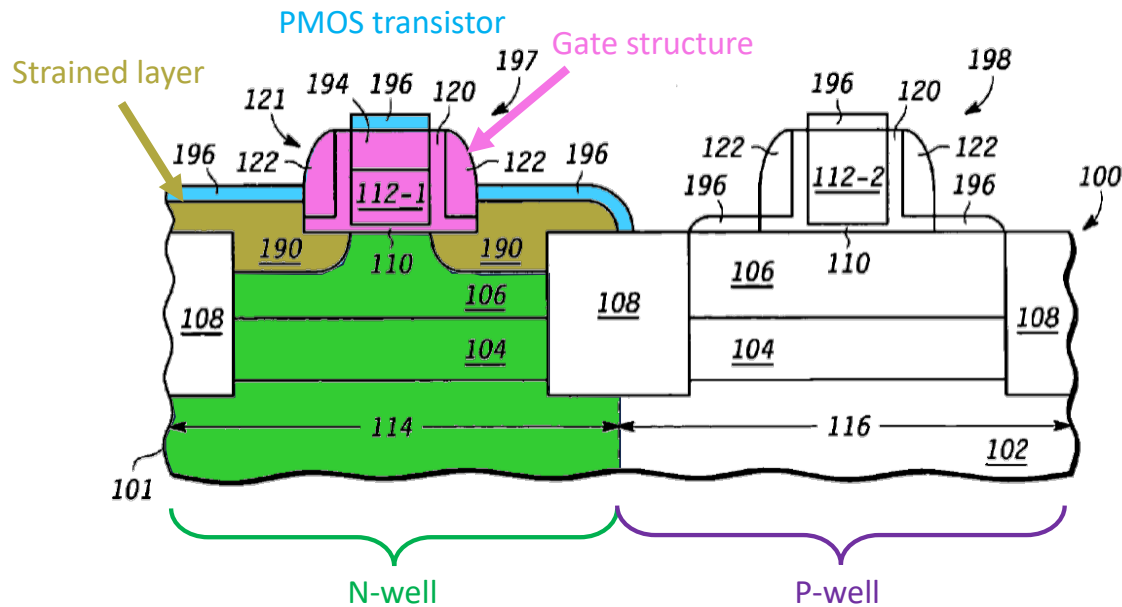
As shown in Figure 13, PMOS transistor 197 (blue) (which as I explained above corresponds to the first MOS transistor of claim 1) includes gate structure 121 (magenta), which includes “gate electrodes 112, liner 120, and spacers 122....” EX1006-Orlowski, Fig. 13, 3:57-62, 8:32-36. Gate structure 121 overlies a N-well 114 (green). EX1006-Orlowski, 8:32-36, Fig. 13. As I explained above, N-well 114 (green) corresponds to the claimed “second well.” Thus, gate structure 121 corresponds to a “first gate structure on the second well.”

- e. **Element [1D]: “first MOS transistor...comprising: ... a first strained layer of the first conductivity type in a first opening in the second well beside the first gate structure, wherein a difference between a lattice parameter of a portion of the first strained layer near**

a bottom of the first opening and a lattice parameter of the substrate is smaller than a difference between a lattice parameter of a portion of the first strained layer apart from the bottom of the first opening and the lattice parameter of the substrate”

162. Orlowski discloses “a first strained layer of the first conductivity type in a first opening in the second well beside the first gate structure, wherein a difference between a lattice parameter of a portion of the first strained layer near a bottom of the first opening and a lattice parameter of the substrate is smaller than a difference between a lattice parameter of a portion of the first strained layer apart from the bottom of the first opening and the lattice parameter of the substrate.”

163. I will first address the portion of Element [1D] reciting “a first strained layer of the first conductivity type in a first opening in the second well beside the first gate structure.” Referring to Figure 13 below, Orlowski discloses that PMOS transistor 197 (the claimed “first MOS transistor”) comprises “a first strained layer of the first conductivity type in a first opening in the second well beside the first gate structure.”

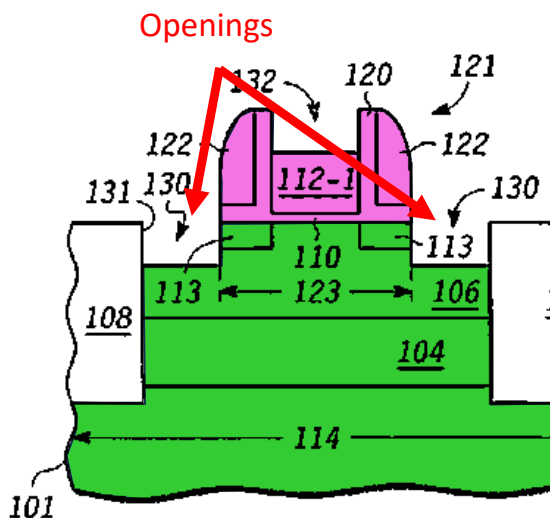


EX1006-Orlowski, Fig. 13 (annotated)

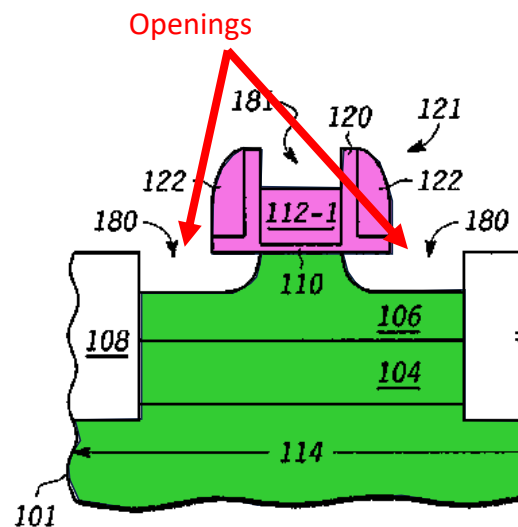
As shown above, PMOS transistor 197 includes a strain inducing source/drain structures 190 (brown) (the claimed “first strained layer”) of the first conductivity type (e.g., p-type) in source/drain recesses 180 (the claimed “first opening,” which is shown in Fig. 9) in N-well 114 (green) (the claimed “second well”) beside gate structure 121 (magenta) (the claimed “first gate structure”). EX1006-Orlowski, Fig. 13, 3:57-62, 8:32-36. Like the ’822 patent, Orlowski teaches that these strain-inducing structures create compressive or tensile stress in the underlying channel region to improve transistor performance. EX1006-Orlowski, 8:4-8; *see also id.*, 1:15-27, 8:39-41.

164. Orlowski’s strain inducing source/drain structures 190 (brown) (which correspond to the claimed “first strained layer”) have a first conductivity type (e.g., p-type). The conductivity type is achieved by introducing “a proper source/drain impurity ... either in situ or by ion implantation.” EX1006-Orlowski, 8:4-56. As I explained above in section VII.B-C, a person of ordinary skill in the art would have understood that PMOS transistors have source/drain regions doped with p-type dopants, such as boron. *Id.*, 3:38-41, 5:30-35, 6:29-38, 6:52-58.

165. Orlowski teaches that strain inducing source/drain structures 190 are located in openings (e.g., source/drain recesses 180) in N-well 114 beside gate structure 121. Figures 4 and 9 of Orlowski are reproduced below.



Orlowski, Fig. 4 (excerpted)

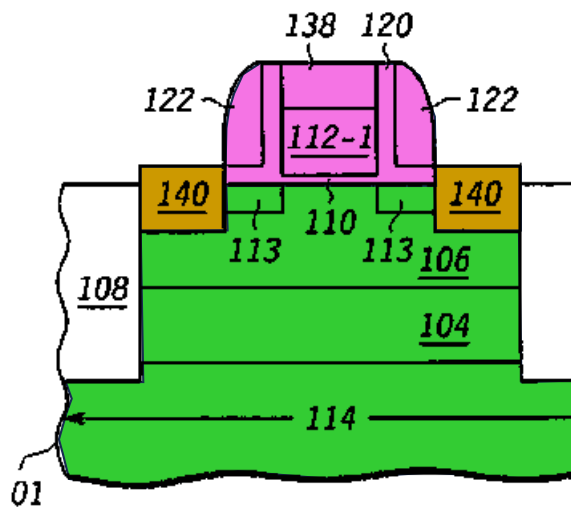


Orlowski, Fig. 9 (excerpted)

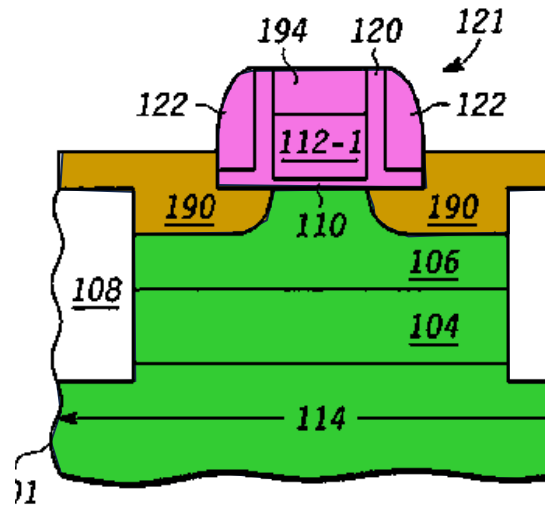
As shown in Figures 4 and 9 above, during manufacturing, Orlowski discloses forming openings N-well 114 (green) aligned with gate structure 121 (magenta).

Depending on the method used to form the openings, the openings may open straight downward into substrate 101 (Figure 4), or may undercut gate structure 121 (Figure 9). EX-1006-Orlowski, 7:53-64, 4:30-38. In both embodiments, the openings are located next to gate structure 121.

166. Moreover, Figures 5 and 10 of Orlowski are reproduced below.



Orlowski, Fig. 5 (excerpted)



Orlowski, Fig. 10 (excerpted)

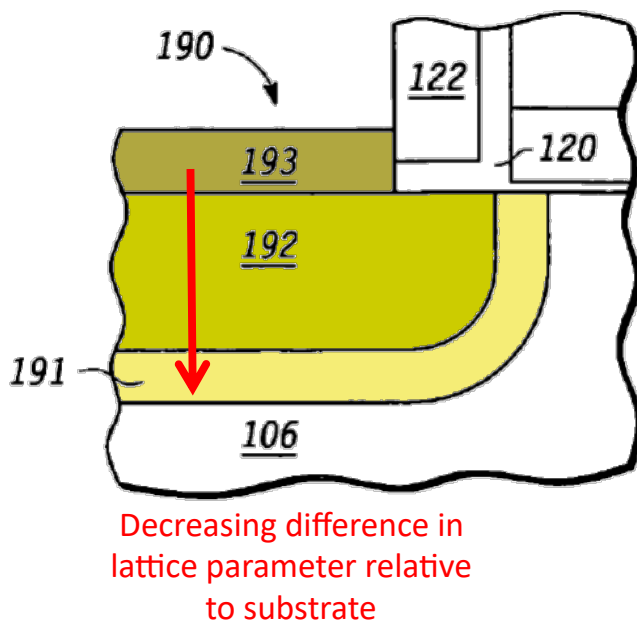
As shown in Figures 5 and 10 of Orlowski above, the openings in N-well 114 are “filled with” the strain inducing source/drain structures (brown). EX-1006-Orlowski, 8:3-4, 4:58-61. Thus, Orlowski teaches multiple techniques for forming a “first strained layer...beside the first gate structure.”

167. Next, I will address the portion of Element [1D] reciting that “a difference between a lattice parameter of a portion of the first strained layer near a bottom of the first opening and a lattice parameter of the substrate is smaller than a

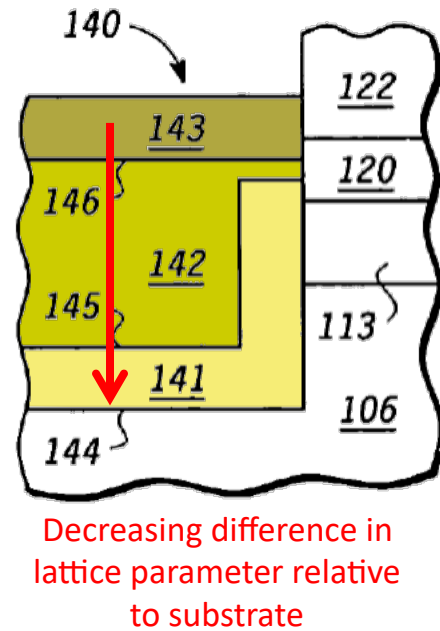
difference between a lattice parameter of a portion of the first strained layer apart from the bottom of the first opening and the lattice parameter of the substrate.”

168. Orlowski discloses that strain inducing source/drain structures 190 have a graded composition that produces a vertical variation in lattice parameter. For example, Orlowski teaches that, for a PMOS transistor, strain inducing source/drain structures 190 are formed using “silicon germanium with a graded concentration of germanium.” EX1006-Orlowski, 7:35-38, 8:10-21, 6:18-28; *see also id.*, Abstract, 1:8-11, 2:62-65 (source/drain structures 190 are “characterized by a composition gradient”), 5:4-29, 8:45-53. Specifically, “the percentage of silicon in SISD structures 190 decrease[s] from the bottom of SISD structures 190 to the top.” *Id.*, 8:10-21, such that the composition near the base of structure 190 more closely matches that of substrate 101 (nearly pure silicon), and the lattice parameter near the bottom is therefore closer to that of the substrate. A person of ordinary skill in the art, recognizing that the lattice parameter increase with Ge content, would have understood the mismatch between the strained SiGe and the silicon substrate is smaller near the bottom of the recess and larger toward the top. *See, e.g.*, EX1006-Orlowski, 2:37-40, 5:4-29; *see also* EX1017-Murthy482, 1:45-48 (“Silicon germanium also has a larger lattice constant [than silicon], the extent of which depends on the percentage composition of germanium”); EX1027-Dismukes, Fig. 3.

169. Figure 11 (left) and figure 6 (right) of Orlowski below show embodiments of the graded composition where the difference in lattice parameter becomes smaller near the bottom of the respective strain inducing source/drain structures (brown/yellow).



Orlowski, Fig. 11 (annotated)



Orlowski, Fig. 6 (excerpted)

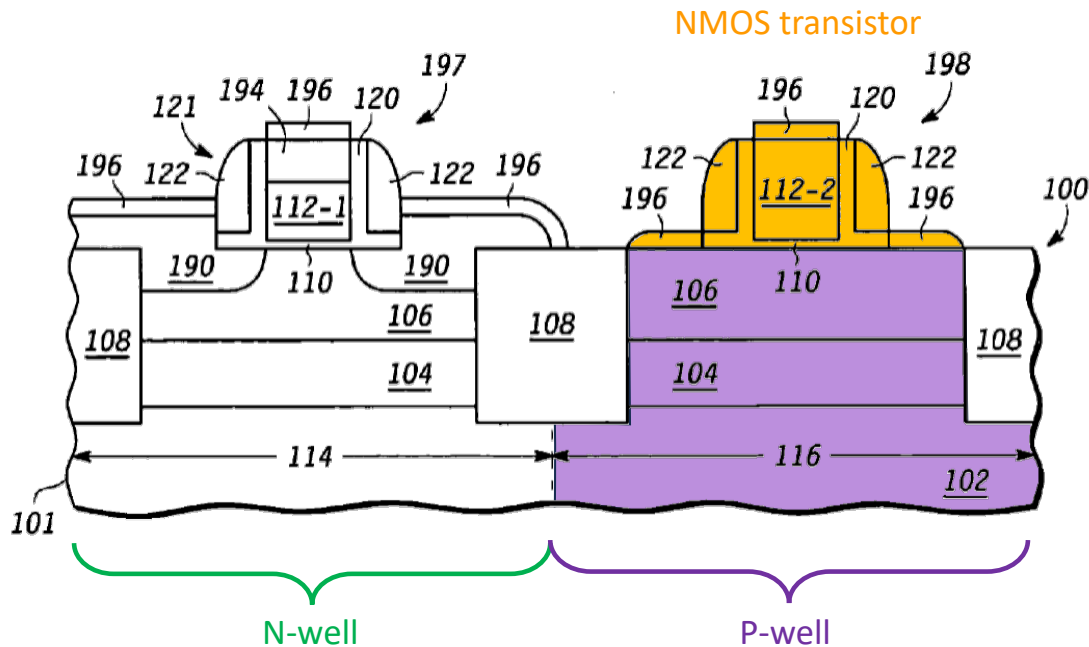
EX1006-Orlowski, 8:17-21 (“In this embodiment, the silicon percentage of SISD structure 190 is greater in first layer 191 than in second layer 192 and the silicon percentage in second layer 192 is greater than the silicon layer in third layer 193.”); 5:63-6:28, 2:17-18, 2:1-3. Accordingly, Orlowski teaches a vertically graded SiGe stressor in which the lattice parameter near the bottom of the recess is closer to that

of the substrate, while the lattice parameter farther from the bottom differs more from the substrate—precisely the relationship required by Claim 1.

f. Element [1E]: “a second MOS transistor of the second conductivity type on the first well.”

170. Orlowski discloses “a second MOS transistor of the second conductivity type on the first well.”

171. Figure 13 of Orlowski is reproduced below.



EX1006-Orlowski, Fig. 13 (annotated)

As shown above, NMOS transistor 198 (orange) is located on P-well 116 (purple).

EX1006-Orlowski, Fig. 13, 8:32-36 (“FIG. 13 depicts an integrated circuit 100 including a first transistor 197 and a second transistor 198.”). For example, Orlowski

discloses that P-well 116 is “suitable for forming NMOS transistors” and portions of NMOS transistor 198 are depicted overlying P-well 116. EX1006-Orlowski, 3:21-31, 8:32-36, Fig. 13. (“In one embodiment, semiconductor layer 106 in first well region 114 is n-doped (thereby making it suitable for forming PMOS transistors) while semiconductor layer 106 in second well region 116 is p-doped (thereby making it suitable for forming NMOS transistors).”), 8:32-36, Fig. 13. Thus, NMOS transistor 198 corresponds to a “second MOS transistor of the second conductivity type” (n-type).

172. Orlowski analogizes NMOS transistor 198 in Figure 13 to NMOS transistor 152 in Figure 8, like NMOS transistor 198, NMOS transistor 152 overlies P-well 116. *Id.*, 7:15-19, 7:35-37, 8:32-36.

2. **Claim 2: “The semiconductor structure of claim 1, wherein the lattice parameter of the first strained layer has a gradient distribution”**

173. Claim 2 depends from claim 1, which, as I explained above, Orlowski teaches. *Supra* §XI.C.1. Moreover, as I explain above in section XI.C.1.e, the lattice parameter of the first strained layer (e.g., strain inducing source/drain structures 190) has a gradient distribution from bottom to top. EX1006-Orlowski, Abstract (“The SISD structure has a composition gradient wherein the percentage of the second element varies from the upper surface of the source/drain structure to a lower surface

of the SISD structure.”), 2:62-65 (“Referring now to the drawings, FIG. 1 through FIG. 9 depict a first embodiment of a semiconductor fabrication method for producing integrated circuits having [strain inducing source/drain structures 190] characterized by a composition gradient”); Element [1D].

174. For example, Figures 7 and 11 of Orlowski are reproduced below.

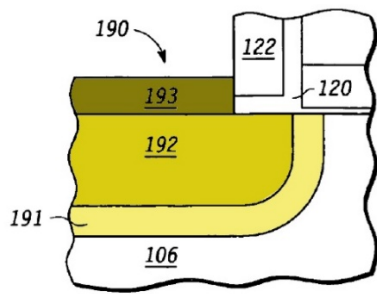


FIG. 11

EX1006-Orlowski, Fig. 11 (annotated)

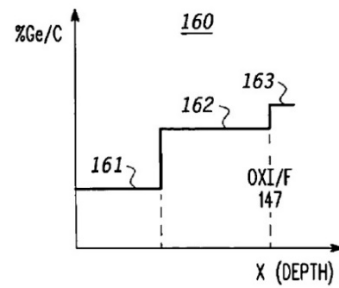


FIG. 7

EX1006-Orlowski, Fig. 7

As shown above, Orlowski’s strain inducing source/drain structures 190 (brown/yellow) have a “stepped composition gradient” with three monotonically increasing levels in terms of the percentage of germanium or carbon in the silicon-germanium or silicon-carbon mixture (the lowest level being at the bottom). *Id.*, 7:29-47; *see also id.*, 5:63-6:14, 8:4-21, 8:41-45. I explained above in Section XI.C.1.e (Limitation [1D]), a person of ordinary skill in the art, would have understood this to mean that the lattice parameter itself has a gradient distribution.

3. **Claim 3: “The semiconductor structure of claim 1, wherein the first conductivity type is P-type, and the lattice parameter of a portion of the first strained layer near the bottom of the first opening is smaller than the lattice parameter of a portion of the first strained layer apart from the bottom of the first opening”**

175. Claim 3 depends from claim 1, which, as I explained above, Orlowski teaches. *Supra* §XI.C.1. Orlowski further discloses that when the first conductivity type is p-type, the lattice parameter of a portion of the first strained layer (e.g., strain inducing source/drain structures 190) near the bottom of the first opening is smaller than the lattice parameter of a portion of the first strained layer apart from the bottom of the first opening.

176. As I previously explained for Limitation [1D], when the first conductivity type is p-type, strain inducing source/drain structures 190 are formed using silicon-germanium. EX1006-Orlowski, Abstract, 1:8-11, 2:40-45, 5:4-29, 5:41-56, 6:22-28, 7:35-38, claims 2, 12. The composition of the silicon-germanium mixture is illustrated in Figures 7 and 11 of Orlowski, reproduced below.

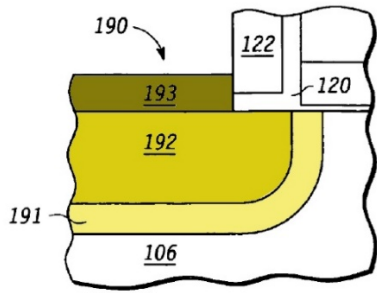


FIG. 11

EX1006-Orlowski, Fig. 11 (annotated)

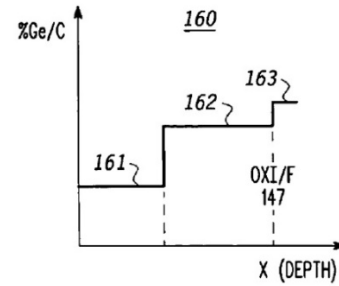


FIG. 7

EX1006-Orlowski, Fig. 7

As shown above, Orlowski's strain inducing source/drain structures 190 (brown/yellow) have a "stepped composition gradient" with three monotonically increasing levels in terms of the percentage of germanium in the silicon-germanium mixture (the lowest level being at the bottom). *Id.*, 7:29-47; *see also id.*, Abstract, 1:8-11, 2:62-65, 5:4-29, 5:63-6:14, 6:18-28, 8:4-21, 8:41-53; *see also* Claim 2. As I explained above in Section XI.C.1.e (Limitation [1D]), a person of ordinary skill in the art would have understood this to mean that the lattice parameter itself is smaller near the bottom of the first opening than in portions apart from the bottom (e.g, near the top).

4. Claim 4: "The semiconductor structure of claim 3, wherein the first strained layer comprises SiGe"

177. Orlowski teaches claim 4 for the reasons in Section XI.C.3 (Claim 3) and XI.A.1.e (Element [1D]). Limitation [1D], claim 3; *see also, e.g.*, EX1006-Orlowski, Abstract, 1:8-11, 2:40-45, 5:4-29, 5:41-56, 6:22-28, 7:35-38, claims 2, 12.

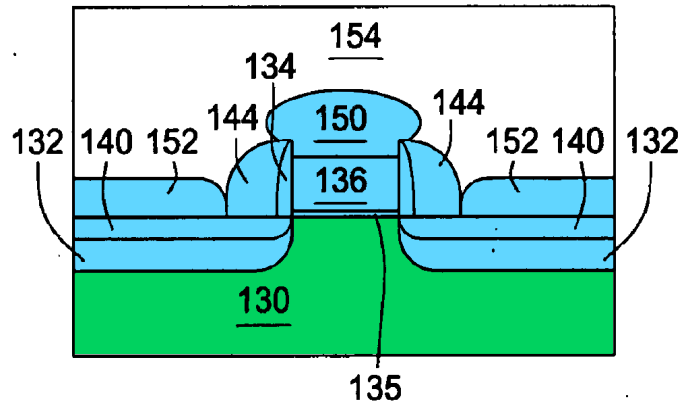
D. GROUND 3A: Claims 1-7, 9, and 11-13 Are Invalid as Obvious Over Samoilov In View of Murthy

1. The Combination of Samoilov and Murthy

a. Samoilov

178. Samoilov describes a MOS transistor architecture that can be configured as either an NMOS or PMOS device, depending on the selection of materials and conductivity types for its components. *See* EX1005-Samoilov ¶¶[0009], [0021], [0027], [0029], [0038]–[0039], [0067]. Specifically, Samoilov explains that “MOSFET devices formed by processes described herein may contain a PMOS component or a NMOS component,” and provides examples of material choices for each configuration. *Id.*, ¶[0067]. For instance, a silicon-containing material such as SiGe may be deposited in a recessed region to form a PMOS component, while a silicon-containing film such as SiC may be used to form an NMOS component.

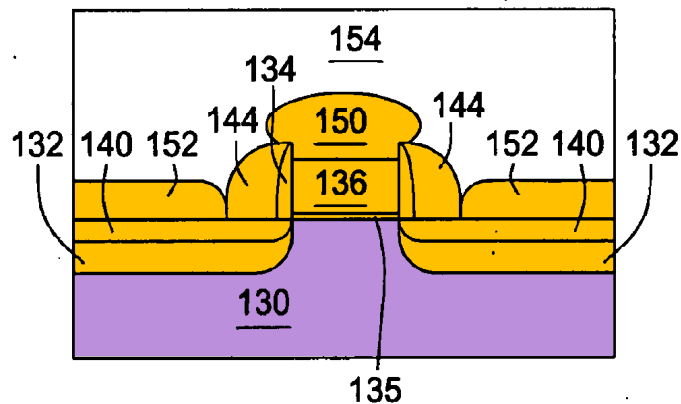
179. Figure 2F of Samoilov is reproduced below.



EX1005-Samoilov, Fig. 2F (annotated)

As shown above, Samoilov discloses a PMOS transistor (blue) (i.e., a “first MOS transistor of the first conductivity type [(p-type)]”) on a doped n-type substrate 130 (green). EX1005-Samoilov, Fig. 2F, ¶¶[0009], [0027], [0029], [0038]-[0039], [0067]-[0068].

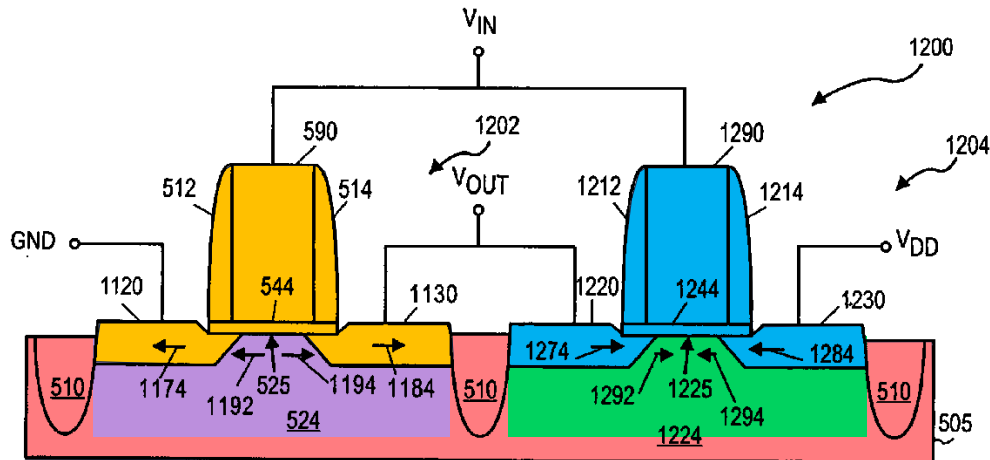
180. Samoilov also teaches NMOS transistors with the same structure depicted in Figure 2F, as illustrated below. See EX1005-Samoilov, ¶[0009], ¶¶[0030]-[0033], ¶¶[0048]-[0049], ¶¶[0067]-[0068].



EX1005-Samoilov, Fig. 2F (annotated)

a. Murthy

181. Figure 12 of Murthy is reproduced below.



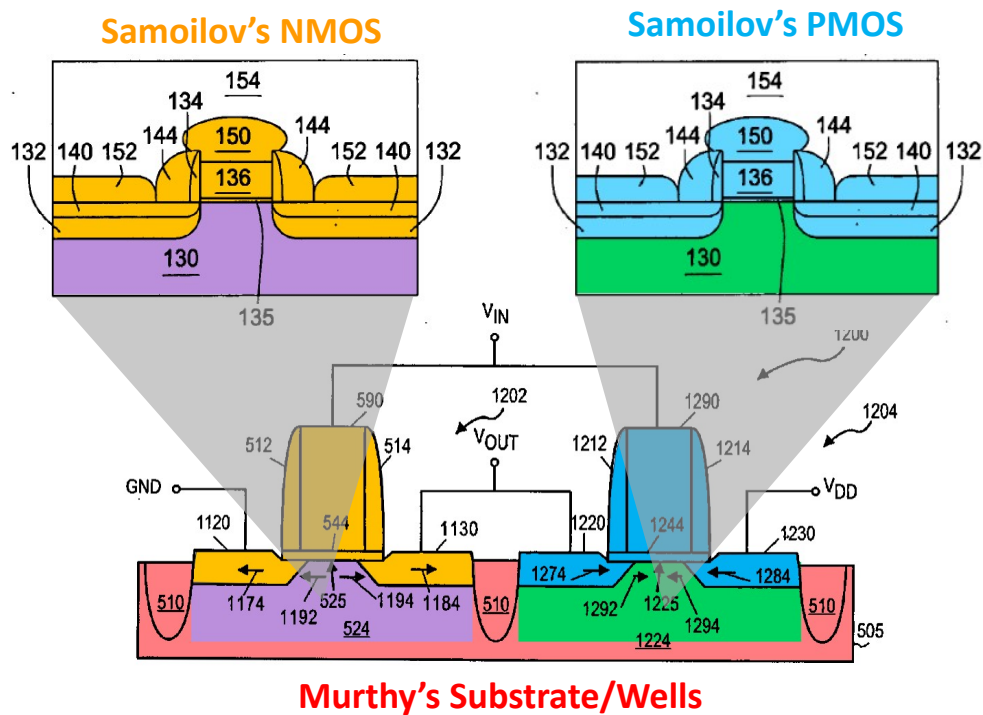
EX1011-Murthy, Fig. 12

As shown above, the semiconductor structure includes a substrate 505 (red), an NMOS transistor (orange) in a P-well 524 (purple) and a PMOS transistor (blue) in an N-well 1224 (green). EX1011-Murthy, 13:50-53, 14:10-12, 23:21-54, 23:5-20. A POSITA would have recognizes this as a typical CMOS configuration involving complementary wells formed in a common substrate.

a. Motivation to Combine Samoilov and Murthy

182. In my opinion, it would have been obvious to a person of ordinary skill in the art to combine the teachings of Samoilov with the semiconductor structure of Murthy. As I explained above, Murthy teaches a semiconductor structure that includes a substrate with a P-well 524 and an N-well 1224. EX1011-Murthy, Fig.

12, 13:50-53, 14:10-12, 23:21-54, 23:5-20. Samoilov teaches PMOS and NMOS transistors that are formed on n-type and p-type substrates, respectively. Combining these references would have yielded a CMOS semiconductor structure comprising PMOS and NMOS transistors, taught by Samoilov, formed on corresponding N-well and P-well regions, as described in Murthy, as illustrated below.



EX1005-Samoilov, Fig. 2F and EX1011-Murthy, Fig. 12 (combined).

A POSITA would have been motivated to combine these teachings as illustrated above with a reasonable expectation of success for the following reasons.

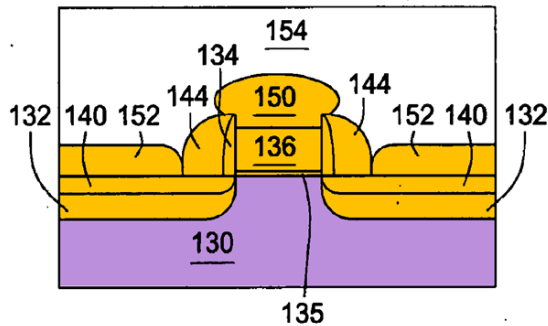
183. Samoilov itself teaches that its NMOS and PMOS transistors can be used together in “CMOS” (complementary MOS) technology. EX1005-Samoilov,

¶¶[0038]-[0039]. CMOS refers to integrated circuits that include both NMOS and PMOS transistors on a common substrate. This was the dominant technology in digital electronics by the mid-2000s. *See, e.g.*, EX1009-Plummer, 12-13, 50-51, Figs. 1-11, 2-2. A person of ordinary skill in the art would have understood that implementing Samoilov’s transistors in CMOS would yield established advantages: faster switching speed, lower power consumption, greater noise immunity, increased integration density, and enhanced compatibility with standard digital electronic components. *See, e.g.*, EX1010-Quirk, 200 (identifying CMOS technology as the “most popular” semiconductor manufacturing process). By 2006, CMOS had become the de facto standard in commercial semiconductor products. Accordingly, a person of ordinary skill in the art would have recognized the clear benefits of applying Samoilov’s transistor structures in a CMOS context and would have been motivated to seek out prior art references like Murthy that disclose suitable CMOS-compatible substrates.

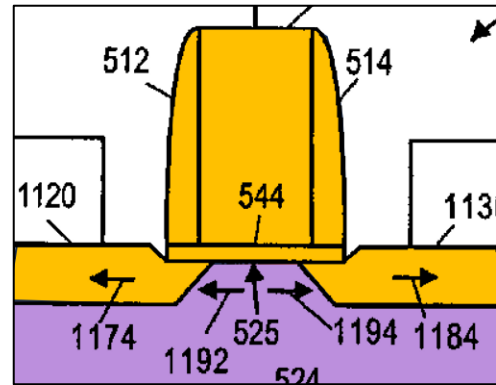
184. Figure 12 of Murthy shows a classic “twin well” CMOS structure, in which P-well and N-well regions are formed on an undoped or lightly doped substrate. Twin-well designs were widely known to enable the formation of NMOS and PMOS transistors on a single chip, offering better control of transistor characteristics during manufacturing than single-well designs. EX1009, 52; *see also supra* §III.A;

EX1010, 205-07, Figs. 9.8-9.9; EX1004-Koontz, ¶¶[0041], ¶¶[0053], Figs. 3, 4A-4N; EX1011-Murthy, 3:14-4:6, Fig. 4; EX1012-Kim, ¶¶[0054], Figs. 2-29; EX1013-Kook, ¶¶[0022]-[0023], Figs. 1-11. Therefore, a person of ordinary skill in the art would have been motivated to implement Samoilov's NMOS and PMOS transistor structures using Murthy's twin well substrate in order to gain known advantages of CMOS and twin-well integration (e.g., improved control in manufacturing).

185. The combination of Samoilov and Murthy would have led to predictable results, as both references disclose structurally and functionally similar semiconductor devices formed using compatible transistors with gate electrodes and adjacent strained source/drain regions. EX1005-Samoilov, ¶¶[0009], [0027], [0029], [0037]-[0039], [0067]-[0068]; EX1011-Murthy, 23:21-54, 23:5-20, Fig. 12. Moreover, both references describe using silicon-germanium or silicon-carbon layers to tailor the stress within the channel region and improve device performance. EX1005-Samoilov, ¶¶[0030], [0032], [0034]; EX1011-Murthy, 2:31-45, 21:55-65, 23:40-54. Thus, both references teach highly compatible device structures and process flows that a POSITA would readily integrate.



Samoilov, Fig. 2F



Murthy, Fig. 12 (excerpted)

186. A person of ordinary skill in the art would have had a reasonable success in applying Murthy’s teachings to those of Samoilov. By 2006, it was routine to generalize processing steps or structural features across NMOS and PMOS devices in CMOS technologies. For example, Orlowski confirms that “[e]xtending the depicted processing sequence to encompass the case of two types of SISD structures [(i.e., CMOS circuits comprising NMOS and PMOS transistors)] would be obvious to one skilled in the art....” EX1006-Orlowski, 4:1-10; *accord id.*, 7:40-47. Murthy discloses a twin-well CMOS substrate, and Samoilov discloses transistor fabrication using such wells. Therefore, a POSITA would have applied Murthy’s teachings of a twin-well substrate to Samoilov’s NMOS and PMOS fabrication in the same manner described in Murthy itself—with confidence in compatibility and predictable results. EX1005-Samoilov, Abstract, ¶¶[0003], [0010], [0022]-[0025]; EX1011-Murthy, 23:21-54, 23:5-20, Fig. 12.

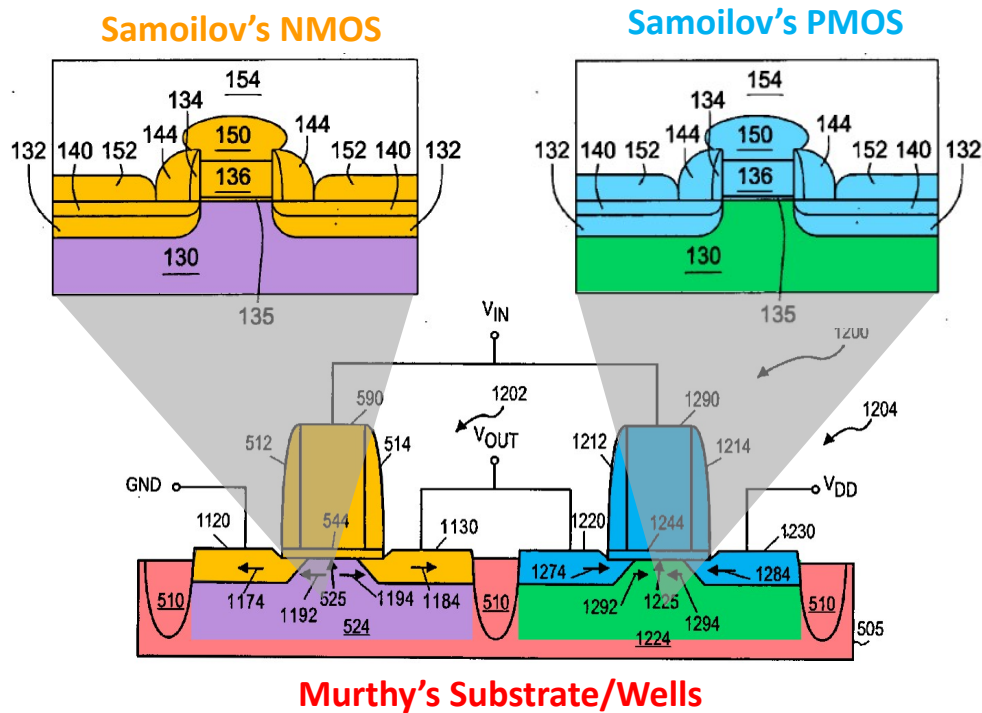
187. A person of ordinary skill in the art would have reasonably expected to integrate Samoilov's strained-layer transistors into the well-defined CMOS architecture of Murthy without undue experimentation. Although Samoilov does not explicitly refer to "well regions," its PMOS and NMOS transistors are described as being formed in p-type and n-type regions of a substrate, which a POSITA would recognize as functionally equivalent to P-well and N-well regions used in CMOS fabrication. In fact, adapting transistor-level innovations like Samoilov's graded SiGe or SiC layers into standard well-based processes was a routine and predictable design choice circa the priority date of the '822 patent, particularly to improve channel strain and enhance carrier mobility. Given that Murthy provides a conventional dual-well layout, a POSITA would find it straightforward to apply Samoilov's process techniques within Murthy's framework, aligning Samoilov's PMOS structures with Murthy's N-well and NMOS structures with its P-well. This combination would have been motivated by the desire to enhance transistor performance while maintaining compatibility with established CMOS process flows.

2. Claim 1

a. Element [1Pre]: "A semiconductor structure"

188. To the extent the preamble is limiting, Samoilov in view of Murthy teaches a semiconductor structure (e.g., strained-channel CMOS devices). As I

explained above (*see* Section XI.D.1), a POSITA would have been motivated to combine the teachings of Samoilov and Murthy as illustrated below.



EX1005-Samoilov, Fig. 2F and EX1011-Murthy, Fig. 12 (combined)

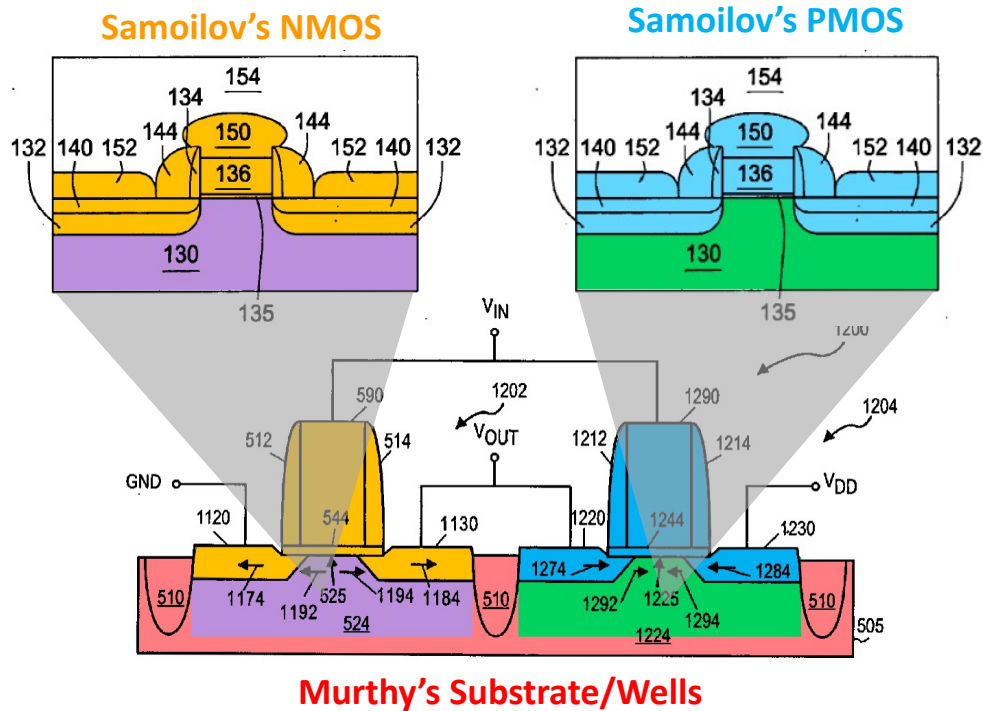
As shown above, the semiconductor structure comprising PMOS (blue) and NMOS (orange) transistors, taught by Samoilov, formed on corresponding N-well (green) and P-well (purple) regions, as described in Murthy.

an N-well 1224 that has an n-type conductivity. EX1011-Murthy, 23:27-39 Accordingly, P-well 524 of Murthy corresponds to the first well of claim 1 and N-well 1224 corresponds to the second well of claim 1. Additionally, and alternatively, these teachings equally satisfy the challenged claims when the conductivity types are reversed, i.e., when the “first conductivity type” is n-type and the “second conductivity type” is p-type, since the claim language permits such symmetry.

c. Element [1B]: “a first MOS transistor of the first conductivity type on the second well, comprising:”

191. Samoilov in view of Murthy renders obvious “a first MOS transistor of the first conductivity type on the second well.”

192. An illustrative representation of the combined teachings of Samoilov and Murthy is shown below.



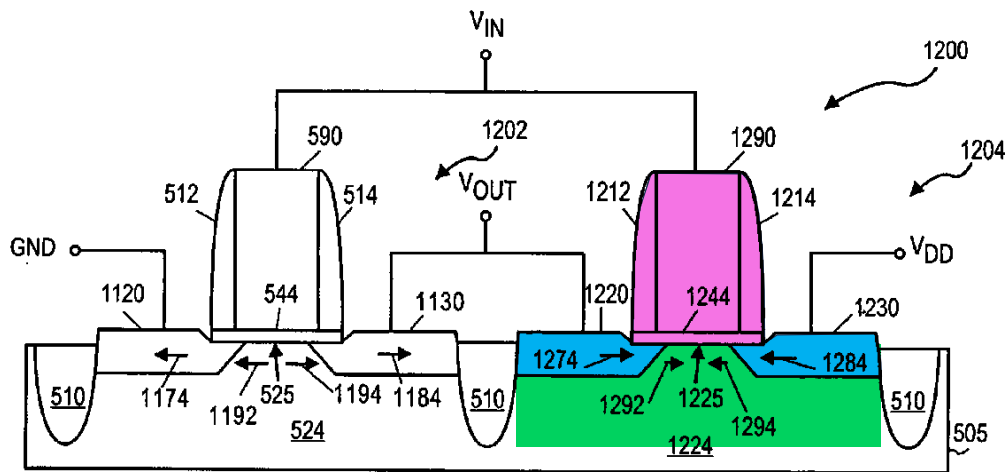
EX1005-Samoilov, Fig. 2F and EX1011-Murthy, Fig. 12 (combined)

As shown above, the combined structure includes a Samoilov's PMOS transistor on Murthy's N-well 1224 and Samoilov's NMOS transistor on Murthy's P-well 524. EX1011-Murthy, 23:23-39. As explained for Limitation [1A], N-well 1224 of Murthy corresponds to the second well of claim 1. Accordingly, Samoilov's PMOS transistor corresponds to the first MOS transistor of claim 1.

193. The Samoilov-Murthy combination equally satisfies the challenged claims regardless of which conductivity type is designated "first" or "second". For example, if the "first conductivity type" is n-type and the "second conductivity type" is p-type, then the first MOS transistor of the Samoilov-Murthy combination would

gate oxide layer 135, gate 136, off-set spacer 134, and/or spacer 144, individually or collectively, constitute a “gate structure” as claimed.

196. In the combined Samoilov-Murthy semiconductor structure, Samoilov’s gate structure identified above would have been located on Murthy’s N-well 1224. Indeed, referring to Figure 12 below, Murthy itself discloses a gate structure (magenta) of a similar PMOS transistor (blue) on N-well 1224 (green). EX1011-Murthy, 23:32-39.



EX1011-Murthy, Fig. 12

197. The Samoilov-Murthy combination equally satisfies the challenged claims when the conductivity types are reversed. That is, when the “first conductivity type” is n-type and the “second conductivity type” is p-type, Samoilov discloses an NMOS transistor including the above-described gate structure.

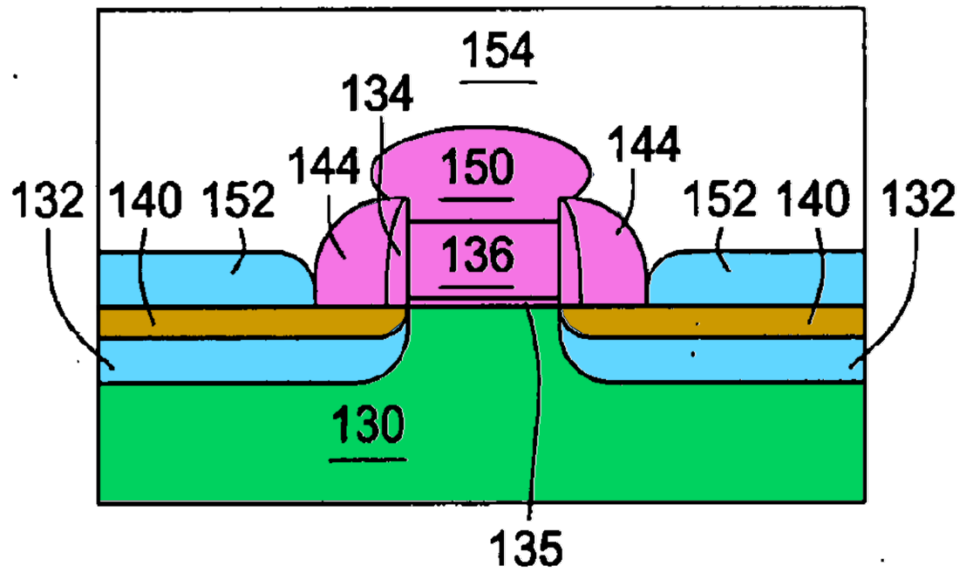
EX1005-Samoilov ¶¶[0009], [0027], [0029], [0038]-[0039], [0067]-[0068], Fig. 2F;
see also Element [7B].

- e. **Element [1D]: “a first MOS transistor ... comprising:
... a first strained layer of the first conductivity type in
a first opening in the second well beside the first gate
structure, wherein a difference between a lattice
parameter of a portion of the first strained layer near
a bottom of the first opening and a lattice parameter of
the substrate is smaller than a difference between a
lattice parameter of a portion of the first strained layer
apart from the bottom of the first opening and the
lattice parameter of the substrate”**

198. Samoilov in view of Murthy discloses “a first strained layer of the first conductivity type in a first opening in the second well beside the first gate structure, wherein a difference between a lattice parameter of a portion of the first strained layer near a bottom of the first opening and a lattice parameter of the substrate is smaller than a difference between a lattice parameter of a portion of the first strained layer apart from the bottom of the first opening and the lattice parameter of the substrate.”

199. I will first address the portion of Element [1D] reciting “a first strained layer of the first conductivity type in a first opening in the second well beside the first gate structure.”

200. Figure 2F of Samoilov is reproduced below.

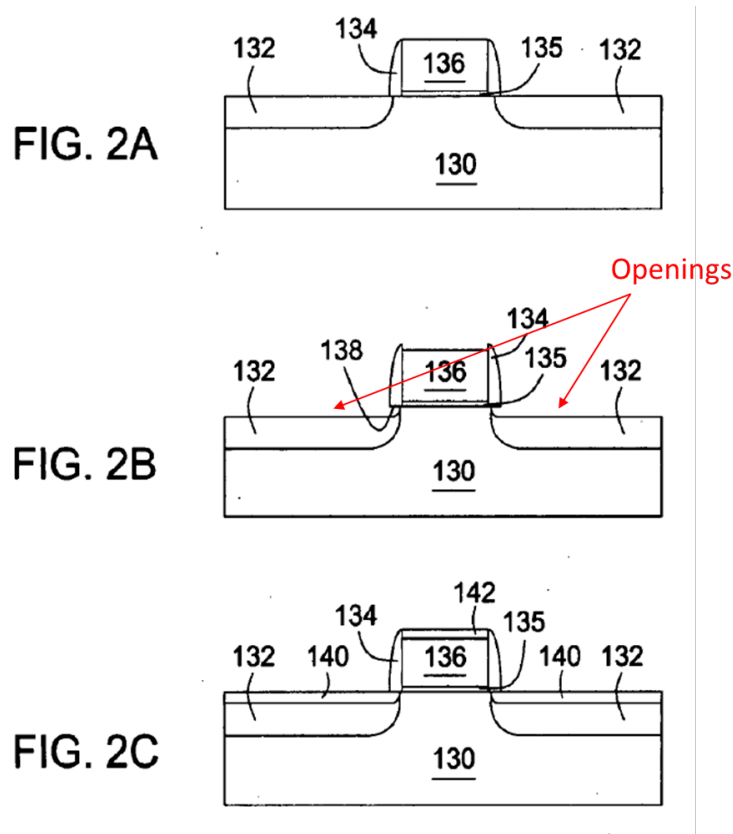


EX1005-Samoilov, Fig. 2F (annotated)

As shown above, Samoilov discloses a PMOS transistor (blue) (i.e., a “first MOS transistor”) with silicon-containing layers 140 (brown) (i.e., a “first strained layer”) of the first conductivity type (e.g., p-type) in a first opening in the second well (e.g., n-type substrate 130, which in the combined semiconductor structure taught by Samoilov and Murthy corresponds to Murthy’s n-well 1224) beside the first gate structure (magenta). EX1005-Samoilov, Fig. 2F, ¶¶[0005], [0009], [0021], [0026], [0039].

201. Samoilov teaches that, for a PMOS transistor, silicon-containing layers 140 are formed using silicon-germanium and are doped with p-type dopants (i.e., dopants of the “first conductivity type”). EX1005-Samoilov, ¶¶[0032], [0067]; *see also id.*, ¶¶[0009], [0024], [0030]-[0033], [0072], [0074]. For example, as shown in

Figures 2A through 2C of Samoilov below, during fabrication of the PMOS transistor, silicon-containing layers 140 are formed in openings beside the gate structure. EX1005-Samoilov, Figs. 2A-2C (annotated); *see also id.*, ¶¶[0029]-[0030].



EX1005-Samoilov, Figs. 2A-2C (annotated)

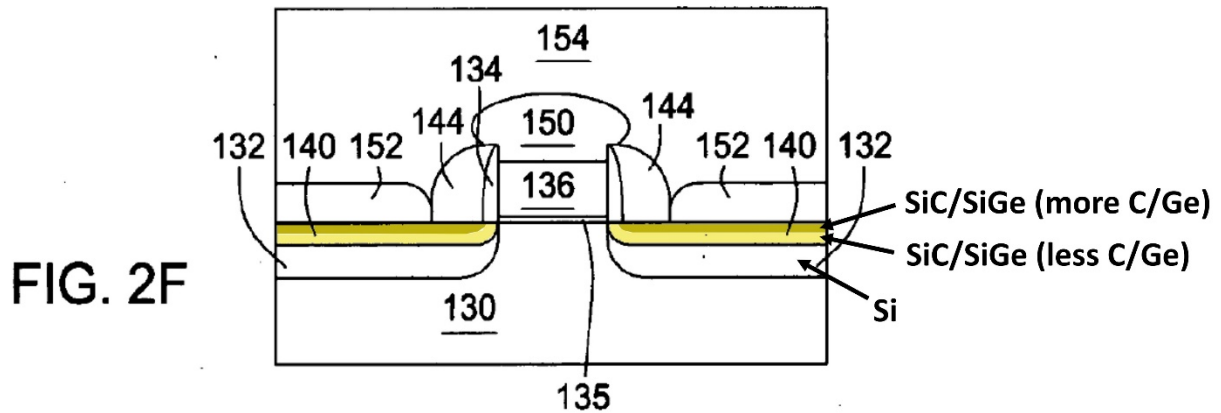
202. Next, I will address the portion of Element [1D] reciting that “a difference between a lattice parameter of a portion of the first strained layer near a bottom of the first opening and a lattice parameter of the substrate is smaller than a

difference between a lattice parameter of a portion of the first strained layer apart from the bottom of the first opening and the lattice parameter of the substrate.”

203. For example, Samoilov discloses that silicon-containing layers 140 can include multiple sub-layers with non-uniform lattice parameters, e.g., the sub-layers are “deposited in varying order to form graded elemental concentrations of silicon-containing layer 140.” EX1005-Samoilov, ¶¶[0030], [0032], [0061], [0072], [0074], claims 1, 7, 11-13, 19, 27, 47, 49, 64. For example, Samoilov teaches that a first silicon-germanium sub-layer near the bottom of silicon-containing layers 140 with a “germanium concentration in a range from about 15 at % to about 25 at %” and a second silicon-germanium sub-layer apart from the bottom of silicon-containing layers 140 with a “germanium concentration in a range from about 25 at % to about 35 at %.” *Id.*, ¶[0030]; *see also id.*, ¶[0072], claims 7, 11-13.¹

204. Samoilov’s use of a non-uniform lattice parameter is illustrated in Figure 2F of Samoilov below.

¹ Although this example describes two layers, silicon-containing layer 140 may contain more than two layers. EX1005-Samoilov, ¶¶[0016]-[0017], ¶[0030], ¶¶[0060]-[0061].

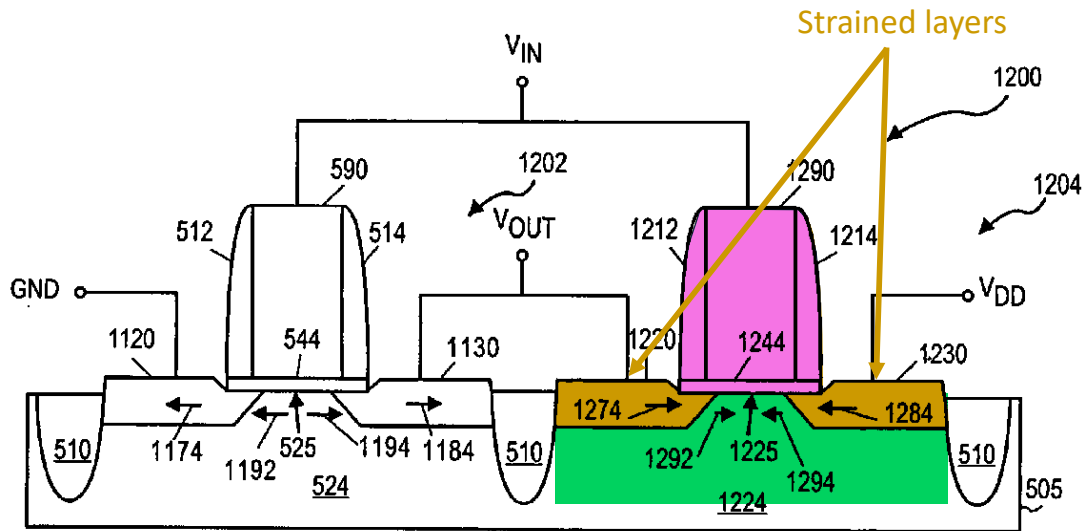


EX1005-Samoilov, Fig. 2F (annotated)

205. As I explained above for Ground 1 (*see* Section XI.A.1.e), a person of ordinary skill in the art would have understood the lattice parameter at the bottom of silicon-containing layer 140 (where the concentration of germanium or carbon is lower) more closely matches the lattice parameter of the substrate than does the rest of silicon-containing layer 140.

206. In the combined Samoilov-Murthy semiconductor structure, the strained layer 140 of Samoilov is located on P-well 1224 as taught by Murthy. Indeed, as shown in Figure 12 below, Murthy depicts an example of a similar PMOS transistor (blue) with junctions 1220 and 1230 (brown) (which “cause compressive strains 1274 and 1284”) on N-well 1224 (green) beside the gate structure (magenta). EX1011-Murthy, 2:40-55 (“junctions 1220 and 1230 may be formed of a material

having a lattice spacing larger than a lattice spacing of substrate 505” such as “SiGe”).



EX1011-Murthy, Fig. 12

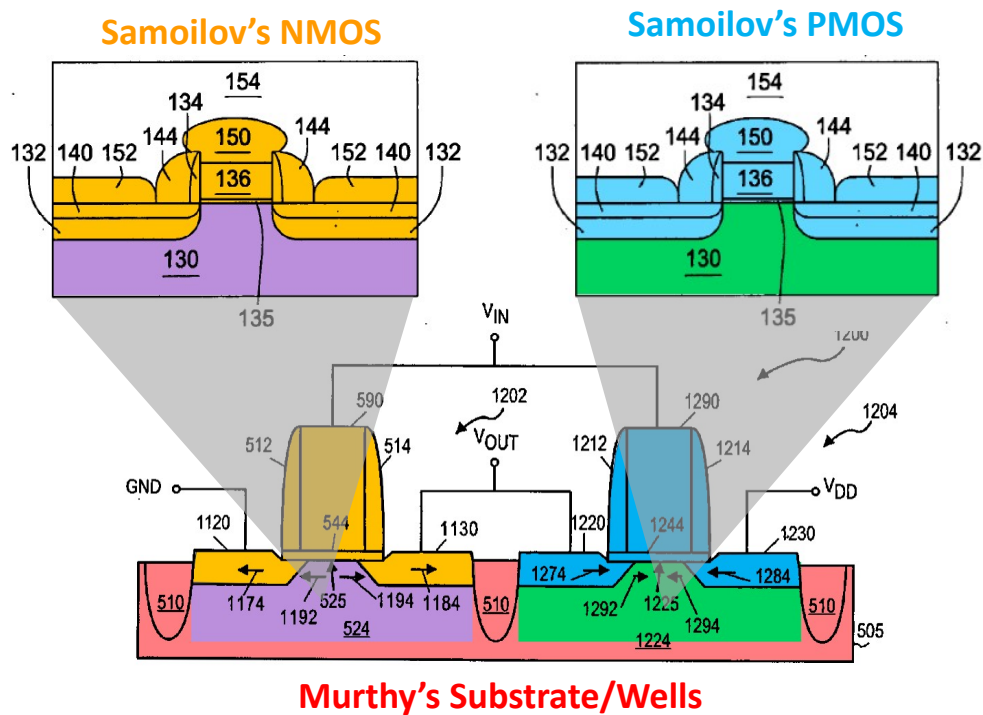
207. The Samoilov-Murthy combination equally satisfies the challenged claims when the conductivity types are reversed. Specifically, Samoilov’s NMOS transistor also includes the above-described silicon-containing layer 140. EX1005-Samoilov, ¶¶[0009], [0030]-[0033], [0067], Fig. 2F. For NMOS transistors, Samoilov teaches that silicon-containing layers 140 are formed using a silicon-carbon (rather than silicon-germanium) and similarly have a non-uniform (e.g., graded) lattice parameter. For example, Samoilov discloses a first silicon-carbon sub-layer closer to the bottom of silicon-containing layers 140 with a “carbon concentration of about 1.25[%]”, and a second sub-layer apart from the bottom of

silicon-containing layers 140 with a “carbon concentration of about 1.75[%]....” *Id.*, ¶[0074]; *see also id.*, claims 19, 27, 47.

f. Element [1E]: “a second MOS transistor of the second conductivity type on the first well”

208. Samoilov in view of Murthy discloses “a second MOS transistor of the second conductivity type [(e.g., n-type)] on the first well.”

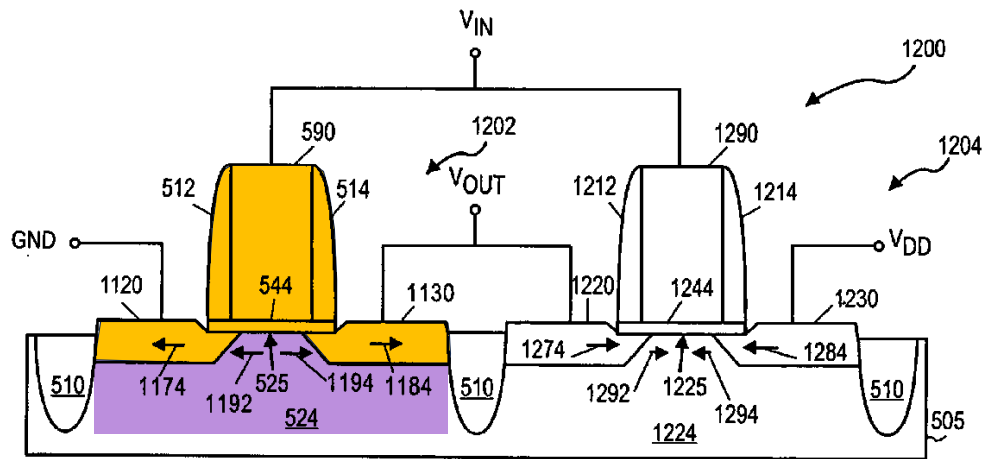
209. An illustrative representation of the combined teachings of Samoilov and Murthy is shown below.



EX1005-Samoilov, Fig. 2F and EX1011-Murthy, Fig. 12 (combined)

As shown above, the combined structure includes Samoilov's NMOS transistor (orange) on Murthy's P-well 524 (purple). *See* EX1011-Murthy, 23:23-39. As I

previously explained for Limitation [1A], Murthy's P-well 524 corresponds to the first well of claim 1. Accordingly, Samoilov's NMOS transistor corresponds to the second MOS transistor of claim 1. In fact, as illustrated in Figure 12 below, Murthy itself depicts an embodiment of a similar NMOS transistor (orange) on P-well 524 (purple).



EX1011-Murthy, Fig. 12

210. The Samoilov-Murthy combination equally satisfies the challenged claims when the conductivity types are reversed. That is, when the “first conductivity type” is n-type and the “second conductivity type” is p-type, the second MOS transistor of the Samoilov-Murthy combination would have corresponded to an PMOS transistor on Samoilov's N-well 1224 (*see* Element [1B], Section XI.C.1.c.iii).

3. **Claim 2: “The semiconductor structure of claim 1, wherein the lattice parameter of the first strained layer has a gradient distribution”**

211. Claim 2 depends from claim 1, which, as I explained above, is obvious over Samoilov in view of Murthy. *Supra* §XI.D.2.

212. Samoilov discloses that the concentration of germanium relative to silicon in the first strained layer has a gradient distribution. EX1005-Samoilov, ¶¶[0030] (“Multiple SiGe-containing layers containing varying amount of elements may be stacked to form silicon-containing layer 140 with a graded elemental concentration.”), [0032] (“Multiple layers containing Si, SiGe, SiC or SiGeC may be deposited in varying order to form graded elemental concentrations of silicon-containing layer 140.”), [0044] (“The germanium concentration may be graded within the SiGe film, preferably graded with a higher germanium concentration in the lower portion of the SiGe film than in the upper portion of the SiGe film.”). As I explained above for Ground 1 (*see* Section XI.A.2), person of ordinary skill in the art would have understood that a gradient distribution in the germanium concentration results in a gradient distribution in the lattice parameter.

4. **Claim 3: “The semiconductor structure of claim 1, wherein the first conductivity type is P-type, and the lattice parameter of a portion of the first strained layer near the bottom of the first opening is smaller than the lattice parameter of a portion of the first strained layer apart from the bottom of the first opening”**

213. Claim 3 depends from claim 1, which, as I explained above, is obvious over Samoilov in view of Murthy. *Supra* §XI.D.2. Samoilov further discloses that when the first conductivity type is p-type, the lattice parameter of a portion of the first strained layer (e.g., silicon-containing layers 140) near the bottom of the first opening is smaller than the lattice parameter of a portion of the first strained layer apart from the bottom of the first opening.

214. As I explained above in Section XI.D.2.e for Element [1D], Samoilov explains that “[m]ultiple SiGe-containing layers containing varying amount of elements may be stacked to form silicon-containing layer 140 with a graded elemental concentration.” EX1005-Samoilov, ¶[0030]; *see also id.*, ¶[0032]. When the “first conductivity type” is p-type, silicon-containing layers 140 are formed using silicon-germanium in which the amount of germanium relative to silicon becomes smaller closer to the bottom of silicon-containing layers 140. For instance, Samoilov teaches that “a first SiGe-layer may be deposited with a germanium concentration in a range from about 15 at % to about 25 at % and a second SiGe-layer may be deposited with a germanium concentration in a range from about 25 at % to about

35 at %.” *Id.*, ¶[0030]; *see also id.*, ¶[0072], claims 7, 11-13. In one PMOS example, a first silicon-germanium layer may have a germanium concentration of about 15 at %, and a second silicon-germanium layer above the first silicon-germanium layer may have a germanium concentration of about 30 at %. *Id.*, ¶[0072]. As I explained above for Ground 1 (*see* Section XI.A.3), a person of ordinary skill in the art would have understood that the lattice parameter in silicon germanium becomes smaller with decreasing germanium concentration and is thus smaller closer to the bottom of silicon-containing layers 140.

5. **Claim 4: “The semiconductor structure of claim 3, wherein the first strained layer comprises SiGe”**

215. The Samoilov-Murthy combination satisfies claim 4 for the reasons in Section XI.D.4 (Claim 3) and XI.D.2.e (Element [1D]). *See also* EX1005-Samoilov, ¶[0067] (“SiGe may be deposited in a recessed area to form a PMOS component.”).

6. **Claim 5: “The semiconductor structure of claim 1, wherein the first conductivity type is N-type, and the lattice parameter of a portion of the first strained layer near the bottom of the first opening is larger than the lattice parameter of a portion of the first strained layer apart from the bottom of the first opening”**

216. Claim 5 depends from claim 1, which, as I explained above, is obvious over Samoilov in view of Murthy. *Supra* §XI.D.2. Samoilov further discloses that when the “first conductivity” type is n-type, the lattice parameter of a portion of the

first strained layer (e.g., silicon-containing layers 140) near the bottom of the first opening is larger than the lattice parameter of a portion of the first strained layer apart from the bottom of the first opening.

217. As I explained above in section XI.A.1.e for Element [1D], Samoilov explains that “[m]ultiple SiGe-containing layers containing varying amount of elements may be stacked to form silicon-containing layer 140 with a graded elemental concentration.” EX1005-Samoilov, ¶[0030]; *see also id.*, ¶[0032]. When the “first conductivity type” is n-type, silicon-containing layers 140 are formed using silicon-carbon in which the amount of carbon relative to silicon becomes smaller closer to the bottom of silicon-containing layers 140. In one NMOS example, for instance, a first silicon-carbon layer may have a carbon concentration of about 1.25 at %, and a second silicon-carbon layer above the first silicon-carbon layer may have a carbon concentration of about 1.75 at %. *Id.*, ¶[0074]; *see also id.*, claims 19, 27, 47. As I explained above for Ground 1 (*see* Section XI.A.5), a person of ordinary skill in the art would have understood that the lattice parameter in silicon-carbon becomes larger with decreasing carbon concentration and is thus larger closer to the bottom of silicon-containing layers 140.

7. **Claim 6: “The semiconductor structure of claim 5, wherein the first strained layer comprises SiC”**

218. The Samoilov-Murthy combination satisfies claim 6 for the reasons in Section VI.D.5 (Claim 5) and XI.D.2.e (Element [1D]). *See also* EX1005-Samoilov, ¶[0067] (“SiC may be deposited in a recessed area to form a NMOS component.”).

8. **Claim 7**

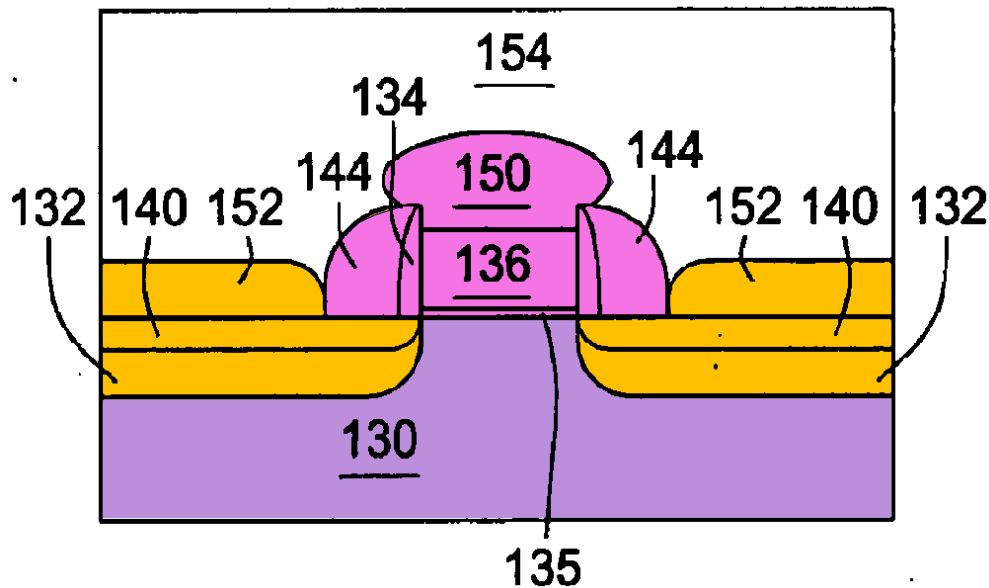
a. **Element [7Pre]: “The semiconductor structure of claim 1”**

219. Claim 7 depends from claim 1, which, as I explained above, the Samoilov-Murthy combination satisfies. *Supra* §XI.D.2.

b. **Element [7A]: “the second MOS transistor comprises: a second gate structure on the first well”**

220. Samoilov in view of Murthy discloses “the second MOS transistor comprises: a second gate structure on the first well.”

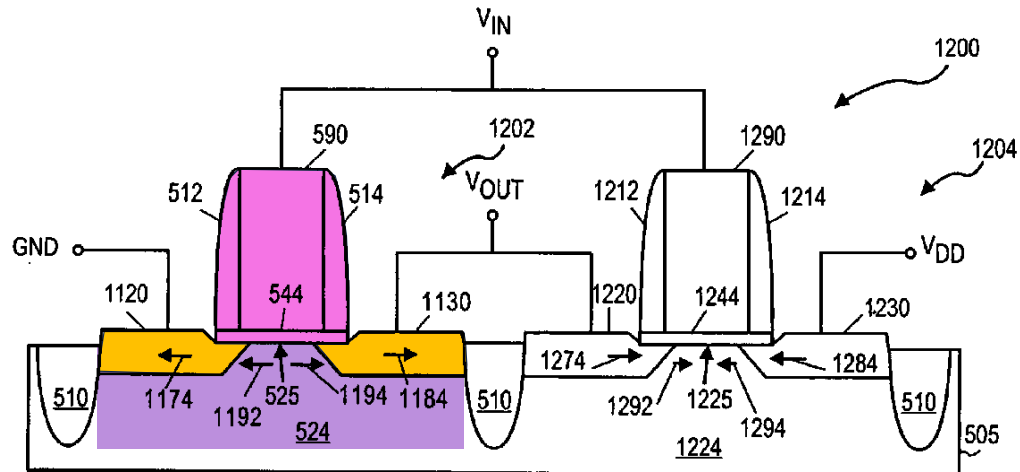
221. Figure 2F of Samoilov is reproduced below.



EX1005-Samoilov, Fig. 2F (annotated).

As shown above, Samoilov discloses an NMOS transistor (orange) (which as I explained above corresponds to the second MOS transistor) having a gate oxide layer 135, gate 136, off-set spacer 134, and/or spacer 144 (magenta). EX1005-Samoilov, Fig. 2F, ¶¶[0027], [0029]. The gate oxide layer 135, gate 136, off-set spacer 134, and/or spacer 144, individually or collectively, constitute a “gate structure” as claimed.

222. In the combined Samoilov-Murthy semiconductor structure, Samoilov’s gate structure identified above would have been located on Murthy’s P-well 524. Indeed, Murthy itself discloses a gate structure (magenta) of a similar NMOS transistor (orange) on P-well 524 (purple). EX1011-Murthy, Fig. 12.

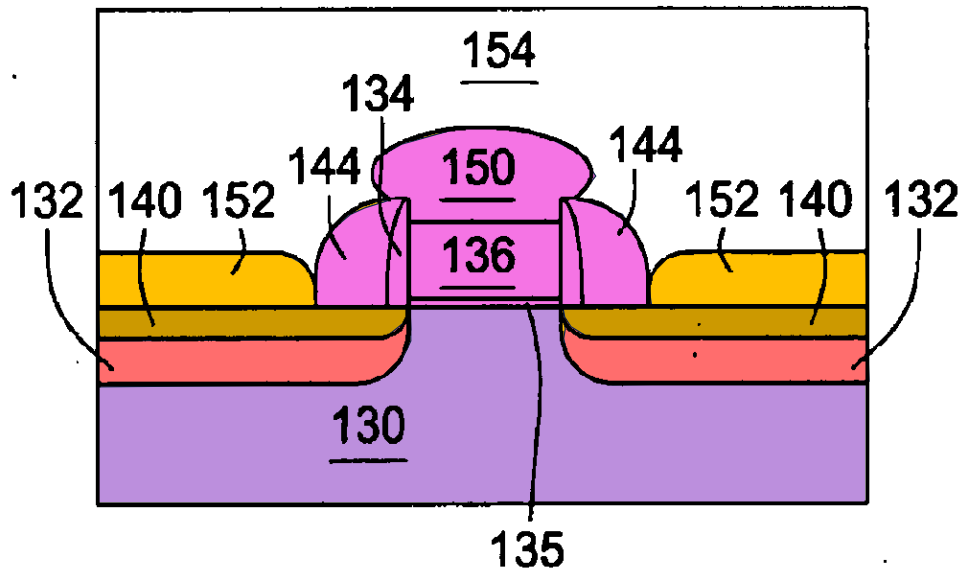


EX1011-Murthy, Fig. 12 (annotated).

223. The Samoilov-Murthy combination equally satisfies the challenged claims when the conductivity types are reversed. That is, when the “first conductivity type” is n-type and the “second conductivity type” is p-type Samoilov discloses a PMOS transistor including the above-described gate structure. *See* Element [1C].

- c. **Element [7B]: “the second MOS transistor comprises: ... a source/drain region of the second conductivity type in the first well beside the second gate structure”**

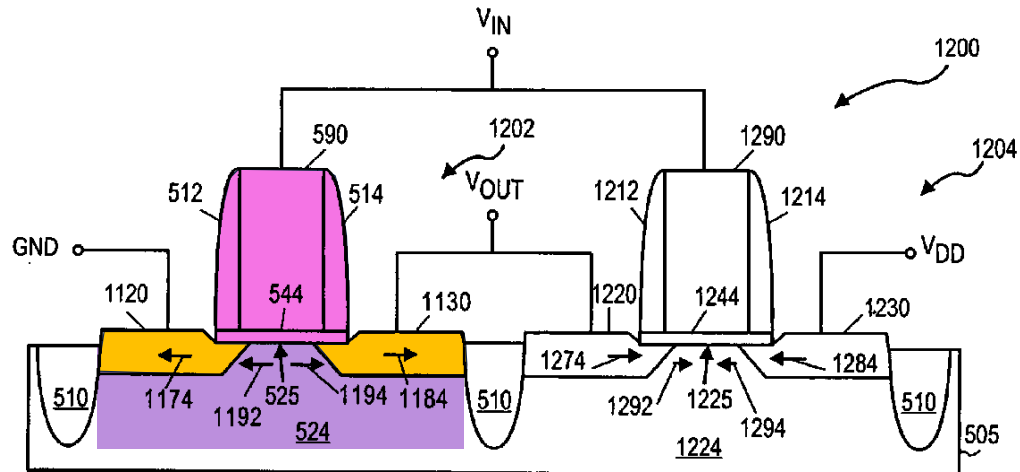
224. Figure 2F of Samoilov is reproduced below.



EX1005-Samoilov, Fig. 2F (annotated).

As shown in above, Samoilov discloses an NMOS transistor (orange) (which as I explained above corresponds to the second MOS transistor) comprising source/drain layers 132 (red) of the second conductivity type (e.g., n-type) beside the second gate structure (magenta). EX1005-Samoilov, Fig. 2F, ¶¶[0005], [0009], [0026]-[0027], [0029], [0039]. A person of ordinary skill in the art would have understood that NMOS transistors are arranged in a p-type region of a substrate.

225. In the combined Samoilov-Murthy semiconductor structure, the source/drain layers 132 would have been located on Murthy's P-well 524. Indeed, Murthy itself discloses a source/drain regions of a similar NMOS transistor (orange) on P-well 524 (purple).



EX1011-Murthy, Fig. 12 (annotated)

226. The Samoilov-Murthy combination equally satisfies the challenged claims when the conductivity types are reversed. That is, when the “first conductivity type” is n-type and the “second conductivity type” is p-type, Samoilov discloses a PMOS transistor including the above-described source/drain regions.

EX1005-Samoilov, ¶¶[0005], [0009], [0026]-[0027], [0029], [0039], Fig. 2F.

9. Claim 9

a. **Element [9Pre]: “The semiconductor structure of claim 1”**

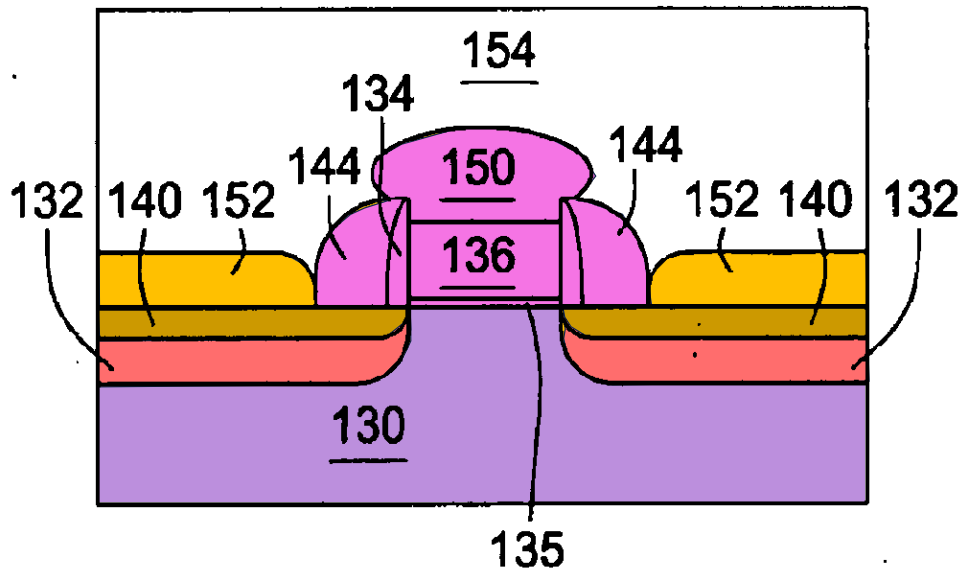
227. Claim 9 depends from claim 1, which, as I explained above, the Samoilov-Murthy combination satisfies. *Supra* §XI.D.2.

b. Element [9A]: “the second MOS transistor comprises: a second gate structure on the first well”

228. Element [9A] recites the same subject matter as Element [7A], which I addressed above. Namely, Element [9A] recites that “the second MOS transistor comprises: a second gate structure on the first well,” which is identical to Element [7A]. As such, my analysis above regarding Element [7A] (Section XI.D.8.b) equally applies here. Therefore, the Samoilov-Murthy Combination discloses this limitation.

c. Element [9B]: “the second MOS transistor comprises: ... a source/drain region of the second conductivity type around and under a second opening in the first well beside the second gate structure”

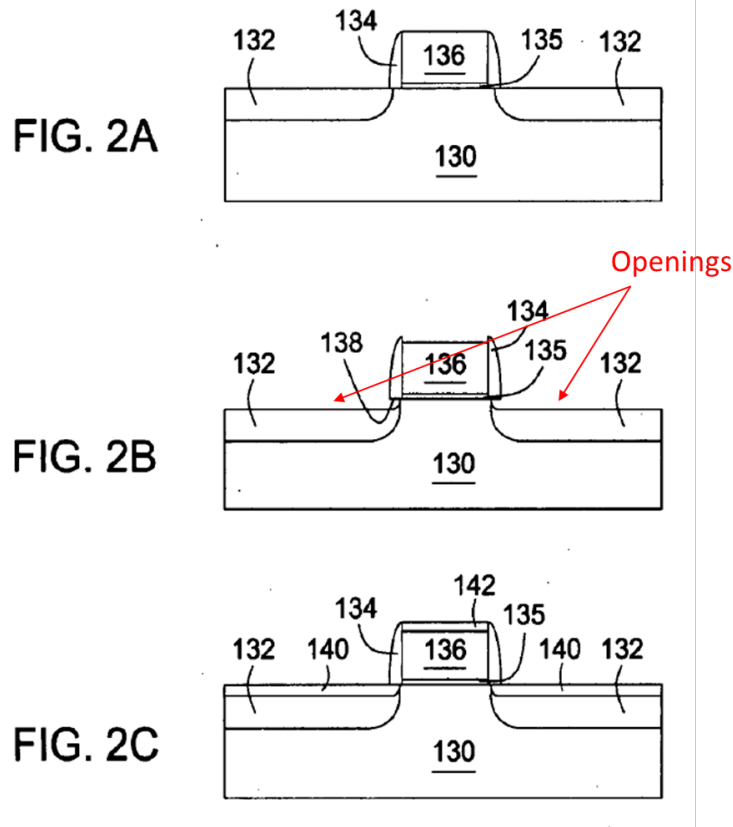
229. As I explained above for Element [7B], Samoilov discloses source/drain layers 132 (red) (source/drain regions) of the second conductivity type (e.g., n-type) beside the second gate structure (magenta). Figure 2F of Samoilov is reproduced below.



EX1005-Samoilov, Fig. 2F (annotated)

As shown above, source/drain layers 132 extend around (e.g., to the right/left of) and under (e.g., below) the opening containing silicon-containing layers 140 (i.e., a second opening in the first well), as claimed. EX1005-Samoilov, Fig. 2F (annotated); *see also id.*, ¶¶[0005], [0009], [0026]-[0027], [0029], [0039].

230. As shown in Figures 2A through 2C of Samoilov below, source/drain layers 132 extend around and under openings that are formed beside the gate structure during the NMOS transistor fabrication (Figure 2B) that are subsequently filled by silicon-containing layers 140 (Figure 2C). EX1005-Samoilov, Figs. 2A-2C (annotated); *see also id.*, ¶¶[0029]-[0030].



EX1005-Samoilov, Figs. 2A-2C (annotated)

231. In the combined Samoilov-Murthy semiconductor structure, the source/drain region would have been located on a P-well 524 as taught in Murthy.

232. The Samoilov-Murthy combination equally satisfies the challenged claims when the conductivity types are reversed. That is, when the “first conductivity type” is n-type and the “second conductivity type” is p-type, Samoilov’s PMOS transistor also includes the above-described source/drain regions. See ¶¶[0005], [0009], [0026]-[0027], [0029], [0039], Fig. 2F.

10. Claim 11

- a. Element [11Pre]: “The semiconductor structure of claim 1”**

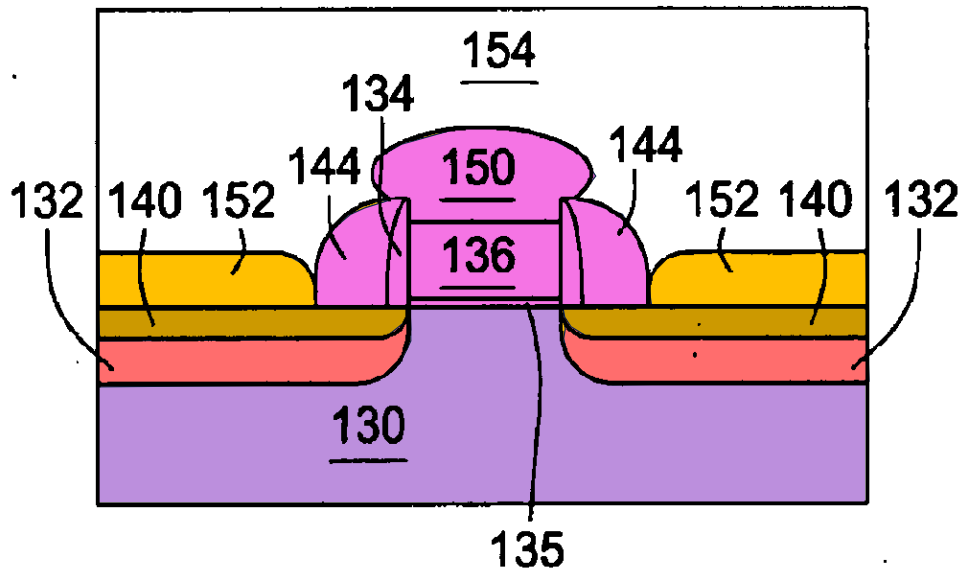
233. Claim 11 depends from claim 1, which, as I explained above, the Samoilov-Murthy combination satisfies. *Supra* §XI.D.2.

- b. Element [11A]: “the second MOS transistor comprises: a second gate structure on the first well”**

234. Element [11A] recites the same subject matter as Element [7A], which I addressed above. Namely, Element [11A] recites that “the second MOS transistor comprises: a second gate structure on the first well,” which is identical to Element [7A]. As such, my analysis above regarding Element [7A] (Section XI.D.8.b) equally applies here. Therefore, the Samoilov-Murthy Combination discloses this limitation.

- c. Element [11B]: “the second MOS transistor comprises: ... a second strained layer of the second conductivity type in a second opening in the first well beside the second gate structure”**

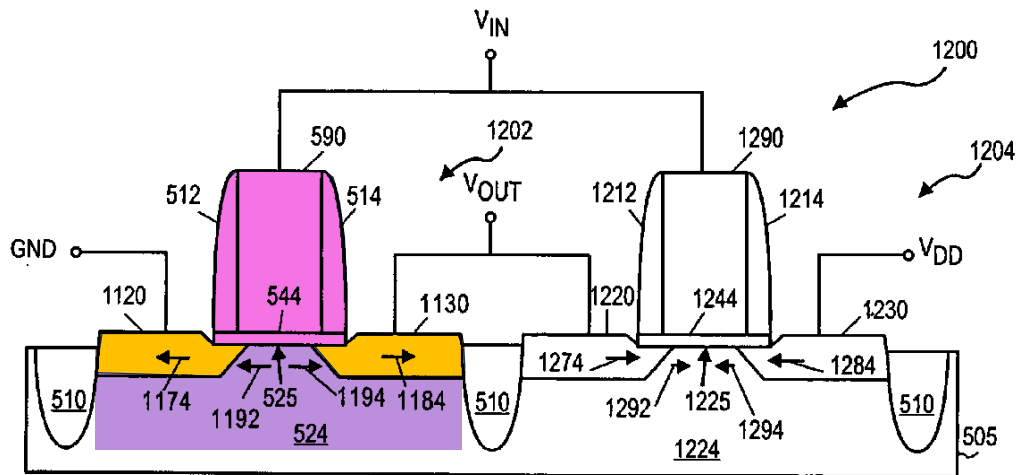
235. Figure 2F of Samoilov is reproduced below.



EX1005-Samoilov, Fig. 2F (annotated).

As shown above, Samoilov discloses an NMOS transistor (orange) (which as I explained above corresponds to the second MOS transistor) comprising silicon-containing layers 140 (brown) of the second conductivity type (e.g., n-type) in a second opening in the first well (e.g., p-type substrate 130). In the combined Samoilov-Murthy structure, this first well corresponds to Murthy's p-well 524. The silicon-containing layers 140 are positioned beside the second gate structure (magenta), consistent with the claim language. EX1005-Samoilov, Fig. 2F, ¶¶[0005], [0009], [0026]-[0027], [0029], [0039]. A person of ordinary skill in the art would have recognized that NMOS transistors are formed in a p-type region of a substrate.

236. In the combined Samoilov-Murthy semiconductor structure, the silicon-containing layers 140 (brown) would therefore be located on Murthy's P-well 524. Murthy itself discloses a strained layers of a similar NMOS transistor (orange) formed on P-well 524 (purple), as illustrated below.



EX1011-Murthy, Fig. 12 (annotated)

237. The Samoilov-Murthy combination also satisfies the challenged claims when the conductivity types are reversed. That is, when the “first conductivity type” is n-type and the “second conductivity type” is p-type, Samoilov discloses a PMOS transistor including a corresponding strained layer. EX1005-Samoilov, ¶¶[0005], [0009], [0026]-[0027], [0029], [0039], Fig. 2F.

11. Claim 12

- a. Element [12Pre]: “The semiconductor structure of claim 11”**

238. Claim 12 depends from claim 11, which, as I explained above, the Samoilov-Murthy combination satisfies. *Supra* §XI.D.10.

- b. Element [12A]: “a difference between a lattice parameter of a portion of the second strained layer near a bottom of the second opening and the lattice parameter of the substrate is smaller than a difference between a lattice parameter of a portion of the second strained layer apart from the bottom of the second opening and the lattice parameter of the substrate”**

239. Limitation [12A] requires that the second strained layer described in Limitation [11B] (*see* Section XI.D.10.b) exhibits the same directional lattice-parameter gradient specified in Limitation [1D], i.e., the lattice parameter of the strained layer changes along the vertical direction such that the mismatch with the substrate is smaller near the bottom of the recess and larger toward the top. As explained above for Limitation [1D] (*see* Section XI.D.2.e), the Samoilov-Murthy combination teaches vertically graded strain-inducing layers that meet this requirement. Murthy discloses that the strain in its epitaxial SiC or SiGe layers can be controlled by varying the composition during growth, and Samoilov similarly employs compositionally graded silicon-containing layers. A person of ordinary skill in the art would have understood that this same vertical compositional control

applies to both the compressive SiGe stressors of the PMOS device and the tensile SiC stressors of the NMOS device, producing the required relationship in which the lattice parameter near the bottom of the recess more closely matches the substrate while the lattice parameter farther from the bottom differs more. Accordingly, the Samoilov–Murthy combination discloses the claimed lattice-parameter gradient for both the first and second strained layers, as required by Limitation [12A].

- c. **Element [12B]: “when the first conductivity type is P-type and the second conductivity type is N-type, the lattice parameter of a portion of the first strained layer near the bottom of the first opening is smaller than the lattice parameter of a portion of the first strained layer apart from the bottom of the first opening, but the lattice parameter of a portion of the second strained layer near the bottom of the second opening is larger than the lattice parameter of a portion of the second strained layer apart from the bottom of the second opening”**

240. Element [12B] recites the same subject matter as Claims 3 and 5, which I addressed above. Namely, the portion of Element [12B] reciting that “the lattice parameter of a portion of the first strained layer near the bottom of the first opening is smaller than the lattice parameter of a portion of the first strained layer apart from the bottom of the first opening,” as applied to a PMOS transistor, is identical to Claim 3. Similarly, the portion of Element [12B] reciting that “the lattice parameter of a portion of the second strained layer near the bottom of the second opening is

smaller than the lattice parameter of a portion of the second strained layer apart from the bottom of the second opening,” as applied to an NMOS transistors, is substantively the same as Claim 5. The only difference is the change between the word “first” and “second,” but as I explained above for Element [1D] (Section XI.D.2.e) and Element [11B] (Section XI.D.10.c), the claims are symmetric to polarity. As such, my analysis above regarding Claim 3 (Section XI.D.4) and Claim 5 (Section XI.D.6) equally applies here. Therefore, Koontz discloses this limitation.

- d. **Element [12C]: “when the first conductivity type is N-type and the second conductivity type is P-type, the lattice parameter of a portion of the first strained layer near the bottom of the first opening is larger than the lattice parameter of a portion of the first strained layer apart from the bottom of the first opening, but the lattice parameter of a portion of the second strained layer near the bottom of the second opening is smaller than the lattice parameter of a portion of the second strained layer apart from the bottom of the second opening”**

241. Element [12C] recites the same subject matter as Claims 3 and 5, which I addressed above. Namely, the portion of Element [12C] reciting that “the lattice parameter of a portion of the first strained layer near the bottom of the first opening is larger than the lattice parameter of a portion of the first strained layer apart from the bottom of the first opening,” as applied to an NMOS transistors, is identical to Claim 5. Similarly, the portion of Element [12C] reciting that “the lattice parameter

of a portion of the first strained layer near the bottom of the first opening is smaller than the lattice parameter of a portion of the first strained layer apart from the bottom of the first opening,” as applied to a PMOS transistor, is substantively the same as Claim 3. The only difference is the change between the word “first” and “second,” but as I explained above for Element [1D] (Section XI.D.2.e) and Element [11B] (Section XI.D.10.c), the claims are symmetric to polarity. As such, my analysis above regarding Claim 3 (Section XI.D.4) and Claim 5 (Section XI.D.6) equally applies here. Therefore, Koontz discloses this limitation.

12. Claim 13: “The semiconductor structure of claim 12, wherein the lattice parameter of the second strained layer has a gradient distribution”

242. Claim 13 depends from claim 12, which, as I explained above, the Samoilov-Murthy combination satisfies. *Supra* §XI.D.11.

243. Claim 13 requires that the second strained layer described in Limitation [11B] (*see* Section XI.D.10.b) exhibits a lattice-parameter gradient distribution—i.e., a continuous variation in lattice parameter along the vertical direction such that the mismatch with the substrate is smaller near the bottom of the recess and larger toward the top. As previously explained with respect to Limitation [1D] (*see* Section XI.D.2.e) and Claim 2 (*see* Section XI.D.3), the Samoilov-Murthy combination teaches precisely this configuration. Murthy discloses compositionally graded

epitaxial SiC or SiGe layers whose composition varies during growth to control strain, and Samoilov likewise employs silicon-containing layers with vertical compositional variation. A person of ordinary skill in the art would have understood that these combined teachings yield a graded lattice parameter within the second strained layer. Accordingly, the Samoilov–Murthy combination satisfies the claimed requirement that the second strained layer have a gradient lattice-parameter distribution, as recited in Claim 13.

E. GROUND 3B: Claims 8, 10, and 14 Are Invalid as Obvious Over Samoilov In View of Murthy and Sridhar

1. Claim 8

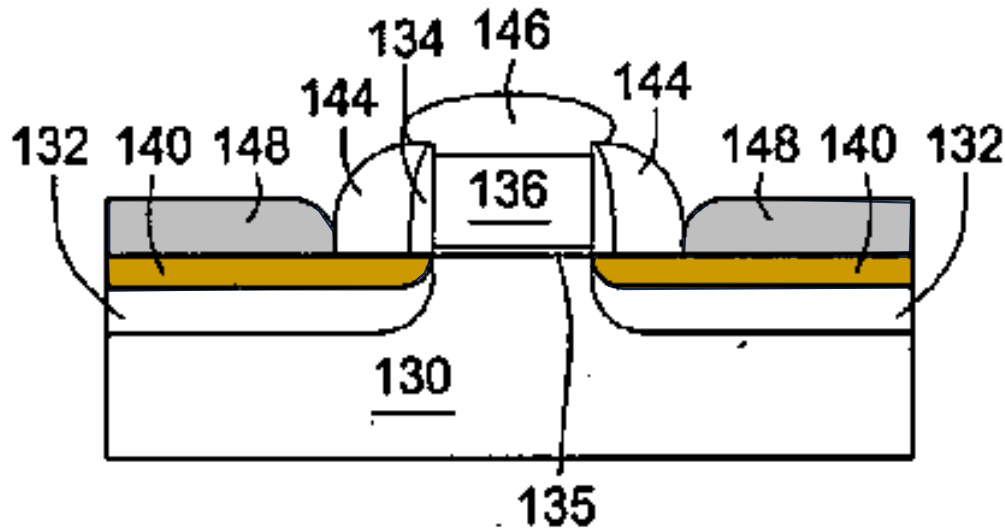
a. Element [8Pre]: “The semiconductor structure of claim 7”

244. Claim 8 depends from claim 7, which, as I explained above, the Samoilov-Murthy combination satisfies. *Supra* §XI.D.8.

b. Element [8A]: “a silicon layer on the first strained layer”

I. Samoilov-Murthy

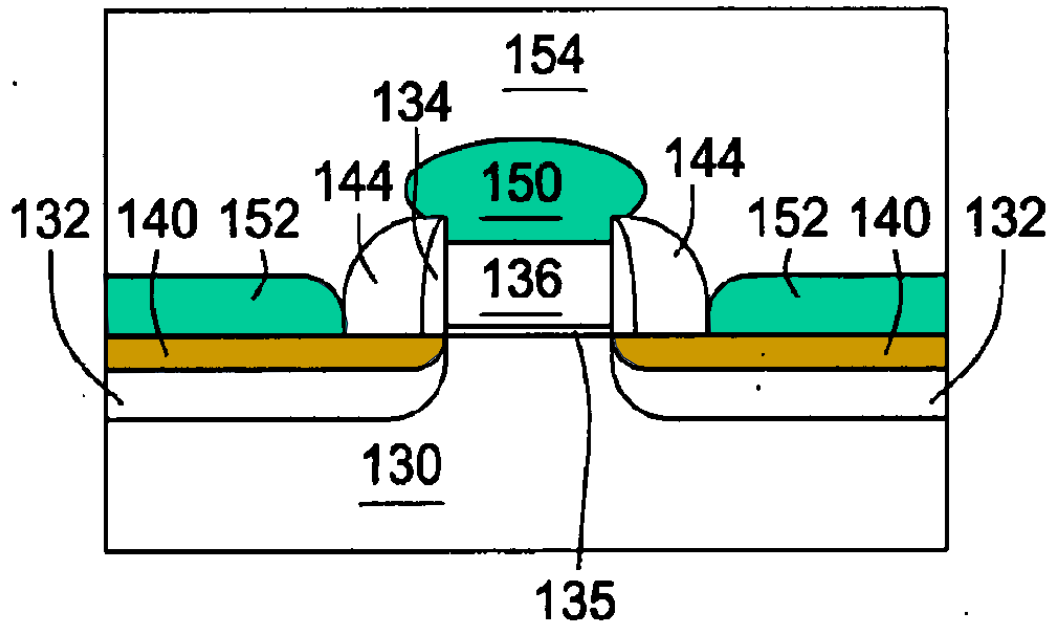
245. Figure 2E of Samoilov is reproduced below.



EX1005-Samoilov (annotated)

As shown above, Samoilov discloses a silicon-containing layer 148 (gray) “containing little or no germanium or carbon” on the silicon-containing layers 140 (brown). EX1005-Samoilov, Fig. 2E, [0035]-[0036].

246. Specifically, Samoilov discloses that “[s]ilicon-containing layer 148 is deposited on layer 140 (e.g., doped-SiGe).” EX1005-Samoilov, ¶[0035]; *see also id.*, Fig. 2E. After forming the silicon containing layer, “a metal layer 154 is deposited over the features and the device is annealed.” *Id.*, ¶[0037]. As a result, the silicon-containing layer 148 is “converted to metal silicide” layer 152. *Id.*; *see also id.*, Fig. 2F.



EX1005-Samoilov, Fig. 2F (annotated)

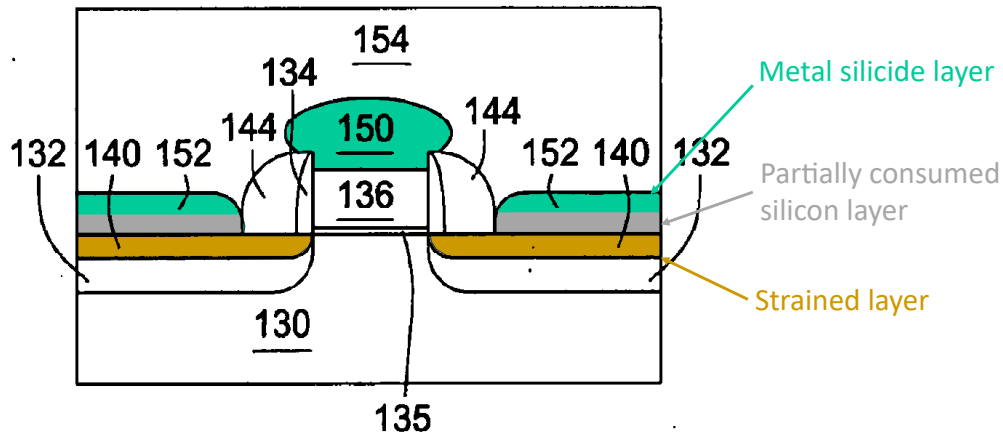
ii. Sridhar

247. As I explained above in Section XI.B.1.b.ii for Ground 1B, Sridhar teaches techniques for forming a silicide layer result in a residual silicon layer remaining on the strained layer after formation of the silicide layer is complete.

iii. Motivation to combine

248. For reasons similar to those discussed above for the Koontz-Sridhar combination in Ground 1B (*see* Section XI.B.1.b.iii), a person of ordinary skill in the art would have found it obvious to combine Sridhar's silicide-forming techniques with the semiconductor structure of Samoilov and Murthy. The result of the combination is illustrated below: a silicon capping layer, as taught by Samoilov, is

partially consumed during silicide formation, as taught by Sridhar, leaving behind a residual silicon layer (gray) between the strained layer (brown) and the silicide layer (teal).



EX1005-Samoilov, Fig. 2F (annotations illustrate the results of applying Sridhar’s teachings).

249. Like Koontz, Samoilov teaches forming a silicide layer on the source/drain regions of a MOS transistor, and Sridhar discloses a specific process for forming such a silicide layer with enhanced properties. Thus, the same rationale that would have motivated a person of ordinary skill in the art to apply Sridhar’s teachings to Koontz’s teachings applies equally to Samoilov and Murthy.

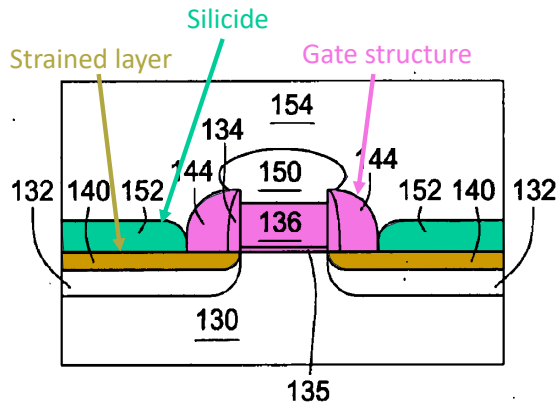
250. Samoilov explicitly teaches that its silicide layer should be formed by first depositing a silicon layer “contain[s] little or no germanium or carbon.” EX1005-Samoilov, ¶¶[0035]-[0037]. This express guidance would lead a person of

ordinary skill in the art to seek out additional references that detail how to deposit the silicon layer and form the resulting silicide. Sridhar provides precisely such guidance—describing the benefits of forming a controlled silicon cap that is only partially consumed during silicide formation. Those benefits, previously explained in Ground 1B, include better silicide uniformity, reduced agglomeration, and improved electrical contact. Thus, a POSITA would have been motivated to apply Sridhar’s silicide process to the Samoilov-Murthy structure to realize these known advantages.

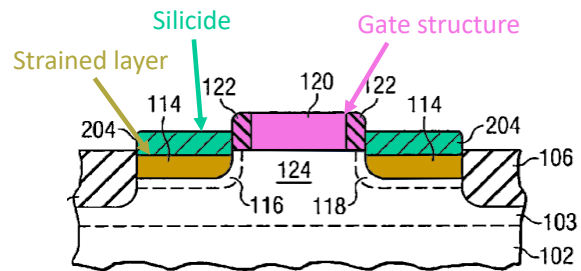
251. The combination of Samoilov, Murthy, and Sridhar would have led to predictable and synergistic results, as all three references describe compatible semiconductor structures and fabrication techniques. For instance, Samoilov teaches forming PMOS and NMOS transistors where “a silicon-containing material such as [silicon germanium or silicon-carbon] may be deposited in a recessed area” of the transistor. EX1005-Samoilov, ¶[0067]; *see also* EX1011-Murthy, 2:31-46, Figs. 1-3. Sridhar likewise teaches forming NMOS and PMOS transistors that includes “forming a silicon-germanium layer in each of the source and drain regions.” EX1007-Sridhar, ¶[0004]; *see also id.*, ¶[0001], ¶[0010]. Sridhar emphasizes that its technique – forming a silicon layer over the strained layer, followed by silicidation – can be “dropped into” existing CMOS fabrication flows

like those used by Orlowski (and by extension, Samoilov and Murthy). *Id.*, ¶[0017]; *see also id.*, ¶[0005]. Additional parallels include:

- Both Samoilov and Sridhar disclose MOSFET devices with source/drain regions, gate structures and silicide contacts. EX1005-Samoilov, ¶¶[0009], [0027], [0029], [0037]-[0039], [0067]-[0068], Fig. 2F; EX1007-Sridhar, ¶¶[0010]-[0013], Fig. 1D.
- Both disclose using strained SiGe or SiC in the source/drain regions to improve carrier mobility. EX1005-Samoilov, ¶¶[0030], [0032], [0034]; EX1007-Sridhar, ¶¶[0003], [0014].
- Both describe forming silicide on the strained material to reduce contact resistance. EX1005-Samoilov, ¶¶[0009], [0037], [0067]; EX1007-Sridhar, ¶¶[0004], [0014]-[0017], Figs. 1C-1D.
- As shown in the annotated figures below, the physical and functional similarities between Samoilov and Sridhar are substantial.



Samoilov, Fig. 2F



Sridhar, Fig. 1D

Therefore, the Samoilov-Murthy-Sridhar combination would have been straightforward and yielded predictable by uniting references with shared objectives and mutually reinforcing techniques.

252. A person of ordinary skill in the art would have had a reasonable expectation of success in applying Sridhar's teachings to the Samoilov-Murthy structure. As explained in Ground 1B (*see* Section XI.B.1.b.iii), Sridhar explicitly states that its process is designed to be compatible with conventional CMOS fabrication flows, including those disclosed in Samoilov and Murthy.

253. Moreover, Sridhar's silicon-capping and silicide-formation techniques would enhance the Samoilov-Murthy device in the same manner that they enhance Orłowski's. Samoilov already discloses a strained SiGe regions layer with a silicide layer formed on top. EX1005-Samoilov, ¶¶[0009], [0037], [0067], Fig. 2F. Sridhar

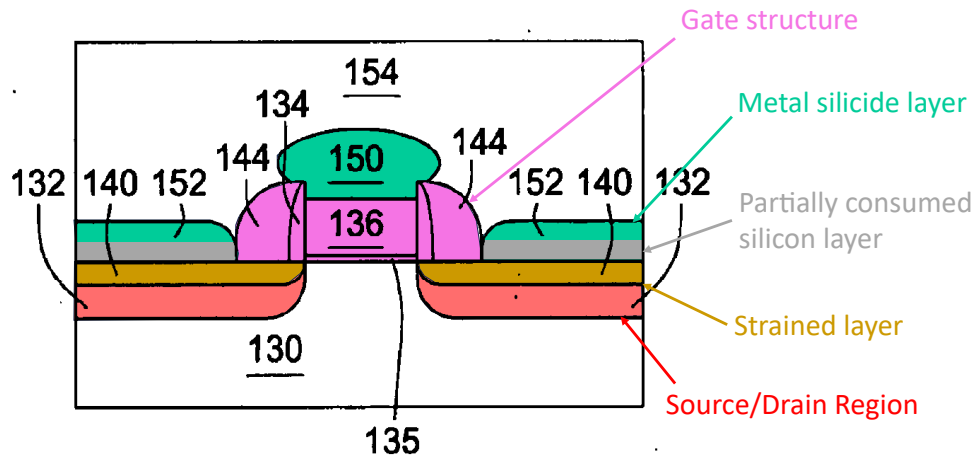
improves on that process by inserting a silicon layer that is only partially consumed during silicidation, thereby preserving stress and improving contact integrity. A POSITA would have seen this as a direct process enhancement to apply to Samoilov's strained S/D structure, without requiring inventive insight.

254. It would have been obvious to apply Sridhar's teachings to either or both of the PMOS and NMOS transistors in the Samoilov-Murthy structure, for the same reasons given in Ground 1B. *See* Section XI.B.1.b.iii.

c. Element [8B]: “a metal silicide layer on the silicon layer, the source/drain region and the first and the second gate structures”

255. As I explained above in Section XI.E.1.b for Element [8A], the combination of Samoilov, Murthy, and Sridhar teaches a metal silicide layer (e.g., Samoilov's silicide layers 152) on a silicon layer (e.g., Samoilov's silicon-containing layers 148, where the silicon-containing layers are only partially consumed during the silicide formation process, as taught by Sridhar).

256. Figure 2F of Samoilov is reproduced below.



EX1005-Samoilov, Fig. 2F (annotated)

As shown above, Samoilov further teaches that silicide layers 152 (teal) are on source/drain region 132 (red) and that a silicide layer 150 (teal) is on the gate structures (magenta). EX1005-Samoilov, Fig. 2F (annotated); *see also id.*, [0037].

2. Claim 10

257. Claim 10 recites the same limitations as claim 8, except it depends from claim 9 rather than claim 7. Thus, as I explained above, the Samoilov-Murthy-Sridhar combination satisfies claim 10 for the reasons I described in Sections XI.D.9 (Claim 9) and XI.E.1 (Claim 8).

3. Claim 14

a. **Element [14Pre]: “The semiconductor structure of claim 11”**

258. Claim 14 depends from claim 11, which, as I explained above, the Samoilov-Murthy combination satisfies. *Supra* §XI.D.10.

b. Element [14A]: “a silicon layer on the first strained layer and the second strained layer”

259. As I explained above in Sections XI.D.2.e and XI.D.10.c for Elements [1D] and [11B], Samoilov in view of Murthy discloses a first strained layer and a second strained layer. Moreover, as I explained above in Section XI.E.1.b for Element [8A], Samoilov in view of Murthy and Sridhar renders obvious the formation of a silicon layer on the strained layers.

c. Element [14B]: “a metal silicide layer on the silicon layer and the first and second gate structures”

260. Element [14B] recites the same subject matter as Element [8B], which I addressed above. Namely, Element [14B] recites that “a metal silicide layer on the silicon layer and the first and second gate structures,” which substantively the same as Element [8B]. The only difference is that Element [8B] additionally requires the metal silicide layer to be on the source/drain region. As such, my analysis above regarding Element [8B] (Section XI.B.1.c) equally applies here. Therefore, Samoilov in view of Murthy and Sridhar discloses this limitation.

XII. SECONDARY CONSIDERATIONS

261. As I explained in Section III.C, I understand that secondary considerations may support or rebut the obviousness of a claim. I am not aware of any secondary considerations that support that the claims of the '822 patent are

nonobvious. To the extent Patent Owner argues that secondary considerations are relevant here, I reserve the right to respond.

XIII. AVAILABILITY FOR CROSS-EXAMINATION

262. In signing this declaration, I recognize that the declaration will be filed as evidence in a contested case before the Patent Trial and Appeal Board of the United States Patent and Trademark Office. I also recognize that I may be subject to cross-examination in the case and that cross-examination will take place within the United States. If cross-examination is required of me, I will appear for cross-examination within the United States during the time allotted for cross-examination.

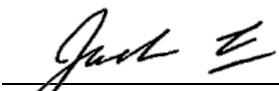
XIV. RIGHT TO SUPPLEMENT

263. I reserve the right to supplement my opinions in the future to respond to any arguments that Patent Owner raises and to take into account new information as it becomes available to me.

XV. JURAT

264. I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Dated: October 20, 2025



Jack Lee

APPENDIX A

Jack C. Lee
Professor Emeritus
Electrical and Computer Engineering Department
The University of Texas at Austin

Current Status

Professor Emeritus
Department of Electrical and Computer Engineering
The University of Texas at Austin

Research / teaching experience and expertise:

- Integrated circuits manufacturing
- Photovoltaic/solar cell technologies
- Alternative channel devices
- Dielectric and passivation processes
- Display technologies
- Semiconductor memory devices

Education

9/84 – 8/88 Ph.D., Electrical Engineering, University of California at Berkeley
9/80 – 12/81 M.S., Electrical Engineering, University of California at Los Angeles
9/76 – 6/80 B.S., Electrical Engineering (with highest honors),
University of California at Los Angeles

Professional Career

9/23 – present Professor Emeritus
Department of Electrical and Computer Engineering
The University of Texas at Austin
9/00 – 8/23 Cullen Trust for Higher Education Endowed Professorship in Engineering #4
Department of Electrical and Computer Engineering
The University of Texas at Austin
9/96 – 8/23 Professor, Department of Electrical and Computer Engineering
The University of Texas at Austin
9/92 – 8/96 Associate Professor, Department of Electrical and Computer Engineering
The University of Texas at Austin
9/88 – 8/92 Assistant Professor, Department of Electrical and Computer Engineering
The University of Texas at Austin
1/88 – 6/88 Lecturer, Electrical Engineering and Computer Science Department
University of California at Berkeley
6/79 – 8/84 Member of Technical Staff, High-Speed Bipolar Device Program
TRW Microelectronics Center, Redondo Beach, CA

Honors and Awards

IEEE Electron Devices Society Distinguished Lecturer, 2004 - 2016.
Fellow, The Institute of Electrical and Electronic Engineers (IEEE), 2002 “For contributions to the understanding and development of ultra-thin dielectrics and their application to silicon devices”
Gordon Lepley IV Endowed Memorial Teaching Award, ECE Department, The University of Texas at Austin, 2004

Cullen Trust For Higher Education Endowed Professorship in Engineering, 2000-present
 Dean's Fellow, College of Engineering, The University of Texas at Austin, 1999, 2003
 Lockheed Fort-Worth Division Award for Excellence in Engineering Teaching,
 College of Engineering, The University of Texas at Austin, 1996
 Award of Excellence, Halliburton Foundation, 1993
 Departmental Teaching Award, College of Engineering, The University of Texas at
 Austin, 1993
 SRC Inventor Recognition Award, Semiconductor Research Corporation, 1991
 Hughes Aircraft Company Endowed Faculty Fellowship in Engineering,
 The University of Texas at Austin, 1991- 2000
 Outstanding Engineering Teaching by an Assistant Professor, College of Engineering,
 The University of Texas at Austin, 1991
 Best Paper Award, SEMATECH Centers of Excellence Coordination Meeting, 1990.
 Dow Outstanding Young Faculty Award, American Society for Engineering Education,
 1990
 Engineering Research Initiation Award, Engineering Foundation of the United
 Engineering Trustees, 1989
 Best Paper Award, IEEE International Reliability Physics Symposium, 1988

Litigation Experience as Testifying Experts

The following is a list of cases in which I have provided expert testimony, including through a declaration, report or testimony at deposition or trial since 2016

- Longitude Flash Memory Solutions and IPValue Management v. SanDisk
 April 2025 –
 (Representing defendant, SanDisk)
- Marlin Semiconductor Limited v. TSMC
 April 2025 –
 (Representing defendant, TSMC)
- Advanced Integrated Circuit Process LLC v. Taiwan Semiconductor Mfg. Co. Ltd
 October 2024 –
 (Representing defendant, TSMC)
- Yangtze Memory Technologies v. Micron
 January 2024 –
 (Representing defendant, Micron)
- BeSang v. Micron
 March 2023 –
 (Representing defendant, Micron)
- The Trustees of Purdue University v. Wolfspeed, Inc.
 February 2022 – March 2025
 (Representing defendant, Wolfspeed)

- GlobalFoundries - IPR
March 2021 –
(Representing petitioner and filed an IPR declaration)
- HD Silicon Solutions LLC v. Microchip Technology Inc.
January 2021 – February 2025
(Representing defendant, Microchip Technology Inc.)
- Longitude Licensing Limited vs Western Digital
March 2023 – January 2024
(Representing defendant, Western Digital)
- Impinj, Inc. v. NXP USA, Inc.
September 2019 – July 2023
(Representing defendant, NXP USA, Inc.)
- Monterey Research, LLC v. Qualcomm Inc.
February 2020 – May 2022
(Representing defendant, Qualcomm)
- Bell Semiconductor, LLC v. Texas Instruments Incorporated
July 2020 – March 2021
(Representing defendant, Texas Instruments)
- Greenthread LLC v. Samsung
February 2020 – July 2020
(Representing plaintiff, Greenthread LLC)
- MLC Intellectual Property LLC vs. Micron Technology, Inc.,
June 2016 – January 2021
(Representing plaintiff, MLC Intellectual Property LLC)
- Hanwha v. LONGi Solar Technology
April 2019 – June 2020
(Representing defendant LONGi Solar Technology)
- Vista Peak Ventures, LLC v. Innolux Corp.
January 2019 – March 2019
(Representing IPR Petitioner, Innolux Corp.)
- Home Semiconductor Corp. v. Samsung
August 2018 – June 2020
(Representing plaintiff, Home Semiconductor Corp.)
- Mariner IC Inc. v. Asustek Computer Inc.

May 2018 – August 2019
(Representing plaintiff, Mariner IC Inc.)

- Godo Kaisha IP Bridge 1 v. OmniVision Technologies, Inc.
January 2018 – December 2018
(Representing defendant, OmniVision Technologies, Inc.)
- Macronix v. Toshiba
May 2017 – February 2018
(Representing defendant, Toshiba)
- University of Illinois v. Micron Technology
September 2009 – November 2017
(Representing plaintiff, Univ. of Illinois)
- Silicon Genesis v. Soitec
October 2016 – March 2017
(Representing plaintiff, Silicon Genesis)

Non-Litigation Consulting

- Applied Materials, Inc.
Teaching short courses on semiconductor physics, devices, design/layout, and fabrication technologies (2-3 courses per year).

Jack C. Lee is a Professor Emeritus of the Electrical and Computer Engineering Department. He held the Cullen Trust for Higher Education Endowed Professorship in Engineering # 4 at The University of Texas at Austin from 2000-2023. He received the B.S. and M.S. degrees in electrical engineering from University of California, Los Angeles, in 1980 and 1981, respectively; and the Ph.D. degree in electrical engineering from University of California, Berkeley, in 1988. From 1979 to 1984, he was a Member of Technical Staff at the TRW Microelectronics Center, CA, in the High-Speed Bipolar Device Program. He worked on bipolar device and circuit design, fabrication and testing. In 1988, he joined the faculty of The University of Texas at Austin. His current research interests include semiconductor devices including 3D structures such as FinFETs, fabrication processes, characterization and modeling, dielectric process, characterization and reliability, high-K gate dielectrics and electrode, semiconductor memory applications, alternative channel materials, display technologies and photovoltaic/solar cell technologies. Dr. Lee has over 40 years of experience in semiconductor technology and dielectric processing. He has published over 600 journal publications and conference

proceedings and 9 patents; and co-authored 8 book and book chapters. He has also been recognized with many teaching and research awards. Dr. Lee is a Fellow of IEEE and had been a Distinguished Lecturer for the IEEE Electron Devices Society.

Publications

Jack C. Lee

Refereed Journal Publications

1. J. Lee, K. Mayaram and C. Hu, "A Theoretical Study of Gate/Drain Offset in LDD MOSFET's," IEEE Electron Device Letters, vol. EDL-7, no. 3, p. 152 - 154, March 1986.
2. J. Lee, I-C Chen and C. Hu, "Comparison Between CVD and Thermal Oxide Dielectric Integrity," IEEE Electron Device Letters, vol. EDL-7, no. 9, p. 506 - 509, September 1986.
3. K. Mayaram, J. Lee and C. Hu, "A Model for the Electric Field in Lightly Doped Drain Structures," IEEE Transactions on Electron Devices, vol. ED-34, no.7, p. 1509 - 1518, July 1987.
4. J. Lee and C. Hu, "Polarity Asymmetry of Oxides Grown on Polycrystalline Silicon," IEEE Transactions on Electron Devices, vol. ED-35, no. 7, p. 1063 - 1070, July 1988.
5. J. Lee, C. Hegarty and C. Hu, "Electrical Characteristics of MOSFET's Using Low-Pressure Chemical Vapor Deposited Oxide," IEEE Electron Device Letters, vol. EDL-9, no. 7, p. 324 - 327, July 1988.
6. J. Lee, I-C Chen and C. Hu, "Modeling and Characterization of Gate Oxide Reliability," Special Issue of IEEE Transactions on Electron Devices on Reliability, Vol. ED-35, no. 12, p. 2268 - 2278, December 1988.
7. H. Hwang, W. Ting, D. L. Kwong, J. Lee, L. Buhrow and R. Bowling, "Electrical Characteristics of Reoxidized-nitrided CVD Oxide," Applied Physics Letters, 55(8), p. 755 - 756, 21 August, 1989.
8. R. Moazzami, J. Lee and C. Hu, "Temperature Acceleration of Time-Dependent Dielectric Breakdown," Special issue of IEEE Transactions on Electron Devices on Vacuum Microelectronic Devices, vol. ED-36, no. 11, p. 2462 - 2465, November 1989.
9. H. Hwang, W. Ting, D.L. Kwong, J. Lee, L. Buhrow and R.A. Bowling, "Effects of Dynamic Stressing on Nitrided and Reoxidized-Nitrided Chemical Vapor Deposited Gate Oxides," IEEE Electron Device Letters, vol. EDL-10, no. 12, p. 568 - 570, December 1989.
10. J. Lin, S. Banerjee, J. Lee, and C. Teng, "Soft Breakdown in Titanium-Silicided Shallow Source/Drain Junction," IEEE Electron Device Letters, vol. EDL-11, no. 5, p. 191 - 193, May 1990.
11. K. Park, S. Batra, J. Lin, S. Yoganathan, J. Lee, S. Banerjee, S. Sun, J. Yeargain, and G. Lux, "Anomalous Capacitance-Voltage Behavior Due to Dopant Segregation and

Carrier Trapping in Arsenic-Implanted Polysilicon and Polycide Gates," *Applied Physics Letters*, vol. 56, no. 23, p.2325 - 2327, June 4, 1990.

12. J. Lin, S. Banerjee, J. Lee, and C. Teng, "Anomalous Current-Voltage Behavior in Titanium-Silicided Source/Drain Junctions," *Journal of Applied Physics*, vol. 68, no. 3, p. 1082 - 1087, August 1, 1990.
13. H. Hwang, W. Ting, B. Maiti, D.L. Kwong and J. Lee, "Electrical Characteristics of Ultrathin Gate Dielectrics Prepared by Rapid Thermal Oxidation of Si in N₂O," *Applied Physics Letters*, vol. 57, no. 10, p. 1010 - 1011, Sept. 3, 1990.
14. S. Batra, K. Park, J. Lin, S. Yoganathan, J. Lee, S. Banerjee, S. Sun, J. Yeargain and G. Lux "Effects of Dopant Redistribution, Segregation and Carrier Trapping in As-Implanted MOS Gates," *IEEE Transactions on Electron Devices*, vol. 37, no. 11, p. 2322 - 2330, October, 1990.
15. S. Bhattacharya, S. Banerjee, J. Lee, A. Tasch and A. Chatterjee, "The Impact of Trench Isolation on Latch-up Immunity in Bulk, Non-epitaxial CMOS," *IEEE Electron Device Letters*, vol. EDL-12, no. 2, p. 77 - 79, February, 1991.
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17. W. Ting, P.C. Li, G. Q. Lo, J. Lee and D.L. Kwong, "Metal-Oxide Semiconductor Characteristics of Rapid Thermal Processed Chemical Vapor Deposited SiO₂ Gate Dielectrics," *Solid State Electronics*, vol. 34, no. 4, p 385 - 388, 1991.
18. W. Ting, H. Hwang, J. Lee and D.L. Kwong, "Growth Kinetics of Ultrathin SiO₂ Films Prepared by Rapid Thermal Oxidation of Si Substrates in N₂O," *Journal of Applied Physics*, vol. 70, no. 2, p. 1072 - 1074, July 15, 1991.
19. J. Lin, K. Park, S. Batra, S. Banerjee, J. Lee and G. Lux, "Enhancement of Boron Diffusion Through Gate Oxides in MOS Devices During Rapid Thermal Silicidation," *Applied Physics Letters*, vol. 58, no. 19, p. 2123 - 2125, May 1991.
20. H. Hwang, W. Ting, D. L. Kwong and J. Lee, "A Physical Model for Boron Penetration Through Oxynitride Gate Dielectric Prepared by Rapid Thermal Processing in N₂O," *Applied Physics Letters*, vol. 59, no. 13, p. 1581 - 1582, September 23, 1991.
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24. M. Hao and J. Lee, "Electrical Characteristics of Oxynitrides Grown on Textured Single-Crystal Silicon," Applied Physics Letters, vol. 60, no. 4, p. 445 - 447, January 27, 1992 .
25. S. Bhattacharya, S. Banerjee, J. Lee, A. Tasch and A. Chatterjee, "Parametric Study of Latchup-Immunity of Deep Trench-Isolated, Bulk, Non-epitaxial CMOS," IEEE Trans. Elec. Dev., vol. 39, no. 4, p. 921 - 931, April 1992.
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27. V. Chikarmane, C. Sudhama, J. Kim, J. Lee and A. Tasch, "Effects of Post-Deposition Annealing Ambient on the Electrical Characteristics and Phase Transformation Kinetics of Sputtered Lead Zirconate titanate (65/35) Thin Film Capacitors," Journal of Vacuum Science and Technology, vol. 10, no. 4, p. 1562 - 1568, July 1992.
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31. H. Hwang, M. Y. Hao, J. Lee, V. Mathews, P. Fazan and C. Dennison, "Furnace N₂O Oxidation Process for Submicron MOSFET Device Applications," Solid-State Electronics, vol. 36, p. 749 - 751, 1993.

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36. J. Lee, V. Chikarmane, C. Sudhama, and J. Kim, "Sputtered PZT Thin Films for Memory Applications," *Journal of Integrated Ferroelectrics*, vol. 3, 1993.
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39. M. Y. Hao, H. Hwang and J. Lee, "Memory Effects of Silicon-Implanted Oxides for EEPROM Applications," *Applied Physics Letters*, vol. 62, No. 13, p. 1530 - 1532, March 1993.
40. S. Batra, K. Picone, K. Park, S. Bhattacharya, S. Banerjee, J. Lee, M. Manning and C. Dennison, "Study of Lateral Non-Uniformity as a Function of Junction Depth in Ultra-Shallow Junctions and Its Effects on Leakage Behavior in As-Deposited Polycrystalline Si and Amorphous Si Diodes," *Solid-State Electronics* vol. 36, no. 7, p. 955 - 960, 1993.
41. J. Lee, C. Sudhama, J. Kim and R. Khamankar, (Invited Paper) "High Dielectric Constant Ferroelectric Thin Films for DRAM Applications", *Extended Abstracts of International Conf. on Solid State Devices and Materials*, p. 850 - 852, 1993.
42. W. M. Chen, S. K. Banerjee, and J. C. Lee, "Degradation mechanism and improvement of thermal stability of CoSi₂/polycrystalline Si layers," *Applied Physics Letters*, vol. 64, no. 12, p. 1505 - 1507, 1994.
43. W. M. Chen, J. Lin, S. K. Banerjee, and J. C. Lee, "Simultaneous Shallow-Junction Formation and Gate Doping p-channel Metal-Semiconductor-Oxide Field-Effect

Transistor Process Using Cobalt Silicide as a Diffusion/Doping Source," *Applied Physics Letters*, vol. 64, no. 3, p. 345 - 347, 1994.

44. M. Y. Hao, B. Maiti, and J. Lee, "Novel Process for Reliable Ultrathin Tunnel Dielectrics," *Appl. Phys. Lett.*, vol. 64, p. 2102 - 2104, April 1994.
45. B. Jiang, C. Sudhama, R. Khamankar, J. Kim and J. Lee, "Effects of Nonlinear Storage Capacitor on DRAM READ/WRITE," *IEEE Electron Device Letters*, vol. 15, no. 4, p.126 - 128, April 1994.
46. J. Kim, C. Sudhama, R. Khamankar, B. Jiang, J. Lee, P. Maniar, R. Moazzami, R. Jones and C. J. Mogab, "La Doped PZT Thin Films for Gigabit DRAM Technology," 1994 Symposium on VLSI Tech. Digest, p. 151 - 152, 1994.
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48. K. Lai, M. Y. Hao, C. Y. Hu, W. M. Chen, and J. Lee, "Effects of Surface Preparation on the Electrical and Reliability Properties of Ultrathin Thermal Oxide," *IEEE Electron Device Letters*, vol. ED-15, no. 11, p. 446 - 448, November, 1994.
49. M. Y. Hao, W. M. Chen, K. Lai, M. Gardner, J. Fulford, and J. Lee, "Correlation of Dielectric Breakdown with Hole Transport for Ultrathin Thermal Oxides and N₂O Oxynitrides," *Applied Physics Letters*, vol. 66, no. 9, p. 1126 - 1128, February 27, 1995.
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51. J. Lee, B. Jiang, R. Khamankar, and J. Kim, "Nonlinearity of Ferroelectric Capacitors on DRAM R/W Operations," *Integrated Ferroelectrics*, p. 319 - 328, 1995.
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6. Yao-Feng Chang, Burt Fowler, Ying-Chen Chen, Fei Zhou, Xiaohan Wu, Yen-Ting Chen, Yanzhen Wang, Fei Xue, and Jack C. Lee, "Resistive Switching Characteristics and Mechanisms in Silicon Oxide Memory Devices," *Nano Devices and Sensors*, p. 73-90, ISBN: 978-1-5015-0153-1, Published by De Gruyter publisher, (March 2016).
7. Y. H. Kim and J. Lee, "Hf-Based High-K Dielectrics, Process Development, Performance Characterization and Reliability," ISBN: 9781598290042, Morgan and Claypool Publishers (Jan. 2006).
8. K. Onishi and J. Lee, "High-*k* Transistor Characteristics" in the book entitled, "High *k* Gate Dielectrics" (Ed. Michel Houssa), ISBN:0-7503-0906-7, published by IOP Publishing Ltd (2004).

APPENDIX B

Appendix B: Materials Considered

No.	Description
EX1001	U.S. Patent No. 7,288,822 to Ting et al. (“’822 Patent”).
EX1002	Prosecution History of the ’822 Patent (“Prosecution History”).
EX1003	RESERVED
EX1004	U.S. Patent Appl. Pub. No. 2006/0134873 A1 to Koontz (“Koontz”).
EX1005	U.S. Patent Appl. Pub. No. 2005/0079692 A1 to Samoilov et al. (“Samoilov”).
EX1006	U.S. Patent No. 7,238,580 B2 to Orlowski et al. (“Orlowski”).
EX1007	U.S. Patent Appl. Pub. No. 2005/0090082 A1 to Sridhar et al. (“Sridhar”).
EX1008	S.M. Sze, <i>Physics of Semiconductor Devices</i> (2d ed. 1981) (excerpted).
EX1009	J.D. Plummer et al., <i>Silicon VLSI Technology: Fundamentals, Practice and Modeling</i> (2000) (excerpted).
EX1010	M. Quirk & J. Serda, <i>Semiconductor Manufacturing Technology</i> (2001) (excerpted).
EX1011	U.S. Patent No. 7,195,985 B2 to Murthy et al. (“Murthy”)
EX1012	U.S. Patent Appl. Pub. No. 2005/0266631 A1 to Kim et al.
EX1013	U.S. Patent Appl. Pub. No. 2007/0238236 A1 to Cook, Jr. et al.
EX1014	S.E. Thompson et al., “A Logic Nanotechnology Featuring Strained-Silicon,” <i>IEEE Electron Device Letters</i> , vol. 25. No. 4, pp. 191-93 (Apr. 2004).
EX1015	Y. Sun et al., <i>Physics of Strain Effects in Semiconductors and Metal-Oxide-Semiconductor Field-Effect Transistors</i> , <i>Journal of Applied Physics</i> , vol. 101, art. No. 104503 (22 pages) (May 2007).
EX1016	P. Bai et al., <i>A 65nm Logic Technology Featuring 35nm Gate Lengths, Enhanced Channel Strain, 8 Cu Interconnect Layers, Low-k ILD and 0.57 μm^2 SRAM Cell</i> , Technical Digest of the 2004

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Appendix B (Materials Considered)

No.	Description
	IEEE International Electron Devices Meeting, pp. 657-60 (Dec. 2004).
EX1017	U.S. Patent No. 6,949,482 B2 to Murthy et al. (“Murthy482”)
EX1018	H. Richter et al., <i>Defect Engineering in SiGe Heterostructures</i> , Proceedings of the 1996 CAS International Semiconductor Conference, pp. 41-50 (Oct. 1996).
EX1019	RESERVED
EX1020	U.S. Patent No. 7,288,443 B2 to Zhu.
EX1021	U.S. Patent Appl. Pub. No. 2004/0115916 A1 to Lochtefeld et al.
EX1022	RESERVED
EX1023	S.-L. Zhang & M. Östling, <i>Metal Silicides in CMOS Technology: Past, Present, and Future Trends</i> , Critical Reviews in Solid-State Materials Sciences, vol. 28, no. 1, pp. 1-129 (2003).
EX1024- EX1026	RESERVED
EX1027	J.P. Dismukes et al., “Lattice Parameter and Density in Silicon-Germanium Alloys,” Journal of Physical Chemistry, vol. 68, no. 10, pp. 3021-27 (Oct. 1964).

APPENDIX C

Appendix C: Challenged Claims

Claim 1	
Element	Claim Language
[1Pre]	A semiconductor structure, comprising:
[1A]	a substrate, having therein a first well of a first conductivity type and a second well of a second conductivity type;
[1B]	a first MOS transistor of the first conductivity type on the second well, comprising:
[1C]	a first gate structure on the second well; and
[1D]	a first strained layer of the first conductivity type in a first opening in the second well beside the first gate structure, wherein a difference between a lattice parameter of a portion of the first strained layer near a bottom of the first opening and a lattice parameter of the substrate is smaller than a difference between a lattice parameter of a portion of the first strained layer apart from the bottom of the first opening and the lattice parameter of the substrate; and
[1E]	a second MOS transistor of the second conductivity type on the first well.

Claim 2
The semiconductor structure of claim 1, wherein the lattice parameter of the first strained layer has a gradient distribution.

Claim 3
The semiconductor structure of claim 1, wherein the first conductivity type is P-type, and the lattice parameter of a portion of the first strained layer near the bottom of the first opening is smaller than the lattice parameter of a portion of the first strained layer apart from the bottom of the first opening.

Claim 4
The semiconductor structure of claim 3, wherein the first strained layer comprises SiGe.

Claim 5
The semiconductor structure of claim 1, wherein the first conductivity type is N-type, and the lattice parameter of a portion of the first strained layer near the bottom of the first opening is larger than the lattice parameter of a portion of the first strained layer apart from the bottom of the first opening.

Claim 6
The semiconductor structure of claim 5, wherein the first strained layer comprises SiC.

Claim 7	
Element	Claim Language
[7Pre]	The semiconductor structure of claim 1, wherein the second MOS transistor comprises:
[7A]	a second gate structure on the first well; and
[7B]	a source/drain region of the second conductivity type in the first well beside the second gate structure.

Claim 8	
Element	Claim Language
[8Pre]	The semiconductor structure of claim 7, further comprising:

Claim 8	
Element	Claim Language
[8A]	a silicon layer on the first strained layer; and
[8B]	a metal silicide layer on the silicon layer, the source/drain region and the first and the second gate structures.

Claim 9	
Element	Claim Language
[9Pre]	The semiconductor structure of claim 1, wherein the second MOS transistor comprises:
[9A]	a second gate structure on the first well; and
[9B]	a source/drain region of the second conductivity type around and under a second opening in the first well beside the second gate structure.

Claim 10	
Element	Claim Language
[10Pre]	The semiconductor structure of claim 9, further comprising:
[10A]	a silicon layer on the first strained layer; and
[10B]	a metal silicide layer on the silicon layer, the source/drain region and the first and the second gate structures.

Claim 11	
Element	Claim Language
[11Pre]	The semiconductor structure of claim 1, wherein the second MOS transistor comprises:

Claim 11	
Element	Claim Language
[11A]	a second gate structure on the first well; and
[11B]	a second strained layer of the second conductivity type in a second opening in the first well beside the second gate structure.

Claim 12	
Element	Claim Language
[12Pre]	The semiconductor structure of claim 11, wherein
[12A]	a difference between a lattice parameter of a portion of the second strained layer near a bottom of the second opening and the lattice parameter of the substrate is smaller than a difference between a lattice parameter of a portion of the second strained layer apart from the bottom of the second opening and the lattice parameter of the substrate;
[12B]	when the first conductivity type is P-type and the second conductivity type is N-type, the lattice parameter of a portion of the first strained layer near the bottom of the first opening is smaller than the lattice parameter of a portion of the first strained layer apart from the bottom of the first opening, but the lattice parameter of a portion of the second strained layer near the bottom of the second opening is larger than the lattice parameter of a portion of the second strained layer apart from the bottom of the second opening; and
[12C]	when the first conductivity type is N-type and the second conductivity type is P-type, the lattice parameter of a portion of the first strained layer near the bottom of the first opening is larger than the lattice parameter of a portion of the first strained layer apart from the bottom of the first opening, but the lattice parameter of a portion of the second strained layer near the bottom of the second opening is smaller than the

Claim 12	
Element	Claim Language
	lattice parameter of a portion of the second strained layer apart from the bottom of the second opening.

Claim 13	
The semiconductor structure of claim 12, wherein the lattice parameter of the second strained layer has a gradient distribution.	

Claim 14	
Element	Claim Language
[14Pre]	The semiconductor structure of claim 11, further comprising:
[14A]	a silicon layer on the first strained layer and the second strained layer; and
[14B]	a metal silicide layer on the silicon layer and the first and second gate structures.