

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Taiwan Semiconductor Manufacturing Company Ltd.,

Petitioner

v.

Marlin Semiconductor Limited,

Patent Owner

Patent No. 7,288,822 B2
Filing Date: April 7, 2006
Issue Date: October 30, 2007

Title: SEMICONDUCTOR STRUCTURE AND
FABRICATING METHOD THEREOF

Inter Partes Review No. IPR2026-00058

PETITION FOR *INTER PARTES* REVIEW

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TABLE OF EXHIBITS

Exhibit	Description
EX1001	U.S. Patent No. 7,288,822 to Ting et al. (“’822 Patent”).
EX1002	Prosecution History of the ’822 Patent (“Prosecution History”).
EX1003	Declaration of Dr. Jack Lee (“Lee Decl.”)
EX1004	U.S. Patent Appl. Pub. No. 2006/0134873 A1 to Koontz (“Koontz”).
EX1005	U.S. Patent Appl. Pub. No. 2005/0079692 A1 to Samoilov et al. (“Samoilov”).
EX1006	U.S. Patent No. 7,238,580 B2 to Orłowski et al. (“Orłowski”).
EX1007	U.S. Patent Appl. Pub. No. 2005/0090082 A1 to Sridhar et al. (“Sridhar”).
EX1008	S.M. Sze, <i>Physics of Semiconductor Devices</i> (2d ed. 1981) (excerpted).
EX1009	J.D. Plummer et al., <i>Silicon VLSI Technology: Fundamentals, Practice and Modeling</i> (2000) (excerpted).
EX1010	M. Quirk & J. Serda, <i>Semiconductor Manufacturing Technology</i> (2001) (excerpted).
EX1011	U.S. Patent No. 7,195,985 B2 to Murthy et al. (“Murthy”)
EX1012	U.S. Patent Appl. Pub. No. 2005/0266631 A1 to Kim et al.
EX1013	U.S. Patent Appl. Pub. No. 2007/0238236 A1 to Cook, Jr. et al.

EX1014	S.E. Thompson et al., “A Logic Nanotechnology Featuring Strained-Silicon,” IEEE Electron Device Letters, vol. 25. No. 4, pp. 191-93 (Apr. 2004).
EX1015	Y. Sun et al., <i>Physics of Strain Effects in Semiconductors and Metal-Oxide-Semiconductor Field-Effect Transistors</i> , Journal of Applied Physics, vol. 101, art. No. 104503 (22 pages) (May 2007).
EX1016	P. Bai et al., <i>A 65nm Logic Technology Featuring 35nm Gate Lengths, Enhanced Channel Strain, 8 Cu Interconnect Layers, Low-k ILD and 0.57 μm^2 SRAM Cell</i> , Technical Digest of the 2004 IEEE International Electron Devices Meeting, pp. 657-60 (Dec. 2004).
EX1017	U.S. Patent No. 6,949,482 B2 to Murthy et al. (“Murthy482”)
EX1018	H. Richter et al., <i>Defect Engineering in SiGe Heterostructures</i> , Proceedings of the 1996 CAS International Semiconductor Conference, pp. 41-50 (Oct. 1996).
EX1019	RESERVED
EX1020	U.S. Patent No. 7,288,443 B2 to Zhu.
EX1021	U.S. Patent Appl. Pub. No. 2004/0115916 A1 to Lochtefeld et al.
EX1022	RESERVED
EX1023	S.-L. Zhang & M. Östling, <i>Metal Silicides in CMOS Technology: Past, Present, and Future Trends</i> , Critical Reviews in Solid-State Materials Sciences, vol. 28, no. 1, pp. 1-129 (2003).
EX1024- EX1026	RESERVED
EX1027	J.P. Dismukes et al., “Lattice Parameter and Density in Silicon-Germanium Alloys,” Journal of Physical Chemistry, vol. 68, no. 10,

	pp. 3021-27 (Oct. 1964).
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LIST OF CHALLENGED CLAIMS

Claim 1	
[1Pre]	A semiconductor structure, comprising:
[1A]	a substrate, having therein a first well of a first conductivity type and a second well of a second conductivity type;
[1B]	a first MOS transistor of the first conductivity type on the second well, comprising:
[1C]	a first gate structure on the second well; and
[1D]	a first strained layer of the first conductivity type in a first opening in the second well beside the first gate structure, wherein a difference between a lattice parameter of a portion of the first strained layer near a bottom of the first opening and a lattice parameter of the substrate is smaller than a difference between a lattice parameter of a portion of the first strained layer apart from the bottom of the first opening and the lattice parameter of the substrate; and
[1E]	a second MOS transistor of the second conductivity type on the first well.
Claim 2	
The semiconductor structure of claim 1, wherein the lattice parameter of the first strained layer has a gradient distribution.	
Claim 3	
The semiconductor structure of claim 1, wherein the first conductivity type is P-type, and the lattice parameter of a portion of the first strained layer near the bottom of the first opening is smaller than the lattice parameter of a portion of the first strained layer apart from the bottom of the first opening.	
Claim 4	
The semiconductor structure of claim 3, wherein the first strained layer comprises SiGe.	

Claim 5	
The semiconductor structure of claim 1, wherein the first conductivity type is N-type, and the lattice parameter of a portion of the first strained layer near the bottom of the first opening is larger than the lattice parameter of a portion of the first strained layer apart from the bottom of the first opening.	
Claim 6	
The semiconductor structure of claim 5, wherein the first strained layer comprises SiC.	
Claim 7	
[7Pre]	The semiconductor structure of claim 1, wherein the second MOS transistor comprises:
[7A]	a second gate structure on the first well; and
[7B]	a source/drain region of the second conductivity type in the first well beside the second gate structure.
Claim 8	
[8Pre]	The semiconductor structure of claim 7, further comprising:
[8A]	a silicon layer on the first strained layer; and
[8B]	a metal silicide layer on the silicon layer, the source/drain region and the first and the second gate structures.
Claim 9	
[9Pre]	The semiconductor structure of claim 1, wherein the second MOS transistor comprises:
[9A]	a second gate structure on the first well; and
[9B]	a source/drain region of the second conductivity type around and under a second opening in the first well beside the second gate structure.

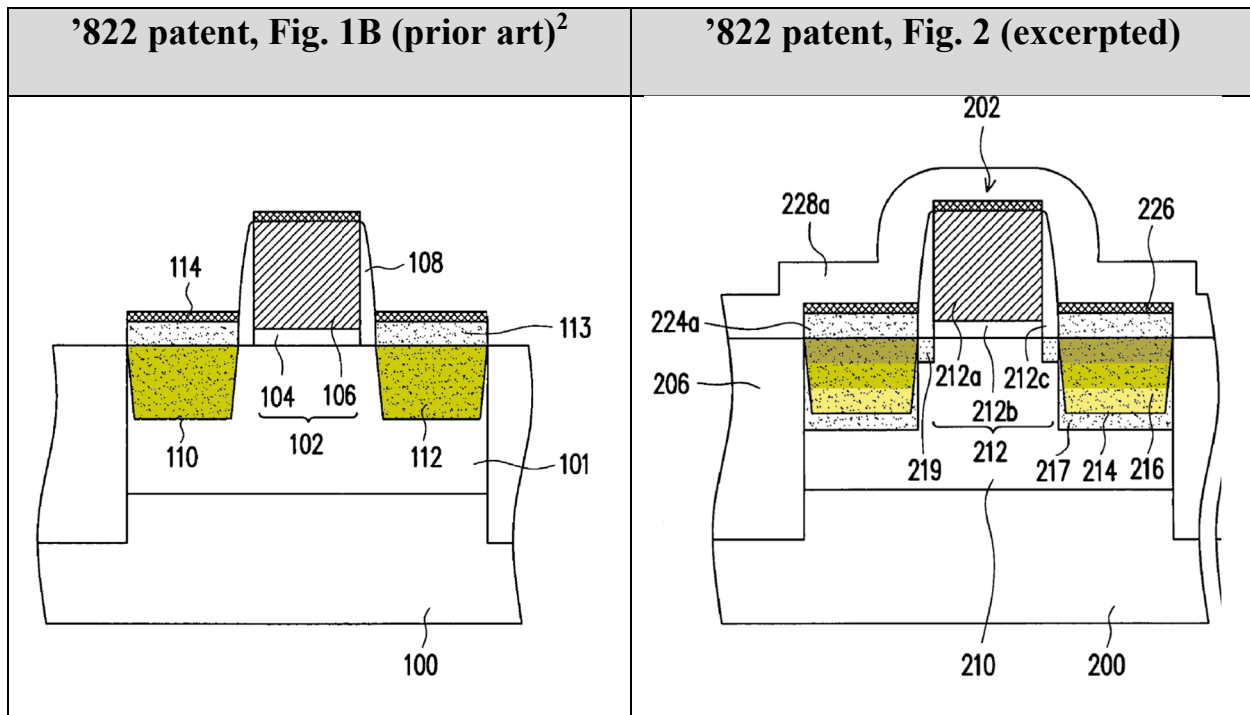
Claim 10	
[10Pre]	The semiconductor structure of claim 9, further comprising:
[10A]	a silicon layer on the first strained layer; and
[10B]	a metal silicide layer on the silicon layer, the source/drain region and the first and the second gate structures.
Claim 11	
[11Pre]	The semiconductor structure of claim 1, wherein the second MOS transistor comprises:
[11A]	a second gate structure on the first well; and
[11B]	a second strained layer of the second conductivity type in a second opening in the first well beside the second gate structure.
Claim 12	
[12Pre]	The semiconductor structure of claim 11, wherein
[12A]	a difference between a lattice parameter of a portion of the second strained layer near a bottom of the second opening and the lattice parameter of the substrate is smaller than a difference between a lattice parameter of a portion of the second strained layer apart from the bottom of the second opening and the lattice parameter of the substrate;
[12B]	when the first conductivity type is P-type and the second conductivity type is N-type, the lattice parameter of a portion of the first strained layer near the bottom of the first opening is smaller than the lattice parameter of a portion of the first strained layer apart from the bottom of the first opening, but the lattice parameter of a portion of the second strained layer near the bottom of the second opening is larger than the lattice parameter of a portion of the second strained layer apart from the bottom of the second opening; and

[12C]	when the first conductivity type is N-type and the second conductivity type is P-type, the lattice parameter of a portion of the first strained layer near the bottom of the first opening is larger than the lattice parameter of a portion of the first strained layer apart from the bottom of the first opening, but the lattice parameter of a portion of the second strained layer near the bottom of the second opening is smaller than the lattice parameter of a portion of the second strained layer apart from the bottom of the second opening.
Claim 13	
The semiconductor structure of claim 12, wherein the lattice parameter of the second strained layer has a gradient distribution.	
Claim 14	
[14Pre]	The semiconductor structure of claim 11, further comprising:
[14A]	a silicon layer on the first strained layer and the second strained layer; and
[14B]	a metal silicide layer on the silicon layer and the first and second gate structures.

I. INTRODUCTION

The '822 patent¹ is directed to a semiconductor structure that supposedly improves upon prior structures. In a semiconductor structure, atoms are arranged in a repeating 3D pattern called a lattice, where the distance between atoms is referred to as a lattice parameter. In general, different semiconductor materials have different lattice parameters; thus, the lattice parameter of a semiconductor device can be controlled through its material composition. The '822 patent allegedly improves upon prior semiconductor structures by having a source/drain region with a *non-uniform* lattice parameter distribution to prevent defects. EX1001-USP'822, 1:57-62. Compared to prior art Figure 1B (left) having uniform source/drain regions 112, Figure 2 (right) has source/drain regions 216 having a “gradient distribution”—the lattice parameter near the bottom of region 216 is closer to that of substrate 200 than the lattice parameter towards the top of region 216. *Id.*, 1:31-34, 4:65-5:19, 5:61-6:2, claim 1.

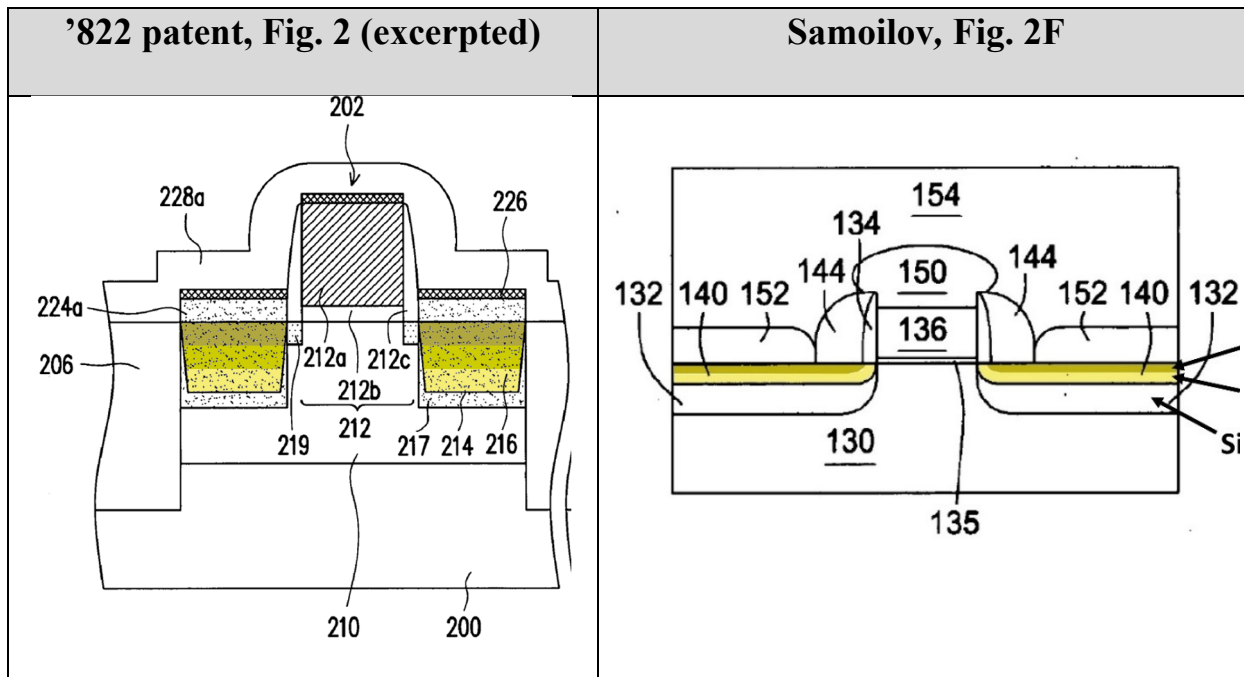
¹ U.S. Patent No. 7,288,822 (EX1001).



However, source/drain regions with a non-uniform lattice parameter distribution were already known before the '822 patent, as shown in Figure 2F (right) of prior art reference Samoilov³ shown below. EX1005-Samoilov, ¶¶[0030], [0032], [0061], [0072], [0074].

² All annotations added unless otherwise noted.

³ U.S. Patent Appl. Pub. No. 2005/0079692.



Notably, the Applicant did not submit any prior art to the Patent office during examination of the '822 patent, nor did the Examiner issue any rejections on the basis of prior art. As set forth in this Petition, Orłowski and other prior art references disclose the purported improvement of the '822 patent as well as each of the remaining claim limitations, rendering the challenged claims unpatentable.

II. RELIEF REQUESTED

Petitioner requests *inter partes* review on the following grounds:

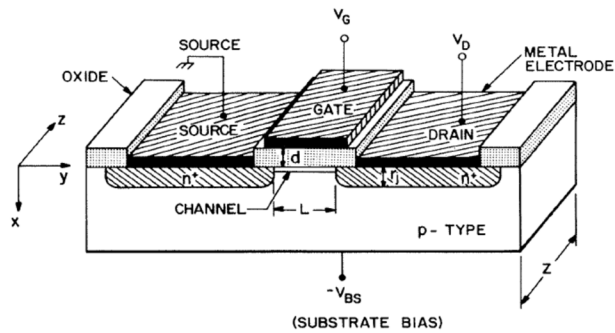
Ground	Claim(s) Challenged	35 U.S.C. §	Reference(s)
1A	1-7, 9, 11-13	§103	Koontz
1B	8, 10, 14	§103	Koontz, Sridhar
2	1-4	§102	Orłowski
3A	1-7, 9, 11-13	§103	Samoilov, Murthy
3B	8, 10, 14	§103	Samoilov, Murthy, Sridhar

III. STATE OF THE ART

The '822 patent is directed to semiconductor structures, specifically for MOSFETs. *See, e.g.*, EX1001-USP'822, Title, Abstract, 1:7-11, claim 1. At the time of the '822 patent, many semiconductor structures for MOSFETs were well-known, as described below.

A. MOSFETs

A *transistor* is a device designed to control the flow of electrical current, i.e. the flow of charge. Fundamentally, transistors operate like a “switch” that can be either ON or OFF. MOSFETs, a type of transistor, have a *source* (current input) and a *drain* (current output) separated by a *channel* region through which current or charge may flow. EX1008-Sze, 433-34, Figs. 3, 6; EX1009-Plummer, 76-82. MOSFETs also have a *gate* over the *channel* region, separated from the channel region by a *gate dielectric* (also called gate “oxide”). EX1008-Sze, 433-34, Fig. 3; EX1009-Plummer, 71-76. Applying appropriate voltage to the gate forms a conductive channel in the channel region, electrically connecting the source and drain so that current or charge flows between them. EX1008-Sze, 433-34, 438, Figs. 3, 6.



EX1008-Sze, Fig. 3. EX1003-Lee-Decl., ¶¶26-27.

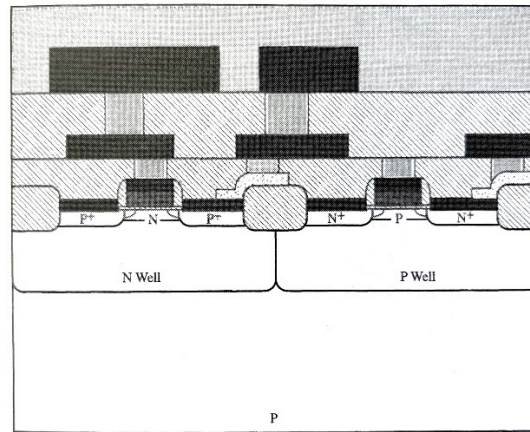
B. Semiconductor Materials

Transistors, such as MOSFETs, in integrated circuits are formed from “semiconductor” material (typically silicon (“Si”)). EX1008-Sze, 431-32; EX1009-Plummer, 7-8. *Semiconductors* are materials with a conductance (i.e., how easy it is for a charge to flow) somewhere in between a conductor (high conductance) and an insulator (low conductance). EX1009-Plummer, 13. The properties of a semiconductor can be altered by adding *impurities* that can introduce extra *electrons* or *holes* (which represent the absence of an electron) into the semiconductor. Impurities that introduce extra electrons are called *n-type* impurities. *Id.*, 7-8, 13. Impurities that introduce extra holes are called *p-type* impurities. *Id.* Semiconductor devices and circuits are fabricated by etching and depositing structures on a semiconductor *substrate*. EX1008-Sze, 433-34, Fig. 3. EX1003-Lee-Decl., ¶¶28-30.

C. MOSFET Fabrication

In a MOSFET, source/drain regions are *doped* with either *p-type* or *n-type* impurities, and the channel region is doped with the opposite type of impurity. *See* EX1008-Sze, 433-34; EX1009-Plummer, 76-82. MOSFETs with *n-type* source/drain regions are called **NMOS**, and ones with *p-type* source/drain regions are called **PMOS**. EX1009-Plummer, 12-13, 50-51, Figs. 1-11, 2-2. Integrated circuits with both NMOS and PMOS devices are called **CMOS**. *Id.* Current flows into and out of a MOSFET through electrical *contacts* on the surfaces of the source/drain regions. These contacts are typically made of *silicide*—a conductive metal-silicon compound. *See, e.g.,* EX1009-Plummer, 82-84; EX1010-Quirk, 214, 309-12, Figs. 9.19, 12.9-13; EX1023-Zhang, 9-12, Fig. 8. EX1003-Lee-Decl., ¶¶31, 41-42.

As the figure below illustrates, MOSFET devices in CMOS circuits are generally formed in respective well regions – an *n-type well* region (“**N Well**”) for PMOS and a *p-type well* region (“**P Well**”) for NMOS. EX1009-Plummer, 51-52, Figs. 1-11, 2-2. This use of wells helps control the device characteristics during manufacturing. *Id.*, 52; *see also* EX1010-Quirk, 205-07, Figs. 9.8, 9.9; EX1004-Koontz ¶[0041], ¶[0053], Figs. 3, 4A-4N; EX1011-Murthy, 3:14-4:6, Fig. 4; EX1012-Kim, ¶[0054], EX1009-Plummer, Fig. 2-29; EX1013-Cook, ¶¶[0022]-[0023], Figs. 1-11.



EX1009-Plummer, Fig. 1-11. EX1003-Lee-Decl., ¶¶32-33.

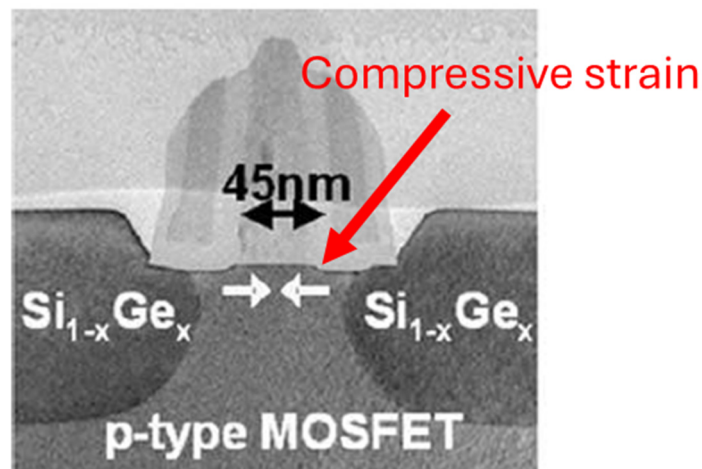
D. Strained Silicon Technology

Strained silicon technology involves applying physical strain (tensile or compressive strain) to a MOSFET's channel region to reduce its electrical resistance, thereby improving operating speed. EX1014-Thompson, 191-93; EX1015-Sun, 2. EX1003-Lee-Decl., ¶34.

Strain can be introduced by adjusting a semiconductor material's *lattice parameter*, which measures the spacing between neighboring atoms. For example, silicon has a lattice parameter that can be increased by mixing the silicon with a larger element such as germanium (forming silicon-germanium) or decreased by mixing with a smaller element such as carbon (forming silicon-carbon). The percentage of silicon in the mixture relative to germanium or carbon determines how small or large the difference is between the lattice parameter of the silicon mixture

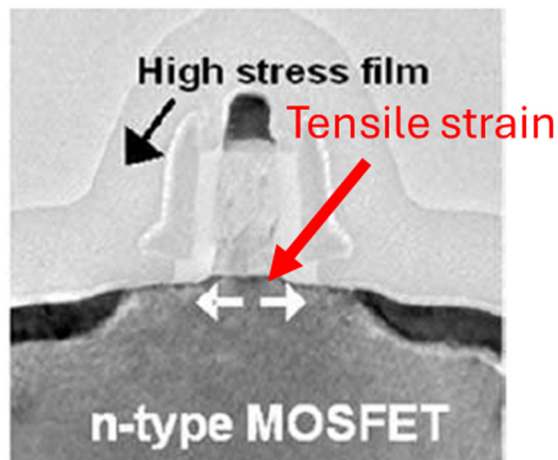
and the lattice parameter of pure silicon. EX1017-Murthy482, 1:45-48; EX1018-Richter, 41, 46; EX1027-Dismukes, Fig. 3, Tbl. IV. EX1003-Lee-Decl., ¶35.

In PMOS transistors, performance improves when the channel region is subject to **compressive** strain (forces pushing the channel region) in the direction of current flow. EX1006-Orlowski, 1:15-23. By using silicon-germanium in the source/drain regions, its larger lattice parameter relative to silicon creates the desired compressive strain, as illustrated below. By 2005, this technique had doubled PMOS operating speeds.



EX1014-Thompson, Fig. 1 (excerpt). EX1003-Lee-Decl., ¶36.

In NMOS transistors, performance improves when the channel region is subject to the opposite, namely **tensile** strain (forces pulling the channel region) in the direction of current flow, as illustrated below.



EX1014-Thompson, Fig. 1 (excerpt); *see also* EX1006-Orlowski, 1:15-23. By using silicon-carbon in the source/drain regions, its smaller lattice parameter relative to silicon creates the desired tensile strain. *See* EX1006-Orlowski, 6:15-28; EX1004-Koontz, ¶[0047], ¶¶[0059]-[0060]; EX1005-Samoilov, ¶[0009], ¶[0068]. EX1003-Lee-Decl., ¶37.

Strained silicon technology has a long history, *see* EX1015-Sun, 1-2, and was well-known by April 2006, *see* EX1001-USP'822, 1:17-27, 1:40-42, Fig. 1B. Two generations of high-volume commercial devices already used it by then. *See* EX1014-Thompson, 191 (Intel's 90nm devices); EX1016-Bai, 28.2.1 (Intel's 65nm devices). EX1003-Lee-Decl., ¶38.

E. Non-Uniform Source/Drain

To form a source/drain region, the material of the source/drain region is grown on a substrate. When the source/drain material has a different lattice parameter than the substrate, strain accumulates in the material as it grows, which may cause

dislocations, essentially cracks, to form in the source/drain region. EX1017-Murthy482, 1:49-56; EX1018-Richter, 41, 46-47; EX1020-Zhu, 5:11-13. EX1003-Lee-Decl., ¶39.

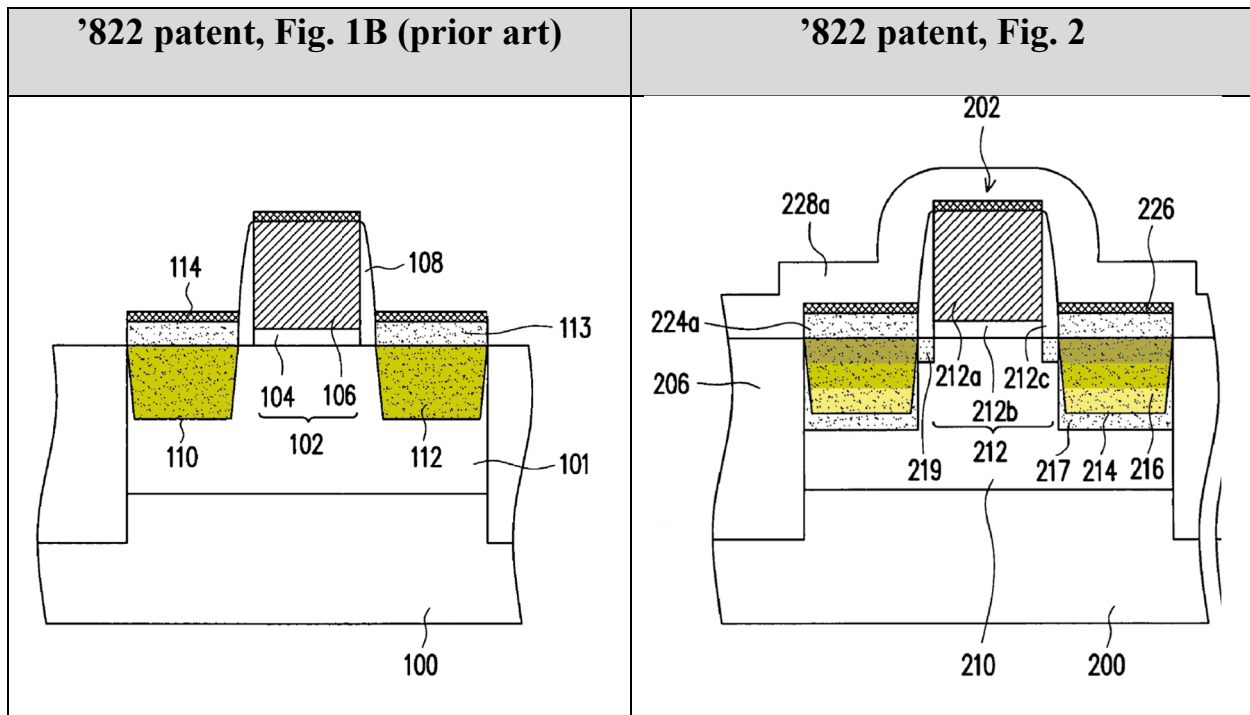
It was well-known to suppress dislocations by gradually increasing the concentration of germanium or carbon, thereby gradually adjusting the lattice parameter, as the source/drain region is formed, resulting in a non-uniform source/drain region with a gradient distribution. *See* EX1018-Richter, 46-48, Fig. 9; EX1020-Zhu, 1:56-64, 5:26-35; EX1006-Orlowski, 5:15-29; EX1005-Samoilov ¶[0030], ¶[0072], ¶[0074]; EX1004-Koontz, ¶[0034], ¶¶[0038]-[0039], Fig. 2C; EX1021-Lochtefeld, ¶[0003]. Since a graded source/drain region “does not have a sharp interface (where the dislocations are generated) between [silicon-germanium (or silicon-carbon)] and Si, dislocations are not easily produced.” EX1020-Zhu, 1:59-64; *see also* EX1018-Richter, 46-47. This technique also “provide[s] a method to optimize stress in order to enhance device performance.” EX1020-Zhu, 1:59-64. EX1003-Lee-Decl., ¶40.

IV. THE '822 PATENT

A. Overview

The '822 patent is directed to MOSFET devices having strained silicon channel regions and silicon-germanium or silicon-carbon source/drain regions. EX1001-USP'822, 1:6-11; *see also id.*, 1:37-44, 7:23-33. The '822 patent contends

that “defects easily occur at the interface of the [silicon-germanium (or silicon-carbon)] layer and the substrate lowering the device performance.” *Id.*, 1:45-51. To address this issue, it describes using source/drain regions “with a non-uniform lattice parameter distribution ... for decreasing the difference between the lattice parameters of the [source/drain] region and the substrate,” which purportedly reduces the likelihood of defects. *Id.*, 1:57-62. Compared to prior art Figure 1B (left) having source/drain region 112, Figure 2 (right) depicts a highly similar MOSFET device except that the silicon-germanium or silicon-carbon source/drain regions 216 are described as having a non-uniform distribution (e.g., a “gradient distribution”) – that is, the lattice parameter near the bottom of the source/drain region is closer to that of the substrate than the lattice parameter towards the top of the source/drain region. *Id.*, 1:31-34, 4:65-5:19, 5:61-6:2.



EX1003-Lee-Decl., ¶¶43-44.

The '822 patent additionally discloses techniques for forming silicide contacts on the source/drain regions and for implanting dopants “around and under” the source/drain regions. EX1001-USP'822, 1:51-53, 4:20-24, 5:19-24, 5:55-60, 6:54-62, 7:1-13. EX1003-Lee-Decl., ¶45.

B. Prosecution History

The '822 patent was filed April 7, 2006, and does not claim priority to any earlier applications. The prosecution history of the '822 patent is uneventful, as the claims received no rejections on the basis of prior art and the examiner's stated reasons for allowance were non-specific. *See* EX1002-PH'822, 40-52, 61-65. Notably, the Applicant did not submit any prior art with the filing or during the brief

prosecution of the '822 patent. EX1001-USP'822 ("References Cited" all "cited by examiner"). EX1003-Lee-Decl., ¶¶46-47.

C. Claim Construction

No terms appear to require construction for purposes of this Petition. Terms should receive their ordinary meaning as understood by one of ordinary skill in the art. *See Phillips v. AWH Corp.*, 415 F.3d 1303, 1312-13 (Fed. Cir. 2005) (en banc). EX1003-Lee-Decl., ¶48.

D. Level of Ordinary Skill

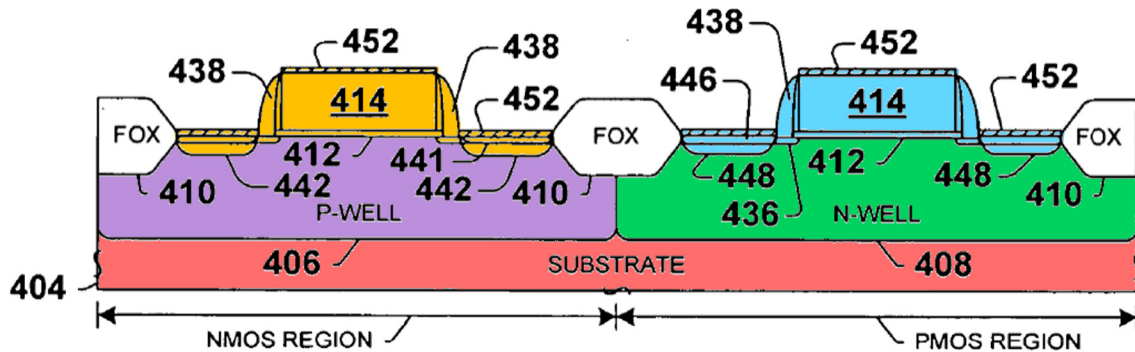
A person of ordinary skill in the art ("POSITA") would have had a master's degree in electrical engineering, physics, chemistry, materials science, or a related field and three years of work experience in semiconductor manufacturing, such as in integrated circuit device (or transistor) design and/or manufacturing. Additional relevant education could substitute for professional experience, and significant work experience or training could substitute for formal education. EX1003-Lee-Decl., ¶¶21-25.

V. OVERVIEW OF PRIOR ART

A. Koontz

U.S. Patent Appl. Pub. No. 2006/0134873 ("Koontz"), filed on December 22, 2004, is prior art at least under pre-AIA §102(e). Koontz teaches strained-channel

MOSFET devices with silicon-germanium or silicon-carbon “recess structures” in the source and drain regions.



EX1004-Koontz, Fig. 4N; *see also id.*, ¶¶[0059], [0063]. EX1003-Lee-Decl., ¶¶50-51.

The recess structures have a non-uniform (e.g., graded) composition of silicon-germanium or silicon-carbon. For example, Koontz discloses “linear” (line 252) and “non-linear” (line 253) strain profiles that can be obtained by correspondingly “adjusting [the] concentration of ... [the] recess structures.”

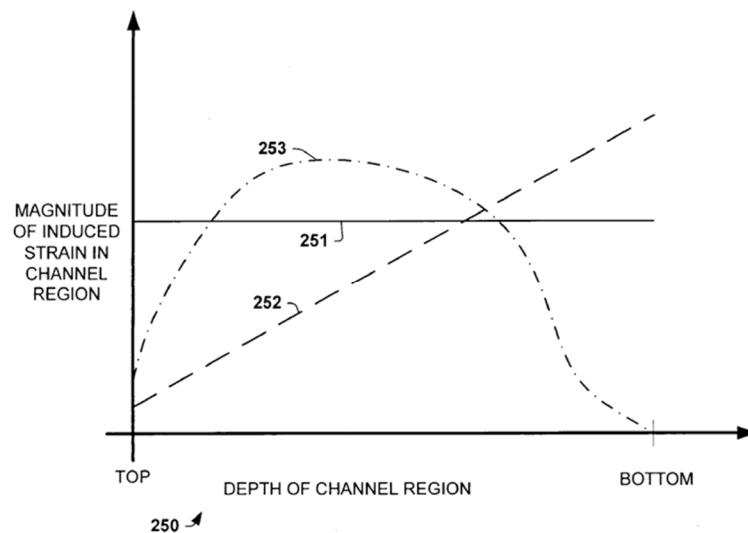
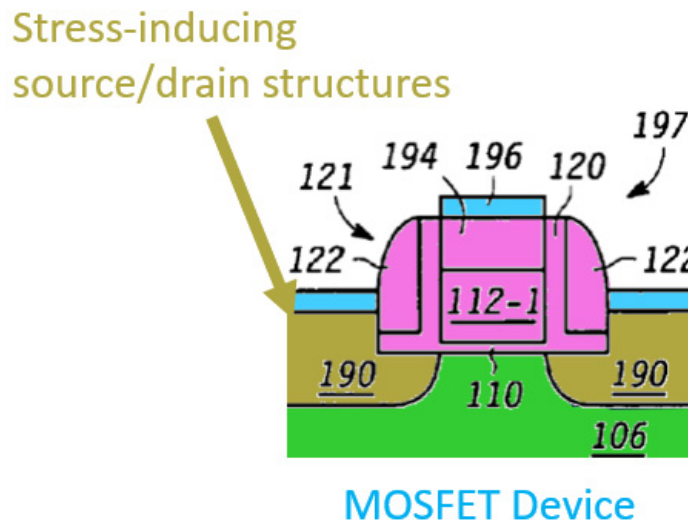


FIG. 2C

EX1004-Koontz, Fig. 2C; *see also id.*, ¶¶ [0038]-[0039]. EX1003-Lee-Decl., ¶52.

B. Orlowski

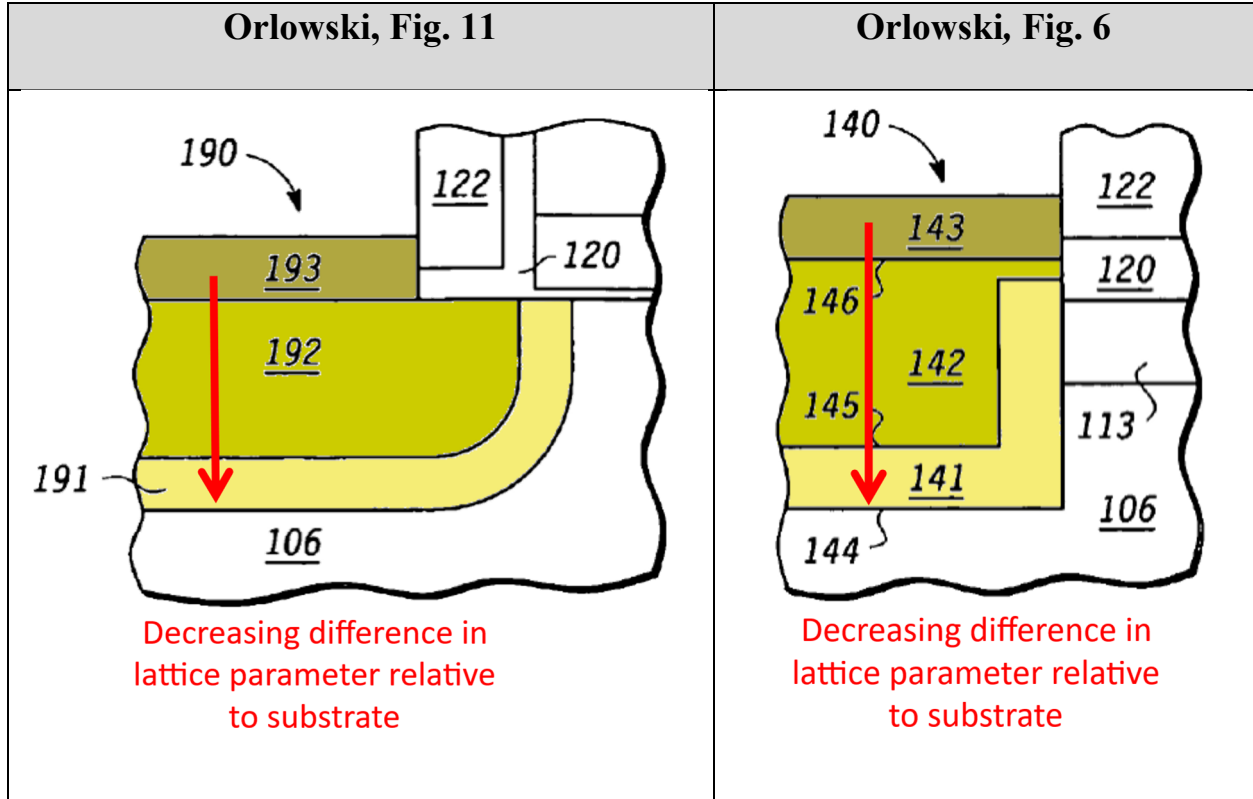
U.S. Patent No. 7,238,580 (“Orlowski”), filed on January 26, 2005, is prior art at least under pre-AIA §102(e). As shown in Figure 13 below, Orlowski teaches strained-channel MOSFET devices with silicon-germanium or silicon-carbon source/drain regions 190 (which it calls “stress-inducing source/drain (SISD) structures [190]”). EX1006-Orlowski, 2:34-37.



EX1006-Orlowski, Fig. 13. EX1003-Lee-Decl., ¶¶53-54.

Like the '822 patent, Orlowski discloses that it would be beneficial to use a non-uniform (e.g., graded) composition for the silicon-germanium or silicon-carbon source/drain structures. EX1006-Orlowski, 1:24-43, 2:34-55. Figures 11 (left) and 6 (right) illustrate embodiments of the graded composition where the difference in the lattice parameter of the source/drain structures 190 and 140, respectively, relative

to the lattice parameter of the substrate 106 becomes smaller near the bottom of the respective source/drain structures.

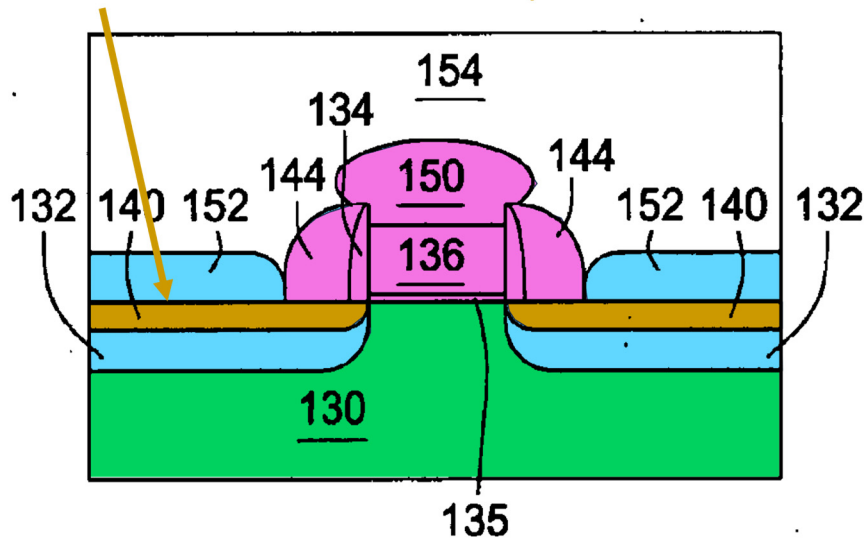


EX1006-Orlowski, 8:17-21. EX1003-Lee-Decl., ¶¶55-57.

C. Samoilov

U.S. Patent Appl. Pub. No. 2005/0079692 (“Samoilov”), published April 14, 2005, and filed on May 14, 2004, is prior art at least under pre-AIA §102(a) and §102(e). As shown in Figure 2F below, Samoilov teaches a strained-channel MOSFET device with strain-inducing silicon-germanium or silicon-carbon layers 140.

Silicon-Germanium or Silicon-Carbon Layer



EX1005-Samoilov, Fig. 2F; *see also id.*, ¶¶[0005], [0009], [0021], [0026], [0039].

Samoilov teaches that the silicon-germanium or silicon carbon layers 140 should be non-uniform (e.g., graded): “Multiple layers ... may be deposited in varying order to form graded elemental concentrations of silicon-containing layer 140.”

Id., ¶[0032]; *see also id.*, ¶¶[0030], [0072], [0074], claim 1. EX1003-Lee-Decl., ¶¶59-62.

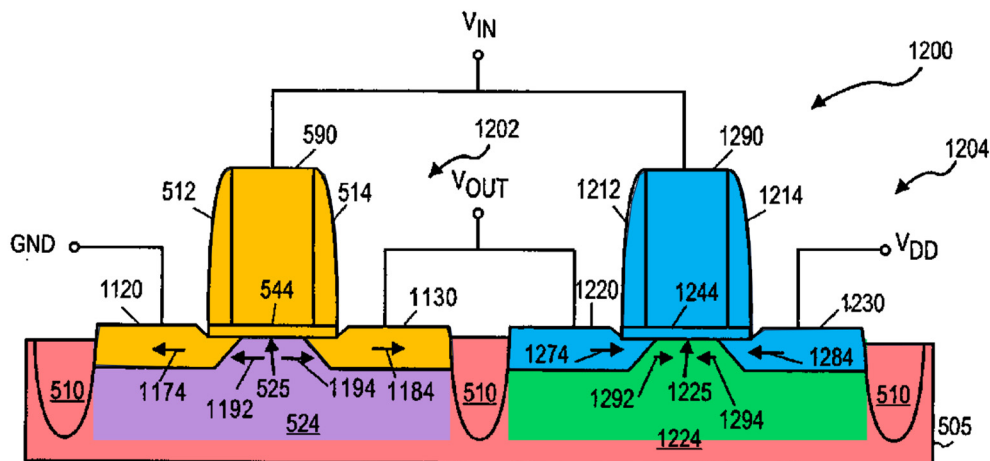
D. Sridhar

U.S. Patent Appl. Pub. No. 2005/0090082 (“Sridhar”), published April 28, 2005, and filed on October 28, 2003, is prior art at least under pre-AIA §102(a) and §102(e). Like Koontz, Samoilov, and Orlowski, Sridhar teaches strained-channel MOSFETs with source/drain regions having a lattice parameter that differs from that of silicon. EX1007-Sridhar, ¶¶[0003]-[0004], [0014]. Sridhar notes, however, that

the process of forming silicide contacts on the strain-inducing source/drain regions “may counteract the benefits by increasing source/drain resistances.” *Id.*, ¶¶[0003], [0014]. To address this issue, Sridhar proposes capping the source/drain regions with a “thin layer of silicon” and then forming a silicide contact layer using the thin layer of silicon. *Id.*, ¶¶[0004]-[0005], [0014]-[0017]. EX1003-Lee-Decl., ¶¶63-65.

E. Murthy

U.S. Patent No. 7,195,985 (“Murthy”), filed on January 4, 2005, is prior art at least under pre-AIA §102(e). Murthy discloses a substrate 505 suitable for forming PMOS and NMOS transistors like those described in the ’822 patent and disclosed in Samoilov and Sridhar.



EX1011-Murthy, Fig. 12; *see also id.*, 23:21-54, 23:5-20. EX1003-Lee-Decl., ¶¶66-67.

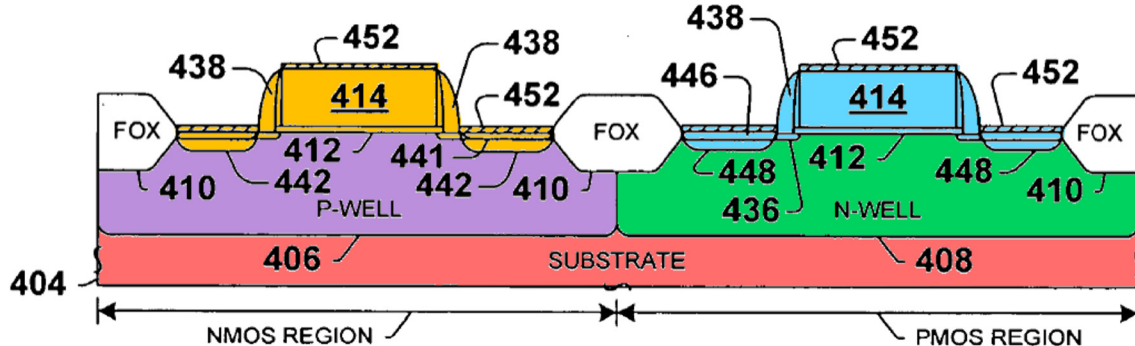
VI. THE CHALLENGED CLAIMS ARE UNPATENTABLE

A. Ground 1A: Koontz Renders Obvious Claims 1-7, 9, and 11-13

1. Claim 1

a. [1Pre]: “A semiconductor structure”

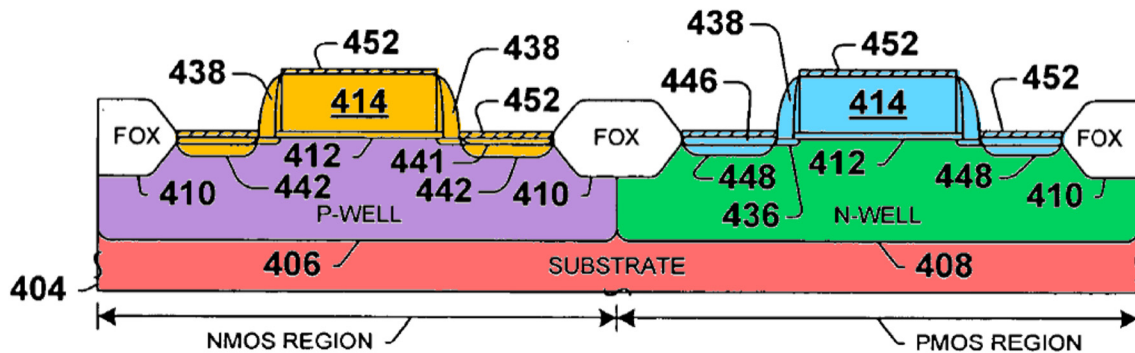
To the extent the preamble is limiting, Koontz discloses a semiconductor structure having “composition controlled filled recess structures.” EX1004-Koontz, ¶¶[0047], [0050], [0059], [0063]; *see also id.*, ¶¶[0013], [0020], [0029], [0031], [0034], [0040], Figs. 1, 2B-2C, 3, 4N. As shown below, the structure includes a substrate 404, a PMOS transistor on an N-well 408, and an NMOS transistor on a P-well 406.



EX1004-Koontz, Fig. 4N; *see also id.*, ¶¶[0015]-[0016], ¶¶[0040]-[0066], Figs. 1, 2B-2C, 3, 4A-4N. EX1003-Lee-Decl., ¶¶70-72.

- b. [1A]: “a substrate, having therein a first well of a first conductivity type and a second well of a second conductivity type”**

Referring to Figure 4N, Koontz teaches a substrate (e.g., **substrate 404**) having therein a first well (e.g., **P-well 406**) of a first conductivity type (e.g., p-type) and a second well (e.g., **N-well 408**) of a second conductivity type (e.g., n-type).



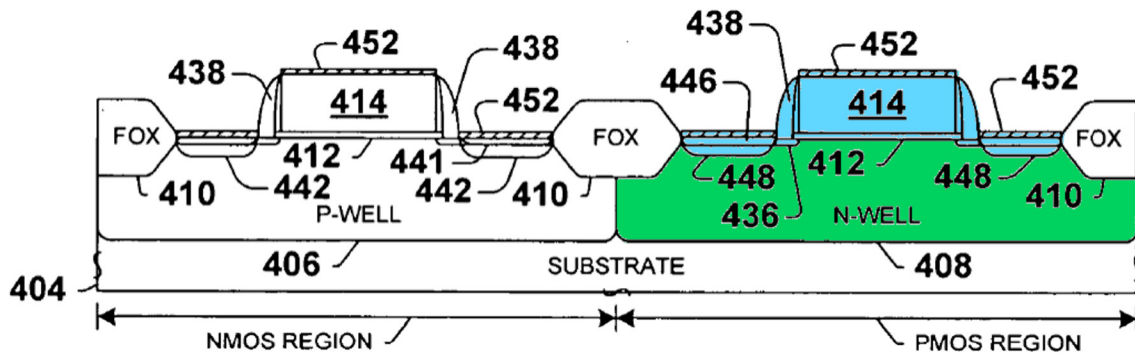
EX1004-Koontz, Fig. 4N; *see also id.*, ¶¶ [0029], [0041], [0053], Figs. 1, 3, 4A-4N.

EX1003-Lee-Decl., ¶¶73-74.

These teachings also satisfy the challenged claims when the conductivity types are reversed, i.e., when the “first conductivity type” is n-type and the “second conductivity type” is p-type. In this scenario, the first well corresponds to N-well 408 and the second well corresponds to P-well 406. EX1003-Lee-Decl., ¶74.

- c. [1B]: “a first MOS transistor of the first conductivity type on the second well”**

Referring to Figure 4N, Koontz discloses a first transistor (e.g., PMOS transistor) of the first conductivity type (e.g., p-type) on the second well (e.g., N-well 408).

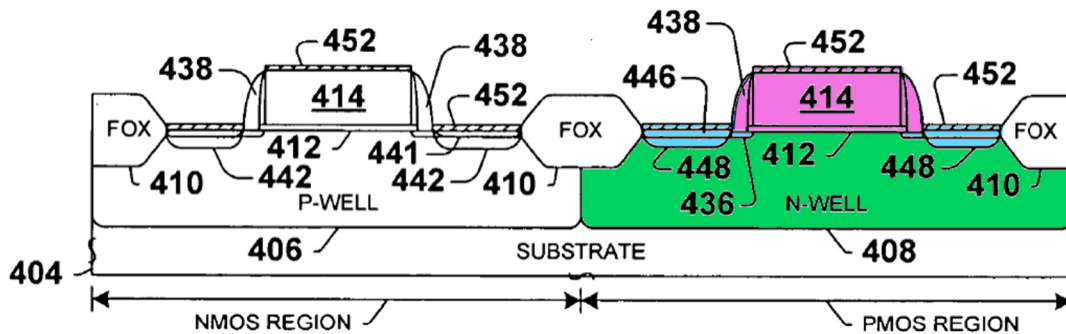


EX1004-Koontz, Fig. 4N; *see also id.*, ¶¶[0020], [0029], [0041], [0053], Figs. 1, 2B, 3. For example, Koontz teaches that “N-well 408 ... define[s] a PMOS transistor device region.” *Id.*, [0053]. EX1003-Lee-Decl., ¶¶75-76.

These teachings equally satisfy the challenged claims when the conductivity types are reversed, i.e., when the “first conductivity type” is n-type and the “second conductivity type” is p-type. In this scenario, the first MOS transistor corresponds an NMOS transistor on P-well 406. EX1003-Lee-Decl., ¶76.

d. [1C]: “first MOS transistor...comprising: a first gate structure on the second well”

Referring to Figure 4N, Koontz teaches that the first MOS transistor (e.g., PMOS transistor) includes a gate structure (e.g., gate electrode 414, gate oxide 412, and sidewall spacers 438) on N-well 408.

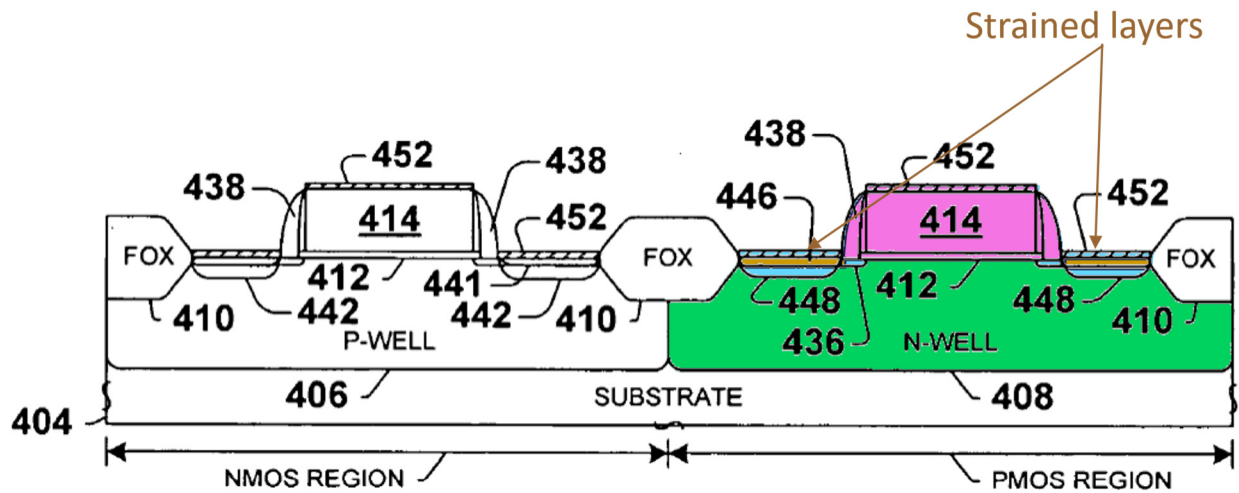


EX1004-Koontz, Fig. 4N; *see also id.*, ¶¶[0053]-[0066]. For example, Koontz teaches that “a gate electrode 414 overl[ies] the gate oxide” which is formed “over the active regions” of n-well 408. *Id.*, ¶¶[0053]-[0054]. EX1003-Lee-Decl., ¶¶77-79.

- e. [1D]: “first MOS transistor...comprising:...a first strained layer of the first conductivity type in a first opening in the second well beside the first gate structure, wherein a difference between a lattice parameter of a portion of the first strained layer near a bottom of the first opening and a lattice parameter of the substrate is smaller than a difference between a lattice parameter of a portion of the first strained layer apart from the bottom of the first opening and the lattice parameter of the substrate”

“first strained layer...beside the first gate structure”

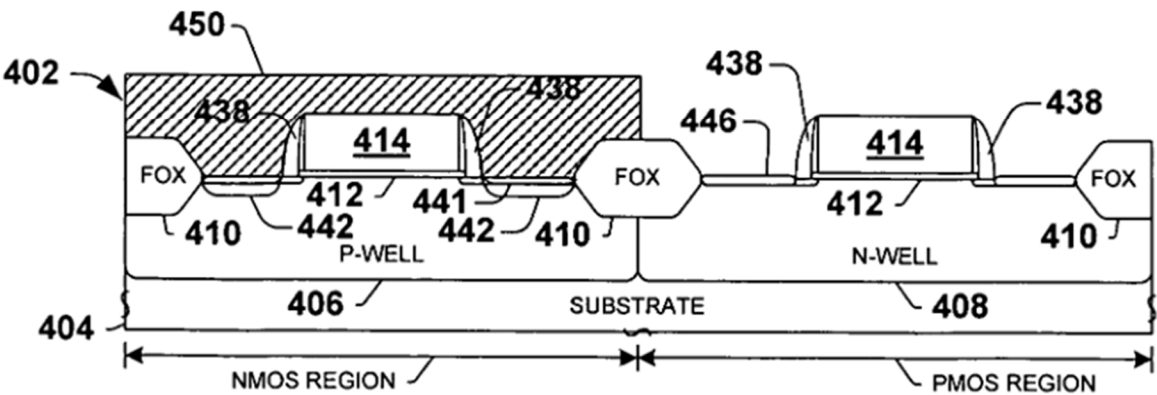
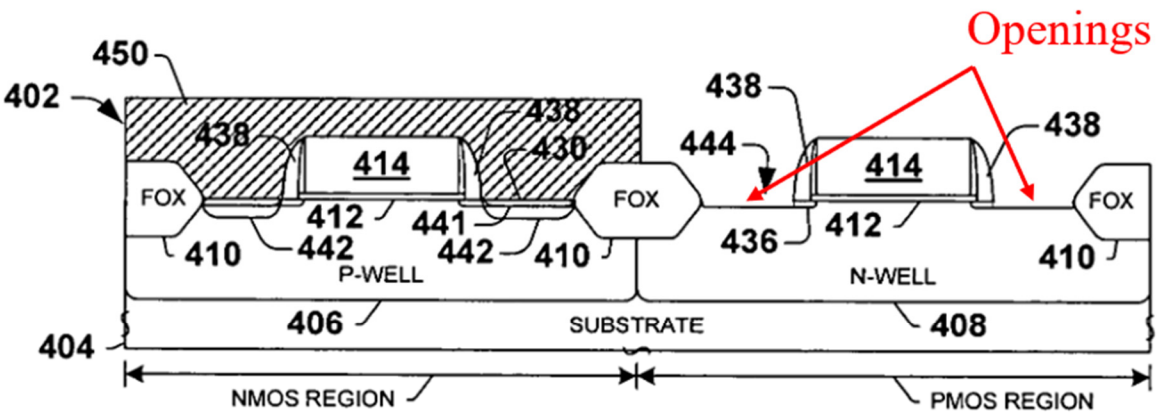
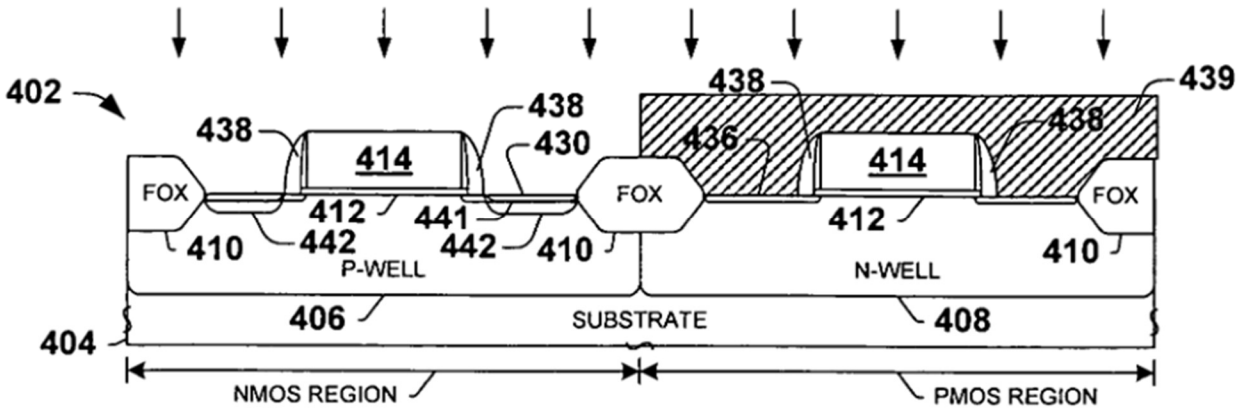
Referring to Figure 4N, Koontz discloses that the first MOS transistor (e.g., PMOS transistor) comprises a first strained layer (e.g., recess structures 446) of the first conductivity type (e.g., p-type) in a first opening in the second well (e.g., N-well 408) besides the first gate structure.



EX1004-Koontz, Fig. 4N; *see also id.*, ¶¶[0005]-[0006], [0025], [0027], [0033]-[0038], [0050], [0062]-[0063], Figs. 1, 2B-2C, 3. For example, Koontz teaches that recess structures 446 (the “first strained layer”) are “comprised of a compressive strain producing material” such that “a vertical strain profile... can be obtained.” *Id.*, ¶[0063]; *see also id.*, ¶¶[0006], [0026]. The ’822 patent describes the “strained layer” in the same way. EX1001-USP’822, 3:19-29, 4:65-5:19 (“strained layer” is “part of the S/D region of the MOS transistor” and creates stress to improve the transistor’s performance). EX1003-Lee-Decl., ¶¶80-83.

Koontz teaches that recess structures 446 (the “first strained layer”) have a first conductivity type (e.g., p-type). This is achieved by “implanting [p]-type dopants (e.g., boron).” EX1004-Koontz, ¶[0051]. Moreover, as shown in Figures 4J through 4L below, Koontz teaches that recess structures 446 are formed in

openings (e.g., recessed regions 444 formed by removing extension region 436) beside the gate structure.



EX1004-Koontz, Figs. 4J-4L; *see also id.*, ¶[0025] (process includes removing material from the substrate and “subsequently re-depositing and forming recess structures...comprised of a compressive strain producing material, such as silicon-germanium.”). EX1003-Lee-Decl., ¶¶84-85.

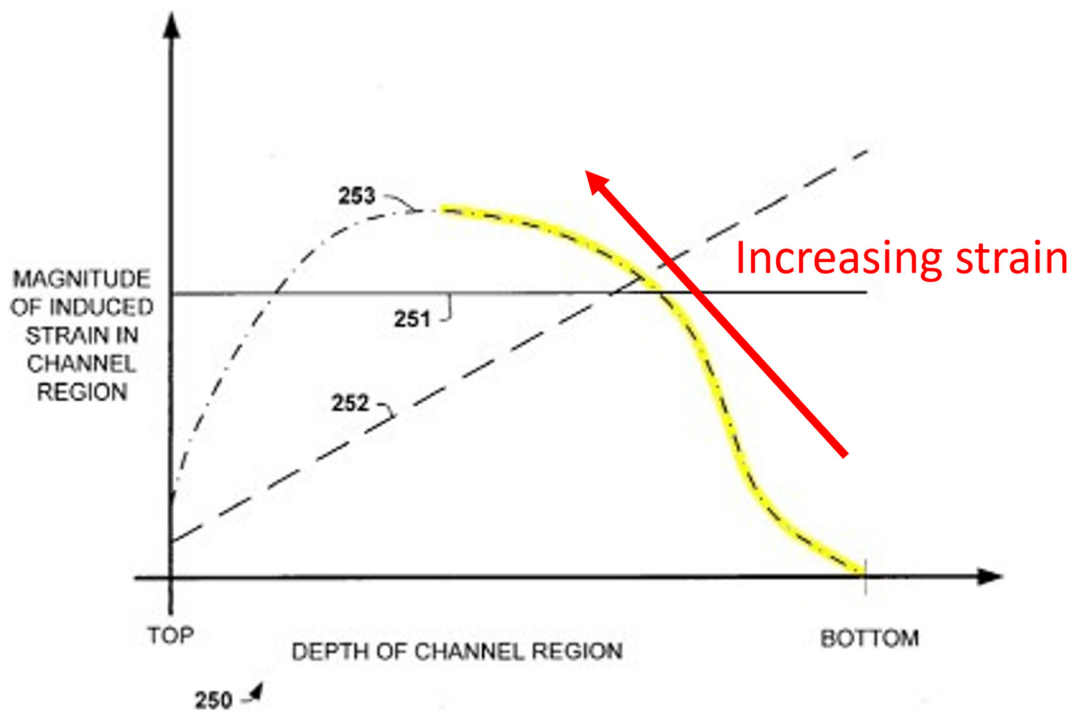
Strained Layer Has Non-Uniform Lattice Parameter in Opening Next to Gate

Koontz renders obvious “wherein a difference between a lattice parameter of a portion of the first strained layer near a bottom of the first opening and a lattice parameter of the substrate is smaller than a difference between a lattice parameter of a portion of the first strained layer apart from the bottom of the first opening and the lattice parameter of the substrate.” EX1003-Lee-Decl., ¶¶86-93.

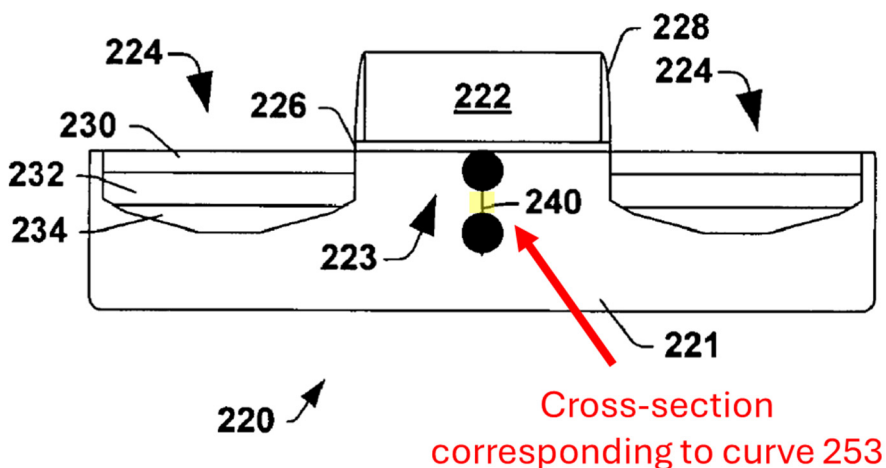
This limitation requires that the strained layer next to the gate has a non-uniform lattice parameter, meaning that its atoms are organized as a crystal lattice, but the *distance* between those atoms (i.e., the lattice parameter) varies vertically. Koontz discloses this limitation, stating that the composition of recess structures 446 (the claimed “first strained layer”) “***can vary in composition vertically*** from bottom to top of the structures 446.” EX1004-Koontz, ¶[0063]. As Dr. Lee explains, a POSITA would have understood that varying the composition (e.g., changing the percentage of germanium in the silicon-germanium mixture) results in a corresponding variation in the lattice parameter. *See* EX1017-Murthy482, 1:45-48 (difference between lattice constant of SiGe and that of Si varies depending on the

Ge percentage); EX1027-Dismukes, Fig. 3 (plotting this relationship). EX1003-Lee-Decl., ¶¶87-88.

However, Koontz does not specifically state that the difference between the lattice parameter of the strained layer and that of the substrate increases from bottom to top, as claimed. Instead, Koontz discloses that the *induced strain* in the channel region *underneath* the gate increases from the bottom to the top of the channel, as shown below in Figures 2C and 2B.



EX1004-Koontz, Fig. 2C;



Id., Fig. 2B. EX1003-Lee-Decl., ¶89.

Although Koontz does not expressly state how the *lattice parameter* of the strained layer *beside* the gate would be structured to produce the effect shown in Figure 2C, a POSITA would have understood (or at least found obvious) that the increasing strain in the channel region from bottom to top—as shown in Koontz’s Figure 2C—results from a corresponding increase in the difference between the lattice parameter of the strain-inducing regions next to the gate and that of the substrate—as claimed. For example, Koontz explains that recessed structures 446 (the “first strained layer”) are designed to create a controlled amount of strain in the transistor’s channel region. EX1004-Koontz, ¶¶[0034]-[0035], [0063]. According to Koontz, the lattice parameter of these structures can vary layer by layer, which allows engineers to shape the strain profile throughout the depth of the channel. *Id.* Indeed, Koontz explains that there is a direct correlation between the lattice

parameter of the recessed structures 446 and the strain in the channel: *increasing* the difference between the lattice parameter of recessed structures 446 and that of the substrate *increases* the strain in the channel, and vice versa. EX1004-Koontz, ¶[0063]; *see also id.*, ¶¶[0033]-[0036], [0059]. Similarly, *linearly* changing the difference between the lattice parameter of recessed structures 446 and that of the substrate causes a *linear* change in the strain in the channel, whereas a *non-linear* change in the lattice parameter causes a *non-linear* change in the strain. *Id.*, ¶[0038]. EX1003-Lee-Decl., ¶90.

Based on these teachings of Koontz, by disclosing increased strain (Fig. 2C, line 253) from the bottom of the channel (corresponding to “a portion of the first strained layer near a bottom of the first opening”) vertically toward a portion apart from the bottom of the channel. Koontz teaches a difference between the lattice parameter of recessed structures 446 near the bottom and that of the substrate is smaller than a difference between the lattice parameter of recessed structures 446 apart from the bottom and that of the substrate. EX1003-Lee-Decl., ¶91.

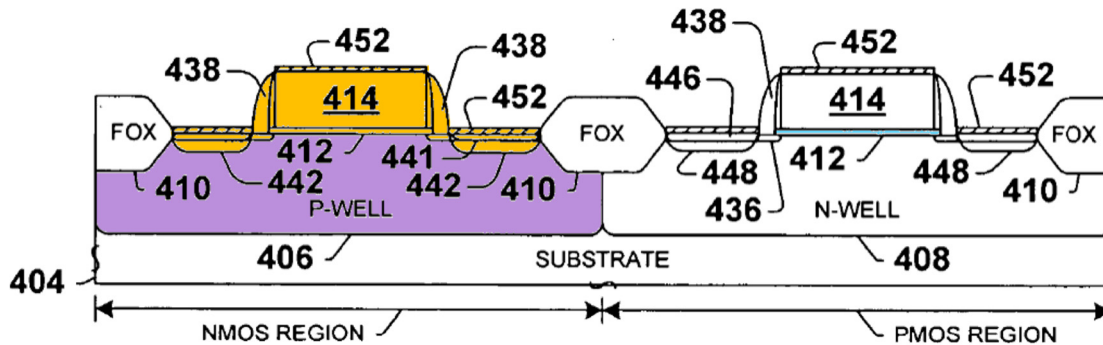
Alternatively, in view of these teachings, it would have been obvious to vary the lattice parameter of Koontz’s recess structures 446 (the “first strained layer”) in the vertical direction to produce the distribution of strain in the channel shown in Figure 2C. A POSITA would have understood that doing so would have yielded various benefits. *See* Section III.E. For example, such a graded lattice parameter

avoids a sharp interface between the silicon-germanium strained layer and the silicon substrate, thereby reducing the likelihood of dislocation defects. EX1020-Zhu, 1:56-64, 3:18-25. Therefore, a POSITA would have been motivated to vary the lattice parameter of Koontz's recessed structures (the "first strained layer") as described above, and would have had a reasonable expectation of success in doing so. EX1003-Lee-Decl., ¶92.

These teachings equally satisfy the challenged claims when the conductivity types are reversed, i.e., when the "first conductivity type" is n-type and the "second conductivity type" is p-type, as Koontz's NMOS transistor also includes the above-described recessed structures. EX1004-Koontz, ¶¶[0020], [0029], [0036], [0059], Figs. 1, 2B, 4N. In this scenario, Koontz teaches that the recessed structures (the "first strained layer") are formed using silicon-carbon (rather than silicon-germanium) and similarly would have rendered obvious the use of a non-uniform lattice parameter that substantially matches curve 253 (Fig. 2C shown above). *Id.*, ¶¶[0008], [0025], [0027], [0047], [0059], Figs. 3, 4N. EX1003-Lee-Decl., ¶93.

f. [1E]: "a second MOS transistor of the second conductivity type on the first well"

As shown in Figure 4N, Koontz discloses a second MOS transistor (e.g., **NMOS transistor**) of the second conductivity type (e.g., n-type) on the first well (e.g., **P-well 406**).

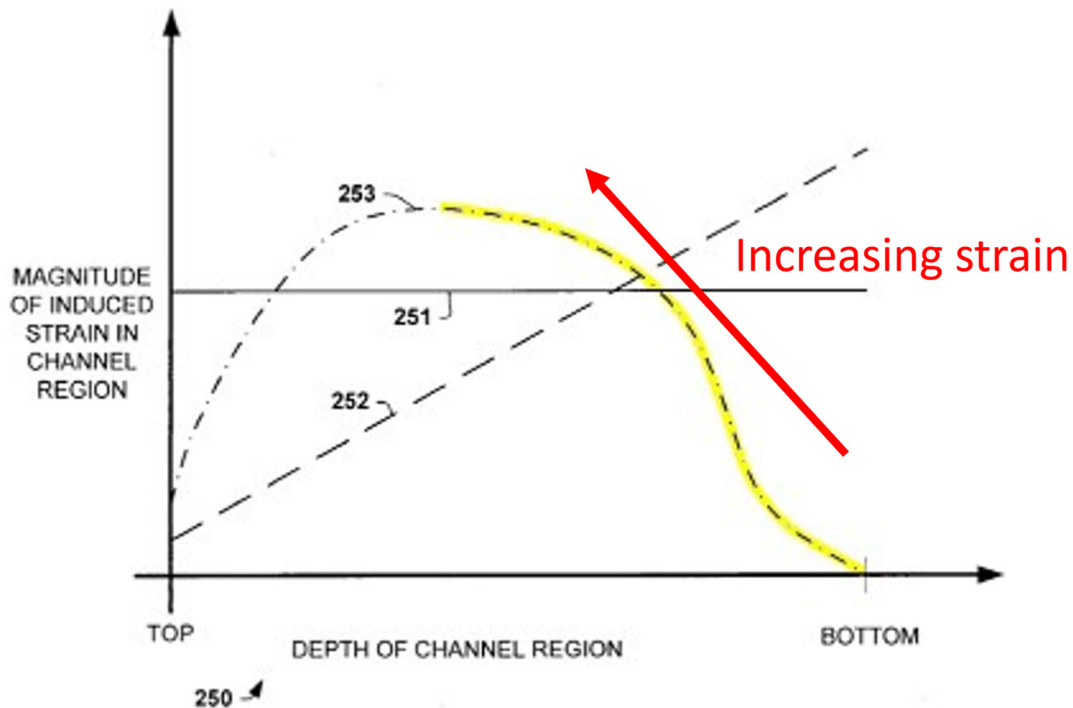


EX1004-Koontz, Fig. 4N; *see also id.*, ¶[0053]. For example, Koontz teaches that “P-well 406...define[s] an NMOS transistor device region.” *Id.*, ¶[0053]. EX1003-Lee-Decl., ¶¶94-95.

These teachings equally satisfy the challenged claims when the conductivity types are reversed, i.e., when the “second conductivity type” is n-type and the “first conductivity type” is p-type. In this scenario, the second MOS transistor corresponds PMOS transistors in N-well 408. EX1003-Lee-Decl., ¶95.

2. Claim 2: “The semiconductor structure of claim 1, wherein the lattice parameter of the first strained layer has a gradient distribution”

As explained above for Limitation [1D], Koontz teaches this limitation. Additionally, it would have been obvious to vary the lattice parameter of recess structures 446 (the “first strained layer”) to substantially match the gradient of curve 253, as shown below.



EX1004-Koontz, Fig. 2C. Doing so would have resulted in the lattice parameter having a gradient distribution, as claimed. *Id.*, [0022], [0034], [0038] (discussing the composition of recess structures having “linear” and “nonlinear” profiles). EX1003-Lee-Decl., ¶96.

3. **Claim 3: “The semiconductor structure of claim 1, wherein the first conductivity type is P-type, and the lattice parameter of a portion of the first strained layer near the bottom of the first opening is smaller than the lattice parameter of a portion of the first strained layer apart from the bottom of the first opening”**

Claim 3 uses technical language to describe a strained layer transistor structure in which the atoms at the bottom of the structure are packed closer together than atoms elsewhere in the structure (i.e., the portion of the strained layer at the bottom of the strained layer has a smaller “lattice parameter” than portions of the

strained layer that are not near the bottom). Koontz discloses claim 3. As explained above for Limitation [1D], when the first conductivity type is p-type, recess structures 446 are formed using silicon-germanium where the amount of germanium relative to silicon becomes smaller closer to the bottom of recess structures 446. EX1004-Koontz, ¶[0063]. A POSITA would have understood that the lattice parameter in silicon-germanium becomes smaller with decreasing germanium concentration (because germanium atoms are larger than silicon atoms). *See* Section III.D; EX1017-Murthy482, 1:46-48 (difference between lattice constant of SiGe and that of Si varies depending on the Ge percentage); EX1027-Dismukes, Fig. 3 (plotting this relationship). EX1003-Lee-Decl., ¶97.

4. Claim 4: “The semiconductor structure of claim 3, wherein the first strained layer comprises SiGe”

Koontz teaches claim 4 for the reasons in Sections VI.A.1.e (Limitation [1D]) and VI.A.3 (claim 3). *See also* EX1004-Koontz, ¶[0063] (recessed structures 446—the “first strained layer”—are “comprised of a compressive strain-producing material, such as silicon-germanium”). EX1003-Lee-Decl., ¶98.

5. Claim 5: “The semiconductor structure of claim 1, wherein the first conductivity type is N-type, and the lattice parameter of a portion of the first strained layer near the bottom of the first opening is larger than the lattice parameter of a portion of the first strained layer apart from the bottom of the first opening”

Claim 5 describes a strained layer transistor structure in which the atoms at the bottom of the structure are spaced further apart than atoms elsewhere in the structure (i.e., the portion of the strained layer at the bottom of the strained layer has a larger “lattice parameter” than portions of the strained layer that are not near the bottom—the opposite relationship of claim 3. Koontz discloses claim 5. For example, as explained above for Limitation [1D], when the first conductivity type is n-type, recess structures 441 are formed using silicon-carbon where the amount of carbon relative to silicon becomes smaller closer to the bottom of recess structures 441. EX1004-Koontz, ¶[0059]. A POSITA would have understood the lattice parameter in silicon-carbon becomes larger with decreasing carbon concentration and is thus larger closer to the bottom of recess structures 441. *See* Section III.D; EX1017-Murthy482, 1:46-48; EX1027-Dismukes, Fig. 3, Tbl. IV. EX1003-Lee-Decl., ¶¶99-100.

6. Claim 6: “The semiconductor structure of claim 5, wherein the first strained layer comprises SiC”

Koontz teaches claim 6 for the reasons in Sections VI.A.1.e (Limitation [1D]) and VI.A.5 (claim 5). *See also* EX1004-Koontz, ¶[0059] (recessed structures 441—

the “first strained layer”—are “comprised of a tensile strain producing material, such as silicon-carbon”). EX1003-Lee-Decl., ¶101.

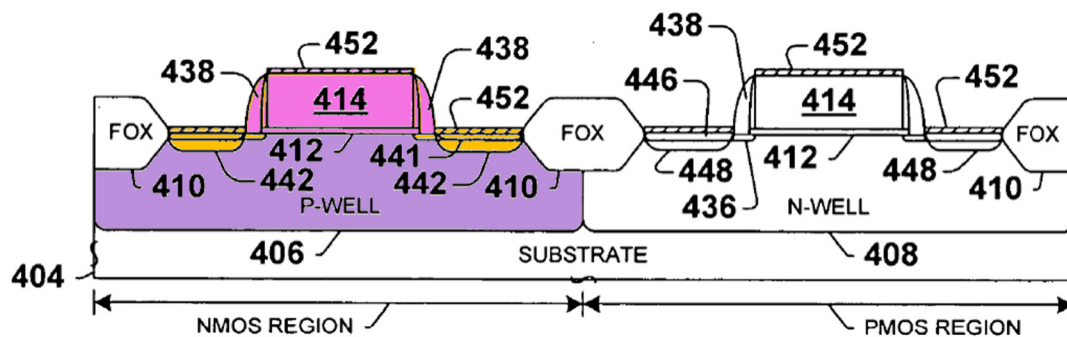
7. Claim 7

a. [7Pre]: “The semiconductor structure of claim 1”

Claim 7 depends from claim 1, which Koontz teaches. Section VI.A.1. EX1003-Lee-Decl., ¶102.

b. [7A]: “the second MOS transistor comprises: a second gate structure on the first well”

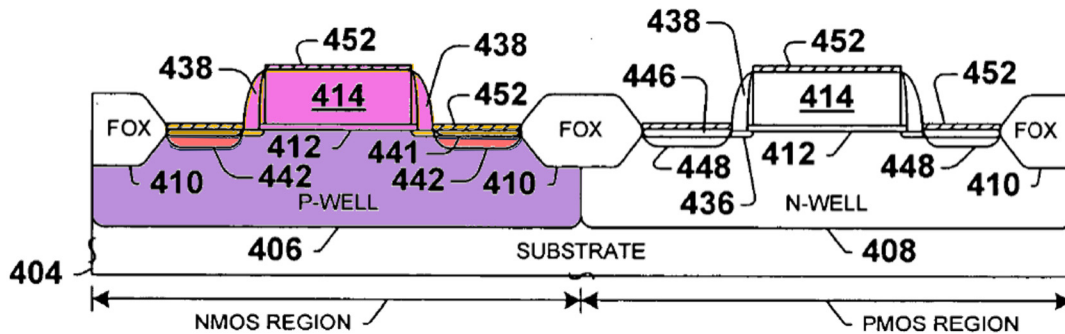
Referring to Figure 4N, Koontz teaches a second **gate structure** (e.g., gate electrode 414 overlying the gate oxide 412 together with sidewall spacers 438) on **P-well 406**.



EX1004-Koontz, Fig. 4N; *see also id.*, ¶¶[0053]-[0066]. EX1003-Lee-Decl., ¶¶103-104.

- c. [7B]: “the second MOS transistor comprises: ... a source/drain region of the second conductivity type in the first well beside the second gate structure”

Referring to Figure 4N, Koontz teaches that the second MOS transistor (e.g., NMOS transistor) comprises a source/drain region (e.g., source and drain regions 442) of the second conductivity type (e.g., n-type) beside the second gate structure.



EX1004-Koontz, Fig. 4N. For example, Koontz teaches that “[s]ource and drain regions 442 are formed in the NMOS region by implanting a suitable n-type dopant.... [and] are self-aligned with respect to the sidewall spacers 438” of the gate structure. EX1004-Koontz, Fig. 4N, ¶[0061]. EX1003-Lee-Decl., ¶¶105-106.

8. Claim 9

- a. [9Pre]: “The semiconductor structure of claim 1”

Claim 9 depends from claim 1, which Koontz teaches. Section VI.A.1. EX1003-Lee-Decl., ¶107.

b. [9A]: “the second MOS transistor comprises: a second gate structure on the first well”

As explained above for limitation [7A] (Section VI.A.7.b), which recites identical limitations, Koontz discloses these limitations. EX1003-Lee-Decl., ¶108.

c. [9B]: “the second MOS transistor comprises: ... a source/drain region of the second conductivity type around and under a second opening in the first well beside the second gate structure”

As explained above for Limitation [7B] (Section VI.A.7.c), Koontz teaches that the second MOS transistor (e.g., NMOS transistor) comprises a source/drain region (e.g., source and drain regions 442) of the second conductivity type (e.g., n-type). The source/drain region is around and under a second opening in the first well (e.g., recessed regions 440 shown in Figure 4H) beside the second gate structure. EX1003-Lee-Decl., ¶¶109-110.

9. Claim 11

a. [11Pre]: “The semiconductor structure of claim 1”

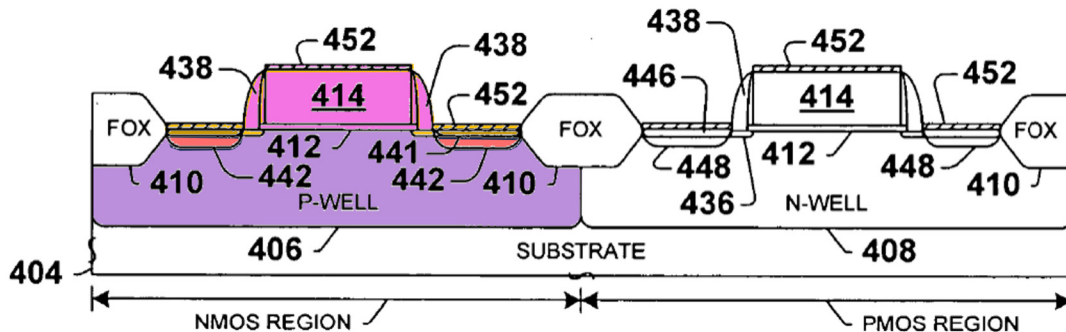
Claim 11 depends from claim 1, which Koontz teaches. Section VI.A.1. EX1003-Lee-Decl., ¶111.

b. [11A]: “the second MOS transistor comprises: a second gate structure on the first well”

As explained above for limitation [7A] (Section VI.A.7.b), which recites identical limitations, Koontz discloses these limitations. EX1003-Lee-Decl., ¶112.

- c. [11B]: “the second MOS transistor comprises: ... a second strained layer of the second conductivity type in a second opening in the first well beside the second gate structure”

Referring to Figure 4N, Koontz teaches that the second MOS transistor (e.g., NMOS transistor) comprises a second strained layer (e.g., recess structures 441) of the second conductivity type (e.g., n-type) in a second opening in the first well (e.g., P-Well 406) beside the second gate structure.



EX1004-Koontz, Fig. 4N. For example, Koontz teaches that “recess structures 441 [are] comprised of a tensile strain producing material [and] are formed in the NMOS recessed region” within P-Well 406. *Id.*, ¶[0059]. EX1003-Lee-Decl., ¶¶113-115.

As explained in Section VI.A.1.e, Koontz teachings regarding the “first strained layer” equally apply when the conductivity type is reversed. Thus, Koontz teachings regarding the “first strained layer” of the “first conductivity type” equally applies to the “second strained layer” of the “second conductivity type.” EX1003-Lee-Decl., ¶¶115.

10. Claim 12

a. [12Pre]: “The semiconductor structure of claim 11”

Claim 12 depends from claim 11, which Koontz teaches. Section VI.E.8. EX1003-Lee-Decl., ¶116.

b. [12A]: “a difference between a lattice parameter of a portion of the second strained layer near a bottom of the second opening and the lattice parameter of the substrate is smaller than a difference between a lattice parameter of a portion of the second strained layer apart from the bottom of the second opening and the lattice parameter of the substrate”

Limitation [12A] applies the same non-uniform lattice parameter limitations as Limitation [1D] to the second strained layer of Limitation [11B]. As explained for Limitation [1D], Koontz teaches that both strained layers, including the second (NMOS) strained layer, satisfy the non-uniform lattice parameter limitations. Accordingly, Koontz teaches element [12A] for the reasons in Sections VI.A.1.e (Limitation [1D]) and VI.A.1.c (Limitation [11B]). EX1003-Lee-Decl., ¶117.

- c. **[12B]: “when the first conductivity type is P-type and the second conductivity type is N-type, the lattice parameter of a portion of the first strained layer near the bottom of the first opening is smaller than the lattice parameter of a portion of the first strained layer apart from the bottom of the first opening, but the lattice parameter of a portion of the second strained layer near the bottom of the second opening is larger than the lattice parameter of a portion of the second strained layer apart from the bottom of the second opening”**

Limitation [12B] recites the same limitations as Claims 3 and 5 (Sections VI.A.3 and VI.D.5) in a configuration where the first conductivity type is P-type and the second conductivity type is N-type. Therefore, Koontz satisfies element [12B] for the reasons set forth above. *See also* Sections VI.A.1.e (Limitation [1D]), VI.A.9.c (Limitation [11B]) (symmetry with respect to which conductivity type is “first”). EX1003-Lee-Decl., ¶118.

- d. **[12C]: “when the first conductivity type is N-type and the second conductivity type is P-type, the lattice parameter of a portion of the first strained layer near the bottom of the first opening is larger than the lattice parameter of a portion of the first strained layer apart from the bottom of the first opening, but the lattice parameter of a portion of the second strained layer near the bottom of the second opening is smaller than the lattice parameter of a portion of the second strained layer apart from the bottom of the second opening”**

Limitation [12C] recites the same limitations as Claims 3 and 5 (Sections VI.A.3 and VI.D.5) in a configuration where the first conductivity type is N-type and the second conductivity type is P-type. Therefore, Koontz satisfies element

[12B] for the reasons set forth above. *See also* Sections VI.A.1.e (Limitation [1D]), VI.A.9.c (Limitation [11B]). EX1003-Lee-Decl., ¶119.

11. Claim 13: “The semiconductor structure of claim 12, wherein the lattice parameter of the second strained layer has a gradient distribution”

Claim 13 applies the same gradient distribution limitations as claim 2 to the second strained layer of Limitation [11B]. As explained for Limitation [1D], Koontz teaches that both strained layers, including the second (NMOS) strained layer, satisfy the gradient distributions limitations. Accordingly, Koontz teaches Claim 13 for the reasons in Sections VI.A.1.e (Limitation [1D]), VI.A.2 (Claim 2), and VI.A.8.c (Limitation [11B]). Koontz teachings regarding the “first strained layer” equally apply when the conductivity type is reversed. Thus, Koontz teachings regarding the “first strained layer” having a “gradient distribution” equally applies to the “second strained layer.” EX1003-Lee-Decl., ¶¶120-121.

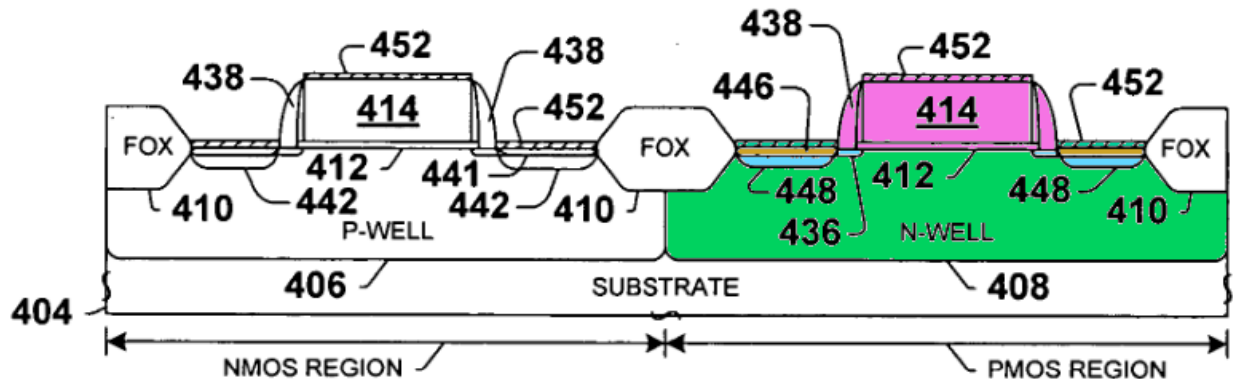
B. Ground 1B: Koontz In View of Sridhar Renders Obvious Claims 8, 10 and 14

Claims 8, 10, and 14 recite a “metal silicide layer.” A silicide layer refers to a layer of silicon combined with a more electropositive element, usually metal. Ex. 1003-Lee-Decl., ¶¶41-42. To the extent PO argues that Koontz does not teach the silicide limitations, Koontz-Sridhar renders these limitations obvious.

1. Koontz-Sridhar

(1) *Koontz*

As shown in Figure 4N, Koontz discloses forming silicide regions 452 over filled recess structures 446.

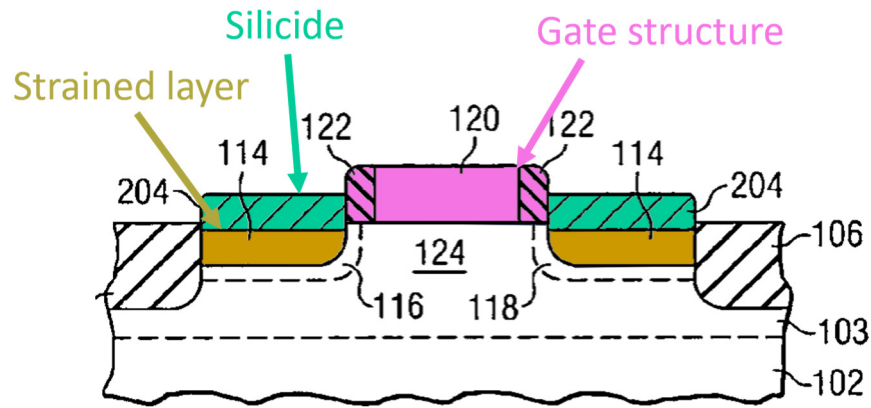


EX1004-Koontz, Fig. 4N; *see also id.*, ¶[0066]. Koontz discloses that the silicide regions 452 are formed using “a suitable silicidation process.” EX1004-Koontz, ¶[0066]; EX1003-Lee-Decl., ¶124.

(2) *Sridhar*

Sridhar discloses such a silicidation process—specifically, a technique for forming a silicide layer that includes forming a silicon layer on the strained layer. Referring to Figure 1D below, Sridhar discloses a MOS device (e.g., NMOS or PMOS transistor) with a gate structure. EX1007-Sridhar, ¶¶[0010]-[0013], Fig. 1D. Like Koontz, Sridhar discloses forming a strained layer beside the gate structure.

Id., ¶¶[0003], [0014]. Also like Koontz, Sridhar discloses forming a **silicide layer**⁴ on the **strained layer**.



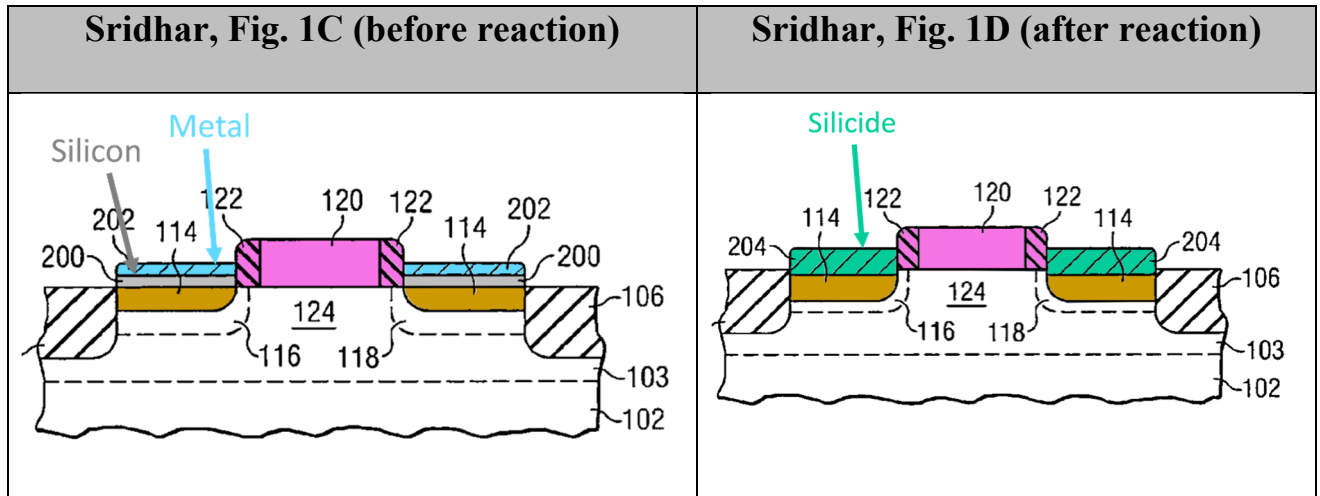
EX1007-Sridhar, Fig. 1D; *see also id.* ¶¶[0004], [0014]-[0017], Fig. 1C. EX1003-Lee-Decl., ¶125.

Sridhar provides examples of “a suitable silicidation process” to form the **silicide layer** of the sort described in Koontz. EX1004-Koontz, ¶[0066]. For example, Sridhar teaches forming the **silicide layer** by first depositing a **silicon layer** on the **strained layer** (e.g., source/drain regions 114). EX1007-Sridhar, ¶[0015],

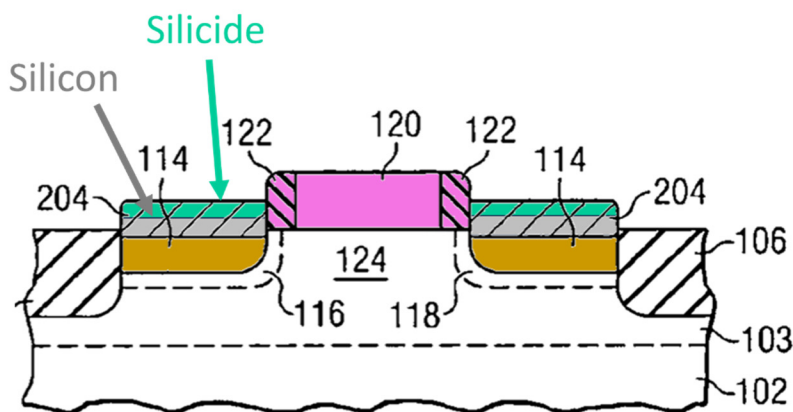
⁴ Sridhar uses the terms “silicide” and “salicide” layer interchangeably. *Compare* EX1007-Sridhar, ¶¶[0004], Claims 1-2, 4, and 12 (“silicide”) *with id.*, ¶¶[0016]-[0017] (“salicide”). This usage is consistent with the understanding that the terms “salicide” or “salicidation” simply refer to the process of forming a silicide.

EX1010-Quirk, 214, 311-12, Fig. 12.13. EX1003-Lee-Decl., ¶123.

Fig. 1B. Then, a **metal layer 202** is deposited and reacted with the **silicon layer** to form the **silicide layer** (e.g., “silicide layer 204”). *Id.* ¶[0016], Figs. 1C, 1D.



EX1007-Sridhar, Figs. 1C, 1D. Although Figure 1D illustrates an embodiment in which the **silicide layer** has reacted with “all of silicon layer 200,” such that silicon layer 200 is no longer visible, Sridhar expressly discloses embodiments in which the **silicide layer** “react[s] with *only a portion* of silicon layer 200.” *Id.*, ¶[0017] (emphasis added). In these embodiments, it is readily apparent that a portion of silicon layer 200 would remain on the **strained layer** following the reaction, as illustrated below.



EX1007-Sridhar, Fig. 1D (annotated to illustrate the effect of replacing silicide layer 204 with a modified silicide layer that overlies a partially consumed silicon cap, as disclosed by Sridhar's alternate embodiments). EX1003-Lee-Decl., ¶¶126-127.

(3) Motivation to combine

As explained above, Koontz teaches a semiconductor structure with a silicide layer (silicide regions 452) on a strained layer (e.g., filled recess structures 446). EX1004-Koontz, ¶[0066], Fig. 4N. Sridhar teaches a technique for forming a silicide layer that includes forming a silicon layer on a strained layer, where a portion of the silicon layer remains on the strained layer following the formation of the silicide layer. A POSITA would have been motivated to combine these teachings

with a reasonable expectation of success for the following reasons.⁵ EX1003-Lee-Decl., ¶128.

First, Koontz states that its silicide layer should be formed “by a suitable silicidation process,” thereby motivating a POSITA to seek out teachings regarding such processes. EX1004-Koontz, ¶[0066]. EX1003-Lee-Decl., ¶129.

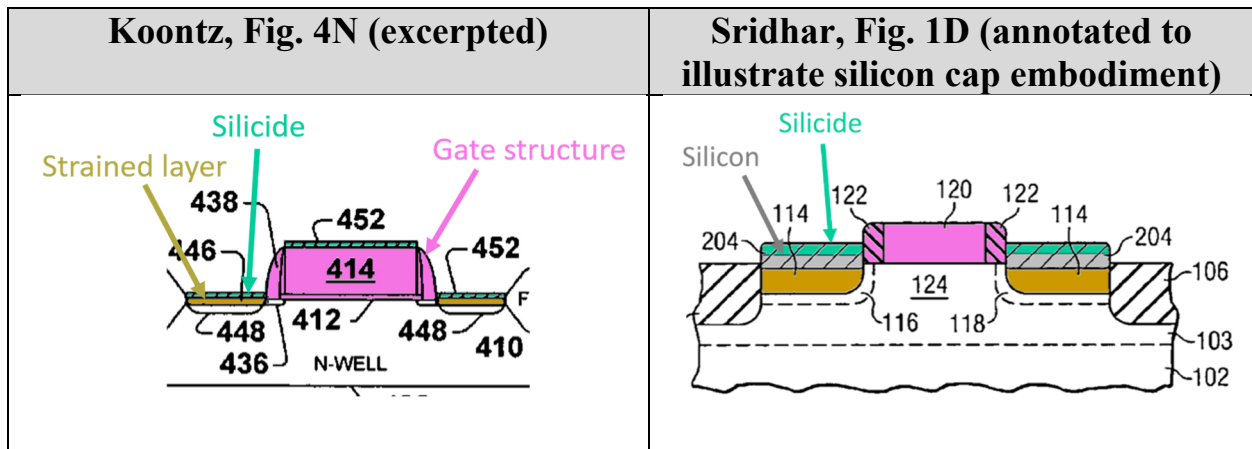
Second, a POSITA would have had an express motivation to turn to Sridhar because Sridhar discloses the benefits of its techniques. For example, Sridhar explains that forming a silicide layer directly on the strained layer (i.e., with no silicon layer in between) may degrade the electrical performance of the transistor. EX1007-Sridhar, ¶[0003] (forming the silicide layer directly on the strained layer “may counteract the benefits [of a strained channel] by increasing source/drain resistances”). To address this issue, Sridhar teaches that it would be beneficial to add a thin silicon layer between the strained layer and the silicide layer. *Id.*, ¶¶[0005], [0015]. This approach desirably “decreases the source/drain resistances

⁵ As explained in Section V, Koontz and Sridhar are in the same field as the ’822 patent and are reasonably pertinent to solving the problems addressed in the ’822 patent (e.g., forming strained channel MOSFETs) and are therefore analogous art to the ’822 patent. *See Corephotonics, Ltd. v. Apple Inc.*, 84 F.4th 990, 1004 (Fed. Cir. 2023).

that would have occurred if [the silicide layer had been formed] directly over [the strained] layers....” *Id.*, ¶[0015]; *see also id.* ¶[0005]. Koontz likewise itself identifies “reduc[ing] contact resistance between active regions and electrodes” as a desirable objective. EX1004-Koontz, ¶[0066]. Other benefits to preserving a portion of the silicon layer, such as improved robustness to process variations, prevention of strain relaxation, and more uniform silicidation, would have been readily apparent to a POSITA. A POSITA would therefore have been motivated to arrive at a silicon layer on the first strained layer in view of Koontz’s teachings of a semiconductor structure and Sridhar’s teachings of a silicon layer between the strained layer and the silicide layer, to obtain these known benefits. EX1003-Lee-Decl., ¶¶130-134.

Third, Koontz and Sridhar each describe similar semiconductor structures (and techniques for forming such structures) such that their combination would have yielded predictable results. For example, Koontz discloses “semiconductor device fabrication by tailoring a vertical channel strain profile by selecting and controlling composition of strain inducing materials... such as silicon-carbon and silicon-germanium.” EX1004-Koontz, ¶[0018]. Koontz’s process “can be applied to NMOS and/or PMOS devices.” *Id.*, ¶[0029]. Similarly, Sridhar discloses techniques for fabricating NMOS and PMOS transistors that includes “forming a silicon-germanium layer in each of the source and drain regions.” EX1007-Sridhar,

¶[0004]; *see also id.* ¶¶[0001], [0010]. In fact, Sridhar states that its technique for forming a silicon layer on the strained layer “may be implemented as a drop-in” solution that is integrated into existing processing technologies like those used by Koontz. *Id.*, ¶[0017]; *see also id.*, ¶[0005]. The similar physical and functional characteristics are illustrated below:



Thus, Koontz and Sridhar each share similar objectives and means for accomplishing those objectives, indicating that their combination would have been straightforward and yielded predictable results. EX1003-Lee-Decl., ¶¶135-137.

Fourth, a POSITA would have had a reasonable expectation of success in applying Sridhar’s teachings to Koontz given that, as explained above, Sridhar expressly discloses that its techniques are compatible with existing semiconductor processing technologies like those used by Koontz. Moreover, in the combination, the known semiconductor structures and processing techniques of Sridhar would have been used to improve Koontz’s similar semiconductor structure in the same way. For example, Koontz discloses a semiconductor structure having a silicide

layer on a strained layer, EX1004-Koontz, ¶[0066], Fig. 4N, and Sridhar discloses a way to form the silicide layer in a manner that improves its electrical characteristics (e.g., by forming a silicon layer on the strained layer that is partially consumed when forming the silicide layer). Thus, Sridhar’s teachings would have been applied to Koontz in the same way that those teachings are used in Sridhar itself. EX1003-Lee-Decl., ¶138.

Finally, it would have been obvious to apply Sridhar’s teachings as described above to PMOS and/or NMOS transistors as taught by Koontz, as Sridhar expressly discloses that its teachings are applicable to “NMOS, PMOS, CMOS, or other suitable semiconductor device.” EX1007-Sridhar, ¶[0010]; *see also* EX1004-Koontz, ¶[0063]. EX1003-Lee-Decl., ¶¶139-142.

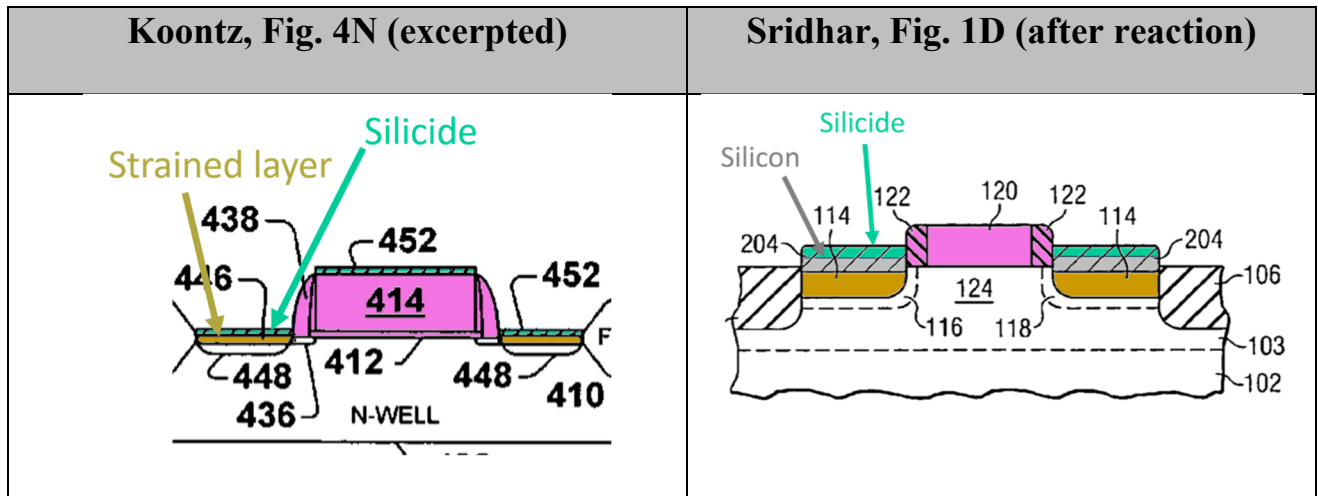
2. Claim 8

a. [8Pre]: “The semiconductor structure of claim 7, further comprising:”

Claim 8 depends from claim 7, which Koontz teaches. *See* Sections VI.A.7, VI.B.2.a. EX1003-Lee-Decl., ¶122.

b. [8A]: “a silicon layer on the first strained layer”

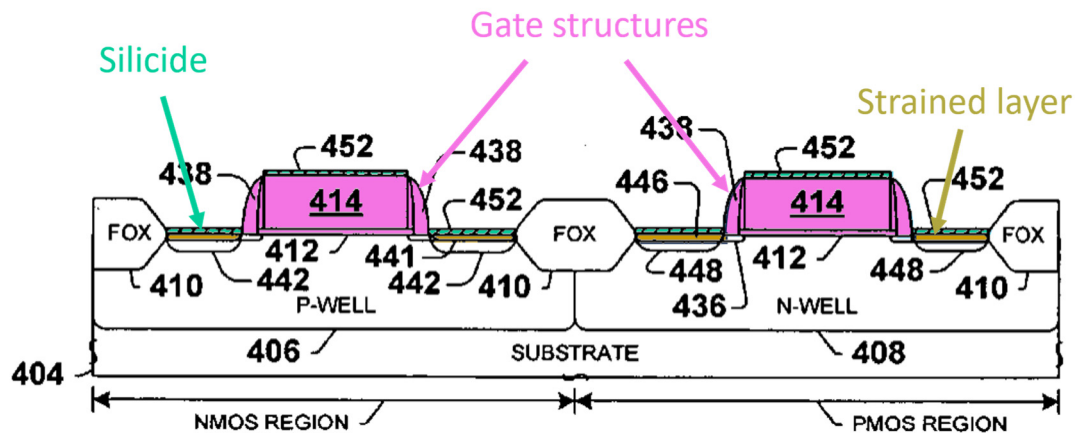
Koontz-Sridhar (*see* Section VI.B.1) includes a silicon layer (e.g., Sridhar’s partially consumed silicon layer) on the first strained layer (e.g., Koontz’s **recess structures 446**), as illustrated below.



EX1004-Koontz, Fig. 4N; EX1007-Sridhar, Fig. 1D (annotations illustrate the results of applying Sridhar’s teachings regarding a partially consumed silicon layer to the silicide layer taught by Koontz). EX1003-Lee-Decl., ¶¶124-127.

- c. [8B]: “a metal silicide layer on the silicon layer, the source/drain region and the first and the second gate structures”

As explained above for Limitation [8A], Koontz-Sridhar has a metal silicide layer (e.g., Koontz’s silicide 452 formed using the process described in Sridhar) on a silicon layer (e.g., Sridhar’s silicon layer). As shown in Figure 4N, Koontz further teaches that silicide 452 is on the source/drain region 446 and on the first and second gate structures 414.



EX1004-Koontz, Fig. 4N; *see also* Limitations [1C], [1D], [7A], [7B]; *cf.* EX1001-USP'822, 5:61-6:7, Fig. 2 (showing a silicide layer 226 located directly on silicon layers 224a and 224b and gate structures 212 and 218 and indirectly on strained layers 216 and 222). EX1003-Lee-Decl., ¶¶143-144.

3. Claim 10

Claim 10 recites the same limitations as claim 8, except it depends from claim 9 rather than claim 7. Koontz-Sridhar thus satisfies claim 10 for the reasons in Sections VI.A.8 (claim 9) and VI.B.2 (claim 8). EX1003-Lee-Decl., ¶145.

4. Claim 14

a. [14Pre]: “The semiconductor structure of claim 11”

Claim 14 depends from claim 11, which Koontz teaches. Section VI.A.9. EX1003-Lee-Decl., ¶146.

b. [14A]: “a silicon layer on the first strained layer and the second strained layer”

As explained for Limitations [1D] and [11B], Koontz-Sridhar includes first and second strained layers and, as explained above (*see* Section VI.B.1), renders obvious the formation of a silicon layer on the strained layers. EX1003-Lee-Decl., ¶147.

c. [14B]: “a metal silicide layer on the silicon layer and the first and second gate structures”

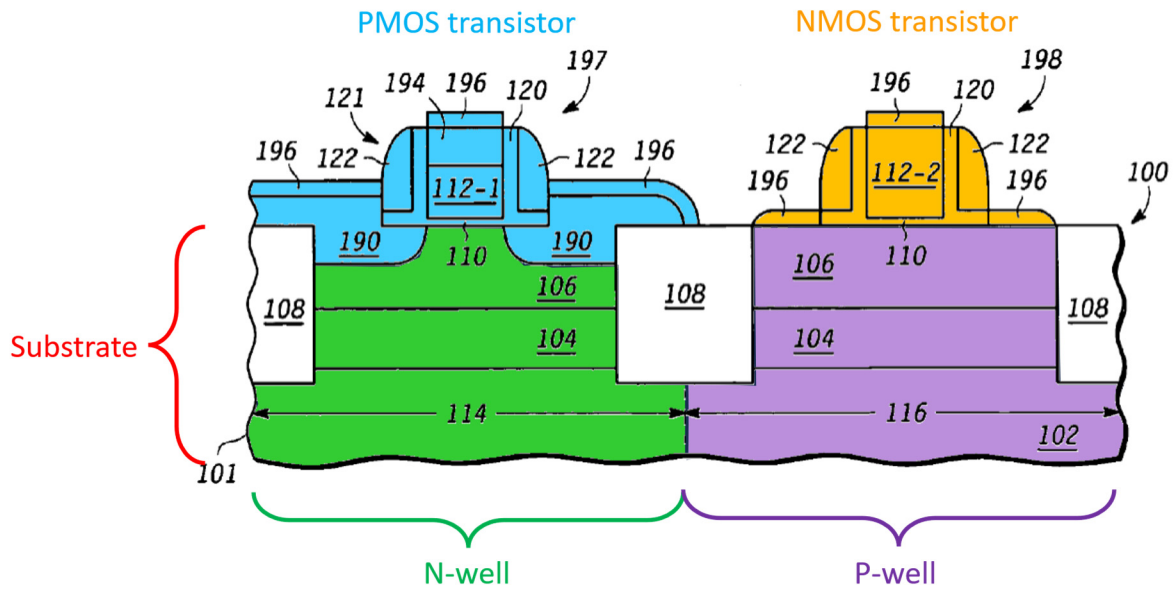
As explained above for limitation [8B] (Section VI.B.2.c), which recites overlapping limitations with an additional limitation, Koontz discloses these limitations. EX1003-Lee-Decl., ¶148.

C. Ground 2: Orlowski Anticipates Claims 1-4

1. Claim 1

a. [1Pre]: “A semiconductor structure”

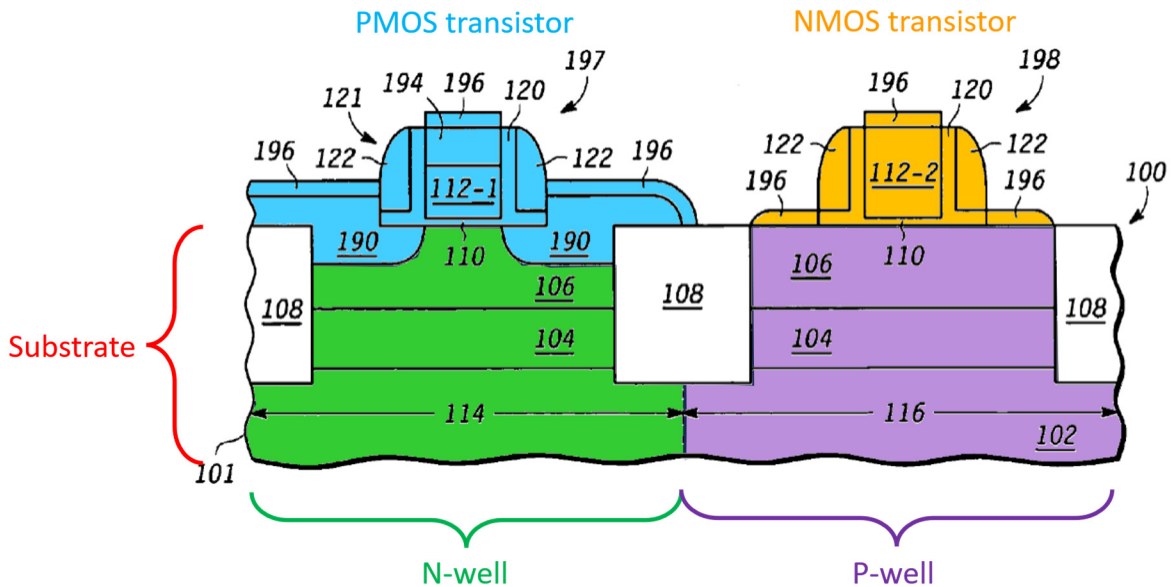
To the extent the preamble is limiting, Orlowski discloses a semiconductor structure (e.g., a CMOS integrated circuit) “having [stress-inducing source/drain] structures characterized by a composition gradient.” EX1006-Orlowski, 2:62-65; *see also id.*, Abstract, 1:35-44, 2:34-61, 3:64-4:10, 7:48-51. As shown in Figure 13, the semiconductor structure includes a substrate 101, a PMOS transistor 197 on an N-well 114, and an NMOS transistor 198 on a P-well 116.



EX1006-Orlowski, Fig. 13; *see also id.*, Fig. 8. EX1003-Lee-Decl., ¶¶150-153.

- b. [1A]: “a substrate, having therein a first well of a first conductivity type and a second well of a second conductivity type”

As shown in Figure 13, Orlowski discloses a substrate (e.g., **substrate 101**) having therein a first well (e.g., **P-well 116**) of a first conductivity type (e.g., p-type) and a second well (e.g., **N-well 114**) of second conductivity type (e.g., n-type).

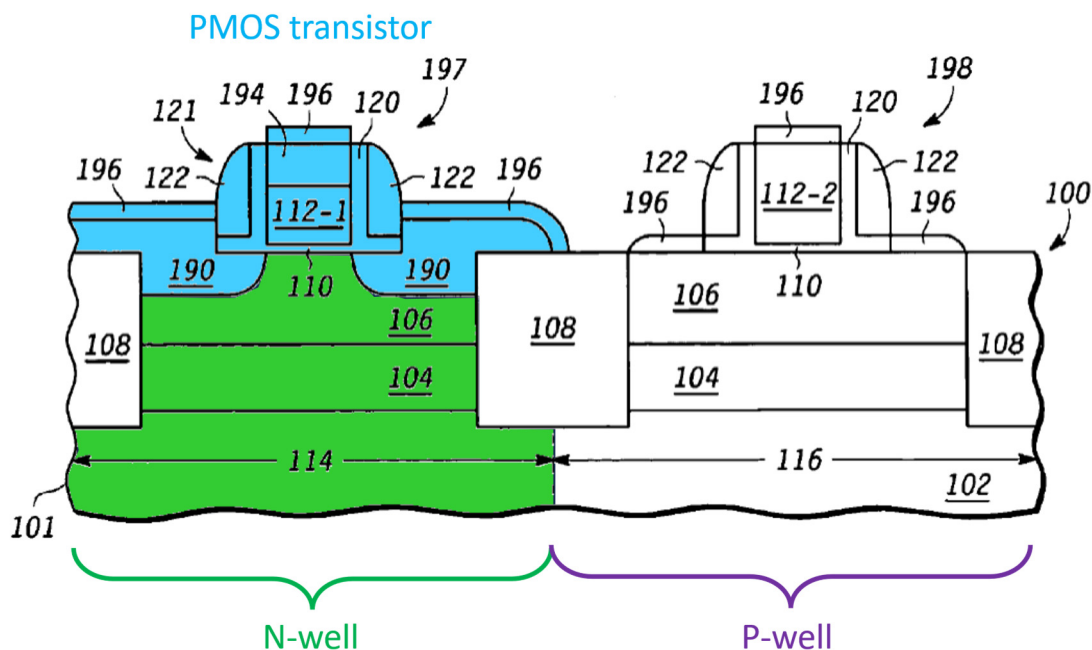


EX1006-Orlowski, Fig. 13; *see also id.*, 3:21-32 (“[S]emiconductor layer 106 in first well region 114 is n-doped (thereby making it suitable for forming PMOS transistors) while semiconductor layer 106 in second well region 116 is p-doped (thereby making it suitable for forming NMOS transistors).”). For example, Orlowski discloses that **substrate 101** can include a silicon-on-insulator (SOI) substrate or a bulk substrate. EX1006-Orlowski, 9:1-3. **P-well 116** is formed on **substrate 101** using a p-type dopant (i.e., first conductivity type) and **N-well 114** is formed using an n-type dopant (i.e., second conductivity type). *Id.*, 3:21-32.

EX1003-Lee-Decl., ¶¶154-156.

c. [1B]: “a first MOS transistor of the first conductivity type on the second well”

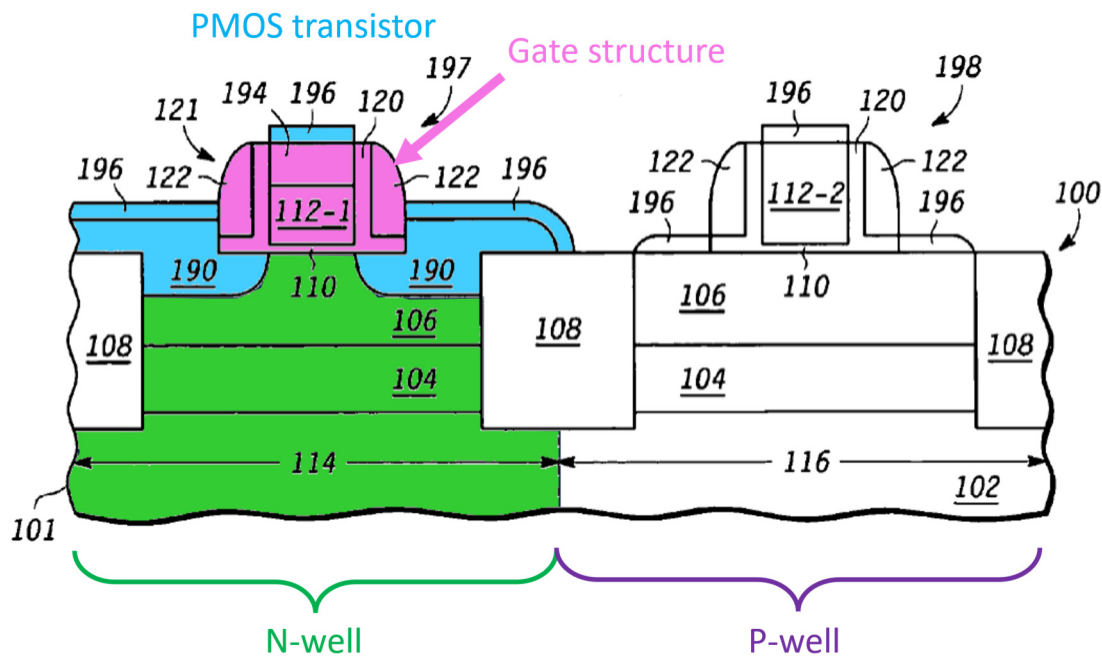
As shown in Figure 13, Orlowski discloses a first MOS transistor (e.g., PMOS transistor 197) of the first conductivity type (e.g., p-type) on the second well (e.g., N-well 114).



EX1006-Orlowski, Fig. 13; *see also id.*, 8:32-36. For example, Orlowski teaches that N-well 114 is “suitable for forming PMOS transistors” and that portions of PMOS transistor 197 “overl[ie]” N-well 114. EX1006-Orlowski, 3:21-32, 8:32-36, Fig. 13. Orlowski analogizes PMOS transistor 197 in Figure 13 to PMOS transistor 151 in Figure 8, which is similarly described as a PMOS transistor that overlies N-well 114. *Id.*, 7:15-19, 7:35-37, 8:32-36. EX1003-Lee-Decl., ¶¶157-159.

d. [1C]: “first MOS transistor...comprising: a first gate structure on the second well”

As shown in Figure 13, Orlowski discloses that the first MOS transistor (e.g., PMOS transistor 197) comprises a first gate structure (e.g., gate structure 121) on the second well (e.g., N-well 114).

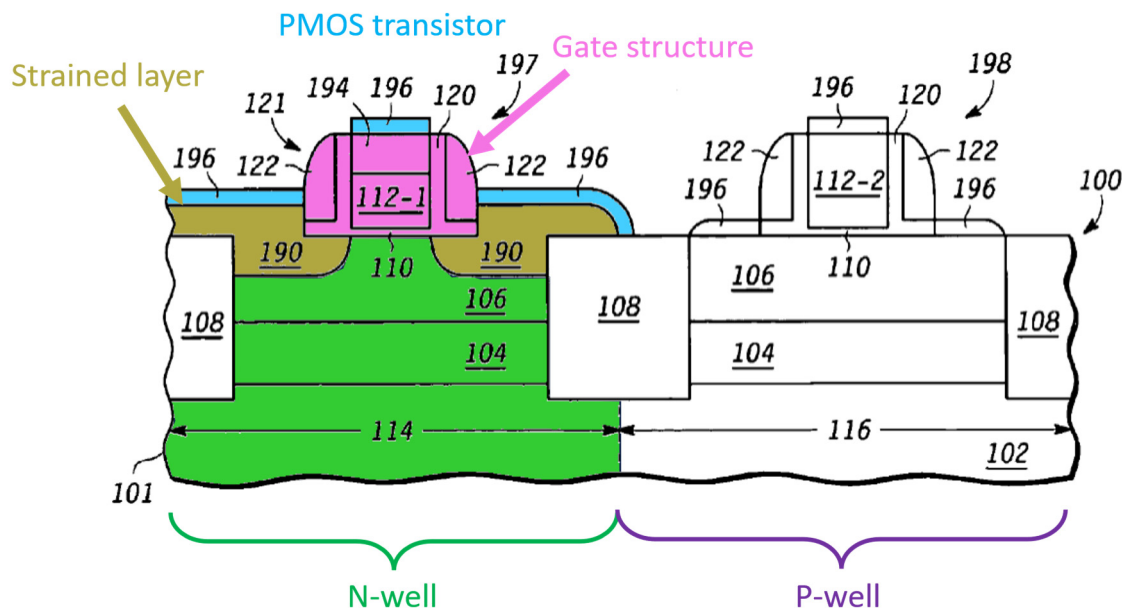


EX1006-Orlowski, Fig. 13; *see also id.*, 3:57-62, 8:32-36. For example, Orlowski teaches that “gate structure 121 overl[ies] a semiconductor layer 10[6] in [n-well] 114...” *Id.*, 8:32-36, Fig. 13. EX1003-Lee-Decl., ¶¶160-161.

- e. [1D]: “first MOS transistor...comprising:...a first strained layer of the first conductivity type in a first opening in the second well beside the first gate structure, wherein a difference between a lattice parameter of a portion of the first strained layer near a bottom of the first opening and a lattice parameter of the substrate is smaller than a difference between a lattice parameter of a portion of the first strained layer apart from the bottom of the first opening and the lattice parameter of the substrate”

“first strained layer...beside the first gate structure”

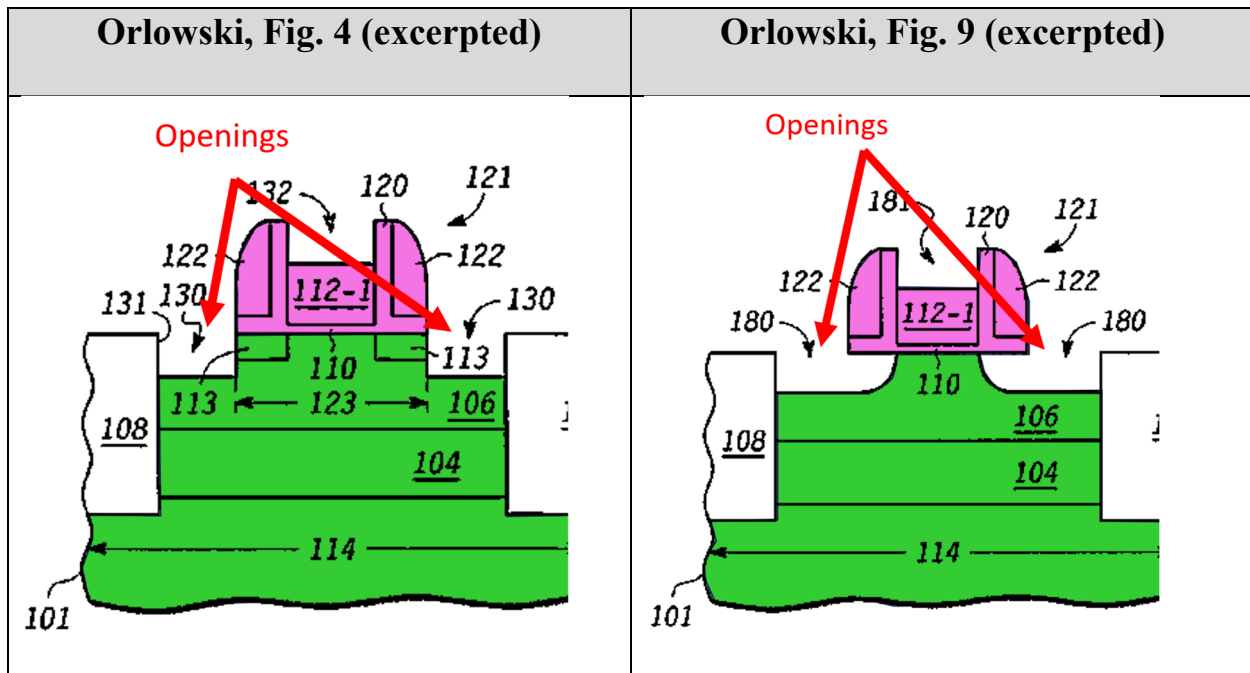
Orlowski discloses that the first MOS transistor (e.g., PMOS transistor 197) comprises a first strained layer (e.g., strain inducing source/drain structures 190) of the first conductivity type (e.g., p-type) in a first opening (e.g., source/drain recesses 180 in Fig. 9) in the second well (e.g., N-well 114) beside the first gate structure (e.g., gate structure 121) on the second well (e.g., N-well 114).



EX1006-Orlowski, Fig. 13; *see also id.*, 3:57-62, 8:32-36. For example, Orlowski teaches that **strain inducing source/drain structures 190** (the “first strained layer”) “preferably create compressive or tensile stress (depending upon the application) within the portion of semiconductor layer 106 underlying **gate structure 121**.” EX1006-Orlowski, 8:4-8; *see also id.*, 1:15-27, 8:39-41. The ’822 patent describes the “strained layer” in the same way. *See* Section VI.A.1.e (Ground 1A). EX1003-Lee-Decl., ¶¶162-163.

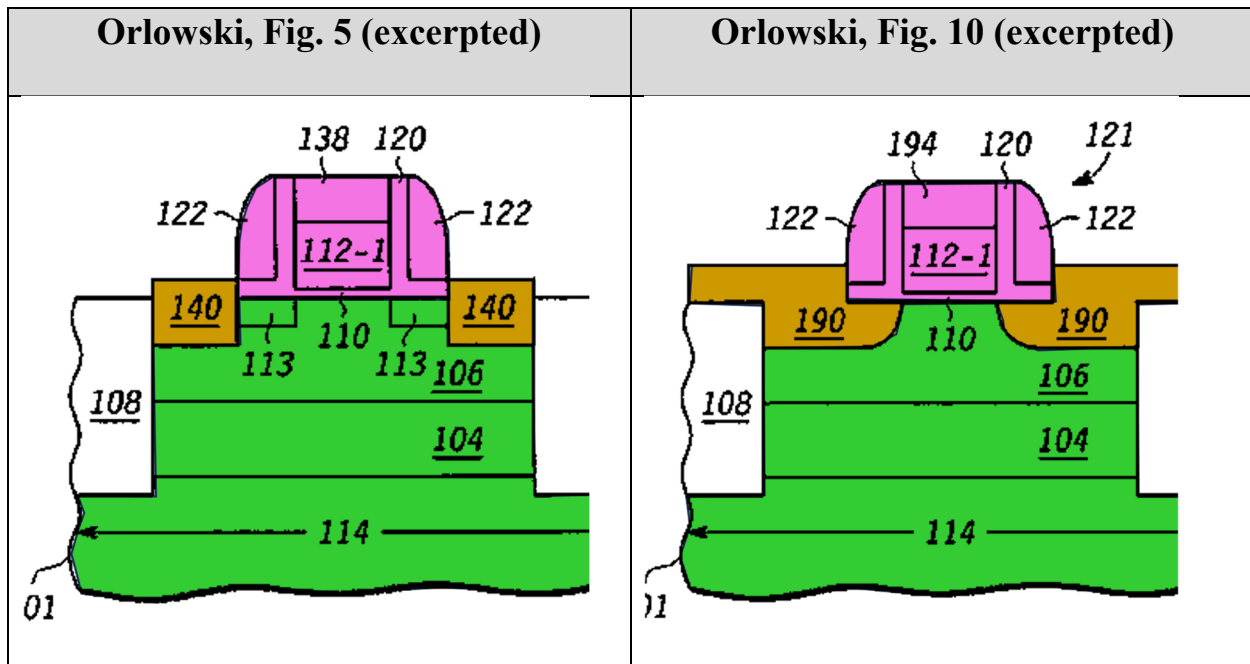
Orlowski teaches that strain inducing source/drain structures 190 (the claimed “first strained layer”) have a first conductivity type (e.g., p-type). This is achieved by introducing “a proper source/drain impurity,” i.e., a p-type dopant such as boron. EX1006-Orlowski, 8:4-56, *see also id.*, 3:38-41, 5:30-35, 6:29-38, 6:52-58. EX1003-Lee-Decl., ¶164.

Orlowski teaches that strain inducing source/drain structures 190 (the claimed “first strained layer”) are located in openings (e.g., source/drain recesses or source/drain voids 180) in **N-well 114** beside **gate structure 121**. During manufacturing, as shown in Figures 4 and 9 below, openings are formed in **N-well 114** aligned with **gate structure 121**. Depending on the method used to form the openings, the openings may undercut **gate structure 121** as shown in Figure 9 or may open straight downward into substrate 101 as shown in Figure 4. EX1006-Orlowski, 7:53-64, 4:30-38. In either case, the openings are located beside **gate structure 121**.



EX1006-Orlowski, Fig. 4 (excerpted), Fig. 9 (excerpted). EX1003-Lee-Decl., ¶165.

Next, as shown in Figures 5 and 10 below, Orlowski teaches that the openings are “filled with” the **strain inducing source/drain structures**. EX1006-Orlowski, 8:3-4, 4:58-61. Thus, Orlowski teaches multiple embodiments for forming a **strained layer** beside a **gate structure**.



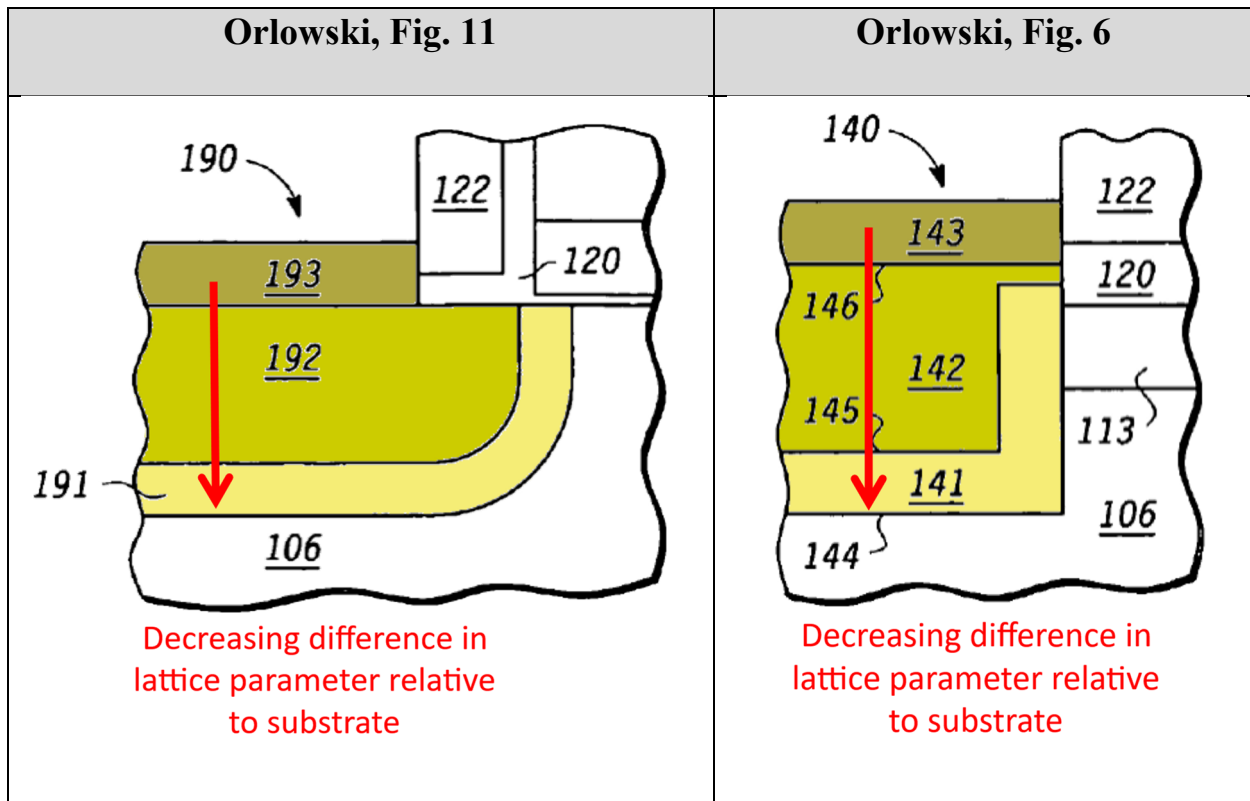
EX1003-Lee-Decl., ¶166.

Strained Layer Has Non-Uniform Lattice Parameter in Opening Next to Gate

As explained in Section VI.A.1.e (Ground 1A), this limitation requires that the strained layer next to the gate has a non-uniform lattice parameter. Orlowski discloses this limitation. For example, Orlowski teaches that, for a PMOS transistor (e.g., PMOS transistor 197), strain inducing source/drain structures 190 are formed using a “graded composition” of silicon-germanium. EX1006-Orlowski, 8:10-21, 6:18-28; *see also id.*, Abstract, 1:8-11, 2:40-61, 2:62-65 (source/drain structures 190 are “characterized by a composition gradient”), 5:4-29, 5:41-56, 7:35-38, 8:45-53, claims 1, 4, 7, 10, 11, 13, 14, 16. That is, the composition of silicon relative to germanium varies in the vertical direction such that “the percentage of silicon in SISD structure[] 190 decrease[s] from the bottom of SISD structures 190 to the top.”

Id., 8:41-45; *see also id.*, 7:22-28. Accordingly, the closer one gets to the bottom of the of strain inducing source/drain structures 190, the closer the composition of the silicon-germanium mixture gets to the composition of substrate 101 (where the percentage is close to 100% silicon). In turn, the closer the composition of the silicon-germanium to that of the substrate, the closer the lattice parameter of the silicon-germanium to that of the substrate—that is, a smaller difference between the lattice parameter of strain inducing source/drain structures 190 and the lattice parameter of substrate 101. *See, e.g.*, EX1006-Orlowski, 2:37-40, 5:4-29; *see also* Section VI.A.1.e. EX1003-Lee-Decl., ¶¶167-168.

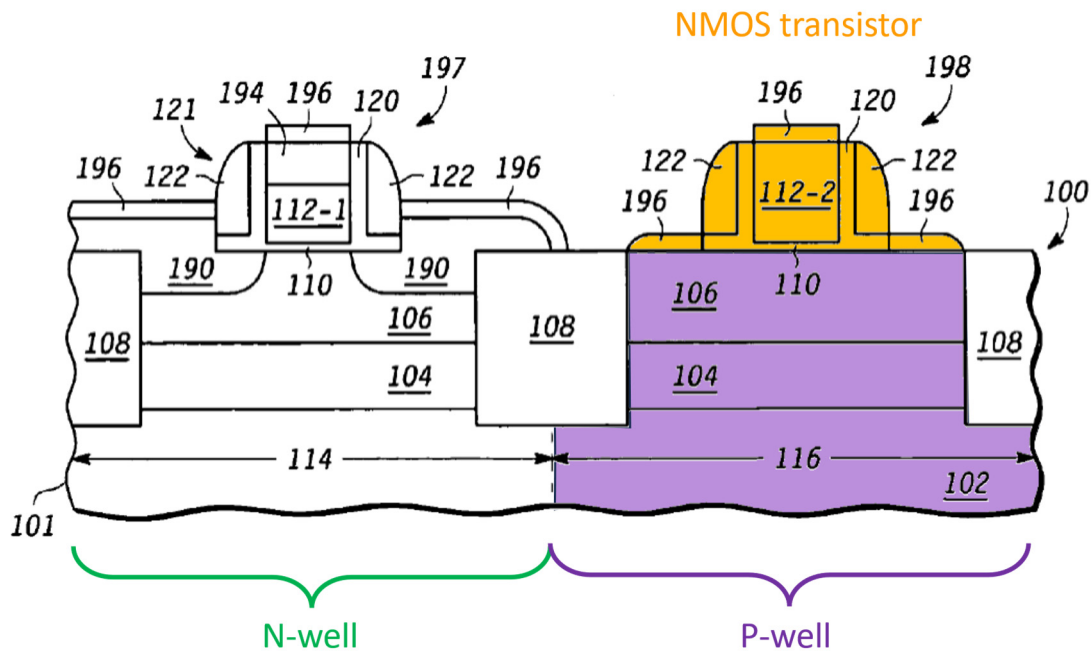
Figures 11 (left) and 6 (right) illustrate embodiments of the graded composition of Figures 10 and 5, respectively, where the difference in lattice parameter becomes smaller near the bottom of the respective **strain inducing source/drain structures**.



EX1006-Orlowski, Fig. 11, Fig. 6, 8:17-21 (“In this embodiment, the silicon percentage of SISD structure 190 is greater in first layer 191 than in second layer 192 and the silicon percentage in second layer 192 is greater than the silicon layer in third layer 193.”); 5:63-6:28, 2:17-18, 2:1-3. EX1003-Lee-Decl., ¶169.

f. [1E]: “a second MOS transistor of the second conductivity type on the first well”

As shown in Figure 13, Orlowski discloses a second MOS transistor (e.g., NMOS transistor 198) of the second conductivity type (e.g., n-type) on the first well (e.g., P-well 116).



EX1006-Orlowski, Fig. 13; *see also id.*, 8:32-36. For example, Orlowski teaches that P-well 116 is “suitable for forming NMOS transistors” and portions of NMOS transistor 198 are depicted overlying P-well 116. *Id.*, 3:21-31, 8:32-36, Fig. 13. Orlowski analogizes NMOS transistor 198 in Figure 13 to NMOS transistor 152 in Figure 8, which is similarly described and depicted as an NMOS transistor that overlies P-well 116. *Id.*, 7:15-19, 7:35-37, 8:32-36. EX1003-Lee-Decl., ¶¶170-172.

2. Claim 2: “The semiconductor structure of claim 1, wherein the lattice parameter of the first strained layer has a gradient distribution”

As explained above for Limitation [1D], Orlowski discloses that source/drain structures 190 (i.e., the “first strained layer”) have a “composition gradient,” meaning their lattice parameter has a gradient distribution. EX1006-Orlowski,

Abstract (“The SISD [stress-inducing source/drain] structure has a composition *gradient* wherein the percentage of the second element varies from the upper surface of the source/drain structure to a lower surface of the SISD structure.”), 2:62-65 (source/drain structures 190 are “characterized by a composition *gradient*”); Section VI.C.1.e. EX1003-Lee-Decl., ¶¶173-174.

3. Claim 3: “The semiconductor structure of claim 1, wherein the first conductivity type is P-type, and the lattice parameter of a portion of the first strained layer near the bottom of the first opening is smaller than the lattice parameter of a portion of the first strained layer apart from the bottom of the first opening”

As explained for Ground 1A, claim 3 describes a strained layer transistor structure in which spacing between the atoms at the bottom of the structure (measured by the “lattice parameter”) is tighter than elsewhere in the structure. Orlowski discloses claim 3. For example, as explained above for Limitation [1D], when the first conductivity type is p-type, strain inducing source/drain structures 190 are formed using silicon-germanium where the amount of germanium relative to silicon becomes smaller closer to the bottom of strain inducing source/drain structures 190. EX1006-Orlowski, Abstract, 1:8-11, 2:40-45, 5:4-29, 5:41-56, 6:22-28, 7:35-38, claims 2, 12. As explained above (*see* Sections III.D, VI.A.3), a POSITA would have understood that the lattice parameter in silicon-germanium becomes smaller with decreasing germanium concentration, i.e., toward the bottom

of the strain inducing source/drain structures 190. Orłowski thus discloses claim 3. EX1003-Lee-Decl., ¶¶175-176.

4. Claim 4: “The semiconductor structure of claim 3, wherein the first strained layer comprises SiGe”

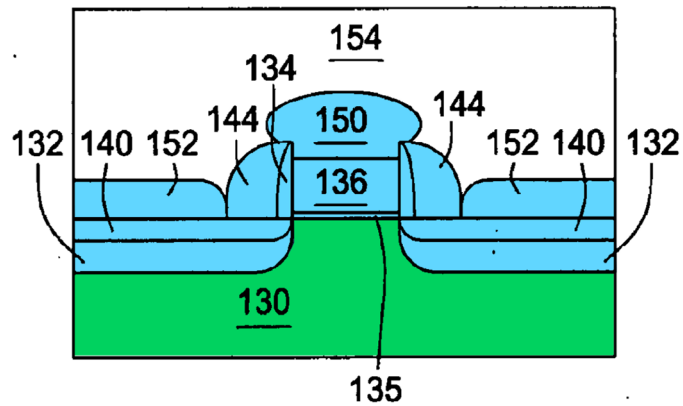
Orłowski teaches claim 4 for the reasons in Sections VI.C.1.e (Limitation [1D]) and VI.C.3 (claim 3). *See also* EX1006-Orłowski, Abstract, 1:8-11, 2:40-45, 5:4-29, 5:41-56, 6:22-28, 7:35-38, claims 2, 12. EX1003-Lee-Decl., ¶177.

D. Ground 3A: Samoilov in view of Murthy Renders Obvious Claims 1-7, 9, and 11-13

1. Samoilov-Murthy

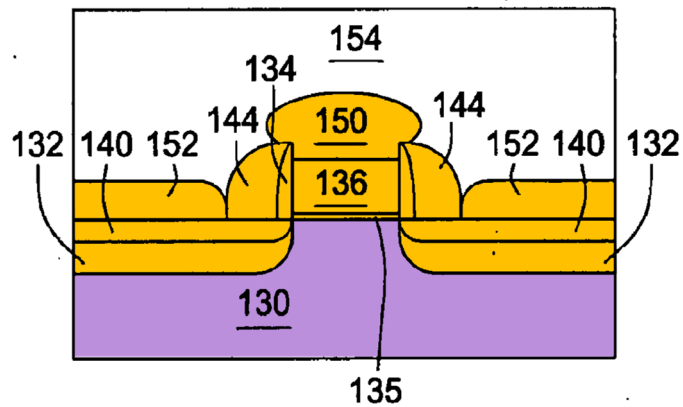
(I) Samoilov

Samoilov discloses a MOS transistor that can be configured as an NMOS or PMOS transistor by appropriately selecting the materials and conductivity types used for its components. EX1005-Samoilov, ¶¶[0009], [0021], [0027], [0029], [0038]-[0039], [0067] (“MOSFET devices formed by processes described herein may contain a PMOS component or a NMOS component.... [F]or example, a silicon-containing material such as SiGe may be deposited in a recessed area to form a PMOS component... SiC may be deposited in a recessed area to form a NMOS component.”). The PMOS configuration – which includes a **PMOS transistor** on an **n-type substrate 130** – is illustrated below.



EX1005-Samoilov, Fig. 2F; *see also id.*, ¶¶[0009], [0027], [0029], [0038]-[0039], [0067]-[0068]. EX1003-Lee-Decl., ¶¶178-179.

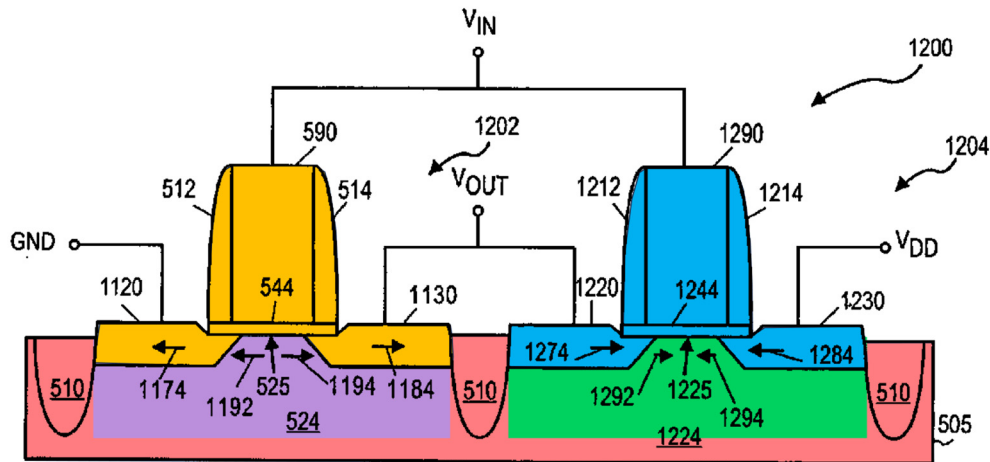
The NMOS configuration – which includes an NMOS transistor on an p-type substrate 130 – is illustrated below.



EX1005-Samoilov, Fig. 2F; *see also id.*, ¶¶[0009], [0027], [0029], [0038]-[0039], [0067]-[0068]. EX1003-Lee-Decl., ¶180.

(2) Murthy

Murthy discloses a substrate 505 with an N-well 1224 and a P-well 524 suitable for forming, respectively, PMOS and NMOS transistors like those described in Samoilov, as illustrated below.



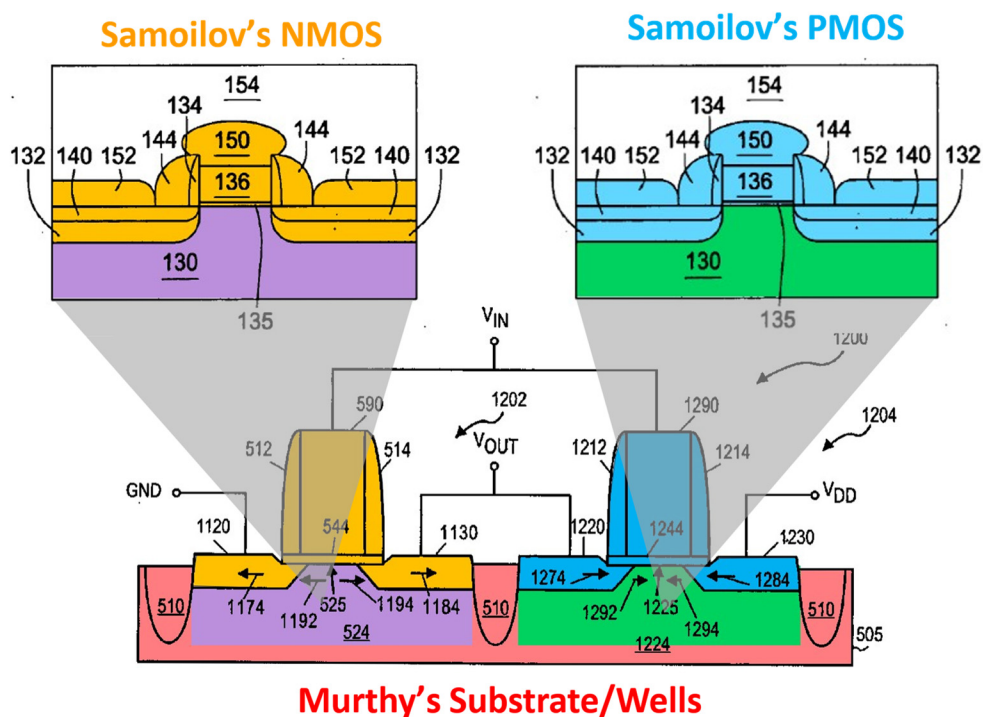
EX1011-Murthy, Fig. 12; *see also id.*, 13:50-53, 14:10-12, 23:21-54, 23:5-20.

EX1003-Lee-Dec1., ¶181.

(3) Motivation to Combine

As explained above, Samoilov teaches PMOS and NMOS transistors that are formed on n-type and p-type substrates, respectively. Murthy teaches a substrate (e.g., substrate 505) with a p-well 524 and an n-well 1124. EX1011-Murthy, Fig. 12, 13:50-53, 14:10-12, 23:21-54, 23:5-20. As illustrated below, a POSITA would have been motivated to combine these teachings by forming PMOS and NMOS transistors, as taught by Samoilov, on a twin-well structure, e.g., Murthy's n-well

1124 and p-well 524, with a reasonable expectation of success for the following reasons.⁶



EX1005-Samoilov, Fig. 2F and EX1011-Murthy, Fig. 12 (combined). EX1003-Lee-Decl., ¶182.

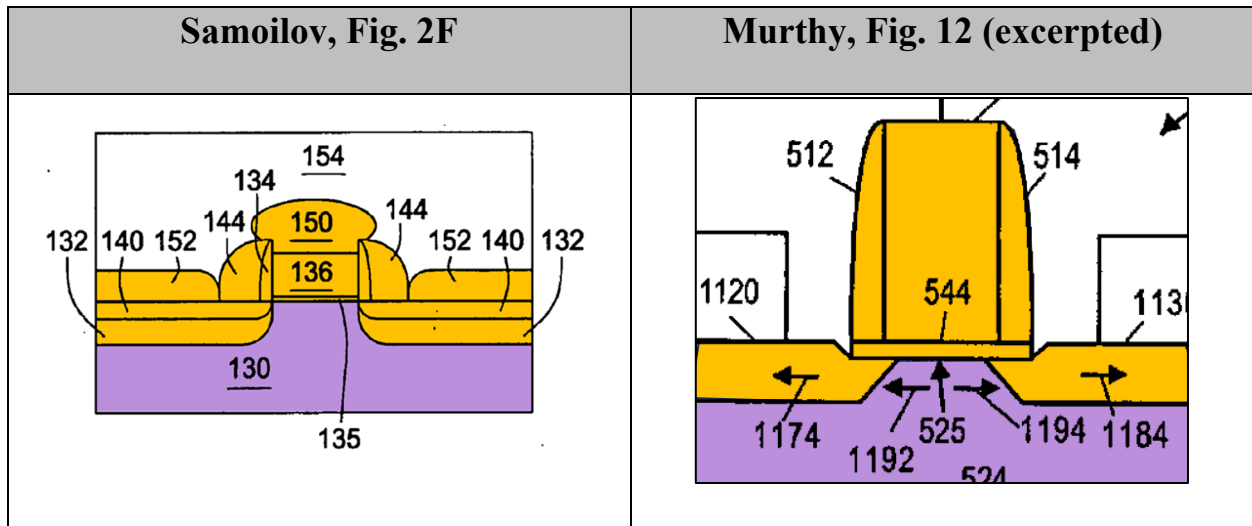
⁶ As explained in Section V, *supra*, Samoilov and Murthy are in the same field as the '822 patent and are reasonably pertinent to solving the problems addressed in the '822 patent (e.g., forming strained channel MOSFETs), and are therefore analogous art to the '822 patent. *See Corephotonics*, 84 F.4th at 1004.

First, Samoilov teaches embodiments that are implemented using “CMOS” (complementary MOS) technology. EX1005-Samoilov, ¶¶[0038]-[0039]. A POSITA would have understood that CMOS technology involves forming NMOS and PMOS devices together on the same substrate. *See, e.g.*, EX1009-Plummer, 12-13, 50-51, Figs. 1-11, 2-2; Section III.C. Moreover, a POSITA would have understood numerous benefits of using CMOS technology. For example, in many applications, compared to PMOS-only or NMOS-only circuitry, CMOS is faster, consumes less power, exhibits superior noise immunity, allows higher circuit density, and is more compatible with other digital electronic components. *See, e.g.*, EX1010-Quirk, 200. As of the ’822 patent’s filing date, CMOS technology was widely used. *Id.* Accordingly, a POSITA would have recognized the benefits of CMOS technology and been motivated to seek out references like Murthy that disclose substrates suitable this purpose. EX1003-Lee-Decl., ¶183.

Second, Murthy’s “twin-well” structure (e.g., p-well 524 paired with n-well 1124) was a well-known substrate for CMOS circuitry (as taught by Samoilov) that provides a high degree of “control[] in manufacturing.” EX1009-Plummer, 52; *see also* Section III.A; EX1010-Quirk, 205-07, Figs. 9.8-9.9; EX1004-Koontz, ¶¶[0041], [0053], Figs. 3, 4A-4N; EX1011-Murthy, 3:14-4:6, Fig. 4; EX1012-Kim, ¶[0054], Figs. 2-29; EX1013-Cook, ¶¶[0022]-[0023], Figs. 1-11. A POSITA would therefore have been motivated to combine the teachings of Samoilov and Murthy to

obtain known benefits, e.g., improved manufacturing control. EX1003-Lee-Decl., ¶184.

Third, Samoilov and Murthy each describe similar semiconductor structures (and techniques for forming such structures) such that their combination would have yielded predictable results. For example, Samoilov and Murthy each disclose MOS transistors with performance-enhancing silicon-germanium or silicon-carbon strained layers. EX1005-Samoilov, ¶¶[0009], [0027], [0029]-[0030], [0032], [0034], [0037]-[0039], [0067]-[0068]; EX1011-Murthy, 2:31-45, 21:55-65, 23:5-54, Fig 12. Consequently, Samoilov and Murthy disclose highly similar devices that are manufactured using compatible processing technology, as shown below.



EX1003-Lee-Decl., ¶185.

Fourth, a POSITA would have had a reasonable success in combining the teachings of Samoilov and Murthy. As of the '822 patent's filing date, a POSITA would have readily understood how to apply teachings regarding one type of

transistor (e.g., NMOS or PMOS) to CMOS circuits with both types. As Orlowski explains for similar teachings, “[e]xtending the depicted processing sequence to encompass the case of two types of SISD structures [(i.e., CMOS circuits comprising NMOS and PMOS transistors)] would be obvious to one skilled in the art....” EX1006-Orlowski, 4:1-10; *accord id.*, 7:40-47. Moreover, in Samoilov-Murthy, the known twin-well processing techniques of Murthy would have been used to improve Samoilov’s similar transistor structures in the same way. For example, Samoilov discloses NMOS and PMOS transistors with a strained layer for improved performance, EX1005-Samoilov, Abstract, ¶¶[0003], [0010], [0022]-[0025], and Murthy discloses a way to form such NMOS and PMOS transistors on a twin-well substrate, EX1011-Murthy, 23:21-54, 23:5-20, Fig. 12. Thus, Murthy’s teachings would have been applied to Samoilov in the same way that those teachings are used in Murthy itself. EX1003-Lee-Decl., ¶¶186-187.

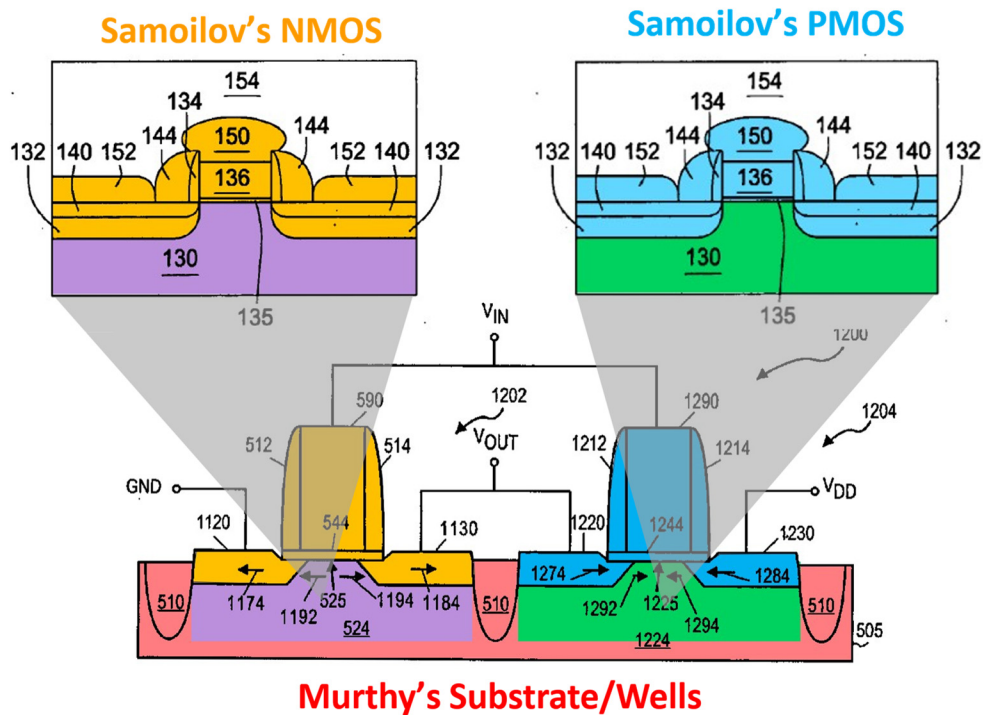
These motivations to combine the teachings Samoilov and Murthy apply to each claim limitation described below.

2. Claim 1

a. [1Pre]: “A semiconductor structure”

To the extent the preamble is limiting, Samoilov in view of Murthy teaches a semiconductor structure (e.g., strained-channel CMOS devices). As explained above (*see* Section VI.D.1), and as will be further detailed in the grounds below,

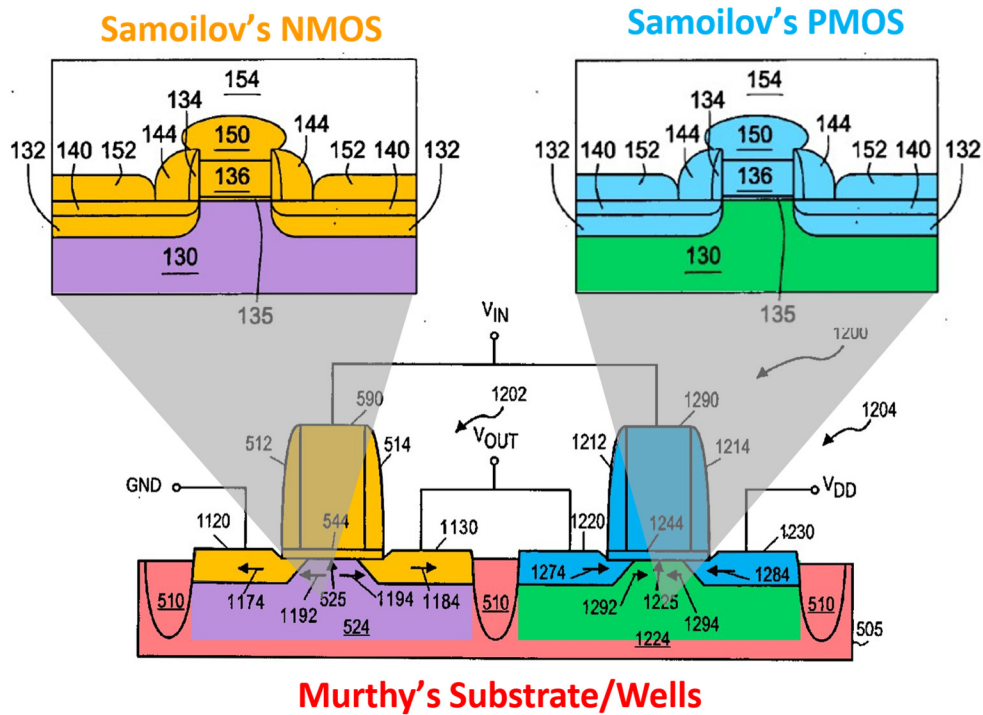
Samoilov-Murthy includes PMOS and NMOS transistors, as taught by Samoilov, on a twin-well structure, as taught by Murthy (e.g., n-well 1224 and p-well 524).



EX1005-Samoilov, Fig. 2F and EX1011-Murthy, Fig. 12 (combined). EX1003-Lee-Decl., ¶188.

- b. [1A]: “a substrate, having therein a first well of a first conductivity type and a second well of a second conductivity type”

Samoilov-Murthy (*see* Section VI.D.1) includes a substrate (e.g., Murthy's substrate 505) having therein a first well (e.g., Murthy's p-well 524) of a first conductivity type (e.g., p-type) and a second well (e.g., Murthy's n-well 1224) of a second conductivity type (e.g., n-type), as illustrated below.

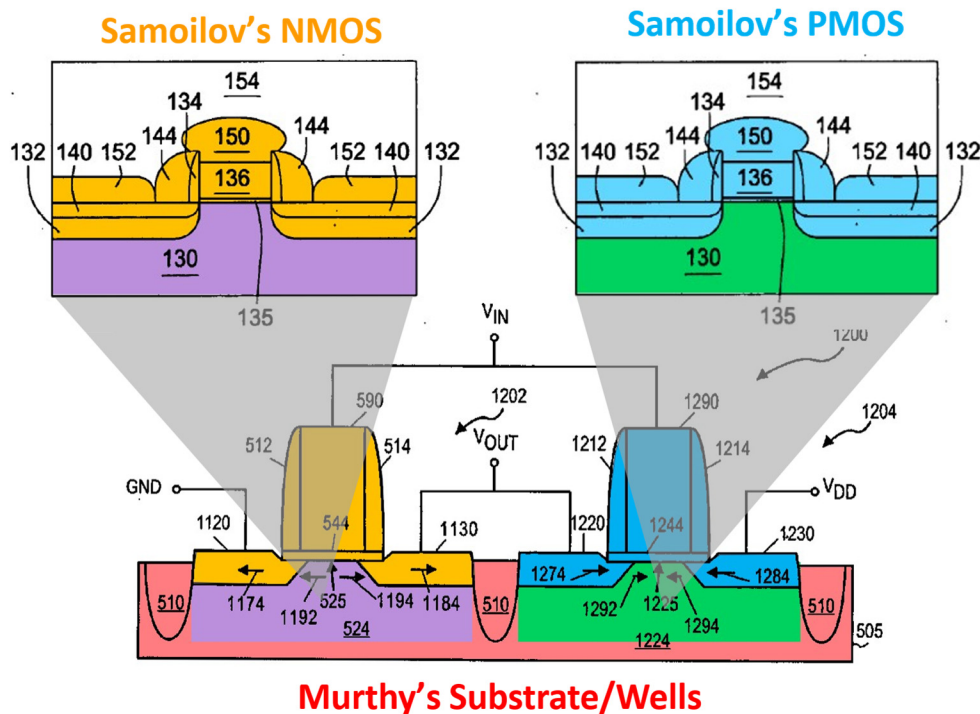


EX1005-Samoilov, Fig. 2F and EX1011-Murthy, Fig. 12 (combined); *see also* EX1011-Murthy, 23:27-39. EX1003-Lee-Decl., ¶¶189-190.

These teachings equally satisfy the challenged claims when the conductivity types are reversed, i.e., when the “first conductivity type” is n-type and the “second conductivity type” is p-type. In this scenario, the first well corresponds to Murthy’s n-well 1224 and the second well corresponds to Murthy’s p-well 524. EX1003-Lee-Decl., ¶190.

- c. [1B]: “a first MOS transistor of the first conductivity type on the second well, comprising:”**

Samoilov-Murthy (*see* Section VI.D.1) includes a first MOS transistor (e.g., Samoilov's **PMOS transistor**) of the first conductivity type (e.g., p-type) on the second well (e.g., Murthy's **n-well 1224**), as illustrated below.



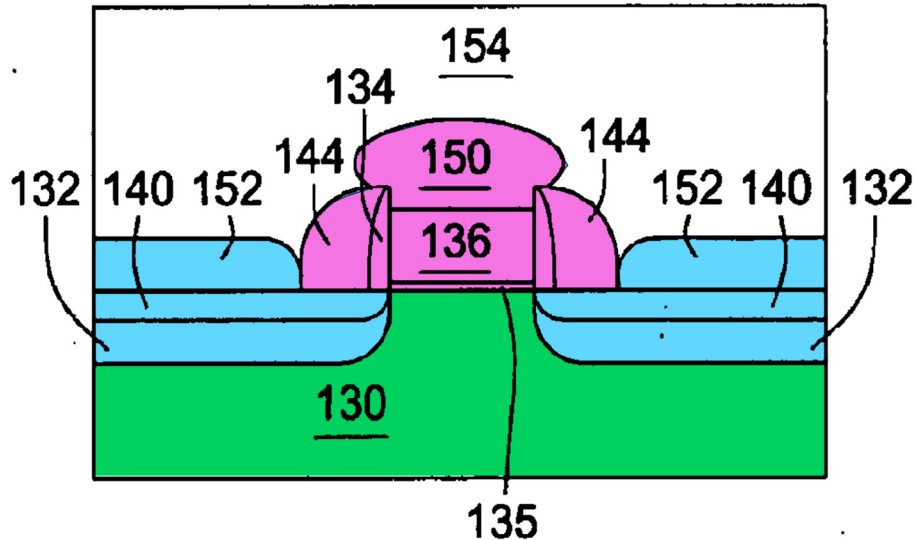
EX1005-Samoilov, Fig. 2F and EX1011-Murthy, Fig. 12 (combined); *see also* EX1011-Murthy, 23:23-39. EX1003-Lee-Decl., ¶¶191-192.

These teachings equally satisfy the challenged claims when the conductivity types are reversed, i.e., when the “first conductivity type” is n-type and the “second conductivity type” is p-type. In this scenario, the first MOS transistor corresponds

to Samoilov's NMOS transistor on Murthy's p-well 1224 (*see* Limitation [1E]).
EX1003-Lee-Decl., ¶193.

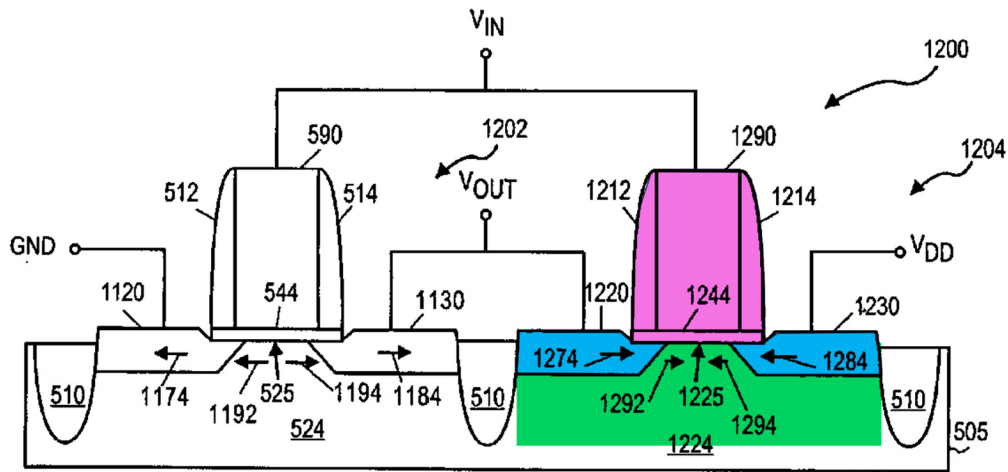
d. [1C]: “a first MOS transistor ... comprising: a first gate structure on the second well”

Referring to Figure 2F below, Samoilov's PMOS transistor has a gate structure (e.g., gate oxide layer 135, gate 136, off-set spacer 134, and/or spacer 144, individually or in combination) on n-type substrate 130.



EX1005-Samoilov, Fig. 2F; *see also id.*, ¶¶[0009], [0027], [0029], [0038]-[0039], [0067]-[0068]. EX1003-Lee-Decl., ¶¶194-195.

In Samoilov-Murthy (*see* Section VI.D.1), a gate structure, as taught by Samoilov, would have been located on a n-well (e.g., Murthy's n-well 1224). In fact, Murthy depicts an embodiment of a similar PMOS transistor with a gate structure on N-well 1224.



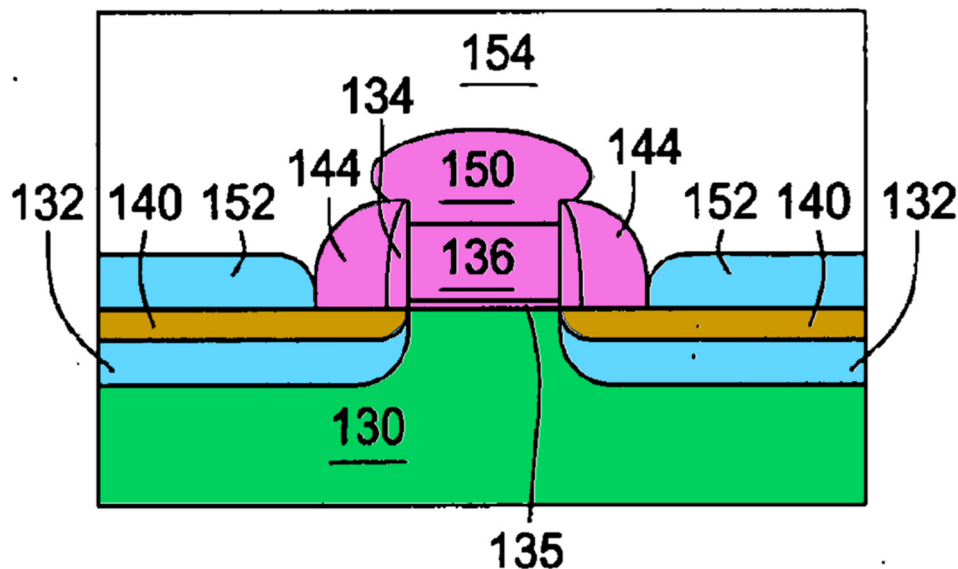
EX1011-Murthy, Fig. 12; *see also id.*, 23:32-39. EX1003-Lee-Decl., ¶196.

These teachings equally satisfy the challenged claims when the conductivity types are reversed, i.e., when the “first conductivity type” is n-type and the “second conductivity type” is p-type, as Samoilov’s NMOS transistor also includes the above-described gate structure. EX1005-Samoilov, ¶¶[0009], [0027], [0029], [0038]-[0039], [0067]-[0068], Fig. 2F; *see also* Limitation [7B] (Section VI.D.8.c). EX1003-Lee-Decl., ¶197.

- e. [1D]: “a first MOS transistor ... comprising: ... a first strained layer of the first conductivity type in a first opening in the second well beside the first gate structure, wherein a difference between a lattice parameter of a portion of the first strained layer near a bottom of the first opening and a lattice parameter of the substrate is smaller than a difference between a lattice parameter of a portion of the first strained layer apart from the bottom of the first opening and the lattice parameter of the substrate”

“first strained layer ... beside the first gate structure”

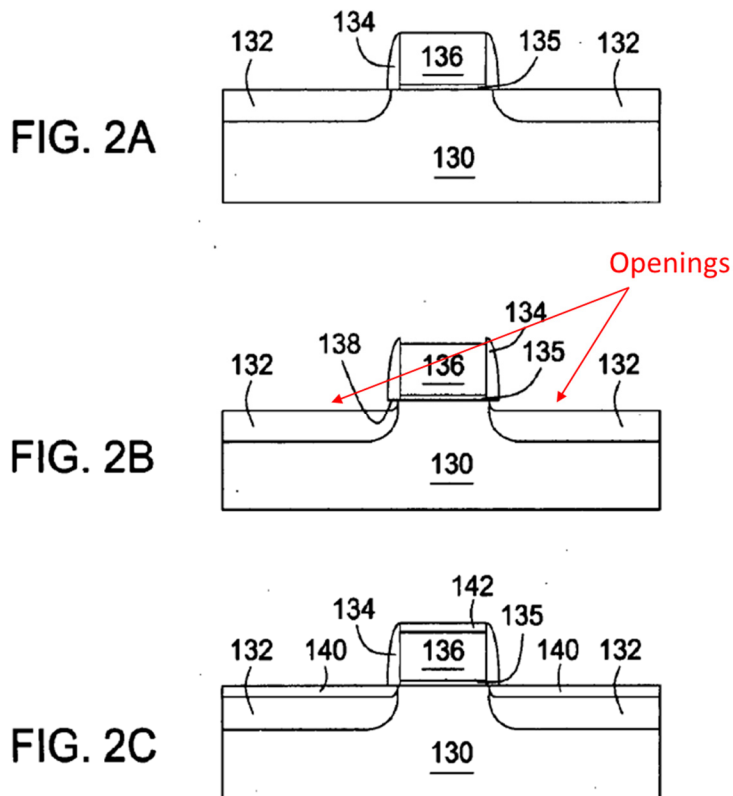
Referring to Figure 2F below, Samoilov discloses that the first MOS transistor (e.g., PMOS transistor) comprises a first strained layer (e.g., silicon-containing layers 140) of the first conductivity type (e.g., p-type) in a first opening in the second well (e.g., n-type substrate 130, which in the combined semiconductor structure taught by Samoilov and Murthy corresponds to Murthy's n-well 1224) beside the first gate structure.



EX1005-Samoilov, Fig. 2F; *see also id.*, ¶¶[0005], [0009], [0021], [0026], [0039].

EX1003-Lee-Decl., ¶¶198-200.

Silicon-containing layers 140 are formed using a silicon-germanium (for a PMOS transistor) and are doped with an appropriate dopant of the first conductivity type (e.g., p-type). EX1005-Samoilov, ¶¶[0032], [0067]; *see also id.*, ¶¶[0009], [0024], [0030]-[0033], [0072], [0074]. For example, Figures 2A through 2C show that silicon-containing layers 140 are formed in openings formed by removing portions of source/drain layer 132 beside the gate structure.



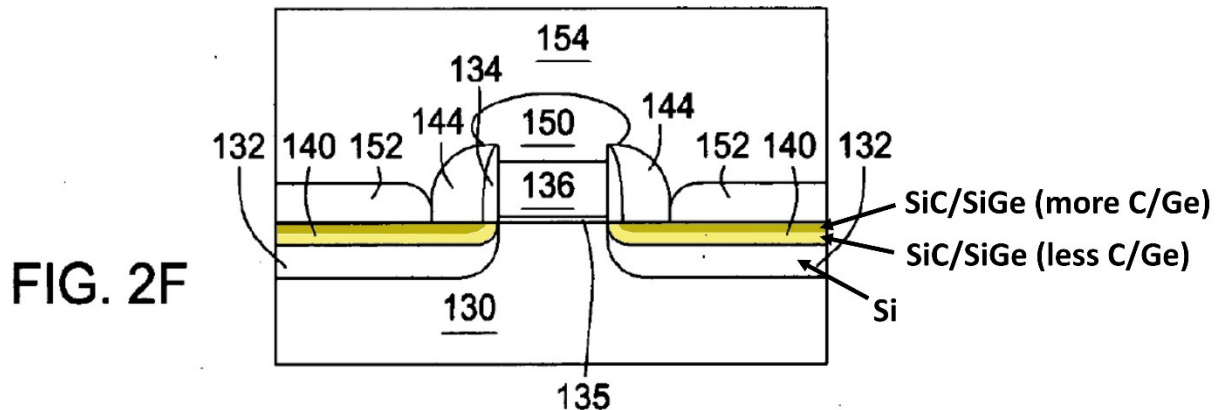
EX1005-Samoilov, Figs. 2A-2C; *see also id.*, ¶¶[0029]-[0030]. EX1003-Lee-Decl.,

¶201.

Strained Layer Has Non-Uniform Lattice Parameter in Opening Next to Gate

As explained in Section VI.A.1.e (Ground 1A), Limitation [1D] requires that the strained layer next to the gate has a non-uniform lattice parameter, which Samoilov discloses. For example, Samoilov discloses that silicon-containing layers 140 have sub-layers “deposited in varying order to form ***graded elemental concentrations of silicon-containing layer 140.***” EX1005-Samoilov, ¶¶[0030], [0032], [0061], [0072], [0074], claims 1, 7, 11-13, 19, 27, 47, 49, 64. In one example, a silicon-germanium sub-layer near the bottom has a “germanium concentration in a range from about 15[% to about 25[%” whereas a sub-layer apart from the bottom has a “germanium concentration in a range from about 25[% to

about 35[%].” *Id.*, ¶¶[0030]; *see also id.*, ¶¶[0072], claims 7, 11-13.⁷ This example is illustrated below in Figure 2F.



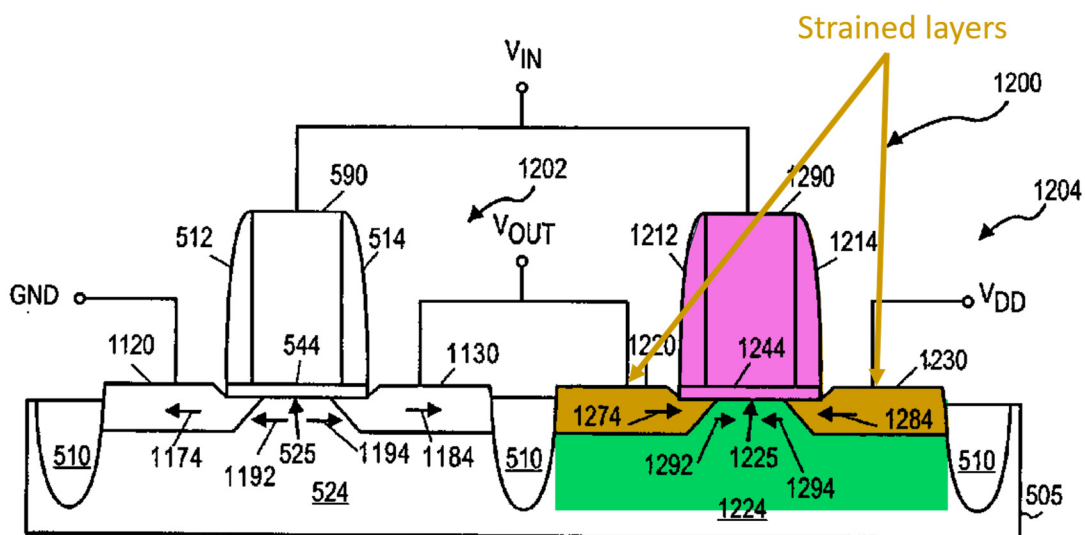
EX1005-Samoilov, Fig. 2F. EX1003-Lee-Decl., ¶¶202-204.

As explained for Ground 1A (*see* Section VI.A.1.e), a non-uniform germanium (or carbon) concentration in the strained layer results in a non-uniform lattice parameter of the strained layer. Accordingly, a POSITA would have understood the lattice parameter at the bottom of silicon-containing layer 140 (where the concentration of germanium or carbon is lower) more closely matches the lattice parameter of the substrate than does the rest of silicon-containing layer 140.

EX1003-Lee-Decl., ¶205.

⁷ Although this example describes two layers, Samoilov teaches that silicon-containing layer 140 may contain more than two layers. EX1005-Samoilov, ¶¶[0016]-[0017], ¶[0030], ¶¶[0060]-[0061]. EX1003-Lee-Decl., ¶183, N.1.

In Samoilov-Murthy (see Section VI.D.1), **strained layer 140** as taught by Samoilov would have been located on **N-well 1224** as taught by Murthy. In fact, Murthy depicts an embodiment of a similar **PMOS transistor** with a strained layer (e.g. **junctions 1220 and 1230**, which “cause compressive strains 1274 and 1284”) on **N-well 1224** beside the **gate structure**.



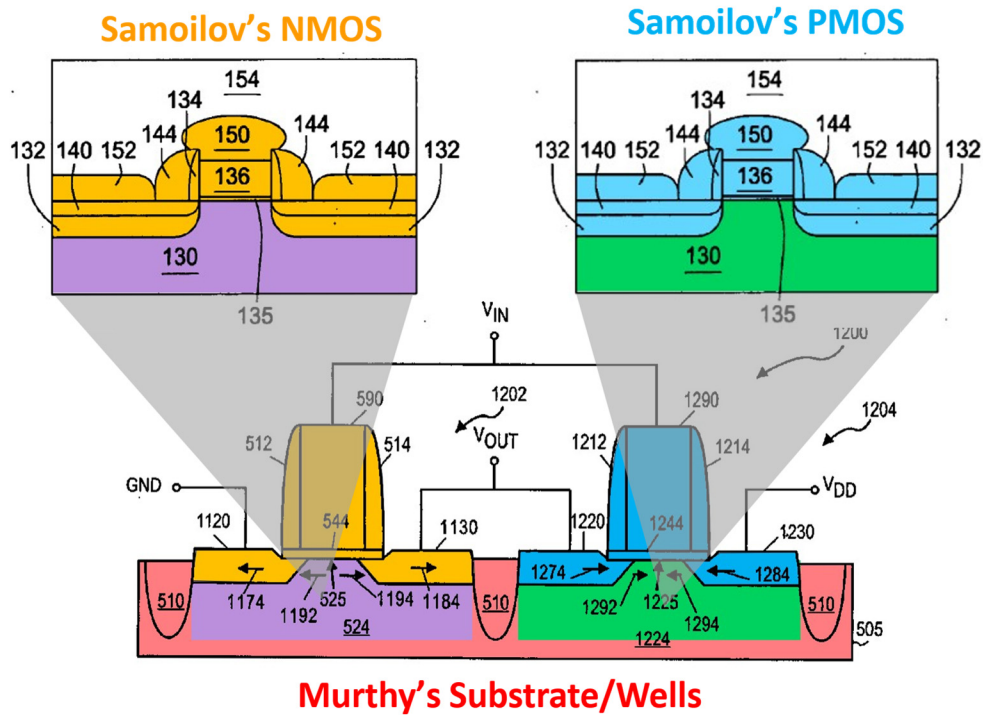
EX1011-Murthy, Fig. 12; see also *id.*, 23:40-55 (“junctions 1220 and 1230 may be formed of a material having a lattice spacing larger than a lattice spacing of substrate 505” such as “SiGe”). EX1003-Lee-Decl., ¶206.

These teachings equally satisfy the challenged claims when the conductivity types are reversed, i.e., when the “first conductivity type” is n-type and the “second conductivity type” is p-type, as Samoilov’s NMOS transistor also includes the above-described silicon-containing layer 140. EX1005-Samoilov, ¶¶[0009], [0030]-[0033], [0067], Fig. 2F. In this scenario, Samoilov teaches that silicon-containing

layers 140 are formed using a silicon-carbon (rather than silicon-germanium) and similarly has a non-uniform, graded lattice parameter, e.g., a silicon-carbon sub-layer closer to the bottom has a “carbon concentration of about 1.25[%]”, whereas a sub-layer apart from the bottom has a “carbon concentration of about 1.75[%]....” *Id.*, ¶¶[0073]-[0074]; *see also id.*, claims 19, 27, 47; EX1011-Murthy, 21:49-22:15 (describing use of silicon-carbon to cause tensile strain in NMOS transistors). EX1003-Lee-Decl., ¶207.

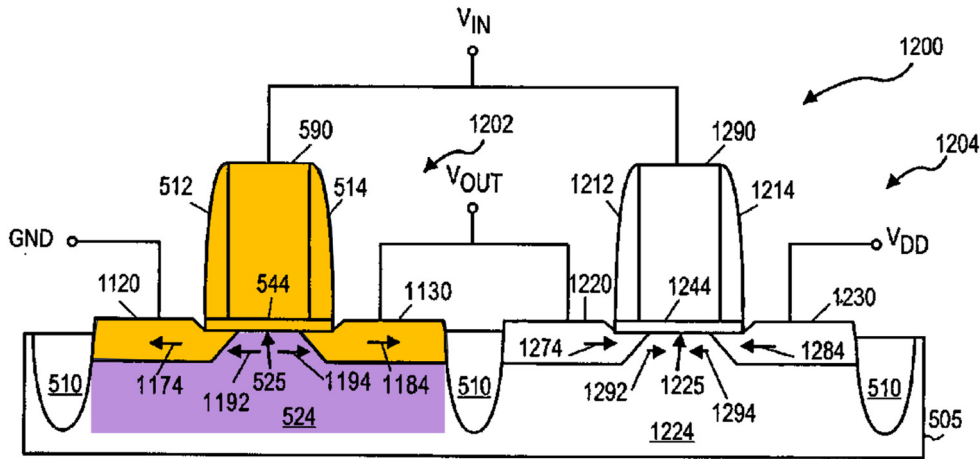
f. [1E]: “a second MOS transistor of the second conductivity type on the first well”

Samoilov-Murthy (*see* Section VI.D.1) includes a second MOS transistor (e.g., Samoilov’s **NMOS transistor**) of the second conductivity type (e.g., n-type) on the first well (e.g., Murthy’s **P-well 524**), as illustrated below.



EX1005-Samoilov, Fig. 2F and EX1011-Murthy, Fig. 12 (combined); *see also* EX1011-Murthy, 23:23-39. EX1003-Lee-Decl., ¶¶208-209.

In the combination, Samoilov's **NMOS transistor** would have been located on Murthy's **P-well 524**. In fact, Murthy depicts an embodiment of a similar **NMOS transistor** on P-well 524.



EX1011-Murthy, Fig. 12; *see also id.*, 23:23-39. EX1003-Lee-Decl., ¶209.

These teachings equally satisfy the challenged claims when the conductivity types are reversed, i.e., when the “first conductivity type” is n-type and the “second conductivity type” is p-type. In this scenario, the second MOS transistor corresponds to Samoilov’s PMOS transistor on Murthy’s N-well 1224 (*see* Limitation [1B]). EX1003-Lee-Decl., ¶210.

3. Claim 2: “The semiconductor structure of claim 1, wherein the lattice parameter of the first strained layer has a gradient distribution”

As explained above for Ground 3A, Limitation [1D] (*see* Section VI.D.2.e), Samoilov discloses that silicon-containing layers 140 (i.e., the claimed “first strained layer”) have a “graded elemental concentration,” meaning their lattice parameter has a gradient distribution. EX1005-Samoilov, ¶¶[0030] (“SiGe-containing layers containing varying amount of elements may be stacked to form silicon-containing

layer 140 with a *graded* elemental concentration”), [0032], [0044]. EX1003-Lee-Decl., ¶¶211-212.

4. **Claim 3: “The semiconductor structure of claim 1, wherein the first conductivity type is P-type, and the lattice parameter of a portion of the first strained layer near the bottom of the first opening is smaller than the lattice parameter of a portion of the first strained layer apart from the bottom of the first opening”**

As explained for Ground 1A, claim 3 describes a strained layer transistor structure in which spacing between the atoms at the bottom of the structure (measured by the “lattice parameter”) is tighter than elsewhere in the structure. Samoilov discloses claim 3. For example, as explained above for Ground 3A, Limitation [1D] (Section VI.D.2.e), when the first conductivity type is p-type, silicon-containing layers 140 are formed using silicon-germanium where the amount of germanium relative to silicon becomes smaller closer to the bottom of silicon-containing layers 140. As explained above (*see* Sections III.D, VI.A.3), a POSITA would have understood the lattice parameter in silicon-germanium becomes smaller with decreasing germanium concentration and is thus smaller closer to the bottom of silicon-containing layers 140. EX1003-Lee-Decl., ¶¶213-214.

5. **Claim 4: “The semiconductor structure of claim 3, wherein the first strained layer comprises SiGe”**

Samoilov-Murthy satisfies claim 4 for the reasons in Section VI.D.2.e (Limitation [1D]) and VI.D.4 (claim 3). *See also* EX1005-Samoilov, ¶[0067]

(“SiGe may be deposited in a recessed area to form a PMOS component.”).

EX1003-Lee-Decl., ¶215.

6. **Claim 5: “The semiconductor structure of claim 1, wherein the first conductivity type is N-type, and the lattice parameter of a portion of the first strained layer near the bottom of the first opening is larger than the lattice parameter of a portion of the first strained layer apart from the bottom of the first opening”**

As explained for Ground 1A, claim 5 describes a strained layer transistor structure in which spacing between the atoms at the bottom of the structure (measured by the “lattice parameter”) is greater than elsewhere in the structure. Samoilov discloses claim 5. For example, as explained above for Ground 3A, Limitation [1D] (Section VI.D.2.e), when the first conductivity type is n-type, silicon-containing layers 140 are formed using silicon-carbon where the amount of carbon relative to silicon becomes smaller closer to the bottom of silicon-containing layers 140. As explained above (*see* Sections III.D, VI.A.5), a POSITA would have understood the lattice parameter in silicon-carbon becomes larger with decreasing carbon concentration and is thus larger closer to the bottom of silicon-containing layers 140. EX1003-Lee-Decl., ¶¶216-217.

7. **Claim 6: “The semiconductor structure of claim 5, wherein the first strained layer comprises SiC”**

Samoilov-Murthy satisfies claim 6 for the reasons in Section VI.D.2.e (Limitation [1D]) and VI.D.6 (claim 5). *See also* EX1005-Samoilov, ¶[0067] (“SiC

may be deposited in a recessed area to form a NMOS component.”). EX1003-Lee-Decl., ¶218.

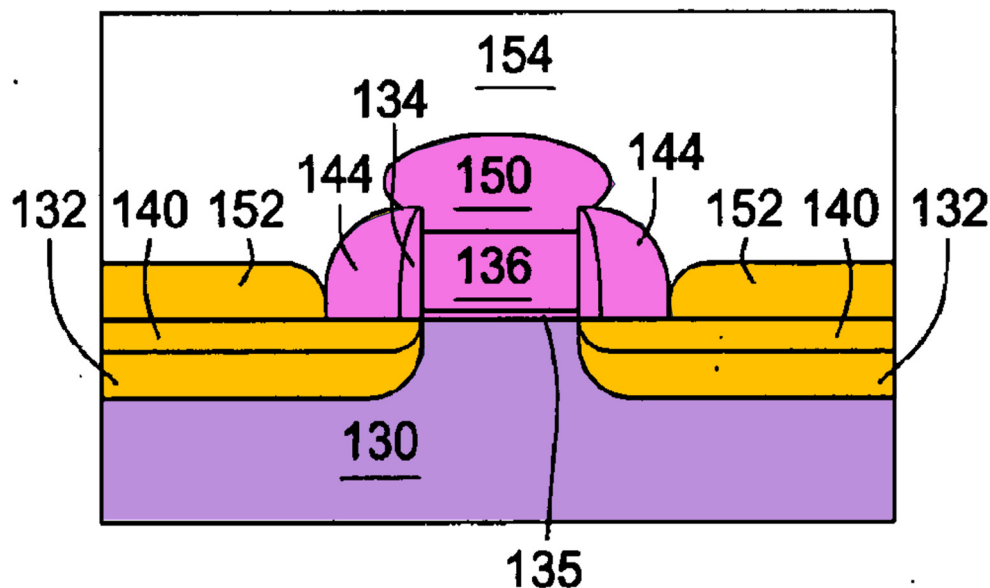
8. Claim 7

a. [7Pre]: “The semiconductor structure of claim 1”

Claim 7 depends from claim 1, which Samoilov-Murthy satisfies. *See* Section VI.D.2. EX1003-Lee-Decl., ¶219.

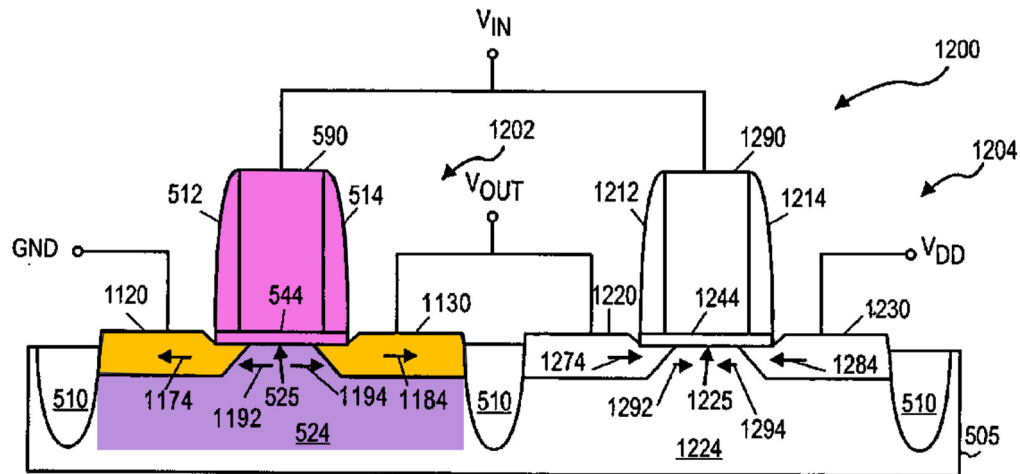
b. [7A]: “the second MOS transistor comprises: a second gate structure on the first well”

Referring to Figure 2F below, Samoilov's NMOS transistor has a gate structure (e.g., gate oxide layer 135, gate 136, off-set spacer 134, and/or spacer 144, individually or in combination).



EX1005-Samoilov, Fig. 2F; *see also id.*, ¶¶ [0027], [0029]. EX1003-Lee-Decl., ¶¶220-221.

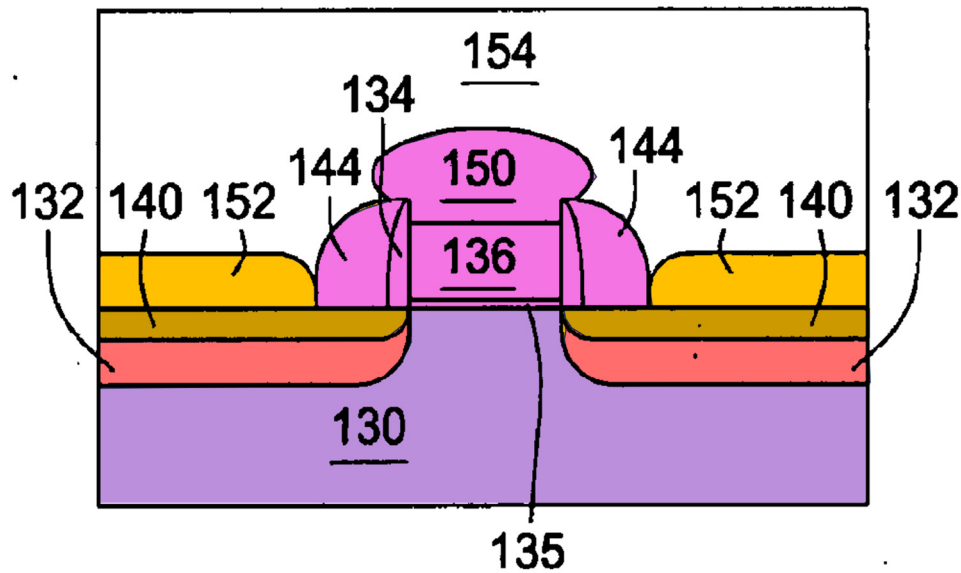
In Samoilov-Murthy (see Section VI.D.1), this **gate structure** would have been located on a **P-well 524**, as taught by Murthy. In fact, Murthy itself depicts an embodiment of a similar **NMOS transistor** with a **gate structure** on **P-well 524**.



EX1011-Murthy, Fig. 12. EX1003-Lee-Decl., ¶¶222-223.

- c. [7B]: “the second MOS transistor comprises: ... a source/drain region of the second conductivity type in the first well beside the second gate structure”

Referring to Figure 2F below, Samoilov discloses that the second MOS transistor (e.g., **NMOS transistor**) comprises a source/drain region (e.g., **source/drain layers 132**) of the second conductivity type (e.g., n-type) in a p-type substrate 130 beside the second **gate structure**.



EX1005-Samoilov, Fig. 2F; *see also id.*, ¶¶[0005], [0009], [0026]-[0027], [0029], [0039]. EX1003-Lee-Decl., ¶224.

In Samoilov-Murthy (*see* Section VI.D.1), this source/drain region would have been located on P-well 406, as taught by Murthy. EX1003-Lee-Decl., ¶¶225-226.

9. Claim 9

a. [9Pre]: “The semiconductor structure of claim 1”

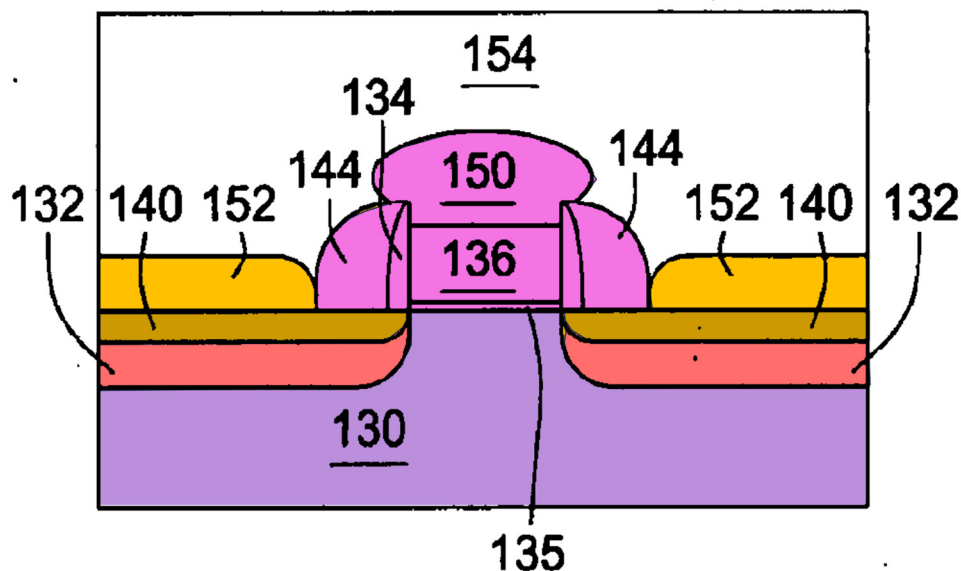
Claim 9 depends from claim 1, which Samoilov-Murthy satisfies. Section VI.D.2. EX1003-Lee-Decl., ¶227.

b. [9A]: “the second MOS transistor comprises: a second gate structure on the first well”

As explained above for limitation [7A] (Section VI.D.8.b), which recites identical limitations, Samoilov-Murthy discloses these limitations. EX1003-Lee-Decl., ¶228.

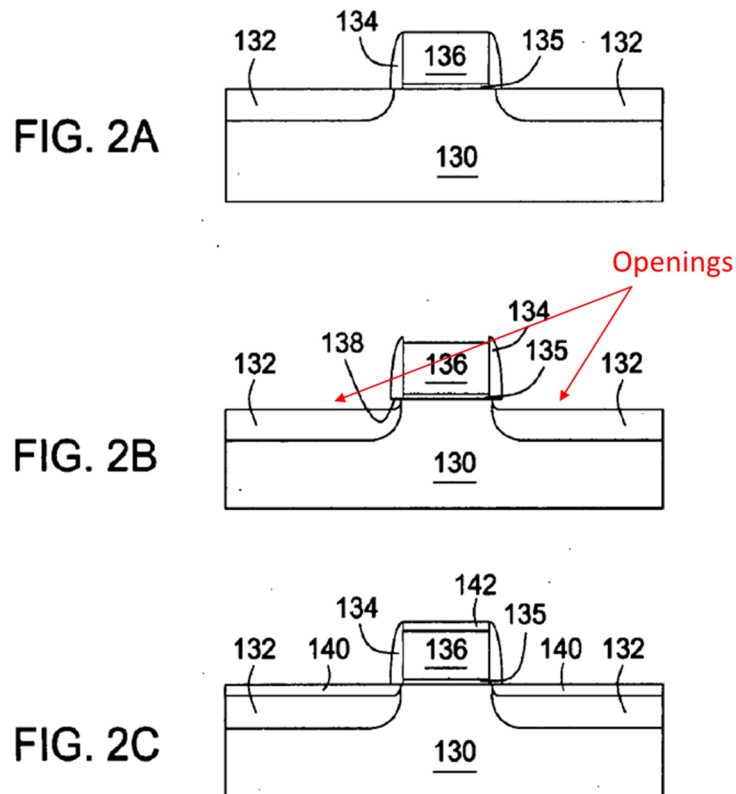
c. [9B]: “the second MOS transistor comprises: ... a source/drain region of the second conductivity type around and under a second opening in the first well beside the second gate structure”

As explained above for Limitation [7B] (Section VI.D.8.c), Samoilov discloses a source/drain region (e.g., **source/drain layers 132**) of the second conductivity type (e.g., n-type) beside the second **gate structure**. As shown in Figure 2F below, Samoilov further discloses that **source/drain layers 132** extend around (e.g., to the right/left of) and under (e.g., below) a second opening in the first well (e.g., the opening containing **silicon-containing layers 140**), as claimed.



EX1005-Samoilov, Fig. 2F; *see also id.*, ¶¶[0005], [0009], [0026]-[0027], [0029], [0039]. EX1003-Lee-Decl., ¶229.

Figures 2A through 2C show that source/drain layers 132 extend around and under openings that are formed beside the gate structure during fabrication of the NMOS transistor (Figure 2B) that are subsequently filled by silicon-containing layers 140 (Figure 2C).



EX1005-Samoilov, Figs. 2A-2C; *see also id.*, ¶¶[0029]-[0030]. EX1003-Lee-Decl., ¶230.

In the combined semiconductor structure taught by Samoilov and Murthy (*see* Section VI.D.1), this source/drain region would have been located on P-well 524, as taught by Murthy. EX1003-Lee-Decl., ¶¶231-232.

10. Claim 11

a. [11Pre]: “The semiconductor structure of claim 1”

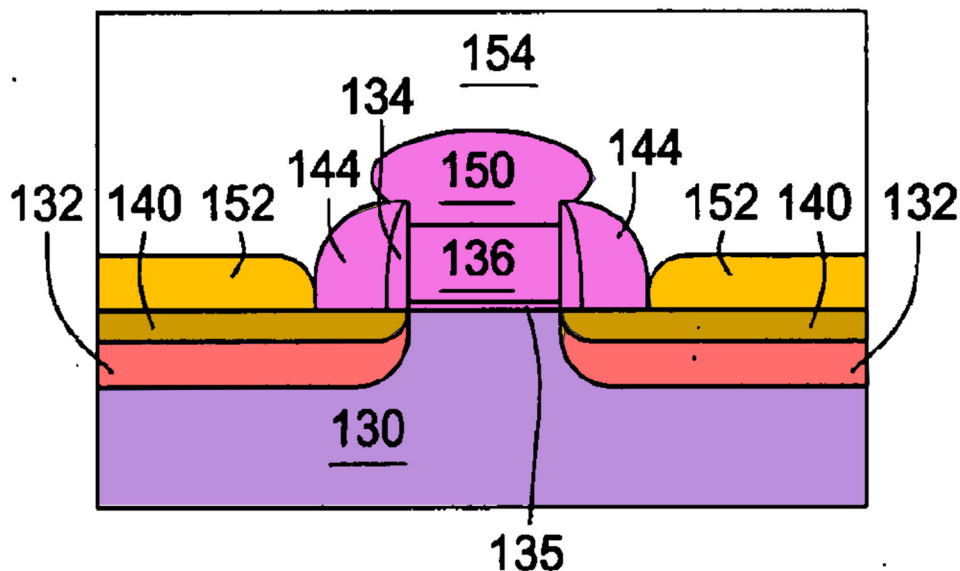
Claim 11 depends from claim 1, which Samoilov-Murthy satisfies. Section VI.D.2. EX1003-Lee-Decl., ¶233.

b. [11A]: “the second MOS transistor comprises: a second gate structure on the first well”

As explained above for limitation [7A] (Section VI.D.8.b), which recites identical limitations, Samoilov-Murthy discloses these limitations. EX1003-Lee-Decl., ¶234.

c. [11B]: “the second MOS transistor comprises: ... a second strained layer of the second conductivity type in a second opening in the first well beside the second gate structure”

Referring to Figure 2F below, Samoilov discloses that the second MOS transistor (e.g., NMOS transistor) comprises a second strained layer (e.g., silicon-containing layers 140) of the second conductivity type (e.g., n-type) in a second opening in the first well (e.g., p-type substrate 130, which in the combined semiconductor structure taught by Samoilov and Murthy corresponds to Murthy’s p-well 524) beside the second gate structure.



EX1005-Samoilov, Fig. 2F; *see also id.*, ¶¶[0005], [0009], [0021], [0026], [0039].

EX1003-Lee-Decl., ¶235.

As explained in Section VI.D.2.e (Limitation [1D]), the strained layer would have been formed in openings in the p-well. EX1005-Samoilov, Figs. 2A-2C; *see also id.*, ¶¶[0029]-[0030]. EX1003-Lee-Decl., ¶¶206, 236.

As explained in Section VI.D.1.e, the teachings of Samoilov-Murthy regarding the “first strained layer” equally apply when the conductivity type is reversed. Thus, the teachings of Samoilov-Murthy regarding the “first strained layer” of the “first conductivity type” equally applies to the “second strained layer” of the “second conductivity type.”. EX1003-Lee-Decl., ¶¶237.

11. Claim 12

a. [12Pre]: “The semiconductor structure of claim 11”

Claim 12 depends from claim 11, which Samoilov-Murthy satisfies. Section VI.D.10. EX1003-Lee-Decl., ¶238.

b. [12A]: “a difference between a lattice parameter of a portion of the second strained layer near a bottom of the second opening and the lattice parameter of the substrate is smaller than a difference between a lattice parameter of a portion of the second strained layer apart from the bottom of the second opening and the lattice parameter of the substrate”

Limitation [12A] applies the same non-uniform lattice parameter limitations as Limitation [1D] to the second strained layer of Limitation [11B]. As explained for Limitation [1D], Samoilov teaches that both strained layers, including the second (NMOS) strained layer, satisfy the non-uniform lattice parameter limitations. Accordingly, Samoilov-Murthy satisfies element [12A] for the reasons in Sections VI.D.2.e (Limitation [1D]) and VI.D.10.c (Limitation [11B]). EX1003-Lee-Decl., ¶239.

- c. **[12B]: “when the first conductivity type is P-type and the second conductivity type is N-type, the lattice parameter of a portion of the first strained layer near the bottom of the first opening is smaller than the lattice parameter of a portion of the first strained layer apart from the bottom of the first opening, but the lattice parameter of a portion of the second strained layer near the bottom of the second opening is larger than the lattice parameter of a portion of the second strained layer apart from the bottom of the second opening”**

Limitation [12B] recites the same limitations as Claims 3 and 5 (Sections VI.D.4 and VI.D.6) in a configuration where the first conductivity type is P-type and the second conductivity type is N-type. Therefore, Samoilov-Murthy satisfies element [12B] for the reasons set forth above. *See also* Sections VI.D.2.e (Limitation [1D]), VI.D.10.c (Limitation [11B]). EX1003-Lee-Decl., ¶240.

- d. **[12C]: “when the first conductivity type is N-type and the second conductivity type is P-type, the lattice parameter of a portion of the first strained layer near the bottom of the first opening is larger than the lattice parameter of a portion of the first strained layer apart from the bottom of the first opening, but the lattice parameter of a portion of the second strained layer near the bottom of the second opening is smaller than the lattice parameter of a portion of the second strained layer apart from the bottom of the second opening”**

Limitation [12C] recites the same limitations as Claims 3 and 5 (Sections VI.D.4 and VI.D.6) in a configuration where the first conductivity type is N-type and the second conductivity type is P-type. Therefore, Samoilov-Murthy satisfies

element [12B] for the reasons set forth above. *See also* Sections VI.D.2.e (Limitation [1D]), VI.D.10.c (Limitation [11B]). EX1003-Lee-Decl., ¶241.

12. Claim 13: “The semiconductor structure of claim 12, wherein the lattice parameter of the second strained layer has a gradient distribution”

Claim 13 applies the same gradient distribution limitations as claim 2 to the second strained layer of Limitation [11B]. As explained for Limitation [1D], Samoilov teaches that both strained layers, including the second (NMOS) strained layer, satisfy the gradient distributions limitations. Accordingly, Samoilov-Murthy satisfies element [12B] for the reasons in Sections VI.D.2.e (Limitation [1D]), VI.D.3 (Claim 2), and VI.D.10.c (Limitation [11B]). EX1005-Samoilov, ¶¶[0030] (stacked layers within silicon-containing layers 140—the claimed “second strained layer”—have a “*graded* elemental concentration”), [0032], [0044]. EX1003-Lee-Decl., ¶¶242-243.

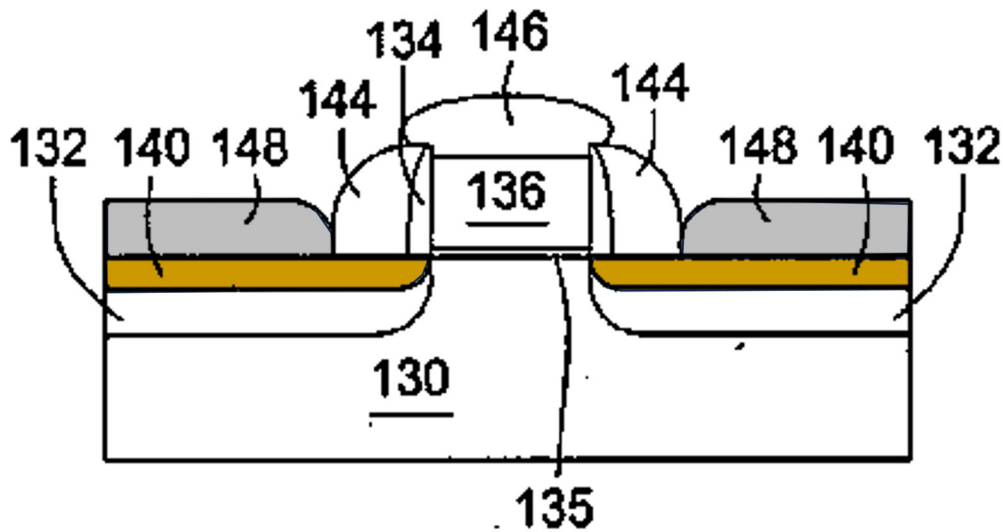
E. Ground 3B: Samoilov in View of Murthy and Sridhar Renders Obvious Claims 8, 10, and 14

Each of claims 8, 10, and 14 recites a process for forming a “metal silicide layer.” To the extent PO argues that Samoilov or Murthy does not disclose these limitations, Sridhar renders these limitations obvious.

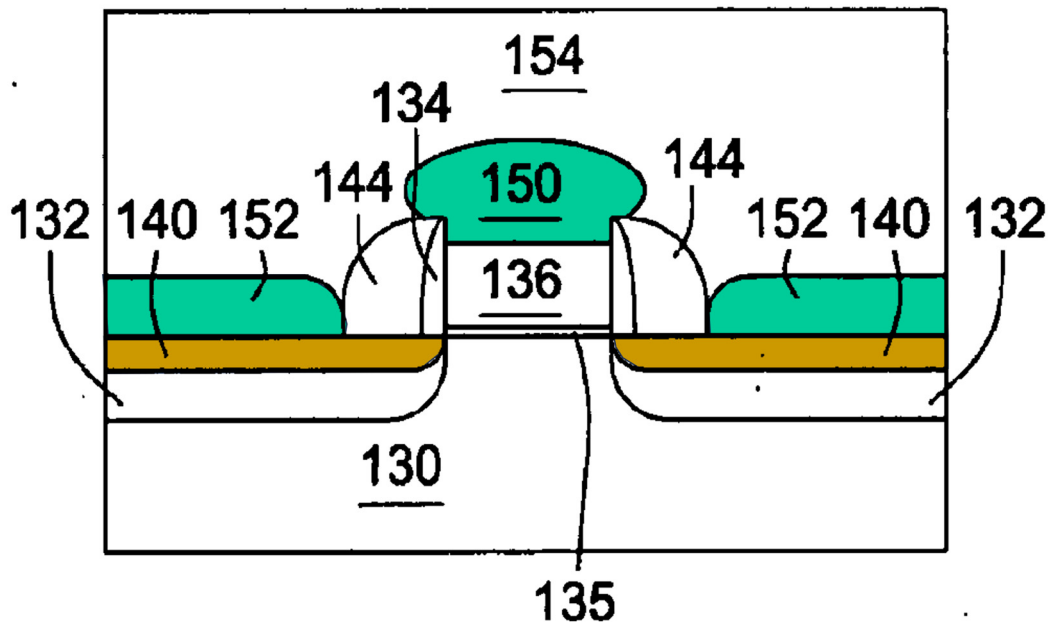
1. Samoilov-Murthy-Sridhar

(I) *Samoilov-Murthy*

As shown in Figure 2E, Samoilov discloses forming a silicon capping layer 148 that “contain[s] little or no germanium or carbon” over layer 140.



EX1005-Samoilov, Fig. 2E, *see also id.*, ¶¶[0035]-[0036]. During processing, capping layer 148 is converted to silicide layers 152, such as cobalt silicide, as shown below.



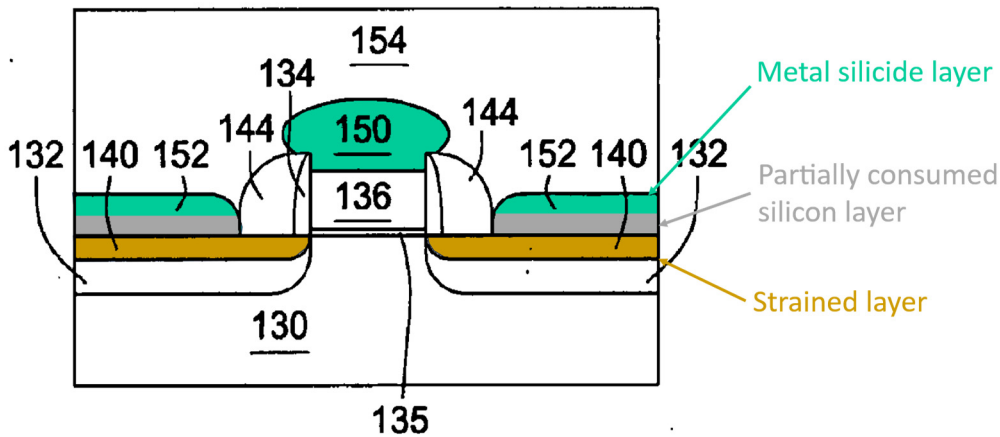
EX1005-Samoilov, Fig. 2F, *see also id.*, ¶[0037]. EX1003-Lee-Decl., ¶¶245-246.

(2) Sridhar

As explained above for Ground 1B, Sridhar teaches forming a silicon capping layer on the strained layer, where the silicon layer is only partially consumed during silicide formation such that a portion of the silicon layer remains on the strained layer when the process is complete. *See* Section VI.B.1.2. EX1003-Lee-Decl., ¶247.

(3) Motivation to combine

Samoilov-Murthy-Sridhar teaches a silicon capping layer, as taught by Samoilov, being partially consumed during silicide formation, as taught by Sridhar, leaving behind a residual silicon layer as illustrated below.



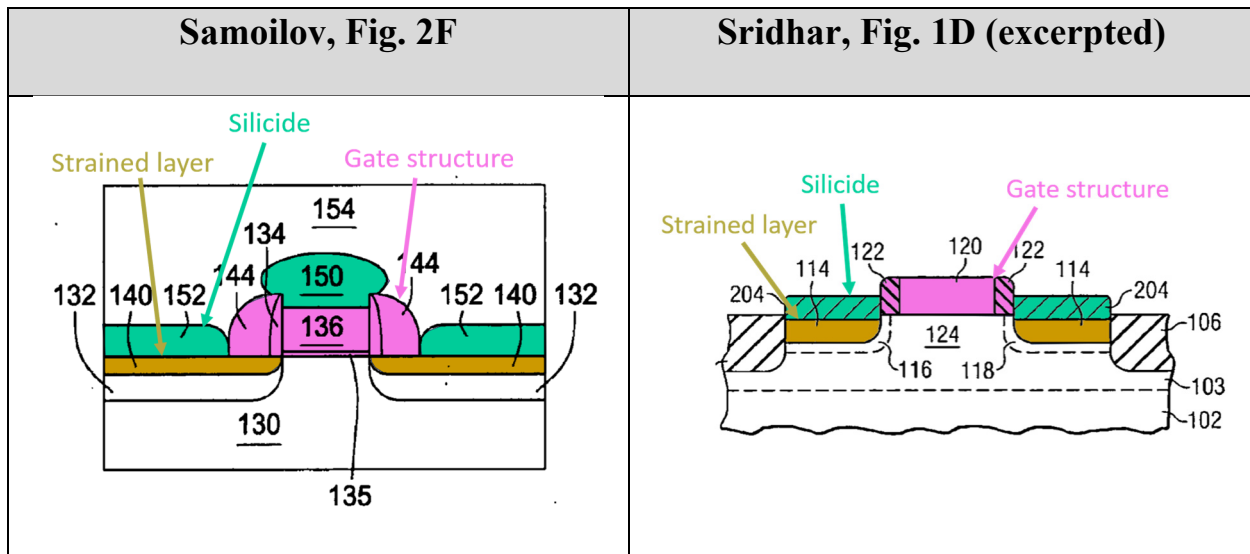
EX1005-Samoilov, Fig. 2F (annotations illustrate the results of applying Sridhar’s teachings). A POSITA would have been motivated to combine these teachings for substantially the same reasons set forth in Ground 1B for Koontz-Sridhar. *See* Section VI.B.1.3.⁸ The following additional reasons apply. EX1003-Lee-Decl., ¶¶248-249.

First, Samoilov suggests that its silicide layer should be formed by first depositing a silicon layer “contain[s] little or no germanium or carbon.” EX1005-Samoilov, ¶¶[0035]-[0037]. Samoilov thus motivates a POSITA to seek out details for converting the silicon layer to the silicide layer. EX1003-Lee-Decl., ¶250.

Second, Sridhar discloses the benefits of its techniques for forming a silicon layer on the strained layer. *See* Section VI.B.1.3. EX1003-Lee-Decl., ¶250.

⁸ As explained in Section V, *supra*, Samoilov, Murthy, and Sridhar are each analogous art to the '822 patent.

Third, the references each describe similar semiconductor structures (and techniques for forming such structures) such that their combination would have yielded predictable results. For example, Samoilov discloses MOS transistors where “a silicon-containing material such as [silicon-germanium or silicon-carbon] may be deposited in a recessed area” of the transistor. EX1005-Samoilov, ¶[0067]; *see also* EX1011-Murthy, 2:31-46, Figs. 1-3. Similarly, Sridhar discloses fabricating MOS transistors by “forming a silicon-germanium layer in each of the source and drain regions....” EX1007-Sridhar, ¶[0004]; *see also id.*, ¶¶[0001], [0010]. In fact, Sridhar states that its techniques “may be implemented as a drop-in” solution that is integrated into existing processing technologies like those used by Samoilov and Murthy. *Id.*, ¶[0017]; *see also id.*, ¶[0005]. Moreover, Samoilov-Murthy and Sridhar disclose similar structures, e.g., MOS transistors with silicon-germanium or silicon-carbon strained layers, as illustrated below. EX1005-Samoilov, ¶¶[0030], [0032], [0034]; EX1007-Sridhar, ¶¶[0003], [0012], [0014].



Thus, Samoilov, Murthy, and Sridhar each share similar objectives and means for accomplishing those objectives, indicating that their combination would have been straightforward and yielded predictable results. EX1003-Lee-Decl., ¶251.

Fourth, a POSITA would have had a reasonable success in applying Sridhar's teachings given that, as explained above, Sridhar discloses that its techniques are compatible with existing semiconductor processing technologies like those used by Samoilov and Murthy. Moreover, in the combination, Sridhar's known semiconductor structures and processing techniques would have been used in the similar semiconductor structure taught by Samoilov and Murthy in the same way. For example, Samoilov discloses a semiconductor structure having a silicide layer on a strained layer, EX1005-Samoilov, ¶¶[0009], [0037], [0067], Fig. 2F, and Sridhar discloses forming the silicide layer in a manner that improves its electrical characteristics (e.g., by forming a silicon layer on the strained layer that is partially

consumed when forming the silicide layer). Thus, Sridhar's teachings would have been applied to Samoilov-Murthy in the same way that those teachings are used in Sridhar itself. EX1003-Lee-Decl., ¶¶252-253.

Finally, it would have been obvious to apply Sridhar's teachings as described above to either or both of the PMOS and NMOS transistors in Samoilov-Murthy for the reasons set forth in Ground 1B. *See* Section VI.B.1.3. EX1003-Lee-Decl., ¶254.

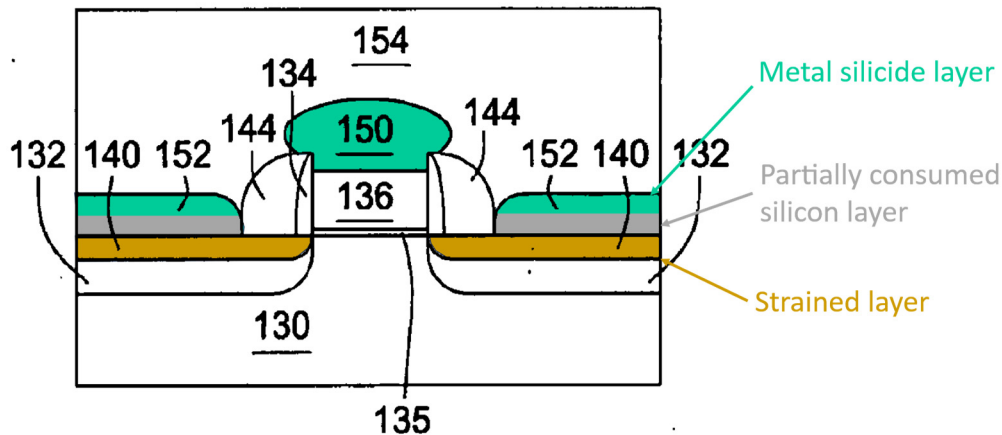
2. Claim 8

a. [8Pre]: "The semiconductor structure of claim 7"

Claim 8 depends from claim 7, which Samoilov-Murthy satisfies. Section VI.D.8. EX1003-Lee-Decl., ¶244.

b. [8A]: "a silicon layer on the first strained layer"

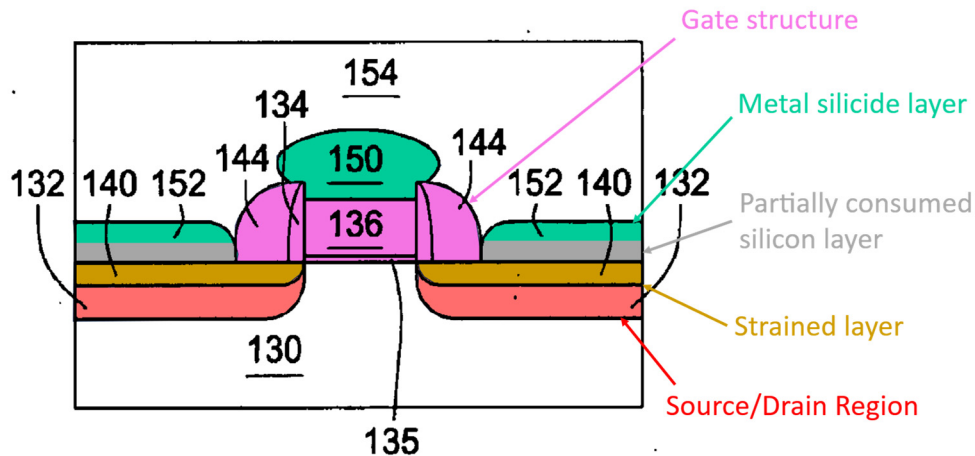
Samoilov-Murthy-Sridhar (*see* Section VI.E.1) includes a silicon layer (e.g., Samoilov's *silicon capping layer*, where the silicon capping layer is only partially consumed during silicide formation as taught by Sridhar) on the first strained layer (e.g., Samoilov's *silicon-containing layers 140*), as illustrated below.



EX1005-Samoilov, Fig. 2F (annotations illustrate the results of applying Sridhar's teachings). EX1003-Lee-Decl., ¶¶245-248.

- c. [8B]: “a metal silicide layer on the silicon layer, the source/drain region and the first and the second gate structures”

As explained above for Limitation [8A], Samoilov-Murthy-Sridhar has a metal silicide layer (e.g., Samoilov's **silicide layers 152**) on a silicon layer (e.g., Samoilov's **silicon-containing layers 148** where the silicon-containing layers are only partially consumed during the silicide formation process, as taught by Sridhar). As shown in Figure 2F, Samoilov further teaches that **silicide layers 150** are on **source/drain region 132** and that a **silicide layer 150** is on the **gate structures**.



EX1005-Samoilov, Fig. 2F (annotations illustrate the results of applying Sridhar's teachings); *see also id.*, [0037]. EX1003-Lee-Decl., ¶¶255-256.

3. Claim 10

Samoilov-Murthy-Sridhar satisfies claim 10 for the reasons in Sections VI.D.9 (claim 9) and VI.E.2 (claim 8). EX1003-Lee-Decl., ¶257.

4. Claim 14

a. [14Pre]: “The semiconductor structure of claim 11”

Claim 14 depends from claim 11, which Samoilov-Murthy satisfies. Section VI.D.10. EX1003-Lee-Decl., ¶258.

b. [14A]: “a silicon layer on the first strained layer and the second strained layer”

As explained for Limitations [1D] and [11B], Koontz-Sridhar includes first and second strained layers and, as explained above (*see* Section VI.E.1), renders obvious the formation of a silicon layer on the strained layers. EX1003-Lee-Decl., ¶259.

c. [14B]: “a metal silicide layer on the silicon layer and the first and second gate structures”

As explained above for limitation [8B] (Section VI.E.2.c), which recites overlapping limitations with an additional limitation, Koontz discloses these limitations. EX1003-Lee-Decl., ¶260.

VII. MANDATORY NOTICES

A. Real Party-in-Interest

Taiwan Semiconductor Manufacturing Company Limited is the real party-in-interest.

B. Related Matters

The '822 patent is assigned to Marlin Semiconductor Limited. Petitioner is unaware of any district court litigation or other proceeding involving the '822 patent.

C. Lead and Back-Up Counsel

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D. Service Information

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VIII. PAYMENT OF FEES

The Office may charge additional fees to Deposit Account No. 08-0219.

IX. GROUNDS FOR STANDING

Petitioner certifies the '822 patent is available for *inter partes* review and Petitioner is not barred or estopped from requesting such review on any grounds identified in this Petition.

X. CERTIFICATION UNDER 37 C.F.R. §42.24(d)

As calculated by the “Word Count” feature of Microsoft Word for Microsoft 365, this Petition contains 13,986 words, excluding this Certification and the following: Table of Contents, Table of Authorities, List of Exhibits, List of Challenged Claims, Mandatory Notices, and Certificate of Service.

XI. CONCLUSION

For the reasons above, claims 1-14 are unpatentable. Trial should be instituted and the challenged claims cancelled.

Dated: October 27, 2025

Respectfully submitted,

/Haixia Lin/

Haixia Lin, Reg. No. 61,318

CERTIFICATE OF SERVICE

The undersigned certifies that, in accordance with 37 C.F.R. § 42.6(e) and 37 C.F.R. § 42.105(a), the following documents were served via FedEx on October 27, 2025, on the correspondence address of record below indicated in the U.S.

Patent Office's Patent Center for U.S. Patent No. 7,288,822:

- Petition for *Inter Partes* Review
- Table of Exhibits
- Exhibits 1001-1018, 1020, 1021, 1023, and 1027
- Petitioner's Power of Attorney
- Certificate of Word Count
- Fee Authorization

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Dated: October 27, 2025

By: /Brian J. Lambson/
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Reg. No. 72,570