

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY LTD.,
Petitioner

v.

MARLIN SEMICONDUCTOR LIMITED,
Patent Owner

Case IPR2026-00058
U.S. Patent No. 7,288,822

**PETITIONER’S OPPOSITION TO PATENT OWNER’S
DISCRETIONARY DENIAL REQUEST**

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Patent Trial and Appeal Board
U.S. Patent and Trademark Office
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PETITIONER’S UPDATED EXHIBIT LIST

Exhibit	Description
EX1001	U.S. Patent No. 7,288,822 to Ting et al. (“’822 Patent”).
EX1002	Prosecution History of the ’822 Patent (“Prosecution History”).
EX1003	Declaration of Dr. Jack Lee (“Lee Decl.”)
EX1004	U.S. Patent Appl. Pub. No. 2006/0134873 A1 to Koontz (“Koontz”).
EX1005	U.S. Patent Appl. Pub. No. 2005/0079692 A1 to Samoilov et al. (“Samoilov”).
EX1006	U.S. Patent No. 7,238,580 B2 to Orłowski et al. (“Orłowski”).
EX1007	U.S. Patent Appl. Pub. No. 2005/0090082 A1 to Sridhar et al. (“Sridhar”).
EX1008	S.M. Sze, <i>Physics of Semiconductor Devices</i> (2d ed. 1981) (excerpted).
EX1009	J.D. Plummer et al., <i>Silicon VLSI Technology: Fundamentals, Practice and Modeling</i> (2000) (excerpted).
EX1010	M. Quirk & J. Serda, <i>Semiconductor Manufacturing Technology</i> (2001) (excerpted).
EX1011	U.S. Patent No. 7,195,985 B2 to Murthy et al. (“Murthy”)
EX1012	U.S. Patent Appl. Pub. No. 2005/0266631 A1 to Kim et al.
EX1013	U.S. Patent Appl. Pub. No. 2007/0238236 A1 to Cook, Jr. et al.

EX1014	S.E. Thompson et al., “A Logic Nanotechnology Featuring Strained-Silicon,” IEEE Electron Device Letters, vol. 25. No. 4, pp. 191-93 (Apr. 2004).
EX1015	Y. Sun et al., <i>Physics of Strain Effects in Semiconductors and Metal-Oxide-Semiconductor Field-Effect Transistors</i> , Journal of Applied Physics, vol. 101, art. No. 104503 (22 pages) (May 2007).
EX1016	P. Bai et al., <i>A 65nm Logic Technology Featuring 35nm Gate Lengths, Enhanced Channel Strain, 8 Cu Interconnect Layers, Low-k ILD and 0.57 μm^2 SRAM Cell</i> , Technical Digest of the 2004 IEEE International Electron Devices Meeting, pp. 657-60 (Dec. 2004).
EX1017	U.S. Patent No. 6,949,482 B2 to Murthy et al. (“Murthy482”)
EX1018	H. Richter et al., <i>Defect Engineering in SiGe Heterostructures</i> , Proceedings of the 1996 CAS International Semiconductor Conference, pp. 41-50 (Oct. 1996).
EX1019	RESERVED
EX1020	U.S. Patent No. 7,288,443 B2 to Zhu.
EX1021	U.S. Patent Appl. Pub. No. 2004/0115916 A1 to Lochtefeld et al.
EX1022	RESERVED
EX1023	S.-L. Zhang & M. Östling, <i>Metal Silicides in CMOS Technology: Past, Present, and Future Trends</i> , Critical Reviews in Solid-State Materials Sciences, vol. 28, no. 1, pp. 1-129 (2003).
EX1024- EX1026	RESERVED
EX1027	J.P. Dismukes et al., “Lattice Parameter and Density in Silicon-Germanium Alloys,” Journal of Physical Chemistry, vol. 68, no. 10,

	pp. 3021-27 (Oct. 1964).
EX1028	USPTO Assignment Data for U.S. Patent No. 7,288,822
EX1029	Docket Navigator Case Search, U.S. Patent No. 7,288,822, captured January 28, 2026
EX1030	Patent Assignment for U.S. Patent No. 7,288,822, Reel and Frame No. 56991/0292
EX1031	“16/12nm Technology” TSMC, captured January 28, 2026 https://www.tsmc.com/english/dedicatedFoundry/technology/logic/l_16_12nm
EX1032	“Another Historic Investment Secured Under President Trump,” The White House, Published Mar. 3, 2025 https://www.whitehouse.gov/articles/2025/03/another-historic-investment-secured-under-president-trump/
EX1033	“CNBC Transcript: United States Commerce Secretary Howard Lutnick Speaks with CNBC’s Brian Sullivan on “The Exchange” Today,” CNBC, Published Apr. 29, 2025 https://www.cnbc.com/2025/04/29/cnbc-transcript-united-states-commerce-secretary-howard-lutnick-speaks-with-cnbc-brian-sullivan-on-the-exchange-today.html
EX1034	“Removing Barriers To American Leadership In Artificial Intelligence,” The White House, Published Jan. 23, 2025 https://www.whitehouse.gov/presidential-actions/2025/01/removing-barriers-to-american-leadership-in-artificial-intelligence/
EX1035	Excerpt of “TSMC Annual Report 2024,” https://investor.tsmc.com/english/annual-reports
EX1036	Shilov, A., “Both Trump and Biden expected to attend TSMC's

	Arizona fab grand opening ceremony — Fab 21 opens in December,” Yahoo! Finance – tom’sHardware, Published Nov. 8, 2024 https://finance.yahoo.com/news/both-trump-biden-expected-attend-151941592.html
EX1037	<i>Longitude Licensing Ltd. et al v. Apple Inc. et al</i>, Case No. WDTX-1-25-cv-00215, Docket Report, Docket Navigator, captured January 28, 2026
EX1038	Docket Navigator Case Search, United Microelectronics Corporation (UMC) Litigation Docket, captured January 28, 2026
EX1039	Nasdaq – This 1 Number May Ensure TSMC’s Market Dominance https://www.nasdaq.com/articles/1-number-may-ensure-tsmcs-market-dominance, captured January 28, 2026
EX1040	“Ansys Strengthens Collaboration with TSMC on Advanced Node Processes Certification and 3D-IC Multiphysics Design Solutions,” Published Apr. 23, 2025 https://investors.ansys.com/news-releases/news-release-details/ansys-strengthens-collaboration-tsmc-advanced-node-processes, captured January 28, 2026
EX1041	TSMC-Cadence Press Release, Published Apr. 24, 2025 https://www.cadence.com/en_US/home/company/newsroom/press-releases/pr/2025/cadence-and-tsmc-advance-ai-and-3d-ic-chip-design-with-certified.html, captured January 28, 2026
EX1042	“TSMC’s Resurgence: What Lies Ahead for the Architect of AI,” Published June 11, 2025 https://www.cmcmarkets.com/en-au/market-news/tsmc-resurgence, captured January 28, 2026
EX1043	Klearman, J., “Decoding TSMC’s Contribution to the AI and 5G Ecosystem” Nov. 20, 2024

	https://graniteshares.com/institutional/us/en-us/research/decoding-tsmc-s-contribution-to-the-ai-and-5g-ecosystem/ , captured January 28, 2026
EX1044	He, A., “In the Global AI Chips Race, China is Playing Catch-Up,” Centre for International Governance Innovation, Published Sept. 18, 2024 https://www.cigionline.org/articles/in-the-global-ai-chips-race-china-is-playing-catch-up/ , captured January 28, 2026
EX1045	“How Military Tensions Are Driving the Next Semiconductor Chip Race,” Microchip USA, Published July 16, 2025 https://www.microchipusa.com/industry-news/how-military-tensions-are-driving-the-next-semiconductor-chip-race , captured January 28, 2026
EX1046	O’Brien, R., “Trump on China Putting - America First,” available at: https://trumpwhitehouse.archives.gov/wp-content/uploads/2020/11/Trump-on-China-Putting-America-First.pdf
EX1047	“NVIDIA CEO Jensen Huang says 'without TSMC, there would be no NVIDIA today,” TweakTown, Published Nov. 9, 2025 https://www.tweaktown.com/news/108766/nvidia-ceo-jensen-huang-says-without-tsmc-there-would-be-no-nvidia-today/index.html , captured January 28, 2026
EX1048	“Nvidia introduces new AI platform featuring six chips made by TSMC,” Taipei Times, Published Jan. 7, 2026 https://www.taipeitimes.com/News/biz/archives/2026/01/07/2003850159 , captured January 28, 2026
EX1049	Search Results from USPTO Public Patent Search https://ppubs.uspto.gov/pubwebapp/ , captured January 28, 2026
EX1050	U.S. Patent No. 10,468,530 B2 to Wang et al.

EX1051	U.S. Patent No. 12,446,255 B2 to Wang et al.
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I. INTRODUCTION

The challenged patent, U.S. Patent No. 7,288,822 (“’822 patent”), issued as a result of multiple Examiner errors: (1) failing to conduct an additional search when, after allowance, the Applicant changed the scope of the claims to fix an “improper term” (per the Applicant) in a key limitation that the Examiner relied on in the Notice of Allowance and (2) identifying the limitation in (1) as novel in the first office action without having searched for that limitation in the prior art. A diligent search – either initially or following the Applicant’s material claim amendment – would have readily established that this limitation was taught by prior art, including the prior art relied upon in the Petition. Institution is warranted to address these material Examiner errors.

Further, the settled expectations of TSMC and its customers outweigh any settled expectations of Marlin and warrant merits consideration. TSMC and its customers had a settled expectation of non-enforcement due to the lack of assertion by UMC, an alleged “primary” competitor of TSMC’s, during the first 14 years of the ’822 patent’s life. During this time, TSMC invested billions of dollars to manufacture FinFET chips, including for American customers who expected to be able to integrate those chips into their own products without incident. Marlin, a foreign entity which only recently acquired the patent, has no comparable expectations.

Institution is also an efficient use of Board resources in view of *Fintiv* because the '822 patent is not currently asserted in a parallel litigation. There is, however, a threat of enforcement, as evidenced by Marlin's claim of infringement and existing lawsuits in the ITC and district court. In response, TSMC diligently challenged the '822 patent's validity in the PTAB to provide a true alternative to district court or ITC litigation. Moreover, this case involves complicated semiconductor technologies, and trained PTAB judges are best suited to adjudicate the merits of the Petition and to correct the past errors of this Office.

Finally, compelling national security, economic, and public interests make review an appropriate use of the Board's resources. TSMC is the world's largest chip maker, by some accounts providing around 90% of the world's advanced chips (e.g., 7nm and smaller). EX1039, 2. Its advanced semiconductor technology is vital to the U.S. supply chain, with a wide range of applications including AI, 5G, health care, and national security and defense. Given TSMC's vital and strategic contribution to the U.S. supply chain, the Administration has a heightened interest in ensuring that the USPTO corrects its error in issuing this patent.

II. INSTITUTION IS WARRANTED IN VIEW OF MATERIAL ERRORS BY THE EXAMINER.

A. The Examiner materially erred by failing to carry out an additional search after Applicant materially amended a key limitation after allowance

The Examiner allowed the '822 patent on the first office action, identifying

the claims' "cell parameter" limitations as the point of alleged novelty.

The following is an examiner's statement of reasons for allowance: The prior art of record does not disclose, make obvious, or otherwise suggest the structure of the applicant's together with the other limitations of the independent claims, such as "a first strained layer of the first conductivity type in a first opening in the second well beside the first gate structure, wherein a difference between a cell parameter of a portion of the first strained layer near a bottom of the first opening and a cell parameter of the substrate is smaller than a difference between a cell parameter of a portion of the first strained layer apart from the bottom of the first opening and the cell parameter of the substrate".

EX1002, p. 63.

However, after the notice of allowance, the Applicant amended the claims to address what the Applicant called "improper terms," by replacing the term "cell parameter" with "lattice parameter." EX1002, p. 72.

a first strained layer of the first conductivity type in a first opening in the second well beside the first gate structure, wherein a difference between a ~~cell~~ lattice parameter of a portion of the first strained layer near a bottom of the first opening and a ~~cell~~ lattice parameter of the substrate is smaller than a difference between a ~~cell~~ lattice parameter of a portion of the first strained layer apart from the bottom of the first opening and the ~~cell~~ lattice parameter of the substrate; and

EX1002, 82. The Applicant replaced this term not only in the claims but throughout the specification, confirming its materiality. *Id.*, 74-81. But despite the Applicant's stated purpose of changing a material term, the Examiner entered these amendments without obtaining approval of a supervisory examiner and without

conducting an additional search. *Id.*, 89.

The Manual of Patent Examining Procedures (M.P.E.P. 8th Ed., Rev. 5 (Aug. 2006)) explains that an Examiner “has authority to enter amendments submitted after Notice of Allowance of an application which ***embody merely the correction of ... formal matters in a claim without changing the scope thereof*** ... without forwarding to the supervisory patent examiner for approval.” M.P.E.P. §714.16. However, “[a]mendments other than those which merely embody the correction of formal matters without changing the scope of the claims ***require approval by the supervisory patent examiner.***” *Id.* Moreover, “[a]s to amendments affecting ... the scope of any claim[,] ... the ***remarks accompanying the amendment must fully and clearly state the reasons ... why the proposed amended or new claims require no additional search or examination.***” *Id.*

These requirements of M.P.E.P. §714.16 were not satisfied here. “Lattice parameter” and “cell parameter” mean different things. On one hand, “lattice parameter” – also referred to as a “lattice constant” – is a well-known term of art describing distance between atoms in a crystal. Pet., 7-8. Conversely, the term “cell parameter” is a coined term without a well-defined meaning in the field of semiconductor technology. For example, within USPC subclass 257/371 (the subclass of the ’822 patent), there are ***zero*** patents that use the term “cell parameter,” whereas 24 patents use the terms “lattice parameter” or “lattice

constant.” EX1049. Thus, contrary to the Applicant’s representation that the “amendments do not change the scope of the claims,” EX1002, 86, the claim amendments were material and should have triggered the requirements of supervisory patent examiner approval and further searching (or an explanation of why such searching was not necessary). Additionally, seeing the change of a limitation underpinning allowable subject matter—which the Applicant called an “improper term[]”—should have immediately triggered a red flag for the Examiner, who, however, merely entered the amendments without conducting addition search.

Had an additional search been carried out using the terms “lattice parameter” and its variants, it would have identified the key references in the Petition: Koontz, Orlowski, and Samoilov. Each of these references includes the terms “lattice” and “lattice constant” and would have been readily located with an additional search. *See* EX1004-Koontz, [0024]; EX1006-Orlowski, 7:22-25; EX1005-Samoilov, [0009]. Conversely, none of these references refer to a “cell” or “cell parameter.”

Institution is warranted for this reason alone. *See, e.g., Anthony, Inc. v. Control-Tec, LLC*, IPR2025-00559, Paper 12 (PTAB July 16, 2025) (noting “[t]he patent examiner issued a notice of allowance . . . as the first office action” and finding that “Petitioner persuasively explains that the patent examiner erred by overlooking the teachings of [a prior art reference in the Petition not located during

prosecution]”); *Yealink (USA) Network Technology Co., Ltd. et al v. Barco NV*

IPR2025-00491, Paper 18, 3 (PTAB June 25, 2025) (finding material error where “the patent examiner appears to have failed to appreciate that ‘[u]nified communication is a term of art’ referring to services such as Skype that are well known in the art”); *Taiwan Semiconductor Mfg. Co. Ltd. v. Marlin Semiconductor Ltd.*, IPR2025-00847, Paper 11, 3-4 (PTAB Sept. 3, 2025) (referring 15-year-old patent based on examiner’s “overlook[ing] certain teachings ... that appear to disclose the claimed features that the examiner indicated were not taught by the prior art of record”).

B. The Examiner materially erred by allowing the claims in the first office action without having searched for the limitation identified as novel in the Notice of Allowance

The Examiner’s failure to carry out an additional search after the Applicant’s material amendment is emblematic of a substandard search that missed multiple key references, resulting in a first action allowance. The Examiner cited just seven background references, none of which even arguably discloses the cell parameter limitations that were identified as the point of alleged novelty. EX1002, p. 64. Applicant similarly did not cite a single reference during prosecution.

Despite identifying the “cell parameter” limitations as the alleged point of novelty, the Examiner *never searched* for this limitation in the prior art. EX1002, p. 54. The Examiner did not include the terms “cell” or “parameter” in any search,

nor any other term or phrase targeting the point of alleged novelty. *Id.* Instead, the Examiner's search focused entirely on well-known background concepts.

Search records confirm the material discrepancy between the scope of the Examiner's search and the point of alleged novelty in the then-presented claims. A complete list of keywords and variants that the Examiner included in searches is shown below.

- **Strained:** “strained,” “strain\$3,” “stress\$3”
- **Conductivity type:** “n,” “n\$1type,” “p,” “doped,” “impurity,” “dopant,” “conduct&5 adj type”¹
- **Opening:** “opening,” “groove,” “trench,” “cavity,” “via”
- **Well:** “well,” “first adj well,” “second adj well”

EX1002, 54-55. A comparison of these terms to claim 1 reveals that each of these keywords relates to the following limitation: “a first **strained** layer of the first **conductivity type** in a first **opening** in the second **well** beside the first gate structure.” However, this limitation merely recites well-known background concepts that the '822 patent itself admits were prior art:

¹ A semiconductor material's conductivity type can be n-type or p-type, which is controlled by introducing dopants, also referred to as impurities, into the material. Pet., 5-6.

FIGS. 1A-1B illustrate a process flow of fabricating a *prior-art MOS transistor* in a cross-sectional view.

Referring to FIG. 1A, a substrate 100 with a **well** 101 therein is provided.... [E]tching is conducted [to] form an opening 110. Referring to FIG. 1B, a **doped strained** layer 112 is formed in the **opening** 110 to serve as an S/D region.

EX1001, 1:22-36.

The Examiner should have known that limiting the search to admitted prior art would have yielded nothing more than background references. The Examiner also should have been aware that the strategy of searching for known background concepts was ineffective given that each of the Examiner's search strings yielded over 100 search results. EX1002, 54-55. At minimum, the abundance of poor-quality results should have triggered the Examiner to try search terms directed to the features that were ultimately identified as novel in the Notice of Allowance. The Examiner's failure to do so constitutes a material Examiner error.

The Examiner's use of ineffective search strings was compounded by the fact that the Examiner omitted relevant USPC classifications from the classification search. For example, expanding the search to include USPC class 438 ("SEMICONDUCTOR DEVICE MANUFACTURING: PROCESS") would

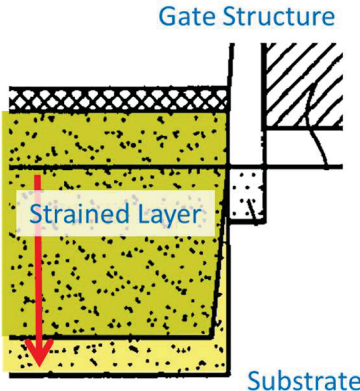
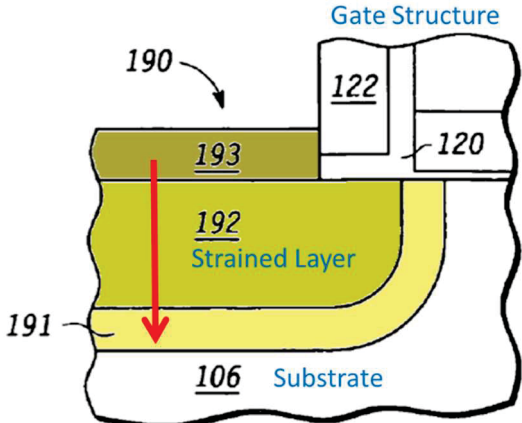
have identified each of the key references. *See* EX1004-Koontz, cover page (USPC subclass 438/301); EX1006-Orlowski, cover page (USPC subclass 438/300); EX1005-Samoilov, cover page (USPC subclass 438/481). The Examiner specifically identified USPC class 438 as a relevant classification yet limited the classification search to USPC class 257 (“ACTIVE SOLID-STATE DEVICES (E.G., TRANSISTORS, SOLID-STATE DIODES)”). EX1002, 42, 54-58; *see* M.P.E.P. §904.02(a) (“The field of search should extend to all probable areas relevant to the claimed subject matter”).

Accordingly, by conducting a search using terms that were divorced from the point of alleged novelty, and omitting relevant USPC classifications, the Examiner failed to locate multiple prior art references that teach this limitation, including the references relied upon in the petition. For this additional and independent reason, the Examiner committed a material error.

III. INSTITUTION IS WARRANTED BECAUSE OF THE STRENGTH OF THE PETITION, WHICH INVALIDATES ALL CLAIMS OVER THREE SEPARATE PRIMARY REFERENCES.

The merits are strong, well-supported, and well-reasoned, and the invalidity positions are straightforward – multiple grounds establish that claim 1 is invalid based on *each of* single-reference obviousness (Koontz), anticipation (Orlowski), and simple obviousness combinations (based on Samoilov). Pet., 3. As set forth in the Petition, each asserted ground teaches all claim 1 limitations, including the

non-uniform lattice parameter limitation allegedly not found in the prior art. For example, the side-by-side figures show the striking similarities between the alleged invention and the disclosure of Orlowski.

'822 patent, Fig. 2 (Excerpt)	Orlowski, Fig. 11
 Decreasing difference in lattice parameter relative to substrate	 Decreasing difference in lattice parameter relative to substrate

The passages below highlight further similarities between the alleged invention and the disclosures of the primary references in the Petition.

'822 patent, claim 1: “[T]his invention provides a semiconductor structure that includes a <i>doped strained</i> layer with a <i>non-uniform</i> lattice parameter distribution.” EX1001, 1:57-62.	Koontz: “[T]he recess structures ... can be <i>doped</i>”; “[R]ecess structures 224 ... have <i>varying</i> compositions of <i>strain</i> material at differing depths.” EX1004, [0026], [0033]
Orlowski: “The composition <i>gradient</i>	Samoilov: “Multiple layers ... may be

in the SiX compound enables the introduction of a <i>doping</i> impurity ... without a significant degradation or relaxation of the <i>stress</i> -inducing characteristics.” EX1006, 5:30-35	deposited in <i>varying</i> order The silicon-containing layers are generally <i>doped</i> ”; “[The] silicon-containing layer is formed with a first lattice <i>strain</i> value.” EX1005, [0032], [0068]
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IV. MERITS CONSIDERATION IS WARRANTED BECAUSE THE SETTLED EXPECTATIONS OF PETITIONER AND OTHERS OUTWEIGH MARLIN’S ALLEGED EXPECTATIONS.

Marlin’s main contention in requesting denial is that the patent issued 18 years ago, allegedly creating “settled expectations” that, alone, effectively override all other considerations. DD Br. (Paper 7), 2-8. Focusing only on Marlin’s expectations, without regard for the expectations of TSMC, its customers, and the public, is not balanced or fair. TSMC, its customers, and the public have “settled expectations,” and they heavily outweigh Marlin’s expectations.

Since acquiring the ’822 patent in June 2021 (EX1028; EX1030), Marlin began an enforcement campaign against the semiconductor industry, including TSMC’s customers. EX2104. And Marlin has since asserted patents against TSMC and its customers in the ITC, seeking an exclusion order. The Petition can resolve patentability of the ’822 patent’s claims before Marlin sues TSMC or its customers and disturbs the parties’ well-settled expectations that the ’822 patent remains dormant.

First, TSMC and its customers had settled expectations that the '822 patent would not be asserted due to the prior patent owner's (UMC's) inaction. TSMC has been engaged in FinFET manufacture since 2013. EX1031, 1. Since the issuance of the '822 patent, TSMC has invested billions of dollars in fabrication facilities to manufacture millions of wafers per year using the FinFET technology, and its customers similarly invested significant resources into designs based on that technology. *See* EX1032. During this time, UMC, who Marlin claims is "TSMC's main competitor," DD Br., 3, remained silent and inactive. *See Apple Inc. v. Ferid Allani*, IPR2025-00856, Paper 11 (September 5, 2025) (informative) (declining to discretionarily deny institution based on Petitioner's expectations that the challenged patent would not be asserted against it after 11 years of Patent Owner inaction).

UMC did not assert this patent against anyone during the first 14 years of the '822 patent's life. Indeed, UMC does not have a history of asserting its patents *at all*. According to DocketNavigator, UMC has been involved in a *total* of 19 patent actions since 1992. EX1038. In most of those cases, UMC was the ITC *respondent* or district court *defendant*. UMC is a listed plaintiff/complainant in only 5 cases, and *none of these* are after 2009. Despite its large patent portfolio, UMC did not have a history of patent enforcement. UMC's inactivity created settled expectations for TSMC and its customers that the patent would remain dormant.

Marlin's activities cannot unwind the settled expectations of TSMC and its customers created by UMC's longstanding inaction with the patent. In analogous bodies of law, the expectations of others would exceed those of a new property owner under such circumstances. *See* Restatement (First) of Prop. § 459 cmt. a (1993) ("Through lapse of time old rights become obscure. A long continued use raises reasonable expectations of its continuance."); *Anaheim Gardens, L.P. v. United States*, 953 F.3d 1344, 1350-51 (Fed. Cir. 2020); *Nordlinger v. Hahn*, 505 U.S. 1, 12-13 (1992) ("[A]n existing owner rationally may be thought to have vested expectations in his property or home that are more deserving of protection than the anticipatory expectations of a new owner at the point of purchase.").

Second, Marlin has not presented persuasive evidence that '822 patent was ever "commercialized, asserted, marked, licensed, or otherwise applied" in the same "particular technology space" where it now seeks enforcement. *Shenzhen Tuozhu Tech. Co., Ltd. v. Stratasys, Inc.*, IPR2025-00531, Paper 10, 3 (PTAB July 17, 2025) (internal quotations omitted). This weighs against any claim by Marlin of "settled expectations." *Id.*; *Home Depot U.S.A., Inc. v. H2 Intellect LLC*, IPR2025-00480, Paper 11, 2-3 (PTAB Sept. 4, 2025) (informative). The '822 patent has not been asserted in litigation in any venue, against any party. EX1029. Marlin alleges that UMC is "another Taiwanese semiconductor foundry" and "TSMC's main business competitor." DD Br., 3. Yet Marlin has not pointed to any

evidence suggesting UMC enforced or demanded a license for the '822 patent against TSMC (or anyone) during the 14 years UMC owned the patent.

Marlin also argues that the '822 patent has been commercialized in the form of licensing with Intel and Samsung. DD Br., 4. Marlin's sole support for this argument is a bare assertion by its corporate representative Paul Ahern (EX2104) that fails to provide *any details* regarding these licenses by which to assess their relevance or significance. And regardless of their scope, it can be inferred that the licenses arose from Marlin's enforcement campaign that started just over a year before the filing of this Petition, by which point the '822 patent was already 17 years old and settled expectations of non-enforcement had long been established. Marlin's licensing-based arguments are therefore readily distinguishable from *Alliance Laundry Sys., LLC v. PayRange LLC*, IPR2025-00950, Paper 11 (September 19, 2025) (informative), where the Patent Owner submitted detailed evidence of the terms of the license (including covered patents and dollar amount) and where there were no settled expectations of non-enforcement because the patent had "not been in force for a significant amount of time (issued in 2021)."

At bottom, when Marlin acquired patents (including the '822 patent) that had never been asserted with the intention of enforcing them, the only reasonable expectation it could have is that their validity would be challenged. *See Anaheim Gardens*, 953 F.3d at 1350-51 ("timing" of property purchase and "knowledge of

the purchaser” are relevant in determining whether purchaser had reasonable investment-backed expectations); *Celgene Corp. v. Peter*, 931 F.3d 1342, 1361-63 (Fed. Cir. 2019) (owners know patents may be subject to post-issuance reconsideration).

Marlin also wrongly argues that TSMC has long been aware of the ’822 patent, asserting that TSMC cited to a family member of the ’822 patent during prosecution of a patent that issued in 2019. This assertion is incorrect. The 2019 patent that Marlin identifies (U.S. 10,468,530) does not cite the ’822 patent or any of its family members. EX1050, 2. Rather, only a much later *continuation* of U.S. 10,468,530 that issued shortly before this IPR was filed cites the ’822 patent family. EX1051, 2. Thus, far from demonstrating a longstanding awareness of the ’822 patent, the facts show that TSMC was unaware of the ’822 patent prior to Marlin’s enforcement campaign.

Finally, Marlin argues that licensing negotiations between the parties beginning in 2024 weigh against any claim of settled expectations by TSMC. DD Br., 6-7 (citing *DataDome S.A. v. Arkose Labs Holdings, Inc.* IPR2025-00693, Paper 13 (PTAB Aug. 14, 2025)). Marlin’s reliance on *DataDome* is unavailing. First, in *DataDome*, there was a parallel proceeding and no argument regarding material error by the Examiner. *DataDome*, Paper 8 at 7-8; Paper 12 at 26-31. Both of these factors differ here and weigh in favor of institution. Moreover, TSMC

filed this Petition just over a year after receiving a licensing proposal, which was followed by a period of evaluation and good faith negotiations, and less than 9 months after those negotiations discontinued due to Marlin asserting patents against TSMC in court. TSMC was far more diligent than the *DataDome* Petitioner who waited over two years after receiving an initial demand and 15 months after refusing a license to file its Petition. *DataDome*, Paper 13 at 7; *DataDome*, EX1013 (Jan. 11, 2023 letter seeking license on one challenged patent).

V. INSTITUTION IS AN EFFICIENT USE OF BOARD RESOURCES.

Institution here is an efficient use of Board resources in view of *Fintiv* because there is no parallel litigation involving the '822 patent. *See, e.g., Intas Pharms. Ltd. v. Atossa Therapeutics, Inc.*, IPR2025-00799, Paper 12, 2-3 (PTAB Aug. 12, 2025); *Azurity Pharms., Inc. v. Helsinn Healthcare S.A.*, IPR IPR2025-00945, Paper 11, 2-3 (PTAB Sept. 19, 2025) (no parallel proceeding and Examiner error outweigh patent owner settled expectations (age of patent and commercialization)). No other tribunal is set to resolve the merits; therefore, no risk of duplicated efforts, inconsistent decisions, or unnecessary expense exists.

Marlin argues this fact is not dispositive because the petitions in *Intel Corp. v. Proxense LLC* were discretionarily denied despite having no *trial date*. DD Br., 7 (citing IPR2025-00327, Paper 12, 2 (PTAB June 26, 2025)). However, in *Intel*, the Acting Director explained the discretionary denial decision was based upon

Petitioner’s failure to “provide any persuasive reasoning as to why an *inter partes* review is an appropriate use of Board resources.” *Intel*, Paper 12 at 2. Here, TSMC presents several compelling reasons why IPR is an appropriate use of resources, e.g., to address the Examiner’s material errors and to resolve the parties’ dispute in an efficient manner avoiding “unnecessary and counterproductive litigation costs” before Marlin asserts this patent in a court against TSMC.

Marlin has already alleged infringement of the ’822 patent and shown a willingness to bring TSMC to court. Institution before litigation promotes the very ideals that underlie the IPR process and is an appropriate use of Board resources.

VI. NATIONAL SECURITY, ECONOMIC, AND PUBLIC INTEREST CONSIDERATIONS STRONGLY FAVOR INSTITUTION.

Marlin acknowledges it has alleged infringement of the ’822 patent by TSMC. EX2104. Given Marlin’s chosen forum for enforcement is the ITC, this threat to weaponize the ’822 patent undermines the U.S. semiconductor supply chain, harming priorities this Administration has made clear are vital to U.S. economic interests and national security. EX1033, 3; EX1034, 1. This makes IPR of the ’822 patent an appropriate use of the Office’s resources—indeed a compelling one. TSMC’s FinFET fabrication capabilities are vital to leading U.S. companies (such as Apple, NVIDIA, Amazon, Broadcom, Qualcomm, and AMD). More specifically, TSMC’s 5 nm processing node supports U.S. advanced semiconductor research and development in industries including AI, health care,

and national security/defense. EX1035, 18-19. Meanwhile, the semiconductor chips that drive artificial intelligence systems, such as NVIDIA's H100, are manufactured with TSMC's 4nm process. EX1044, 2. And NVIDIA's latest B100 and B200 chips, along with the next generation Rubin chips, are manufactured using TSMC's world-leading 3 nm process. *See id.*; EX1047; EX1048. Promoting these emerging industries is an important step in advancing the Administration's priorities. EX1033, 3; EX1034, 1.

Indeed, the U.S. government has recognized AI's importance to national security, and TSMC is an important part of the American AI-dominance strategy. EX1040; EX1041. The semiconductor chips manufactured by TSMC are vital to U.S. industries and to the U.S. military. As Secretary Lutnick explained in April 2025, "national security" is the "key" reason to "bring semiconductors home." EX1033, 3. That has been a key principle of President Trump's agenda: "Our national security depends on bringing our supply chain home. This is especially true when we are dealing with critical technology, computer chips that are not only important to our civilian world ... but also to our military." EX1046, 40.

Moreover, TSMC "produces the advanced processors that Nvidia [] and Apple [] rely on to bring AI to life," including, NVIDIA's next-generation Blackwell AI chips for NVIDIA's AI supercomputers. EX1042, 2. Moreover, healthcare is a key area of projected growth in the AI semiconductor market, where

the demand for “advanced chips—TSMC’s specialty—will continue to surge.”

EX1043, 5. Further, as industry publications report, TSMC’s “3nm and 5nm nodes power everything from smartphones to stealth fighters.” EX1045, 3-4. And the U.S. Air Force estimates “90% of its precision-guided munitions rely on TSMC chips.” *Id.*, 4. And a similar calculus applies to warships, satellites, and communication systems. *Id.* And, blocking or burdening access to TSMC-made advanced semiconductors could create a catastrophic single-point failure for medical R&D, causing direct effects on future patient care and far-reaching consequences for the development of life-saving technology.

Marlin does not dispute the serious impact a ban on importing FinFET products into the United States would have to vital U.S. national security, public health, or economic interests. Instead, Marlin sets up a strawman—painting itself as protector of local industries. DD Br., 10. The facts belie Marlin’s pronouncement. Marlin does not practice the ’822 patent, nor any patent it holds. There is no evidence that Marlin, a foreign entity, has invested in the U.S. semiconductor technology space, except by trying to assert its recently acquired patents. Given Marlin’s assertion of its patents in the ITC against U.S.-based companies (e.g., Apple, Qualcomm, Broadcom), *see* EX1037, Marlin’s arguments that it is a protector of “local industry” ring hollow.

Finally, trying to cast TSMC as a “foreign entity” that “import[s] infringing

products” and must be protected against twists the facts beyond recognition. There is zero evidence, other than a bare, unsupported statement from an interested party, Mr. Ahern, that any product of TSMC infringes any patent in Marlin’s portfolio, including the ’822 patent. Additionally, Marlin ignores TSMC’s commitment to invest \$165 billion in building manufacturing facilities in the United States in support of this Administration’s goal to onshore advanced semiconductor manufacturing to bolster U.S. economic and national security interests. EX1033, 3. Indeed, TSMC’s Arizona facilities are already producing 4nm chips for American customers. EX1036, 2. Marlin’s enforcement campaign against TSMC seeks to damage the core supply chain of semiconductor chips from TSMC to the United States. These considerations therefore warrant institution.

VII. CONCLUSION

For these reasons, the Director should deny Marlin’s request to discretionarily deny this IPR and should institute review of the challenged claims.

Respectfully submitted,

/Haixia Lin/

Haixia Lin, Reg. No. 61,318

Dated: January 29, 2026

CERTIFICATION OF SERVICE (37 C.F.R. § 42.6(e))

The undersigned hereby certifies that, on January 29, 2026, true and correct copies of the foregoing **PETITIONER'S OPPOSITION TO PATENT OWNER'S DISCRETIONARY DENIAL REQUEST** and **Exhibits EX1028-1051** were served electronically via e-mail in their entirety on the following counsel for Patent Owner:

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