

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY LTD.,

Petitioner,

v.

MARLIN SEMICONDUCTOR LIMITED.

Patent Owner.

Case No. IPR2026-00058

U.S. Patent No. 7,288,822 B2

**PATENT OWNER'S PRELIMINARY RESPONSE
PURSUANT TO 37 C.F.R. § 42.107(a)**

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TABLE OF EXHIBITS

Exhibit	Description
2001	Declaration of Joseph C. McAlexander III
2002	Peter Van Zant, <i>Microchip Fabrication, A Practical Guide to Semiconductor Processing</i> , (4 th ed. 2000)
2003	<i>Curriculum Vitae</i> of Joseph C. McAlexander III
2101	Website: Foundries to Grow Faster than Integrated Circuits in 2016 (https://marketrealist.com/2015/12/foundries-grow-faster-integrated-circuits-2016/)
2102	Website: Ranked: Semiconductor Foundries by Revenue Share (www.visualcapitalist.com/ranked-semiconductor-foundries-by-revenue-share/)
2103	Website: US Patent No. 7,288,822 B1 – Semiconductor Structure And Fabricating Method Thereof – Google Patents https://patents.google.com/patent/US7288822B1/en?q=7288822
2104	Declaration of Paul Ahern Regarding Patent Owner’s Request for Discretionary Denial of Institution

I. INTRODUCTION

The Petition should be denied because all grounds fail to disclose or render obvious claim element [1.d]: “a first strained layer of the first conductivity type in a first opening in the second well beside the first gate structure, ***wherein a difference between a lattice parameter of a portion of the first strained layer near a bottom of the first opening and a lattice parameter of the substrate is smaller than a difference between a lattice parameter of a portion of the first strained layer apart from the bottom of the first opening and the lattice parameter of the substrate.***” This element is required by all challenged claims.

Each of the Petition’s Grounds is premised on an oversimplification of element [1.d] that ignores key claim limitations. Specifically, each of Grounds 1A, 2, and 3A—the only grounds challenging independent claim 1—are based on the faulty premise that element [1.d], in the Petition’s words, requires only “that the strained layer next to the gate has a non-uniform lattice parameter.” Pet., 25 (Ground 1A), 59 (Ground 2), 78 (Ground 3A). The Petition’s analysis therefore focuses on whether the strained layer has a non-uniform lattice parameter. But that is an inaccurate statement of what the claim language recites, because it ignores the claim language regarding “a difference between a lattice parameter of a portion of the first strained layer . . . and ***a lattice parameter of the substrate.***” Element [1.d] requires that the ***difference*** between the lattice parameter of the substrate and the lattice

parameter of the strained layer is ***smaller near the bottom*** of the opening than at a portion apart from the bottom, not merely that the strained layer have a non-uniform lattice parameter as the Petition alleges. None of the Petition Grounds disclose or render obvious this requirement.

None of the asserted grounds meaningfully address the lattice parameter of the substrate. The Petition assumes inherency of two facts in all its prior art references, neither of which is inherent or true: (1) that the substrate is necessarily 100% silicon or close to it, so that discussion of the composition of the alleged strained layer is sufficient to disclose the amount of difference between the lattice parameter of the strained layer and that of the substrate, and (2) that the substrate necessarily has a uniform lattice parameter throughout, so that discussion of variation in the alleged strained layer implies how the difference in lattice parameter between strained layer and substrate varies. *See* Pet., 60. Neither is true, and both individually cause the Petition's arguments to fail. Substrates are "doped" with additional material, such that they are not 100% silicon, for at least two reasons: (1) to modify resistivity and (2) to create conductive wells of a particular conductivity. EX2001-McAlexander-Decl., ¶39. This doping process changes the composition of the substrate such that it is not 100% silicon and may also affect the lattice parameter of the substrate. *Id.* Moreover, the dopant may not be introduced uniformly throughout the substrate, which would cause the substrate to have a non-uniform

lattice parameter. *Id.* Thus, the Petition's assumptions that the substrate is necessarily nearly 100% silicon and has a uniform lattice parameter throughout are incorrect, and so its complete lack of proof as to the (potentially varying) lattice parameter of the substrate is fatal to its conclusions, which are entirely based on analysis of the alleged strained regions in the prior art references.

Specifically, for Grounds 1A and 1B, the Petition relies on Koontz's disclosure that an alleged strained layer "can vary in composition vertically from bottom to top." But this bare disclosure does not support the Petition's conclusion that Koontz discloses or renders obvious "a difference between a lattice parameter of a portion of the first strained layer near a bottom of the first opening and a lattice parameter of the substrate is smaller than a difference between a lattice parameter of a portion of the first strained layer apart from the bottom of the first opening and the lattice parameter of the substrate." The Petition also points to Koontz's disclosure of increasing the magnitude of induced strain in the channel region underneath the gate but neither Koontz nor the Petition explain any correlation between the claimed difference in lattice parameters and this disclosure.

For Ground 2, the Petition alleges that in Orłowski, the percentage of silicon in the alleged strained layer decreases from the bottom to the top. Similar to Grounds 1A and 1B, this does not support the Petition's conclusion that Orłowski discloses "a difference between a lattice parameter of a portion of the first strained layer near

a bottom of the first opening and a lattice parameter of the substrate is smaller than a difference between a lattice parameter of a portion of the first strained layer apart from the bottom of the first opening and the lattice parameter of the substrate.” This is especially so given that Ground 2 is an anticipation-only ground.

For Grounds 3A and 3B, the Petition relies on Samoilov’s statement that “[m]ultiple SiGe-containing layers containing varying amount of elements may be stacked to form silicon-containing layer 140 with a graded elemental concentration.” As with the above grounds, the Petition concludes, without adequate support or explanation, that this renders obvious “a difference between a lattice parameter of a portion of the first strained layer near a bottom of the first opening and a lattice parameter of the substrate is smaller than a difference between a lattice parameter of a portion of the first strained layer apart from the bottom of the first opening and the lattice parameter of the substrate.”

In summary, all of the Petition Grounds require unsupported leaps in logic to reach the conclusion that element [1.d] is disclosed or rendered obvious. Accordingly, the Petition fails to establish the required likelihood of success of any ground. Institution should therefore be denied.

II. SEMICONDUCTOR TRANSISTOR TECHNOLOGY PRIMER

The following is a brief primer of semiconductor transistors to establish a foundation of common terms and concepts that can be used in addressing the defects in the Petition.

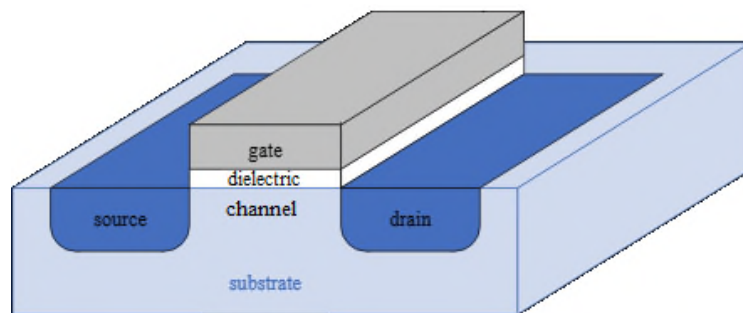
A. Basic Transistor Components

Today's semiconductor devices trace their lineage back to the first computers of the 1940s, which used vacuum tubes to perform two key electrical functions: switching (*i.e.*, turning access to electrical current on and off) and amplification (*i.e.*, increasing the amplitude of a signal while retaining its electrical characteristics). EX2002 at 1-2; EX2001-McAlexander-Decl, ¶17. Where earlier tube devices used a vacuum tube to control the flow of electrons (turning electrical current on and off), today's semiconductor devices use transistors. EX2002 at 3; EX2001-McAlexander-Decl, ¶17.

One type of transistor typically used in an integrated circuit (or "chip") is a "field effect transistor," or FET. EX2001-McAlexander-Decl, ¶18. Materials used to build such transistors are divided into three categories based on their ability to conduct electrical current: conductors, dielectrics, and semiconductors. EX2002 at 29-34; EX2001-McAlexander-Decl, ¶18. In a conductor (*e.g.*, a metal), electric current can flow freely. EX2002 at 29; EX2001-McAlexander-Decl, ¶18. A dielectric (*e.g.*, silicon dioxide) is an insulative material at the opposite end of the

conductivity spectrum and has a high resistance to the flow of current. EX2002 at 30; EX2001-McAlexander-Decl, ¶18. Semiconductors (*e.g.*, silicon) fall between conductors and dielectrics and have some conducting and some resisting ability. EX2002 at 31-34; EX2001-McAlexander-Decl, ¶18.

The simplified FET below illustrates how these materials may be used to create a semiconductor transistor device. EX2001-McAlexander-Decl, ¶19. As shown, the transistor is built on a semiconductor substrate and comprises a source, a drain, a gate, and a channel. *See, e.g.*, EX2002 at 510-511. The source, drain and channel comprise semiconductor material, the gate comprises a conductor, and the gate and channel are separated by a thin dielectric layer.



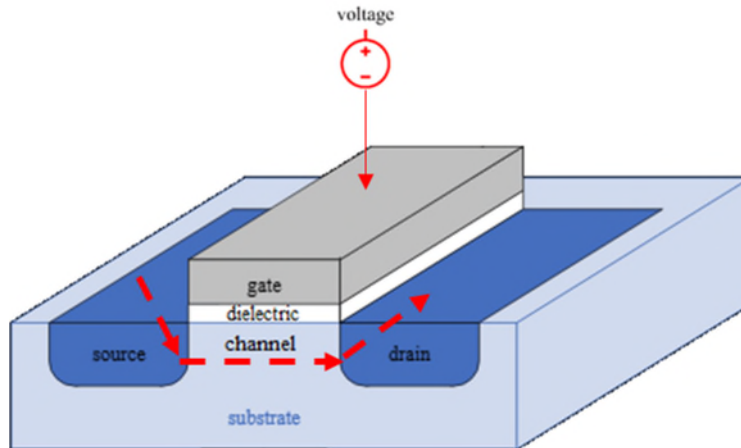
See, e.g., EX2002 at 510-511; EX2001-McAlexander-Decl, ¶19.

The source and drain are regions in the semiconductor substrate that are either rich in electrons (a negative, or n-type, region) or rich in holes (a positive, or p-type, region). EX2002 at 26-28, 427-28; EX2001-McAlexander-Decl, ¶20. The channel is a region under the gate and between the source and drain, and is of the opposite type to that of the source and drain. In other words, if the source and drain are n-

type regions, then the channel will be a p-type region (and vice versa). EX2002 at 510-511; EX2001-McAlexander-Decl, ¶20.

The gate is a conductor (or semiconductor) located above the channel. EX2001-McAlexander-Decl, ¶21. In this simplified version of a FET, there is a dielectric between the channel and the gate. EX2002 at 510-511; EX2001-McAlexander-Decl, ¶32. When a voltage is applied to the gate, the dielectric prevents the “flow of charge” (current) between the gate and the channel, but the applied voltage results in the creation of a “field effect” in the channel. EX2002 at 510-511; EX2001-McAlexander-Decl, ¶21. This “field effect” either builds up or depletes the charges in the channel (depending on whether it is a p- or n-type channel). EX2002 at 510-511; EX2001-McAlexander-Decl, ¶21.

As illustrated below, this field effect allows charge to flow from the source, through the channel, to the drain. EX2001-McAlexander-Decl, ¶22. Thus, selectively applying voltage to the gate switches the transistor on and off, starting and stopping drain-to-source or source-to-drain current. EX2001-McAlexander-Decl, ¶22.



B. Processes For Manufacturing Integrated Circuits And Transistors

1. The Four Stages Of Fabricating Integrated Circuits

The intricate, complex manufacturing process developed over the years for achieving such highly-dense integrated circuits can be divided into four distinct stages: (1) material preparation; (2) wafer preparation; (3) wafer fabrication; and (4) packaging. EX2001-McAlexander-Decl, ¶23.

In the first stage, the semiconductor material itself is created. EX2002 at 13. For a silicon semiconductor, the raw starting material is sand, which is converted to pure silicon with a polysilicon structure. EX2002 at 13; EX2001-McAlexander-Decl, ¶24.

In the second stage, the semiconductor material is first formed into a silicon crystal with specific electrical and structural parameters, and it is then sliced into thin disks called “wafers.” EX2002 at 13-14; EX2001-McAlexander-Decl, ¶25. A

wafer acts as a semiconductor substrate on and in which transistors may be formed.

EX2001-McAlexander-Decl, ¶25.

The third stage is wafer fabrication, during which individual integrated circuits are formed in and on the wafer semiconductor substrate. EX2002 at 14; EX2001-McAlexander-Decl, ¶26. Thousands of integrated circuits can be formed on the substrate of a single wafer. EX2002 at 14; EX2001-McAlexander-Decl, ¶26.

In the packaging stage, the wafer is separated into individual chips. EX2002 at 14-15; EX2001-McAlexander-Decl, ¶27.

2. The Wafer Fabrication Stage

The third manufacturing stage, wafer fabrication, is the one most relevant here, and it can take several thousand steps, during which transistors and other devices are formed in and on the wafer's substrate. EX2002 at 14; EX2001-McAlexander-Decl, ¶28. These steps are generally performed using three categories of materials (conductors, semiconductors, and dielectrics) in four basic operations (layering, patterning, doping, and heat treatments). See EX2002 at 29-31, 71; EX2001-McAlexander-Decl, ¶28. For purposes of understanding the Petition and its deficiencies, the most important basic operations are layering, patterning, and doping. EX2001-McAlexander-Decl, ¶28.

Layering is the operation used to add thin layers to the semiconductor substrate. EX2002 at 72; EX2001-McAlexander-Decl, ¶29. The layers may be

conductors, semiconductors, or dielectrics; and they can have a variety of functions and be made in a variety of ways. EX2002 at 72; EX2001-McAlexander-Decl, ¶29.

For example, one way of adding a layer of material is to deposit that material onto the semiconductor substrate. EX2001-McAlexander-Decl, ¶30. Another way of adding a layer of material is to grow the material on the semiconductor substrate. *Id.* After an initial layer is added to the semiconductor substrate, additional layers may be added to the earlier layers using similar growth or deposition processes. *Id.* To illustrate, the transistor structure shown below shows a number of layers that have been added to the wafer's semiconductor substrate, some deposited, some grown. EX2002 at 72; EX2001-McAlexander-Decl, ¶30.

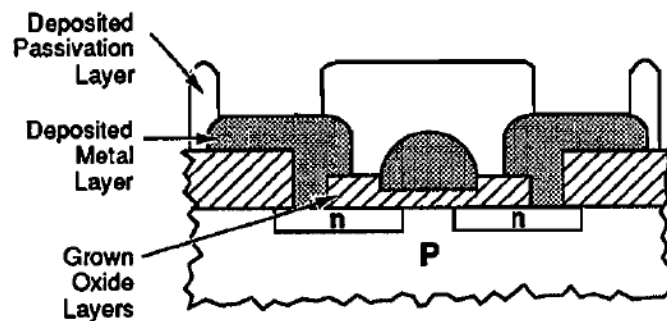


Figure 4.4 Cross section of completed metal gate MOS transistor with grown and deposited layers.

Patterning is the series of steps to remove (etch away) selected portions of the semiconductor substrate or one or more layers of materials that were added during one or more prior layering operations. EX2002 at 72-73; EX2001-

McAlexander-Decl, ¶31. This creates a pattern on the wafer surface. EX2002 at 72-73; EX2001-McAlexander-Decl, ¶31.

The patterning may result in one or more holes in the layered material or one or more remaining islands of material. EX2002 at 72-73; EX2001-McAlexander-Decl, ¶32. For example, the following figures illustrate the use of patterning to make (1) a hole in a previously formed layer: and (2) an island from a previously formed layer:

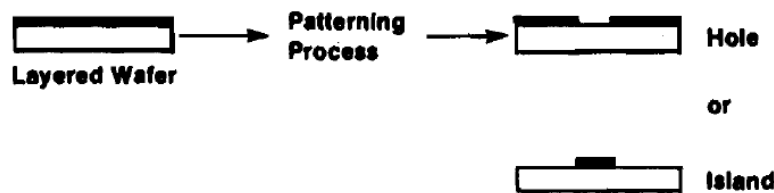


Figure 4.7 Patterning.

EX2001-McAlexander-Decl, ¶32.

The repeated combination of layering and patterning in different sequences and variations is critical to the formation of transistors in and on the semiconductor wafer:

These parts are created one layer at a time by the combination of putting a layer on the surface and removing a portion, with a patterning process, to leave a specific shape. The goal of the patterning operations is to create the desired shapes in the exact dimensions (feature size) required by the circuit design, and to locate them in their proper location on the wafer surface and in relation to the other parts.

EX2002 at 73; EX2001-McAlexander-Decl, ¶33.

Doping: Impurities are intentionally introduced during the transistor fabrication process to enhance the conductivity of a given material or to create an isolation region that impedes conductivity. Various, well-known techniques, such as high temperature diffusion and ion implantation, are used to introduce impurities into selective regions of a semiconductor substrate and/or into different layers created during the layering and patterning processes. EX2002 at 31-34; EX2001-McAlexander-Decl, ¶34.

III. THE CHALLENGED '822 PATENT

The challenged '822 patent provides a semiconductor structure in which “the difference between the lattice parameter of a portion of the strained layer near the bottom of the opening and the lattice parameter of the substrate is smaller than the difference between the lattice parameter of a portion of the strained layer apart from the bottom of the opening and the lattice parameter of the substrate.” EX1001, 4:13-19. “Thus, less defects occur at the interface of the strained layer and the substrate.” *Id.*, 4:19-20. “Moreover, since a silicon layer is formed on the strained layer before the metal silicide layer is formed, the non-silicon IV-group element does not enter the metal silicide layer in the silicide process, so that the quality of the metal silicide layer is not degraded.” *Id.*, 4:20-24.

IV. THE PETITION FAILS TO ESTABLISH THE REQUIRED LIKELIHOOD OF SUCCESS

The Petition asserts the following grounds:

Ground	Claim(s) Challenged	35 U.S.C. §	Reference(s)
1A	1-7, 9, 11-13	§103	Koontz
1B	8, 10, 14	§103	Koontz, Sridhar
2	1-4	§102	Orlowski
3A	1-7, 9, 11-13	§103	Samoilov, Murthy
3B	8, 10, 14	§103	Samoilov, Murthy, Sridhar

Pet., 3. The Petition fails to establish the required likelihood of success because all grounds fail to disclose or render obvious “wherein a difference between a lattice parameter of a portion of the first strained layer near a bottom of the first opening and a lattice parameter of the substrate is smaller than a difference between a lattice parameter of a portion of the first strained layer apart from the bottom of the first opening and the lattice parameter of the substrate.”

A. Grounds 1A and 1B

In Ground 1A, the Petition alleges that Koontz renders obvious independent claim 1 and dependent claims 2-7, 9, and 11-13, which depend from claim 1. Pet., 19. In Ground 1B, the Petition alleges the combination of Koontz and Sridhar renders obvious dependent claims 8, 10, and 14, which depend from claim 1. Pet., 40. Both of these grounds fail because Koontz does not disclose or render obvious element [1.d].

Regarding element [1.d], the Petition alleges that “[t]his limitation requires that the strained layer next to the gate has a non-uniform lattice parameter, meaning

that its atoms are organized as a crystal lattice, but the distance between those atoms (i.e., the lattice parameter) varies vertically.” Pet., 25. But this statement does not accurately reflect what the claim language recites, because it ignores the claim language regarding “a lattice parameter of the substrate.” Element [1.d] requires that the **difference** between the lattice parameter of the substrate and the lattice parameter of the strained layer is **smaller near the bottom** than at a portion apart from the bottom, not merely that the strained layer must have a non-uniform lattice parameter as the Petition alleges. For example, even if a strained layer has a non-uniform lattice parameter, as the Petition alleges is sufficient, it could be non-uniform such that the lattice parameter of strained layer is further from the lattice parameter of the substrate at the bottom, rather than at the top (as required by the claims), because there is no discussion of the substrate lattice parameter in Koontz. Such a scenario, which the Petition would argue meets the claim limitations, would clearly contradict the express language of element [1.d]. The Petition’s analysis is thus deficient in that it is based on an inaccurate statement of what the claim language requires.

As an initial matter, even under the Petitioner’s misstatement of what the claim requires (the strained layer merely having a non-uniform lattice parameter), Ground 1A would fail, as no such structure is disclosed in Koontz. The Petition alleges that Koontz discloses that the strained layer has a non-uniform lattice parameter because Koontz states that “recess structures 446”—the alleged strained

layer—“can vary in composition vertically from bottom to top of the structures 446.” Pet., 25 (quoting EX1004-Koontz, ¶[0063]). But a POSITA would have understood that a variation *in composition* does not necessarily indicate a non-uniform *lattice parameter*. EX2001-McAlexander-Decl., ¶38, For example, a compound may consist of two elements of a similar size, such that varying the composition of the compound would not change the lattice parameter of the compound. *Id.* Moreover, even with elements of varying sizes, varying the composition may still result in a uniform lattice parameter due to other variables, such as temperature, that change how the elements bond together. *Id.* The Petition (and Petitioner’s expert) do not address these issues at all.

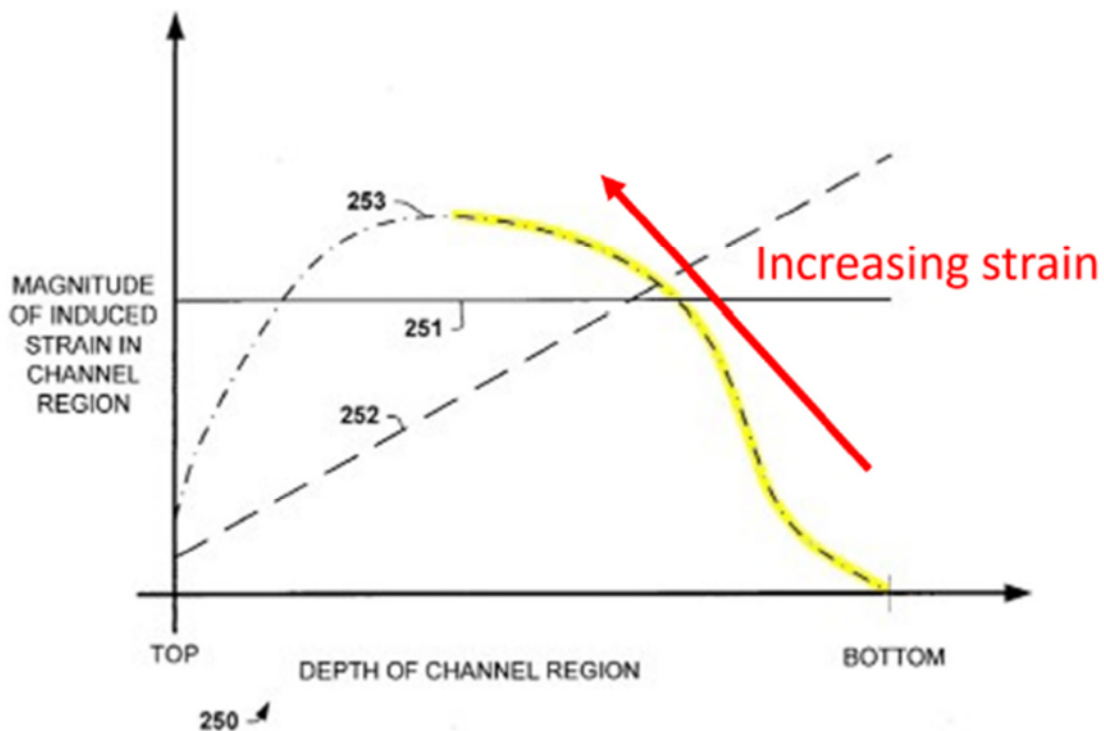
Even if the Petition were correct that Koontz’s “recess structures 446” have a non-uniform lattice parameter, this still would not be sufficient to render obvious element [1.d] because it assumes, without support, that the lattice parameter of the substrate is uniform. A semiconductor substrate may not have a uniform lattice parameter due to non-uniform doping. EX2001-McAlexander-Decl., ¶39. For example, wafers for semiconductor manufacturing are sold based on their resistivity. *Id.* For this reason, these wafers are “doped” with additional impurities to modify their resistivity. Additionally, the challenged claims require “a substrate, having therein a first well of a first conductivity type and a second well of a second conductivity type.” In order to create conductive wells of the proper type (n-type

wells associated with p-type transistors, and p-type wells associated with n-type transistors), the substrate must be doped by introducing a particular impurity to the substrate (typically phosphorous for an n-well and boron for a p-well). EX2001-McAlexander-Decl., ¶39. This doping process changes the composition of the substrate and may also affect the lattice parameter of the substrate. *Id.* Moreover, the dopant may not be introduced uniformly throughout the substrate, which would cause the substrate to have a non-uniform lattice parameter. *Id.* Thus, Grounds 1A and 1B are premised on an incorrect and unsupported assumption regarding the lattice parameter of the substrate.

Moreover, the Petition's argument is that "the lattice parameter of these structures [recessed structures 446 in Koontz] can vary **layer by layer**, which allows engineers to shape the strain profile throughout the depth of the channel." Pet., 27. But the claims require more—the variation of lattice constant as claimed occur within **the same layer**: "a difference between a lattice parameter of a portion **of the first strained layer** near a bottom of the first opening and a lattice parameter of the substrate is smaller than a difference between a lattice parameter of a portion **of the first strained layer** apart from the bottom of the first opening and the lattice parameter of the substrate." Ex 1001, claim 1. Further, there is no disclosure in Koontz or elsewhere cited in the Petition of "changing the percentage of germanium [sic] in the silicon-germanium mixture," as the Petition alleges, and it is not implicit

or implied by the statement that the recess structure 446 “can vary in composition vertically.” Pet., 25.

Regardless, Koontz does not render obvious the specific requirements of element [1.d]: “wherein a difference between a lattice parameter of a portion of the first strained layer near a bottom of the first opening and a lattice parameter of the substrate is smaller than a difference between a lattice parameter of a portion of the first strained layer apart from the bottom of the first opening and the lattice parameter of the substrate.” The Petition admits that “Koontz does not specifically state that the difference between the lattice parameter of the strained layer and that of the substrate increases from bottom to top, as claimed.” Pet., 26. Instead, the Petition argues that Koontz renders obvious element [1.d] because “Koontz discloses that the induced strain in the channel region underneath the gate increases from the bottom to the top of the channel, as shown in Figures 2C and 2B.”



Pet., 26 (showing annotated EX1004-Koontz, Fig. 2C). The Petition alleges that “Koontz explains that there is a direct correlation between the lattice parameter of the recessed structures 446 and the strain in the channel: increasing the difference between the lattice parameter of recessed structures 446 and that of the substrate increases the strain in the channel, and vice versa.” Pet., 28 (quoting EX1004-Koontz, ¶¶[0063]; *see also id.*, [0033]-[0036], [0059). Not so. Koontz does not say this, and none of the cited paragraphs of Koontz support the Petition’s allegation. Paragraph [0063] merely states that “the resulting compressive strain can be increased or decreased by correspondingly increasing or decreasing **one or more components of the tensile strain producing material.**” EX1004-Koontz, ¶[0063] (emphasis added). It does not mention lattice parameters at all, much less that

increasing the difference between the lattice parameter of recessed structures 446 and that of the substrate increases the strain in the channel. *Id.*

Put simply, the Petition fails to explain how Koontz's disclosure of increasing ***induced strain in the channel region underneath the gate*** renders obvious element [1.d]'s requirement that the ***difference between the lattice parameter of the strained layer next to the gate and the lattice parameter of the substrate*** increases from bottom to top. A POSITA would have understood that strain in the channel region can be induced in many different ways, other than through a difference in lattice parameters, much less a difference in varying lattice parameters of material beside the gate. EX2001-McAlexander-Decl., ¶43. For example, local strain can be induced through other techniques, such as silicidation of the source/drain regions or a contact etch stop layer above the gate. *Id.* Indeed, the '822 patent specifically discloses disposing contact etching stop layers and a metal silicide layer as alternative ways to create strain, distinct from the claimed method. EX1001, 6:3-18. Accordingly, Koontz does not render obvious element [1.d] and Ground 1A fails.

Ground 1B adds the Sridhar reference to address additional limitations of claims depending from independent claim 1. Pet., 40. Ground 1B does not provide any further analysis regarding claim 1. Pet., 40-51. Thus, Ground 1B fails for the same reasons as Ground 1A.

B. Ground 2

In Ground 2 the Petition alleges that Orlowski anticipates claims 1-4. Pet., 51. Notably, Ground 2 is an anticipation-only ground, alleging invalidity only under §102. Ground 2 fails because Orlowski fails to disclose element [1.d].

Regarding element [1.d], the Petition again alleges that “[t]his limitation requires that the strained layer next to the gate has a non-uniform lattice parameter.” Pet., 59. As explained above in Section IV.A, this is incorrect. The Petition’s analysis is deficient in that it does not meaningfully address the claim language regarding “a lattice parameter of the substrate.”

The Petition points to Orlowski’s disclosure that “the percentage of silicon in SISD structure[] 190 decrease[s] from the bottom of SISD structures 190 to the top.” Pet., 59 (quoting EX1006-Orlowski, 8:41-45; *see also id.*, 7:22-28). The Petition claims, without support, that “the closer one gets to the bottom of the of [sic] strain inducing source/drain structures 190, the closer the composition of the silicon-germanium mixture gets to the composition of substrate 101 (where the percentage is close to 100% silicon).” Pet., 60 (no citation). But contrary to the Petition’s allegations, Orlowski does not disclose that the composition of the alleged substrate is close to 100% silicon, or that the difference between the lattice parameters of the SISD and the substrate increases if the percentage of silicon in the SISD increases. Rather, these are assumptions that the Petition makes, without support or

explanation. Moreover, the Petition argues that “wafer 101” is the claimed substrate, and argues that it is “close to 100% silicon,” but that is incorrect because it is a silicon-on-insulator structure, in which a significant portion of wafer 101 is made up of “buried oxide (BOX) layer 104,” which is not silicon. Pet., 60; EX1006-Orlowski, Figs. 1-13, 3:9-16; *supra* at 2; EX-2001-McAlexander-Decl., ¶46. Further, as explained above, in order to create conductive wells of the proper type (n-type wells associated with p-type transistors, and p-type wells associated with n-type transistors), the substrate must be doped by introducing a particular impurity to the substrate (typically phosphorous for an n-well and boron for a p-well). EX2001-McAlexander-Decl., ¶46. This doping process changes the composition of the substrate such that the substrate is not 100% silicon and may also affect the lattice parameter of the substrate. *Id.* Moreover, the dopant may not be introduced uniformly throughout the substrate, which would cause the substrate to have a non-uniform lattice parameter. *Id.* Thus, Ground 2 is premised on an incorrect and unsupported assumption regarding the lattice parameter of the substrate.

Thus, for this separate and additional reason, the Petition’s argument regarding the strained layer’s lattice constant compared to the substrate’s alleged implicit lattice constant, which is not discussed, fails. Pet., 59-61. *See Verdegaa Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631 (Fed. Cir. 1987) (“A claim

is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference.”).

Moreover, although Orlowski states repeatedly that the lattice constant of the SSID structures are different from that of the surrounding material, it never states that the SSID has a varying lattice constant itself. EX1006-Orlowski, Abstract, 2:34-45, 5:4-23. A POSITA would know that given the emphasis by the inventors on the former, if the latter were true, the applicant would have said so at least once. Instead, a POSITA would view the lattice constant (always referred to in the singular in Orlowski) of the SSID structures as being constant. Much less does Orlowski say specifically that the lattice constant of the SSID structures is closer to that of the substrate at the bottom than it is at the top, and rather than, for example, the reverse.

Accordingly, Orlowski does not disclose element [1.d] and Ground 2 fails.

C. Grounds 3A and 3B

In Ground 3A, the Petition alleges that the combination of Samoilov and Murthy renders obvious independent claim 1 and dependent claims 2-7, 9, and 11-13, which depend from claim 1. Pet., 64. In Ground 3B, the Petition alleges the combination of Samoilov, Murthy, and Sridhar renders obvious dependent claims 8, 10, and 14, which depend from claim 1. Pet., 95. Both of these grounds fail because Samoilov and Murthy do not disclose or render obvious element [1.d].

Regarding element [1.d], the Petition again alleges that “[t]his limitation requires that the strained layer next to the gate has a non-uniform lattice parameter.” Pet., 78. As explained above in Section IV.A, this is incorrect. The Petition’s analysis is deficient in that it does not meaningfully address the claim language regarding “a lattice parameter of the substrate.”

The Petition relies on Samoiloﬀ’s statement that “[m]ultiple SiGe-containing layers containing varying amount of elements may be stacked to form silicon-containing layer 140 with a graded elemental concentration.” EX1005-Samoiloﬀ, ¶[0030]; Pet., 83-84. The Petition points to an embodiment in which “a first SiGe-layer may be deposited with a germanium concentration in a range from about 15 at % to about 25 at % and a second SiGe-layer may be deposited with a germanium concentration in a range from about 25 at % to about 35 at %.” EX1005-Samoiloﬀ, ¶[0030]; Pet., 78-79. The Petition then concludes, without explanation, that one would be above the other, with no support in the reference itself: “a POSITA would have understood the lattice parameter at the bottom of silicon-containing layer 140 (where the concentration of germanium or carbon is lower) more closely matches the lattice parameter of the substrate than does the rest of silicon-containing layer 140.” Pet., 79.

The Petition’s analysis is wholly inadequate. **First**, the Petition presumes that in the cited example in Samoiloﬀ, the layer containing less germanium is at the

bottom and the layer containing more germanium is at the top, but Samoilov does not say this, as explained above. *Compare* Pet., 78-79 (Petitioner arguing that “[i]n one example, a silicon-germanium sub-layer near the bottom has a ‘germanium concentration in a range from about 15[]% to about 25[]%’ whereas a sub-layer apart from the bottom has a ‘germanium concentration in a range from about 25[]% to about 35[]%.’”) *with* EX1005-Samoilov, ¶[0030] (“a first SiGe-layer may be deposited with a germanium concentration in a range from about 15 at % to about 25 at % and a second SiGe-layer may be deposited with a germanium concentration in a range from about 25 at % to about 35 at %.”). **Second**, even if the Petition were correct about the ordering, it still does not establish why this necessarily means that “a difference between a lattice parameter of a portion of the first strained layer near a bottom of the first opening and a lattice parameter of the substrate is smaller than a difference between a lattice parameter of a portion of the first strained layer apart from the bottom of the first opening and the lattice parameter of the substrate,” as element [1.d] recites. The Petition makes no allegation that Samoilov teaches or suggests anything about the lattice parameter of the substrate. **Third**, Samoilov never states that the two layers the Petition relies on, EX1005-Samoilov, ¶[0030] (referring to “a first SiGe-layer” that is deposited, followed by “a second SiGe-layer,” that is subsequently and separately deposited), have different lattice constants. Samoilov does point out that SiGe and SiC have different lattice constants

from Silicon, one larger and one smaller, to be used for PMOS and NMOS, respectively. EX1005-Samoilov, ¶¶ [0009], [0068]. But the claims require the variation of lattice constant as claimed occur within *the same layer*: “a difference between a lattice parameter of a portion *of the first strained layer* near a bottom of the first opening and a lattice parameter of the substrate is smaller than a difference between a lattice parameter of a portion *of the first strained layer* apart from the bottom of the first opening and the lattice parameter of the substrate.” Ex 1001, claim 1. **Fourth**, as explained above, the lattice parameter of the substrate cannot be assumed because the whole wafer is doped and is thus not necessarily purely silicon, and the substrate may not have a uniform lattice parameter due to non-uniform doping of the wells. EX2001-McAlexander-Decl., ¶52. For example, wafers for semiconductor manufacturing are sold in part based on their resistivity. *Id.* For this reason, these wafers are “doped” with additional impurities to modify their resistivity. Additionally, the challenged claims require “a substrate, having therein a first well of a first conductivity type and a second well of a second conductivity type.” In order to create conductive wells of the proper type (n-type wells and p-type wells), the substrate must be doped by introducing a particular impurity to the substrate (typically phosphorous for an n-well and boron for a p-well). EX2001-McAlexander-Decl., ¶52. This doping process changes the composition of the substrate and may also affect the lattice parameter of the substrate. *Id.* Moreover,

the dopant may not be introduced uniformly throughout the substrate, which would cause the substrate to have a non-uniform lattice parameter. *Id.* Thus, Grounds 3A and 3B are premised on an incorrect and unsupported assumption regarding the lattice parameter of the substrate.

Accordingly, Samoilov does not disclose or render obvious element [1.d] and Ground 3A fails.

Ground 3B adds the Sridhar reference to address additional limitations of claims depending from independent claim 1. Pet., 95. Ground 3B does not provide any further analysis regarding claim 1. Pet., 95-104. Thus, Ground 3B fails for the same reasons as Ground 3A.

V. CONCLUSION

For the above reasons, the Petition should be denied.

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CERTIFICATE OF SERVICE

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