

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY LTD.,

Petitioner,

v.

MARLIN SEMICONDUCTOR LIMITED.

Patent Owner.

Case No. IPR2026-00058

U.S. Patent No. 7,288,822 B2

DECLARATION OF JOSEPH C. MCALEXANDER III REGARDING PATENT
OWNER'S PRELIMINARY RESPONSE

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I. QUALIFICATIONS

1. I am a Registered Professional Engineer (#79454) and the President of McAlexander Sound, Inc. I hold a Bachelor of Science degree in Electrical Engineering from North Carolina State University. I have been associated with the integrated circuit and electronics industry as a designer and consultant for the past 53 years and am a named inventor on 31 U.S. patents and a number of foreign patents, many of which are directly related to the design and operation of transistors and circuits incorporating transistors, including control, addressing, comparing and sensing, and fabrication.

2. My skills and experience are in areas of circuit design and analysis, device and board fabrication and assembly, testing, marketing, control system design and analysis, manufacturing operations, and respective areas of quality, reliability, and defect/failure analysis. Specifically, I have:

- designed memories, including Dynamic Random Access Memories (DRAMs), Static Random Access Memories (SRAMs), Charge Coupled Devices (CCDs), Shift Registers (SRs), and functional circuits including I/O buffers for address and data, decoders, clocks, sense amplifiers, fault tolerant (incorporating both non-volatile EPROM and random access memory components), parallel-to-serial data paths for video applications, level shifters, converters, pumps, and logic, as well as wireless communication systems and MEMs;
- managed operations including engineering, training, and quality assurance for device fabrication, assembly, test, analysis, and reliability assessment, as well as manufacturing control, each of which involved both volatile and non-volatile memory; testing, analysis, and control involved use of mechanical calibration and

measuring equipment, including optical, scanning e-beam, IR, capacitive, and laser using phase contrast and FFT for HARI applications;

- taught courses in solid-state device physics, integrated circuit design, integrated circuit fabrication, and statistical control;
- provided expert services, investigating both process and design technologies of various devices (microprocessor and controller, volatile and non-volatile memory, programmable logic, card, tag, module, mixed signal, custom, and other), systems (PC and peripheral, computer, control, laser measurement, switch, architecture, software, and other), and consumer products (medical, TV, telephone, VCR, facsimile, copier, lighting, game, and other); and
- designed and managed development, testing, and evaluation of memory devices and systems incorporating such devices, including simulation of operation. I have also had experience in programming, erasing, and wearout of electrically programmable and erasable non-volatile memories.

3. Because of my background, training, and experience, I am qualified as an expert to opine on the challenged patent. A more detailed account of my work experience and other qualifications is listed in my Curriculum Vitae, which is submitted as Exhibit 2003.

II. OVERVIEW

4. The Petition should be denied because all grounds fail to disclose or render obvious claim element [1.d]: “a first strained layer of the first conductivity type in a first opening in the second well beside the first gate structure, wherein a difference between a lattice parameter of a portion of the first strained layer near a

bottom of the first opening and a lattice parameter of the substrate is smaller than a difference between a lattice parameter of a portion of the first strained layer apart from the bottom of the first opening and the lattice parameter of the substrate.” This element is required by all challenged claims.

5. Each of the Petition’s Grounds is premised on an oversimplification of element [1.d] that ignores key claim limitations. Specifically, each of Grounds 1A, 2, and 3A—the only grounds challenging independent claim 1—are based on the faulty premise that element [1.d] “requires that the strained layer next to the gate has a non-uniform lattice parameter.” Pet., 25 (Ground 1A), 59 (Ground 2), 78 (Ground 3A). The Petition’s analysis, therefore, focuses on whether the strained layer has a non-uniform lattice parameter. But that statement does not align with what the claim language recites, because it ignores the claim language regarding the claimed difference limitation between the lattice parameter of a portion of the strained layer near the bottom of the opening to “a lattice parameter of the substrate.” Element [1.d] requires that the *difference* between the lattice parameter of the substrate and the lattice parameter of the strained layer is *smaller near the bottom* than at a portion apart from the bottom, not that only the strained layer must have a non-uniform lattice parameter as the Petition alleges. None of the Petition Grounds disclose or render obvious this requirement.

III. MATERIALS CONSIDERED

6. In preparing this declaration, I have reviewed the Petition and the declaration of Petitioner's expert, as well as the materials that they cite, including the asserted prior art.

IV. UNDERSTANDING OF THE LAW

7. In preparing and expressing my opinions and considering the subject matter of the challenged patent, I am relying on certain basic legal principles that counsel have explained to me. These principles are discussed below.

A. Claim Construction

8. I understand that the scope of a patent is defined by its claims. I understand that a claim can be:

- a. a method claim, which covers a process/activity, or
- b. an apparatus claim, which covers a structure, such as a circuit component, physical machine, etc.

9. I understand that the first step in determining the validity of a claim is for the claim to be properly construed. I have been further advised that, in an inter partes review proceeding, the claims of a patent are typically given their ordinary and customary meaning as would be understood by one of ordinary skill in the art in the context of the claims and the patent disclosure (specification).

10. I further understand that an inventor can provide special definitions for specific claim term(s) within the patent. However, any special definition for a claim term must be set forth in the specification with reasonable clarity and precision.

B. Invalidity

11. I have been informed that a claim may be invalid as obvious if the subject matter described by the claim, as a whole, would have been obvious to a POSITA at the time the claimed invention was made. I understand that the standard for obviousness in an inter partes review proceeding is by a preponderance of the evidence.

12. I have also been informed that a determination of obviousness involves an analysis of the scope and content of the prior art, the similarities between the claimed invention and the prior art, and the level of ordinary skill in the art. I have been informed and understand that a prior art reference should be viewed as a whole.

13. I have been informed that, in considering whether an invention for a claimed combination would have been obvious, I may assess whether there are apparent reasons to combine known elements in the prior art in the manner claimed in view of interrelated teachings of multiple prior art references, the effects of demands known to the design community or present in the market place, and/or the background knowledge possessed by a POSITA. I also understand that other

principles may be relied on in evaluating whether a claimed invention would have been obvious.

14. I have been informed that, in making a determination as to whether or not the claimed invention would have been obvious to a POSITA, one is to consider certain objective indicators of non-obviousness if they are present, such as: commercial success of product(s) practicing the claimed invention; long-felt but unsolved need; teaching away; unexpected results; copying; and praise by others in the field. I understand that, for such objective evidence to be relevant to the non-obviousness of claim, there must be a causal relationship (called a “nexus”) between the claim and the evidence. I also understand that this nexus must be based on a novel element of the claim rather than something available in the prior art.

15. I have also been informed and understand that, when considering the obviousness of a patent claim, one should consider whether a reason or motivation existed for combining the elements of the references in the manner claimed, and that the prior art must create a reasonable expectation of success in producing the claimed subject matter.

V. SEMICONDUCTOR TRANSISTOR TECHNOLOGY PRIMER

16. The following is a brief primer of semiconductor transistors to establish a foundation of common terms and concepts that can be used in addressing the defects in the Petition.

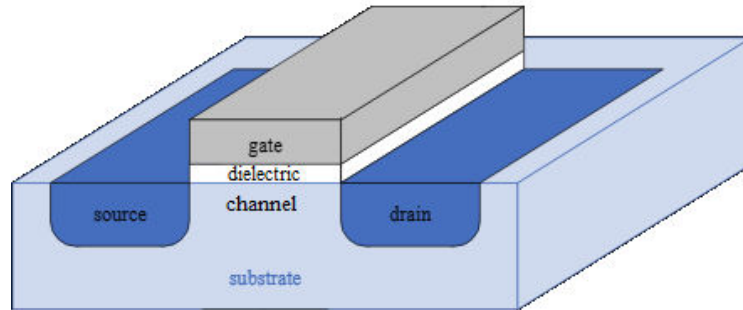
A. Basic Transistor Components

17. Today's semiconductor devices trace their lineage back to the first computers of the 1940s, which used vacuum tubes to perform two key electrical functions: switching (*i.e.*, turning access to electrical current on and off) and amplification (*i.e.*, increasing the amplitude of a signal while retaining its electrical characteristics). EX2002 at 1-2. Where earlier tube devices used a vacuum tube to control the flow of electrons (turning electrical current on and off), today's semiconductor devices use transistors. EX2002 at 3.

18. One type of transistor typically used in an integrated circuit (or "chip") is a "field effect transistor," or FET. Materials used to build such transistors are divided into three categories based on their ability to conduct electrical current: conductors, dielectrics, and semiconductors. EX2002 at 29-34. In a conductor (*e.g.*, a metal), electric current can flow freely. EX2002 at 29. A dielectric (*e.g.*, silicon dioxide) is an insulative material at the opposite end of the conductivity spectrum and has a high resistance to the flow of current. EX2002 at 30. Semiconductors (*e.g.*, silicon) fall between conductors and dielectrics and have some conducting and some resisting ability. EX2002 at 31-34.

19. The simplified FET below illustrates how these materials may be used to create a semiconductor transistor device. As shown, the transistor is built on a semiconductor substrate and comprises a source, a drain, a gate, and a channel. *See*,

e.g., EX2002 at 510-511. The source, drain and channel comprise semiconductor material, the gate comprises a conductor, and the gate and channel are separated by a thin dielectric layer.



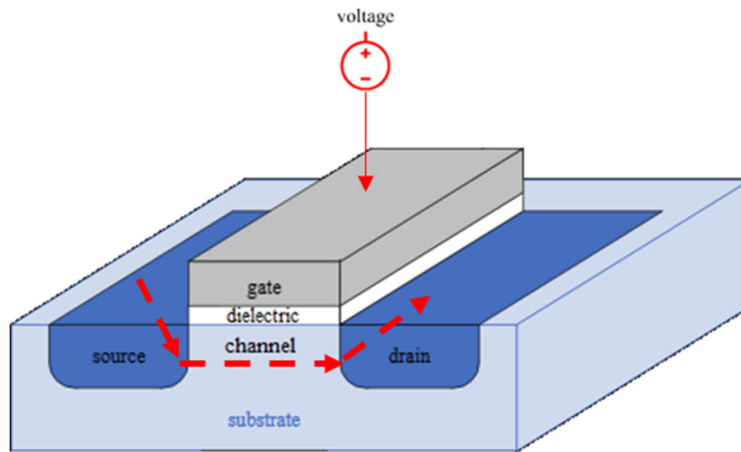
See, e.g., EX2002 at 510-511.

20. The source and drain are regions in the semiconductor substrate that are either rich in electrons (a negative, or n-type, region) or rich in holes (a positive, or p-type, region). EX2002 at 26-28, 427-28. The channel is a region under the gate and between the source and drain, and is of the opposite type to that of the source and drain. In other words, if the source and drain are n-type regions, then the channel will be a p-type region (and vice versa). EX2002 at 510-511.

21. The gate is a conductor (or semiconductor) located above the channel. In this simplified version of a FET, there is a dielectric between the channel and the gate. EX2002 at 510-511. When a voltage is applied to the gate, the dielectric prevents the “flow of charge” (current) between the gate and the channel, but the applied voltage results in the creation of a “field effect” in the channel. EX2002 at

510-511. This “field effect” either builds up or depletes the charges in the channel (depending on whether it is a p- or n-type channel). EX2002 at 510-511.

22. As illustrated below, this field effect allows charge to flow from the source, through the channel, to the drain. Thus, selectively applying voltage to the gate switches the transistor on and off, starting and stopping drain-to-source or source-to-drain current.



B. Processes For Manufacturing Integrated Circuits And Transistors

1. The Four Stages Of Fabricating Integrated Circuits

23. The intricate, complex manufacturing process developed over the years for achieving such highly-dense integrated circuits can be divided into four distinct stages: (1) material preparation; (2) wafer preparation; (3) wafer fabrication; and (4) packaging.

24. In the first stage, the semiconductor material itself is created. EX2002 at 13. For a silicon semiconductor, the raw starting material is sand, which is converted to pure silicon with a polysilicon structure. EX2002 at 13.

25. In the second stage, the semiconductor material is first formed into a silicon crystal with specific electrical and structural parameters, and it is then sliced into thin disks called “wafers.” EX2002 at 13-14. A wafer acts as a semiconductor substrate on and in which transistors may be formed.

26. The third stage is wafer fabrication, during which individual integrated circuits are formed in and on the wafer semiconductor substrate. EX2002 at 14. Thousands of integrated circuits can be formed on the substrate of a single wafer. EX2002 at 14.

27. In the packaging stage, the wafer is separated into individual chips. EX2002 at 14-15.

2. The Wafer Fabrication Stage

28. The third manufacturing stage, wafer fabrication, is the one most relevant here, and it can take several thousand steps, during which transistors and other devices are formed in and on the wafer’s substrate. EX2002 at 14. These steps are generally performed using three categories of materials (conductors, semiconductors, and dielectrics) in four basic operations (layering, patterning, doping, and heat treatments). *See* EX2002 at 29-31, 71. For purposes of

understanding the Petition and its deficiencies, the most important basic operations are layering, patterning, and doping.

29. **Layering** is the operation used to add thin layers to the semiconductor substrate. EX2002 at 72. The layers may be conductors, semiconductors, or dielectrics; and they can have a variety of functions and be made in a variety of ways. EX2002 at 72.

30. For example, one way of adding a layer of material is to deposit that material onto the semiconductor substrate. Another way of adding a layer of material is to grow the material on the semiconductor substrate. After an initial layer is added to the semiconductor substrate, additional layers may be added to the earlier layers using similar growth or deposition processes. To illustrate, the transistor structure shown below shows a number of layers that have been added to the wafer's semiconductor substrate, some deposited, some grown. EX2002 at 72.

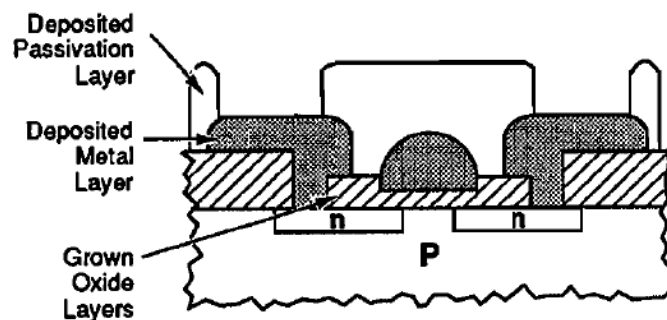


Figure 4.4 Cross section of completed metal gate MOS transistor with grown and deposited layers.

31. **Patterning** is the series of steps to remove (etch away) selected portions of the semiconductor substrate or one or more layers of materials that were added during one or more prior layering operations. EX2002 at 72-73. This creates a pattern on the wafer surface. EX2002 at 72-73.

32. The patterning may result in one or more holes in the layered material or one or more remaining islands of material. EX2002 at 72-73. For example, the following figures illustrate the use of patterning to make (1) a hole in a previously formed layer: and (2) an island from a previously formed layer:

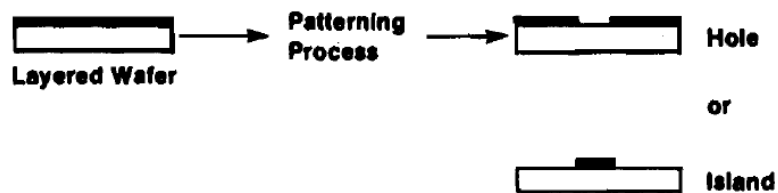


Figure 4.7 Patterning.

33. The repeated combination of layering and patterning in different sequences and variations is critical to the formation of transistors in and on the semiconductor wafer:

These parts are created one layer at a time by the combination of putting a layer on the surface and removing a portion, with a patterning process, to leave a specific shape. The goal of the patterning operations is to create the desired shapes in the exact dimensions (feature size) required by the circuit design, and to locate them in their proper location on the wafer surface and in relation to the other parts.

EX2002 at 73.

34. **Doping.** Impurities are intentionally introduced during the transistor fabrication process to enhance the conductivity of a given material or to create an isolation region that impedes conductivity. Various, well-known techniques, such as high temperature diffusion and ion implantation, are used to introduce impurities into selective regions of a semiconductor substrate and/or into different layers created during the layering and patterning processes.

EX2002 at 31-34.

VI. THE CHALLENGED '822 PATENT

35. The challenged '822 patent provides a semiconductor structure in which “the difference between the lattice parameter of a portion of the strained layer near the bottom of the opening and the lattice parameter of the substrate is smaller than the difference between the lattice parameter of a portion of the strained layer apart from the bottom of the opening and the lattice parameter of the substrate.” EX1001, 4:13-19. “Thus, less defects occur at the interface of the strained layer and the substrate.” *Id.*, 4:19-20. “Moreover, since a silicon layer is formed on the strained layer before the metal silicide layer is formed, the non-silicon IV-group element does not enter the metal silicide layer in the silicide process, so that the quality of the metal silicide layer is not degraded.” *Id.*, 4:20-24.

VII. THE PETITION FAILS TO ESTABLISH THE REQUIRED LIKELIHOOD OF SUCCESS

A. Grounds 1A and 1B

36. In Ground 1A, the Petition alleges that Koontz renders obvious independent claim 1 and dependent claims 2-7, 9, and 11-13, which depend from claim 1. Pet., 19. In Ground 1B, the Petition alleges the combination of Koontz and Sridhar renders obvious dependent claims 8, 10, and 14, which depend from claim 1. Pet., 40. Both of these grounds fail because Koontz does not disclose or render obvious element [1.d].

37. Regarding element [1.d], the Petition alleges that “[t]his limitation requires that the strained layer next to the gate has a non-uniform lattice parameter, meaning that its atoms are organized as a crystal lattice, but the distance between those atoms (*i.e.*, the lattice parameter) varies vertically.” Pet., 25. But this statement does not accurately reflect what the claim language requires, because it ignores the claim language regarding “a lattice parameter of the substrate.” Element [1.d] requires that the *difference* between the lattice parameter of the substrate and the lattice parameter of the strained layer is *smaller near the bottom* of the opening than at a portion apart from the bottom, not only that the strained layer must have a non-uniform lattice parameter as the Petition alleges. For example, even if a strained layer has a non-uniform lattice parameter, as the Petition alleges is sufficient, it could be non-uniform such that the lattice parameter of the strained layer near the bottom

of the opening is further from the lattice parameter of the substrate, rather than being such apart from the bottom of the opening (as required by the claims). There is no discussion of the substrate lattice parameter in Koontz. Such a scenario, which the Petition would incorrectly argue meets the claim limitations, would clearly contradict the express language of element [1.d]. The Petition's analysis is thus deficient in that it is based on an inaccurate assessment and application of what the claim language expressly requires.

38. As an initial matter, even under the Petitioner's misstatement of what the claim requires (the strained layer merely having a non-uniform lattice parameter), Ground 1A would fail, as no such structure is disclosed in Koontz. The Petition alleges that Koontz discloses that the strained layer has a non-uniform lattice parameter because Koontz states that "recess structures 446"—the alleged strained layer—"can vary in composition vertically from bottom to top of the structures 446." Pet., 25 (quoting EX1004-Koontz, ¶[0063]). But a POSITA would have understood that a variation *in composition* does not necessarily translate to a non-uniform *lattice parameter* or even one that is distributed in the way required by the claim. For example, a compound may consist of two elements of a similar size such that varying the composition of the compound would not change the lattice parameter of the compound. Moreover, even with elements of varying sizes, varying the composition may still result in a uniform lattice parameter due to other variables, such as

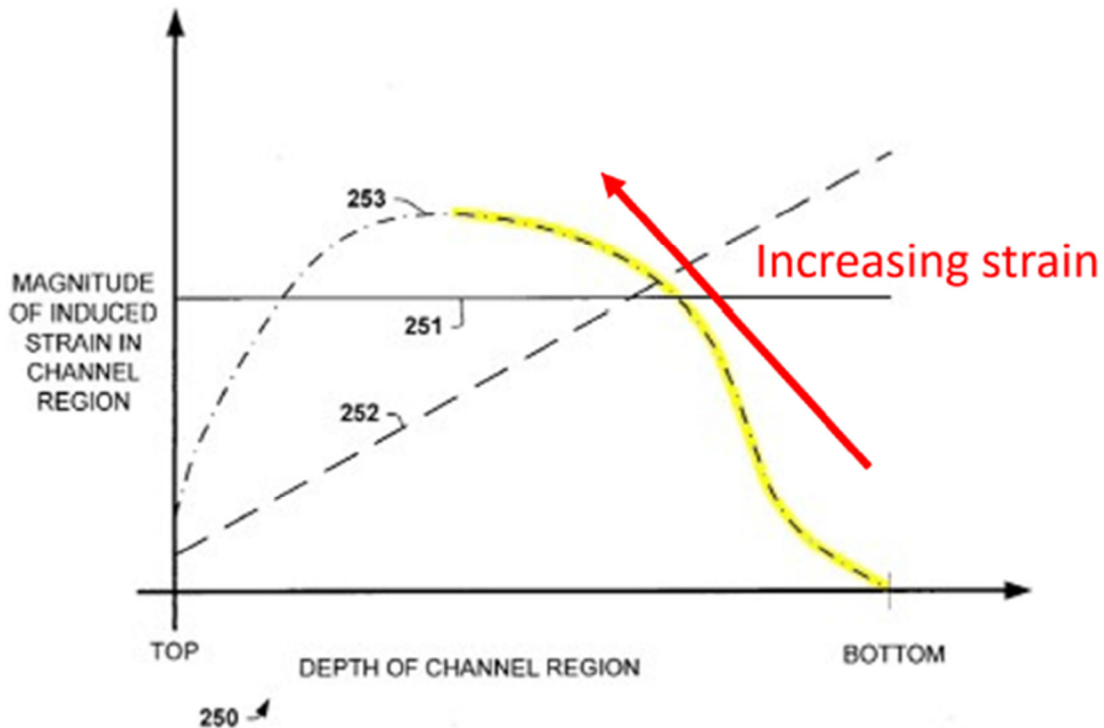
temperature that affect how the elements bond together. The Petition (and Petitioner's expert) do not address these issues at all.

39. Even if the Petition were correct that Koontz's "recess structures 446" has a non-uniform lattice parameter, this still would not meet the requirements of element [1.d] because it assumes, without support, that the lattice parameter of the substrate is uniform. A semiconductor substrate may not have a uniform lattice parameter due to non-uniform doping. For example, wafers for semiconductor manufacturing are sold in part based on their resistivity. For this reason, these wafers are "doped" with additional impurities to modify their resistivity. Additionally, the challenged claims require "a substrate, having therein a first well of a first conductivity type and a second well of a second conductivity type." In order to create conductive wells of the proper type (n-type wells associated with p-type transistors, and p-type wells associated with n-type transistors), the substrate must be doped by introducing a particular impurity to the substrate (typically phosphorous for an n-well and boron for a p-well). This doping process changes the composition of the substrate and may also affect the lattice parameter of the substrate. Moreover, the dopant may not be introduced uniformly throughout the substrate, which would cause the substrate to have a non-uniform lattice parameter. Thus, Grounds 1A and 1B are premised on an incorrect and unsupported assumption regarding the lattice parameter of the substrate.

40. Moreover, the Petition’s argument is that “the lattice parameter of these structures [recessed structures 446 in Koontz] can vary *layer by layer*, which allows engineers to shape the strain profile throughout the depth of the channel.” Pet., 27. But the claims require something different—the variation of the lattice constant as claimed must occur within *the same layer*: “a difference between a lattice parameter of a portion *of the first strained layer* near a bottom of the first opening and a lattice parameter of the substrate is smaller than a difference between a lattice parameter of a portion *of the first strained layer* apart from the bottom of the first opening and the lattice parameter of the substrate.” Ex 1001, claim 1. Further, there is no disclosure in Koontz, or elsewhere cited in the Petition, of “changing the percentage of germanium [*sic*] in the silicon-germanium mixture,” as the Petition alleges; and it is not implicit or implied by the statement that the recess structure 446 “can vary in composition vertically.” Pet., 25.

41. Koontz, therefore, does not render obvious the specific requirements of element [1.d]: “wherein a difference between a lattice parameter of a portion of the first strained layer near a bottom of the first opening and a lattice parameter of the substrate is smaller than a difference between a lattice parameter of a portion of the first strained layer apart from the bottom of the first opening and the lattice parameter of the substrate.” The Petition admits that “Koontz does not specifically state that the difference between the lattice parameter of the strained layer and that of the

substrate increases from bottom to top, as claimed.” Pet., 26. Instead, the Petition argues that Koontz renders obvious element [1.d] because “Koontz discloses that the induced strain in the channel region underneath the gate increases from the bottom to the top of the channel, as shown in Figures 2C and 2B.”



Pet., 26 (showing annotated EX1004-Koontz, Fig. 2C).

42. The Petition alleges that “Koontz explains that there is a direct correlation between the lattice parameter of the recessed structures 446 and the strain in the channel: increasing the difference between the lattice parameter of recessed structures 446 and that of the substrate increases the strain in the channel, and vice versa.” Pet., 28 (quoting EX1004-Koontz, ¶¶[0063]; *see also id.*, [0033]-[0036], [0059]). Not so. Koontz does not say this, and none of the cited paragraphs of Koontz

support the Petition's allegation. Paragraph [0063] merely states that "the resulting compressive strain can be increased or decreased by correspondingly increasing or decreasing *one or more components of the tensile strain producing material.*" EX1004-Koontz, ¶[0063] (emphasis added). It does not mention lattice parameters at all, much less that increasing the difference between the lattice parameter of recessed structures 446 and that of the substrate increases the strain in the channel. *Id.*

43. Put simply, the Petition fails to explain how Koontz's disclosure of increasing *induced strain in the channel region underneath the gate* renders obvious element [1.d]'s requirement that the *difference between the lattice parameter of the strained layer and the lattice parameter of the substrate* increases from bottom to top of the strained layer. A POSITA would have understood that strain in the channel region can be induced in many different ways, other than through a difference in lattice parameters, much less a difference in varying lattice parameters of a material beside the gate structure. For example, local strain can be induced through other techniques, such as shallow trench isolation, a contact etch stop layer above the gate, and silicidation of the source/drain regions. A contact etch stop layer is a highly stressed film deposited on top of the gate stack, which transfers stress into the gate channel. Silicidation is a process in which a metal is deposited on silicon and sintered to form low-resistance electrical contact regions. This

silicide layer on the top surface area of the source/drain regions can also exert stress on the gate's channel. The '822 patent specifically discloses disposing contact etching stop layers and a metal silicide layer as alternative ways to create strain. EX1001, 6:3-18.

B. Ground 2

44. In Ground 2, the Petition alleges that Orlowski anticipates claims 1-4. Pet., 51. Orlowski fails to disclose element [1.d].

45. Regarding element [1.d], the Petition again alleges that “[t]his limitation requires that the strained layer next to the gate has a non-uniform lattice parameter.” Pet., 59. As explained above in Section VII.A, this is incorrect. The Petition’s analysis is deficient in that it does not meaningfully address the claim language regarding the claimed difference limitation between the lattice parameter of a portion of the strained layer near the bottom of the opening to “a lattice parameter of the substrate.”

46. The Petition points to Orlowski’s disclosure that “the percentage of silicon in SISD structure[] 190 decrease[s] from the bottom of SISD structures 190 to the top.” Pet., 59 (quoting EX1006-Orlowski, 8:41-45; *see also id.*, 7:22-28). The Petition claims, without support, that “the closer one gets to the bottom of the of [sic] strain inducing source/drain structures 190, the closer the composition of the silicon-germanium mixture gets to the composition of substrate 101 (where the percentage

is close to 100% silicon)." Pet., 60 (no citation). But contrary to the Petition's allegations, Orlowski does not disclose that the composition of the alleged substrate is close to 100% silicon, or that the difference between the lattice parameters of the SSID and the substrate increases if the percentage of silicon in the SSID increases. Rather, these are assumptions that the Petition imports, without support or explanation. Moreover, the Petition argues that "wafer 101" is the claimed substrate, and that it is "close to 100% silicon." That is incorrect because wafer 101 is a silicon-on-insulator structure, in which a significant portion of wafer 101 is made up of "buried oxide (BOX) layer 104," which is not silicon. EX1006-Orlowski, Figs. 1-13, 3:9-16. Further, in order to create conductive wells of the proper type (n-type wells and p-type wells), the substrate must be doped by introducing a particular impurity to the substrate (typically phosphorous for an n-well and boron for a p-well. This doping process changes the composition of the substrate such that the substrate is not 100% silicon and may also affect the lattice parameter of the substrate. Moreover, the dopant may not be introduced uniformly throughout the substrate, which would cause the substrate to have a non-uniform lattice parameter. Thus, Ground 2 is premised on an incorrect and unsupported assumption regarding the lattice parameter of the substrate.

47. Moreover, although Orlowski states repeatedly that the lattice constant of the SSID structures is different from that of the surrounding material, it never

states that the SSID has a varying lattice constant itself. EX1006-Orlowski, Abstract, 2:34-45, 5:4-23. A POSITA would know that, given the emphasis by the inventors on the former, if the latter were true, the applicant would have said so. Instead, a POSITA would view the lattice constant (always referred to in the singular in Orlowski) of the SSID structures as being constant.

48. Accordingly, Orlowski does not disclose element [1.d].

C. Grounds 3A and 3B

49. In Ground 3A, the Petition alleges that the combination of Samoilov and Murthy renders obvious independent claim 1 and dependent claims 2-7, 9, and 11-13, which depend from claim 1. Pet., 64. In Ground 3B, the Petition alleges the combination of Samoilov, Murthy, and Sridhar renders obvious dependent claims 8, 10, and 14, which depend from claim 1. Pet., 95. Both of these grounds fail because Samoilov and Murthy do not disclose or render obvious element [1.d].

50. Regarding element [1.d], the Petition again alleges that “[t]his limitation requires that the strained layer next to the gate has a non-uniform lattice parameter.” Pet., 78. As explained above in Section VII.A, this is incorrect. The Petition’s analysis is deficient in that it does not meaningfully address the claim language regarding “a lattice parameter of the substrate.”

51. The Petition relies on Samoilov’s statement that “[m]ultiple SiGe-containing layers containing varying amount of elements may be stacked to form

silicon-containing layer 140 with a graded elemental concentration.” EX1005-Samailov, ¶[0030]; Pet., 83-84. The Petition points to an embodiment in which “a first SiGe-layer may be deposited with a germanium concentration in a range from about 15 at % to about 25 at % and a second SiGe-layer may be deposited with a germanium concentration in a range from about 25 at % to about 35 at %.” EX1005-Samailov, ¶[0030]; Pet., 78-79. The Petition then concludes, without explanation, that one would be above the other, with no support in the reference itself: “a POSITA would have understood the lattice parameter at the bottom of silicon-containing layer 140 (where the concentration of germanium or carbon is lower) more closely matches the lattice parameter of the substrate than does the rest of silicon-containing layer 140.” Pet., 79.

52. The Petition’s analysis is wholly inadequate. *First*, the Petition presumes that, in the cited example in Samoilov, the layer containing less germanium is at the bottom and the layer containing more germanium is at the top, but Samoilov does not say this, as explained above. *Compare* Pet., 78-79 (Petitioner arguing that “[i]n one example, a silicon-germanium sub-layer near the bottom has a ‘germanium concentration in a range from about 15[]% to about 25[]%’ whereas a sub-layer apart from the bottom has a ‘germanium concentration in a range from about 25[]% to about 35[]%.’”) *with* EX1005-Samailov, ¶[0030] (“a first SiGe-layer may be deposited with a germanium concentration in a range from about 15 at % to

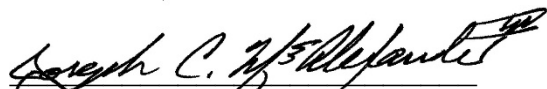
about 25 at % and a second SiGe-layer may be deposited with a germanium concentration in a range from about 25 at % to about 35 at %.”). **Second**, even if the Petition were correct about the ordering of the layers, it still does not establish why this necessarily means that “a difference between a lattice parameter of a portion of the first strained layer near a bottom of the first opening and a lattice parameter of the substrate is smaller than a difference between a lattice parameter of a portion of the first strained layer apart from the bottom of the first opening and the lattice parameter of the substrate,” as element [1.d] recites. The Petition makes no allegation that Samoilov teaches or suggests anything about the lattice parameter of the substrate. **Third**, Samoilov never states that the two layers have different lattice constants. Samoilov does point out that SiGe and SiC have different lattice constants from Silicon, one larger and one smaller, to be used for PMOS and NMOS, respectively. EX1005-Samailov, ¶¶ [0009], [0068]. But the claims require the variation of lattice constant as claimed occur within *the same layer*: “a difference between a lattice parameter of a portion *of the first strained layer* near a bottom of the first opening and a lattice parameter of the substrate is smaller than a difference between a lattice parameter of a portion *of the first strained layer* apart from the bottom of the first opening and the lattice parameter of the substrate.” Ex 1001, claim 1. As explained above, the lattice parameter of the substrate cannot be assumed because the whole wafer is doped and is thus not necessarily purely silicon, and the

substrate may not have a uniform lattice parameter due to non-uniform doping of the wells. For example, wafers for semiconductor manufacturing are sold based in part on their resistivity. For this reason, these wafers are “doped” with additional impurities to modify their resistivity. Additionally, the challenged claims require “a substrate, having therein a first well of a first conductivity type and a second well of a second conductivity type.” In order to create conductive wells of the proper type (n-type wells and p-type wells), the substrate must be doped by introducing a particular impurity to the substrate (typically phosphorous for an n-well and boron for a p-well). This doping process changes the composition of the substrate and may also affect the lattice parameter of the substrate. Moreover, the dopant may not be introduced uniformly throughout the substrate, which would cause the substrate to have a non-uniform lattice parameter. Thus, Grounds 3A and 3B are premised on an incorrect and unsupported assumption regarding the lattice parameter of the substrate.

VIII. CONCLUSION

53. For the above reasons, the Petition should be denied.

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