

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	
	Filing Date	
	First Named Inventor	Chu-Yin Tseng
	Art Unit	N/A
	Examiner Name	N/A
	Attorney Docket Number	NAUP0913USA1

U.S.PATENTS						
Examiner Initial*	Cite No	Patent Number	Kind Code	Issue Date	Name	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
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	5	6429084	B1	2002-08-06	Park	
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	2	20080006818	A1	2008-01-10	Luo	
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Examiner Initial*	Cite No	Foreign Document Number	Country Code	Kind Code	Publication Date	Name	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear	
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NON-PATENT LITERATURE DOCUMENTS			
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Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	
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☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).			
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☐ See attached certification statement.			
☐ Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.			
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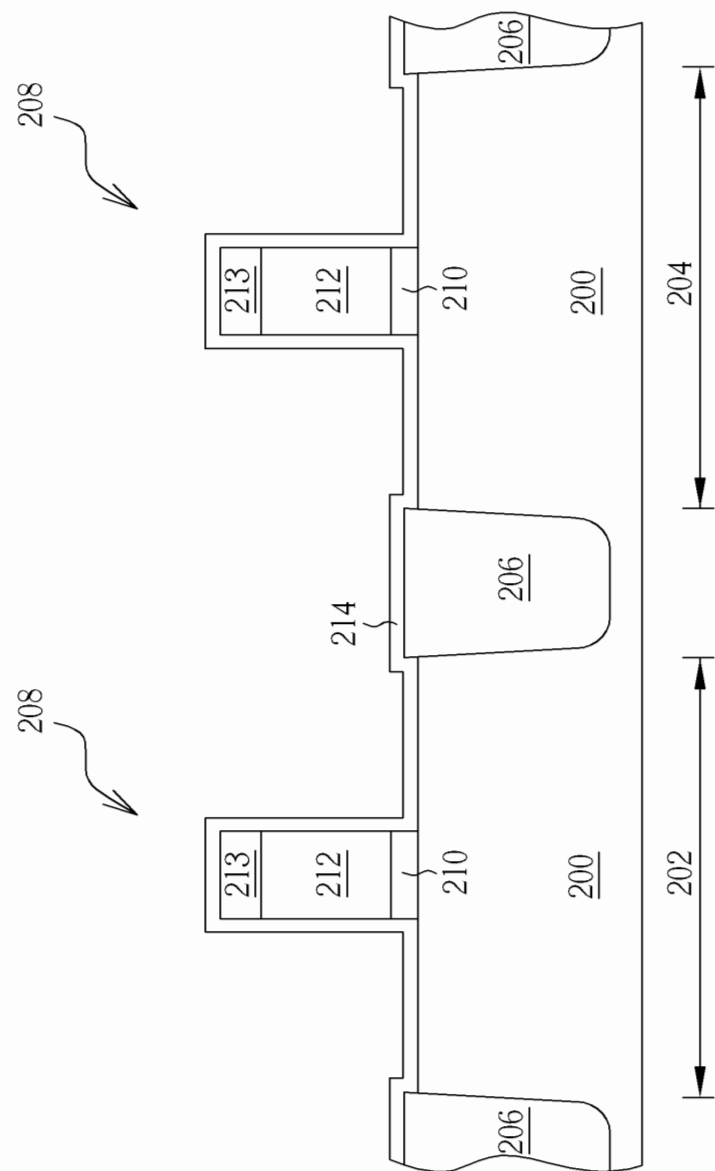


FIG. 1

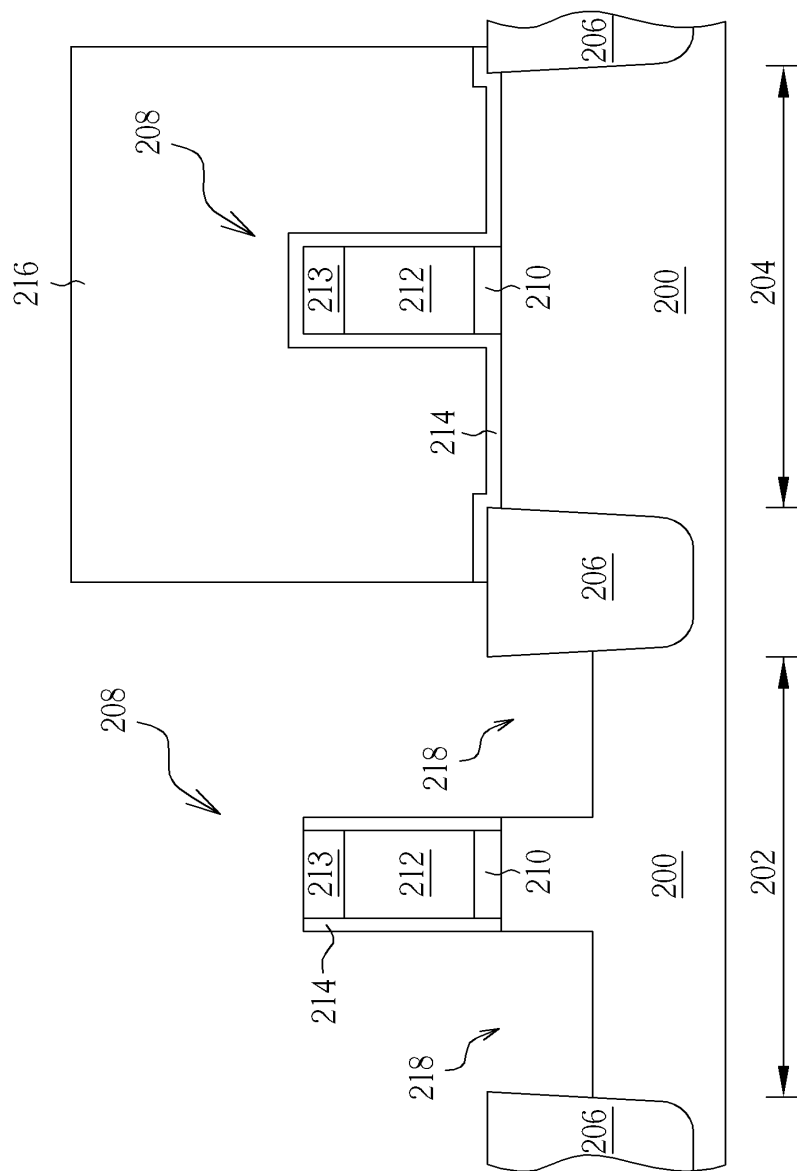


FIG. 2

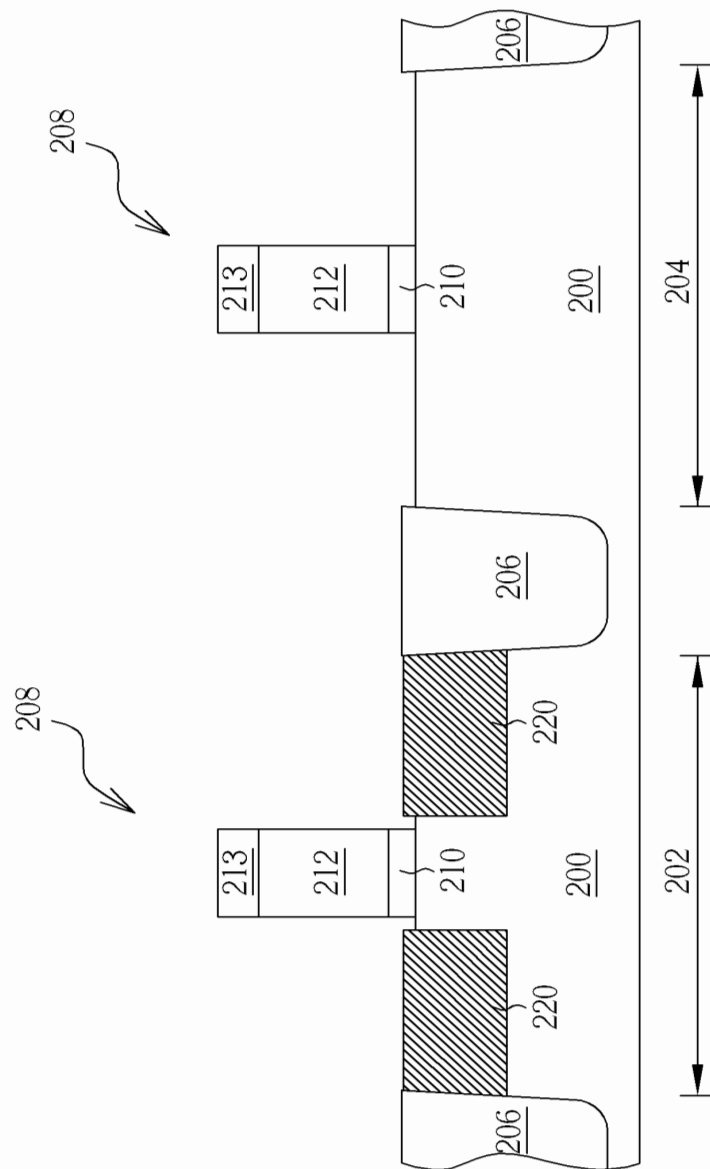
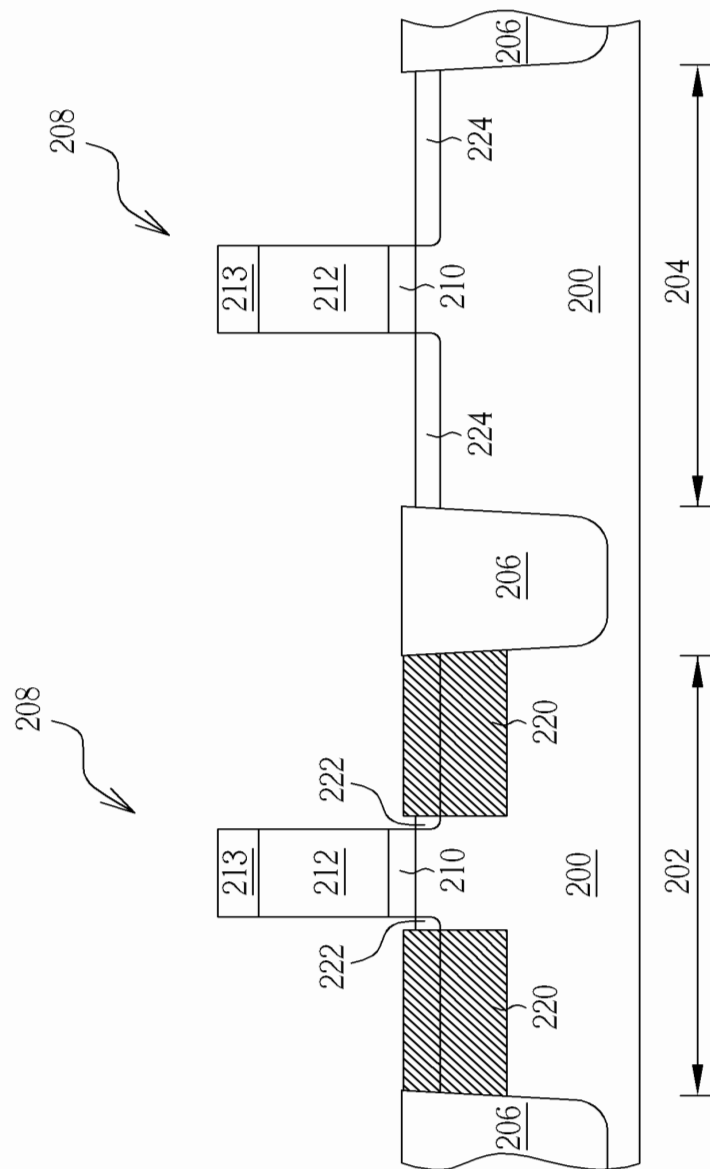
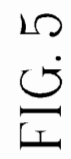


FIG. 3





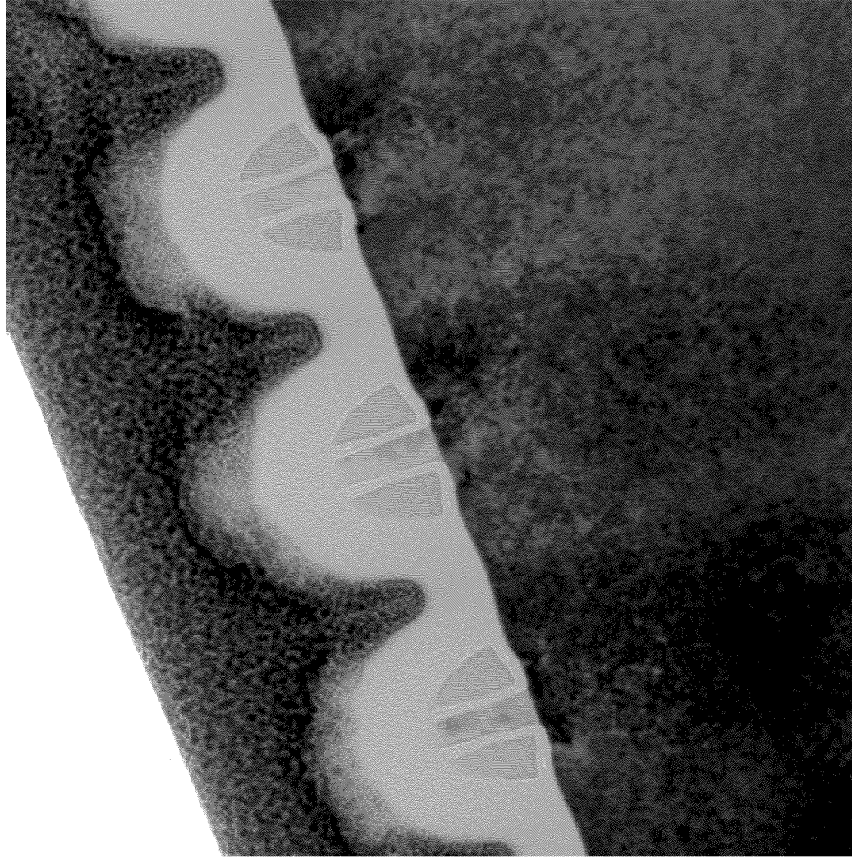


FIG. 6

FIG. 7

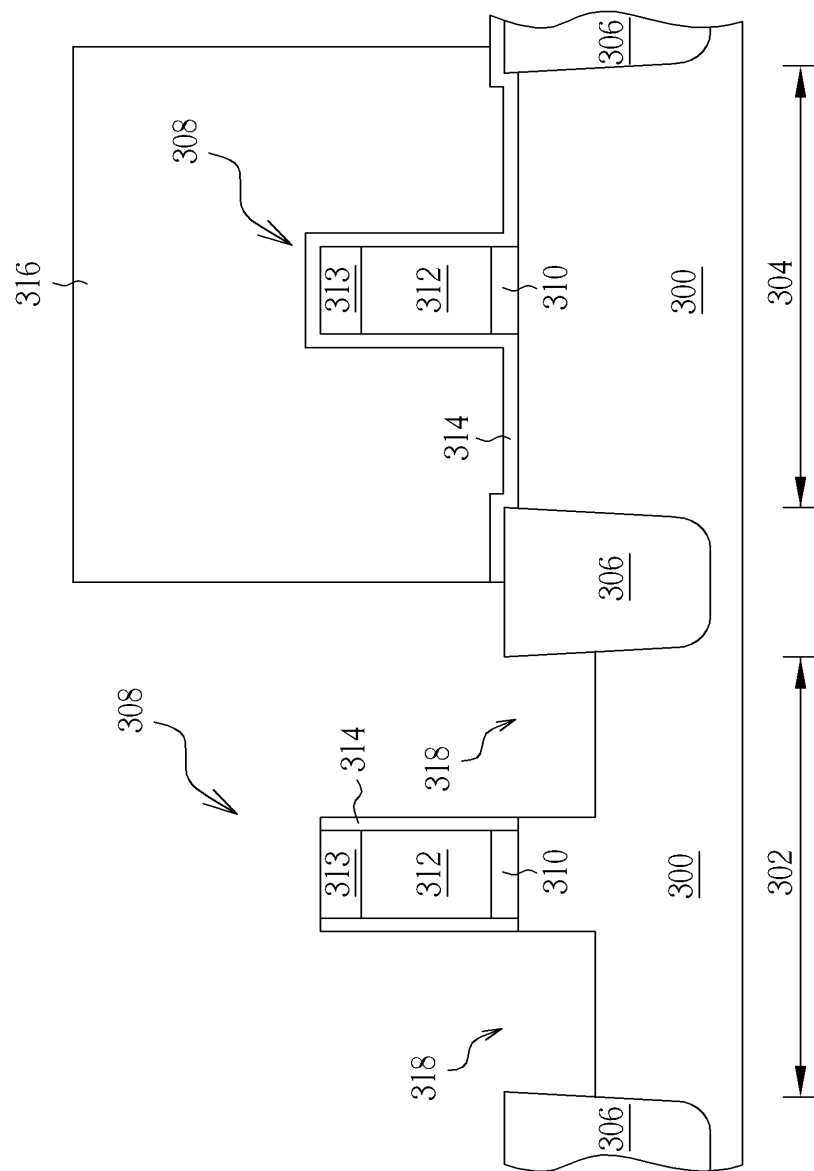


FIG. 8

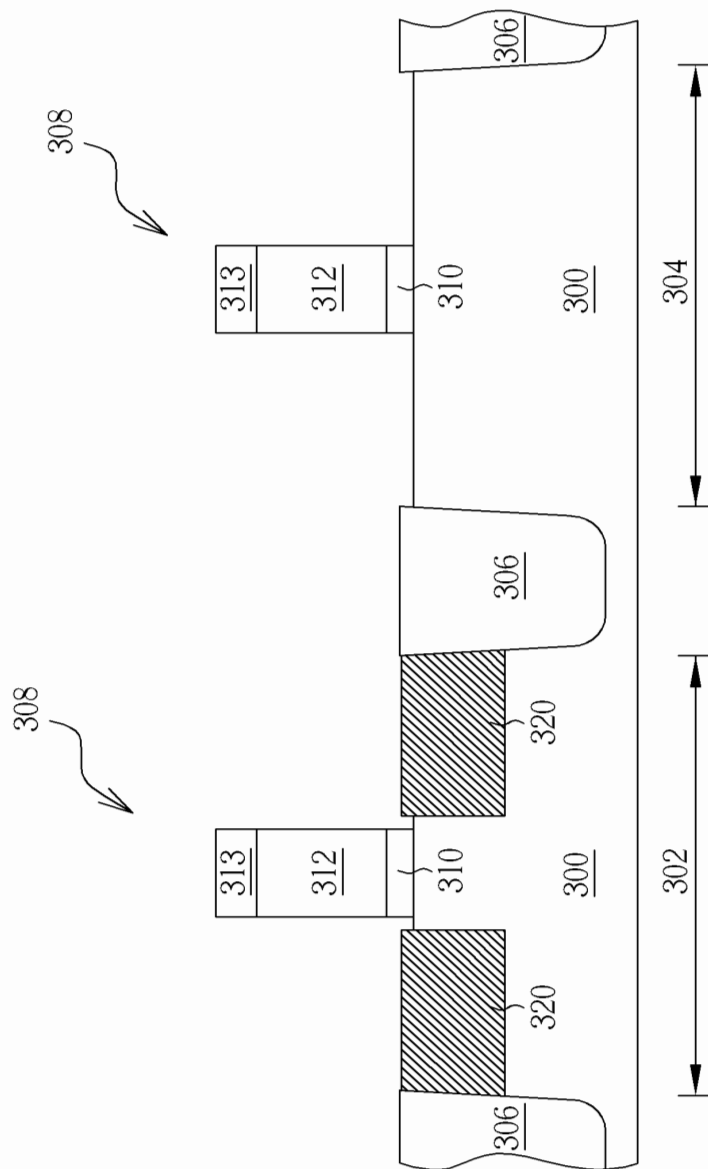


FIG. 9

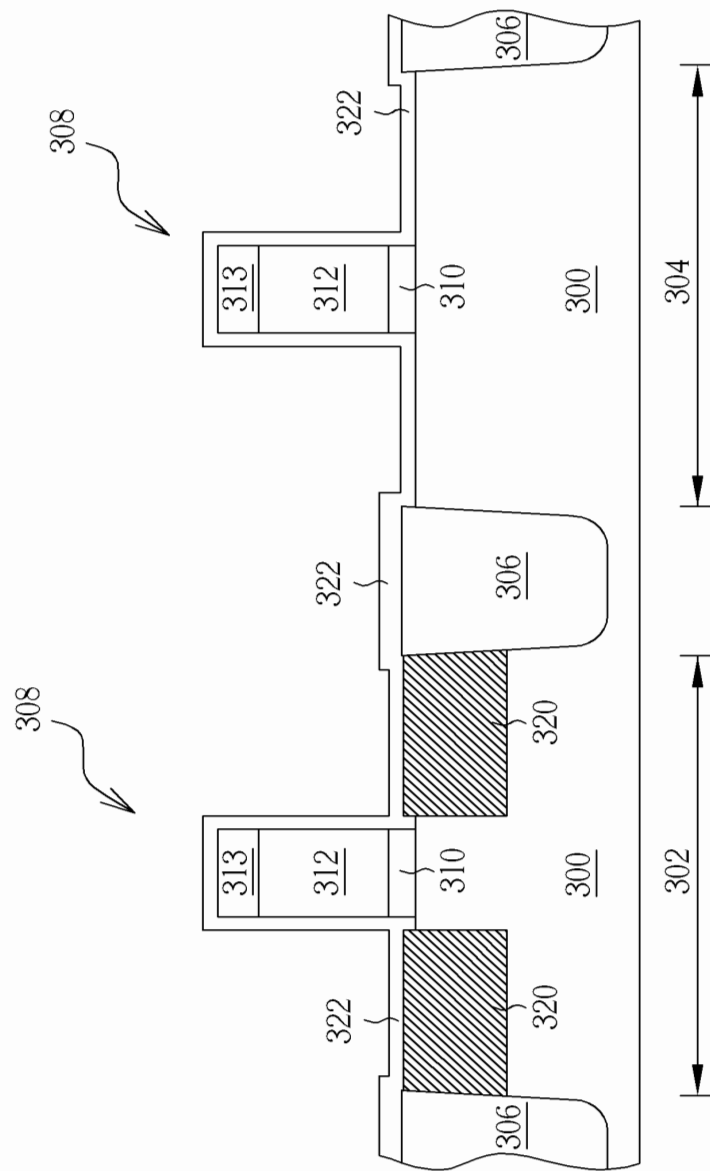


FIG. 10

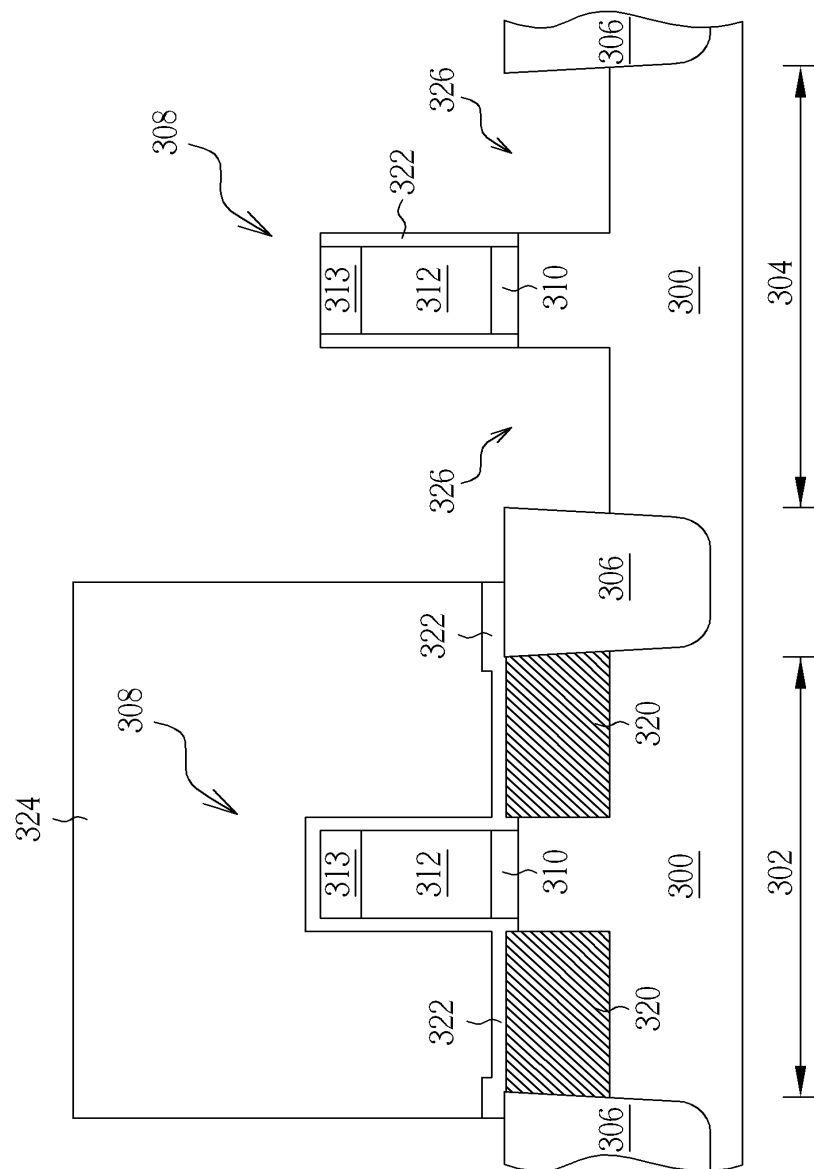


FIG. 11

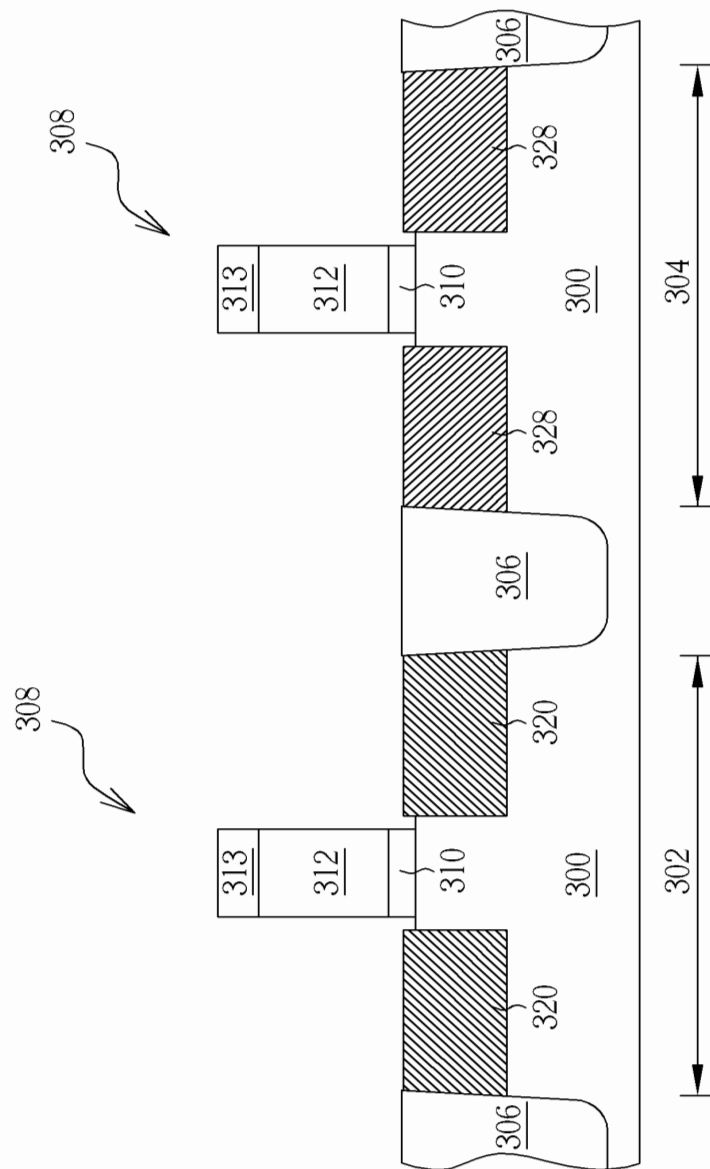


FIG. 12

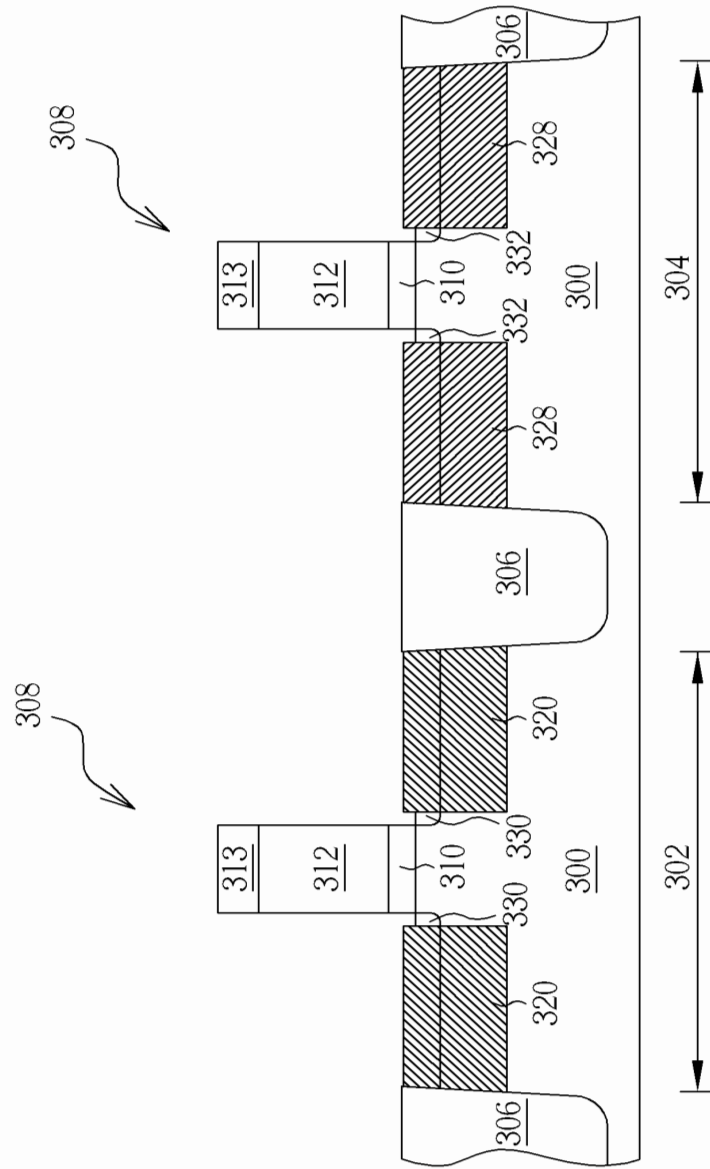


FIG. 13

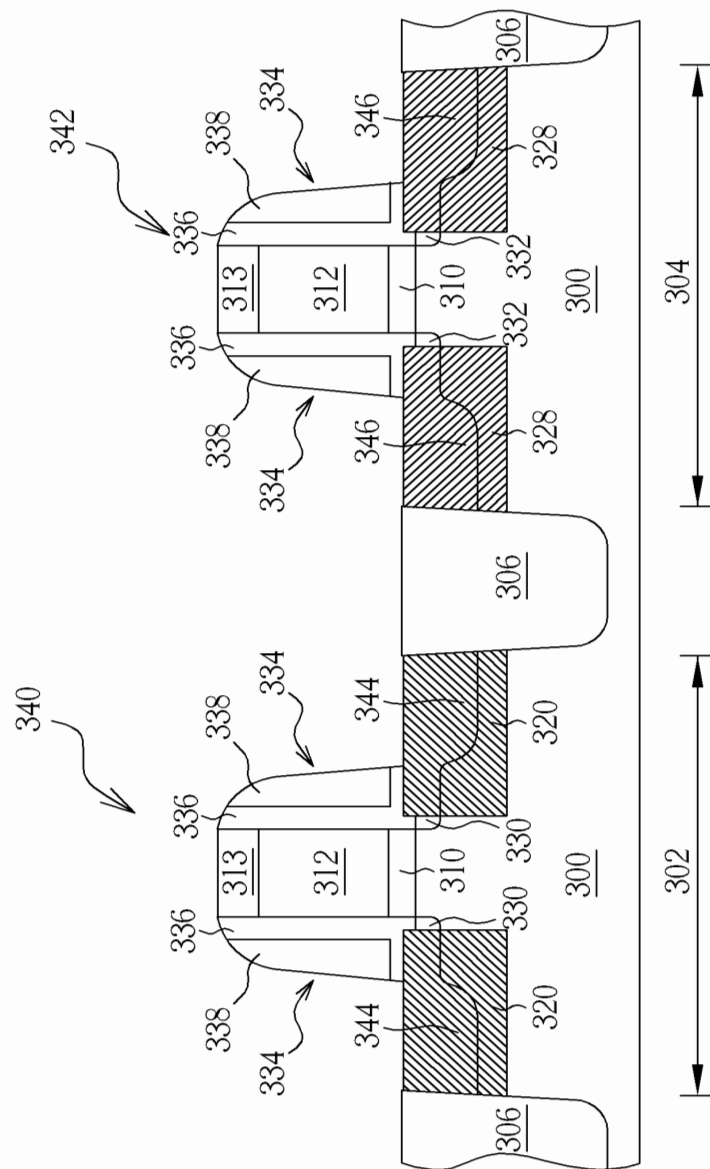


FIG. 14

Abstract of Disclosure

A method of fabricating a MOS transistor is disclosed. The method includes the steps of: providing a semiconductor substrate; forming at least a gate on the semiconductor substrate; forming a protective layer on the semiconductor substrate, and the protective layer covering the surface of the gate; forming at least a recess within the semiconductor substrate adjacent to the gate; forming an epitaxial layer in the recess, wherein the top surface of the epitaxial layer is above the surface of the semiconductor substrate; and forming a spacer on the sidewall of the gate and on a portion of the epitaxial layer, wherein a contact surface of the epitaxial layer and the spacer is above the surface of the semiconductor substrate.

Claims

What is claimed is:

1. A method of fabricating a MOS transistor, comprising:
 - providing a semiconductor substrate;
 - forming at least a gate on the semiconductor substrate;
 - forming a protective layer on the semiconductor substrate, and the protective layer covering the surface of the gate;
 - forming at least a recess within the semiconductor substrate adjacent to the gate;
 - forming an epitaxial layer in the recess, wherein the top surface of the epitaxial layer is above the surface of the semiconductor substrate; and
 - forming a spacer on the sidewall of the gate and on a portion of the epitaxial layer, wherein a contact surface of the epitaxial layer and the spacer is above the surface of the semiconductor substrate.
2. The method of claim 1, further comprising a step of removing the protective layer after forming the epitaxial layer in the recess.
3. The method of claim 1, wherein the protective layer comprises silicon nitride.
4. The method of claim 3, wherein the protective layer has a thickness of about 150 to 250 angstroms.
5. The method of claim 1, wherein the spacer further comprises an oxide liner and a nitride spacer.
6. The method of claim 1, wherein the spacer further comprises an offset spacer, positioned between the gate and the spacer.
7. The method of claim 1, further comprising a step of forming a source/drain region within the semiconductor substrate adjacent to the gate after forming the spacer.
8. The method of claim 1, further comprising a step of forming a lightly doped region within the semiconductor substrate adjacent to the gate.
9. A method of fabricating a CMOS transistor, comprising:

providing a semiconductor substrate having at least a first conductive transistor area for fabricating first conductive transistors and at least a second conductive transistor area for fabricating second conductive transistors, and an isolation structure between the first conductive transistor area and the second conductive transistor area;

forming a gate on the first conductive transistor area and on the second conductive transistor area respectively;

forming a first protective layer on the semiconductor substrate, and the first protective layer covering the surface of each gate;

forming at least a first recess within the semiconductor substrate adjacent to the gate in the first conductive transistor area;

forming a first epitaxial layer in the first recess, wherein the top surface of the first epitaxial layer is above the surface of the semiconductor substrate; and

forming a spacer on the sidewall of each gate and at least on a portion of the first epitaxial layer, wherein a contact surface of the first epitaxial layer and the spacer is above the surface of the semiconductor substrate.

10. The method of claim 9, further comprising a step of forming a first ion lightly doped region within the semiconductor substrate adjacent to the gate in the first conductive transistor area.

11. The method of claim 9, wherein the first protective layer comprises silicon nitride.

12. The method of claim 9, wherein the first protective layer has a thickness of about 150 to 250 angstroms.

13. The method of claim 9, wherein each spacer further comprises an oxide liner and a nitride spacer.

14. The method of claim 9, wherein each spacer further comprises an offset spacer, positioned between each gate and each spacer.

15. The method of claim 9, further comprising a step of removing the first protective layer after forming the first epitaxial layer in the first recess.

16. The method of claim 15, after removing the first protective layer, the method further comprising:

forming a second protective layer on the semiconductor substrate, and the second protective layer covering the surface of each gate;

forming at least a second recess within the semiconductor substrate adjacent to the gate in the second conductive transistor area;

forming a second epitaxial layer in the second recess;

removing the second protective layer; and

forming a second ion lightly doped region within the semiconductor substrate adjacent to the gate in the second conductive transistor area before forming the spacer.

17. The method of claim 16, wherein the second protective layer comprises silicon nitride.

18. The method of claim 17, wherein the second protective layer has a thickness of about 150 to 250 angstroms.

19. The method of claim 9, after forming the first epitaxial layer, the method further comprising:

forming at least a second recess within the semiconductor substrate adjacent to the gate in the second conductive transistor area;

forming a second epitaxial layer in the second recess;

removing the first protective layer; and

forming a second ion lightly doped region within the semiconductor substrate adjacent to the gate in the second conductive transistor area before forming the spacer.

20. The method of claim 9, wherein the first conductive transistors comprise PMOS transistors and the second conductive transistors comprise NMOS transistors.

21. The method of claim 9, wherein the first conductive transistors comprise NMOS transistors and the second conductive transistors comprise PMOS transistors.

Title

Method of fabricating metal oxide semiconductor transistor

Cross Reference To Related Applications

[0001] This is a divisional application of U. S. patent application Ser. No. 11/836,772 filed on August 9, 2007, and the contents of which are included herein by reference.

Background of the Invention

1. Field of the Invention

[0002] The present invention relates to a method for fabricating a metal oxide semiconductor (MOS) transistor, and more particularly, to a method for fabricating a strained silicon channel MOS transistor.

2. Description of the Prior Art

[0003] A conventional MOS transistor generally includes a semiconductor substrate, such as silicon, a source region, a drain region, a channel positioned between the source region and the drain region, and a gate located above the channel. The gate composed of a gate dielectric layer, a gate conductive layer positioned on the gate dielectric layer, and spacers positioned on the sidewalls of the gate conductive layer. Generally, for a given electric field across the channel of a MOS transistor, the amount of current that flows through the channel is directly proportional to a mobility of the carriers in the channel. Therefore, how to improve the carrier mobility so as to increase the speed performance of MOS transistors has become a major topic for study in the semiconductor field.

[0004] One way to increase the mobility of the carriers in the channel of an MOS transistor is to produce a mechanical stress in the channel. A compressive strained channel, such as a silicon germanium (SiGe) channel layer grown on silicon, has significant hole mobility enhancement. A tensile strained channel, such as a thin silicon channel layer grown on silicon germanium, achieves significant electron mobility enhancement. Another prior art method of obtaining a strained channel is to epitaxially grow a SiGe layer adjacent to the spacers within the semiconductor substrate after forming the spacer.

[0005] In this type of MOS transistor, a biaxial tensile strain occurs in the epitaxial silicon layer due to the silicon germanium, which has a larger lattice constant than silicon, and, as a result, the band structure alters, and the carrier mobility increases. This enhances the speed

performance of the MOS transistor.

[0006] The performance of MOS transistors has increased year after year with the diminution of critical dimensions and the advance of very large scale integrated circuits (VLSI); therefore, the demand for the speed performance of the MOS transistor has also greatly increased. However, the compressive or tensile stress obtained according to the conventional method has been hardly achieved the required extent.

[0007] Accordingly, the applicants provide a method of fabricating strained silicon channel MOS transistors to improve the shortages from the prior art, and then increase the carrier mobility of MOS transistors.

Summary of the Invention

[0008] The present invention relates to a method of fabricating a MOS transistor, and more particularly, to a method of fabricating a strained silicon channel MOS transistor to improve the disadvantages of the prior art.

[0009] According to a preferred embodiment of the present invention, a method of fabricating a MOS transistor is disclosed. The method includes the steps of: providing a semiconductor substrate; forming at least a gate on the semiconductor substrate; forming a protective layer on the semiconductor substrate, and the protective layer covering the surface of the gate; forming at least a recess within the semiconductor substrate adjacent to the gate; forming an epitaxial layer in the recess, wherein the top surface of the epitaxial layer is above the surface of the semiconductor substrate; and forming a spacer on the sidewall of the gate and on a portion of the epitaxial layer, wherein a contact surface of the epitaxial layer and the spacer is above the surface of the semiconductor substrate.

[0010] According to another aspect of the present invention, a method of fabricating a CMOS transistor is disclosed. The method includes the steps of: providing a semiconductor substrate having at least a first conductive transistor area for fabricating first conductive transistors and at least a second conductive transistor area for fabricating second conductive transistors, and an isolation structure between the first conductive transistor area and the second conductive transistor area; forming a gate on the first conductive transistor area and on the second conductive transistor area respectively; forming a first protective layer on the semiconductor substrate, and the first protective layer covering the surface of each gate; forming at least a first

recess within the semiconductor substrate adjacent to the gate in the first conductive transistor area; forming a first epitaxial layer in the first recess, wherein the top surface of the first epitaxial layer is above the surface of the semiconductor substrate; and forming a spacer on the sidewall of each gate and at least on a portion of the first epitaxial layer, wherein a contact surface of the first epitaxial layer and the spacer is above the surface of the semiconductor substrate.

[0011] The present invention further provides a MOS transistor structure, the structure comprising a gate formed on a semiconductor substrate; two raised epitaxial layers positioned respectively in the semiconductor substrate next to the relative sides of the gate; a spacer formed on the sidewall of the gate and extending laterally upon a portion of the raised epitaxial layer; and two doped region formed respectively in the semiconductor substrate next to the relative sides of the gate.

[0012] These and other objectives of the present invention will no doubt become obvious to those of ordinary skill in the art after reading the following detailed description of the preferred embodiment that is illustrated in the various figures and drawings.

Brief Description of the Drawings

[0013] Fig. 1 to Fig. 5 are cross-sectional diagrams, illustrating a fabricating method of MOS transistors in accordance with the first preferred embodiment of the present invention.

[0014] Fig. 6 shows a transmission electron microscopy picture of MOS transistors in accordance with the first preferred embodiment of the present invention.

[0015] Fig. 7 to Fig. 14 are cross-sectional diagrams, illustrating a fabricating method of MOS transistors in accordance with the second preferred embodiment of the present invention.

Detailed Description

[0016] Please refer to Fig. 1 to Fig. 5, which are cross-sectional diagrams illustrating a method for fabricating a MOS transistor in accordance with the first preferred embodiment of the present invention. For highlighting the characteristic of the present invention and for clarity of illustration, Fig. 1 to Fig. 5 merely show a first conductive transistor area and a second conductive transistor area. As shown in Fig. 1, a semiconductor substrate 200 is provided such as a silicon substrate or a silicon-on-insulator (SOI) substrate, but not limited thereto. The

semiconductor substrate 200 comprises a plurality of first conductive transistor areas 202 and a plurality of second conductive transistor areas 204, and the first conductive transistor areas 202 and the second conductive transistor areas 204 are isolated by isolation structures such as shallow trench isolations (STI) 206. Generally speaking, the STI 206 is formed by etching a trench in the semiconductor substrate 200 and then filling the trench with insulating materials such as silicon oxide. Besides, the semiconductor substrate 200 further comprises a plurality of gates 208, positioned respectively on each first conductive transistor area 202 and each second conductive transistor area 204. Each gate 208 comprises a dielectric layer 210, a conductive layer 212 positioned on the dielectric layer 210 and a cap layer 213 positioned on the conductive layer 212. In general, the dielectric layer 210 comprises isolating materials such as silicon oxide components or silicon nitride components, etc; the conductive layer 212 comprises conductive materials such as polysilicon or metal silicide; and the cap layer 213 comprises dielectric materials such as silicon nitride.

[0017] Subsequently, a protective layer 214 is formed on the semiconductor substrate 200, and the protective layer 214 covers the surface of each gate 208. According to the first preferred embodiment of the present invention, the protective layer 214 may comprise any materials with an appropriate etching selectivity to the semiconductor substrate 200 and the conductive layer 212: silicon nitride component, for instance, but not limited thereto. Silicon oxide component may also be used, but the effect of using silicon nitride is better. The protective layer 214 has a thickness of about 150 to 250Å, and is preferably about 200Å.

[0018] As shown in Fig. 2, a patterned mask 216 is coated on the second conductive transistor area 204 and a portion of the STI 206. An etching process such as an anisotropic dry etching is then carried out to etch recesses 218 in the first conductive transistor area 202. Thereafter, the patterned mask 216 is removed.

[0019] As shown in Fig. 3, after a pre-cleaning step is performed to clean the semiconductor substrate 200 of the first conductive transistor area 202, such as using DHF solution or SPM solution to remove impurities upon the surface of the recesses 218, an epitaxial growth process is carried out to form epitaxial layers 220 in the recesses 218. Then, the protective layer 214 is removed. The epitaxial layer 220 is grown in the recess 218 and it may be grown higher than the surface of the semiconductor substrate 200, so as to form a raised epitaxial layer 220. Besides, the epitaxial growth process may be an in-situ doped ion epitaxial growth process. According to the first preferred embodiment of the present invention, when the first conductive transistor area

202 is a PMOS transistor area, the epitaxial layer 220 is composed of SiGe. And when the first conductive transistor area 202 is an NMOS transistor, the epitaxial layer 220 is composed of SiC.

[0020] As shown in Fig. 4, a patterned mask (not shown) is coated on the second conductive transistor area 204. A first ion lightly doped process is carried out to form a first ion lightly doped region 222 in the first conductive transistor area 202. Then the patterned mask is removed. Thereafter, another patterned mask (not shown) is coated on the first conductive transistor area 202. A second ion lightly doped process is then carried out to form a second ion lightly doped region 224 in the second conductive transistor area 204. Then the patterned mask is removed.

[0021] As shown in Fig. 5, spacers 228 are formed on the sidewalls of each gate 280. According to the first preferred embodiment of the present invention, each spacer 228 comprises an oxide liner 230 and a nitride spacer 232. The spacers 228 cover the sidewalls of each gate 208 and also extend laterally onto the first ion lightly doped region 222 and the second ion lightly doped region 224. Each spacer 228 may also comprise an offset spacer (not shown) positioned between the gate 208 and the oxide liner 230. Because each spacer 228 in the first conductive transistor area 202 lies over the raised epitaxial layer 220, thus each spacer 228 in the first conductive transistor area 202 is tilted upward. Please refer to Fig. 10, which is a transmission electron microscopy (TEM) picture of the MOS transistors in accordance with the first preferred embodiment of the present invention.

[0022] Finally, a patterned mask (not shown) is coated on the second conductive transistor area 204. A first ion source/drain implantation process is then carried out to form a first ion source/drain region 238 in the first conductive transistor area 202; thereby a first conductive transistor 234 such as a PMOS transistor is formed in the first conductive transistor area 202. Thereafter, the patterned mask is removed. Subsequently, another patterned mask (not shown) is coated on the first conductive transistor area 202. A second ion source/drain implantation process is carried out to form a second ion source/drain region 240 in the second conductive transistor area 204; thereby a second conductive transistor 236 such as an NMOS transistor is formed in the second conductive transistor area 204. Thereafter, the patterned mask is removed.

[0023] It should be noticed that the process of forming the source/drain regions 238 as shown in Fig. 5 is an optional step depending on the method used in the epitaxial growth process. Because the epitaxial growth process as shown in Fig. 3 may be an in-situ doped epitaxial growth process, therefore, while the epitaxial layer 200 is formed, the demanded doped ions can

also be implanted into the semiconductor substrate 200 or the grown epitaxial layer 200, as a result, the corresponding source/drain regions are formed. Thus, the source/drain implantation process as shown in Fig. 5 can be skipped. According to the first preferred embodiment of the present invention, when the first conductive transistor area 202 is a PMOS transistor area, the epitaxial growth process, which is carried out to form the epitaxial layer 220 composed of silicon germanium, may be an in-situ doped boron epitaxial growth process. Accordingly, the corresponding source/drain regions are formed by implanting the demanded boron ions within the semiconductor substrate 200 while the epitaxial layer 220 is formed.

[0024] Please refer to Fig. 7 to Fig. 14, which are cross-sectional diagrams illustrating a method for fabricating a MOS transistor in accordance with the second preferred embodiment of the present invention. For highlighting the characteristic of the present invention and for clarity of illustration, Fig. 7 to Fig. 14 merely show a first conductive transistor area and a second conductive transistor area. As shown in Fig. 7, a semiconductor substrate 300 is provided such as a silicon substrate or a silicon-on-insulator (SOI) substrate, but not limited thereto. The semiconductor substrate 300 comprises a plurality of first conductive transistor areas 302 and a plurality of second conductive transistor areas 304, and the first conductive transistor areas 302 and the second conductive transistor areas 304 are isolated by isolation structures such as shallow trench isolations (STI) 306. Generally speaking, STI 306 is formed by etching a trench in the semiconductor substrate 300 and then filling the trench with insulating materials such as silicon oxide. Besides, the semiconductor substrate 300 further comprises a plurality of gates 308, positioned respectively on each first conductive transistor area 302 and each second conductive transistor area 304. Each gate 308 comprises a dielectric layer 310, a conductive layer 312 positioned on the dielectric layer 310 and a cap layer 313 positioned on the conductive layer 312. In general, the dielectric layer 310 comprises isolating materials such as silicon oxide components or silicon nitride components, etc; the conductive layer 312 comprises conductive materials such as polysilicon or metal silicide; and the cap layer 313 comprises dielectric materials such as silicon nitride.

[0025] Subsequently, a first protective layer 314 is formed on the semiconductor substrate 300, and the first protective layer 314 covers the surface of each gate 308. According to the second preferred embodiment of the present invention, the first protective layer 314 may comprise any materials with an appropriate etching selectivity to the semiconductor substrate 300 and the conductive layer 312: silicon nitride component, for instance, but not limited thereto. Silicon oxide component may also be used, but the effect of using silicon nitride is better. The first

protective layer 314 has a thickness of about 150 to 250Å, and is preferably about 200Å.

[0026] As shown in Fig. 8, a first patterned mask 316 is coated on the second conductive transistor area 304 and a portion of the STI 306. An etching process such as an anisotropic dry etching is carried out to form first recesses 318 in the first conductive transistor area 302. Thereafter, the first patterned mask 316 is removed.

[0027] As shown in Fig. 9, after a pre-cleaning step is performed to clean the semiconductor substrate 300 of the first conductive transistor area 302, such as using DHF solution or SPM solution to remove impurities upon the surface of the first recesses 318, an epitaxial growth process is carried out to form first epitaxial layers 320 in the first recesses 318. Then, the first protective layer 314 is removed. The first epitaxial layer 320 is grown in the first recess 318 and it may be grown higher than the surface of the semiconductor substrate 300, so as to form a raised epitaxial layer. Besides, the epitaxial growth process may be an in-situ doped ion epitaxial growth process. According to the second preferred embodiment of the present invention, when the first conductive transistor area 302 is a PMOS transistor area, the first epitaxial layer 320 is composed of SiGe.

[0028] As shown in Fig. 10, a second protective layer 322 is formed on the semiconductor substrate 300 and the second protective layer 322 covers the surface of each gate 308. According to the second preferred embodiment of the present invention, the second protective layer 322 may comprise any materials with an appropriate etching selectivity to the semiconductor substrate 300 and the conductive layer 312: silicon nitride component, for instance, but not limited thereto. Silicon oxide component may also be used, but the effect of using silicon nitride is better. The second protective layer 322 has a thickness of about 150 to 250Å, and is preferably about 200Å.

[0029] As shown in Fig. 11, a second patterned mask 324 is coated on the first conductive transistor area 302 and a portion of the STI 306. An etching process such as an anisotropic dry etching is carried out to form second recesses 326 in the second conductive transistor area 304. Thereafter, the second patterned mask 324 is removed.

[0030] It should be noticed that the steps of forming the second recess 326 shown in Fig. 10 to Fig. 11 might be performed without using the second protective layer 322. Namely, after forming the first epitaxial layer 320 as shown in Fig. 9, the first protective layer 314 is not removed and

then the second patterned mask 324 is coated directly on the first conductive transistor area 302 and a portion of the STI 306. Subsequently, an etching process such as that shown in Fig. 11 is carried out to form the second recesses 326 in the second conductive transistor area 304. Thereafter, the second patterned mask 324 and the first protective layer 314 are removed. Those skilled in the art will readily observe that numerous modifications and alterations of the method may be made while retaining the teachings of the invention.

[0031] As shown in Fig. 12, after a pre-cleaning step is performed to clean the semiconductor substrate 300 of the second conductive transistor area 304, such as using DHF solution or SPM solution to remove impurities upon the surface of the second recesses 326, an epitaxial growth process is carried out to form second epitaxial layers 328 in the second recesses 326. Then, the second protective layer 322 is removed. The second epitaxial layer 328 is grown in the second recess 326 and it may be grown higher than the surface of the semiconductor substrate 300, so as to form a raised epitaxial layer. Besides, the epitaxial growth process may be an in-situ doped ion epitaxial growth process. According to the second preferred embodiment of the present invention, when the second conductive transistor area 304 is an NMOS transistor area, the second epitaxial layer 328 is composed of SiC. It should be noticed that the process of forming the first epitaxial layer 320 as shown in Fig. 7 to Fig. 9 might be performed after the process of forming the second epitaxial layer 328 as shown in Fig. 10 to Fig. 12. Those skilled in the art will readily observe that numerous modifications and alterations of the method may be made while retaining the teachings of the invention.

[0032] As shown in Fig. 13, a patterned mask (not shown) is coated on the second conductive transistor area 304. A first ion lightly doped process is carried out to form a first ion lightly doped region 330 in the first conductive transistor area 302. Then the patterned mask is removed. Thereafter, another patterned mask (not shown) is coated on the first conductive transistor area 302. A second ion lightly doped process is then carried out to form a second ion lightly doped region 332 in the second conductive transistor area 304. Then the patterned mask is removed.

[0033] As shown in Fig. 14, spacers 334 are formed on the sidewalls of each gate 308. According to the second preferred embodiment of the present invention, each spacer 334 comprises an oxide liner 336 and a nitride spacer 338. The spacers 334 cover the sidewalls of each gate 308 and extend laterally onto the first ion lightly doped region 330 and the second ion lightly doped region 332. The spacers 334 also cover a portion of the first epitaxial layer 320 and a portion of the second epitaxial layer 328. Additionally, each spacer 334 may further comprise

an offset spacer (not shown) positioned between the gate 308 and the oxide liner 336.

[0034] Finally, a patterned mask (not shown) is coated on the second conductive transistor area 304. A first ion source/drain implantation process is then carried out to form a first ion source/drain region 344 in the first conductive transistor area 302; thereby a first conductive transistor 340 such as a PMOS transistor is formed in the first conductive transistor area 302. Thereafter, the patterned mask is removed. Subsequently, another patterned mask (not shown) is coated on the first conductive transistor area 302. A second ion source/drain implantation process is carried out to form a second ion source/drain region 346 in the second conductive transistor area 304; thereby a second conductive transistor 342 such as an NMOS transistor is formed in the second conductive transistor area 304. Thereafter, the patterned mask is removed.

[0035] It should be noticed that the processes of forming the first source/drain regions 334 and the second source/drain regions 346 as shown in Fig. 14 is an optional step depending on the method used in the epitaxial growth process. Because the epitaxial growth process as shown in Fig. 9 may be an in-situ doped epitaxial growth process, therefore, while the first epitaxial layer 320 or the second epitaxial layer 328 is formed, the demanded doped ions can also be implanted into the semiconductor substrate 300 or the grown epitaxial layers 320, 328, as a result, the corresponding source/drain regions are formed. Accordingly, source/drain implantation as shown in Fig. 14 can be skipped.

[0036] Since the characteristic of the present invention is to form the epitaxial layer before forming the spacer, thus the distance between the gate and the epitaxial layer is no longer limited by the width of the spacer. Besides, the process of etching the recess is carried out before forming the spacer. At this moment, the pattern density on the semiconductor substrate is lower than the time when the spacer is formed, thus the micro-loading effect caused by the pattern density can be reduced, and then the uniformity in etching the recess is increased. Additionally, the lightly doped regions and the source/drain regions are doped after forming the epitaxial layer, thus the doped ions will not be affected by the high temperature epitaxial growth process, which leads the doped ions to diffuse. Finally, since the present invention provides a protective layer to cover the semiconductor substrate and the shallow trench isolation (STI), the problem of the STI thickness loss will be reduced.

[0037] Those skilled in the art will readily observe that numerous modifications and alterations of the device and method may be made while retaining the teachings of the invention.

Accordingly, the above disclosure should be construed as limited only by the metes and bounds of the appended claims.

Electronic Patent Application Fee Transmittal				
Application Number:				
Filing Date:				
Title of Invention:		Method of fabricating metal oxide semiconductor transistor		
First Named Inventor/Applicant Name:		Chu-Yin Tseng		
Filer:		Winston Hsu/Sibyl Yu		
Attorney Docket Number:		NAUP0913USA1		
Filed as Large Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Utility application filing	1011	1	330	330
Utility Search Fee	1111	1	540	540
Utility Examination Fee	1311	1	220	220
Pages:				
Claims:				
Claims in excess of 20	1202	1	52	52
Miscellaneous-Filing:				
Petition:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				1142

Electronic Acknowledgement Receipt	
EFS ID:	7629814
Application Number:	12781826
International Application Number:	
Confirmation Number:	3483
Title of Invention:	Method of fabricating metal oxide semiconductor transistor
First Named Inventor/Applicant Name:	Chu-Yin Tseng
Customer Number:	27765
Filer:	Winston Hsu/Janine Chang
Filer Authorized By:	Winston Hsu
Attorney Docket Number:	NAUP0913USA1
Receipt Date:	18-MAY-2010
Filing Date:	
Time Stamp:	03:22:41
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	\$1142
RAM confirmation Number	7570
Deposit Account	503105
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees) Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)	

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)					
Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees)					
Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)					
File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Application Data Sheet	846423.PDF	890640	no	6
			1fec60a819e97e56e8f9d9e31c5e8bfdc58c0b4		
Warnings:					
Information:					
2	Oath or Declaration filed	846369.PDF	186362	no	3
			1fd6921dd2c17a9b879479700258fc896c5cb332		
Warnings:					
Information:					
3	Power of Attorney	846368.PDF	186362	no	3
			238a5591af2d0122e4e8d013eaeef4fb1a350b196		
Warnings:					
Information:					
4	Information Disclosure Statement (IDS) Filed (SB/08)	846354.PDF	347755	no	4
			5c3dcdfab09041e1123fcd7e36a7510bb4d884fa		
Warnings:					
Information:					
This is not an USPTO supplied IDS fillable form					
5	Drawings-other than black and white line drawings	845865.PDF	457209	no	14
			d9d9b89e1f5d19feab597e883ee81c7f5213b0e8		
Warnings:					
Information:					
6	Abstract	845864.PDF	31718	no	1
			7f07e1432f20c497d1c3e4971f9bf3c6ef620e7f		
Warnings:					
Information:					
7	Claims	845863.PDF	40558	no	3
			920b10ccb3a01fafee88e706393e5822c35218d8		
Warnings:					
Information:					

8	Specification	845862.PDF	84942 0134ef0020a8f36e834d51d824b367217ffb8c	no	10
Warnings:					
Information:					
9	Fee Worksheet (PTO-875)	fee-info.pdf	36036 77f16a6b3c4c07f1e53abe33e2b4124515082aef	no	2
Warnings:					
Information:					
Total Files Size (in bytes):			2261582		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	NAUP0913USA1
		Application Number	
Title of Invention	Method of fabricating metal oxide semiconductor transistor		
The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76. This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.			

Secrecy Order 37 CFR 5.2

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Applicant Information:

Applicant 1					Remove
Applicant Authority		☒ Inventor		☐ Legal Representative under 35 U.S.C. 117	☐ Party of Interest under 35 U.S.C. 118
Prefix	Given Name	Middle Name	Family Name	Suffix	
	Chu-Yin		Tseng		
Residence Information (Select One) ☐ US Residency ☒ Non US Residency ☐ Active US Military Service					
City	Tainan County		Country Of Residenceⁱ	TW	
Citizenship under 37 CFR 1.41(b)ⁱ		TW			
Mailing Address of Applicant:					
Address 1		No.270, Jiabei Village, Shanhua Township			
Address 2					
City	Tainan County		State/Province		
Postal Code			Countryⁱ	TW	
Applicant 2					Remove
Applicant Authority		☒ Inventor		☐ Legal Representative under 35 U.S.C. 117	☐ Party of Interest under 35 U.S.C. 118
Prefix	Given Name	Middle Name	Family Name	Suffix	
	Shih-Chieh		Hsu		
Residence Information (Select One) ☐ US Residency ☒ Non US Residency ☐ Active US Military Service					
City	Hsinchu City		Country Of Residenceⁱ	TW	
Citizenship under 37 CFR 1.41(b)ⁱ		TW			
Mailing Address of Applicant:					
Address 1		No.63, Jinshan 9th St			
Address 2					
City	Hsinchu City		State/Province		
Postal Code			Countryⁱ	TW	
Applicant 3					Remove
Applicant Authority		☒ Inventor		☐ Legal Representative under 35 U.S.C. 117	☐ Party of Interest under 35 U.S.C. 118
Prefix	Given Name	Middle Name	Family Name	Suffix	
	Chih-Chiang		Wu		
Residence Information (Select One) ☐ US Residency ☒ Non US Residency ☐ Active US Military Service					
City	Taichung County		Country Of Residenceⁱ	TW	

Application Data Sheet 37 CFR 1.76		Attorney Docket Number		NAUP0913USA1	
		Application Number			
Title of Invention		Method of fabricating metal oxide semiconductor transistor			

Citizenship under 37 CFR 1.41(b) i		TW			
Mailing Address of Applicant:					
Address 1		No.67-4, Sec. 3, Minzu Rd., Tanzih Township			
Address 2					
City	Taichung County		State/Province		
Postal Code			Countryⁱ	TW	
Applicant 4					Remove
Applicant Authority		☒ Inventor		☐ Legal Representative under 35 U.S.C. 117	
				☐ Party of Interest under 35 U.S.C. 118	
Prefix	Given Name	Middle Name		Family Name	Suffix
	Shyh-Fann			Ting	
Residence Information (Select One) ☐ US Residency ☒ Non US Residency ☐ Active US Military Service					
City	Tai-Nan City		Country Of Residenceⁱ		TW
Citizenship under 37 CFR 1.41(b) i		TW			
Mailing Address of Applicant:					
Address 1		11F., No.2, Lane 6, Chongshan 12th St., East District			
Address 2					
City	Tai-Nan City		State/Province		
Postal Code			Countryⁱ	TW	
Applicant 5					Remove
Applicant Authority		☒ Inventor		☐ Legal Representative under 35 U.S.C. 117	
				☐ Party of Interest under 35 U.S.C. 118	
Prefix	Given Name	Middle Name		Family Name	Suffix
	Po-Lun			Cheng	
Residence Information (Select One) ☐ US Residency ☒ Non US Residency ☐ Active US Military Service					
City	Kao-Hsiung Hsien		Country Of Residenceⁱ		TW
Citizenship under 37 CFR 1.41(b) i		TW			
Mailing Address of Applicant:					
Address 1		No. 6, Jui-Chu Rd., Feng-Shan City			
Address 2					
City	Kao-Hsiung Hsien		State/Province		
Postal Code			Countryⁱ	TW	
Applicant 6					Remove
Applicant Authority		☒ Inventor		☐ Legal Representative under 35 U.S.C. 117	
				☐ Party of Interest under 35 U.S.C. 118	
Prefix	Given Name	Middle Name		Family Name	Suffix
	Hsuan-Hsu			Chen	
Residence Information (Select One) ☐ US Residency ☒ Non US Residency ☐ Active US Military Service					
City	Tai-Nan City		Country Of Residenceⁱ		TW
Citizenship under 37 CFR 1.41(b) i		TW			

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	NAUP0913USA1
		Application Number	
Title of Invention	Method of fabricating metal oxide semiconductor transistor		

Mailing Address of Applicant:

Address 1	No.2, Lane 276, Yujhong Rd.		
Address 2			
City	Tai-Nan City	State/Province	
Postal Code		Country	TW

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button.

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

☐ An Address is being provided for the correspondence information of this application.

Customer Number	27765		
Email Address	winstonhsu@naipo.com	Add Email	Remove Email

Application Information:

Title of the Invention	Method of fabricating metal oxide semiconductor transistor		
Attorney Docket Number	NAUP0913USA1	Small Entity Status Claimed	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Suggested Class (if any)		Sub Class (if any)	
Suggested Technology Center (if any)			
Total Number of Drawing Sheets (if any)	14	Suggested Figure for Publication (if any)	

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32). Enter either Customer Number or complete the Representative Name section below. If both sections are completed the Customer Number will be used for the Representative Information during processing.

Please Select One:	☒ Customer Number	☐ US Patent Practitioner	☐ Limited Recognition (37 CFR 11.9)
Customer Number	27765		

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	NAUP0913USA1
		Application Number	
Title of Invention	Method of fabricating metal oxide semiconductor transistor		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, or 365(c) or indicate National Stage entry from a PCT application. Providing this information in the application data sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78(a)(2) or CFR 1.78(a)(4), and need not otherwise be made part of the specification.

Prior Application Status	Pending	Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
	Division of	11836772	2007-08-09
Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the Add button.			Add

Foreign Priority Information:

This section allows for the applicant to claim benefit of foreign priority and to identify any prior foreign application for which priority is not claimed. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55(a).

			Remove
Application Number	Country ⁱ	Parent Filing Date (YYYY-MM-DD)	Priority Claimed
			☐ Yes ☐ No
Additional Foreign Priority Data may be generated within this form by selecting the Add button.			Add

Assignee Information:

Providing this information in the application data sheet does not substitute for compliance with any requirement of part 3 of Title 37 of the CFR to have an assignment recorded in the Office.

Assignee 1					Remove
If the Assignee is an Organization check here. ☐					
Prefix	Given Name	Middle Name	Family Name	Suffix	
Mailing Address Information:					
Address 1					
Address 2					
City		State/Province			
Country ⁱ		Postal Code			
Phone Number		Fax Number			
Email Address					
Additional Assignee Data may be generated within this form by selecting the Add button.					Add

Signature:

A signature of the applicant or representative is required in accordance with 37 CFR 1.33 and 10.18. Please see 37 CFR 1.4(d) for the form of the signature.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number		NAUP0913USA1	
		Application Number			
Title of Invention		Method of fabricating metal oxide semiconductor transistor			
Signature		/WINSTON HSU/		Date (YYYY-MM-DD)	
				2010-05-17	
First Name	WINSTON	Last Name	HSU	Registration Number	41526

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

COMBINED DECLARATION AND POWER OF ATTORNEY

As a below named inventor , I hereby declare that :

I believe I am the sole (if only one name appears below) , or joint (if more than one name appears) , original and first inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled :

"Method of fabricating metal oxide semiconductor transistor"

 † The specification for the above entitled invention is filed herewith.

 The specification for the above entitled invention was filed previously

with application serial number: Filing Date:

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the patentability of the invention disclosed in this application in accordance with Title 37, Code of Federal Regulations, Section 1.56 (a). I further acknowledge the duty in any continuation-in-part application to disclose to the Patent and Trademark Office all information known to be material to the patentability of the invention disclosed in this application, as defined in 1.56, which became available to me between the filing date of the prior application and the filing date of this application.

PRIORITY CLAIM

 + There is no claim of priority

 Claim of priority is based on the following:

**POWER OF ATTORNEY and
CORRESPONDENCE ADDRESS INDICATION**

I hereby revoke all previous powers of attorney given in the above-identified application.

I hereby appoint the practitioners associated with the Customer Number: 27765 as my/our attorney(s) or agent(s) to prosecute the application identified above, and to transact all business in the United States Patent and Trademark Office connected therewith.

Please recognize or change the correspondence address for the above-identified application to the address associated with the above-mentioned Customer Number.

DECLARATION

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment or both under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued hereon.

(請發明人務必簽署日期)

Date:	<u>JUN 28 2007</u>	<u>Chu Yin Tseng</u>
	Printed Name:	<u>Chu-Yin Tseng</u>
	Citizen of:	<u>R.O.C.</u>
Date:	<u>JUN 28 2007</u>	<u>Shih-Chieh Hsu</u>
	Printed Name:	<u>Shih-Chieh Hsu</u>
	Citizen of:	<u>R.O.C.</u>
Date:	<u>JUN 28 2007</u>	<u>Chih-Chiang Wu</u>
	Printed Name:	<u>Chih-Chiang Wu</u>
	Citizen of:	<u>R.O.C.</u>
Date:	<u>JUN 28 2007</u>	<u>Shyh-Fann Ting</u>
	Printed Name:	<u>Shyh-Fann Ting</u>
	Citizen of:	<u>R.O.C.</u>
Date:	<u>JUN 28 2007</u>	<u>Po-Lun Cheng</u>
	Printed Name:	<u>Po-Lun Cheng</u>
	Citizen of:	<u>R.O.C.</u>

Date: JUN 28 2007

Hsuan-Hsu Chen

Printed Name: Hsuan-Hsu Chen

Citizen of: R.O.C.

NPO#NAU-P0913-USA:0
CUST#UMCD-2007-0007

Combined Declaration and Power of Attorney, Page 3 of 3

F#NPO-P0001E-US
DSB0-096U010242

COMBINED DECLARATION AND POWER OF ATTORNEY

As a below named inventor , I hereby declare that :

I believe I am the sole (if only one name appears below) , or joint (if more than one name appears) , original and first inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled :

"Method of fabricating metal oxide semiconductor transistor"

 † The specification for the above entitled invention is filed herewith.

 The specification for the above entitled invention was filed previously

with application serial number: Filing Date:

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the patentability of the invention disclosed in this application in accordance with Title 37, Code of Federal Regulations, Section 1.56 (a). I further acknowledge the duty in any continuation-in-part application to disclose to the Patent and Trademark Office all information known to be material to the patentability of the invention disclosed in this application, as defined in 1.56, which became available to me between the filing date of the prior application and the filing date of this application.

PRIORITY CLAIM

 + There is no claim of priority

 Claim of priority is based on the following:

POWER OF ATTORNEY and CORRESPONDENCE ADDRESS INDICATION

I hereby revoke all previous powers of attorney given in the above-identified application.

I hereby appoint the practitioners associated with the Customer Number: 27765 as my/our attorney(s) or agent(s) to prosecute the application identified above, and to transact all business in the United States Patent and Trademark Office connected therewith.

Please recognize or change the correspondence address for the above-identified application to the address associated with the above-mentioned Customer Number.

DECLARATION

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment or both under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued hereon.

(請發明人務必簽署日期)

Date:	<u>JUN 28 2007</u>	<u>Chu Yin Tseng</u>
	Printed Name:	<u>Chu-Yin Tseng</u>
	Citizen of:	<u>R.O.C.</u>
Date:	<u>JUN 28 2007</u>	<u>Shih-Chieh Hsu</u>
	Printed Name:	<u>Shih-Chieh Hsu</u>
	Citizen of:	<u>R.O.C.</u>
Date:	<u>JUN 28 2007</u>	<u>Chih-Chiang Wu</u>
	Printed Name:	<u>Chih-Chiang Wu</u>
	Citizen of:	<u>R.O.C.</u>
Date:	<u>JUN 28 2007</u>	<u>Shyh-Fann Ting</u>
	Printed Name:	<u>Shyh-Fann Ting</u>
	Citizen of:	<u>R.O.C.</u>
Date:	<u>JUN 28 2007</u>	<u>Po-Lun Cheng</u>
	Printed Name:	<u>Po-Lun Cheng</u>
	Citizen of:	<u>R.O.C.</u>

Date: JUN 28 2007

Hsuan-Hsu Chen

Printed Name: Hsuan-Hsu Chen

Citizen of: R.O.C.

NPO#NAU-P0913-USA:0
CUST#UMCD-2007-0007

Combined Declaration and Power of Attorney, Page 3 of 3

F#NPO-P0001E-US
DSB0-096U010242

Date: 05/18/10

Approved for use through 7/31/2006. OMB 0651-0032

U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875					Application or Docket Number 12/781,826		
APPLICATION AS FILED – PART I							
(Column 1)		(Column 2)		SMALL ENTITY		OR	
OTHER THAN SMALL ENTITY							
FOR	NUMBER FILED	NUMBER EXTRA	RATE (\$)	FEE (\$)	RATE (\$)	FEE (\$)	
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A		N/A	330	
SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A		N/A	540	
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A		N/A	220	
TOTAL CLAIMS (37 CFR 1.16(i))	21	minus 20 = 1	x\$26		x\$52	52	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	2	minus 3 = *	x\$110		x\$220		
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$260 (\$130 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR						
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))			195		390		
			TOTAL		TOTAL	1142	
* If the difference in column 1 is less than zero, enter "0" in column 2.							
APPLICATION AS AMENDED – PART II							
(Column 1)		(Column 2)		SMALL ENTITY		OR	
OTHER THAN SMALL ENTITY							
AMENDMENT A	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	RATE (\$)	ADDITIONAL FEE (\$)
Total (37 CFR 1.16(i))	*	Minus **	=	X =		X =	
Independent (37 CFR 1.16(h))	*	Minus ***	=	X =		X =	
Application Size Fee (37 CFR 1.16(s))							
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))				N/A		N/A	
				TOTAL ADD'T FEE		TOTAL ADD'T FEE	
(Column 1)		(Column 2)		SMALL ENTITY		OR	
OTHER THAN SMALL ENTITY							
AMENDMENT B	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	RATE (\$)	ADDITIONAL FEE (\$)
Total (37 CFR 1.16(i))	*	Minus **	=	X =		X =	
Independent (37 CFR 1.16(h))	*	Minus ***	=	X =		X =	
Application Size Fee (37 CFR 1.16(s))							
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))				N/A		N/A	
				TOTAL ADD'T FEE		TOTAL ADD'T FEE	
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.							

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

SCORE Placeholder Sheet for IFW Content

Application Number: 12781826

Document Date: 5/18/2010

The presence of this form in the IFW record indicates that the following document type was received in electronic format on the date identified above. This content is stored in the SCORE database.

- Drawings

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Form Revision Date: May 1, 2009



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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO.	TOT CLAIMS	IND CLAIMS
12/781,826	05/18/2010	2811	1142	NAUP0913USA1	21	2

CONFIRMATION NO. 3483

27765
NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
P.O. BOX 506
MERRIFIELD, VA 22116

FILING RECEIPT



OC000000041846605

Date Mailed: 06/02/2010

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Applicant(s)

Chu-Yin Tseng, Tainan County, TAIWAN;
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Shyh-Fann Ting, Tai-Nan City, TAIWAN;
Po-Lun Cheng, Kao-Hsiung Hsien, TAIWAN;
Hsuan-Hsu Chen, Tai-Nan City, TAIWAN;

Power of Attorney: The patent practitioners associated with Customer Number 27765

Domestic Priority data as claimed by applicant

This application is a DIV of 11/836,772 08/09/2007

Foreign Applications

If Required, Foreign Filing License Granted: 05/27/2010

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 12/781,826**

Projected Publication Date: 09/09/2010

Non-Publication Request: No

Early Publication Request: No

Title

Method of fabricating metal oxide semiconductor transistor

Preliminary Class

257

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at <http://www.uspto.gov/web/offices/pac/doc/general/index.html>.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, <http://www.stopfakes.gov>. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4158).

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Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

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NOT GRANTED

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
12/781,826	05/18/2010	Chu-Yin Tseng	NAUP0913USA1

CONFIRMATION NO. 3483

27765
NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
P.O. BOX 506
MERRIFIELD, VA 22116

PUBLICATION NOTICE



OC000000043415669

Title:Method of fabricating metal oxide semiconductor transistor

Publication No.US-2010-0227445-A1

Publication Date:09/09/2010

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publicly available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently <http://www.uspto.gov/patft/>.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Office of Public Records. The Office of Public Records can be reached by telephone at (703) 308-9726 or (800) 972-6382, by facsimile at (703) 305-8759, by mail addressed to the United States Patent and Trademark Office, Office of Public Records, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently <http://pair.uspto.gov/>. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 1-866-217-9197.

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/781,826	05/18/2010	Chu-Yin Tseng	NAUP0913USA1	3483
27765 7590 01/27/2011 NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION P.O. BOX 506 MERRIFIELD, VA 22116			EXAMINER DANG, PHUC T	
			ART UNIT 2892	PAPER NUMBER
			NOTIFICATION DATE 01/27/2011	DELIVERY MODE ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

Patent.admin.uspto.Rcv@naipo.com
mis.ap.uspto@naipo.com

Office Action Summary	Application No. 12/781,826	Applicant(s) TSENG ET AL.	
	Examiner Phuc T. Dang	Art Unit 2892	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on 18 May 2010.

2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) 1-21 is/are pending in the application.

 4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) 1-15, 20 and 21 is/are rejected.

7) ☒ Claim(s) 16-19 is/are objected to.

8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) ☒ The specification is objected to by the Examiner.

10) ☒ The drawing(s) filed on 18 May 2010 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) ☐ All b) ☐ Some * c) ☐ None of:
 1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892) 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date <u>05/18/2010</u>	4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____. 5) ☐ Notice of Informal Patent Application 6) ☐ Other: _____.
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DETAILED ACTION

1. This application is a DIV of 11/836,772 08/09/2007 PAT 7,745,847.

Oath/Declaration

2. The oath/declaration filed on 05/18/2010 is acceptable.

Information Disclosure Statement

3. The office acknowledges receipt of the following items from the applicant:

Information Disclosure Statement (IDS) filed on 05/18/2010.

Drawings

4. The drawings are objected to because there is no figure showing a contact surface between the epitaxial layer in the recess and the spacer on the sidewall of the gate is above the surface of the semiconductor substrate as claimed in claims 1 and 9. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any

Art Unit: 2892

required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

5. The specification is objected to for the following reason:

On the specification filed on 05/18/2010, paragraph [0001], line 2, insert -- PAT 7,745,847 -- after "...August 9, 2007".

The specification has been updated.

Claim Rejections - 35 USC § 102

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

6. Claims 1-3 and 7 are rejected under 35 U.S.C. 102 (e) as being anticipated by Chen et al., hereafter "Chen" (U.S. Patent No. 7,381,623 B1).

Regarding claims 1-3, Chen discloses a method of fabricating a MOS transistor, comprising:

providing a semiconductor substrate (110);

forming at least a gate (140) on the semiconductor substrate;

forming a protective layer (160) on the semiconductor substrate, and the protective layer covering the surface of the gate;

forming at least a recess (400a) within the semiconductor substrate adjacent to the gate;

forming an epitaxial layer (500a/500b) in the recess, wherein the top surface of the epitaxial layer is above the surface of the semiconductor substrate; and

forming a spacer (720b) on the sidewall of the gate and on a portion of the epitaxial layer, wherein a contact surface of the epitaxial layer and the spacer is above the surface of the semiconductor substrate (Figs. 1-7).

Regarding claim 7, Chen discloses further comprising a step of forming a source/drain region (700a/710a) within the semiconductor substrate adjacent to the gate after forming the spacer (220b) (Fig. 7).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claims 9-12, 15 and 20-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen in view of Han et al., hereafter "Han" (U.S. Patent No. 7,800,182 B2).

Regarding claims 9-11 and 15, Chen discloses a method of fabricating a CMOS transistor, comprising:

providing a semiconductor substrate (110) having at least a first conductive transistor area

(12) for fabricating first conductive transistors and at least a second conductive transistor area

(130) for fabricating second conductive transistors;

forming a gate (140) on the first conductive transistor area and on the second conductive transistor area respectively;

forming a first protective layer (160) on the semiconductor substrate, and the first protective layer covering the surface of each gate;

forming at least a first recess (400a) within the semiconductor substrate adjacent to the gate in the first conductive transistor area;

forming a first epitaxial layer (500a/500b) in the first recess, wherein the top surface of the first epitaxial layer is above the surface of the semiconductor substrate; and

forming a spacer (720b) on the sidewall of each gate and at least on a portion of the first epitaxial layer, wherein a contact surface of the first epitaxial layer and the spacer is above the surface of the semiconductor substrate (Figs. 1-7).

Chen discloses the features of the claimed invention as discussed above, but does not disclose an isolation structure between the first conductive transistor area and the second conductive transistor area.

However, Han, in the same field of endeavor, discloses an isolation (38) between the first conductive transistor area (31) and the second conductive transistor area (32) (Fig. 1).

It would have been obvious to one having ordinary skilled in the art at the time the invention was made to modify the teaching of Chen to form an isolation structure between the first conductive transistor area and the second conductive transistor area as taught by Han for a purpose of defining the boundaries of their diffusion regions.

Regarding claim 12, Chen does not disclose the first protective layer has a thickness of about 150 to 250 angstroms. However, the selection of the claimed process parameters would have been obvious to one having ordinary skill in the art at the time the invention was made to form the thickness of the first protective layer within the claimed range, since it is well settled that when the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding claims 20-21, Chen does not disclose wherein the first conductive transistors comprise PMOS transistors and the first conductive transistors comprise PMOS transistors and vice-versa.

It would have been an obvious matter of design choice to modify the MOS transistor comprises PMOS and NMOS in order to improve the performance of the MOS transistor, since it has been held to be within the general skill of the worker in the art to select any type of the transistor on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416.

8. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al., hereafter "Chen" (U.S. Patent No. 7,381,623 B1).

Regarding claim 4, Chen does not disclose the protective layer has a thickness of about 150 to 250 angstroms. However, the selection of the claimed process parameters would have been obvious to one having ordinary skill in the art at the time the invention was made to form the thickness of the protective layer within the claimed range, since it is well settled that when the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

9. Claims 5-6 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen in view of Chien et al., hereafter “Chien” (U.S. Patent No. 6,815,770 B1).

Regarding claims 5-6, Chen discloses the features of the claimed invention as discussed above, but does not disclose wherein the spacer further comprises an offset spacer, positioned between the gate and the spacer, wherein the spacer further comprises an oxide liner and a nitride spacer.

However, Chien, in the same field of endeavor, discloses the spacer further comprises an offset spacer, positioned between the gate and the spacer, wherein the spacer further comprises an oxide liner and a nitride spacer (Fig. 1).

It would have been obvious to one having ordinary skilled in the art at the time the invention was made to modify the teaching of Chen to form the spacer further comprises an offset spacer, positioned between the gate and the spacer, wherein the spacer further comprises an oxide liner and a nitride spacer as taught by Chien for a purpose of controlling the step of doping.

Regarding claim 8, Chen discloses the features of the claimed invention as discussed above, but does not disclose further comprising a lightly doped drain disposed in the semiconductor substrate adjacent to the gate.

However, Chien, in the same field of endeavor, discloses further comprising a lightly doped drain disposed in the semiconductor substrate adjacent to the gate (Figs. 1 & 4 and Abstract).

It would have been obvious to one having ordinary skilled in the art at the time the invention was made to modify the teaching of Chen to form a lightly doped drain disposed in the semiconductor substrate adjacent to the gate as taught by Chien for a purpose of improving the performance of the MOS transistor.

10. Claims 13-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen and Han in view of Chien et al., hereafter "Chien" (U.S. Patent No. 6,815,770 B1).

Regarding claims 13-14, claims 13-14 are rejected similar to claims 5-6 above.

Allowable Subject Matter

11. The following is a statement of reason for the indication of allowable subject matter:

Claims 16-19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

None of the prior art of records disclose after removing the first protective layer, the method further comprising forming a second protective layer on the semiconductor substrate, and the second protective layer covering the surface of each gate; forming at least a second recess within the semiconductor substrate adjacent to the gate in the second conductive transistor area; forming a second epitaxial layer in the second recess; removing the second protective layer; and forming a second ion lightly doped region within the semiconductor substrate adjacent to the gate in the second conductive transistor area before forming the spacer as cited in claim 16 and after forming the first epitaxial layer, the method further comprising forming at least a second recess within the semiconductor substrate adjacent to the gate in the second conductive transistor area; forming a second epitaxial layer in the second recess; removing the first protective layer; and forming a second ion lightly doped region within the semiconductor substrate adjacent to the gate in the second conductive transistor area before forming the spacer as cited in claim 19.

Claims 17-18 are directly or indirectly depend on claim 16, then, they also would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Cited Prior Arts

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Tseng et al. (U.S. Patent No. 7,745,847 B2).

Conclusion

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phuc T. Dang whose telephone number is 571-272-1776. The examiner can normally be reached on 8:00 am-5:00 pm.

14. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thao X. Le can be reached on (571) 272-1708. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9306 for regular communications and Final communications.

15. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

/Phuc T Dang/

Primary Examiner, Art Unit 2892

Application/Control Number: 12/781,826
Art Unit: 2892

Page 10

Notice of References Cited	Application/Control No. 12/781,826	Applicant(s)/Patent Under Reexamination TSENG ET AL.	
	Examiner Phuc T. Dang	Art Unit 2892	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-7,381,623 B1	06-2008	Chen et al.	438/300
*	B	US-7,800,182 B2	09-2010	Han et al.	257/369
*	C	US-6,815,770 B1	11-2004	Chien et al.	257/344
*	D	US-7,745,847 B2	06-2010	Tseng et al.	257/190
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

<i>Index of Claims</i> 	Application/Control No. 12781826	Applicant(s)/Patent Under Reexamination TSENG ET AL.
	Examiner Phuc T Dang	Art Unit 2892

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47										
CLAIM		DATE								
Final	Original	01/21/2011								
	1	✓								
	2	✓								
	3	✓								
	4	✓								
	5	✓								
	6	✓								
	7	✓								
	8	✓								
	9	✓								
	10	✓								
	11	✓								
	12	✓								
	13	✓								
	14	✓								
	15	✓								
	16	O								
	17	O								
	18	O								
	19	O								
	20	✓								
	21	✓								

Search Notes 	Application/Control No. 12781826	Applicant(s)/Patent Under Reexamination TSENG ET AL.
	Examiner Phuc T Dang	Art Unit 2892

SEARCHED			
Class	Subclass	Date	Examiner
438	229,300	01/21/2011	PD
257	19,190,192,197,E21.437	01/21/2011	PD

SEARCH NOTES			
Search Notes		Date	Examiner
INVENTOR SEARCH		01/21/2011	PD
EAST SEARCH		01/21/2011	PD

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner

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EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	3	"20080006818"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/20 15:50
L2	3	1 and recess\$2	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/20 15:55
L3	3	2 and epitaxial	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/20 15:55
L4	0	"12786826"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/20 16:00
L5	1	"12781826"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/20 16:00
L6	1	5 and (epitaxial) with (spacer) with (above)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/20 16:00
L7	1	5 and (epitaxial) with (spacer)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/20 16:01

L8	258	(epitaxial) with (spacer) with (above)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/20 16:08
L9	210	8 and @ad<="20070809"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/20 16:08
L10	2969	(epitaxial) with (spacer)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/20 16:26
L11	973	10 and (recess\$2)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/20 16:26
L12	505	11 and (protect\$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/20 16:27
L13	361	12 and @ad<="20070809"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/20 16:27
L14	28	11 and (protective) with (silicon near nitride)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/20 17:25
L15	23	14 and @ad<="20070809"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/20 17:25

L16	22	"7381623" "7800182" "20070096194" "7745847"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/20 17:26
L17	18	16 and @ad<="20070809"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/20 17:27
L18	6	17 and ((silicon near nitride) (sin))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/20 17:27
L19	4	16 and isolation	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/20 17:39
L20	4	16 and sti	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/20 17:40
L21	2	16 and (thick\$4) with (protective)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/20 17:44
L22	72996	(thick\$4) with (protective)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/20 17:45
L23	61225	(thickness) with (protective)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/20 17:45

L24	252	23 and (method) with (mos near transistor)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/20 17:45
L25	208	24 and @ad<="20070809"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/20 17:46
L27	92	25 and ((ldd) (lightly-doped) (lightly near doped))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/20 17:47
L28	18	27 and recess\$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/20 17:47
L29	4	16 and ((ldd) (lightly-doped) (lightly near doped))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/20 17:50
L30	5	16 and (nmos pmos)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/20 17:59
L31	0	16 and (n-mos p-mos)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/20 17:59
L32	7	16 and (mos)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/20 17:59
L33	3	16 and (metal near oxide)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/20 17:59

L34	18	16 and @ad<="20070809"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/20 18:02
L35	0	34 and ldd	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/20 18:02
L36	0	34 and lightly-doped	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/20 18:02
L37	20503	(second near2 protective)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/20 18:07
L38	2	(second near protective) with (ldd)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/20 18:07
L39	127	((second adj1 (epi epitaxial)) with (recess\$2 cavit\$2))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/20 18:12
L40	0	39 and ((second) adj2 ((ldd) (lightly-doped)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/20 18:12
L41	3	39 and ((second) adj2 ((ldd) (lightly near doped)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/20 18:13
S1	1	"12383481"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/14 18:58

S2	1	"12382481"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/14 18:58
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1/ 20/ 2011 6:18:16 PM

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	12/781,826
	Filing Date	05/18/2010
	First Named Inventor	Chu-Yin Tseng
	Art Unit	~~N/A~~ 2892
	Examiner Name	~~N/A~~ P. Dang
	Attorney Docket Number	NAUP0913USA1

U.S.PATENTS						
Examiner Initial*	Cite No	Patent Number	Kind Code	Issue Date	Name	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
/PD/	1	6815770	B1	2004-11-09	Chien	
	2	6774000	B2	2004-08-10	Natzle	
	3	7195985	B2	2007-03-27	Murthy	
	4	6110787		2000-08-29	Chan	
↓ /PD/	5	6429084	B1	2002-08-06	Park	
U.S.PATENT APPLICATION PUBLICATIONS						
Examiner Initial*	Cite No	Publication Number	Kind Code	Publication Date	Name	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
/PD/	1	20070298558	A1	2007-12-27	YAMAUCHI	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	
	Filing Date	
	First Named Inventor	Chu-Yin Tseng
	Art Unit	N/A
	Examiner Name	N/A
	Attorney Docket Number	NAUP0913USA1

/PD/	2	20080006818	A1	2008-01-10	Luo	
↓	3	20080032468	A1	2008-02-07	Cheng	
	4	20060211245	A1	2006-09-21	Maszara	
	5	20080179636	A1	2008-07-31	Chidambarao	
/PD/	6	20050156154	A1	2005-07-21	Zhu	

FOREIGN PATENT DOCUMENTS

Examiner Initial*	Cite No	Foreign Document Number	Country Code	Kind Code	Publication Date	Name	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear	
	1							

NON-PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	
	1		

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	12/781,826
	Filing Date	05/18/2010
	First Named Inventor	Chu-Yin Tseng
	Art Unit	~~NA~~ 2892
	Examiner Name	~~NA~~ P. Dang
	Attorney Docket Number	NAUP0913USA1

EXAMINER SIGNATURE			
Examiner Signature	/Phuc Dang/	Date Considered	01/21/2011
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.			



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BIB DATA SHEET

CONFIRMATION NO. 3483

SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.		
12/781,826	05/18/2010	257	2892	NAUP0913USA1		
RULE						
APPLICANTS Chu-Yin Tseng, Tainan County, TAIWAN; Shih-Chieh Hsu, Hsinchu City, TAIWAN; Chih-Chiang Wu, Taichung County, TAIWAN; Shyh-Fann Ting, Tai-Nan City, TAIWAN; Po-Lun Cheng, Kao-Hsiung Hsien, TAIWAN; Hsuan-Hsu Chen, Tai-Nan City, TAIWAN;						
** CONTINUING DATA ***** This application is a DIV of 11/836,772 08/09/2007 PAT 7,745,847						
** FOREIGN APPLICATIONS *****						
** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** 05/27/2010						
Foreign Priority claimed ☐ Yes ☒ No 35 USC 119(a-d) conditions met ☐ Yes ☒ No Verified and Acknowledged <u>/PHUC T DANG/</u> Examiner's Signature		☐ Met after Allowance Initials	STATE OR COUNTRY TAIWAN	SHEETS DRAWINGS 14	TOTAL CLAIMS 21	INDEPENDENT CLAIMS 2
ADDRESS NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION P.O. BOX 506 MERRIFIELD, VA 22116 UNITED STATES						
TITLE Method of fabricating metal oxide semiconductor transistor						
FILING FEE RECEIVED 1142	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:			☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit		

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	12781826
	Filing Date	2010-05-18
	First Named Inventor	Chu-Yin Tseng
	Art Unit	2892
	Examiner Name	DANG, PHUC T
	Attorney Docket Number	NAUP0913USA1

U.S.PATENTS						
Examiner Initial*	Cite No	Patent Number	Kind Code	Issue Date	Name	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					
U.S.PATENT APPLICATION PUBLICATIONS						
Examiner Initial*	Cite No	Publication Number	Kind Code	Publication Date	Name	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20060138479	A1	2006-06-29	Ngo	
	2	20040142545	A1	2004-07-22	Ngo	
	3	20040232513	A1	2004-11-25	Chi	
	4	20060024879	A1	2006-02-02	Fu	
	5	20060134873	A1	2006-06-22	Koontz	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	12781826
	Filing Date	2010-05-18
	First Named Inventor	Chu-Yin Tseng
	Art Unit	2892
	Examiner Name	DANG, PHUC T
	Attorney Docket Number	NAUP0913USA1

	6	20060226483	A1	2006-10-12	Lo	
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FOREIGN PATENT DOCUMENTS

Examiner Initial*	Cite No	Foreign Document Number	Country Code	Kind Code	Publication Date	Name	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear	
	1	200509310	TW		2005-03-01			Abstract
	2	200636996	TW		2006-10-16			Abstract

NON-PATENT LITERATURE DOCUMENTS
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Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	
	1		

EXAMINER SIGNATURE

Examiner Signature		Date Considered	
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	12781826
	Filing Date	2010-05-18
	First Named Inventor	Chu-Yin Tseng
	Art Unit	2892
	Examiner Name	DANG, PHUC T
	Attorney Docket Number	NAUP0913USA1

CERTIFICATION STATEMENT			
Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):			
☒ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).			
OR			
☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).			
☒ See attached certification statement.			
☐ Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.			
☐ None			
SIGNATURE			
A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.			
Signature	/Scott Margo/	Date (YYYY-MM-DD)	2011-03-30
Name/Print	Scott Margo	Registration Number	56277

Abstract of TW 200509310

According to one exemplary embodiment, a FET which is situated over a substrate (104), comprises a channel (112) situated in the substrate (104). The FET further comprises a first gate dielectric (116) situated over the channel (112), where the first gate dielectric (116) has a first coefficient of thermal expansion. The FET further comprises a first gate electrode (114) situated over the first gate dielectric (116), where the first gate electrode (114) has a second coefficient of thermal expansion, and where the second coefficient of thermal expansion is different than the first coefficient of thermal expansion so as to cause an increase in carrier mobility in the FET. The second coefficient of thermal expansion may be greater than the first coefficient of thermal expansion, for example. The increase in carrier mobility may be caused by, for example, a tensile strain created in the channel (112).

200509310

發明專利說明書 200509310

(本說明書格式、順序及粗體字，請勿任意更動，※記號部分請勿填寫)

※ 申請案號：97124153

※ 申請日期：97.8.12

※IPC 分類：H01L 21/8232

一、發明名稱：(中文/英文)

具有增加之載子移動率的場效電晶體

FIELD EFFECT TRANSISTOR HAVING INCREASED CARRIER MOBILITY

二、申請人：(共 1 人)

姓名或名稱：(中文/英文)

高級微裝置公司

ADVANCED MICRO DEVICES, INC.

代表人：(中文/英文) 柯洛皮 丹尼爾 R / COLLOPY, DANIEL R.

住居所或營業所地址：(中文/英文)

美國·加州 94088-3453·桑尼威·第 1AMD 區·M/S 68·郵政信箱 3453 號
One AMD Place, M/S 68, P. O. Box 3453, Sunnyvale, CA 94088-3453,
U. S. A.

國 籍：(中文/英文) 美國 / U. S. A.

三、發明人：(共 3 人)

姓 名：(中文/英文)

1. 相奇 / XIANG, QI
2. 安文勇 / ANG, BOON-YONG
3. 丘政錫 / GOO, JUNG-SUK

國 籍：(中文/英文)

1. 中國大陸 / CHINA
2. 新加坡 / SINGAPORE
3. 韓國 / KOREA

四、聲明事項：

☐ 主張專利法第二十二條第二項 ☐ 第一款或 ☐ 第二款規定之事實，其事實發生日期為： 年 月 日。

☐ 申請前已向下列國家（地區）申請專利：

【格式請依：受理國家（地區）、申請日、申請案號 順序註記】

☒ 有主張專利法第二十七條第一項國際優先權：

1. 美國；2003 年 08 月 18 日；10/643,461（主張優先權）

☐ 無主張專利法第二十七條第一項國際優先權：

☐ 主張專利法第二十九條第一項國內優先權：

【格式請依：申請日、申請案號 順序註記】

☐ 主張專利法第三十條生物材料：

☐ 須寄存生物材料者：

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☐ 不須寄存生物材料者：

所屬技術領域中具有通常知識者易於獲得時，不須寄存。

五、中文發明摘要：

依據本發明之範例實施例，位於基板(104)上之場效電晶體(FET)含有位於該基板(104)中之通道(112)。該 FET 更進一步包含位於該通道(112)上之第一閘極介電質(116)，該第一閘極介電質(116)具有第一熱膨脹係數。該 FET 復包含位於該第一閘極介電質上之第一閘極電極層(114)，該第一閘極電極具有第二熱膨脹係數，此第二熱膨脹係數係不同於該第一熱膨脹係數，導致於該 FET 中載子移動率之增加。舉例來說，該第二熱膨脹係數可高於該第一熱膨脹係數；而該增加之載子移動率可由於該通道(112)中之拉伸應變所造成。

六、英文發明摘要：

According to one exemplary embodiment, a FET which is situated over a substrate (104), comprises a channel (112) situated in the substrate (104). The FET further comprises a first gate dielectric (116) situated over the channel (112), where the first gate dielectric (116) has a first coefficient of thermal expansion. The FET further comprises a first gate electrode (114) situated over the first gate dielectric (116), where the first gate electrode (114) has a second coefficient of thermal expansion, and where the second coefficient of thermal expansion is different than the first coefficient of thermal expansion so as to cause an increase in carrier mobility in the FET. The second coefficient of thermal expansion may be greater than the first coefficient of thermal expansion, for example. The increase in carrier mobility may be caused by, for example, a tensile strain created in the channel (112).

七、指定代表圖：

(一)本案指定代表圖為：第 (1) 圖。

(二)本代表圖之元件符號簡單說明：

100	構造	102	場效電晶體(FET)
104	基板	106	閘極堆疊
108	源極	110	汲極
112	通道	114	閘極電極層
116	閘極介電質	118	基板上表面

八、本案若有化學式時，請揭示最能顯示發明特徵的化學式：

九、發明說明：

【發明所屬之技術領域】

本發明係關於半導體裝置之領域。更詳言之，本發明係關於半導體場效電晶體(FETs)之製程領域。

【先前技術】

在積體電路(IC)的發展中，如超大型積體電路(VLSI)，一直都存在著追求更高的積體電路效能的需求。因此，半導體製造業面臨增加電晶體效能的挑戰，電晶體係指用於ICs中之N通道場效電晶體(NFETs)或P通道場效電晶體(PFETs)。

衡量場效電晶體(FETs)的重要指標之一為工作速度，工作速度與FET中之電流有關。典型的FET包含閘極堆疊，包含位於閘極介電質上之閘極電極、汲極、源極以及位於該源極和該汲極間且於矽基板中之通道。該通道同時位於基板(如：矽基板)上之該閘極介電質下。當施加高於臨限電壓之電壓於閘極介電質時，通道中將產生移動電荷載子層，該移動電荷載子如：NFET中的電子或PFET中的電洞。藉由施加電壓於該FET之汲極，使汲極和源極間產生電流之流動。

於上述對於FET之討論中，該載子移動率直接與流動於汲極和源極間的電流有關，且於本申請書中同時稱作FET電流而與FET之工作速度有關。除了別的因素外，載子移動率亦為溫度、由該閘極電壓於閘極介電值和通道間所造成之電場以及參雜濃度之函數。藉由增加載子移動

率，FET 電流以及必然的 FET 工作速度將可提升。因此增加載子移動率之結果使得 FET 效能可提升至預期之目標。

如此一來，就需要發展具有增加之載子移動率的 FET 之技術以完成提升 FET 效能之目標。

【發明內容】

本發明係針對具有增加之載子移動率的場效電晶體 (FETs)。本發明係滿足並解決於此項技藝中增加之載子移動率(carrier mobility)的 FET 之需求以達成提升 FET 效能之目標。

依據示範實施例之一，位於基板上之 FET 包含位於該基板中之通道。該 FET 更進一步包含位於該通道上之第一閘極介電質，該第一閘極介電質之熱膨脹係數稱為第一熱膨脹係數。該 FET 復包含位於該第一閘極介電質上之第一閘極電極，該第一閘極之熱膨脹係數稱為第二熱膨脹係數，且該第二熱膨脹係數係不同於該第一熱膨脹係數，造成於該 FET 中載子移動率的增加。舉例來說該第二熱膨脹係數可高於該第一熱膨脹係數；而該載子移動率的增加可由於該通道中所產生的拉伸應變所造成(tensile strain)。

根據此示範實施例，FET 可復包含位於第一閘極電介電質旁之“閘極襯層”(gate liner)，以及位於閘極襯層旁之“閘極間隔物”(gate spacer)，其中該閘極襯層具有第三熱膨脹係數，以及閘極間隔體具有第四熱膨脹係數，而第四熱膨脹係數大於第三熱膨脹係數，故於通道中造成拉伸

應變。

根據示範實施例之一，該 FET 可進一步包含位於該第一閘極介電質和該第一閘極間之第二閘極，該第二閘極具有第三熱膨脹係數，該第三熱膨脹係數係大於該第一熱膨脹係數但小於該第二熱膨脹係數，造成通道中產生拉伸應變而增加載子移動率。本發明之其他特徵與優點將於熟悉此領域之技術人員於檢閱於後伴隨圖式之詳述後更趨明顯。

【實施方式】

本發明係針對具有增加之載子移動率的場效電晶體 (FETs)。於後之敘述包含本發明實施之特定資訊。此領域中之技術人員將了解本發明可以不同於本申請書所揭示之方法完成。此外，為不使本發明模糊難懂某些本發明之特定細節將不多做贅論。

於本說明書之圖式中及所伴隨之詳細敘述係針對本發明之示範實施例。為求簡潔，本發明其他實施例於本申請書中將不特別敘述且不會於圖中揭示。

第 1 圖為依據本發明一實施例之示範之場效電晶體 (FET) 之構造剖面圖。構造 100 包含位於基板 104 上之 FET 102。FET 102 包含閘極堆疊 106，而閘極堆疊 106 包含了閘極電極層 114 以及閘極介電質層 116、源極 108、汲極 110 和通道 112。於本實施例中 FET 102 可為 N 型場效電晶體 (NFET) 或 P 型場效電晶體 (PFET)。

如第 1 圖所示，源極 108 和汲極 110 係以習知之技術

形成於基板 104 中，且通道 112 位於源極 108 和汲極 110 之間。於第 1 圖中更進一步揭示，閘極介電層 116 係覆蓋通道 112 位於基板 104 之上表面 118 上。舉例來說，閘極介電層 116 可具有 10.0 埃至 15.0 埃之間的厚度。亦顯示於第 1 圖中，閘極電極層 114 位於閘極介電層 116 之上。舉例來說，閘極電極層 114 之厚度可於 500.0 埃至 2000.0 埃之間。閘極電極層 114 可利用化學氣相沉積法 (CVD) 或其他適當之製程於高溫中沉積於閘極介電層 116 上。

於本實施例中，閘極電極層 114 和閘極介電層 116 係經過選擇，使得閘極電極層 114 具有高於閘極介電層 116 之熱膨脹係數 (coefficient of thermal expansion, CTE)。因此，當包含構造 100 之晶圓由沉積閘極電極層 114 之高溫冷卻之後，閘極電極層 114 之尺寸比閘極介電層 116 更縮小 (亦即收縮更多)。因此拉伸應變形成於通道 112 中而造成 FET 102 中之載子移動率增加。於實施例中，FET 102 為 PFET，且閘極介電層 116 和閘極電極層 114 係經過選擇使閘極介電層 116 有高於閘極電極層 114 之熱膨脹係數。於此實施例中，於通道 112 中產生壓縮應變而於該 PFET 中增加載子移動率。

第 2 圖為依據本發明實施例中含有示範之場效電晶體 (FET) 之構造剖面圖。構造 200 包含位於基板 204 上之 FET 202，FET 202 包含閘極堆疊 206，而閘極堆疊 206 包含閘極電極層 220 與 222 及閘極介電層 216、源極 208、汲極

210 以及通道 212。FET 202 可為 NFET 或 PFET，此點類似於 FET102。於第 2 圖中之構造 200，其基板 204、源極 208、汲極 210 以及通道 212 分別對應至構造 100 中之基板 104、源極 108、汲極 110 以及通道 112。

如第 2 圖所示，閘極介電質層 216 係覆蓋通道 212 位於基底 204 之上表面 218 上。舉例來說，閘極介電質層 216 之厚度可為 10.0 埃至 15.0 埃。第 2 圖中同時也顯示，閘極電極層 220 係位於閘極介電層 216 上，且可由如多晶矽或其他適當之材料所組成，舉例來說，閘極電極層 220 之厚度可為 100.0 埃至 500.0 埃間。於第 2 圖中復指出，閘極電極層 222 係位於閘極電極層 220 上，且可由如矽化物或其他適當材料組成。舉例來說，閘極電極層 220 之厚度可為 400.0 埃至 1500.0 埃。閘極電極層 222 可於高溫中以 CVD 或其他適當之製程沉積於閘極電極層 220 上。

於第 2 圖之本發明實施例中，閘極電極層 220 和 222 以及閘極介電質層 216 係經過選擇，使得該閘極電極層 222 擁有高於閘極電極層 220 之熱膨脹係數，且該閘極電極層 220 之該熱膨脹係數係高於該閘極介電質層 216。因此，當包含構造 200 之晶圓由沉積閘極電極層 222 之高溫冷卻之後，閘極電極層 222 之尺寸比閘極介電質層 216 更縮小，並且閘極電極層 220 比閘極介電層 216 縮得更小。因而於通道 212 中產生拉伸應變，使於 FET202 中之載子移動率增加。於實施例中，FET 202 可為 PFET，而閘極介電質層 216 以及閘極電極層 220 和 222 係經過選擇，使閘極介電質層

216 擁有高於閘極電極層 220 之熱膨脹係數，而閘極電極層 220 之熱膨脹係數高於閘極電極層 222。於此實施例中，通道 212 中產生壓縮應變，使得 PFET 中之載子移動率增加。

第 3 圖為依據本發明實施例中含有示範之場效電晶體 (FET) 之結構剖面圖。結構 300 係包含位於基板 304 上之 FET 302。FET 302 包含閘極堆疊 306，閘極堆疊 306 包含閘極電極層 314 和閘極介電質層 316 和 324、源極 308、汲極 110 以及通道 312。FET 302 可為 NFET 或 PFET，此點類似於 FET 102。於第三圖中之構造 300，基板 304、源極 308、汲極 310 以及通道 312 分別對應於構造 100 中之基板 104、源極 108、汲極 110 以及通道 112。

如第 3 圖中所示，閘極介電質層 316 係覆蓋通道 312 位於基板 304 之上表面 318 上，且可由二氧化矽或其他適當之介電質層組成。於第 3 圖中同時顯示，閘極介電質層 324 係位於閘極介電質層 316 上且可由氮化矽或其他適當之介電質層組成。第 3 圖中進一步顯示，閘極電極層 314 位於閘極介電質層 324 上，閘極電極層 314 可於高溫中以 CVD 或其他適當之製程沉積於閘極介電質層 324 上。

於本實施例中，閘極電極層 314 以及閘極介電質層 316 和 324 係經過選擇，使得閘極電極層 314 擁有高於閘極介電質層 324 之熱膨脹係數，而閘極介電質層 324 之熱膨脹係數係高於閘極介電質層 316 之熱膨脹係數。因此，當含有構造 300 之晶圓由沉積閘極電極層 314 之高溫冷卻之

後，閘極電極層 314 之尺寸比閘極介電質層 324 更縮小，且閘極介電質層 324 比閘極介電質層 316 更縮小。因而於通道 312 中產生拉伸應變造成 FET 302 中之載子移動率增加。於實施例中，FET 302 為 PFET，而閘極介電質層 316 和 324 以及閘極電極層 314 皆經過選擇，使閘極介電質層 316 具有高於閘極介電質層 324 之熱膨脹係數，且閘極介電質層 324 之熱膨脹係數係高於閘極電極層 314 之熱膨脹係數，於此實施例中，於通道 312 中產生壓縮應變而使 PFET 中之載子移動率增加。

第 4 圖為依據本發明實施例中含有示範之場效電晶體 (FET) 之結構剖面圖。構造 400 包含位於基板 404 上之 FET 402。FET 402 包含閘極堆疊 406、源極 408、汲極 410、通道 412、“閘極襯層”426、428 以及“閘極間隔物”430、432。FET 402 可為 NFET 或 PFET，此點與 FET 102 相似。於第 4 圖中之構造 400，其基板 404、源極 408、汲極 410 以及通道 412 分別對應至構造 100 中之基板 104、源極 108、汲極 110 以及通道 112。

如第 4 圖所示，閘極堆疊 406 係位於基板 404 上。閘極堆疊 406 可為第 1 圖中之閘極堆疊 106、第 2 圖中之閘極堆疊 206 或第 3 圖中之閘極堆疊 306。於第 4 圖中更進一步顯示，閘極襯層 426 和 428 係位於基板 404 上方個別緊鄰於閘極堆疊 406。舉例來說，閘極襯層 426 和 428 之厚度可為 50.0 埃至 200.0 埃。第 4 圖中同時顯示，閘極間隔物 430 與 432 係個別緊鄰於閘極堆疊 426 與 428。因此，

閘極襯層 426 與 428 係個別位於閘極間隔物 430 與 432 間且位於閘極堆疊 406 旁，並也同時位於個別對應之閘極間隔物 430 及 432 與基板 404 之間。

於本實施例中，閘極襯層 426 與 428 以及閘極間隔物 430 與 432 係經過選擇，使得閘極間隔物 430 與 432 有個別高於對應之閘極襯層 426 與 428 的個別熱膨脹係數。因此，如前述之原因，於通道 412 中產生拉伸應變使得 FET 402 中之載子移動率增加。於實施例中，FET 302 係為 PFET，而閘極襯層 426 和 428 以及閘極間隔物 430 與 432 係經過選擇，使得閘極襯層 426 與 428 有個別高於閘極間隔物 430 與 432 之個別熱膨脹率。因此，於通道 412 中產生了壓縮應變使該 PFET 中之載子移動率增加。

如上之討論，本發明係藉由選擇閘極堆疊之閘極和介電質層，使之具有適當之個別熱膨脹係數，而達成於 FET 之通道中增加拉伸應變，FET 亦即 FET 102, 202, 302 或 402。因此，本發明有助於達成於 FET 中增加載子移動率，而提升 FET 之效能。此外，本發明藉選擇閘極和閘極堆疊之介電質層，使之個別具有適當之熱膨脹係數，而達成於 PFET 之通道中增加壓縮應變，導致載子移動率之增加，進而提升 FET 之效能。

上述之本發明實施例可於不悖離其發明領域下以各種技術完成。此外，於此領域之技術人員應了解到對於本發明實施例之敘述可於不悖離本發明精神與範疇下完成其細節。且實施例之敘述係為示範而非意於限制之用。在此也

必須了解本發明並限於特定之示範實施例而是涵括於本發明範疇下所有的修飾與變更。

具有增加之載子移動率的場效電晶體已如上之敘述。

【圖式簡單說明】

第 1 圖為依據本發明實施例中含有示範之場效電晶體 (FET) 之構造剖面圖。

第 2 圖為依據本發明實施例中含有示範之場效電晶體 (FET) 之構造剖面圖。

第 3 圖為依據本發明實施例中含有示範之場效電晶體 (FET) 之構造剖面圖。

第 4 圖為依據本發明實施例中含有示範之場效電晶體 (FET) 之構造剖面圖。

【主要元件符號說明】

100、200、300、400	構造
102、202、302、402	場效電晶體 (FET)
104、204、304、404	基板
106、206、306、406	閘極堆疊
108、208、308、408	源極
110、210、310、410	汲極
112、212、312、412	通道
114、314 閘極電極層	116 閘極介電質
118、218、318 基板上表面	220、222 閘極電極層
216、316 閘極介電質層	426、428 閘極襯層
430、432 閘極間隔物	

十、申請專利範圍：

1. 一種位於基板(104)上之場效電晶體(FET)，該 FET 包含：

通道(112)，係位於該基板(104)中；

第一閘極介電質(116)，係位於該通道(112)上方，
該第一閘極介電質(116)具有第一熱膨脹係數；

第一閘極電極層(114)，係位於該第一閘極介電質(116)上方，該第一閘極電極層(114)具有第二熱膨脹係數；

其中該第二熱膨脹係數係不同於該第一熱膨脹係數，使該 FET 中產生載子移動率之增加。

2. 如申請專利範圍第 1 項之 FET，其中，該第二熱膨脹係數大於該第一熱膨脹係數。
3. 如申請專利範圍第 2 項之 FET，其中，該增加之載子移動率係由該通道(112)之拉伸應變所造成。
4. 一種 FET 位於基板(104)上，該 FET 包含：位於該基板(104)中之通道(112)、位於該通道(112)上方之第一閘極介電質(116)且該第一閘極介電質(116)具有第一熱膨脹係數、位於該第一閘極介電質(116)上之第一閘極電極層(114)且該第一閘極電極層(114)具有第二熱膨脹係數，該 FET 之特徵為：

該第二熱膨脹係數係不同於該第一熱膨脹係數，致使該 FET 中載子移動率之增加。

5. 如申請專利範圍第 4 項之 FET，其中該第二熱膨脹係數

係高於該第一熱膨脹係數，造成在該通道(112)中產生拉伸應變，而該拉伸應變引起該載子移動率之增加。

6. 如申請專利範圍第 4 項之 FET，更進一步包含位於該第一閘極電極層(222)與該第一閘極介電質(216)間之第二閘極電極層(220)，該第二閘極電極層(220)具有第三熱膨脹係數，該第三熱膨脹係數係大於該第一熱膨脹係數但小於該第二熱膨脹係數，於該通道(212)中產生拉伸應變，而該拉伸應變造成該載子移動率之增加。
7. 如申請專利範圍第 4 項之 FET，更進一步包含位於該第一閘極介電質(316)與該基板(304)間之第二閘極介電質(324)，該第二閘極介電質(324)具有第三熱膨脹係數，該第三熱膨脹係數低於該第一熱膨脹係數，而該第二熱膨脹係數高於該第一熱膨脹係數，使該通道(312)中產生拉伸應變，而該拉伸應變造成該載子移動率之增加。
8. 如申請專利範圍第 4 項之 FET，其中，該 FET 為 PFET，該第一熱膨脹係數係高於該第二熱膨脹係數，使該通道(112)中產生壓縮應變，而該壓縮應變造成該載子移動率之增加。
9. 如申請專利範圍第 4 項之 FET，更進一步包含：緊鄰於該第一閘極介電質(116)之閘極襯層(426、428)、緊鄰於該閘極襯層(426、428)之閘極間隔物(430、432)，該閘極襯層(426、428)具有第四熱膨脹係數，該第四熱膨脹係數係高於該第三熱膨脹係數，使通道(412)中產生

拉伸應變。

10. 一種 FET 位於基板(104)上, 該 FET 包含:

通道(112), 係位於該基板(104)中;

閘極堆疊(106), 係位於該通道(112)上;

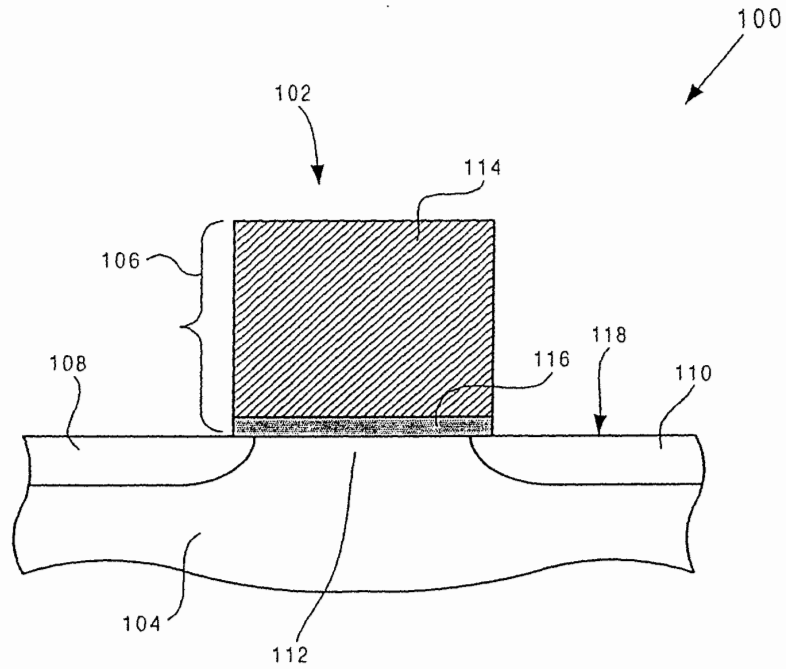
第一閘極介電質(116)係位於該閘極堆疊(106)上, 該第一閘極介電質(116)具有第一熱膨脹係數;

第一閘極電極層(114)係位於該第一閘極介電質(116)上方, 該第一閘極電極層(114)具有第二熱膨脹係數;

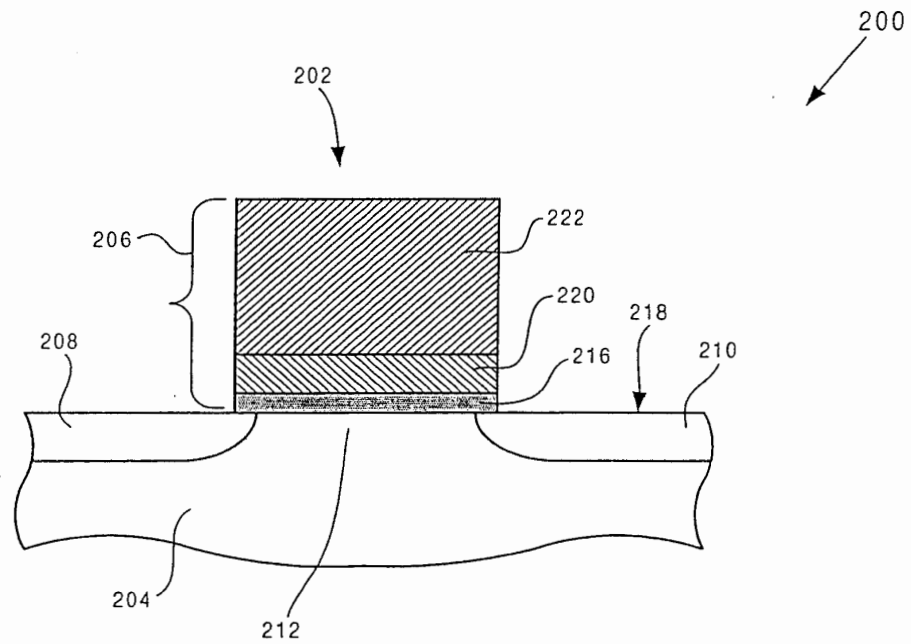
其中, 該第二熱膨脹係數係不同於該第一熱膨脹係數, 使通道(112)中產生應變, 而該應變於該 FET 中造成載子移動率之增加。

9/21/24/15

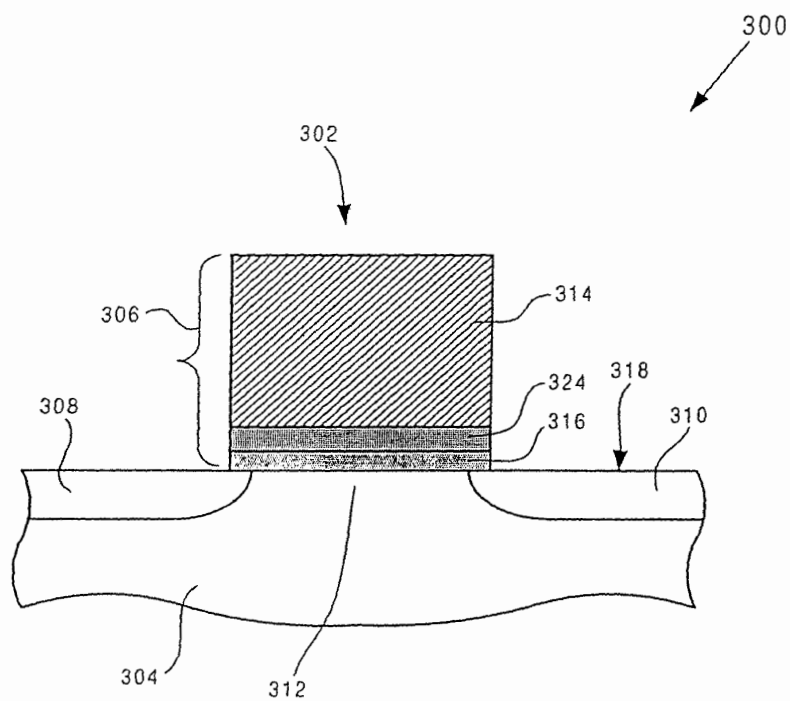
1/4



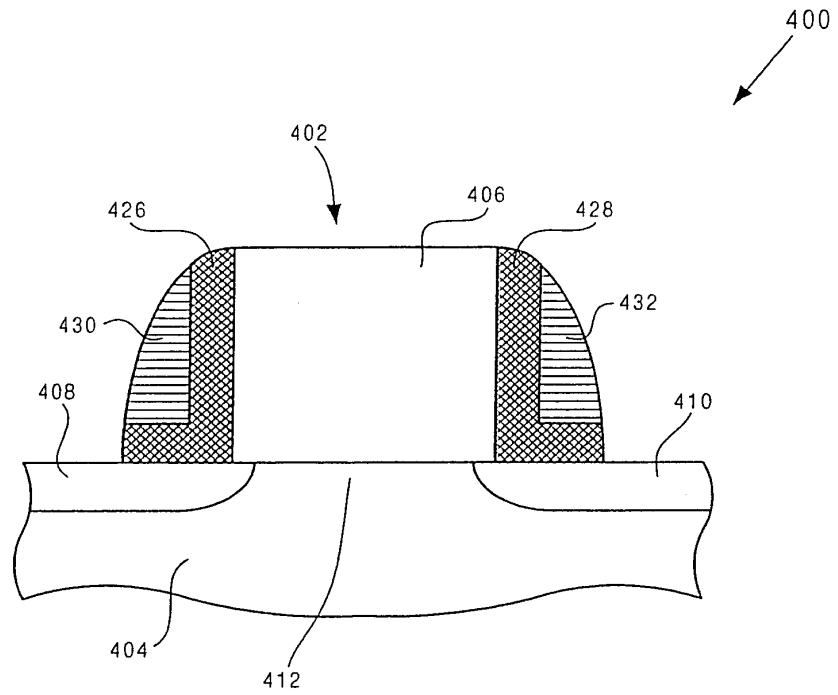
第 1 圖



第 2 圖



第 3 圖



第 4 圖

Abstract of TW 200636996

STRUCTURE AND METHOD FOR MANUFACTURING STRAINED FINFET

ABSTRACT OF THE DISCLOSURE

A part of the gate of a FINFET is replaced with a stress material to apply stress to the channel of the FINFET to enhance electron and hole mobility and improve performance. The FINFET has a SiGe/Si stacked gate, and before silicidation the SiGe part of the gate is selectively etched to form a gate gap that makes the gate thin enough to be fully silicidated. After silicidation, the gate-gap is filled with a stress nitride film to create stress in the channel and enhance the performance of the FINFET.

發明專利說明書

200636996

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一、發明名稱：(中文/英文)

應變過的鰭式場效電晶體之製造方法及結構

STRUCTURE AND METHOD FOR MANUFACTURING STRAINED
FINFET

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2. 美國 U.S.A.

四、聲明事項：

☐ 主張專利法第二十二條第二項 ☐ 第一款或 ☐ 第二款規定之事實，其事實發生日期為： 年 月 日。

☒ 申請前已向下列國家（地區）申請專利：

【格式請依：受理國家（地區）、申請日、申請案號 順序註記】

☒ 有主張專利法第二十七條第一項國際優先權：

1. 美國；2005年02月15日；10/906,335

2.

☐ 無主張專利法第二十七條第一項國際優先權：

1.

2.

☐ 主張專利法第二十九條第一項國內優先權：

【格式請依：申請日、申請案號 順序註記】

☐ 主張專利法第三十條生物材料：

☐ 須寄存生物材料者：

國內生物材料 【格式請依：寄存機構、日期、號碼 順序註記】

國外生物材料 【格式請依：寄存國家、機構、日期、號碼 順序註記】

☐ 不須寄存生物材料者：

所屬技術領域中具有通常知識者易於獲得時，不須寄存。

五、中文發明摘要：

本發明揭示一種應變過的鰭式場效電晶體之製造方法及結構。以一應力材料取代一FINFET(鰭式場效電晶體)之閘極之一部分以便對該FINFET之通道施加應力，從而提高電子及電洞移動率且改進效能。該FINFET具有一SiGe/Si層疊閘極，且在矽化之前，該閘極之該SiGe部分經選擇性地蝕刻以形成一使該閘極足夠薄以便完全矽化的閘極間隙。在矽化之後，該閘極間隙以一應力氮化物薄膜填充，從而在通道中產生應力且提高該FINFET之效能。

六、英文發明摘要：

200636996

95104784

108409

18156.WCR

STRUCTURE AND METHOD FOR MANUFACTURING STRAINED FINFET

ABSTRACT OF THE DISCLOSURE

A part of the gate of a FINFET is replaced with a stress material to apply stress to the channel of the FINFET to enhance electron and hole mobility and improve performance. The FINFET has a SiGe/Si stacked gate, and before silicidation the SiGe part of the gate is selectively etched to form a gate gap that makes the gate thin enough to be fully silicidated. After silicidation, the gate-gap is filled with a stress nitride film to create stress in the channel and enhance the performance of the FINFET.

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七、指定代表圖：

(一)本案指定代表圖為：第（ 5 ）圖。

(二)本代表圖之元件符號簡單說明：

- | | |
|----|-------------------|
| 16 | 內埋氧化物 (BOX) |
| 18 | 硬式光罩氮化物層 |
| 22 | Si 緒狀物 |
| 24 | 閘極氧化物 |
| 26 | 聚 Si 層 / 聚 Si |
| 28 | 聚 SiGe 層 / 聚 SiGe |

八、本案若有化學式時，請揭示最能顯示發明特徵的化學式：

(無)

九、發明說明：

【發明所屬之技術領域】

本發明大體而言係關於一種稱為鰭式場效電晶體(FINFET)之具有一用於通道之非常薄之垂直矽層(鰭狀物)之應變過的雙閘極金屬氧化物半導體場效電晶體(MOSFET)的結構，且本發明大體而言係關於一種用於製造應變過的FINFET之方法，該方法以應力材料取代FINFET之閘極之一部分以便對該FINFET之通道施加應力。該應力提高電子及電洞移動率且改進FINFET之效能。更特定而言，以應力氮化物薄膜取代FINFET之SiGe/Si層疊閘極之SiGe部分以便對該FINFET之通道施加應力。

【先前技術】

在過去之約25年中，超大型積體電路(VLSI)之主要挑戰為愈來愈多之具有高產率及可靠性之金屬氧化物半導體場效電晶體(MOSFET)裝置的整合。在先前技術中此主要藉由在無過度之短通道效應的情況下按比例縮小MOSFET通道長度而達成。熟習此項技術者鹹知，短通道效應是短通道裝置中之臨限電壓 V_t 歸因於閘極與源極/汲極擴散區之間之二維靜電荷之共用而降低。

為了在無過度之短通道效應的情況下按比例縮小MOSFET通道長度，必須在增大通道摻雜濃度的同時減小閘極氧化物厚度。然而，IEEE Trans. Elect. Dev.之1992年7月第39卷第1704頁之Yan等人之"Scaling the Si MOSFET:

From bulk to SOI to bulk"已展示為了減小低於 $0.05\ \mu\text{m}$ 之MOSFET的短通道效應，在結構中具有一能將汲極場與通道屏蔽之背面導電層是重要的。Yan等人之結果展示雙閘極MOSFET及具有頂部閘極與背面接地平面之MOSFET愈加不受短通道效應之影響且因此能按比例縮小至比習知之MOSFET更短之尺寸。

典型之先前技術之雙閘極MOSFET之結構由用於通道之非常薄的垂直Si層(鰭狀物)及兩個閘極(每一個在該通道之每一側上)組成。本文使用術語"鰭狀物"指示用作場效電晶體(FET)之主體的半導體材料。電連接兩個閘極以使得其用於調變通道。因為兩個閘極十分有效地終止汲極場線以防止汲極電位在通道之源極端處得以感應，所以在此結構中之短通道效應得以大大地抑制。隨後，先前技術之雙閘極MOSFET之臨限電壓隨汲極電壓及閘極長度的變化比相同通道長度之習知之單閘極結構之臨限電壓的變化小得多。

對於FinFET CMOS(互補金屬氧化物半導體)之應用而言，提供具有對裝置主體而言之可能之最薄的單晶矽鰭狀物的結構是有益的。然而，此使得源極與汲極區之接觸相當困難。最優地，鰭狀物之裝置部分相當薄，而源極及汲極區較厚，從而有助於矽化物生長及金屬接觸方案。

在此技術之當前狀態中已知應力可提高FINFET之通道中之電子及電洞移動率，但在FINFET之通道中施加大應力較難。沿通道之壓縮縱向應力增大p型場效電晶體

(pFET)中之驅動電流且降低n型場效電晶體(nFET)中之驅動電流。若拉伸強度約1.0 Gpa或小於1.0 Gpa，則沿通道之拉伸縱向應力增大n型場效電晶體中之驅動電流且降低p型場效電晶體中之驅動電流。

【發明內容】

本發明提供一種應變過的FINFET之結構及一種製造應變過的FINFET之方法，該方法以應力材料取代閘極之一部分以便對FINFET之通道施加應力，從而提高電子及電洞移動率且改進FINFET之效能。FINFET具有一SiGe/Si層疊閘極，且在矽化之前，閘極之SiGe部分經選擇性地蝕刻以形成使閘極足夠薄以便完全矽化的閘極間隙。在矽化之後，以應力氮化物薄膜填充閘極間隙。此可在通道中產生應力且提高FINFET之效能。

【實施方式】

應力可提高電子及電洞移動率，但在FINFET裝置之通道中施加大應力較難。本發明以應力材料取代FINFET之閘極之一部分以便對FINFET之通道施加應力，從而提高電子及電洞移動率且改進FINFET之效能。更特定而言，本發明以應力氮化物薄膜取代FINFET之SiGe/Si層疊閘極之SiGe部分以便對FINFET之通道施加應力，從而提高電子及電洞移動率且改進FINFET之效能。

一般而言，本發明使用SiGe/Si層疊閘極取代聚Si閘極。在矽化之前，選擇性地蝕刻閘極之SiGe部分以使得閘極足夠薄以便完全矽化。在矽化且蝕刻殘餘金屬後，以應力氮

化物薄膜再填充該閘極間隙。此可在通道中產生應力且提高 FINFET 之效能。其他製程步驟可與用於製造習知之 FINFET 之步驟完全相同。

下述步驟大體對應於圖 1 至 15 中之說明。

起初，如圖 1 所示，以 BOX(內埋氧化物)16 上之 SOI 10(氧化物絕緣體 14 上之矽 12)晶圓(SOI 厚度約 50-100 nm)開始。基板較佳為 SOI，但並不限於 SOI 且可包括任何半導體材料，諸如 GaAs、InAs 及其他類似半導體。含 Si 之材料包括(但不限於)Si、塊體 Si、單晶 Si、多晶 Si、SiGe、非晶 Si、絕緣體上矽(SOI)、絕緣體上 SiGe(SGOI)、應變過的絕緣體上矽、退火過的之聚 Si 及聚 Si 線結構。

當基板 10 為絕緣體上矽(SOI)或絕緣體上 SiGe(SGOI)基板時，在內埋絕緣層頂上之含 Si 層之厚度可為約 10 nm 或更厚。絕緣體或介電質可為氧化物、氮化物或氮氧化物。SOI 或 SGOI 基板可使用熟習此項技術者所熟知之技術製造。例如，SOI 或 SGOI 基板可使用熱結合製程或替代地藉由離子植入製程(在此項技術中指氧離子植入分離法(SIMOX))而製造。

在基板頂部形成之閘極介電層較佳為氧化物或氮化物材料，且通常厚於 0.8 nm，且較佳自約 1.0 nm 至約 6.0 nm 厚。閘極介電層亦可包含氮氧化物或此等材料之組合。閘極介電質層使用習知技術形成，諸如化學氣相沈積(CVD)、原子層 CVD(ALCVD)、脈衝 CVD、電漿輔助 CVD、噴濺及化學溶液沈積，或者藉由包括氧化、氮氧化、氮化

及/或電漿或原子團處理之熱生長製程形成閘極介電層。可用作閘極介電質之氧化物的實例包括(但不限於) SiO_2 、 Al_2O_3 、 ZrO_2 、 HfO_2 、 Ta_2O_3 、 TiO_2 、鈣鈦礦型氧化物及其之組合及多層。閘極介電層隨後經蝕刻以形成閘極介電質。

遵循習知步驟製造Si鰭狀物。如圖2所示，沈積一硬式光罩氮化物層18(約20-40 nm)且圖案化光阻劑(PR)20。如圖3所示，反應性離子蝕刻(RIE)氮化物18、RIE SOI 10且在BOX 16上停止、記時RIE氧化物/BOX以達成約20-40 nm之蝕刻深度(使得越過Si鰭狀物施加更均一之應力，蝕刻至BOX)且移除PR 20。

該結構係利用熟習此項技術者所熟知之習知製程製造。舉例而言，硬式光罩18藉由使用諸如化學氣相沈積(CVD)、電漿輔助CVD或化學溶液沈積之習知沈積製程而形成於半導體材料層10之頂部。或者，硬式光罩可利用其後接有氮化製程之習知熱氧化製程而生長於半導體主體上。此等兩種熱製程(意即氧化及氮化)為熟習此項技術者所熟知的。本發明亦涵蓋經由沈積形成一硬式光罩材料層且經由熱氧化/氮化製程形成另一材料層。

接著，如圖2A-2B所示，使用習知微影術及蝕刻圖案化氮化物層18。特別地，微影製程包括塗覆光阻劑至氮化物層，曝露光阻劑於一幅射圖案且利用習知之光阻劑顯影機顯影圖案至光阻劑內。在光阻劑圖案化後，利用與移除氧化物相比對移除氮化物具有高度選擇性之蝕刻製程移除未

藉由圖案化之光阻劑保護之氮化物層的曝露部分。

可用於形成圖案化之氮化物層之適合蝕刻類型包括(但不限於): 反應性離子蝕刻、離子束蝕刻、電漿蝕刻或雷射剝蝕。在此蝕刻步驟之後, 可自該結構移除光阻。

然後, 如圖4所示, 熱氧化Si鍍狀物22以在Si鍍狀物之側壁上形成閘極氧化物24。在替代性實施例中, 藉由使用氮化物及氮氧化物, 其他形式之側壁保護為可用的。

接著, 如圖5所示, 沈積聚Si層26(約20-30 nm)及隨後之聚SiGe層28(約80-100 nm)。聚Si 26亦可為本文所說明之半導體或Si的其他形式。同樣, 聚SiGe層28亦可為半導體的其他形式(諸如Ge)。重要的是, 該等兩種材料在結合圖12所示之隨後蝕刻步驟中之蝕刻相異。

接著, 如俯視圖圖6及沿圖6中之箭頭A-A所剖開之側面剖視圖圖6A所示, 圖案化PR 30以用於閘極RIE。接著, 如俯視圖圖7、沿圖7中之箭頭A-A所剖開之側面剖視圖圖7A及沿圖7中之箭頭B-B所剖開之側面剖視圖7B所示, RIE聚SiGe 28且RIE聚Si 26以形成閘極, 且移除PR 30。

然後, 如俯視圖圖8所示, 熱再氧化以形成薄氧化物32, 從而保護閘極側壁及/或作為隔片用於擴展植入。在替代性實施例中, 以氮化物及氮氧化物之其他保護形式為可用的。然而, 熱再氧化因使轉角變圓而為較佳的。

接著, 如沿(如圖8中之)箭頭B-B所剖開之側面剖視圖圖9所示, 進行角形摻雜劑植入34以用於擴展形成。如圖8中之鹵基離子/植入(鹵基I/I)箭頭所指示之, 若需要, 則可

執行鹵基植入。所有植入步驟與用於習知 FINFET 製造之步驟相同。

然後，如俯視圖圖 10 及沿圖 10 中之箭頭 A-A 所剖開之側面剖視圖圖 10A、沿圖 10 中之箭頭 B-B 所剖開之側面剖視圖圖 10B、沿圖 10 中之箭頭 C-C 所剖開之側面剖視圖圖 10C(亦展示 L 閘極)及沿圖 10 中之箭頭 D-D 所剖開之側面剖視圖圖 10D 所示，沈積氮化物(30-50 nm)且 RIE 該氮化物以在閘極側壁上形成氮化物隔片 36。此製程亦與用於形成 FINFET 隔片之習知步驟相同。

接著，進行 SD(源極汲極)摻雜劑植入 38 及 SD 退火。如沿(如圖 10 中之)箭頭 A-A 所剖開之側面剖視圖圖 11A 及沿(如圖 10 中之)箭頭 D-D 所剖開之側面剖視圖圖 11D 所示，SD 摻雜劑植入 38 摻雜 SD 區域及閘極，且可用於調節 FINFET 裝置之臨限電壓以便完全矽化 FINFET 之閘極。執行習知植入製程以使得在該結構中與鰭狀物 22 鄰近之區域內形成源極/汲極植入區。此處之摻雜可為 n 型或 p 型。在本發明之一實施例中，使用不同之植入物質(諸如 As 及 B)摻雜與 Fin 22 相鄰之曝露區域，以使得分別形成具有施體或受體雜質之源極/汲極區。

然後，如俯視圖圖 12、沿圖 12 中之箭頭 A-A 所剖開之側面剖視圖圖 12A 及沿圖 12 中之箭頭 C-C 所剖開之側面剖視圖圖 12C 所示，選擇地乾式蝕刻(電漿)聚 SiGe 28 至 Si 26，其中圖 12C 展示移除閘極之 SiGe 部分以使得在聚 Si 上方形成一間隙 40 且以使得閘極足夠薄以便完全矽化。在該種狀

況下，閘極之SiGe部分經蝕刻去除以形成間隙且閘極變得更薄，以此方式增大閘極之電阻。稍後之矽化製程降低閘極之電阻至一較可接受之水平。

然後，如俯視圖圖13、沿圖13中之箭頭A-A所剖開之側面剖視圖圖13A及沿圖13中之箭頭C-C所剖開之側面剖視圖圖13C所示，遵循習知方法以製造矽化物接觸。首先，在SD區域中濕式蝕刻薄氧化物。然後，沈積薄金屬薄膜（較佳為4-10 nmNi）且退火（在300-450℃下）以形成NiSi₄₂。然後，濕式蝕刻殘餘金屬。在矽化製程期間，聚Si轉化為NiSi₄₂。

接著，如俯視圖圖14、沿圖14中之箭頭A-A所剖開之側面剖視圖圖14A及沿圖14中之箭頭C-C所剖開之側面剖視圖圖14C所示，沈積一應力氮化物薄膜44以填充閘極之間隙。較佳地，對於nFINFET而言沈積可壓縮氮化物薄膜而對於pFINFET而言沈積可拉伸氮化物薄膜。如此項技術中所熟知之，可藉由改變電漿沈積之功率而選擇性地沈積可壓縮氮化物薄膜或可拉伸氮化物薄膜。雖然在本發明中可使用諸如金屬（諸如鎢）之其他應力材料替代氮化物薄膜，但氮化物薄膜在一致性上具有優勢。

本發明之應力誘發薄膜可包含氮化物，較佳為Si₃N₄或替代地為TiN、氧化物、Al₂O₃、HfO₂、ZrO₂、HfSiO及半導體製程共用之其他介電質材料或其之任何組合。應力誘發薄膜可具有自約10 nm至約100 nm範圍內之厚度。應力誘發薄膜可提供裝置通道中之可壓縮應力以改進pFET之效

能或提供裝置通道中之可拉伸應力以改進nFET之效能。

然後，如俯視圖圖15、沿圖15中之箭頭A-A所剖開之側面剖視圖圖15A及沿圖15中之箭頭C-C所剖開之側面剖視圖圖15C所示，各向同性地回蝕應力氮化物薄膜。通道中之自閘極中及SD區域中之應力薄膜的應力可相互消除/降低。因為SD區域中之應力薄膜得以移除，所以此氮化物撤離之步驟提高通道中之應力。在此步驟之後，遵循習知製程以完成該裝置。

另一選擇為使用另一應力氮化物薄膜覆蓋整個裝置以進一步對通道施加應力。此時較佳對於nFINFET而言使用可拉伸薄膜而對於pFINFET而言使用可壓縮薄膜。

雖然本文詳細描述本發明之結構的若干實施例及變化及應變過的FINFET的製造方法，但應顯而易見本發明之揭示內容及教示將向熟習此項技術者暗示許多替代設計。

【圖式簡單說明】

圖1說明在內埋氧化物(BOX)上之絕緣體上矽(SOI)晶圓。

圖2展示製造Si鰭狀物之習知步驟。

圖3說明形成於BOX上之Si鰭狀物。

圖4說明熱氧化以形成在Si鰭狀物之側壁上的閘極氧化物。

圖5展示沈積聚Si層及隨後之聚SiGe層。

圖6及6A說明如俯視圖圖6及沿圖6中之箭頭A-A所剖開之側面剖視圖圖6A所示之圖案化光阻劑(PR)以用於閘極反

應性離子蝕刻(RIE)。

圖 7、7A 及 7B 說明如俯視圖圖 7、沿圖 7 中之箭頭 A-A 所剖開之側面剖視圖圖 7A 及沿圖 7 中之箭頭 B-B 所剖開之側面剖視圖圖 7B 所示之 RIE 聚 SiGe 且 RIE 聚 Si 以形成閘極。

圖 8 為展示熱再氧化以形成薄氧化物以便保護閘極側壁及/或作為隔片用於擴展植入的俯視圖。

圖 9 為沿(如圖 8 中之)箭頭 B-B 所剖開之側面剖視圖，其說明植入角形摻雜劑以用於擴展形成。

圖 10、10A、10B、10C 及 10D 說明如俯視圖圖 10、沿圖 10 中之箭頭 A-A 所剖開之側面剖視圖圖 10A、沿圖 10 中之箭頭 B-B 所剖開之側面剖視圖圖 10B、沿圖 10 中之箭頭 C-C 所剖開之側面剖視圖圖 10C 及沿圖 10 中之箭頭 D-D 所剖開之側面剖視圖圖 10D 所示之沈積氮化物且 RIE 該氮化物以在閘極側壁上形成氮化物隔片。

圖 11A 及圖 11D 說明如沿(如圖 10 中之)箭頭 A-A 所剖開之側面剖視圖圖 11A 及沿(如圖 10 中之)箭頭 D-D 所剖開之側面剖視圖圖 11D 所示之植入 SD(源極汲極)且退火。

圖 12、12A 及 12C 說明如俯視圖圖 12、沿圖 12 中之箭頭 A-A 所剖開之側面剖視圖圖 12A 及沿圖 12 中之箭頭 C-C 所剖開之側面剖視圖圖 12C 所示之選擇性地蝕刻聚 SiGe 至 Si。

圖 13、13A 及 13C 說明如俯視圖圖 13、沿圖 13 中之箭頭 A-A 所剖開之側面剖視圖圖 13A 及沿圖 13 中之箭頭 C-C 所剖開之側面剖視圖圖 13C 所示之形成矽化物接觸之習知方法。

圖 14、14A 及 14C 說明如俯視圖圖 14、沿圖 14 中之箭頭 A-A 所剖開之側面剖視圖圖 14A 及沿圖 14 中之箭頭 C-C 所剖開之側面剖視圖圖 14C 所示之沈積應力氮化物薄膜以填充閘極之間隙。

圖 15、15A 及 15C 說明如俯視圖圖 15、沿圖 15 中之箭頭 A-A 所剖開之側面剖視圖圖 15A 及沿圖 15 中之箭頭 C-C 所剖開之側面剖視圖圖 15C 所示之各向同性地回蝕應力氮化物薄膜。

【主要元件符號說明】

- | | |
|----|----------------------|
| 10 | 半導體材料層 / SOI / 基板 |
| 12 | 矽 |
| 14 | 氧化物絕緣體 |
| 16 | 內埋氧化物 (BOX) |
| 18 | 硬式光罩氮化物層 |
| 20 | 光阻劑 (PR) |
| 22 | Si 鰭狀物 |
| 24 | 閘極氧化物 |
| 26 | 聚 Si 層 / 聚 Si |
| 28 | 聚 SiGe 層 / 聚 SiGe |
| 30 | 光阻劑 (PR) |
| 32 | 薄氧化物 |
| 34 | 角形摻雜劑植入 |
| 36 | 氮化物隔片 |
| 38 | 源極汲極摻雜劑植入 / SD 摻雜劑植入 |

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40	間 隙
42	NiSi
44	應 力 氮 化 物 薄 膜

十、申請專利範圍：

1. 一種鰭式場效電晶體(FINFET)，其具有施加至該FINFET之通道上之應力以提高電子及電洞移動率，從而改進效能，該FINFET包含：
一源極、一汲極及一閘極；及
該閘極包含一層疊閘極，其中該閘極之一部分經選擇性地蝕刻以形成一以一應力薄膜再填充之閘極間隙以使得在該FINFET通道中產生應力，從而提高電子及電洞移動率且改進該FINFET之該效能。
2. 如請求項1之FINFET，其中該閘極包含一聚SiGe/聚Si層疊閘極且該閘極之該聚SiGe部分經選擇性地蝕刻以形成一以一應力薄膜再填充之閘極間隙以使得在該FINFET通道中產生應力。
3. 如請求項1之FINFET，其中該閘極間隙以一應力氮化物薄膜再填充以使得在該FINFET通道中產生應力。
4. 如請求項1之FINFET，其中該閘極間隙以一可壓縮應力氮化物薄膜再填充以使得在一pFINFET通道中產生應力。
5. 如請求項1之FINFET，其中該閘極間隙以一可拉伸應力氮化物薄膜再填充以使得在一nFINFET通道中產生應力。
6. 如請求項1之FINFET，其包括覆蓋該FINFET之另一應力氮化物薄膜以使得進一步對該通道施加應力。
7. 如請求項1之FINFET，其包括覆蓋一nFINFET之另一可

拉伸應力氮化物薄膜以使得進一步對該nFINFET之通道施加應力。

8. 如請求項1之FINFET，其包括覆蓋一pFINFET之另一可壓縮應力氮化物薄膜以使得進一步對該pFINFET之通道施加應力。
9. 如請求項1之FINFET，在一積體電路(IC)中該FINFET作為該IC之一個元件。
10. 一種製造一應變過的鰭式場效電晶體(FINFET)之方法，其使用應力材料取代閘極之一部分以使得對該FINFET之通道施加應力，該方法包含：

製造FINFET，其具有一源極、一汲極及包含具有不同蝕刻特性之兩種不同類型之半導體材料的一層疊閘極；

選擇性地蝕刻該層疊閘極之該等兩種不同類型之半導體材料的一者以形成一閘極間隙；及

以一應力薄膜再填充該閘極間隙以使得在該FINFET通道中產生應力，從而提高電子及電洞移動率且改進該FINFET之效能。

11. 如請求項10之方法，其包括製造該層疊閘極為一聚SiGe/聚Si層疊閘極，且選擇性地蝕刻該閘極之該聚SiGe部分以形成該閘極間隙。
12. 如請求項10之方法，其包括以一應力氮化物薄膜再填充該閘極間隙以使得在該FINFET通道中產生應力。
13. 如請求項10之方法，其包括以一可壓縮應力氮化物薄膜再填充該閘極間隙以使得在一pFINFET通道中產生應

力。

14. 如請求項10之方法，其包括以一可拉伸應力氮化物薄膜再填充該閘極間隙以使得在一nFINFET通道中產生應力。
15. 如請求項10之方法，其包括以另一可應力氮化物薄膜覆蓋該FINFET以使得進一步對該通道施加應力。
16. 如請求項10之方法，其包括以另一可拉伸應力氮化物薄膜覆蓋一nFINFET以使得進一步對該nFINFET之通道施加應力。
17. 如請求項10之方法，其包括以另一壓縮應力氮化物薄膜覆蓋一pFINFET以使得進一步對該pFINFET之通道施加應力。
18. 一種製造一應變過的鰭式場效電晶體(FINFET)之方法，其使用應力材料取代閘極之一部分以使得對該FINFET之通道施加應力，該方法其包含：
 - 以一Si鰭狀物開始，該Si鰭狀物在其側壁上具有一側壁保護層，沈積一聚Si層及一隨後之聚SiGe層於該Si鰭狀物上；
 - 圖案化光阻劑(PR)以用於一閘極反應性離子蝕刻(RIE)；
 - RIE聚SiGe且RIE該聚Si以形成一閘極；
 - 選擇性地蝕刻該聚SiGe至聚Si，其中該閘極之該SiGe部分經蝕刻去除以在該閘極中形成一間隙；
 - 形成矽化物接觸；及

沈積應力薄膜以填充該閘極中之該間隙。

19. 如請求項18之方法，其中遵循以下RIE步驟：

植入摻雜劑以用於擴展形成；

沈積氮化物且RIE該氮化物以在閘極側壁上形成氮化物隔片；及

植入源極及汲極(S/D)摻雜劑且退火。

20. 如請求項18之方法，其中遵循以下RIE步驟：

熱再氧化閘極側壁以形成一薄氧化物，以便保護該等閘極側壁及/或作為一隔片用於擴展植入；及

植入角形摻雜劑以用於擴展形成。

21. 如請求項18之方法，其中遵循以下沈積應力薄膜之步驟：各向同性地回蝕該應力薄膜以移除源極及汲極區域中之該應力薄膜。

22. 如請求項18之方法，其包括藉由濕式蝕刻源極及汲極區域中之薄氧化物而形成矽化物接觸，沈積薄Ni且退火以形成NiSi。

23. 如請求項18之方法，其包括對於一pFINFET而言沈積可壓縮應力氮化物薄膜。

24. 如請求項18之方法，其包括對於一nFINFET而言沈積可拉伸應力氮化物薄膜。

25. 如請求項18之方法，其包括以另一應力氮化物薄膜覆蓋該FINFET以使得進一步對該通道施加應力。

26. 如請求項18之方法，其包括以另一可拉伸應力氮化物薄膜覆蓋一nFINFET以使得進一步對該通道施加應力。

27. 如請求項18之方法，其包括以另一可壓縮應力氮化物薄膜覆蓋一pFINFET以使得進一步對該通道施加應力。

十一、圖式：

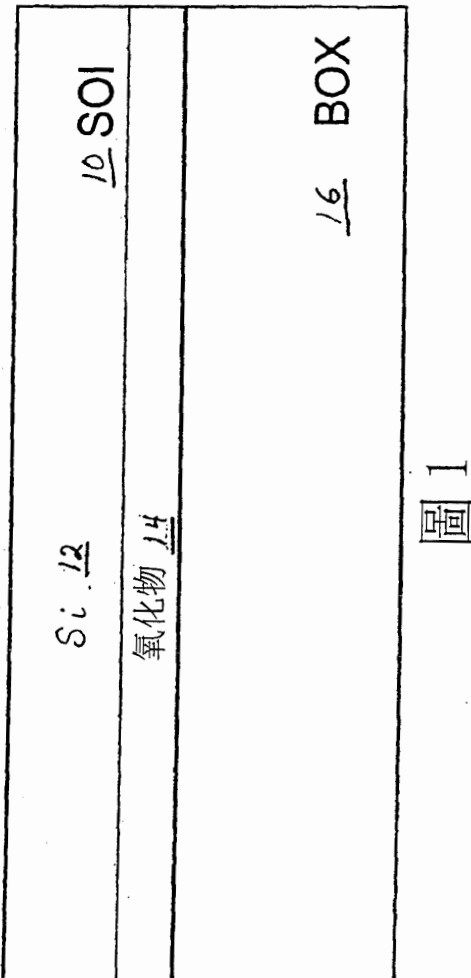


圖 1

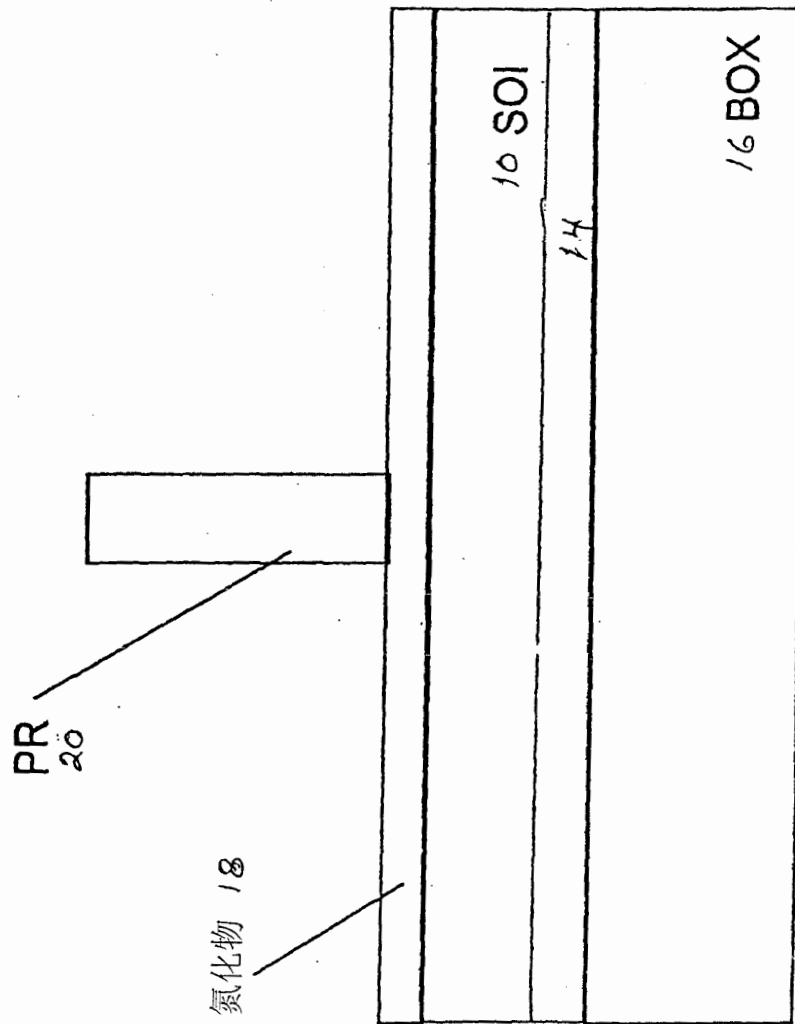


圖 2

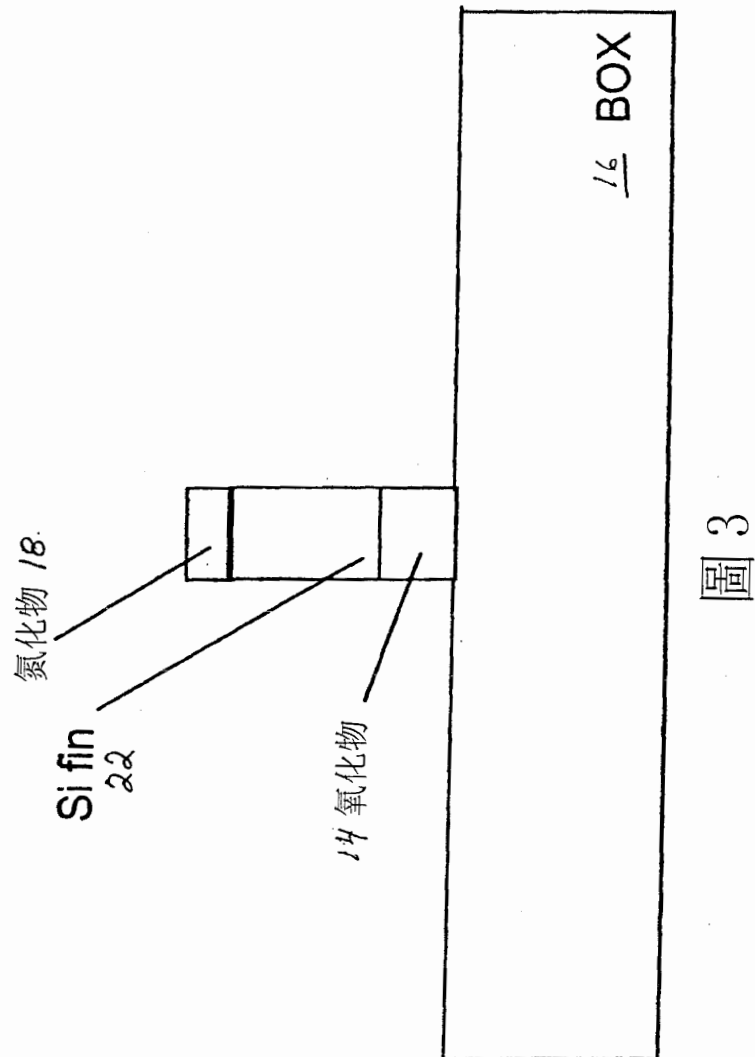


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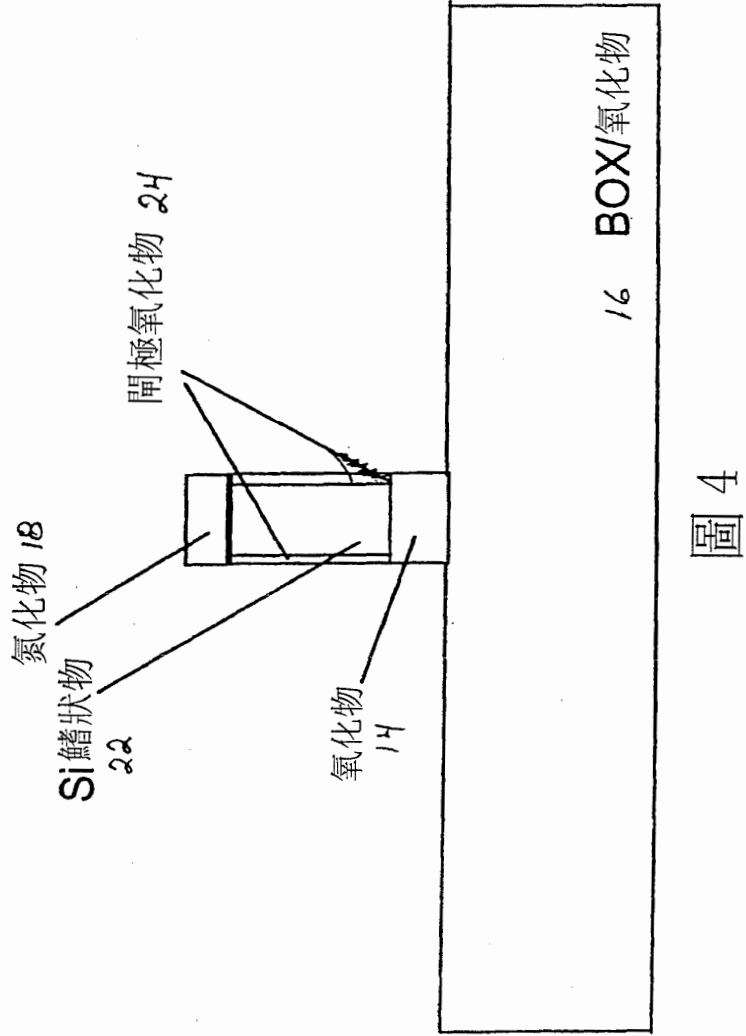


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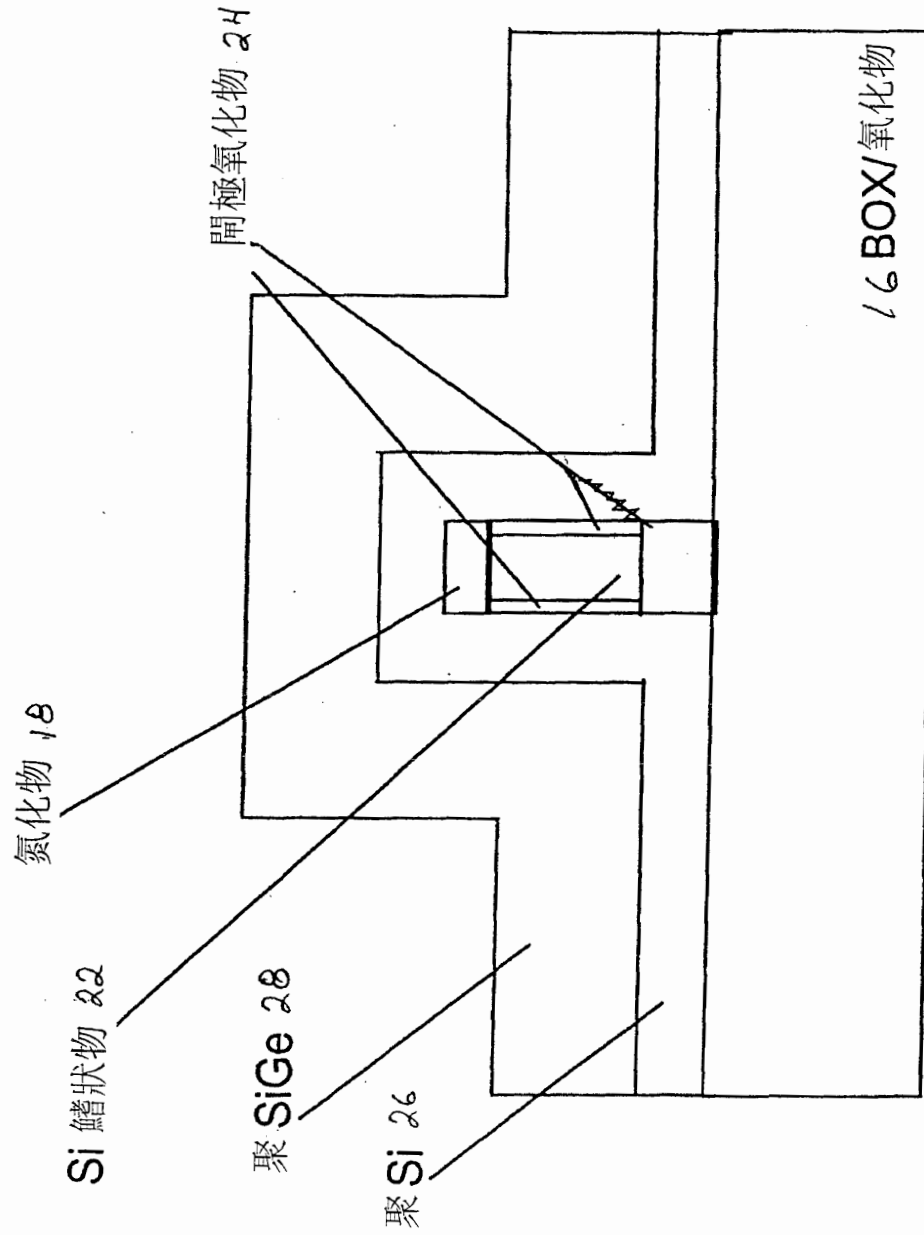


圖 5

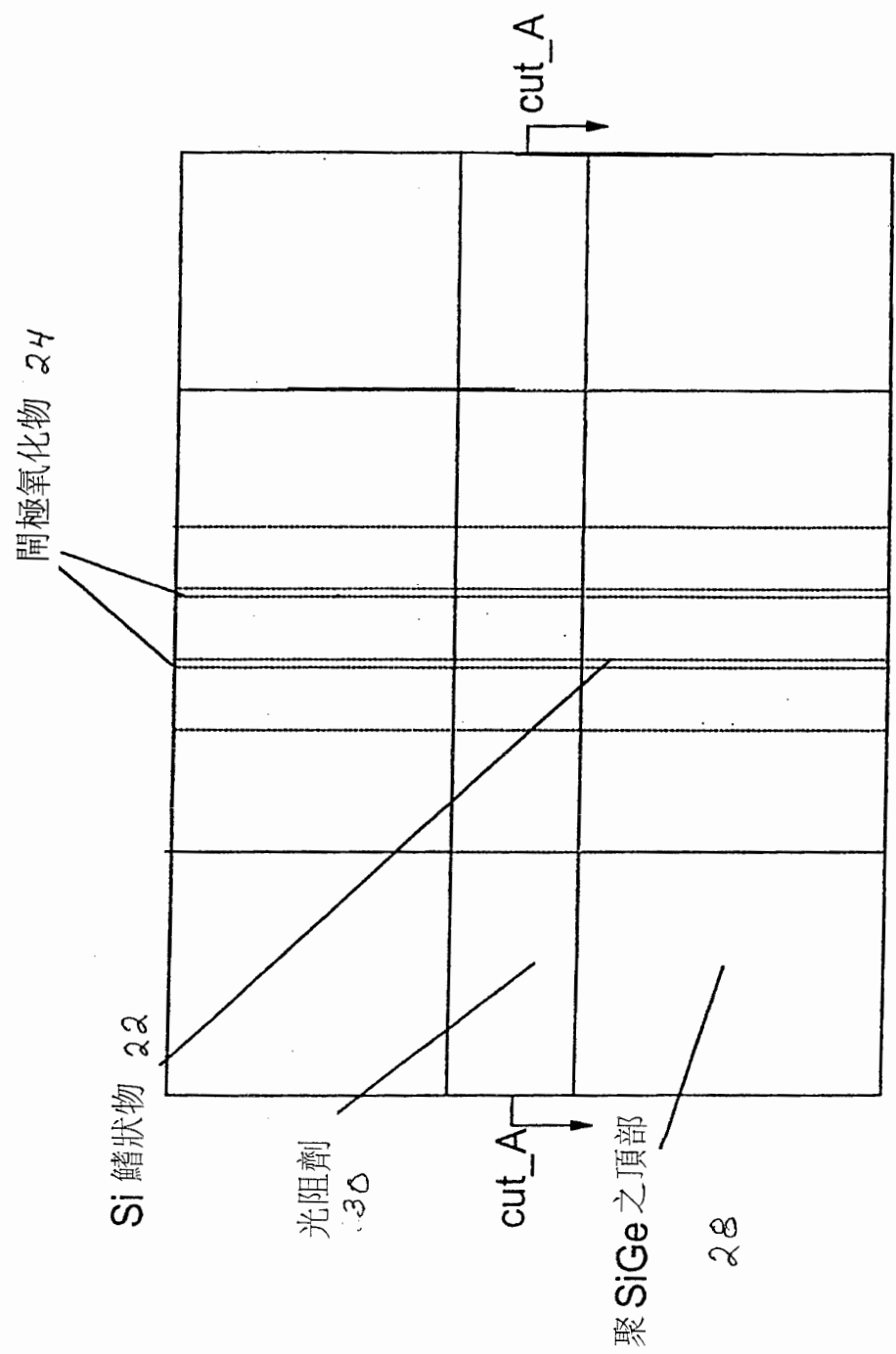


圖 6

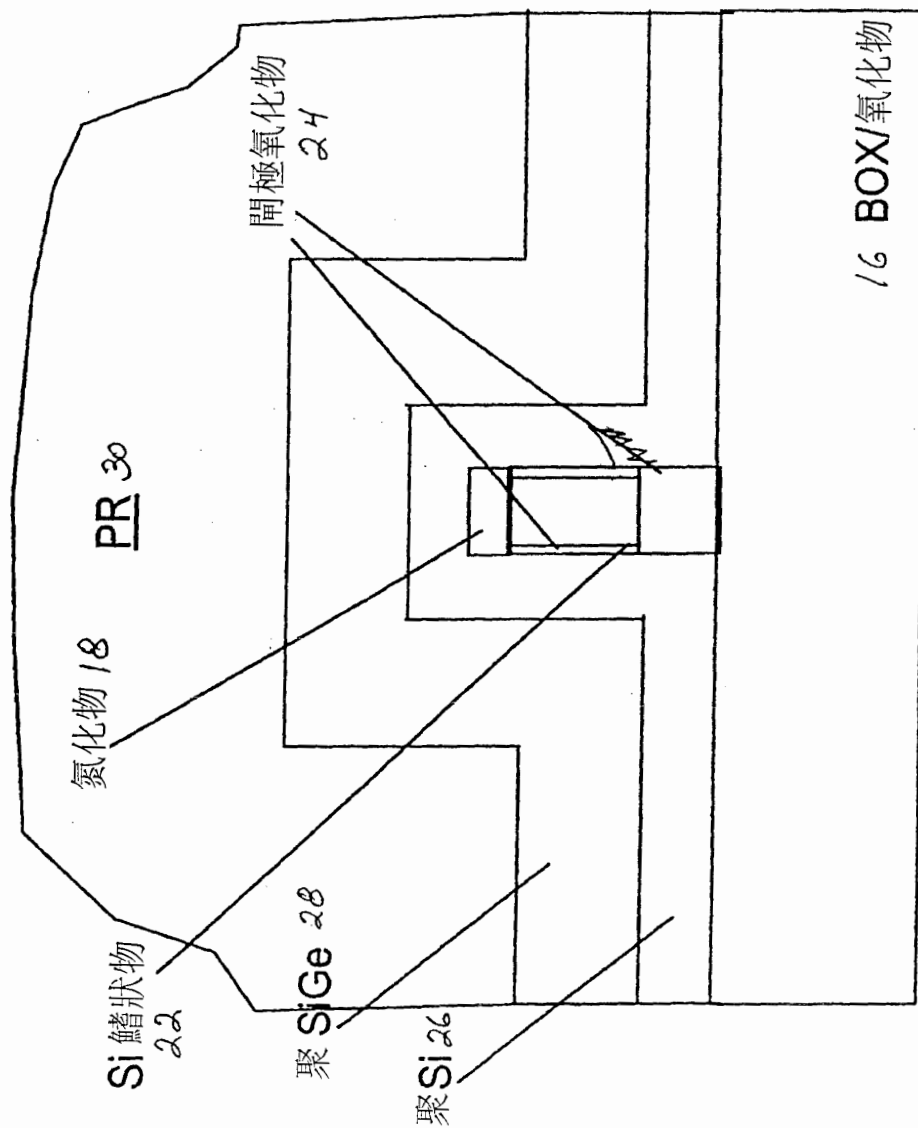


圖 6A

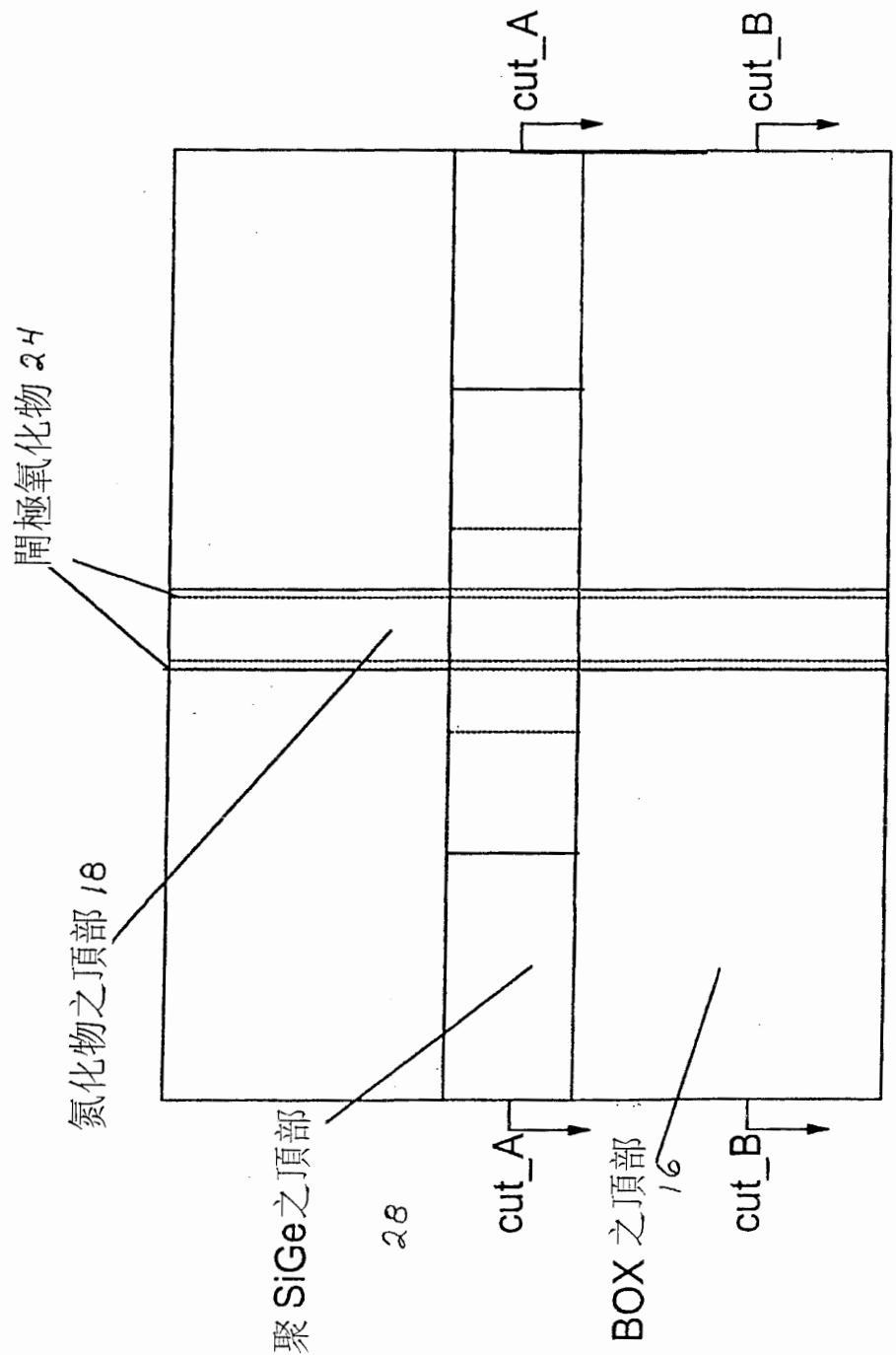


圖 7

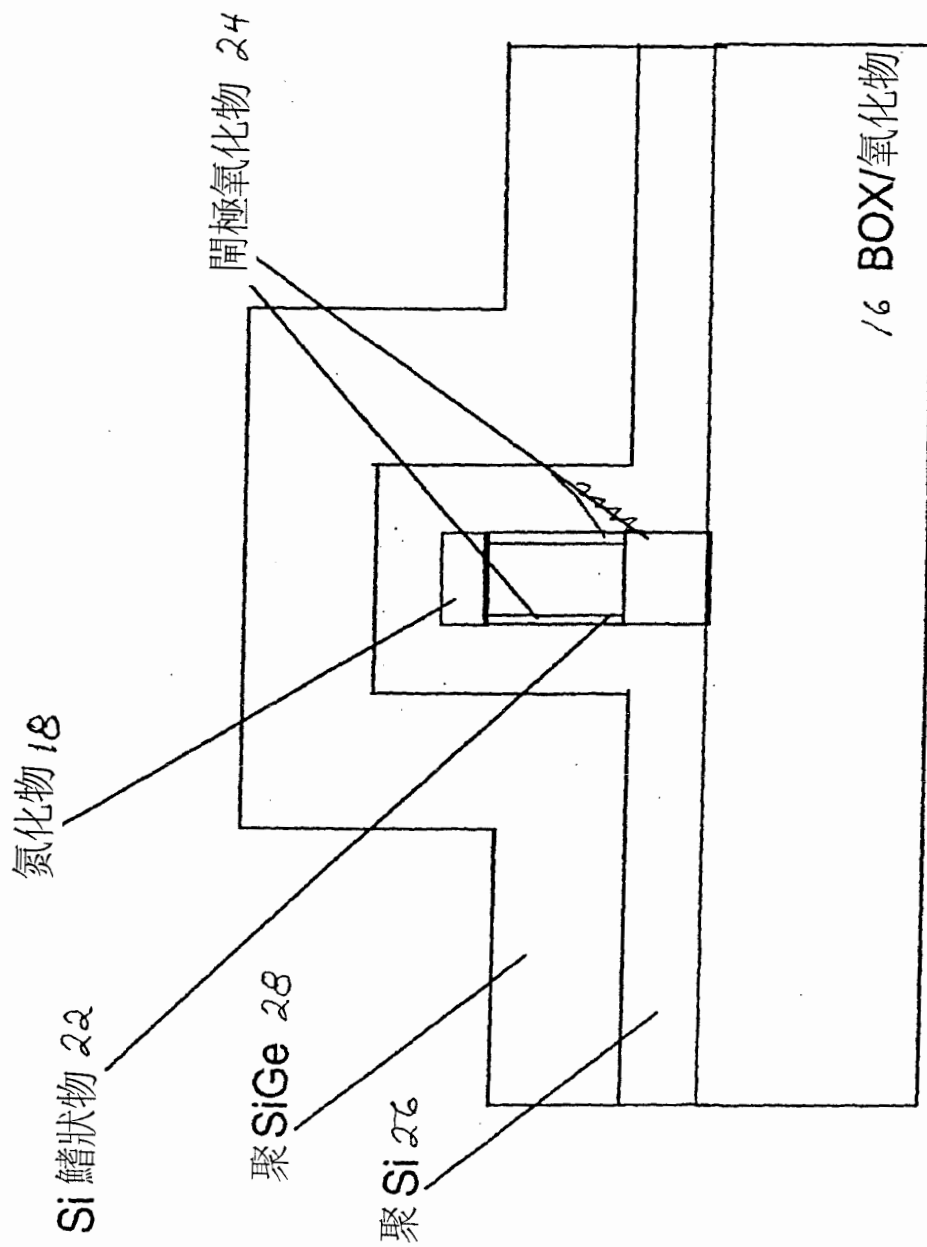
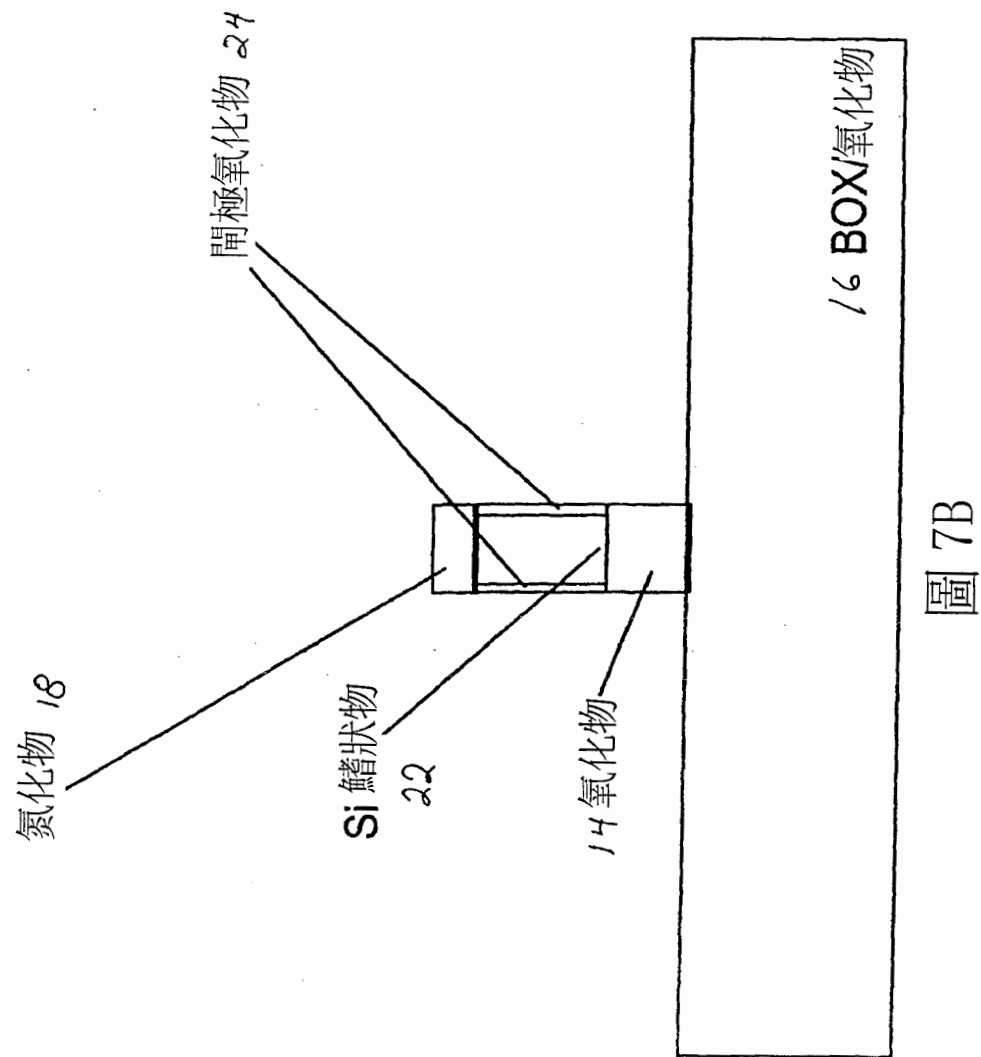
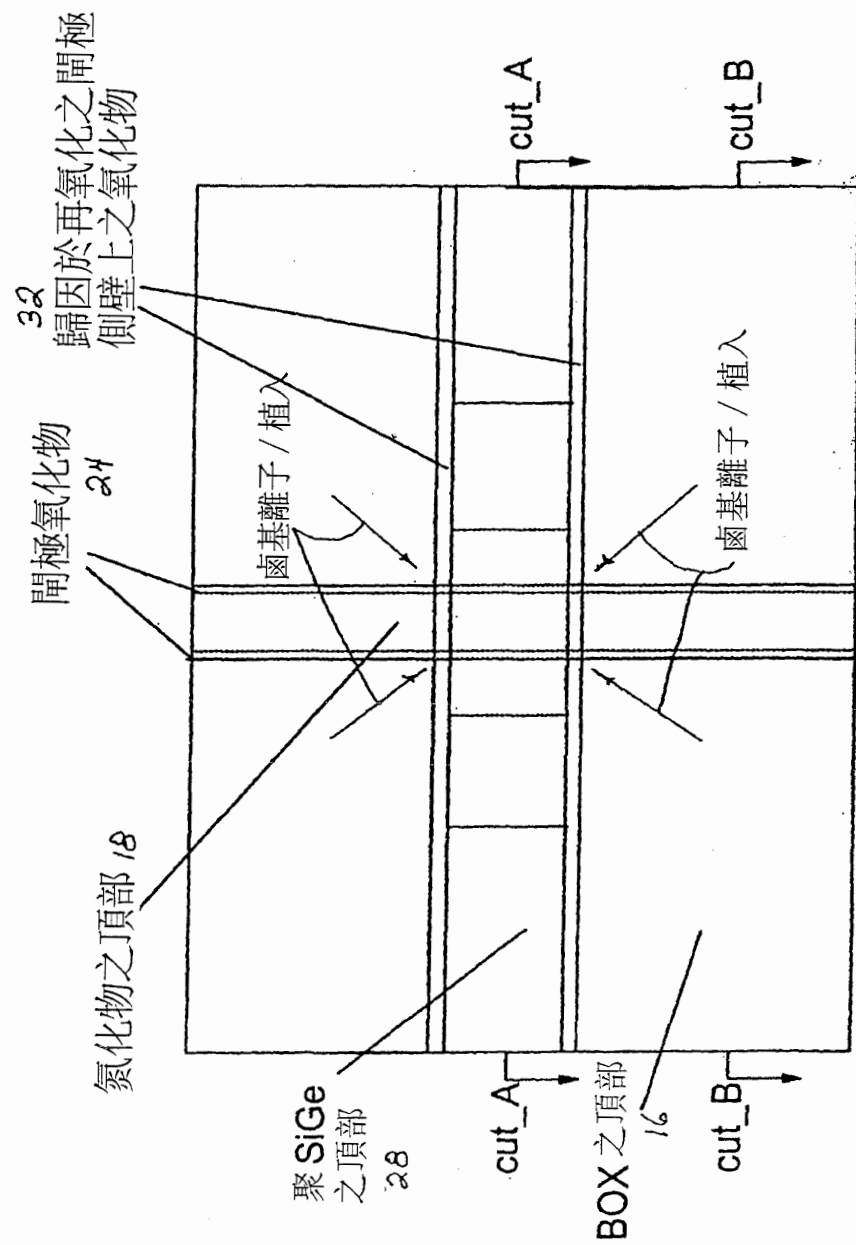


圖 7A





回

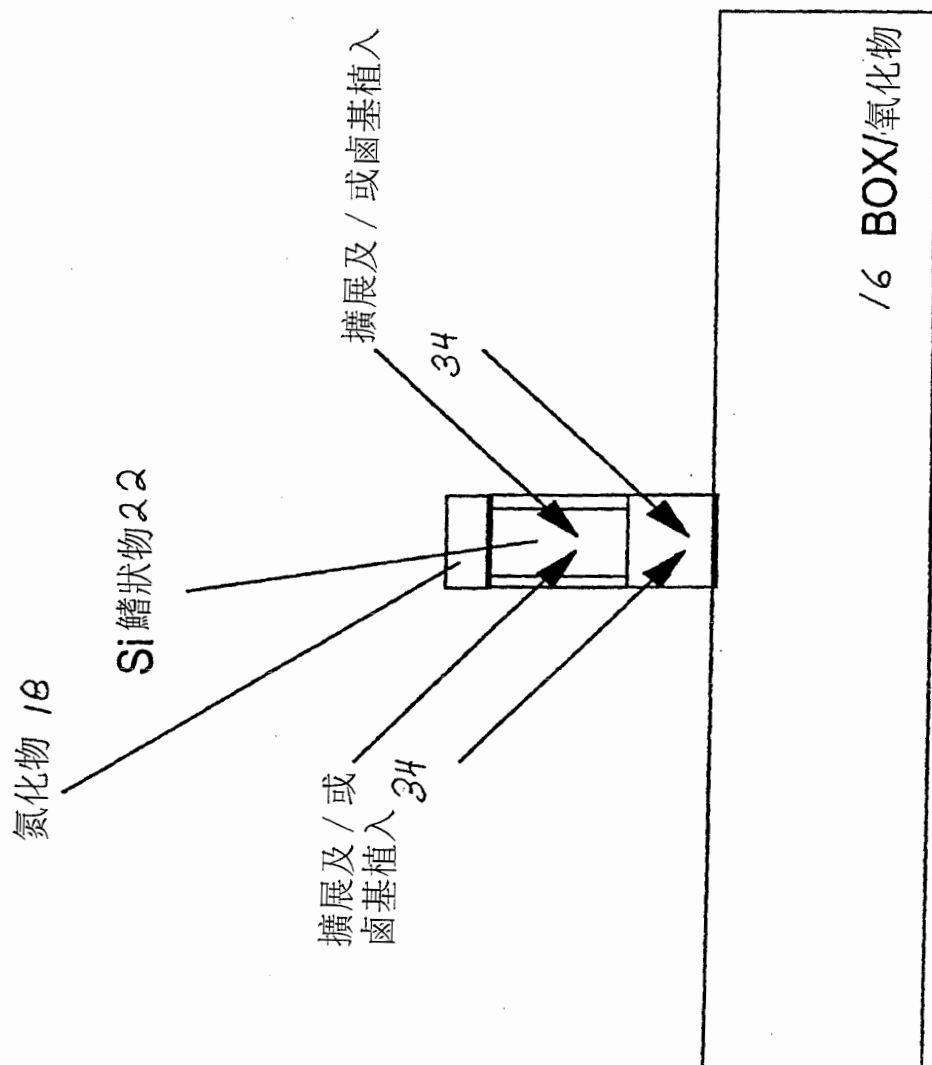


圖 9

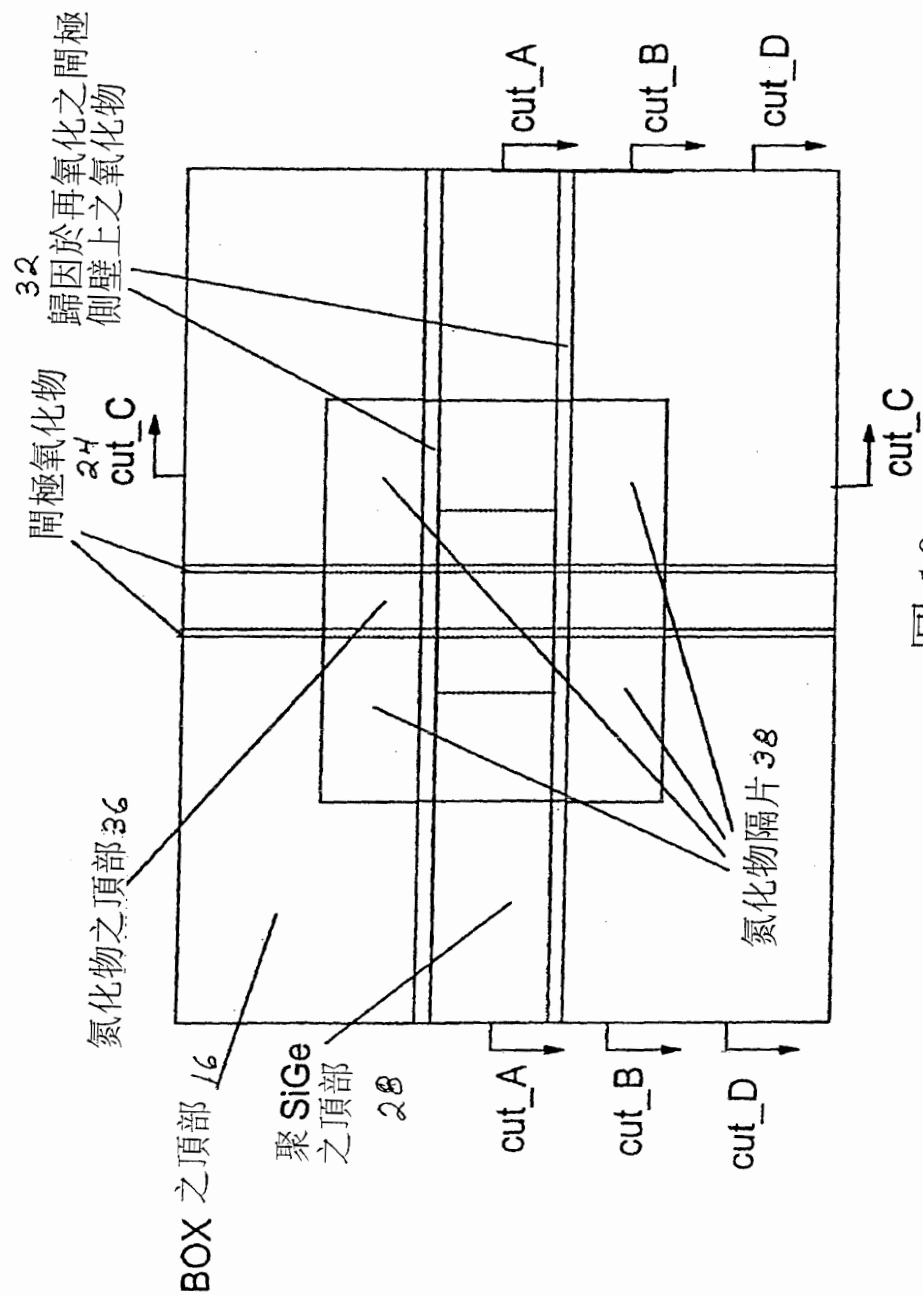


圖 10

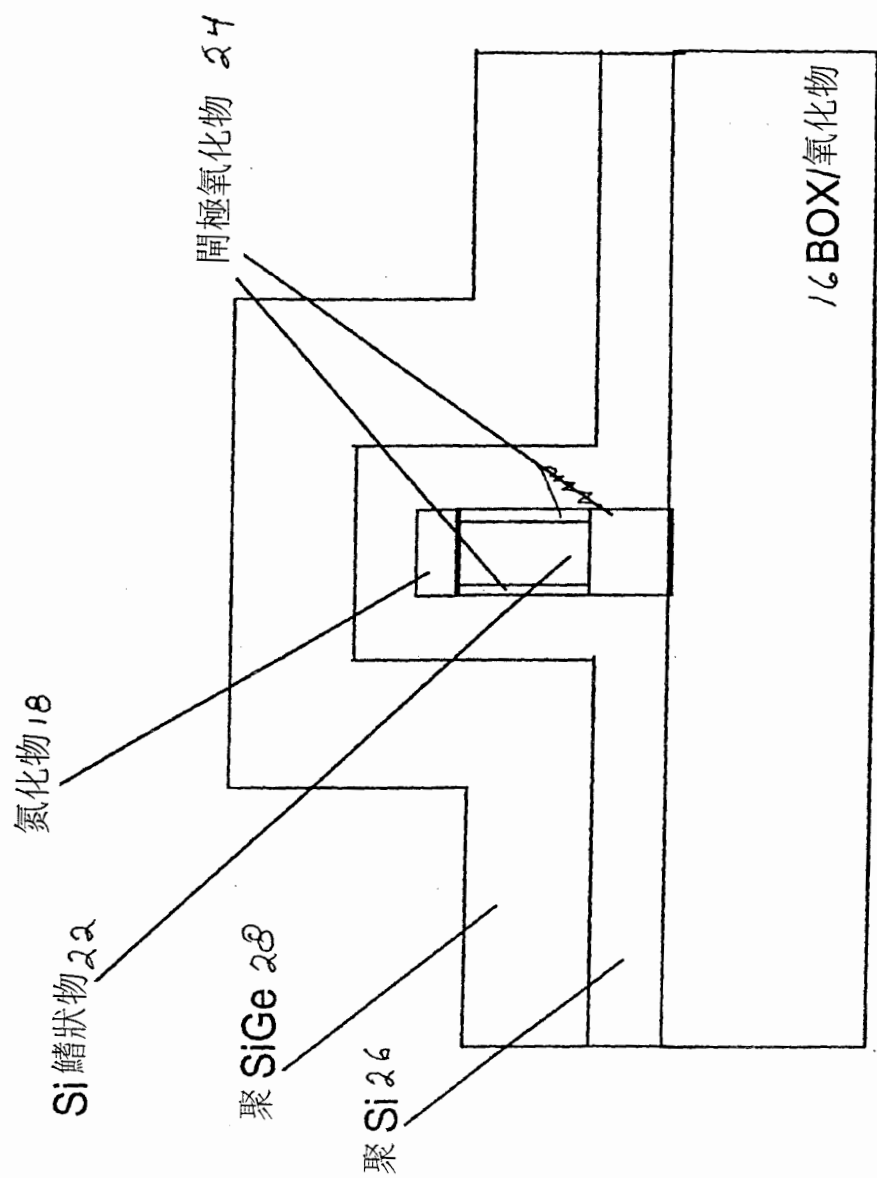


圖 10A

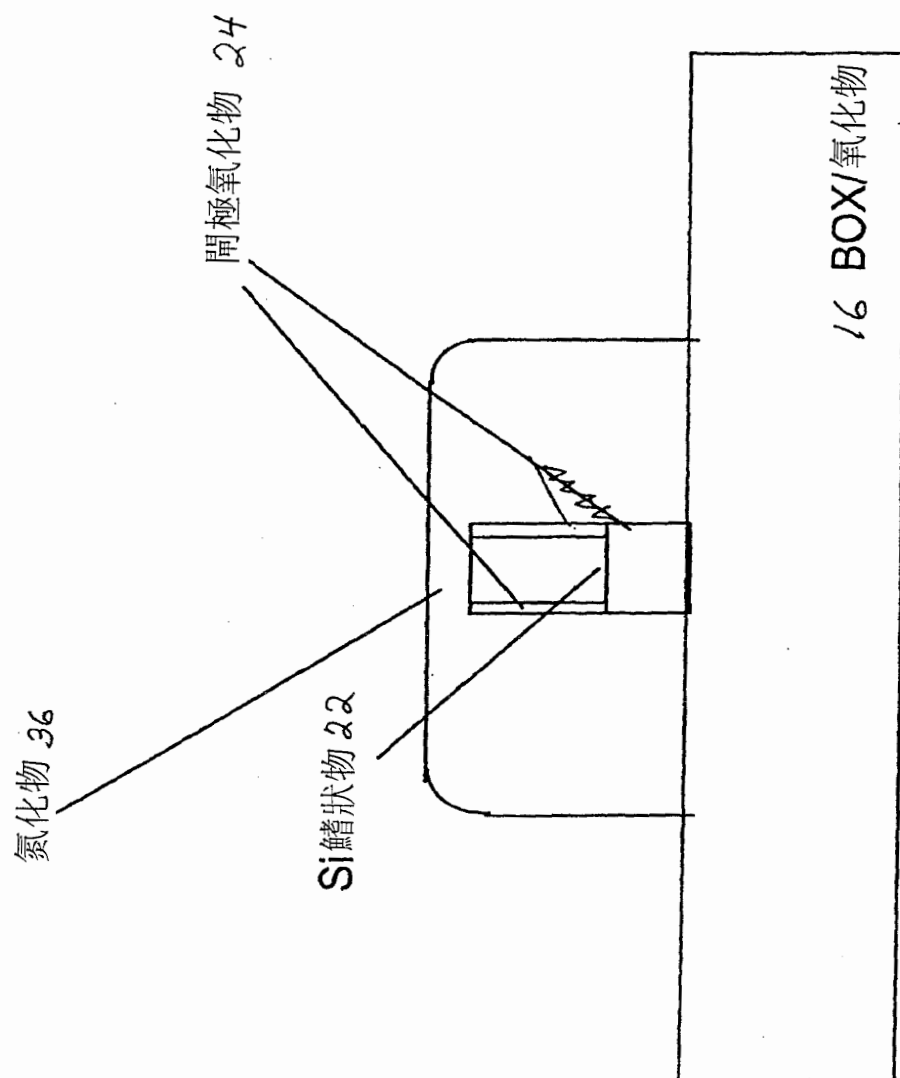


圖 10B

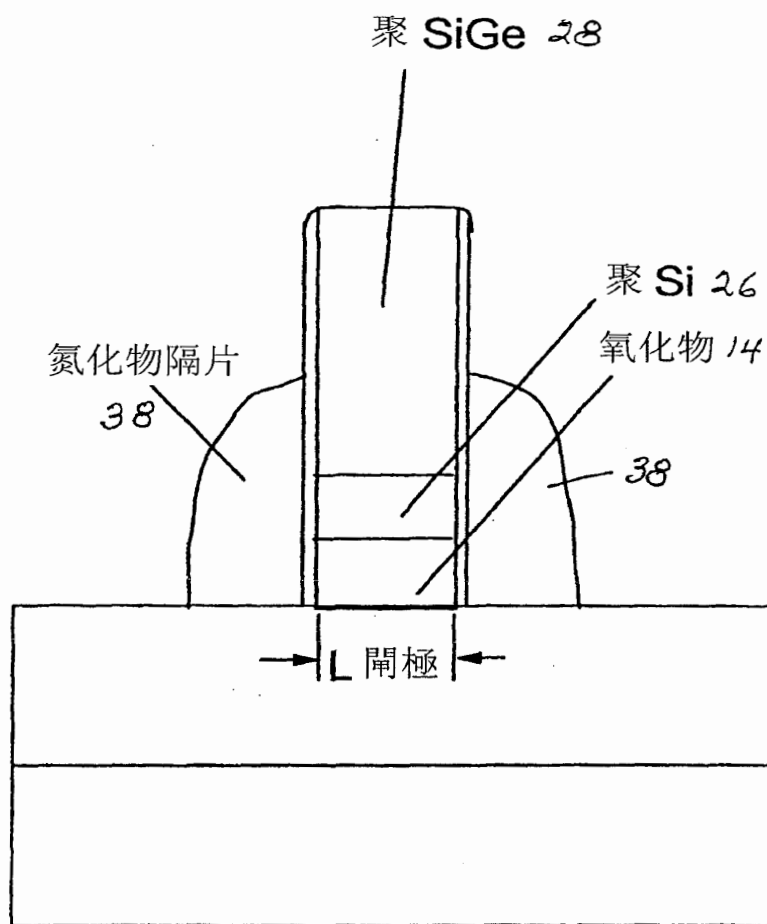
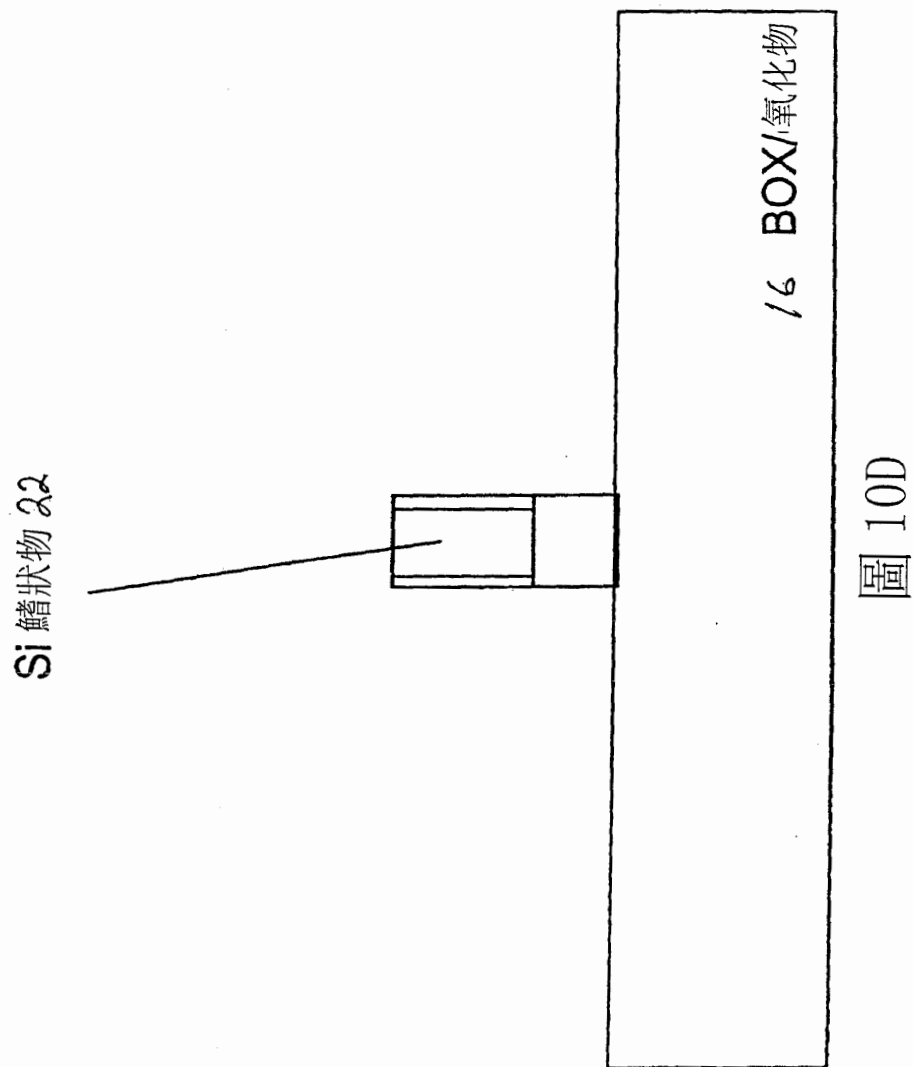


圖 10C



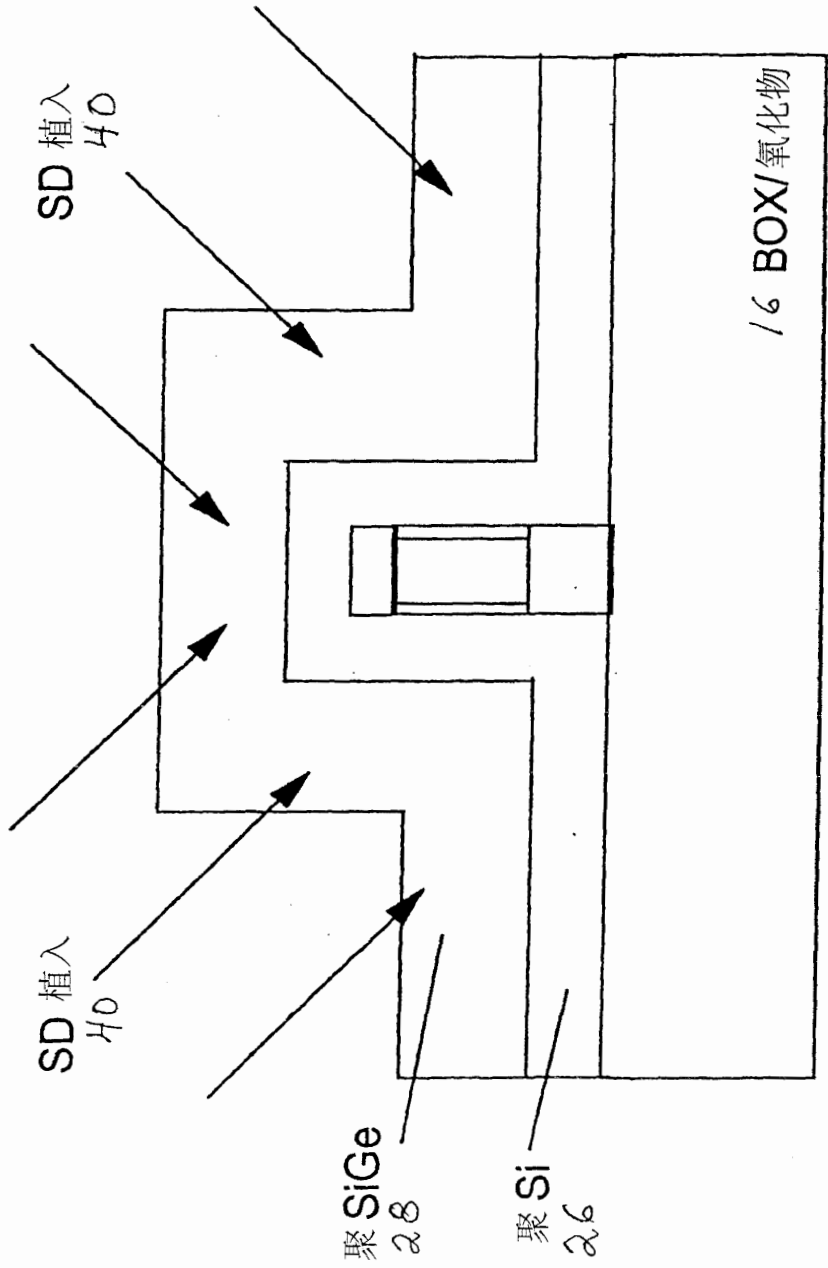


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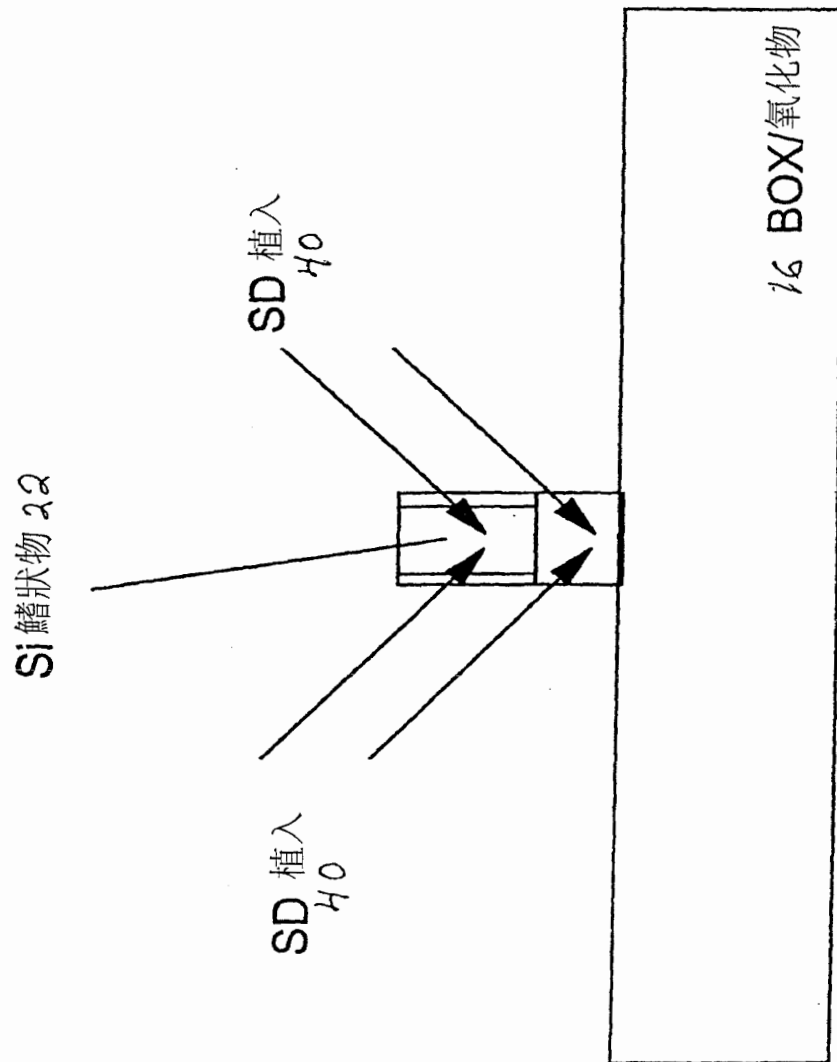


圖 11D

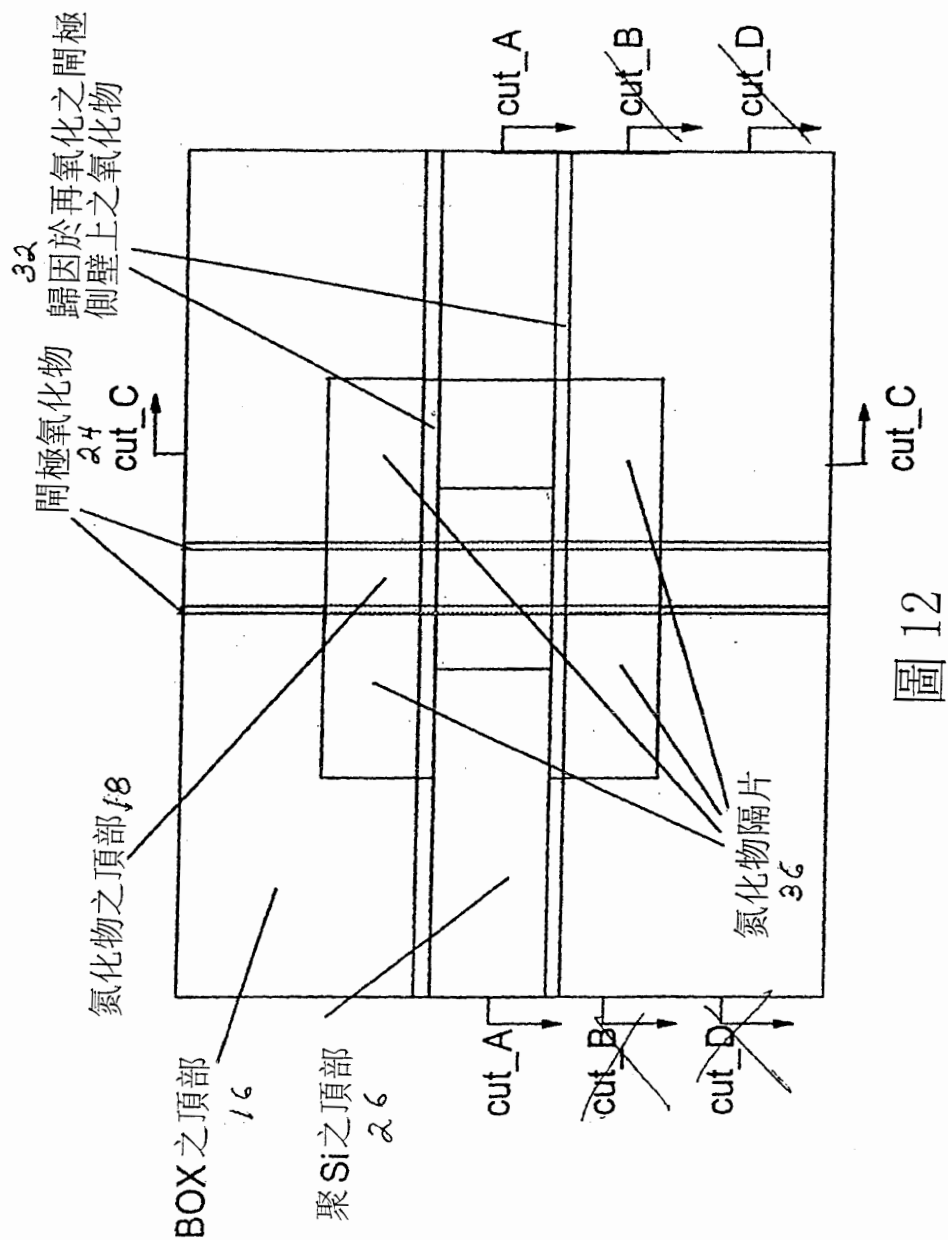


圖 12

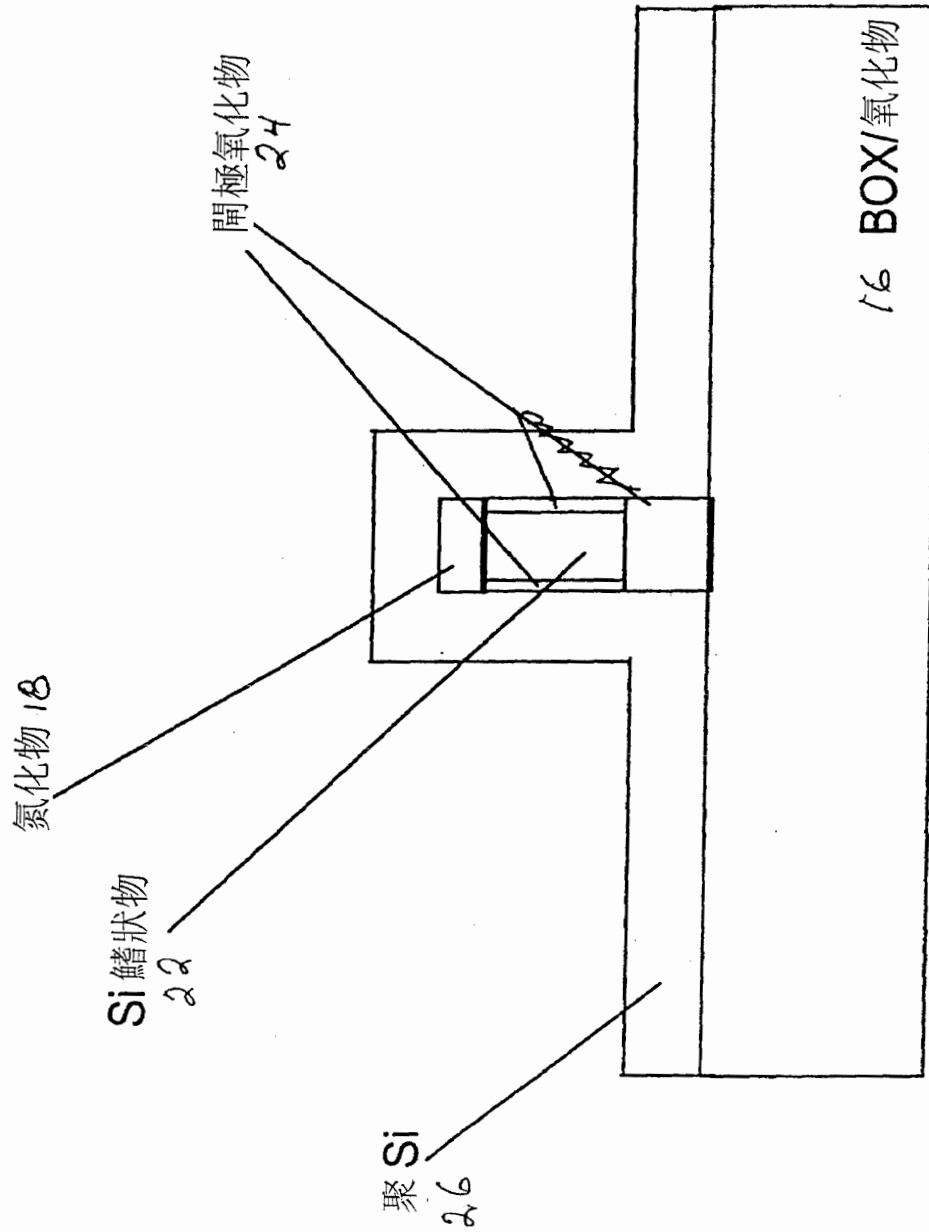


圖 12A

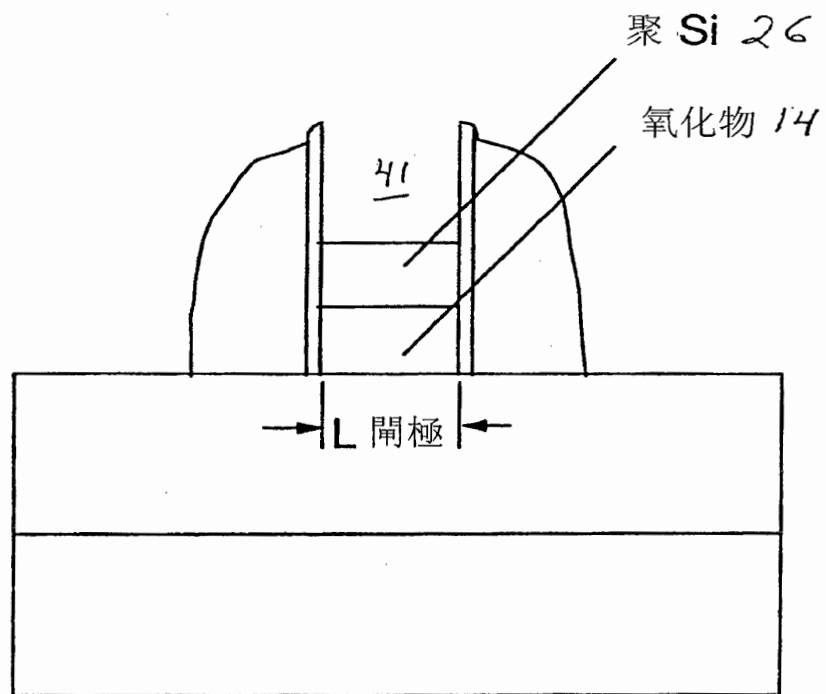
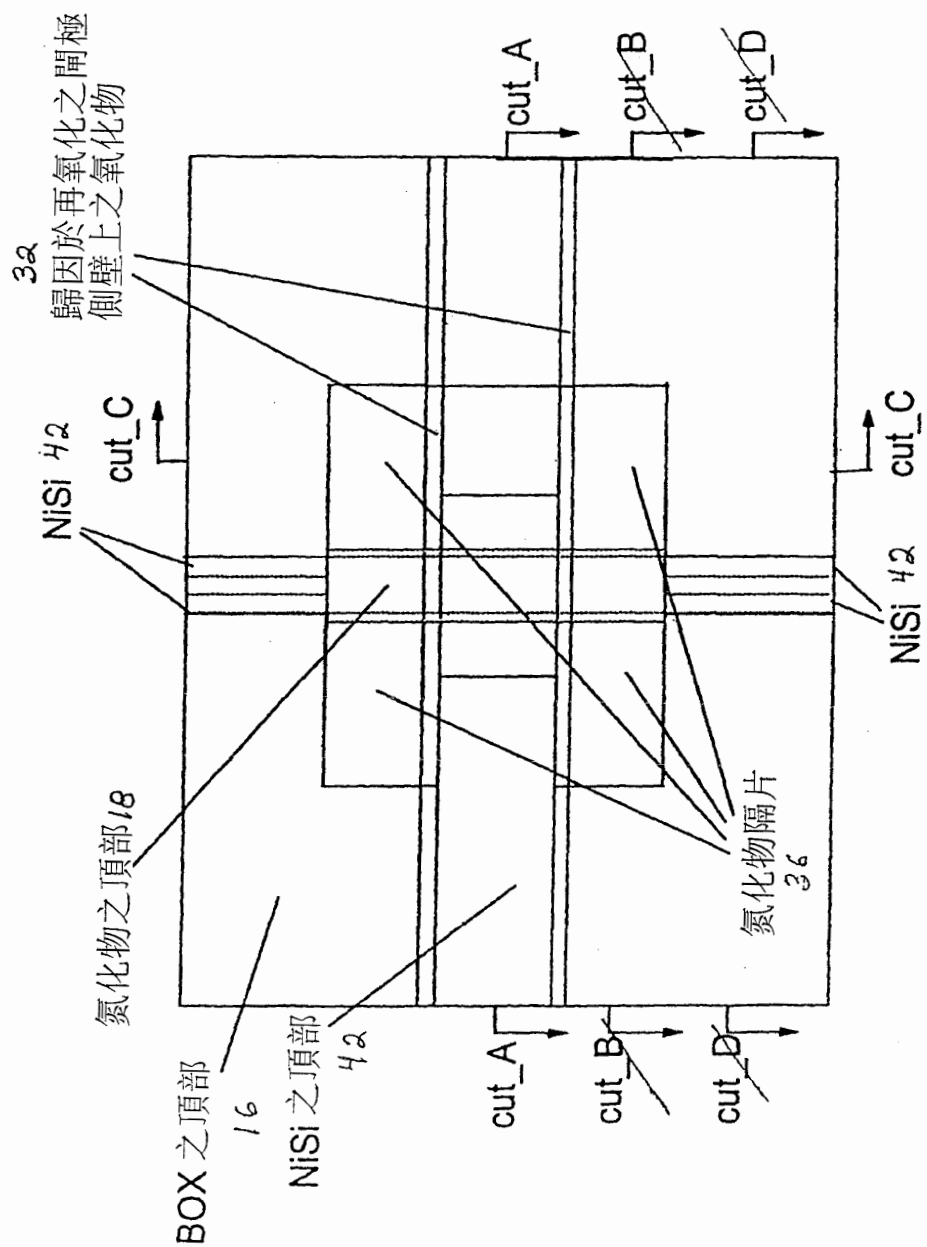
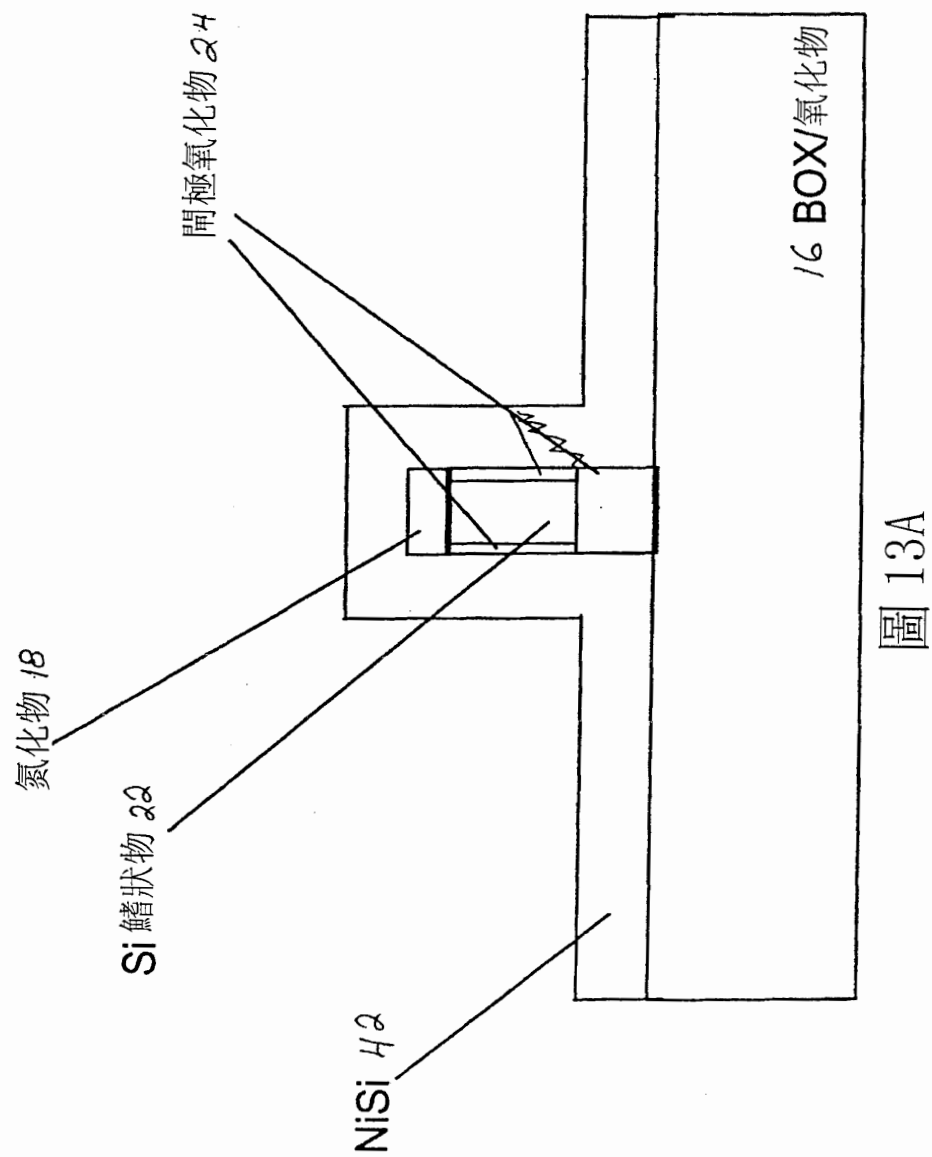


圖 12C



13



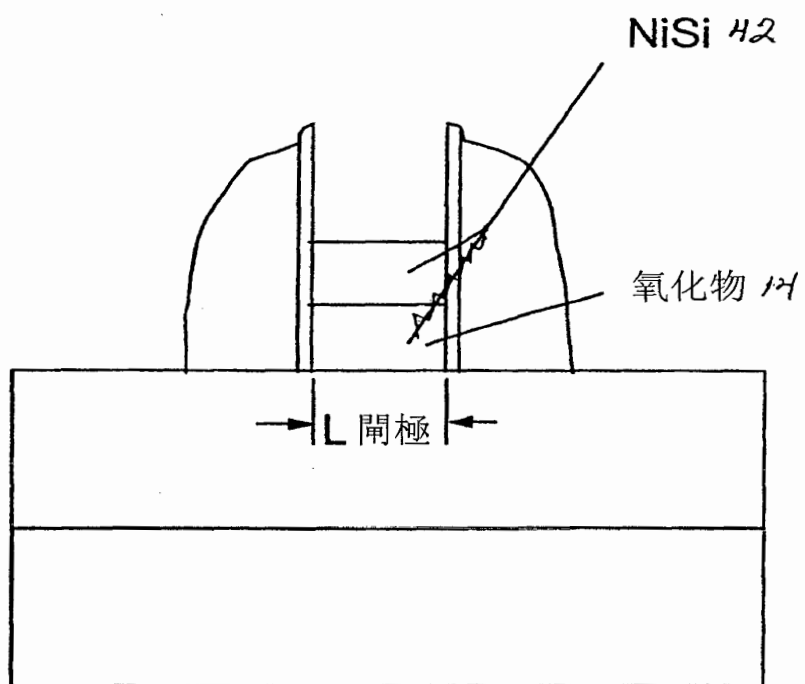


圖 13C

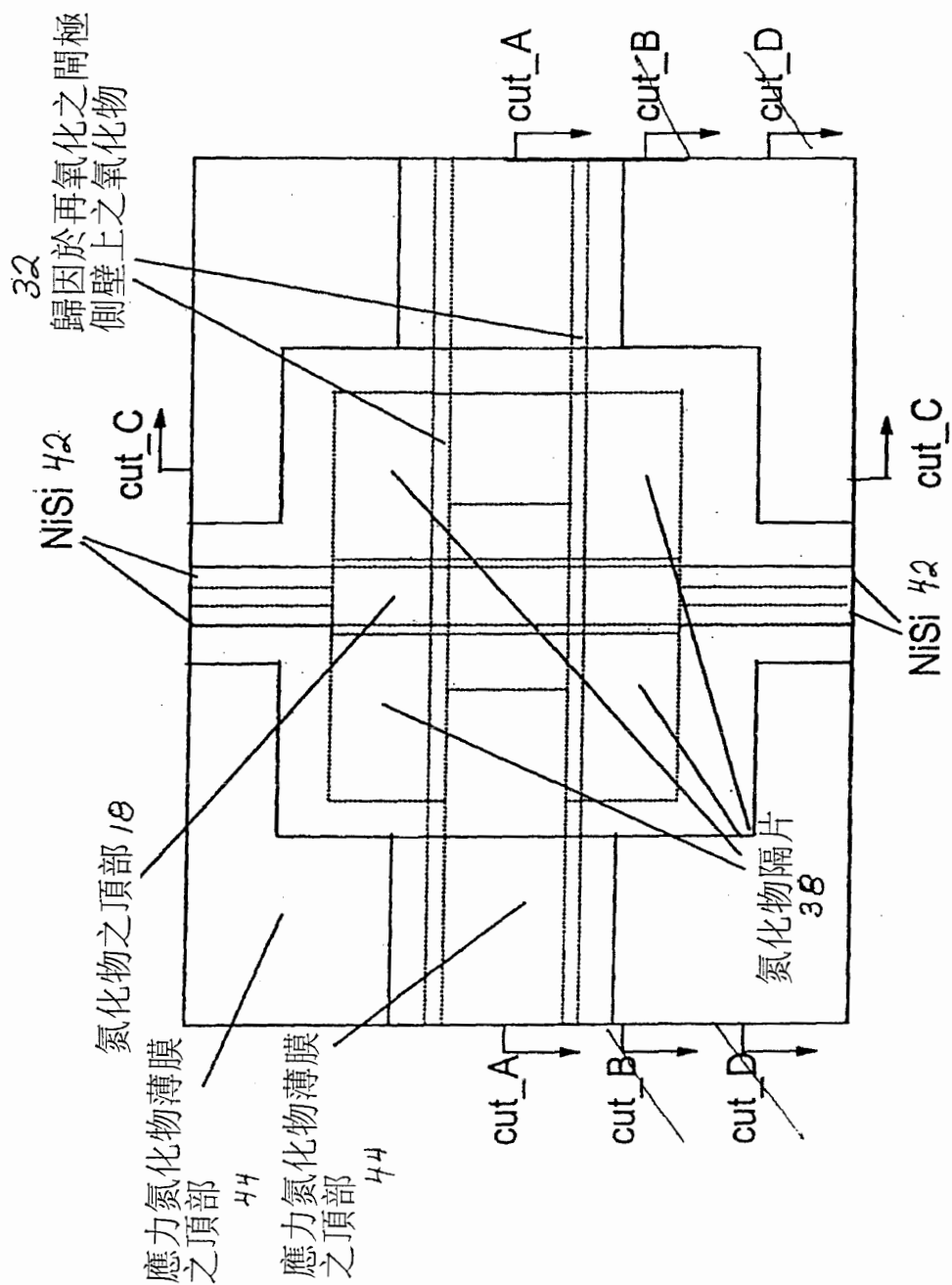


圖 14

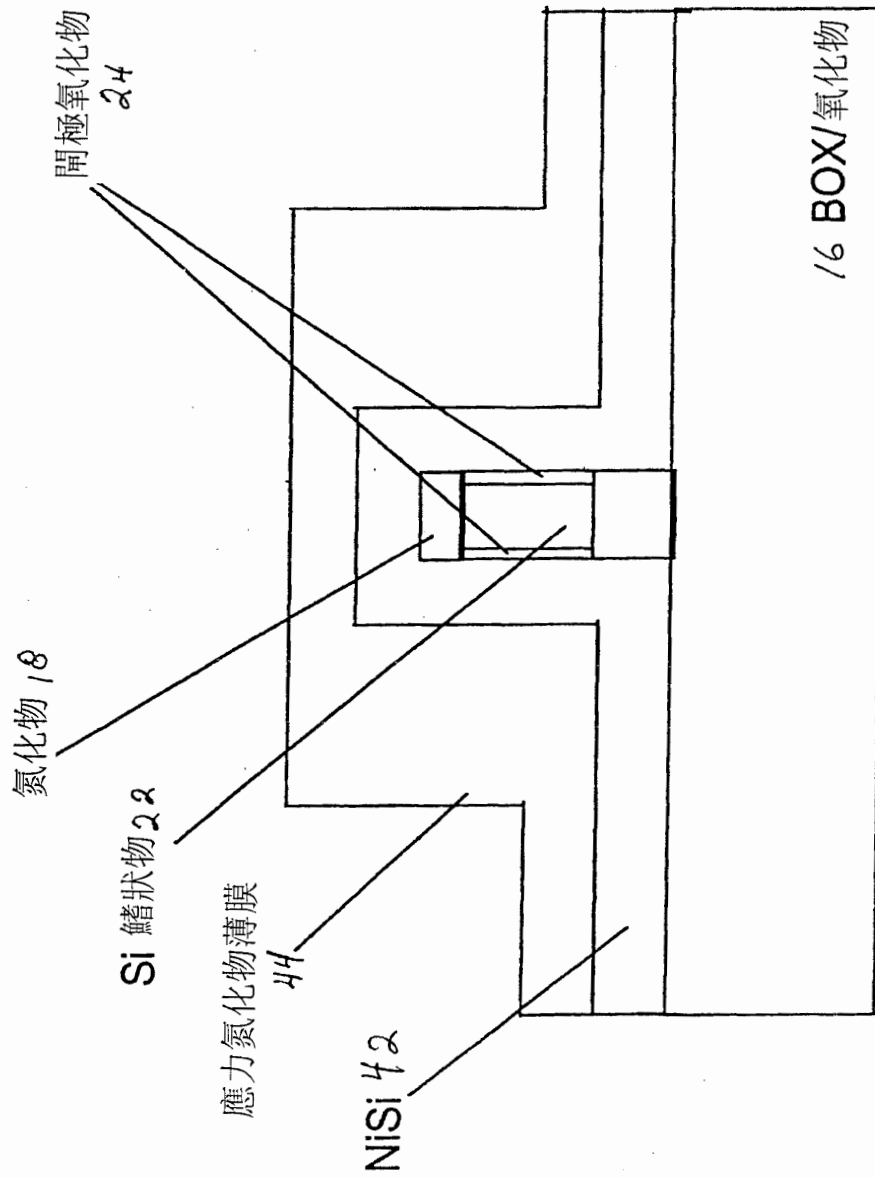


圖 14A

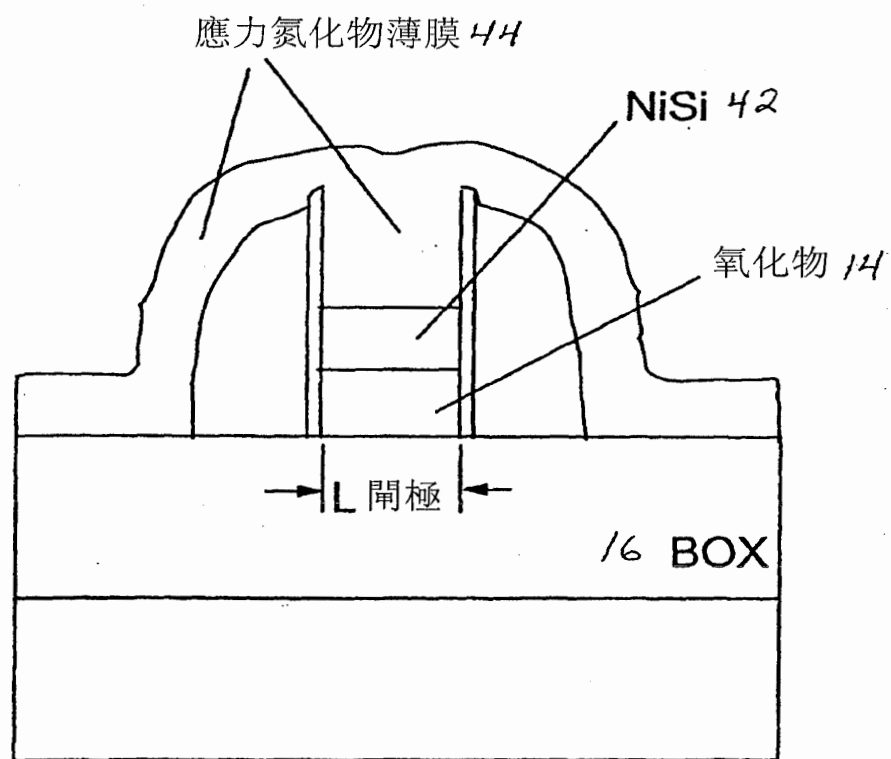


圖 14C

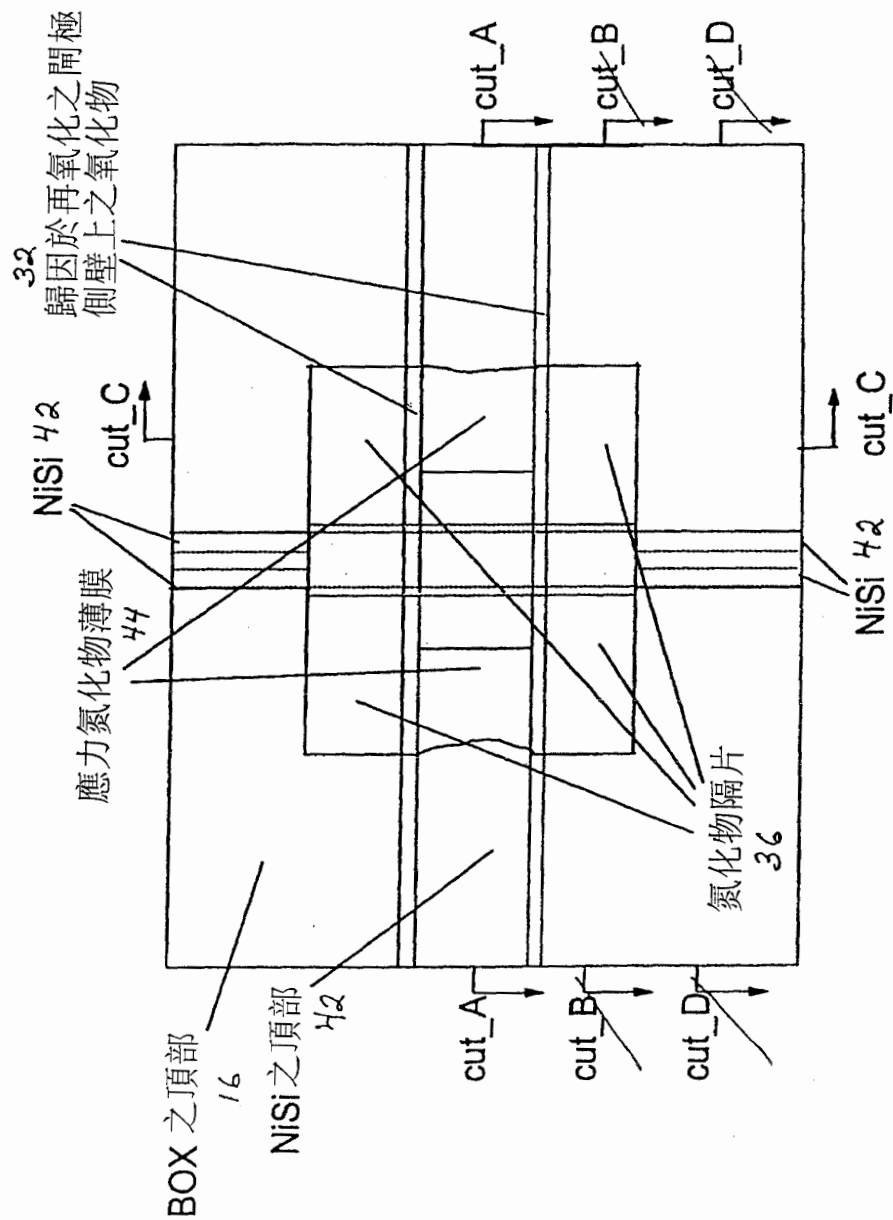


圖 15

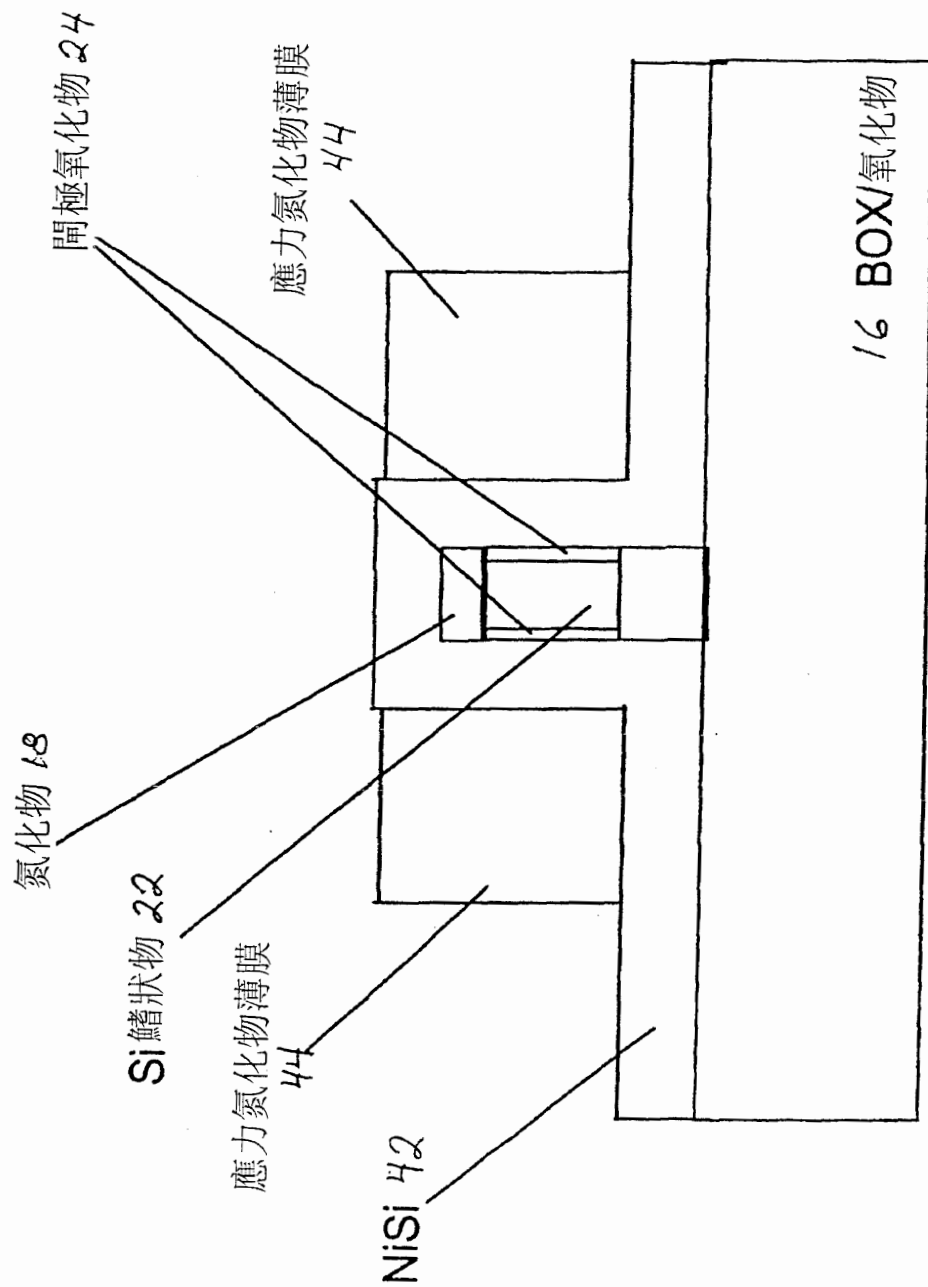


圖 15A

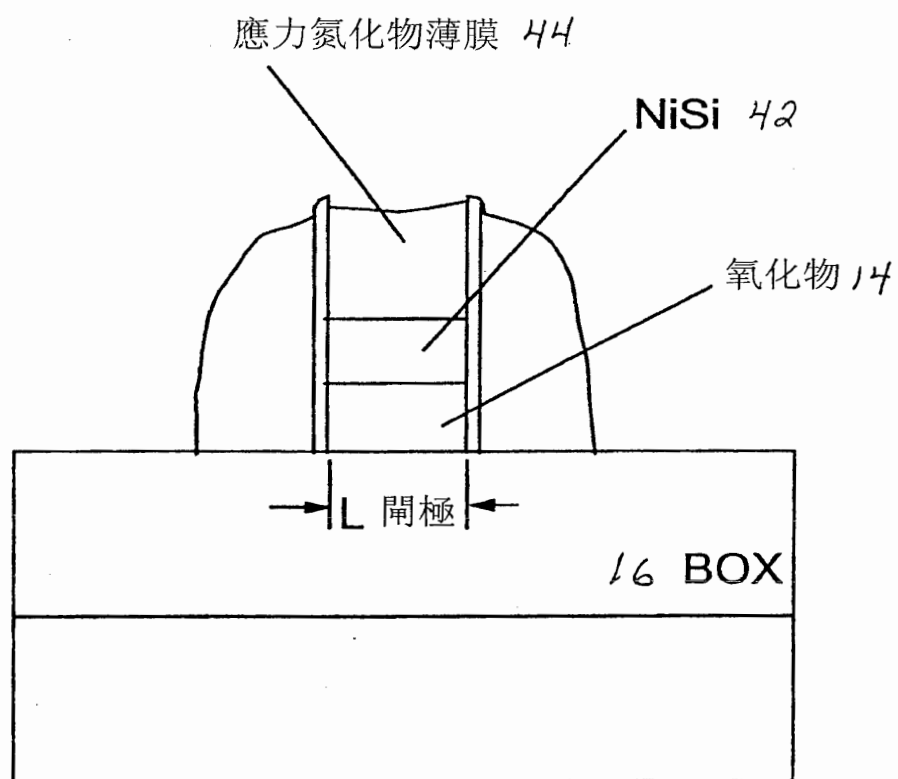


圖 15C

Electronic Acknowledgement Receipt	
EFS ID:	9778052
Application Number:	12781826
International Application Number:	
Confirmation Number:	3483
Title of Invention:	Method of fabricating metal oxide semiconductor transistor
First Named Inventor/Applicant Name:	Chu-Yin Tseng
Customer Number:	27765
Filer:	Winston Hsu/Maggie Ko
Filer Authorized By:	Winston Hsu
Attorney Docket Number:	NAUP0913USA1
Receipt Date:	31-MAR-2011
Filing Date:	18-MAY-2010
Time Stamp:	04:54:58
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal Letter	1084784.PDF	22203 72e651787fa5f3aa29d7a9ca2f69b196de11929b	no	2

Warnings:

Information:

2	Information Disclosure Statement (IDS) Filed (SB/08)	1084786.PDF	30047 19a06fff504065842cc9bc28205a8196e3270415	no	3
Warnings:					
Information:					
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3	Foreign Reference	TW_200509310.pdf	1632387 bf5df20ba7c3a9e322b4298648eca86f351d9ae2	no	21
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Information:					
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Warnings:					
Information:					
Total Files Size (in bytes):			4146422		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Chu-Yin Tseng
5 Shih-Chieh Hsu
Chih-Chiang Wu
Shyh-Fann Ting
Po-Lun Cheng
Hsuan-Hsu Chen
10 Appl. No.: 12/781,826 Filing Date: 05/18/2010
Examiner: DANG, PHUC T Art Unit: 2892
Docket No.: NAUP0913USA1 Confirmation No.: 3483

Title: Method of fabricating metal oxide semiconductor transistor

15

To: Commissioner for Patents
P.O. BOX 1450
Alexandria, VA 22313-1450

20 Subject: Information disclosure statement under 37 CFR §1.56

Dear Sir,

25 This is an Information Disclosure Statement in accordance with the
duty to disclose information material to patentability under 37 CFR
§1.56. The applicant wishes to make of record the document(s) listed on
the accompanying form PTO/SB/08.

30 Since this IDS is filed after the mailing date of the first Office action but

before final Office action/notice of allowance, consideration of the information disclosure statement is hereby requested according to 37 CFR §1.97(c).

5 That each item of information contained in the information disclosure statement was first cited in an Office communication mailed on Office communication for the counterpart Taiwan application number 096129401, which are no more than three months prior to the filing of the information disclosure statement.

10 According to the requirement set forth in 37 CFR 1.98(a)(3) and MPEP 609.04(a) III, an English language abstract of each cited reference is included herewith to fulfill the concise explanation requirement.

15 It is respectfully requested that the examiner can consider the document(s) listed on the accompanying form PTO/SB/08 and that it be made of record in the application. The applicant sincerely hopes that the examiner initials the cited reference(s) on the form and that a copy of the initialed form be sent to the applicant with the next communication from the examiner.

20 Sincerely yours,

/Scott Margo/

Date: 03/30/2011

Scott Margo, Patent Agent No. 56,277

P.O. BOX 506, Merrifield, VA 22116, U.S.A.

25 Voice Mail: 302-729-1562

Facsimile: 806-498-6673

e-mail : ScottMargo@naipo.com

Note: Please leave a message in my voice mail if you need to talk to me. (The time in
30 D.C. is 12 hours behind the Taiwan time, i.e. 9 AM in D.C. = 9 PM in Taiwan.)

Method of fabricating metal oxide semiconductor transistor

Appl. No. : 12/781,826 Confirmation No. 3483
Applicant : Chu-Yin Tseng et al.
Filed : May 18, 2010
TC/A.U. : 2892
Examiner : DANG, PHUC T
Docket No. : NAUP0913USA1
Customer No. : 27765

Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

AMENDMENT

Sir:

5 In response to the Office action of January 27, 2011, please amend the
above-identified application as follows:

Amendments to the Specification begin on page 2 of this paper.

Amendments to the Drawings begin on page 3 of this paper.

Remarks/Arguments begin on page 4 of this paper.

10 An **Appendix** including amended drawing figures is attached following page 8 of this
paper.

TSMC Exhibit 1002, Page 164 of 244



FIG. 5

Amendments to the Specification:

Please replace paragraph [0001] with the following amended paragraph:

- 5 [0001] This is a divisional application of U. S. patent application Ser. No. 11/836,772
filed on August 9, 2007, PAT 7,745,847, and the contents of which are included herein
by reference.

10

Please replace paragraph [0023] with the following amended paragraph:

- [0023] As shown in Fig. 5, spacers 228 are formed on the sidewalls of each gate 280.
According to the first preferred embodiment of the present invention, each spacer 228
15 comprises an oxide liner 230 and a nitride spacer 232. The spacers 228 cover the
sidewalls of each gate 208 and also extend laterally onto the first ion lightly doped
region 222 and the second ion lightly doped region 224. Each spacer 228 may also
comprise an offset spacer (not shown) positioned between the gate 208 and the oxide
liner 230. Because each spacer 228 in the first conductive transistor area 202 lies over
20 the raised epitaxial layer 220, thus each spacer 228 in the first conductive transistor
area 202 is tilted upward and a contact surface 350 of the epitaxial layer 220 and the
spacer 228 is above the surface of the semiconductor substrate 200. Please refer to Fig.
10, which is a transmission electron microscopy (TEM) picture of the MOS transistors
in accordance with the first preferred embodiment of the present invention.

25

Electronic Acknowledgement Receipt	
EFS ID:	9953911
Application Number:	12781826
International Application Number:	
Confirmation Number:	3483
Title of Invention:	Method of fabricating metal oxide semiconductor transistor
First Named Inventor/Applicant Name:	Chu-Yin Tseng
Customer Number:	27765
Filer:	Winston Hsu/Connie Chen
Filer Authorized By:	Winston Hsu
Attorney Docket Number:	NAUP0913USA1
Receipt Date:	27-APR-2011
Filing Date:	18-MAY-2010
Time Stamp:	03:44:20
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Applicant Arguments/Remarks Made in an Amendment	1105618.PDF	339298 71fa44e634f5130fd8b93d9ea885b7aec983961	no	6

Warnings:

Information:

2	Amendment/Req. Reconsideration-After Non-Final Reject	1105617.PDF	74863 0d9c9d163f4aa5f322b4c371f8096dcc96fb 5554	no	1
Warnings:					
Information:					
3	Drawings-only black and white line drawings	1105616.PDF	68077 71eeaf681ca8d812e063732ae8e4c236d6d 68b6e	no	1
Warnings:					
Information:					
4	Specification	1105615.PDF	75461 6d78155c944840d1a3ddfd3e8572b2b68fdd c35e8	no	1
Warnings:					
Information:					
Total Files Size (in bytes):			557699		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					

Amendments to the Drawings:

The attached sheet of drawings includes changes to Fig. 5. This sheet, which includes Fig. 5, replaces the original sheet including Fig. 5. In Fig. 5, a contact
5 surface 350 between the epitaxial layer 220 and the spacer 228 is shown.

Attachment: Replacement Sheet 1 page(s)

REMARKS/ARGUMENTS

Objection of the drawings.

5 Fig. 5 has been amended to show a contact surface between the epitaxial layer in the recess and the spacer on the sidewall of the gate is above the surface of the semiconductor substrate as claimed in claims 1 and 9, as requested by the Examiner. Acceptance of the corrected drawings is respectfully requested.

10

Objection of the specification.

Paragraph [0001] of the specification has been amended to insert -- PAT 7,745,847-- after "...August 9, 2007", as requested by the Examiner. Acceptance of the amended
15 specification is respectfully requested.

Rejection of claims 1-3 and 7 under 35 U.S.C. 102(e) as being anticipated by Chen et al (US 7381623).

20

Claim 1 recites a method that specifies after forming an epitaxial layer in the recess, a spacer is formed on the sidewall of the gate and on a portion of the epitaxial layer such that a contact surface of the epitaxial layer and the spacer is above the surface of the semiconductor substrate.

25

Chen in Fig. 7 (shown below) of the cited reference recites a step of forming an epitaxial layer 500a/500b and a spacer 720a/720b on the sidewall of the gate. The spacer 720a/720b however is not formed on a portion of the first epitaxial layer 500b/500b, as recited in claim 1 of the present invention. Instead, the spacer
30 720a/720b is specifically sandwiched between the gate 140 and the epitaxial layer

Rejection of claims 9-12, 15 and 20-21 under 35 U.S.C. 103(a) as being unpatentable over Chen in view of Han et al (US 7800182).

Claim 9 recites a method that specifies after forming a first epitaxial layer in the first recess, a spacer is formed on the sidewall of each gate and at least on a portion of the first epitaxial layer such that a contact surface of the first epitaxial layer and the spacer is above the surface of the semiconductor substrate.

5

Similar to the arguments made for claim 1, Chen in Fig. 7 of the cited reference recites a step of forming a first epitaxial layer 500a/500b and a spacer 720a/720b on the sidewall of the gate. The spacer 720a/720b however is not formed on a portion of the first epitaxial layer 500b/500b, as recited in claim 9 of the present invention.

10 Instead, the spacer 720a/720b is specifically sandwiched between the gate 140 and the epitaxial layer 500a/500b.

Moreover, even though a very tiny portion of the spacer 720a/720b formed on top of the silicide 730 is revealed in Fig. 7 of Chen, the fact that the silicide 730 being
15 formed after the spacer (as specified in the specification of Chen) and the spacer being formed between the gate and the epitaxial layer both proves that the spacer 720a/720b could not have been formed on top of the silicide 730.

As the feature of a spacer formed on the sidewall of the gate and on a portion of the
20 epitaxial layer such that a contact surface between the epitaxial layer and the spacer is
above the surface of the semiconductor substrate is clearly absent in Chen's invention, applicants submit that the method of the present invention is patentable over the cited reference. Reconsideration of claim 9 is respectfully requested. As claims 10-12,
15, and 20-21 are dependent upon claim 9, applicants submit that if claim 9 is found
25 allowable, claims 10-12, 15, and 20-21 should additionally be found allowable.

Rejection of claim 4 under 35 U.S.C. 103(a) as being unpatentable over Chen et al (US 7381623).

30

As claim 4 is dependent upon claim 1, applicants submit that if claim 1 is found allowable, claim 4 should additionally be found allowable.

5 **Rejection of claims 5-6 and 8 under 35 U.S.C. 103(a) as being unpatentable over Chen in view of Chien et al (US 6815770).**

As claims 5-6 and 8 are dependent upon claim 1, applicants submit that if claim 1 is found allowable, claims 5-6 and 8 should additionally be found allowable.

10

Rejection of claims 13-14 under 35 U.S.C. 103(a) as being unpatentable over Chen and Han in view of Chien et al (US 6815770).

15 AS claims 13-14 are dependent upon claim 9, applicants submit that if claim 9 is found allowable, claims 13-14 should additionally be found allowable.

20 Recognizing that Internet communications are not secure, I hereby authorize the USPTO to communicate with me concerning any subject matter of this application by electronic mail. I understand that a copy of these communications will be made of record in the application file.

25 Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Appl. No. 12/781,826
Reply to Office action of January 27, 2011

Sincerely yours,

/Scott Margo/

Date: 04/26/2011

Scott Margo, Patent Agent No. 56,277

5 P.O. BOX 506, Merrifield, VA 22116, U.S.A.

Voice Mail: 302-729-1562

Facsimile: 806-498-6673

e-mail : ScottMargo@naipo.com

10 Note: Please leave a message in my voice mail if you need to talk to me. (The time in D.C. is 12 hours behind the Taiwan time, i.e. 9 AM in D.C. = 9 PM in Taiwan.)

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875					Application or Docket Number 12/781,826		Filing Date 05/18/2010		☐ To be Mailed				
APPLICATION AS FILED – PART I													
(Column 1)			(Column 2)			SMALL ENTITY ☐ OR		OTHER THAN SMALL ENTITY					
FOR	NUMBER FILED	NUMBER EXTRA	RATE (\$)	FEE (\$)	OR		RATE (\$)	FEE (\$)					
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A		OR		N/A						
☐ SEARCH FEE (37 CFR 1.16(k), (j), or (m))	N/A	N/A	N/A		OR		N/A						
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A		OR		N/A						
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X \$ =		OR		X \$ =						
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X \$ =		OR		X \$ =						
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))			If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$250 (\$125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).										
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))													
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL		OR		TOTAL						
APPLICATION AS AMENDED – PART II													
(Column 1)			(Column 2)			SMALL ENTITY		OR		OTHER THAN SMALL ENTITY			
AMENDMENT	04/27/2011	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	OR		RATE (\$)	ADDITIONAL FEE (\$)		
	Total (37 CFR 1.16(i))	* 21	Minus	** 21	= 0	X \$ =		OR		X \$52=	0		
	Independent (37 CFR 1.16(h))	* 2	Minus	***3	= 0	X \$ =		OR		X \$220=	0		
	☐ Application Size Fee (37 CFR 1.16(s))							OR					
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR					
						TOTAL ADD'L FEE		OR		TOTAL ADD'L FEE	0		
(Column 1)			(Column 2)			(Column 3)		SMALL ENTITY		OR		OTHER THAN SMALL ENTITY	
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	OR		RATE (\$)	ADDITIONAL FEE (\$)		
	Total (37 CFR 1.16(i))	*	Minus	**	=	X \$ =		OR		X \$ =			
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X \$ =		OR		X \$ =			
	☐ Application Size Fee (37 CFR 1.16(s))							OR					
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR					
						TOTAL ADD'L FEE		OR		TOTAL ADD'L FEE			
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.													

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/781,826	05/18/2010	Chu-Yin Tseng	NAUP0913USA1	3483
27765 7590 06/15/2011 NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION P.O. BOX 506 MERRIFIELD, VA 22116			EXAMINER DANG, PHUC T	
			ART UNIT 2892	PAPER NUMBER
			NOTIFICATION DATE 06/15/2011	DELIVERY MODE ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

Patent.admin.uspto.Rcv@naipo.com
mis.ap.uspto@naipo.com

Office Action Summary	Application No.	Applicant(s)	
	12/781,826	TSENG ET AL.	
	Examiner	Art Unit	
	PHUC DANG	2892	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on amendment filed on 04/27/2011.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-21 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-15, 20 and 21 is/are rejected.
- 7) ☒ Claim(s) 16-19 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 18 May 2010 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) ☒ Notice of References Cited (PTO-892) | 4) ☐ Interview Summary (PTO-413) |
| 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date: _____ |
| 3) ☒ Information Disclosure Statement(s) (PTO/SB/08) | 5) ☐ Notice of Informal Patent Application |
| Paper No(s)/Mail Date <u>03/31/2011</u> | 6) ☐ Other: _____ |

DETAILED ACTION

1. This application is a CON of 11/836,772 08/09/2007 PAT 7,745,847.

Response to Arguments

2. Applicant's arguments with respect to claims 1-21 have been considered but are moot in view of the new ground(s) of rejection.

Information Disclosure Statement

3. The office acknowledges receipt of the following items from the applicant:

Information Disclosure Statement (IDS) filed on 03/31/2011.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 1-4 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al., hereafter "Chen" (U.S. Patent No. 7,381,623 B1) in view of Zhang et al., hereafter "Zhang" (U.S. Publication No. 2008/0203449 A1).

Regarding claims 1-3, Chen discloses a method of fabricating a MOS transistor, comprising:

providing a semiconductor substrate (110);

forming at least a gate (140) on the semiconductor substrate;

forming a protective layer (160) on the semiconductor substrate, and the protective layer covering the surface of the gate;

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forming at least a recess (400a) within the semiconductor substrate adjacent to the gate;

forming an epitaxial layer (500a/500b) in the recess, wherein the top surface of the epitaxial layer is above the surface of the semiconductor substrate (Figs. 1-6).

Chen discloses the features of the claimed invention as discussed above, but does not forming a spacer on the sidewall of the gate and on a portion of the epitaxial layer, wherein a contact surface of the epitaxial layer and the spacer is above the surface of the semiconductor substrate.

Zhang, however, discloses forming a spacer (40) on the sidewall of the gate (22) and on a portion of the epitaxial layer (36), wherein a contact surface of the epitaxial layer (36) and the spacer (40) is above the surface of the semiconductor substrate (12) (e.g. fig. 6).

It would have been obvious to one having ordinary skilled in the art at the time the invention was made to modify the teaching of Chen to form a spacer on the sidewall of the gate and on a portion of the epitaxial layer, wherein a contact surface of the epitaxial layer and the spacer is above the surface of the semiconductor substrate as taught by Zhang for a purpose of improving the carrier mobility of the transistor.

Regarding claim 4, Chen does not disclose the protective layer has a thickness of about 150 to 250 angstroms. However, the selection of the claimed process parameters would have been obvious to one having ordinary skill in the art at the time the invention was made to form the thickness of the protective layer within the claimed range, since it is well settle that when the general conditions of a claim are discloses in the prior art,

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discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding claim 7, Chen discloses further comprising a step of forming a source/drain region (700a/710a) within the semiconductor substrate adjacent to the gate after forming the spacer (220b) (Fig. 7).

5. Claims 9-12, 15 and 20-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen and Zhang in view of Han et al., hereafter “Han” (U.S. Patent No. 7,800,182 B2).

Regarding claims 9-11 and 15, Chen discloses a method of fabricating a CMOS transistor, comprising:

providing a semiconductor substrate (110) having at least a first conductive transistor area (12) for fabricating first conductive transistors and at least a second conductive transistor area (130) for fabricating second conductive transistors;

forming a gate (140) on the first conductive transistor area and on the second conductive transistor area respectively;

forming a first protective layer (160) on the semiconductor substrate, and the first protective layer covering the surface of each gate;

forming at least a first recess (400a) within the semiconductor substrate adjacent to the gate in the first conductive transistor area;

forming a first epitaxial layer (500a/500b) in the first recess, wherein the top surface of the first epitaxial layer is above the surface of the semiconductor substrate (Figs. 1-6).

Chen discloses the features of the claimed invention as discussed above, but does not forming a spacer on the sidewall of each gate and at least on a portion of the first

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epitaxial layer, wherein a contact surface of the first epitaxial layer and the spacer is above the surface of the semiconductor substrate.

Zhang, however, discloses forming a spacer (40) on the sidewall of each gate (22) and on a portion of the first epitaxial layer (36), wherein a contact surface of the first epitaxial layer (36) and the spacer (40) is above the surface of the semiconductor substrate (12) (e.g. fig. 6).

It would have been obvious to one having ordinary skilled in the art at the time the invention was made to modify the teaching of Chen to form a spacer on the sidewall of each gate and on a portion of the first epitaxial layer, wherein a contact surface of the first epitaxial layer and the spacer is above the surface of the semiconductor substrate as taught by Zhang for a purpose of improving the carrier mobility of the transistor.

Chen and Zhang discloses the features of the claimed invention as discussed above, but does not disclose an isolation structure between the first conductive transistor area and the second conductive transistor area.

However, Han, in the same field of endeavor, discloses an isolation (38) between the first conductive transistor area (31) and the second conductive transistor area (32) (Fig. 1).

It would have been obvious to one having ordinary skilled in the art at the time the invention was made to modify the teaching of Chen and Zhang to form an isolation structure between the first conductive transistor area and the second conductive transistor area as taught by Han for a purpose of defining the boundaries of their diffusion regions.

Regarding claim 12, Chen does not disclose the first protective layer has a thickness of about 150 to 250 angstroms. However, the selection of the claimed process parameters

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would have been obvious to one having ordinary skill in the art at the time the invention was made to form the thickness of the first protective layer within the claimed range, since it is well settled that when the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In *re Aller*, 105 USPQ 233.

Regarding claims 20-21, Chen does not disclose wherein the first conductive transistors comprise PMOS transistors and the first conductive transistors comprise PMOS transistors and vice-versa.

It would have been an obvious matter of the design choice to modify the MOS transistor comprises PMOS and NMOS in order to improve the performance of the MOS transistor, since it has been held to be within the general skill of the worker in the art to select any type of the transistor on the basis of its suitability for the intended use as a matter of obvious design choice. In *re Leshin*, 125 USPQ 416.

6. Claims 5-6 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen and Zhang in view of Chien et al., hereafter “Chien” (U.S. Patent No. 6,815,770 B1).

Regarding claims 5-6, Chen and Zhang discloses the features of the claimed invention as discussed above, but does not disclose wherein the spacer further comprises an offset spacer, positioned between the gate and the spacer, wherein the spacer further comprises an oxide liner and a nitride spacer.

However, Chien, in the same field of endeavor, discloses the spacer further comprises an offset spacer, positioned between the gate and the spacer, wherein the spacer further comprises an oxide liner and a nitride spacer (Fig. 1).

It would have been obvious to one having ordinary skilled in the art at the time the invention was made to modify the teaching of Chen and Zhang to form the spacer further comprises an offset spacer, positioned between the gate and the spacer, wherein the spacer further comprises an oxide liner and a nitride spacer as taught by Chien for a purpose of controlling the step of doping.

Regarding claim 8, Chen and Zhang discloses the features of the claimed invention as discussed above, but does not disclose further comprising a lightly doped drain disposed in the semiconductor substrate adjacent to the gate.

However, Chien, in the same field of endeavor, discloses further comprising a lightly doped drain disposed in the semiconductor substrate adjacent to the gate (Figs. 1 & 4 and Abstract).

It would have been obvious to one having ordinary skilled in the art at the time the invention was made to modify the teaching of Chen and Zhang to form a lightly doped drain disposed in the semiconductor substrate adjacent to the gate as taught by Chien for a purpose of improving the performance of the MOS transistor.

7. Claims 13-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen, Zhang and Han in view of Chien et al., hereafter "Chien" (U.S. Patent No. 6,815,770 B1).

Regarding claims 13-14, claims 13-14 are rejected similar to claims 5-6 above.

Allowable Subject Matter

8. The following is a statement of reason for the indication of allowable subject matter:

Claims 16-19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

None of the prior art of records disclose after removing the first protective layer, the method further comprising forming a second protective layer on the semiconductor substrate, and the second protective layer covering the surface of each gate; forming at least a second recess within the semiconductor substrate adjacent to the gate in the second conductive transistor area; forming a second epitaxial layer in the second recess; removing the second protective layer; and forming a second ion lightly doped region within the semiconductor substrate adjacent to the gate in the second conductive transistor area before forming the spacer as cited in claim 16 and after forming the first epitaxial layer, the method further comprising forming at least a second recess within the semiconductor substrate adjacent to the gate in the second conductive transistor area; forming a second epitaxial layer in the second recess; removing the first protective layer; and forming a second ion lightly doped region within the semiconductor substrate adjacent to the gate in the second conductive transistor area before forming the spacer as cited in claim 19.

Claims 17-18 are directly or indirectly depend on claim 16, then, they also would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phuc T. Dang whose telephone number is 571-272-1776. The examiner can normally be reached on 8:00 am-5:00 pm.
10. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thao X. Le can be reached on (571) 272-1708. The fax phone numbers for

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the organization where this application or proceeding is assigned are 703-872-9306 for regular communications and Final communications.

11. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

/Phuc T Dang/

Primary Examiner, Art Unit 2892

Notice of References Cited	Application/Control No. 12/781,826		Applicant(s)/Patent Under Reexamination TSENG ET AL.	
	Examiner PHUC DANG		Art Unit 2892	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-2008/0203449 A1	08-2008	Zhang et al.	257/288
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	2	"7381623".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/05/18 18:56
L2	1	"12781826"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/05/18 19:02
L3	1	2 and spacer with epitaxial	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/05/18 19:03
L4	1452	(spacer) with (epi epitaxial \$2) near (layer)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/05/18 19:10
L5	36964	438/229-300.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/05/18 19:10
L6	342	4 and 5	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/05/18 19:10
L7	235	6 and @ad<="20070809"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/05/18 19:11

L8	90	7 and recess\$2	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/05/18 19:13
L9	7946	(epi epitaxial) with (above) with (substrate)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/05/18 19:17
L10	289	4 and 9	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/05/18 19:18
L11	129	10 and recess\$2	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/05/18 19:18
L12	74	11 and @ad<="20070809"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/05/18 19:18
L13	3183	257/190-192.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/05/18 19:31
L14	73	4 and 13	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/05/18 19:31
L15	57	14 and @ad<="20070809"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/05/18 19:31

L16	1572	257/197.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/05/18 19:35
L17	28	4 and 16	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/05/18 19:35
L18	25	17 and @ad<="20070809"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/05/18 19:35
L19	3	"20060211245"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/05/18 19:38

EAST Search History (Interference)

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5/ 18/ 2011 7:40:51 PM**C:\ Documents and Settings\ PDang1\ My Documents\ EAST\ Workspaces\ 12781826.wsp**

Search Notes 	Application/Control No. 12781826	Applicant(s)/Patent Under Reexamination TSENG ET AL.
	Examiner Phuc T Dang	Art Unit 2892

SEARCHED			
Class	Subclass	Date	Examiner
438	229,300	01/21/2011	PD
257	19,190,192,197,E21.437	01/21/2011	PD

SEARCH NOTES		
Search Notes	Date	Examiner
INVENTOR SEARCH	01/21/2011	PD
EAST SEARCH	01/21/2011	PD
EAST SEARCH (Updated)	06/06/2011	PD

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner

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<i>Index of Claims</i> 	Application/Control No. 12781826	Applicant(s)/Patent Under Reexamination TSENG ET AL.
	Examiner Phuc T Dang	Art Unit 2892

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant				☐ CPA		☐ T.D.		☐ R.1.47	
CLAIM		DATE							
Final	Original	01/21/2011	06/06/2011						
	1	✓	✓						
	2	✓	✓						
	3	✓	✓						
	4	✓	✓						
	5	✓	✓						
	6	✓	✓						
	7	✓	✓						
	8	✓	✓						
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	11	✓	✓						
	12	✓	✓						
	13	✓	✓						
	14	✓	✓						
	15	✓	✓						
	16	O	O						
	17	O	O						
	18	O	O						
	19	O	O						
	20	✓	✓						
	21	✓	✓						

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	1586	(spacer) with (gate) with (epi epitaxial\$2)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/05/19 09:37
L2	1217	1 and @ad<="20070809"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/05/19 09:38
L3	506	(spacer) adj15 (gate) adj15 (epi epitaxial\$2)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/05/19 09:39
L4	368	3 and @ad<="20070809"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/05/19 09:39
L5	551	(sidewall\$1 side-wall\$1) adj15 (gate) adj15 (epi epitaxial\$2)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/05/19 10:03
L6	403	5 and @ad<="20070809"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/05/19 10:03
L7	5	"7381623"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/05/19 10:05

L8	3	7 and "160"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/05/19 10:06
L9	10	"7800182".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/05/19 10:08
L10	2	"6815770".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/05/19 10:10
L11	3	"20080203449"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/05/19 10:11

EAST Search History (I nterference)

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5/ 19/ 2011 10:14:43 AM**C:\ Documents and Settings\ PDang1\ My Documents\ EAST\ Workspaces\ 12781826.wsp**

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	12781826
	Filing Date	2010-05-18
	First Named Inventor	Chu-Yin Tseng
	Art Unit	2892
	Examiner Name	DANG, PHUC T
	Attorney Docket Number	NAUP0913USA1

U.S.PATENTS						
Examiner Initial*	Cite No	Patent Number	Kind Code	Issue Date	Name	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					
U.S.PATENT APPLICATION PUBLICATIONS						
Examiner Initial*	Cite No	Publication Number	Kind Code	Publication Date	Name	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
/PD/	1	20060138479	A1	2006-06-29	Ngo	
	2	20040142545	A1	2004-07-22	Ngo	
	3	20040232513	A1	2004-11-25	Chi	
	4	20060024879	A1	2006-02-02	Fu	
/PD/	5	20060134873	A1	2006-06-22	Koontz	

Receipt date: 03/31/2011

12781826 - GAU: 2892

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	12781826
	Filing Date	2010-05-18
	First Named Inventor	Chu-Yin Tseng
	Art Unit	2892
	Examiner Name	DANG, PHUC T
	Attorney Docket Number	NAUP0913USA1

/PD/	6	20060226483	A1	2006-10-12	Lo	
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FOREIGN PATENT DOCUMENTS

Examiner Initial*	Cite No	Foreign Document Number	Country Code	Kind Code	Publication Date	Name	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear	
/PD/	1	200509310	TW		2005-03-01			Abstract
/PD/	2	200636996	TW		2006-10-16			Abstract

NON-PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	
	1		

EXAMINER SIGNATURE

Examiner Signature	/Phuc Dang/	Date Considered	06/06/2011
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Method of fabricating metal oxide semiconductor transistor

Appl. No. : 12/781,826 Confirmation No. 3483
Applicant : Chu-Yin Tseng et al.
Filed : May 18, 2010
TC/A.U. : 2892
Examiner : DANG, PHUC T
Docket No. : NAUP0913USA1
Customer No. : 27765

Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

AMENDMENT

Sir:

5 In response to the Office action of June 15, 2011, please amend the above-identified application as follows:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks/Arguments begin on page 6 of this paper.

Amendments to the Claims:

The listing of claims will replace all prior versions and listings of claims in the application:

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Listing of Claims:

1. (original) A method of fabricating a MOS transistor, comprising:
 - providing a semiconductor substrate;
 - 10 forming at least a gate on the semiconductor substrate;
 - forming a protective layer on the semiconductor substrate, and the protective layer covering the surface of the gate;
 - forming at least a recess within the semiconductor substrate adjacent to the gate;
 - forming an epitaxial layer in the recess, wherein the top surface of the epitaxial
 - 15 layer is above the surface of the semiconductor substrate; and
 - forming a spacer on the sidewall of the gate and on a portion of the epitaxial layer, wherein a contact surface of the epitaxial layer and the spacer is above the surface of the semiconductor substrate.
- 20 2. (original) The method of claim 1, further comprising a step of removing the protective layer after forming the epitaxial layer in the recess.
3. (original) The method of claim 1, wherein the protective layer comprises silicon nitride.
- 25 4. (original) The method of claim 3, wherein the protective layer has a thickness of about 150 to 250 angstroms.
5. (original) The method of claim 1, wherein the spacer further comprises an oxide
- 30 liner and a nitride spacer.

6. (original) The method of claim 1, wherein the spacer further comprises an offset spacer, positioned between the gate and the spacer.
- 5 7. (original) The method of claim 1, further comprising a step of forming a source/drain region within the semiconductor substrate adjacent to the gate after forming the spacer.
8. (original) The method of claim 1, further comprising a step of forming a lightly
10 doped region within the semiconductor substrate adjacent to the gate.
9. (original) A method of fabricating a CMOS transistor, comprising:
providing a semiconductor substrate having at least a first conductive transistor area for fabricating first conductive transistors and at least a second conductive
15 transistor area for fabricating second conductive transistors, and an isolation structure between the first conductive transistor area and the second conductive transistor area;
forming a gate on the first conductive transistor area and on the second conductive transistor area respectively;
forming a first protective layer on the semiconductor substrate, and the first
20 protective layer covering the surface of each gate;
forming at least a first recess within the semiconductor substrate adjacent to the gate in the first conductive transistor area;
forming a first epitaxial layer in the first recess, wherein the top surface of the first epitaxial layer is above the surface of the semiconductor substrate; and
25 forming a spacer on the sidewall of each gate and at least on a portion of the first epitaxial layer, wherein a contact surface of the first epitaxial layer and the spacer is above the surface of the semiconductor substrate.
10. (original) The method of claim 9, further comprising a step of forming a first ion
30 lightly doped region within the semiconductor substrate adjacent to the gate in the first

conductive transistor area.

11. (original) The method of claim 9, wherein the first protective layer comprises silicon nitride.

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12. (original) The method of claim 9, wherein the first protective layer has a thickness of about 150 to 250 angstroms.

13. (original) The method of claim 9, wherein each spacer further comprises an oxide
10 liner and a nitride spacer.

14. (original) The method of claim 9, wherein each spacer further comprises an offset spacer, positioned between each gate and each spacer.

15 15. (original) The method of claim 9, further comprising a step of removing the first protective layer after forming the first epitaxial layer in the first recess.

16. (original) The method of claim 15, after removing the first protective layer, the method further comprising:

20 forming a second protective layer on the semiconductor substrate, and the second protective layer covering the surface of each gate;

forming at least a second recess within the semiconductor substrate adjacent to the gate in the second conductive transistor area;

forming a second epitaxial layer in the second recess;

25 removing the second protective layer; and

forming a second ion lightly doped region within the semiconductor substrate adjacent to the gate in the second conductive transistor area before forming the spacer.

17. (original) The method of claim 16, wherein the second protective layer comprises
30 silicon nitride.

18. (original) The method of claim 17, wherein the second protective layer has a thickness of about 150 to 250 angstroms.

5 19. (original) The method of claim 9, after forming the first epitaxial layer, the method further comprising:

forming at least a second recess within the semiconductor substrate adjacent to the gate in the second conductive transistor area;

forming a second epitaxial layer in the second recess;

10 removing the first protective layer; and

forming a second ion lightly doped region within the semiconductor substrate adjacent to the gate in the second conductive transistor area before forming the spacer.

20. (original) The method of claim 9, wherein the first conductive transistors comprise
15 PMOS transistors and the second conductive transistors comprise NMOS transistors.

21. (original) The method of claim 9, wherein the first conductive transistors comprise NMOS transistors and the second conductive transistors comprise PMOS transistors.

20 22. (new) The method of claim 1, further comprising:

forming a lightly doped region in the semiconductor substrate adjacent to the gate after forming the epitaxial layer;

forming the spacer on the sidewall of the gate and on the portion of the epitaxial layer after forming the lightly doped region; and

25 forming a source/drain region in the semiconductor substrate adjacent to the spacer.

BEFORE THE UNITED STATES PATENT AND TRADEMARK OFFICE

Swear Back declaration under 37 CFR 1.131 in the Matter of U.S. Patent Application No. 12/781,826

I, as an authorized legal representative of the undersigned assignee for U.S. Patent Application No. **12/781,826**, depose and do solemnly swear:

1. The attached Invention Disclosure document is an accurate and unaltered copy of a United Microelectronics Corporation internal Invention Disclosure document UMCD-2007-0007.
2. Said General-Purpose Report is accurately dated as December 29, 2006, proving date of invention to be at least as early as December 29, 2006.
3. Due diligence was practiced in subsequently filing a U.S. Patent Application comprising inventive concepts first disclosed in said General-Purpose Report on February 28, 2007 as U.S. Patent Application No. 12/781,826.
4. All acts relied upon to establish the date prior to the reference or activity were carried out in the United States or in a NAFTA country or WTO member country. In this regard, all acts and actions set forth above were carried out in the country of Taiwan (also known as "Chinese Taipei" by the World Trade Organization), which became a WTO member country in January 2002.
5. As one of the inventors signing below:
I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under § 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

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Attachment

System Use Field

Application Use Field

UMC

Invention Disclosure

Version : 2006.05

Case Type : ☐ AI ☐ CI
☒ BI ☐ PI

☐ X級

Strategy Case

Inventor Response Deadline :
 2007/04/12

Invention Disclosure No.	UMCD-2007-0007
Submission Date:	2006/12/29
Patent Appl. Country	US ; Taiwan(發明)
	☐ 將群 ☒ 北美 ☐ 博拓 ☐ 三達 ☐ UMC ☐ Other
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Spec. Reviewer(規格書審閱人):	☐ Inventor1 ☐ Inventor2 ☐ Inventor3 ☐ Inventor4 ☐ Inventor5 ☐ Inventor6
說明: 本系統頂設規格書會簽者為	☐ Inventor7 ☐ Inventor8 ☐ Inventor9 ☐ Inventor10 ☒ Author ☐ Other
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審查會議, 新案面談, 提供PS撰稿所需	
之技術細節及校稿), 可指定由其他發明	
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 Employee ?

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 Dept. *
 Official Tel. *
 E-Mail Address *

Bank Information :
 (Please provide the bank account which your compensation is entered into.)
 Bank Name
 Bank Branch
 Bank Account No.
 Attach files.

SDataFromSQL ☐ Yes ☐ No

Update Inventors' Information by IPR
 Update Date Request Link and Comment
 2006/12/29

Invention Classification (Only for IPR Engineer)

By Product :	All
By Module :	PEI
By Process Flow :	FEOL / S/D
Key Words :	Others; SiGe; Cap Layer; S/D; LDD; Spacer Please specify : RECSS ;EPI
Key Project :	Is Key Project : ☒ Yes ☐ No StrainedSi / SiGe
Committee Member :	☐ 竹科 ☐ 南科 ☐ FinFET ☐ TSV

☐ DF
 ☐ TF
 ☐ ET
 ☐ LT
 ☐ Integration
 ☐ Circuit

Same Classification Search :

Invention Dept
 UMC * CRD_Logid45NM_2/INT2 <System Calculate>

1). Invention Title * 説明
 New approach for SiGe

2). Background (please attach drawing 説明)
 a). What is the current approach? *
 1.The growth technology of SiGe material can provide higher carrier mobility in strained P-channel as compares with bulk Si. The current approach is LDD->SP2->S/D->SiGe. As for we suffer some issues at present that 1.distance to gate is on pattern dependency 2.USJ is difficult to be implemented. 3.STI oxide loss is too deep.

b). The problem this invention trying to resolve *
 1.Pattern dependent on recess etch
 2.STI oxide loss

3). Invention 説明
 a). Detailed description of the invention *

Step1: Poly->capoxide200A

Step2: EPI photo

Step3: Si recess
Concern oxide thk for poly pump defect)

Step4: SiGe growth

Step5: LDD->SP2->S/D

b). Please attach exp. data & plot

c). Please specify possible application of this invention?

4). Reference 説明
 a). Please provide information related to the problem or this invention (Paper, Patent, Document)

5). Have you performed any prior art (including any earlier similar patent, paper & publications) search? What is your search result? * 說明

☐ Yes ☒ No

a). Search key word(ex: metal gate or high-k) :

b). Review article number :

patent :

paper :

others :

c). Search Result(ex:292 patents are found) :

6). Have you co-work this invention with any Non-UMC parties (companies or organizations)? * 說明

☐ Yes ☒ No

Contract Number :

Contract Title :

Party Name :

(Customer Name)

7). Please answer the following question, and provide your comments

Has the invention been applied in mass production

within a year? (已量產或一年內量產) *

☒ Yes ☐ No

Please attach your files here: (For Inventor Only)

Attachment :



Format : New invention disclosure_format.ppt

IPLA review comment

1) 發明之策略目標/方向

1-1). 此發明是否符合公司之策略目標/方向

☐ Yes ☐ No

1-2). 此發明之策略目標/方向(可複選):

☐ 保護公司技術/創新發明

☐ 延阻競爭對手

☐ 增加授權談判籌碼

☐ 其他

2). 專利性

2-1)實用性(UMC 及半導體業界, 現在或將來是否會使用該發明;該發明是否為公司本業)

☐ Yes ☐ No

2-2).新穎性(UMC 及業界公開之資訊查無相關專利前案, 論文或相關資訊未公開過或業界尚無人使用)

☐ Yes ☐ No

2-3).進步性(發明是否為將已知事物組合, 且該組合為一般習知技藝人士所顯而易知者, 且發明較目前 UMC 及業界正在使用的裝置, 方法及設計是否更快, 更好, 更省時, 更省錢, 更省電, 步驟更少.)

☐ Yes ☐ No

2-4).舉證性(確認發明本身是否容易進行舉證以方便行使專利權, 若不易舉證但改善效果極佳, 是否列為營業機密更能保障公司權益)

☐ Yes (易舉證) ☐ No (不易舉證)

2-5). 迴避性(發明雖查無前案, 應查其作法是否輕易為他人進行迴避設計, 或找到其它更有效的方法)

- ☐ Yes (易迴避) ☐ No (不易迴避)
3). IPLA comment

Please attach prior art files here (published documents if possible and named as US/234567 or US20120123456)(For IPLA Engineer Only)
Invention feature :

Prior art: ☒ Yes ☐ No (text and attachment)

曾朱吟
12390
CRD_LogiC/45NM_2/INT2
Ju Ying Tseng
2007/03/28 07:58 PM

Dear sir:

1. for distance to gate is on pattern dependency. Si recess will make unstable etch depth with SP2 for different pitch. New SiGe process can improve it.
2. USJ is difficult to be implemented. The thermal effect of EPI will induce deeper USJ. New SiGe process can avoid this condition.
3. STI oxide loss is too deep. Si recess etch deeper with SP2 induce high STI oxide loss. Stable Si recess make STI oxide loss lower for new scheme.

Comparison & suggestion :

Additional Remark for Provisional Case Review: (For IPLA Engineer Only)

Attachment :

Questionnaires after prior search

Questionnaires after NID committee review

IPLA/LA Review

Section Manager Review

Department Manager Review

Committee Review

Provisional Case -- IPR Engineer Review

Current Approvers

Approve History

2006/12/29 11:23 Draft : CRD_LogiC/45NM_2/INT2 曾朱吟(Ju Ying Tseng/UMC) submit for further review
2006/12/29 11:27 IPRWindowReview : IPR/PP 許慧如 (Betty Hsu/UMC) Reject Comments:

>>as author request

2006/12/29 15:06 Draft : CRD_LogiC/45NM_2/INT2 曾朱吟(Ju Ying Tseng/UMC) submit for further review
2006/12/31 14:41 IPRWindowReview : IPR/PP 許慧如 (Betty Hsu/UMC) Agree. Comments:

>>ok!

2007/01/03 09:45 DeptManagerReview : CRD_LogiC/45NM_2/INT2 徐世杰 (Steven Hsu/UMC) review. Comments in Review Sheet : better device variation control

2007/01/03 09:45 DeptManagerReview : CRD_LogiC/45NM_2/INT2 徐世杰(Steven Hsu/UMC) send to IPR/PP 許慧如(Betty Hsu/UMC) for further review.

2007/01/03 15:20 IPRIspatch : IPR/PP 許慧如(Betty Hsu/UMC) send to CRD_LogiC/45NM_2 盛義忠(Y C Sheng/UMC) for further review.

2007/01/03 15:20 IPRIspatch : IPR/PP Betty Hsu/UMC(許慧如) send to committee member review manually.

2007/01/03 15:53 CommitteeMemberReview : CRD_LogiC/45NM_2 盛義忠 (Y C Sheng/UMC) review. Comments in Review Sheet : It's better than current SiGe baseline inters of process control

2007/01/04 14:13 IPRIspatch : IPR/PP 許慧如 (Betty Hsu/UMC) dispatched an IPR review engineer.. Comments: >>ok!

2007/01/09 08:51 IPRIReview : IPR/PF 劉志建(C C Liu/UMC) reassign an IPR review engineer N S Shen/UMC, and without comment

2007/03/29 12:54 IPRIReview : IPR/PF 沈能興 (N S Shen/UMC) review. Comments in Review Sheet:

J Y : AFTER 3/29 review meeting, committee command to take a patent protection for this case, Tahniks! IPR/PF NS

2007/03/30 09:31 IPRIAssignPatentEng : IPR/PF 劉志建 (C C Liu/UMC) assign Duncan Peng/UMC, and without comment

2007/04/02 09:14 IPRIAssignAgent : IPR/PP 賴仰乾(Joey Lai/UMC) assign a patent agent, and without comment

2007/04/20 09:30 PatentDrafting : IPR/PF 彭翔鴻(Duncan Peng/UMC) creates a drafting document. Invention Disclosure cosign completed.

DataUpdate

Merge Case

SystemAdmin

Electronic Patent Application Fee Transmittal				
Application Number:		12781826		
Filing Date:		18-May-2010		
Title of Invention:		Method of fabricating metal oxide semiconductor transistor		
First Named Inventor/Applicant Name:		Chu-Yin Tseng		
Filer:		Winston Hsu/Lauren Chang		
Attorney Docket Number:		NAUP0913USA1		
Filed as Large Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Claims in excess of 20	1202	1	52	52
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Miscellaneous:				
Total in USD (\$)				52

Electronic Acknowledgement Receipt	
EFS ID:	10952342
Application Number:	12781826
International Application Number:	
Confirmation Number:	3483
Title of Invention:	Method of fabricating metal oxide semiconductor transistor
First Named Inventor/Applicant Name:	Chu-Yin Tseng
Customer Number:	27765
Filer:	Winston Hsu/Lauren Chang
Filer Authorized By:	Winston Hsu
Attorney Docket Number:	NAUP0913USA1
Receipt Date:	15-SEP-2011
Filing Date:	18-MAY-2010
Time Stamp:	22:28:42
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	\$ 52
RAM confirmation Number	6754
Deposit Account	503105
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees) Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)	

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)					
Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees)					
Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)					
File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Applicant Arguments/Remarks Made in an Amendment	1204128.PDF	324527	no	3
			6ea8c76db96707fe763f9e26a317cb96ca85dc7c		
Warnings:					
Information:					
2	Amendment/Req. Reconsideration-After Non-Final Reject	1204127.PDF	76201	no	1
			c04671007a3d4cc8d226e91fd83acd50485deef9		
Warnings:					
Information:					
3	Claims	1204126.PDF	82065	no	4
			91225f990b37441d53f6de917e5d401c37e049c		
Warnings:					
Information:					
4	Rule 130, 131 or 132 Affidavits	NAUP0913USA1_A2_2_NP070.pdf	2876407	no	19
			075f986cbffc2effdd7761e554f6e204d9cfeb6		
Warnings:					
Information:					
5	Fee Worksheet (SB06)	fee-info.pdf	29894	no	2
			f57f89dbb34e776041003fc3a736ff23c4cd4aae		
Warnings:					
Information:					
Total Files Size (in bytes):			3389094		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

REMARKS/ARGUMENTS

Reconsideration of the instant application and favorable action are solicited. Claims 1-21 are rejected.

5

**SWEAR BACK AFFIDAVIT UNDER 37 CFR 1.131 IN THE MATTER OF U.S.
PATENT APPLICATION NO. 12/781,826**

10 The applicants respectfully submit a Swear Back Affidavit under 37 C.F.R. 1.131 in the matter of U.S. patent application no. 12/781,826 along with the Invention Disclosure made by the applicants to prove the reduction of practice of this application is prior to the filing date of the cited reference (US 2008/0203449).

15 This invention was made in Taiwan and Taiwan is a member of WTO (World Trade Organization) since 2002.

The Invention Disclosure provided plainly shows that the inventive concepts were first disclosed in said Invention Disclosure **no later than 12/29/2006**, which is earlier than the filing date of US 2008/0203449 (2/28/2007).

20

Regarding diligence between the completion date of the invention disclosure and the filing date of 8/9/2007 of the parent application (U.S. patent application no. 11/836,772), the undersigned representative of the applicants and co-working assistants under his direct supervision, including a draft person, an editor, an electronic filing system operator, etc., were diligent in preparing the instant patent application based on applicants' written description of the invention disclosure and diligent in filing the finalized draft of the instant patent application reviewed and confirmed by the applicants.

30 In conclusion, the prior art U.S. Patent Application US 2008/0203449 (Zhang) is

NO longer a qualified document as the basis for the 103 rejection of the present application.

5 **103 REJECTIONS OVER CLAIMS 1-21**

The applicants have submitted the Swear Back Affidavit along with other corresponding evidence showing that the prior art US 2008/0203449 is NO longer a qualified document as the basis for the 103 rejection of the present application.

10 Accordingly, the other cited document, i.e. US 7381623 **alone**, is no longer a complete document as the basis for the 103 rejection of the present application. Therefore, the applicants respectfully request the rejection over claims 1-21 be withdrawn.

15

New Claim

Dependent claim 22 has been added to describe an embodiment of the present invention.

With regards to patentability, applicants submit that claim 22 is patentable over the

20 Examiner's cited reference. No new or additional matter is added in the above claim and the claim is fully supported in the original disclosure. In addition, as claim 22 is dependent upon claim 1, applicants submit that if claim 1 is found allowable, claim 22 should additionally be found allowable.

25

Recognizing that Internet communications are not secure, I hereby authorize the USPTO to communicate with me concerning any subject matter of this application by electronic mail. I understand that a copy of these communications will be made of record in the application file.

30

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

5 Sincerely yours,

/Scott Margo/

Date: 09/15/2011

Scott Margo, Patent Agent No. 56,277

P.O. BOX 506, Merrifield, VA 22116, U.S.A.

10 Voice Mail: 302-729-1562

Facsimile: 806-498-6673

e-mail : ScottMargo@naipo.com

Note: Please leave a message in my voice mail if you need to talk to me. (The time in
15 D.C. is 12 hours behind the Taiwan time, i.e. 9 AM in D.C. = 9 PM in Taiwan.)

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875					Application or Docket Number 12/781,826	Filing Date 05/18/2010	☐ To be Mailed
APPLICATION AS FILED – PART I							
(Column 1)		(Column 2)		SMALL ENTITY ☐ OR		OTHER THAN SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE (\$)	FEE (\$)	OR	RATE (\$)	FEE (\$)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (j), or (m))	N/A	N/A	N/A			N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X \$ =		OR	X \$ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X \$ =			X \$ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$250 (\$125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	
APPLICATION AS AMENDED – PART II							
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY OR OTHER THAN SMALL ENTITY	
09/15/2011	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	RATE (\$)
Total (37 CFR 1.16(i))	* 22	Minus	** 21	= 1	X \$ =		OR X \$52=
Independent (37 CFR 1.16(h))	* 2	Minus	***3	= 0	X \$ =		OR X \$220=
☐ Application Size Fee (37 CFR 1.16(s))							
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
					TOTAL ADD'L FEE		OR TOTAL ADD'L FEE
							52
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY OR OTHER THAN SMALL ENTITY	
	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	RATE (\$)
Total (37 CFR 1.16(i))	*	Minus	**	=	X \$ =		OR X \$ =
Independent (37 CFR 1.16(h))	*	Minus	***	=	X \$ =		OR X \$ =
☐ Application Size Fee (37 CFR 1.16(s))							
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
					TOTAL ADD'L FEE		OR TOTAL ADD'L FEE
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.							

Legal Instrument Examiner:
/ANTHONY WILLIAMS/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.



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NOTICE OF ALLOWANCE AND FEE(S) DUE

27765 7590 10/05/2011
NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
P.O. BOX 506
MERRIFIELD, VA 22116

EXAMINER

DANG, PHUC T

ART UNIT

PAPER NUMBER

2892

DATE MAILED: 10/05/2011

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/781,826	05/18/2010	Chu-Yin Tseng	NAUP0913USA1	3483

TITLE OF INVENTION: METHOD OF FABRICATING METAL OXIDE SEMICONDUCTOR TRANSISTOR

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1740	\$300	\$0	\$2040	01/05/2012

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: **Mail** **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax **(571)-273-2885**

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

27765 7590 10/05/2011
NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
P.O. BOX 506
MERRIFIELD, VA 22116

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/781,826	05/18/2010	Chu-Yin Tseng	NAUP0913USA1	3483

TITLE OF INVENTION: METHOD OF FABRICATING METAL OXIDE SEMICONDUCTOR TRANSISTOR

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1740	\$300	\$0	\$2040	01/05/2012

EXAMINER	ART UNIT	CLASS-SUBCLASS
DANG, PHUC T	2892	438-229000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

- (1) the names of up to 3 registered patent attorneys or agents OR, alternatively, 1 _____
- (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2 _____
- 3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☐ Issue Fee
- ☐ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____

Date _____

Typed or printed name _____

Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/781,826	05/18/2010	Chu-Yin Tseng	NAUP0913USA1	3483
27765 7590 10/05/2011 NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION P.O. BOX 506 MERRIFIELD, VA 22116			EXAMINER DANG, PHUC T	
			ART UNIT	PAPER NUMBER
			2892	

DATE MAILED: 10/05/2011

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 0 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 0 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No.	Applicant(s)	
	12/781,826	TSENG ET AL.	
	Examiner	Art Unit	
	PHUC DANG	2892	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to amendment filed on 04/27/2011 and 09/15/2011.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on ____; the restriction requirement and election have been incorporated into this action.

3. ☒ The allowed claim(s) is/are 1-22.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some* c) ☐ None of the:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).
* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
(a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
(b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.
Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892) 2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948) 3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____ 4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material	5. ☐ Notice of Informal Patent Application 6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ 7. ☐ Examiner's Amendment/Comment 8. ☐ Examiner's Statement of Reasons for Allowance 9. ☐ Other _____.
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/Phuc T Dang/ Primary Examiner, Art Unit 2892	
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EAST Search History**EAST Search History (Prior Art)**

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	328	438/229.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/20 10:59
L2	192	1 and (spacer\$1) with (gate)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/20 11:00
L3	150	2 and @ad<="20070809"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/20 11:01
L4	1158	438/300.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/20 11:01
L5	834	4 and (spacer\$1) with (gate)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/20 11:01
L6	704	5 and @ad<="20070809"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/20 11:01
L7	283	6 and recess\$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/20 11:02
L8	186	257/140.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/20 11:02
L9	10	8 and (spacer\$1) with (gate)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/20 11:04
L15	141	2 and @ad<="20061229"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/20 11:13
L16	662	5 and @ad<="20061229"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/20 11:13

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L12	99	((substrate) and (gate) and (protective near layer) and (recess\$2) and ((epitaxial epi) near (layer)) and (spacer) with (sidewall\$1))	USPAT; UPAD	OR	ON	2011/09/20 11:06
L13	1	"20080203449"	USPAT; UPAD	OR	ON	2011/09/20 11:10
L14	1	"7381623".pn.	USPAT; UPAD	OR	ON	2011/09/20 11:11

9/ 20/ 2011 11:16:54 AM

C:\Users\pdang1.000\Documents\EAST\Workspaces\12781826.wsp

Search Notes 	Application/Control No. 12781826	Applicant(s)/Patent Under Reexamination TSENG ET AL.
	Examiner Phuc T Dang	Art Unit 2892

SEARCHED			
Class	Subclass	Date	Examiner
438	229,300	01/21/2011	PD
257	19,190,192,197,E21.437	01/21/2011	PD
same	as above	09/20/2011	PD

SEARCH NOTES		
Search Notes	Date	Examiner
INVENTOR SEARCH	01/21/2011	PD
EAST SEARCH	01/21/2011	PD
EAST SEARCH (Updated)	06/06/2011	PD
EAST SEARCH (Interference Search History Printout)	09/20/2011	PD

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner
same	as above	09/20/2011	PD

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UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
 United States Patent and Trademark Office
 Address: COMMISSIONER FOR PATENTS
 P.O. Box 1450
 Alexandria, Virginia 22313-1450
 www.uspto.gov

BIB DATA SHEET

CONFIRMATION NO. 3483

SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.		
12/781,826	05/18/2010	257	2892	NAUP0913USA1		
APPLICANTS Chu-Yin Tseng, Tainan County, TAIWAN; Shih-Chieh Hsu, Hsinchu City, TAIWAN; Chih-Chiang Wu, Taichung County, TAIWAN; Shyh-Fann Ting, Tai-Nan City, TAIWAN; Po-Lun Cheng, Kao-Hsiung Hsien, TAIWAN; Hsuan-Hsu Chen, Tai-Nan City, TAIWAN;						
** CONTINUING DATA ***** This application is a DIV of 11/836,772 08/09/2007 PAT 7,745,847						
** FOREIGN APPLICATIONS *****						
** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** 05/27/2010						
Foreign Priority claimed ☐ Yes ☒ No 35 USC 119(a-d) conditions met ☐ Yes ☒ No Verified and Acknowledged <u>/PHUC T DANG/</u> Examiner's Signature		☐ Met after Allowance Initials	STATE OR COUNTRY TAIWAN	SHEETS DRAWINGS 14	TOTAL CLAIMS 21	INDEPENDENT CLAIMS 2
ADDRESS NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION P.O. BOX 506 MERRIFIELD, VA 22116 UNITED STATES						
TITLE Method of fabricating metal oxide semiconductor transistor						
FILING FEE RECEIVED 1194	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:			☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit		

<i>Index of Claims</i> 	Application/Control No. 12781826	Applicant(s)/Patent Under Reexamination TSENG ET AL.
	Examiner PHUC DANG	Art Unit 2892

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant					☐ CPA					☐ T.D.					☐ R.1.47				
CLAIM		DATE																	
Final	Original	01/21/2011	06/06/2011	09/20/2011															
1	1	✓	✓	=															
2	2	✓	✓	=															
3	3	✓	✓	=															
4	4	✓	✓	=															
5	5	✓	✓	=															
6	6	✓	✓	=															
7	7	✓	✓	=															
8	8	✓	✓	=															
10	9	✓	✓	=															
11	10	✓	✓	=															
12	11	✓	✓	=															
13	12	✓	✓	=															
14	13	✓	✓	=															
15	14	✓	✓	=															
16	15	✓	✓	=															
17	16	O	O	=															
18	17	O	O	=															
19	18	O	O	=															
20	19	O	O	=															
21	20	✓	✓	=															
22	21	✓	✓	=															
9	22			=															

Issue Classification 	Application/Control No. 12781826	Applicant(s)/Patent Under Reexamination TSENG ET AL.
	Examiner PHUC DANG	Art Unit 2892

ORIGINAL						INTERNATIONAL CLASSIFICATION												
CLASS		SUBCLASS				CLAIMED					NON-CLAIMED							
438		229				H	O	1	L	21 / 8238 (2006.01.01)								
CROSS REFERENCE(S)																		
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)																	
438	300																	
257	140																	

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47															
Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1	18	17												
2	2	19	18												
3	3	20	19												
4	4	21	20												
5	5	22	21												
6	6	9	22												
7	7														
8	8														
10	9														
11	10														
12	11														
13	12														
14	13														
15	14														
16	15														
17	16														

NONE		Total Claims Allowed:	
		22	
(Assistant Examiner)	(Date)		
/PHUC DANG/ Primary Examiner. Art Unit 2892	09/20/2011	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	5

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: **Mail** Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571) 273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

27765 7590 10/05/2011

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
P.O. BOX 506
MERRIFIELD, VA 22116

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

Stephanie Lai	(Depositor's name)
/Stephanie Lai/	(Signature)
11/02/2011	(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/781,826	05/18/2010	Chu-Yin Tseng	NAUP0913USA1	3483

TITLE OF INVENTION:

Method of fabricating metal oxide semiconductor transistor

APPLN TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	No	\$1740	\$300	\$2040	01/05/2012

EXAMINER	ART UNIT	CLASS-SUBCLASS
DANG, PHUC T	2892	438-229000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

- (1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
- (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 Winston Hsu

2 Scott Margo

3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

UNITED MICROELECTRONICS CORP.

No.3, Li-Hsin Road 2, Science-Based Industrial Park, Hsin-Chu City, Taiwan, R.O.C.

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are enclosed:

- ☒ Issue Fee
- ☒ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies _____

4b. Payment of Fee(s):

- ☐ A check in the amount of the fee(s) is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☒ The Director is hereby authorized by charge the required fee(s), or credit any overpayment, to Deposit Account Number 50-3105.

5. Change in Entity Status (from status indicated above)

- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

The Director of the USPTO is requested to apply the Issue Fee and Publication Fee (if any) or to re-apply any previously paid issue fee to the application identified above.

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature /Winston Hsu/ Date 11/02/2011

Typed or printed name Winston Hsu Registration No. 41,526

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Electronic Patent Application Fee Transmittal				
Application Number:		12781826		
Filing Date:		18-May-2010		
Title of Invention:		METHOD OF FABRICATING METAL OXIDE SEMICONDUCTOR TRANSISTOR		
First Named Inventor/Applicant Name:		Chu-Yin Tseng		
Filer:		Winston Hsu/Stephanie Lai		
Attorney Docket Number:		NAUP0913USA1		
Filed as Large Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl issue fee	1501	1	1740	1740
Publ. Fee- early, voluntary, or normal	1504	1	300	300

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				2040

Electronic Acknowledgement Receipt	
EFS ID:	11315784
Application Number:	12781826
International Application Number:	
Confirmation Number:	3483
Title of Invention:	METHOD OF FABRICATING METAL OXIDE SEMICONDUCTOR TRANSISTOR
First Named Inventor/Applicant Name:	Chu-Yin Tseng
Customer Number:	27765
Filer:	Winston Hsu/Stephanie Lai
Filer Authorized By:	Winston Hsu
Attorney Docket Number:	NAUP0913USA1
Receipt Date:	02-NOV-2011
Filing Date:	18-MAY-2010
Time Stamp:	03:04:37
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	\$ 2040
RAM confirmation Number	6415
Deposit Account	503105
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees) Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)	

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)					
Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees)					
Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)					
File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
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2	Fee Worksheet (SB06)	fee-info.pdf	32222 dd5123c799ed0e6ec1fed9835be89ba232390dbd	no	2
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Amendments to the Specification:

Please replace paragraph [0001] with the following amended paragraph:

- 5 [0001] This is a divisional application of U. S. patent application Ser. No. 11/836,772 filed on August 9, 2007, PAT 7,745,847, and the contents of which are included herein by reference.

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Change(s) applied to document,
/S.D.W./
11/3/2011

21
Please replace paragraph [0023] with the following amended paragraph:

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[0023] As shown in Fig. 5, spacers 228 are formed on the sidewalls of each gate 280. According to the first preferred embodiment of the present invention, each spacer 228 comprises an oxide liner 230 and a nitride spacer 232. The spacers 228 cover the sidewalls of each gate 208 and also extend laterally onto the first ion lightly doped region 222 and the second ion lightly doped region 224. Each spacer 228 may also comprise an offset spacer (not shown) positioned between the gate 208 and the oxide liner 230. Because each spacer 228 in the first conductive transistor area 202 lies over the raised epitaxial layer 220, thus each spacer 228 in the first conductive transistor area 202 is tilted upward and a contact surface 350 of the epitaxial layer 220 and the spacer 228 is above the surface of the semiconductor substrate 200. Please refer to Fig. 10, which is a transmission electron microscopy (TEM) picture of the MOS transistors in accordance with the first preferred embodiment of the present invention.

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ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

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