SEMICONDUCTOR MANUFACTURING TECHNOLOGY

MICHAEL QUIRK
STAKTEK CORPORATION

JULIAN SERDA
ADVANCED MICRO DEVICES



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Thin Film Metallization Work Bay
(Photo courtesy of Advanced Micro Devices)

CMOS MANUFACTURING STEPS

The remainder of this chapter focuses on the manufacturing steps that a wafer follows in a typical CMOS process. Although there are some operations in the process flow that can be performed in batches of wafers at one time, this process flow describes the manufacturing of a single wafer. For further simplification, this process describes the production of only a microscopic area of a single CMOS inverter consisting of two transistors—nMOS and pMOS. Cross-sectional views of the product will be provided for each major operation.

The CMOS manufacturing steps to be described are:

1. Twin Well Process
2. Shallow Trench Isolation Process
3. Poly Gate Structure Process
4. Lightly Doped Drain (LDD) Implant Processes
5. Sidewall Spacer Formation
6. Source/Drain (S/D) Implant Processes
7. Contact Formation
8. Local Interconnect Processes
9. Via-1 and Plug-1 Formation
10. Metal-1 Interconnect Formation
11. Via-2 and Plug-2 Formation
12. Metal-2 Interconnect Formation
13. Metal-3 to Pad Etch and Alloy
14. Parametric Testing

1. Twin Well Process

The first step in some CMOS wafer fabrication processes is to define the active regions of the MOSFETs. Many of today's sub-quarter micron processes use a *twin-well* (also referred to as *twin-tub*) approach to define the active regions of the nMOS and pMOS transistors. A twin-well consists of a p-well and an n-well, with each well requiring at least three to five major processing steps to fabricate. A *retrograde implant* technique is used to obtain optimum electrical characteristics for the FETs. This technique starts with a high-energy, high-dose implant that penetrates approximately 1 μm into the epilayer. Subsequent well implants are done at the same active site with a progressive

decrease in energy, junction depth, and dose of dopant material such as phosphorus or boron (measured in atoms/cm^2). The results help set the threshold operating voltage for the FETs as well as prevent common CMOS problems, such as *latchup* and other reliability issues. Figure 9.8 and Figure 9.9 illustrate, respectively, the major steps required in the formation of the n-well and p-well.

n-well Formation ■ The five major steps in n-well formation are described below in the following process and illustrated in Figure 9.8.

Description of Five Major Steps in n-well Formation

	Process Step	Description
1.	Epitaxial Growth	The silicon wafer, having already a thin layer of *epitaxial* silicon (epilayer), arrives in the diffusion bay. The epilayer has the exact crystal structure as the substrate, except with improved purity and fewer crystal defects. The epilayer has already been lightly doped with p-type dopant (boron).
2.	Initial Oxide Growth	In diffusion the wafer is cleaned in a series of chemical baths to remove particles, organic and inorganic contamination, and *native oxide* growth (natural silicon dioxide growth) from the wafers. After the wafer is rinsed and dried, the wafer is placed in a high temperature (~1000 °C) furnace process chamber. Oxygen is flowed into the process chamber to react with silicon to grow approximately 150 Å of oxide. This initial oxide serves several functions: (1) it protects the top surface of the epi silicon from contamination, (2) it prevents excessive damage to the silicon during implantation, and (3) as a screen oxide, it helps control the depth of the dopants during implantation.
3.	1st Mask, n-well Implant	In photolithography the wafer undergoes a series of process steps in the coater/developer track tool. The "tracks," as commonly referred to, prime the top surface of the wafer, coat the wafer with photoresist (liquid photographic film), spin the wafer, and bake the wafer. An internal automatic wafer-handling system transfers the wafer between process stations within the tracks. Another wafer handler removes resist-coated wafers, one at a time, and transfers them to the *alignment-and-exposure system* (an extremely complex and precise camera). The alignment-and-exposure system photographs the image of a specific mask layer directly onto the resist-coated wafer. In this case, the mask layer defines the areas of the product that are to be implanted in order to form the n-wells for the pMOS transistors. The exposed wafer is then transferred back to the tracks, where the image first appears when the wafer is sprayed with the chemical developer. The developed wafer undergoes another bake step and is inspected before being transferred to the ion implant bay. The printed pattern is inspected for proper *linewidths,* called *critical dimensions* (*CD*). In the event of a major defect, the photoresist can be stripped off and the wafer can then be reworked. Photolithography is the only area in the fab where a wafer can be easily reworked.
4.	n-well Implant (High energy)	The patterned wafer arrives in the ion implant bay. The photoresist pattern covers specific areas of the wafer that are to be protected from ion implantation. Windows, or openings, in the photoresist allow high-energy positive dopant ions to penetrate into the upper surface of the epilayer (~1 μm *junction depth*). In this case, phosphorus is the desired dopant. The *ion implanter* is the main process tool in this bay. Its purpose is to ionize dopant atoms, accelerate them with high voltage (~200 KeV), select the most appropriate dopant species to implant, focus the ions into a narrow beam, and, finally, scan the wafer to provide uniform doping across all unprotected areas of the wafer. At this point the dopant ions penetrate the crystal lattice of the silicon causing damage to the covalent atomic structure. This damage will be repaired later in a diffusion and annealing step. *Note:* After each ion implant operation, an oxygen-plasma reactor tool strips the photoresist off each implanted wafer. The wafer is then cleaned by a wet chemical process to remove residual photoresist and polymers created by the plasma process. This note applies to all subsequent implant operations but will be listed only this one time.
5.	Anneal	The implanted wafer is transferred to diffusion where the wafer is cleaned before being inserted into an *anneal* furnace. Four things occur as a result of this anneal process. (1) A new barrier oxide layer is grown over the bare silicon. (2) The higher temperatures cause the movement of dopants further into the silicon (called diffusion). (3) The implant damage is repaired. (4) The bonds between the dopant atoms and the silicon atoms are activated, making the dopant atoms a part of the crystal lattice structure (electrical activation).

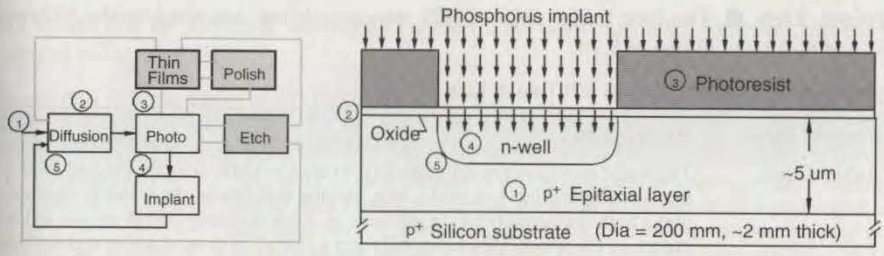


FIGURE 9.8 n-well Formation

p-well Formation ■ The three major steps in p-well formation are described in the following process and illustrated in Figure 9.9.

Description of Three Major Steps in p-well Formation

	Process Step	Description
1.	2nd Mask, p-well Implant	The photolithography steps for the p-well implant mask are exactly the same as for the first mask. The only difference is the mask is the direct opposite of the n-well implant mask. Compare Figure 9.8 and Figure 9.9 to see the differences.
2.	p-well Implant (High energy)	The retrograde p-well implant energy levels are considerably lower than the n-well. This condition is due to the difference in the masses of the elements being implanted. Comparing the atomic mass unit (amu) of boron (~11) to phosphorus (~31), boron is about one-third the mass of phosphorus. Thus, the energy needed to implant boron should only require about one-third of that used to implant phosphorus to the same junction depth.
3.	Anneal	This anneal step is basically the same as the first annealing step.

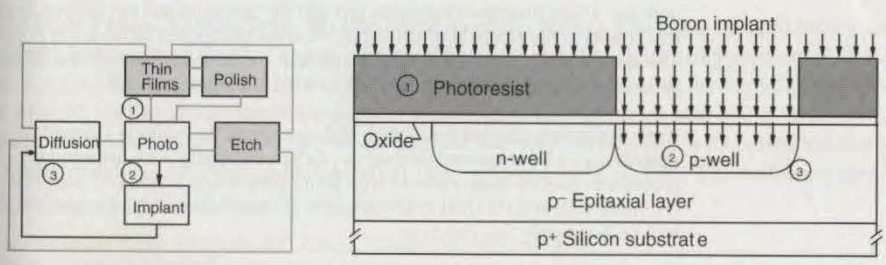


FIGURE 9.9 P-well Formation

2. Shallow Trench Isolation Process

Shallow trench isolation (STI) is an alternative method for creating isolation regions between active transistor areas on a substrate.[1] This method is especially useful in the manufacturing of quarter-micron devices. The preferred isolation technique up until the late 1990s had been the LOCOS (local oxidation of silicon) technique that was instituted in the early 1970s.[2] Despite its complexity, STI is gaining in popularity with ULSI chip manufacturing. STI formation is explained as follows in three major steps: trench etch (see Figure 9.10 on page 208), oxide fill (see Figure 9.11 on page 209), and oxide polish (see Figure 9.12 on page 209).

STI Trench Etch ■ The four major steps in STI trench etch are described in the following process and illustrated in Figure 9.10.

Description of Four Major Steps in STI Trench Etch

	Process Step	Description
1.	Barrier Oxide	The wafer arrives in the diffusion bay where the wafer is again cleaned to remove contamination and oxide. After rinsing and drying, the wafer is inserted into a high-temperature oxidation furnace. Approximately 150 Å of new oxide is grown on the wafer. This layer will form a barrier to protect active regions from chemical contamination during nitride strip.
2.	Nitride Deposition	The wafer is inserted into a high-temperature (~750 °C) *LPCVD* (*low-pressure chemical vapor deposition*) furnace. Inside the process chamber ammonia and dichlorosilane gases react to form a thin layer of silicon nitride (nitride, Si_3N_4) on the wafer. The nitride will serve two functions throughout the STI formation process steps. (1) Nitride is a durable masking material, which protects active regions during the STI oxide deposition process and (2) nitride serves as a polish-stop material during the chemical mechanical planarization (CMP) step.
3.	3rd Mask, STI	The wafer arrives in photolithography from diffusion. This photolithography process step is similar to the previous masking step, except a different mask is used. This masking step is much more critical than the first mask due to the smaller dimensions. Inspection of the wafer includes CD measurements as well as checking for *defect inspection* (*DI*), and optical *visual inspection* (*VI*). These measurements require checking the accuracy of the alignment-exposure system relative to the written specifications.
4.	STI Trench Etch	The photoresist pattern is designed to protect areas of the silicon that are not to be etched. The windows in the photoresist allow ions and highly reactive *radical chemicals* to etch nitride, oxide, and silicon in unprotected areas. The preferred tool for etching these deep trenches is the *dry plasma etcher.* The etcher uses high-powered radio frequency (RF) energy to ionize a fluorine- or chlorine-based gas inside a vacuum process chamber. The RF energy dissociates molecules and ionizes atoms to create a chamber filled with a variety of plasma components. These plasma components provide the chemical and physical etching that results in the removal of silicon in locations designated as *isolation regions.* The slanted profile and the rounded bottom of the trenches improve the filling process and the electrical characteristics of the isolation structure. *Note:* Following completion of each etch operation, the wafer is stripped of photoresist and wet cleaned in a series of chemical baths. Key inspection procedures include measurements that verify proper step height (Å), etch rate (Å /min), CD, and DI. This note applies to all subsequent etch operations but will be listed only this one time.

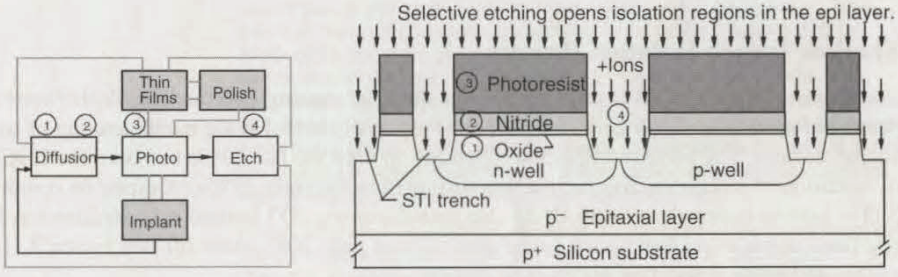


FIGURE 9.10 STI Trench Etch

STI Oxide Fill ■ The basic steps in STI oxide fill are described in the following process and illustrated in Figure 9.11.

Description of Basic Steps in STI Oxide Fill

	Process Step	Description
1.	Trench Liner Oxide	The wafer is again cleaned in the diffusion bay to remove contamination and oxide. After rinsing and drying, the wafer is inserted into a high-temperature oxidation furnace. Approximately 150 Å of oxide grows in the exposed walls of the isolation trenches. The nitride mask prevents oxygen diffusion into the active regions. The purpose of the liner oxide is to improve the interface between the silicon and the trench CVD oxide.
2.	Trench Fill with CVD Oxide	This deposition process is performed either in diffusion using an LPCVD furnace or in thin films using a variety of oxide CVD systems. Higher throughput and deposition rates are obtained with the furnace.

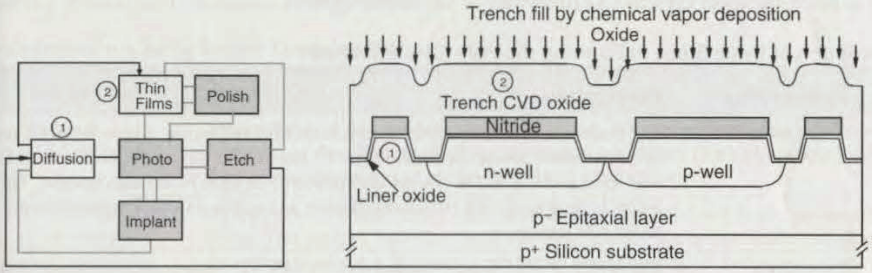


FIGURE 9.11 STI Oxide Fill

STI Oxide Polish-Nitride Strip ■ Planarization of the wafer surface is accomplished by several methods. In the past, filling the gap to planarize the wafer could be done using *spin-on-glass* (*SOG*), consisting of 80% solvent and 20% silicon dioxide. Baking the SOG after the deposition evaporated the solvent, leaving oxide inside the gaps. A complete surface *etchback* also could be performed to reduce the overall thickness. However, no method has been as effective a planarization technique as CMP, chemical mechanical planarization (also referred to as *polish*). The following table and Figure 9.12 on page 210 describe and illustrate the process.

Description of Basic Steps in STI Oxide Polish and Nitride Strip

	Process Step	Description
1.	Trench Oxide Polish (CMP)	In the CMP area the wafer is turned upside down and held by vacuum to a wafer carrier. The wafer rotates in the same direction as a polishing pad attached to a rotating polishing table. A chemical slurry keeps the pad and wafer wet during the polishing process and provides reactants to help abrade the oxide surface. The nitride, being a harder material than the oxide, serves as the polish-stop material to prevent over-polishing the isolation structures. *Note:* The following statement applies to all polishing operations and will not be repeated again. The polishing process creates excessive particles and chemical contaminants that must be thoroughly removed before transferring the wafer to other areas in the wafer fab. Special scrub stations clean the top and bottom of the wafer and ensure it is rinsed and dried. Inspections for film thickness, particles, and defects are also conducted before wafer is transferred.
2.	Nitride Strip	The diffusion bay is traditionally equipped with hot phosphoric acid stations for stripping the nitride from the wafer. In the diffusion bay the wafer is stripped, cleaned, rinsed, and dried, then inspected to check the thickness of the isolation oxide.

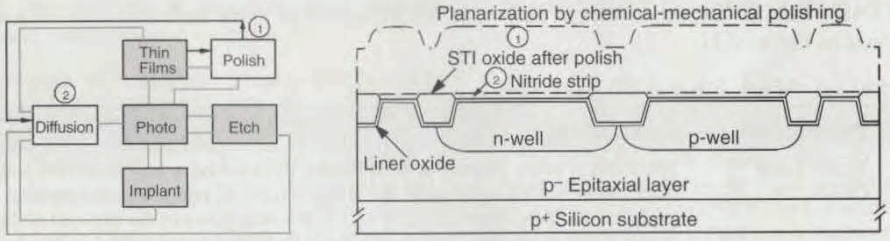


FIGURE 9.12 STI Formation

3. Poly Gate Structure Process

Forming the structure of the transistor gate is a critical step in the process because it includes thermally growing the thinnest *gate oxide* and patterning and etching the *polysilicon gate*, one of the smallest physical structures in the entire IC process (see Figure 9.13). The width of the polysilicon gate is often the most critical CD linewidth of the entire wafer.

Description of Basic Steps in Forming the Poly Gate Structure

	Process Step	Description
1.	Gate Oxide Growth	The wafer is cleaned to remove contamination and oxide. There is only a matter of a few hours before the wafer must be inserted in the oxidation furnace. Oxide will form as long as the silicon is exposed to oxygen in the atmosphere. The wafer is inserted in the oxidation furnace and a thin oxide of approximately 20 to 50 Å is grown.
2.	Polysilicon Deposition	The wafer is immediately loaded into an LPCVD furnace where silane (SiH_4) is introduced into the process chamber. The silane dissociates and polysilicon is deposited on the wafer. Approximately 5000 Å of polysilicon (also referred to as poly) is deposited. Some processes may call for doping the polysilicon immediately following the deposition step. This action can be done in the same process chamber or in a separate furnace.
3.	4th Mask, Poly Gate	In photolithography, deep UV lithography (assuming sub-0.25 μm technology) techniques are used to pattern the fine structures of the polysilicon gates. An *antireflective coating* (*ARC*) is commonly applied between the poly and the photoresist to reduce undesirable reflections. The resist linewidths for the gates are the narrowest structures on the IC; therefore, various quality measurements are required, such as CD and overlay registration (OL), and defect inspection (DI).
4.	Poly Gate Etch	By far one of the most critical etch steps in the IC process requires the use of the best *anisotropic plasma etchers* available in the fab. These single-direction etchers etch the polysilicon to provide the vertical profile as shown in Figure 9.13.

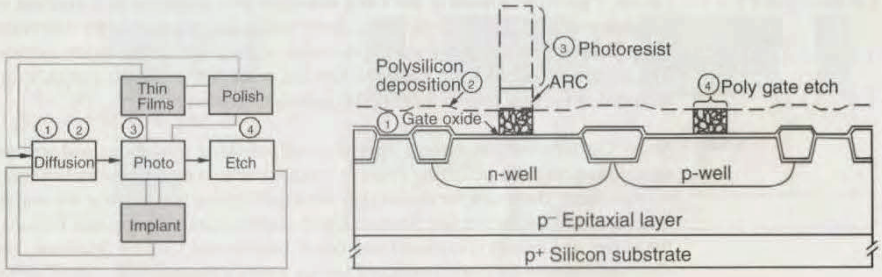


FIGURE 9.13 Poly Gate Structural Process

4. Lightly Doped Drain (LDD) Implant Process

As gate widths get smaller, the *channel length* below the gate structure (the silicon region between the source and drain) also decreases. This reduction increases the potential for charges to *punchthrough* the transistor source and drain and cause undesirable channel leakage current. There are techniques that are used to reduce the occurrence of this leakage in the channel.

The next series of ion implant steps begins to define the source and drain regions of transistors. Each pMOS and nMOS transistor will be implanted twice—once with a shallow implant called the *lightly doped drain (LDD) implant,* then followed by a medium or high dose *source/drain implant.* Lightly doped drain (LDD) implants (see Figure 9.14 below and Figure 9.15 on page 212) use the larger mass of arsenic and BF_2 dopant materials to create an *amorphous* (disorganized with no long-range order or crystal structure) upper layer of silicon. The combination of large mass and amorphous surface conditions helps maintain a shallow junction, which also helps reduce channel current leakage effects between the source and drain.

n^- LDD Implant ■ The steps for creating n^- lightly doped drain implants are described in the following process and illustrated in Figure 9.14.

Description of n- Lightly Doped Drain Implant

	Process Step	Description
1.	5th Mask, n^- LDD Implant	The purpose of this masking step is to pattern the wafer in a manner that opens windows in the photoresist where n-channel transistors can be implanted. All other areas are protected by the remaining photoresist.
2.	n^- LDD Implant (Low energy, shallowjunction depth)	Arsenic ions are selectively implanted through the windows in the patterned resist. The energy, dose and depth are significantly lower than in the previous n-well implant steps. Arsenic is preferred over phosphorus because its larger mass amorphizes the silicon surface to create a more uniform dopant depth during implant.

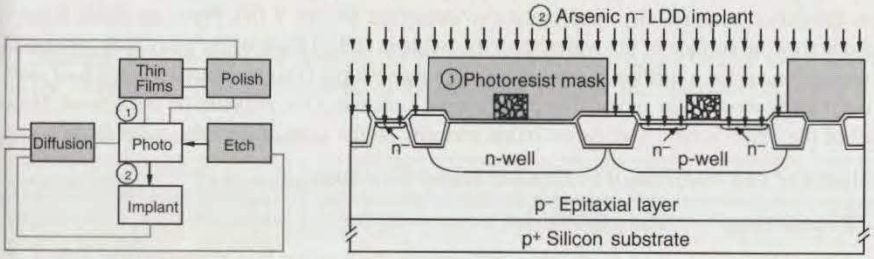


FIGURE 9.14 n^- LDD Implant

p⁻ LDD Implant ■ The steps for creating p⁻ lightly doped drain implants are described in the following process and illustrated in Figure 9.15.

Description of p- Lightly Doped Drain Implant

	Process Step	Description
1.	6th Mask, p⁻ LDD Implant	The purpose of this masking step is to pattern the wafer in a manner that opens windows in the photoresist where p-channel transistors can be implanted. All other areas are protected by the remaining photoresist.
2.	p⁻ LDD Implant (Low energy, shallow junction depth)	Boron difluoride, BF_2, is preferred over boron for this implant step. BF_2 is a heavier substance than boron. The heavier BF_2 helps amorphize the silicon surface.

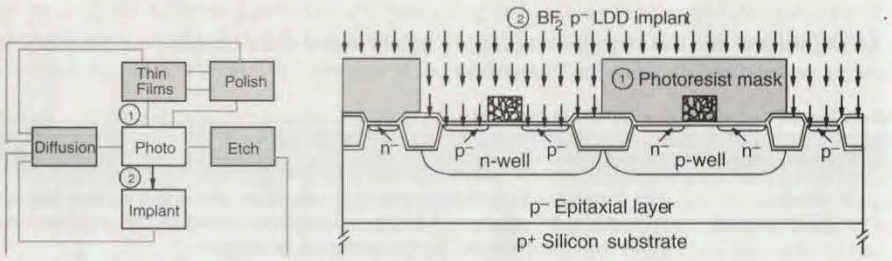


FIGURE 9.15 p⁻ LDD Implant

5. Sidewall Spacer Formation

Sidewall spacers will be used alongside the poly gates to prevent the higher source/drain (S/D) implant from penetrating too close to the channel where S/D punchthrough could occur. Sidewall spacer formation requires two major process steps (see Figure 9.16). First, an oxide layer is deposited across the surface of the wafer, then the oxide is etched back using a dry etch process. There is no requirement for a masking step because the anisotropic (single-direction) etch tool uses ions to sputter away most of the oxide. The etch process ends when the polysilicon is exposed. However, not all of the oxide is removed. Some oxide remains on the sidewalls of the polysilicon gates.

Description of Two Major Steps in Sidewall Spacer Formation

	Process Step	Description
1.	Spacer Oxide Deposition	This procedure is performed in the thin film bay. Approximately 1000 Å of oxide is deposited with a chemical vapor deposition (CVD) process. This layer will be used to form spacers on the sides of the polysilicon gates.
2.	Spacer Oxide Etchback	The dry plasma etcher removes most of the CVD oxide leaving behind the thicker oxide on the sidewalls of the polysilicon gates.

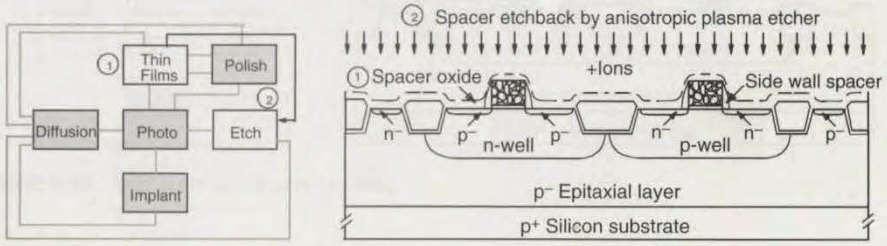


FIGURE 9.16 Sidewall Spacer Formation

6. Source/Drain (S/D) Implant Processes

To complete the retrograde implant technique, medium-dose implants are made to penetrate the silicon slightly beyond the LDD junction depth, but not as deep as the original twin-well implants (see Figure 9.17 and Figure 9.18). The spacer oxide from the previous step will protect the channel from the dopant atoms during the implant process.

n^+ S/D Implant ■ The steps for creating n^+ source/drain implants are described in the following process and illustrated in Figure 9.17.

Description of n+ Source/Drain Implant

	Process Step	Description
1.	7th Mask, n^+ S/D Implant	This masking step defines areas of the nMOS transistors that are to be implanted.
2.	n^+ S/D Implant (Medium energy)	This is a medium-energy implant step that penetrates the silicon deeper than the LDD junction depth. Spacer oxide prevents the arsenic dopant from encroaching into the narrow channel.

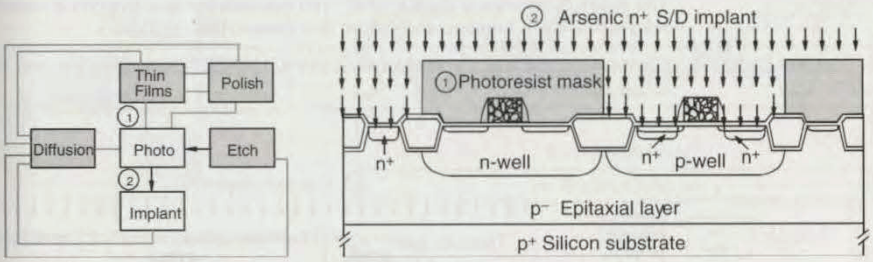


FIGURE 9.17 n^+ S/D Implant

p^+ S/D Implant ■ The steps for creating the p^+ source/drain regions are similar to n^+ S/D formation. The steps for p^+ S/D are described in the following process and illustrated in Figure 9.18.

Description of p+ Source/Drain Implant

	Process Step	Description
1.	8th Mask, p^+ S/D Implant	This masking step defines areas of the pMOS transistors that are to be implanted.
2.	p^+ S/D Implant (Medium energy)	This implant step penetrates the silicon slightly beyond the LDD junction depth. Spacer oxide prevents boron dopant from encroaching into the narrow channel.
3.	Anneal	The implanted wafer is annealed in a *rapid thermal process* (*RTP*) tool. RTP tools have the ability to quickly reach temperatures of ~1000 °C and maintain the setpoint for several seconds. This condition is important to prevent structures from spreading and to control the diffusion of dopants in the S/D regions.

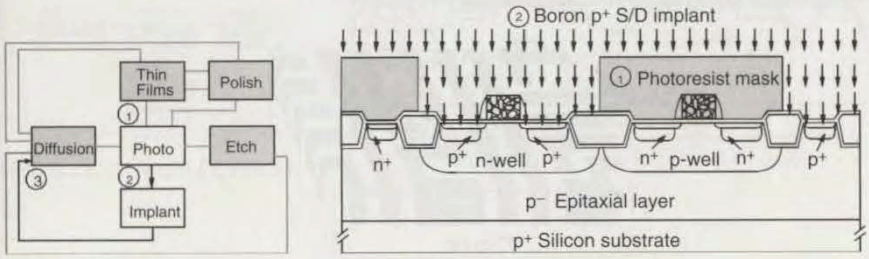


FIGURE 9.18 p^+ S/D Implant

7. Contact Formation

The purpose of the contact formation process steps is to form *metal contacts* on all active areas of silicon. These metal contacts serve to promote adhesion between the silicon and the metal conductor material that will be deposited later (see Figure 9.19). Titanium is a good choice for the metal contact material, although cobalt can also be used. Titanium has low resistivity characteristics and reacts very well with silicon. When raised to a temperature >700 °C, titanium bonds with silicon to form a *titanium silicide* ($TiSi_2$) compound, or *tisilicide*. Titanium and silicon dioxide do not react; therefore, no chemical bonding or physical connection is made between these two materials. Thus, titanium can be easily etched off the oxide without the need for a masking step. Tisilicide remains at all locations where active silicon exists (e.g. source, drain, and gate).

Description of Major Steps in Titanium Contact Formation

	Process Step	Description
1.	Titanium Deposition	The wafer is cleaned thoroughly to remove contaminants and oxides from the silicon. Titanium (Ti) is deposited on wafers using a sputtering process. *Sputtering* is a *physical vapor deposition* (*PVD*) process that is performed in a plasma process chamber where energetic argon ions bombard a metal target to release metal atoms, which deposit onto a wafer.
2.	Anneal	The wafer is inserted in the RTP tool. The high temperature triggers a chemical reaction between titanium and silicon that forms $TiSi_2$ (tisilicide).
3.	Titanium Etch	Chemicals etch away the unreacted titanium, leaving behind tisilicide over the active silicon areas.

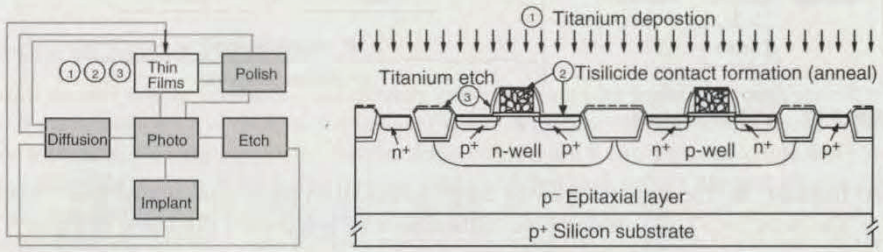


FIGURE 9.19 Contact Formation

8. Local Interconnect (LI) Process

The next step in the IC manufacturing process is to form metal connecting lines between transistors and other tisilicide contacts. The method used in this process flow is referred to as *local interconnect* (*LI*). The steps leading up to the formation of LI are as complicated as the formation of the STI. The process begins with the deposition of dielectric films, followed by CMP, patterning, etch, and tungsten metal deposition and finished off with a metal polish (see Figure 9.20 and Figure 9.21). This process is referred to as *damascene*—a name adopted from a practice that began thousands of years ago by artisans in Damascus, Syria.[3] The result of these steps produces a top surface that resembles intricate inlaid jewelry or artwork. The graphic in Figure 9.22 illustrates how the metal lines are formed within the walls of the etched oxide.

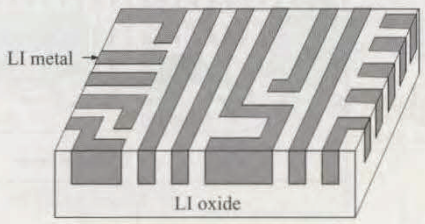


FIGURE 9.20 LI Oxide as a Dielectric for Inlaid LI Metal

Description of LI Oxide Dielectric Formation

	Process Step	Description
1.	Nitride (Si_3N_4) CVD	A barrier layer of silicon nitride is deposited using a CVD process. The nitride provides protection for the active regions from the dopants in the next film layer.
2.	Doped Oxide CVD	The LI dielectric component of the local interconnect structure is formed from CVD oxide (SiO_2). This oxide is lightly doped with phosphorus or boron. The addition of dopants to the oxide improves the dielectric qualities of the glass. An additional RTP step allows the glass to flow and smooth the surface.
3.	Oxide Polish (CMP)	CMP is used to planarize the LI oxide. The resulting thickness of the oxide after polish is ~8000 Å.
4.	9th Mask, LI Etch	The wafer is patterned in photolithography and then etched in the etch bay. Narrow trenches are created in the LI oxide that will serve as the forms for defining the paths for the LI metal.

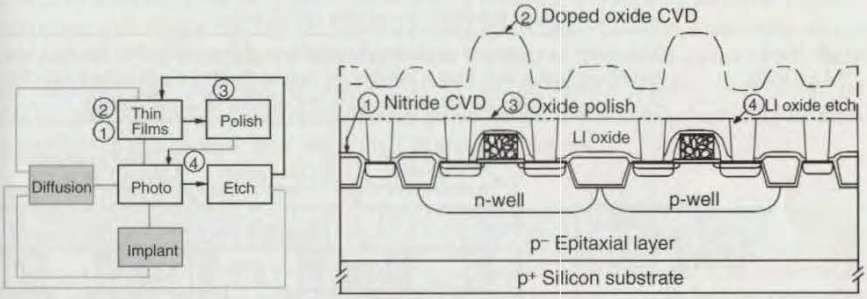


FIGURE 9.21 LI Oxide Dielectric Formation

Description of LI Metal Formation

	Process Step	Description
1.	Titanium Deposition (PVD process)	A thin barrier layer of titanium (Ti) lines the bottom and the inside of the LI walls. The Ti serves as a "double-adhesive tape" to hold the tungsten (W) to the SiO_2.
2.	Titanium Nitride Deposition	Titanium nitride (TiN) is deposited immediately over the Ti to serve as a diffusion barrier for the tungsten metal.
3.	Tungsten Deposition (CVD process polish)	Tungsten fills the LI trenches and coats the entire wafer. Tungsten is preferred over aluminum for LI metal due to its ability to fill holes without leaving voids in the formed metal plug. Another reason is for its good polishing characteristics.
4.	Tungsten polish	The tungsten is polished down to the upper surface of the LI oxide.

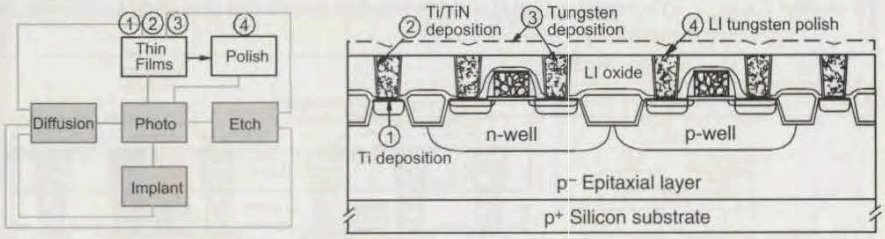


FIGURE 9.22 LI Metal Formation

9. Via-1 and Plug-1 Formation

The *interlayer dielectric* (*ILD*) serves as an insulator material between each metal layer or between the first metal layer and silicon. The ILD will have many small *vias,* which are small openings in the ILD that provide an electrical pathway from one metal layer to adjacent metal layers. Vias are filled with a conductive metal (usually tungsten, and referred to as a *tungsten plug*) and are placed at the appropriate locations to form the electrical circuit between metal layers (see Figure 9.23 and Figure 9.24). ILD-1 is the first of a series of interconnection process to be described.

Description of Major Steps in Via-1 Formation

	Process Step	Description
1.	ILD-1 Oxide Deposition (CVD)	Oxide is deposited across the surface of the wafer with a CVD tool in thin films. This layer (ILD-1) will serve as the dielectric material from which vias are to be formed.
2.	Oxide Polish	CMP is used to planarize the ILD-1 oxide. The resulting thickness of the oxide after polish is approximately 8000 Å. The wafer is scrubbed and cleaned to remove particles generated during the polish step.
3.	10th Mask, ILD-1 Etch	The wafer is patterned in photolithography and then etched in the etch bay. Small via holes, less than a quarter micron in diameter, are etched into the ILD-1 oxide. This step is critical in terms of CD, OL, and defects.

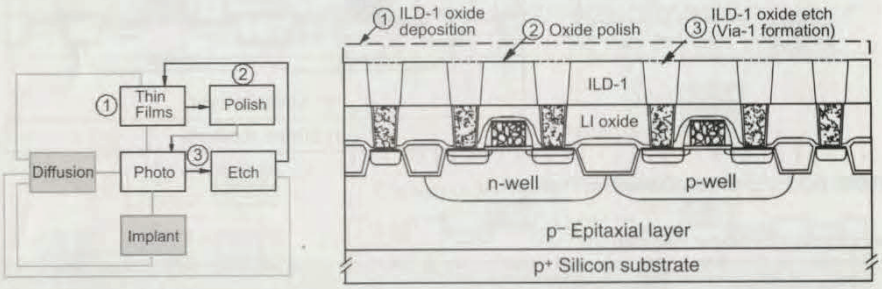


FIGURE 9.23 Via-1 Formation

Description of Major Steps in Plug-1 Formation

	Process Step	Description
1.	Titanium Barrier Metal Deposition (PVD)	A thin layer of titanium is deposited across the surface of the wafer with a PVD tool in thin films. Titanium lines the bottom and the walls of the via holes. The Ti serves as the glue that holds the tungsten plug inside the hole.
2.	Titanium Nitride Deposition (CVD)	TiN is thinly deposited on top of the Ti layer. The TiN serves as a diffusion barrier for the tungsten in the next deposition step.
3.	Tungsten Deposition (CVD)	Another CVD tool is used to deposit tungsten on the wafer. Tungsten fills the small openings to form the plug.
4.	Tungsten Polish	The tungsten-coated wafer is polished down to the upper surface of the ILD-1 oxide.

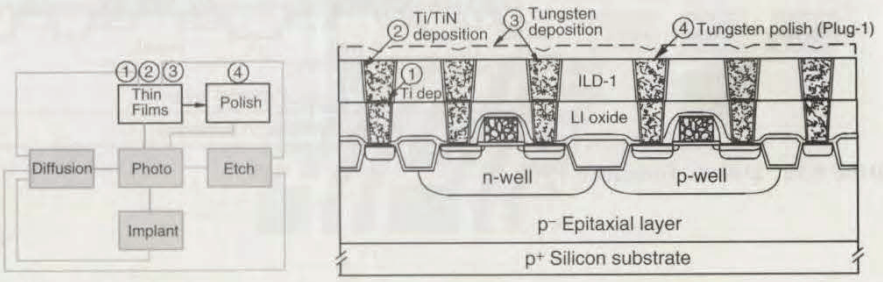
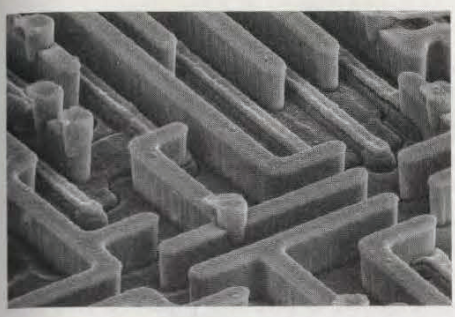


FIGURE 9.24 Plug-1 Formation



SEM Micrograph of Polysilicon, Tungsten LI and Tungsten Plugs (Polysilicon is represented by the thin lines between the taller LI lines). (Micrograph courtesy of Integrated Circuit Engineering)

10. Metal-1 Interconnect Formation

The next series of operations has to do with depositing a three-layer metal film, referred to as a *metal stack* or *sandwich,* on the wafer, followed by a masking and etching step (see Figure 9.25). The multilayer metal stack consists of different refractory metals—titanium, aluminum/ copper, and titanium nitride. When finished, the wafer will have the first of five metal stacks to be constructed on the device. The number of metal layers on a device varies depending on die complexity, with advanced die currently having around eight metal layers. Including LI metal, the device covered in this process flow has a total of six metal layers.

Description of Steps in Metal-1 Interconnect Formation

	Process Step	Description
1.	Titanium Barrier Metal Deposition (PVD)	As with other metal processes, titanium is the first metal to be deposited on the entire wafer. It provides a good bond between the tungsten plugs and the next metal, aluminum. It also bonds well to the interlayer dielectric material and improves the reliability of the metal stack.
2.	Aluminum-Copper Deposition (PVD)	The aluminum-copper (99% Al, 1% Cu) metal is sputtered onto the titanium-coated wafer by a PVD tool in thin films. The 1% Cu is added to the aluminum to improve the reliability of the aluminum.
3.	Titanium Nitride Deposition (PVD)	TiN is thinly deposited on top of the aluminum-copper layer to serve as an antireflective coating for the next photomasking step.
4.	11th Mask, Metal Etch	The wafer is patterned with photoresist, then the three-layer metal stack is etched using a plasma etcher.

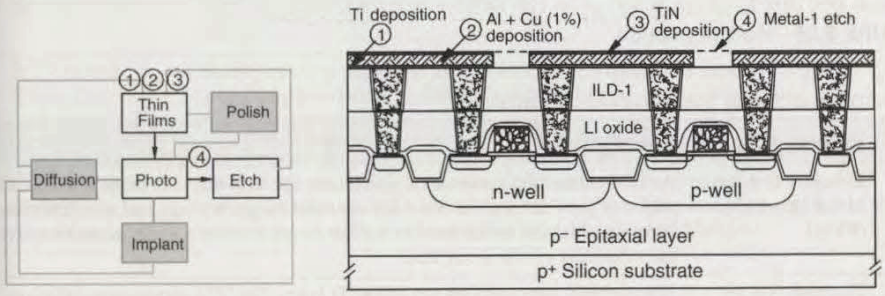


FIGURE 9.25 Metal-1 Interconnect Formation

11. Via-2 and Plug-2 Formation

The next four operations will result in the formation of the second interlayer dielectric (ILD-2) and the via openings (see Figure 9.26 and Figure 9.27). ILD-2 is similar to ILD-1 except for the very first step of filling small and large gaps that were etched into Metal-1. *Gap fill* is the filling of these gaps with a dielectric material that can be placed into the narrow spaces without creating voids or other defects that could affect electrical performance. There are two common methods for filling gaps—spin-on-glass (SOG) with etchback and *high-density plasma chemical vapor deposition* (HDPCVD). HDPCVD is the preferred method for sub-quarter micron processes. Once the gaps are filled, a plasma-enhanced CVD (PECVD) system finishes depositing the remainder of the ILD-2 oxide. Following the deposition of the ILD-2, the oxide is polished, patterned, and then etched to open the vias for the tungsten plugs to be formed.

Description of Major Steps in Via-2 Formation

	Process Step	Description
1.	ILD-2 Gap Fill	The latest gap-fill method for ULSI devices utilizes a high-density plasma process to alternately deposit and etch the interlayer oxide as its being deposited. The result is a dense oxide with few or no voids in the metal gaps.
2.	ILD-2 Oxide Deposition	A PECVD system is used to deposit the remainder of the ILD-2 oxide layer.
3.	ILD-2 Oxide Polish	The wafer is polished to planarize the surface prior to the next patterning step.
4.	12th Mask, ILD-2 Etch	The wafer is patterned with photoresist, then the ILD-2 oxide is etched using a plasma etcher.

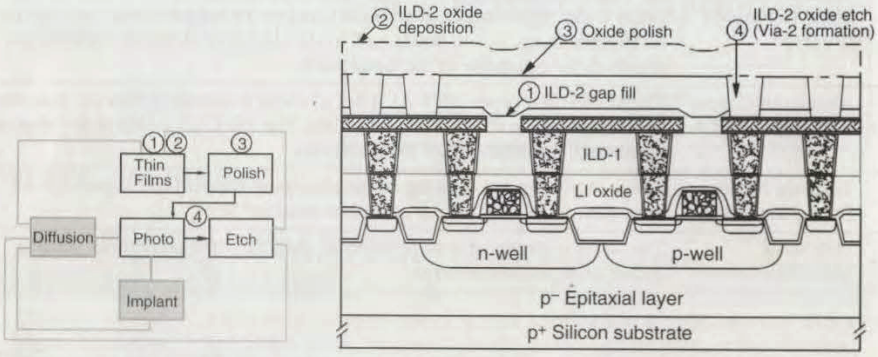


FIGURE 9.26 Via-2 Formation

Description of Major Steps in Plug-2 Formation

	Process Step	Description
1.	Titanium Barrier Metal Deposition (PVD)	As with other metal processes, titanium is the first metal to be deposited on the wafer. It provides a good bond between the tungsten plugs and the next metal, aluminum. It also bonds well to the interlayer dielectric material and improves the reliability of the metal stack.
2.	Titanium Nitride Deposition (CVD)	TiN is thinly deposited on top of the Ti layer. The TiN serves as a diffusion barrier for the tungsten in the deposition step.
3.	Tungsten Deposition (CVD)	Another CVD tool is used to deposit tungsten on the wafer. Tungsten fills the small via openings to form the plug.
4.	Tungsten Polish	The tungsten-coated wafer is polished down to the upper surface of the ILD-2 oxide, leaving the tungsten plugs in the vias.

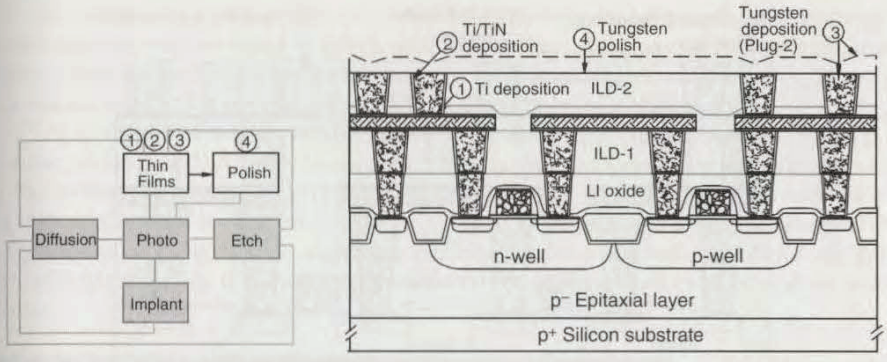
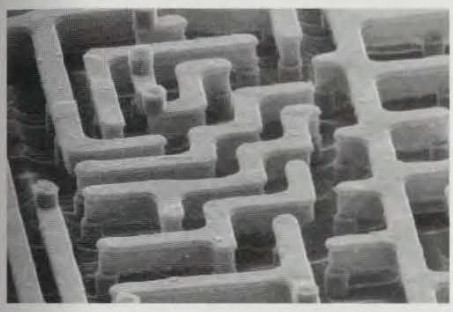


FIGURE 9.27 Plug-2 Formation



SEM Micrograph of First Metal Layer over First Set of Tungsten Vias (Note TiN Cap over Aluminum)
(Micrograph courtesy of Integrated Circuit Engineering)

12. Metal-2 Interconnect Formation

The next series of operations describes the process of forming the interconnects between layers (see Figure 9.28 on page 220). The process is repeated in the same manner for all remaining metal stacks.

Description of Major Steps in Metal-2 Interconnect Formation

Process Step	Description
1. Metal-2 Deposition to Etch	The second metal stack is deposited exactly as the first metal stack. The stack is a composite of three layers—Ti, Al/Cu, and TiN. A plasma etcher is used to etch the Metal-2 lines through windows in the patterned resist.
2. ILD-3 Gap Fill	Following the Metal-2 etch, HDPCVD is used to fill the metal gaps with dense oxide.
3. ILD-3 Oxide Deposition to Polish	ILD-3 oxide is deposited using a PECVD method. This action is followed by polishing the oxide to attain surface planarity.
4. Via-3 Etch, Ti/TiN Deposition, Tungsten Deposition, Polish	Via-3 openings are etched, then these are filled with barrier metal (Ti/TiN). Tungsten is deposited across the wafer surface. The tungsten is polished off the wafer until the ILD-3 oxide layer is reached. Tungsten plugs are left in the vias to provide the interconnect between Metal-2 and Metal-3.

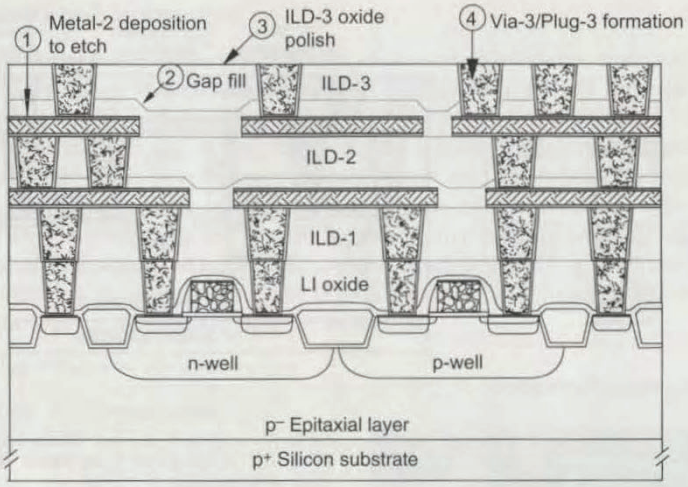


FIGURE 9.28 Metal-2 Interconnect Formation

13. Metal-3 to Pad Etch and Alloy

After repeating the layering process for layers 3 and 4 and at the completion of the Metal-4 etch, ILD-5 oxide is deposited using the thin film process (Figure 9.29). CMP is not required for this dielectric layer because the structures to be patterned are much larger than the quarter micron dimensions formed earlier in the process. The ILD-5 layer is etched to allow metal filling by the Metal-5 deposition. The Metal-5 layer is deposited thicker than previous metal stacks. This metal layer is etched as necessary to form bonding pads and to remove metal from areas where it is not needed.

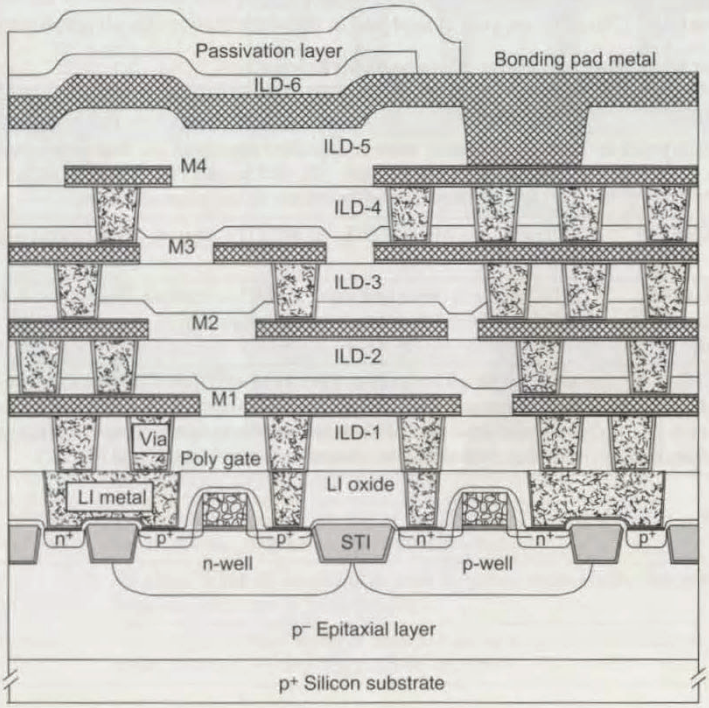
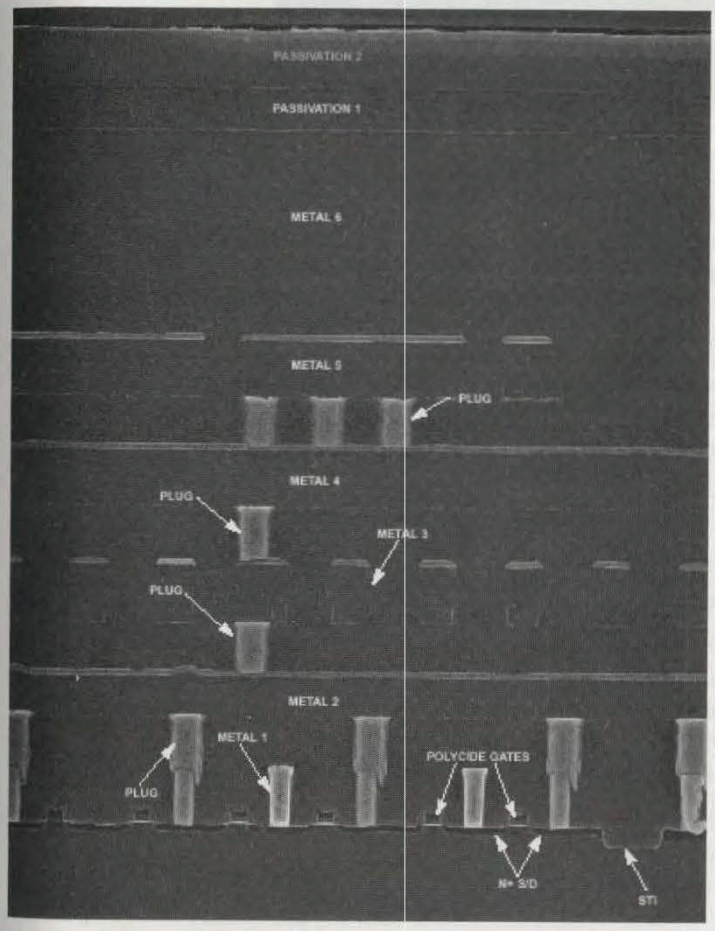


FIGURE 9.29 Full 0.18 μm CMOS Cross Section

This product incorporates 0.18 μm processing technology, including twin-tub technology, retrograde implants, shallow trench isolation, shallow S/D diffused regions, sidewall spacers, titanium silicide contacts, titanium barrier metal, tungsten local interconnect, tungsten plugs, three-layer metal stacks, HDP oxide gap fill, and PECVD oxide as the interlayer dielectric.

The final steps of the process include one more oxide layer (ILD-6) followed by a top layer of silicon nitride (~2000 Å). This layer is referred to as the *passivation layer*. Its purpose is to protect the product from moisture, scratches, and contamination. A final low-temperature alloy step in a diffusion furnace is performed. This heat treatment helps improve the metallurgical bonds between metal connections, thus improving electrical performance and reliability. Care must be taken with this alloy step to prevent overheating the product, which can cause permanent structural defects.



SEM Micrograph of Cross-section of Microprocessor (Micrograph courtesy of Integrated Circuit Engineering)

14. Parametric Testing

The wafer is tested twice to determine its product-worthiness—once when the wafer completes the first metal etch and again after the completion of the last wafer fab process step. Following metal etch, special microprobes connected to electronic test instruments are used to measure certain electrical parameters of specific device test structures on the wafer. This in-line parametric testing procedure is also referred to as *wafer electrical test,* or WET.

INTRODUCTION

Wafer metallization is the deposition of a thin film of conductive metal onto a wafer by use of a chemical or physical process. This process is closely linked to dielectric deposition. Metal lines conduct the signal through the IC circuit while the dielectric layers ensure signals are not influenced by adjacent lines. Both metal and dielectrics are thin film processes. In some cases, metal and dielectrics are deposited by the same type of equipment.

Metallization has unique terminology for the different metal connections. The term *interconnect* describes the conductor materials, such as aluminum, polysilicon, or copper, that create the metal wiring that carries electrical signals to different parts of the chip. Interconnect is also used as a general term for the wiring between devices on a die and the overall package. A *contact* is the electrical connection at the silicon surface between the devices in the silicon wafer and the first metal layer. *Vias* are openings that pass through the various dielectric layers to form an electrical pathway from one metal layer to the adjacent metal layer. A metal *plug* fills the vias to form the electrical connection (interconnect) between the two metal layers. These connections are illustrated in Figure 12.1.

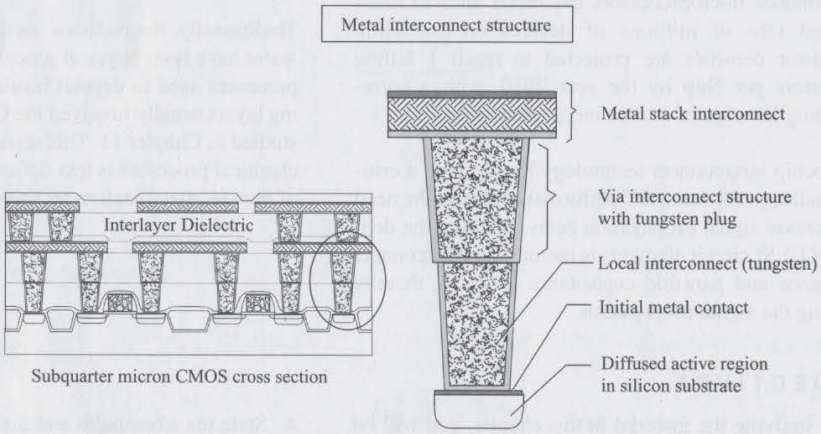


FIGURE 12.1 Multilevel Metallization

The interlayer dielectric (ILD) is an insulating material that electrically separates the metal levels. Once deposited, the ILD is patterned and etched to form via pathways for the various metal layers and the silicon. The vias are filled with a metal, traditionally tungsten (W), to form the via plug. Appreciate that there are many vias on a wafer, up to 10^{11} vias on each individual layer of a 300-mm product wafer.[1] This process of creating vias in the ILD is repeated for every ILD layer on the die. In traditional metallization, a blanket layer of aluminum alloy metal is deposited on the dielectric layer and then patterned and etched to form metal lines. Metal etch is an important technology for traditional metallization.

Metallization is in a transition period and is undergoing rapid change with the introduction of copper metallurgy to replace aluminum alloy. This change is due to the difficulty of etching copper. To overcome this problem, copper metallurgy uses the dual damascene process to form vias and copper interconnects (explained later in this chapter). This metallization process is literally the opposite approach of traditional metallization (see Figure 12.2). Damascene starts with deposition of a blanket dielectric, planarizes the dielectric, patterns and etches holes or trenches in the dielectric for vias and connecting metal lines, deposits blanket metal into the trenches, and then planarizes the metal down to the dielectric to define the metal interconnects.

Metallization technology is critical for increasing performance in advanced ICs, as explained in Chapter 11. Reducing chip performance signal delay caused by interconnect lines was not a significant concern for older IC technologies. The dominant signal delay has traditionally been caused by the device. However, for newer ULSI products manufactured with denser wiring, signal delay

due to interconnect has become a larger portion of the clock cycle time and has more effect on limiting the IC performance.[2]

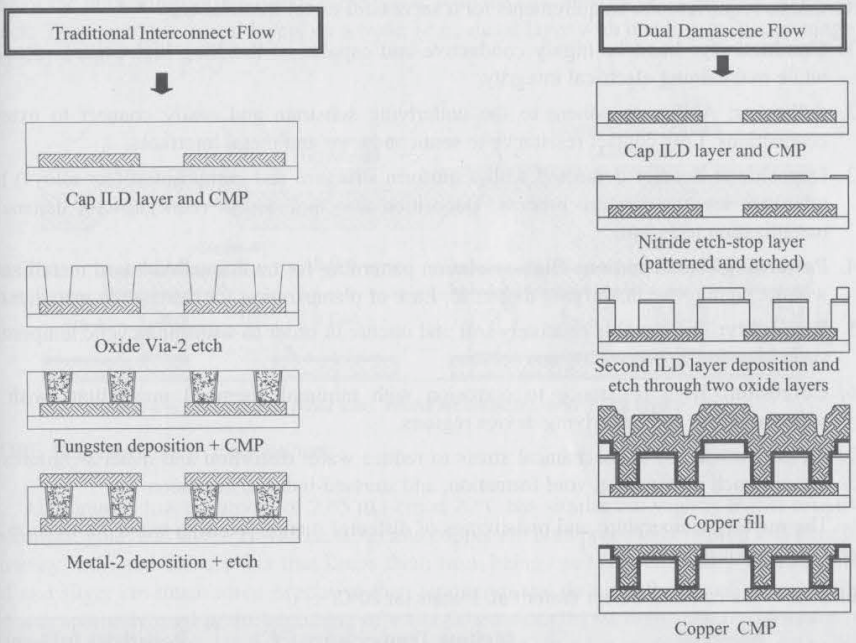
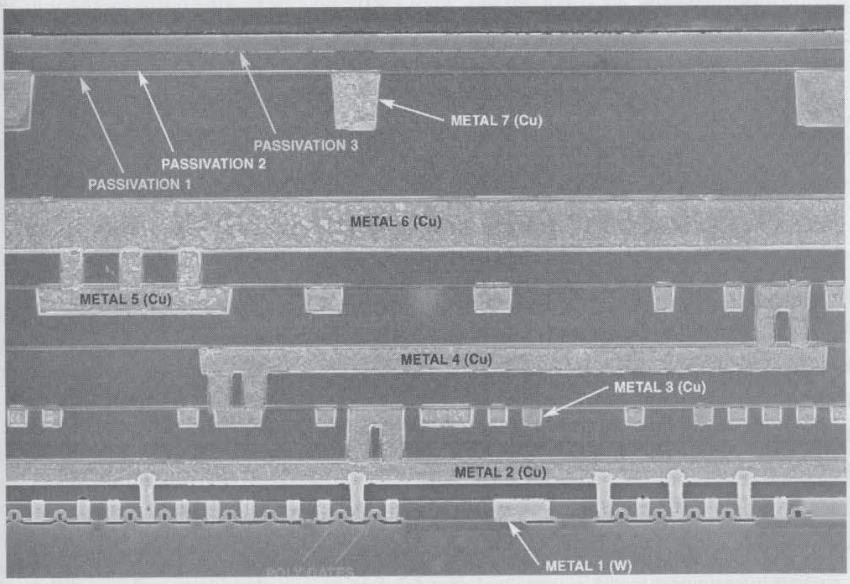


FIGURE 12.2 Traditional Versus Damascene Metallization



Copper Metallization
(Micrograph courtesy of Integrated Circuit Engineering)

TYPES OF METALS

The types of metals and metal alloys used for chip interconnects are evolving based on the performance requirements. Requirements for a successful metal material are:[3, 4]

1. **Conductivity:** Must be highly conductive and capable of handling high current densities while maintaining electrical integrity.
2. **Adhesion:** Ability to adhere to the underlying substrate and easily connect to external connections. Low contact resistance to semiconductor and metal interfaces.
3. **Deposition:** Readily deposited with a uniform structure and composition (for alloys) by a relatively low-temperature process. Deposition into high-aspect ratio gaps for damascene metallization technique.
4. **Patterning/Planarization:** High-resolution patterning for traditional Al-based metallization without etching the underlying dielectric. Ease of planarization for damascene metallization.
5. **Reliability:** The metal is relatively soft and ductile in order to withstand cyclic temperature variations during processing and service.
6. **Corrosion:** High resistance to corrosion with minimal chemical interactions with the adjacent layers and underlying device regions.
7. **Stress:** Resistance to mechanical stress to reduce wafer distortion and material failures for reasons such as cracking, void formation, and stressed-induced corrosion.

The melting temperature and resistivities of different metals found in wafer fabrication and silicon are shown in Table 12.1.[5]

TABLE 12.1 Silicon and Select Wafer Fab Metals (at 20°C)

Material	Melting Temperature (°C)	Resistivity (μΩ-cm)
Silicon (Si)	1412	$\approx 10^9$
Doped Polysilicon (Doped Poly)	1412	≈ 500 to 525
Aluminum (Al)	660	2.65
Copper (Cu)	1083	1.678
Tungsten (W)	3417	8
Titanium (Ti)	1670	60
Tantalum (Ta)	2996	13 to 16
Molybdenum (Mo)	2620	5
Platinum (Pt)	1772	10

The various metals and metal alloys used in wafer fabrication can be grouped into the following categories:

- Aluminum
- Aluminum-copper alloys
- Copper
- Barrier metals
- Silicides
- Metal plugs

Aluminum

The earliest interconnect metal in semiconductor fabrication was aluminum, and it is still the most common interconnect metal in wafer fabrication. Aluminum is projected to continue as the dominant fab interconnect metal for several more years.[6] Copper interconnect metal is expected to replace aluminum for high-performance IC fabrication during the early 2000s. Nevertheless, it is beneficial to review the background into the selection of aluminum for metallization because many of the same basic technical challenges exist today.

Selection of Aluminum ■ Aluminum has been one of the major materials used in wafer fabrication, along with silicon and silicon dioxide. It is used during wafer fabrication in thin film form to interconnect the different devices in the silicon wafer (see Figure 12.3). At the same time, aluminum is one of the thickest films deposited on the wafer, with the first metal layer deposition about 5,000 Å thick. The upper noncritical layers on a wafer (e.g., metal layer with bonding pads) can range up to 20,000 Å thick.

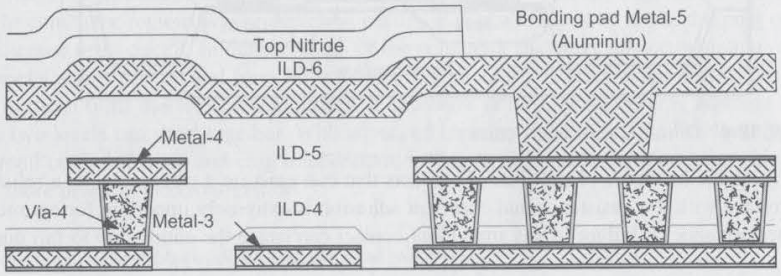


FIGURE 12.3 Aluminum Interconnect

Aluminum's low resistivity of 2.65 μΩ-cm at 20°C has similar but slightly higher resistivity than copper, gold, and silver. However, silver and copper are both prone to corrosion and have high diffusivity in Si and SiO_2, a fact that keeps them from being used for semiconductor fabrication. Gold and silver are much more expensive than aluminum and do not adhere well to oxide films. Gold was sparingly used in the beginning of wafer fabrication, but its high contact resistance with silicon required a platinum barrier metal. On the other hand, aluminum reacts readily with silicon dioxide (SiO_2) when heated to form a thin layer of aluminum oxide (Al_2O_3), which promotes adhesion between the silicon dioxide and aluminum. Aluminum is easily deposited on the wafer and etches in solutions that do not attack underlying films. For these reasons, aluminum was selected as the preferred metal for metallization.

Overall, aluminum is compatible with the major processes in silicon IC fabrication and is relatively inexpensive, making it the choice for metallization since the early days of IC fabrication. However, because of increased circuit density, increased number of metal layers on a wafer, and the reduction in linewidth due to scaling, the metallization technology has evolved from the simple one-level metal layer to a scheme of multiple metal layers. With its lower resistivity, copper is desirable to replace aluminum as the primary interconnect material.

Ohmic Contact ■ Before VLSI circuitry, pure aluminum was used for metallization. Silicon melts at a temperature of 1412°C and pure aluminum melts at 660°C. However, aluminum and silicon alloyed together actually have a lower melting temperature depending on their composition. For an alloy of 88.7% aluminum and 11.3% silicon, the alloy melts at 577°C, which is referred to as the *eutectic temperature*.[7] The eutectic temperature is the lowest temperature that an alloy melts at a particular eutectic composition.

To form a contact between aluminum and silicon, it is necessary to heat the interface, usually in an inert or reducing H_2 atmosphere at a temperature of 450 to 500°C. This thermal bake is also referred to as a low temperature *anneal* or *sinter*. Baking the aluminum on silicon forms a desirable electrical interface referred to as an *ohmic contact*. An ohmic contact has very low resistance (the voltage-current characteristics of the contact interface behave according to Ohm's law). However, there is a small resistance associated with the ohmic contact and it is inversely proportional to the area of the contact. That is, smaller contacts have higher resistance. In modern chip design, ohmic contacts use a special refractory metal (e.g., titanium in the form of a silicide) as a contact at the silicon interface to reduce electrical resistance and improve adhesion (see Figure 12.4 on page 304). Ohmic contacts are fabricated with a salicide (self-aligned silicide) process to achieve optimal positioning above the source/drain and in close proximity to the gate structure. The salicide process is discussed later in this chapter.

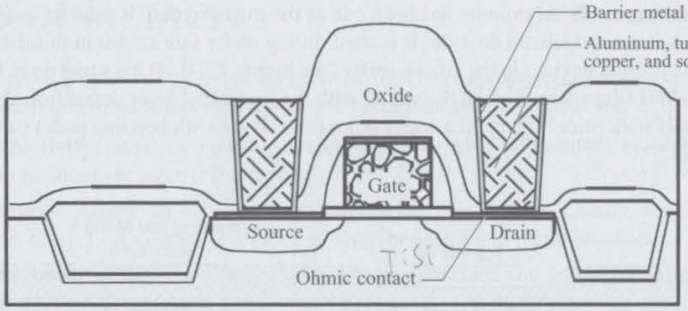


FIGURE 12.4 Ohmic Contact Structure

Given the hundreds of millions of contacts that can exist on a particular die, a reliable contact interface with low resistance and excellent adhesion is extremely important for optimum electrical performance. A failure in any individual contact can cause the entire chip to fail during test or use.

A problem encountered during the earliest work to develop ohmic contacts was undesirable interaction between the aluminum and silicon during the thermal step. This condition led to the microalloying of the contact metal to the silicon, and was referred to as *junction spiking*. Spiking occurs when the interface of pure aluminum and silicon is heated (see Figure 12.5), causing the diffusion of silicon into the aluminum. The amount of silicon dissolved into the aluminum is not uniform and will depend on the time and temperature involved in the heating process. If pure aluminum is heated to 450°C and a source of silicon is present, silicon will begin to dissolve in the aluminum until it reaches a concentration of about 0.5%.[8] The problem is that the source of this silicon is the wafer. As the silicon is dissolved in the aluminum, it leaves behind voids in the wafer, permitting spikes of aluminum to form and penetrate into the silicon contact region. If the aluminum forms an ohmic contact to a shallow junction, the spike may cause a junction short.

The problem of junction spiking was addressed by two methods: the addition of silicon to the aluminum and barrier metallization. The first approach was to use an alloy of aluminum and silicon instead of pure aluminum. If there is already silicon in the aluminum, this will slow down the dissolution of additional silicon from the substrate. However, silicon alloying in aluminum is limited and can lead to silicon nodule formation (small regions of high silicon concentration) in the aluminum due to silicon condensation. Nodule formation can significantly increase the contact resistance and pose a serious reliability concern from local heating at the nodules. The main method to resolve junction spiking was the introduction of barrier metallization to inhibit diffusion (see the following section).

It is important that the oxide at the contact interface be as thin as possible. Wafers with exposed contact regions are often dipped in a dilute hydrofluoric (HF) acid solution immediately before placing the wafers in the deposition chamber. This serves to remove the native oxide layer prior to contact formation.

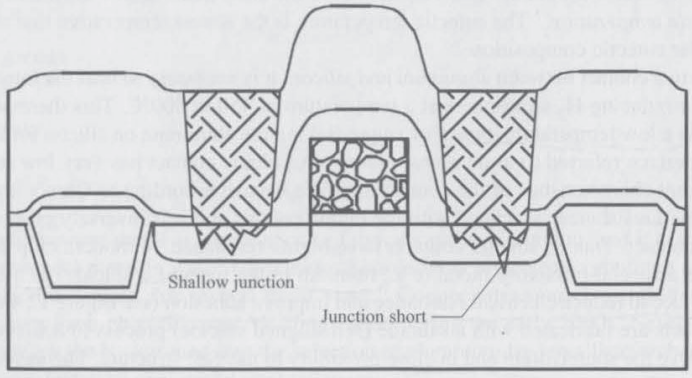


FIGURE 12.5 Junction Spiking

Aluminum-Copper Alloys

Aluminum metal was selected as the primary interconnect material for ICs because of its low resistivity and its compatibility with silicon and the wafer fabrication process. However, aluminum suffers from a reliability problem known as *electromigration*. This is the movement of aluminum atoms in the conductor due to momentum transfer from the electrons carrying the current.[9] Under high current-density conditions, electrons collide with aluminum atoms, causing the atoms to gradually move. This movement of atoms leads to a depletion of atoms at the negative end of the conductor. In conductor regions where depletion occurs, this action leads to voids, thinning of lines, and a potential open circuit. In other regions of the conductor that have an accumulation of metal atoms, metal atoms pile up and form hillocks (see Figure 12.6).[10] *Hillocks* are protrusions on the surface of metal films due to electromigration. If excessive or large hillocks form, adjacent lines or lines on two levels can short together. With advanced circuitry designs in ULSI technology, there is increased current density and chip temperature, both of which make the aluminum chip metallization more prone to electromigration.

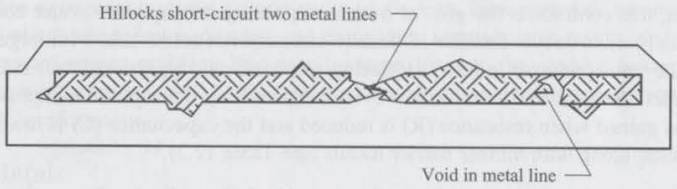


FIGURE 12.6 Hillock on a Metal Line

Electromigration in interconnects is controlled by alloying the aluminum with between 0.5 to 4% copper. This alloying essentially increases the conductor's current-carrying capacity by reducing the grain boundary diffusion effects in the aluminum. At the same time, it has been shown that values of copper in aluminum greater than 8% will actually increase electromigration.[11] The exact reason why the addition of copper reduces the chance of electromigration failure in Al-Cu alloys is not well understood.[12] If copper is alloyed with aluminum, more care must be given to plasma etching this alloyed aluminum (etching is discussed in Chapter 16). Copper is difficult to etch, and any residual copper remaining after etching the aluminum alloy interconnect can promote corrosion.[13] It is also possible to have electromigration in contacts and vias. Electromigration failure in contacts is resolved by the use of barrier metallization.

Electromigration is probably one of the most widely studied failure mechanisms of integrated circuits. Studies of this failure began in the 1950s with the development of the semiconductor and intensified in the late 1960s with the discovery of crack formation in the aluminum conductor leading to failures.[14] The significance of electromigration is that it usually occurs after the chip has been in service for an amount of time, which means that failure occurs catastrophically during customer usage.

Copper

A major transformation is underway in IC design and fabrication by means of the introduction of *copper interconnect* technology. Copper interconnects will replace aluminum metallization with copper to achieve significant benefits in chip performance. A legitimate question that someone may pose is why introduce copper if aluminum has performed so admirably over the years.

Need for Copper ■ The benefits for introducing copper for IC interconnect metallization are:[15]

1. **Reduction in resistivity.** The interconnect wiring resistivity reduces from 2.65 μΩ-cm for aluminum to 1.678 μΩ-cm at 20°C for copper, reducing RC signal delay and increasing chip speed.
2. **Reduction in power consumption.** Narrower lines consume less power.

3. **Tighter packing density.** Narrower lines permit tighter circuitry packing, which means that fewer levels of metal are needed.
4. **Superior resistance to electromigration.** Copper does not have a concern for electromigration.
5. **Fewer process steps.** Potential for 20 to 30% fewer processing steps with damascene processing of copper.

As wafer fabrication design rules reduce to 0.15-μm linewidths and below, the increased packing density of devices on the chip permits more electrical signal speed from device to device (the transistors are closer; therefore, the signal has less distance to travel). This density leads to improved chip performance. However, this improved chip performance is only possible if the interconnect system between the devices is optimized. Narrower linewidths lead to increased line resistance. Tightly spaced conductor lines with a dielectric material between them act as capacitors, leading to a degradation in performance from an increase in resistance (R) and capacitance (C). This condition is the signal delay or interconnect delay discussed in Chapter 11. If either or both of these two parameters are reduced, then the signal delay reduces, leading to increased chip performance.

One possible method reducing interconnect resistance is to increase the conductor cross section. However, this contradicts the goal of increased packing density since wider conductors will take substantially more space. Smaller IC feature sizes are not achievable with larger linewidths. This is why the semiconductor industry is placing emphasis on copper—to lower the interconnect resistance, which lowers R and therefore the overall signal delay. The optimum improvement to RC signal delay is gained when resistance (R) is reduced and the capacitance (C) is lowered by using a low-*k* dielectric along with thinner barrier metals (see Table 12.2).[16]

TABLE 12.2 Change in Interconnect Delay Compared to 0.25-μm Device Generation

Technology	0.25 μm	0.18 μm	0.13 μm
Conventional Interconnect Technology: • Al/Cu interconnect alloy and TiN barrier metal	0	+21%	+93%
New Technology Introduced by Generation: • Reduced barrier thickness • Low-*k* (3.0) dielectric • Dual damascene Cu interconnect and plugs	−10%	−27%	−16%

Another benefit from the implementation of copper is that smaller linewidths can carry the same amount of current, permitting a tighter packing density on each metal level. This condition produces fewer overall levels of metal on a chip, leading to significantly reduced manufacturing costs.[17]

Copper is a relatively soft metal. It has superior resistance to electromigration, a common reliability problem with aluminum.[18] This means that chips fabricated with copper can handle higher electrical power densities, which permits the development of new product applications. Table 12.3 compares Cu and Al for different properties and processes common in wafer fabrication.[19]

TABLE 12.3 Comparison of Properties/Processes Between Al and Cu

Property/Process	Al	Cu
Resistivity (μΩ-cm)	2.65 (3.2 for Al—0.5% Cu)	1.678
Electromigration resistance	Low	High
Corrosion resistance (in air)	High	Low
Etch processing	Yes	No
CMP (chemical mechanical planarization) processing	Yes	Yes

Copper Challenges ■ There are three major challenges involved with using copper as semiconductor interconnects that distinguish it from traditional aluminum interconnects. These three challenges differ significantly from aluminum technology and must be resolved before the implementation of copper for IC interconnects:[20]

1. Copper diffuses quickly into oxides and silicon. This is a concern if copper diffuses into the active region of the silicon (i.e., source/drain/gate region of the transistor) because it will damage the device by creating junction or oxide leakage.
2. Copper cannot be easily patterned using regular plasma etching techniques (see Chapter 16 for a discussion of etching). Copper dry etching does not produce a volatile by-product during the chemical reaction that is necessary for economical dry etching.
3. Copper oxidizes quickly in air at low temperatures (<200°C) and does not form a protective layer to stop further oxidation.

These challenges are addressed by converting to dual damascene processing with special barrier metals optimized for copper. Damascene processing eliminates the need to etch copper. Furthermore, tungsten plugs are expected to be used as the first level of metal to contact the source, drain, and gate regions.[21] This use of tungsten overcomes the concern of copper contaminating the silicon (referred to as copper poisoning). The tungsten may even be patterned for wiring of the local interconnect (LI). All other metal lines and vias for the multiple metal layers are expected to be copper.

Another major hindrance to converting to copper in semiconductor manufacturing is the natural reluctance to introducing new materials into production. New materials means there are new sources of contamination, new equipment and procedures, unpredictable results, and so on. Change always brings unforeseen problems that pose increased risks to the semiconductor manufacturer. However, these risks are balanced by the benefits from changing the interconnect material in order to improve IC performance.

Barrier Metals

A more effective way to make reliable ohmic contacts to shallow junctions without material diffusion or problems such as junction spiking is to use barrier metallization. A *barrier metal* is a thin layer of deposited metal or metals that is designed to prevent intermixing of the materials above and below the barrier (see Figure 12.7). The thickness of barrier metals has typically been around 100 nm for features sizes in the 0.25-μm generation, which is substantially thinner than the 400 to 600 nm thickness required for 0.35-μm generation of devices. Thickness of barrier metals is projected to decrease to 23 nm or less for the 0.18-μm technology node and beyond.[22]

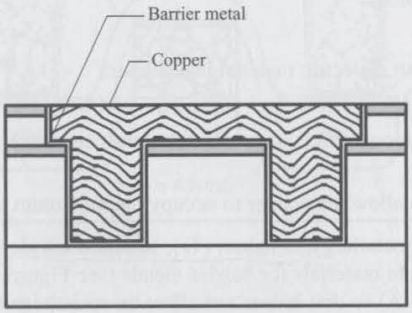


FIGURE 12.7 Barrier Layer for Copper Interconnect Structure

Barrier metals are widely used in semiconductor manufacturing. For contacts between the tungsten (W) plug that connects the aluminum interconnect wiring and the silicon source/drains, the barrier metal prevents the silicon and W from coming into contact with each other. This barrier prevents diffusion between the W and silicon and any junction spiking.

The essential properties of an acceptable barrier layer metal are:

1. Good diffusion barrier properties so that the diffusivity of the two interface materials (e.g., tungsten and silicon) is low at the sintering temperature (*sintering* refers to joining the materials by thermal means).
2. High electrical conductivity with low ohmic contact resistance.
3. Good adhesion between the semiconductor and the metal.

4. Resistance to electromigration.
5. Stability when thin and at high temperature.
6. Resistance to corrosion and oxidation.

Metals commonly used for barrier metals are a class of high melting point metals known as *refractory metals*. Common refractory metals used in multilevel metallization for wafer fabrication are titanium (Ti), tungsten (W), tantalum (Ta), molybdenum (Mo), cobalt (Co), and platinum (Pt). Refractory metals have been used in wafer fabrication since the 1960s, such as in the formation of Schottky barrier diodes in bipolar processes. The benefits of using titanium as a barrier metal for aluminum alloy wiring are improved adhesion, reduced contact resistance, reduced stress, and controlled electromigration. To achieve good barrier properties, wafers undergo a clean step (referred to as *sputter etch* and explained in a later section) before deposition in the processing chamber to remove native oxides and oxide residues on the wafer.

Titanium tungsten (TiW) and titanium nitride (TiN) are two common barrier metal layers that inhibit diffusion between the silicon substrate and aluminum. TiN is widely used in ULSI manufacturing for its superior barrier performance in aluminum alloy interconnect processing. TiN functions as a barrier metal for both tungsten and aluminum. TiN is also widely used as an antireflective coating on aluminum to improve the photolithography patterning process (see Chapter 14). However, TiN does not produce good contact resistance to silicon. To resolve this problem, a thin layer of titanium (e.g., several hundred angstroms or less) is typically deposited before the TiN so that it can react with the underlying material as a silicide (see the following section for an explanation of silicide) and lower the contact resistance. The Ti and TiN are typically deposited in a cluster tool to keep oxides from forming between the two layers.

Copper Barrier Metals ■ Barrier metals are critical for copper metallurgy. Cu has high diffusivity in silicon and silicon dioxide, which will destroy device performance. Traditional barrier metals are not sufficient barriers for copper. Cu requires complete encapsulation by a thin-film barrier layer that functions as an adhesion promoter and effective diffusion barrier.[23] There is a trade-off between these two requirements since good adhesion requires some reaction with Cu, whereas a good barrier metal should not react with Cu. The special barrier metal requirements for copper are:[24]

1. Prevent copper diffusion.
2. Low film resistivity.
3. Good adhesion to both dielectric material and copper.
4. Compatible with chemical mechanical planarization (CMP).
5. Metal layer is continuous and conformal with good step coverage and deposition in high aspect ratio gaps.
6. Minimal thickness to allow the copper to occupy the maximum cross-sectional area.

For Cu interconnect metallurgy, tantalum (Ta), tantalum nitride (TaN), and tantalum silicon nitride (TaSiN) are candidate materials for barrier metals (see Figure 12.8). The diffusion barrier must remain thin (about 75 Å) so that it does not affect the resistivity of the high-aspect ratio plug while still acting as a barrier metal. This condition is difficult to maintain as geometries continue to shrink and metals are deposited into high-aspect ratio vias. Research has shown Ta has good barrier and adhesion properties for copper, whereas TiN, a traditional barrier metal for Al/SiO_2 interconnects, has good barrier properties but poorer adhesion.[25] If TaN is used, it is obtained by small amounts of nitrogen doping or by deposition with a tantalum nitride compound. Investigations have also shown tungsten nitride (WN) functions as an effective barrier for Cu metal.[26] There is ongoing research in the development of barrier metals for Cu metallurgy.

Copper barrier layers can be deposited by using high-density plasma CVD (HDPCVD) or ionized metal plasma physical vapor deposition. Ionized metal plasma PVD for tantalum achieves good step coverage. For deposition with high aspect ratio gaps, then HDPCVD barrier deposition is often the choice.[27]

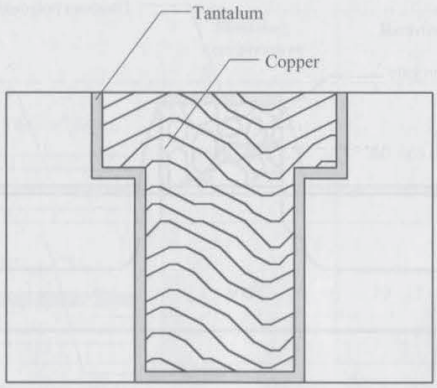


FIGURE 12.8 Ta for Copper Barrier Metal

Silicides

Refractory metals react with silicon when alloyed together to form a silicide. A *silicide* is a metal compound that is thermally stable and provides for low electrical resistivity at the silicon/refractory metal interface (see Figure 12.9). Refractory metal silicides are important in wafer fabrication because of the need to reduce the electrical resistance of the many silicon contacts in the source/drain and gate regions for chip performance. Titanium and cobalt are common refractory metal used for contacts in aluminum interconnect technology.

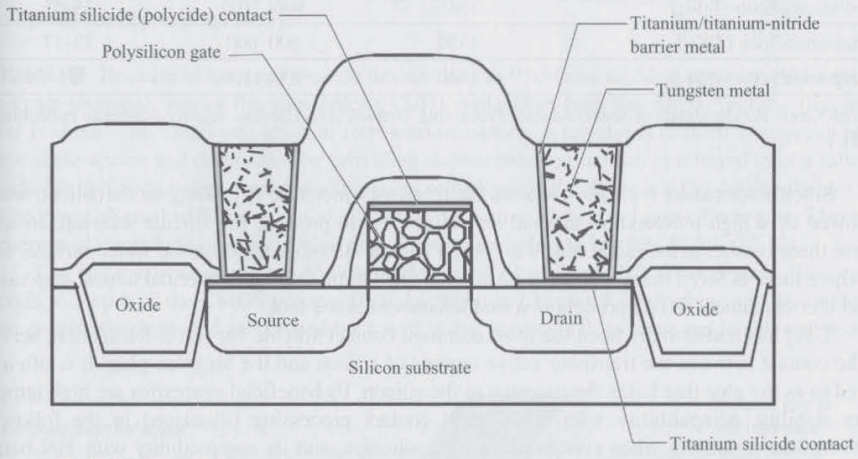


FIGURE 12.9 Refractory Metal Silicide at a Silicon Contact

If the refractory metal is reacted with polysilicon, it is called a *polycide* (see Figure 12.10 on page 310). Doped polysilicon is used as the gate electrode and has a relatively high resistivity (about 500 $\mu\Omega$-cm), which leads to an undesirable RC signal delay. A polycide is beneficial for reducing the series resistance of an interconnection to polysilicon. At the same time, it maintains polysilicon's good interfacial characteristics to oxides.

Silicides improve contact resistance by reducing residual oxides on the silicon surface during silicide formation. Silicides form extremely good metallurgic contact to the silicon, serving as a critical adhesion layer between the contact metal and the silicon junction regions. Many silicides are stable at temperatures exceeding 1000°C with a relatively high eutectic temperature. Table 12.4 on page 310 lists some properties of common silicides used in wafer fabrication.[28] Recall that the eutectic temperature is the lowest temperature where the alloy melts. It is undesirable for the silicide to melt because the liquid alloy can extend into the substrate material and cause junction spiking.

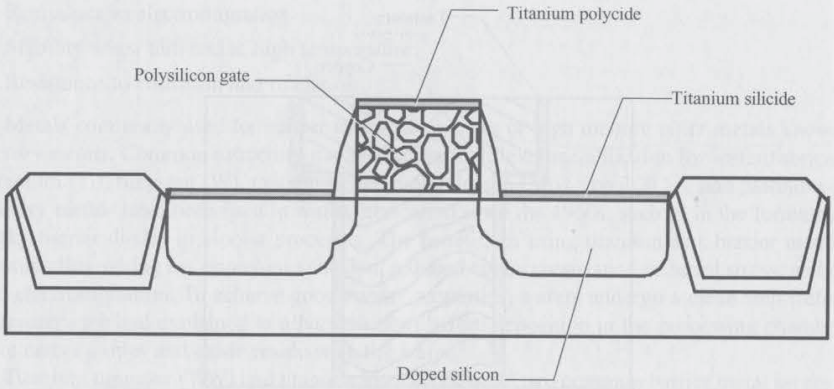


FIGURE 12.10 Polycide on Polysilicon

TABLE 12.4 Some Properties of Select Silicides

Silicide	Lowest Eutectic Temperature (°C)	Typical Forming Temperature* (°C)	Resistivity (μΩ-cm)
Cobalt/silicon ($CoSi_2$)	900	550–700	13–19
Molybdenum/silicon ($MoSi_2$)	1410	900–1100	40–70
Platinum/silicon (PtSi)	830	700–800	28–35
Tantalum/silicon ($TaSi_2$)	1385	900–1100	35–55
Titanium/silicon ($TiSi_2$)	1330	600–800	13–17
Tungsten/silicon (WSi_2)	1440	900–1100	31

* B. El-Kareh, *Fundamentals of Semiconductor Processing Technologies,* (Boston: Kluwer Academic Publishing 1995), p. 537.

Silicide formation typically requires the refractory metal be deposited on the silicon wafer, followed by a high temperature thermal anneal process to produce the silicide material. In areas where there is silicon, the metal reacts to form a silicide. In other areas on the wafer surface, such as where there is SiO_2, there is little or no silicide formation. Often this thermal anneal step uses a rapid thermal anneal (RTA) process in a multichamber cluster tool.

$TiSi_2$ has traditionally been the most common contact silicide for wafer fabrication, serving as the contact between the transistor active regions of silicon and the tungsten plug. It is often referred to as the glue that holds the tungsten to the silicon. Its beneficial properties are high temperature stability, compatibility with self-aligned contact processing (discussed in the following section), low resistivity when compared to other silicides, and its compatibility with TiN barrier metals.[29] $TiSi_2$ forms two different grain phases (a phase is a physically homogeneous material state) as it is annealed, a low-temperature C49 phase and a high-temperature C54 phase (see Figure 12.11). Both of these phases are $TiSi_2$.

The C49 phase of $TiSi_2$ forms at an anneal temperature of 625 to 675°C with a resistivity of 60 to 65 μΩ-cm. The C54 phase is formed in a second anneal following the C49 phase formation and requires a temperature of 800°C or more. It has a much lower resistivity of only 10 to 15 μΩ-cm, which is desirable to lower the overall contact resistance.[30]

However, at the time of this writing, $TiSi_2$ appears limited in its future use as a contact silicide in sub-0.25 μm technologies. Contacts for ultrashallow source/drain junctions are becoming thin. $TiSi_2$ is undesirable for thin contacts because the silicide resistivity increases.[31] It is also difficult to form this contact during the second anneal because of critical time at temperature requirements.

The silicide that appears promising for the 0.18 μm and below technology nodes is cobalt silicide ($CoSi_2$). This silicide maintains a reduced contact resistance of 13 to 19 μΩ-cm after its

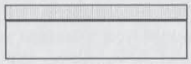
	Sintering Temperature	Resistivity
$TiSi_2$ – C49 	625 – 675°C	60 – 65 μΩ-cm
$TiSi_2$ – C54 	800°C	10 – 15 μΩ-cm

FIGURE 12.11 Anneal Phases of $TiSi_2$

anneal operation, even with deep submicron geometries of 0.18 μm and less. This reduced resistivity occurs because the grain size of $CoSi_2$ is about ten times smaller than the grain size of $TiSi_2$. Therefore, the low resistance phase is completely nucleated and grown during the thermal anneal operation. A $CoSi_2$ contact is also easier to form because of the smaller grain size.

Note that a silicide is not a barrier metal. In some silicides it is found that silicon diffuses rapidly through them. This diffusion occurs during heat treatment of the metal-silicide-silicon system where silicon diffuses through the silicide to the metal, which then reduces the integrity of the system. The solution to this problem is to place a metal barrier layer between the silicide and the metallization layer (discussed in the preceding section). A common silicide barrier film is titanium nitride (TiN), which is effective for both tungsten and aluminum. A tantalum-based barrier layer is anticipated for copper metallurgy.

Salicide ■ Because of the need to scale device sizes in VLSI and ULSI to optimize performance, the cross-sectional area of the source/drain (S/D) contact between the silicon and the first metal layer is small. This small size leads to increased resistance. A technique to decrease contact resistance at the source and drain areas by providing stable contact structures is referred to as a salicide. A *salicide* approach (taken from the expression *self-aligned silicide*) is used to create silicides that are properly aligned with the exposed silicon of the source, drain, and polysilicon gate. There are numerous chip performance issues that depend on salicide formation (see Figure 12.12).

The basic salicide steps are shown in Figure 12.13 on page 312. This process flow corresponds to Step 6 of the CMOS process flow described in Chapter 9. To form a salicide, oxide has been previously deposited and etched back with a dry plasma etch to leave oxide sidewall spacers

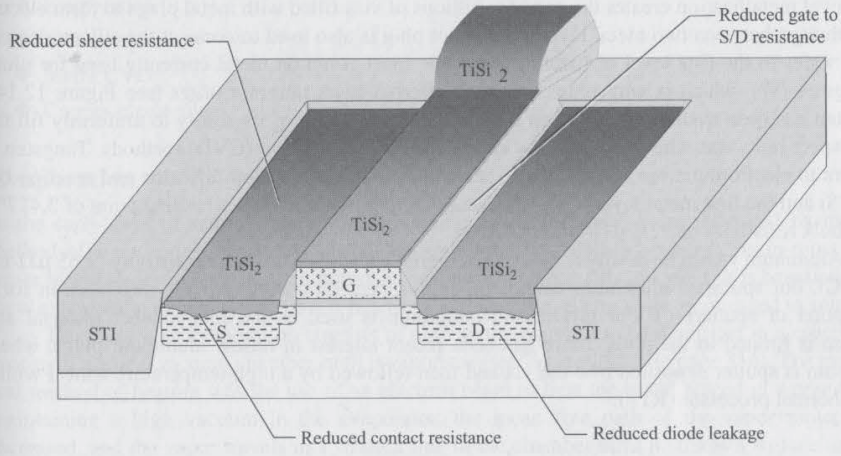


FIGURE 12.12 Chip Performance Issues Related to a Salicide Structure

on the side of the polysilicon gate (Step 5 of the CMOS process flow described in Chapter 9). With the sidewall spacers, only the top poly surface of the gate is exposed. After an HF-dip clean step to remove native oxides, a 250 to 350 Å thin layer of titanium metal is deposited on the wafer. The refractory metal undergoes an RTP rapid anneal at 600 to 800°C to create the high-resistivity C49 titanium silicide phase wherever the refractory metal contacts silicon. The sidewall spacer keeps the S/D $TiSi_2$ from shorting out to the sides of the gate poly, while the oxide of the shallow trench isolation separates the devices. After the first RTP anneal, all unreacted titanium is removed by a wet chemical etch in ammonium hydroxide (NH_4OH) and hydrogen peroxide (H_2O_2). $TiSi_2$ remains and covers the S/D areas and top surface of the poly gate. A second RTP silicide anneal at 800 to 900°C creates the low-resistivity C54 metallic silicide. A major benefit of the salicide process is the avoidance of alignment tolerances that would occur if patterning were required to align the refractory metal on the silicon contact. Care must be taken during the anneal steps to avoid oxygen contamination in the furnace tube. Titanium reacts easily with oxygen to form undesirable titanium oxides. This oxide contamination can promote silicide formation on top of the oxide spacer regions, leading to a short between the polysilicon gate and source or drain.

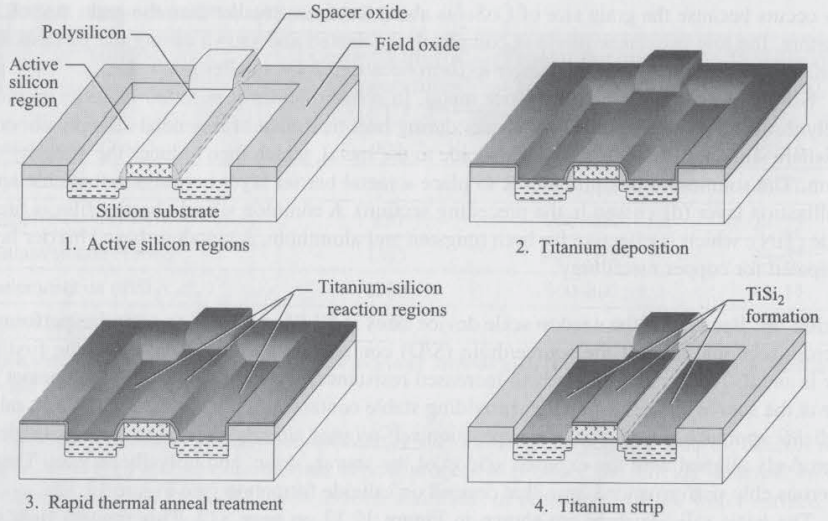


FIGURE 12.13 Formation of Self-Aligned Metal Silicide (Salicide)

Metal Plugs

Multilevel metallization creates the need for billions of vias filled with metal plugs to form electrical pathways between two metal layers. A contact plug is also used to connect the silicon devices in the wafer to the first level of metallization. The most common metal currently used for plugs is tungsten (W), which is why plugs are often referred to as *tungsten plugs* (see Figure 12.14). Tungsten has been traditionally used as a plug material because of its ability to uniformly fill the high-aspect ratio vias when deposited by chemical vapor deposition (CVD) methods. Tungsten is resistant to electromigration failure. It also serves as a barrier to inhibit diffusion and reaction between Si and the first metal layer. Tungsten is a refractory material with a melting point of 3,417°C and a bulk resistivity of 52.8 μΩ-cm at 20°C.

Aluminum would be desirable as a plug material because of its lower resistivity (2.65 μΩ-cm at 20°C), but sputtered aluminum cannot fill high-aspect ratio vias (see the next section for a description of sputtering). For this reason aluminum is used as the interconnect material and tungsten is limited to the plug. There has been recent interest in reflow aluminum plugs, where aluminum is sputter deposited into the via and then reflowed by a high-temperature anneal with a rapid thermal processor (RTP).[32]

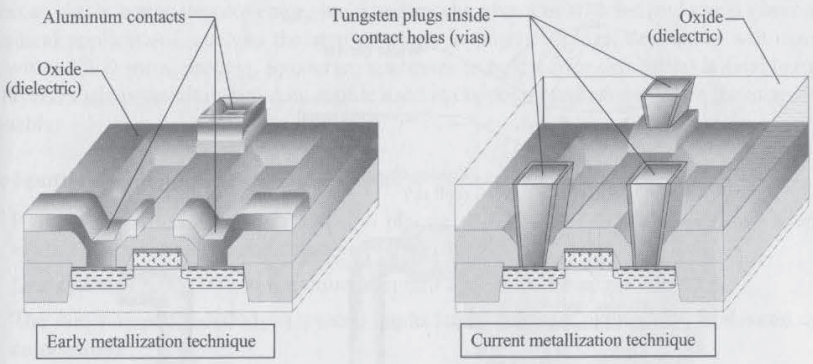


FIGURE 12.14 Tungsten Plug for Multilevel Metal Layers

METAL DEPOSITION SYSTEMS

The traditional metallization techniques used in semiconductor manufacturing fall under a category called *physical vapor deposition* (*PVD*). PVD has been done with filament evaporation, followed by electron beam evaporation and, most recently, sputtering. Chemical vapor deposition (CVD) has recently become a frequently used technique to deposit metal films. Each change in the deposition system has brought improved control of thin film properties and quality.

During the SSI and MSI eras of semiconductor manufacturing, evaporation was the method for metallization. It was replaced by sputtering primarily because evaporation has poor step coverage. Evaporation is still used in research applications and for semiconductors using III–V technologies. It is also used in some specialized areas, such as for C4 bump deposition during packaging (see Chapter 20).

Electroplating technology has been employed in various applications. In recent years it has been used for thin film head metallization in the disk drive industry. However, electroplating is just now being introduced for semiconductor manufacturing as a copper deposition method. It is the early deposition method of choice for creating copper interconnects.

The different metal deposition systems used in traditional and dual damascene metallization are:

- Evaporation
- Sputtering
- Metal CVD
- Copper electroplate

Evaporation

In the early days of semiconductor manufacturing, all metal layers were deposited by the PVD method of *evaporation.* Since the late 1970s, sputtering has replaced evaporation in most silicon wafer technologies in order to gain improved step coverage, gap fill, and yield. It is beneficial to review evaporation to understand how it functions and why the silicon industry changed to sputtering.

The process of evaporation consists of placing the material to be deposited in a crucible and heating it inside a vacuum chamber until it vaporizes (see Figure 12.15 on page 314). The most typical method of heating was the use of an electron beam to heat the metal placed in a crucible. By maintaining a high vacuum in the evaporator, the mean free path of the vapor molecules is increased, and the vapor travels in a straight line in the chamber until it strikes a surface and condenses to form a film.