

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Taiwan Semiconductor Manufacturing Company Ltd.,

Petitioner,

v.

Marlin Semiconductor Ltd.,

Patent Owner.

Patent No. 8,076,194 B2

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Title: METHOD OF FABRICATING METAL OXIDE SEMICONDUCTOR
TRANSISTOR

Inter Partes Review No. IPR2026-00061

**DECLARATION OF PROF. EUGENE FITZGERALD, PH.D.,
IN SUPPORT OF PETITION FOR *INTER PARTES* REVIEW OF
UNITED STATES PATENT NO. 8,076,194**

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I, Prof. Eugene Fitzgerald, Ph.D., declare as follows:

I. Introduction

1. My name is Eugene Fitzgerald. I have been asked to submit this declaration on behalf of Taiwan Semiconductor Manufacturing Company Limited (“TSMC”) in connection with a petition for *inter partes* review of U.S. Patent No. 9,076,194 (“’194 Patent”), which I have been told is being submitted to the Patent Trial and Appeal Board of the United States Patent and Trademark Office.

2. TSMC has retained me as a technical expert to study and provide my opinions on the technology covered by, and the patentability or non-patentability of, claims 1-22 of the ’194 Patent (“Challenged Claims”).

3. This declaration is directed to the Challenged Claims and sets forth certain opinions I have formed, the conclusions I have reached, and the basis for each.

4. Based on my experience, knowledge of the art at the relevant time, analysis of prior art references, and the understanding a person of ordinary skill in the art would have had regarding the claim terms in light of the specification, it is my opinion that each of the Challenged Claims of the ’194 Patent is unpatentable for at least the reasons I discuss below.

II. Background and Qualifications

A. Education and Career

5. I have summarized in this section my educational background, career history, and other relevant qualifications.

6. I have over 30 years of academic and industrial experience in designing, applying, studying, teaching, manufacturing, and writing about semiconductor devices, microprocessors, and computer chip technologies, including the design, process integration, fabrication, and yield of various types of transistors.

7. I received a B.S. in Materials Science and Engineering from the Massachusetts Institute of Technology (“MIT”) in 1985, a M.S. in Materials Science and Engineering from Cornell University in 1987, and a Ph.D. in Materials Science and Engineering from Cornell University in 1989.

8. From 1988 to 1994, I worked as a research scientist at AT&T Bell Laboratories in Murray Hill, N.J., in the Materials Science and Engineering Department. While at AT&T Bell Laboratories, I conducted fundamental research in semiconductor materials and devices, specifically the use epitaxial layers in field effect transistors (“FETs”).

9. From 1994 to 2000, I was an Associate Professor at MIT. From 2000 to the present, I have been a Professor of Materials Science at MIT, in the Materials Science and Engineering Department. I am currently the Merton C. Flemings-

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Singapore-MIT-Alliance Professor of Materials Engineering. Through 2022, I was Lead Principal Investigator of MIT SMART LEES (Singapore- MIT Alliance for Research and Technology, MIT's Research Center in Singapore, Low Energy Electronic Systems), where I managed the ninety- million-dollar research program (2011-2025).

10. Of specific relevance to this case, my research involves studying semiconductor structures with strained materials, and specifically the use of epitaxially grown germanium alloys—such as silicon germanium (“SiGe”)—to strain semiconductor devices. The use of epitaxial SiGe to form source/drain regions that strain the channel in Metal-Oxide-Semiconductor (“MOS”) transistors, was technology developed by at least the year 2000 (about seven years before the earliest claimed priority date for the '194 Patent).

11. Early on my research group studied (and we continue to work on) epitaxy growth of SiGe on silicon substrates. (See, for example, Z. Cheng, E.A. Fitzgerald & D.A. Antoniadis, “SiGe-On-Insulator (SGOI) Technology and MOSFET Fabrication,” Advanced Materials for Micro- and Nano-Systems (AMMNS) (2002); O. Kwon, J.J. Boeckl, M.L. Lee, A.J. Pitera, E.A. Fitzgerald & S.A. Ringel, “Monolithic Integration of AlGaInP Laser Diodes on SiGe/Si Substrates By Molecular Beam Epitaxy,” Journal of Applied Physics, vol. 100, no. 1 (2006); J. Wang, C. Heidelberger, E.A. Fitzgerald & N.J. Quitoriano, “Liquid Phase Epitaxy

SiGe Films on a CVD-Grown SiGe/Si (001) Graded Film,” Journal of Crystal Growth, vol. 535, 125541 (2020).)

12. I have received numerous honors and awards for my work. For example, I was a co-recipient of the Institute of Electrical and Electronics Engineers (“IEEE”) 2011 Andrew S. Grove Award for outstanding contributions to solid state devices and technology including “seminal contributions to the demonstration of Si/Ge lattice mismatch strain engineering for enhanced carrier transport properties in MOSFET devices,” the IEEE 2004 EDS George Smith Award for Best Paper for a paper I co-authored entitled “Fully Depleted Strained-SOI n- and p- MOSFETs on Bonded SGOI Substrates and Study of the SiGe/BOX Interface,” and the TMS 1994 Robert Lansing Hardy Medal Award for exceptional promise of a successful career in the field of metallurgy and materials science.

13. I am the founder, co-founder, or a founding team member of the following companies and organizations: AmberWave Systems Corporation (a company focused on strained silicon semiconductor technology); Contour Semiconductor (a company focused on a unique semiconductor fabrication process for non-volatile memory); 4Power LLC (manufacturer of high efficiency, low cost solar cells using III-V thin films on silicon substrates); Paradigm Research LLC (commercializing true monolithic III-V/Si CMOS integrated circuits); The Innovation Interface (a not-for-profit organization that trains future innovators

through university-corporate innovation projects); The Water Initiative (creating customized point-of-drinking water solutions and scaling those solutions through micro-entrepreneurs, developers and government entities), and New Silicon Corporation Pte. Ltd. (III-V+CMOS integrated circuit company).

14. A full list of my research and professional experience, my expert witness or consultant experience, and other activities and awards is further detailed in my curriculum vitae, which I understand is being included as Exhibit 1004.

15. As a co-founder, professor, and inventor myself, I am familiar with patents, the patent process, patent claims, and patent analysis.

B. Publications

16. A list of the publications that I have authored and patents I have been awarded during my technical career can be found in my Google Scholar Profile <https://scholar.google.com/citations?hl=en&user=YsZ6EjkAAAAJ>.

17. I am a named inventor on over 100 granted United States patents and have authored over 700 peer-reviewed academic journal publications. I have coauthored several publications on strained silicon transistors. For example, I co-authored the book *Silicon Heterostructure Handbook: Materials, Fabrication, Devices, Circuits and Applications of SiGe and Si Strained-Layer Epitaxy*, published in 2018 by CRC press. I also have patents specifically discussing SiGe/silicon strain technology, gate sidewall spacer formation, and lightly doped drains, metal gate

electrodes, and MOSFET transistors, all of which are relevant technologies in this case. Some examples of my relevant patents and publications that predate the '194

Patent are:

- Y.J. Mii, Y.H. Xie, E.A. Fitzgerald, D. Monroe, F.A. Thiel, B.E. Weir & L.C. Feldman, "Extremely High Electron Mobility in Si/Ge_xSi_{1-x} Structures Grown by Molecular Beam Epitaxy," Applied Physics Letters, vol. 59, no. 13, pp. 1611-13 (1991).
- M.L. Lee & E.A. Fitzgerald, "Optimized Strained Si/Strained Ge Dual-Channel Heterostructures for High Mobility P-and N-MOSFETs," Technical Digest of the 2003 IEEE International Electron Devices Meeting ("IEDM"), pp. 18.1.1-4 (2003).
- M.L. Lee, E.A. Fitzgerald, M.T. Bulsara, M.T. Currie & A. Lochtefeld, "Strained Si, SiGe, and Ge Channels for High-Mobility Metal-Oxide-Semiconductor Field-Effect Transistors," Journal of Applied Physics, vol. 97, no. 1 (2005).
- E.A. Fitzgerald, R. Hammond & M. Currie, "Gate Technology for Strained Surface Channel and Strained Buried Channel MOSFET Devices," U.S. Patent No. 6,583,015 (filed Aug. 6, 2001).
- T.A. Langdo, M.T. Currie, R. Hammond, A.J. Lochtefeld & E.A. Fitzgerald, "Strained-Semiconductor-On-Insulator Device Structures," U.S. Patent No. 6,995,430 (filed June 6, 2003).

C. Compensation

18. I am being compensated for services provided in this matter at my standard consulting rate. I am also being reimbursed for expenses that I incur during the course of my work in this matter. My compensation is not contingent upon the results of my study or analysis, the substance of my opinions, or the outcome of any

proceeding involving the Challenged Claims. I have no financial interest in the outcome of this matter or in any litigation involving the '194 Patent.

III. Materials Reviewed

19. In forming my opinions regarding the '194 Patent, I reviewed the materials discussed in this declaration, including the references listed in Appendix A. All citations to materials in Appendix A in this declaration are to the page number of the original reference, not the stamped exhibit page numbers.

IV. Legal Standards

20. I am not an attorney and have not been asked to offer my opinion on the law. However, as an expert offering an opinion on whether the claims in the '194 Patent are patentable, I have been told that I am obliged to follow existing law.

A. Anticipation

21. I have been told the following legal principles apply to analysis of patentability pursuant to 35 U.S.C. §102, a provision in the patent law regarding anticipation. I have been told that, in *inter partes* review proceedings, a patent claim may be deemed unpatentable for anticipation if it is shown by preponderance of the evidence (i.e., it is more likely than not) that the claim was anticipated by a prior-art patent or publication.

22. I have been told that for a claim to be anticipated, every limitation of the claimed invention must be disclosed by a single prior-art reference, viewed from the perspective of a person of ordinary skill in the art.

23. I understand that a claim may sometimes recite a range of values, such as a range of physical dimensions. I have been informed that when the prior art discloses a broader range of values that encompasses a narrower range of claimed values, the broader prior art range discloses the narrower claimed range so long as the narrower claimed range is not “critical” (meaning different in kind, not just degree) as compared to the other values in the broader disclosed range.

B. Obviousness

24. I have been told that under 35 U.S.C. §103(a), “[a] patent may not be obtained though the invention is not identically disclosed or described as set forth in §102, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.” I have been told that, in inter partes review proceedings, a patent claim may be deemed unpatentable if it is shown by preponderance of the evidence (i.e., it is more likely than not) that it would have been obvious.

25. When considering the issues of obviousness, I have been told that I am to do the following:

- a. Determine the scope and content of the prior art;
- b. Ascertain the differences between the prior art and the claims at issue;
- c. Resolve the level of ordinary skill in the pertinent art; and
- d. Consider evidence of secondary indicia of obviousness or non-obviousness (if available).

26. I have been told that the relevant time for considering whether a claim would have been obvious to a person of ordinary skill in the art is the time of alleged invention, which I have been asked to assume is just before December 29, 2006. I do not have any opinions regarding whether December 29, 2006, is the correct date of invention.

27. I have been told that obviousness is a determination of law based on underlying determinations of fact. I have been told that these factual determinations include the scope and content of the prior art, the level of ordinary skill in the art, the differences between the claimed invention and the prior art, and any objective indications of obviousness or non-obviousness that may exist (although I am not aware of any objective indications of non-obviousness relating to the '194 Patent).

28. I have been told that a prior-art reference may be combined with one or more other references and/or the knowledge of a person of ordinary skill in the art to show obviousness. I also have been told that a person of ordinary skill in the art is presumed to know all relevant prior art. I have been told that the obviousness analysis may account for the inferences and creative steps that a person of ordinary skill in the art would have employed at the time of invention.

29. In determining whether the teachings contained in one prior-art reference would have been combined with the teachings contained in another reference or information known to a person of ordinary skill in the art, I have been told that the following principles may be considered, and I have been asked to consider them:

- a. A combination of familiar elements according to known methods is likely to be obvious if it yields predictable results;
- b. The substitution of one known element for another is likely to be obvious if it yields predictable results;
- c. The use of a known technique to improve similar items or methods in the same way is likely to be obvious if it yields predictable results;
- d. The application of a known technique to a prior art reference that is ready for improvement, to yield predictable results;

- e. Any need or problem known in the field and addressed by the reference can provide a reason for combining the elements in the manner claimed;
- f. A person of ordinary skill often will be able to fit the teachings of multiple references together like a puzzle; and
- g. The proper analysis of obviousness requires a determination of whether a person of ordinary skill in the art would have a “reasonable expectation of success”—not “absolute predictability” of success—in achieving the claimed invention by combining prior art references.

30. I have been told that whether a prior art reference renders a patent claim unpatentable as obvious is determined from the perspective of a person of ordinary skill in the art. I have been told that there is no requirement that the prior art contain an express suggestion to combine known elements to achieve the claimed invention, but a suggestion to combine known elements to achieve the claimed invention may come from the prior art, as filtered through the knowledge of one skilled in the art. In addition, I have been told that the inferences and creative steps a person of ordinary skill in the art would have employed are also relevant to the obviousness inquiry.

31. I have been told the reasons a person of ordinary skill in the art would have wanted to modify teachings available in the prior art teachings do not need to

match the inventor's reasons for making the claimed invention. In determining whether the subject matter of a patent claim is obvious, I have been told that what matters is the objective reach of the claim and whether it covers an obvious variation of the prior art. I have been told it would be improper to consider only the specific problem the patentee was trying to solve.

32. I have been told that when a work is available in one field, design alternatives and other market forces can prompt variations of it, either in the same field or in another. I have been told that if a person of ordinary skill in the art could have implemented a predictable variation and would have seen the benefit of doing so, that variation was likely to have been obvious. I have been told that in many fields, there may be little discussion of obvious combinations, and, in these fields, market demand, not scientific literature, may drive design trends. I have been told that when there was a design need or market pressure and there were a finite number of predictable solutions, a person of ordinary skill in the art would have had good reason to pursue those known options.

33. I have been told that there is no rigid rule that a reference or combination of references must contain a "teaching, suggestion, or motivation" to combine them. But I also understand that any "teaching, suggestion, or motivation" present in the prior art may be useful in establishing a rationale for combining aspects of the prior art. I have been told this "teaching, suggestion, or motivation"

test poses the question as to whether the prior art contains an express or implied teaching, suggestion, or motivation to combine prior art elements in a way that realizes the claimed invention, and that it seeks to counter impermissible hindsight analysis.

34. I have been told that a claimed invention may be obvious even when the prior art does not teach each claim limitation, so long as the record contains some reason why a person of ordinary skill in the art would have applied the prior art to obtain the claimed invention.

35. I have been told that when there is a known technique to address a known problem using prior art elements according to their established functions, then a person of ordinary skill in the art would have had a motivation to combine.

36. I have been informed that, in an obviousness analysis, prior art must be analogous prior art to the patent being considered. I have been informed that a prior art reference is considered to be analogous, or in the same field of art, if the reference is either (1) in the same field of endeavor as the challenged patent, regardless of the problems the challenged patent and the prior art address; or (2) reasonably pertinent to the particular problem being solved by the challenged patent.

V. Level of Ordinary Skill in the Art

37. I have been informed that a person of ordinary skill in the art (“person of ordinary skill in the art”) is determined by considering several factors, including

the (i) type of problems encountered in the art; (ii) prior art solutions to those problems; (iii) rapidity with which innovations are made; (iv) sophistication of the technology; and (v) educational level of active workers in the field.

38. I have been instructed to assume a person of ordinary skill in the art is not a specific real individual, but rather a hypothetical individual having the qualities reflected by the factors discussed above.

39. In my opinion, a person having ordinary skill in the art in reference to the '194 Patent would have had a master's degree in electrical engineering, physics, chemistry, materials science, or a related field and three years of work experience in semiconductor manufacturing, such as, for example, in integrated circuit device (or transistor) design and/or manufacturing. Additional relevant education could substitute for professional experience, and significant work experience or training could substitute for formal education.

40. I have not analyzed the priority date of the '194 Patent, but I note that the earliest claim of priority listed on the face of the '194 Patent is the filing date of its parent application, August 9, 2007. I also have been informed that during prosecution the applicant alleged an earlier invention date of December 29, 2006. Because all the prior art discussed in this Declaration predates December 29, 2006, I have been asked for simplicity to treat **December 29, 2006**, as the priority date for the '194 Patent. I have also treated this date as the date from which to assess the

knowledge available to a person of ordinary skill in the art. I do not have any opinions regarding whether December 29, 2006, is the correct priority date.

VI. Technological Background

41. The '194 Patent describes methods of fabricating Metal Oxide Semiconductor ("MOS") transistors with epitaxial source/drain regions to provide mechanical stress and boost transistor performance. ('194 Patent at Title, Abstract, 1:16-19.) As I further discuss below, in my opinion, the elements described and claimed in the '194 Patent were well known before December 29, 2006.

42. The '194 Patent generally relates to a technology that is known in the field as "strained silicon channel MOS transistor[s]"—i.e., MOS transistors using SiGe source/drain stressors. ('194 Patent, 1:16-19.) That technology was known and had been developed at least since the early 2000s. For example, as I explain below in more detail, MOS transistors using strained silicon SiGe source/drain stressors was widespread by the mid-2000s. In fact, two generations of high-volume commercial devices (e.g., 90 nm devices, released in 2003, and 65 nm devices, released in 2005) used strained-silicon channel MOS transistors before the alleged invention date.

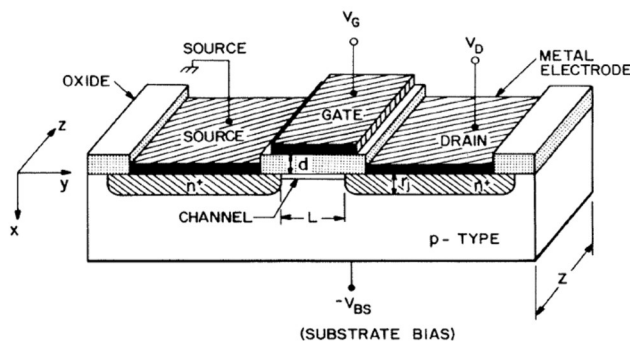
43. During the timeframe relevant to the '194 Patent, the person of ordinary skill in the art would have been familiar with the background information I describe below in subsections A through C.

A. MOS Transistors

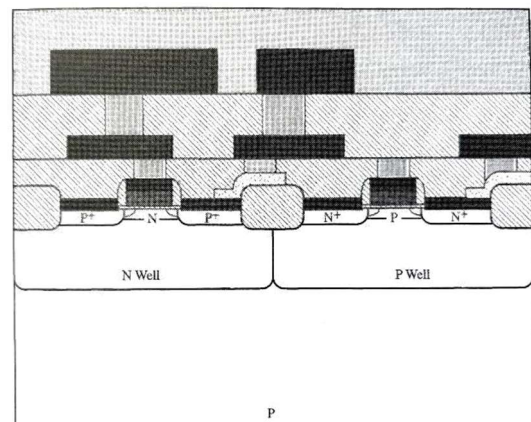
44. By December 29, 2006, MOS transistors had been known for decades. Introduced in the 1960s, MOS transistors had been a cornerstone of modern electronics for many decades. (Size at 431.)

45. MOS transistors, and specifically MOS field-effect transistors (“MOSFETs”) like the ones at issue here, include four main regions: *source* and *drain* regions allow for current input and output, and a *gate* overlies a *channel* region located between the source/drain regions. (Size at 433-34, Fig. 3.)

46. The gate comprises a gate electrode (which is normally made of a metal or doped polysilicon) and a thin gate dielectric layer (which is an electrically insulating film) that separates the gate from the semiconductor channel underneath it, as the figures below illustrate. (Size at 433-34, Fig. 3.) These figures show typical MOSFET arrangements as described in textbooks. (Size at 433-34, Fig. 3; Plummer at 71-90, Figs. 1-11, 2-2, 2-22 to 2-44.)



Size, Fig. 3



Plummer, Fig. 1-11

47. The *source* and *drain* regions are generally *doped* with impurities that modify the conductivity or resistivity of the region. (Plummer at 60-63.) More specifically, source/drain regions are usually doped with *p-type* or *n-type* impurities, and channel regions are doped with impurities of the opposite type. (Sze at 433-34; Plummer at 76-82.)

48. Generally, the terms **PMOS** and **NMOS** refer to MOSFETs with p-type or n-type source/drain regions, respectively. (Plummer at 12-13, 50-51, Figs. 1-11, 2-2.) Most typical devices are **CMOS** (“Complementary MOS”), which include both PMOS and NMOS. (Plummer at Fig. 1-11.)

49. Applying voltage to the gate electrode controls the channel underneath to connect or disconnect the source and drain. (Sze at 433-34, 438, Figs. 3, 6.) In an enhancement-mode transistor (which is normally “off”), applying a voltage to the gate can induce a conducting channel between the source and drain (what is known as turning “on” the transistor). On the other hand, applying no voltage to the gate destroys the conducting channel (what is known as turning “off” the transistor). In a depletion-mode transistor (which is normally “on”), the situation is reversed.

B. Strained Channel Technology

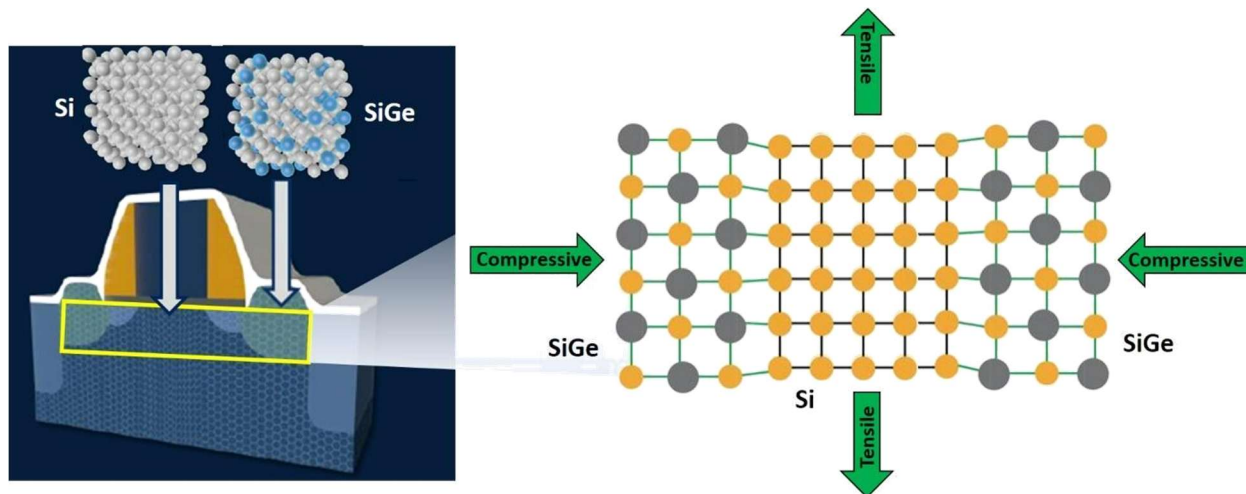
50. Strained-silicon channel MOSFETs with SiGe source/drain stressors predate the '194 Patent, finding use in even high-volume commercial devices. (See Thompson at 1790-71; Bai at 657-58.) Manufacturers found that using stressor

films or epitaxy layers in the source/drains in MOSFETs could increase the channel mobility of charge carriers (electrons in NMOS and holes in PMOS). (James at 2.) Stressing the channel modifies the band structure of the silicon and reduces phonon scattering, which allows the charge carriers to move more easily through the channel, enhancing the transistor's switching speed and drive current. (James at 2; Thompson at 1790-96; Murthy ¶¶[0005].) Manufacturers understood that using compressive source/drain stressors improved carrier mobility in PMOS (hole mobility), whereas tensile stress improved carrier mobility in NMOS (electron mobility). (James at 2; Thompson at 1790-96; Murthy ¶¶[0005].)

51. The first high-volume strained-channel MOSFETs included epitaxial SiGe layers in the source/drain regions. By 2005, using SiGe source/drain stressors to compress high-volume manufactured PMOS devices was common, and reverse-engineering reports on such commercial devices had showed that SiGe had increased PMOS "hole mobility by as much as 50%." (James at 2.)

52. SiGe stressor layers strain the channel because germanium atoms are *larger* than silicon atoms, leading to a germanium lattice constant (i.e., inter-atomic spacing in the crystal) that is roughly 4% larger than in silicon. Thus, adding SiGe source/drain regions near the silicon channel *compressively* strains the silicon channel region along the current flow direction (left-to-right in the graphic below). (James at 2; Thompson at 1790-96; Murthy ¶¶[0046]-[0047]; Bohr ¶[0024], FIG. 4.)

The graphic below exemplifies how SiGe source/drain stressors compress a silicon channel.¹ The Ge atoms (shown in gray in the graphic on the right) are larger than the silicon atoms (shown in yellow in the graphic on the right). This increases the inter-atomic spacing of the lattice, which compresses the silicon channel.



53. Ensuring adequate strain transfer commonly involved growing epitaxial source/drain regions that extended above the substrate (protruding over the silicon surface) to provide sufficient SiGe to effectively compress the silicon channel. (See Ghani at 978, Figs. 1-4; Wang906 ¶¶[0030]-[0032], FIG. 9; Bohr at FIGS. 4-7; Kavalieros at Abstract, ¶¶[0025], ¶¶[0043], FIGS. 5, 13.) These “raised” SiGe regions also improve PMOS performance by reducing contact resistance in the source and drain regions. (See James at 2.)

¹ Adapted from <https://www.intechopen.com/chapters/62046> and <https://www.semiconductor-digest.com/a-dispatch-from-semicon-west-applied-materials-launches-epi-system-focused-on-nmos-strain/>.

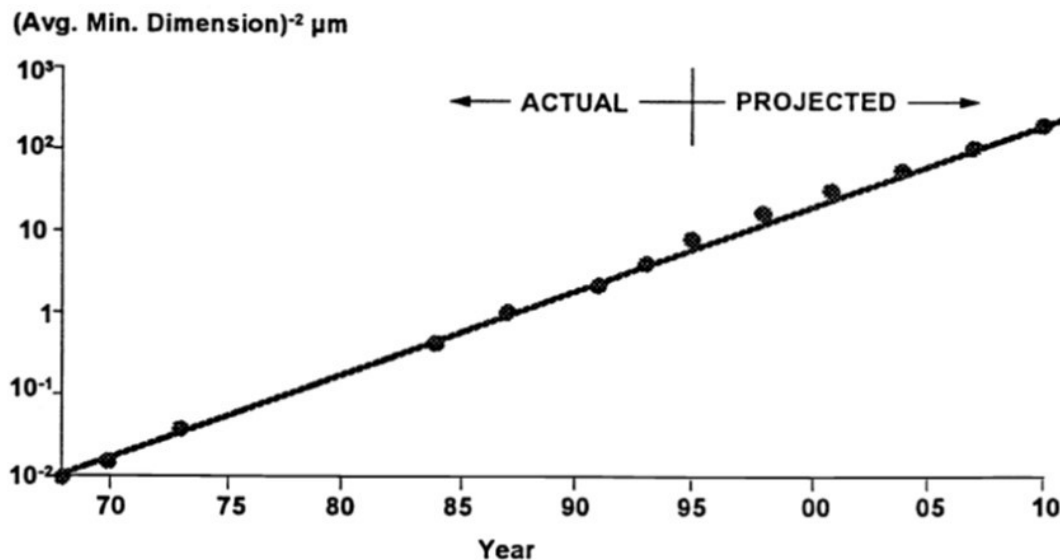
54. Compressive strain does not benefit NMOS devices because the charge carriers in NMOS devices are electrons, not holes as in PMOS devices. Electron carrier mobility benefits from *tensile* strain, not compressive strain. In the first high-volume, strain-enhanced commercial NMOS devices, manufacturers used tensile-strained silicon nitride layers to impart tensile strain to the NMOS channel, thereby enhancing electron mobility. (James at 4.) A further evolution of strained-channel NMOS devices, to induce more tensile strain, involved using epitaxial source/drain stressors (similar to PMOS devices). To achieve tensile stress, the material in the source/drain requires a smaller atom than silicon (unlike the larger atom Ge used for compression). For example, by growing silicon carbide (SiC) in the source/drain regions, carbon—being a *smaller* than silicon—tends to create a smaller lattice spacing than silicon, inducing a tensile strain to the silicon channel region of an NMOS device. (Murthy ¶¶[0005], ¶¶[0048], ¶¶[0072]; Bohr ¶¶[0045].)

55. By the alleged priority date of the '194 Patent (December 29, 2006), epitaxial SiGe source/drain stressors already had been used in two generations of high-volume commercial MOSFET devices. (Thompson at 1790-91 (Intel 90 nm devices); Bai at 657-58 (Intel 65 nm devices).)

C. Gate Sidewall Spacers

56. Since the invention of MOS transistors, there has always been a drive to shrink individual transistors and increase their density. This trend is known as

device “scaling.” (Chang at xviii-xxi; Wolf2 at 1 at Fig. 1-1(b).) Device scaling was such a well-established trend that it followed a predictable cadence, known as “Moore’s Law.” (See Moore at 1-16; Wolf2 at 1.) Although not technically a “law,” Gordon Moore’s prediction that the number of transistors in a single integrated circuit would double every two years held true for many decades. The figure below shows one aspect of Moore’s law—the rate at which the average minimum device dimension shrank. (Moore at Fig. 14.)



Moore at Fig. 14

57. When shrinking a MOSFET, the channel must become shorter, which brings the source and drain regions closer to one other. (Wolf3 at 205, 233-34; Wolf2 at 338.) This also brings the source/drain regions closer to the channel/gate regions. As this occurs, the electric field from the drain may eventually “penetrate into the source region” and cause unwanted increases in current. (Wolf2 at 341.) This

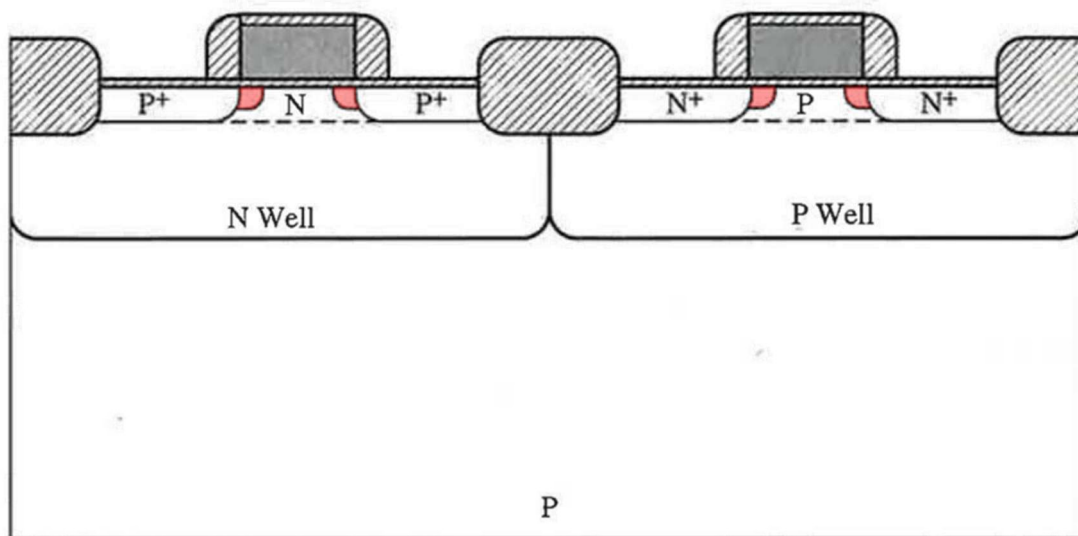
phenomenon is called *punchthrough*, which is an example of what are known as short-channel effects (“SCEs”). (Wolf³ at 233; Sze at 433; Quirk at 211; Plummer at 77-78.)

58. Researchers and engineers discovered punchthrough and other SCEs as early as the 1970s, and they developed a variety of techniques to mitigate those effects. (Plummer at 77-78.) By the 1990s, one very common technique to mitigate SCEs in high-volume commercial semiconductor fabrication was to use lightly doped drain (“LDD”) regions.² (Plummer at 76-82; Quirk at 211-13.) Because source and drain regions generate an electric field that can affect the channel of the transistors, it was found that introducing LDD regions alleviated punchthrough by positioning more heavily doped source/drain regions (and their larger electric fields) further away from the channel, thereby controlling electric fields near the channel and improving the transistor’s performance. (Plummer at 77-78; Quirk at 211-13.)

59. As early as 1980s, researchers found they could better control electric fields near the channel, improve transistor performance, and minimize SCEs by controlling the source/drain doping. The LDD approach, illustrated below, uses a sequence of doping implantations that “carefully tailor the doping profile near the

² Although the last “D” in “LDD” stands for “drain,” a person of ordinary skill in the art would have known that LDD regions were almost always formed in both source and drain regions. Accordingly, LDD regions may be more accurately be understood as lightly doped source and drain regions.

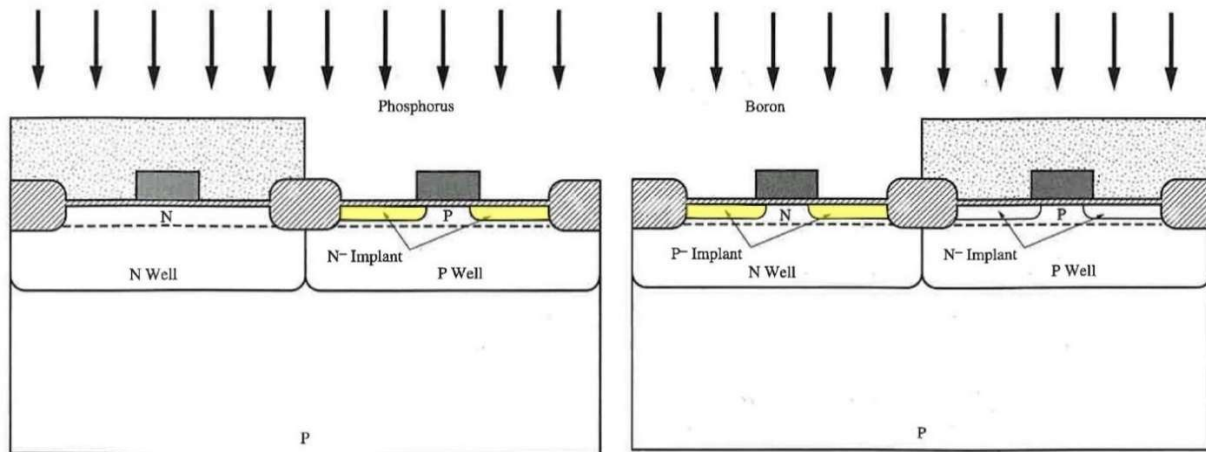
drain junction (and the source junction) in order to minimize short channel effects.” (Plummer at 78.) For example, as Plummer shows in Fig. 2-33 (reproduced below), LDD regions (annotated in red) are introduced close to the channel to facilitate control of electric fields there. (Plummer at 76-78.)



Plummer at Fig. 2-33^[3]

60. Plummer’s Figs. 2-27 through 2-32 illustrate a typical method of forming and the LDD regions by using “sidewall spacers.” (See Plummer at 76-82.) Impurities like boron or phosphorus are used to create lightly doped implant regions on the sides of the gate (the rectangle between the yellow regions). (See Plummer at 76-77.) As shown below, ion implantation forms lightly doped source/drain regions (yellow) using the gate as a mask to block the ions from the channel region.

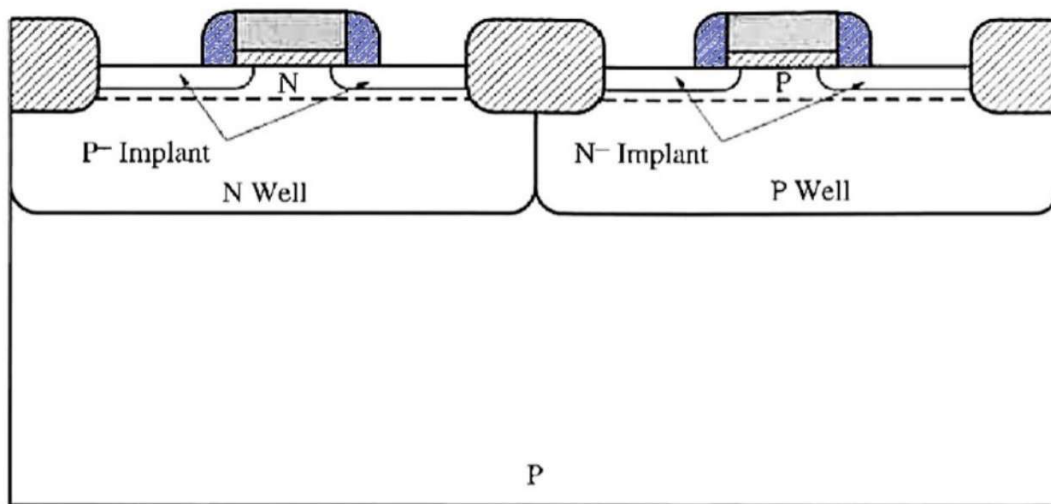
³ All color annotations from here through the end of this declaration have been added unless I note otherwise.



Plummer at Fig. 2-27

Plummer at Fig. 2-28

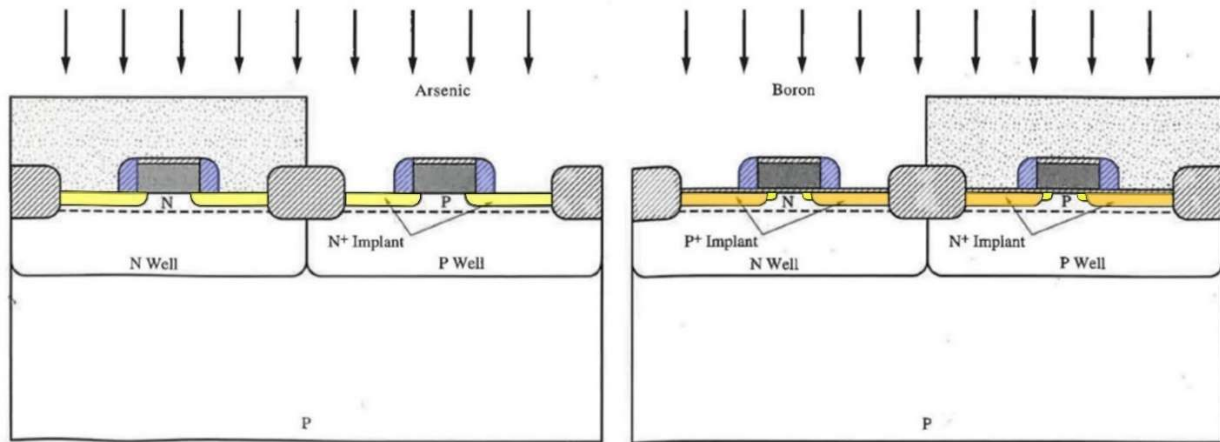
61. Then the “sidewall spacers” (purple) are formed on gate edges. (See Plummer at 78-80.)



Plummer at Fig. 2-30

62. As shown below, such sidewall spacers act as masks near the edge of the channel during subsequent ion implantation to more heavily dope part of the substrate. The sidewall spacers protect the LDD regions (yellow) and help position the more heavily doped regions (orange) further away from the channel edge.

(Plummer at 80-82 at Figs. 2-31 to 2-33; Quirk at 213 at Fig. 9.17; Wolf3 at 595-96 at Fig. 9-31(f).) This reduces the electric field near the channel to mitigate SCEs.



Plummer at Fig. 2-31

Plummer at Fig. 2-32

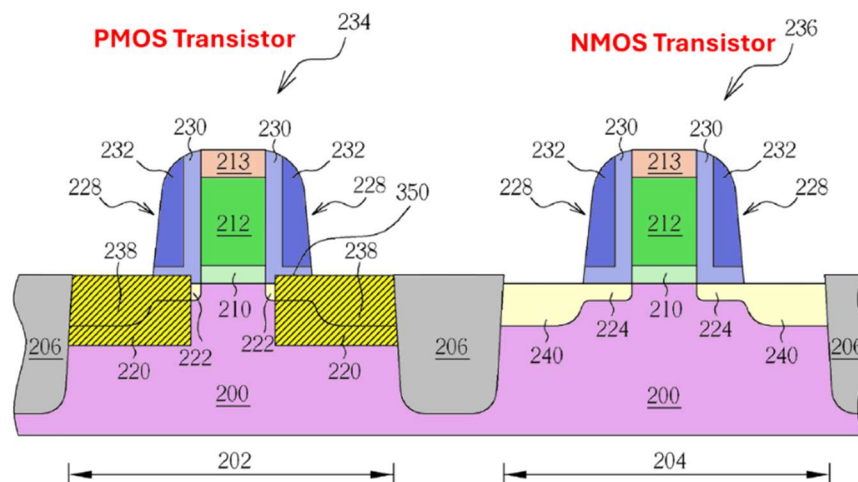
63. This way of forming LDD regions, gate sidewall spacers, and source/drain regions was very well-known by the priority date of the '194 Patent. For example, Plummer published his book in 2000. Even back then, this process was a routine part of undergraduate courses on semiconductor design and manufacturing. By the time of the '194 Patent, the use of gate sidewall spacers to form LDD regions in this way had been fundamental in semiconductor manufacturing for more than a decade. Sidewall spacers, including those extending onto epitaxial source/drain regions, were common and a routine device element, as illustrated by the references I analyze in this declaration below.

VII. THE '194 PATENT

64. To perform my analysis, I reviewed the '194 Patent and its prosecution history. Below, I provide a brief overview of both.

A. Overview

65. The '194 patent describes a “method of fabricating a MOS transistor structure.” ('194 Patent at 1:64-2:49.) The embodiment in FIG. 5 below shows the different elements of the MOS transistor structure described in the patent. The table beneath FIG. 5 summarizes the elements depicted in FIG. 5. (See '194 Patent at 2:65-4:53.)



'194 Patent, FIG. 5 (annotated)

PMOS

220: Epitaxial layer
222: First ion lightly doped region
234: First conductive transistor
238: First ion source/drain regions

NMOS

224: Second ion lightly doped region
236: Second conductive transistor
240: Second ion source/drain regions

NMOS & PMOS

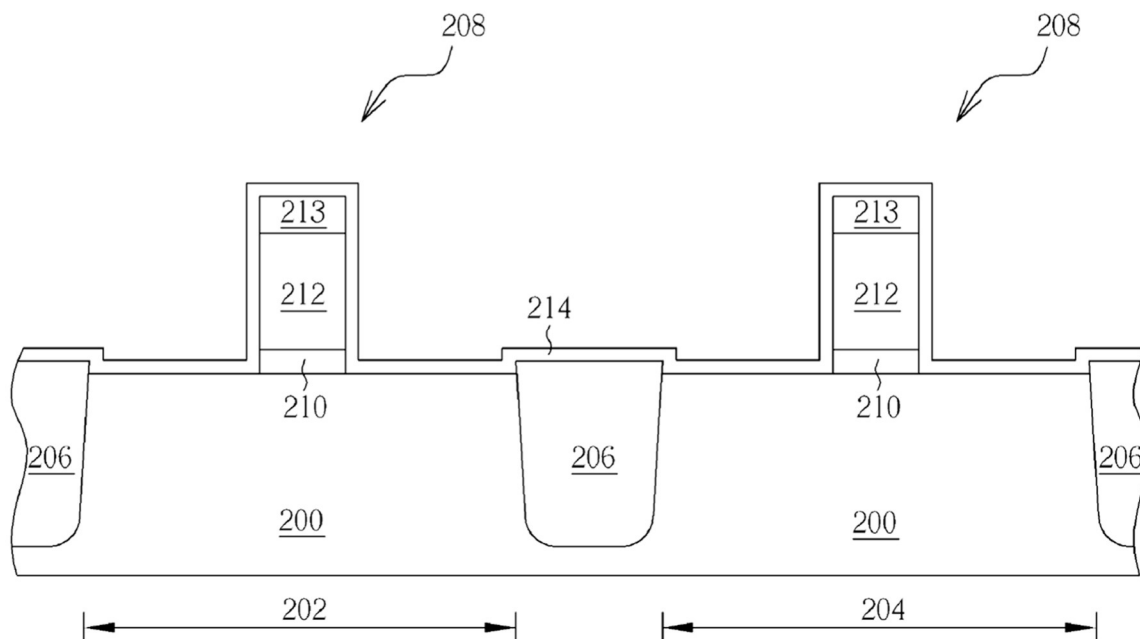
200: Semiconductor substrate	213: Cap layer
206: Shallow trench isolation (STI)	228: Spacers
210: Dielectric layer	230: Oxide liner
212: Conductive layer	232: Nitride spacer

66. As FIG. 5 shows above, this exemplary MOS structure described in the '194 Patent includes “a first conductive transistor 234” (e.g., PMOS) formed “in the first conductive transistor area 202” and “a second conductive transistor 236” (e.g., NMOS) formed “in the second conductive transistor area 204.” (’194 Patent at 4:25-34.) Each transistor also comprises a gate that includes a dielectric layer 210, a conductive layer 212, and a cap layer 213. (’194 Patent at 3:19-22.) And each gate is flanked by a pair of sidewall spacers 228 comprising “an oxide liner 230 and a nitride spacer 232.” (’194 Patent at 4:6-10.)

67. As FIG. 5 shows, the PMOS device additionally includes two epitaxial layers 220 formed “next to the relative sides of the gates.” (’194 Patent at 2:38-40, 3:49-54.) Those epitaxial layers “may be grown higher than the surface of the semiconductor substrate 200, so as to form a raised epitaxial layer 220.” (’194 Patent at 3:51-54.)

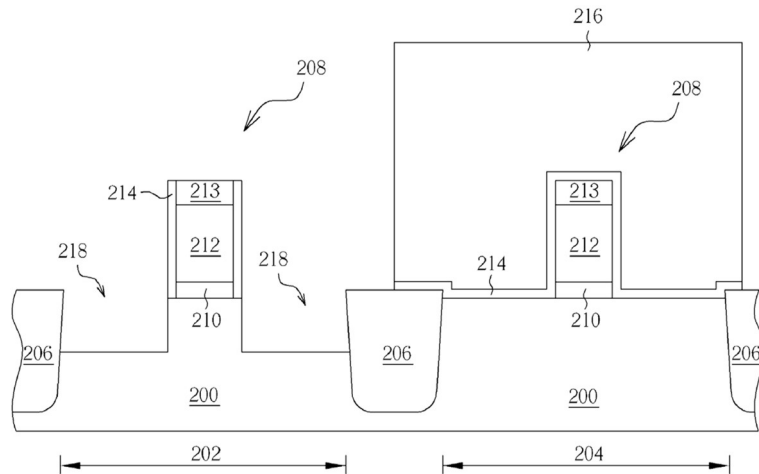
68. The '194 patent depicts the steps of manufacture in FIGS. 1-5. (’194 Patent at 2:65-4:53). Beginning with FIG. 1, it shows “a semiconductor substrate 200” with “a plurality of first conductive transistor areas 202 and a plurality of second conductive transistor areas 204” isolated by “shallow trench isolations (STI) 206.” (’194 Patent at 3:4-13.) FIG. 1 also depicts “a plurality of gates 208” comprising “a dielectric layer 210, a conductive layer 212 positioned on the dielectric layer 210 and a cap layer 213 positioned on the conductive layer 212.”

(’194 Patent at 3:16-22.) After the formation of the gate, “a protective layer 214” is formed on the device, covering the substrate and each gate. (’194 Patent at 3:28-30.) This protective layer is usually composed of silicon nitride, and the ’194 Patent states its thickness is “about 150 to 250 Å” but “preferably about 200 Å.” (’194 Patent at 3:30-38.)



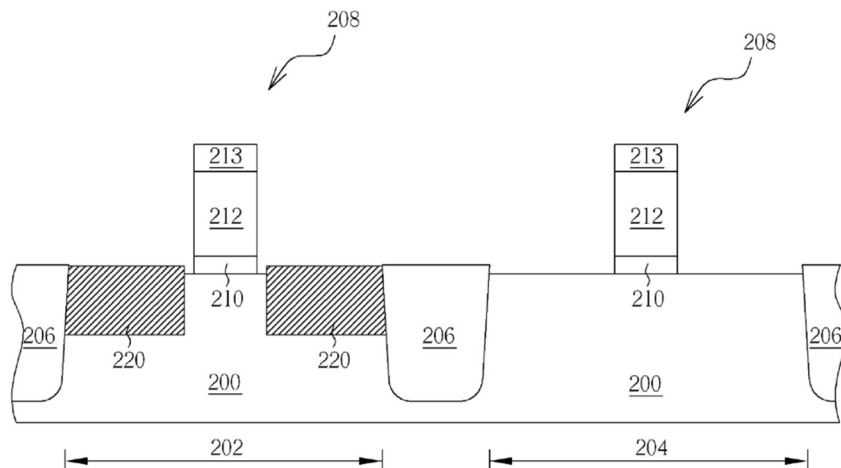
’194 Patent, FIG. 1

69. Next, as shown in FIG. 2, recesses 218 are etched in the first conductive transistor area 202, using a patterned mask 216 (which is subsequently removed). (’194 Patent at 3:39-44.)



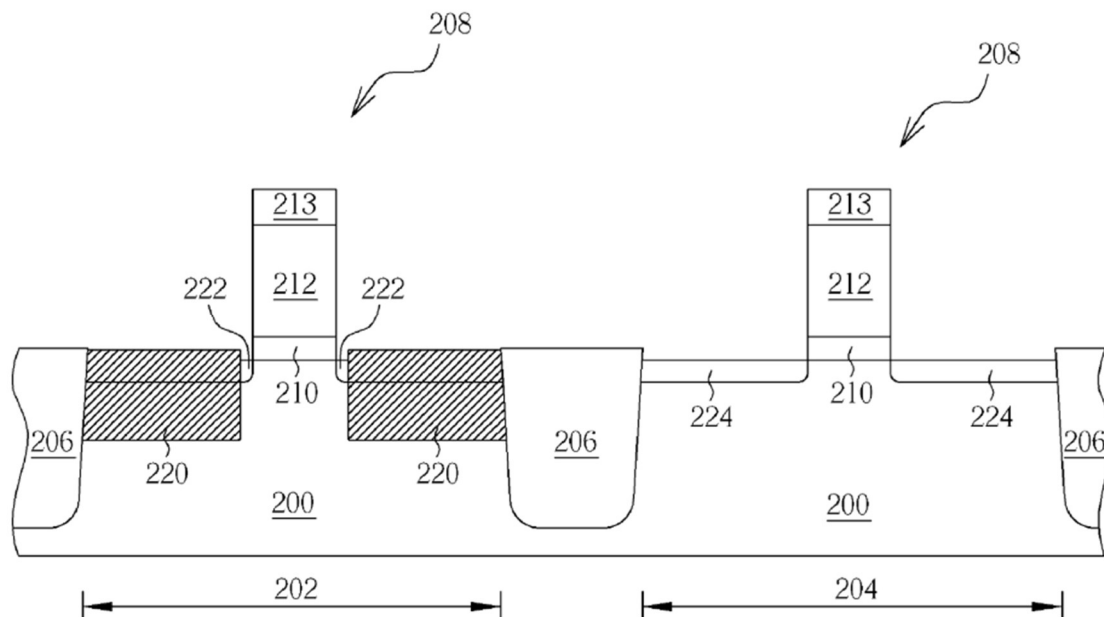
'194 Patent, FIG. 2

70. FIG. 3 depicts the result of an epitaxial growth process, which forms “epitaxial layers 220 in the recesses 218,” and the subsequent removal of protective layer 214. ('194 Patent at 3:45-51.) The epitaxial layer for a PMOS transistor is composed of SiGe, and for an NMOS transistor is composed of SiC. ('194 Patent at 3:55-60.) It may also be grown higher than the surface of the substrate, to form a raised epitaxial layer. ('194 Patent at 3:51-54.)



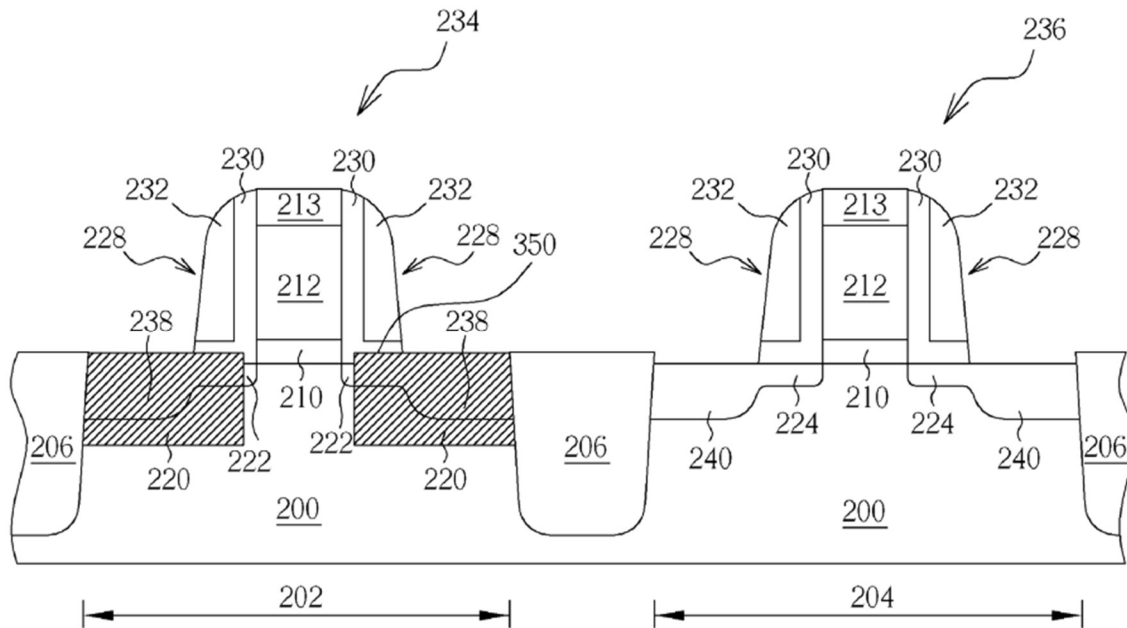
'194 Patent, FIG. 3

71. FIG. 4 depicts the creation of “ion lightly doped region 222” and “ion lightly doped region 224,” also called “lightly doped drain” or “LDD” regions, using two patterned masks (that are not shown) to mask the areas that are not being doped. ('194 Patent at 3:61-4:3.)



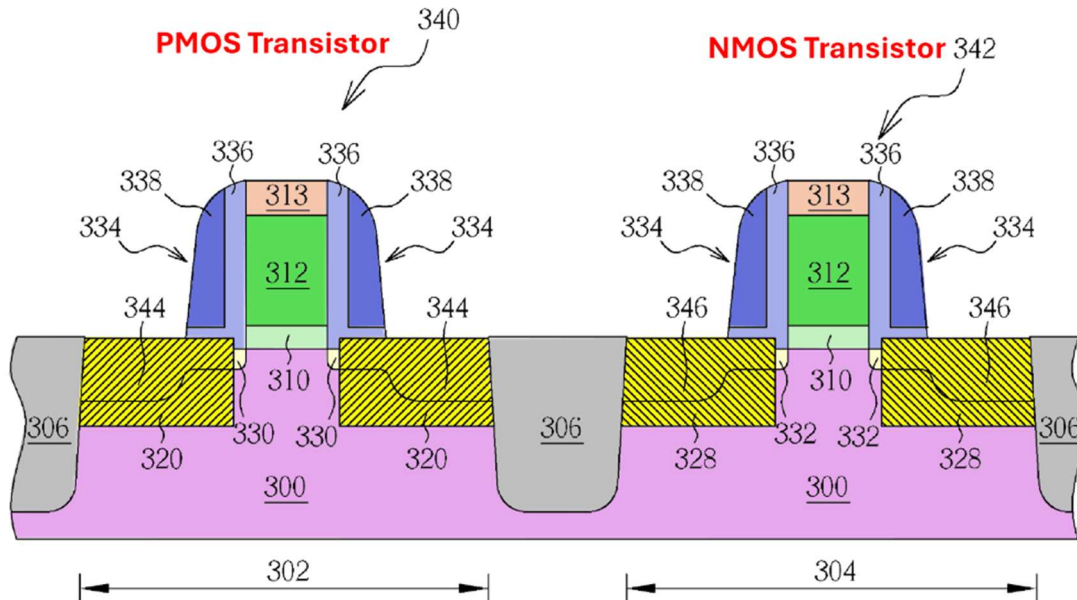
'194 Patent, FIG. 4

72. Finally, FIG. 5 depicts the result of the process. “[S]pacers 228 are formed on the sidewalls of each gate 208,” comprised of “an oxide liner 230 and a nitride spacer 232.” (’194 Patent at 4:4-7.) These spacers “cover the sidewalls of each gate” and “extend laterally onto” the LDD regions and the epitaxial regions 220. (’194 Patent at 4:7-17.) Then “ion source/drain implantation process[es]” form the source/drain regions 238 and 240, using patterned masks (again not shown) to mask the area not being implanted. (’194 Patent at 4:21-34.)



'194 Patent, FIG. 5

73. The methods of the '194 Patent are not limited to this exemplary embodiment, but includes other exemplary "CMOS" devices where both transistor areas include stressor elements. ('194 Patent at 1:64-2:49.) The embodiment in FIG. 14 below shows the different elements of the MOS transistor structure described in this second embodiment. The table beneath FIG. 14 summarizes the elements depicted in FIG. 14. (See '194 Patent at 4:54-7:14.)



'194 Patent, FIG. 14 (annotated)

PMOS

320: First Epitaxial layer
330: First ion lightly doped region
340: First conductive transistor
344: First ion source/drain regions

NMOS

328: Second Epitaxial layer
332: Second ion lightly doped region
342: Second conductive transistor
346: Second ion source/drain regions

NMOS & PMOS

300: Semiconductor substrate
306: Shallow trench isolation (STI)
310: Dielectric layer
312: Conductive layer
313: Cap layer
334: Spacers
336: Oxide liner
338: Nitride spacer

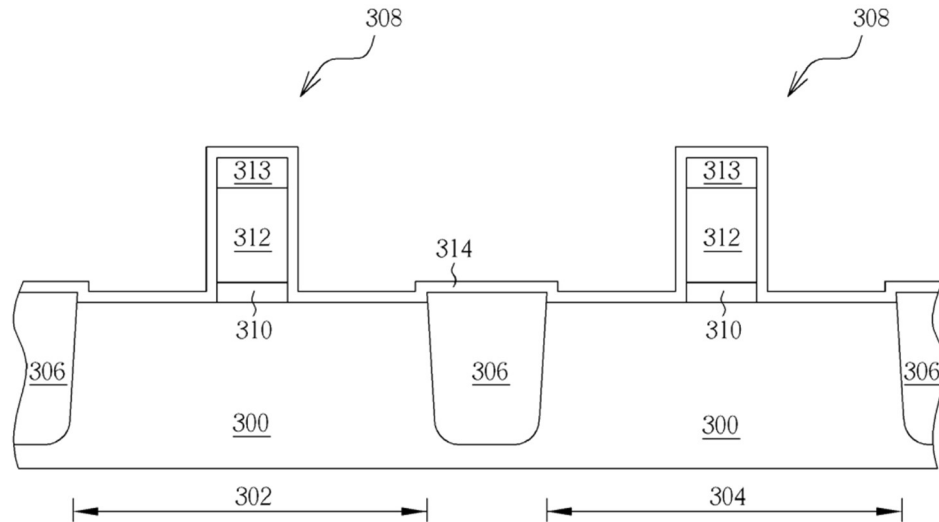
74. As FIG. 14 shows above, this exemplary MOS structure described in the '194 Patent also includes “a first conductive transistor 240” (e.g., PMOS) formed “in the first conductive transistor area 302” and “a second conductive transistor 242” (e.g., NMOS) formed “in the second conductive transistor area 304.” ('194 Patent

at 6:60-7:2) Each transistor, like the FIG. 5 embodiment, also comprises a gate that includes a dielectric layer 310, a conductive layer 312, and a cap layer 313. ('194 Patent at 5:7-10.) And each gate is flanked by a pair of sidewall spacers 334 comprising "an oxide liner 336 and a nitride spacer 338." ('194 Patent at 6:45-51.)

75. As FIG. 14 shows, both the PMOS and the NMOS devices additionally include two epitaxial layers 320 (for the PMOS device) and 328 (for the NMOS device) formed "next to the relative sides of the gates." ('194 Patent at 2:38-40; 5:37-38; 6:17-19.) Those epitaxial layers, like in the embodiment shown in FIG. 5, "may be grown higher than the surface of the semiconductor substrate 300, so as to form a raised epitaxial layer" 320 and 328. ('194 Patent at 5:39-42; 6:19-22.).)

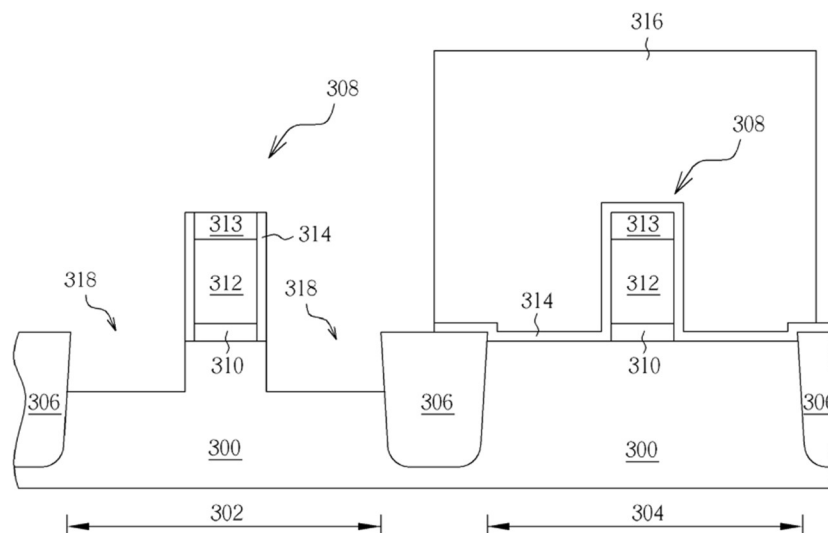
76. The '194 Patent describes a similar process of manufacture for the embodiment shown in FIG. 14. ('194 Patent at 4:54-7:14) Beginning with FIG. 7, it shows "a semiconductor substrate 300" with "a plurality of first conductive transistor areas 302 and a plurality of second conductive transistor areas 304" isolated by "shallow trench isolations (STI) 306." ('194 Patent at 4:63-5:1.) FIG. 7 also depicts "a plurality of gates 308" comprising "a dielectric layer 310, a conductive layer 312 positioned on the dielectric layer 310 and a cap layer 313 positioned on the conductive layer 312." ('194 Patent at 5:4-10.) After the formation of the gate, "a protective layer 314" is formed on the device, covering the substrate and each gate. ('194 Patent at 5:16-18.) This protective layer is usually composed of

silicon nitride, and the '194 Patent states its thickness is “about 150 to 250 Å” but “preferably about 200 Å.” ('194 Patent at 5:17-26.)



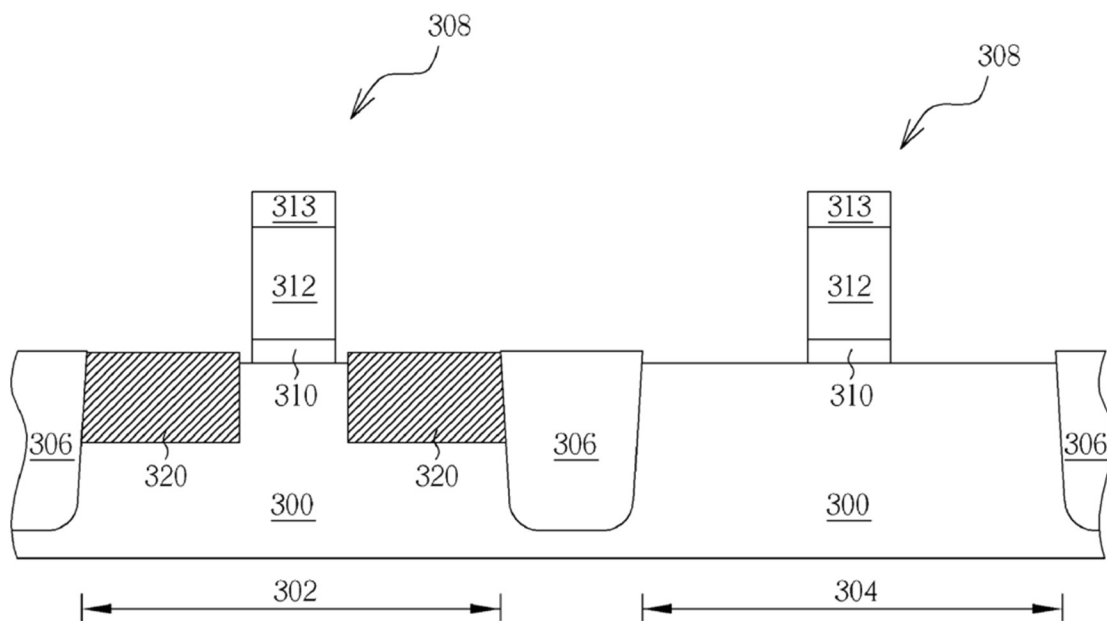
'194 Patent, FIG. 7

77. Next, as shown in FIG. 8, recesses 318 are etched in the first conductive transistor area 302, using a patterned mask 316 (which is subsequently removed). ('194 Patent at 5:27-32.)



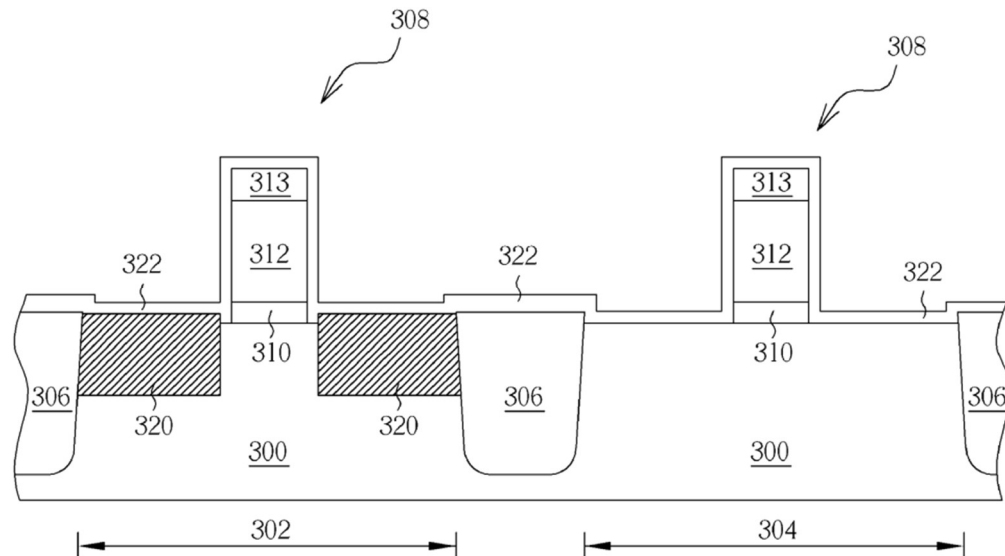
'194 Patent, FIG. 8

78. FIG. 9 depicts the result of an epitaxial growth process, which forms “epitaxial layers 320 in the recesses 318,” and the subsequent removal of protective layer 314. ('194 Patent at 5:33-39.) The epitaxial layer for a PMOS transistor is composed of SiGe. ('194 Patent at 5:44-47.) It may also be grown higher than the surface of the substrate, to form a raised epitaxial layer. ('194 Patent at 5:39-42.)



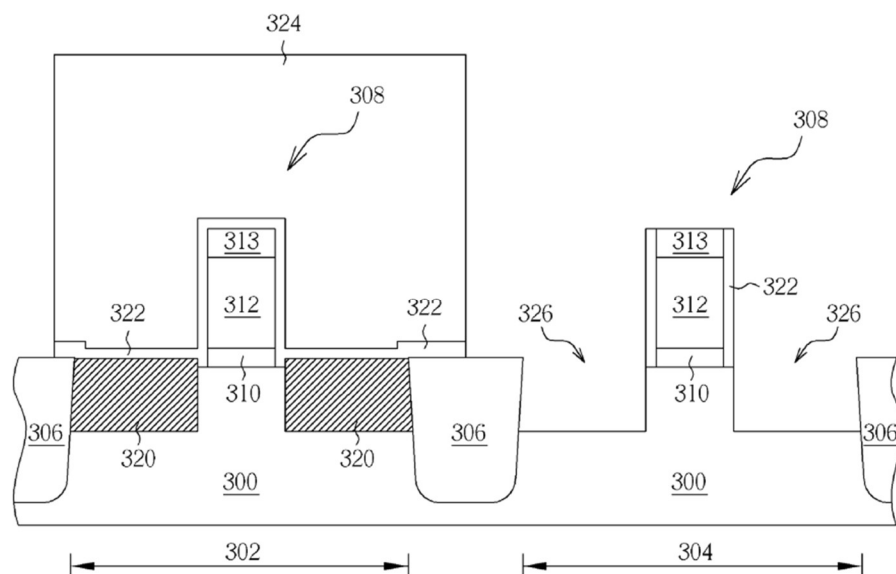
'194 Patent, FIG. 9

79. As FIG. 10 illustrates, the same process is carried out again to form a similar, complementary structure in the second transistor area. “[A] second protective layer 322” is formed on the device, covering the substrate and each gate. ('194 Patent at 5:48-50.) This protective layer is usually composed of silicon nitride, and its thickness is “about 150 to 250 Å” but “preferably about 200 Å.” ('194 Patent at 5:51-59.)



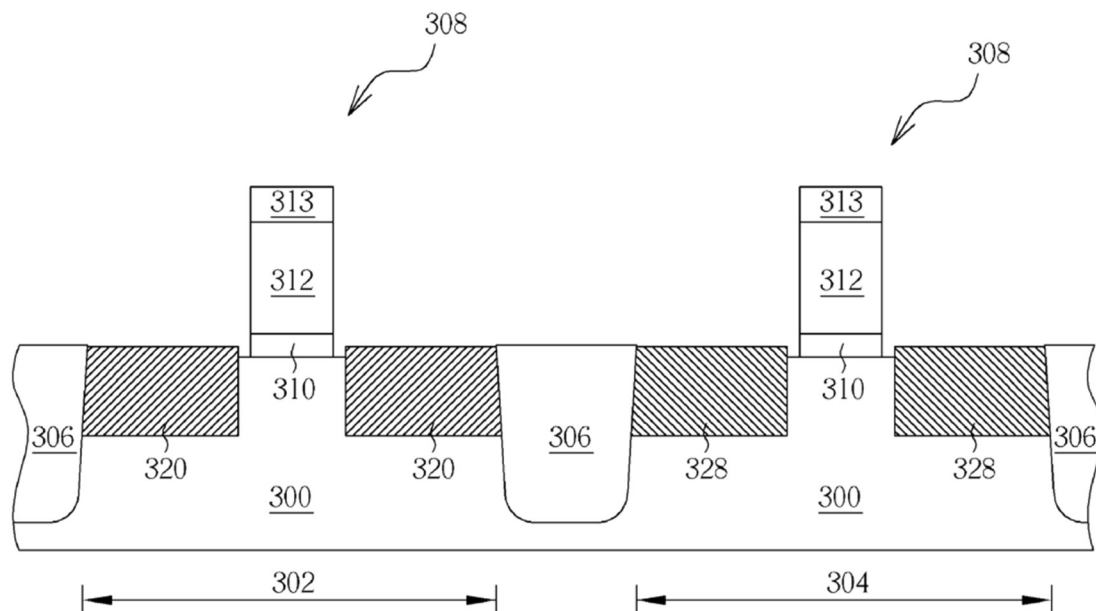
'194 Patent, FIG. 10

80. In FIG. 11, second recesses 326 are etched in the second conductive transistor area 304, using a patterned mask 324 (which is subsequently removed). ('194 Patent at 5:60-65.) These steps could also be done using the first protective layer 314, rather than a second protective layer. ('194 Patent at 5:66-12.)



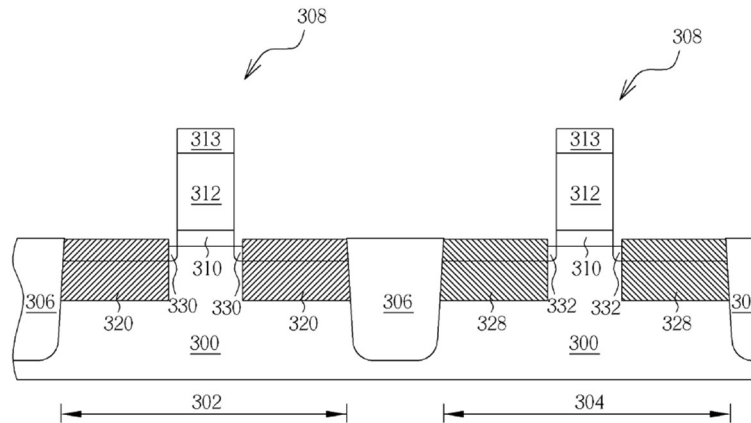
'194 Patent, FIG. 11

81. FIG. 12 depicts the result of a second epitaxial growth process, which forms “second epitaxial layers 328 in the second recesses 326,” and the subsequent removal of protective layer 322. (’194 Patent at 6:13-19.) The epitaxial layer for a NMOS transistor is composed of SiC. (’194 Patent at 6:14-27.) It may also be grown higher than the surface of the substrate, to form a raised epitaxial layer. (’194 Patent at 6:19-22.)



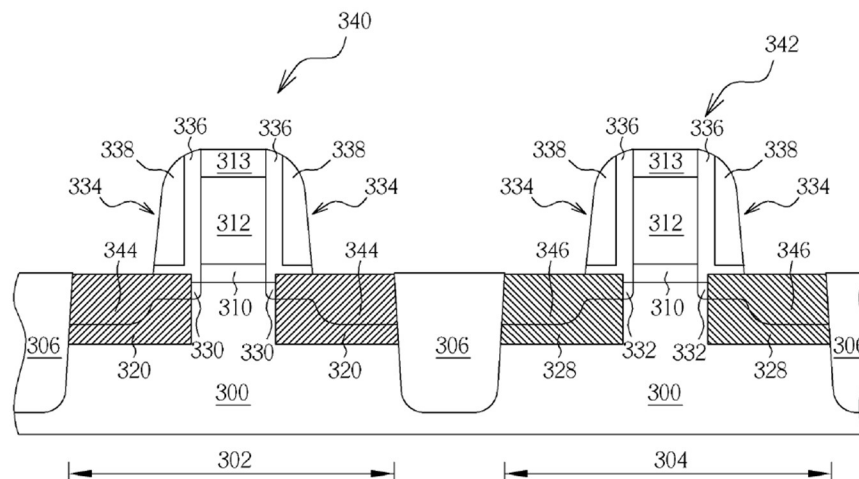
'194 Patent, FIG. 12

82. FIG. 13 depicts the creation of “ion lightly doped region 330” and “ion lightly doped region 332,” also called “lightly doped drain” or “LDD” regions, using two patterned masks (that are not shown) to mask the area that is not being doped. ('194 Patent at 6:35-44.)



'194 Patent, FIG. 13

83. Finally, FIG. 14 depicts the result of the process. “[S]pacers 334 are formed on the sidewalls of each gate 308,” comprised of “an oxide liner 336 and a nitride spacer 338.” (’194 Patent at 6:45-48.) These spacers “cover the sidewalls of each gate” and “extend laterally onto” the LDD regions and the epitaxial regions 320 and 328. (’194 Patent at 6:48-53.) Then “ion source/drain implantation process[es]” form the source/drain regions 344 and 346, using patterned masks (again not shown) to mask the area not being implanted. (’194 Patent at 6:56-7:2.)

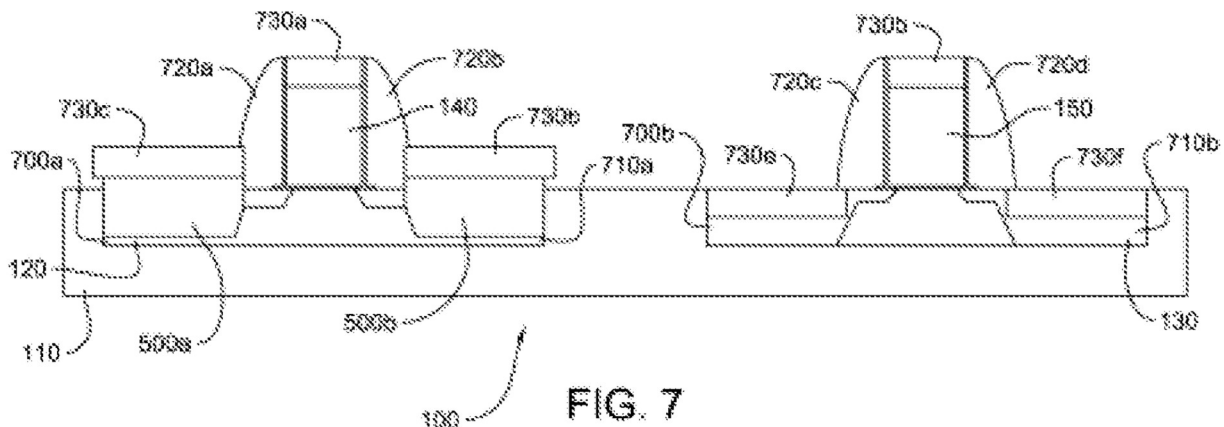


'194 Patent, FIG. 14

84. According to the '194 Patent, "the characteristic of the present invention is to form the epitaxial layer before forming the spacer, thus the distance between the gate and the epitaxial layer is no longer limited by the width of the spacer." ('194 Patent at 7:15-18.)

B. Prosecution History

85. Based on my review of the prosecution file history for the '194 Patent, I understand that the Examiner first rejected the claims as anticipated or rendered obvious by the prior art, depicted in part below. (Prosecution History at 56-66.) In response, the Applicant did not amend the claims, but argued the prior art did not disclose the feature "on a portion of the epitaxial layer such that a contact surface between the epitaxial layer and the spacer is above the surface of the semiconductor substrate," arguing "that even though a very tiny portion of the spacer 720a/720b formed on top of the silicide 730 is revealed in Fig. 7 of Chen, the fact that the silicide 730 being formed after the spacer (as specified in the specification of Chen) and the spacer being formed between the gate and the epitaxial layer both proves that the spacer could not have been formed on top of the silicide." (Prosecution History at 163-173.) Below, I have reproduced Fig. 7 of the prior art reference, Chen et al. (US 7381623).



Prosecution History at 170

86. The Examiner again rejected again the claims based on the prior art, including by combining Chen with a new prior art reference, Zhang et al. (U.S. Publication No. 2008/0203449 A1), which “discloses forming a spacer (40) on the sidewall of the gate (22) and on a portion of the epitaxial layer (36) wherein a contact surface of the epitaxial layer (36) and the spacer (40) is above the surface of the semiconductor substrate (12) (e.g. fig. 6).” (Prosecution History at 175-184.) In response, the Applicant again declined to amend the pending claims (although new claim 22 was added) and submitted an invention disclosure dated December 29, 2006, to allege an invention date before the Zhang reference. (Prosecution History at 195-226.)

87. After this, the Examiner issued a notice of allowability, with no further comment on the reasons for allowance. (Prosecution History at 232.) The Examiner appears to have overlooked the prior art I discuss below (as well as other prior art

cited in this Declaration), all of which predates the invention disclosure. The claimed manufacturing methods were quite common before the '194 Patent.

C. Claim Construction

88. I have been told that claim terms are construed with the meanings they would have to a person of ordinary skill in the art in the context of the patent and prosecution history. Except for claims 6 and 15 of the '194 Patent, that is how I have applied the claim language.

89. For claims 6 and 15, I tried to apply the meaning of the claim as understood by the person of ordinary skill, but I was unable because I find that claims 6 and 15 are confusing as written. Claim 6 recites: "The method of claim 1, wherein the spacer further comprises an offset spacer, positioned between the gate and the spacer." Therefore, claim 6 requires the "offset spacer" to be part of the "spacer." But claim 6 also requires the "offset spacer" to be located between the "spacer" and the gate. Those two requirements seem to conflict.

90. Claim 15 is substantially similar to claim 6: "The method of claim 10, wherein each spacer further comprises an offset spacer, positioned between each gate and each spacer." The claim differs only in that it depends from independent claim 10 rather than independent claim 1, and uses the language "each spacer" and "each gate," rather than "the spacer" and "the gate." It is confusing for the same

reason, as claim 15 also requires the “offset spacer” to conflicting be both part of the “spacer” and located between the “spacer” and the gate.

91. Instead of applying the literal language of claims 6 and 15 as written, I was asked to analyze claims 6 and 15 by analogy to the examples in the '194 Patent. Specifically, I was asked to assume claims 6 and 15 may be satisfied so long as one layer (an “offset spacer”) of the claimed “spacer” lies between another layer of the claimed “spacer” and the claimed “gate.”

92. If the Patent Owner offers constructions of any terms, I reserve the right to address those constructions at an appropriate time in the future.

VIII. REVIEW OF THE PRIOR ART

A. The Hoentschel262 Reference

93. I am not an attorney and am not qualified to assess whether a particular reference qualifies as prior art, but I have been asked to assume that Hoentschel262 qualifies as prior art to the '194 Patent. I note, however, that Hoentschel262 seems to have been filed on November 21, 2006. (Hoentschel262 at cover page.)

94. Hoentschel262 is in the same field of endeavor as the '194 Patent (MOSFETs and their fabrication), and Hoentschel262 is reasonably pertinent to a problem the '194 Patent purports to address (fabricating strained silicon channel MOS transistors). (See Hoentschel262 at Title, Abstract, 1:7-14, 2:66-3:2; '194 Patent at 1:15-19, 1:57-60.) Applying the standard for “analogous art” stated in the

final paragraph of Section IV.B, it is my opinion that a person of ordinary skill in the art would have considered Hoentschel262 to be analogous art to the '194 Patent.

95. Like the '194 patent, Hoentschel262 describes “the formation of different transistor types” including “strained channel regions [] using an embedded strain layer to enhance charge carrier mobility in the channel region.” (Hoentschel262 at 1:7-14.) FIGS. 2a-2i show the manufacturing steps for a pair of MOS transistors, where “a strained semiconductor material of different strain characteristics may be formed adjacent to respective gate electrodes.” (Hoentschel262 at 12:4-12.)

96. FIG. 2a shows the respective gate insulation layers 204, gate electrodes 205, and capping layers 209 for a first transistor 250p and a second transistor 250n. (Hoentschel262 at 12:13-31.)

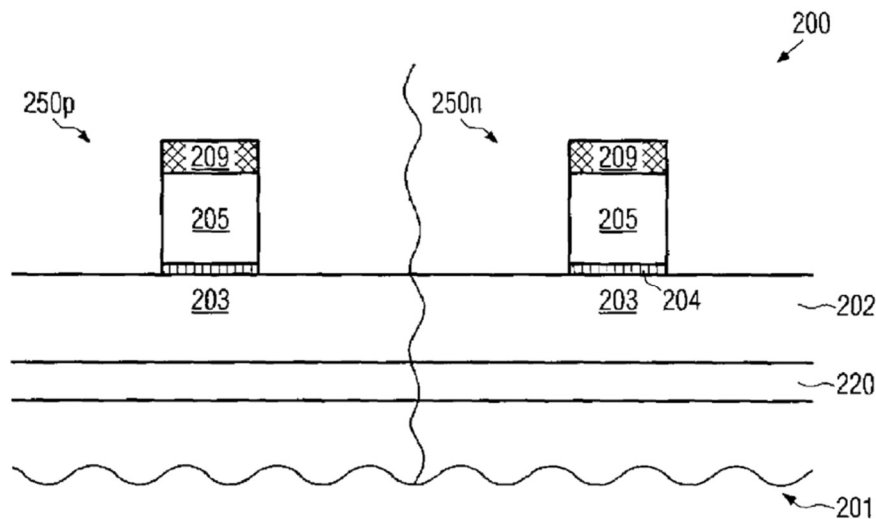


FIG. 2a

Hoentschel262, FIGs. 2a

97. Hoentschel262 then uses “a disposable spacer” to form the recesses and corresponding epitaxial layers of strained semiconductor material, which “enable[es] the positioning of strained semiconductor material close to a channel region.” (Hoentschel262, 3:30-40.) Spacer layers 206A or 226A (with or without liner 207A), are formed on the first and second transistors 250p, 250n, as Figs. 2b and 2e show below. (Hoentschel262, 12:32-49, 13:39-51.)

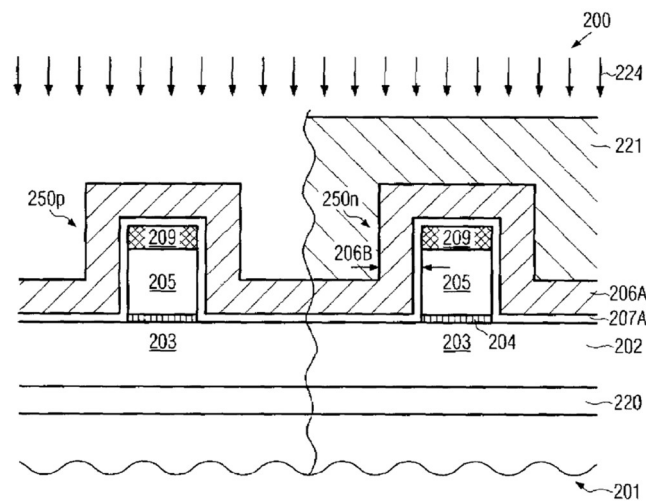


FIG. 2b

Hoentschel262, FIG. 2b

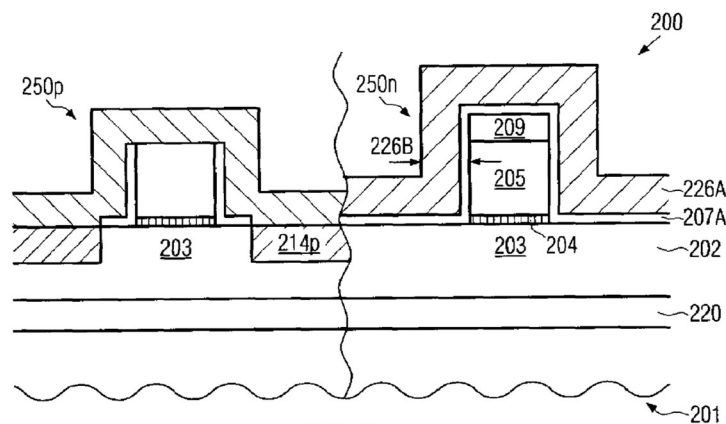
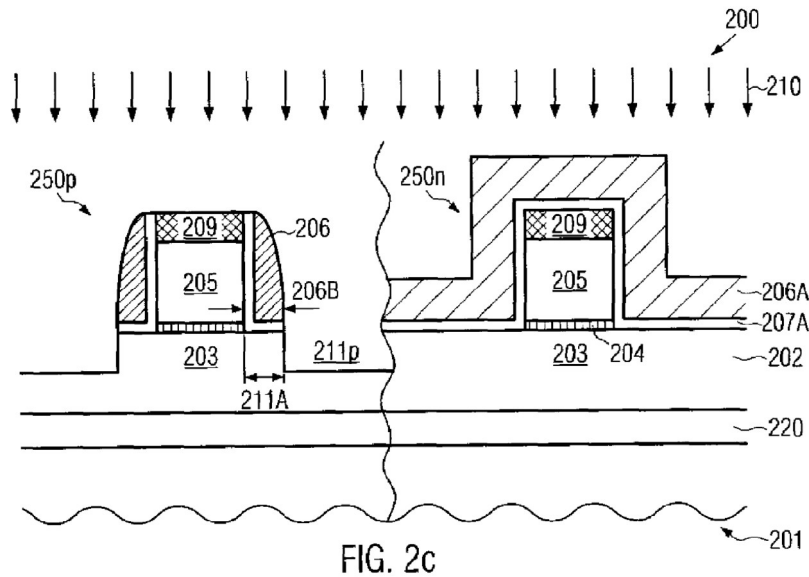


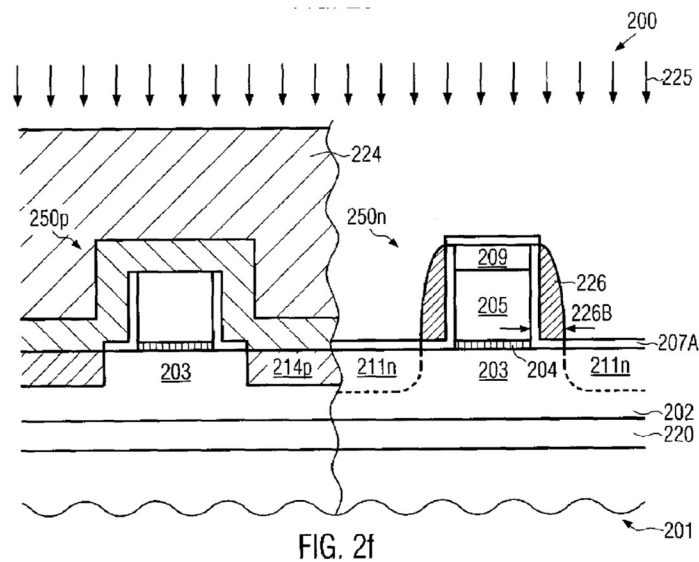
FIG. 2e

Hoentschel262, FIG. 2e

98. These spacer layers are etched to form disposable spacers 206 and 226 with thicknesses 206B and 226B, respectively. Those thicknesses define the locations for recesses 211p and 211n, respectively, in the substrate, as FIGS. 2c and 2f show below. (Hoentschel262 at 12:49-13:20, 13:52-14:17.)



Hoentschel262, FIG. 2c



Hoentschel262, FIG. 2f

99. An epitaxial growth process forms the strained semiconductor materials 214p or 214n in the respective recesses 211p and 211n, with “any desired degree of underfilling or overfilling.” (Hoentschel262 at 13:21-30, 14:18-33.) This strained semiconductor material may be “a silicon/germanium material with a high intrinsic compressive strain” for a PMOS device, or a “silicon/carbon mixture for imposing a tensile strain the channel region” for an NMOS device. (Hoentschel262 at 13:24-30, 14:25-33.)

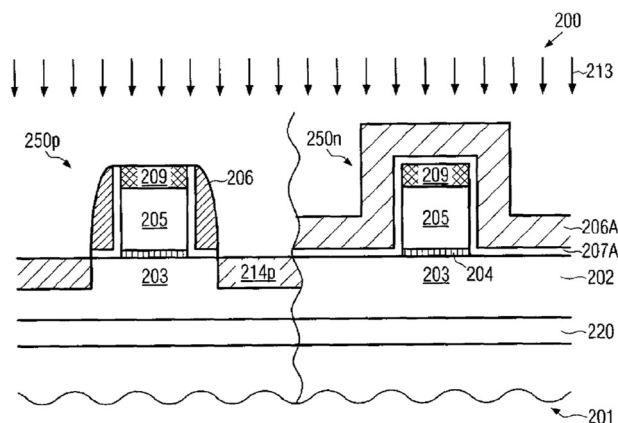


FIG. 2d

Hoentschel262, FIG. 2d

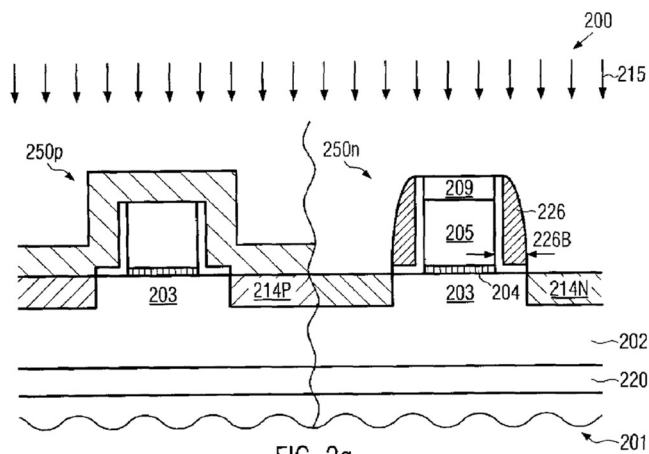
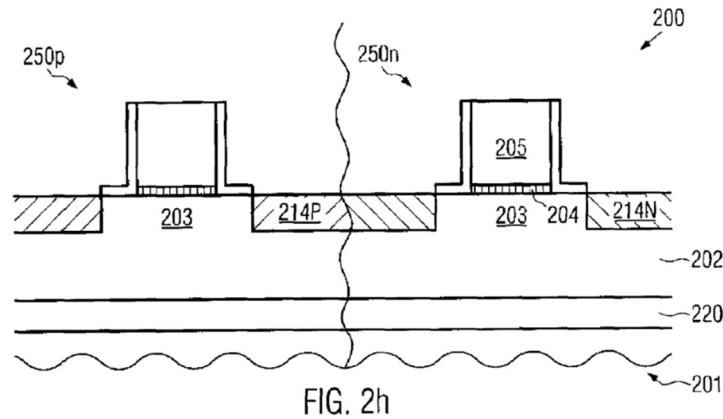


FIG. 2g

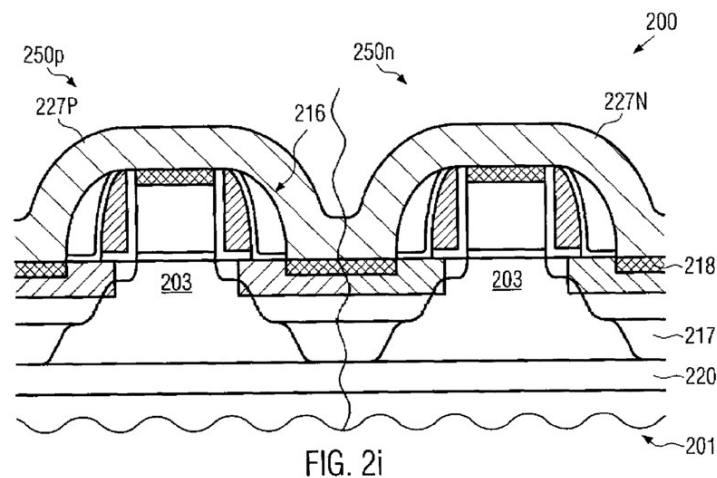
Hoentschel262, FIG. 2g

100. The disposable spacers are removed after the etching and epitaxy steps are complete. (Hoentschel262 at 13:30-38, 13:60-14:1, 14:34-43.)



Hoentschel262, FIG. 2h

101. The source and drain regions are formed through “appropriate spacer techniques and implantation processes” using “any appropriate number of individual spacer elements, depending on the complexity of the required dopant profile of the regions 217,” resulting in a P-channel transistor 250p and an N-channel transistor 250n. (Hoentschel262 at 14:44-15:7.)

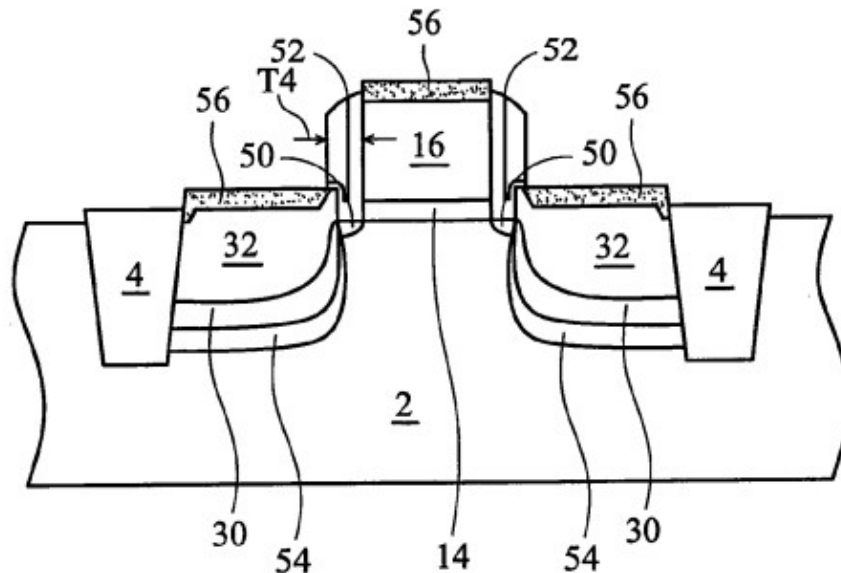


Hoentschel262, FIG. 2i

B. The Wang407 Reference

102. I am not an attorney and am not qualified to assess whether a particular reference qualifies as prior art, but I have been asked to assume that Wang407 qualifies as prior art to the '194 Patent. I note, however, that Wang407 seems to have been filed on September 6, 2006. (Wang407 at cover page.)

103. Wang407 is in the same field of endeavor as the '194 Patent (MOSFETs and MOSFET fabrication), and Wang407 is reasonably pertinent to a problem the '194 Patent purports to address (fabricating strained silicon channel MOS transistors). (See Wang407 at Title, 1:65-2:2; '194 Patent at 1:15-19, 1:57-60.) Applying the standard for “analogous art” stated in the final paragraph of Section IV.B, it is my opinion that a person of ordinary skill in the art would have considered Wang407 to be analogous art to the '194 Patent.



Wang407, Fig. 9

104. Like the '194 Patent, Wang407 describes a “method for forming stressors in metal-oxide-semiconductor (MOS) devices.” (Wang407 at 3:15-16.) And, like the '194 Patent, Wang407 recognized that to “further enhance the performance of MOS devices, stress may be introduced in the channel region of a MOS transistor to improve carrier mobility.” (Wang407 at 1:28-30.) With the goal of improving carrier mobility, Wang407 describes NMOS and PMOS transistors that include raised epitaxial “stressors” adjacent to the gate to strain the channel. (Wang407 at 4:4-21 & Figs. 1-9 (PMOS), 5:58-6:4 & Fig. 11 (NMOS).) Wang407 discloses “formation of shallow trench isolation (STI) regions in a substrate 2,” which can either be bulk silicon or a composite structure, such as silicon-on-insulator (SOI), which are “formed to isolate device regions.” (Wang407 at 3:23-45.) Wang407 further discloses “[l]ightly doped source/drain (LDD) regions 50” formed “by implanting a p-type impurity.” (Wang407 at 4:55-56.) These are formed after “dummy spacers” have been removed, such that Wang407’s “gate stack 12 acts as a mask” and “LDD regions 50 are substantially aligned with the respective edge of gate stack 12.” (Wang407 at 4:49-58, Fig. 8.)

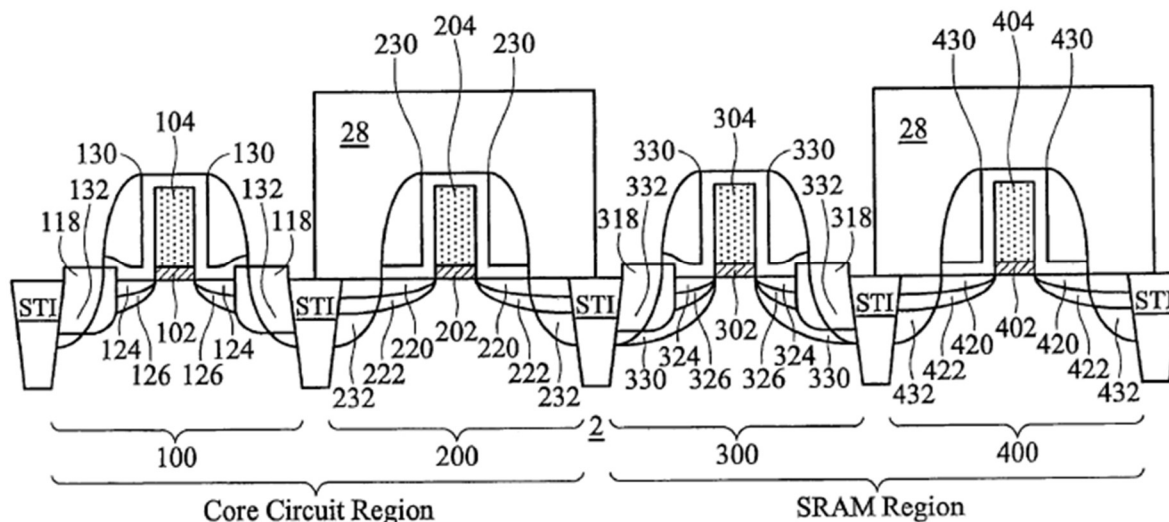
105. As Fig. 9 shows above, the Wang407 device structure includes multi-layered sidewall spacers 52, as well as “a semiconductor substrate [2], a gate stack [including gate dielectric 14 and gate electrode 16] on the semiconductor substrate,

and a stressor [32] adjacent the gate stack and having at least a portion in the semiconductor substrate.” (Wang407 at Abstract, 4:61-67, Fig. 9.)

C. The Wang753 Reference

106. I am not an attorney and am not qualified to assess whether a particular reference qualifies as prior art, but I have been asked to assume that Wang753 qualifies as prior art to the '194 Patent. I note, however, that Wang753 seems to have been filed on April 10, 2006. (Wang753 at cover page.)

107. Wang753 is in the same field as the '194 Patent (MOSFETs and their fabrication), and Wang753 is reasonably pertinent to a problem the '194 Patent purports to address (fabricating strained silicon channel MOS transistors). (*See* Wang753 at Title, Abstract, 1:6-9, 2:29-35; '194 Patent at 1:15-19, 1:57-60.) Applying the standard for “analogous art” stated in the final paragraph of Section IV.B, it is my opinion that a person of ordinary skill in the art would have considered Wang753 to be analogous art to the '194 Patent.



Wang753, FIG. 13^[4]

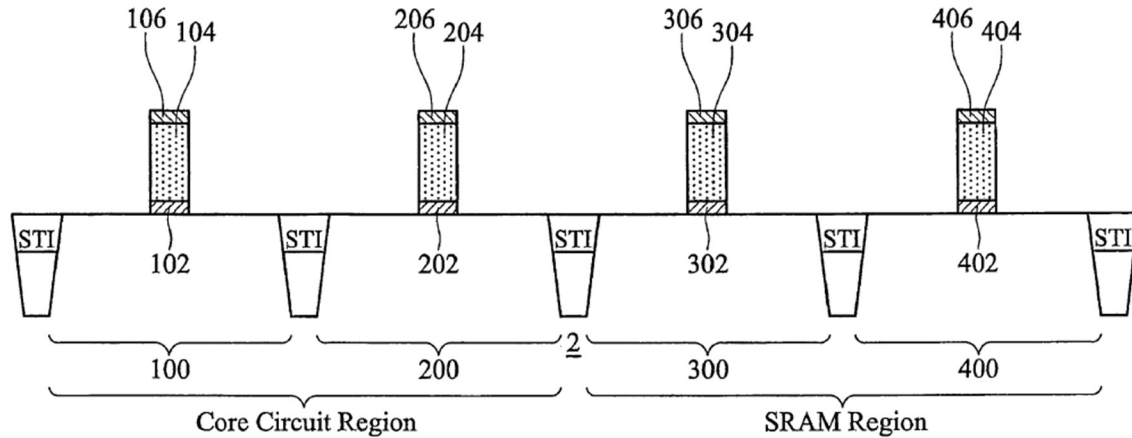
108. The Wang753 reference “relates generally to semiconductor devices, and more particularly to PMOS devices with SiGe stressors, and even more particularly to methods of manufacturing pull-up PMOS devices.” (Wang753 at 1:6-9.) FIG. 13 above shows a “semiconductor structure” with “a core circuit and an SRAM cell.” (Wang753 at 1:51-56, 2:24-29.)

109. The core PMOS devices in active region 100 include “a gate dielectric 102 on substrate 2 and a gate electrode 104 on gate dielectric 102” (Wang753

⁴ Although it does not meaningfully affect my analysis of Wang753, liner oxide layer 25 would not extend over gate electrode 104 in FIG. 13. Rather, it would appear as in Wang753’s FIGS. 11 and 12. A person of ordinary skill in the art would have identified this as a drawing error in FIG. 13. Wang753 explains that the liner oxide layer is “patterned to form spacers 130 . . . as shown in FIG. 11.” (Wang753 at 5:19-22.) Accordingly, the liner oxide layer (25) would appear as in FIGS. 11 and 12, not as in FIG. 13. A person of ordinary skill in the art would have identified this as a drawing error because no processing steps are disclosed that would alter that aspect of the liner oxide layer. (See Wang753 at 5:19-42, FIGS. 11-13.)

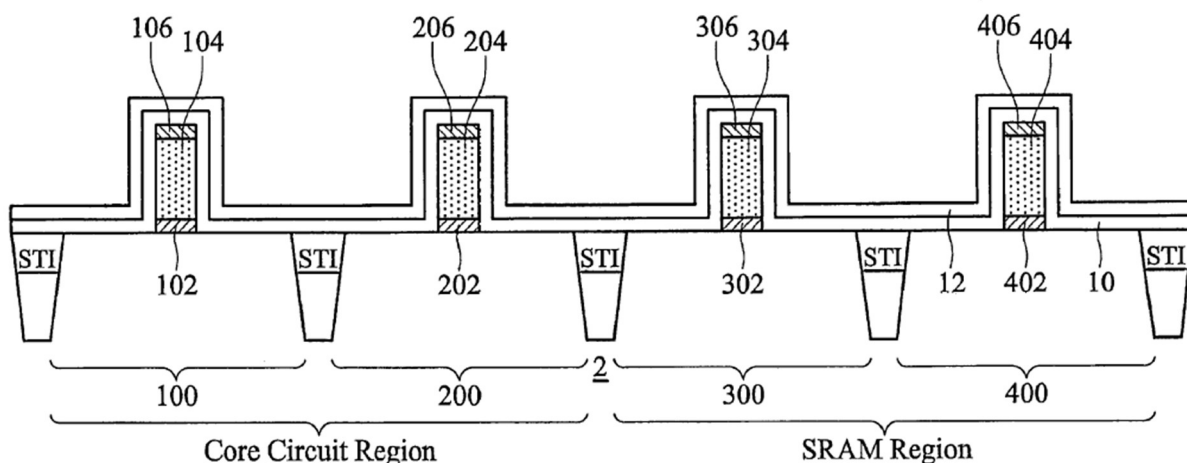
at 3:43-52), raised “SiGe stressors 118” (Wang753 at 4:14-18), and “spacers 130” comprising “a liner oxide layer 25 and a nitride layer 27” (Wang753 at 5:19-26). The core PMOS devices further include “LDD regions 124” formed by introducing p-type impurities. (Wang753 at 4:45-51.) The SRAM PMOS devices in active region 300 are similar, but they additionally include current-tuning regions 330. (Wang753 at 3:52-59, 4:14-18, 4:45-51, 4:56-58.)

110. The Wang753 fabrication process begins by forming shallow trench isolation (“STI”) regions in a semiconductor substrate 2. (Wang753 at 3:39-43.) Gate stacks comprising a gate dielectric (102 / 202 / 302 / 402), a gate electrode (104 / 204 / 304 / 404), and a hard mask (106 / 206 / 306 / 406) are then formed in active regions 100, 200, 300, and 400, as FIG. 2 shows below. (Wang753 at 3:43-59.) Active region 100 contains PMOS devices for the core circuit; active region 200 contains NMOS devices for the core circuit; active region 300 contains PMOS devices for the SRAM circuit; and active region 400 contains NMOS devices for the SRAM circuit. (Wang753 at 3:43-59.)



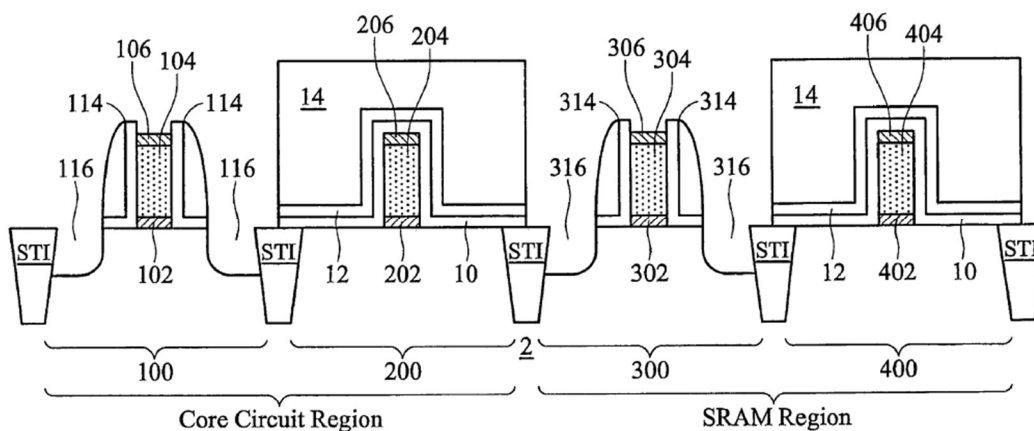
Wang753, FIG. 2

111. Next, “[a] dummy layer, which is used to form spacers, is formed over the core circuit region and the SRAM region, as shown in FIG. 3.” (Wang753 at 3:60-62.) As illustrated below, “the dummy layer [may] comprise[] a liner oxide layer 10 and a nitride layer 12,” but it may alternatively “include single or composite layers comprising oxide, silicon nitride, silicon oxynitride (SiON) and/or other dielectric materials.” (Wang753 at 3:62-4:3.)



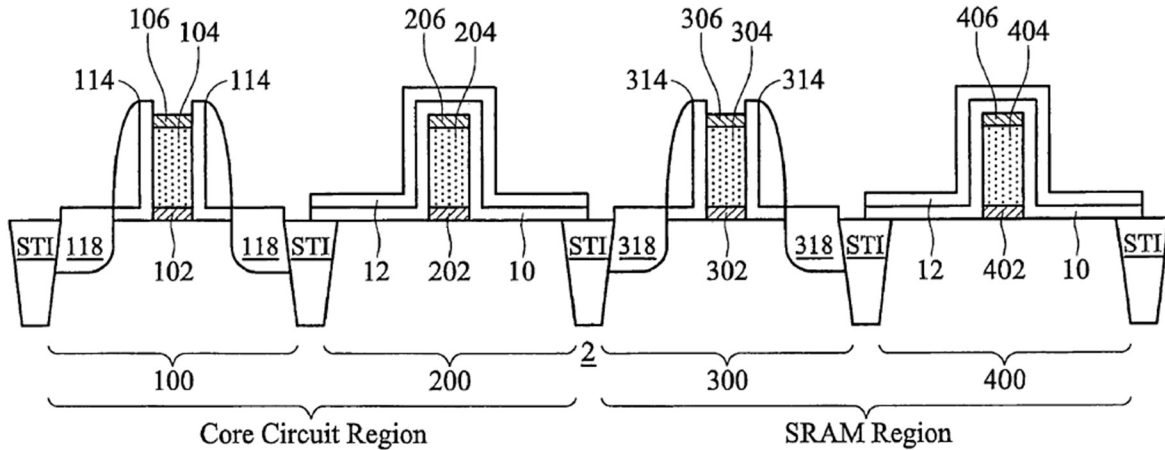
Wang753, FIG. 3

112. “FIG. 4 illustrates the liner oxide layer 10 and nitride layer 12 in PMOS regions 100 and 300 being patterned to form gate spacers 114 and 314, respectively.” (Wang753 at 4:4-6.) The NMOS regions are masked by a photoresist layer 14, and a further etching step creates recesses 116 and 316 “along the outside edges of the spacers 114 and 314, respectively.” (Wang753 at 4:6-12.) The photoresist is then removed. (Wang753 at 4:12-13.)



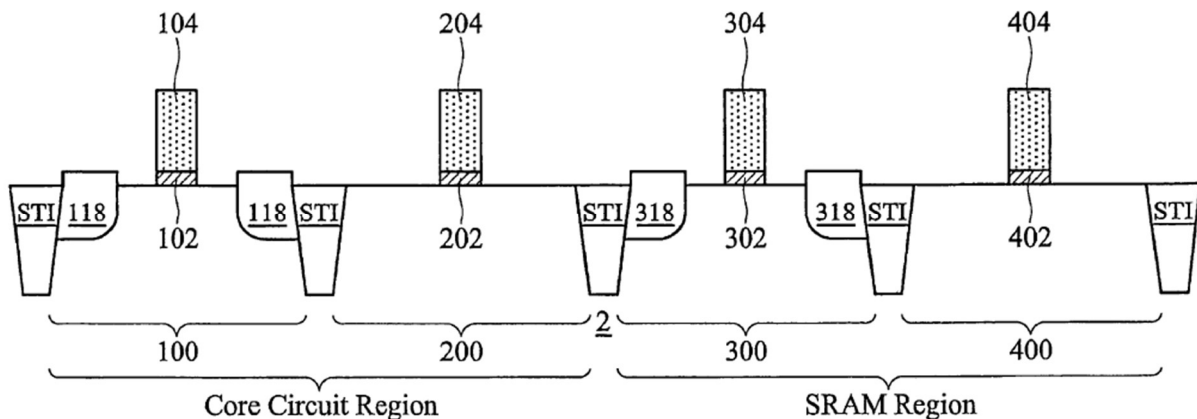
Wang753, FIG. 4

113. “FIG. 5 [below] illustrates the formation of SiGe stressors 118 and 318 in recesses 116 and 316, respectively.” (Wang753 at 4:14-15.) SiGe stressors 118 and 318 are epitaxially grown in recesses 116 and 316, respectively, and they are preferably doped p-type using boron during growth. (Wang753 at 4:15-18.) These SiGe stressors “introduce[] a compressive stress in the channel regions of the resulting PMOS device, and the device drive current of the respective PMOS device is enhanced.” (Wang753 at 4:18-22.)



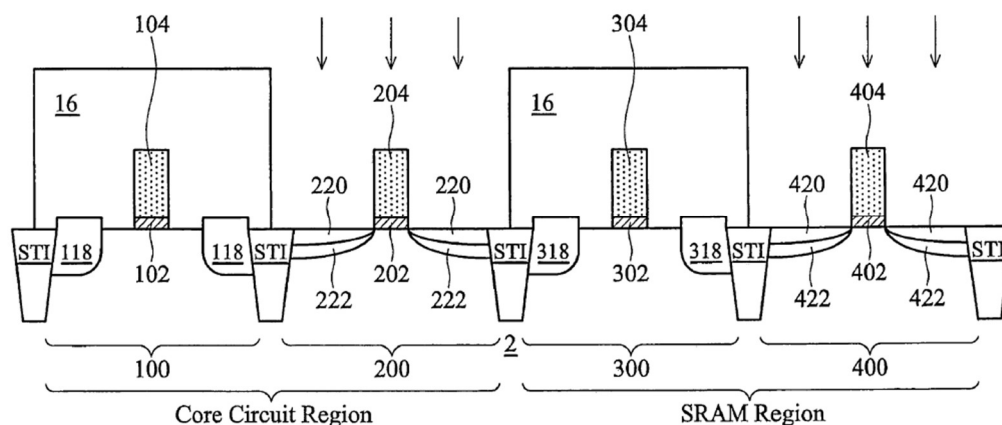
Wang753, FIG. 5

114. After epitaxial stressors 118 and 318 have been grown, “spacers 114 and 314, liner oxide layer 10, silicon nitride layer 12 and hard masks 106, 206, 306 and 406 are removed,” as FIG. 6 shows below. (Wang753 at 4:23-25.) For example, a nitride spacer layer 12 may be removed with hot phosphoric acid, and an oxide liner 10 may be removed using dilute hydrofluoric acid (as was common for selectively removing such materials). (Wang753 at 4:25-29.)



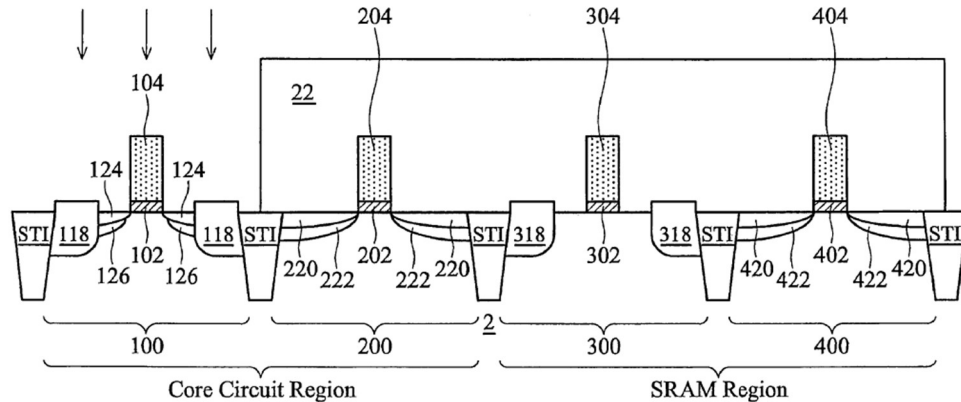
Wang753, FIG. 6

115. Next, “FIGS. 7, 8 and 9 illustrate the formation of lightly doped drain/source (LDD) regions and halo regions for PMOS and NMOS devices.” (Wang753 at 4:30-32.) For example, a photoresist layer 16 is used to mask the PMOS regions, and ion implantation “is performed to introduce n-type impurities into the NMOS regions 200 and 400.” (Wang753 at 4:32-35.) This creates “LDD regions 220 and 420 ... substantially aligned with the edges of the gate electrodes 204 and 404, respectively.” (Wang753 at 4:35-37.) “Halo regions 222 and 422 are formed by implanting p-type impurities. Preferably, halo regions 222 and 422 have a greater depth than the respective LDD regions 220 and 420. More preferably, halo regions 222 and 422 are located substantially adjacent junction borders at the bottoms and sides of the respective LDD regions 220 and 420. ” (Wang753 at 4:37-43.) Photoresist layer 16 is then removed. (Wang753 at 4:43.) Wang753 further explains: “The details for forming LDD regions and halo regions are known in the art, thus are not repeated herein.” (Wang753 at 4:43-45.)



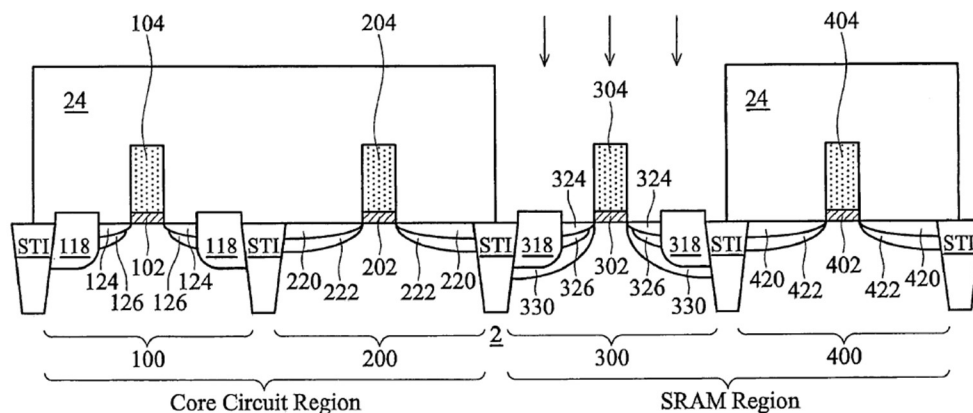
Wang753, FIG. 7

116. Then, as FIG. 8 shows below, “active regions 200, 300 and 400 are masked by a photo resist 22,” and “LDD regions 124 are formed by introducing p-type impurities” into active region 100. (Wang753 at 4:46-50.) Photoresist layer 22 is then removed. (Wang753 at 4:51.)



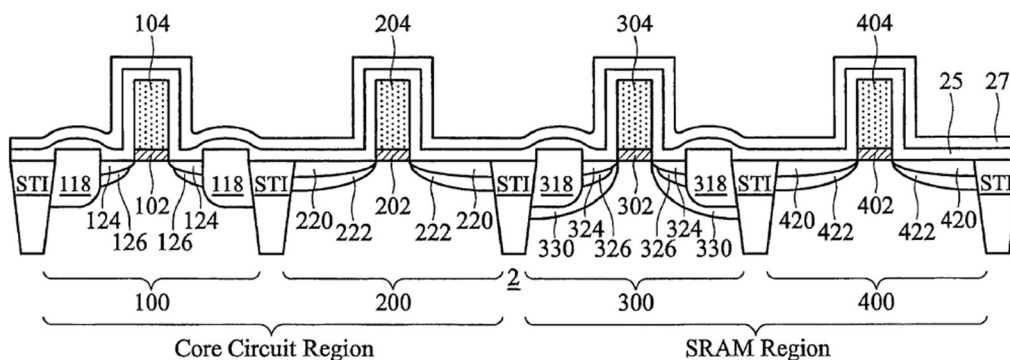
Wang753, FIG. 8

117. Next, as FIG. 9 illustrates below, “photo resist 24 is formed covering the core circuit region and NMOS region 400,” and “LDD regions 324 are the[n] formed by implanting p-type impurities.” (Wang753 at 4:52-55.) Current-tuning regions 330 are then formed in action region 300. (Wang753 at 4:56-5:18.)

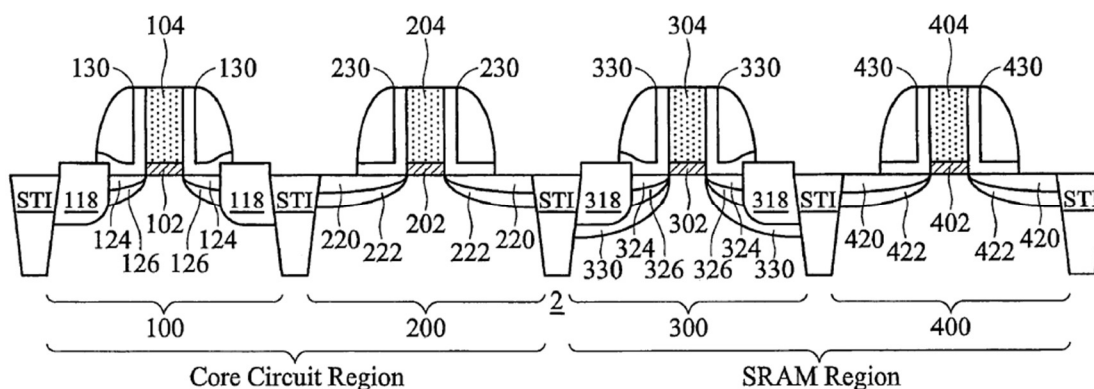


Wang753, FIG. 9

118. Subsequently, “FIGS. 10 and 11 illustrate the formation of spacers.” (Wang753 at 5:19.) For example, “a liner oxide layer 25 and a nitride layer 27 are blanket formed” (FIG. 10), and “[t]he two layers are then patterned to form spacers 130, 230, 330 and 430, as shown in FIG. 11.” (Wang753 at 5:19-22.) Wang753 further explains that, preferably, “spacers 130 and 330 have a thickness greater than that of spacers 114 and 314” such that “spacers 130 and 330 have portions on SiGe stressors 118 and 318, respectively.” (Wang753 at 5:22-27.)

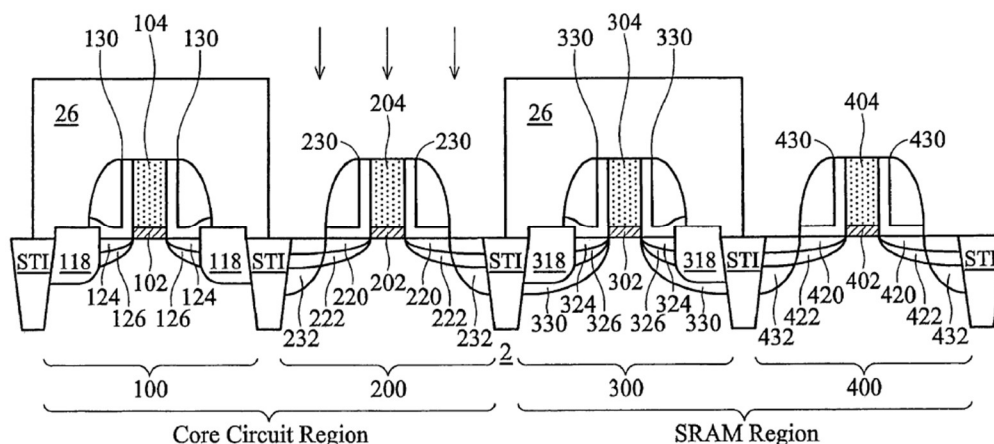


Wang753, FIG. 10



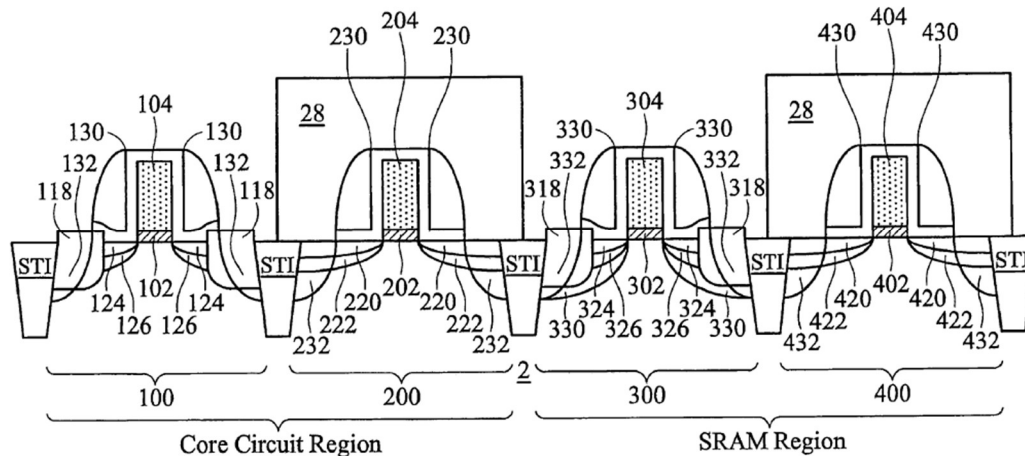
Wang753, FIG. 11

119. After spacers 130 / 230 / 330 / 430 have been formed, “FIG. 12 [below] illustrates the formation of deep source/drain regions 232 and 432 in core NMOS region 200 and SRAM NMOS region 400, respectively, preferably by implanting n-type impurities.” (Wang753 at 5:28-31.) PMOS active regions 100 and 300 are masked by a photoresist layer 26 during this process. (Wang753 at 5:31-32.) Photoresist layer 26 is then removed. (Wang753 at 5:34-35.)



Wang753, FIG. 12

120. Finally, “FIG. 13 illustrates a similar process for forming deep source/drain regions [132 and 332] for PMOS devices, preferably by implanting p-type impurities.” (Wang753 at 5:36-38.) NMOS active regions 200 and 400 are masked by a photoresist layer 28 during this process. (Wang753 at 5:38-39.) Photoresist layer 28 is then removed. (Wang753 at 5:42.)



Wang753, FIG. 13

IX. THE CHALLENGED CLAIMS ARE ANTICIPATED AND/OR OBVIOUS IN VIEW OF THE PRIOR ART

121. By December 29, 2006, methods of forming structures like the ones described in the '194 Patent were already known and used throughout the semiconductor industry. Because the relevant principles, fabrication methods, and MOS structures were already thoroughly established and widely known, a person of ordinary skill in the art would have found the claimed structures in the '194 Patent were already known or at least obvious. The following sections explain why I reach that conclusion in greater detail, and the chart below summarizes the grounds I address in my analysis.

Ground	Claim(s) Challenged	35 U.S.C. §	Reference(s)
1A	1-4, 6-7, 10, 12-13, 15-16, 21-22	102	Hoentschel262
1B	1-22	103	Hoentschel262
1C	5, 7-9, 11, 14, 17-20	103	Hoentschel262, Wang407
2A	1-3, 5-12, 14-16, 21, 22	102	Wang753
2B	1-3, 5-12, 14-16, 21, 22	103	Wang753
2C	4, 13	103	Wang753, Hoentschel262

A. Grounds 1A and 1B: Hoentschel262 Alone Anticipates (Ground 1A) and Renders Obvious (Ground 1B) Claims 1-4, 6-7, 10, 12-13, 15-16, and 21-22

122. Hoentschel262 teaches, suggests, and renders obvious all the elements of claims 1-4, 6-7, 10, 12-13, 15-16, and 21-22 of the '194 Patent.

123. Through the analysis below, I conclude that Hoentschel262 anticipates claims 1-4, 6-7, 10, 12-13, 15-16, and 21-22 (Ground 1A) because Hoentschel262 discloses every limitation of those claims when viewed from the perspective of a person of ordinary skill in the art.

124. For essentially the same reasons stated in my analysis below, I also conclude that Hoentschel262 renders claims 1-4, 6-7, 10, 12-13, 15-16, and 21-22 obvious (Ground 1B) because the differences between claims 1-4, 6-7, 10, 12-13, 15-16, and 21-22 and Hoentschel262 are such that claims 1-4, 6-7, 10, 12-13, 15-16, and 21-22 would have been obvious to a person of ordinary skill in the art.

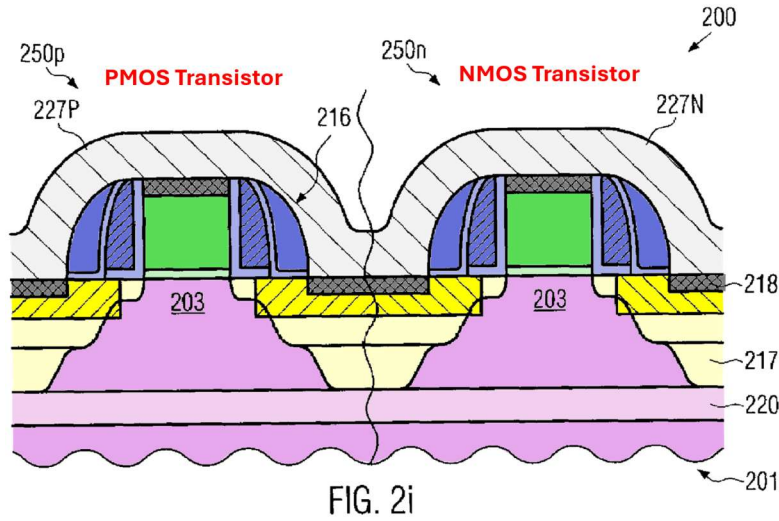
1. Independent Claims 1 and 10

a. 1[pre]/10[pre]: “A method of fabricating a [MOS/CMOS] transistor, comprising:”

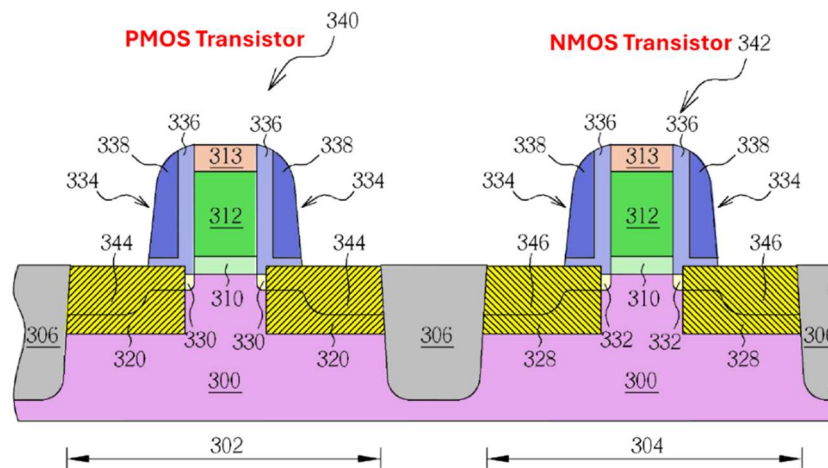
125. Hoentschel262 discloses both “[a] method of fabricating a MOS transistor” as recited in 1[pre] and “[a] method of fabricating a CMOS transistor” as recited in 10[pre].

126. Hoentschel262 discloses “the formation of different transistor types,” including CMOS circuits with both P-channel and N-channel transistors (Hoentschel262 at 1:8-14; 1:24-27; 14:56-15:5.)

127. As the comparison between Hoentschel262 and the '194 Patent below demonstrates, Hoentschel262's CMOS transistors have the same basic arrangement as in the '194 Patent. For example, both include the same basic arrangement of gate, spacers, source/drain epitaxy layers, lightly doped regions, and substrate.



Hoentschel262, FIG. 2i

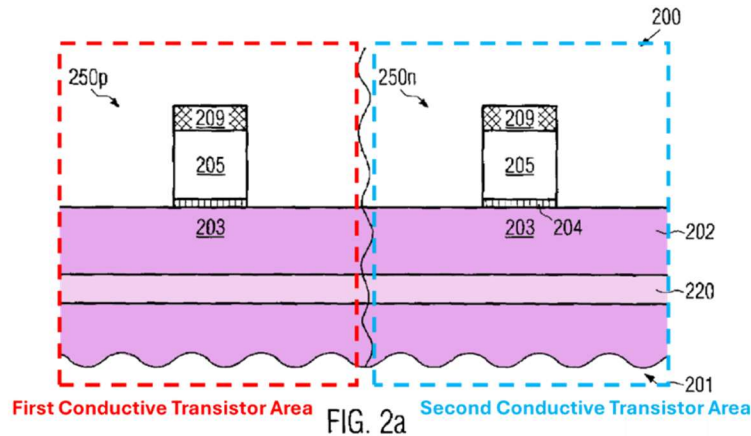


- b. 1[a]/10[a]: “providing a semiconductor substrate [having at least a first conductive transistor area for fabricating first conductive transistors and at least a second conductive transistor area for fabricating second conductive transistors, and an isolation structure between the first conductive transistor area and the second conductive transistor area]”

128. Hoentschel262 discloses both “providing a semiconductor substrate” as recited in 1[a] and “providing a semiconductor substrate having at least a first

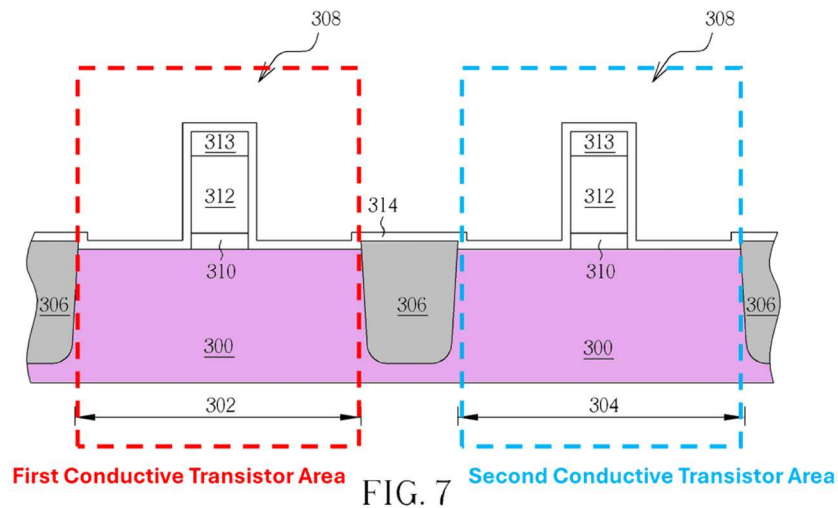
conductive transistor area for fabricating first conductive transistors and at least a second conductive transistor area for fabricating second conductive transistors, and an isolation structure between the first conductive transistor area and the second conductive transistor area” as recited in 10[a].

129. The '194 Patent explains that semiconductor substrate 200 may be “a silicon-on-insulator (SOI) substrate, but not limited thereto.” ('194 Patent at 3:4-6.) Hoentschel262 likewise discloses “an SOI substrate.” (Hoentschel262 at 6:12-15.) For example, Hoentschel262’s disclosed method includes an SOI substrate that includes, collectively, “a substrate 201 [dark pink] having formed thereon, in one illustrative embodiment, a buried insulating layer 220 [light pink], above which is formed a semiconductor layer 202 [dark pink].” (Hoentschel262 at 12:13-17.) Hoentschel262 includes an SOI substrate having at least two conductive transistor areas—a “first transistor 250p” [red] and a “second transistor 250n” [blue] (Hoentschel262 at 12:24-27.)



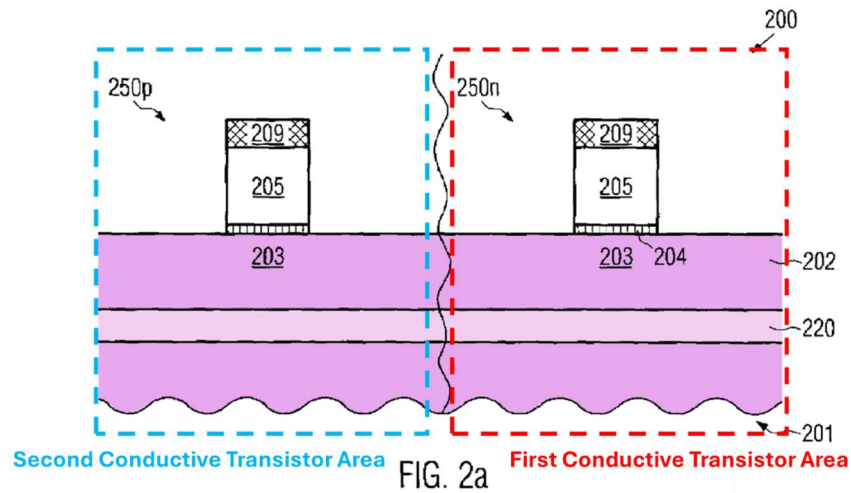
Hoenstchel262, FIG. 2a

130. As the comparison to FIG. 7 of the '194 Patent shows, the '194 Patent's method is substantially similar:



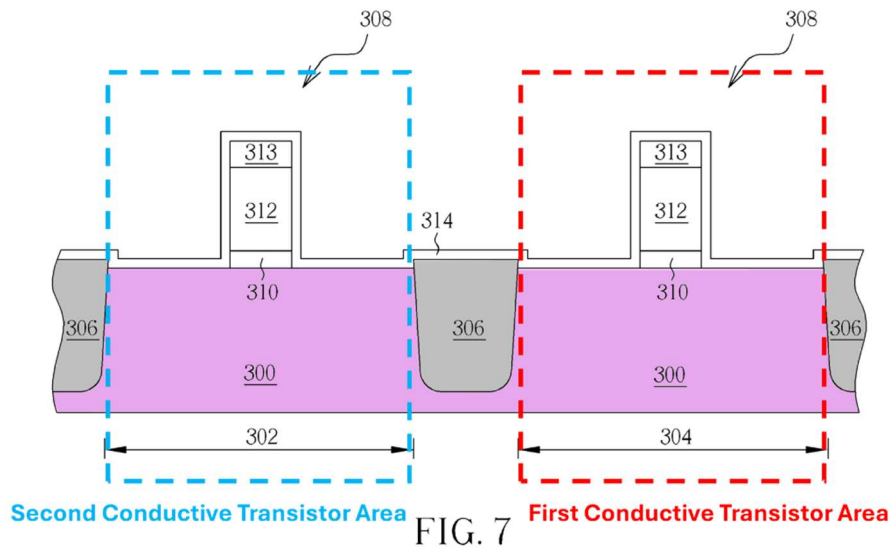
'194 Patent FIG. 7

131. Alternatively, for claim 22, the “first” and “second” designations could be swapped, as they are arbitrary. I have been instructed that designation of “first” and “second” are a common patent-law convention to distinguish between repeated instances of an element or limitation (e.g., multiple conductive transistor areas).



Hoenstchel262, FIG. 2a

132. The same is true for the '194 Patent, as the designation of “first” and “second” is arbitrary. Indeed, the '194 Patent states that “the process of forming the first epitaxial layer 320 as shown in FIG. 7 to FIG. 9 might be performed after the process of forming the second epitaxial layer 328 as shown in FIG. 10 to FIG. 12.” ('194 Patent at 6:27-34.).



'194 Patent, FIG. 7

133. Hoenstchel262 discloses isolation structures, including shallow trench isolation regions. The specification states, for example, that “manufacturing processes for forming isolation structures (not shown), such as shallow trench isolations, may be performed on the basis of well-established techniques.” (Hoentschel262 at 7:17-20.) A person of skill would have understood isolation structures like shallow trench isolation (“STI”) structures are an essential, textbook element of any MOSFET integrated circuits, used to electrically separate the transistors from one another. Plummer’s textbook, for example, explains that “we need to make certain that the individual devices on the chip are electrically isolated from each other. This is accomplished most often by growing a fairly thick layer of SiO₂ in between each of the active devices.” (Plummer at 53; *see also* Plummer at 52-63 (describing LOCOS and STI isolation methods); Quirk at 207-10, 311-12 & FIG. 12.12 (similar); Wang407 at 3:23-30, FIGS. 9, 11 (similar).) A person of ordinary skill in the art would have understood that the squiggly vertical line between PMOS and NMOS devices in Hoentschel262’s figures is a simplification to avoid depicting the necessary isolation structure between them.

134. I have been informed that a disclosure is anticipatory if a person of ordinary skill in the art would “at once envisage” the claimed arrangement or combination. That is certainly true for the isolation structures described in Hoentschel262’s text but omitted from the figures. A person of ordinary skill in the

art would have understood an isolation structure separates PMOS device 250p and NMOS device 250n because it was part of basic semiconductor device design—a detail unnecessary to describe in any detail given its fundamental nature in the art and the training and knowledge of a person of ordinary skill in the art. It is therefore my opinion that Hoentschel262 expressly discloses an isolation structure between PMOS device 250p and NMOS device 250n (Ground 1A).

135. Additionally, it is my opinion that a person of ordinary skill in the art would have found it obvious to include STI as an isolation structure between PMOS device 250p and NMOS device 250n (Ground 1B). First, Hoentschel262 expressly states that “shallow trench isolations, may be performed on the basis of well-established techniques.” (Hoentschel262 at 7:17-20.) And second, such isolation structures were a fundamental part of MOSFET device design and semiconductor processing.

136. Additionally, it is my opinion that buried insulation layer 220 also constitutes an isolation structure between the first and second conductive transistor areas. As Hoentschel262 describes, “a substrate 201 having formed thereon, in one illustrative embodiment, a buried insulating layer 220, above which is formed a semiconductor layer 202.” (Hoentschel262, 12:14-17.) This buried insulation layer 220, shown in pink below, is present across the entire wafer, including between first transistor 250p and second transistor 250n, and acts to provide “an SOI-like

device.” (Hoentschel262, 12:13-31.) This, too, is an isolation structure between the first and second transistor areas. Buried oxide insulation layer 220 itself provides isolation between transistors, as current flowing downward and upward between devices is eliminated.

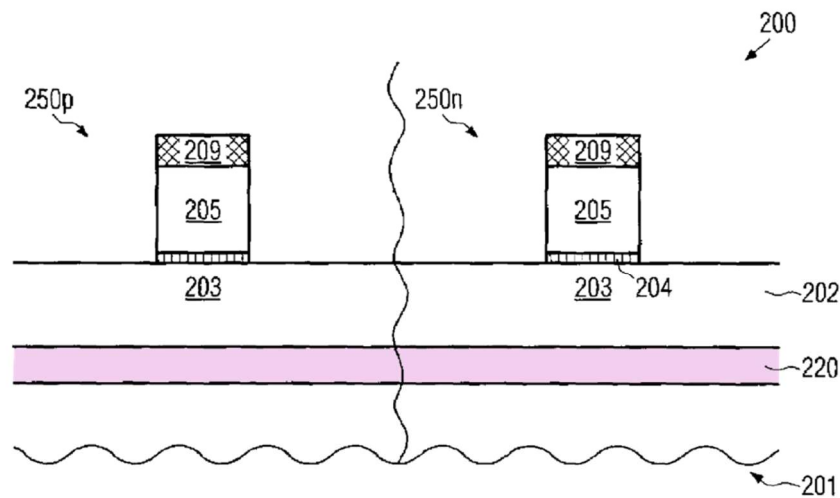


FIG. 2a

Hoentschel262, FIG. 2a

137. To create functional transistors, a person of ordinary skill in the art would have understood that adjacent device regions would additionally be separated by a shallow trench isolation (STI) or the like that extends down to the buried oxide layer 220 to fully isolate those adjacent device regions. (See Hoentschel292, 7:11-21 (“After the provision of the substrate 101 and the semiconductor layer 102, . . . manufacturing processes for forming isolation structures (not shown), such as shallow trench isolations, may be performed on the basis of well-established techniques.”).) A person of ordinary skill in the art would have known that a SOI

CMOS configuration would further include an isolation structure like STI in addition to the buried oxide layer of an SOI wafer.

- c. **1[b]/10[b]: “forming [at least a / a] gate on the [semiconductor substrate / first conductive transistor area and on the second conductive transistor area respectively];”**

138. Hoentschel262 discloses both “forming at least a gate on the semiconductor substrate” as recited in 1[b] and “forming a gate on the first conductive transistor area and on the second conductive transistor area respectively” as recited in 10[b].

139. In Hoenstchel262, “respective gate electrodes 205 [dark green] are formed on respective gate insulation layers 204 [light green],” with “capping layers 209 [peach].” (Hoentschel262 at 12:24-27.) Thereby, the first and second gate electrodes are “formed above a substrate comprising a crystalline semiconductor layer,” thus forming a gate on each transistor area of the substrate as claimed. (Hoentschel262 at 3:51-56.)

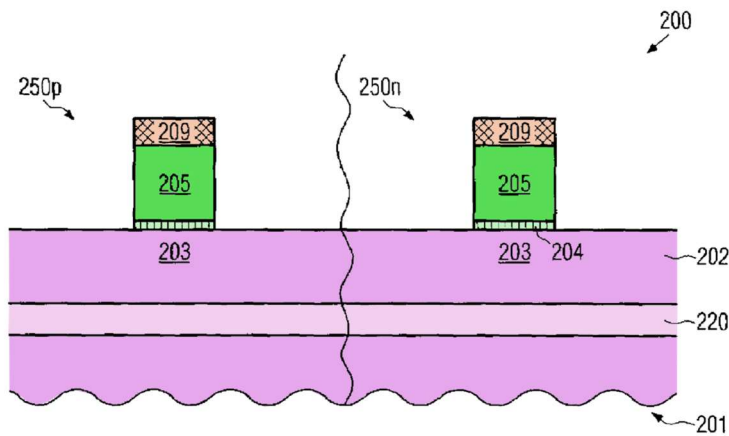
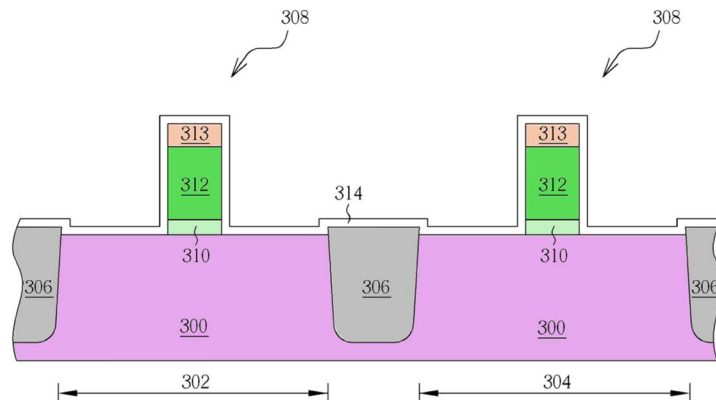


FIG. 2a

Hoentschel262, FIG. 2a

140. The '194 Patent's method similarly forms gates 308, which include dielectric layers 310, conductive layers 312, and capping layers 313. ('194 Patent at 5:4-15.)



'194 Patent, FIG. 7

- d. 1[c]/10[c]: “forming a [first] protective layer on the semiconductor substrate, and the [first] protective layer covering the surface of [the/each] gate;”

141. Hoentschel262 discloses both “forming a protective layer on the semiconductor substrate, and the protective layer covering the surface of the gate”

as recited in 1[c] and “forming a first protective layer on the semiconductor substrate, and the first protective layer covering the surface of each gate” as recited in 10[c].

142. In Hoentschel262, “a first spacer layer 206A [dark blue], possibly in combination with a respective liner 207A [light blue], may be formed on the first and second transistors 250p, 250n,” thereby forming a first protective layer covering the surface of each gate. (Hoentschel262 at 12:33-35.) This layer protects the devices when subsequently etching recesses 211p into the substrate. (Hoentschel262 at 12:64-13:20, FIG. 2d.)

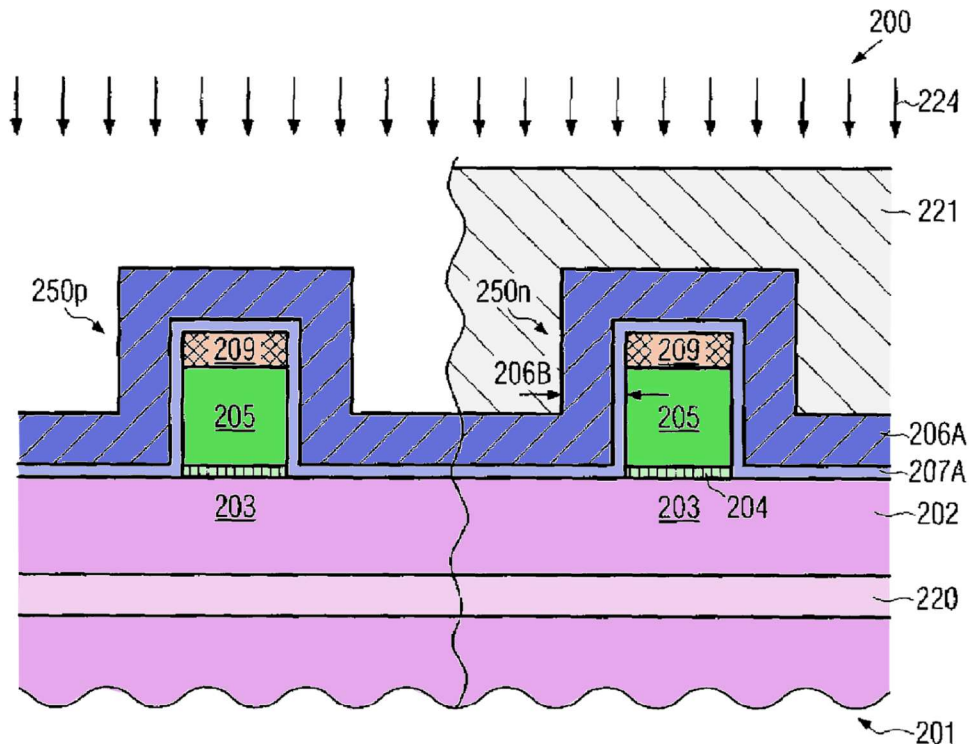
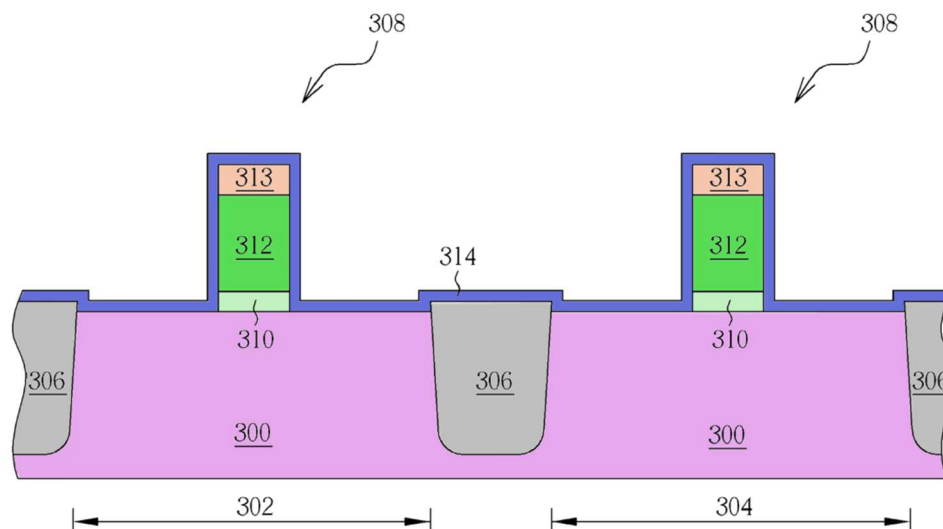


FIG. 2b

Hoentschel262, FIG. 2b

143. The '194 Patent's method similarly forms protective layer 314.
('194 Patent at 5:16-32.)



'194 Patent, FIG. 7

- e. **1[d]/10[d]: “forming at least a [first] recess within the semiconductor substrate adjacent to the gate [in the first conductive transistor area];”**

144. Hoentschel262 discloses both “forming at least a recess within the semiconductor substrate adjacent to the gate” as recited in 1[d] and “forming at least a first recess within the semiconductor substrate adjacent to the gate in the first conductive transistor area” as recited in 10[d].

145. In Hoentschel262, the device is etched to form respective recesses or cavities 211p [dotted red lines] in the first transistor 250p.” (Hoentschel262 at 13:2-5.) Recess 211p forms adjacent to the gate with an offset defined by “spacer width 206B.” (Hoentschel262 at 13:5-20.) This advantageously “enable[es] the

positioning of strained semiconductor material close to a channel region.”
(Hoentschel262 at 3:30-40.)

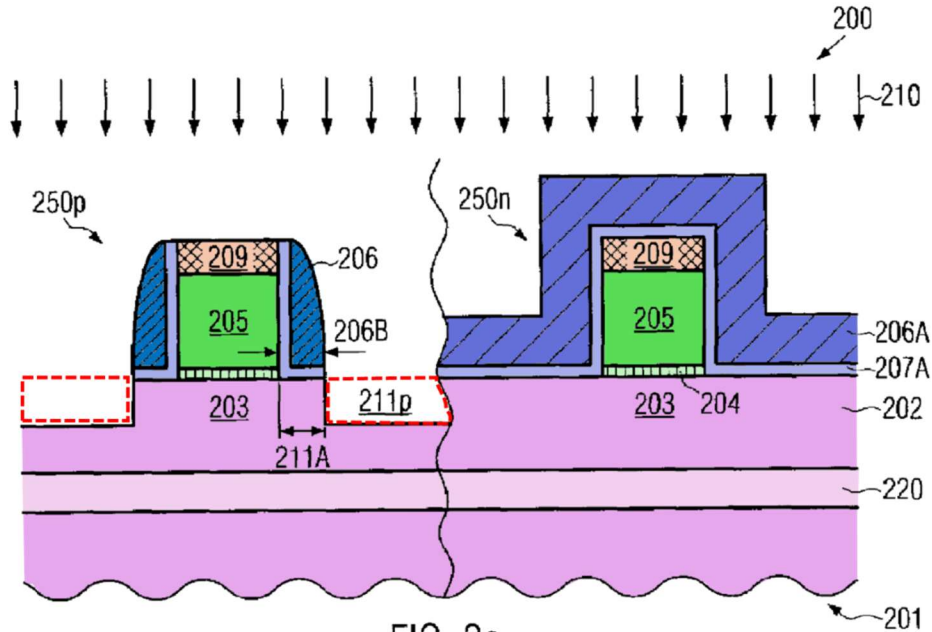
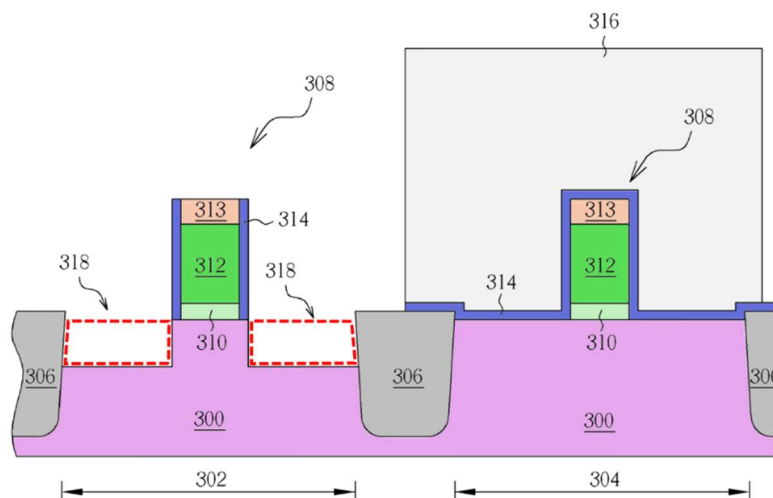


FIG. 2c

Hoentschel262, FIG. 2c

146. The '194 Patent's method similarly etches the substrate to form first recesses 318. ('194 Patent at 5:27-32.)



'194 Patent, FIG. 8

147. Alternatively, for purposes of analyzing claim 22, the “first” area is the NMOS transistor area. Hoentschel262 also explains that “a further etch process may be performed to form a respective recess or cavity 211n, as indicated in dashed lines.” (Hoentschel262 at 14:7-13.)

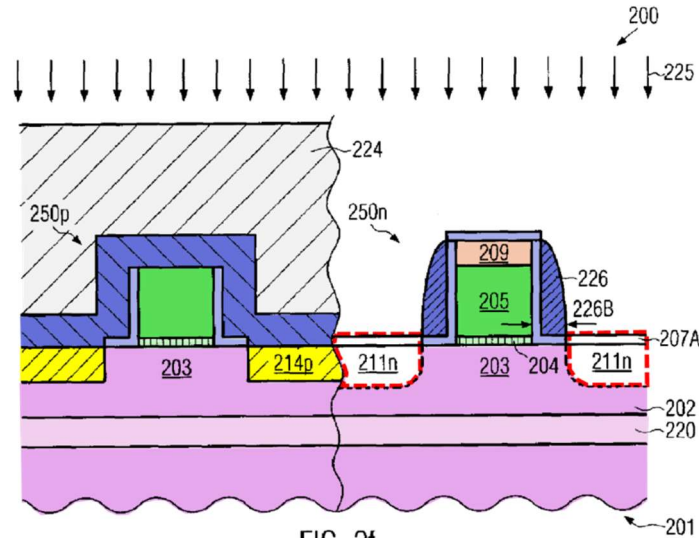
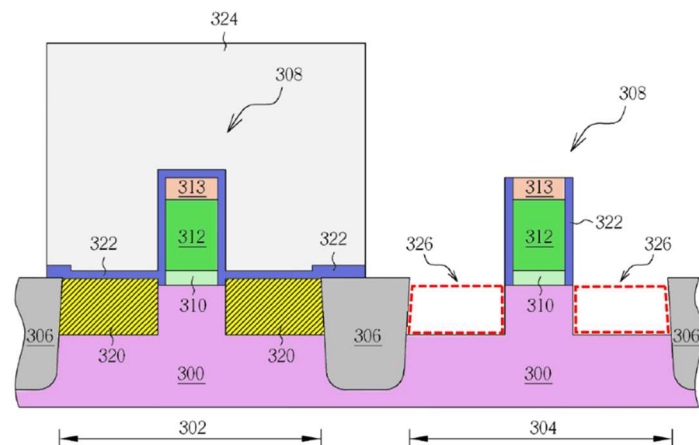


FIG. 2f

Hoentschel262, FIG. 2f

148. The '194 Patent's method similarly etches the substrate to form recesses 326. ('194 Patent at 5:60-65.)



'194 Patent, FIG. 11

f. 1[e]/10[e]: “forming [an/a first] epitaxial layer in the [first] recess, wherein the top surface of the [first] epitaxial layer is above the surface of the semiconductor substrate; and”

149. Hoentschel262 discloses both “forming an epitaxial layer in the recess, wherein the top surface of the epitaxial layer is above the surface of the semiconductor substrate” as recited in 1[e] and “forming a first epitaxial layer in the first recess, wherein the top surface of the first epitaxial layer is above the surface of the semiconductor substrate” as recited in 10[e].

150. In Hoentschel262, “an epitaxial growth process 213” forms “a strained semiconductor material 214p [yellow] in the recess 211p.” (Hoentschel262 at 13:21-26.) This epitaxial process can include “*any desired degree of* underfilling or *overfilling*.” (Hoentschel262 at 13:21-26.) FIG. 2d may show material 214p flush with the substrate, but a person of ordinary skill in the art would have understood from this disclosure that it may be raised, as was common. (See Section VI.B above.)

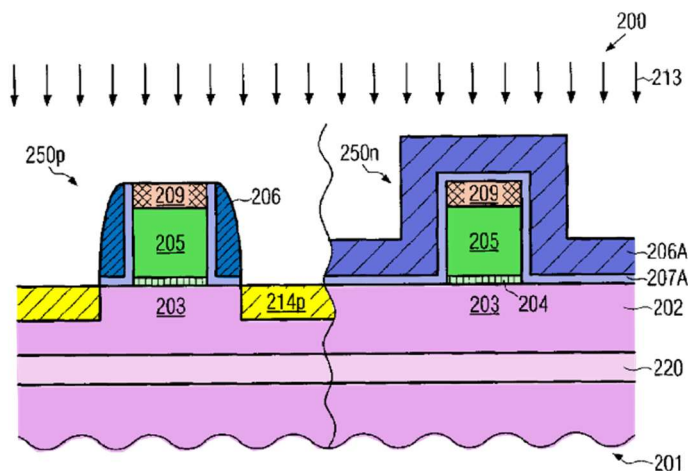
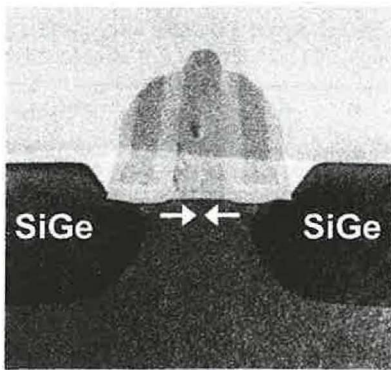


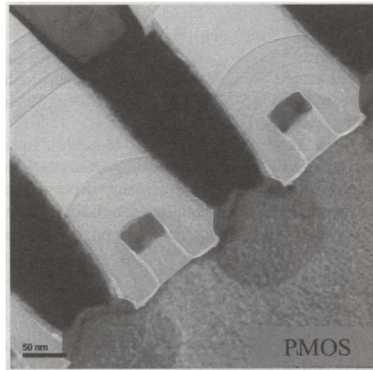
FIG. 2d

Hoerstchel262, FIG. 2d

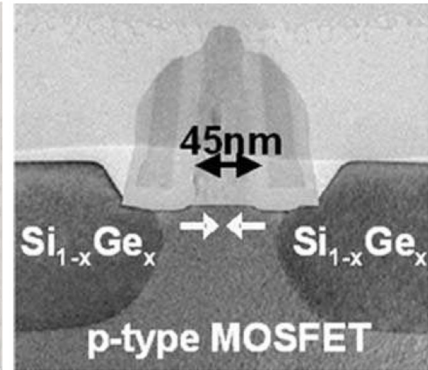
151. Although a person of ordinary skill in the art would have understood Hoentschel262 discloses a raised epitaxial layer (Ground 1A), a person of ordinary skill in the art also would have found it obvious (Ground 1B). A person of ordinary skill in the art would have understood raised epitaxy regions improved performance by increasing strain transfer and reducing contact resistance. For example, the James reference explains that epitaxial SiGe “[c]rystalline facets form raised source/drains, reducing the series resistance.” (James at 2-3; *see also* James at Fig. 6.) Such raised epitaxy regions were common in widely used commercial devices, as shown below.



Ghani, Fig. 1

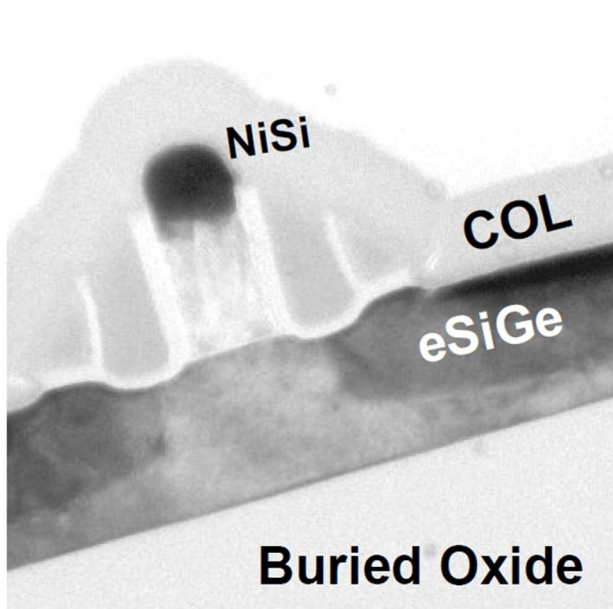


Bai, Fig. 4

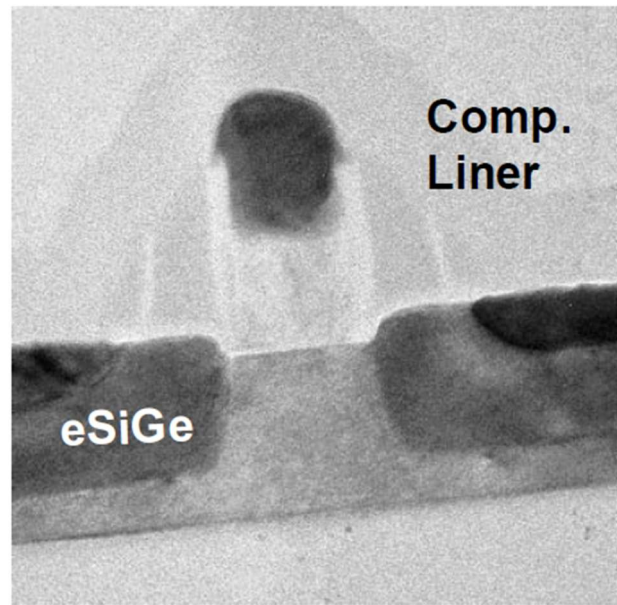


Thompson, Fig. 1

Moreover, the inventors of Hoentschel262 publicly disclosed real-world embodiments of their device structure with raised epitaxial SiGe stressors, as shown below. Those embodiments look exactly as one would have readily understand from Hoentschel262’s textual disclosures.

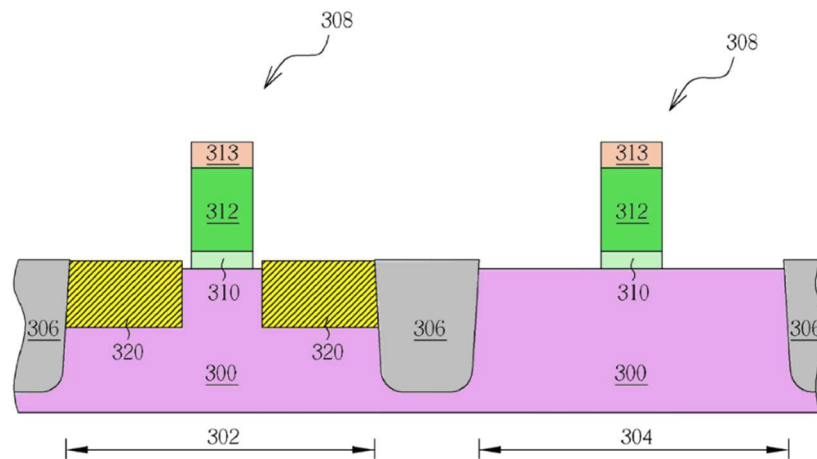


Wei, Fig. 2



Horstmann, Fig. 2

152. The '194 Patent's method similarly grows epitaxial layers 320 "higher than the surface of the semiconductor substrate 300." ('194 Patent at 5:33-42.)



'194 Patent, FIG. 9

153. Alternatively, for purposes of analyzing claim 22, the "first" area is the NMOS transistor area. Hoentschel262 further discloses that, "after a corresponding cavity etch process for actually forming the recesses 211n, [device 200] is subjected

to a further selective epitaxial growth process 215 for forming a strained semiconductor material 214N.” (Hoenstchel262 at 14:18-27.) “[T]he same criteria apply as previously explained [for device 100].” (Hoenstchel262 at 14:18-27.) Accordingly, this epitaxial process can include “*any desired degree of underfilling or overfilling.*” (Hoentschel262 at 13:21-26.)

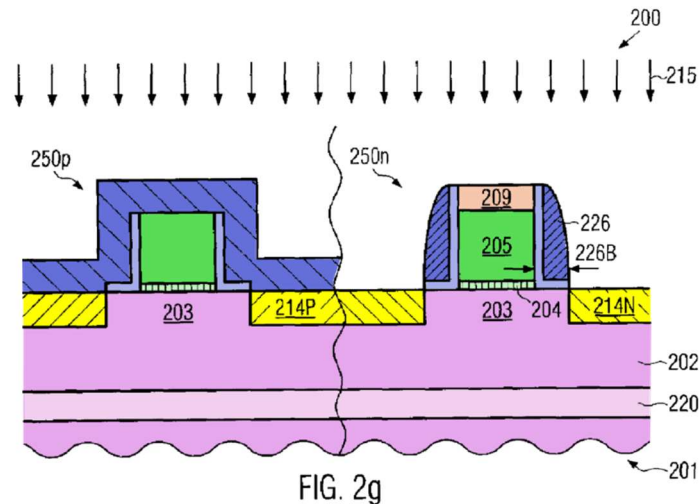
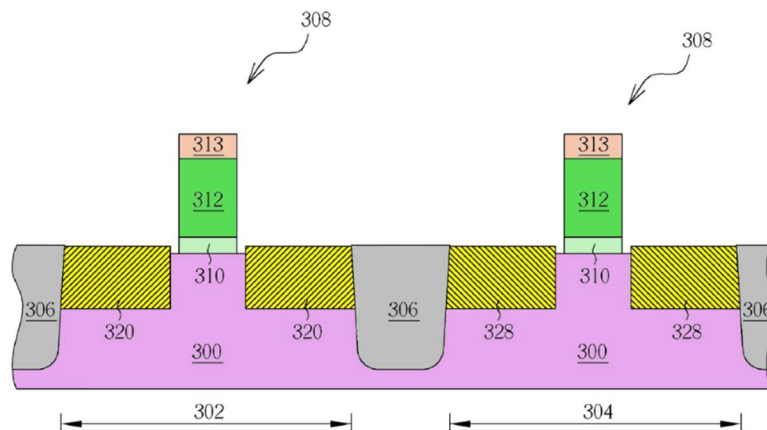


FIG. 2g
Hoenstchel262, FIG. 2g

154. The '194 Patent's method similarly grows epitaxial layers 328 “higher than the surface of the semiconductor substrate 300.” ('194 Patent at 6:13-22.)

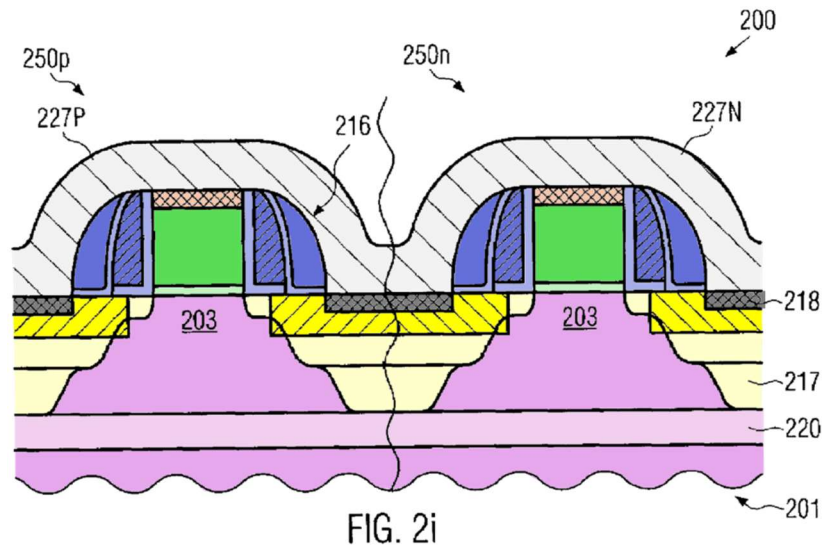


'194 Patent, FIG. 12

- g. 1[f]/10[f]: “forming a spacer on the sidewall of [the/each] gate and [at least] on a portion of the [first] epitaxial layer[,] wherein a contact surface of the [first] epitaxial layer and the spacer is above the surface of the semiconductor substrate.”**

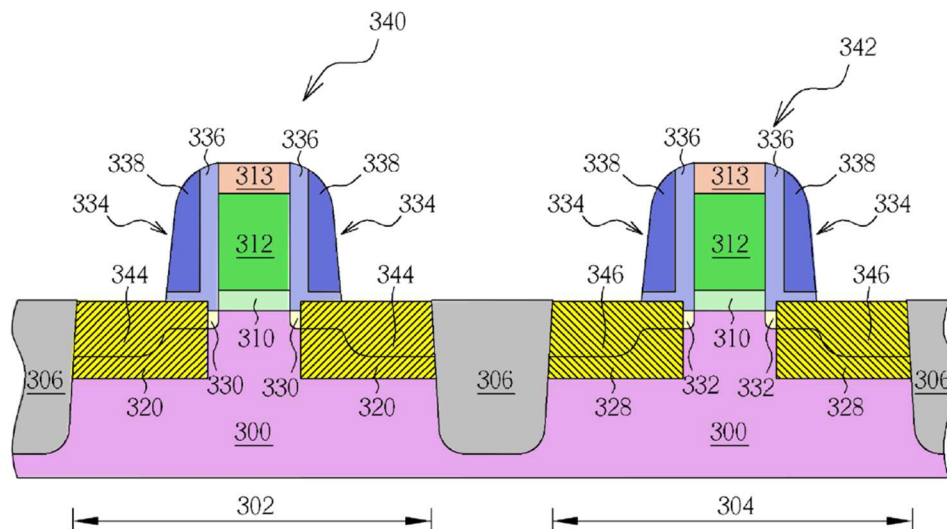
155. Hoentschel262 discloses both “forming a spacer on the sidewall of the gate and on a portion of the epitaxial layer wherein a contact surface of the epitaxial layer and the spacer is above the surface of the semiconductor substrate” as recited in 1[f] and “forming a spacer on the sidewall of each gate and at least on a portion of the first epitaxial layer, wherein a contact surface of the first epitaxial layer and the spacer is above the surface of the semiconductor substrate” as recited in 10[f].

156. In Hoentschel262, “a corresponding sidewall spacer structure 216 [dark blue and light blue], [is] formed on the respective gate electrodes 205.” (Hoentschel262 at 14:48-52.) These spacers “may have been used for defining respective lateral and vertical dopant profiles for respective drain and source regions 217,” and “the spacer structures 216 may comprise any appropriate number of individual spacer elements, depending on the complexity of the required dopant profile of the regions 217.”) (Hoentschel262 at 14:48-56.)



Hoentschel262, FIG. 2i

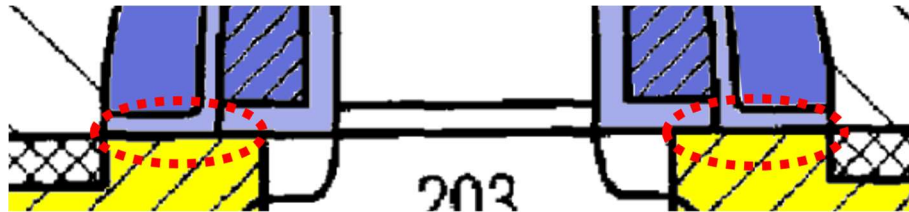
157. Similarly, in the '194 Patent method “spacers 334 are formed on the sidewalls of each gate 308.” ('194 Patent at 6:45-46.)



158. Further, in Hoentschel262, the spacers are pictured as formed above, extending onto a portion of the previously formed epitaxial layers 214p and 214n. Since those epitaxial layers may be raised (as I explain above for 1[e] and 10[e]), a

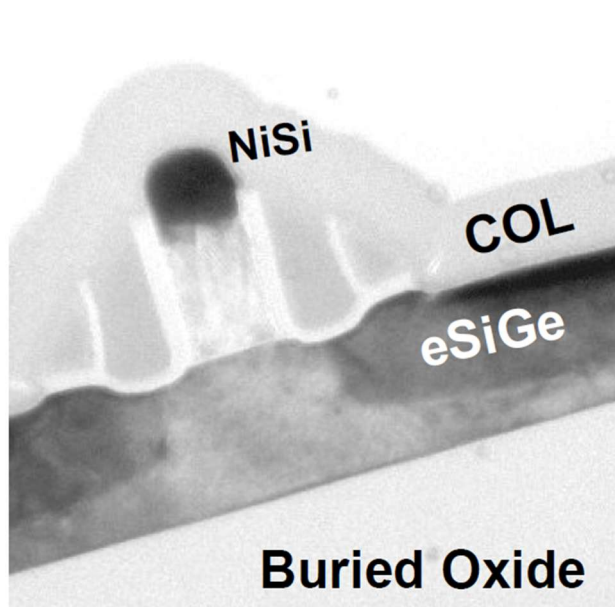
Declaration of Prof. Eugene Fitzgerald, Ph.D.

person of ordinary skill in the art would have understood (Ground 1A) and at least found obvious (Ground 1B) that the spacers and the [first] epitaxial layer have a contact surface (circled in red) above the substrate.

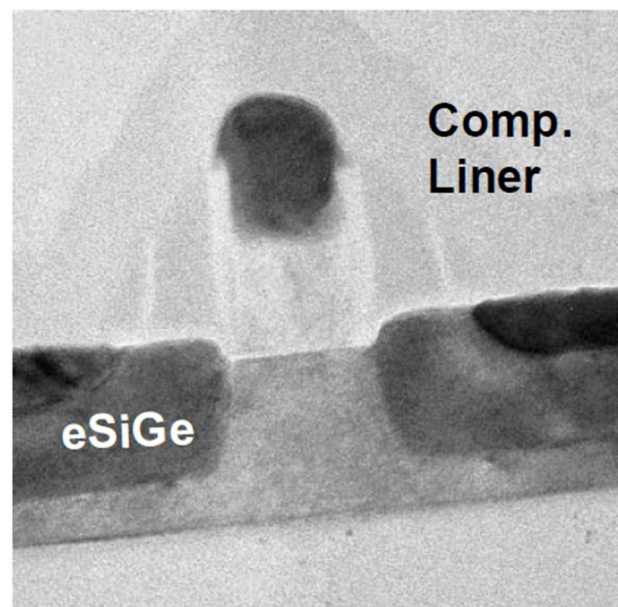


Hoentschel262, FIG. 2i (excerpted)

The inventors of Hoentschel262 publicly disclosed real-world embodiments of their device structure with precisely such a configuration (shown below), consistent with what a person of ordinary skill in the art would have readily understood from Hoentschel262's textual disclosures.

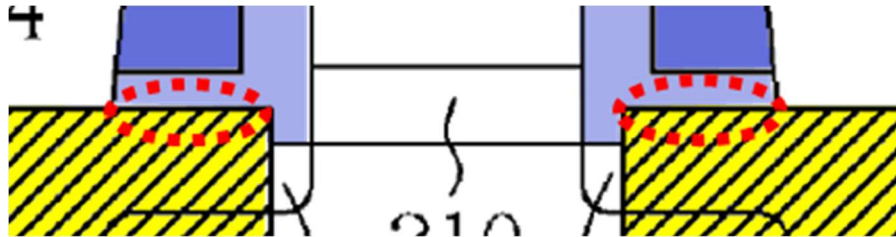


Wei, Fig. 2



Horstmann, Fig. 2

159. The '194 Patent spacers similarly “cover a portion of the first epitaxial layer 320 and a portion of the second epitaxial layer 328,” thus forming the same contact surface ('194 Patent at 6:51-53.)



'194 Patent, FIG. 14 (excerpted)

2. Dependent Claims

- a. **Claims 2/16: “The method of claim [1/10], further comprising a step of removing the [first] protective layer after forming the [first] epitaxial layer in the [first] recess.”**

160. As I explain in Section IX.A.1, Hoentschel262 discloses and renders obvious the methods of claims 1 and 10.

161. Hoentschel262 also discloses both “further comprising a step of removing the protective layer after forming the epitaxial layer in the recess,” as recited in claim 2, and “further comprising a step of removing the first protective layer after forming the first epitaxial layer in the first recess,” as recited in claim 16.

162. Hoentschel262 describes that “[a]fter the epitaxial growth process 213, the spacer layer 206A may be removed on the basis of any appropriate selective etch process.” (Hoentschel262 at 13:30-38, FIGS. 2d, 2e.) Hoentschel262 thus removes

the protective layer (disposable spacer layer 206A) after the epitaxial layer is formed in the recess.

b. Claims 3/12: “The method of claim [1/10], wherein the [first] protective layer comprises silicon nitride.”

163. As I explain in Section IX.A.1, Hoentschel262 discloses and renders obvious the methods of claims 1 and 10.

164. Hoentschel262 also discloses both “wherein the protective layer comprises silicon nitride,” as recited in claim 3, and “wherein the first protective layer comprises silicon nitride,” as recited in claim 12.

165. Hoentschel262 states the protective layer, spacer layer 206A, can be “comprised of *silicon nitride*.” (Hoentschel262 at 13:34-38 (emphasis added).) Similarly, spacer layer 106A from the first embodiment of Hoentschel262, a similar disposable layer establishing the offset for the recess region, “may be comprised of any appropriate material, *such as silicon nitride*, silicon dioxide and the like,” further disclosing and rendering obvious that the protective layer may comprise silicon nitride. (Hoentschel262 at 6:61-7:1 (emphasis added).) Regarding spacer layer 106A, Hoentschel262 states:

A thickness of the spacer layer 106A in combination with a thickness of the layer 107A may substantially determine a spacer width formed from the layers 106A, 107A during the etch process 108, which in turn may *substantially determine a resulting offset from the gate electrode 105 for a recess to be formed in the semiconductor layer 102* adjacent to respective channel regions 103. . . . [T]he

spacer layer 106A and the layer 107A may be formed with a thickness that is selected merely with respect to *a desired offset for recesses* to be formed in the layer 112 later on.

After the deposition of the layers 107A, 106A, the etch process 108 is performed on the basis of an appropriate etch chemistry to obtain a *substantially anisotropic* behavior with a high etch selectivity between the layers 106A, 107A. Respective selective etch recipes are well established in the art.

(Hoentschel262 at 7:52-8:6 (emphases added).) Likewise, regarding spacer layer 206A, Hoentschel262 states:

FIG.2c schematically illustrates the semiconductor device 200 after the completion of the above-described process sequence. Hence, the transistor 250p comprises respective spacer elements 206 having a width that substantially corresponds to the thickness 206B, while the second transistor 250n is still covered by the spacer layer 206A. Moreover, the device 200 is exposed to a further etch ambient 210 in order to form respective recesses or cavities 211p in the first transistor 250p. *As previously explained, an offset 211A of the recess 211p with respect to the gate electrode 205 and thus the channel region 203 is influenced by the spacer width 206B*, and may be substantially determined thereby if the etch process 210 is a *substantially anisotropic process*.

(Hoentschel262 at 12:64-13:9 (emphases added).) These two passages make clear that spacer 106A serves the same purpose as spacer 206A: defining the recess and providing the offset between epitaxial layer and the gate.

c. Claims 4/13: “The method of claim [3/10], wherein the [first] protective layer has a thickness of about 150 to 250 angstroms.”

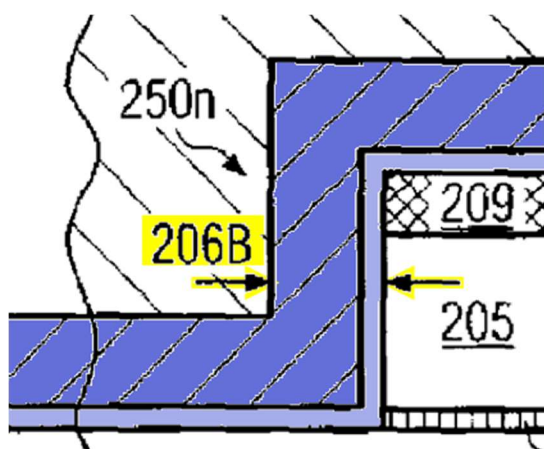
166. As I explain in Section IX.A.2.i, Hoentschel262 discloses and renders obvious the method of claim 3. Further, as I explain in Section IX.A.1, Hoentschel262 also discloses and renders obvious the method of claim 10.

167. Hoentschel262 also discloses “wherein the protective layer has a thickness of about 150 to 250 angstroms,” as recited in claim 4, and “wherein the first protective layer has a thickness of about 150 to 250 angstroms,” as recited in claim 13.

168. Hoentschel262 states the “thickness of the conformal spacer layer 206A may be selected to provide a desired offset for a recess to be formed adjacent to the gate electrode 205 of the first transistor 250p in a subsequent etch process,” and that “a thickness 206B of the layer stack 206A, 207A may range from several nanometers, for instance 3-50 nm, depending on the specific application.” (Hoentschel262 at 12:40-49.) A thickness of 3 to 50 nm equates to a thickness of 30 to 500 angstroms. Further, liner 207A is optional. If not used, thickness 206B would correspond to 206A alone. (Hoentschel262 at 12:33-35.)

169. I have been informed that when the prior art discloses a broader range of values (e.g., 30 to 500 angstroms) that encompasses a narrower range of claimed values (e.g., 150 to 250 angstroms), the broader prior art range discloses the narrower

claimed range so long as the narrower claimed range is not “critical” (meaning different in kind, not just degree) as compared to the other values in the broader disclosed range. Here, there have been no allegations of criticality, and I am not aware of any. The thickness of the protective layer sets the spacing between the gate electrode and epitaxial material, which is a design parameter that merely depends on device scaling. I am not aware of anything special, and certainly not critical, regarding a range of 150 to 250 angstroms. I therefore understand that Hoentschel262 discloses the claimed range (Ground 1A). For essentially the same reasons, a person of ordinary skill in the art would have found the claimed range obvious based on the disclosed thickness range. (Ground 1B). In fact, the claimed range is approximately in the middle of the disclosed range, and it is consistent with the spacing a person of ordinary skill in the art would have expected for contemporaneous devices (e.g., around the 65 nm node).



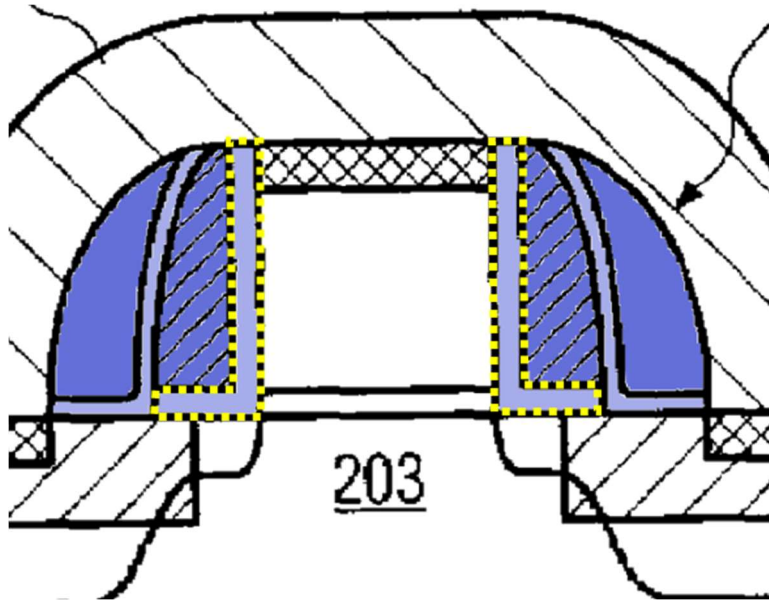
Hoentschel262, FIG. 2b (excerpt)

- d. **Claim 6/15: “The method of claim [1/10], wherein [the/each] spacer further comprises an offset spacer, positioned between [the/each] gate and [the/each] spacer.”**

170. As I explain in Section IX.A.1 Hoentschel262 discloses and renders obvious the methods of claims 1 and 10.

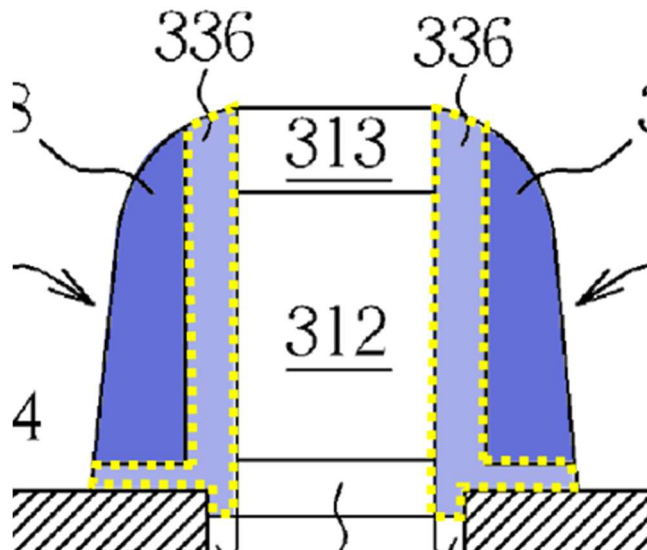
171. For the reasons I explain in section VII.C, I analyze claims 6 and 15 assuming that the claim can be satisfied if one layer (an “offset spacer”) of the claimed “spacer” lies between another layer of the claimed “spacer” and the claimed “gate.” Under such an interpretation, Hoentschel262 also discloses both “wherein the spacer further comprises an offset spacer, positioned between the gate and the spacer,” as recited in claim 6, and “wherein each spacer further comprises an offset spacer, positioned between each gate and each spacer,” as recited in claim 15.

172. Hoentschel262 discloses this by stating “[i]t should be appreciated that the spacer structures 216 may comprise *any appropriate number of individual spacer elements*, depending on the complexity of the required dopant profile of the regions 217.”) (Hoentschel262 at 14:52-56 (emphasis added).) At a minimum Hoentschel262 shows a spacer liner, highlighted by the dotted yellow line below:



Hoenstchel262, FIG. 2i (excerpted)

173. The '194 Patent shows a similar structure:



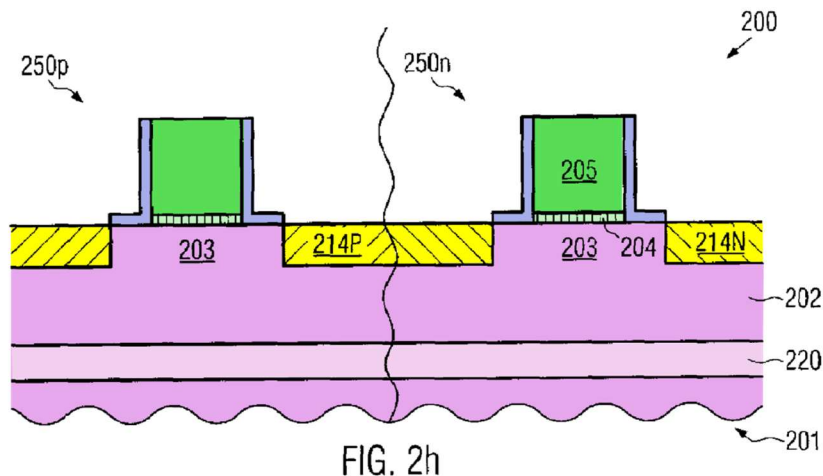
'194 Patent, FIG. 14 (excerpted)

- e. **Claim 7: “The method of claim 1, further comprising a step of forming a source/drain region within the semiconductor substrate adjacent to the gate after forming the spacer.”**

174. As I explain in Section IX.A.1, Hoentschel262 discloses and renders obvious the method of claim 1.

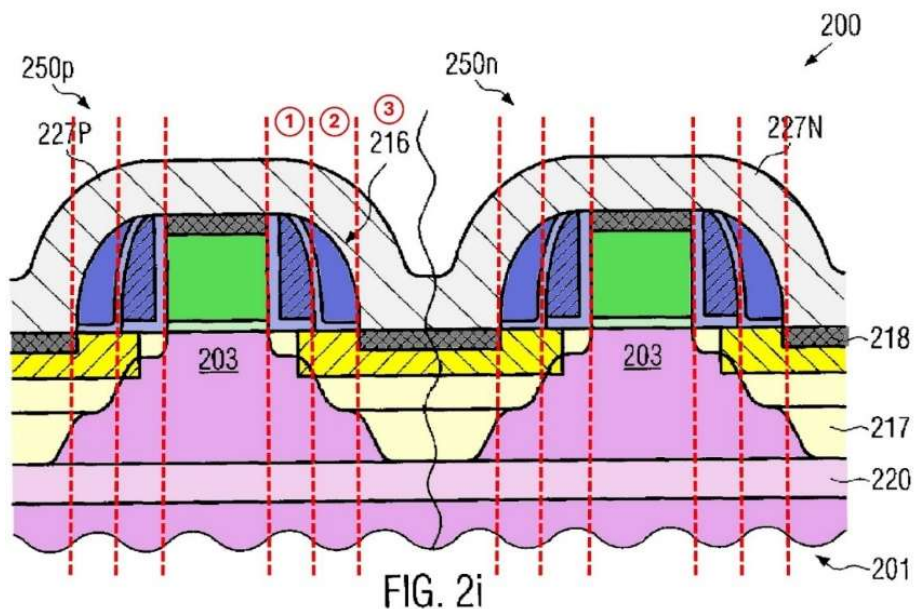
175. Hoentschel262 also discloses “a step of forming a source/drain region within the semiconductor substrate adjacent to the gate after forming the spacer,” as recited in claim 7.

176. In Hoentschel262 the source/drain regions are formed after the spacer, adjacent to the gate. (Hoentschel262 at 14:34-47.) Hoentschel262 states that “FIG. 2h schematically illustrates the device 200 in a further advanced manufacturing stage, in which the spacer layer 226A and the spacers 226 have been removed by an appropriate selective etch process.” (Hoentschel262 at 14:34-37.) At this point, the disposable, also referred to as sacrificial, spacers 206 and 226 have been removed.



**Hoenstchel262, FIG. 2h
(after the protective layer has been removed)**

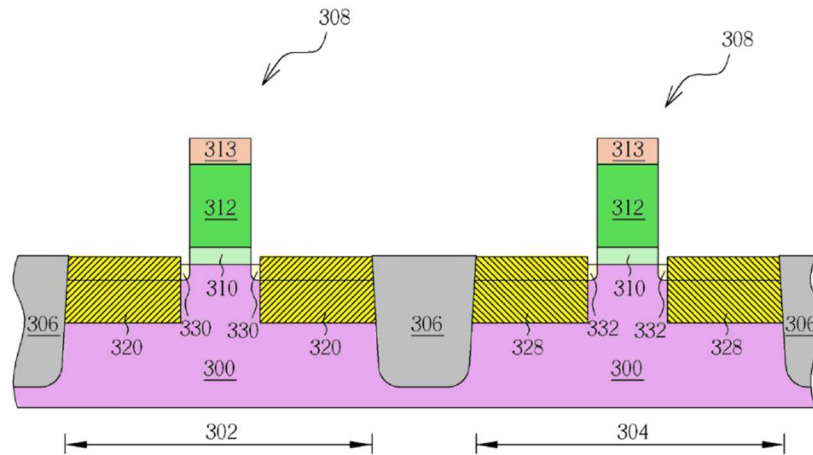
177. “Thereafter, the further processing may be continued by forming source and drain regions in the semiconductor layer 202 and within the strained semiconductor materials 214P, 214N on the basis of appropriate spacer techniques and implantation processes.” (Hoenstchel262 at 14:43-47.) For example, “FIG. 2i schematically illustrates the device 200 with a corresponding sidewall spacer structure 216 formed on the respective gate electrodes 205, which may have been used for defining respective lateral and vertical dopant profiles for respective drain and source regions 217. It should be appreciated that the spacer structures 216 may comprise any appropriate number of individual spacer elements, depending on the complexity of the required dopant profile of the regions 217.” (Hoenstchel262 at 14:48-56.) At this point, new (and permanent) spacers for establishing source/drain regions have been added, and they have been used to define source/drain profile 217, as shown below.



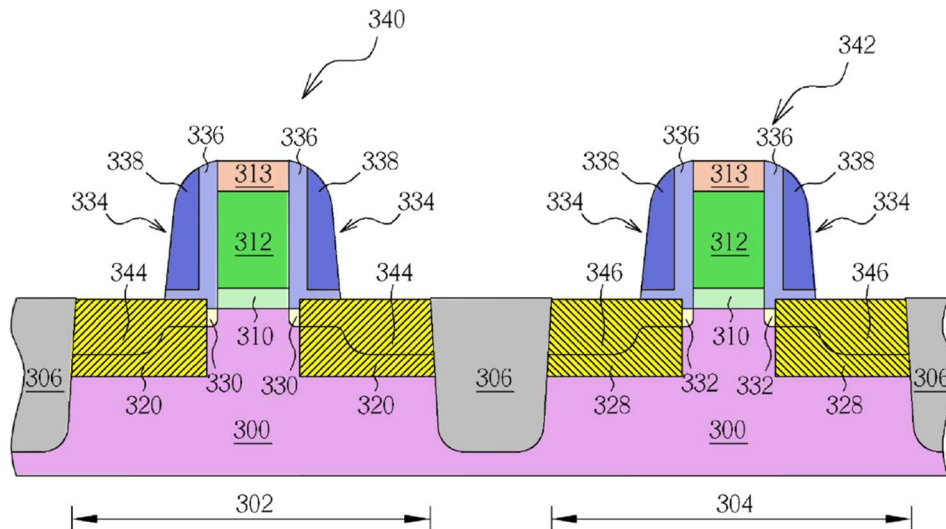
Hoentschel262, FIG. 2i (annotated)
(after the source/drain regions with profile 217 have been formed)

A person of ordinary skill in the art would have understood this means successive ion implantation steps take place in association with each constituent component of spacer structure 216. As I further describe in Section IX.B.3.c, a person of ordinary skill in the art would have understood Hoentschel262's source/drain profile 217 above is created by performing (1) an ion implantation masked by the gate to form a lightly doped extension (LDD) region, (2) an ion implantation masked by the inner liner/spacer pair to form a medium doped region, and (3) an ion implantation masked by the outer liner/spacer pair to form a heavily doped region after spacer structure 216 has been fully formed.

178. Similarly, the '194 Patent method uses new spacers formed on the sides of the gates to form the source/drain regions. ('194 Patent at 6:45-7:2.)



'194 Patent, FIG. 13
(after the protective layer has been removed)



'194 Patent, FIG. 14
(after forming source/drain regions 334)

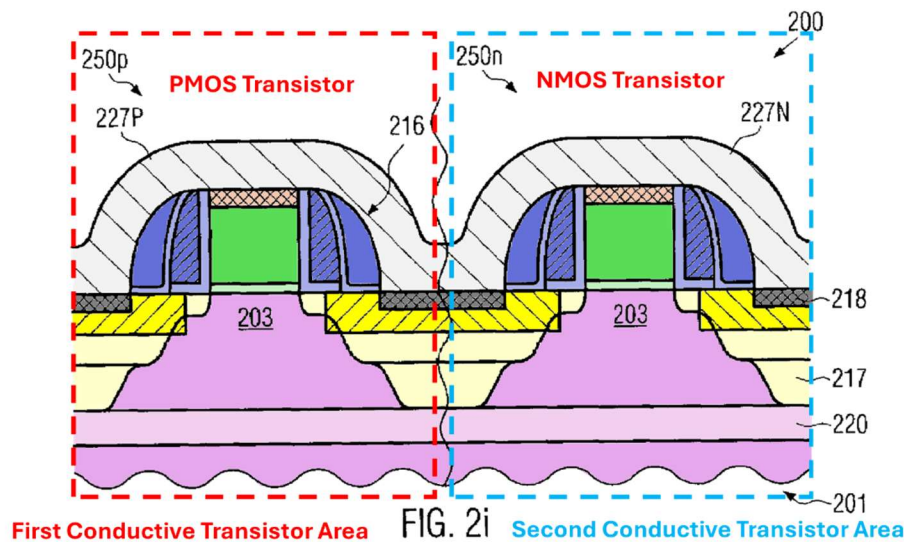
- f. **Claim 21: “The method of claim 10, wherein the first conductive transistors comprise PMOS transistors and the second conductive transistors comprise NMOS transistors.”**

179. As I explain in Section IX.A.1, Hoentschel262 discloses and renders obvious the method of claim 10.

180. Hoentschel262 also discloses “wherein the first conductive transistors comprise PMOS transistors and the second conductive transistors comprise NMOS transistors,” as recited in claim 21.

181. I understand that “the first conductive transistors” and “the second conductive transistors” lack an antecedent basis. For the purposes of this petition, I have been asked to assume they refer to transistors formed in the “first conductive transistor area” and “second conductive transistor area” recited in claim 10.

182. Hoentschel262 discloses that “transistor 250p may represent a P-channel transistor” (i.e., a PMOS transistor) and that “second transistor 250n represents an N-channel transistor” (i.e., an NMOS transistor). (Hoentschel262 at 13:26-30, 14:25-33, 14:64-15:5.)



Hoentschel262, FIG. 2i

183. The '194 Patent similarly discloses PMOS and NMOS transistors.

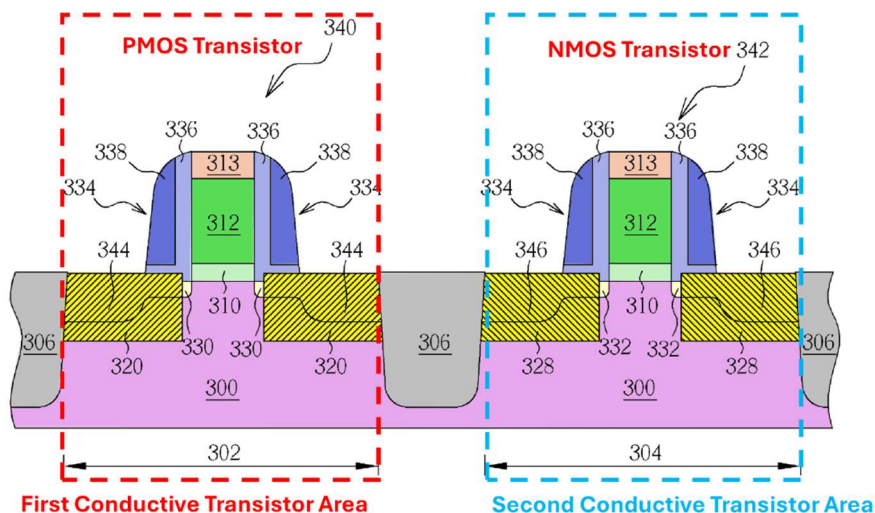


FIG. 14

'194 Patent, FIG. 14

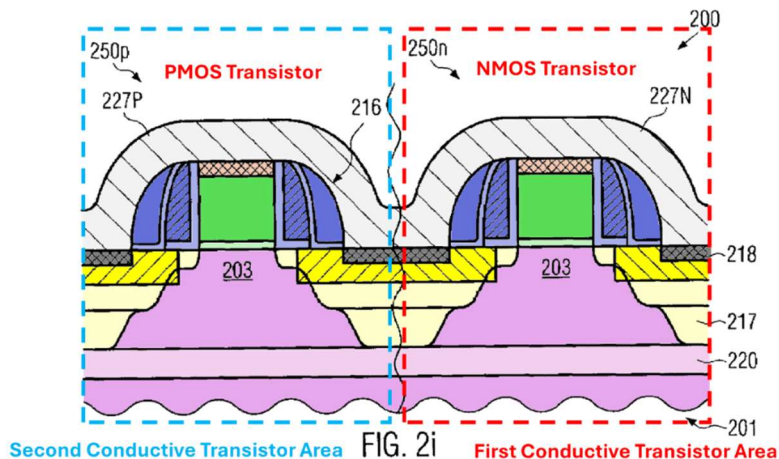
- g. **Claim 22: “The method of claim 10, wherein the first conductive transistors comprise NMOS transistors and the second conductive transistors comprise PMOS transistors.”**

184. As I explain in Section IX.A.1, Hoentschel262 discloses and renders obvious the method of claim 10.

185. I understand that “the first conductive transistors” and “the second conductive transistors” lack an antecedent basis. For the purposes of this petition, I have been asked to assume they refer to transistors formed in the “first conductive transistor area” and “second conductive transistor area” recited in claim 10.

186. As I discuss in Section IX.A.1.b, transistor 250n may be identified as the “first conductive transistor,” and transistor 250p may be identified as the “second conductive transistor.” Hoentschel262’s “transistor 250n represents an N-channel

transistor” (NMOS transistor), and “transistor 250p may represent a P-channel transistor” (PMOS transistor). (Hoentschel262 at 13:26-30, 14:25-33, 14:64-15:5.)



Hoentschel262, FIG. 2i

B. Ground 1B (Cont'd): Hoentschel262 Alone Renders Obvious Claims 5, 8-9, 11, 14, and 17-20.

187. Hoentschel262 teaches, suggests, and/or renders obvious all the elements of claims 5, 8-9, 11, 14, and 17-20 of the '194 Patent.

188. For the same reasons stated in my analysis below, I conclude that Hoentschel262 renders claims 5, 8-9, 11, 14, and 17-20 obvious because the differences between claims 5, 8-9, 11, 14, and 17-20 and Hoentschel262 are such that claims 5, 8-9, 11, 14, and 17-20 would have been obvious to a person of ordinary skill in the art.

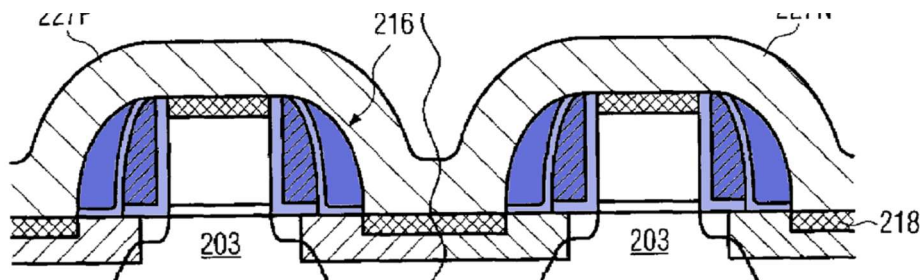
1. Claim 5/14: “The method of claim [1/10], wherein [the/each] spacer further comprises an oxide liner and a nitride spacer.”

189. As I explain in Section IX.A.1, Hoentschel262 discloses and renders obvious the methods of claims 1 and 10.

190. Hoentschel262 also renders obvious “wherein the spacer further comprises an oxide liner and a nitride spacer,” as recited in claim 5, and “wherein each spacer further comprises an oxide liner and a nitride spacer,” as recited in claim 14.

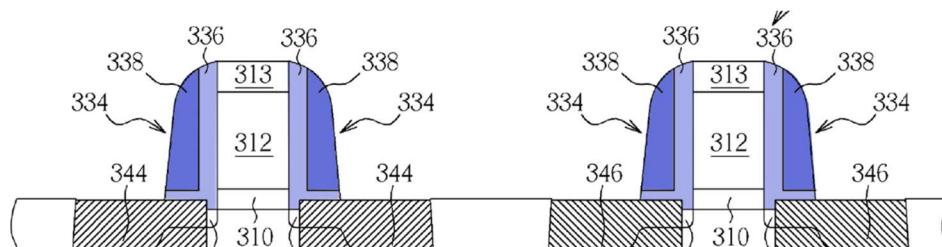
191. Hoentschel262 states that “the spacer structures 216 may comprise any appropriate number of individual spacer elements, depending on the complexity of the required dopant profile of the regions 217.” (Hoentschel262 at 14:52-56.)

FIG. 2i depicts four individual spacer elements. (Hoentschel262 at 14:49-56.)



Hoentschel262, FIG. 2i (excerpt)

192. Similarly, the '194 Patent shows spacers with two individual spacer elements—an oxide liner 336 and a nitride spacer 338. ('194 Patent at 14:45-48.)

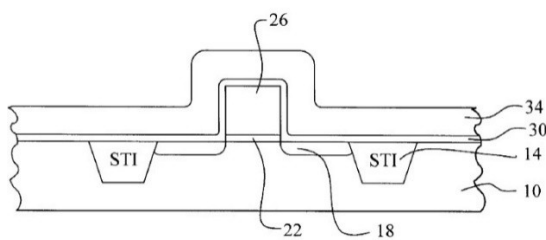


'194 Patent, FIG. 14 (excerpt)

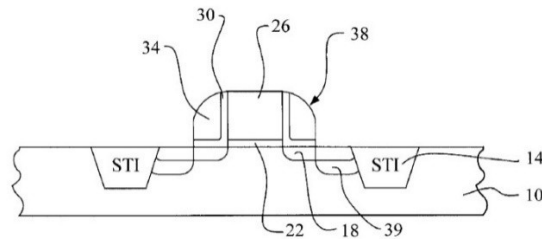
193. A person of ordinary skill in the art would have found it obvious to use an oxide liner and a nitride spacer when implementing Hoentschel262's spacer structure 216, because this pairing was extremely common for spacers, sacrificial or otherwise. Indeed, when describing its first embodiment, Hoentschel262 states "spacer layer 106A may be comprised of any appropriate material, such as silicon nitride, silicon dioxide and the like, while the liner 107A may be provided in the form of any appropriate material having the required etch selectivity to the material of the layer 106A. For example, silicon dioxide may be used for the liner 107A when the spacer layer 106A is comprised of silicon nitride." (Hoenstchel262 at 6:61-7:1; *see also* Hoentschel262 at 8:1-14.) Hoentschel262 also frequently refers back to the first embodiment's descriptions for details regarding how to implement features of other embodiments. (Hoenstchel262 at 10:39-45; 10:55-62; 12:29-31; 13:26-28; 13:47-51; 15:56-59; 17:20-23.) Such disclosures (e.g., explaining that spacer structure 116 in Fig. 1e is a two-layer structure and that the same would apply for spacer structure 216 in Fig. 2) confirm the obviousness of using an analogous approach to forming spacer structures 216.

194. Additionally, a person of ordinary skill in the art would have been very familiar with using of an oxide liner and nitride spacer to make a composition spacer structure. This approach was quite common in the art, and it is consistent with Hoentschel262's FIG. 2i. A person of ordinary skill in the art would have understood that an oxide liner helps adhesion of the spacer, protects the semiconductor surfaces underneath from defects, and assists with spacer formation.

195. Gupta, for instance, discloses a silicon nitride layer 34 deposited overlying an oxide liner layer 30. (Gupta at 1:41-42.) Gutpa explains that "oxide liner layer 30 . . . improves the adhesion of the silicon nitride." (Gupta at 1:39-41.) Then, "the silicon nitride layer 34 and the oxide liner layer 30 are anisotropically etched, as conventional in the art, to form sidewall spacers adjacent to the polysilicon gates" as shown in the transition from FIG. 1 to FIG. 2 below. (Gupta at 1:43-47.)

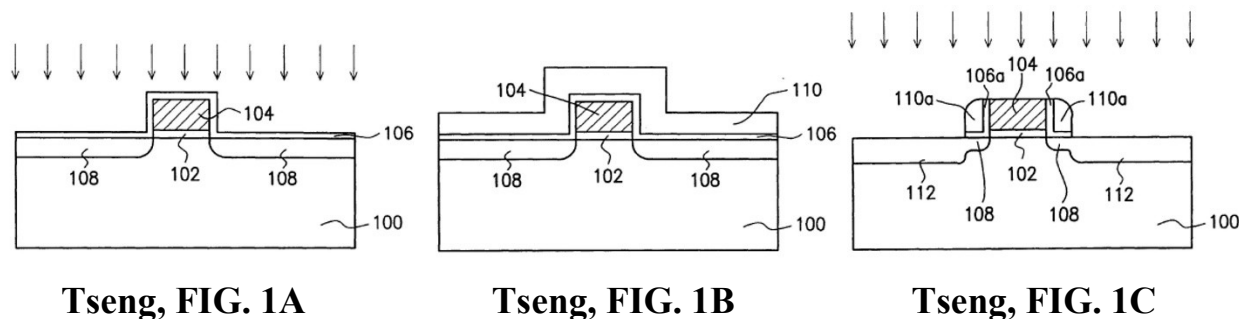


Gupta, FIG. 1



Gupta, FIG. 2

196. Tseng similarly refers to such an approach "conventional" when "forming a MOSFET device," as in FIGS. 1A to 1C below. (Tseng at 1:50-65.)



197. Plummer also explains, for example, that direct contact between silicon nitride and silicon “can lead to defect generation” that that “the major purpose of [an] SiO₂ layer under the S₃N₄ is to help relieve this.” (Plummer at 54.) Studying such effects in sidewall spacers, Damiano similarly notes that “the presence of a liner under the gate spacer nitride” influences dislocations in the source/drain regions. (Damiano at 212.) Damiano explains: “An oxide liner under the nitride spacer is known to reduce the stress from the spacer on the underlying silicon, which could also prevent formation of trench dislocations.” (Damiano at 212.) Indeed, Damiano found that an oxide liner “reduced the incidence of dislocations by as much as 70%.” (Damiano at 212.) Koldiaev likewise explains that an oxide liner isolates the silicon nitride spacer layer from the substrate surface to prevent such defects. (Koldiaev ¶[0031], FIG. 3.) This was well known in the art and why such an approach was considered conventional.

198. The oxide liner also beneficially provides an etch stop when etching the thicker silicon nitride spacer layer to form the spacer. Hoentschel²⁶² itself notes this benefit when establishing such a spacer structure. (Hoentschel²⁶² at 12:53-56.)

199. A person of ordinary skill in the art also would have understood that a composite spacer comprising an oxide liner and nitride spacer was commonly used to perform source/drain engineering, including to form LDD regions and deeper, more heavily doped source/drain regions. (*See* Gupta at 1:27-47, FIG. 2 (above); Tseng at 1:53-65, FIG. 1C (above); Koldiaev ¶[0029].) Such source/drain engineering is precisely why Hoentschel²⁶² discloses spacer structures 216: “for defining respective lateral and vertical dopant profiles for respective drain and source regions 217.” (Hoentschel²⁶² at 14:48-52.) Moreover, “[i]t should be appreciated that the spacer structures 216 may comprise any appropriate number of individual spacer elements, depending on the complexity of the required dopant profile of the regions 217.” (Hoentschel²⁶² at 14:52-56.)

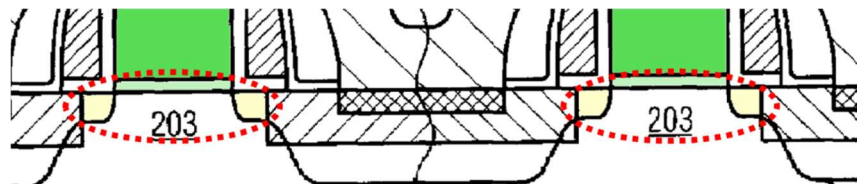
200. A person of ordinary skill in the art would have found it obvious to use the same materials (an oxide liner and nitride spacer) for the same reasons (to perform source/drain engineering with a structure that improves spacer adhesion, protects the semiconductor surfaces, and assists with spacer formation) when forming the constituent layers of spacer structure 216 in FIG. 2i. Indeed, this is consistent with the appearance of spacer structures 216 in FIG. 2i, which resembles two composite spacers, each with a liner layer and a spacer layer. (*See also* Wei at Fig. 2 (showing such an embodiment created by the Hoentschel²⁶² inventors); Horstmann at Fig. 2 (same).)

2. Claims 8/11: “The method of claim [1/10], further comprising a step of forming a [first ion] lightly doped region within the semiconductor substrate adjacent to the gate [in the first conductive transistor area].”

201. As I explain in Section IX.A.1, Hoentschel262 discloses and renders obvious the methods of claims 1 and 10.

202. Hoentschel262 also renders obvious both “a step of forming a lightly doped region within the semiconductor substrate adjacent to the gate,” as recited in claim 8, and “a step of forming a first ion lightly doped region within the semiconductor substrate adjacent to the gate in the first conductive transistor area,” as recited in claim 11.

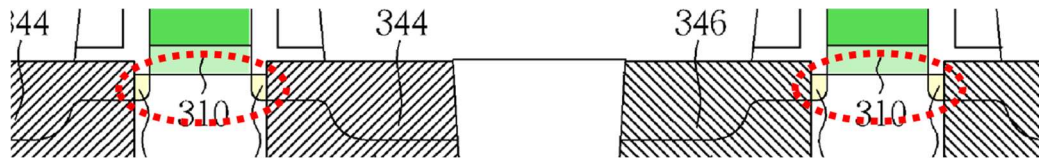
203. Hoentschel262 shows LDD or extension structures [light yellow, circled in red] next to the gate in FIG. 2i. (Hoentschel262 at 14:43-56.) In the context of its first embodiment, Hoentschel262 states “respective *extension regions*, if required, may be formed after the removal of the spacers 106” (analogous to 206). (Hoentschel262 at 10:25-33 (emphasis added).) Such extension regions appear in FIG. 1f and resemble the regions indicated below in FIG. 2i. A person of ordinary skill in the art would have understood the structures in FIG. 2i below are also extension regions.



Hoentschel262, FIG. 2i (excerpted)

204. A person of ordinary skill in the art would have expected, and certainly found it obvious, that the extension regions circled above are lightly doped regions (LDD regions). LDD regions were often considered synonymous with source/drain “extension regions,” as Hoentschel262 calls them. Plummer’s textbook, for instance, includes a section titled, “Tip or Extension (LDD) Formation.” (Plummer at 76-80.) Plummer explains: “The LDD structure also provides these shallow junctions which in this context are often called the ‘tip’ or ‘extension’ regions since they must be combined with deeper source and drain junctions away from the channel in order to make reliable contacts to the device.” (Plummer at 78.) Moreover, they appear as drawn in FIG. 2i. Such LDD structures were a textbook aspect of MOSFET fabrication to mitigate short-channel effects. (*See* Section VI.C above; Plummer at 76-82; Quirk at 211-13; Wolf3 at 595-98.) A person of ordinary skill in the art thus would have found it obvious for the source/drain extension regions identified in FIG. 2i above to be ion implanted LDD regions.

205. The ’194 Patent includes similar structures. (’194 Patent at 6:35-51).



'194 Patent, FIG. 14 (excerpted)

3. Claim 9:

a. 9[pre] “The method of claim 1, further comprising:”

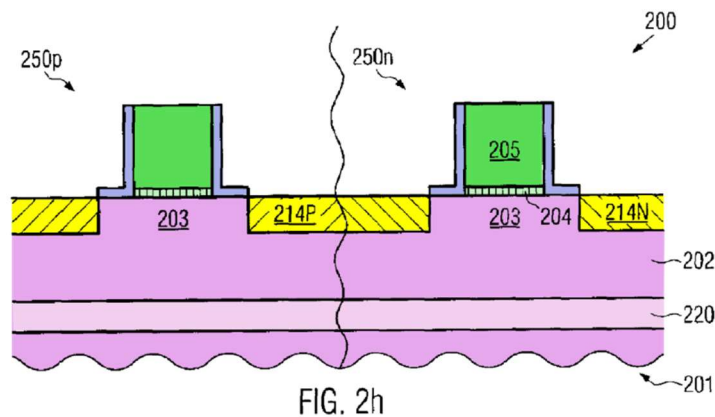
206. As I explain in Section IX.A.1, Hoentschel262 discloses and renders obvious the method of claim 1.

b. 9[a] “forming a lightly doped region in the semiconductor substrate adjacent to the gate after forming the epitaxial layer;”

207. As I explain in Section IX.B.2, Hoentschel262 renders obvious the formation of lightly doped regions adjacent to the gate, as described for claim 8.

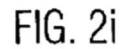
208. Hoentschel262 also renders obvious “forming a lightly doped region in the semiconductor substrate adjacent to the gate after forming the epitaxial layer,” as recited in claim element 9[a].

209. Hoentschel262’s LDD extensions are formed after removing both protective layer 206A, after epitaxial layer 214p is formed. (Hoentschel262 at 14:34-47.) FIG. 2h below shows the structure after epitaxy is complete and the protective layer has been removed. (Hoentschel262 at 14:34-43.). Note, the light blue L shaped structure is the optional disposable optional liner layer 207A, not the spacer 216.



Hoentschel262, FIG. 2h
(epitaxy complete and protective layer removed)

210. FIG. 2i below shows the result of “further processing” conducted “thereafter,” which forms the source and drain regions with “lateral and vertical dopant profiles for respective drain and source regions 217,” including the LDD source/drain extensions. (Hoentschel262 at 14:43-56; *see also* Section IX.B.2 above (describing the LDD extensions in Hoentschel262).) As FIG. 2h above indicates, epitaxial regions 214p and 214n are present, but the LDD regions (part of source/drain profile 217) are not. In FIG. 2i below, the LDD regions are formed. Thus, a person of ordinary skill in the art would have understood that the LDD regions are formed *after* the epitaxial layers.

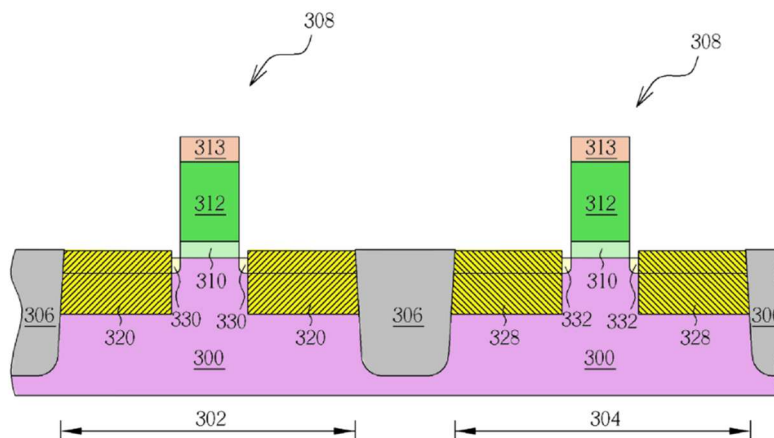


Hoenstchel262, FIG. 2i

211. The '194 Patent describes a similar process. ('194 Patent at 6:13-44)



(before LDD, epitaxy complete and protective layer removed)



**'194 Patent, FIG. 13
(after LDD)**

- c. **9[b] “forming the spacer on the sidewall of the gate and on the portion of the epitaxial layer after forming the lightly doped region; and”**

212. As I explain in Section IX.A.1.g, Hoentschel262 discloses and renders obvious the formation of spacers on the sidewall of the gate and on the portion of the epitaxial layer, as described for claim element 1[f].

213. Hoentschel262 also renders obvious “forming the spacer on the sidewall of the gate and on the portion of the epitaxial layer after forming the lightly doped region,” as recited in claim element 9[b].

214. Hoentschel262’s FIG. 2i “schematically illustrates the device 200 with a corresponding sidewall spacer structure 216 formed on the respective gate electrodes 205, which may have been used for defining respective lateral and vertical dopant profiles for respective drain and source regions 217.” (Hoentschel262 at 14:48-56.) “[T]he spacer structures 216 may comprise any appropriate number of

individual spacer elements, depending on the complexity of the required dopant profile of the regions 217.” (Hoenstchel262 at 14:52-56.)

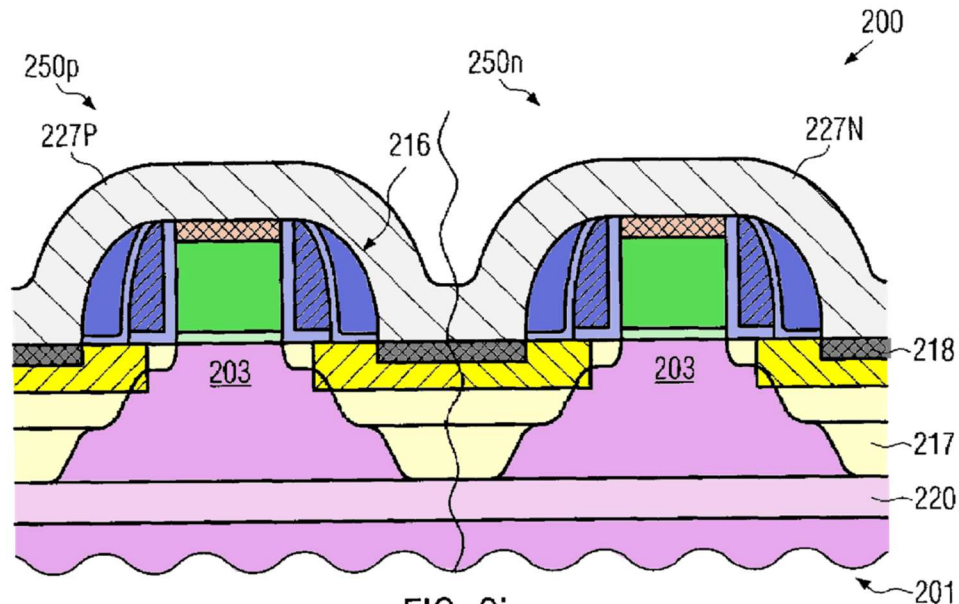
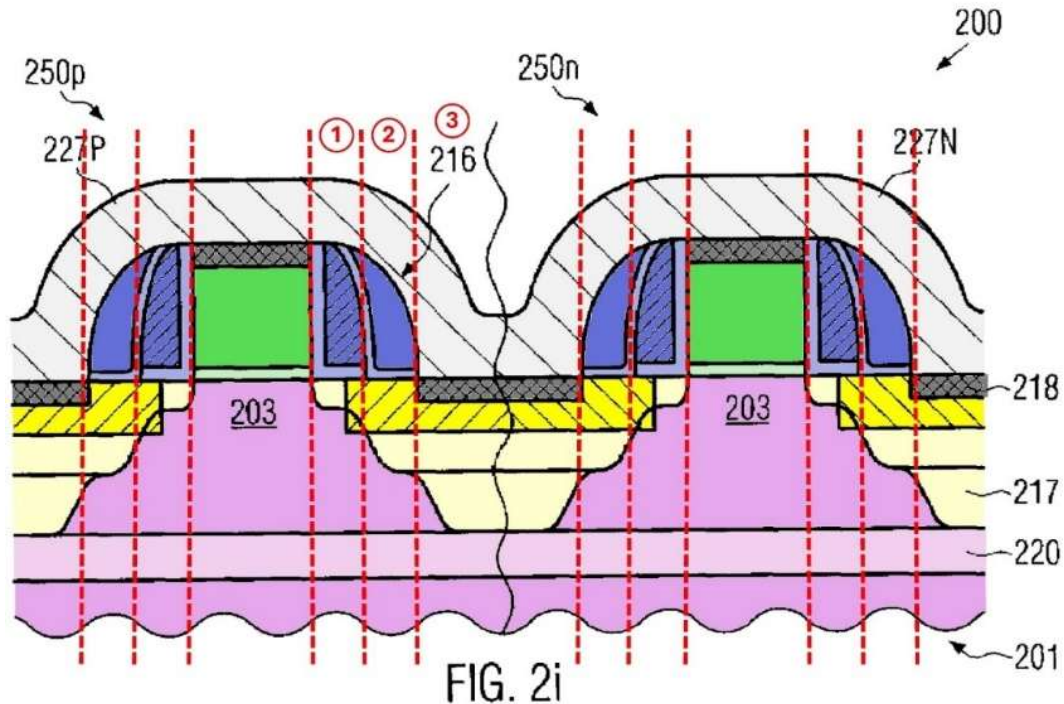


FIG. 2i

Hoenstchel262, FIG. 2i

215. A person of ordinary skill in the art would have understood that FIG. 2i illustrates a dopant profile 217 with three different regions: (1) a lightly doped (LDD) region immediately adjacent to the gate, which is defined by the gate, (2) a medium doped region just outside of the inner spacer (i.e., the inner liner/spacer pair), which is defined by the inner spacer, and (3) a heavily doped region just outside of the outer spacer (i.e., the outer liner/spacer pair), which is defined by the outer spacer. I have added the numbers and dotted red lines below to illustrate this. Because the LDD/extension regions otherwise would be masked by spacer structure

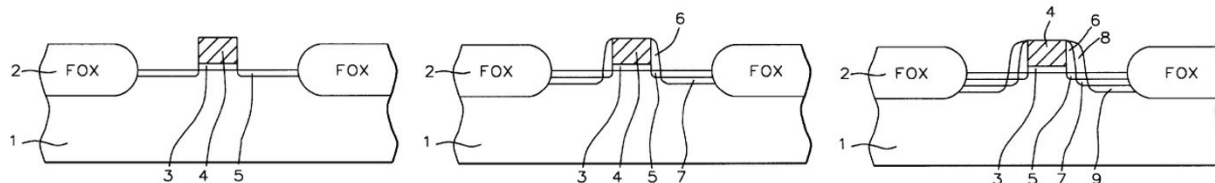
216, a person of ordinary skill in the art would have found it obvious to form the LDD/extension regions *before* spacer structure 216.



Hoentschel262, FIG. 2i (annotated)

216. Such an approach was well known. Referring to FIG. 1 below, for instance, Hua explains that “[a] lightly doped source and drain region, 5, is . . . formed in semiconductor substrate, 1, via ion implantation.” (Hua at 3:34-39.) Then, a spacer 6 is formed, and “a medium doped source and drain region, 7, is created . . . via ion implantation,” as FIG. 2 shows below. (Hua at 4:5-10.) “This medium doped source and drain region will not be as heavily doped as a subsequent source and drain region, needed for contact purposes,” which means “less lateral diffusion will occur, . . . thus reducing the risk of hot electron carrier injection.” (Hua at 4:10-16.)

It also “reduces the resistance of the lightly doped source and drain region, 5, . . . thus improving performance.” (Hua at 4:16-20.) Finally, “FIG. 3 shows the creation of a second insulator spacer, 8,” which is used to define “the heavily doped source and drain region, 9, needed for low resistance contacts.” (Hua at 4:21-37.)



Hua, FIG. 1

Hua, FIG. 2

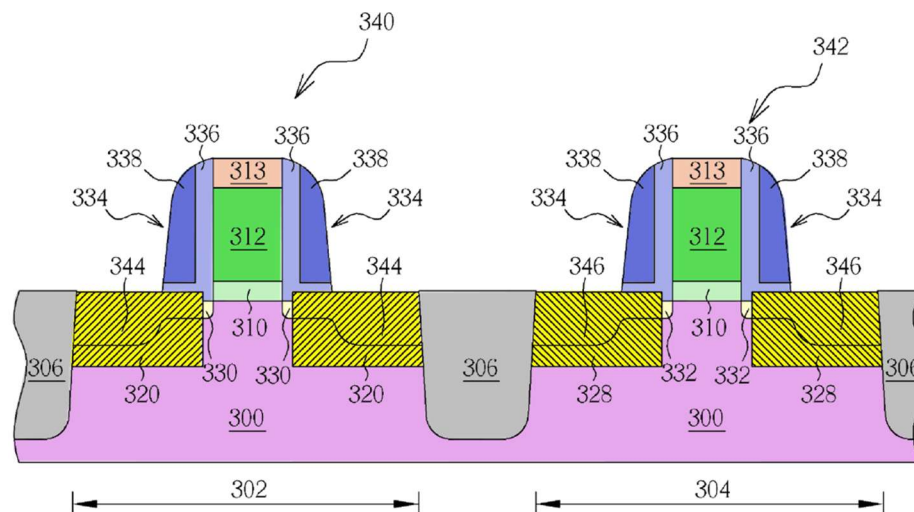
Hua, FIG. 3

217. A person of ordinary skill in the art would have understood that LDD and heavily doped regions were standard in MOSFET processing and that a medium doped region is optional. A person of ordinary skill in the art would have understood Hoentschel262’s FIG. 2i illustrates the presence of a medium doped region, but Hoentschel262 alternatively explains that spacer structure 216 may use “any appropriate number of individual spacer elements, depending on the complexity of the required dopant profile of the regions 217.” (Hoentschel262 at 14:43-56.)

218. A person of ordinary skill in the art would have understood that the lightly doped region helps mitigate punchthrough and hot carrier effects (excessively energetic carriers that can degrade performance). (See Section VI.C above; Wolf3 at 238; Quirk at 211; Plummer at 76-77.) A person of ordinary skill in the art would have understood that the medium doped region is a bridge between LDD and heavily

doped regions that further helps reduce such effects. (Hua at 4:10-16.) And a person of ordinary skill in the art would have understood the heavily doped region is needed to reduce source/drain contact resistance. (Hua at 4:29-31.)

219. Similarly, the '194 Patent includes spacers formed on the gate. ('194 Patent at 6:45-46.)



'194 Patent, FIG. 14

d. 9[c] “forming a source/drain region in the semiconductor substrate adjacent to the spacer.”

220. As I explain in Section IX.A.2.e, Hoentschel262 discloses and renders obvious the formation of a source/drain region adjacent to the spacer, as described for claim 7. Hoentschel262 therefor also renders obvious “forming a source/drain region in the semiconductor substrate adjacent to the spacer,” as recited in claim element 9[c], for the same reasons.

4. Claim 17

- a. 17[pre] “The method of claim 16, after removing the first protective layer, the method further comprising:”**

221. As I explain in Section IX.A.2.a., Hoentschel262 discloses and renders obvious the method of claim 16.

222. Further, in Hoentschel262, the first protective layer (206A) is removed in the transition from FIG. 2d to FIG. 2e. (Hoenstchel262 at 13:30-41.) The steps described and pictured in FIG. 2e through FIG. 2i take place thereafter—i.e., after layer 206A has been removed. (Hoenstchel262 at 13:39-15:38, FIGS. 2e-FIG. 2i).

- b. 17[a] “forming a second protective layer on the semiconductor substrate, and the second protective layer covering the surface of each gate;”**

223. Hoentschel262 renders obvious “forming a second protective layer on the semiconductor substrate, and the second protective layer covering the surface of each gate,” as recited in claim element 17[a].

224. Hoentschel262 explains that, “after the completion” of removing the first protective later, the formation of “a further spacer layer 226A” covering the surface of each gate. (Hoenstchel262 at 13:30-47.) This may optionally be formed on liner 207A as “may still be present and may be used for etching the spacer layer 226A,” or “a corresponding liner (not shown) may be formed on the first and second transistors 250p, 250n prior to the deposition of the spacer layer 226A” in which

case both gates may “be covered by the newly formed liner material.”
(Hoenstchel262 at 13:60-14:4.)

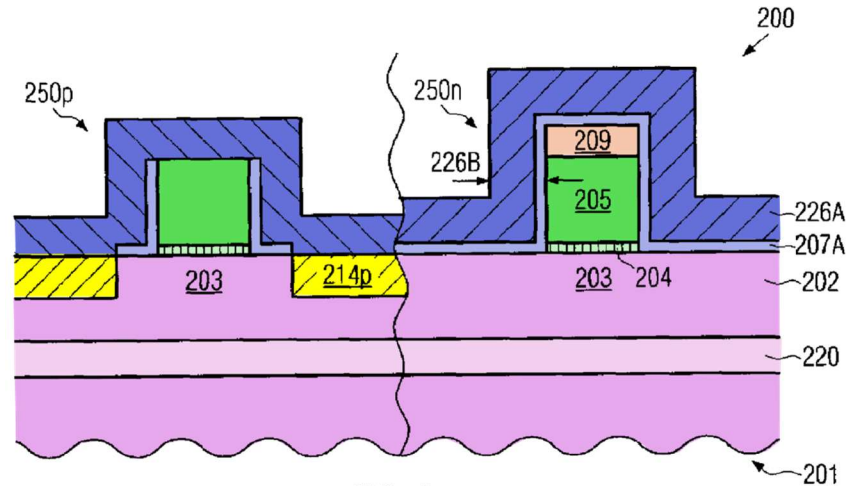
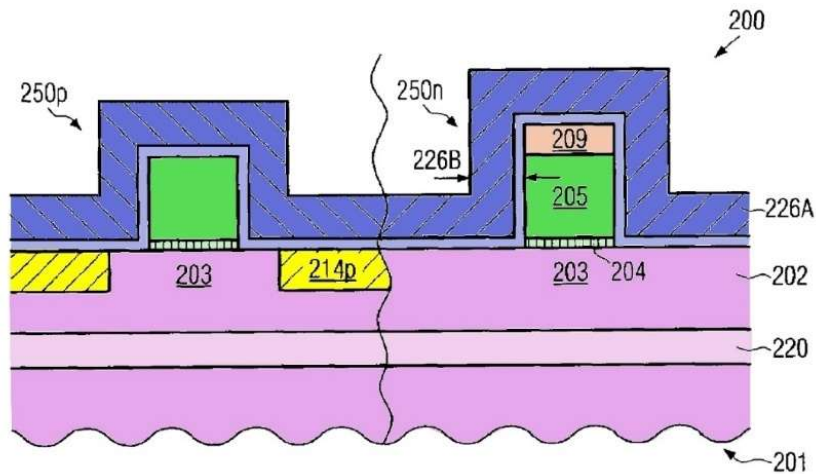


FIG. 2e

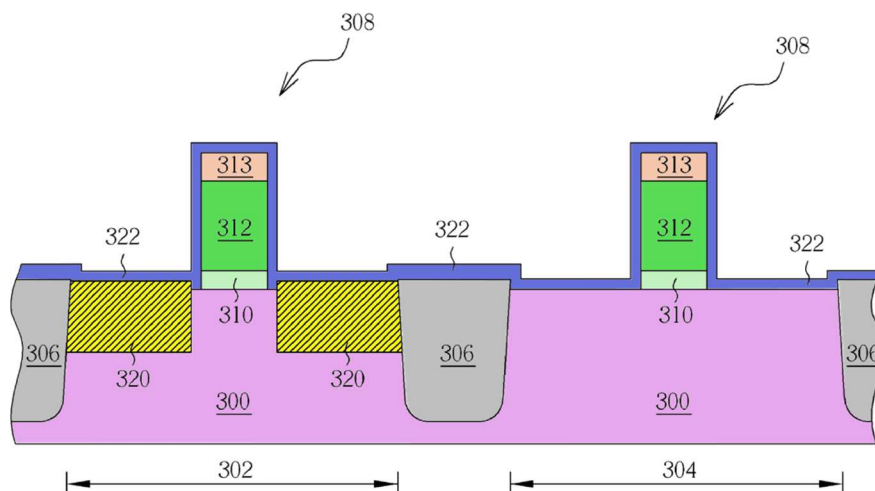
Hoenstchel262, FIG. 2e

225. In FIG. 2e above, optional liner 207A remains. Hoentschel262’s alternative embodiment, however, includes removal (or omission) of that layer and deposition of another optional liner (not shown) underneath spacer layer 226A. (Hoentschel262 at 13:60-14:4.) A person of ordinary skill in the art would have understood that such a structure would resemble the alternative FIG. 2e below, as the L-shaped spacers on PMOS transistor 214p would have first been removed before blanket depositing another liner layer. In either embodiment (above or below), a second protective layer (226A) is blanket formed on the SOI substrate and covers the surface of each gate.



Petitioner's Alternative FIG. 2e (see Hoentschel262 at 13:60-14:4)

226. Similarly, the '194 Patent shows the deposition of a second protective layer. ('194 Patent at 5:48-50.)



'194 Patent, FIG. 10

c. 17[b] “forming at least a second recess within the semiconductor substrate adjacent to the gate in the second conductive transistor area;”

227. Hoentschel262 renders obvious “forming at least a second recess within the semiconductor substrate adjacent to the gate in the second conductive transistor area,” as recited in claim element 17[b].

228. After removing the first protective layer (206A) and forming the second protective layer (226A), Hoentschel262 states: “Thereafter, a further etch process may be performed to *form a respective recess or cavity 211n*, as indicated in dashed lines,” and the “respective size and offset of the recesses 211n is influenced by the spacer width 226B.” (Hoenstchel262 at 14:7-13 (emphasis added).)

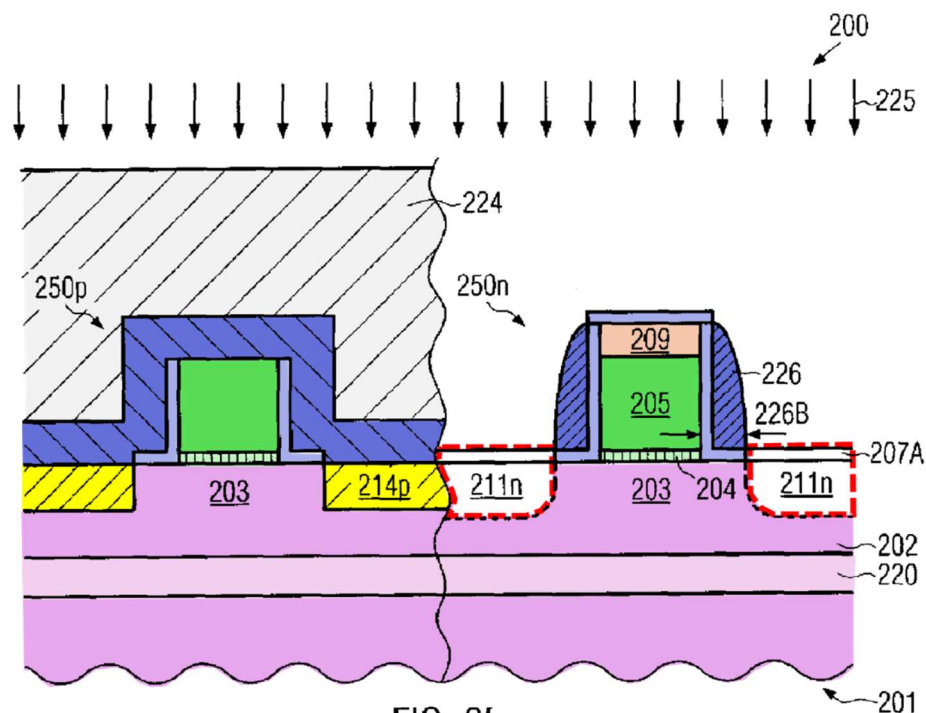
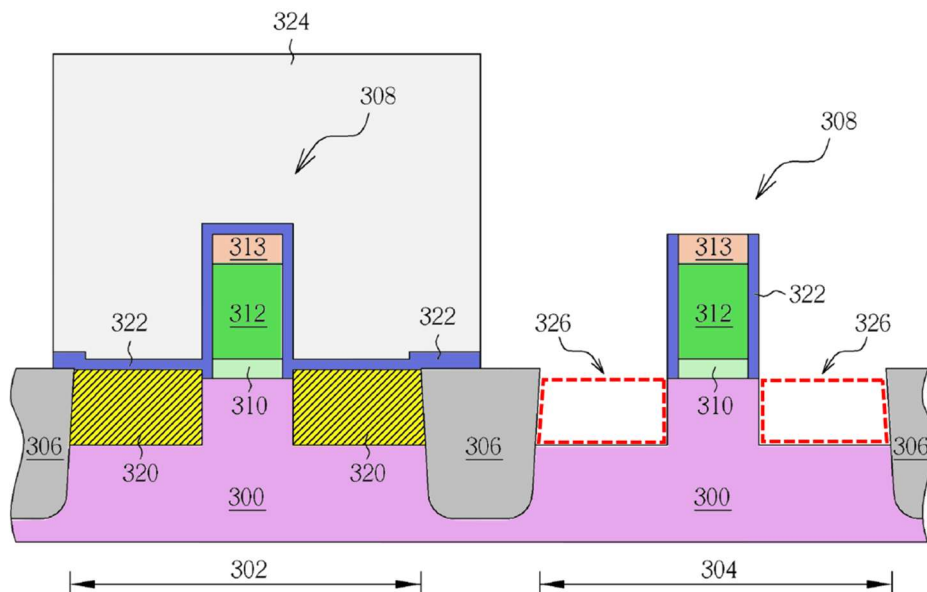


FIG. 2f

Hoenstchel262, FIG. 2f

229. Similarly, the '194 Patent method describes etching recesses 326. ('194 Patent at 5:62-64.)



d. 17[c] “forming a second epitaxial layer in the second recess;”

230. Hoentschel262 renders obvious “forming a second epitaxial layer in the second recess,” as recited in claim element 17[c].

231. Hoentschel262’s fabrication method includes forming strained semiconductor material 214n in recess 211n after spacer layer 206A has been removed: “FIG. 2g schematically illustrates the device 200 in a further advanced manufacturing stage, wherein the device 200, after a corresponding cavity etch process for actually forming the recesses 211n, is subjected to a further selective epitaxial growth process 215 for forming a strained semiconductor

material 214N adjacent to the respective channel region 203 of the second transistor 250n.” (Hoenstchel262 at 14:18-27.) “With respect to the epitaxial growth process 215, the same criteria apply as previously explained” for growing epitaxial material 214p, except that semiconductor material 214n “may comprise a silicon/carbon mixture for imposing a tensile strain to the channel region 203 of the second transistor 250n.” (Hoenstchel262 at 14:25-33.)

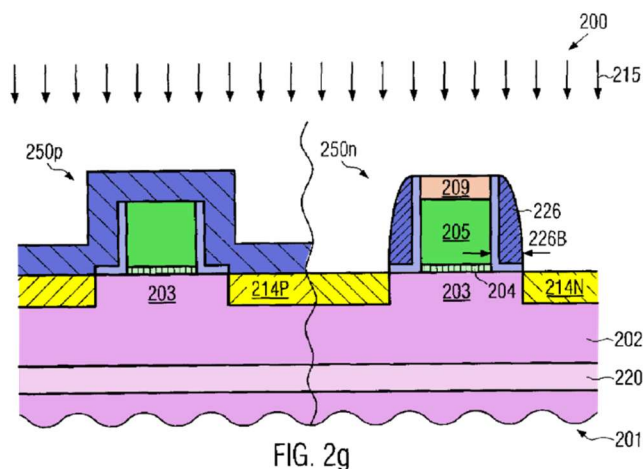
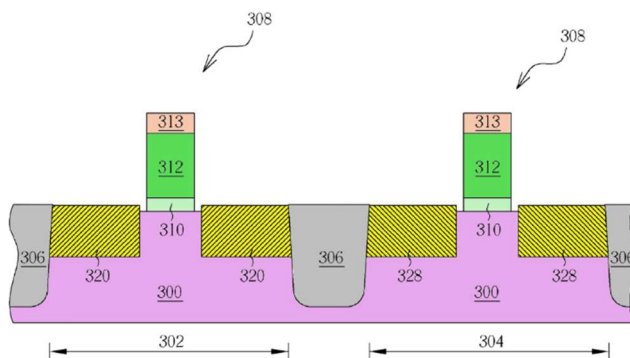


FIG. 2g

Hoenstchel262, FIG. 2g

232. The '194 Patent similarly grows second epitaxial layers in the second region. ('194 Patent at 6:13-22.)

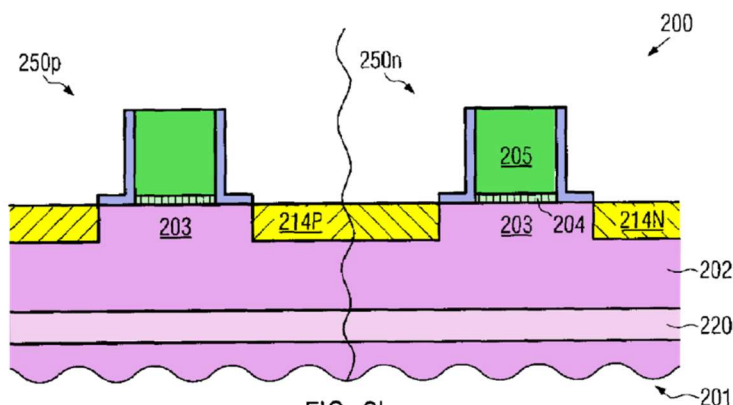


'194 Patent, FIG. 12

e. 17[d] “removing the second protective layer; and”

233. Hoentschel262 renders obvious “removing the second protective layer,” as recited in claim element 17[d].

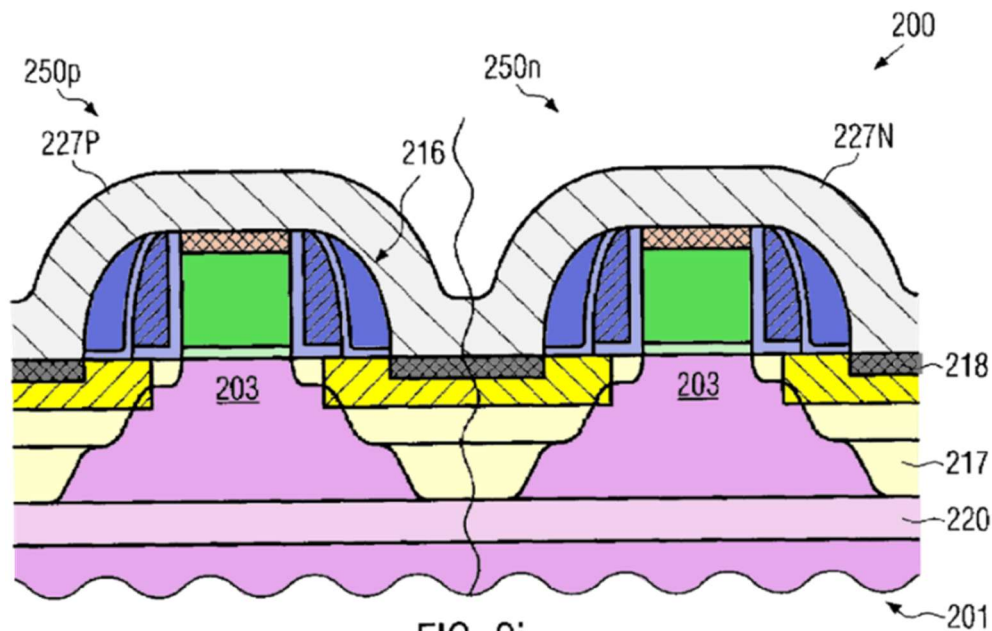
234. Hoentschel262 explains that spacer layer 226A is removed after spacer layer 206A has been removed. According to Hoentschel262, FIG. 2h below “schematically illustrates the device 200 in a further advanced manufacturing stage, in which the spacer layer 226A and the spacers 226 have been removed by an appropriate selective etch process.” (Hoentschel262 at 14:34-40.)



Hoentschel262, FIG. 2h

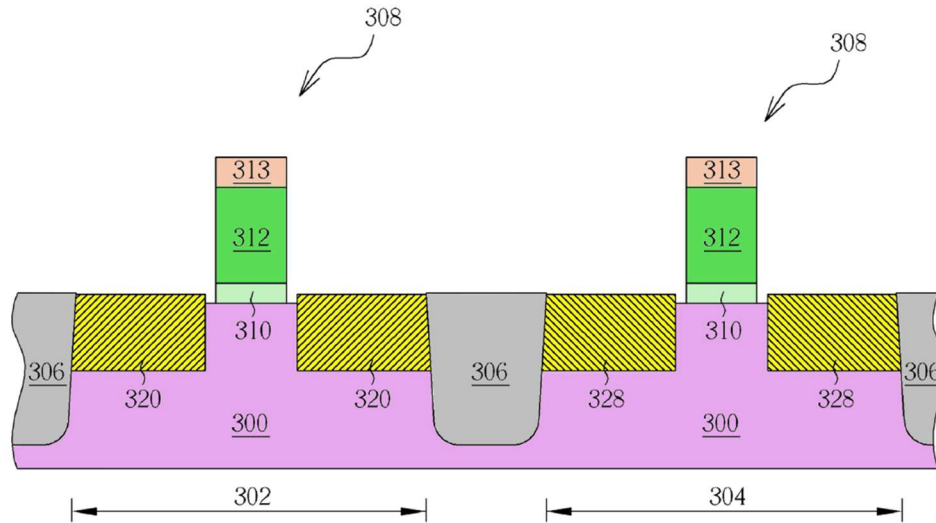
235. Additionally, a person of ordinary skill in the art would have understood that, in FIG. 2i below, the innermost L-shaped sidewall spacer layers are not the same as the L-shaped liner layers 207A shown in FIG. 2h above. Hoentschel262 even notes that liner layer 207A is optional and may be omitted. (Hoentschel262 at 12:33-35 (“[A] first spacer layer 206A, *possibly in combination with a respective liner 207A*, may be formed” (emphasis added)).) When liner

layers are used, they are part of disposable spacers 206 and 226, which define the location of recesses 211p and 211n for epitaxial layers 214p and 214n, as FIG. 2h shows. (Hoentschel262 at 13:5-9, 14:7-17, FIGS. 2c-2h.) In FIG. 2i below, however, the innermost L-shaped sidewall spacer layer extends **onto** epitaxial layers 214p and 214n (dark yellow), indicating it is a different liner layer than the one in FIG. 2h that defines where to form epitaxial layers 214p and 214n. Hoentschel262 also explains that liner layer 207A may be removed from the gate before forming spacer structures 216. (Hoentschel262 at 13:60-14:4 (explaining that, “in some illustrative embodiments, the liner 207A, previously formed in combination with the spacer layer 206A, may still be present . . . after removing spacers 206,” but not “in other illustrative embodiments”).)



Hoentschel262, FIG. 2i

236. Similarly, the protective layer is removed in the method of the '194 Patent. ('194 Patent at 6:19).



'194 Patent, FIG. 12

- f. **17[e] “forming a second ion lightly doped region within the semiconductor substrate adjacent to the gate in the second conductive transistor area before forming the spacer.”**

237. As I explain in Sections IX.B.2 and IX.B.3 regarding claims 8, 9, and 11, Hoentschel262 renders obvious the formation of lightly doped (LDD) regions adjacent to the gate before forming the spacer.

238. Hoentschel262 also renders obvious “forming a second ion lightly doped region within the semiconductor substrate adjacent to the gate in the second conductive transistor area before forming the spacer,” as recited in claim element 17[e], for the same reasons.

5. Claim 18: “The method of claim 17, wherein the second protective layer comprises silicon nitride.”

239. As I explain in Section IX.B.4, Hoentschel262 renders obvious the method of claim 17.

240. Hoentschel262 also discloses “wherein the second protective layer comprises silicon nitride,” as recited in claim 18. Hoentschel262 explicitly states that “the spacer layer 226A [may be] substantially comprised of silicon nitride.” (Hoentschel262 at 14:34-40.)

6. Claim 19: “The method of claim 18, wherein the second protective layer has a thickness of about 150 to 250 angstroms.”

241. As I explain in Section IX.B.5, Hoentschel262 renders obvious the method of claim 18.

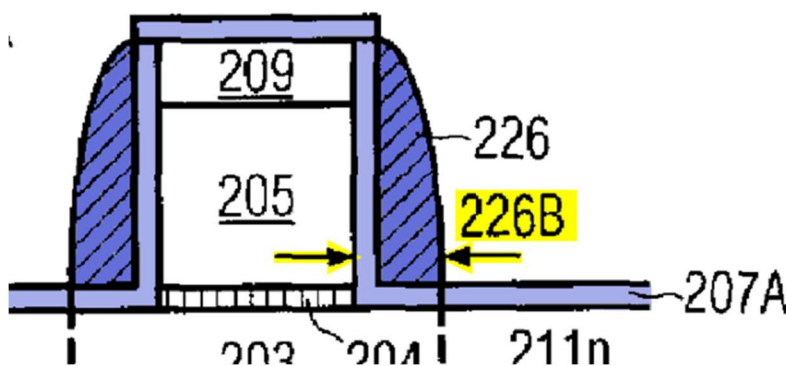
242. Hoentschel262 also discloses “wherein the second protective layer has a thickness of about 150 to 250 angstroms,” as recited in claim 19. Similarly to what I explain in Section IX.A.2.c regarding claims 4 and 13, Hoentschel262 states that “the respective size and offset of the recesses 211n is influenced by the spacer width 226B” of spacer layer 226A, and “the width 226B may range from approximately several nanometers, such as **3-50 nm**, depending on the process requirements.” (Hoentschel262 at 14:7-17 (emphasis added); *see also* Hoentschel262 at 13:39-47 (“[A] thickness of the spacer layer 226A, indicated as 226B, may be selected on the basis of device requirements of the second

transistor 250n, since the thickness 226B may substantially determine the resulting width of spacers formed from the layer 226A in the second transistor 250n.”), 13:56-60 (“[T]he spacer layer 226A is etched in order to form respective spacers 226, the width of which is substantially determined by the thickness 226B and thus the corresponding width will also be indicated as 226B.”).)

243. A thickness of 3 to 50 nm equates to a thickness of 30 to 500 angstroms. Further, a liner layer underneath spacer layer 226A is optional. If not used, thickness 226B would correspond to 226A alone. (Hoentschel²⁶² at 13:39-47 (referring to “a *thickness of the spacer layer 226A*, indicated as 226B” (emphasis added)); *see also* Hoentschel²⁶² at 13:60-14:1 (noting that “the liner 207A . . . *may* still be present” and that “a corresponding liner (not shown) *may* be formed” (emphases added))).)

244. I have been informed that when the prior art discloses a broader range of values (e.g., 30 to 500 angstroms) that encompasses a narrower range of claimed values (e.g., 150 to 250 angstroms), the broader prior art range discloses the narrower claimed range so long as the narrower claimed range is not “critical” (meaning different in kind, not just degree) as compared to the other values in the broader disclosed range. Here, there have been no allegations of criticality, and I am not aware of any. The thickness of the protective layer sets the spacing between the gate electrode and epitaxial material, which is a design parameter that merely depends on

device scaling. I am not aware of anything special, and certainly not critical, regarding a range of 150 to 250 angstroms. I therefore understand that Hoentschel262 discloses and renders obvious the claimed range. In fact, the claimed range is approximately in the middle of the disclosed range, and it is consistent with the spacing a person of ordinary skill in the art would have expected for contemporaneous devices (e.g., around the 65 nm node).



Hoenstchel262, FIG. 2g (excerpted)

7. Claim 20:

- a. 20[pre] “The method of claim 10, after forming the first epitaxial layer, the method further comprising:”**

245. As I explain in Section IX.A.1., Hoentschel262 discloses and renders obvious the method of claim 10.

246. Further, as I explain in Section IX.A.1.f, the first epitaxial layer is formed in FIG 2d. (Hoenstchel262 at 13:21-30). The steps described and pictured in FIG. 2e through FIG. 2i take place thereafter, and thus after forming the first epitaxial layer. (See Hoenstchel262 at 13:30-15:38, FIGS. 2d-2i.)

b. 20[a] “forming at least a second recess within the semiconductor substrate adjacent to the gate in the second conductive transistor area;”

247. Hoentschel²⁶² renders obvious “forming at least a second recess within the semiconductor substrate adjacent to the gate in the second conductive transistor area,” as recited in claim element 20[a].

248. After epitaxial layer 214p has been grown, Hoeschel262 states that “a further etch process may be performed to *form a respective recess or cavity 211n*, as indicated in dashed lines.” (Hoeschel262 at 14:7-13.) Recess/cavity 211n is located adjacent to the gate for NMOS transistor 250n, offset by an amount equal to the width of disposable spacer layer 226A as FIG. 2f shows below: “[T]he respective size and offset of the recesses 211n is influenced by the spacer width 226B . . . as is also explained with reference to the recesses 211p.” (Hoeschel262 at 14:7-13.)

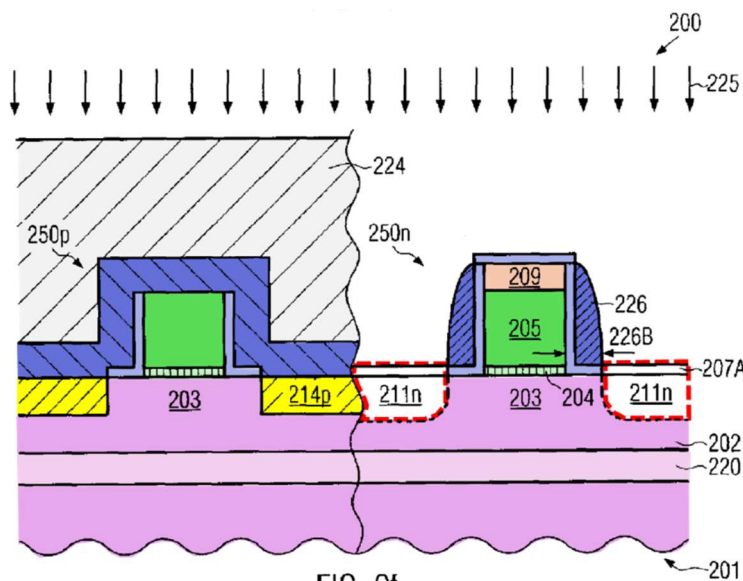
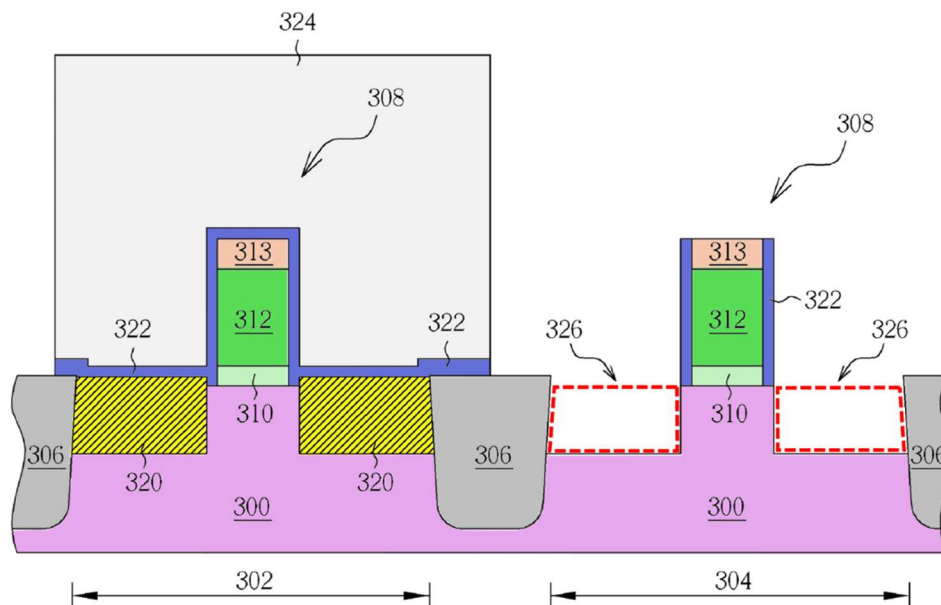


FIG. 2f

Hoenstchel262, FIG. 2f

249. Similarly, the method of the '194 Patent includes etching recesses 326. ('194 Patent at 5:62-64.)



'194 Patent, FIG. 11

c. 20[b] “forming a second epitaxial layer in the second recess;”

250. Hoentschel262 renders obvious “forming a second epitaxial layer in the second recess,” as recited in claim element 20[b].

251. Hoentschel262’s fabrication method includes forming strained semiconductor material 214n in recess 211n after epitaxial layer 214p has been formed: “FIG. 2g schematically illustrates the device 200 in a further advanced manufacturing stage, wherein the device 200, after a corresponding cavity etch process for actually forming the recesses 211n, is subjected to a further selective epitaxial growth process 215 for forming a strained semiconductor

material 214N adjacent to the respective channel region 203 of the second transistor 250n.” (Hoenstchel262 at 14:18-27.) “With respect to the epitaxial growth process 215, the same criteria apply as previously explained” for growing epitaxial material 214p, except that semiconductor material 214n “may comprise a silicon/carbon mixture for imposing a tensile strain to the channel region 203 of the second transistor 250n.” (Hoenstchel262 at 14:25-33.)

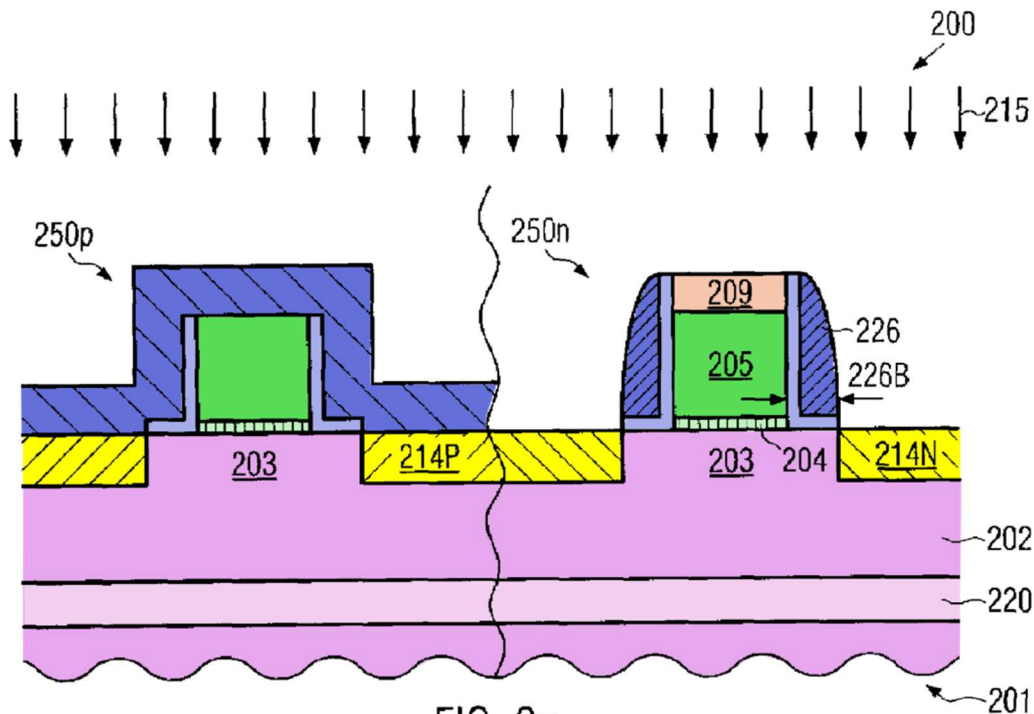
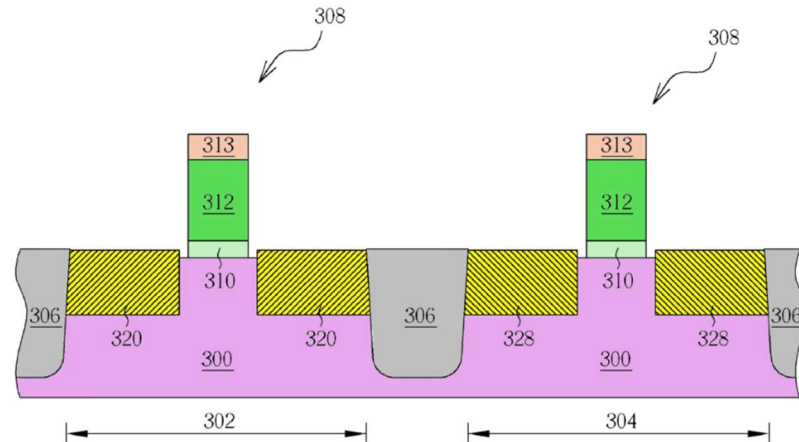


FIG. 2g

Hoenstchel262, FIG. 2g

252. The '194 Patent similarly discloses growing a second epitaxial layer in the second region. ('194 Patent at 6:13-22.)



'194 Patent, FIG. 12

d. 20[c] “removing the first protective layer; and”

253. Hoentschel262 renders obvious “removing the first protective layer,” as recited in claim element 20[c].

254. Hoentschel262 states: “After the epitaxial growth process 213 [for forming epitaxial layer 214p], the spacer layer 206A may be removed on the basis of any appropriate selective etch process.” (Hoentschel262 at 13:30-38.) Accordingly, the first protective layer (spacer layer 206A) may be removed after forming the first epitaxial layer (layer 214p).

e. 20[d] “forming a second ion lightly doped region within the semiconductor substrate adjacent to the gate in the second conductive transistor area before forming the spacer.”

255. As I describe in Section IX.B.2. and IX.B.3 regarding claims 8, 9, and 11, Hoentschel262 renders obvious the formation of lightly doped (LDD) regions adjacent to the gate before forming the spacer. Hoentschel262 renders

obvious “forming a second ion lightly doped region within the semiconductor substrate adjacent to the gate in the second conductive transistor area before forming the spacer,” as recited in claim element 20[d], for the same reasons.

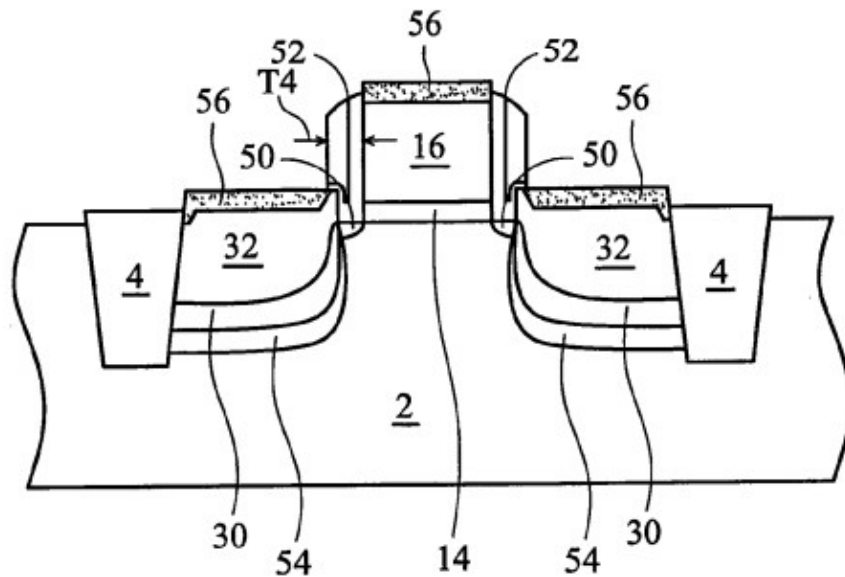
C. Ground 1C: The Combination of Hoentschel262 and Wang407 Renders Obvious Claims 5, 7-9, 11, 14, and 17-20.

256. Hoentschel262 in view of Wang407 teaches, suggests, and renders obvious all the elements of claims 5, 7-9, 11, 14, and 17- 20 of the '194 Patent.

257. For the reasons stated in my analysis below, I conclude that Hoentschel262, further viewed in light of Wang407, renders obvious claims 5, 7-9, 11, 14, and 17-20 because the differences between these claims, Hoentschel262, and Wang407 are such that these claims would have been obvious over these references.

258. As I explain in Section VIII.B, Wang407 is analogous art to both the '194 Patent and Hoentschel262. Like the '194 Patent, Wang407 describes a “method for forming stressors in metal-oxide-semiconductor (MOS) devices.” (Wang407 at 3:15-16.) Also similar to the '194 Patent, Wang407 recognized that, to “further enhance the performance of MOS devices, stress may be introduced in the channel region of a MOS transistor to improve carrier mobility.” (Wang407 at 1:28-30.) To accomplish such a result, Wang407 describes NMOS and PMOS transistors with raised epitaxial “stressors” grown adjacent to the gate that strain the channel region. (Wang407 at 4:4-21, Figs. 1-9 (PMOS), 5:58-6:4, Fig. 11 (NMOS).) As Wang407's Fig. 9 illustrates below, the Wang407 device structure includes “[l]ightly doped

source/drain (LDD) regions 50,” as well as multi-layered sidewall spacers 52, “a semiconductor substrate [2], a gate stack [comprising gate dielectric 14 and gate electrode 16] on the semiconductor substrate, and a stressor [32] adjacent the gate stack and having at least a portion in the semiconductor substrate.” (Wang407 at Abstract, 4:55-67.)



Wang407, Fig. 9

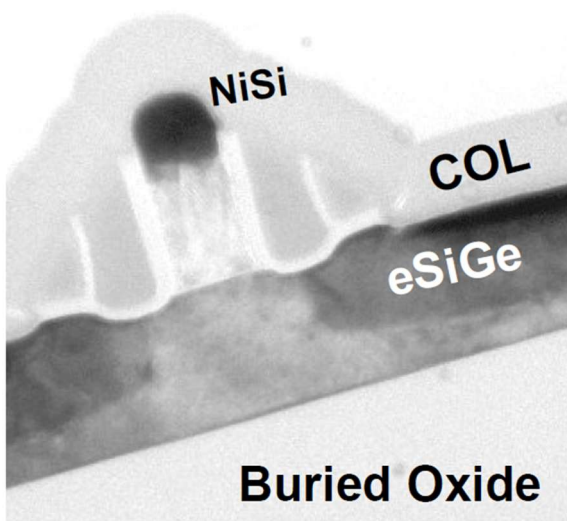
259. A person of ordinary skill in the art would have been motivated to combine Hoentschel262 with Wang407. Both references are analogous art to the '194 Patent, and to each other, as all are concerned with the fabrication of MOS devices using epitaxially grown stressors. (See '194 Patent at 1:15-19, 1:57-60; Hoentschel262 at Title, Abstract, 1:7-14, 2:66-3:2; Wang407 at Title, 1:65-2:2.) A person of ordinary skill in the art would have been motivated to look to Wang407 for specific details regarding Hoentschel262. For example, if a person of ordinary

skill in the art wanted additional details regarding what materials to use when making Hoentschel262's spacer structure 216, a person of ordinary skill in the art would have considered Wang407's spacers 52, which comprise "a liner oxide layer and a nitride layer." (Wang407 at 4:61-64.) A person of ordinary skill in the art would have understood that Hoentschel262's spacer structure 216 and Wang407's spacer 52 both serve the same purpose: establishing the doping profiles for the source/drain regions after growing epitaxial layers. (*See* Hoentschel262 at 14:43-56; Wang407 at 4:61-5:3, 5:58-60.)

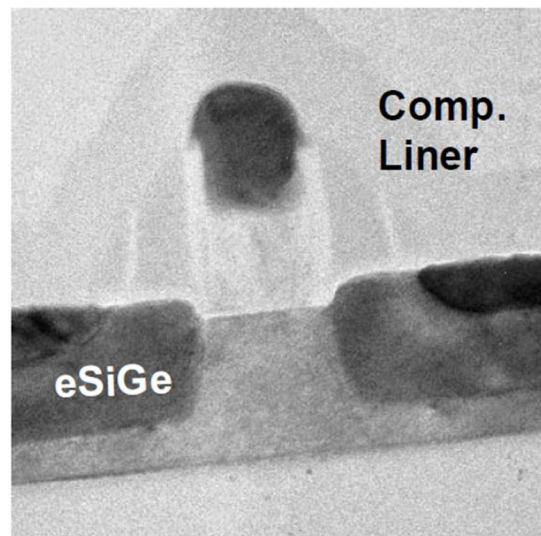
260. Additionally, a person of ordinary skill in the art would have reasonably expected to succeed when using an oxide liner and nitride spacer layer in the context of Hoentschel262's spacer structures 216. Hoentschel262 explains that spacer structures 216 "may comprise any appropriate number of individual spacer elements, depending on the complexity of the required dopant profile of the regions 217." (Hoentschel262 at 14:52-56.) As I explain in Section VI.C above, LDD and heavily doped source/drain regions were standard features of MOSFETs at the time. (*See also* Plummer at 76-82; Quirk at 211-13; Wolf3 at 595-98; Gupta at 1:13-47, FIGS. 1-2; Tseng at 1:50-65, FIGS. 1A-1C.) And, as I explain in Section IX.B.3.c regarding the Hua reference, medium doped source/drain regions were sometimes used as a bridge between LDD and heavily doped regions. (*See* Hua at 3:34-4:37, FIGS. 1-3.) When Hoentschel262 mentions "any appropriate number of

individual spacer elements, depending on the complexity of the required dopant profile” (Hoentschel262 at 14:52-56), a person of ordinary skill in the art would have understood these are the types of considerations in question.

261. For example, if a medium doped region is unnecessary, a person of ordinary skill in the art would have found it obvious to implement Hoentschel262’s spacer structure 216 simply by applying Wang407’s spacers 52 as they are disclosed in Wang407. (See Wang407 at 4:61-5:3, 5:58-60, Figs. 9, 11.) Or, if a more complex doping profile 217 is desired, such as one that includes a medium-doped region, a person of ordinary skill in the art would have found it obvious to implement Hoentschel262’s spacer structure 216 by repeating Wang407’s spacers twice, consistent with the drawing in Hoentschel262’s FIG. 2i and the real-world public disclosures thereof (below) in the scientific literature from the same authors.



Wei, FIG. 2



Horstmann, FIG. 2

262. Additionally, Wang407 demonstrates a reasonable expectation of success implementing Hoentschel262's disclosed method when epitaxial materials 214p and 214n are "overfill[ed]" into cavities 211p and 211n, respectively. (See Hoentschel262 at 9:9-15, 13:21-26, 14:18-33, FIGS. 2e-2i; Wang407 at 4:33-48, 5:58-6:4, Figs. 7-11; Wei at Fig. 2; Horstmann at Fig. 2.)

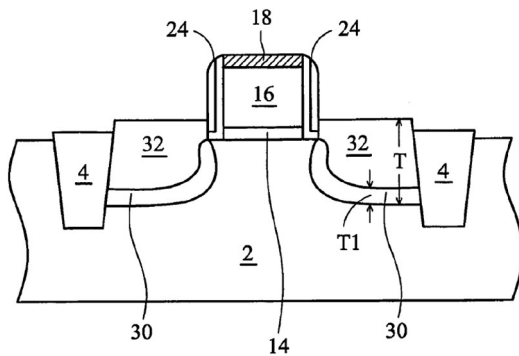
263. In my opinion, a person of ordinary skill in the art would have found such combinations of Hoentschel262 and Wang407 to be examples of (1) combining prior art elements (e.g., Hoentschel262's spacer structures 216 and Wang407's spacers 52) according to known methods to yield predictable results; (2) adopting one disclosed element (e.g., one or more of Wang407's spacers, each comprising a liner oxide and nitride spacer) to implement another (e.g., Hoentschel262's spacer structures 216) to obtain predictable results; (3) using a known technique (e.g., using one or more of Wang407's spacers, each comprising a liner oxide and nitride spacer, to define source/drain doping profiles) to improve similar devices (e.g., Hoentschel262's device and doping profiles 217) in the same way; (4) applying a known technique (e.g., using one or more of Wang407's spacers, each comprising a liner oxide and nitride spacer, to define source/drain doping profiles) to a known device ready for improvement (e.g., Hoentschel262's device and doping profiles 217) to yield predictable results; and (5) a teaching, suggestion, or motivation in the prior art (e.g., Wang407's teachings to use an oxide liner and

nitride spacer to define source/drain doping profiles) that would have led a person of ordinary skill in the art to modify Hoentschel262 as I indicated above.

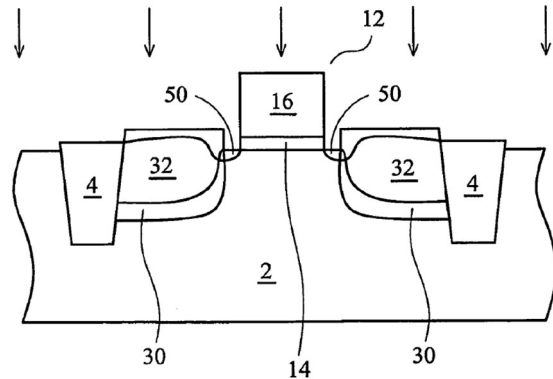
264. The combined teachings of Hoentschel262 and Wang407 further confirm that a person of ordinary skill in the art would have found it obvious for Hoentschel262's doping profile 217 to include LDD/extension regions, as I discuss in Section IX.B.2 above. Like Hoentschel262's disposable spacer layers 206A and 226A, the silicon nitride portions of Wang407's "dummy spacers" 24 "are removed by etching in phosphoric acid." (Wang407 at 4:49-54; *see also* Hoentschel262 at 13:30-38, 14:34-40 ("hot phosphoric acid").) Additionally, "the liner oxide portions of Wang407's dummy spacers 24 are stripped using diluted hydrofluoric acid." (Wang407 at 4:49-54.) "Lightly doped source/drain (LDD) regions 50 are then formed" in Wang407 by ion implantation, using the gate "as a mask so that LDD regions 50 are substantially aligned with the . . . gate stack." (Wang407 at 4:49-58.)

265. A person of ordinary skill in the art would have found it obvious to do the same in Hoentschel262, as this would have been a readily apparent an example "of appropriate spacer techniques and implantation processes" to establish "respective lateral and vertical dopant profiles for respective drain and source regions 217." (*See* Hoentschel262 at 14:43-56.) Like LDD regions 50 in Wang407's Figs. 9 and 11, the extension regions in Hoentschel262's FIG. 2i (circled in red

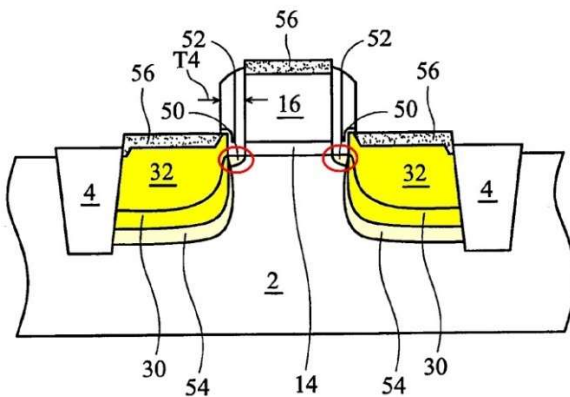
below) are aligned with the gate edge. A person of ordinary skill in the art would have found it obvious to use Wang407's disclosed method for forming them. (See Wang407 at 4:49-58, Figs. 7-9.) Additionally, a person of ordinary skill in the art would have found it obvious to form those extension regions as LDD regions, which was a standard part of processing MOSFET devices to mitigate short-channel effects. (See Section VI.C above; Plummer at 76-82; Quirk at 211-13; Wolf3 at 595-98.)



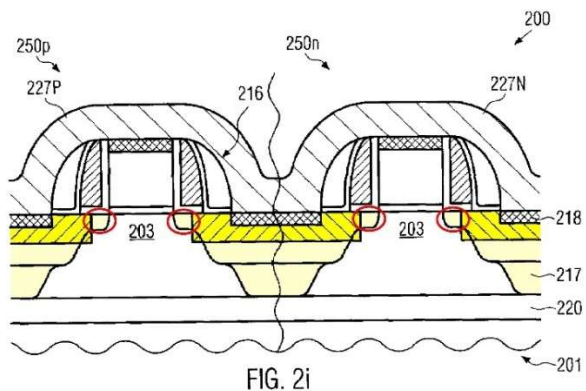
Wang407, Fig. 7



Wang407, Fig. 8



Wang407, Fig. 9

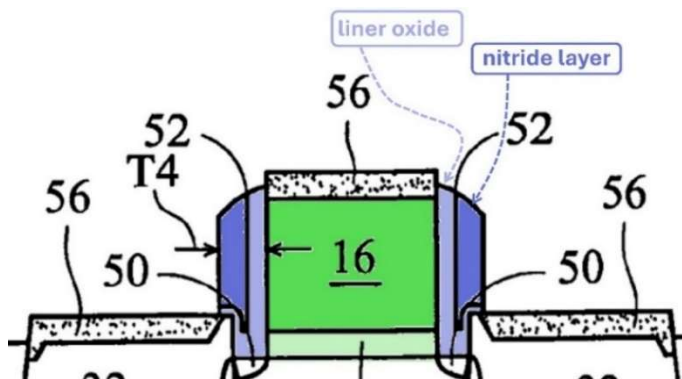


Hoentschel262, FIG. 2i

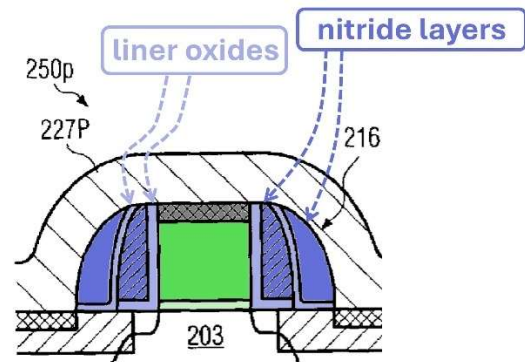
1. Claim 5/14: “The method of claim [1/10], wherein [the/each] spacer further comprises an oxide liner and a nitride spacer.”

266. As I explain in Section IX.B.1, Hoentschel262 renders obvious the methods of claims 5 and 14. Additionally, by further applying Wang407’s teachings to Hoentschel262, a person of ordinary skill in the art also would have found it rendered obvious both “wherein the spacer further comprises an oxide liner and a nitride spacer,” as recited in claim 5, and “wherein each spacer further comprises an oxide liner and a nitride spacer,” as recited in claim 14.

267. Wang407 explicitly states that spacer 52 comprises “a liner oxide layer and a nitride layer,” as in Fig. 9 below. (Wang407 at 4:61-64.) As I explain in Section IX.C above, a person of ordinary skill in the art would have found it obvious to implement Hoentschel262’s spacer structures 216 using either one liner oxide / nitride spacer pair (e.g., if a medium doped region is not desired), as depicted in Wang407’s Fig. 9, or two liner oxide / nitride spacer pairs (e.g., if a medium doped region is desired), as depicted in Hoentschel262’s FIG. 2i.



Wang407, Fig. 9 (excerpted)

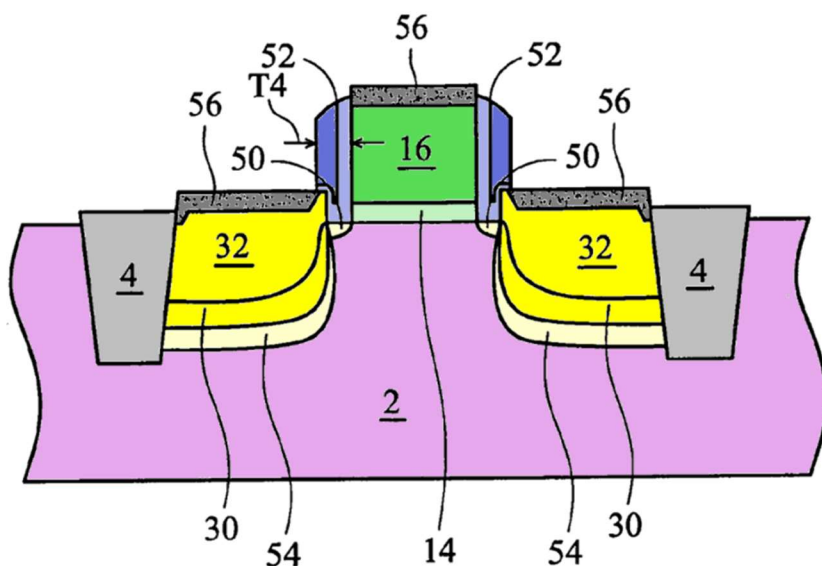


Hoentschel262, FIG. 2i (excerpted)

2. Claim 7: “The method of claim 1, further comprising a step of forming a source/drain region within the semiconductor substrate adjacent to the gate after forming the spacer.”

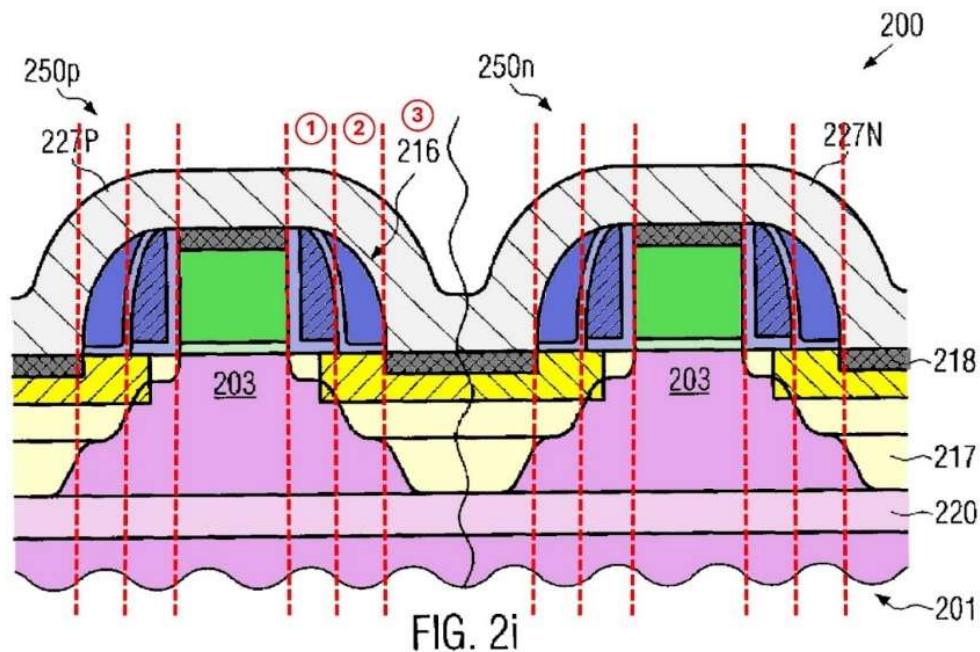
268. As I explain in Section IX.A.2.e, Hoentschel262 discloses and renders obvious the method of claim 7. Additionally, by further applying Wang407's teachings to Hoentschel262, a person of ordinary skill in the art would have found obvious "a step of forming a source/drain region within the semiconductor substrate adjacent to the gate after forming the spacer," as recited in claim 7.

269. Wang407 discloses the formation of source/drain regions adjacent to the gate after forming the spacer. (Wang407 at 4:61-5:3.) “In FIG. 9, spacers 52 are formed.” (Wang407 at 4:61.) “*Deep source/drain regions 54 are then formed, preferably by implanting p-type impurities such boron, indium, and the like.*” (Wang407 at 5:1-3 (emphasis added).)



Wang407, Fig. 9

270. As I explain in Section IX.C above, a person of ordinary skill in the art would have found it obvious to follow similar spacer/implantation sequences in Hoentschel262 to establish “respective lateral and vertical dopant profiles for respective drain and source regions 217.” (Hoentschel262 at 14:43-56.) For example, as I explain in Section IX.B.3.c above, Hoentschel262’s FIG. 2i illustrates a dopant profile 217 with three different regions: (1) a lightly doped (LDD) region immediately adjacent to the gate, which is defined by the gate, (2) a medium doped region just outside of the inner spacer (i.e., the inner liner/spacer pair), which is defined by the inner spacer, and (3) a heavily doped region just outside of the outer spacer (i.e., the outer liner/spacer pair), which is defined by the outer spacer. I have added the numbers and dotted red lines below to illustrate this.



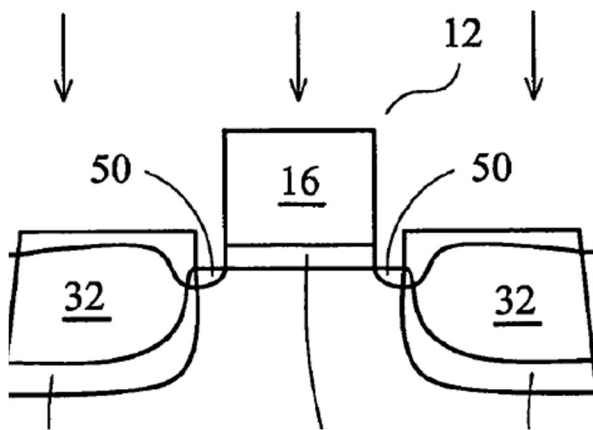
Hoentschel262, FIG. 2i (annotated)

271. A person of ordinary skill in the art would have understood, consistent with the disclosed process in Wang407, that each doped region above is formed by ion implantation using a corresponding mask: the gate masks the LDD implant of region 1; the inner spacer (first liner layer/spacer layer pair) masks the medium doped implant of region 2; and the outer spacer (second liner layer/spacer layer pair) masks the heavy doped implant of region 3. (*See* Hua at 3:34-39, 4:5-10, 4:29-33, FIGS. 1-3; Hoentschel262 at 14:43-56, FIG. 2i.) In other words, a person of skill would have understood that each successive spacer would restrict the implantation only to the exposed regions, as the dotted red lines above indicate. If medium doped region 2 is not desired, then a person of ordinary skill in the art would have understood only one spacer (liner layer/spacer layer pair) would be used. (Wang407 at 4:49-5:3, Figs. 8-9.) Either way, the heavily doped regions masked by the outermost spacer layers are formed after completing formation of spacer structure 216. (*See* Wang407 at 4:61-5:3; Hua at 4:29-33, FIG. 3; Hoentschel262 at 14:43-56.) Indeed, this is fundamentally how spacers are used to perform source/drain engineering. (*See*, for example, Plummer at 76-82, Figs. 2-31 to 2-33; Quirk at 211-13, Fig. 9.17; Wolf3 at 595-98, Fig. 9-31(a)-(f).)

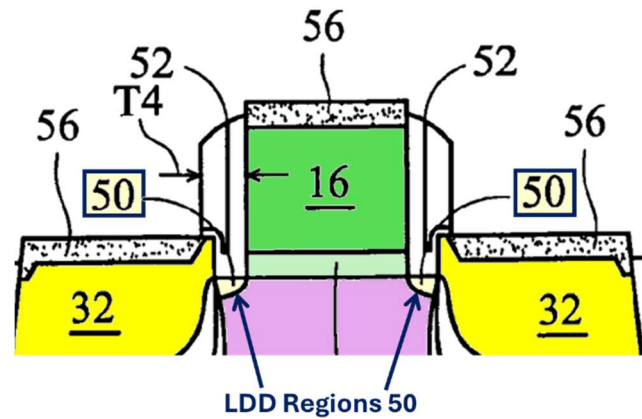
3. Claims 8/11: “The method of claim [1/10], further comprising a step of forming a [first] lightly doped region within the semiconductor substrate adjacent to the gate [in the first conductive transistor area].”

272. As I explain in Section IX.B.2 above, Hoentschel262 discloses and renders obvious the method of claims 8 and 11. Additionally, by further applying Wang407’s teachings to Hoentschel262, a person of ordinary skill in the art also would have found it rendered obvious both “a step of forming a lightly doped region within the semiconductor substrate adjacent to the gate,” as recited in claim 8, and “a step of forming a first lightly doped region within the semiconductor substrate adjacent to the gate in the first conductive transistor area,” as recited in claim 11.

273. Wang407 discloses “[l]ightly doped source/drain (LDD) regions 50” formed “by implanting a p-type impurity.” (Wang407 at 4:55-56.) This process takes place after dummy spacers 24 have been removed, such that only Wang407’s “gate stack 12 acts as a mask” and “LDD regions 50 are substantially aligned with the respective edge of gate stack 12.” (Wang407 at 4:56-58, 4:49-54, Fig. 8.) This process—making and removing a spacer to form LDD regions outside epitaxial regions—is the same process the ’194 Patent describes for forming its “lightly doped region 222.” (’194 Patent at 3:29-54, Figs. 3-4.)

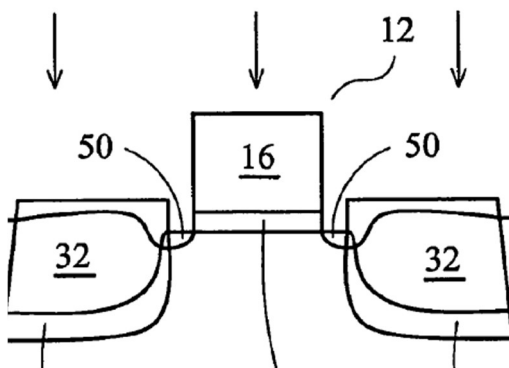


Wang407, Fig. 8 (excerpted)

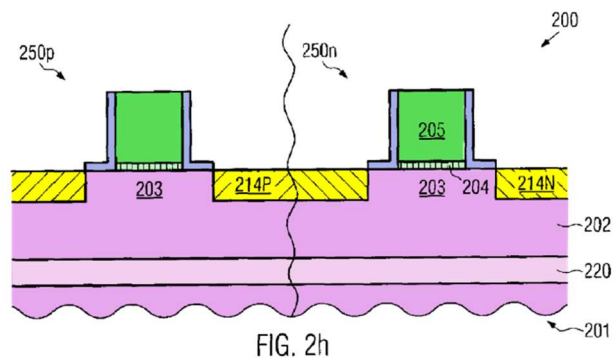


Wang407, Fig. 9 (excerpted)

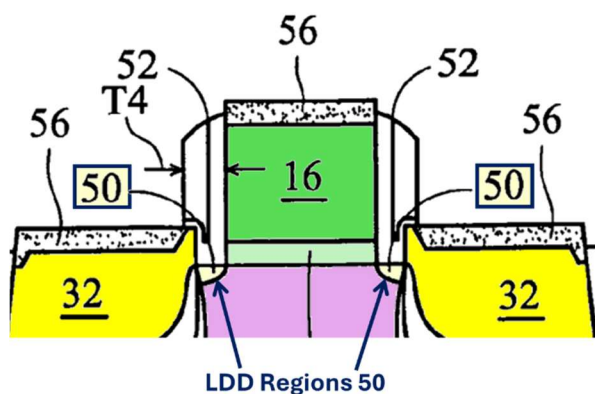
274. Thus, as Figs. 8 and 9 confirm, Wang407 discloses a step of forming a lightly doped region (LDD regions 50) within the semiconductor substrate (substrate 2) adjacent to the gate (gate stack 12). As I explain above in Section IX.C, a person of ordinary skill in the art would have found it obvious to form the extension regions in Hoentschel262's FIG. 2i in the same way. (See also Section IX.B.2 above.) Note, the light blue L shaped structure in Hoentschel262, FIG. 2h, is the optional disposable optional liner layer 207A, not the spacer 216.



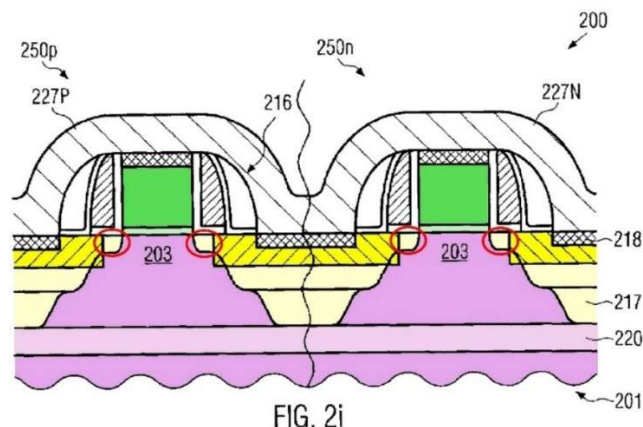
Wang407, Fig. 8 (excerpted)



Hoentschel262, FIG. 2h (annotated)



Wang407, Fig. 9 (excerpted)



Hoentschel262, FIG. 2i (annotated)

4. Claim 9:

a. 9[pre] “The method of claim 1, further comprising:”

275. As I explain in Section IX.A.1, Hoentschel262 discloses and renders obvious the method of claim 1.

b. 9[a] “forming a lightly doped region in the semiconductor substrate adjacent to the gate after forming the epitaxial layer;”

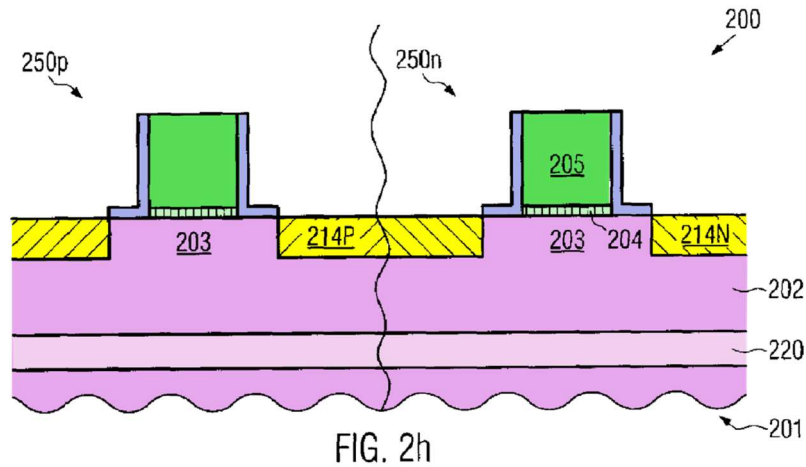
276. As I explain in Section IX.B.3.b, Hoentschel262 renders obvious claim element 9[a]. Additionally, by further applying Wang407’s teachings to Hoentschel262, a person of ordinary skill in the art would have found it rendered obvious “forming a lightly doped region in the semiconductor substrate adjacent to the gate after forming the epitaxial layer,” as recited in claim element 9[a].

277. Wang407 discloses to selectively grow epitaxial regions 32 in recesses 26, offset from the gate by a distance set by dummy spacers 24. (Wang407

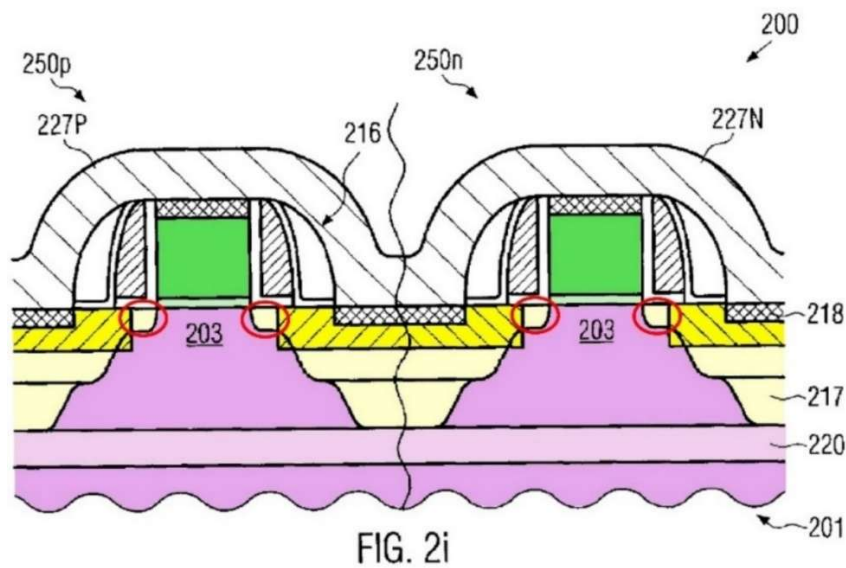
at 3:63-65, 4:34-48, Figs. 5-7.) Removing dummy spacers 24, as Wang407's Fig. 8 shows below, creates a gap between the epitaxial regions and gate stack 12. (Wang407 at 4:49-54, Fig. 8.) A person of skill in the art would understand that this exposes a portion of substrate 2 to the ion implantation process used to form LDD regions 50. (Wang407 at 4:55-58, Fig. 8.) Thus, LDD regions 50 are formed after forming epitaxial regions 32. This is the same arrangement the '194 Patent describes for its "lightly doped region." (See '194 Patent at 3:45-4:3, 5:60-6:44, Figs. 3-4, 11-13.)



278. As I explain in Section IX.C above, a person of ordinary skill in the art would have found it obvious to form Hoentschel262's source/drain extension regions (circled below in red) in an analogous manner. (Hoentschel262, 14:43-56.)



Hoentschel262, FIG. 2h (annotated)



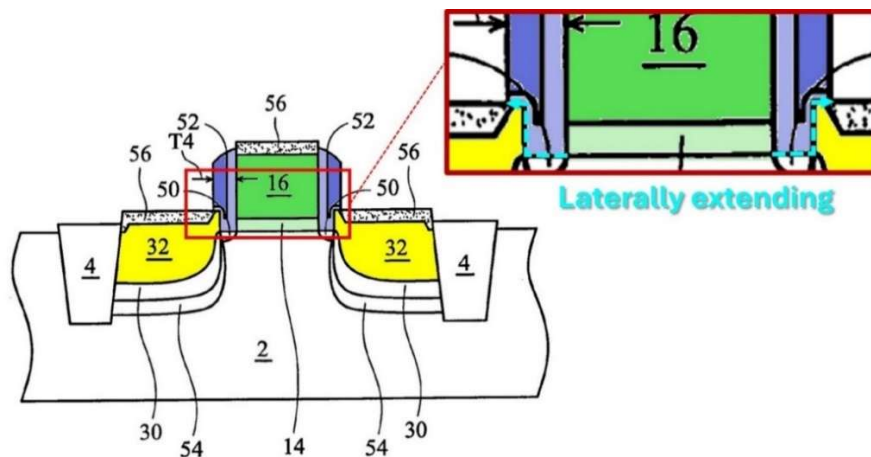
Hoentschel262, FIG. 2i (annotated)

- c. 9[b] “forming the spacer on the sidewall of the gate and on the portion of the epitaxial layer after forming the lightly doped region; and”

279. As I explain in Section IX.B.3.c, Hoentschel262 renders obvious claim element 9[b]. Additionally, by further applying Wang407’s teachings to

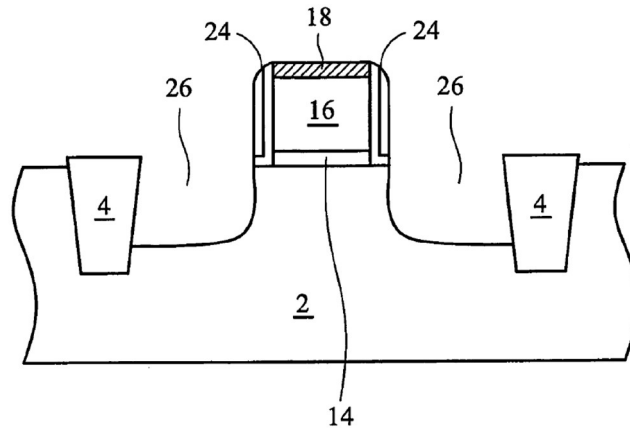
Hoentschel262, a person of ordinary skill in the art would have found it rendered obvious “forming the spacer on the sidewall of the gate and on the portion of the epitaxial layer after forming the lightly doped region,” as recited in claim element 9[b].

280. Wang407 discloses “a liner oxide layer and a nitride layer [that] are blanket formed” and “then patterned to form spacers 52.” (Wang407 at 4:61-64.) As Fig. 9 shows below (in which I have magnified the bottom of the spacers 52 and colored the two different layers dark and light blue), a person of ordinary skill in the art would have understood that Wang407’s spacers 52 are formed (a) on the sidewall of the gate (gate stack 12 comprising gate dielectric 14 and gate electrode 16) and (b) on a portion of the epitaxial layer (SiGe region 32) after (c) the lightly doped region 50 is formed.



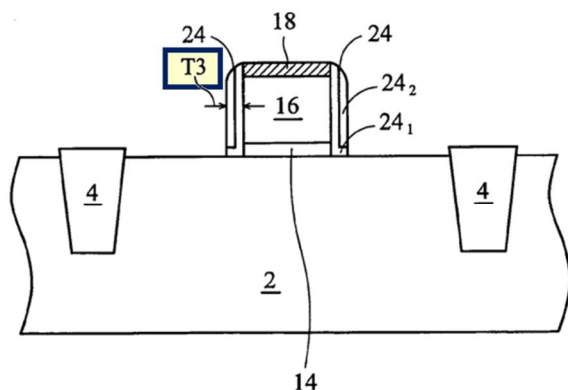
Wang407, Fig. 9 (annotated & magnified)

281. Wang407 explains that recesses 26 (shown in Fig. 5), where epitaxial growth of SiGe regions 30/32 takes place, “are formed along the edges of dummy spacers.” (Wang407 at 3:63-65; *see also* Wang407 at 4:33-40, Figs. 5-7.)

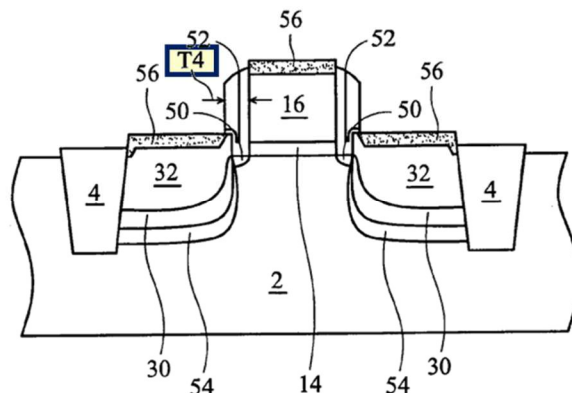


Wang407, Fig. 5

282. According to Wang407, dummy spacers 24 have a thickness T3, as Fig. 4 shows below. (Wang at 4:64-67.) Because “recesses 26 are formed along the edges of dummy spacers 24,” SiGe regions 30/32 are spaced a distance T3 away from the sidewalls of gate stack 12. (Wang407 at 3:63-65, Figs. 4-9.) Then, dummy spacers 24 “are removed.” (Wang407 at 4:49-54.) After ion implantation, new spacers 52 are formed. (Wang407 at 4:61-67.) Spacers 52 “have a thickness T4 greater than a thickness T3 of dummy spacers 24.” (Wang407 at 4:64-67.) Wang407’s Fig. 9 shows the thicknesses T4. Because T4 is **greater** than T3, a person of ordinary skill in the art would have understood Wang407’s fabrication process necessary results in spacers 52 forming on a portion of epitaxial SiGe regions 32.

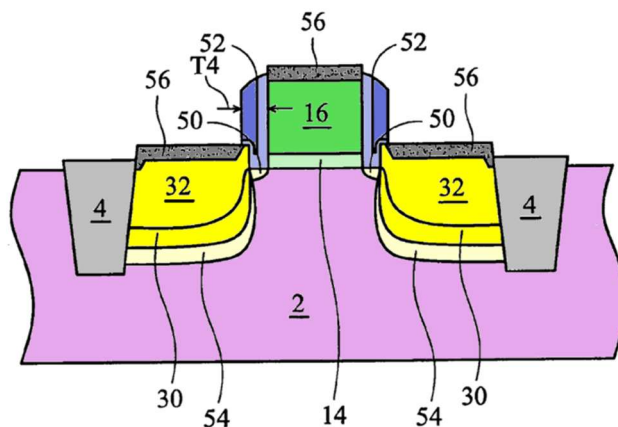


Wang407, Fig. 4



Wang407, Fig. 9

283. Therefore, as Fig. 9 shows, a person of skill in the art would have understood spacers 52 are formed (a) on the sidewall of the gate (gate stack 12) and (b) on a portion of the raised epitaxial layer (SiGe region 32) after (c) the lightly doped region (LDD 50) is formed. Hoentschel262 discloses an analogous process, using spacer layers 206A and 226A as dummy spacers for defining the location of epitaxial layers 214p and 214, then using a replacement spacer structure 216 (analogous to Wang407's spacer 52) to establish the source/drain doping profile 217. (Hoentschel262 at 12:64-14:56, FIGS. 2c-2i.) As I explain in Section IX.C above, a person of ordinary skill in the art would have found it obvious to form Hoentschel262's LDD extension regions and spacer structures 216 in the same manner.



Wang407, Fig. 9

d. 9[c] “forming a source/drain region in the semiconductor substrate adjacent to the spacer.”

284. As I explain in Section IX.B.3.d, Hoentschel262 renders obvious claim element 9[c]. Additionally, by further applying Wang407’s teachings to Hoentschel262, a person of ordinary skill in the art also would have found it rendered obvious “forming a source/drain region in the semiconductor substrate adjacent to the spacer,” as recited in claim element 9[b].

285. For the same reasons I explain in Section IX.C.2 above regarding claim 7, a person of ordinary skill in the art would have found it obvious to form the heavily doped regions masked by the outermost spacer layers after completing the formation of spacer structure 216. (See Wang407 at 4:61-5:3; Hua at 4:29-33, FIG. 3; Hoentschel262 at 14:43-56.)

5. Claim 17

a. 17[pre]-17[c]

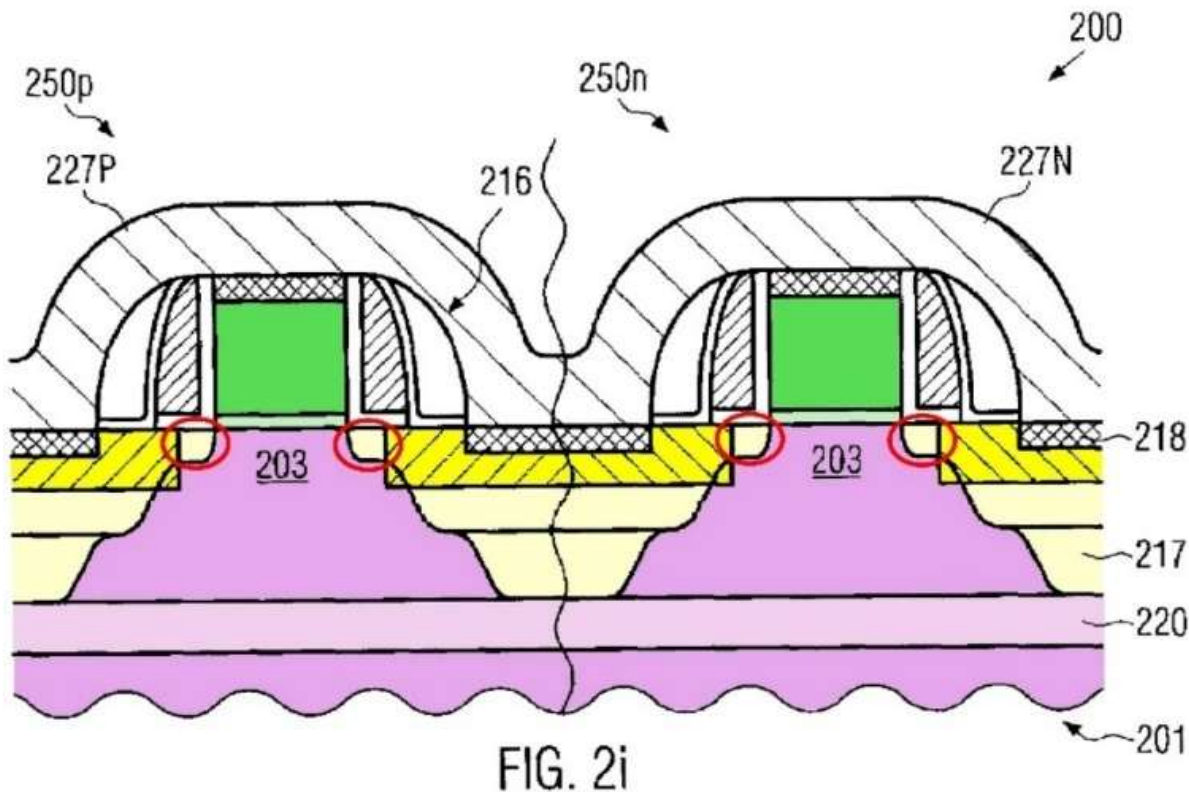
286. As I explain in Section IX.B.4.a through IX.B.4.d above, Hoentschel262 discloses and renders obvious claim elements 17[pre] through 17[c].

b. 17[d] “removing the second protective layer; and”

287. As I explain in Section IX.B.4.e, Hoentschel262 renders obvious claim element 17[d]. Additionally, by further applying Wang407’s teachings to Hoentschel262, a person of ordinary skill in the art also would have found it rendered obvious “removing the second protective layer,” as recited in claim element 17[d].

288. Wang407 teaches that dummy spacers 24 (which are directly analogous to Hoentschel262’s spacers 206 and 226) “are removed” after growing the epitaxial source/drain layer. (Wang407 at 4:49-50.) Specifically, Wang407 teaches that “the silicon nitride portions of dummy spacers 24 and hard mask 18 are removed by etching in phosphoric acid, and the liner oxide portions of dummy spacers 24 are stripped using diluted hydrofluoric acid.” (Wang407 at 4:50-54.) This accommodates the LDD doping process by exposing the substrate next to the gate. (See Wang407 at 4:55-58, Figs. 8-9.) The same process “may also be used with the formation of NMOS devices,” not just PMOS devices. (Wang407 at 5:58-60, Fig. 11.)

289. As I explained above in Section IX.C, a person of ordinary skill in the art would have found it obvious to form Hoentschel262's source/drain extension regions (circled in red) in an analogous manner, including by removing the "second protective layer" (layer 226A). (Hoentschel262 at 14:34-56.)



Hoentschel262, FIG. 2i (annotated)

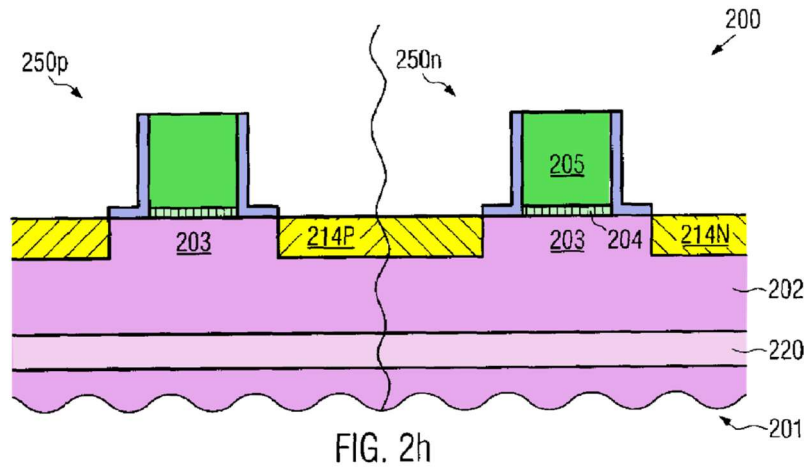
- c. [17e] “forming a second ion lightly doped region within the semiconductor substrate adjacent to the gate in the second conductive transistor area before forming the spacer.”

290. As I explain in Section IX.B.4.f above, Hoentschel262 renders obvious claim element 17[e]. Additionally, by further applying Wang407's teachings to Hoentschel262, a person of ordinary skill in the art also would have found it rendered

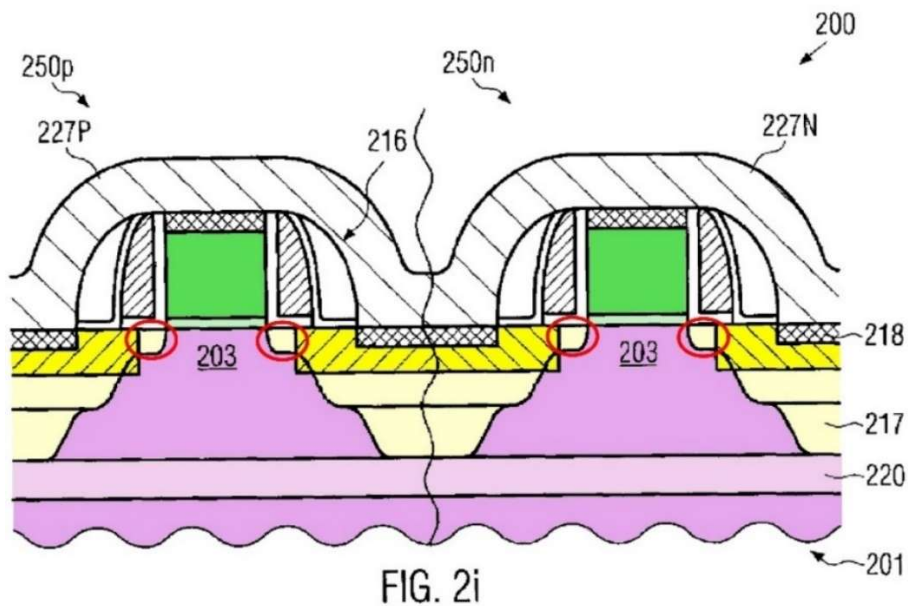
obvious “forming a second ion lightly doped region within the semiconductor substrate adjacent to the gate in the second conductive transistor area before forming the spacer,” as recited in claim element 17[e].

291. As I explain in Sections IX.C, IX.C.3, and IX.C.4 above regarding claims 8, 9, and 11, a person of ordinary skill in the art would have found it obvious, in view of Wang407’s disclosures, to form Hoentschel262’s extension/LDD regions in the SOI substrate adjacent to the gates before forming spacer structures 216. (*See* Wang407 at 4:49-5:3, Figs. 7-9, 11; Hoentschel262 at 14:34-56, FIGS. 2h-2i.)

292. Wang407 teaches that the same process applies to both PMOS devices with epitaxially grown SiGe and NMOS devices with epitaxially grown SiC. (Wang407 at 4:33-48, 5:58-6:4, Fig. 11.) As I explain in Section IX.C above, a person of ordinary skill in the art would have found it obvious to form Hoentschel262’s source/drain extension regions (circled below in red) in an analogous manner, including for NMOS device 250n. (Hoentschel262 at 14:34-56.)



Hoentschel262, FIG. 2h (annotated)



Hoentschel262, FIG. 2i (annotated)

6. Claim 18: “The method of claim 17, wherein the second protective layer comprises silicon nitride” and
Claim 19: “The method of claim 18, wherein the second

protective layer has a thickness of about 150 to 250 angstroms.”

293. As I explain in Section IX.B.5 through IX.B.6, Hoentschel262 discloses and renders obvious claims 18 and 19 by itself.

7. Claim 20:

a. 20[pre]-20[c]

294. As I explain in Section IX.B.7.a through IX.B.7.d, Hoentschel262 discloses and renders obvious claim elements 20[pre] through 20[c].

b. 20[d] “forming a second ion lightly doped region within the semiconductor substrate adjacent to the gate in the second conductive transistor area before forming the spacer.”

295. As I explain in Section IX.B.7.e., Hoentschel262 renders obvious the method of claim element 20[d]. Additionally, by further applying Wang407’s teachings to Hoentschel262, a person of ordinary skill in the art also would have found it rendered obvious “forming a second ion lightly doped region within the semiconductor substrate adjacent to the gate in the second conductive transistor area before forming the spacer,” as recited in claim element 20[d].

296. For the same reasons I explain in Sections IX.C, IX.C.3, and IX.C.4 above regarding claims 8, 9, and 11, a person of ordinary skill in the art would have found it obvious to form Hoentschel262’s LDD/extension regions adjacent to the

gate before forming spacer structure 216. (See Wang407 at 4:61-5:3; Hoentschel262 at 14:34-56.)

D. Grounds 2A and 2B: Wang753 Alone Anticipates (Ground 2A) and Renders Obvious (Ground 2B) Claims 1-3, 5-12, 14-16, 21, and 22

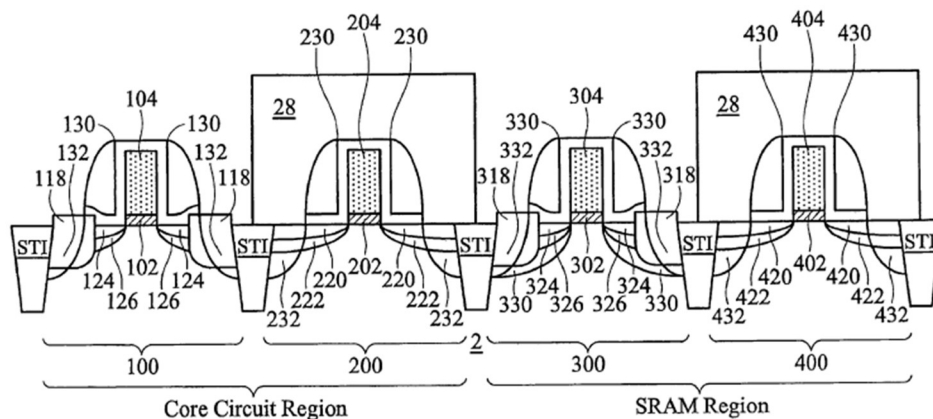
297. Wang753 teaches, suggests, and renders obvious all the elements of claims 1-3, 5-12, 14-16, 21, and 22 of the '194 Patent.

298. Through the analysis below, I conclude that Wang753 anticipates claims 1-3, 5-12, 14-16, 21, and 22 (Ground 2A) because Wang753 discloses every limitation of those claims when viewed from the perspective of a person of ordinary skill in the art.

299. For essentially the same reasons stated in my analysis below, I also conclude that Wang753 renders claims 1-3, 5-12, 14-16, 21, and 22 obvious (Ground 2B), because the differences between claims 1-3, 5-12, 14-16, 21, and 22 and Wang753 are such that claims 1-3, 5-12, 14-16, 21, and 22 would have been obvious to a person of ordinary skill in the art.

300. Wang753 “relates generally to semiconductor devices, and more particularly to PMOS devices with SiGe stressors.” (Wang753 at 1:6-9.) As FIG. 13 shows below, Wang753 describes a “semiconductor structure [that] includes a core circuit and an SRAM cell.” (Wang753 at 1:51-56, 2:24-29.) Active region 100 contains core PMOS devices; active region 200 contains core NMOS devices; active

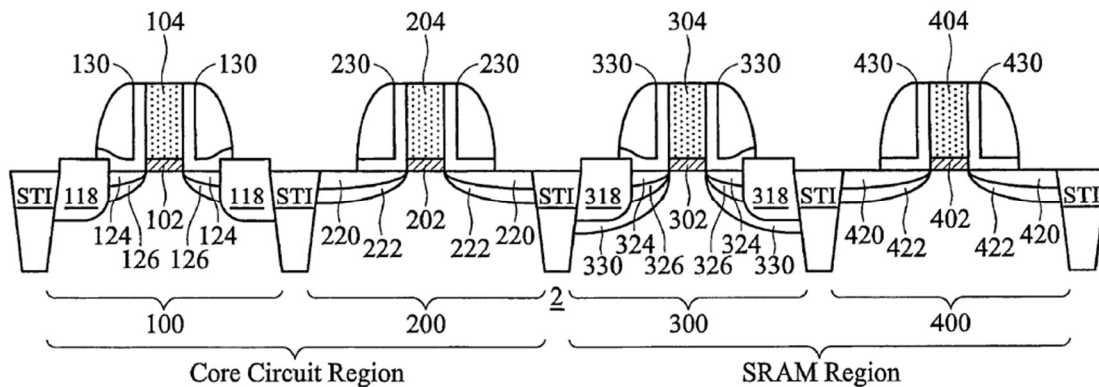
region 300 contains SRAM PMOS devices; and active region 400 contains SRAM NMOS devices. (Wang753 at 3:43-49, FIG. 13.) The core PMOS devices include “a gate dielectric 102 on substrate 2 and a gate electrode 104 on gate dielectric 102” (Wang753 at 3:49-52), raised “SiGe stressors 118” (Wang753 at 4:14-18), and “spacers 130” comprising “a liner oxide layer 25 and a nitride layer 27” (Wang753 at 5:19-26). Additionally, the core PMOS devices include “LDD regions 124” formed by introducing p-type impurities. (Wang753 at 4:45-51.) The SRAM PMOS devices are similar and further include current-tuning regions 330. (Wang753 at 3:52-59, 4:14-18, 4:45-51, 4:56-58.)



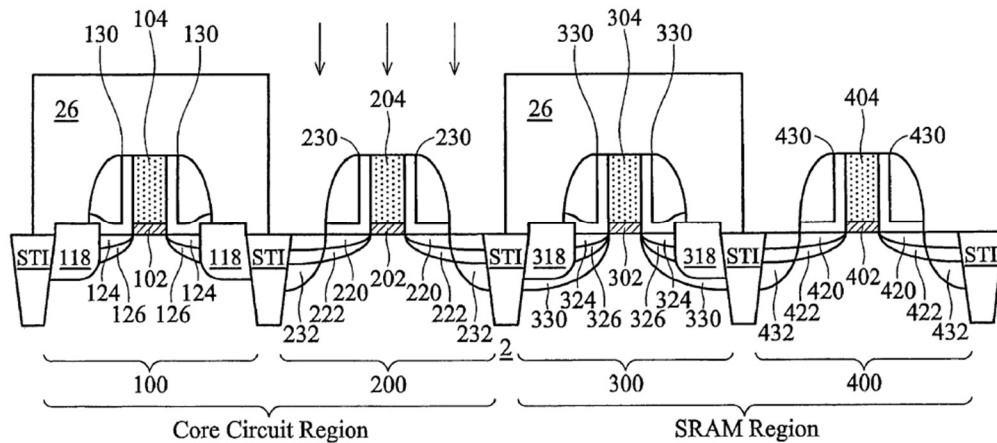
Wang753, FIG. 13

301. Although it does not meaningfully affect my analysis of Wang753, liner oxide layer 25 would not extend over gate electrode 104 as it is shown in FIG. 13 above. Rather, it would appear as in Wang753’s FIGS. 11 and 12 (shown below). A person of ordinary skill in the art would have identified this as a drawing error in FIG. 13. Wang753 explains that the liner oxide layer is “patterned to form

spacers 130 . . . as shown in FIG. 11.” (Wang753 at 5:19-22.) Accordingly, the liner oxide layer (25) would appear as in FIGS. 11 and 12, not as in FIG. 13. A person of ordinary skill in the art would have identified this as a drawing error because no processing steps are disclosed that would alter that aspect of the liner oxide layer. (See Wang753 at 5:19-42, FIGS. 11-13.)



Wang753, FIG. 11



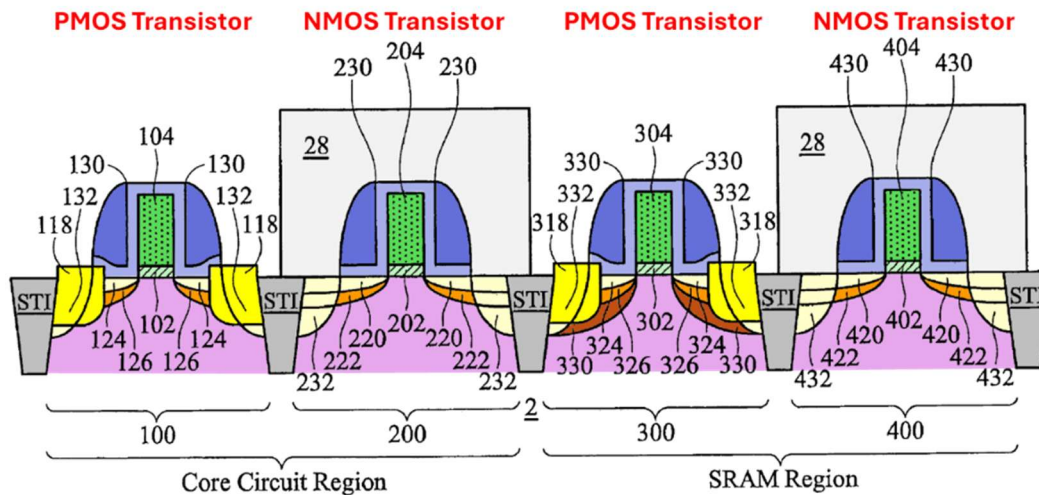
Wang753, FIG. 12

1. Independent Claims 1 and 10

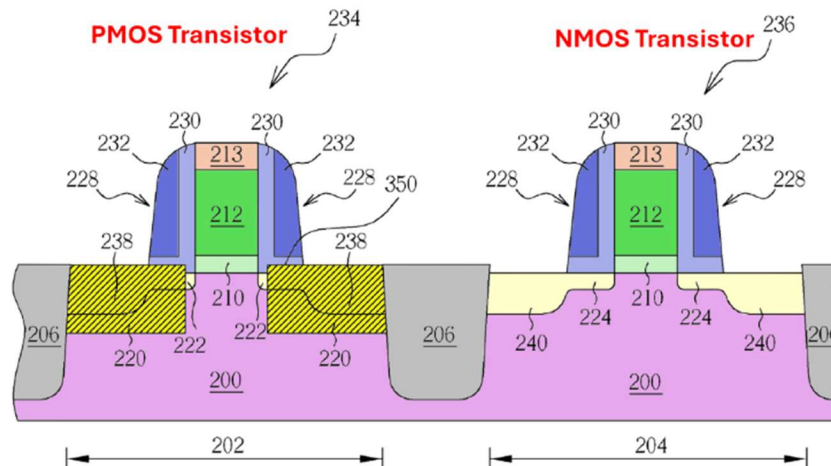
a. 1[pre]/10[pre]: “A method of fabricating a [MOS/CMOS] transistor, comprising:”

302. Wang753 discloses both “[a] method of fabricating a MOS transistor,” as recited in 1[pre], and “[a] method of fabricating a CMOS transistor,” as recited in 10[pre].

303. Wang753 discloses a method of making a semiconductor structure that “combines the formation of PMOS and NMOS devices for core circuits and SRAM cells.” (Wang753 at 3:33-36, 3:43-49, FIGS. 2-13.) Wang753’s PMOS and NMOS transistors have the same basic arrangement as in the ’194 Patent. For example, both include the same basic arrangement of gate, spacers, source/drain epitaxy layers, lightly doped regions, and substrate.



Wang753, FIG. 13



'194 Patent, Fig. 5

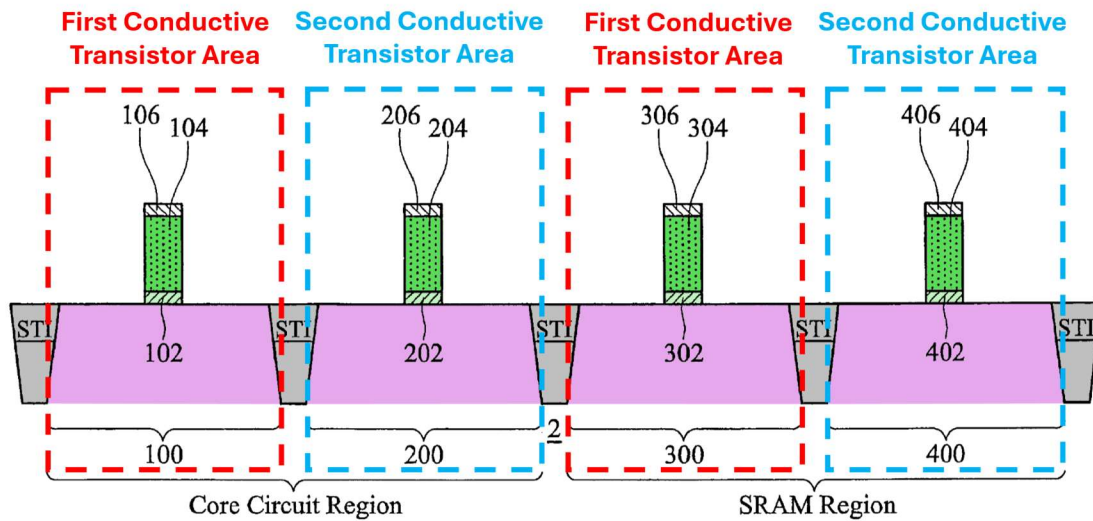
- b. 1[a]/10[a]: “providing a semiconductor substrate [having at least a first conductive transistor area for fabricating first conductive transistors and at least a second conductive transistor area for fabricating second conductive transistors, and an isolation structure between the first conductive transistor area and the second conductive transistor area]”

304. Wang753 discloses both “providing a semiconductor substrate,” as recited in 1[a], and “providing a semiconductor substrate having at least a first

conductive transistor area for fabricating first conductive transistors and at least a second conductive transistor area for fabricating second conductive transistors, and an isolation structure between the first conductive transistor area and the second conductive transistor area,” as recited in 10[a].

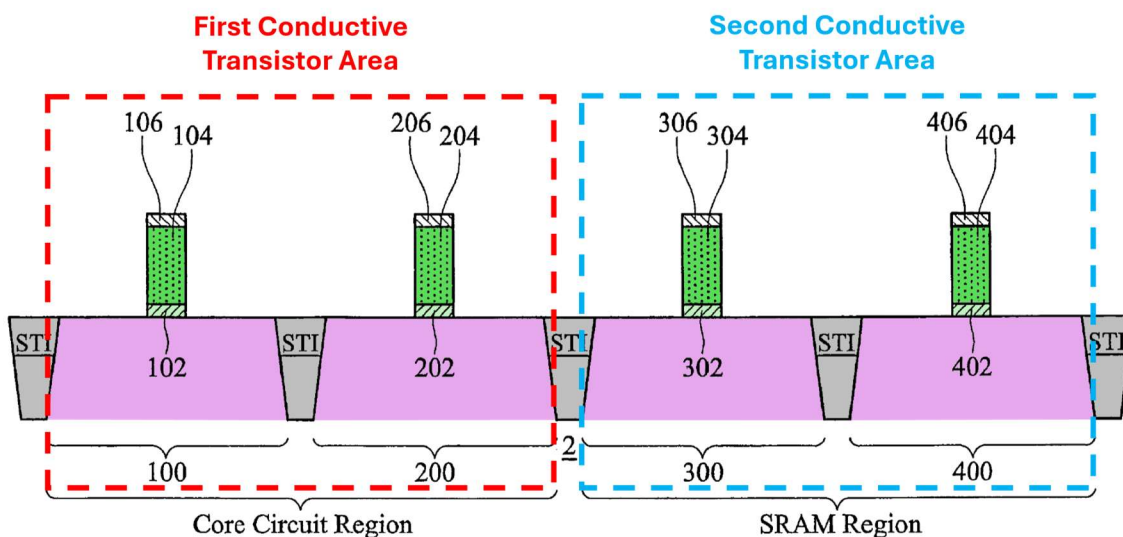
305. Wang753 discloses that “[s]ubstrate 2 preferably comprises bulk silicon,” which was a well-known semiconductor substrate. (Wang753 at 3:41-43.) Additionally, Wang753’s substrate 2 includes first and second conductive transistor areas: “[T]he core circuit region further includes an active region 100 for forming a PMOS device and an active region 200 for forming an NMOS device. The SRAM region further includes an active region 300 for forming a pull-up PMOS device and an active region 400 for forming pull-down and pass-gate NMOS devices.” (Wang753 at 3:43-49.) Wang753 further explains that these transistor areas are “isolated by shallow trench isolation (STI) regions [gray].” (Wang753 at 3:39-41.)

306. I have analyzed claim 10 under two alternative mappings of the “first conductive transistor area” and the “second conductive transistor area.” First, I map the “first conductive transistor area” to PMOS active areas 100 and/or 300 and the “second conductive transistor area” to NMOS active areas 200 and/or 400. Each area is isolated by STI regions (gray). The annotated figure below illustrates this first mapping of claim 10.



Wang753, FIG. 2

307. I have also analyzed claim 10 by mapping the “first conductive transistor area” to core active areas 100 and 200 and the “second conductive transistor area” to SRAM active areas 300 and 400. Each area is again isolated by STI regions (gray). The annotated figure below illustrates this second mapping of claim 10.



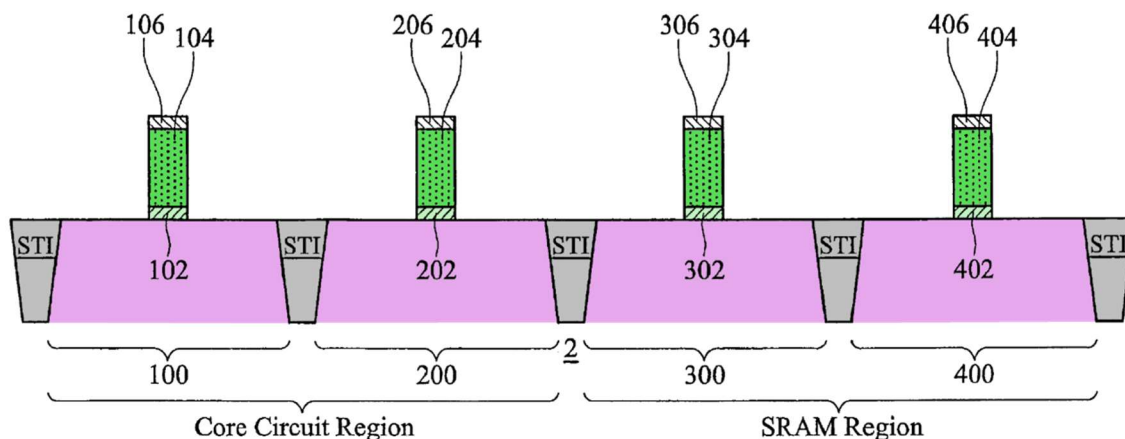
Wang753, FIG. 2

308. Both mappings apply to claims 10-16 and 21, because PMOS region 100 and/or 300 is included within the “first conductive transistor area” in both cases. For claim 22, as discussed below, I apply only the second mapping.

c. 1[b]/10[b]: “forming [at least a / a] gate on the [semiconductor substrate / first conductive transistor area and on the second conductive transistor area respectively];”

309. Wang753 discloses both “forming at least a gate on the semiconductor substrate,” as recited in 1[b], and “forming a gate on the first conductive transistor area and on the second conductive transistor area respectively,” as recited in 10[b].

310. Each of Wang753’s devices includes “a gate stack formed on the substrate 2.” (Wang753 at 3:49-55.) As FIG. 2 shows below, each MOSFET structure comprises “a gate dielectric 102[/202/302/402] on substrate 2 and a gate electrode 104[204/304/404] on gate dielectric 102[/202/302/402].” (Wang753 at 3:49-59.) Wang753 therefore discloses gates (e.g., Wang753’s “gate stack[s]” comprising gate dielectrics 102/202/302/402 and gate electrodes 104/204/304/404) formed on the first and second conductive transistor areas of silicon substrate 2 (as identified under the mappings of Section IX.D.1.b above).

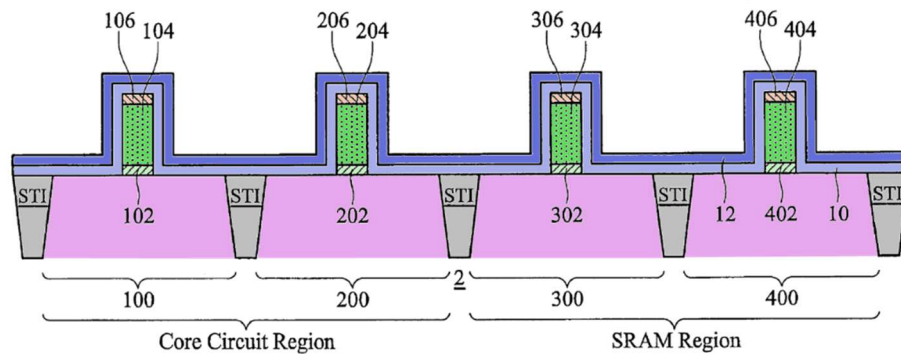


Wang753, FIG. 2

- d. 1[c]/10[c]: “forming a [first] protective layer on the semiconductor substrate, and the [first] protective layer covering the surface of [the/each] gate;”

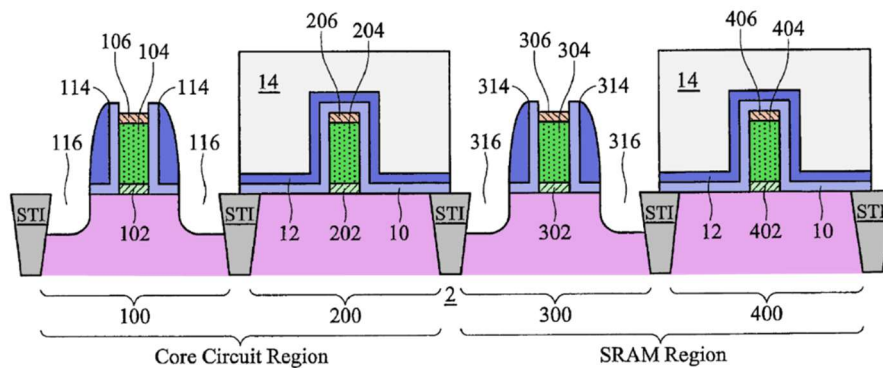
311. Wang753 discloses both “forming a protective layer on the semiconductor substrate, and the protective layer covering the surface of the gate,” as recited in 1[c], and “forming a first protective layer on the semiconductor substrate, and the first protective layer covering the surface of each gate,” as recited in 10[c].

312. In Wang753, “[a] dummy layer, which is used to form spacers, is formed over the core circuit region and the SRAM region, as shown in FIG. 3.” (Wang753 at 3:60-63.) This dummy layer “may include single or composite layers,” and, as shown below, it “comprises a liner oxide layer 10 [light blue] and a nitride layer 12 [dark blue].” (Wang753 at 3:62-4:3.)



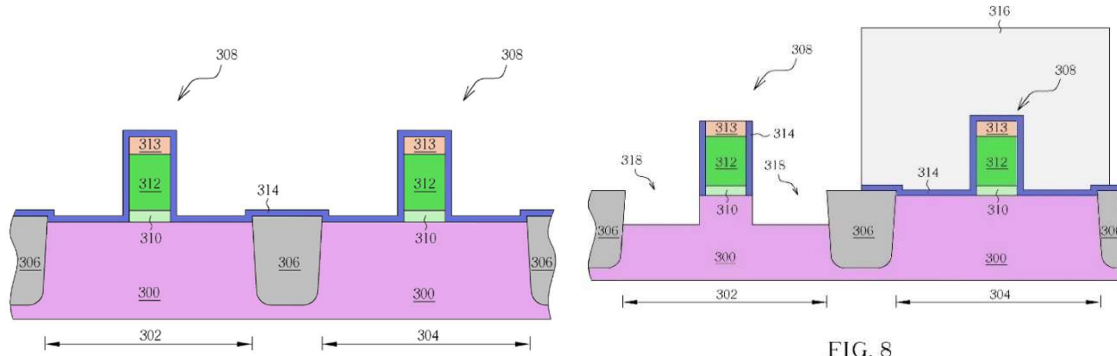
Wang753, FIG. 3

313. Consistent with the descriptions of the protective layer in the '194 Patent (e.g., at 3:28-44 & FIG. 2, 5:16-32 & FIG. 8), Wang753's dummy layer is a protective layer because it provides etch selectivity relative to the substrate, thereby protecting the gate during PMOS source/drain recess etching. (Wang753 at 4:4-13, FIG. 4.) As shown below, "FIG. 4 illustrates the liner oxide layer 10 and nitride layer 12 in PMOS regions 100 and 300 being patterned to form gate spacers 114 and 314, respectively. . . . Recesses 116 and 316 are formed along the outside edges of the spacers 114 and 314, respectively, preferably by etching isotropically and/or anisotropically." (Wang753 at 4:4-13.)



Wang753, FIG. 4

314. The '194 patent discloses essentially the same method of forming a protective layer 314 and recesses 318, for example. ('194 Patent at 5:16-32.)



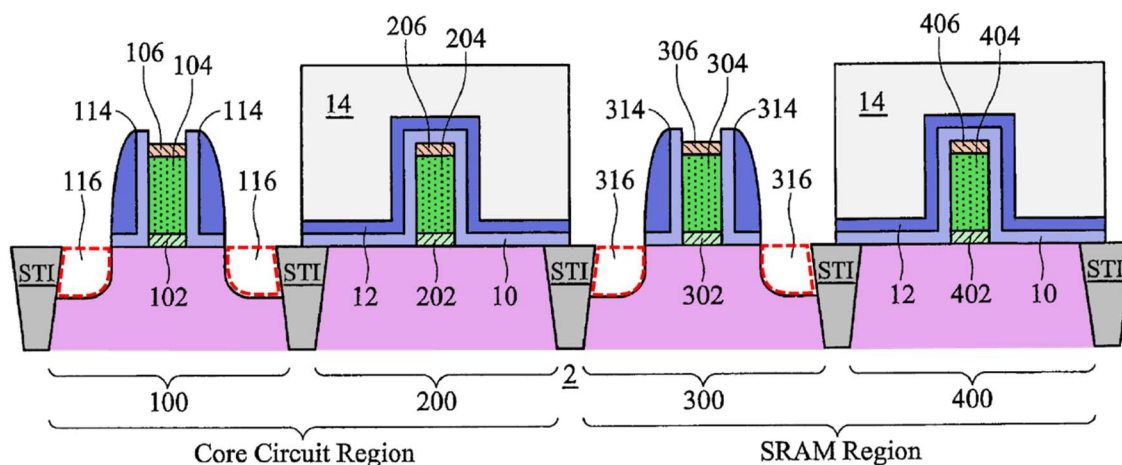
'194 Patent, FIG. 7

'194 Patent, FIG. 8

- e. **1[d]/10[d]: “forming at least a [first] recess within the semiconductor substrate adjacent to the gate [in the first conductive transistor area];”**

315. Wang753 discloses both “forming at least a recess within the semiconductor substrate adjacent to the gate,” as recited in 1[d], and “forming at least a first recess within the semiconductor substrate adjacent to the gate in the first conductive transistor area,” as recited in 10[d].

316. The substrate in Wang753 is subsequently etched to form recesses, as FIG. 4 shows below. Wang753 explains: “Recesses 116 and 316 are formed along the outside edges of the spacers 114 and 314, respectively, preferably by etching isotropically and/or anisotropically.” (Wang753, 4:10-13.) These recesses 116 and 316 are adjacent to the gate, being offset by a distance set by the thickness of spacers 114 and 314, respectively.

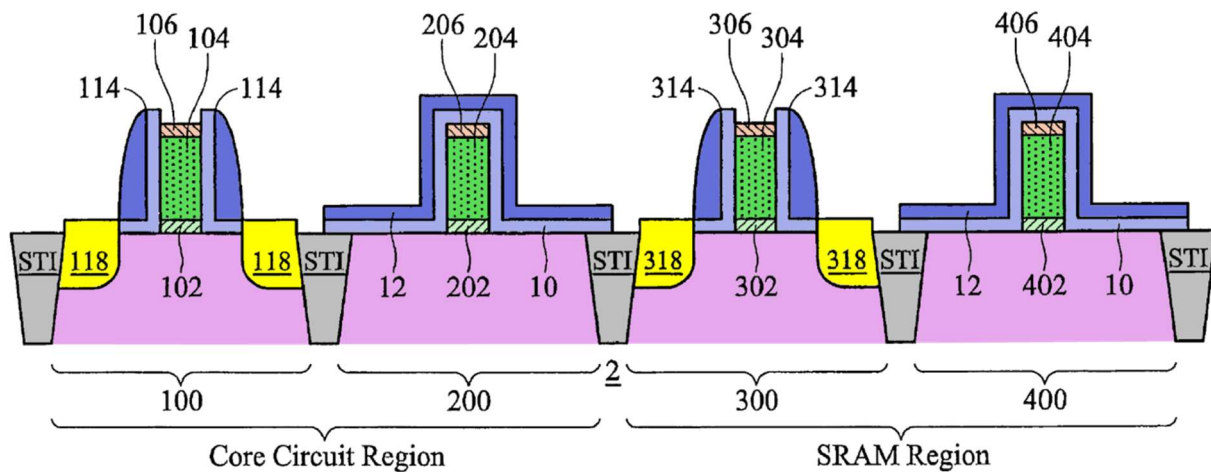


Wang753, FIG. 4

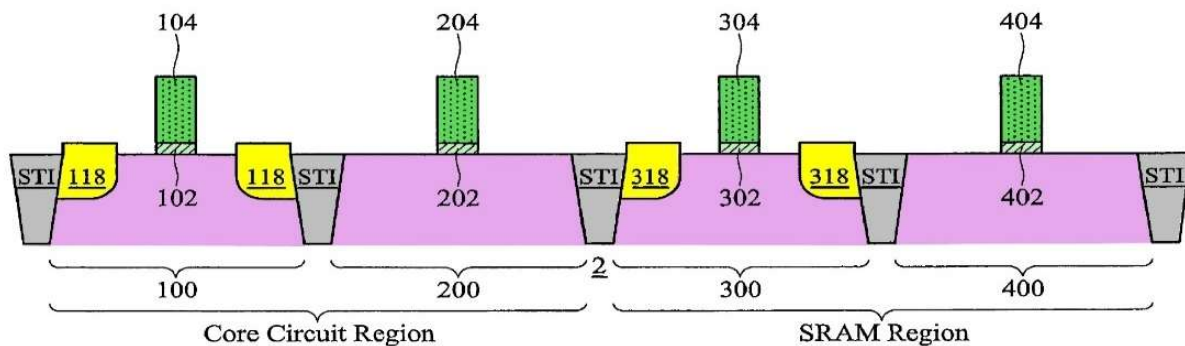
- f. 1[e]/10[e]: “forming [an/a first] epitaxial layer in the [first] recess, wherein the top surface of the [first] epitaxial layer is above the surface of the semiconductor substrate; and”

317. Wang753 discloses both “forming an epitaxial layer in the recess, wherein the top surface of the epitaxial layer is above the surface of the semiconductor substrate,” as recited in 1[e], and “forming a first epitaxial layer in the first recess, wherein the top surface of the first epitaxial layer is above the surface of the semiconductor substrate,” as recited in 10[e].

318. Wang753’s process includes growing epitaxial layers in recesses 116 and 316. Wang753 explains: “FIG. 5 illustrates the formation of SiGe stressors 118 and 318 in recesses 116 and 316, respectively. It is preferred that the SiGe stressors be epitaxially grown in the recesses 116 and 316.” (Wang753 at 4:14-17.)

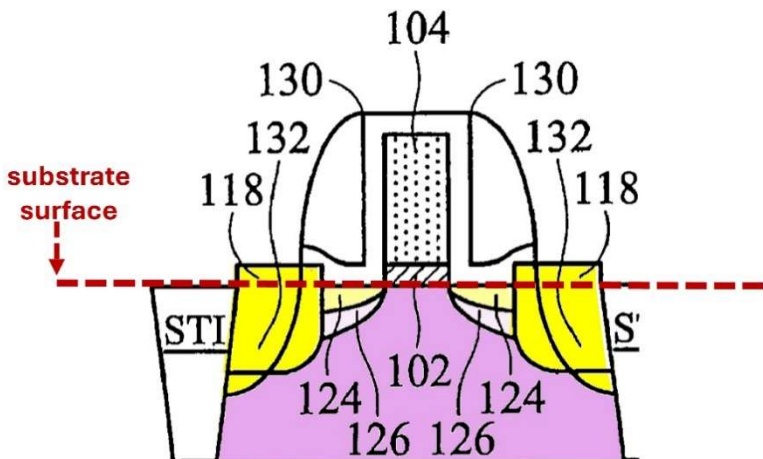


Wang753, FIG. 5



Wang753, FIG. 6

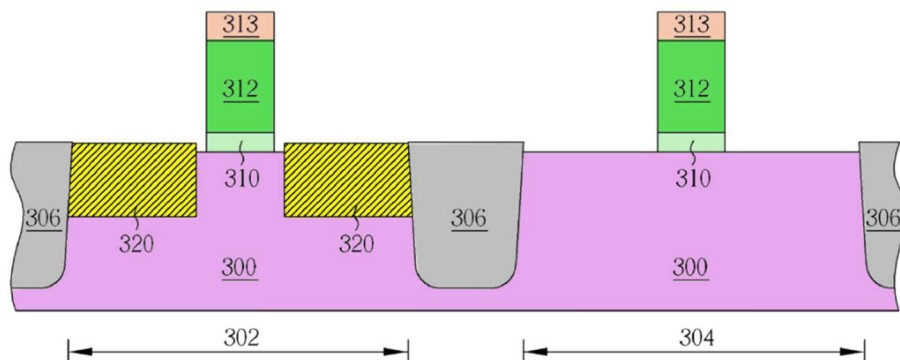
319. I have been informed that patent drawings may be useful in shedding light about the general shapes and relative sizes of elements of the claimed invention, as well as their spatial relations to one another. As Wang753's FIGS. 5 and 6 show above and the excerpt of FIG. 13 shows below, a person of ordinary skill in the art would have understood (Ground 2A), and at least found obvious (Ground 2B), that SiGe stressors 118 and 318 extend above the semiconductor substrate's surface. (Wang753 at 4:14-22.)



Wang753, FIG. 13 (excerpted & annotated)

320. Moreover, a person of ordinary skill in the art would have understood that such raised epitaxial source/drain layers were well-known in the art—including in two generations of commercial MOSFETs before the '194 Patent—and commonly used to improve carrier mobility in the silicon channel region and to reduce source/drain contact resistance. (*See* Section VI.B above; Ghani at 978, Figs. 1-4; Wang⁹⁰⁶ ¶¶[0030]-[0032], FIG. 9; Bohr at FIGS. 4-7; Kavalieros at Abstract, ¶¶[0025], ¶¶[0043], FIGS. 5, 13; James at 2.)

321. The '194 Patent similarly discloses epitaxial layers 320 grown “higher than the surface of the semiconductor substrate 300.” ('194 Patent at 5:33-42.)

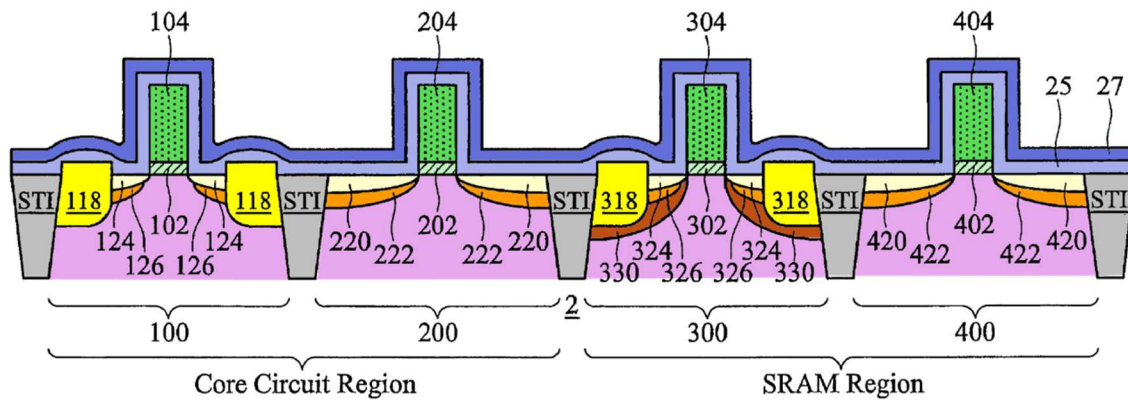


'194 Patent, FIG. 9

- g. 1[f]/10[f]: “forming a spacer on the sidewall of [the/each] gate and [at least] on a portion of the [first] epitaxial layer[,] wherein a contact surface of the [first] epitaxial layer and the spacer is above the surface of the semiconductor substrate.”

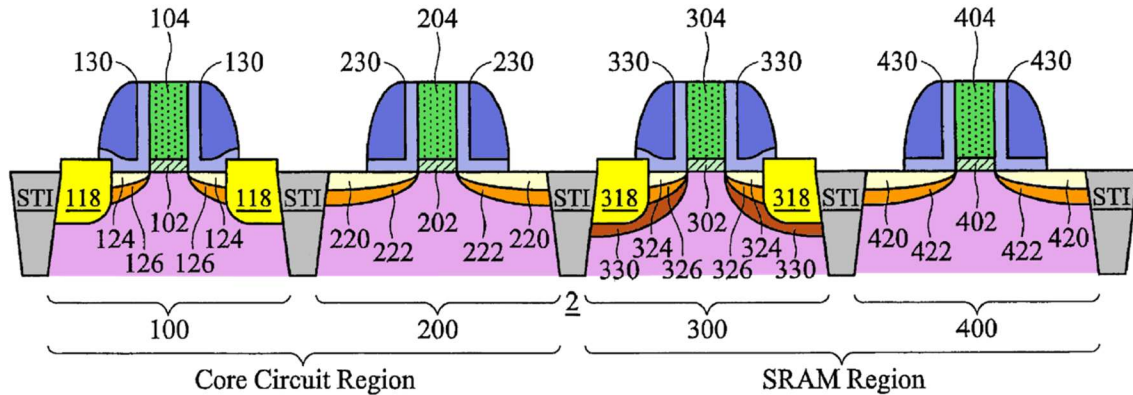
322. Wang753 discloses both “forming a spacer on the sidewall of the gate and on a portion of the epitaxial layer wherein a contact surface of the epitaxial layer and the spacer is above the surface of the semiconductor substrate,” as recited in 1[f], and “forming a spacer on the sidewall of each gate and at least on a portion of the first epitaxial layer, wherein a contact surface of the first epitaxial layer and the spacer is above the surface of the semiconductor substrate,” as recited in 10[f].

323. Wang753 discloses “a liner oxide layer 25 and a nitride layer 27 [that] are blanket formed” on the PMOS device, as FIG. 10 shows below. (Wang753 at 5:19-21, FIG. 10.)



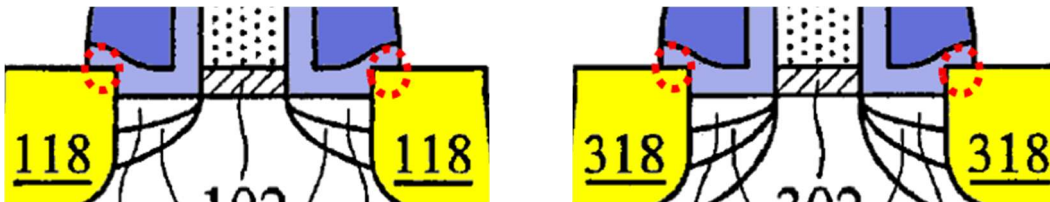
Wang753, FIG. 10

324. Next, Wang753 explains that “[t]he two layers are then patterned to form spacers 130, 230, 330, and 430, as shown in FIG. 11” below. (Wang753 at 5:21-22.) Spacers 130 are thicker than the dummy spacers 114 that were used to set the distance between the gate and SiGe stressors 118. (Wang753 at 5:22-25). “As a result, spacers 130 and 330 have portions on SiGe stressors 118 and 318, respectively.” (Wang753 at 5:25-27.) Wang753’s spacers 130 are thus formed on portions of SiGe stressors 118. (Wang753 at 5:19-27, FIGS. 6-13.) As Wang753’s FIG. 13 below confirms, spacers 130 and SiGe stressors 118 intersect at a contact surface above the substrate surface.



Wang753, FIG. 11

325. Below, close-up excerpts of FIG. 13 show the core and SRAM PMOS devices. The red circles indicate the contact surfaces between spacers 130/330 and epitaxial SiGe stressors 118/318, which are raised above the substrate surface.



Wang753, FIG. 11 (excerpted & annotated))

2. Dependent Claims

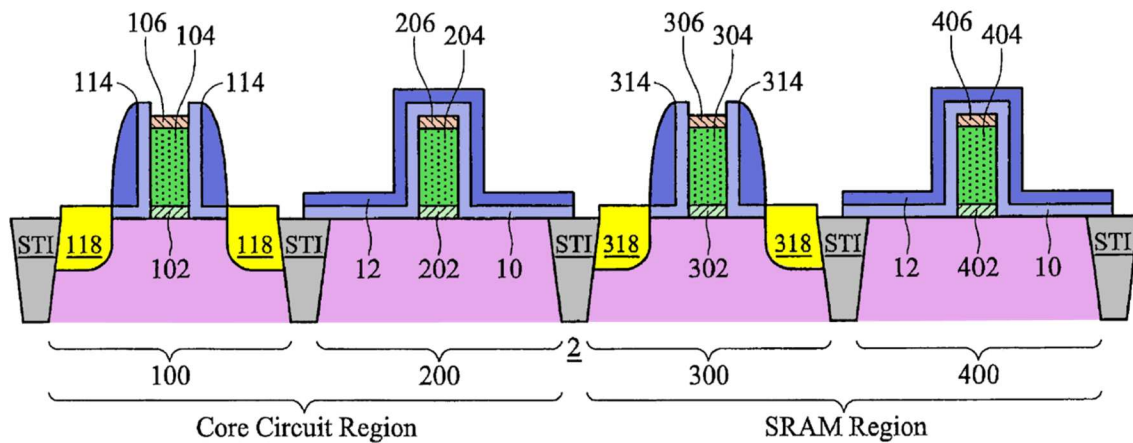
- a. **Claims 2/16:** “The method of claim [1/10], further comprising a step of removing the [first] protective layer after forming the [first] epitaxial layer in the [first] recess.

326. As I explain in Section IX.D.1, Wang753 discloses and renders obvious the methods of claims 1 and 10.

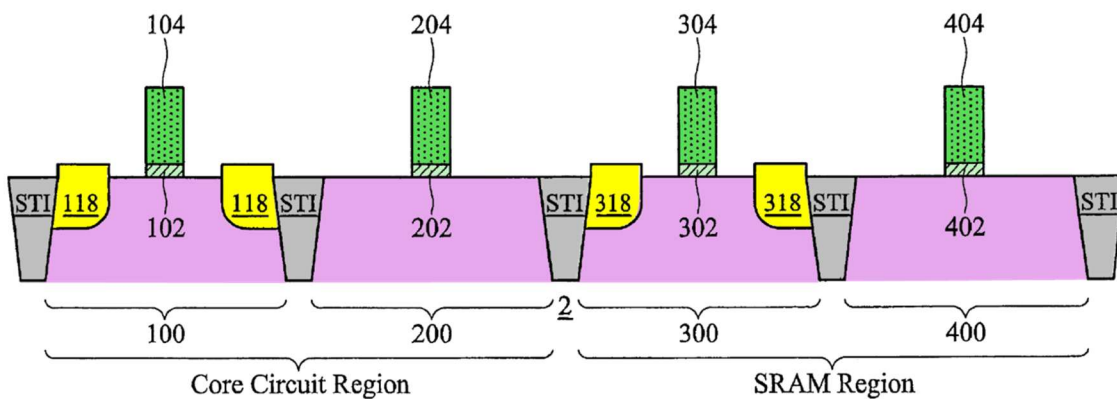
327. Wang753 also discloses both “further comprising a step of removing the protective layer after forming the epitaxial layer in the recess,” as recited in

claim 2 and “further comprising a step of removing the first protective layer after forming the first epitaxial layer in the first recess,” as recited in claim 16.

328. In Wang753, “spacers 114 and 314, liner oxide layer 10, silicon nitride layer 12 and hard masks 106, 206, 306 and 406 are removed,” as in FIG. 6, after the first epitaxial layer is formed in the first recess. (Wang753 at 4:23-25.)



Wang753, FIG. 5 (before removal)



Wang753, FIG. 6 (after removal)

329. This is like the '194 Patent, which discloses essentially the same step of removing protective layer 314. ('194 Patent at 5:38-39.)

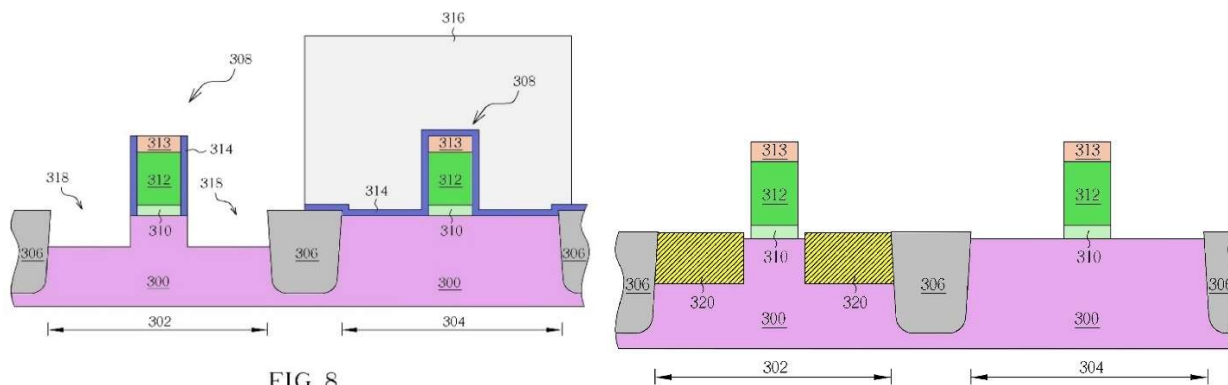


FIG. 8

'194 Patent, FIG. 8 (before removal)

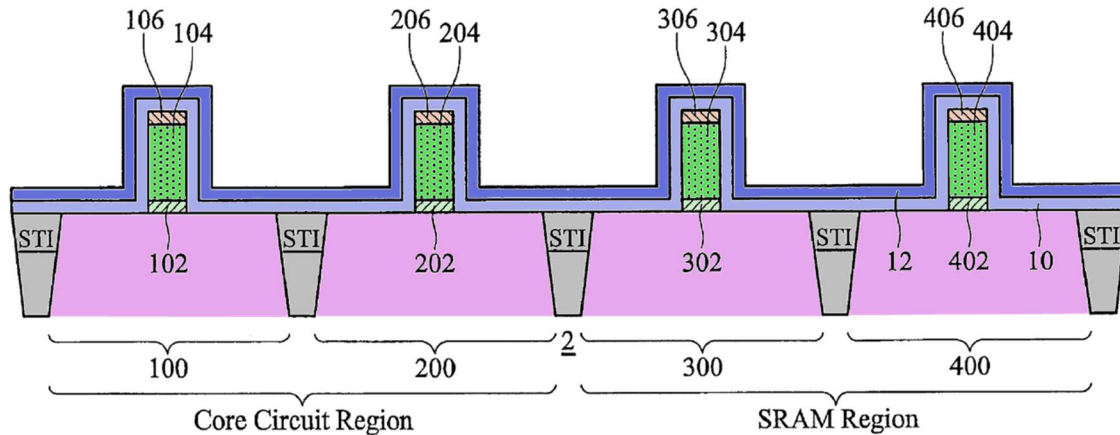
'194 Patent, FIG. 9 (after removal)

b. Claims 3/12: “The method of claim [1/10], wherein the [first] protective layer comprises silicon nitride.”

330. As I explain in Section IX.D.1, Wang753 discloses and renders obvious the methods of claims 1 and 10.

331. Wang753 also discloses both “wherein the protective layer comprises silicon nitride,” as recited in claim 3, and “wherein the first protective layer comprises silicon nitride,” as recited in claim 12.

332. Wang753 states that “[a] dummy layer, which is used to form spacers, is formed over the core circuit region and the SRAM region, as shown in FIG. 3. In the preferred embodiment, the dummy layer comprises a liner oxide layer 10 and *a nitride layer 12*. In alternative embodiments, the dummy layer may include single or composite layers comprising oxide, *silicon nitride*, silicon oxynitride (SiON) and/or other dielectric materials.” (Wang753 at 3:60-66 (emphasis added).) The dummy layer in Wang753 thus comprises silicon nitride, as claimed.



Wang753, FIG. 3

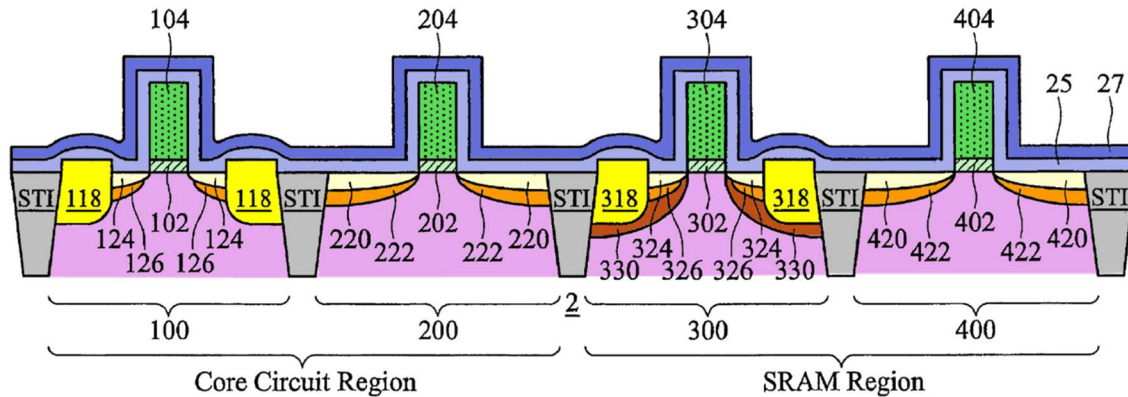
- c. **Claim 5/14: “The method of claim [1/10], wherein [the/each] spacer further comprises an oxide liner and a nitride spacer.”**

333. As I explain in Section IX.D.1, Wang753 discloses and renders obvious the methods of claims 1 and 10.

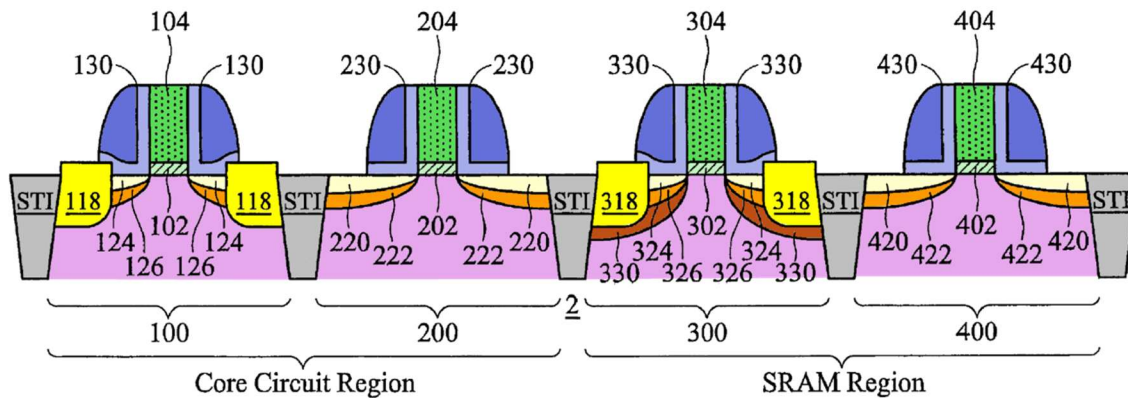
334. Wang753 also discloses and renders obvious both “wherein the spacer further comprises an oxide liner and a nitride spacer,” as recited in claim 5, and “wherein each spacer further comprises an oxide liner and a nitride spacer,” as recited in claim 14.

335. Like the “dummy layer” I describe above, Wang753 discloses that its spacer structure comprises an oxide liner and nitride spacer: “FIGS. 10 and 11 illustrate the formation of spacers. Referring to FIG. 10, *a liner oxide layer 25* and *a nitride layer 27* are blanket formed. The two layers are *then patterned to form*

spacers 130, 230, 330 and 430, as shown in FIG. 11.” (Wang753 at 5:19-22 (emphases added).)



Wang753, FIG. 10



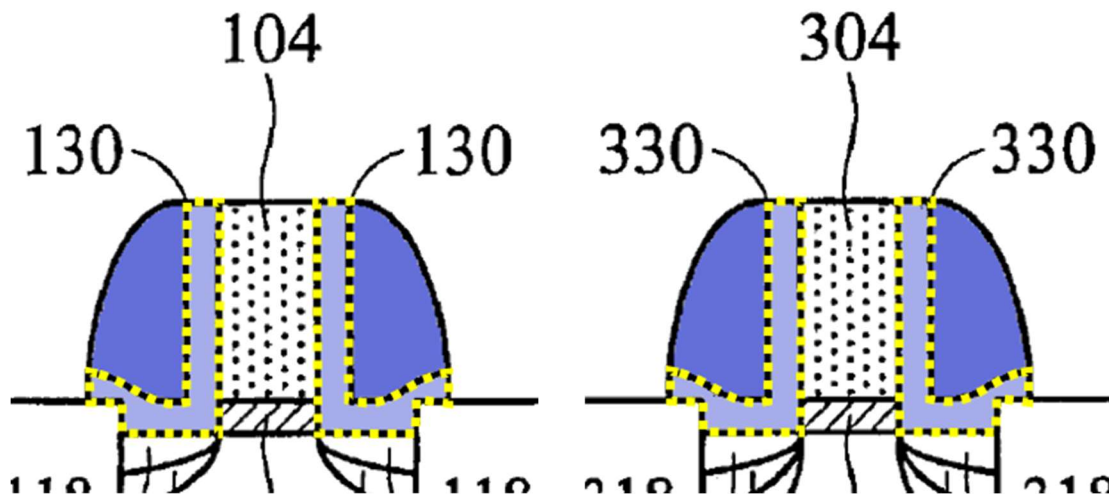
Wang753, FIG. 11

- d. **Claim 6/15:** “The method of claim [1/10], wherein [the/each] spacer further comprises an offset spacer, positioned between [the/each] gate and [the/each] spacer.”

336. As I explain in Section IX.D.1 Wang753 discloses and renders obvious the methods of claims 1 and 10.

337. For the reasons I explain in section VII.C, here I analyze claims 6 and 15 assuming that the claim can be satisfied if one layer (an “offset spacer”) of the claimed “spacer” lies between another layer of the claimed “spacer” and the claimed “gate.” Under such an interpretation, Wang753 also discloses both “wherein the spacer further comprises an offset spacer, positioned between the gate and the spacer,” as recited in claim 6, and “wherein each spacer further comprises an offset spacer, positioned between each gate and each spacer,” as recited in claim 15.

338. Specifically, Wang753 explains: “FIGS. 10 and 11 illustrate the formation of spacers. Referring to FIG. 10, a liner oxide layer 25 and a nitride layer 27 are blanket formed. The two layers are then patterned to form spacers 130, 230, 330 and 430, as shown in FIG. 11.” (Wang753 at 5:19-22.) I have circled the “offset” layer of the claimed spacer in yellow below:



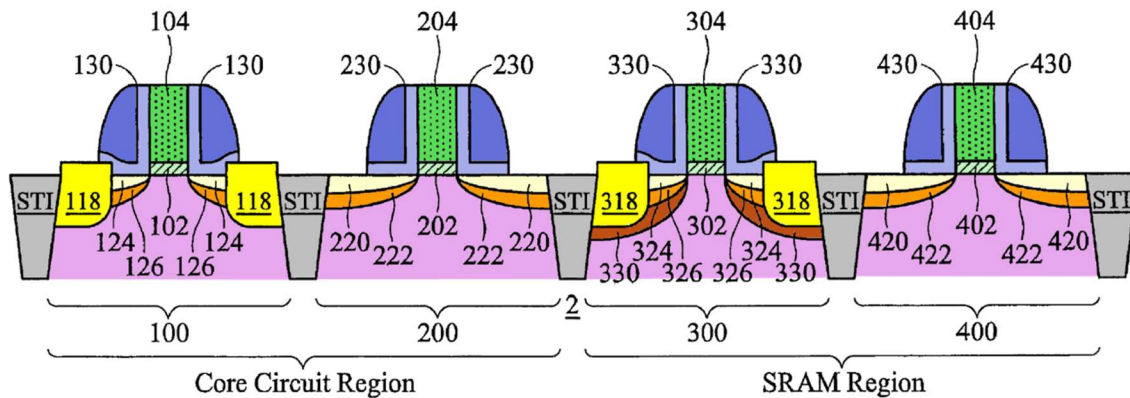
Wang753, FIG. 11 (excerpted & annotated)

- e. **Claim 7: The method of claim 1, further comprising a step of forming a source/drain region within the semiconductor substrate adjacent to the gate after forming the spacer.**

339. As I explain in Section IX.D.1, Wang753 discloses and renders obvious the method of claim 1.

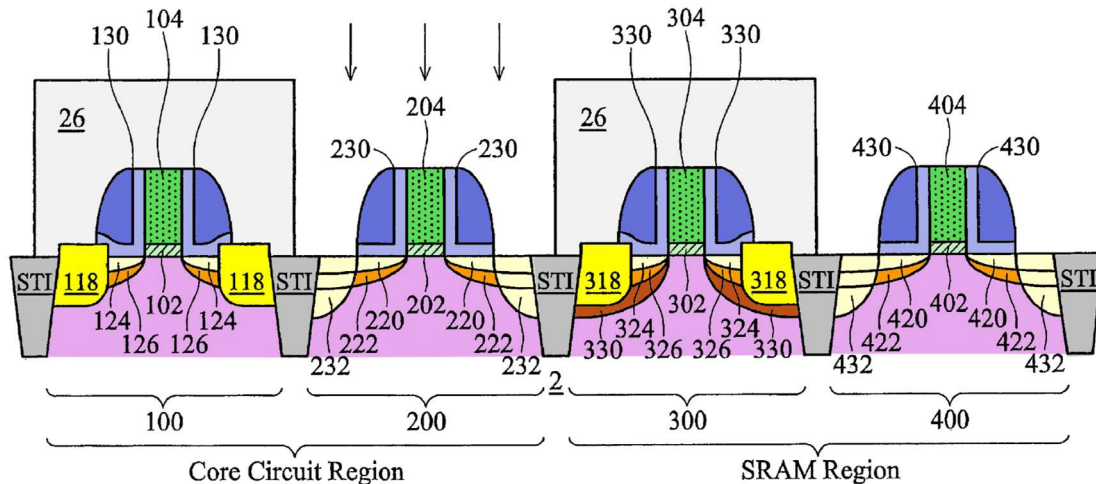
340. Wang753 also discloses “a step of forming a source/drain region within the semiconductor substrate adjacent to the gate after forming the spacer,” as recited in claim 7.

341. In Wang753, the source/drain regions are formed after removing the protective layer (dummy layer) and forming spacers 130/230/330/430. FIG. 11 shows a stage of fabrication in which the spacers have been formed.



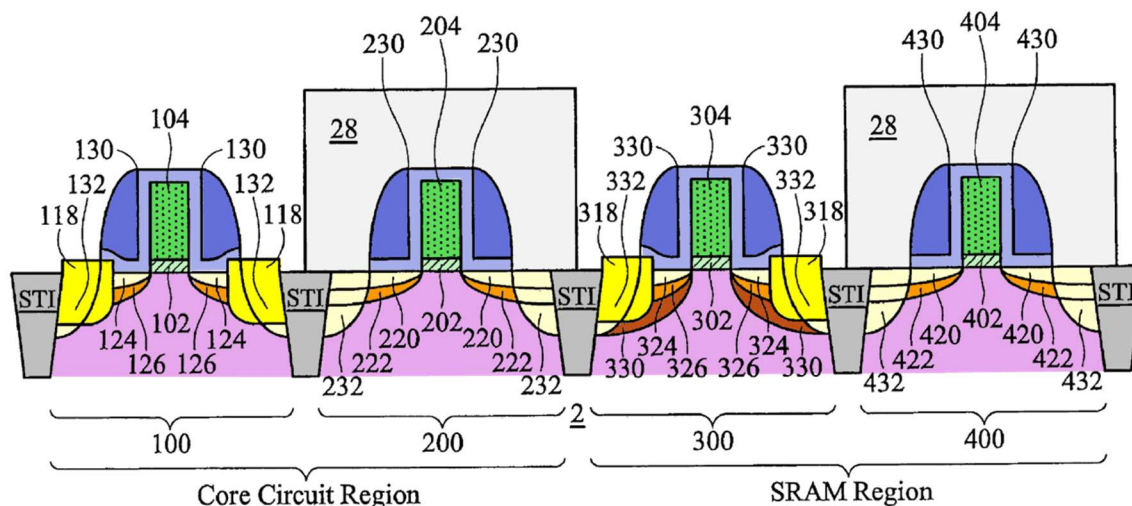
Wang753, FIG. 11 (before further ion implantation)

342. Wang753 then discloses further NMOS ion implantation in active regions 200 and 400: “FIG. 12 illustrates the formation of deep source/drain regions 232 and 432 in core NMOS region 200 and SRAM NMOS region 400, respectively, preferably by implanting n-type impurities. During the implantation, PMOS regions 100 and 300 are masked by a photo resist 26. The resulting source/drain regions 232 and 432 are substantially aligned with edges of the spacers 230 and 430, respectively” and thus also the gate. (Wang753 at 5:28-35.) Accordingly, Wang753 discloses a step of forming a source/drain region (e.g., deep source/drain regions 232 and/or 432) within the substrate adjacent to the gate after forming spacer 230 and/or 430.



Wang753, FIG. 12 (after further NMOS ion implantation)

343. Wang753 then discloses further PMOS ion implantation in active regions 100 and 300: “FIG. 13 illustrates a similar process for forming deep source/drain regions for PMOS devices, preferably by implanting p-type impurities. A photo resist 28 is formed to mask core NMOS region 200 and SRAM NMOS region 400. The resulting deep source/drain regions 132 and 332 are substantially aligned with edges of the spacers 130 and 330, respectively,” and thus also the gate. (Wang753 at 5:36-42.) Accordingly, Wang753 discloses a step of forming a source/drain region (e.g., deep source/drain regions 132 and/or 332) within the substrate adjacent to the gate after forming spacer 130 and/or 330.



Wang753, FIG. 13 (after further PMOS ion implantation)

- f. **Claims 8/11: “The method of claim [1/10], further comprising a step of forming a [first] lightly doped region within the semiconductor substrate adjacent to the gate [in the first conductive transistor area].”**

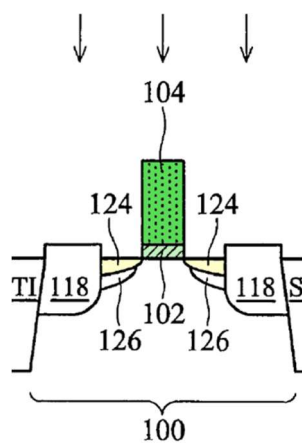
344. As I explain in Section IX.D.1, Wang753 discloses and renders obvious the methods of claims 1 and 10.

345. Wang753 also renders obvious both “a step of forming a lightly doped region within the semiconductor substrate adjacent to the gate,” as recited in claim 8, and “a step of forming a first lightly doped region within the semiconductor substrate adjacent to the gate in the first conductive transistor area,” as recited in claim 11.

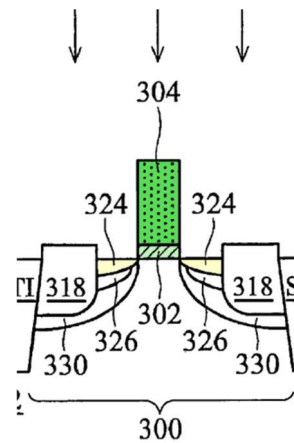
346. Wang753’s PMOS devices in core region 100 include source/drain regions with several components on both sides of the gate stack, such as SiGe stressors 118, LDD regions 124, and deep source/drain regions 132. (Wang753 at 4:14-22, 4:46-51, 5:36-42, FIG. 13.) Wang753 explains the following:

- SiGe stressors 118 are preferably doped with “P-type impurities such as boron . . . during epitaxial growth.” (Wang753 at 4:14-18; *see also* Wang753 at FIG. 5.)
- “LDD regions 124 are formed by introducing p-type impurities” into the substrate.” (Wang753 at 4:49-51; *see also* Wang753 at 4:29-37, 4:46-51, FIG. 8.)
- “[D]eep source/drain regions 132,” which are “substantially aligned with edges of the spacers 130,” are formed by “implanting p-type impurities.” (Wang753 at 5:36-42; *see also* Wang753 at FIG. 13.)

347. In FIG. 8, “LDD regions 124 are formed by introducing p-type impurities” into the substrate adjacent to the gate. (Wang753 at 4:46-51; *see also* Wang753 at 4:29-37.) In FIG. 9, “LDD regions 324 are the[n] formed by implanting p-type impurities” into the substrate adjacent to the gate. (Wang753 at 4:53-54.)

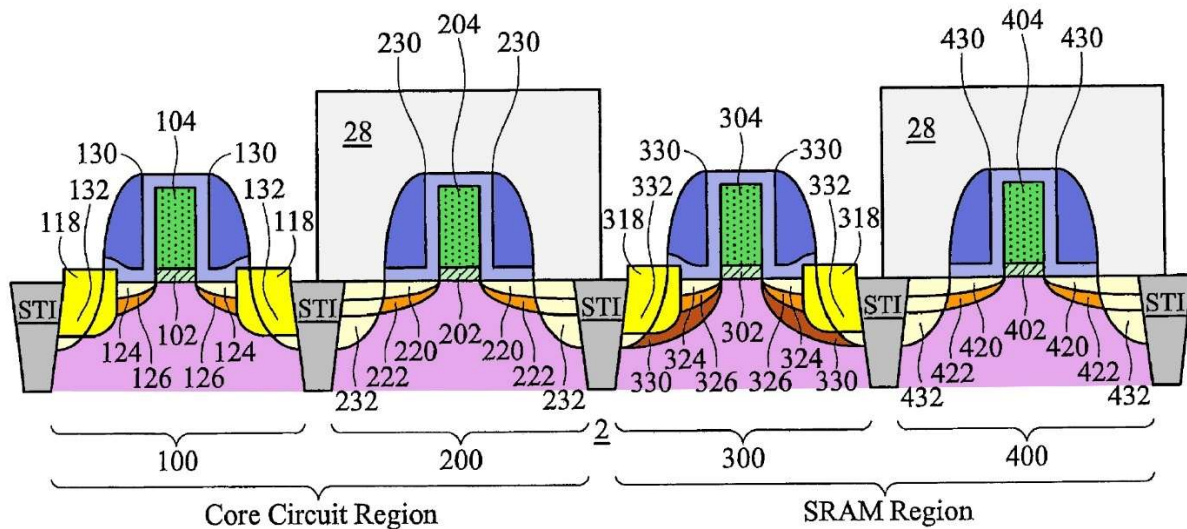


Wang753, FIG. 8 (excerpted)



Wang753, FIG. 9 (excerpted)

348. As FIG. 13 further shows below, Wang753's LDD regions 124 and 324, for example, lie next to the gate stack (light and dark green). They are also “substantially aligned with the edges of the gate electrodes.” (Wang753 at 4:34-36.)



Wang753, FIG. 13

g. Claim 9:

i. 9[pre] “The method of claim 1, further comprising:”

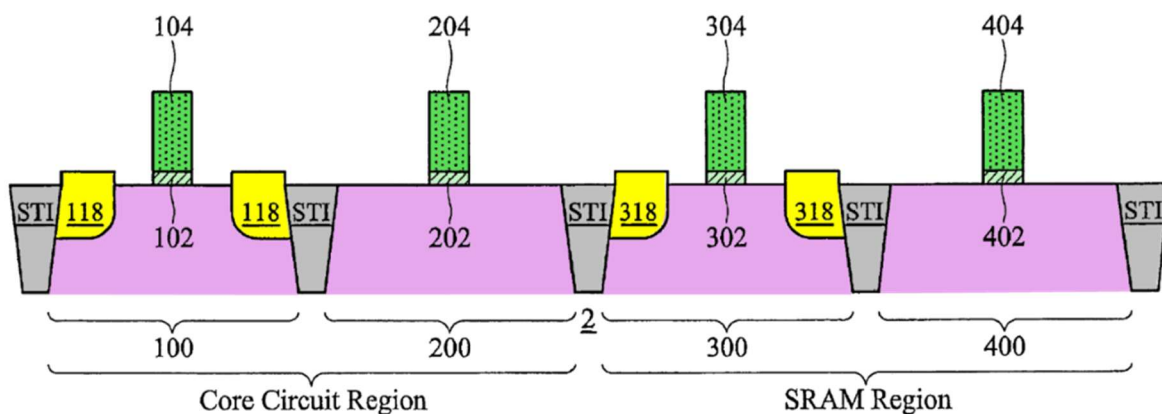
349. As I explain in Section IX.D.1, Wang753 discloses and renders obvious the method of claim 1.

ii. 9[a] “forming a lightly doped region in the semiconductor substrate adjacent to the gate after forming the epitaxial layer;”

350. As I explain in Section IX.D.2.f for claim 8, Wang753 discloses and renders obvious the formation of lightly doped regions adjacent to the gate.

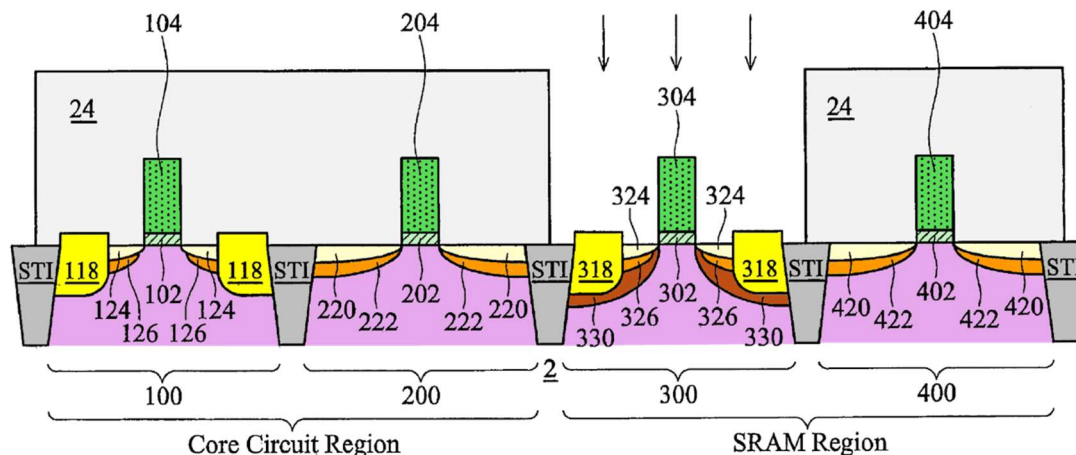
351. Wang753 also discloses and renders obvious “forming a lightly doped region in the semiconductor substrate adjacent to the gate after forming the epitaxial layer,” as recited in claim element 9[a].

352. Wang753’s LDD structures are formed after forming the SiGe epitaxial layers and removing the dummy spacers. “Referring to FIG. 6, spacers 114 and 314, liner oxide layer 10, silicon nitride layer 12 and hard masks 106, 206, 306 and 406 are removed.” (Wang753 at 4:23-26.) As FIG. 6 shows, epitaxial layers 118 and 318 have been formed already.



Wang753, FIG. 6

353. *Subsequently*, “FIGS. 7, 8 and 9 illustrate the formation of lightly doped drain/source (LDD) regions and halo regions for PMOS and NMOS devices.” (Wang753 at 4:30-32; *see also* Wang753 at 4:30-55.) As FIG. 9 shows below, LDD regions 124, 220, 324, and 440 are not formed until after SiGe epitaxial layers 118 and 318 have been formed.



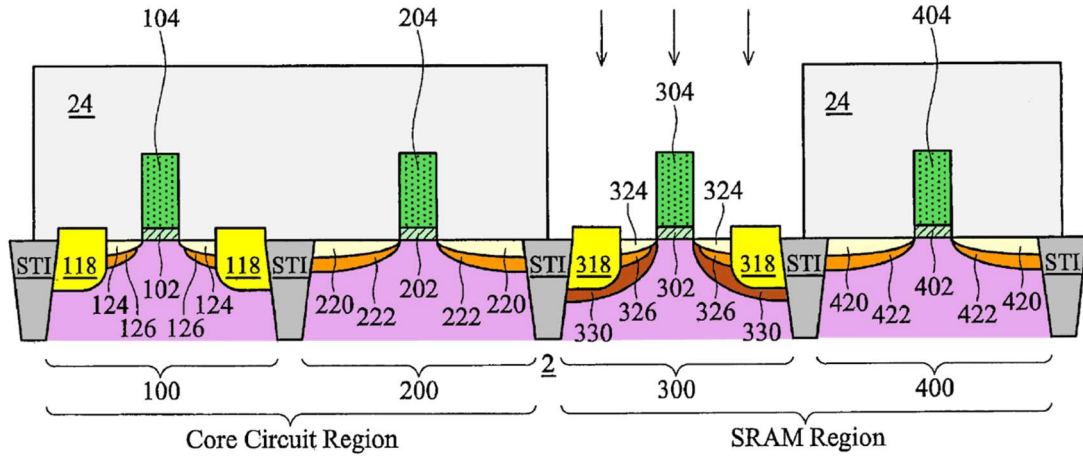
Wang753, FIG. 9

iii. 9[b] “forming the spacer on the sidewall of the gate and on the portion of the epitaxial layer after forming the lightly doped region; and”

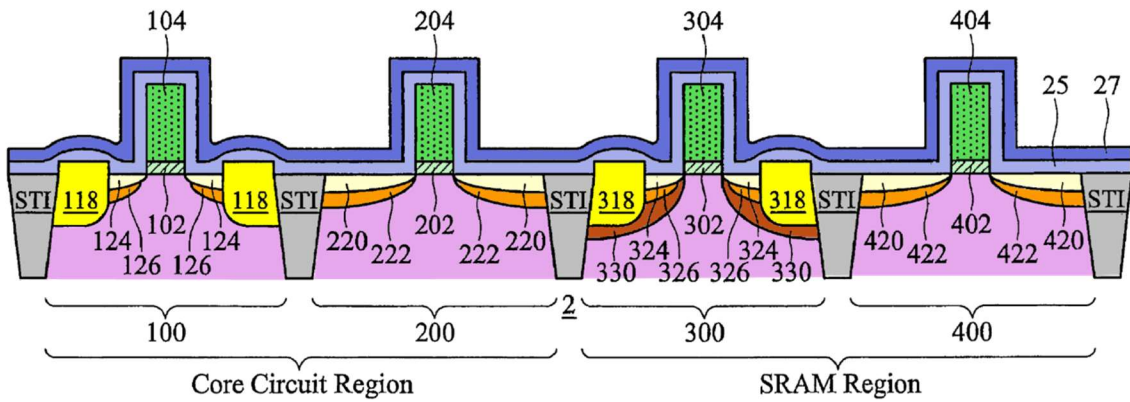
354. As I explain in Section IX.D.1.g for claim element 1[f], Wang753 discloses and renders obvious the formation of spacers on the sidewall of the gate and on the portion of the epitaxial layer.

355. Wang753 also discloses and renders obvious “forming the spacer on the sidewall of the gate and on the portion of the epitaxial layer after forming the lightly doped region,” as recited in claim element 9[b].

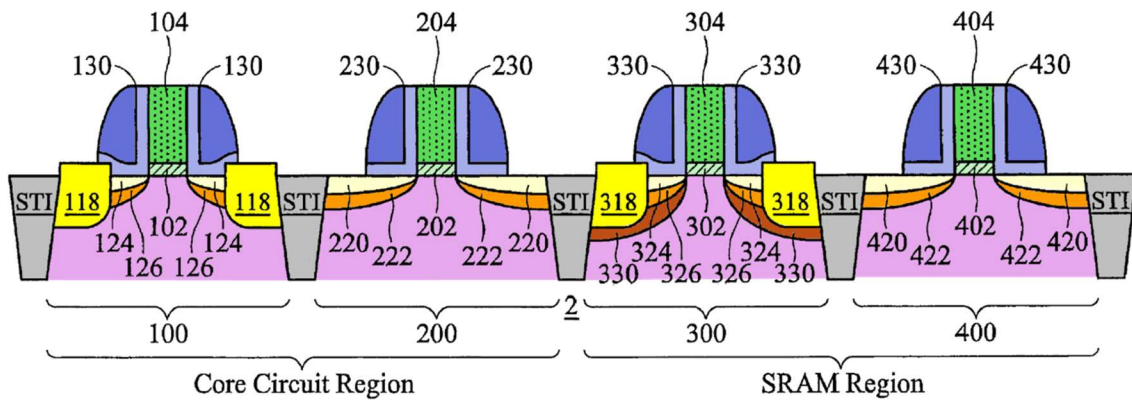
356. LDD regions 124, 220, 324, and 420 in Wang753 are formed as shown in FIGS. 7-9, which illustrates fabrications stages that take place before spacers 130/230/330/430 are formed, as shown in FIGS. 10-11. (See Wang753 at 4:30-5:2, FIGS. 7-9; *see also* Wang753 at 5:19-27, FIGS. 10-11.)



Wang753, FIG. 9



Wang753, FIG. 10



Wang753, FIG. 11

iv. 9[c] “forming a source/drain region in the semiconductor substrate adjacent to the spacer.”

357. As I explain in Section IX.D.2.e for claim 7, Wang753 discloses and renders obvious the formation of a source/drain region adjacent to the spacer. Wang753 also renders obvious “forming a source/drain region in the semiconductor substrate adjacent to the spacer,” as recited in claim element 9[c], for the same reasons.

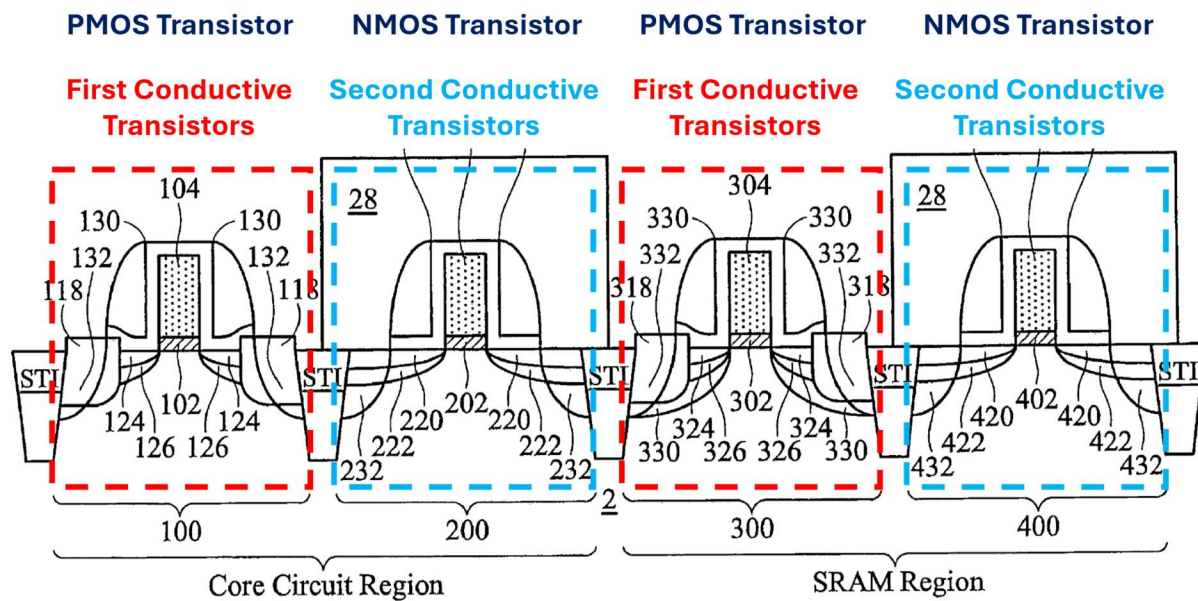
h. Claim 21: “The method of claim 10, wherein the first conductive transistors comprise PMOS transistors and the second conductive transistors comprise NMOS transistors.”

358. As I explain in Section IX.D.1, Wang753 discloses and renders obvious the method of claim 10.

359. Wang753 also discloses “wherein the first conductive transistors comprise PMOS transistors and the second conductive transistors comprise NMOS transistors,” as recited in claim 21.

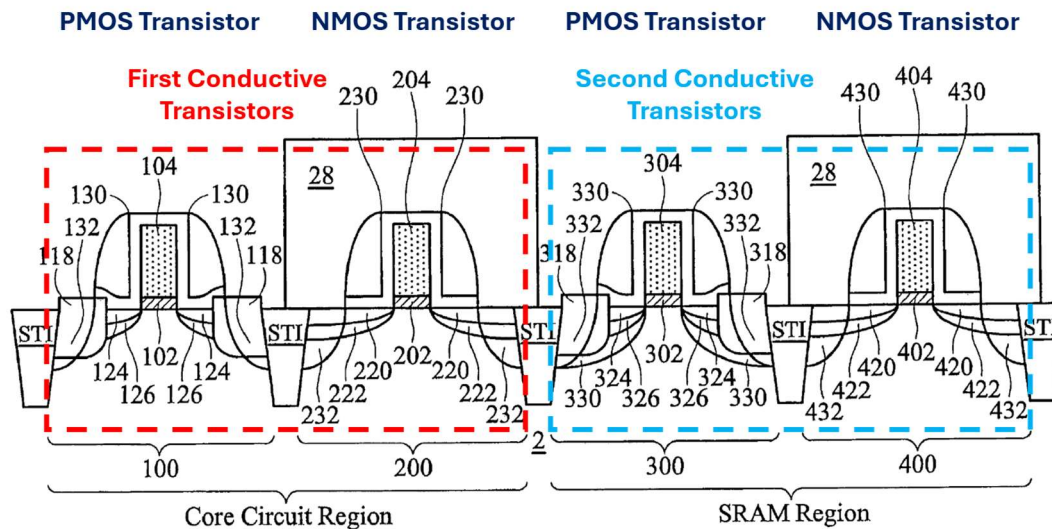
360. Wang753 discloses two pairs of active regions, including “an *active region 100* for forming *a PMOS device* and an *active region 200* for forming *an NMOS device*” and “an *active region 300* for forming a pull-up *PMOS device* and an *active region 400* for forming pull-down and pass-gate *NMOS devices*.” (Wang753 at 3:39-49 (emphases added).)

361. Wang753 thus discloses and renders obvious claim 21 under both of the mappings I describe above for claim element 10[a] in Section IX.D.1.b. Under the first mapping, the “first conductive transistors” are the PMOS transistors in active regions 100 and/or 300, and the “second conductive transistors” are the NMOS transistors in active regions 200 and/or 400:



Wang753, FIG. 13

362. Under the second mapping, the “first conductive transistors” are the PMOS and NMOS transistors in core active regions 100 and 200, and the “second conductive transistors” are the PMOS and NMOS transistors in SRAM active regions 300 and 400. Thus, the first conductive transistors include a PMOS transistor, and the second conductive transistors include an NMOS transistor:



Wang753, FIG. 13

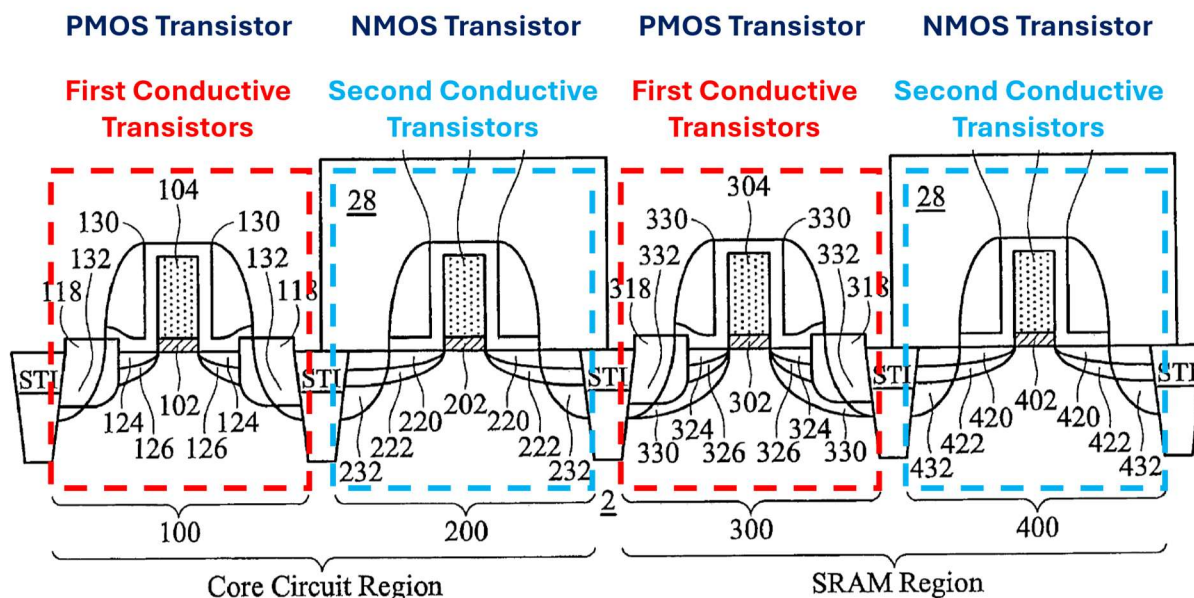
- i. **Claim 22:** “The method of claim 10, wherein the first conductive transistors comprise NMOS transistors and the second conductive transistors comprise PMOS transistors.”

363. As I explain in Section IX.D.1, Wang753 discloses and renders obvious the method of claim 10.

364. Wang753 also discloses “wherein the first conductive transistors comprise NMOS transistors and the second conductive transistors comprise PMOS transistors,” as recited in claim 22.

365. Wang753 discloses two pairs of active regions, including “an *active region 100* for forming a *PMOS device* and an *active region 200* for forming an *NMOS device*” and “an *active region 300* for forming a pull-up *PMOS device* and an *active region 400* for forming pull-down and pass-gate *NMOS devices*.” (Wang753 at 3:39-49 (emphases added).)

366. Wang753 thus discloses and renders obvious claim 22 under the second mapping I describe above for claim element 10[a] in Section IX.D.1.b. Under that mapping, the “first conductive transistors” are the PMOS and NMOS transistors in core active regions 100 and 200, and the “second conductive transistors” are the PMOS and NMOS transistors in SRAM active regions 300 and 400. Thus, the first conductive transistors include an NMOS transistor, and the second conductive transistors include a PMOS transistor:



Wang753, FIG. 13

E. Ground 2C: The Combined Teachings of Wang753 and Hoentschel262 Render Obvious Claims 4 and 13 (Ground 2C)

367. In my opinion, the combination of Wang753 and Hoentschel262 teaches, suggests, and renders obvious all the elements of claims 4 and 13 of the '194 Patent.

368. Hoentschel262, like Wang753, relates to a “technique that enables an increase of performance of PMOS transistors and NMOS transistors on the basis of strained layers in an efficient manner.” (Hoentschel262 at 2:66-3:2.) As shown in Hoentschel262’s FIG. 2i, Hoentschel262 describes a similar device with largely the same structures as Wang753, including “a first transistor 250p and a second transistor 250n.” (Hoentschel262 at 12:24-27.) Transistor 250p is a PMOS device with “a strained semiconductor material 214p [formed] in [a] recess 211p,” which is an epitaxially grown SiGe layer with “any desired degree of . . . overfilling” relative to the substrate surface. (Hoentschel262 at 13:21-30; *see also* Hontschel262 at FIG. 2d.) Further, transistor 250p uses a disposable or sacrificial dummy spacer 206 to define the location of recess 211p. (Hoentschel262 at 12:32-13:20, FIG. 2c.)

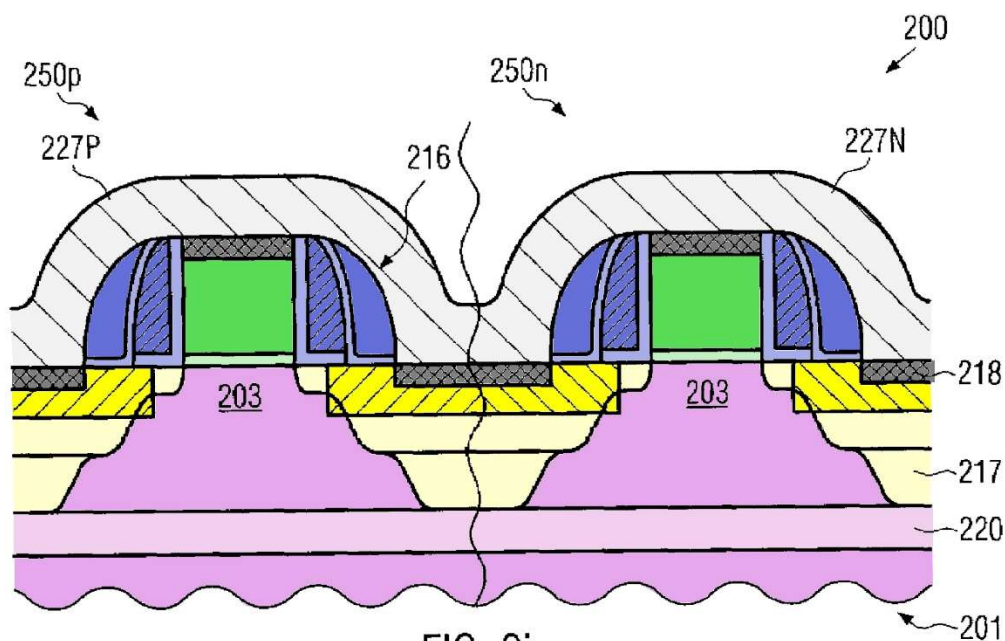
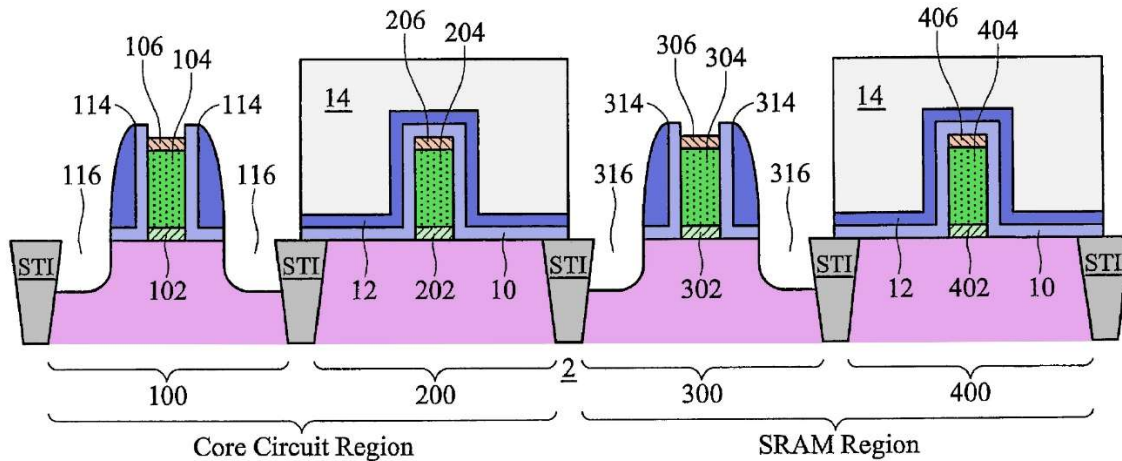


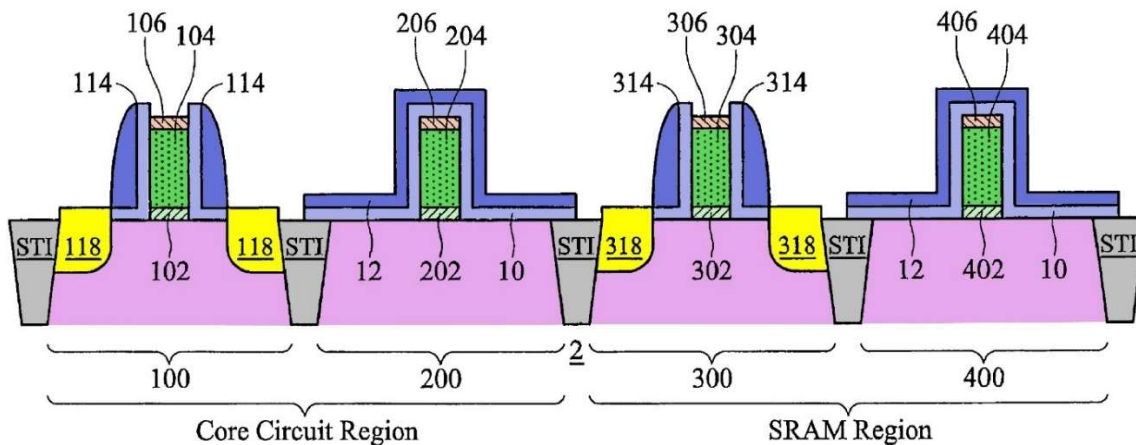
FIG. 2i
Hoentschel262, FIG. 2i

369. Wang753 explains: “Recesses 116 and 316 are formed along the outside edges of the spacers 114 and 314, respectively, preferably by etching isotropically and/or anisotropically.” (Wang753 at 4:10-12.) This can be seen in Wang753’s FIG. 4 below.



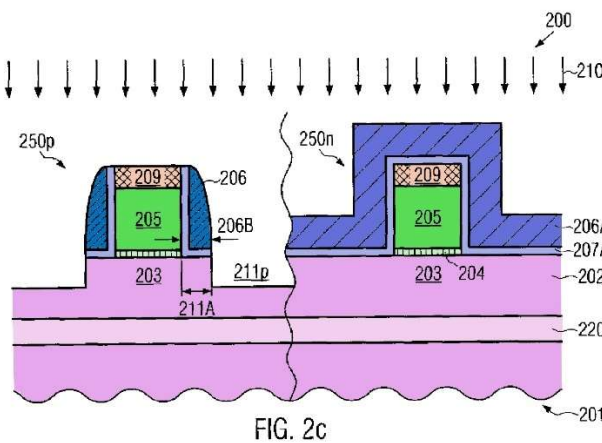
Wang753, FIG. 4

370. Wang753 goes on to explain: “FIG. 5 illustrates the formation of SiGe stressors 118 and 318 in recesses 116 and 316, respectively.” (Wang753 at 4:14-15.) Subsequently, “spacers 114 and 314 . . . are removed.” (Wang753 at 4:23-25.)

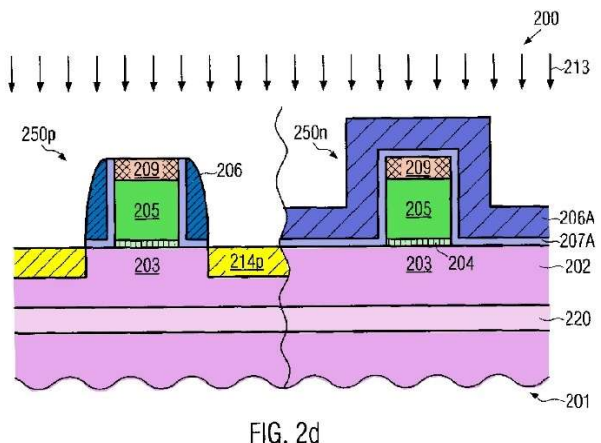


Wang753, FIG. 5

371. Hoentschel262 describes the same fabrication sequence, in which spacer structure 206 has the same structure as, and serves the same purpose as, Wang753's dummy spacer structure (shown in light and dark blue above). (See Wang753 at 3:60-4:22, FIGS. 3-5.) As FIG. 2c in Hoentschel262 shows below, "spacer elements 206 hav[e] a width that substantially corresponds to the thickness 206B," such that "an offset 211A of the recess 211p with respect to the gate electrode 205 . . . is influenced by the spacer width 206B." (Hoentschel262 at 12:66-13:9.) Then, the process continues with an "epitaxial growth process 213 for forming a strained semiconductor material 214p in the recess 211p," as FIG. 2d shows below. (Hoentschel262 at 13:21-30.) "After the epitaxial growth process 213, the spacer layer 206A may be removed on the basis of any appropriate selective etch process." (Hoentschel262 at 13:30-32.)



Hoentschel262, FIG. 2c



Hoentschel262, FIG. 2d

372. Although Wang753 does not disclose the thickness of its disposable spacers 114 and 314, a person of ordinary skill in the art would have known the

appropriate thickness depends on the size of the transistors being made. For example, a person of ordinary skill in the art would have found it obvious to look to Hoentschel262's analogous spacer structures 206 for such information.

373. Hoentschel262 discloses that the thickness 206B of spacer structures 206 "may range from several nanometers, for instance 3-50 nm, depending on the specific application." (Hoentschel262 at 12:46-49.) Because Wang753 and Hoentschel262 both disclose the same types of MOSFETs and use the same technique (a disposable or sacrificial spacer) to define the location of the source/drain epitaxial regions, a person of ordinary skill in the art would have found it obvious to use a disposable spacer thickness in the range Hoentschel262 discloses when fabricating Wang753's spacers 114 and 314. Moreover, a person of ordinary skill in the art would have reasonably expected to succeed in using such thicknesses because it does not affect any other aspects of the process disclosed by Wang753.

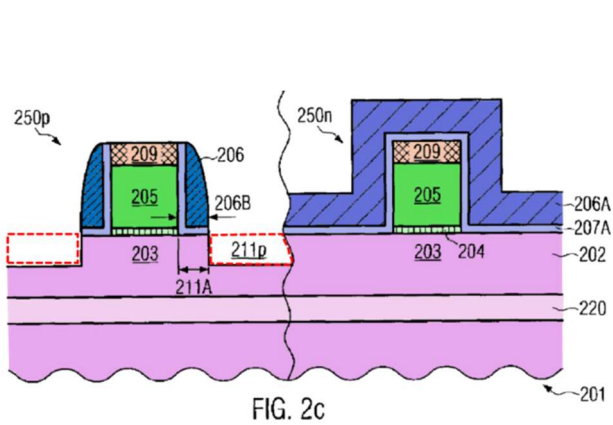
374. In my opinion, a person of ordinary skill in the art would have found it obvious to use the thickness range disclosed for Hoentschel262's spacer structure 206 when making Wang753's spacers 114 and 314 because this would have been an example of (1) adopting one disclosed element (a thickness 206B of Hoentschel262's disposable spacers 206) to implement another (a thickness of Wang753's disposable spacers 114 and 314) to obtain predictable results; (2) using a known technique (using a thickness 206B of Hoentschel262's disposable

spacers 206) to improve similar devices (e.g., Wang753's disposable spacers 114 and 314) in the same way; (3) applying a known technique (using a thickness 206B of Hoentschel262's disposable spacers 206) to a known device ready for improvement (e.g., Wang753's disposable spacers 114 and 314) to yield predictable results; and (4) a teaching, suggestion, or motivation in the prior art (e.g., Hoentschel262's teaching to use a disposable spacer 3-50 nm thick to define the location of epitaxial source/drain regions) that would have led a person of ordinary skill in the art to modify Wang753 and arrive at the claimed invention.

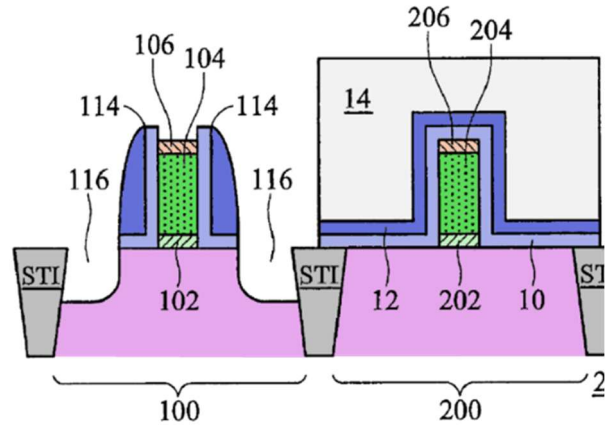
Claims 4/13: “The method of claim [3/10], wherein the [first] protective layer has a thickness of about 150 to 250 angstroms.

375. Wang753 does not specify the thickness of the disposable spacer layer (the protective layer), but Hoentschel262 does. Hoentschel262 uses a substantially similar disposable spacer structure 206 as Wang753's spacers 114 and 314, and Hoentschel262 specifies that its disposable spacer structure 206 is from 3 to 50 nm (i.e., 30 to 500 angstroms) wide. According to Hoentschel262, “transistor 250p comprises respective spacer elements 206 having a width that substantially corresponds to [a] thickness 206B,” wherein “thickness 206B . . . may range from several nanometers, for instance 3-50 nm, depending on the specific application.” (Hoentschel262 at 12:46-49, 12:66-13:2.) In this manner, “an offset 211A of the recess 211p with respect to the gate electrode 205 . . . is influenced by the spacer

width 206B, and may be substantially determined thereby.” (Hoentschel262 at 13:5-9; *see also* Hoentschel262 at FIG. 2c.)



Hoentschel262, FIG. 2c



Wang753, FIG. 4 (excerpted)

376. Further, I have been informed that when the prior art discloses a broader range of values (e.g., 30 to 500 angstroms) that encompasses a narrower range of claimed values (e.g., 150 to 250 angstroms), the broader prior art range discloses the narrower claimed range so long as the narrower claimed range is not “critical” (meaning different in kind, not just degree) as compared to the other values in the broader disclosed range. Here, there have been no allegations of criticality, and I am not aware of any. The thickness of Hoentschel’s spacer structure 206, and its analogous spacers 114 and 314 in Wang753, sets the spacing between the gate electrode and epitaxial material, which is a design parameter that merely depends on device scaling. I am not aware of anything special, and certainly not critical, regarding a range of 150 to 250 angstroms. I therefore understand that Hoentschel262 discloses the claimed range. In fact, the claimed range is

Declaration of Prof. Eugene Fitzgerald, Ph.D.

approximately in the middle of the disclosed range, and it is consistent with the spacing a person of ordinary skill in the art would have expected for contemporaneous devices (e.g., around the 65 nm node). Because Wang753's spacers 114 and 314 are analogous to Hoentschel262's disposable spacer structure 206, a person of skill in the art would have found it obvious to use the same thickness range for Wang753's spacers 114 and 314.

X. Conclusion

377. As discussed above, it is my opinion that the Challenged Claims of the '194 Patent are unpatentable because they are anticipated by the prior art, because they would have been obvious to a person of ordinary skill in view of the prior art, or both.

378. In signing this declaration, I recognize that the declaration will be filed as evidence in a contested proceeding before the Patent Trial and Appeal Board of the United States Patent and Trademark Office. I also recognize that I may be subject to cross-examination in the proceeding and that cross-examination will take place within the United States. If cross-examination is required of me, I will appear for cross-examination within the United States during the time allotted for cross-examination.

379. I reserve the right to supplement my opinions in the future to respond to any arguments that Patent Owner raises and to account for new information as it becomes available to me.

380. I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Declaration of Prof. Eugene Fitzgerald, Ph.D.

Executed on this 2nd day of December 2025.

By:  _____

Prof. Eugene Fitzgerald, Ph.D.

Appendix A

Declaration of Prof. Eugene Fitzgerald, Ph.D.

Exhibit	Description
Ex-1001	U.S. Patent No. 8,076,194 B2 to Tseng et al. (“’194 patent”).
Ex-1002	Prosecution File History of the ’194 patent (“Prosecution History”).
Ex-1004	Curriculum Vitae of Dr. Eugene Fitzgerald, Ph.D.
Ex-1005	U.S. Pat. No. 7,579,262 B2 to Hoentschel et al. (“Hoentschel262”)
Ex-1006	U.S. Pat. No. 7,605,407 B2 to Wang (“Wang407”).
Ex-1007	U.S. Pat. No. 7,449,753 B2 to Wang et. al. (“Wang753”)
Ex-1008	S.M. Sze, <i>Physics of Semiconductor Devices</i> . (2d ed. 1981) (excerpted) (“Sze”).
Ex-1009	J.D. Plummer et al., <i>Silicon VLSI Technology: Fundamentals, Practice and Modeling</i> (2000) (excerpted) (“Plummer”).
Ex-1010	D. James, “2004 – The Year of 90-nm: A Review of 90 nm Devices,” 2005 IEEE/SEMI Advanced Semiconductor Manufacturing Conference, pp. 72-76 (2005) (“James”).
Ex-1011	S.E. Thompson et al., “A 90-nm Logic Technology Featuring Strained-Silicon,” IEEE Transactions on Electron Devices, vol. 51. No. 11, pp. 1790-97 (Nov. 2004) (“Thompson”).
Ex-1012	U.S. Pat. Pub. No. 2006/0148151 A1 to Murthy et al (“Murthy”).
Ex-1013	U.S. Pat. Pub. No. 2004/0262683 A1 to Bohr et al (“Bohr”).

Exhibit	Description
Ex-1014	T. Ghani et al., “A 90nm High Volume Manufacturing Logic Technology Featuring Novel 45nm Gate Length Strained Silicon CMOS Transistors,” Technical Digest of the 2003 IEEE International Electron Devices Meeting (“IEDM”), pp. 978-80 (Dec. 10, 2003) (“Ghani”).
Ex-1015	U.S. Pat. Pub. No. 2007/0034906 A1 to Wang et al. (“Wang906”).
Ex-1016	U.S. Pat. Pub. No. 2006/0286729 A1 to Kavalieros et al (“Kavalieros”).
Ex-1017	P. Bai et al., “A 65nm Logic Technology Featuring 35nm Gate Lengths, Enhanced Channel Strain, 8 Cu Interconnect Layers, Low-k ILD and 0.57 μm^2 SRAM Cell,” Technical Digest of the 2004 IEEE International Electron Devices Meeting (IEDM), pp. 657-60 (Dec. 2004) (“Bai”).
Ex-1018	Excerpts from C.Y. Chang & S.M Sze, <i>ULSI Technology</i> (1996) (“Chang”).
Ex-1019	Excerpts from S. Wolf, <i>Silicon Processing for the VLSI Era, Volume 2: Process Integration</i> (1990) (“Wolf2”).
Ex-1020	G.E. Moore, <i>Lithography and the Future of Moore’s Law</i> , Proceedings of the Society of Photo-Optical Instrumentation Engineers (SPIE) 2437, pp. 2-17 (May 19, 1995) (“Moore”).
Ex-1021	Excerpts from S. Wolf, <i>Silicon Processing for the VLSI Era, Volume 3: The Submicron MOSFET</i> (1995) (“Wolf3”).
Ex-1022	M. Quirk & J. Serda, <i>Semiconductor Manufacturing Technology</i> (2001) (excerpted) (“Quirk”).

Exhibit	Description
Ex-1023	A. Wei T. Kammler, J. Höntschel & M. Horstmann, et al., “Combining Embedded and Overlayer Compressive Stressors in Advanced SOI CMOS Technologies,” Extended Abstracts of the 2005 International Conference on Solid State Devices and Materials (“SSDM”), pp. 32-33 (Sept. 2005) (“Wei”).
Ex-1024	M. Horstmann, A. Wei T. Kammler & J. Höntschel, et al., “Integration and Optimization of Embedded-SiGe, Compressive and Tensile Stressed Liner Films, and Stress Memorization in Advanced SOI CMOS Technologies,” 2005 IEEE International Electron Devices Meeting (“IEDM”), pp. 1-4 (Dec. 2005) (“Horstmann”).
Ex-1025	U.S. Patent No. 6,043,545 to Tseng et al. (“Tseng”)
Ex-1026	U.S. Patent No. 6,391,732 to Gupta et al. (“Gupta”)
Ex-1027	J. Damiano et al., “Characterization and Elimination of Trench Dislocations,” Digest of Technical Papers, 1998 Symposium on VLSI Technology, pp. 212-13 (June 1998) (“Damiano”).
Ex-1028	U.S. Patent Appl. Pub. No. 2005/0040479 to Koldiaev et al. (“Koldiaev”).
Ex-1029	U.S. Patent No. 6,191,462 to Chen-Hua (“Hua”).

Appendix B

Claim 1	
1[pre]	A method of fabricating a MOS transistor, comprising:
1[a]	providing a semiconductor substrate;
1[b]	forming at least a gate on the semiconductor substrate;
1[c]	forming a protective layer on the semiconductor substrate, and the protective layer covering the surface of the gate;
1[d]	forming at least a recess within the semiconductor substrate adjacent to the gate;
1[e]	forming an epitaxial layer in the recess, wherein the top surface of the epitaxial layer is above the surface of the semiconductor substrate; and
1[f]	forming a spacer on the sidewall of the gate and on a portion of the epitaxial layer wherein a contact surface of the epitaxial layer and the spacer is above the surface of the semiconductor substrate.
Claim 2	
The method of claim 1, further comprising a step of removing the protective layer after forming the epitaxial layer in the recess.	
Claim 3	
The method of claim 1, wherein the protective layer comprises silicon nitride.	
Claim 4	
The method of claim 3, wherein the protective layer has a thickness of about 150 to 250 angstroms.	
Claim 5	
The method of claim 1, wherein the spacer further comprises an oxide liner and a nitride spacer.	

Claim 6	
The method of claim 1, wherein the spacer further comprises an offset spacer, positioned between the gate and the spacer.	
Claim 7	
The method of claim 1, further comprising a step of forming a source/drain region within the semiconductor substrate adjacent to the gate after forming the spacer.	
Claim 8	
The method of claim 1, further comprising a step of forming a lightly doped region within the semiconductor substrate adjacent to the gate.	
Claim 9	
9[pre]	The method of claim 1, further comprising:
9[a]	forming a lightly doped region in the semiconductor substrate adjacent to the gate after forming the epitaxial layer;
9[b]	forming the spacer on the sidewall of the gate and on the portion of the epitaxial layer after forming the lightly doped region; and
9[c]	forming a source/drain region in the semiconductor substrate adjacent to the spacer.

Claim 10	
10[pre]	A method of fabricating a CMOS transistor, comprising:
10[a]	providing a semiconductor substrate having at least a first conductive transistor area for fabricating first conductive transistors and at least a second conductive transistor area for fabricating second conductive transistors, and an isolation structure between the first conductive transistor area and the second conductive transistor area;
10[b]	forming a gate on the first conductive transistor area and on the second conductive transistor area respectively;
10[c]	forming a first protective layer on the semiconductor substrate, and the first protective layer covering the surface of each gate;
10[d]	forming at least a first recess within the semiconductor substrate adjacent to the gate in the first conductive transistor area;
10[e]	forming a first epitaxial layer in the first recess, wherein the top surface of the first epitaxial layer is above the surface of the semiconductor substrate; and
10[f]	forming a spacer on the sidewall of each gate and at least on a portion of the first epitaxial layer, wherein a contact surface of the first epitaxial layer and the spacer is above the surface of the semiconductor substrate.
Claim 11	
The method of claim 10, further comprising a step of forming a first ion lightly doped region within the semiconductor substrate adjacent to the gate in the first conductive transistor area	
Claim 12	
The method of claim 10, wherein the first protective layer comprises silicon nitride.	

Claim 13	
The method of claim 10, wherein the first protective layer has a thickness of about 150 to 250 angstroms.	
Claim 14	
The method of claim 10, wherein each spacer further comprises an oxide liner and a nitride spacer.	
Claim 15	
The method of claim 10, wherein each spacer further comprises an offset spacer, positioned between each gate and each spacer.	
Claim 16	
The method of claim 10, further comprising a step of removing the first protective layer after forming the first epitaxial layer in the first recess.	
Claim 17	
17[pre]	The method of claim 16, after removing the first protective layer, the method further comprising:
17[a]	forming a second protective layer on the semiconductor substrate, and the second protective layer covering the surface of each gate;
17[b]	forming at least a second recess within the semiconductor substrate adjacent to the gate in the second conductive transistor area;
17[c]	forming a second epitaxial layer in the second recess;
17[d]	removing the second protective layer; and
17[e]	forming a second ion lightly doped region within the semiconductor substrate adjacent to the gate in the second conductive transistor area before forming the spacer.

Claim 18	
The method of claim 17, wherein the second protective layer comprises silicon nitride.	
Claim 19	
The method of claim 18, wherein the second protective layer has a thickness of about 150 to 250 angstroms.	
Claim 20	
20[pre]	The method of claim 10, after forming the first epitaxial layer, the method further comprising
20[a]	forming at least a second recess within the semiconductor substrate adjacent to the gate in the second conductive transistor area;
20[b]	forming a second epitaxial layer in the second recess;
20[c]	removing the first protective layer; and
20[d]	forming a second ion lightly doped region within the semiconductor substrate adjacent to the gate in the second conductive transistor area before forming the spacer.
Claim 21	
The method of claim 10, wherein the first conductive transistors comprise PMOS transistors and the second conductive transistors comprise NMOS transistors.	
Claim 22	
The method of claim 10, wherein the first conductive transistors comprise NMOS transistors and the second conductive transistors comprise PMOS transistors.	