

PUBLIC EXHIBIT 18

US Patent No. 7,745,847

Intel Core Ultra 7 Integrated Circuit

US 7,745,847

Claim 1(pre): “A MOS transistor structure, comprising:”

1. A MOS transistor structure, comprising:

The Intel Core Ultra 7 Integrated Circuit (“Domestic Industry Product”), include a MOS transistor structure.



See Intel Core Ultra 7 Processor, IMG_3131.JPG.

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Claim 1(pre): "A MOS transistor structure, comprising:"



See Intel Core Ultra 7 Processor, IMG_3133.JPG.



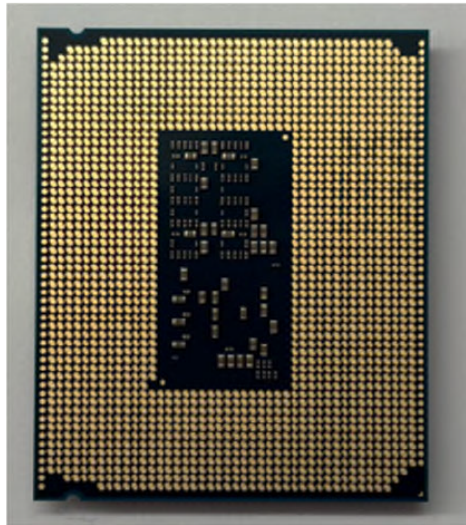
See Intel Core Ultra 7 Processor, IMG_3146.JPG.

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Claim 1(pre): "A MOS transistor structure, comprising:"



See Intel Core Ultra 7 Processor, IMG_3149.JPG.



See Intel Core Ultra 7 Processor, IMG_3154.JPG.

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Claim 1(pre): “A MOS transistor structure, comprising:”

The Domestic Industry Product contains a TSMC semiconductor die which TSMC manufactured using its 5 nm finFET HKMG CMOS.

The Domestic Industry Product belongs to the product family identified with the “Arrow Lake” code name.

Essentials	Essentials	Download Specifications
CPU Specifications	Product Collection	Intel® Core™ Ultra Processors (Series 2)
Supplemental Information	Code Name	Products formerly Arrow Lake
Memory Specifications	Vertical Segment	Desktop
GPU Specifications	Processor Number	265K
NPU Specifications	Overall Peak TOPS (int8)	33
Expansion Options	Recommended Customer Price	\$394.00-\$404.00

See Intel® Core™ Ultra 7 Processor 265K, <https://www.intel.com/content/www/us/en/products/sku/241063/intel-core-ultra-7-processor-265k-30m-cache-up-to-5-50-ghz/specifications.html>.

For example, Arrow Lake products contain a “disaggregated tile-based processor design.”

With “Arrow Lake,” Intel retains the disaggregated tile-based processor design that it embarked upon with “Meteor Lake” in the client segment. The governing idea here is that you needn’t built a large monolithic chip based on the latest foundry node, but rather identify specific IP blocks that benefit the most from the node, such as the CPU cores and the iGPU, and build just those components on the latest nodes, as breakout tiles. The rest of the processor that deals mainly with platform I/O interfaces, can be built on a tile with a slightly older foundry node, thereby letting Intel maximize its yields on the latest foundry node, since the tiles it builds on these nodes are smaller.

See <https://www.techpowerup.com/review/intel-core-ultra-arrow-lake-preview/3.html> (annotated).

Further, for example, “[t]here are five types of tiles making up ‘Arrow Lake.’”

Claim 1(pre): "A MOS transistor structure, comprising:"

There are five types of tiles making up "Arrow Lake." It begins with the Foveros base tile. This is a silicon interposer that sits on the fiberglass package substrates, and seats the other tiles on top. An interposer facilitates high-density microscopic wiring between tiles or chiplets stacked on top of it, which would otherwise not be achievable on the fiberglass substrate. This is the key difference between Intel's tile-based processor, and AMD's chiplet-based ones, which rely on the package substrate to connect the CPU complex dies (CCDs) to the I/O die (IOD). The perks of this interposer include closer physical proximity of the tiles, benefitting latency, and lower power needed to move data around between the tiles.

See <https://www.techpowerup.com/review/intel-core-ultra-arrow-lake-preview/3.html> (annotated).

Further, for example, one of the Arrow Lake tiles is the Graphics tile, which is "built on the 5 nm TSMC N5P node."

The third key tile of "Arrow Lake" is the Graphics tile, built on the Xe-LPG graphics architecture which, interestingly, is a generation older than the Xe2 architecture powering the iGPU of "Lunar Lake." The Graphics tile is built on the 5 nm TSMC N5P node. The Graphics tile only contains the iGPU's number crunching and graphics rendering machinery, in the form of a single Xe Rendering Slice with four Xe cores, worth 64 execution units (EUs) or 512 unified shaders. The Xe cores of Arrow Lake's graphics tile lack XMX units. Any AI acceleration is in the form of DP4a, and not XMX. The enthusiast mobile "Arrow Lake-HX" uses the same Graphics tile. On the other hand, the "Arrow Lake-H" comes with a larger Graphics tile with eight Xe cores (128 EU, 1,024 unified shaders), and the Xe cores there feature XMX units. Despite having just 4 Xe cores, the Graphics tiles of "Arrow Lake-S" and "Arrow Lake-HX" feature ray tracing units, one per Xe core, which give them full DirectX 12 Ultimate capability. Intel has also given the iGPU a rather large 4 MB L2 cache, which cushions transfers between it and the SoC tile.

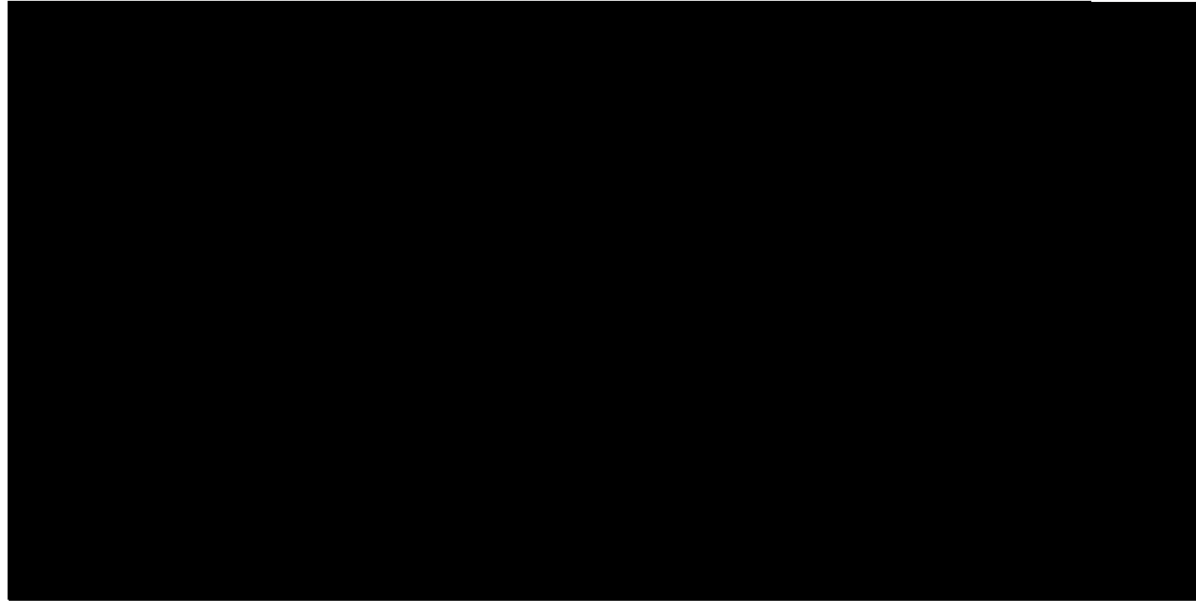
See <https://www.techpowerup.com/review/intel-core-ultra-arrow-lake-preview/3.html> (annotated).

Upon information and belief, the features and process of manufacturing of the Domestic Industry Product integrated circuit is substantially similar to other integrated circuits manufactured by TSMC at the 5 nm process node. Accordingly, upon information and belief, the features and process of manufacturing of the Domestic Industry Product integrated circuit, is manufactured substantially similar to the APL1W07 A15 Bionic Processor, which is also manufactured by TSMC using its 5 nm process node.

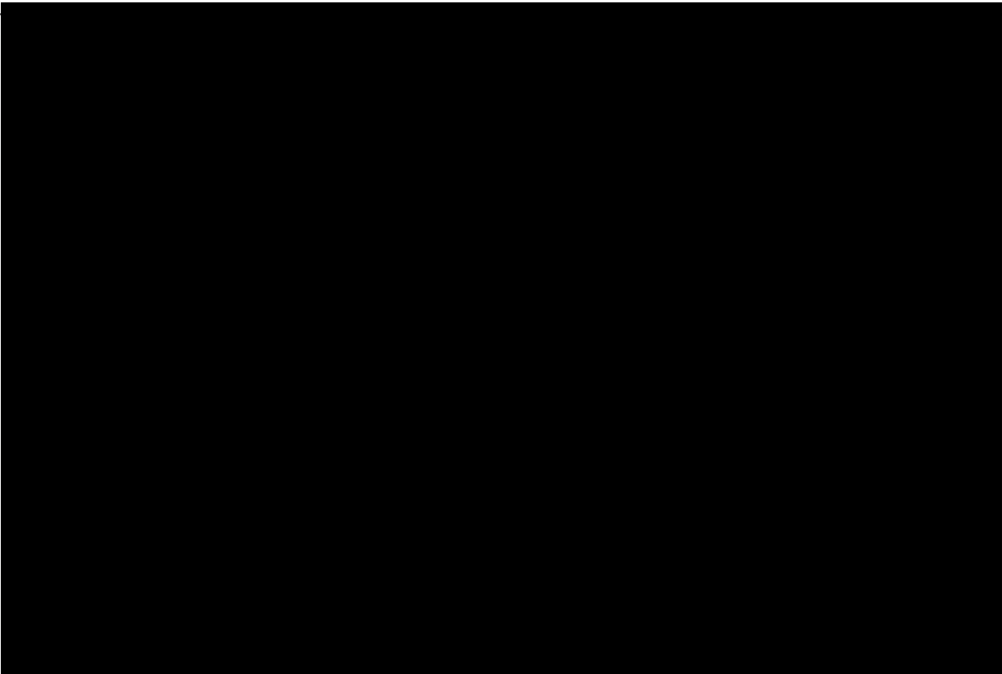
Therefore, upon information and belief, the TechInsight Report for the Apple APL1W07 A15 Bionic Processor TSMC N5P FinFET Process (ACE 2109-801) is representative of the Domestic Industry Product.

Claim 1(pre): “A MOS transistor structure, comprising:”

The Domestic Industry Product contains a TSMC semiconductor die, extracted from a 300 mm finished wafer, which TSMC manufactured using its “5 nm finFET HKMG CMOS” / “N5P” manufacturing process.



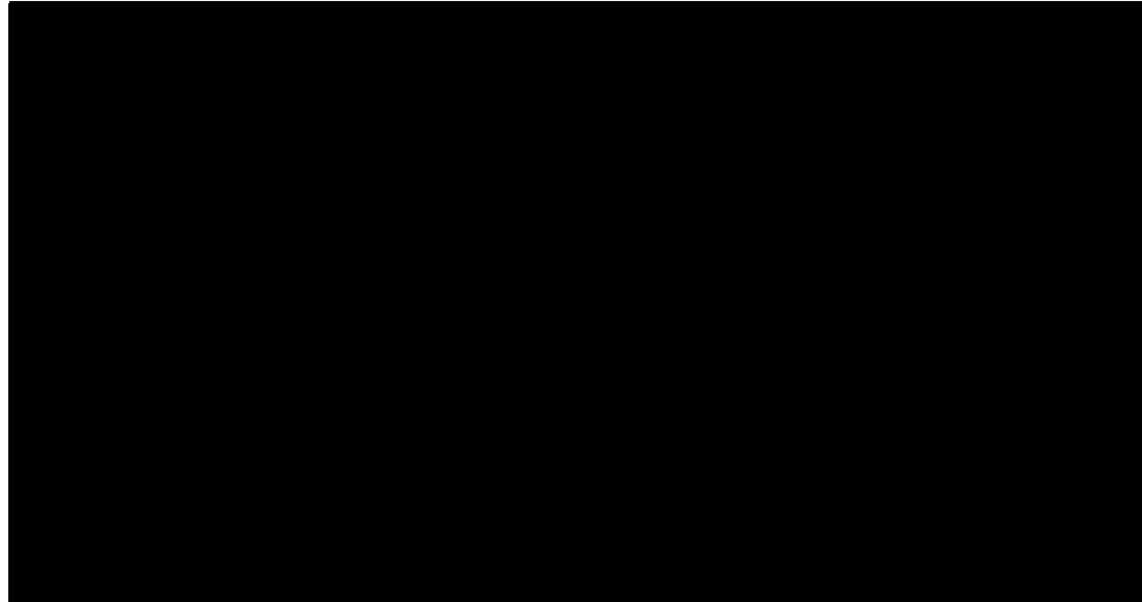
See TechInsights Report for Apple APL1W07 A15 Bionic Processor TSMC N5P FinFET Process (ACE 2109-801), at 4 (annotated).

	 See TechInsights Report for Apple APL1W07 A15 Bionic Processor TSMC N5P FinFET Process (ACE 2109-801), at 10.
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Claim 1(pre): "A MOS transistor structure, comprising:"

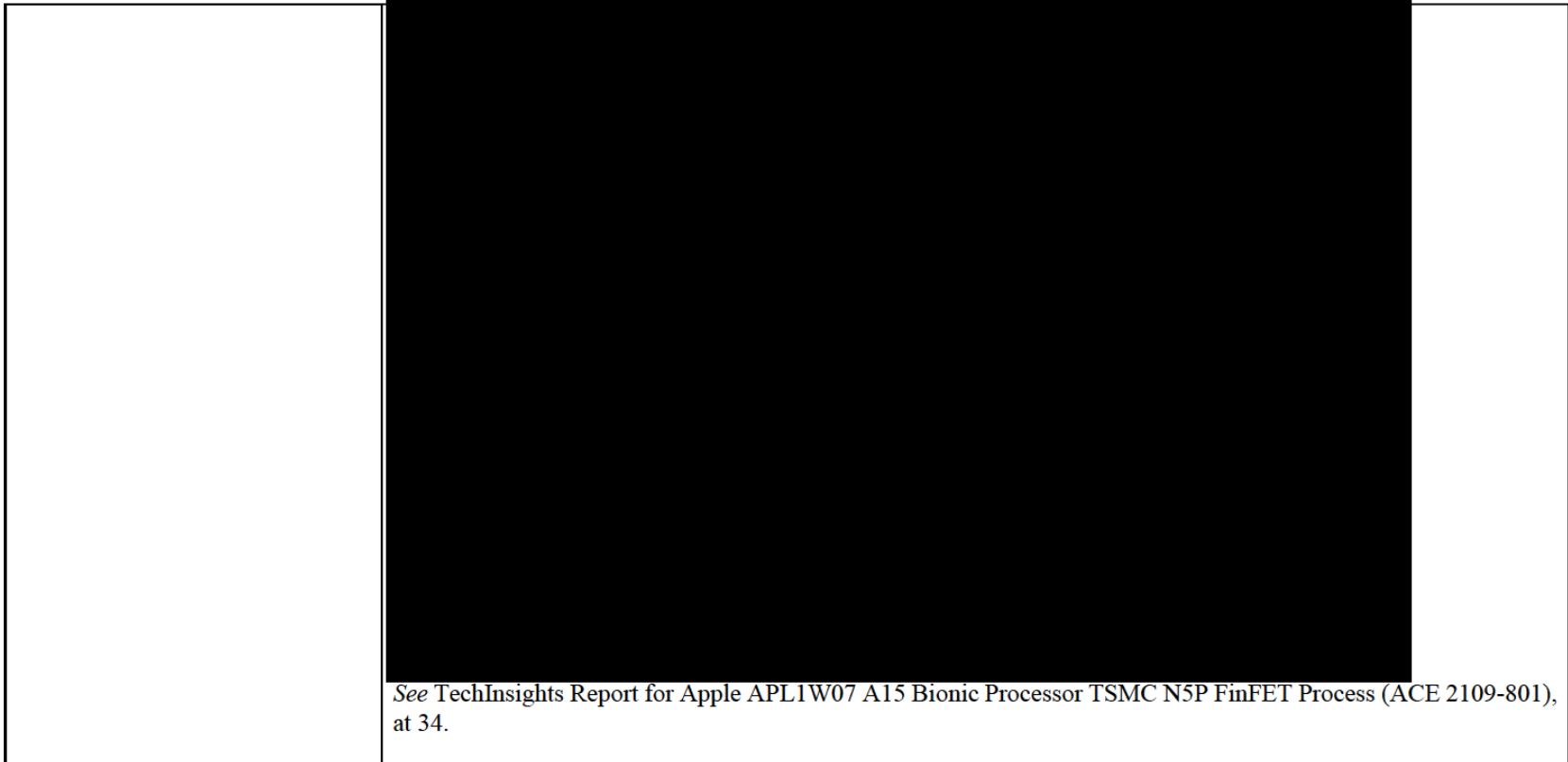
The Domestic Industry Product includes MOS semiconductor structures. For example, TSMC's N5P manufacturing process contains high-k metal gate ("HKMG") complimentary metal oxide semiconductor ("CMOS") transistor structures.



See TechInsights Report for Apple APL1W07 A15 Bionic Processor TSMC N5P FinFET Process (ACE 2109-801), at 4 (annotated).

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Claim 1(pre): "A MOS transistor structure, comprising:"



Claim 1(a): “a gate formed on a semiconductor substrate;”

a gate formed on a semiconductor substrate;

The Domestic Industry Product includes a gate formed on a semiconductor substrate.

For example, the Domestic Industry Product includes a gate.



See TechInsights Report for Apple APL1W07 A15 Bionic Processor TSMC N5P FinFET Process (ACE 2109-801), Images, 3 TEM, Cross Section Across Gate, Area 1_26,5Kx_391809.png (annotated).

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Claim 1(a): "a gate formed on a semiconductor substrate;"

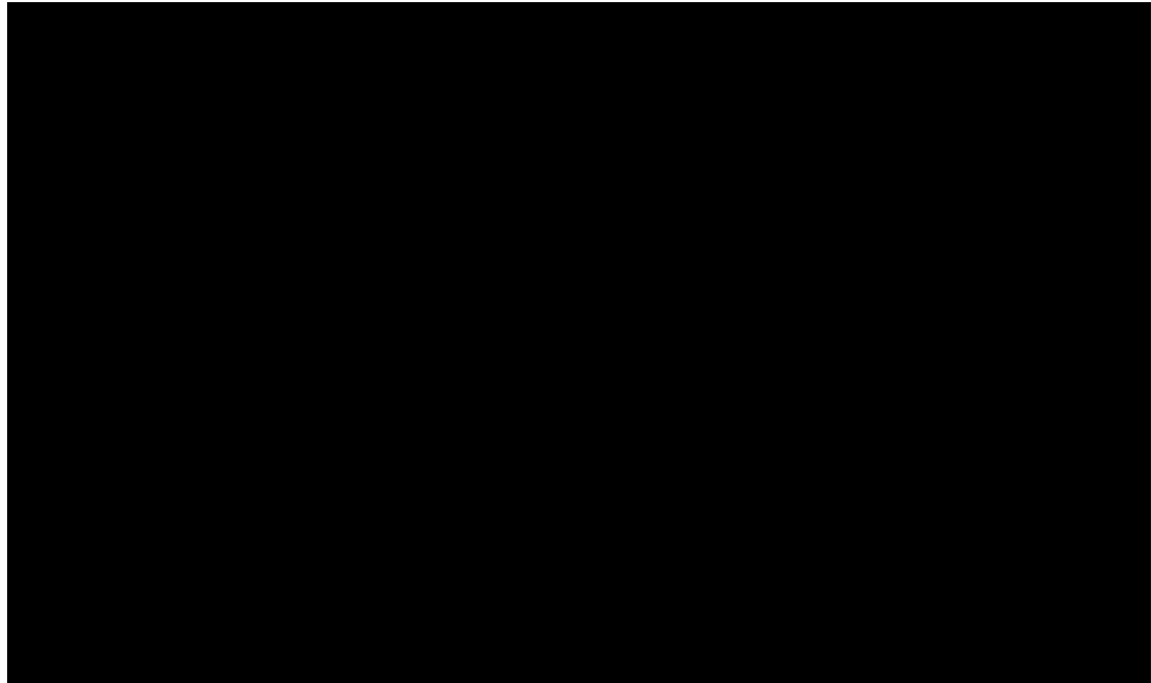


See TechInsights Report for Apple APLIW07 A15 Bionic Processor TSMC N5P FinFET Process (ACE 2109-801), Images, 3 TEM, Cross Section Across Gate, Area 1_NmosSRAM_130Kx_391810.png (annotated).

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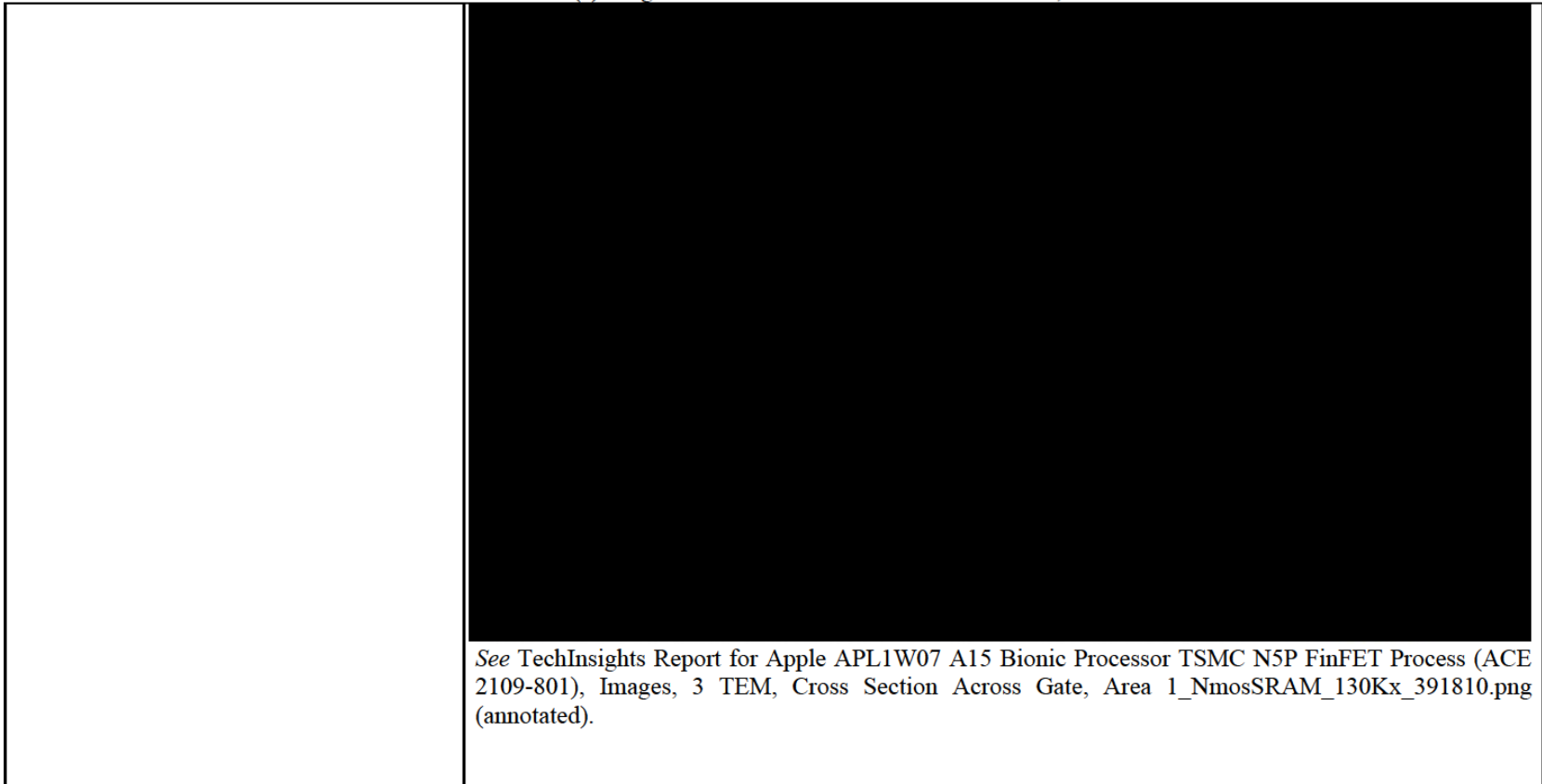
Claim 1(a): “a gate formed on a semiconductor substrate;”

For further example, the Domestic Industry Product includes a gate that is formed on a semiconductor substrate.



See TechInsights Report for Apple APL1W07 A15 Bionic Processor TSMC N5P FinFET Process (ACE 2109-801), Images, 3 TEM, Cross Section Across Gate, Area 1_26,5Kx_391809.png (annotated).

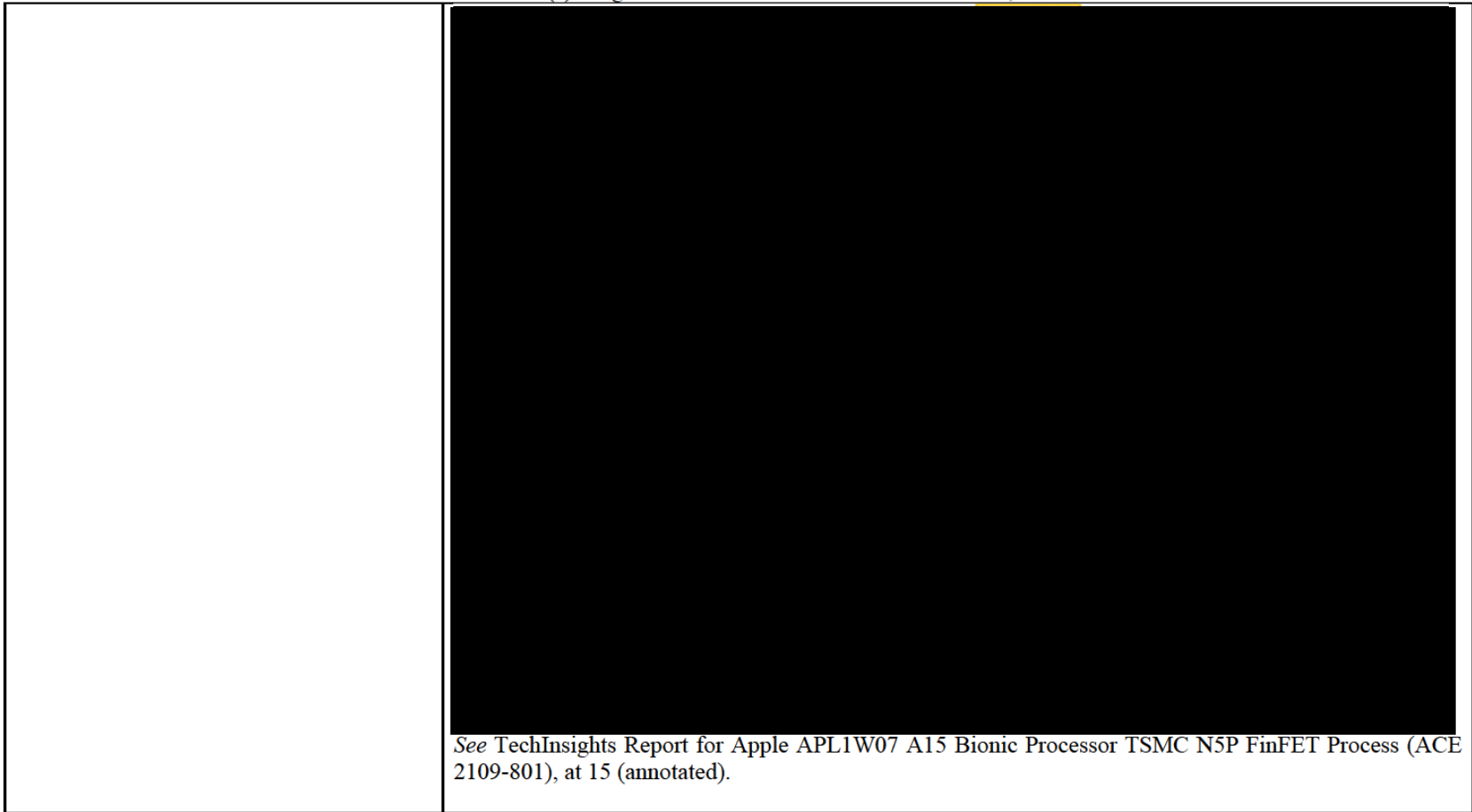
Claim 1(a): “a gate formed on a semiconductor substrate;”



See TechInsights Report for Apple APL1W07 A15 Bionic Processor TSMC N5P FinFET Process (ACE 2109-801), Images, 3 TEM, Cross Section Across Gate, Area 1_NmosSRAM_130Kx_391810.png (annotated).

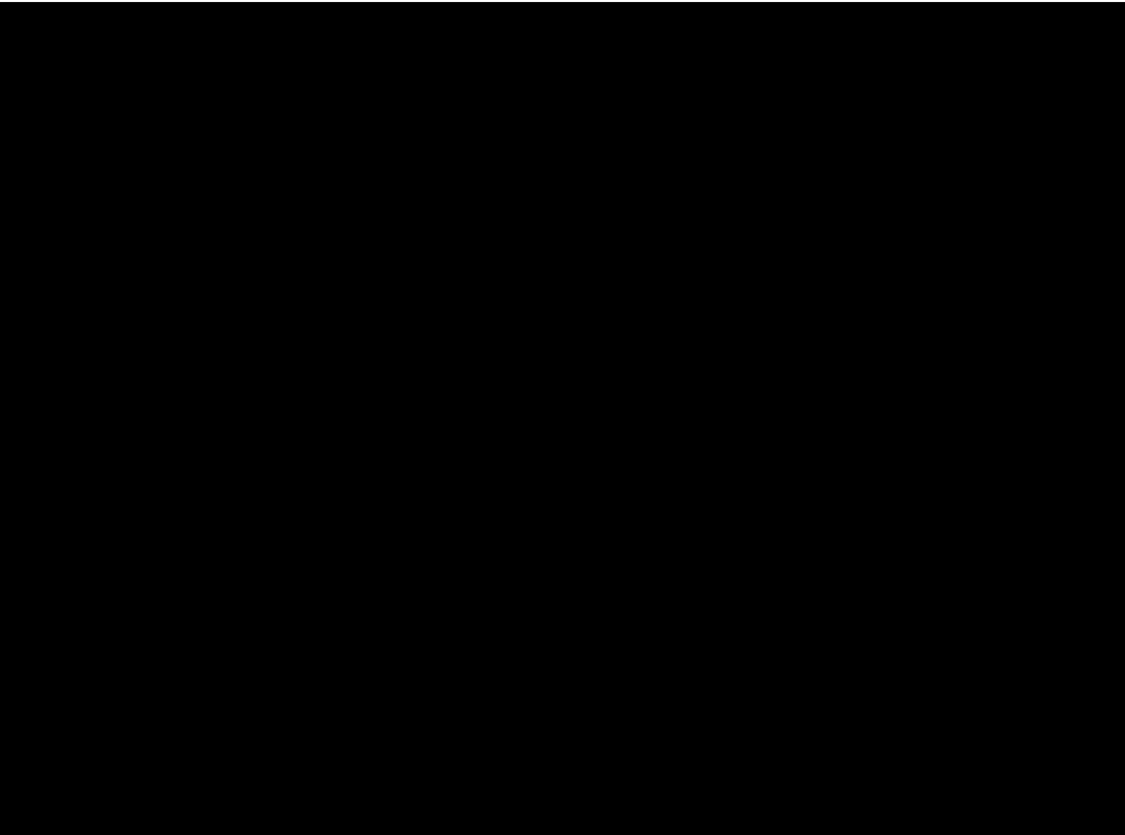
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Claim 1(a): “a gate formed on a semiconductor substrate;”



See TechInsights Report for Apple APL1W07 A15 Bionic Processor TSMC N5P FinFET Process (ACE 2109-801), at 15 (annotated).

Claim 1(b): “two raised epitaxial layers positioned respectively in the semiconductor substrate next to the relative sides of the gate and above the surface of the semiconductor substrate;”

two raised epitaxial layers positioned respectively in the semiconductor substrate next to the relative sides of the gate and above the surface of the semiconductor substrate;	The Domestic Industry Product includes two raised epitaxial layers positioned respectively in the semiconductor substrate next to the relative sides of the gate and above the surface of the semiconductor substrate. For example, the Domestic Industry Product includes source/drain regions that are formed using an epitaxial process. 
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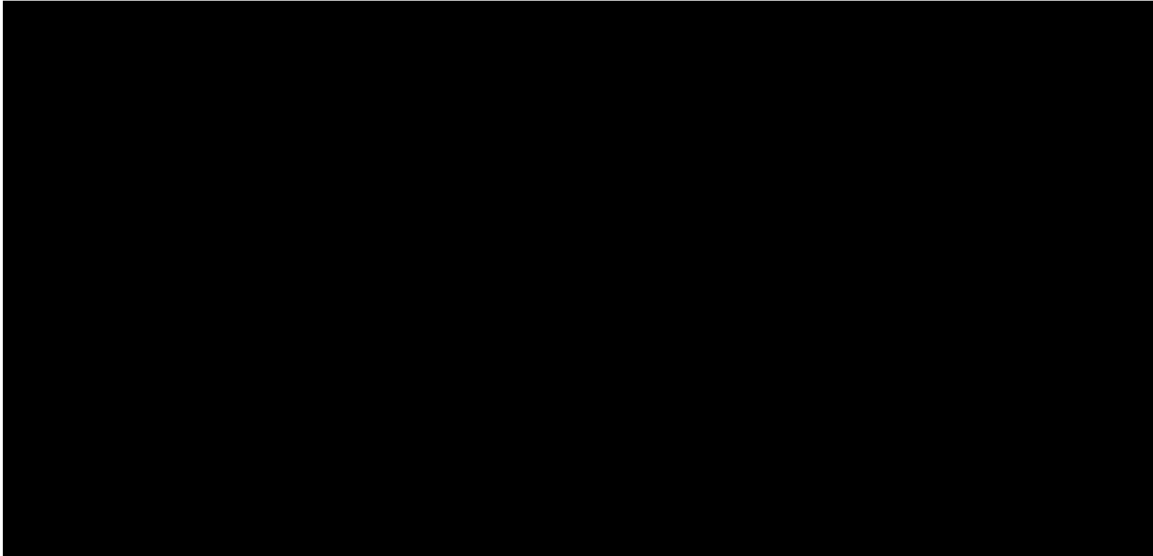
Claim 1(b): “two raised epitaxial layers positioned respectively in the semiconductor substrate next to the relative sides of the gate and above the surface of the semiconductor substrate;”

See TechInsights Report for Apple APL1W07 A15 Bionic Processor TSMC N5P FinFET Process (ACE 2109-801), at 5 (annotated).

For further example, the Domestic Industry Product includes two raised source/drain regions that are positioned respectively in the substrate next to the relative sides of the gate.

See TechInsights Report for Apple APL1W07 A15 Bionic Processor TSMC N5P FinFET Process (ACE 2109-801), Images, 3 TEM, Cross Section Across Gate, Area 1_NmosSRAM_64Kx_391810.png (annotated).

Claim 1(b): “two raised epitaxial layers positioned respectively in the semiconductor substrate next to the relative sides of the gate and above the surface of the semiconductor substrate;”

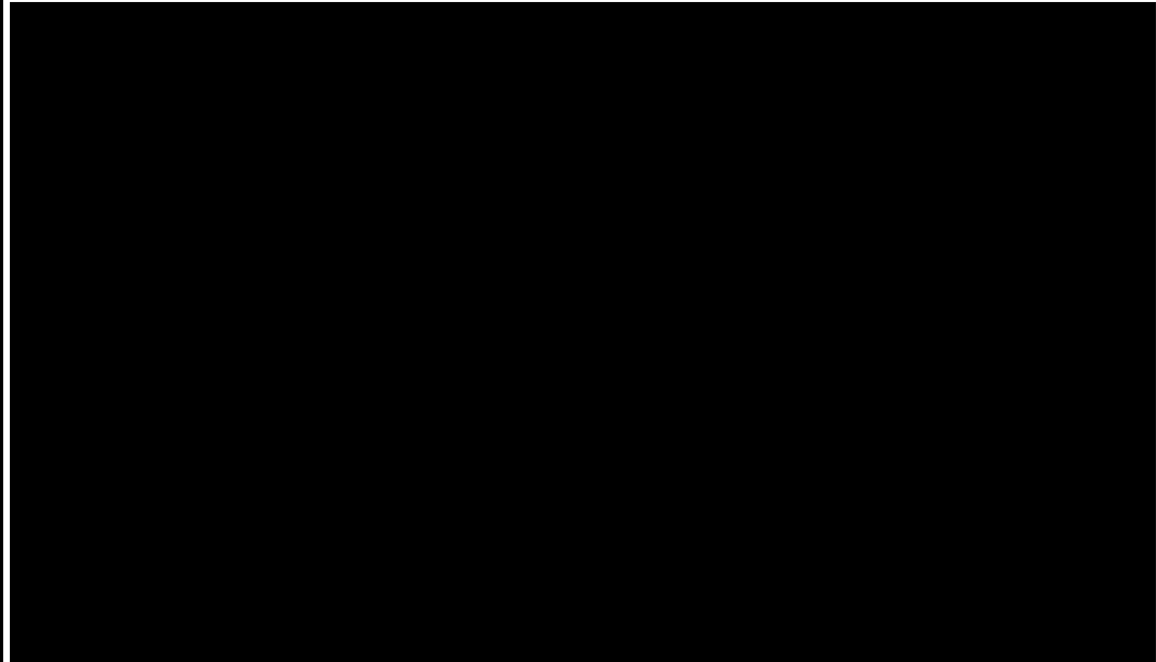
	Further, the epitaxial source/drain regions are formed in the substrate and are raised above the surface of the semiconductor substrate.  See TechInsights Report for Apple APL1W07 A15 Bionic Processor TSMC N5P FinFET Process (ACE 2109-801), Images, 3 TEM, Cross Section Across Gate, Area 1_NmosSRAM_64Kx_391810.png (annotated).
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Claim 1(c): “a spacer formed on the sidewall of the gate and extending laterally upon a portion of the raised epitaxial layers, and”

a spacer formed on the sidewall of the gate and extending laterally upon a portion of the raised epitaxial layers, and

The Domestic Industry Product includes a spacer formed on the sidewall of the gate and extending laterally upon a portion of the raised epitaxial layers.

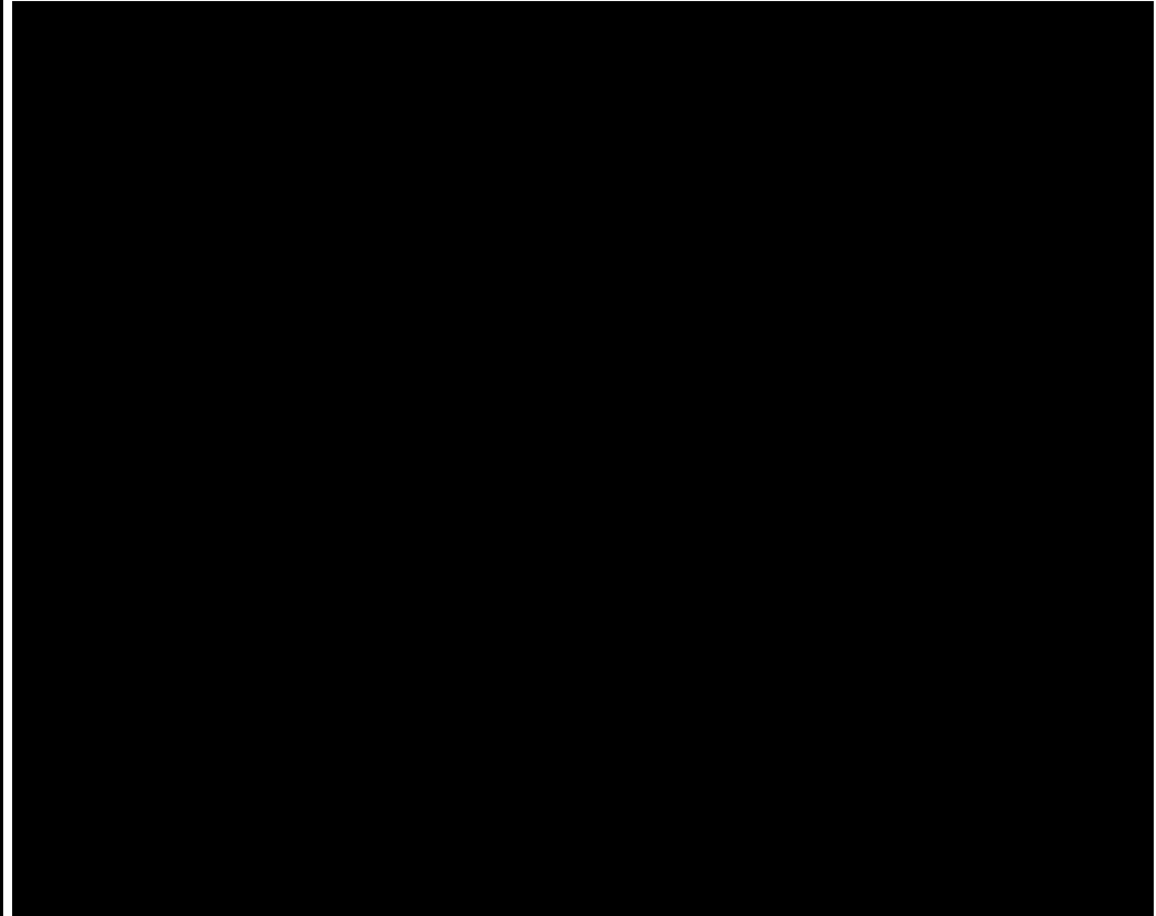
For example, the Domestic Industry Product includes a spacer on the sidewall of the gate.



See TechInsights Report for Apple APL1W07 A15 Bionic Processor TSMC N5P FinFET Process (ACE 2109-801), Images, 3 TEM, Cross Section Across Gate, Area 1_NmosSRAM_64Kx_391810.png (annotated).

Claim 1(c): “a spacer formed on the sidewall of the gate and extending laterally upon a portion of the raised epitaxial layers, and”

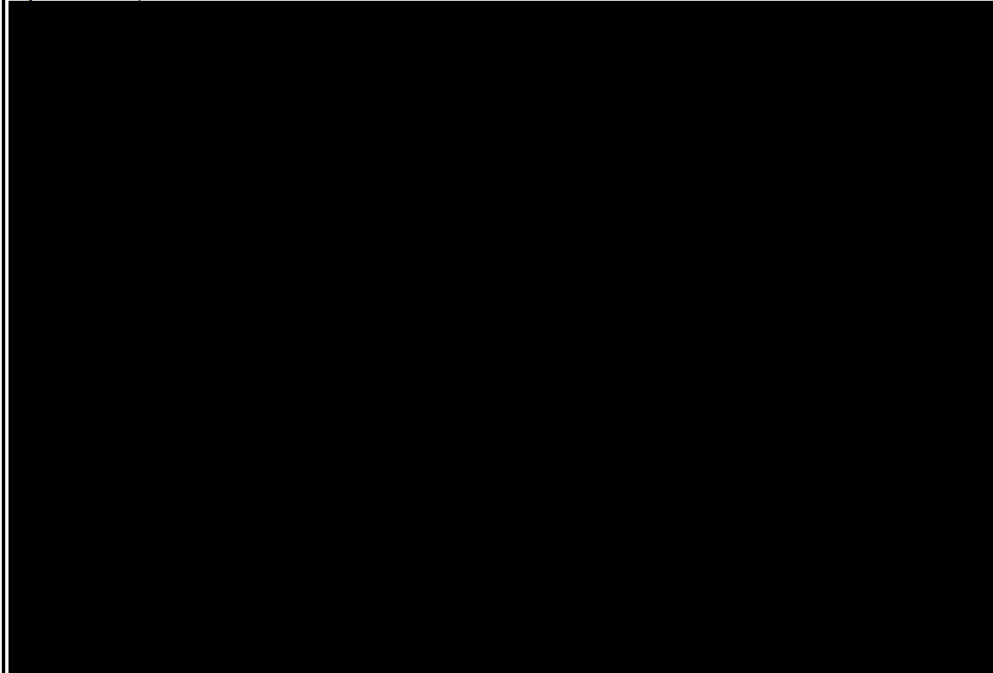
For further example, the Domestic Industry Product includes a spacer extending laterally.



See TechInsights Report for Apple APL1W07 A15 Bionic Processor TSMC N5P FinFET Process (ACE 2109-801), at 15 (annotated).

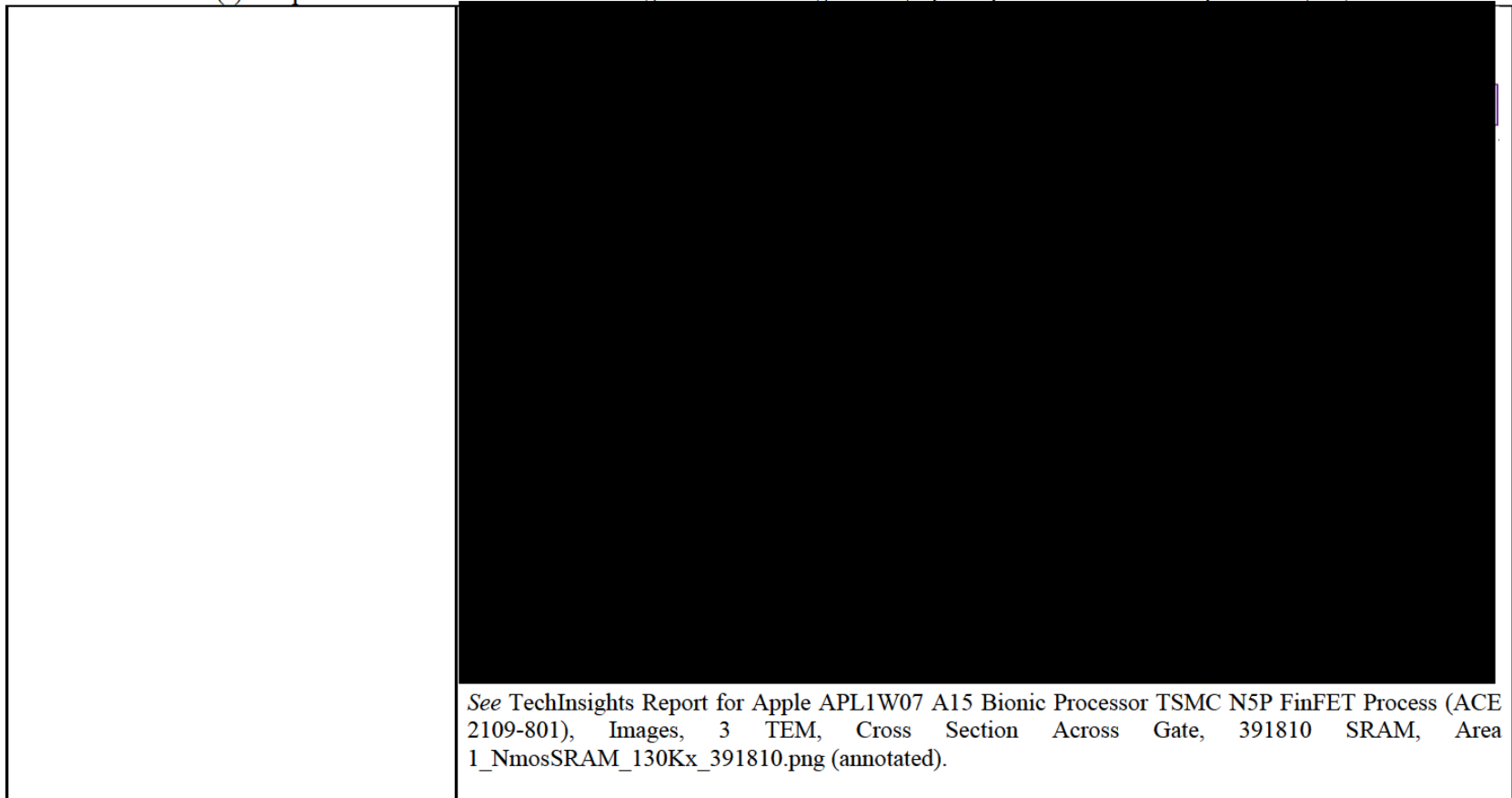
Claim 1(c): “a spacer formed on the sidewall of the gate and extending laterally upon a portion of the raised epitaxial layers, and”

For further example, the Domestic Industry Product includes a spacer formed upon a portion of the raised epitaxial layers.

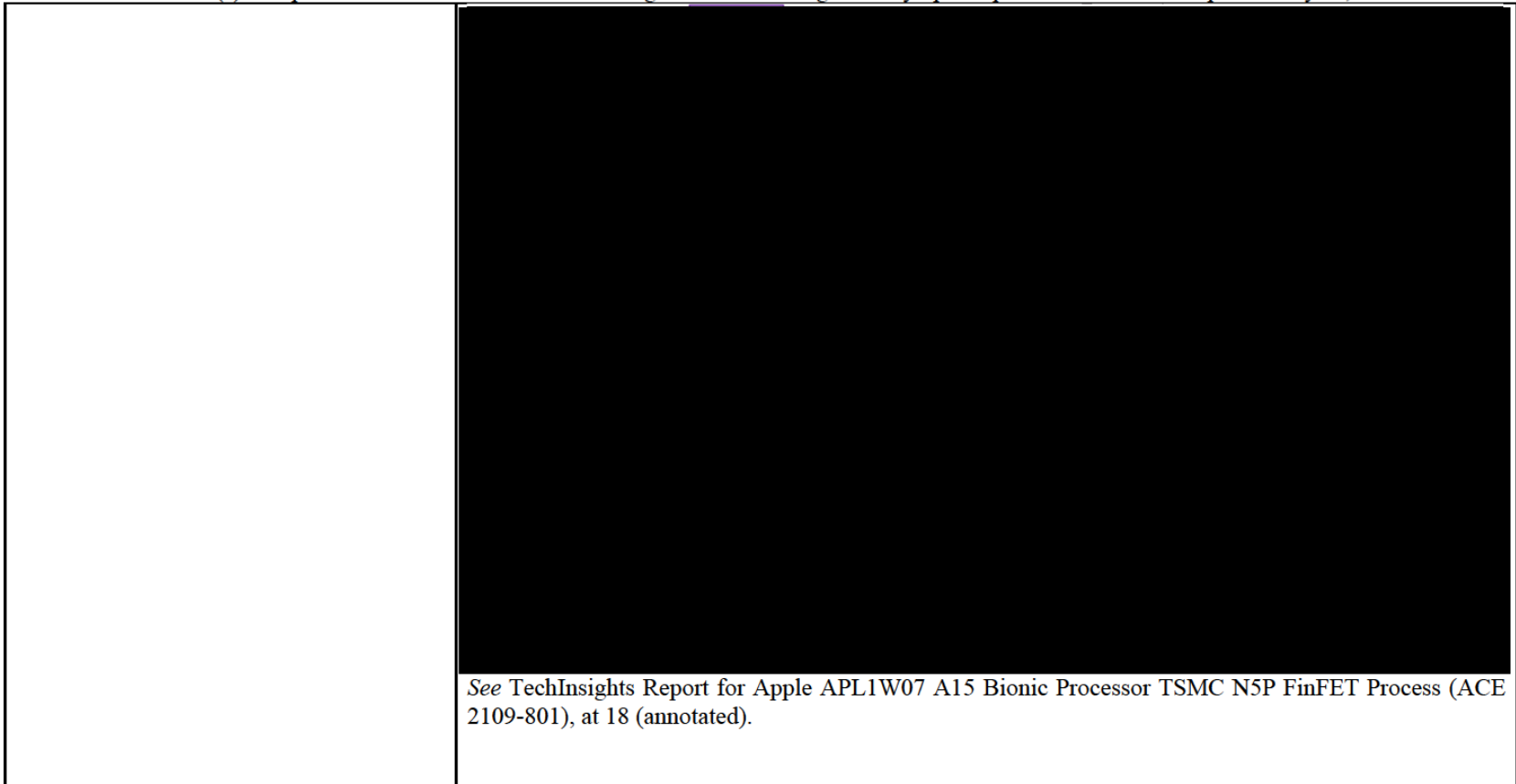


See TechInsights Report for Apple APL1W07 A15 Bionic Processor TSMC N5P FinFET Process (ACE 2109-801), Images, 3 TEM, Cross Section Across Gate, Area 1_NmosSRAM_64Kx_391810.png (annotated).

Claim 1(c): “a spacer formed on the sidewall of the gate and extending laterally upon a portion of the raised epitaxial layers, and”



Claim 1(c): “a spacer formed on the sidewall of the gate and extending laterally upon a portion of the raised epitaxial layers, and”



Claim 1(c): “a spacer formed on the sidewall of the gate and extending laterally upon a portion of the raised epitaxial layers, and”

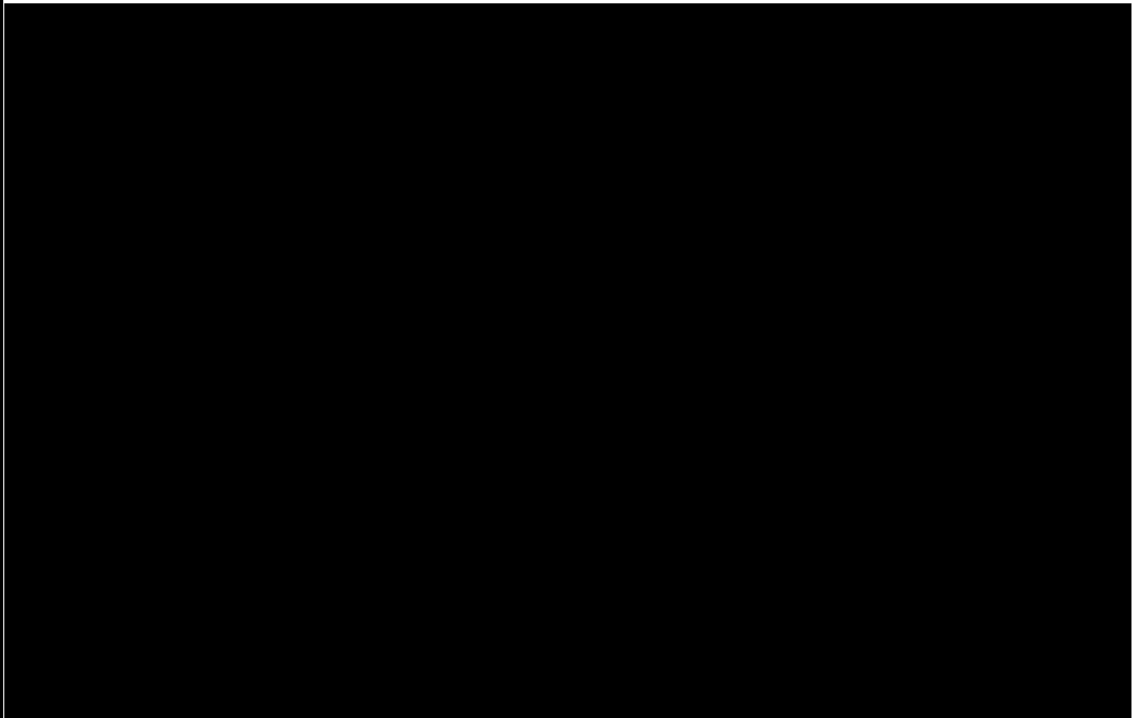


Claim 1(d): “a contact surface of the raised epitaxial layers and a bottom of the spacer is above the surface of the semiconductor substrate; and”

a contact surface of the raised epitaxial layers and a bottom of the spacer is above the surface of the semiconductor substrate; and

The Domestic Industry Product includes a contact surface of the raised epitaxial layers and a bottom of the spacer is above the surface of the semiconductor substrate.

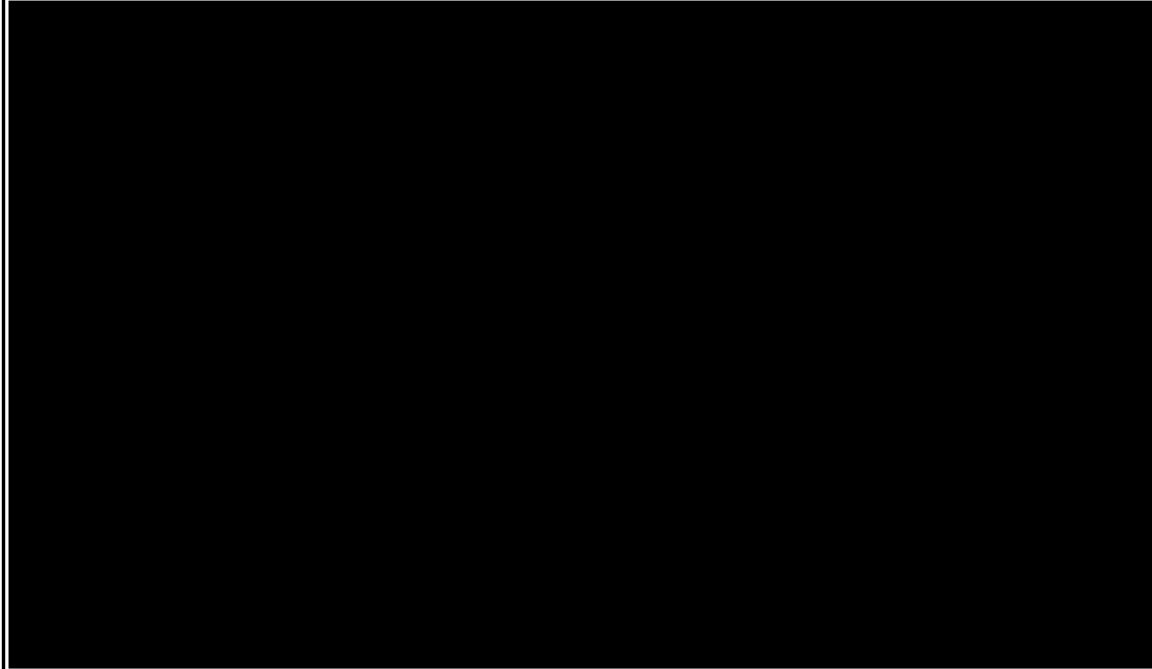
For example, the Domestic Industry Product includes a contact surface between the epitaxial source/drain region and the spacer.



See TechInsights Report for Apple APL1W07 A15 Bionic Processor TSMC N5P FinFET Process (ACE 2109-801), Images, 3 TEM, Cross Section Across Gate, 391810 SRAM, Area 1_NmosSRAM_130Kx_391810.png (annotated).

Claim 1(d): “a contact surface of the raised epitaxial layers and a bottom of the spacer is above the surface of the semiconductor substrate; and”

For further example, the Domestic Industry Product has a contact surface that is above the surface of the semiconductor substrate.



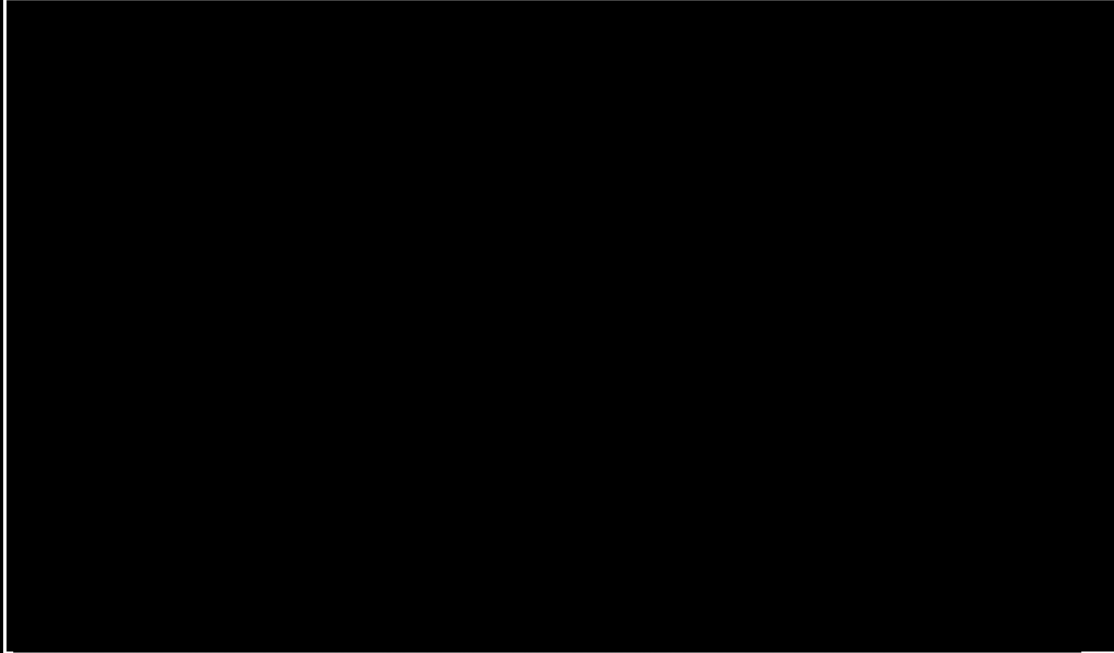
See TechInsights Report for Apple APL1W07 A15 Bionic Processor TSMC N5P FinFET Process (ACE 2109-801), Images, 3 TEM, Cross Section Across Gate, 391810 SRAM, Area 1_NmosSRAM_130Kx_391810.png (annotated).

Claim 1(e): “two doped region formed respectively in the semiconductor substrate next to the relative sides of the gate.”

two doped region formed respectively in the semiconductor substrate next to the relative sides of the gate.

The Domestic Industry Product includes two doped region formed respectively in the semiconductor substrate next to the relative sides of the gate.

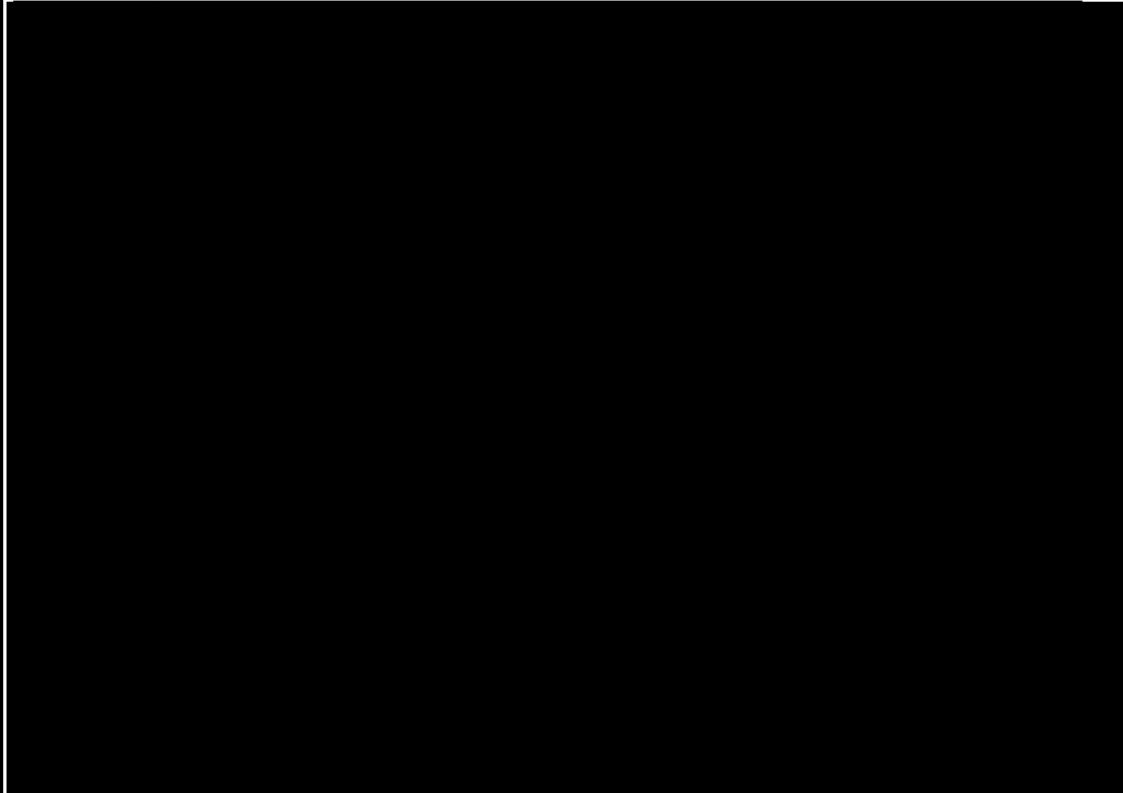
For example, the Domestic Industry Product includes two doped source/drain regions in the substrate next to each side of the gate respectively.



See TechInsights Report for Apple APL1W07 A15 Bionic Processor TSMC N5P FinFET Process (ACE 2109-801), Images, 3 TEM, Cross Section Across Gate, 391810 SRAM, Area 1_NmosSRAM_130Kx_391810.png (annotated).

Claim 1(e): “two doped region formed respectively in the semiconductor substrate next to the relative sides of the gate.”

For further example, the Domestic Industry Product includes a phosphorus (P) doped region in the source drain regions.



See TechInsights Report for Apple APL1W07 A15 Bionic Processor TSMC N5P FinFET Process (ACE 2109-801), at 28 (annotated).