US 20100244245A1

(19) United States

(12) Patent Application Publication

Pendse et al.

(10) Pub. No.: US 2010/0244245 A1

(43) Pub. Date: Sep. 30, 2010

(54) **FILP CHIP INTERCONNECTION STRUCTURE WITH BUMP ON PARTIAL PAD AND METHOD THEREOF**

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(21) Appl. No.: **12/813,335**

(22) Filed: **Jun. 10, 2010**

Related U.S. Application Data

(62) Division of application No. 12/055,152, filed on Mar. 25, 2008, now Pat. No. 7,759,137.

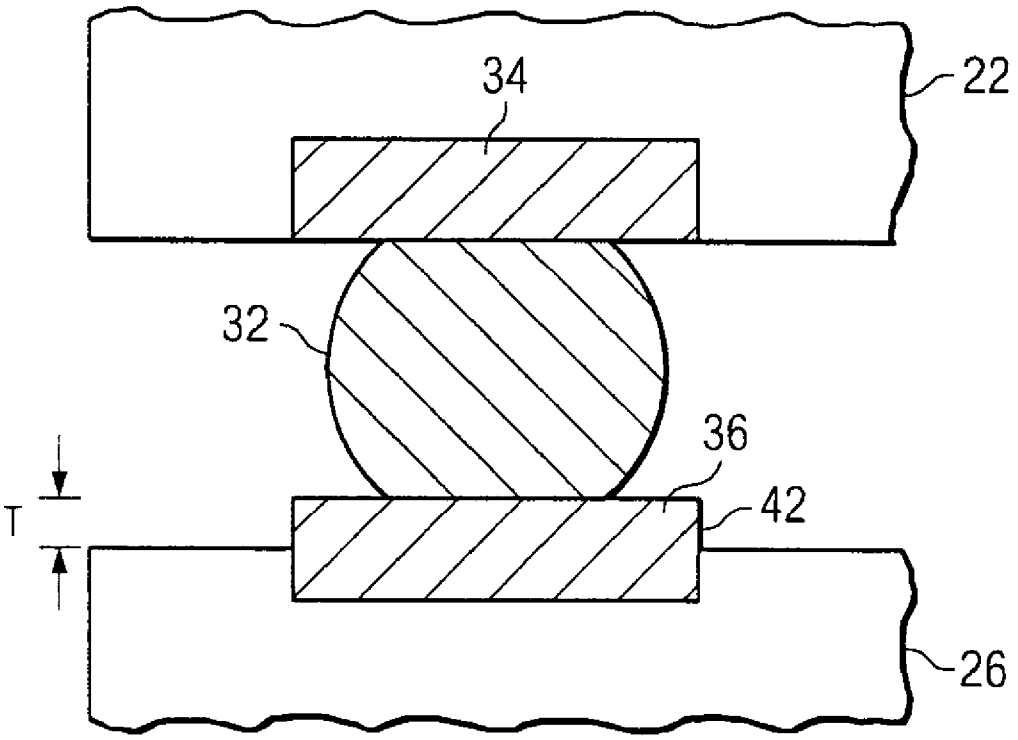
Publication Classification

(51) **Int. Cl.**
H01L 23/498 (2006.01)

(52) **U.S. Cl.** **257/737**; 257/E23.068

(57) **ABSTRACT**

A semiconductor package includes a semiconductor die with a plurality of solder bumps formed on bump pads. A substrate has a plurality of contact pads each with an exposed sidewall. A solder resist is disposed opening over at least a portion of each contact pad. The solder bumps are reflowed to metallurgically and electrically connect to the contact pads. Each contact pad is sized according to a design rule defined by SRO+2*SRR−2X, where SRO is the solder resist opening, SRR is a solder registration for the manufacturing process, and X is a function of a thickness of the exposed sidewall of the contact pad. The value of X ranges from 5 to 20 microns. The solder bump wets the exposed sidewall of the contact pad and substantially fills an area adjacent to the exposed sidewall. The contact pad can be made circular, rectangular, or donut-shaped.



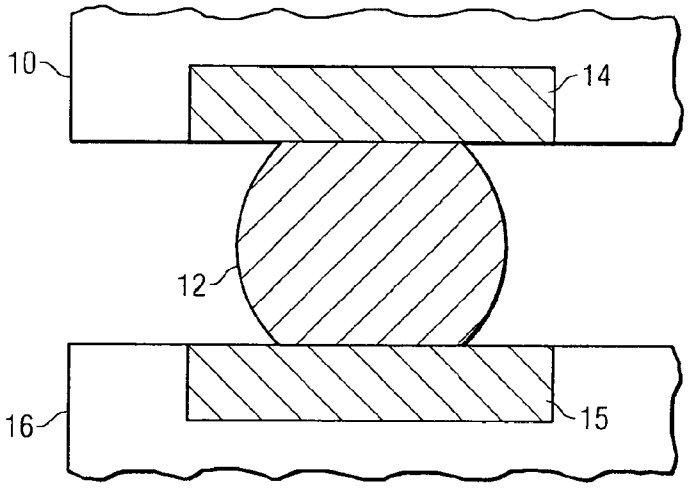


FIG. 1
(PRIOR ART)

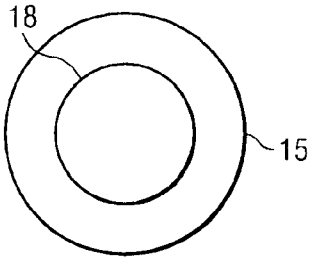


FIG. 2a
(PRIOR ART)

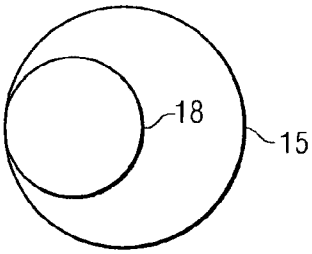


FIG. 2b
(PRIOR ART)

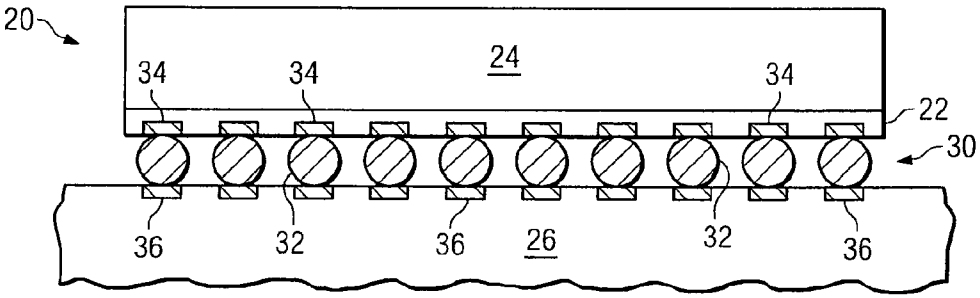


FIG. 3

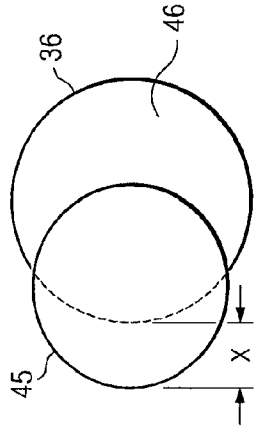


FIG. 4a

FIG. 4c

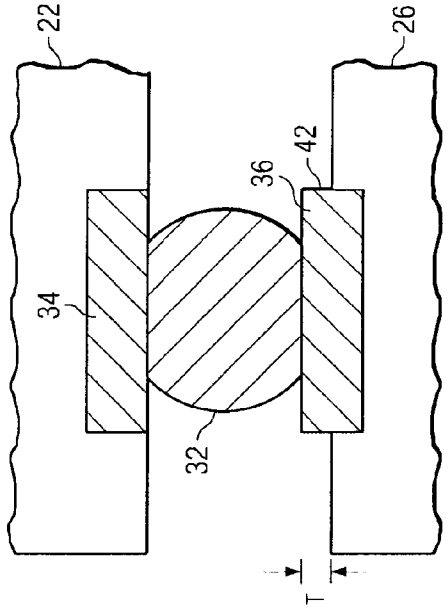


FIG. 4b

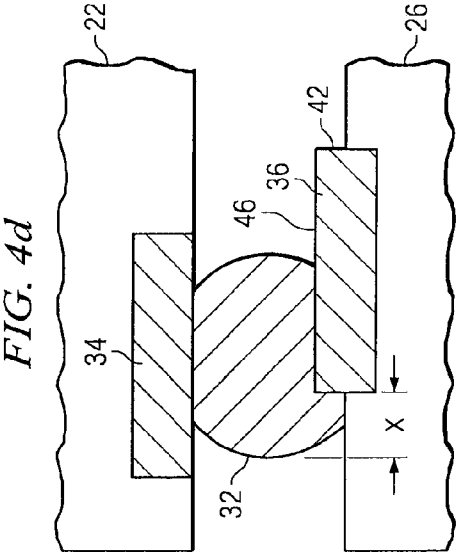


FIG. 4d

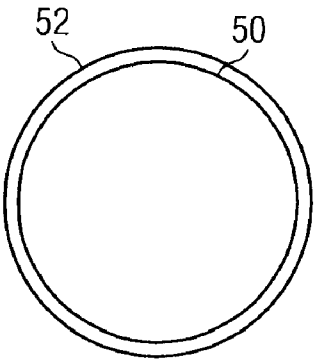


FIG. 5a

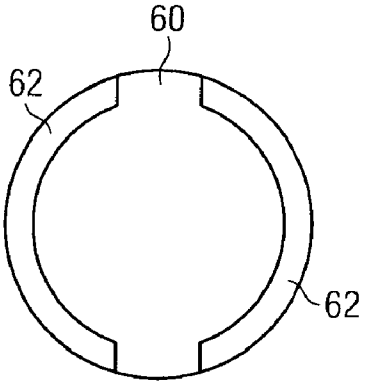


FIG. 5b

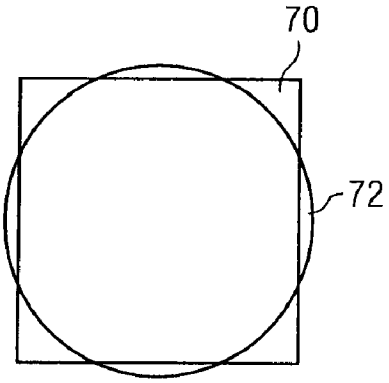


FIG. 5c

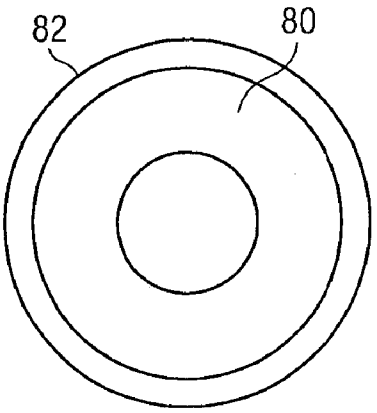


FIG. 5d

FILP CHIP INTERCONNECTION STRUCTURE WITH BUMP ON PARTIAL PAD AND METHOD THEREOF

CLAIM TO DOMESTIC PRIORITY

[0001] The present application is a division of U.S. patent application Ser. No. 12/055,152, filed Mar. 25, 2008, and claims priority to the foregoing parent application pursuant to 35 U.S.C. §120.

FIELD OF THE INVENTION

[0002] The present invention relates in general to semiconductor packages and, more particularly, to a flip chip interconnect structure having a bump on a partial pad.

BACKGROUND OF THE INVENTION

[0003] Semiconductor devices are found in many products in the fields of entertainment, communications, networks, computers, and household markets. Semiconductor devices are also found in military, aviation, automotive, industrial controllers, and office equipment. The semiconductor devices perform a variety of electrical functions necessary for each of these applications.

[0004] The manufacture of semiconductor devices involves formation of a wafer having a plurality of die. Each semiconductor die contains hundreds or thousands of transistors and other active and passive devices performing a variety of electrical functions. For a given wafer, each die from the wafer typically performs the same electrical function. Front-end manufacturing generally refers to formation of the semiconductor devices on the wafer. The finished wafer has an active side containing the transistors and other active and passive components. Back-end manufacturing refers to cutting or singulating the finished wafer into the individual die and then packaging the die for structural support and environmental isolation.

[0005] One goal of semiconductor manufacturing is to produce a package suitable for faster, reliable, smaller, and higher-density integrated circuits (IC) at lower cost. Flip chip packages or wafer level packages (WLP) are ideally suited for ICs demanding high speed, high density, and greater pin count. Flip chip style packaging involves mounting the active side of the die facedown toward a chip carrier substrate or printed circuit board (PCB). The electrical and mechanical interconnect between the active devices on the die and conduction tracks on the carrier substrate is achieved through a solder bump structure comprising a large number of conductive solder bumps or balls. The solder bumps are formed by a reflow process applied to solder material deposited on metal contact pads which are disposed on the semiconductor substrate. The solder bumps are then soldered to the carrier substrate. The flip chip semiconductor package provides a short electrical conduction path from the active devices on the die to the carrier substrate in order to reduce signal propagation, lower capacitance, and achieve overall better circuit performance.

[0006] FIG. **1** illustrates a portion of flip chip **10** with a solder bump **12** formed on metal contact pad **14**. The solder bump **12** is then metallurgically and electrically connected to metal contact pad **15** on substrate **16** using a solder reflow process. To connect solder bump **12** and contact pad **15**, a solder resist or mask opening **18** is disposed over a surface of the substrate to confine the solder reflow to the physical boundaries of contact pad **15**, see FIG. **2***a*. Due to manufacturing alignment tolerances as to the relative position between contact pad **15** and solder resist opening **18**, contact pad **15** is made substantially larger than solder resist opening **18** to ensure that the full metal area of the contact pad is exposed, given the alignment tolerance of the solder resist opening. In generally, the minimum size of contact pad **15** is P_{min}=SRO+2*SRR, where SRO is the minimum solder resist opening required to ensure good metallurgical connection and SRR is the solder resist alignment tolerance, also known as solder registration. In one example, if solder resist opening **18** is 90 microns and the solder resist alignment tolerance is 25 microns, then, according to the known design rule, contact pad **15** is made 140 microns in diameter. Thus, under the known design rule, and given the maximum manufacturing alignment tolerance, the solder resist opening always falls within the contact pad and leaves no voids or empty space around the pad, as shown in FIG. **2***b*.

[0007] Unfortunately, the larger contact pad required to ensure that the solder resist opening always falls within the full metal area of the contact pad limits the metal signal trace or track routing density that can be achieved on the substrate. The larger contact pad necessarily reduces trace routing density as fewer traces can be placed between the contact pads. In addition, the larger contact pad translates to fewer contacts pads per unit area of the substrate.

SUMMARY OF THE INVENTION

[0008] A need exists to minimize the contact pad size to increase trace routing density without impacting electrical functionality or manufacturing reliability. Accordingly, in one embodiment, the present invention is a semiconductor device comprising a semiconductor die having a plurality of bumps formed on bump pads. A substrate has a plurality of contact pads each with an exposed sidewall. An opening is disposed over at least a portion of each contact pad. The bumps are metallurgically and electrically connected to the contact pads. Each contact pad is sized according to a design rule defined by SRO+2*SRR−2X, where SRO is the opening, SRR is a registration for the manufacturing process, and X is a function of a thickness of the exposed sidewall of the contact pad.

[0009] In another embodiment, the present invention is a semiconductor device comprising a substrate having a contact pad with an exposed sidewall. An opening is disposed over at least a portion of the contact pad. The contact pad is sized such that the opening extends over the substrate by a maximum distance of X which is a function of a thickness of the exposed sidewall of the contact pad.

[0010] In another embodiment, the present invention is a semiconductor device comprising a semiconductor die having a bump formed on a bump pad. A substrate has a contact pad with an exposed sidewall. An opening is disposed over at least a portion of the contact pad. The opening extends over a portion of the substrate by a maximum distance of X which is a function of a thickness of the exposed sidewall of the contact pad. The bump is electrically connected to the contact pad. The bump extends down the exposed sidewall of the contact pad.

[0011] In another embodiment, the present invention is a semiconductor device comprising a semiconductor die having a bump formed on a bump pad. A substrate has a contact pad with an exposed sidewall. An opening is disposed over at least a portion of the contact pad. The contact pad is sized

such that the opening extends over the substrate by a maximum distance of X which is a function of a thickness of the exposed sidewall of the contact pad.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] FIG. **1** is a conventional solder bump interconnect to a contact pad on a flip chip;

[0013] FIGS. **2***a*-**2***b* illustrate a conventional alignment design rule for a solder resist opening over the contact pad;

[0014] FIG. **3** is a flip chip semiconductor device with bumps providing electrical interconnect between an active area of the die and a chip carrier substrate;

[0015] FIGS. **4***a*-**4***d* illustrate a contact pad reduced in size by a 2X reduced design rule which allows for misalignment between the contact pad and solder resist opening; and

[0016] FIGS. **5***a*-**5***d* illustrate alternate shapes for the contact pad subject to the 2X reduced design rule.

DETAILED DESCRIPTION OF THE DRAWINGS

[0017] The present invention is described in one or more embodiments in the following description with reference to the Figures, in which like numerals represent the same or similar elements. While the invention is described in terms of the best mode for achieving the invention's objectives, it will be appreciated by those skilled in the art that it is intended to cover alternatives, modifications, and equivalents as may be included within the spirit and scope of the invention as defined by the appended claims and their equivalents as supported by the following disclosure and drawings.

[0018] The manufacture of semiconductor devices involves formation of a wafer having a plurality of die. Each die contains hundreds or thousands of transistors and other active and passive devices performing one or more electrical functions. For a given wafer, each die from the wafer typically performs the same electrical function. Front-end manufacturing generally refers to formation of the semiconductor devices on the wafer. The finished wafer has an active side containing the transistors and other active and passive components. Back-end manufacturing refers to cutting or singulating the finished wafer into the individual die and then packaging the die for structural support and/or environmental isolation.

[0019] A semiconductor wafer generally includes an active surface having semiconductor devices disposed thereon, and a backside surface formed with bulk semiconductor material, e.g., silicon. The active side surface contains a plurality of semiconductor die. The active surface is formed by a variety of semiconductor processes, including layering, patterning, doping, and heat treatment. In the layering process, semiconductor materials are grown or deposited on the substrate by techniques involving thermal oxidation, nitridation, chemical vapor deposition, evaporation, and sputtering. Photolithography involves the masking of areas of the surface and etching away undesired material to form specific structures. The doping process injects concentrations of dopant material by thermal diffusion or ion implantation.

[0020] Flip chip semiconductor packages and wafer level packages (WLP) are commonly used with integrated circuits (ICs) demanding high speed, high density, and greater pin count. Flip chip style semiconductor device or package **20** involves mounting an active area **22** of die **24** facedown toward a chip carrier substrate or printed circuit board (PCB) **26**, as shown in FIG. **3**. Active area **22** contains active and passive devices, conductive layers, and dielectric layers according to the electrical design of the die. The bump pads **34** are formed on active area **22** using an evaporation, electrolytic plating, electroless plating, screen printing, or other suitable metal deposition process. Bump pads **34** connect to the active and passive circuits by conduction tracks in active area **22**. The contact pad **36** can be aluminum (Al), tin (Sn), nickel (Ni), gold (Au), silver (Ag), or copper (Cu). The electrical and mechanical interconnect is achieved through a solder bump structure **30**. A solder material is deposited on bump pads **34** using an evaporation, electrolytic plating, electroless plating, ball drop, or screen printing process with any metal or electrically conductive material, e.g., Sn, lead (Pb), Ni, Au, Ag, Cu, bismuthinite (Bi), and alloys thereof. For example, the solder material can be eutectic Sn/Pb, high lead, or lead free. The solder material is reflowed to form solder bumps or balls **32**. The solder bumps **32** are electrically and mechanically connected to contact pads or interconnect sites **36** on carrier substrate **26** by a solder reflow process. The flip chip semiconductor device provides a short electrical conduction path from the active devices on die **24** to conduction tracks on carrier substrate **26** in order to reduce signal propagation, lower capacitance, and achieve overall better circuit performance.

[0021] Further detail of the solder bump connection to the substrate contact pad is shown in FIGS. **4***a*-**4***d*. Solder bump **32** is formed on bump pad **34** in active area **22** of semiconductor die **24**, as described above. Metal contact pad **36** is formed on substrate **26** using an evaporation, electrolytic plating, electroless plating, screen printing, or other suitable metal deposition process. The contact pad **36** can be Al, Cu, Sn, Ni, Au, or Ag. Contact pad **36** has a sidewall **42** with an exposed thickness T. FIG. **4***a*, a solder resist or mask opening **45** is disposed over at least a portion of contact pad **36**. Depending on its alignment, the solder resist opening **45** may extend over a portion of substrate **26**, as shown in FIG. **4***c*. To electrically and metallurgically connect solder bump **32** to contact pad **36**, the solder bump is reflowed through solder resist opening **45** onto the contact pad, as shown in FIGS. **4***b* and **4***d*.

[0022] In another embodiment, solder material can be deposited through the solder resist opening **45** directly onto contact pad **36** on substrate **26** using an evaporation, electrolytic plating, electroless plating, ball drop, or screen printing process with any metal or electrically conductive material, e.g., Sn, Pb, Ni, Au, Ag, Cu, Bi, and alloys thereof. The solder material is reflowed to form a solder bump, as described above.

[0023] The manufacturing process for semiconductor device **20** employs a new design rule including a solder registration (SRR) which defines an alignment tolerance for the solder resist opening. Under the new design rule, the solder resist opening need not necessarily be aligned within the contact pad, but rather can be offset or misaligned with respect to the physical area of the contact pad due to manufacturing alignment tolerances.

[0024] FIGS. **4***a* and **4***b* show the ideal case where solder resist opening **45** is substantially aligned to a center region of contact pad **36**. In practice, contact pad **36** may be misaligned with respect to solder resist opening **45** during the manufacturing process. For example, in FIG. **4***c*, the solder registration in combination with the smaller contact pad results in solder resist opening **45** extending outside the footprint of contact pad **36** by a distance of X. That is, solder resist

opening **45** is offset or misaligned to the physical area of contact pad **36**. The new design rule allows for this misalignment between contact pad **36** on substrate **26** and solder resist opening **45**. During the wetting process, the surface tension of the solder flux material causes the solder bump **32** to reflow across and adhere to surface **46** of contact pad **36**. In cases where contact pad **36** is misaligned with solder resist opening **45**, i.e. a portion of the contact pad extends outside the solder resist opening, the reflow of solder bump **32** also overlaps and wets sidewall **42** of contact pad **36** to substantially fill the area adjacent to sidewall **42**, as seen in FIG. **4***d*. The solder bump **32** leaves no void or empty space around contact pad **36**, including sidewall **42**. In either case, under the present design rule, solder bump **32** makes good metallurgical and electrical connection to contact pad **36**.

[0025] As a feature of the present invention, the contact pad **36** is made smaller, relative to solder resist opening **45**, as compared to dimensions and design rules found in the prior art. In general, the contact pad **36** is sized according to the following design rule:

$$P_{size}=\text{SRO}+2*SRR-2X \quad (1)$$

[0026] where:

[0027] SRO is solder resist opening,

[0028] SRR is solder registration or manufacturing alignment tolerance, and

[0029] X is a design rule defining the amount by which the solder bump can overlap the edge and sidewall of the contact pad

[0030] The new design rule reduces the size of contact pad **36** by 2X in accordance with equation (1). The value of X is a function of the flux material and thickness of contact pad **36**. In general, the value of X ranges from one to two times the thickness of the exposed sidewall of the contact pad. The exposed portion of contact pad **36** (T) is typically 5-20 microns in thickness. The value of X can increase with flux effectiveness. Accordingly, given a 90-micron solder resist opening and a 25-micron solder resist alignment tolerance, contact pad **36** can be made 120 microns, assuming a design rule with X=10 microns. In another example, given a 90-micron solder resist opening and a 25-micron solder resist alignment tolerance, contact pad **36** can be made 60 microns, assuming a design rule with X=40 microns. In practice, the contact pad is typically made size equal to or smaller than the solder resist opening. In other cases, the contact pad can be larger than the solder resist opening.

[0031] The 2X reduced design rule of equation (1) provides smaller contact pads which provides for more contact pads per unit area of the substrate. In addition, the smaller contact pads provide more space for signal trace routing between the contact pads, thereby increasing trace routing density. The 2X design rule maintains reliability of the metallurgical connection and electrical functionality of the semiconductor device. The reflowed solder material adhering to sidewall **42** increases the metallurgical integrity and reliability of interconnection by providing more solder contact area. Since the solder material wets to sidewall **42**, little or no voids are formed between the solder bump and sidewall **42**. The area of substrate **26** immediately around contact pad **36** is electrically isolated to avoid shorting the solder bump to adjacent traces or devices.

[0032] FIG. **5***a* shows contact pad **50** with a circular shape that is made the same size or slightly smaller than solder resist or mask opening **52**. In this case, the overlap or wetting of the sidewall of the contact pad occurs completely around the circumference of the contact pad. Alternatively, the contact pad can be made larger than the solder resist opening.

[0033] In FIG. **5***b*, contact pad **60** is shown with a generally circular shape and narrow trace lines extending from the pad. The trace lines are substantially narrower than solder resist opening **62**. The overlap or wetting of the sidewall of the contact pad occurs substantially around the circumference of the contact pad.

[0034] In FIG. **5***c*, contact pad **70** is made rectangular to further reduce the exposed volume when solder resist opening **72** is misaligned.

[0035] In FIG. **5***d*, a donut-shaped contact pad **80** provides for wetting of the solder material through solder resist opening **82** on the inner and outer sidewalls of the contact pad. Contact pad **80** reduces the wettable surface area of the pad and provides higher standoff after solder joint is formed.

[0036] In summary, given the alignment tolerance for the solder resist opening, the solder bump will necessary overlap the contact pad in at least some of the manufactured semiconductor devices. By employing the 2X reduced design rule that reduces the contact pad size according to equation (1) and allows the solder material to overlap and wet sidewall **42**, the contact pads can be made smaller in size which provides for placement of more signal traces between the contact pads. The signal trace routing density correspondingly increases. In addition, the smaller contact pads translate to more pads per unit area of the substrate. From the prior art design rule discussed in the background, which resulted in a 140-micron contact pad with a 90-micron solder resist opening, the 2X reduced design rule substantially reduces the contact pad by 2X.

[0037] While one or more embodiments of the present invention have been illustrated in detail, the skilled artisan will appreciate that modifications and adaptations to those embodiments may be made without departing from the scope of the present invention as set forth in the following claims.

What is claimed:

1. A semiconductor device, comprising:

a semiconductor die having a plurality of bumps formed on bump pads;

a substrate having a plurality of contact pads each with an exposed sidewall; and

an opening disposed over at least a portion of each contact pad, wherein the bumps are metallurgically and electrically connected to the contact pads, each contact pad is sized according to a design rule defined by SRO+2*SRR−2X, where SRO is the opening, SRR is a registration for the manufacturing process, and X is a function of a thickness of the exposed sidewall of the contact pad.

2. The semiconductor device of claim **1**, wherein a value of X ranges from 5 to 20 microns.

3. The semiconductor device of claim **1**, wherein the contact pad is equal in size to the opening.

4. The semiconductor device of claim **1**, wherein the contact pad is smaller in size than the opening.

5. The semiconductor device of claim **1**, wherein the contact pad is larger in size than the opening.

6. The semiconductor device of claim **1**, wherein the bump substantially fills an area adjacent to the exposed sidewall of the contact pad.

7. The semiconductor device of claim **1**, wherein the contact pad is circular, rectangular, and donut-shaped.

8. A semiconductor device, comprising:

a substrate having a contact pad with an exposed sidewall; and

an opening disposed over at least a portion of the contact pad, wherein the contact pad is sized such that the opening extends over the substrate by a maximum distance of X which is a function of a thickness of the exposed sidewall of the contact pad.

9. The semiconductor device of claim **8**, wherein the contact pad is sized according to a design rule defined by SRO+2*SRR−2X, where SRO is the opening and SRR is a registration for the manufacturing process.

10. The semiconductor device of claim **8**, further including a semiconductor die with a bump formed on a bump pad, wherein the bump is electrically connected to the contact pad.

11. The semiconductor device of claim **8**, further including a bump formed through the opening over the contact pad.

12. The semiconductor device of claim **8**, wherein a value of X ranges from 5 to 20 microns.

13. The semiconductor device of claim **8**, wherein the contact pad is equal in size to the opening.

14. The semiconductor device of claim **8**, wherein the contact pad is smaller or larger in size than the opening.

15. A semiconductor device, comprising:

a semiconductor die having a bump formed on a bump pad;

a substrate having a contact pad with an exposed sidewall; and

an opening disposed over at least a portion of the contact pad, the opening extending over a portion of the substrate by a maximum distance of X which is a function of a thickness of the exposed sidewall of the contact pad, wherein the bump is electrically connected to the contact pad, the bump extending down the exposed sidewall of the contact pad.

16. The semiconductor device of claim **15**, wherein the contact pad is sized according to a design rule defined by SRO+2*SRR−2X, where SRO is the opening and SRR is a registration for the manufacturing process.

17. The semiconductor device of claim **15**, wherein a value of X ranges from 5 to 20 microns.

18. The semiconductor device of claim **15**, wherein the contact pad is equal in size to the opening.

19. The semiconductor device of claim **15**, wherein the contact pad is smaller or larger in size than the opening.

20. A semiconductor device, comprising:

a semiconductor die having a bump formed on a bump pad;

a substrate having a contact pad with an exposed sidewall; and

an opening disposed over at least a portion of the contact pad, wherein the contact pad is sized such that the opening extends over the substrate by a maximum distance of X which is a function of a thickness of the exposed sidewall of the contact pad.

21. The semiconductor device of claim **20**, wherein the bump is electrically connected to the contact pad and the bump extends down the exposed sidewall of the contact pad.

22. The semiconductor device of claim **20**, wherein the contact pad is sized according to a design rule defined by SRO+2*SRR−2X, where SRO is the opening and SRR is a registration for the manufacturing process.

23. The semiconductor device of claim **20**, wherein a value of X ranges from 5 to 20 microns.

24. The semiconductor device of claim **20**, wherein the contact pad is equal in size to the opening.

25. The semiconductor device of claim **20**, wherein the contact pad is smaller or larger in size than the opening.

* * * * *