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(54) **LOW FABRICATION COST, FINE PITCH AND HIGH RELIABILITY SOLDER BUMP**

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(60) Continuation of application No. 11/930,998, filed on Oct. 31, 2007, which is a continuation of application No. 10/935,451, filed on Sep. 7, 2004, which is a division of application No. 09/798,654, filed on Mar. 5, 2001, now Pat. No. 6,818,545.

Publication Classification

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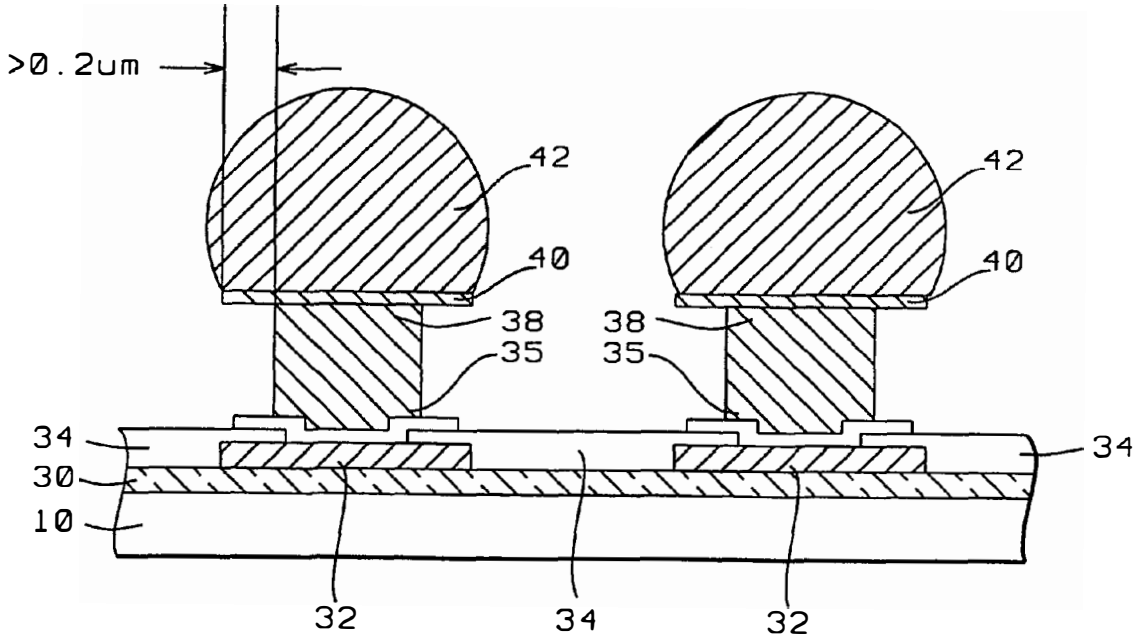
(57) **ABSTRACT**

A barrier layer is deposited over a layer of passivation including in an opening to a contact pad created in the layer of passivation. A column of three layers of metal is formed overlying the barrier layer and aligned with the contact pad and having a diameter that is about equal to the surface of the contact pad. The three metal layers of the column comprise, in succession when proceeding from the layer that is in contact with the barrier layer, a layer of pillar metal, a layer of under bump metal and a layer of solder metal. The layer of pillar metal is reduced in diameter, the barrier layer is selectively removed from the surface of the layer of passivation after which reflowing of the solder metal completes the solder bump of the invention.



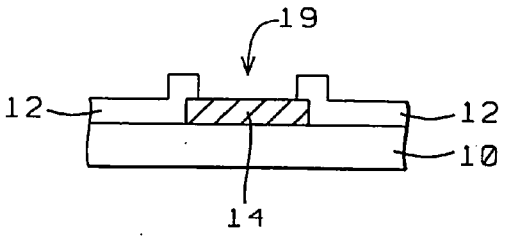


FIG. 1 – Prior Art

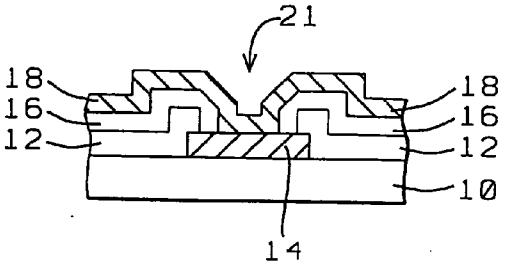


FIG. 2 – Prior Art

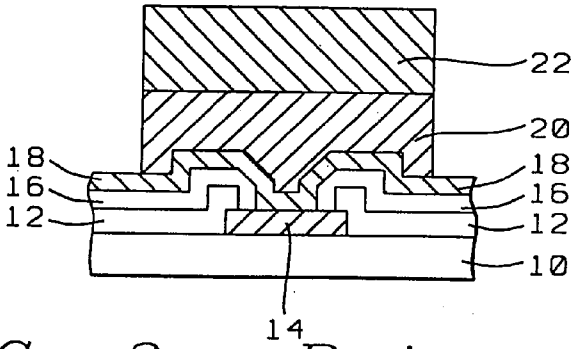


FIG. 3 – Prior Art

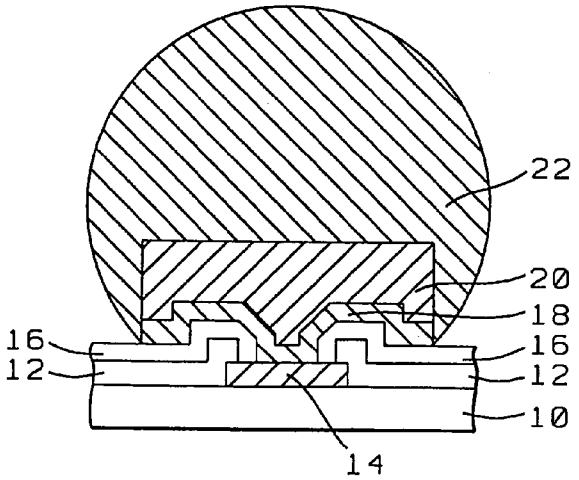


FIG. 4 – Prior Art

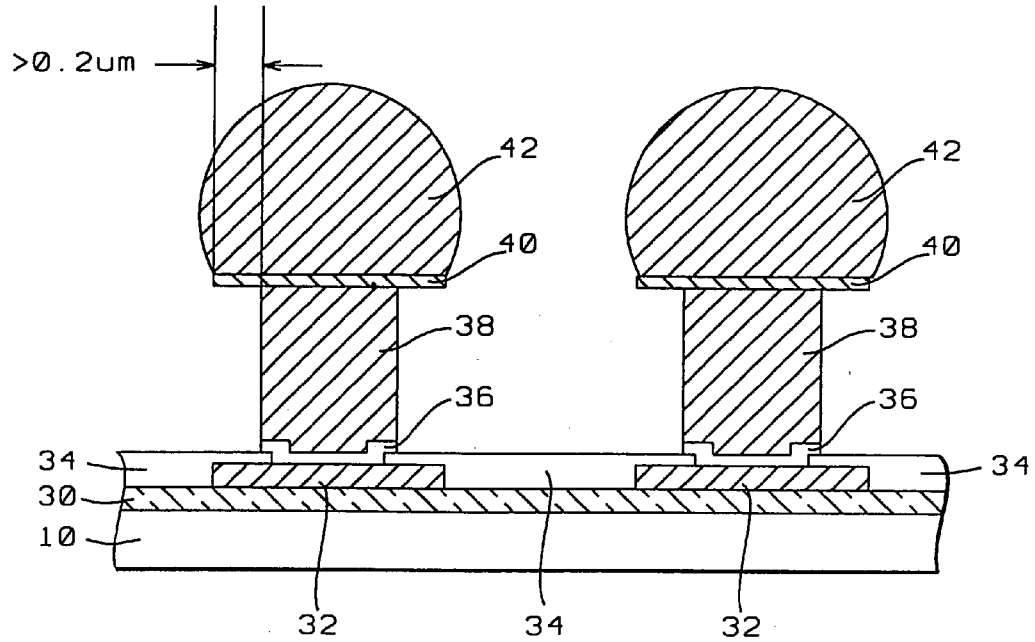

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FIG. 5

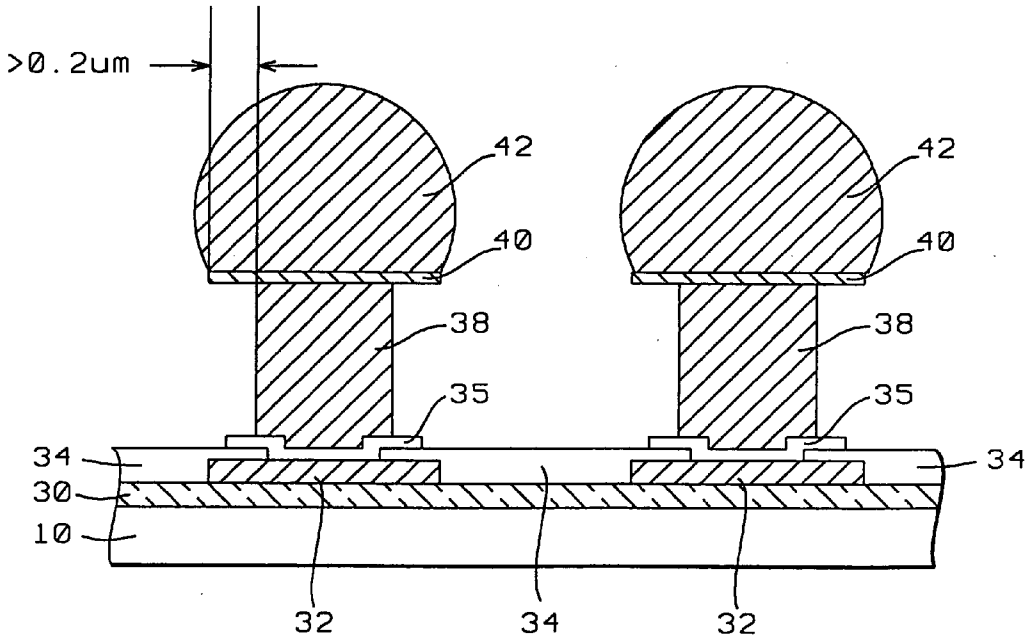
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FIG. 6

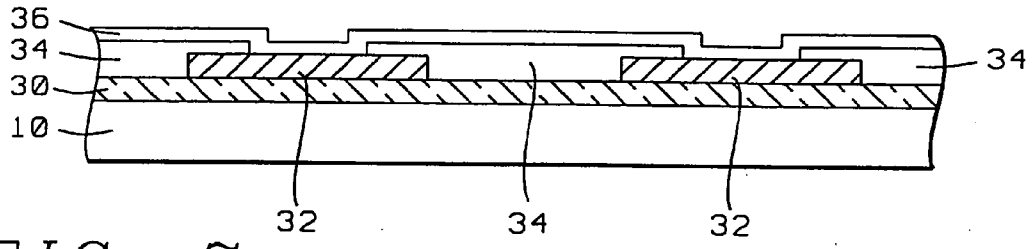

FIG. 7

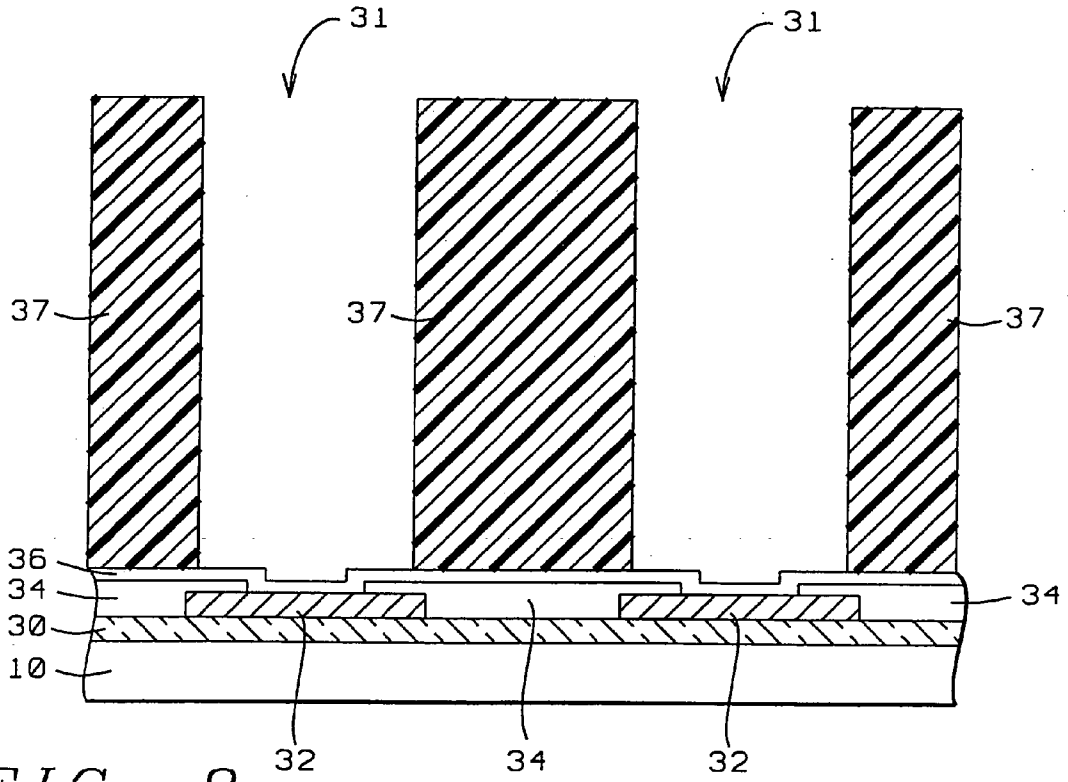

FIG. 8

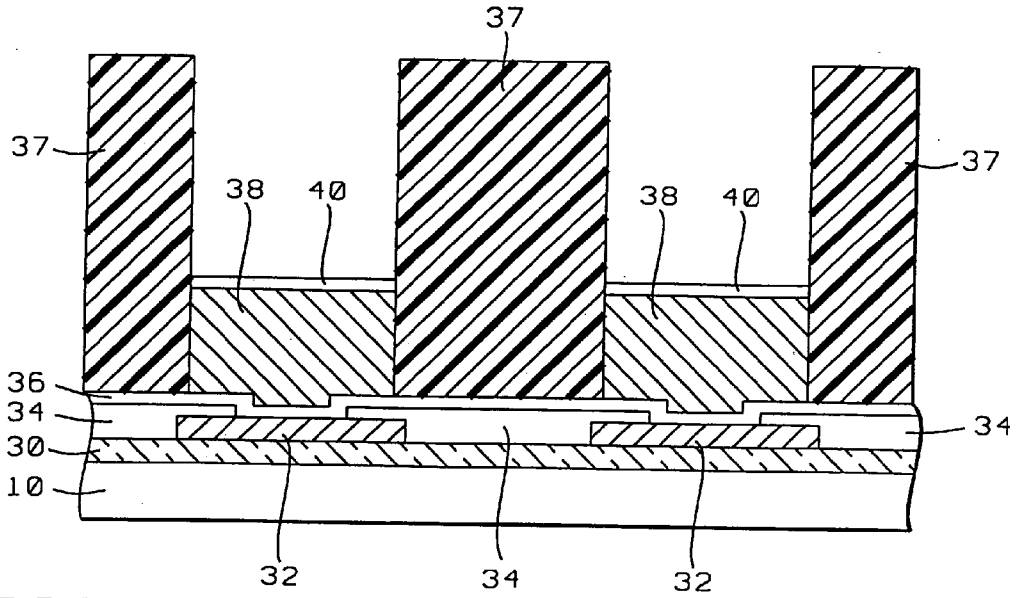
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FIG. 9

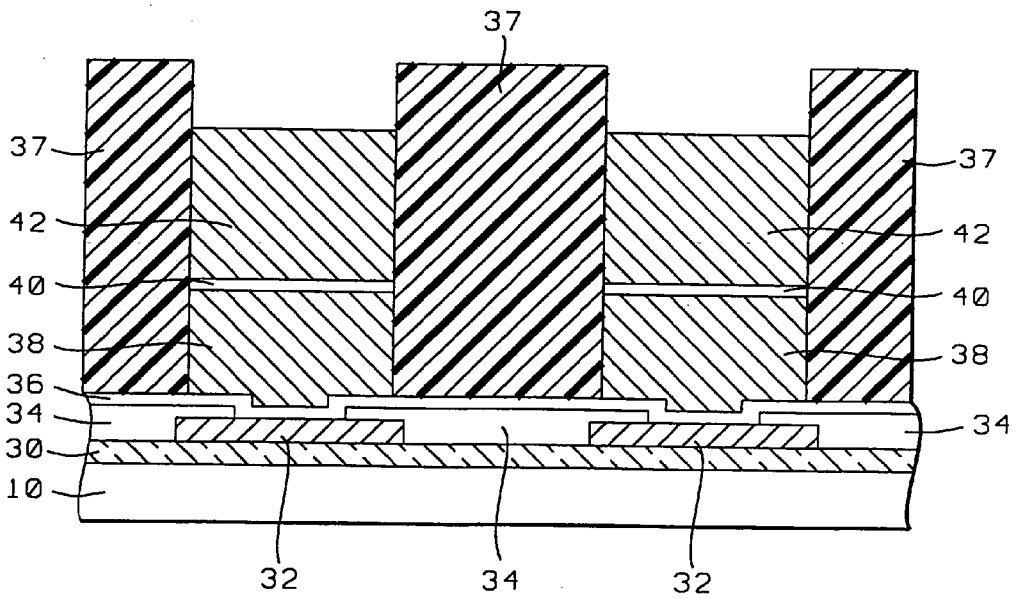
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FIG. 10

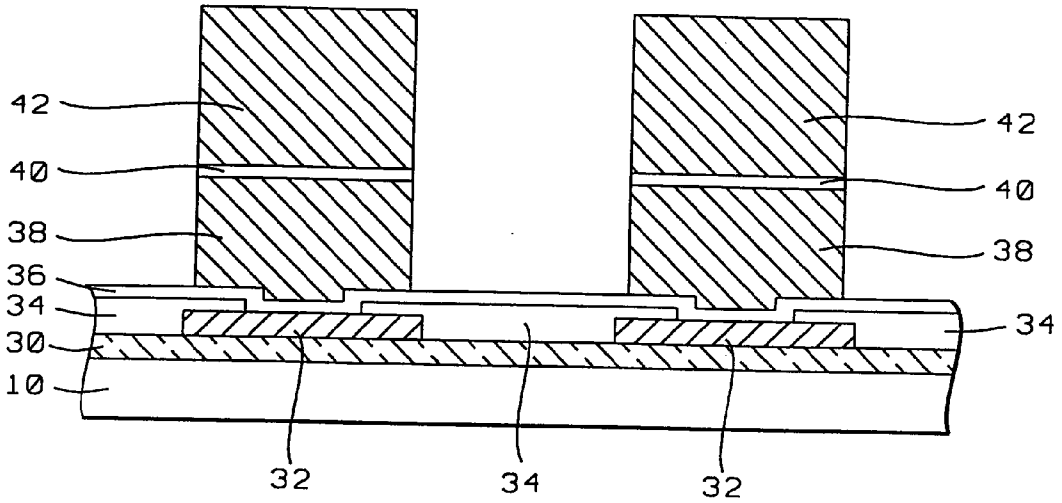
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FIG. 11

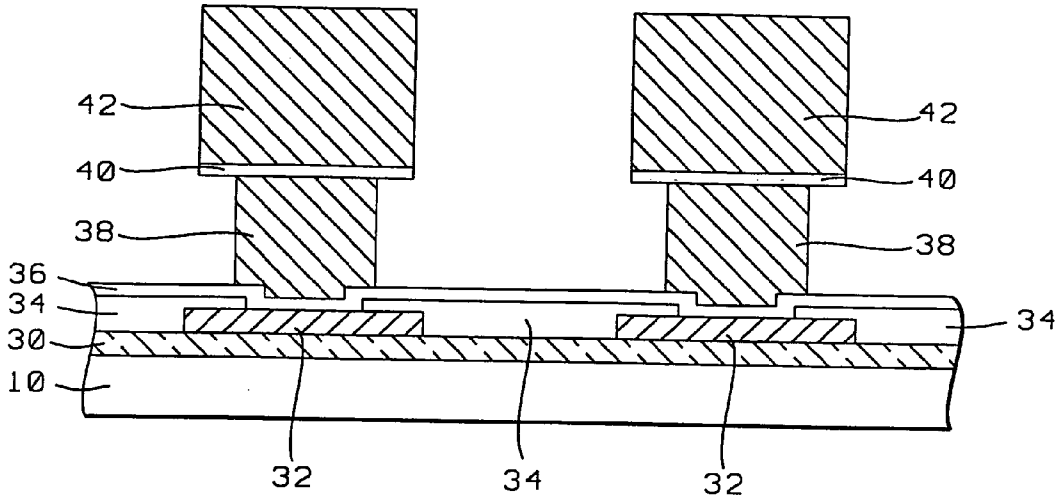
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FIG. 12

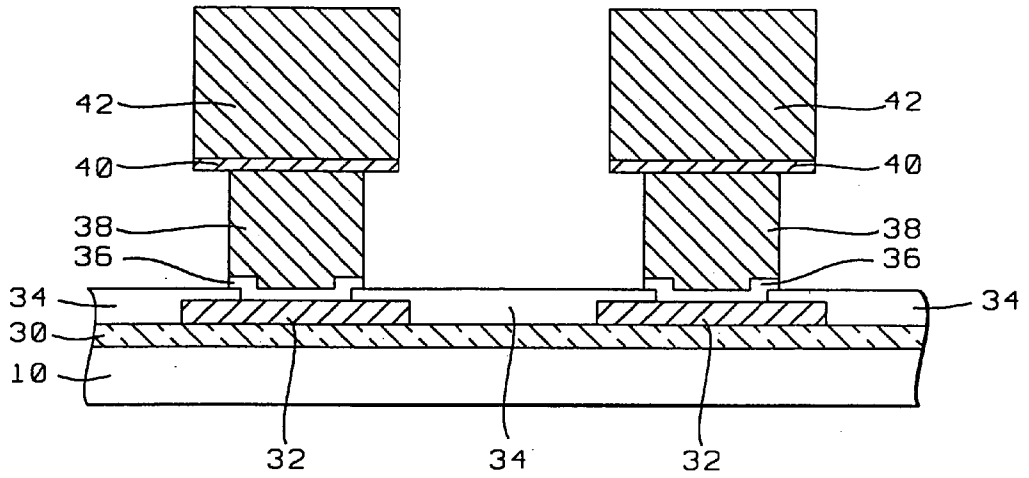
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FIG. 13

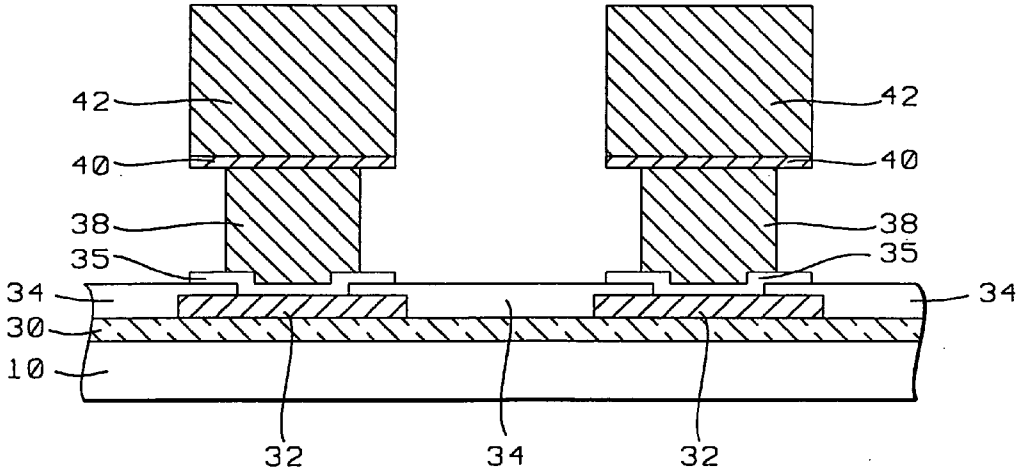
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FIG. 14

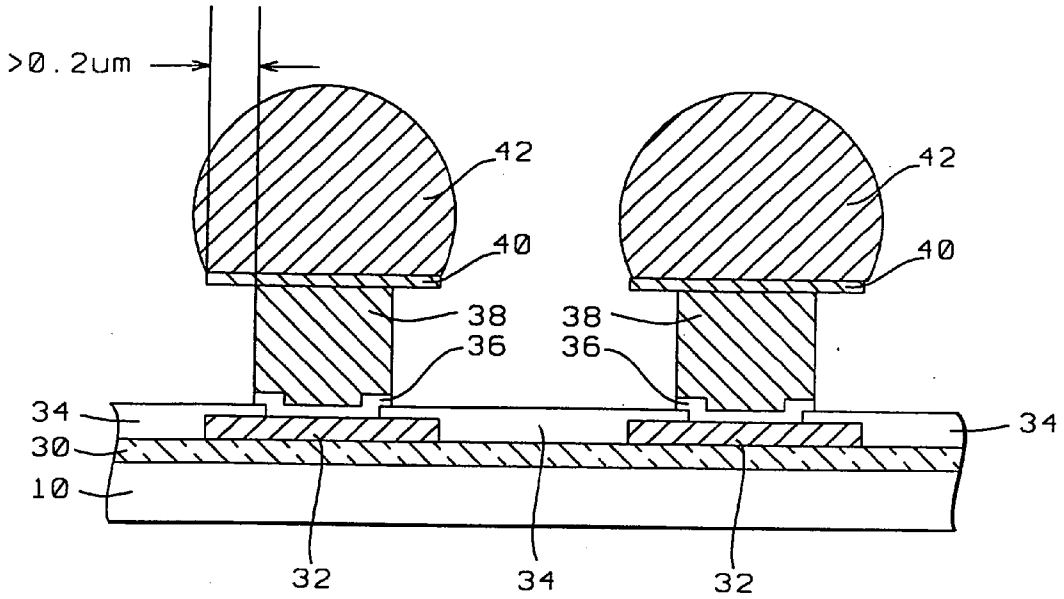
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FIG. 15

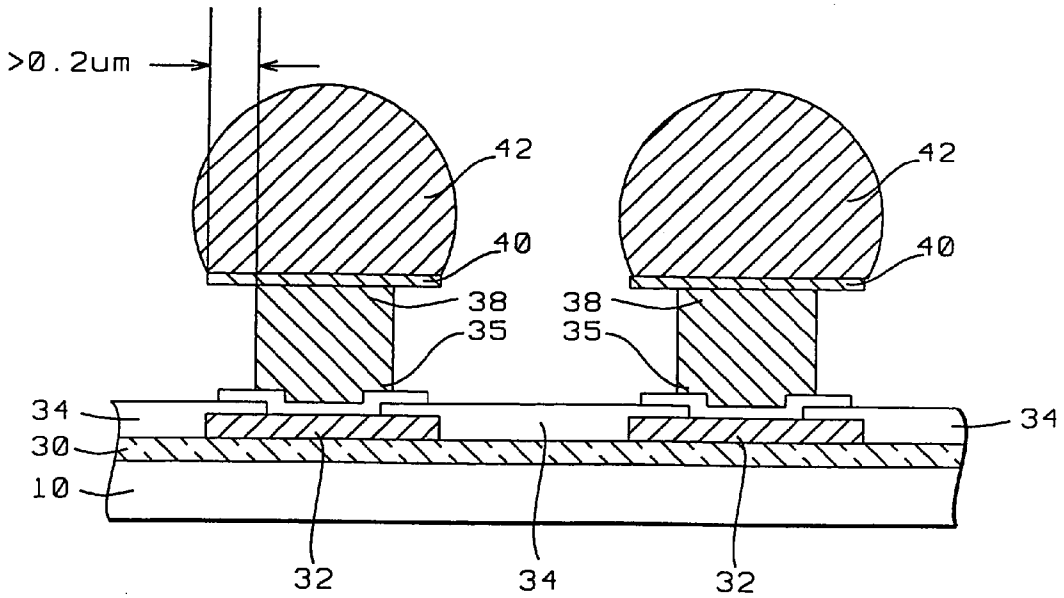
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FIG. 16

LOW FABRICATION COST, FINE PITCH AND HIGH RELIABILITY SOLDER BUMP

[0001] This application is a continuation of application Ser. No. 11/930,998, filed on Oct. 31, 2007, now pending, which is a continuation of application Ser. No. 10/935,451, filed on Sep. 7, 2004, now pending, which is a division of application Ser. No. 09/798,654, filed on Mar. 5, 2001, now Pat. 6,818,545.

BACKGROUND OF THE INVENTION

[0002] (1) Field of the Invention

[0003] The invention relates to the fabrication of integrated circuit devices, and more particularly, to a method of creating a reliable, fine pitch solder bump at low cost.

[0004] (2) Description of the Prior Art

[0005] Semiconductor device packaging has over the years received increased emphasis due to a continued decrease in semiconductor device feature size, a decrease that is driven by the dual requirements of improved device performance and reduced device manufacturing cost. This trend has led to a significant increase in semiconductor device density, which places increased emphasis on device or package I/O capabilities. The metal connections, which connect the Integrated Circuit to other circuits or to system components, have therefore become more important and can, with further miniaturization of the semiconductor device, have an increasingly negative impact on circuit performance. Increasing parasitic capacitance and resistance of the metal interconnections can significantly degrade chip performance. Of most concern in this respect is the voltage drop along the power and ground buses and the RC delay of the critical signal paths. Attempts to reduce the resistance by using wider metal lines result in higher capacitance of these wires.

[0006] One of the approaches that has been taken to solve these packaging problems is to develop low resistance metals (such as copper) for the interconnect wires, while low dielectric constant materials are being used in between signal lines. Another approach to solve problems of I/O capability has been to design chips and chip packaging techniques that offer dependable methods of increased interconnecting of chips at a reasonable manufacturing cost. This has led to the development of Flip Chip Packages.

[0007] Flip-chip technology fabricates bumps (typically Pb/Sn solders) on Al pads on the chips and interconnects the bumps directly to the package media, which are usually ceramic or plastic based. The flip-chip is bonded face down to the package medium through the shortest paths. These technologies can be applied not only to single-chip packaging, but also to higher or integrated levels of packaging in which the packages are larger, and to more sophisticated substrates that accommodate several chips to form larger functional units.

[0008] The flip-chip technique, using an array of I/O interconnects has the advantage of achieving the highest density of interconnection to the device combined with a very low inductance interconnection to the package. However, pre-testability, post-bonding visual inspection, and Coefficient of Thermal Expansion (CTE) matching to avoid solder bump fatigue are still challenges. In mounting several packages together, such as surface mounting a ceramic package to a plastic board, the TCE mismatch can cause a large thermal stress on the solder-lead joints that can lead to joint breakage caused by solder fatigue from temperature cycling operations.

[0009] Prior Art substrate packaging uses ceramic and plastic flip chip packaging. Ceramic substrate packaging is expensive and has proven to limit the performance of the overall package. Recent years has seen the emergence of plastic substrate flip chip packaging, this type of packaging has become the main stream design and is frequently used in high volume flip chip package fabrication. The plastic substrate flip chip package performs satisfactorily when used for low-density flip chip Integrated Circuits (IC's). If the number of pins emanating from the IC is high, that is in excess of 350 pins, or if the number of pins coming from the IC is less than 350 but the required overall package size is small, the plastic flip chip structure becomes complicated and expensive. This can be traced to the multi-layer structure used to create the plastic flip chip package. This multi-layer structure results in a line density within the package of typically 2-3 mil range. This line density is not sufficiently high for realizing the fan out from the chip I/O to the solder balls on the package within a single layer, leading to the multi-layer approach. The multi-layer approach brings with it the use of relatively thick (50 to 75 micrometers) dielectric layers, these layers have a Coefficient of Thermal Expansion (CTE) that is considerably higher than the CTE of the laminate board on which the plastic flip chip package is mounted. To counteract this difference in CTE's the overall package must be (thermally and mechanically) balanced resulting in the use of additional material and processing steps to apply these materials, increasing the cost of the Ball Grid Array (BGA) package and creating a yield detractor.

[0010] In creating semiconductor devices, the technology of interconnecting devices and device features is a continuing challenge in the era of sub-micron devices. Bond pads and solder bumps are frequently used for this purpose, whereby continuous effort is dedicated to creating bond pads and solder bumps that are simple, reliable and inexpensive.

[0011] Bond pads are generally used to wire device elements and to provide exposed contact regions of the die. These contact regions are suitable for wiring the die to components that are external to the die. An example is where a bond wire is attached to a bond pad of a semiconductor die at one end and to a portion of a Printed Circuit Board at the other end of the wire. The art is constantly striving to achieve improvements in the creation of bond pads that simplify the manufacturing process while enhancing bond pad reliability.

[0012] Materials that are typically used for bond pads include metallic materials, such as tungsten and aluminum, while heavily doped polysilicon can also be used for contacting material. The bond pad is formed on the top surface of the semiconductor device whereby the electrically conducting material is frequently embedded in an insulating layer of dielectric. In using polysilicon as the bond pad material, polysilicon can be doped with an n-type dopant for contacting N-regions while it can be doped with p-type dopant for contacting P-regions. This approach of doping avoids inter-diffusion of the dopants and dopant migration. It is clear that low contact resistance for the bond pad area is required while concerns of avoidance of moisture or chemical solvent absorption, thin film adhesion characteristics, delamination and cracking play an important part in the creation of bond pads.

[0013] The conventional processing sequence that is used to create an aluminum bond pad starts with a semiconductor surface, typically the surface of a silicon single crystalline substrate. A layer of Intra Metal Dielectric (IMD) is deposited over the surface, a layer of metal, typically aluminum, is deposited over the surface of the layer of IMD. The layer of metal is patterned and etched typically using a layer of photoresist and conventional methods of photolithography and etching. After a bond pad has been created in this manner, a layer of passivation is deposited over the layer of IMD. An opening that aligns with the bond pad is created in the layer of passivation, again using methods of photolithography and etching.

[0014] A conventional method that is used to create a solder bump over a contact pad is next highlighted. FIGS. **1** through **4** show an example of one of the methods that is used to create an interconnect bump. A semiconductor surface **10** has been provided with a metal contact pad **14**, the semiconductor surface **10** is protected with a layer **12** of passivation. An opening **19** has been created in the layer **12** of passivation, the surface of the metal contact pad **14** is exposed through this opening **19**. Next, FIG. **2**, a dielectric layer **16** is deposited over the surface of the layer **12** of passivation. The layer **16** of dielectric is patterned and etched, creating an opening **21** in the layer **16** of dielectric that aligns with the metal pad **14** and that partially exposes the surface of the metal pad **14**. A layer **18** of metal, typically using Under-Bump-Metallurgy (UBM), is created over the layer **16** of dielectric, layer **18** of metal is in contact with the surface of the metal pad **14** inside opening **21**. The region of layer **18** of metal that is above the metal pad **14** will, at a later point in the processing, form a pedestal over which the interconnect bump will be formed. This pedestal can be further extended in a vertical direction by the deposition and patterning of one or more additional layers that may contain a photoresist or a dielectric material, these additional layers are not shown in FIG. **2**. These layers essentially have the shape of layer **16** and are removed during one of the final processing steps that is applied for the formation of the interconnect bump.

[0015] A layer of photoresist (not shown) is deposited, patterned and etched, creating an opening that aligns with the contact pad **14**. A layer **20** of metal, such as copper or nickel, FIG. **3**, that forms an integral part of the pedestal of the to be created interconnect bump, is next electroplated in the opening created in the layer of photoresist and on the surface of the layer **18** of metal, whereby the layer **18** serves as the lower electrode during the plating process. Layer **20** in prior art applications has a thickness of between about 1 and 10 micrometers with a typical value of about 5 micrometers. The final layer **22** of solder is electroplated on the surface of layer **20**. The patterned layer of photoresist is then removed.

[0016] The layer **18** of metal is next etched, FIG. **4**, leaving in place only the pedestal for the interconnect bump. During this etch process the deposited layers **20** and **22** serve as a mask. If, as indicated above, additional layers of dielectric or photoresist have been deposited for the further shaping of pedestal **18** in FIG. **2**, these layers are also removed at this time.

[0017] A solder paste or flux (not shown) is now applied to the layer **22** of solder, the solder **22** is melted in a reflow surface typically under a nitrogen atmosphere, creating the spherically shaped interconnect bump **22** that is shown in FIG. **4**.

[0018] In addition to the above indicated additional layers of dielectric or photoresist that can be used to further shape the pedestal of the interconnect bump, many of the applications that are aimed at creating interconnect bumps make use of layers of metal that serve as barrier layers or that have other specific purposes, such as the improvement of adhesion of the various overlying layers or the prevention of diffusion of materials between adjacent layers. These layers collectively form layer **18** of FIG. **4** and have, as is clear from the above, an effect on the shape of the completed bump and are therefore frequently referred to as Ball Limiting Metal (BLM) layer. Frequently used BLM layers are successive and overlying layers of chrome, copper and gold, whereby the chrome is used to enhance adhesion with an underlying aluminum contact pad, the copper layer serves to prevent diffusion of solder materials into underlying layers while the gold layer serves to prevent oxidation of the surface of the copper layer. The BLM layer is layer **18** of FIGS. **2** through **4**.

[0019] Increased device density brings with it increased closeness of components and elements that are part of the created semiconductor devices. This increased closeness is expressed as a reduction in the spacing or "pitch" between elements of a semiconductor device. State-of-the-art technology uses solder bumps having a pitch of about 200 micrometers, which imposes a limitation on further increasing device density. The limitation in further reducing the pitch of solder bumps is imposed by concerns of reliability, which impose a relatively large ball size for the solder bump. This relatively large solder ball restricts further reducing the solder ball pitch.

[0020] In the majority of applications, solder bumps are used as interconnections between I/O bond pads and a substrate or printed circuit board. Large solder balls bring with it high standoff since a solder ball with high standoff has better thermal performance (CTE mismatching is easier to avoid resulting in reduced thermal stress on the solder balls). Large solder balls are therefore required in order to maintain interconnect reliability. Low-alpha solder is applied to avoid soft error (electrical or functional errors) from occurring, thereby eliminating the potential for inadvertent memory discharge and incorrect setting of the voltage (1 or 0).

[0021] U.S. Pat. No. 6,162,652 (Dass et al.) provides for the testing of an integrated circuit device including depositing a solder bump on a surface of a bond pad.

[0022] U.S. Pat. No. 5,756,370 (Farnworth et al.) provides a compliant contact system for making temporary connection with a semiconductor die for testing and a method for fabricating the pliable contact system.

[0023] U.S. Pat. No. 5,554,940 (Hubacker) addresses the probing of semiconductor devices that have been provided with contact bumps and the formation of peripheral test pads.

[0024] U.S. Pat. No. 5,665,639 (Seppala et al.), U.S. Pat. No. 6,051,450 (Ohsawa et al.) and U.S. Pat. No. 5,882,957 (Lin) show related bump processes.

[0025] U.S. Pat. No. 5,633,535 (Chao et al.) shows a pedestal process using dry resist.

[0026] U.S. Pat. No. 6,103,552 (Lin) provides a process and package for achieving wafer scale packaging, which includes formation of a solder bump.

SUMMARY OF THE INVENTION

[0027] A principal objective of the invention is to provide a method of creating a fine-pitch solder bump.

[0028] Another objective of the invention is to provide a method of creating smaller solder bumps, further allowing for the creation of fine-pitched solder bumps.

[0029] Another objective of the invention is to provide a cost-effective method to create a fine-pitch solder bump of high reliability, due to the increased height of the solder bump. This objective is based on the believe that solder bump reliability improves proportionally to the square of the distance between the solder ball and the underlying substrate.

[0030] Another objective of the invention is to provide a cost-effective way of creating a solder bump. This cost-effective way is realized by using standard solder material and therewith eliminating the need for expensive "low-.alpha. solder".

[0031] Another objective of the invention is to provide a cost-effective method of creating a fine-pitch solder bump by reducing the alpha-effect on memory products.

[0032] Another objective of the invention is to provide a method of creating solder bumps which allows an easy method of cleaning flux after the process of creating the solder bump has been completed.

[0033] Another objective of the invention is to provide a method of creating solder bumps which allows easy application of underfill.

[0034] In accordance with the process of the invention, a contact pad is formed on a semiconductor surface, overlying a layer of dielectric. A layer of passivation is deposited over the layer of dielectric for the protection of the contact pad, an opening is created in the layer of passivation that partially exposes the surface of the contact pad. A barrier layer is deposited over the layer of passivation including the opening created in the layer of passivation. A column of three layers of metal is formed overlying the barrier layer and aligned with the contact pad and having a diameter that is about equal to the surface of the contact pad. The three metal layers of the column comprise, in succession when proceeding from the layer that is in contact with the barrier layer, a layer of pillar metal, a layer of under bump metal and a layer of solder metal. The layer of pillar metal is reduced in diameter, the barrier layer is selectively removed from the surface of the layer of passivation after which reflowing of the solder metal completes the solder bump of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

[0035] FIGS. **1** through **4** show a prior art method of creating a solder bump overlying a point of electrical contact, as follows:

[0036] FIG. **1** shows a cross section of a semiconductor surface on the surface of which a contact pad has been created, the semiconductor surface is covered with a patterned layer of passivation.

[0037] FIG. **2** shows the cross section of FIG. **1** after a patterned layer of dielectric and a layer of metal have been created on the semiconductor surface.

[0038] FIG. **3** shows a cross section of FIG. **2** after a layer of bump metal and solder compound have been selectively deposited.

[0039] FIG. **4** show a cross section after excessive layers have been removed from the semiconductor surface and after the solder has been reflowed, forming the interconnect bump.

[0040] FIGS. **5** through **16** address the invention, as follows:

[0041] FIGS. **5** and **6** show a cross section of completed solder bumps of the invention.

[0042] FIG. **7** shows a cross section of a semiconductor surface, a layer of dielectric has been deposited, metal pads have been created, a layer of passivation has been deposited and patterned, a layer of barrier material has been deposited.

[0043] FIG. **8** shows a cross section after a patterned layer of photoresist has been created over the structure of FIG. **7**.

[0044] FIG. **9** shows a cross section after pillar metal has been created aligned with the metal pads, under bump metal has been deposited over the surface of the pillar metal.

[0045] FIG. **10** shows a cross section after solder metal has been plated over the under bump metal.

[0046] FIG. **11** shows a cross section after the patterned layer of photoresist has been removed from the surface.

[0047] FIG. **12** shows a cross section after the diameter of the pillar metal has been reduced.

[0048] FIG. **13** shows a cross section after the barrier layer has been etched using isotropic etching, creating a first profile.

[0049] FIG. **14** shows a cross section after the barrier layer has been etched using anisotropic etching or RIE, creating a second profile.

[0050] FIG. **15** shows a cross-section after the solder metal of the first profile has been reflowed.

[0051] FIG. **16** shows a cross-section after the solder metal of the second profile has been reflowed.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0052] Referring now specifically to FIG. **5**, there is shown a cross section of completed solder bumps of the invention having a first profile. The term profile refers to the difference in which, during one of the final steps of the creation of the solder bumps, the layer of barrier metal is etched.

[0053] For the first profile of the solder bumps of the invention, an isotropic etch of the exposed barrier metal is performed, removing the exposed barrier metal except for where this barrier metal underlies the pillar metal of the invention.

[0054] For the second profile of the solder bumps of the invention, an anisotropic etch of the exposed barrier metal is performed, removing the exposed barrier metal except where the barrier metal is shielded from the anisotropic etch by the solder bump, prior to reflow of the solder bump.

[0055] Shown in cross section in FIG. **5** is the first profile of the solder bump of the invention, the elements of this solder bump are:

[0056] **10**, the semiconductor surface over which the solder bump is created, typically the surface of a silicon semiconductor substrate

[0057] **30**, a layer of dielectric that has been deposited over the semiconductor surface **10**

[0058] **32**, contact pads that have been created on the surface of the layer **30** of dielectric

[0059] **34**, a patterned layer of passivation that has been deposited over the surface of the layer **30** of dielectric; openings have been created in the layer **34** of passivation, partially exposing the surface of contact pads **32**

[0060] **36**, an isotropically etched layer of barrier metal; because this layer of barrier metal has been isotropically etched, the barrier metal has been completely removed from the surface of the layer **34** of passivation except where the barrier metal is covered by the overlying pillar metal (**38**) of the solder bump

[0061] **38**, the pillar metal of the solder bump

[0062] **40**, a layer of under bump metal created overlying the pillar metal **38** of the solder bump

[0063] **42**, the solder metal.

[0064] Shown in cross section in FIG. **6** is the second profile of the solder bump of the invention, the elements of this solder

bump are the same as the elements that have been described above for the first profile of the solder bump of the invention with the exception of layer **35** which is an anisotropically etched layer of barrier metal which, due to the nature of the anisotropic etch, protrudes for the pillar metal **38** as shown in the cross section of FIG. **6**.

[0065] FIGS. **7** through **16** provide detail of the process of the invention which leads to the solder bumps that have been shown in cross section in FIGS. **5** and **6**.

[0066] FIG. **7** shows a cross section of substrate **10** on the surface, the following elements are highlighted:

[0067] **10**, a silicon substrate over the surface of which metal contact pads **32** have been created

[0068] **30**, a layer of dielectric that has been deposited over the surface of substrate **10**

[0069] **32**, the metal contact pads, typically comprising aluminum, created over the surface of the layer **30** of dielectric

[0070] **34**, a layer of passivation that has been deposited over the surface of the layer **30** of dielectric. Openings have been created in the layer **34** of passivation that align with the metal contact pads **32**, partially exposing the surface of the contact pads **32**

[0071] **36**, a layer of barrier metal that has been created over the surface of layer **34** of passivation, including the openings that have been created in the layer **34** of passivation, contacting the underlying contact pads **32**.

[0072] As dielectric material for layer **30** can be used any of the typically applied dielectrics such as silicon dioxide (doped or undoped), silicon oxynitride, parylene or polyimide, spin-on-glass, plasma oxide or LPCVD oxide. The material that is used for the deposition of layer **30** of dielectric of the invention is not limited to the materials indicated above but can include any of the commonly used dielectrics in the art.

[0073] The creation of metal contact pads **32** can use conventional methods of metal rf sputtering at a temperature between about 100 and 400 degrees C. and a pressure between about 1 and 100 mTorr using as source for instance aluminum-copper material (for the creation of aluminum contact pads) at a flow rate of between about 10 and 400 sccm to a thickness between about 4000 and 11000 Angstrom. After a layer of metal has been deposited, the layer must be patterned and etched to create the aluminum contact pads **32**. This patterning and etching uses conventional methods of photolithography and patterning and etching. A deposited layer of AlCu can be etched using Cl_2/Ar as an etchant at a temperature between 50 and 200 degrees C., an etchant flow rate of about 20 sccm for the Cl_2 and 1000 sccm for the Ar, a pressure between about 50 mTorr and 10 Torr, a time of the etch between 30 and 200 seconds.

[0074] In a typical application insulating layers, such as silicon oxide and oxygen-containing polymers, are deposited using Chemical Vapor Deposition (CVD) technique over the surface of various layers of conducting lines in a semiconductor device or substrate to separate the conductive interconnect lines from each other. The insulating layers can also deposited over patterned layers of interconnecting lines, electrical contact between successive layers of interconnecting lines is established with metal vias created in the insulating layers. Electrical contact to the chip is typically established by means of bonding pads or contact pads that form electrical interfaces with patterned levels of interconnecting metal lines. Signal lines and power/ground lines can be connected to the bonding pads or contact pads. After the bonding pads or contact pads have been created on the surfaces of the chip, the bonding pads or contact pads are passivated and electrically insulated by the deposition of a passivation layer over the surface of the bonding pads. A passivation layer can contain silicon oxide/silicon nitride (SiO_2/Si_3N_4) deposited by CVD. The passivation layer is patterned and etched to create openings in the passivation layer for the bonding pads or contact pads after which a second and relatively thick passivation layer can be deposited for further insulation and protection of the surface of the chips from moisture and other contaminants and from mechanical damage during assembling of the chips.

[0075] Various materials have found application in the creation of passivation layers. Passivation layer can contain silicon oxide/silicon nitride (SiO_2/Si_3N_4) deposited by CVD, a passivation layer can be a layer of photosensitive polyimide or can comprise titanium nitride. Another material often used for a passivation layer is phosphorous doped silicon dioxide that is typically deposited over a final layer of aluminum interconnect using a Low Temperature CVD process. In recent years, photosensitive polyimide has frequently been used for the creation of passivation layers. Conventional polyimides have a number of attractive characteristics for their application in a semiconductor device structure, which have been highlighted above. Photosensitive polyimides have these same characteristics but can, in addition, be patterned like a photoresist mask and can, after patterning and etching, remain on the surface on which it has been deposited to serve as a passivation layer. Typically and to improve surface adhesion and tension reduction, a precursor layer is first deposited by, for example, conventional photoresist spin coating. The precursor is, after a low temperature pre-bake, exposed using, for example, a step and repeat projection aligner and Ultra Violet (UV) light as a light source. The portions of the precursor that have been exposed in this manner are cross-linked, thereby leaving unexposed regions (that are not cross-linked) over the bonding pads. During subsequent development, the unexposed polyimide precursor layer (over the bonding pads) is dissolved, thereby providing openings over the bonding pads. A final step of thermal curing leaves a permanent high quality passivation layer of polyimide over the substrate.

[0076] The preferred material of the invention for the deposition of layer **34** of passivation is Plasma Enhanced silicon nitride (PE Si_3N_4), deposited using PECVD technology at a temperature between about 350 and 450 degrees C. with a pressure of between about 2.0 and 2.8 Torr for the duration between about 8 and 12 seconds. Layer **32** of PE Si_3N_4 can be deposited to a thickness between about 200 and 800 Angstrom.

[0077] Layer **34** of PE Si_3N_4 is next patterned and etched to create openings in the layer **34** that overlay and align with the underlying contact pads **32**.

[0078] The etching of layer **34** of passivation can use Ar/CF_4 as an etchant at a temperature of between about 120 and 160 degrees C. and a pressure of between about 0.30 and 0.40 Torr for a time of between about 33 and 39 seconds using a dry etch process.

[0079] The etching of layer **34** of passivation can also use He/NF_3 as an etchant at a temperature of between about 80 and 100 degrees C. and a pressure of between about 1.20 and 1.30 Torr for a time of between about 20 and 30 seconds using a dry etch process.

[0080] Barrier layers, such as layer **36**, are typically used to prevent diffusion of an interconnect metal into surrounding layers of dielectric and silicon. Some of the considerations that apply in selecting a material for the barrier layer become apparent by using copper for interconnect metal as an example. Although copper has a relatively low cost and low resistivity, it has a relatively large diffusion coefficient into silicon dioxide and silicon and is therefore not typically used as an interconnect metal. Copper from an interconnect may diffuse into the silicon dioxide layer causing the dielectric to be conductive and decreasing the dielectric strength of the silicon dioxide layer. Copper interconnects should be encapsulated by at least one diffusion barrier to prevent diffusion into the silicon dioxide layer. Silicon nitride is a diffusion barrier to copper, but the prior art teaches that the interconnects should not lie on a silicon nitride layer because it has a high dielectric constant compared with silicon dioxide. The high dielectric constant causes a desired increase in capacitance between the interconnect and the substrate.

[0081] A typical diffusion barrier layer may contain silicon nitride, phosphosilicate glass (PSG), silicon oxynitride, aluminum, aluminum oxide (Al_xO_y), tantalum, Ti/TiN or Ti/W, nionbium, or molybdenum and is more preferably formed from TiN. The barrier layer can also be used to improve the adhesion of the subsequent overlying tungsten layer.

[0082] A barrier layer is preferably about 500 and 2000 angstrom thick and more preferably about 300 angstrom thick and can be deposited using rf sputtering.

[0083] After the creation of barrier layer **36**, a seed layer (not shown in FIG. **7**) can be blanket deposited over the surface of the wafer. For a seed layer that is blanket deposited over the surface of the wafer any of the conventional metallic seed materials can be used. The metallic seed layer can be deposited using a sputter chamber or an Ion Metal Plasma (IMP) chamber at a temperature of between about 0 and 300 degrees C. and a pressure of between about 1 and 100 mTorr, using (for instance) copper or a copper alloy as the source (as highlighted above) at a flow rate of between about 10 and 400 sccm and using argon as an ambient gas.

[0084] FIG. **8** shows a cross section of the substrate after a layer **37** of photoresist has been deposited over the surface of the barrier layer **36**. The layer **37** of photoresist has been patterned and etched, creating openings **31** in the layer **37** of photoresist. Openings **31** partially expose the surface of the barrier layer **36**. Layer **37** of photoresist is typically applied to a thickness of between about 100 and 200 micrometers but more preferably to a thickness of about 150 micrometers.

[0085] Layer **37** of photoresist Layer **37** is typically applied to a thickness of between about 100 and 200 micrometers but more preferably to a thickness of about 150 micrometers. The methods used for the deposition and development of the layer **37** of photoresist uses conventional methods of photolithography. Photolithography is a common approach wherein patterned layers are formed by spinning on a layer of photoresist, projecting light through a photomask with the desired pattern onto the photoresist to expose the photoresist to the pattern, developing the photoresist, washing off the undeveloped photoresist, and plasma etching to clean out the areas where the photoresist has been washed away. The exposed resist may be rendered soluble (positive working) and washed away, or insoluble (negative working) and form the pattern.

[0086] The deposited layer **37** of photoresist can, prior to patterning and etching, be cured or pre-baked further hardening the surface of the layer **37** of photoresist.

[0087] Layer **37** of photoresist can be etched by applying O_2 plasma and then wet stripping by using H_2SO_4, H_2O_2 and NH_4OH solution. Sulfuric acid (H_2SO_4) and mixtures of H_2SO_4 with other oxidizing agents such as hydrogen peroxide (H_2O_2) are widely used in stripping photoresist after the photoresist has been stripped by other means. Wafers to be stripped can be immersed in the mixture at a temperature between about 100 degrees C. and about 150 degrees C. for 5 to 10 minutes and then subjected to a thorough cleaning with deionized water and dried by dry nitrogen. Inorganic resist strippers, such as the sulfuric acid mixtures, are very effective in the residual free removal of highly postbaked resist. They are more effective than organic strippers and the longer the immersion time, the cleaner and more residue free wafer surface can be obtained.

[0088] The photoresist layer **37** can also be partially removed using plasma oxygen ashing and careful wet clean. The oxygen plasma ashing is heating the photoresist in a highly oxidized environment, such as an oxygen plasma, thereby converting the photoresist to an easily removed ash. The oxygen plasma ashing can be followed by a native oxide dip for 90 seconds in a 200:1 diluted solution of hydrofluoric acid.

[0089] FIG. **9** shows a cross section of the substrate **10** after a layer **38** of pillar metal has been deposited (electroplated) over the surface of the layer **36** of barrier material and bounded by openings **31** that have been created in the layer **37** of photoresist. Over the surface of the layers **38** of metal, which will be referred to as pillar metal in view of the role these layers play in the completed structure of the solder bumps of the invention, layers **40** of under bump metal have been deposited using deposition methods such as electroplating.

[0090] Layer **36** preferably comprises titanium or copper and is preferably deposited to a thickness of between about 500 and 2000 angstrom and more preferably to a thickness of about 1000 Angstrom.

[0091] Layer **38** preferably comprise copper and is preferred to be applied to a thickness of between about 10 and 100 micrometers but more preferably to a thickness of about 50 micrometers.

[0092] Layer **40** preferably comprises nickel and is preferred to be applied to a thickness of between about 1 and 10 micrometers but more preferably to a thickness of about 4 micrometers.

[0093] FIG. **10** shows a cross section where the process of the invention has further electroplated layers **42** of solder metal over the surface of layers **40** of under bump metal (UBM) and bounded by the openings **31** that have been created in the layer **37** of photoresist.

[0094] Layer **40** of UBM, typically of nickel and of a thickness between about 1 and 10 micrometers, is electroplated over the layer **38** of pillar metal. The layer **42** of bump metal (typically solder) is electroplated in contact with the layer **40** of UBM to a thickness of between about 30 and 100 micrometers but more preferably to a thickness of about 50 micrometers. The layers **38**, **40** and **42** of electroplated metal are centered in the opening **31** that has been created in the layer **37** of photoresist.

[0095] In the cross section that is shown in FIG. **11**, it is shown that the patterned layer **37** of photoresist has been removed from above the surface of the barrier layer **36**. The previously highlighted methods and processing conditions for the removal of a layer of photoresist can be applied for the purpose of the removal of layer **37** that is shown in cross section in FIG. **11**. The invention further proceeds with the partial etching of the pillar metal **38**, as shown in cross section in FIG. **12**, using methods of wet chemical etching or an isotropic dry etch, selective to the pillar metal material. It is clear that, by adjusting the etching parameters, of which the

time of etch is most beneficial, the diameter of the pillar metal **38** can be reduced by almost any desired amount. The limitation that is imposed on the extent to which the diameter of the pillar metal **38** is reduced is not imposed by the wet etching process but by concerns of metal bump reliability and functionality. Too small a remaining diameter of the pillar metal **38** will affect the robustness of the solder bumps while this may also have the affect of increasing the resistance of the metal bump.

[0096] The final two processing steps of the invention, before the solder metal is reflowed, are shown in the cross section of FIGS. **13** and **14** and affect the etching of the exposed surface of the barrier layer **36**. Using isotropic etching, FIG. **13**, the exposed barrier layer is completely removed as is shown in FIG. **13**. Using anisotropic etching, FIG. **14**, the etching of the barrier layer is partially impeded by the presence of the columns **42** of solder metal.

[0097] It is believed that the undercut shape of pillar **38** will prevent wetting of pillar **38** and the UBM layer **40** during subsequent solder reflow. It is also believed that exposure to air will oxidize the sidewalls of pillar **38** and UBM layer **40** and therefore prevent wetting of these surfaces during subsequent solder reflow. Optionally, the sidewalls of pillar **38** and UBM layer **40** may be further oxidized by, for example, a thermal oxidation below reflow temperature of about 240 degrees C. such as heating in oxygen ambient at about 125 degrees C.

[0098] FIGS. **15** and **16** show the final cross section of the solder bump of the invention after the solder metal has been reflowed. FIG. **15** corresponds to FIG. **13** while FIG. **16** corresponds to FIG. **14**, this relating to the etch in the barrier layer **36** that has been explained using FIGS. **13** and **14**. It is noted that the etched layer **36** of barrier material that is shown in cross section in FIG. **15** corresponds to the etched layer of barrier material that is shown in FIG. **13**. The same correspondence exists between FIGS. **16** and **14**.

[0099] The above summarized processing steps of electroplating that are used for the creation of a metal bump can be supplemented by the step of curing or pre-baking of the layer of photoresist after this layer has been deposited.

[0100] To review and summarize the invention:

[0101] prior to and in preparation for the invention, a semiconductor surface is provided, a layer of dielectric has been deposited over the semiconductor surface, a contact pad has been provided on the layer of dielectric, the contact pad has an exposed surface, a layer of passivation has been deposited over a semiconductor surface including the surface of said contact pad, the layer of passivation has been patterned and etched, creating an opening in the layer of passivation, partially exposing the surface of the contact pad, the opening in the layer of passivation is centered with respect to the contact pad

[0102] the invention starts with a barrier layer deposited over the surface of the layer of passivation, making contact with the contact pad through the opening created in the layer of passivation

[0103] a layer of photoresist is deposited over the surface of the barrier layer

[0104] the layer of photoresist is patterned and etched, creating an opening through the layer of photoresist, the opening in the layer of photoresist aligns with and is centered with respect to the contact pad

[0105] in sequence are deposited, bounded by the opening created in the layer of photoresist, a layer of pillar metal, a layer of under bump metal and a layer of solder metal

[0106] the patterned layer of photoresist is removed from the surface of the barrier layer

[0107] the layer of pillar metal is etched, reducing the diameter of the pillar metal

[0108] the barrier layer is etched, using either isotropic or anisotropic etching

[0109] the solder metal is reflowed.

[0110] The invention offers the following advantages:

[0111] ball height is a very important reliability concern; in order to prevent thermal mismatch between overlying layers of a package (such as a semiconductor device and an underlying printed circuit board and the like) it is important to increase the distance between overlying elements; the invention provides this ability

[0112] a larger solder ball (for better thermal or reliability performance) results in increased pitch, this is contrary to state of the art design requirements

[0113] if small solder balls are used without providing height, it is very difficult to underfill the small gaps

[0114] the solder is, using the invention, relatively far removed from the semiconductor device which means that the application of low-alpha solder is not required (alpha-particles create soft errors in memory products, lead is known to emit alpha-particles when lead decays)

[0115] for the pillar metal a metal needs to be selected that has good conductivity and good ductility, such as copper. This is in order to provide improved thermal performance by counteracting thermal stress

[0116] the height of the pillar of the solder bump of the invention is important and should be between about 10 to 100 micrometers in order to achieve objectives of high stand-off

[0117] the metal that is used for the under bump metal layer is important in that this metal must have good adhesion with the overlying solder during solder reflow while this metal must not solve too fast and in so doing form a barrier to the solder; in addition, the UBM metal when exposed to air can form a layer of protective oxide thus preventing solder wetting to the pillar metal around the perimeter of the UBM metal during the reflow process; nickel is therefore preferred for the UBM metal

[0118] Although the invention has been described and illustrated with reference to specific illustrative embodiments thereof, it is not intended that the invention be limited to those illustrative embodiments. Those skilled in the art will recognize that variations and modifications can be made without departing from the spirit of the invention. It is therefore intended to include within the invention all such variations and modifications which fall within the scope of the appended claims and equivalents thereof.

What is claimed is:

1. A chip comprising:

a silicon substrate;

a dielectric layer over said silicon substrate;

an aluminum pad over said dielectric layer;

a topmost insulating layer of said chip over said dielectric layer, wherein an opening in said topmost insulating layer of said chip exposes said aluminum pad, and wherein said topmost insulating layer of said chip is a polymer layer; and

a metal bump on said aluminum pad and on a first top surface of said topmost insulating layer of said chip, wherein said metal bump comprises a metal layer on said aluminum pad, in said opening and on said first top surface, a copper pillar on said metal layer, over said opening and over said first top surface, and a solder over said copper pillar, over said opening and over said first top surface, wherein said solder is connected to said copper pillar, wherein said copper pillar has a height

between 10 and 100 micrometers, and wherein said copper pillar has a second top surface higher than said first top surface and a sidewall not covered by said solder.

2. The chip of claim **1**, wherein said metal layer comprises titanium.

3. The chip of claim **1**, wherein said metal layer comprises tantalum.

4. The chip of claim **1**, wherein said metal layer has a thickness between 500 and 2,000 angstroms.

5. The chip of claim **1**, wherein said metal bump further comprises a nickel layer between said copper pillar and said solder.

6. The chip of claim **1**, wherein said topmost insulating layer of said chip is a polyimide layer.

7. The chip of claim **1** further comprising multiple layers of interconnecting lines, multiple additional insulating layers and multiple metal vias in said multiple additional insulating layers and between said multiple layers of interconnecting lines, wherein said multiple additional insulating layers comprise an oxide, wherein said multiple metal vias are connected to said multiple layers of interconnecting lines, and wherein said aluminum pad provides an electrical interface with said multiple layers of interconnecting lines.

8. The chip of claim **1**, wherein said solder has a thickness between 30 and 100 micrometers.

9. A chip comprising:

a silicon substrate;

a dielectric layer over said silicon substrate;

a metal layer over said dielectric layer, wherein said metal layer comprises an aluminum pad and a metal piece separate from said aluminum pad and neighboring said aluminum pad;

a topmost insulating layer of said chip over said dielectric layer, over said aluminum pad, over said metal piece and in a gap between said aluminum pad and said metal piece, wherein an opening in said topmost insulating layer of said chip is over a contact point of said aluminum pad, and said contact point is at a bottom of said opening, and wherein said topmost insulating layer of said chip is a polymer layer; and

a metal bump on said contact point and on a first top surface of said topmost insulating layer of said chip, wherein said metal bump comprises a titanium-containing layer on said contact point, in said opening and on said first top surface, and a copper pillar over said titanium-containing layer, over said opening and over said first top surface, wherein said copper pillar has a height between 10 and 100 micrometers, and wherein said copper pillar has a second top surface higher than said first top surface and a sidewall not covered by any solder, and wherein said first top surface has a first region directly under said metal bump and directly over said aluminum pad and a second region directly over the middle of said gap, wherein said first region is at a substantially same horizontal level as said second region, and there is no significant step between said first region and said second region.

10. The chip of claim **9**, wherein said titanium-containing layer comprises titanium nitride.

11. The chip of claim **9**, wherein said metal bump further comprises a nickel-containing layer on said copper pillar, over said opening and over said first top surface.

12. The chip of claim **9**, wherein said metal bump further comprises a solder over said copper pillar, over said opening and over said first top surface, wherein said solder is connected to said copper pillar.

13. The chip of claim **9**, wherein said topmost insulating layer of said chip is a polyimide layer.

14. The chip of claim **9** further comprising multiple layers of interconnecting lines, multiple additional insulating layers and multiple metal vias in said multiple additional insulating layers and between said multiple layers of interconnecting lines, wherein said multiple additional insulating layers comprise an oxide, wherein said multiple metal vias are connected to said multiple layers of interconnecting lines, and wherein said aluminum pad provides an electrical interface with said multiple layers of interconnecting lines.

15. The chip of claim **12**, wherein said solder has a thickness between 30 and 100 micrometers.

16. A chip comprising:

a silicon substrate;

a dielectric layer over said silicon substrate;

an aluminum pad over said dielectric layer;

a topmost insulating layer of said chip over said dielectric layer, wherein an opening in said topmost insulating layer of said chip exposes said aluminum pad, and wherein said topmost insulating layer of said chip is a polymer layer; and

a metal bump on said aluminum pad and on a first top surface of said topmost insulating layer of said chip, wherein said metal bump comprises a metal layer on said aluminum pad, in said opening and on said first top surface, and a copper pillar on said metal layer, over said opening and over said first top surface, wherein said copper pillar has a height between 10 and 100 micrometers and greater than a transverse dimension of said copper pillar, and wherein said copper pillar has a second top surface higher than said first top surface.

17. The chip of claim **16**, wherein said metal layer comprises titanium.

18. The chip of claim **16**, wherein said metal layer comprises tantalum.

19. The chip of claim **16**, wherein said metal layer has a thickness between 500 and 2,000 angstroms.

20. The chip of claim **16**, wherein said metal bump further comprises an electroplated metal over said copper pillar, over said opening and over said first top surface.

21. The chip of claim **16**, wherein said metal bump further comprises a nickel-containing layer on said copper pillar, over said opening and over said first top surface.

22. The chip of claim **16**, wherein said metal bump further comprises a solder over said copper pillar, over said opening and over said first top surface.

23. The chip of claim **16**, wherein ssaid topmost insulating layer of said chip is a polyimide layer.

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