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(54) **SEMICONDUCTOR PACKAGE SUBSTRATE AND METHODS FOR FORMING SAME, IN PARTICULAR FOR MEMS DEVICES**

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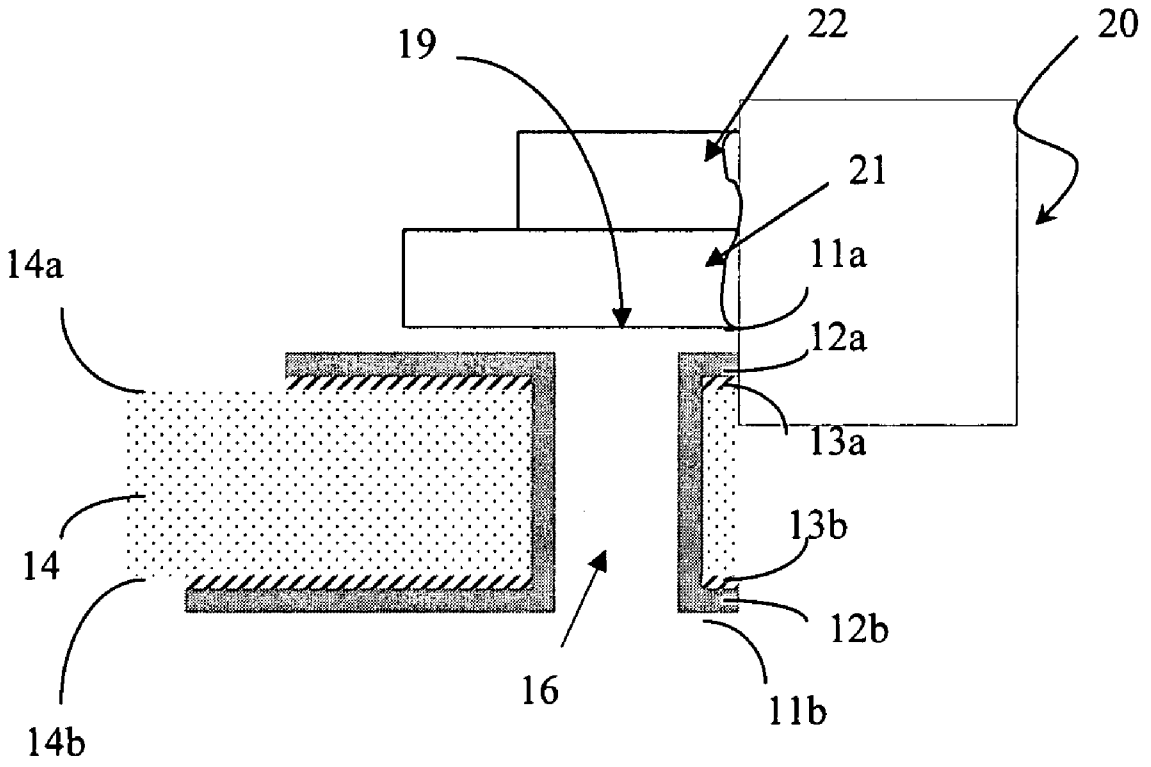
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(57) **ABSTRACT**

A semiconductor package substrate suitable for supporting a damage-sensitive device and a package substrate core having an upper and a lower surface. At least one pair of metal layers coats the upper and lower surfaces of the package substrate core. One pair of solder mask layers coats the outer metal layers of the at least one pair of metal layers. A plurality of vias is formed across the package substrate core and the at least one pair of metal layers. Advantageously, the plurality of vias is substantially distributed according to a homogeneous pattern in an area that is to be covered by the damage-sensitive device. A method for the production of such semiconductor package substrate is also described.



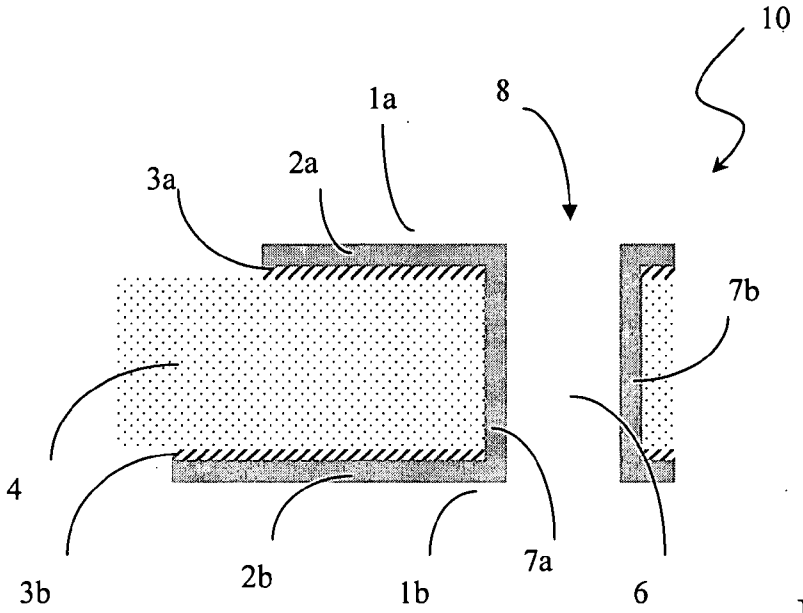


FIG. 1
PRIOR ART

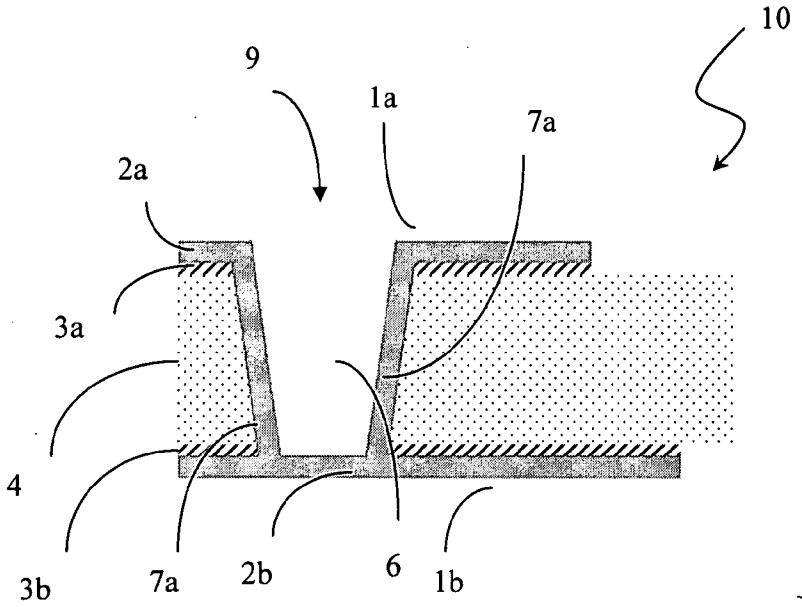


FIG. 2
PRIOR ART

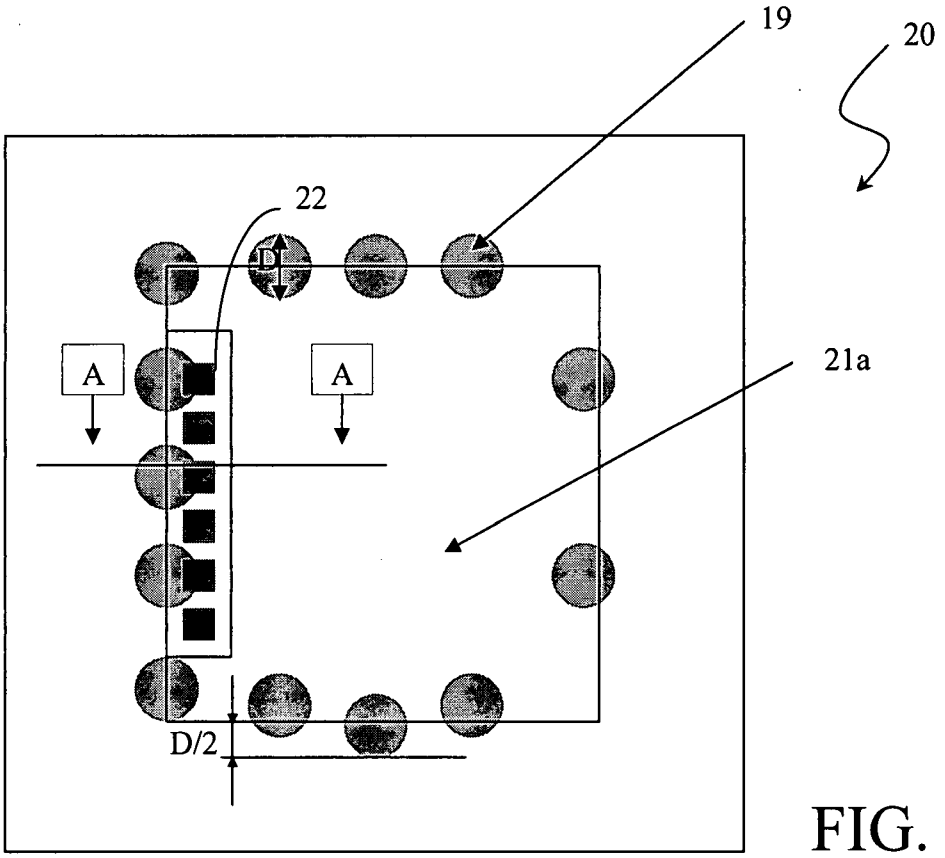

19
20
22
D
A
A
21a
D/2

FIG. 3

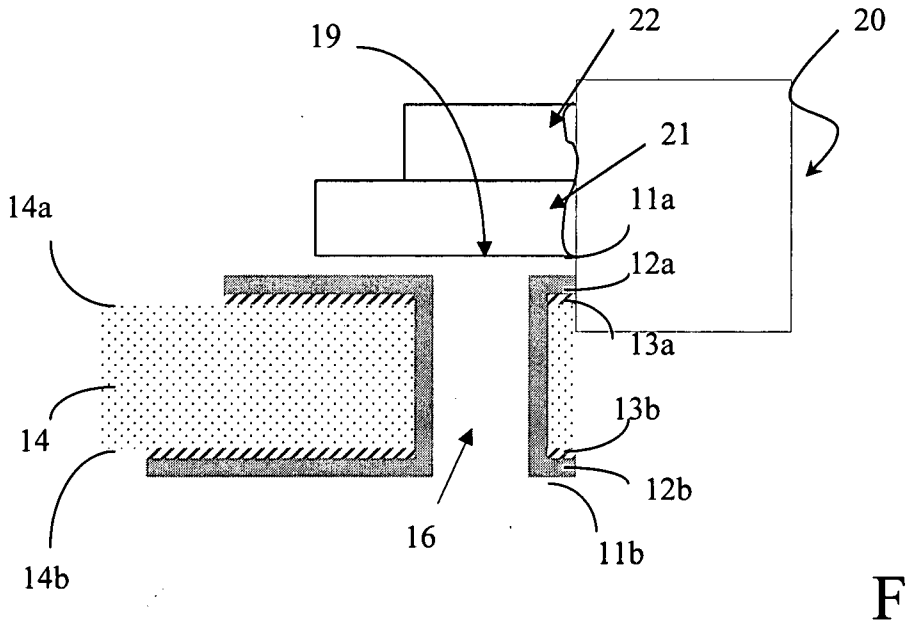

19
22
20
21
11a
14a
12a
13a
13b
14
12b
16
11b
14b

FIG. 4

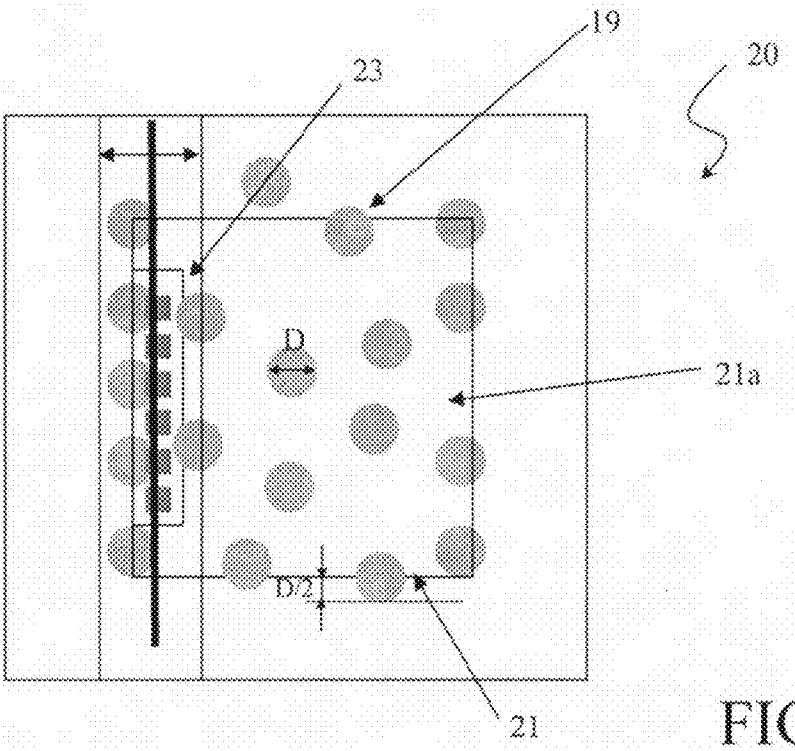


FIG. 5

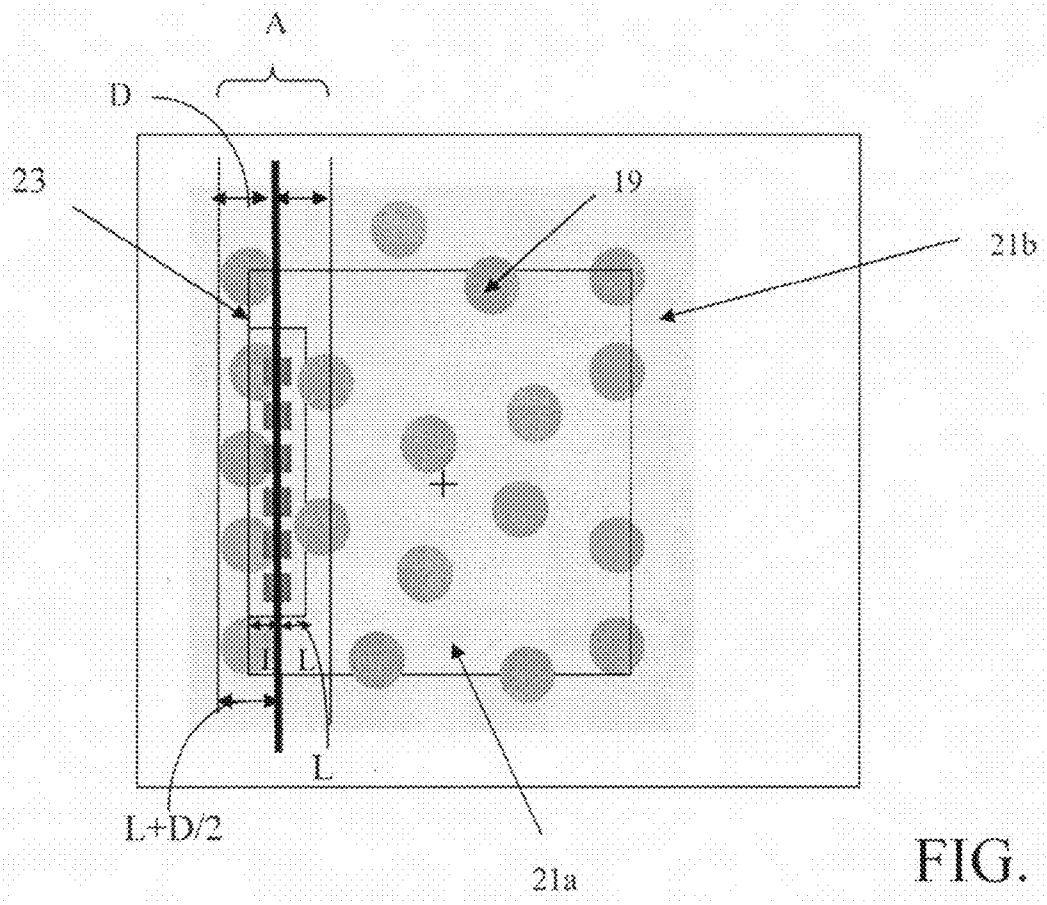


FIG. 6

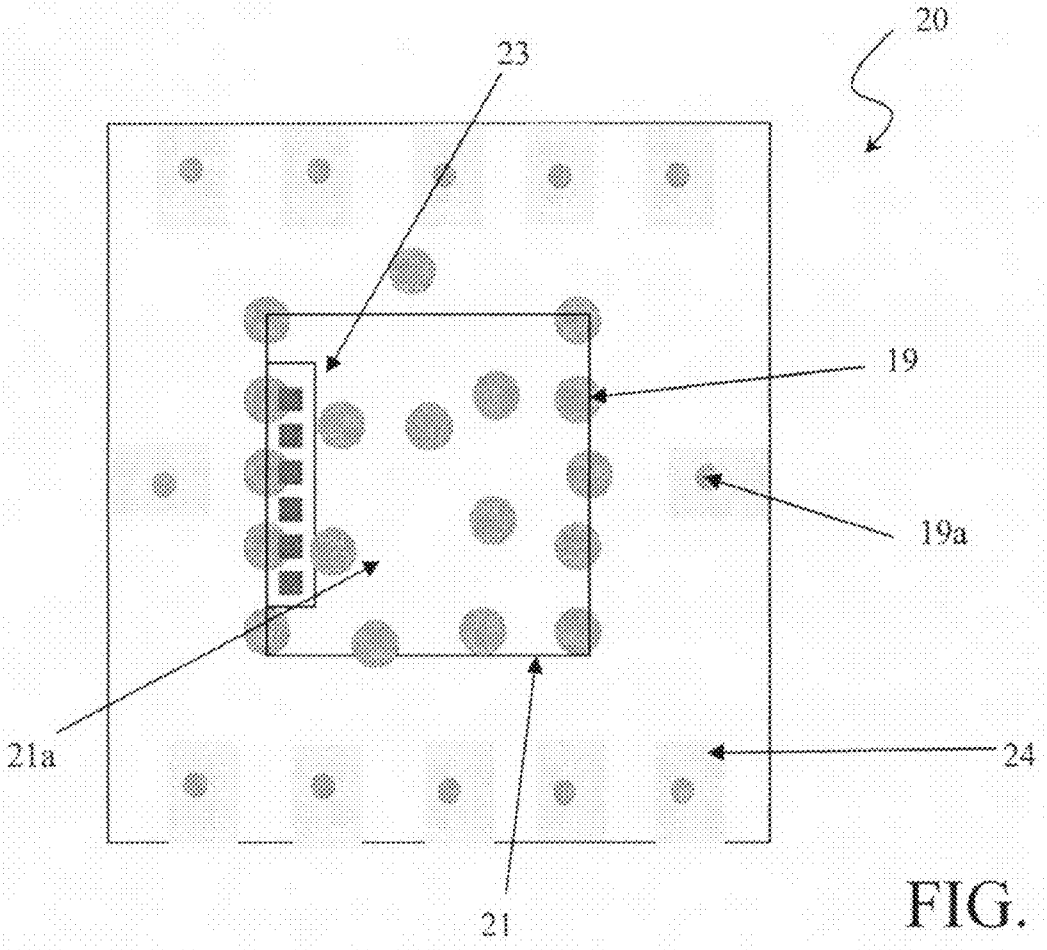


FIG. 7

SEMICONDUCTOR PACKAGE SUBSTRATE AND METHODS FOR FORMING SAME, IN PARTICULAR FOR MEMS DEVICES

PRIORITY CLAIM

[0001] This application claims priority from European patent application No. 06014651.1, filed Jul. 14, 2006, which is incorporated herein by reference.

TECHNICAL FIELD

[0002] Embodiments of the present invention generally relate to semiconductor package substrates and manufacturing methods thereof.

[0003] More in particular, but not exclusively, embodiments of the present invention relate to a land grid array (LGA) and ball grid array (BGA) semiconductor package substrate supporting a micro-electro-mechanical system (MEMS) device, and the following description is made with reference to such a specific technical field for the sole purpose of simplifying the present disclosure.

BACKGROUND

[0004] As it is well known, a micro-electro-mechanical system (MEMS) device is a microdevice that integrates mechanical and electrical functions in a silicon chip realized using lithographic microfabrication techniques.

[0005] The final device is typically composed of a MEMS die and optionally ASICs assembled on top of an organic substrate (e.g., a BT resin) using standard assembly processes. The assembly thus formed is then encapsulated in a resin (molding compound) using standard injection molding technologies.

[0006] In fact, it is well known that integrated circuits (IC) are fabricated on the surface of a semiconductor wafer in layers and later singulated into individual semiconductor devices, or "dice." Since the material of a semiconductor wafer—commonly silicon—tends to be relatively fragile and brittle, dice are usually assembled into protective housings, or "packages," before being interconnected with a printed circuit board (PCB), the package ensuring the interconnection between the dice and the board.

[0007] In the case of MEMS devices, bulk type packages are generally used, such as SO, QFN, cavity (plastic or ceramic).

[0008] Metal layers include patterns of conductive material (usually copper) that are vertically insulated from one another by alternating layers of insulating or dielectric material. Conductive traces are also separated within each layer by an insulating, or dielectric, material. Vertical, conductive tunnels called "vias" typically pass through insulating layers to form conductive pathways between adjacent conductive patterns, such vias thus providing the electrical connection between the metal layers.

[0009] Such vias are to be provided in the package substrate of a die or a MEMS device in order to ensure a correct signal transmission between different metal layers.

[0010] Commonly used in the field are land grid array (LGA) packages wherein a die is mounted on a package substrate and enclosed in a homogenous material molding compound.

[0011] The LGA package is so named because the package substrate has an array of electrical contact pads, or "lands," arranged in a grid pattern on its underside. The lands are brought into electrical contact with the printed circuit board (PCB) generally by vias having polymer interposers, metal tracks or other electrically conductive element for contacting both the lands and the appropriate conductive portions of the PCB below. The PCB is substantially a support board for mounting the LGA/BGA packages, in connection in particular with their package substrates.

[0012] Owing to their structure, LGA packages are highly desirable in those cases where size reduction, performance and cost issues are particularly important.

[0013] The upper surface of a package substrate is surmounted by the silicon die, for example a MEMS device, which can be connected to the pads or to the bond fingers on the top metal layer of the land grid array by wire-bonding. Normally, the die is attached to the package substrate **10** with the aid of an adhesive material such as a glue or a tape.

[0014] The semiconductor devices (e.g., MEMS) can be found in a variety of relations with respect to each other on the integrated circuit, depending on the type of stacking configuration that applies. The devices can thus be found to be side by side, stacked, inversely stacked, etc.

[0015] The semiconductor device is normally encapsulated with a protecting material (normally epoxy resin), or cap or molding compound, to ensure electrical and mechanical protection, in general, as well as to protect against moisture, dust, and other external agents.

[0016] As well as constituting the mechanical support of the die or MEMS device, the package substrate also has a fundamental role from the electrical point of view.

[0017] A standard package substrate **10** is schematically shown in FIG. **1**.

[0018] The substrate **10** is made of a polymeric material (for example, BT resin) core **4** and comprises a top **3***a* and a bottom copper layer **3***b* surrounding the core **4** as well as a top **2***a* and a bottom copper layer **2***b* on the copper layers **3***a* and **3***b*, in turn surrounded by a top **1***a* and a bottom solder-mask **1***b*.

[0019] The number of layers that can be used in the composition of package substrates **10** is variable.

[0020] For a two-layer LGA/BGA substrate, standard thickness values are in the range of 180 to 300 μm, wherein the core is approximately 100 μm or 200 um, each copper layer is 12-28 μm, and each solder mask layer is approximately 25 μm in thickness.

[0021] In the example shown in FIG. **1**, vias are realized by plated through holes or PTH **8** drilled in the core **4** to provide electrical connections between the two copper layers.

[0022] An alternative package substrate is shown in FIG. **2**, the package substrate **10** including vias in pad or VIP **9**. As it is well known, according to the via-in-pad approach, the via is directly placed on the lands of the LGA substrate. The VIP **9** are usually drilled and copper plated, and then filled with a solder mask.

[0023] Typical dimensions of vias are in the range of 100 to 200 μm in diameter.

[0024] The number of vias that are usually formed in the substrate varies according to need and, similarly, their distribution is dependent upon factors such as routing complexity, package or substrate sizes and, in general, design requirements and constraints.

[0025] Along the production line, the assembly of the package can represent quite a critical step for a sensitive electronic device, such as MEMS. The package, in fact, can undergo considerable mechanical stresses, especially during the

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molding step, which can lead to failure by delamination of the cap, and consequent loss of the sealing effect, which in turn affects the quality of performance, in terms of offset stability and drift of the package, upon use.

[0026] In order reduce this technical problem, the package substrate should be of a physical structure such that the metal layers are well-balanced, so that, throughout the production steps, it is less exposed to those mechanical stresses which are damaging to the package itself.

[0027] Such balancing, in fact, enables smoother assembly steps on the substrate and thus leads to the production of a package of longer durability and better long-term performance.

[0028] For this purpose, it is common, for example, to balance the copper layers by means of a copper mesh. Such meshes can have variable sizes, patterns and widths, and can be suitably chosen to match the specific requirements of the package substrate.

[0029] Other known solutions comprise package substrates having an increased thickness in order to enhance their tolerance to the production processes usually employed in the field. In this case, however, the total thickness of the package is also increased, which is obviously undesirable.

[0030] Moreover, in the case of devices that are especially sensitive to the mechanical stresses of the assembly step, in particular the molding step, such as the MEMS devices, such known solutions are still not sufficient to ensure effective balancing and an optimal final packaged device.

[0031] Ideally, a package substrate would be capable of withstanding the mechanical stresses of assembly, in particular of the molding step.

SUMMARY

[0032] According to one embodiment of the present invention, a semiconductor package substrate suitable for supporting a damage-sensitive device includes a package substrate core having an upper and a lower surface. At least one pair of metal layers coats the upper and lower surfaces of the package substrate core. One pair of solder mask layers coats the outer metal layers of the at least one pair of metal layers. A plurality of vias are formed across the package substrate and the at least one pair of metal layers. The plurality of vias is substantially distributed according to a homogeneous pattern in an area that is to be covered by the damage-sensitive device.

[0033] According to another embodiment of the present invention, a method for the production of a semiconductor package substrate suitable for supporting a damage-sensitive device includes providing a package substrate core having an upper and a lower surface, depositing at least one pair of metal layers on the upper and lower surfaces of the package substrate core, forming a plurality of vias formed through the substrate package core and the at least one pair of metal layers, and depositing one pair of solder mask layers on the outer layers of the at least one pair of metal layers. The step of forming the plurality of vias distributes the plurality of vias substantially according to a homogeneous pattern in an area that is to be covered by the damage-sensitive device.

[0034] By distributing the vias according to the patterns of embodiments of the invention, the package substrate is considerably more balanced and stable upon assembly, so that the device is less exposed to delamination, stresses and consequent loss of performance quality upon use.

[0035] Features and advantages of the package substrate and method of forming such a substrate according to embodiments of the invention will appear clearer from the description that follows and here provided for illustrative and non-limiting purposes with reference to the figures below.

BRIEF DESCRIPTION OF THE DRAWINGS

[0036] FIG. **1** is a schematic representation of a package substrate according to the prior art.

[0037] FIG. **2** is a schematic representation of an alternative package substrate according to the prior art.

[0038] FIG. **3** is a schematic representation of a package substrate according to one embodiment of the invention.

[0039] FIG. **4** is a schematic cross section of a package including the package substrate of FIG. **3** cut along line A-A.

[0040] FIG. **5** is a schematic representation of a package substrate according to a second embodiment of the invention.

[0041] FIG. **6** is a schematic representation of the package substrate according to the second embodiment of the invention.

[0042] FIG. **7** is a schematic representation of a package substrate according to a third embodiment of the invention.

DETAILED DESCRIPTION

[0043] The following discussion is presented to enable a person skilled in the art to make and use the invention. Various modifications to the embodiments will be readily apparent to those skilled in the art, and the generic principles herein may be applied to other embodiments and applications without departing from the spirit and scope of the present invention. Thus, the present invention is not intended to be limited to the embodiments shown, but is to be accorded the widest scope consistent with the principles and features disclosed herein.

[0044] With reference to such figures, and in particular with reference to FIGS. **3** to **6**, a package substrate according to one embodiment of the present invention, referred to in its entirety by reference number **20**, will now be described in greater detail also by means of three representative examples concerning package substrates intended to support damage-sensitive devices, such as MEMS devices.

[0045] Components that are functionally or structurally similar or equivalent to those of FIGS. **1** and **2** will be indicated by the same reference numeral, increased by 10.

[0046] The semiconductor package substrate **20** according to this embodiment of the invention includes a core **14** made of BT resin as according to conventional techniques in the field. The core **14** comprises an upper surface **14***a*, whereover a device **21**, in particular a semiconductor device such as a MEMS device, will be supported and an opposite lower surface **14***b*.

[0047] As already described with reference to the prior art examples, both such upper and lower surfaces of the core **14**, **14***a* and **14***b*, are coated with at least one pair of metal layers **12***a*, **13***a* and **12***b*, **13***b*, respectively, on each opposite surfaces.

[0048] Such metal is copper (Cu), with a finishing in NiAu, and the number of layers, which is always an even number, can range from 2 to 8, preferably 2.

[0049] The outer metal layers **12***a* and **12***b* are then coated with one pair of solder mask layers **11***a*, **11***b*, one on each of the opposite outer copper coated surfaces, again, according to conventional techniques.

[0050] A plurality of vias **19** is then formed through the semiconductor package substrate **20** so that the core **14**, and the metal coating layers **12***a*, **12***b*, **13***a*, **13***b* are perforated

throughout. In particular, the vias **19** are preferably provided as plated through holes, or PTH. Then, the solder mask layers are deposited on the semiconductor package substrate **20**.

[0051] According to this embodiment of the invention, the vias **19** are positioned so that they are distributed according to a homogeneous pattern in an area **21***a* that is to be covered by the device **21**.

[0052] In particular, according to the first embodiment of the semiconductor package substrate **20** as shown in FIG. **3**, the vias **19**, are distributed so that they substantially coincide with the outline of the device **21** that the semiconductor package substrate **20** is intended to support. In such embodiment, the number of vias **19** on each side of the outline should be greater than 1. It should be noted that it is not necessary that the number of vias is the same on each side of the outline of the device **21**, as long as they are substantially positioned along such an outline.

[0053] It should be also noted that by substantially what is meant is that the vias are to be positioned in such a way that at least one half of the corresponding via land (i.e., the metallization around the via drill) is positioned inside the area **21***a*.

[0054] As clearly seen in FIG. **3**, when considering round vias having a via land of diameter D, and a straight portion of the area **21***a*, the vias are positioned in such a way that no more than one half of the via land diameter sits outside such area.

[0055] Suitable semiconductor devices **21** can be MEMS, ASICs, and in general all devices sensitive to mechanical stresses, such as MEMS devices.

[0056] A cap or molding compound **22** encapsulating the semiconductor device **21** is also provided.

[0057] In a further embodiment of the semiconductor package substrate **20**, dummy vias are used in those circumstances where the number of vias **19** actually required is smaller than two per outline side.

[0058] According to a second embodiment of the semiconductor package substrate **20** as shown in FIG. **5**, the semiconductor device **21** is small with respect to the number of vias **19** required or with respect to the routing requirements. In such case, a majority of the vias **19** are homogeneously positioned in the area **21***a* that is to be covered by the semiconductor device **21**. In particular, at least two vias **19** are positioned in a security area A surrounding a pad line **23**.

[0059] In fact, it is worth noting that such a pad line **23**, which can be freely positioned within the area **21***a* according to need, is a critical portion of a package comprising the semiconductor device **21**, the delamination of the cap **22** being extremely high in this portion.

[0060] According to this second embodiment of the semiconductor package substrate **20**, the vias **19** are thus distributed in order to ensure an effective "covering" of the critical portion corresponding to the pad line **23**.

[0061] In particular, in the case of small devices and where, owing to routing needs, it is not possible to place vias along the outline of area **21***a*, the majority of vias are positioned in an area **21***b* being bigger than the area **21***a*, preferably 40% bigger than the area **21***a* and centered with it, as shown in FIG. **6**. Moreover according to this second embodiment, at least two vias must be placed over the security area A within a range of ±(L+D/2) from the center of the pad line **23**, where **2**L is the pad opening width of the die and D is the diameter of the via land.

[0062] Also in this case, dummy vias can be added so as to respect these rules.

[0063] A third embodiment of the semiconductor package substrate **20** is shown in FIG. **7**, the number of vias **19** required is too large to be included in the area **21***a* to be covered by the semiconductor device **21**. In this case, the additional vias **19***a* are positioned in lands **24**.

[0064] In one embodiment, such additional vias **19***a* are realized using VIP (vias in pad) technology.

[0065] As above, dummy vias are also used in those circumstances where the number of vias **19** required is smaller than that necessary to provide the best stability.

[0066] Whenever necessary, a combination of the three embodiments described may be used to better meet the specific requirements of the case.

[0067] Embodiments of the present invention also relate to methods for the production of a semiconductor package substrate **20** suitable for supporting a damage-sensitive device **21**. One such method includes providing a package substrate core **14** having an upper and a lower surface, **14***a*, **14***b*. At least one pair of copper layers, **12***a*, **12***b* and **13***a*, **13***b*, is deposited on the upper and lower surfaces, **14***a*, **14***b*, of the core **14**. One pair of solder mask is deposited on one pair of metal, preferably copper, layers, **11***a*, **11***b*, on outer layers, **12***a*, **12***b*, of the at least one pair of copper layers, **12***a*, **12***b* and **13***a*, **13***b*. A plurality of vias **19** are formed through the core **14** and one pair of copper layers, **12***a*, **12***b*, **13***a*, **13***b*.

[0068] The step of forming the plurality of vias **19** may distribute them according to a homogeneous pattern in the area **21***a* that is to be covered by the device **21**. The distribution of the plurality of vias **19** may thus be made as above explained with reference to the embodiments shown in FIGS. **3** to **7**. A damage-sensitive device **21** is then mounted on top of the upper solder mask layer **11***a* and wire connections between the package substrate **20** and the damage-sensitive device **21** are carried out. A semiconductor package including the package substrate **20** and the damage-sensitive **21** may then be sealed with the sealant cap **22**.

EXAMPLE 1

[0069] An LGA/BGA semiconductor package substrate was composed of a BT resin core as according to conventional techniques in the field. The substrate comprised an upper surface, solder mask, destined to support a MEMS device and an opposite lower surface.

[0070] Both such surfaces were then coated with two copper layers on each opposite surfaces according to conventional techniques.

[0071] Eight vias were then formed through the substrate so that the core and the copper layers were perforated throughout. The vias were positioned so that they would be found beneath the outline of the MEMS device it was intended to support, two for each of the four sides of the MEMS device.

[0072] A solder mask was then deposited on the LGA/BGA semiconductor package substrate.

[0073] The MEMS device was then mounted on top of the solder mask layer of the upper core surface and wire connections between the substrate and the MEMS device were carried out.

[0074] The semiconductor package was then sealed with a sealant cap or molding compound.

[0075] It was found that such package gave good functioning performance in the long term in terms of offset stability

and drift, given by the fewer cap delamination and loss of sealing effect risks during assembly, in particular during molding.

EXAMPLE 2

[0076] An LGA/BGA semiconductor package substrate was composed of a BT resin core as according to conventional techniques in the field. The core comprised an upper surface, destined to support a MEMS device and an opposite lower surface.

[0077] Both such surfaces were then coated with two copper layers on each opposite surfaces according to conventional techniques.

[0078] Nineteen vias were then formed through the substrate so that the core and the copper plating layers were perforated throughout. The vias were positioned so that they would be found beneath the outline of the MEMS device it was intended to support, as well as throughout the area within such outline. Two vias were positioned in the area ±300 μm with respect to the pad line.

[0079] A solder mask was then deposited on the LGA/BGA semiconductor package substrate.

[0080] The MEMS device was then mounted on top of the solder mask layer of the upper core surface and wire connections between the substrate and the MEMS device were carried out.

[0081] The semiconductor package was then sealed with a sealant cap or molding compound.

[0082] It was found that such package gave good functioning performance in the long term in terms of offset stability and drift, and an assembly yield increase given by the fewer cap delamination and loss of sealing effect, in particular during molding.

EXAMPLE 3

[0083] An LGA/BGA semiconductor package substrate was composed of a BT resin core as according to conventional techniques in the field. The substrate comprised an upper surface, solder mask, destined to support a MEMS device and an opposite lower surface.

[0084] Both such surfaces were then coated with two copper layers on each opposite surfaces, according to conventional techniques.

[0085] Thirty vias were then formed on the substrate so that the core and the copper plating were perforated throughout. The vias were positioned so that they would be found beneath the outline of the MEMS device it was intended to support, throughout the area within such outline, as well as outside such outline, on the lands. The vias were positioned on the lands using VIP technology.

[0086] A solder mask was then deposited on the LGA/BGA semiconductor package substrate.

[0087] The MEMS device was then mounted on top of the solder mask layer of the upper core surface and wire connections between the substrate and the MEMS device were carried out.

[0088] The semiconductor package was then sealed with a sealant cap or a moulding compound.

[0089] It was found that such package gave good functioning performance in the long term in terms of offset stability and drift, given by the fewer cap delamination and loss of sealing effect risks during assembly, in particular during molding.

[0090] It is envisaged that semiconductor packages, and therefore the respective positions of the package devices with respect to the IC, can take on any of the configuration known in the field (side by side, stacked, inverse stacking, etc.). In such cases, the above description should be modified according to the requirements.

[0091] In conclusion, embodiments of the present invention provide improved semiconductor package substrates which are capable of better withstanding the mechanical stresses caused by the assembly steps of the production line.

[0092] It has been found, in fact, that by distributing the vias according to the homogeneous pattern according to embodiment of the invention, the package substrate becomes more stable and can undergo the assembly steps without suffering from the common problem of delamination of the cap and loss of the seal effect. The result is a package substrate which is suitable to support stress-sensitive devices such as MEMS and the like during assembly and is thus capable of ensuring good performance of the device in the long term.

[0093] MEMS or other devices contained in semiconductor package substrates according to embodiments of the present invention may be contained in a variety of different types of electronic systems, such as video display systems, televisions, bar code scanners, and so on.

[0094] From the foregoing it will be appreciated that, although specific embodiments of the invention have been described herein for purposes of illustration, various modifications may be made without deviating from the spirit and scope of the invention.

1. A semiconductor package substrate suitable for supporting a damage-sensitive device, comprising:

a) a package substrate core having an upper and a lower surface;

b) at least one pair of metal layers coating said upper and lower surfaces of said package substrate core;

c) one pair of solder mask layers coating the outer metal layers of said one pair of metal layers;

a plurality of vias formed across said package substrate core and said at least one pair of metal layers; and wherein

said plurality of vias is substantially distributed according to a homogeneous pattern in an area that is to be covered by said damage-sensitive device.

2. The semiconductor package substrate of claim **1** wherein said vias are positioned so that they substantially coincide with an outline of said damage-sensitive device that the semiconductor package substrate is intended to support.

3. The semiconductor package substrate of claim **2** wherein the number of vias on each side of said outline is the same and said number is greater than 1.

4. The semiconductor package substrate of claim **1** wherein said vias are positioned so that the majority of the vias are homogeneously positioned within a second area which is bigger than said area, preferably 40% bigger than said area and centered with it.

5. The semiconductor package substrate of claim **4** wherein at least two vias are positioned in a security area surrounding a pad line of said damage-sensitive device (**21**).

6. The semiconductor package substrate of claim **5** wherein said security area covers a distance of ±(L+D/2) from the center of said pad line, where **2**L is a pad opening width and D is a diameter of a via land.

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7. The semiconductor package substrate of claim 1 wherein additional vias are positioned in lands outside said area and said second area.

8. The semiconductor package substrate of claim 1 wherein the substrate further includes dummy vias.

9. The semiconductor package substrate of claim 1 wherein said package substrate core is a BT resin.

10. The semiconductor package substrate of claim 1 wherein said at least one pair of metal layers is copper.

11. The semiconductor package substrate of claim 1 wherein the number of said metal layers is comprised between 2 and 8.

12. The semiconductor package substrate of claim 1 wherein said at least one pair of solder mask layers is epoxy resin.

13. A method for the production of a semiconductor package substrate suitable for supporting a damage-sensitive device, comprising the steps of:

a) providing a package substrate core having an upper and a lower surface;

b) depositing at least one pair of metal layers on said upper and lower surfaces of said package substrate core;

c) forming a plurality of vias through said package substrate core and said at least one pair of metal layers;

d) depositing one pair of solder mask layers on the outer layers of said at least one pair of metal layers; and wherein

said step of forming said plurality of vias distributes said plurality of vias substantially according to a homogeneous pattern in an area that is to be covered by said damage-sensitive device.

14. The method of claim 13 wherein said step of forming said plurality of vias distributes said plurality of vias so that they substantially coincide with an outline of said damage-sensitive device.

15. The method of claim 14 wherein said step of forming said plurality of vias distributes said plurality of vias so that the number of vias on each side of said outline is the same and said number is greater than 1.

16. The method of claim 14 wherein said step of forming said plurality of vias distributes said plurality of vias so that so that the majority of said vias are homogeneously positioned within a second area which is bigger than said area, preferably 40% bigger than said area and centered with it.

17. The method of claim 16 wherein said step of forming said plurality of vias distributes said plurality of vias so that at least two vias are positioned in a security area surrounding a pad line of said damage-sensitive device.

18. The method of claim 17 wherein said step of forming said plurality of vias distributes said plurality of vias so that at least two vias are positioned in a security area which covers a distance of ±(L+D/2) from the center of said pad line, where 2L is a pad opening width and D is a diameter of a via land.

19. The method of any of claim 13 to 18 further comprising a step of forming additional vias positioned in lands outside said area and said second area.

20. The method of claim 13 further comprising a step of forming dummy vias where the number of vias required is smaller than that necessary to provide a best stability of said semiconductor package substrate.

21. The method of claim 19 wherein said step of forming additional vias is realized according to the Vias-In-Pad or VIP technology.

22. The method of claim 13 wherein said step of forming said plurality of vias is realized according to the plated through holes or vias in pad technology.

23. The semiconductor package substrate of claim 1 wherein said damage-sensitive device is a MEMS device.

24. A semiconductor package including a package substrate having an upper surface and a lower surface, the package substrate being adapted to support a device and the package substrate further including a plurality of vias extending through the package substrate from the upper surface to the lower surface, the vias being arranged in a pattern within an area to which the device is to be attached and the pattern of the vias reducing stresses experienced by the device during subsequent manufacturing steps of the semiconductor package.

25. The semiconductor package of claim 24 wherein the pattern corresponds to an even distribution of the vias within the area.

26. The semiconductor package of claim 24 wherein the pattern includes dummy vias.

27. The semiconductor package of claim 24 wherein the area to which the device is to be attached is defined by a periphery of the device, and wherein the pattern of vias are positioned to substantially coincide with the periphery of device.

28. The semiconductor package of claim 27 wherein the device has a plurality of sides such that the area to which the device is to be attached has the plurality of sides, and wherein at least one via is formed on each side of the area.

29. The semiconductor package of claim 28 wherein the vias are positioned homogeneously within a second area which is larger than the area.

30. The semiconductor package of claim 29 wherein the second area is approximately 40% larger than the area.

31. The semiconductor package of claim 24 wherein,

the package substrate including a package substrate core having an upper surface and a lower surface;

at least one pair of metal layers coating the upper and lower surfaces of the package substrate core; and

one pair of solder mask layers coating the outer metal layers of the one pair of metal layers; and

the plurality of vias is formed extending through the package substrate core and each pair of metal layers.

32. The semiconductor package of claim 24 further comprising the device attached to the package substrate.

33. The semiconductor package of claim 32 wherein the device comprises a MEMS device.

34. The semiconductor package of claim 24 wherein the package substrate comprises a land grid array.

35. The semiconductor package of claim 24 wherein the package substrate comprises a ball grid array.

36. An electronic system including electronic circuitry operable to perform a desired function, the electronic circuitry including a semiconductor package including a package substrate having an upper surface and a lower surface, the package substrate being adapted to support a device and the package substrate further including a plurality of vias extending through the package substrate from the upper surface to the lower surface, the vias being arranged in a pattern within an area to which the device is to be attached and the pattern of the vias reducing stresses experienced by the device during subsequent manufacturing steps of the semiconductor package.

37. The electronic system of claim **36** wherein the electronic circuitry comprises one of television, bar code scanning, and video display circuitry.

38. A method of manufacturing a semiconductor package including a package substrate having an upper surface and a lower surface, the method comprising:

attaching a device to the package substrate; and

forming a pattern of vias within an area of the package substrate underlying the device, the vias extending through the package substrate from the upper surface to the lower surface and being arranged in a pattern that reduces stresses experienced by the device during subsequent manufacturing steps of the semiconductor package.

39. The method of claim **38** wherein the subsequent manufacturing steps include encapsulating the semiconductor package in an epoxy resin.

40. The method of claim **38** wherein the pattern corresponds to an even distribution of the vias within the area.

41. The method of claim **40** wherein the device has an area and wherein the area of the package substrate is larger than the area of the device.

42. The method of claim **38** wherein the area is defined by a periphery of the device, and wherein the pattern of vias are positioned to substantially coincide with the periphery of device.

43. The method of claim **42** wherein the device has a plurality of sides such that the area has the plurality of sides, and wherein at least one via is formed on each side of the area.

44. The method of claim **38** wherein the vias are positioned homogeneously within a second area which is larger than the area.

45. The method of claim **38** wherein the package substrate includes a package substrate core having an upper and a lower surface, and wherein the method further comprises:

depositing at least one pair of metal layers on the upper and lower surfaces of the package substrate core;

forming a plurality of vias through the package substrate core and the at least one pair of metal layers; and

depositing one pair of solder mask layers on the outer layers of the at least one pair of metal layers.

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