UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY LTD.,

and

APPLE INC.,

Petitioners

v.

MYW SEMITECH, LLC,

Patent Owner

Case No. IPR2026-00065
U.S. Patent No. 11,107,768

DECLARATION OF STANLEY SHANFIELD, PH.D

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2. Claim 25(b): "wherein said third metal interconnect comprises a second metal layer on said metal pad and a fifth copper layer over said second metal layer, wherein said fifth copper layer has a thickness between 5 and 30 micrometers," *350*

3. Claim 25(c): "wherein said third metal interconnect is connected to said a fourth metal interconnect of said first interconnection scheme." *351*

H. CLAIM 26: "THE CHIP PACKAGE OF CLAIM 16, WHEREIN A HEIGHT IS BETWEEN A BACKSIDE SURFACE OF SAID FIRST SEMICONDUCTOR CHIP AND A TOP SURFACE OF SAID SECOND POLYMER LAYER IS SMALLER THAN A THICKNESS OF SAID FIRST METAL BUMP." 352

I. CLAIM 27: "THE CHIP PACKAGE OF CLAIM 16, WHEREIN SAID SECOND SEMICONDUCTOR CHIP IS COUPLED TO SAID FIRST SEMICONDUCTOR CHIP THROUGH SAID FIRST INTERCONNECTION SCHEME." 353

J. CLAIM 28: "THE CHIP PACKAGE OF CLAIM 16, WHEREIN SAID FIRST METAL PLUG HAS A THICKNESS BETWEEN 100 AND 300 MICROMETERS." 355

XIII. OPINIONS REGARDING GROUND 3B: CLAIMS 18 AND 21 ARE OBVIOUS OVER YU, LIN-191, AND CAMACHO 355

A. CLAIM 18: 355

1. 18(a): "The chip package of claim 16, wherein said second semiconductor chip comprises a first metal pad on a top surface of said second semiconductor chip and a second metal pad on a bottom surface of said second semiconductor chip," *356*

a) Camacho's "Metal Pad" Teachings 357

2. 18(b): "wherein said first metal pad is connected to said second metal pad through a through-silicon-via metal layer." *358*

a) Camacho's Teachings 358

3. Claim 18 MTC 359

B. CLAIM 21 361

1. Claim 21(a): "The chip package of claim 16, further comprising a third semiconductor chip under said second semiconductor chip and" 361

2. Claim 21(b): "multiple fourth metal bumps between said second and third semiconductor chips," 362

3. Claim 21(c): "wherein said second semiconductor chip comprises a first metal pad on a top surface of said second semiconductor chip and a second metal pad on a bottom surface of said second semiconductor chip," 363

4. Claim 21(d): "wherein said first metal pad is connected to said second metal pad through a through-silicon-via metal layer." 363

5. Claim 21 MTC 363

XIV. OPINIONS REGARDING GROUND 3C: CLAIM 20 IS OBVIOUS OVER YU, LIN-191, AND HABA 366

A. CLAIM 20: "THE CHIP PACKAGE OF CLAIM 16, WHEREIN SAID FIRST POLYMER LAYER HAS A COEFFICIENT OF EXPANSION BETWEEN 3 AND 10 PPM/°C." 366

a) Haba's Teachings and Motivation to Combine 366

XV. CONCLUSION 367

CLAIM LISTING

Claim 1:

Claim 1(Pre): A chip package comprising:

Claim 1(a): a first polymer layer having a first surface and a second surface opposite to said first surface,

Claim 1(a)(i): wherein said first surface is substantially parallel to said second surface,

Claim 1(a)(ii): wherein said first polymer layer has a thickness between 100 and 300 micrometers and…

Claim 1(a)(iii): [wherein said first polymer layer] has a coefficient of expansion between 3 and 10 ppm/° C.;

Claim 1(b): a first metal plug vertically in a first through via in said first polymer layer,

Claim 1(b)(i): wherein said first metal plug comprises a first copper layer, wherein the first copper layer contacts with a sidewall of said first through via;

Claim 1(c): a second metal plug vertically in a second through via in said first polymer layer,

Claim 1(c)(i): wherein said second metal plug comprises a second copper layer,

Claim 1(c)(ii): wherein a top surface of said second metal plug and a top surface of said first metal plug are in the same horizontal plane;

Claim 1(d): a first interconnection scheme over said first surface,

Claim 1(d)(i): wherein said first interconnection scheme comprises a first metal interconnect over said first surface, a second metal interconnect over said first surface, a third metal interconnect over said first surface and a second polymer layer over said first, second and third metal interconnects

Claim 1(d)(ii): wherein said first metal interconnect is connected to said first metal plug, wherein said second metal interconnect is connected to said second metal plug,

Claim 1(d)(iii): wherein said first metal interconnect comprises a first metal layer, a third copper layer on said first metal layer, and a fourth copper layer on said third copper layer

Claim 1(e): a first metal bump over said first interconnection scheme and said second metal plug,

Claim 1(e)(i): wherein said first metal bump comprises a tin-containing layer; and

Claim 1(f): a first semiconductor chip under said first interconnection scheme,

Claim 1(f)(i): wherein said first semiconductor chip comprises a fourth metal interconnect on a first metal pad of said first semiconductor chip,

Claim 1(f)(ii): wherein said fourth metal interconnect comprises a second metal layer on said first metal pad and a fifth copper layer over said second metal layer, wherein said fifth copper layer has a thickness between 5 and 30 micrometers,

Claim 1(f)(iii): wherein said fourth metal interconnect is connected to said third metal interconnect.

Claim 2:

The chip package of claim 1, further comprising a passive component over said first interconnection scheme and connected to said first interconnection scheme through a solder layer.

Claim 3:

The chip package of claim 1, wherein said first interconnection scheme comprise a fifth metal interconnect across over a sidewall of the first semiconductor chip.

Claim 4:

Claim 4(a): The chip package of claim 1, further comprising a second semiconductor chip over said first interconnection scheme,

Claim 4(b): wherein said second semiconductor chip comprises a second metal bump between said second semiconductor chip and said first interconnection scheme.

Claim 5:

The chip package of claim 1, wherein said first semiconductor chip comprises a central-processing-unit (CPU) circuit block and a graphics-processing-unit (GPU) circuit block.

Claim 6:

Claim 6(a): The chip package of claim 1, wherein said first semiconductor chip comprises a second metal pad on a top surface of said first semiconductor chip and a third metal pad on a bottom surface of said first semiconductor chip,

Claim 6(b): wherein said second metal pad is connected to said third metal pad through a through-silicon-via metal layer.

Claim 7:

Claim 7(a): The chip package of claim 1, wherein said first interconnection scheme further comprises a fifth metal interconnect over said first metal interconnect and said second polymer layer,

Claim 7(b): wherein said second polymer is between said first and fifth metal interconnects,

Claim 7(c): wherein said fifth metal interconnect comprises a third metal layer, a sixth copper layer on said third metal layer, and a seventh copper layer on said sixth copper layer.

Claim 8:

The chip package of claim 1, further comprising a second interconnection scheme under said first polymer layer and on said second surface.

Claim 9:

The chip package of claim 1, wherein said first metal plugs has a top surface substantially coplanar with said first surface.

Claim 10:

The chip package of claim 1, wherein said first metal pad is an aluminum pad.

Claim 11:

Claim 11(a): The chip package of claim 1, further comprising a second semiconductor chip over said first interconnection scheme and connected to said first interconnection scheme through a second metal bump

Claim 11(b): wherein said second semiconductor chip has a height is between a backside surface of said second semiconductor chip and a top surface of said second polymer layer is smaller than a thickness of said first metal bump.

Claim 12:

Claim 12(a): The chip package of claim 1, further comprising a second semiconductor chip under said first semiconductor chip,

Claim 12(b): wherein said first semiconductor chip comprises a second metal pad connected to a third metal pad of said second semiconductor chip through a solder layer, wherein said solder layer between said first and second semiconductor chips.

Claim 13:

Claim 13(a): The chip package of claim 1, further comprising a second semiconductor chip under said first semiconductor chip,

Claim 13(b): wherein said first semiconductor chip comprises a second metal pad on a top surface of said first semiconductor chip, a third metal pad on a bottom surface of said first semiconductor chip

Claim 13(c): and a through-silicon-via metal layer connects to said second metal pad,

Claim 13(d): wherein said third metal pad is connected to a fourth metal pad of said second semiconductor chip.

Claim 14:

The chip package of claim 1, further comprising a third metal plug vertically in a third through via in said first polymer layer, wherein a pitch between said first and third metal plugs is between 200 and 1000 micrometers.

Claim 15:

The chip package of claim 1, wherein said first metal plug has a thickness between 100 and 300 micrometers.

Claim 16:

Claim 16(Pre): A chip package comprising:

Claim 16(a): a first polymer layer having a first surface and a second surface opposite to said first surface,

Claim 16(a)(i): wherein said first surface is substantially parallel to said second surface,

Claim 16(a)(ii): wherein said first polymer layer has a thickness between 100 and 300 micrometers;

Claim 16(b): a first metal plug vertically in a first through via in said first polymer layer,

Claim 16(b)(i): wherein said first metal plug comprises a first copper layer, wherein the first copper layer contacts with a sidewall of said first through via;

Claim 16(c): a second metal plug vertically in a second through via in said first polymer layer,

Claim 16(c)(i): wherein said second metal plug comprises a second copper layer,

Claim 16(c)(ii): wherein a top surface of said second metal plug and a top surface of said first metal plug are in the same horizontal plane;

Claim 16(d): a first interconnection scheme over said first surface,

Claim 16(d)(i): wherein said first interconnection scheme comprises a first metal interconnect over said first surface, a second metal interconnect over said first surface and a second polymer layer over said first and second metal interconnects,

Claim 16(d)(ii): wherein said first metal interconnect is connected to said first metal plug,

Claim 16(d)(iii): wherein said first metal interconnect comprises a first metal layer, a third copper layer on said first metal layer, and a fourth copper layer on said third copper layer

Claim 16(e): a first metal bump over said first interconnection scheme,

Claim 16(e)(i): wherein said first metal bump is connected to said first interconnection scheme through a first opening in said second polymer layer,

Claim 16(e)(ii): wherein said first metal bump comprises a tin-containing layer;

Claim 16(f): a second metal bump over said first interconnection scheme,

Claim 16(f)(i): wherein said second metal bump is connected to said first interconnection scheme through a second opening in said second polymer layer;

Claim 16(g): a first semiconductor chip over said first interconnection scheme and between said first and second metal bumps;

Claim 16(h): a third metal bump between said first semiconductor chip and said first interconnection scheme,

Claim 16(h)(i): wherein said third metal bump connected to said second metal interconnect through a third opening in said second polymer layer; and

Claim 16(i): a second semiconductor chip under said first interconnection scheme and said first semiconductor chip,

Claim 16(i)(i): wherein said first interconnection scheme is between said first and second semiconductor chips,

Claim 16(i)(ii): wherein said second semiconductor chip comprises a central-processing-unit (CPU) circuit block and a graphics-processing-unit (GPU) circuit block.

Claim 17:

The chip package of claim 16, further comprising a third semiconductor chip over said first interconnection scheme.

Claim 18:

The chip package of claim 16, wherein said second semiconductor chip comprises a first metal pad on a top surface of said second semiconductor chip and a second metal pad on a bottom surface of said second semiconductor chip, wherein said first metal pad is connected to said second metal pad through a through-silicon-via metal layer.

Claim 19:

The chip package of claim 16, further comprising a third metal plug vertically in a third through via in said polymer layer, wherein a pitch between said first and third metal plugs is between 200 and 1000 micrometers.

Claim 20:

The chip package of claim 16, wherein said first polymer layer has a coefficient of expansion between 3 and 10 ppm/°C.

Claim 21:

Claim 21(a): The chip package of claim 16, further comprising a third semiconductor chip under said second semiconductor chip and

Claim 21(b): multiple fourth metal bumps between said second and third semiconductor chips,

Claim 21(c): wherein said second semiconductor chip comprises a first metal pad on a top surface of said second semiconductor chip and a second metal pad on a bottom surface of said second semiconductor chip,

Claim 21(d): wherein said first metal pad is connected to said second metal pad through a through-silicon-via metal layer.

Claim 22:

The chip package of claim 16, further comprising a passive component over said first surface.

Claim 23:

The chip package of claim 16, wherein said first interconnection scheme comprise a third metal interconnect across over a sidewall of the second semiconductor chip.

Claim 24:

The chip package of claim 16, further comprising a third semiconductor chip under said first interconnection scheme, wherein said third semiconductor chip is a memory chip.

Claim 25:

Claim 25(a): The chip package of claim 16, wherein said second semiconductor chip comprises a third metal interconnect on a metal pad of said second semiconductor chip,

Claim 25(b): wherein said third metal interconnect comprises a second metal layer on said metal pad and a fifth copper layer over said second metal layer, wherein said fifth copper layer has a thickness between 5 and 30 micrometers,

Claim 25(c): wherein said third metal interconnect is connected to said a fourth metal interconnect of said first interconnection scheme.

Claim 26:

The chip package of claim 16, wherein a height is between a backside surface of said first semiconductor chip and a top surface of said second polymer layer is smaller than a thickness of said first metal bump.

Claim 27:

The chip package of claim 16, wherein said second semiconductor chip is coupled to said first semiconductor chip through said first interconnection scheme.

Claim 28:

The chip package of claim 16, wherein said first metal plug has a thickness between 100 and 300 micrometers.

I, Dr. Stanley Shanfield, declare the following:

I. INTRODUCTION

1. I have been retained by counsel for Petitioners as a technical expert in the above-captioned case. Specifically, I have been asked to render certain options regarding the IPR petition with respect to U.S. Patent No. 11,107,768 (the "'768 Patent"). I understand that the Challenged Claims are 1-28, and my opinions are limited to those claims. A true and correct copy of my Curriculum Vitae, which provides further details about my background and experience, is appended to this Declaration.

A. *Educational Background and Professional Experience*

2. In 1977, I received a B.S. Degree in Physics *cum laude* from the University of California, Irvine. I received a Ph.D. in Physics from Massachusetts Institute of Technology in 1981.

3. After obtaining my Ph.D. in 1981, I was a Staff Scientist at Spire Corporation in Bedford, Massachusetts. From 1985-1999, I worked at Raytheon Corporation. As staff and later as section manager, among many other projects, I developed reactive ion etching (RIE) processes for patterning dielectrics (silicon dioxide, silicon nitride, silicon oxynitride, etc.), conductive layers (aluminum-copper, copper-silicon, W-silicide, TaN, doped polysilicon, etc.) and organic layers (photoresist, polyimide, etc.). In 1996, I became the Manager of Semiconductor

Operations at Raytheon. As Manager, I built and led a 300-employee, $60 million revenue-generating semiconductor development, commercial system design, and electronic module manufacturing operation. I worked directly with engineers in the selection, installation, and optimization of several chemo-mechanical polishing systems (CMP), including analysis of operational maintenance and performance monitoring. The manufacturing facility eventually used multiple production CMP systems, and I directly participated in establishing the required metrology (optical thickness monitoring) for maintaining polishing uniformity standards.

4. In 1999, I was a co-founder and became Vice President of Operations at AXSUN Technologies in Bedford/Billerica, Massachusetts and later became Director of Manufacturing and Wafer Fab Technology.

5. In 2003, I joined the Draper Laboratory in Cambridge, Massachusetts. Currently, I am the Division Leader of Advanced Hardware Development, with around 80 staff members; a Distinguished Member of Technical Staff; and Technical Director. I led the Advanced Hardware Development division in relaunching a multi-chip integrated circuit module facility. The laboratory has acquired several semiconductor-grade CMP systems for the purpose of fabricating multi-chip modules and for planarization operations in MEMS devices, and I have been involved in their operation and optimization. I invented and led the implementation of an ultra-miniature electronics fabrication technology. I also developed fabrication

technology for semiconductor-based low-phase noise oscillator design. I have received many awards at Draper, including the 2010 Distinguished Performance Award and the 2010 Best Patent Award.

6. During the 1990's I developed early stacked-chip plastic packages while working for Raytheon. Additionally, I have led the implementation and qualification of MCM-D (multi-chip module – deposited) technology for military and space applications during my time at Draper Labs. Also during my time at Draper Labs, I have (1) developed improved fabrication and test methods for advanced multichip modules using ceramic and glass packages, (2) led efforts involving die thinning, copper interconnect plating, and component stacking at multiple interconnect levels, (3) managed thermos-mechanical modeling efforts to assess packaging reliability under demanding conditions, and (4) oversaw a large team of next-gen multichip module process development at Draper (2010-2015). Additionally, I am an inventor on U.S. Patent No. 7,727,806 which is directed to systems and methods for high density multi-component modules.

B. ***Materials Considered***

7. I have relied upon my education, knowledge, and experience with semiconductor chip packaging, as well as the other materials as discussed in this declaration in forming my opinions.

8. In developing my opinions, I have considered the following materials:

Exhibit 1001	U.S. Patent No. 11,107,768
Exhibit 1002	File History of the '768 Patent
Exhibit 1004	U.S. Patent No. 9,167,694 to Sundaram, et al.
Exhibit 1005	U.S. Patent Publication No. 2010/0290191 to Lin, et al.
Exhibit 1006	U.S. Patent Publication No. 2011/0215458 to Camacho, et al.
Exhibit 1007-1008	Intentionally left blank
Exhibit 1009	U.S. Patent No. 8,709,933 to Haba, et al.
Exhibit 1010	U.S. Patent No. 9,123,763 to Yu, et al.
Exhibit 1011	Intentionally left blank
Exhibit 1012	Andrea Chen, et al. *Semiconductor Packaging Materials Interaction and Reliability*, CRC Press, 2012
Exhibit 1013	Philip Garrou, et al., *RDL: an integral part of today's advanced packaging technologies*, Solid State Technology, May 2011
Exhibit 1014	U.S. Patent No. 8,780,576 to Haba, et al.
Exhibit 1015	U.S. Patent No. 7,902,648 to Lee
Exhibit 1016	U.S. Patent No. 7,964,961 to Lee, et al.
Exhibit 1017	U.S. Patent No. 7,241,641 to Savastiouk, et al.
Exhibit 1018	U.S. Patent Publication No. 2005/0110168 to Chuang
Exhibit 1019	U.S. Patent Publication No. 2011/0026232 to Lin, et al.
Exhibit 1020	U.S. Patent No. 5,086,558 to Grube, et al.
Exhibit 1021	U.S. Patent Publication No. 2011/0193219 to Lai, et al.
Exhibit 1022	U.S. Patent No. 6,818,545 to Lee, et al.
Exhibit 1023	U.S. Patent No. 6,974,659 to Su, et al.
Exhibit 1024	U.S. Patent Publication No. 2006/0175686 to Murata, et al.
Exhibit 1025	U.S. Patent Publication No. 2012/0098124 to Wu, et al.
Exhibit 1026	U.S. Patent No. 8,193,604 to Lin et al.
Exhibit 1027	U.S. Patent Publication No. 2004/0203224 to Halahan, et al.
Exhibit 1028	Philip Garrou, *Introduction to 3D Integration,* Handbook of 3D integration: Volumes 1 and 2, Technology and Application of 3D Integrated Circuits, 2012
Exhibit 1029	U.S. Patent Publication No. 2003/0068877 to Kinsman
Exhibit 1030	U.S. Patent Publication No. 2010/0246152 to Lin, et al.
Exhibit 1031	Yi Yang, et al, *CPU-Assisted GPGPU on Fused CPU-GPU Architectures,* IEEE Xplore
Exhibit 1032-1034	Intentionally left blank
Exhibit 1035	E.D. Blackshear, et al., *The evolution of build-up package technology and its design challenges*, International Business Machines Corporation, 2005
Exhibit 1036	Intentionally left blank
Exhibit 1037	U.S. Patent No. 7,374,969 to Cho, et al.
Exhibit 1038	Intentionally left blank
Exhibit 1039	Intentionally left blank
Exhibit 1040	U.S. Patent No. 6,619,538 to Test, et al.
Exhibit 1041	Intentionally left blank
Exhibit 1042	U.S. Patent No. 6,831,003 to Huang, et al.

Exhibit 1043	U.S. Patent Publication No. 2009/0226611 to Suzuki, et al.
Exhibit 1044	U.S. Patent No. 6,077,726 to Mistry, et al.
Exhibit 1045	U.S. Patent Publication No. 2010/0244245 to Pendse, et al.
Exhibit 1046	U.S. Patent Publication No. 2012/0206160 to Wu, et al.
Exhibit 1047	U.S. Patent Publication No. 2009/0174052 to Sogawa, et al.
Exhibit 1048	U.S. Patent Publication No. 2013/0100624 to Carpenter, et al.
Exhibit 1049	U.S. Patent No. 7,047,515 to Vitek, et al.
Exhibit 1050	U.S. Patent No. 8,116,097 to Love, et al.
Exhibit 1051	U.S. Patent Publication No. 2009/0237900 to Origuchi, et al.
Exhibit 1052	U.S. Patent Publication No. 2005/0002167 to Hsuan, et al.
Exhibit 1053	U.S. Patent Publication No. 2008/0067695 to Chow, et al.
Exhibit 1054	U.S. Patent No. 6,489,240 to Iacoponi, et al.
Exhibit 1055	U.S. Patent No. 6,578,178 to Mau
Exhibit 1056	U.S. Patent Publication No. 2012/0001190 to Okabe, et al.
Exhibit 1057	U.S. Patent No. 7,307,348 to Wood, et al.
Exhibit 1058	U.S. Patent No. 8,138,014 to Chi, et al.
Exhibit 1059	U.S. Patent No. 6,506,672 to Dagenais, et al.
Exhibit 1060	Intentionally left blank
Exhibit 1061	U.S. Patent Publication No. 2009/0261473 to Lee, et al.
Exhibit 1062	Intentionally left blank
Exhibit 1063	U.S. Patent No. 6,812,143 to Lane, et al.
Exhibit 1064	Intentionally left blank
Exhibit 1065	U.S. Patent Publication No. 2011/0147950 to Tai, et al.
Exhibit 1066	U.S. Patent Publication No. 2009/0070727 to Solomon
Exhibit 1067	U.S. Patent Publication No. 2012/0098114 to Ishibashi
Exhibit 1068	U.S. Patent Publication No. 2011/0074028 to Pendse
Exhibit 1069-1070	Intentionally left blank
Exhibit 1071	U.S. Patent No. 7,649,368 to Eldridge, et al.
Exhibit 1072-1077	Intentionally left blank
Exhibit 1078	U.S. Patent Publication No. 2012/0139068 to Stacey
Exhibit 1079	Intentionally left blank
Exhibit 1080	U.S. Patent Publication No. 2012/0319251 to Yu, et al.
Exhibit 1081	U.S. Patent No. 7,838,759 to Alley, et al.
Exhibit 1082	U.S. Patent No. 6,982,874 to Smalc, et al.
Exhibit 1083	U.S. Patent Publication No. 2009/0166069 to Kinoshita
Exhibit 1084	U.S. Patent No. 7,759,782 to Haba, et al.
Exhibit 1085	U.S. Patent No. 6,946,727 to Ho, et al.
Exhibit 1086	U.S. Patent Publication No. 2003/0013298 to May
Exhibit 1087	U.S. Patent No. 5,834,945 to Akram, et al.
Exhibit 1088	U.S. Patent No. 6,611,046 to Yang
Exhibit 1089	U.S. Patent No. 7,638,254 to Hattori, et al.
Exhibit 1090	U.S. Patent Publication No. 2005/0156280 to Patel, et al.
Exhibit 1091	U.S. Patent Publication No. 2011/0215470 to Chen, et al.

Exhibit 1092	Moody Dreiza, et al., *High Density PoP (Package-on-Package) and Package Stacking Development*, Electronic Components and Technology Conference, 2007
Exhibit 1093	U.S. Patent No. 6,107,180 to Munroe, et al.
Exhibit 1094	U.S. Patent Publication No. 2011/0210283 to Ramirez, et al.
Exhibit 1095	U.S. Patent No. 6,452,502 to Dishongh, et al.
Exhibit 1096	U.S. Patent No. 6,344,401 to Lam.
Exhibit 1097	Richard K. Ulrich, et al., *Advanced Electronic Packaging,* IEEE Press Series on Microelectrical Systems, 2006
Exhibit 1098	Mulugeta Abtew, et al., *Lead-free Solders in Microelectronics*, Materials Science and Engineering, 2000
Exhibit 1099	Karl J. Puttlitz, et al., *Handbook of Lead-Free Solder Technology for Microelectronic Assemblies*, 2005
Exhibit 1100	U.S. Patent Publication No. 2013/0309832 to Cheng, et al.
Exhibit 1101	U.S. Patent Publication No. 2013/0151869 to Steinman, et al.
Exhibit 1102	Linely Gwennap, *Sandy Bridge Spans Generations: Intel Focuses on Graphics, Multimedia in New Processor Design*, Microprocessor, 2010
Exhibit 1103	Intentionally left blank
Exhibit 1104	U.S. Patent No. 6,710,447 to Nogami.
Exhibit 1105	U.S. Patent Publication No. 2011/0059305 to Kaneya, et al.
Exhibit 1106	U.S. Patent No. 7,057,896 to Matsuo, et al.
Exhibit 1107	U.S. Patent No. 7,777,333 to Bachman, et al.
Exhibit 1108	U.S. Patent No. 7,095,105 to Cherukuri, et al.
Exhibit 1109	U.S. Patent No. 7,423,347 to Chen, et al.
Exhibit 1110	U.S. Patent Publication No. 2008/0128891 to Ziglioli, et al.
Exhibit 1111	U.S. Patent Publication No. 2008/0042280 to Lin, et al.
Exhibit 1112	U.S. Patent No. 7,923,836 to Farooq, et al.
Exhibit 1113	U.S. Patent Publication No. 2005/0121711 to Pogge, et al.
Exhibit 1114	U.S. Patent Publication No. 2012/0313240 to Cheng, et al.
Exhibit 1115	U.S. Patent No. 7,262,444 to Fillion, et al.
Exhibit 1116	U.S. Patent Publication No. 2013/0037944 to Lee, et al.
Exhibit 1117-1125	Intentionally left blank
Exhibit 1126	U.S. Patent No. 8,592,988 to Lee, et al.
Exhibit 1127	Intentionally left blank
Exhibit 1128	U.S. Patent No. 6,528,179 to Jimarez, et al.
Exhibit 1129	U.S. Patent No. 6,468,413 to Fanti, et al.
Exhibit 1130	U.S. Patent No. 8,132,775 to Goldmann.
Exhibit 1131	U.S. Patent Publication No. 2011/0186977 to Chi, et al.
Exhibit 1132	U.S. Patent No. 7,169,627 to Duh, et al.
Exhibit 1133	U.S. Patent No. 6,614,243 to Klehn, et al.
Exhibit 1134	U.S. Patent Publication No. 2009/0162622 to Van Veen, et al.
Exhibit 1135	U.S. Patent No. 6,570,259 to Alcoe, et al.
Exhibit 1136	U.S. Patent No. 7,741,567 to Beddingfield, et al.
Exhibit 1137	U.S. Patent No. 6,407,341 to Anstrom, et al.

9. I have considered these materials from the viewpoint of a POSITA as of the priority date of the ’768 Patent. For the purposes of this declaration, I have been asked to assume that the priority date of the ’768 Patent is September 26, 2012. I note that my opinions provided in this Declaration are made from the perspective of a POSITA as of this priority date of the ’768 Patent unless expressly stated otherwise. To the extent that I use any verb tense in this Declaration that is present tense (e.g., “a POSITA would understand” instead of “a POSITA would have understood”), such verb tense should be understood to be my opinion as of the ’768 Patent’s priority date (again, unless expressly stated otherwise). I merely use the present verb tense for ease of reading.

II. OVERVIEW AND LEGAL STANDARDS

10. In formulating my opinions, I have been instructed to apply certain legal standards. I am not a lawyer. I do not offer any testimony regarding what the law is. Instead, the following sections summarize the law as I have been instructed to apply it in formulating and rendering my opinions found later in this declaration. I understand that, in an *inter partes* review (“IPR”) proceeding, patent claims may be deemed unpatentable if it is shown that they are anticipated or rendered obvious in view of the prior art. I understand that prior art in an IPR review is limited to patents or printed publications that predate the priority date of the patent at issue. I understand that questions of claim clarity (definiteness) and enablement cannot be

considered as a ground for considering the patentability of a claim in these proceedings.

A. *Person of Ordinary Skill in the Art*

11. I understand that the ’768 Patent, the record of the proceedings at the Patent Office (which I understand is called the “File History” or “Prosecution History”), and the teachings of the prior art are evaluated from the perspective of a person of ordinary skill in the art (“POSITA”). I understand that the factors considered in determining the ordinary level of skill in the art may include: (i) the levels of education of the inventor; (ii) the types of problems encountered in the art; (iii) prior art solutions to those problems; (iv) the rapidity with which innovations are made; (v) the sophistication of the technology; and (vi) the educational level of persons working in the field.

12. I understand that a person of ordinary skill in the art is not a specific real individual, but rather a hypothetical individual having the qualities reflected by the factors above. The hypothetical person is presumed to have the same level of skill as the typical practitioner of the art and is presumed to have knowledge of all prior art in the relevant field. I understand that the inventor’s actual knowledge or lack of knowledge of prior art reference is irrelevant to the obviousness determination.

B. *Obviousness*

13. I understand that a claim may be invalid under 35 U.S.C. § 103(a) if the subject matter described by the claim as a whole would have been "obvious" to a POSITA in view of a single or combination of prior art references at the time the claimed invention was made. I further understand that a POSITA is assumed to know and to have all relevant prior art in the field of endeavor covered by the patent-in-suit and all analogous prior art. I understand that obviousness in an IPR review proceeding is evaluated using a preponderance of the evidence standard, which means that the claims must be more likely obvious than nonobvious.

14. I also understand that an obviousness determination includes the consideration of various factors including: (1) the scope and content of the prior art, (2) the differences between the prior art and the claim at issue, and (3) the level of ordinary skill in the pertinent art. I understand that secondary considerations of non-obviousness such as commercial success, long-felt but unresolved needs, failure of others, and so forth may be assessed as well. I have been informed that an obviousness analysis must consider the full scope of the claims to avoid impermissibly using hindsight to invalidate a patent.

15. In considering whether certain prior art renders a particular patent claim obvious, I have been informed that I can consider the scope and content of the prior art, including the fact that a POSITA would regularly look to the disclosures in patents, trade publications, journal articles, conference papers, industry standards,

product literature and documentation, texts describing competitive technologies, requests for comment published by standard setting organizations, and materials from industry conferences, as examples.

16. I have been informed that for a prior art reference to be proper for use in an obviousness analysis, the reference must be "analogous art" to the claimed invention. A reference is analogous art if: (1) the reference is from the same field of endeavor as the claimed invention (even if it addresses a different problem); or (2) the reference is reasonably pertinent to the problem faced by the inventor (even if it is not in the same field of endeavor as the claimed invention). For a reference to be "reasonably pertinent" to the problem, it must logically have commended itself to an inventor's attention in considering the problem. In determining whether a reference is reasonably pertinent, one should consider the problem faced by the inventor, as reflected either explicitly or implicitly, in the specification. I believe that the documents I considered in forming my opinions in this IPR are well within the range of documents a POSITA would have consulted to address the type of problems described in the Challenged Claims.

17. I have been informed that to establish that a claimed invention was obvious based on a combination of prior art elements, an articulation of the reason(s) why a claimed invention would have been obvious must be provided. Specifically, I have been informed that the prior art, either as a single reference or a combination

of multiple items of prior art, renders a patent claim obvious when there was an apparent reason for a POSITA, at the time of the invention, to combine or modify the prior art. Rationales for combining or modifying the prior art include, but are not limited to, any of the following: (A) combining prior art methods according to known methods to yield predictable results; (B) substituting one known element for another to obtain predictable results; (C) using a known technique to improve a similar device in the same way; (D) applying a known technique to a known device ready for improvement to yield predictable results; (E) trying a finite number of identified, predictable potential solutions, with a reasonable expectation of success; (F) identifying that known work in one field of endeavor may prompt variations of it for use in either the same field or a different one based on design incentives or other market forces if the variations are predictable to one of ordinary skill in the art; or (G) identifying an explicit teaching, suggestion, or motivation in the prior art that would have led one of ordinary skill to modify the prior art reference or to combine the prior art references to arrive at the claimed invention.

18. I have also been informed that where there is a motivation to combine, claims may be rejected as obvious provided a POSITA would have had a reasonable expectation of success regarding the proposed combination. I have also been informed that common sense may be considered. Common sense teaches that familiar items may have obvious uses beyond their primary purposes. I have been

informed that if the combination was obvious to try (regardless of whether it was actually tried) or leads to anticipated success, then it is likely the result of ordinary skill and common sense rather than non-obvious innovation.

19. I have been informed that the existence of an explicit teaching, suggestion, or motivation to combine known elements of the prior art is a sufficient, but not a necessary, condition to a finding of obviousness. In determining whether the subject matter of a patent claim is obvious, neither the particular motivation nor the avowed purpose described in the patent-in-suit controls. I have been further informed that the obviousness analysis may consider the effects of demands known to the technological community or present in the marketplace and the background knowledge possessed by a POSITA. These issues may be considered to determine whether there was an apparent reason to combine the known elements in the fashion claimed by the patent.

20. I have been informed that it is improper to combine references where the references teach away from their combination. A reference may be said to teach away when a POSITA, upon reading the reference, would be discouraged from following the path set out in the reference, or would be led in a direction divergent from the path that was taken by the patent applicant. I have also been informed that a reference does not teach away if it merely expresses a general preference for an

alternative invention but does not criticize, discredit, or otherwise discourage investigation into the invention claimed.

21. I am informed that even if a case of obviousness is established, the final determination of obviousness must also consider "secondary considerations" if presented. Secondary considerations include: (a) commercial success of a product due to the merits of the claimed invention; (b) a long-felt, but unsatisfied need for the invention; (c) failure of others to find the solution provided by the claimed invention; (d) deliberate copying of the invention by others; (e) unexpected results achieved by the invention; (f) praise of the invention by others skilled in the art; (g) lack of independent simultaneous invention within a comparatively short space of time; and (h) teaching away from the invention in the prior art.

22. I have been further informed that secondary considerations evidence is only relevant if the offering party establishes a connection, or nexus, between the evidence and the claimed invention. The nexus cannot be based on prior art features. The establishment of a nexus is a question of fact. While I understand that Patent Owner here has not offered any secondary considerations at this time, I will supplement my opinions should Patent Owner raise secondary considerations during the course of this proceeding.

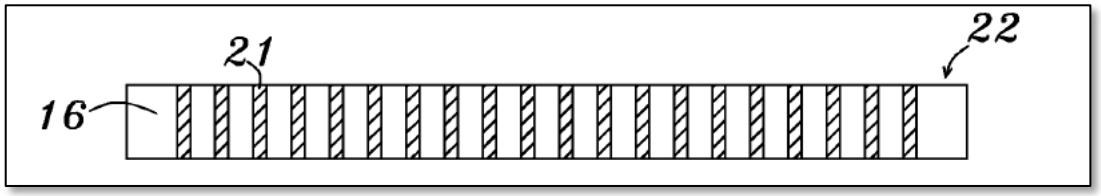
C. *Claim Construction*

23. I understand that the claim terms in an IPR proceeding are construed according to their plain and ordinary meaning as understood in light of the claim language, the patent's description, and the prosecution history viewed from the perspective of a POSITA. I further understand that where a patent defines claim language, the definition of the patent controls, even if there are other definitions that might be understood by those working in the art.

III. OVERVIEW OF THE '768 PATENT

A. *Summary of the '768 Patent*

24. The '768 Patent describes a chip package having a "second substrate 22" with an "amorphous solid glass layer/body 16 and multiple metal plugs 21" wherein the "amorphous solid glass layer/body 16 having a top surface and an opposing bottom surface and the metal plugs 21 extending through the amorphous solid glass layer/body 16 beginning at the top surface and ending at the bottom surface." *EX1001* at 11:3-8.



EX1001 at FIG. 8a.

25. The '768 Patent further describes the metal plugs are "formed from metal traces 6." *EX1001* at 7:64-65. To obtain the plugs, the metal traces 6 are (1)

stretched (5:65–6:5, FIG. 6a); (2) placed in a mold (6:31-33, FIG. 6d); (3) a polymer is filled into the mold (6:50-54, 7:42-45); and (4) cut into "multiple first substrates 20," which comprises "multiple seconds substrates 22" that each have "multiple metal plugs 21." *EX1001* at 7:51-67, FIGS. 6j-6k.

26. As shown below in FIG. 9b, a "first dielectric layer 24" that may be a "polymer (such as polyimide…)" is formed "formed on the top surface of the first substrate 20." *EX1001* at 11:39-48. "Multiple openings 24a are formed in the first dielectric layer 24 to expose the metal plugs 21" by "etching." *EX1001* at 11:53-56.

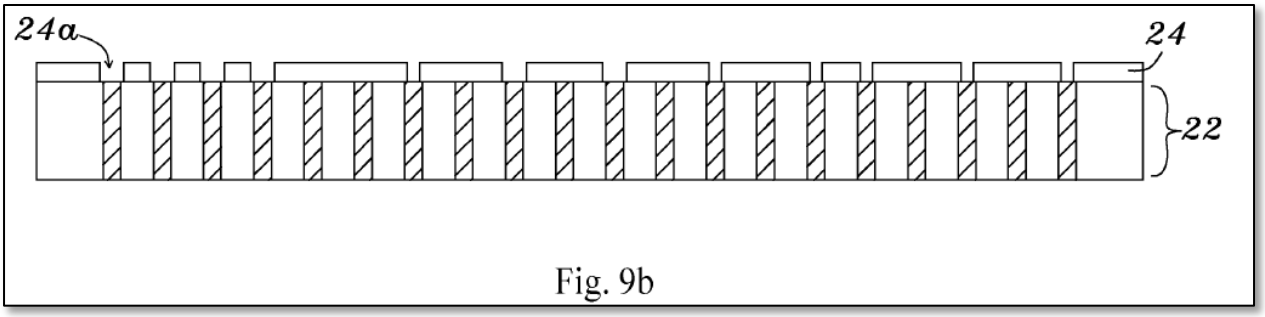
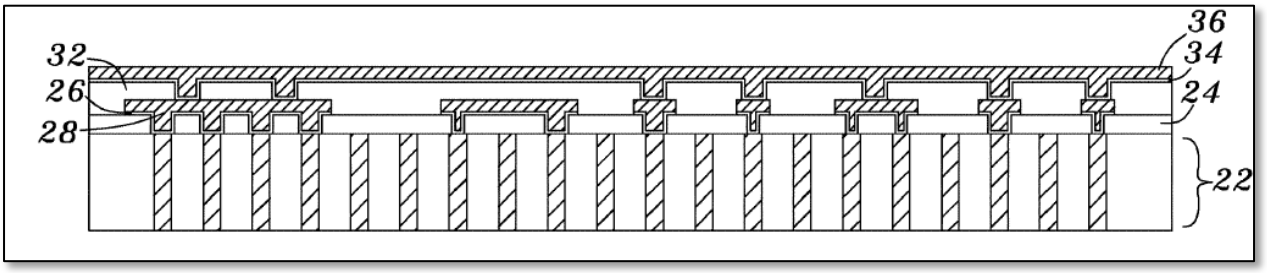


Fig. 9b

EX1001 at FIG. 9b.

27. A "first metal layer 26 is formed on the first dielectric layer 24, on the metal plugs 21 and in the openings 24" that "may include an adhesion/barrier layer, such as a layer of titanium…" *EX1001* at 11:60-63. Next, a "second metal layer 28 is formed on the first metal layer 26" that "maybe comprises copper." *EX1001* at 12:5-7. A "second dielectric layer 32 is formed on the first dielectric layer 24 and on the second metal layer 28" that may be "a polymer[.]" *EX1001* at 12:30-38. Multiple "openings 32a are formed in the second dielectric layer 32 to expose the second

metal layer 28" then a "third metal layer 34 is formed on the second dielectric layer 32, on the second metal layer 28 and in the openings 32a." *EX1001* at 12:45-54. A "fourth metal layer 36 is formed on the third metal layer 34." *EX1001* at 12:64-65.



EX1001 at FIG. 9k.

28. A "third dielectric layer 40 is formed on the second dielectric layer 32 and on the fourth metal layer 36" that may be a "polymer[.]" *EX1001* at 13:22-29. Multiple "openings 40a are formed in the third dielectric layer 40 to expose the fourth metal layer 36" then a "protecting layer 42 is formed in the openings 40a, on the third dielectric layer 40 and on the fourth metal layer 36[.]" *EX1001* at 13:37-46. Multiple "chips 46 and chips 56" are "set up over the third dielectric layer 40 through a flip-chip package process" where the "chip 46 comprises multiple metal pads 48 and multiple metal bumps 50 formed on the metal pads 48." *EX1001* at 13:58-60, 14:11-13.

29. The '768 Patent further describes a "metal bump 72" that may have "an adhesion/barrier metal layer 61…a metal seed layer 63 formed on the adhesion/barrier metal layer 61, an electroplated metal layer 65 formed on the metal

seed layer 63 and a solder layer 67 formed on the electroplated metal layer 65." *EX1001* at 14:55-60. The "electroplated metal layer 65 comprises a copper layer" and the "solder layer 67 can be formed" of "gold-tin alloy, tin-silver alloy, tin-silver copper alloy, indium, tin-bismuth allow or other lead-free alloy." *EX1001* at 14:64–15:2.

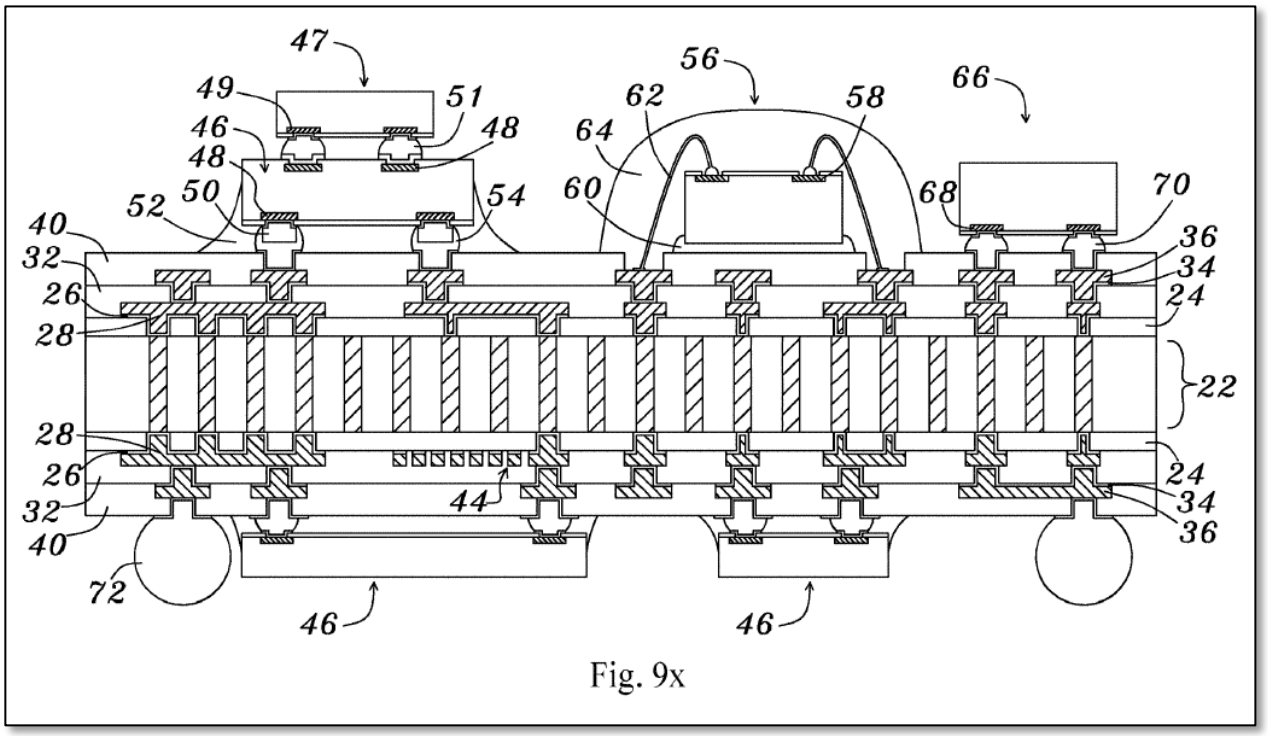


Fig. 9x

EX1001 at FIG. 9x.

30. As I will explain in detail below, there is nothing novel about the disclosure or claims of the '768 Patent. The claims as a whole recite a litany of claim elements that were both well-known on their own and well-known in combination with other recited claim elements. For example, the claims recite well-known features such as metal interconnects, copper plugs, semiconductor chips, and metal

bumps, all of which were commonplace in chip packages before well before the '768 Patent.

B. *Field of Endeavor*

31. I have been informed that the field of endeavor of the claimed invention can be determined by reference to explanations of the invention's subject matter in the patent application, including the embodiments, function, and structure of the claimed invention.

32. The '768 Patent, titled "Chip Package" generally relates to semiconductor packaging. *EX1001* at Title. The '768 Patent describes that "microelectronic devices have a tendency to be minimized and thinned with its functional development and a semiconductor package mounted on a mother board is also following the tendency in order to realize a mounting of high integration" *EX1001* at 1:24-28. The described embodiments "illustrates a cross-section view of multiple chips and a 3D-IC package…" *EX1001* at 3:32-35. Additionally, the '768 Patent describes that "chips 46 are set up…through a flip-chip package process." *EX1001* at 14:10-11.

33. Further still, the '768 Patent expressly places its work in the context of flip-chip technology, explaining that "flip-chip technology fabricates bumps… on Al pads of chip and interconnects the bumps directly to the package media" and that this arrangement provides "the highest density of interconnection to the device and

a very low inductance interconnection to the package[.]" *EX1001* at 1:48-50. For these reasons, a POSITA would understand that the field of endeavor of the '768 Patent includes semiconductor packaging. *EX1001* at 1:24-67.

C. *Problem Solved by the Inventors of the '768 Patent*

34. I have been informed that a prior art reference is "reasonably pertinent" if a POSITA would have consulted it and applied its teachings when faced with the problem(s) that the inventor was trying to solve. As such, I have been asked to analyze the '768 Patent and determine the problem(s) that the inventors were trying to solve.

35. The '768 Patent recognizes the problem of "TCE (Temperature Coefficient of Expansion) matching to avoid solder bump fatigue [is] still [a] challenge[]" *EX1001* at 1:58-64. Thus, a POSITA would have understood the '768 Patent is directed, in part, to solving the problem of minimizing temperature coefficient of expansion mismatching in semiconductor packages.

36. The '768 Patent also explains that "pre-testability, post-bonding visual inspection… [is] still [a] challenge[]" *EX1001* at 1:58-64. Thus, a POSITA would have understood the '768 Patent to be directed, in part, to solving the problem of creating chip packages with pre-testability capability.

37. Further, the '768 Patent states that "with the further miniaturization of the IC" there is "an increasingly negative impact on the circuit performance."

EX1001 at 1:31-35. Thus, a POSITA would have understood the '768 Patent to be directed, in part, to solving the problem the impact of miniaturization on circuit performance.

38. Additionally, the '768 Patent describes that "parasitic capacitance and resistance of the metal interconnections increase, which degrades the chip performance significantly." *EX1001* at 1:32-37. Thus, a POSITA would have understood the '768 Patent to be directed, in part, to solving the problem the impact of parasitic capacitance of interconnections in a chip package.

IV. LEVEL OF A PERSON OF ORDINARY SKILL

39. Based on my review and analysis of the '768 Patent, the cited prior art, and the ordinary skill factors described in this section, a POSITA in the field of the '768 Patent at the time of the earliest possible priority date (September 26, 2012) would have had a at least a bachelor's degree in electrical engineering, materials science, or physics (or an equivalent degree), and at least two years of experience in semiconductor design or semiconductor manufacturing. A master's degree or Ph.D. in a relevant field may substitute for some work experience or vice versa. Additional education or experience might substitute for the above requirements. When I refer to the understanding of a POSITA, I am referring to the understanding of such a person as of September 26, 2012.

V. OVERVIEW OF THE TECHNOLOGY

40. I was asked to briefly summarize the background of the prior art from the standpoint of a person having ordinary skill in the art prior to September 26, 2012. As explained below, the chip packaging technology described by the '768 Patent was based on well-known packaging techniques and chip package structures. Thus, the techniques discussed in the '768 Patent were well-known and conventional prior to the invention of the '768 Patent.

A. *History of Chip Packaging*

41. Chip packaging technology was known and widely used well before the priority date of the '768 Patent. In fact, semiconductor chip packaging had been in development at least 40 years in advance of the 2012 priority date of the '768 Patent with the 1960s seeing "rapid proliferation of new packages for ICs" as a response to the development of silicon planar technology and higher pin count versions of early metal can packages. *EX1097* at p. 8. Additionally, "[p]ackaging costs also received considerable attention during the 1960s while the industry was deciding which package or packages would become standard[.]" along with "early attempts to develop a low-cost, hermetic package[.]" *EX1097* at p. 11, *see also EX1012* at p. 4. Subsequently, plastic packaging, more specifically, the plastic version of the dual in-line packaging (DIP) family was "introduced in the early 1970s[.]" *EX1012* at p. 4.

42. Eventually, "the early 1990s saw the emergence of both pin grid array (PGA) and ball grid array (BGA) packages" responsive to the ultimate goal for high-performance electronic systems to "pack devices as close together as possible in order to minimize circuit path length." *EX1097* at p. 12. "MCM technology, still a viable technology today, played a major role in the evolution of multichip packaging in the 1990s, which includes three-dimensional (3D) stacking of ICs within a single package[.]" *EX1097* at p. 15.

43. Traditional wire bonding techniques were eventually replaced with flip-chip package technology, "[n]amely, the chip is not wire bonded for interconnect but instead flipped face-to-face with the substrate surface—hence the name *flip chip*—and the interconnection between the die and substrate is made through an array of bumps that are placed on the bonding pads of the die surface." *EX1012* at p. 18.

44. "The concept of flip-chip (FC) can be traced back to what IBM called 'controlled collapse chip connection' (C-4) in the late 1960s. It has always been clear that FC is a superior interconnect based on size, I/O density, electrical and thermal performance. However, during the 1960s-1980s, the technology was mainly confined to high end main frame computer companies because the CTE mismatch between Si and PWB laminate required that FC use expensive ceramic packaging." *EX1013* at p. 1.

45. "For FC to find widespread acceptance by those interested in miniaturized portable products such as lap tops, cell phones, pagers, camcorders etc., reliable lower cost FC processes were needed. In the early 1990s, IBM Japan reported that FC chips could be reliably attached directly to PWB laminate if the chips were underfilled. Unitive and Flip Chip Technologies (FTC) subsequently developed lower cost UBMs [(under bump metallization)], lower cost solder deposition technologies (FCT – stencil printing; Unitive – plating) and redistribution (RDL). The FCT and Unitive technologies were licensed by all the key assembly houses… as they initiated production in the early 2000s. This brought flip-chip technology to the masses." *EX1013* at p. 1.

46. Flip chip packages were recognized as providing a number of benefits and solutions, namely, "for low to high pin count, high electrical performance demands from high-end memory, ASICs, and microprocessor applications where high frequency and high speed are required." *EX1012* at p. 18.

47. In particular, it was known that "[f]lip-chip interconnections allow better electrical performance through lower inductances due to the shorter electrical path between the chip and the substrate. The array of bumps under the chip also allows the die to shrink in size, which can reduce wafer cost. The flip-chip structure also allows you to make power and ground connections to internal points on a die,

resulting in better chip performance. To increase thermal performance, optional heat spreaders can be attached on the backside of the flipped die." *EX1012* at p. 18.

B. *Interposers and Dielectric Materials*

48. "Interconnection components, such as interposers are used in electronic assemblies to facilitate connection between components with different connection configurations or to provide needed spacing between components in a microelectronic assembly. Interposers can include a dielectric element [electrically insulating] in the form of a sheet or layer of dielectric material having numerous conductive traces extending on or within the sheet or layer. The traces can be provided in one level or in multiple levels throughout a single dielectric layer, separated by portions of dielectric material within the layer." *EX1014* at 1:5-14. Within chip packages, such as a BGA package, an interposer was known to be used for "matching the chip I/O pitch with the pitch on the PWB." *EX1013* at p. 1.

49. "Conventionally, semiconductor dice have been packaged in plastic or, less commonly, in ceramic packages." *EX1015* at 1:50-51. Therefore, materials such as plastic (i.e., polymer) and ceramic were known and commonly used within the field of chip packaging. In particular, polymer materials, such as, epoxy and polyimide, as well as ceramic materials, such as, silica (silicon dioxide), were commonly used as dielectric/insulation layers within interposer structures for chip packaging. *See, e.g., EX1016* at 23:10-13 (providing providing epoxy or polyimide

as options for "insulating layers 320 and 330"); *EX1016* at 24:1-10 (specifying that the substrate 300 (BGA) may be a "glass fiber reinforced epoxy" or alternatively, a "ceramic substrate").

50. "Packages may support, protect, and dissipate heat from semiconductor dice. Packages may also provide external connective elements for providing power and signal distribution to and from semiconductor dice, as well as for facilitating electrical testing, such as burn-in testing and circuit evaluation, of semiconductor dice prior to or after assembly thereof with higher level components, such as carrier substrates or circuit boards." *EX1015* at 1:51-58. Thus, it would have been understood that a polymer substrate layer would have a suitable thickness to support and protect the coupled semiconductor devices, as well as to support mechanical processes such as drilling to form vias or "receptacles." Specifically, Lee teaches "[s]ubstrates 12 that are formed from resins, or polymers, may have receptacles 11 formed therein by mechanical processes, such as drilling (including laser drilling), punching, milling, or die cutting." *EX1015* at 8:38-41.

51. Savastiouk teaches a silicon substrate of an interposer with a thickness that "can be 100 μm or less." *EX1017* at 4:32-34. Savastiouk also suggests a larger thickness by specifying "silicon substrate 140 can be thicker than described above[.]" *EX1017* at 4:47-50. Therefore, in light of the teachings of Savastiouk interposer substrates were known to include thicknesses of at least 100 μm.

52. Further, it was known to provide interposers with materials other than silicon. Specifically, polymer-based interposers such as epoxy substrates with thicknesses within the range of 100 to 300 μm were known. Specifically, Lee-961 teaches "[t]he substrate 300 may be a ball grid array (BGA) substrate with a thickness [] of between 200 and 2,000 μm. Alternatively, **the substrate 300 may be a glass fiber reinforced epoxy based substrate with a thickness [] of between 200 and 2,000 μm**. Alternatively, the substrate 300 may be a silicon substrate with a thickness [] of between 200 and 2,000 μm. Alternatively, the substrate 300 may be a ceramic substrate with a thickness t15 of between 200 and 2,000 μm. Alternatively, the substrate 300 may be an organic substrate with a thickness t15 of between 200 and 2,000 μm." *EX1016* at 24:1-10 (emphasis added.) Similarly, Haba'576 teaches "**First support portion 12 can, in some embodiments, have a thickness between 50 μm and up to 300 μm**, although a greater thickness is possible. First support portion 12 can be of a dielectric material, **such as a polymeric resin material, for example polyimide, glass, or fiber-reinforced epoxy**." *EX1014* at 7:24-29 (emphasis added).

53. Additionally, Haba-576 teaches that "first support portion 12 further includes an inside surface 16 that is generally parallel to outside surface 14 and spaced apart therefrom to define a thickness of first support portion 12," where "in an embodiment, first support portion 12 has a thickness of at least 5 μm" and "can,

in some embodiments, have a thickness between 50 μm and up to 300 μm … [and] can be of a dielectric material such as a polymeric resin material, for example polyimide, glass, or fiber-reinforced epoxy" *EX1014* at 7:20-29. Haba-576 further teaches that "[f]irst in-process unit 10A' includes first support portion 12 having first conductive vias 122 formed therein and first dielectric layer 52 formed over inside surface 16 of first support portion 12." *EX1014* at 15:9-12. Thus, it was known that polymer layers, such as the first support portion 12 of Haba-576 could be fabricated at least up to 300 μm, while still supporting structures such as conductive vias 122.

54. Dielectric materials such as polymers were also used to form chip packages with dies/chip embedded in the dielectric layer. For example, Chi-977 teaches a chip package having a "semiconductor die 138" and an "encapsulant or molding compound 148 [that] is deposited over die 138." *EX1131*at [0046]. The encapsulant 148 "can be a polymer composite material, such as epoxy resin with filler, epoxy acrylate with filler, or polymer with proper filler." *EX1131*at [0046]. As shown below, a plurality of "conductive pillars 156" are formed in encapsulant 148 having "a height ranging from 20-200 micrometers (μm)." *EX1131* at [0048]. As shown, the encapsulant/molding compound 148 has a height equal to the conductive pillars, demonstrating that dielectric/polymer layers were known to be formed at such a height. *EX1131* at FIG. 4. Further, dielectric/polymer layers having

Chi-977's thickness were known to "environmentally protect[] the semiconductor device from external elements and contaminants." *EX1131* at [0046].

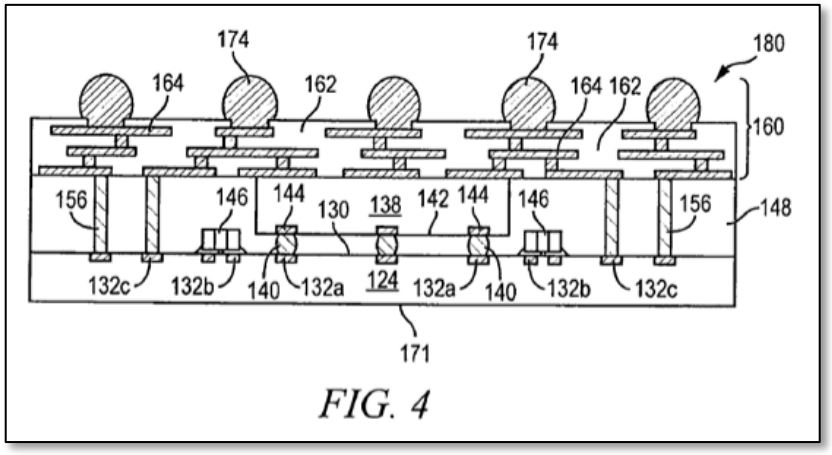


FIG. 4

EX1131 at FIG. 4.

C. *Coefficient of Thermal Expansion*

55. The problem of mismatch of the coefficient of thermal expansion between packaging materials was well known. In particular, it was well known that "The thermal expansion mismatch between the chip and underfill causes stress concentrations in certain locations, like at a die corner. As the crack propagates during continued stressing, the crack opens up the chip–underfill interface or another weakened section, causing either interconnect fatigue or an electrical failure in the chip's dielectric." *EX1012* at p. 45. As a result of this understanding, temperature cycling tests were typically employed in evaluating package reliability. "The purpose of temperature cycling is to check on package integrity in spite of the coefficient of thermal expansion mismatches between the various materials and their

respective interfaces within the plastic package[.]" and that "[a]ll the components—the semiconductor chip, the metal lead frame or organic substrate, the polymer-based molding compound or die attach adhesive—within a package will likely have very different expansion and contraction rates while being heated or otherwise thermally stressed[.]" *EX1012* at p. 48-52. "Temperature cycling and thermal shock are the cause of numerous failure modes in semiconductor packages. Some of these modes include broken bond wire or lifted bonds from pads, solder joint/bump/ball fatigue (an example of which is shown in Figure 5.5), cracked molding compound, and the aforementioned interface delamination. *EX1012* at p. 54.

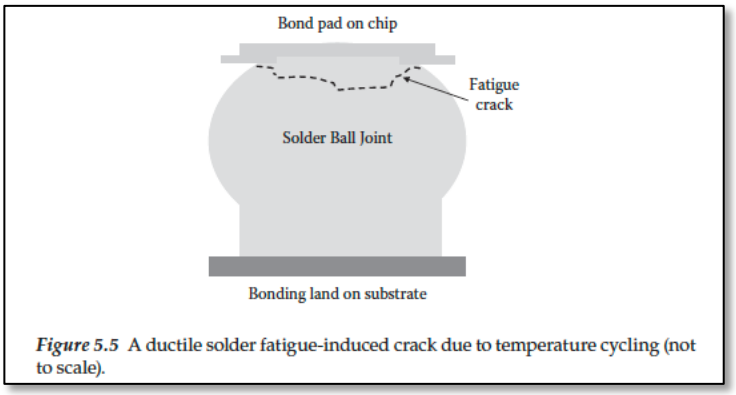


Figure 5.5 A ductile solder fatigue-induced crack due to temperature cycling (not to scale).

EX1012 at FIG. 5.5.

56. It was known that while "epoxy alone has a very high coefficient of thermal expansion, around 80×10^{-6}/ºC, compared to the silicon chip or copper lead frame or organic substrate[.]" (*EX1012* at p. 68) there were known techniques to reduce the coefficient of thermal expansion to more closely match that of silicon. Notably, "[f]illing the epoxy with silica filler brings down the thermal expansion

coefficient into the teens, which would match the lead frame or substrate but would still be high compared to silicon. Using biphenyl or similar epoxy types allows more filler to be added and brings the coefficient down to the high single digits but still not as low as silicon, which is about 3 × 10–6/ºC." *EX1012* at p. 68.

57. Chuang teaches "a low-CTE packaging material for assembling a semiconductor die into a package[.]" *EX1018* at [0004]. Specifically, Chuang suggests that "[a] low-CTE die attach material 318 preferably comprises an epoxy with a negative-CTE filler, such as zirconium tungstate (ZrWOs), halfnium tungstate (HfWOs), or a solid solution of zirconium and halfnium tungstate (Zos HfsWOs). Filler materials have a lower CTE than the packaging material in which they are mixed. This is generally done to more closely approximate the CTE of a silicon die, which may be about 3 ppm/C." *EX1018* at [0019]. Thus, it was well understood that low-CTE polymer-based materials, such as a filled epoxy, could be used as a packaging material to more closely match the coefficient of thermal expansion of silicon.

D. *Through Vias and Metal Plugs*

58. It was widely known that through vias could be disposed through an interposer substrate to provide a conductive path between the top and bottom of the interposer substrate. For example, Savastiouk teaches that "silicon substrate 140 includes metalized through-silicon vias 330 that pass between the top and bottom

surfaces of substrate 140. Conductive paths are provided from contact pads 136C at the top of the interposer to contact pads 340 at the bottom of the interposer through the vias 330." *EX1017* at 4:51-56.

59. Vias were also known to be used in non-silicon interposers. For example, Haba-576 teaches a first support portion 12, which "can be a dielectric material. Such as a polymeric resin material, for example polyimide, glass, or fiber-reinforced epoxy[.]" (*EX1014* at 7:26-29) and further that "[t]he interposer can also include conductive elements such as conductive vias extending through the layer of dielectric material to interconnect traces in different levels." *EX1014* at 1:14-17.

60. Through vias were metalized with materials such as copper to provide electrically conductive paths through an interposer. For example, Haba-576 teaches that "first conductive vias 22 are of a conductive material such as metal including copper, gold, nickel, aluminum, etc." *EX1014* at 7:44-47. Additionally, Savastiouk teaches that "[c]onductive paths are provided from contact pads 136C at the top of the interposer to contact pads 340 at the bottom of the interposer through the vias 330." *EX1017* at 4:54-56; *see also I.D*, 5:54-61, 7:58-59.

61. It was commonly understood that metal plugs could be positioned in vias. Specifically, Lin-232 teaches "The layers 52, 54 and 56 in the through vias 170 v compose multiple metal plugs (or metal vias) 5 p in the through vias 170v, including metal plugs (or metal vias) 5a, 5b, 5c, 5d, 5e and 5f in the through vias

170a, 170b, 170c, 170d, 170e and 170f as shown in FIG. 23, respectively." *EX1019* at [0141].

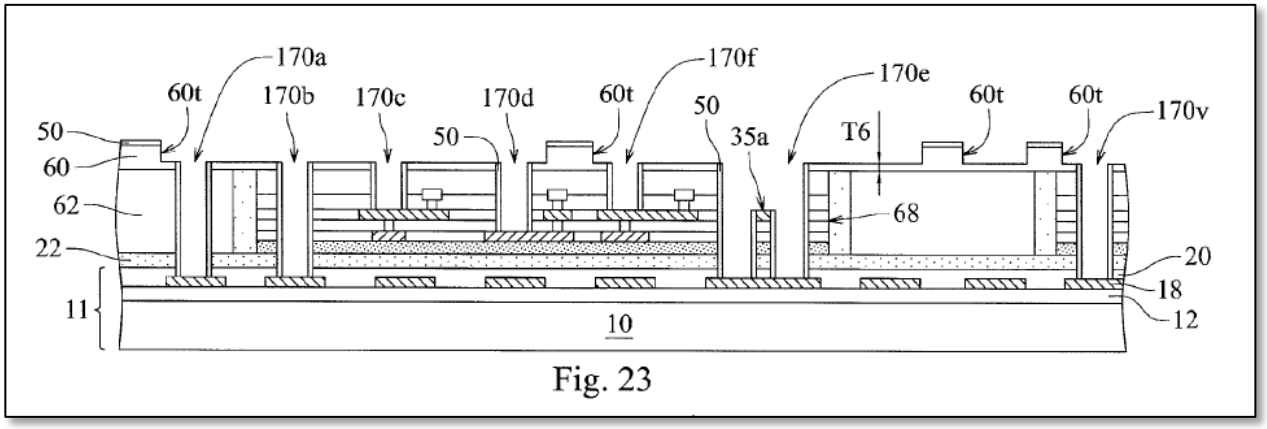


Fig. 23

EX1019 at FIG. 23.

62. Additionally, it was well known that the vias could be positioned into a pattern to match a contact pattern of a respective chip. For example, Grube teaches placing chips upon an interposer sheet with "each chip being positioned on a conforming via pattern[.]" *EX1020* at Abstract. The via patterns are taught as "conforming to the contact patterns of the chips." *EX1020* at 2:42-47.

63. Similarly, via patterns could be arranged in other specific geometries, such as along the perimeter of the substrate. For example, Figure 3.5 of Chen, shown below, illustrates a ball grid array with respective solder balls coupled to vias arranged along the perimeter of the package with an open central region most clearly illustrated in the bottom view.

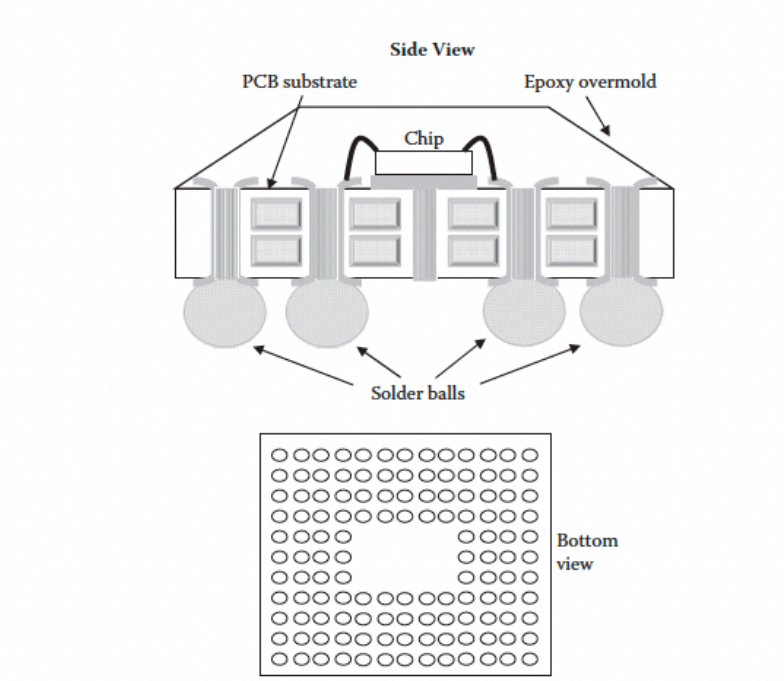


Figure 3.5 Example of a ball grid array package (not to scale).

EX1012 at Figure 3.5, p. 29.

E. *Solder Bumps*

64. Within chip packaging solder bumps were widely used as an interconnection means between packaging components prior to September 26, 2012. Specifically, Chen teaches "[w]afer bumping is necessary to create an electrical and physical connection between a chip and a substrate in lieu of wire bonding. This method is used in flip-chip packaging and in wafer-level chip scale packaging." *EX1012* at p. 121. Additionally, Chen illustrates an exemplary flip-chip interconnect including a solder bump.

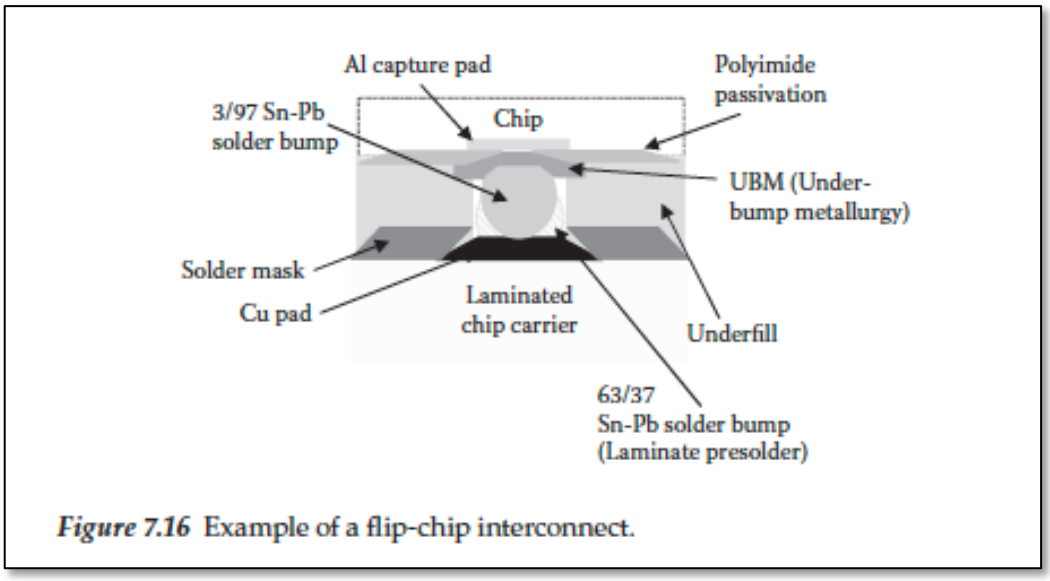


Figure 7.16 Example of a flip-chip interconnect.

EX1012 at FIG. 7.16, p. 122.

65. As shown in the above image, solder bumps were formed on the metal pads of a chip (an "Al capture pad" in the above image). Indeed, in flip-chip packaging "solder bumps are firstly formed on the metal pad of a chip" then the chip "is put on a substrate" and the solder bumps "are aligned with pads of the substrate, and the chip and substrate are processed by means of heat treatment of reflow." *EX1132* at 1:40-45. "After the solder [is] melted, it forms a ball by means of surface tension, such that the connection between the chip and the substrate is complete." *EX1132* at 1:44-47.

66. It was well known that solder contained "pure tin, a tin-silver alloy, a tin-lead alloy or a tin silver-copper alloy[.] *EX1016* at 46:5-7. Additionally, referring to the European Union's RoHS (Restriction of Hazardous Substances) directive made effective in 2006, "with RoHS and other 'green' initiatives, there is the move

toward Pb-free solders and alternate bump metallurgies." *EX1012* at p. 123. Thus, motivation was present at least as early as 2006 to replace traditional lead-based solders with lead-free solder compositions, such as those taught by Lai, which contained tin (Sn). Specifically, Lai teaches a lead-free solder system with a lead-free solder layer 22 that "is SnAg with Ag content being controlled lower than 1.6 weight percent (wt%)." *EX1021* at [0022].

67. Additionally, it was known that solder bump structures could include multiple layers. For example, Lee-545 teaches a solder bump structure having layers including: barrier layers that "are typically used to prevent diffusion of an interconnect metal into surrounding layers of dielectric and silicon[.]" *EX1022* at 8:42-44; a pillar metal layer, notably, "a layer 38 of pillar metal has been deposited (electroplated) over the surface of the layer 36 of barrier material[.]" *EX1022* at 9:61-63; and an under-bump-metallurgy layer with "Layer 40 of UBM, typically of nickel and of a thickness between about 1 and 10 μm, is electroplated over the layer 38 of pillar metal." *EX1022* at 10:19-21.

68. Multiple layers of distinct compositions were known to provide benefits within solder bump structures, such as "the improvement of adhesion of the various overlying layers or the prevention of diffusion of materials between adjacent layers." *EX1022* at 3:49-56.

69. "The conductive bumps formed or placed on the bond pads fulfill several important electrical and mechanical functions. For one thing, it would be physically necessary to create a mechanical and electrical interconnect between the thin, recessed aluminum IC pads to a substrate land. Another issue is that connecting solder directly to aluminum is very tricky at best, but a thin metal layer would probably end up "leached" or dissolved by solder. A sandwich of various metallic layers, usually called the under-bump metallization or UBM, could prevent any material diffusion that would adversely affect the integrity of the connection. The bumps also insured a controlled gap between chip and substrate. If the chip and substrate were touching or nearly so, any CTE mismatch could result in high stress concentrations. By adding a gap, the bumps provide some stress relief." *EX1012* at p. 122.

70. A common type of solder bump was known as 'Controlled Collapse Chip Connection" or "C4" bumps. The "basic idea of C4 is to connect chips (semiconductor devices), chip packages, or such other units by means of solder bumps between two surfaces of the units." *EX1129* at 1:9-17. The "tiny bumps of electrically conductive solder bridge the gaps between respective pairs of metal pads on the units being connected. Each pad has a corresponding pad on the other unit's surface; the pad arrangements are mirror images. As the units are pressed together and heated the solder bumps on the pads of the first unit are contacted with

corresponding conductive pads (having no bumps) on the second unit and reflowed, partially collapsing the solder bumps and making connections between respective pads" *EX1129* at 1:17-26. Conventionally, C4 bumps are "made from lead tin solder" but "lead-free requirements" required manufactures to "implement new ways to produce chip to substrates joints. For example, solder interconnects consisting of tin/copper, tin/silver and SAC alloys have been used as a replacement for leaded solder interconnects." *EX1130* at 1:15-31.

F. *Methods of Forming Solder Bumps*

71. As I will detail herein, solder bumps/balls were typically formed by depositing layer(s) of solder material then performing a reflow step to form a spherical bump/ball geometry. For example, as shown below in FIG. 1C, a "column of solder material 18A may either be deposited in layers, for example, a layer of Pb followed by a layer of Sn, the solder material layers later being formed into a homogenous solder during a first reflow process[.]" *EX1023* at 2:45-39. "If the column of solder material is inhomogenous…a first reflow process is typically performed to harden the printed solder paste and form a homogenous column (plug) of solder material confined by the photoresist layer 16[.]" *EX1023* at 2:42-48. After the photoresist layer 16 is removed, the "solder column 18 is then heated to reflow to form a solder bump 18B…as shown in FIG. 1E." *EX1023* at 2:55-57.

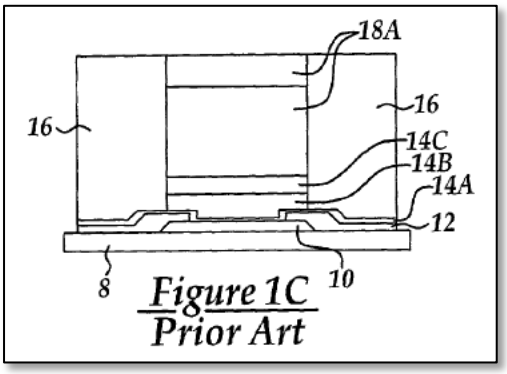


Figure 1C
Prior Art

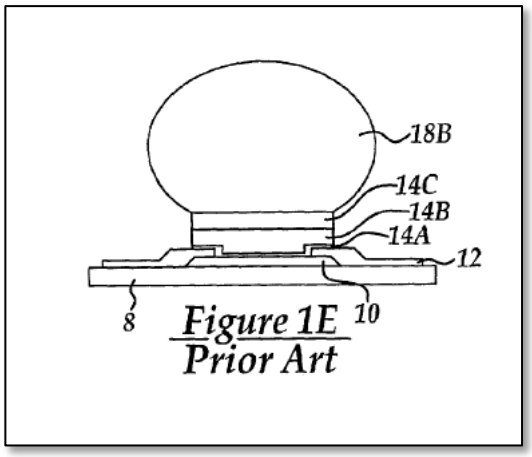
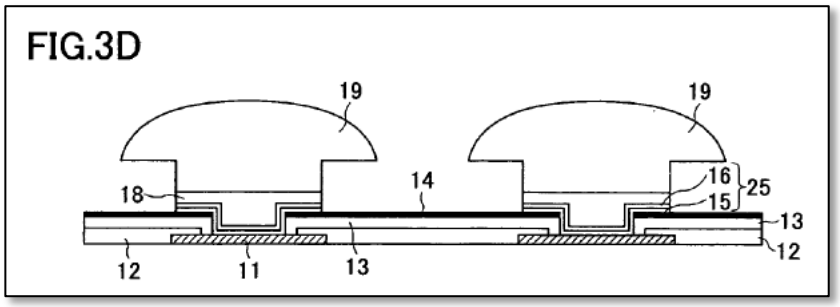


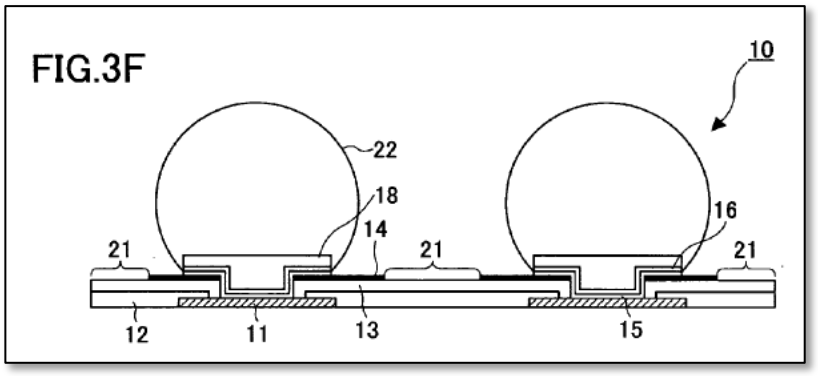
Figure 1E
Prior Art

EX1023 at FIGS. 1C, 1E.

72. As another example, a solder bump may be formed by "plating" a "solder layer 19" that may be "an appropriate material, such as Sn/Cu, Sn/Ag, Sn/Ag/Cu, or Pb/Sn" in and on a resist 17. *EX1024* at [0046]; FIG. 3C. As shown below, in FIG. 3D, the "resist 17 may be removed" then "as illustrated in FIG. 3F, a "reflow treatment is performed to form a bump 22[.]" *EX1024* at [0049].



EX1024 at FIG. 3D.



EX1024 at FIG. 3F.

73. Wu-124 also demonstrates how solder balls/bumps are formed. Specifically, "as shown in FIG. 2C, a metallization layer 22 and a **solder material layer 24** are successfully formed in the opening 21" of a masker layer 20. "The solder material 24 is "electroplated within the opening 21 of the mask layer 20," and as a result "the solder material layer retains a pillar shape within the opening 21." *EX1025* at [0018]-[0019] (emphasis added).

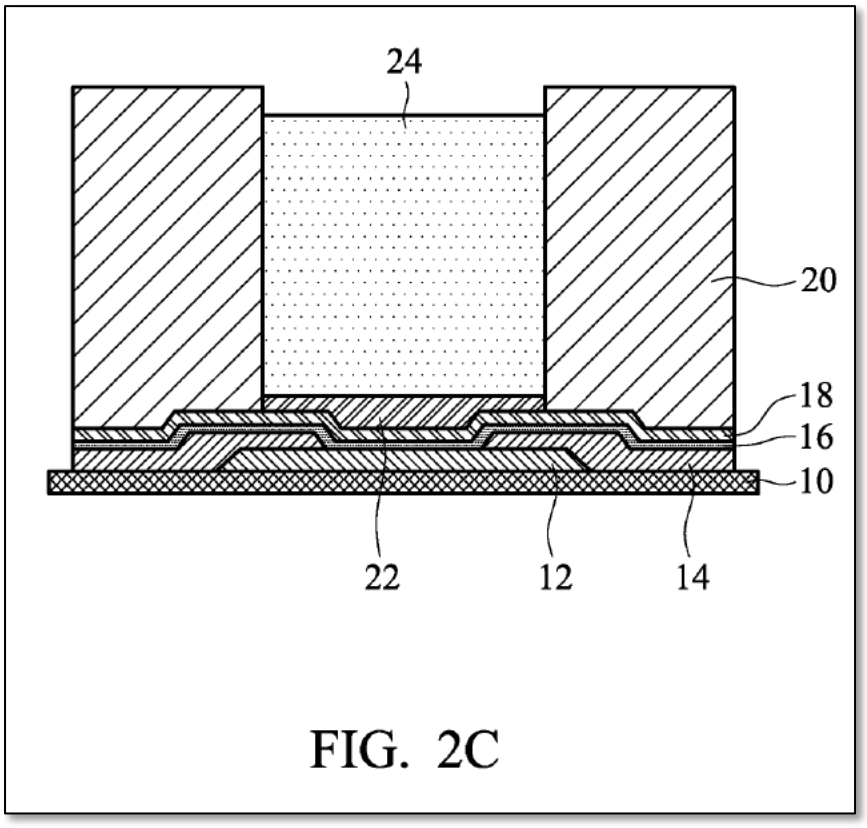


FIG. 2C

EX1025 at FIG. 2C.

74. The "mask layer 20 is then removed" and, as shown in FIG. 2F, a "thermal reflowing process is performed on the solder material layer 24, forming a hemi-sphere-shaped solder bump 24a." *EX1025* at [0021].

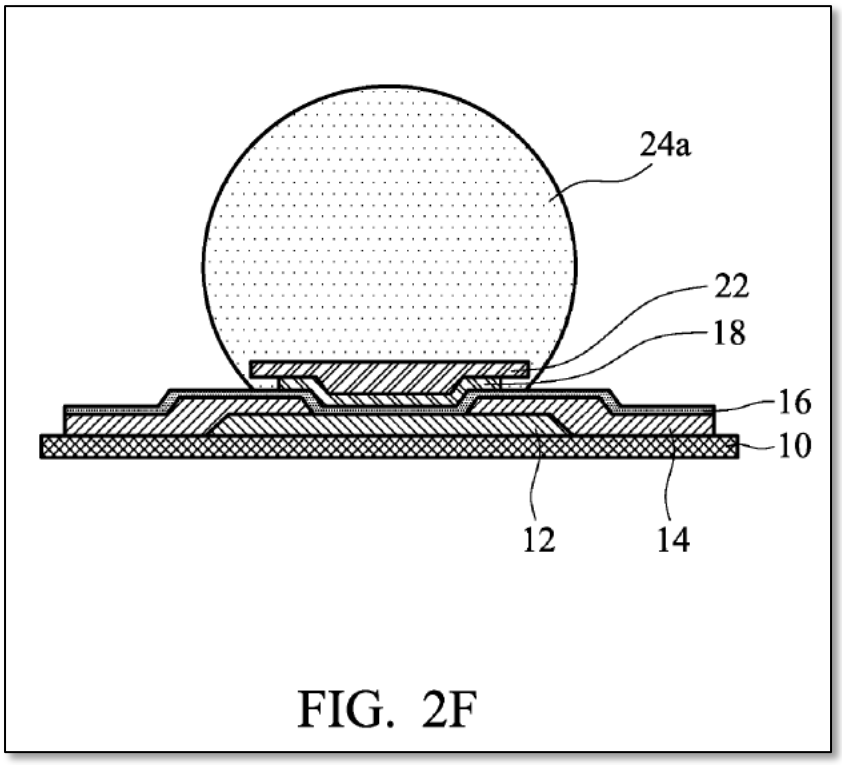


FIG. 2F

EX1025 at FIG. 2F.

75. To control the size of the solder ball, it was known that "the actual amount of solder [] deposited will be a function of the desired end bump size. In other words, in order to form a large solder bump, a greater amount of solder [] material would be applied to the device than would be applied to form a small bump." *EX1093* at 4:7-11.

76. Each of the above examples illustrate the process of forming solder bump/ball and particularly demonstrate that to form a solder bump/ball, a layer or layers of solder material (i.e., solder layers) are deposited, that are then subjected to a reflow treatment, thereby forming the bump/ball geometry. *See also EX1005* at [0324] ("…the **solder layer** is reflowed to form multiple solid solder bumps or balls

29a[.]") (emphasis added). The formation of solder bumps/balls via solder layers becomes relevant to the mapping of claims 2 and 12, reciting a "solder layer."

G. *Interconnection Schemes and Redistribution Layers*

77. Interconnection schemes, such as those utilizing redistribution layers were well known and widely used prior to the '768 Patent. For example, Lin-604 teaches "[a]n RDL interconnection is formed over a surface of core 744. RDL interconnection may include passive circuitry as well, such as capacitor, resistor and inductor. As an example, insulation layer 747 is deposited over core 744 and patterned to expose metal layer 748. Metal layer 749 is deposited over insulation layer 747 and provides for re-routing electrical connections over a surface of core 744 within semiconductor package 700." *EX1026* at 17:24-31.

78. The metal layers of an interconnection could be formed of copper and a dielectric layer could be formed of a polymer, such as polyimide, among other suitable materials. Specifically, Savastiouk teaches "[m]etal layers 136 (FIG. 7) and dielectric layers 144 are deposited on the interposer wafer and patterned to provide interconnects and, possibly, other elements as described above. In some embodiments, metal 136 is copper and dielectric 144 is polyimide, but other materials can also be used. Some or all of dielectric layers 144 can be silicon dioxide, photosensitive benzocyclobutene (BCB), polybenzoxazole (PBO), or other materials." *EX1017* at 6:18-26.

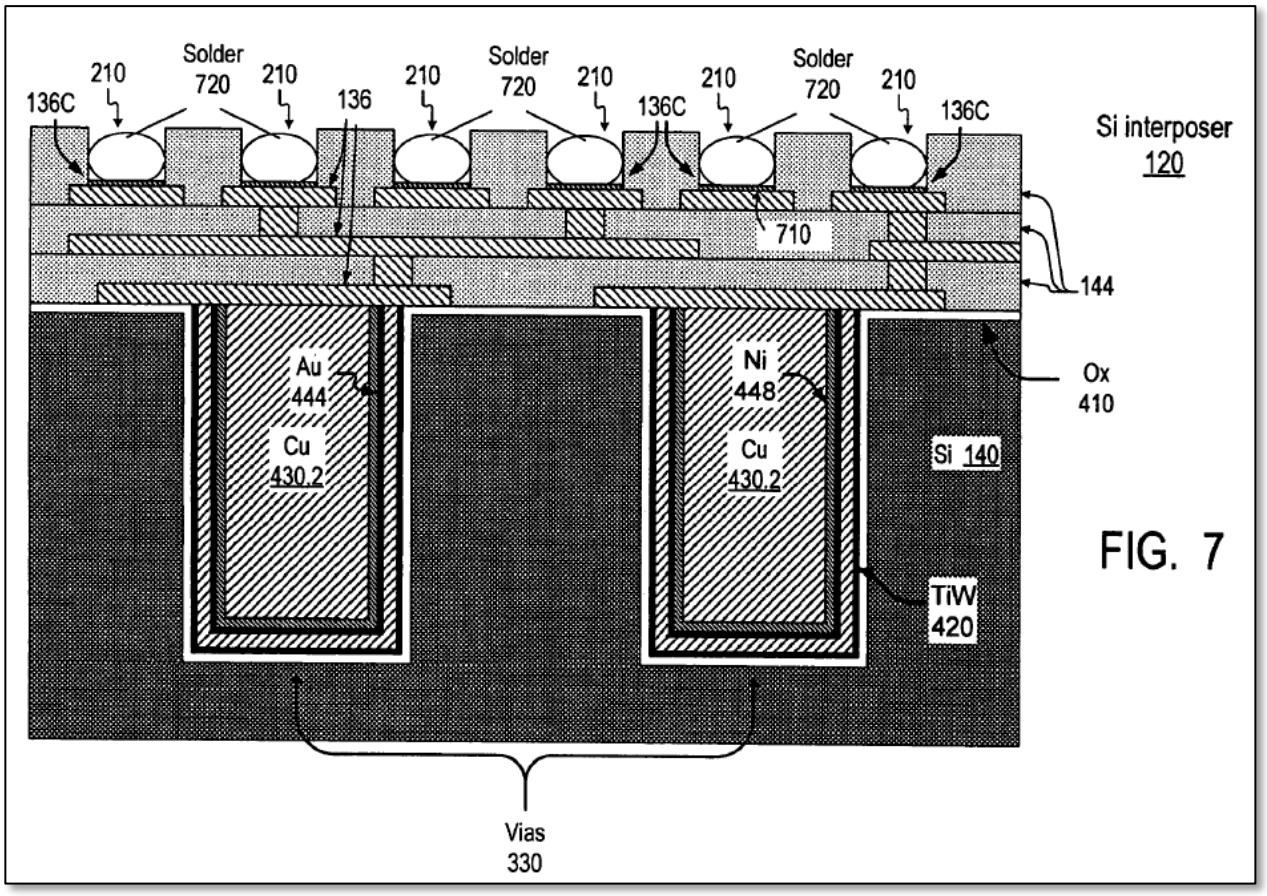
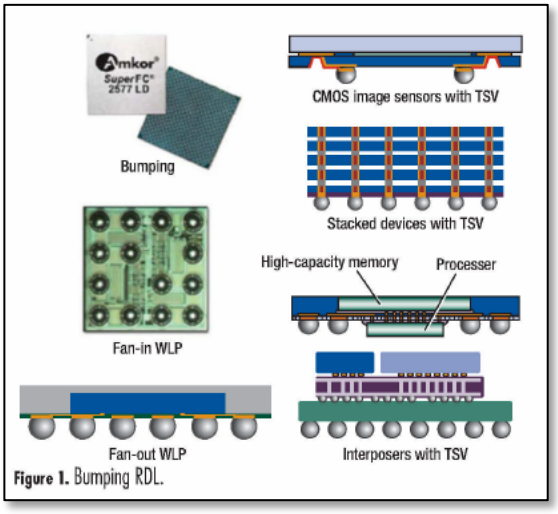


FIG. 7

EX1017 at FIG. 7.

79. Further still, prior to the '768 Patent, it was well known that conductive metals, such as copper, were suitable as metallization for providing electrical conductivity to make electrical connections within a redistribution layer. For example, Garrou teaches "[t]he lack of area array designed chips was a major impediment to the early use of FC. RDL addressed this issue (**Fig. 1**) – – defined by the addition of metal and dielectric layers onto the surface of the wafer to re-route the I/O layout into a new, looser pitch footprint. Such redistribution requires thin film polymers (BCB, PI or newer polymers such as Asahi Glass ALX) and

metallization (Al or Cu) to reroute the peripheral pads to an area array configuration." *EX1013* at p. 1.



EX1013 at FIG. 1.

80. At the time of the '768 Patent, a number of manufacturing methods were known and widely used for providing interconnect structures. For example, Halahan teaches "electroplating and electroless plating of conductive materials into openings[.]" where the plated materials are "used to form through hole interconnects in integrated circuits." *EX1027* at [0001]. Specifically, Halahan teaches "Dielectric 120 is deposited in the openings by chemical vapor deposition (CVD) or thermal oxidation. Metal 130 is sputtered on dielectric 120. Metal 140 is electrodeposited (electroplated) to fill up the openings." *EX1027* at [0002]. Halahan further teaches that "[m]etal 140 increases the mechanical strength of the structure and improves heat dissipation." *EX1027* at [0003]. Notably, Halahan lists advantages of

electroplating as "high throughput and low tool cost" with electroless plating having "similar advantages." *EX1027* at [0005].

H. *Semiconductor Chips*

81. Semiconductor chips were widely used well in advance of the '768 Patent. Specifically, semiconductor chips, such as integrated circuits, were known to be coupled using chip packaging techniques such as flip-chip packaging as noted above. For example, Savastiouk teaches attachment of integrated circuits to other substrates in which "Integrated circuit dies ('chips') can be attached to a lead frame and then packaged in a ceramic or plastic carrier. The leads of the lead frame can then be soldered to a printed circuit board (PCB). Alternatively, the chip can be soldered directly to the PCB ('flip chip' packaging). The flip chip packaging reduces the package size and shortens the electrical connections between the die and the PCB." *EX1017* at 1:26-32.

82. It was also known that packaging techniques could be used to couple multiple chips into a single package. For example, Savastiouk teaches coupling IC dies 124.1, 124.2, and 124.3 onto a single interposer 120. Specifically, Savastiouk teaches "FIGS. 13–14 illustrate a possible manufacturing sequence with multiple die levels 124.1, 124.2, 124.3 attached to the packaging substrate." *EX1017* at 10:22-24. The attachment of dies 124.1, 124.2, and 124.3 is further illustrated in FIG. 13 of

Savastiouk shown below with multiple die levels stacked vertically over the interposer 120.

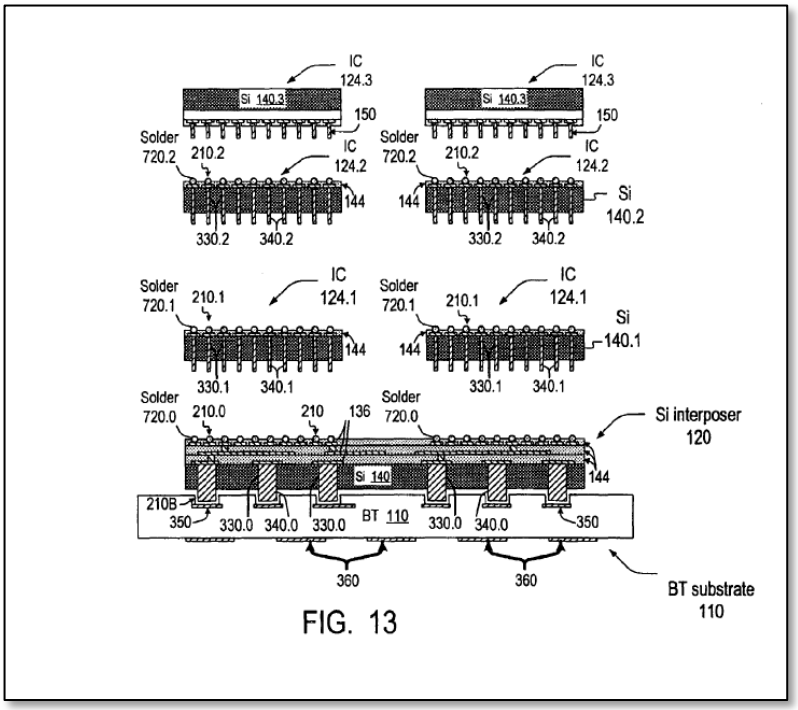


FIG. 13

EX1017 at FIG. 13.

83. Further, Garrou teaches that "[i]ntegrating chips vertically in a single package multiplies the amount of silicon that can be crammed in a given package footprint, conserving hand held device real estate. At the same time, it enables shorter chip to chip routing, which speeds communication between them. Another benefit is the simplification of board assembly because there are fewer components to be placed on the board." *EX1028* at p. 4. Thus, a variety of benefits of vertically integrating chips was known.

84. In addition to vertically stacking chips, it was well known that integrated circuit chips could be attached on opposing sides of an interposer or circuit board. For example, Kinsman teaches attaching integrated circuits to opposing sides of a dielectric circuit board. "One way to satisfy the demand for increased integrated circuit density is to attach integrated circuits to opposing sides of a dielectric circuit board. A technique developed by the semiconductor industry to couple integrated circuits positioned on opposite sides of a circuit board to each other has been the creation of conductive vias through circuit boards. FIG. 1 is a partial isometric view of a circuit board 1 comprising a substrate 8 with holes 10 extending through its thickness 11 in any desired arrangement according to the prior art. The substrate 8 may comprise a BT or FR dielectric core, and the methods used to make the holes 10 include drilling, etching and laser ablation." *EX1029* at [0003]. Thus, it was known that multiple semiconductor chips, such as integrated circuits, could be coupled to opposing sides of a substrate to increase integrated circuit density.

85. Savastiouk also suggests attaching integrated circuit structures on opposing sides of substrate by stating that PCB 130, which is positioned beneath interposer 120 on an opposing side of integrated circuit dies 124 can be "replaced with another integrated circuit structure (a die or a wafer)." *EX1017* at 3:22-23; *see also I.D.* at FIGs. 2 and 3.

86. It was well known that semiconductor chips could include processing units such as central processing units and graphics processing units. More specifically, packaged systems included multiple distinct processing units. For example, Lin'152 teaches a system-on chip (SOC) including both a graphics processing unit and a central processing unit. "[A] system-on chip (SOC) including a graphics-processing-unit (GPU) circuit block, a wireless local area network (WLAN) circuit block and a central-processing-unit (CPU) circuit block designed by x86 architecture or by non x86 architectures, but not including any baseband circuit block," *EX1030* at [1000].

87. Integration of central processing units and graphics processing units on a single chip, as well as the benefits associated with such integration, were well known in advance of the '768 Patent. For example, it was known as early as 2011 that the "integration trend of CMOS devices has led to fused architectures, in which the central processing units (CPUs) and graphics processing units (GPUs) are integrated onto the same chip." *EX1031* at p. 1. "Recent examples include Intel's sandy bridge [21], on which CPUs and GPUs are on one chip with a shared on-chip L3 cache, and AMD accelerated processing unit (APU) [26] on which both on-chip CPUs and GPUs share the same off-chip memory [19]." *EX1031* at p. 1. Such combined GPU/GPU architectures were known to provide benefits such as the "opportunity to leverage both the high computational power from GPUs for regular

applications and flexible execution from CPUs for irregular workloads" as well as bypassing "costly CPU-GPU data transfers[.]" *EX1031* at p. 1-2.

88. It was known that semiconductor chips may also comprise various insulating (dielectric) materials with interconnection structures therein that were used to connect such chips to each other and to chip packages. For example, Savastiouk teaches that "[e]ach die 124.1 has one or more metalized through vias 330.1 formed in the die's semiconductor substrate 140.1 (e.g. monocrystalline silicon). Each via 330.1 passes between the top and bottom surfaces of substrate 140.1. Conductive paths are provided from contact pads at the top of each die 124.1 to contact pads 340.1 at the bottom of the die through the vias 330.1. Contact pads 340.1 protrude out of the respective vias 330.1. The dies 124.1 can be manufactured using the same techniques as described above for interposer 120 (involving the wafer thinning to expose the contact pads 340.1). Each die may have the same general structure as interposer 120 in FIGS. 10–12. Of course, the circuitry in dies 124.1 does not have to be identical to the interposer circuitry, and different dies 124.1 may differ from each other. Also, contact pads 340.1 may have smaller dimensions, and may be placed closer to each other, as they do not have to meet the BT substrate dimension requirements. Pads 340.1 can be copper/nickel/gold structures as in FIG. 12, or they can be made from other materials. The metal in vias 330.1 is insulated from substrate 140.1 by a dielectric 410 (FIG. 12)." *EX1017* at 10:30-50.

Additionally, Savastiouk teaches that "[d]ies 124.2 may be similar to dies 124.1. Dies 124.2 include metalized vias 330.2 in semiconductor substrates 140.2, and contact pads 340.2 protruding out of the vias on the bottom." *EX1017* at 10:62-65.

VI. SUMMARY OF THE PRIOR ART REFERENCES

A. *Sundaram*

89. Sundaram describes "various 3D packaging schemes" such as "a system-in-package (SIP) structure[,]" a "package-on-package (POP) structure[,]" a "face-to-face (F2F) structure[,]" and a "logic bottom stack [] structure." *EX1004* at 1:33-42 Sundaram further describes that "multi-die stacking with TSVs imposes great challenges in forming TSVs within complementary metal oxide semiconductor (CMOS) chips, power delivery, testability, reliability, and thermal management of the logic chip, all of which remain major barriers in achieving high bandwidth for 3D ICs." *EX1004* at 2:1-6. Sundaram teaches various "interposer interconnect structure[s]" and explains "embodiments of the present invention provide a testable interposer interconnect structure[.]" *EX1004* at 2:24-67. The term "interposer interconnect structure" may "refer to connecting devices to form a package[.]" *EX1004* at 5:16-19

90. As shown below in FIG. 3, Sundaram teaches an "interconnect structure 100" having an "interposer 105" with a "first side 115 and a second side 120." *EX1004* at 5:46-48. Interposer 105 "can be made of many substrate materials, for

example, glass, silicon, ceramic, polymer-glass laminates, and flexible polymers." *EX1004* at 5:54-56. There are a "plurality of small through vias 110…within the interposer 105" that "extends from the first side 115 to the second side 120." *EX1004* at 6:6-9. Sundaram's "through vias 110 can be metalized in such a way that the metallization provides die pad surfaces 135 that correspond to each of the vias 110" where the metallization material is "a highly-conductive metal, for example copper." *EX1005* at 6:22-27.

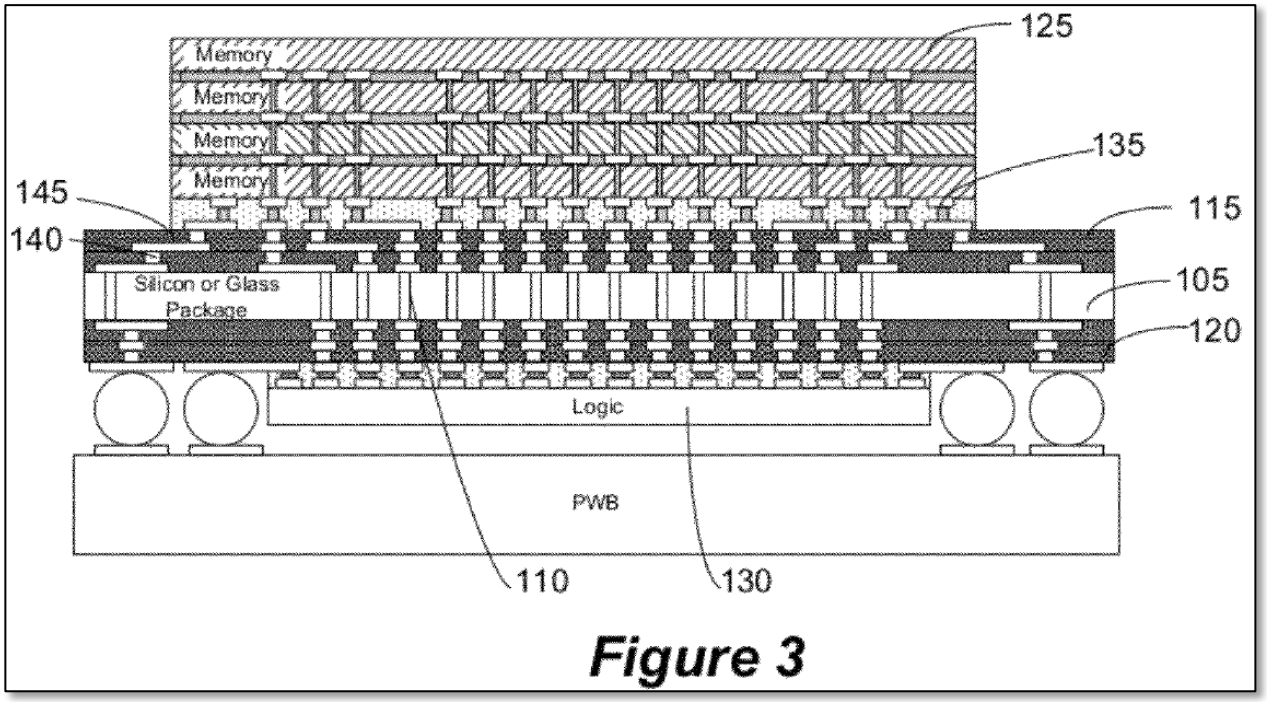


Figure 3

EX1004 at FIG. 3.

91. As shown above, a "first electronic device 125 can be attached to the first side 115 of the interposer 105 and a second electronic device 130 can be attached to the second side 120 of the interposer 105." *EX1004* at 6:34-36. first

electronic device 125 "can be single or stacked memory IC devices, and the second electronic device 130 can be a logic IC device or devices." *EX1004* at 6:37-39. Though "other electronic devices can also be used as the first electronic device 125 and/or the second electronic device 130." *EX1004* at 6:39-42. Interposer 105 and through vias 110 "work to electrically connect the first electronic device 125 and second electronic device 130." *EX1004* at 6:46-50. Additionally, as shown above, Sundaram's interconnect structure 100 comprises "blind vias 140 and conductor traces 145 defined within polymer-metal redistribution layers deposited on the first side 115 and second side 120 of interposer 105." *EX1004* at 6:62-67. Sundaram's teachings allow for the "interposer 105 and the package [sic] can be one and the same." *EX1004* at 7:61-67.

92. I have been informed that for a prior art reference to be proper for use in an obviousness analysis, the reference must be "analogous art" to the claimed invention. I have been informed that a prior art reference is analogous to the claimed invention if the reference is from the same field of endeavor as the claimed invention or if it is reasonably pertinent to the particular problem that the inventor was trying to solve.

93. As discussed above, the field of endeavor of the claimed invention of the '768 Patent includes semiconductor packaging. *See* ¶¶ 31-33. As demonstrated above, Sundaram is directed to "interposer interconnect structure[s]" which may

"refer to connecting devices to form a package[.]". *EX1004* at 5:16-19. Thus, Sundaram is directed to semiconductor chip packaging and accordingly is in the same field of endeavor as the claimed invention of the '768 Patent.

94. Sundaram is also reasonably pertinent to the problems solved by the inventors of the '768 Patent. As discussed above, the '768 Patent is directed to minimizing temperature coefficient of expansion mismatching. *See* ¶¶ 34-38. Sundaram teaches that "[g]lass presents several advantages, namely, silicon-matched coefficient of thermal expansions (CTE)[.]" *EX1004* at 5:62-63. Thus, a POSITA would have consulted Sundaram and applied its teachings when faced with the problem of minimizing temperature coefficient of expansion mismatching. Additionally, the '768 Patent is directed to creating chip packages with pre-testability capability. *See* ¶¶ 34-38. Sundaram is concerned with the "testability" of 3D ICs and provides a "testable interposer interconnect structure." *EX1004* at 7:41-43, 2:34-35. Thus, a POSITA would have consulted Sundaram and applied its teachings when faced with the problem of creating chip packages with pre-testability capability. Finally, the '768 Patent is concerned with the impact of miniaturization on circuit performance. *See* ¶¶ 34-38. Sundaram is likewise concerned with "ultra-fine pitch and ultra-short interconnections" in chip packages and associated "challenges[.]" *EX1004* at 1:65–2:20, *see also* 1:15-32, 2:21–3:6. Thus, a POSITA

would have consulted Sundaram and applied its teachings when faced with the problem of the impact of miniaturization on circuit performance.

B. *Haba*

95. Haba teaches an interposer having molded low CTE dielectric for use as an interconnection component in microelectronic assemblies. *EX1009* at Abstract. Haba explains that interposers are commonly used in electronic packaging "to facilitate connection between components with different connection configurations or to provide needed spacing between components in a microelectronic assembly." *EX1009* at 1:7-10. Traditional interposers "can include a dielectric element in the form of a sheet or layer of dielectric material having numerous conductive traces extending on or within the sheet or layer" and "conductive elements such as conductive vias extending through the layer of dielectric material to interconnect traces in different levels." *EX1009* at 1:8-18. However, "when structures within an interconnection component have differing CTEs, the different amounts by which they expand and contract due to changing temperatures can apply stresses … which can lead to delamination or cracking under certain conditions." *EX1009* at 6:6-11.

96. To address these issues, Haba proposes an interposer structure that incorporates "a plurality of substantially rigid solid metal posts extending away from a reference surface" and a dielectric layer molded around the posts, where the dielectric layer has "a coefficient of thermal expansion of less than 8 ppm/°C."

EX1009 at 1:44-55. The dielectric layer "contact[s] the edge surfaces [of the posts] and fill[s] spaces between adjacent ones of the posts," while leaving the post end surfaces exposed to serve as wettable contacts. *EX1009* at 1:49-51. Haba emphasizes that "the interconnection component has no interconnects between the first and second end surfaces of the posts that extend in a lateral direction." *EX1009* at 1:55-55. "As shown in the Figures, interconnection component 2 is free from any electrically conductive interconnects running between the posts 10 or elsewhere in an at least partially lateral direction (parallel to the surfaces 26,28 of dielectric layer 20) within the dielectric material between the end surfaces 10A and 10B. Traces 30 or the like can be used to form connections running in a lateral direction outside of the area between end surfaces 10A and 10B." *EX1009* at 6:27-34.

97. Haba explains that "the posts can be formed from materials such as: gold, copper, copper alloy, aluminum, or nickel" and "can also be in the form of conductive pins … organized, for example, in one or more grid-like patterns having a pitch in a range from 100 to 10000 μm (e.g., 400-650 μm)." *EX1009* at 2:37-40, 5:33-39. "Widths of the end surfaces 10A, and 10B are generally selected in a range from about 50 to 1000 μm" and post edge surfaces "can form a substantially cylindrical shape[,]" "a substantially frustroconical shape[,]" or "a surface of revolution formed by a parabola." *EX1009* at 5:30-32, 8:41-51. In some embodiments, "an anchoring feature, such as ridge 15 is formed therein, which helps

secure post 10 in position within dielectric layer 20." *EX1009* at 8:65–9:1. The dielectric material have a low-CTE and may include "low temperature co-fired ceramic, liquid crystal polymer, glass or high filler content epoxy, among others." *EX1009* at 6:20-27.

98. Haba further discloses the use of redistribution layers (RDLs). For example, FIG. 8 illustrates a "redistribution layer 60" having "traces 30 [that] can electrically connect to and overlie respective end surfaces 10A[.]" *EX1009* at 6:62-65. Haba's FIG. 9B depicts a "second redistribution layer 70" comprising "traces 30 and additional conductive vias 26 formed within redistribution dielectric 72." *EX1009* at 7:57-65.

99. Haba teaches that by molding posts in a low-CTE dielectric there is "reduced stress at the bonding interface can permit reductions in solder bump sizes at the bonding interface to help achieve finer pitch." *EX1009* at 5:55–6:5. The structure thereby "will expand and contract by closer amounts, thereby potentially reducing the likelihood of bonding interface failures," so that "a component having such a dielectric material layer can be less likely … to have posts or pins 10 become detached…during use." *EX1009* at 6:11-18. Moreover, the redistribution layers enable configurations where "the first wettable contacts can define a first pitch and the second wettable contacts can define a second pitch that is smaller than the first pitch." *EX1009* at 4:36-39. The wettable contacts facilitate redistribution layers that

allow "interconnection component 2 to be used to connect to a microelectronic component having a different connection configuration than the configuration of posts 10" thereby accommodating "components with respective contacts having different pitches or other different configurations." *EX1009* at 7:27-31, 7:43-45.

100. Haba illustrates that interconnection components may be incorporated into larger electronic systems. For example, "the interconnection components described above can be utilized in construction of diverse electronic systems," and that "a system 90 … can include a microelectronic assembly … and a circuit panel … within a common housing 91," such as "a portable housing of the type usable, for example, in a cellular telephone or personal digital assistant.". *EX1009* at 11:1-45. Thus, Haba provides "an interconnection component" including "a plurality of substantially rigid solid metal posts" embedded in "a dielectric layer having a coefficient of thermal expansion of less than 8 parts per million per degree Celsius (ppm/°C.)," with "first and second pluralities of wettable contacts … usable to bond the interconnection component to at least one of a microelectronic element and a circuit panel," thereby providing improved assemblies for "microelectronic packaging." *EX1009* at 11:1-25.

101. I have been informed that for a prior art reference to be proper for use in an obviousness analysis, the reference must be "analogous art" to the claimed invention. I have been informed that a prior art reference is analogous to the claimed

invention if the reference is from the same field of endeavor as the claimed invention or if it is reasonably pertinent to the particular problem that the inventor was trying to solve.

102. As discussed above, the field of endeavor of the claimed invention of the '768 Patent includes semiconductor packaging. *See* ¶¶ 31-33. As demonstrated above, Haba is directed to "interposers" used in "microelectronic assemblies" including "one or more packaged microelectronic elements such as one or more semiconductor chips[.]" *EX1009* at 1:18-28, *see also* 8:18-40. Accordingly, Haba is in the same field of endeavor as the claimed invention of the '768 Patent.

103. Haba is also reasonably pertinent to the problems solved by the inventors of the '768 Patent. As discussed above, the '768 Patent is directed to solving the problem of minimizing temperature coefficient of expansion mismatching. *See* ¶¶ 34-38. As demonstrated above, Haba discloses "the present invention relates to interconnection components, such as interposers" *EX1009* at 1:53-55, and more particularly to "an interconnection component" with "a dielectric layer having a coefficient of thermal expansion of less than 8 ppm/°C." *EX1009* at 3:36-38. By using such a low-CTE dielectric, "the structures will expand and contract by closer amounts, thereby potentially reducing the likelihood of bonding interface failures," so that "a component having such a dielectric material layer can be less likely … to have pins 210 become detached … during use." *EX1009* at 1:53-

55, 3:36-38, 5:55–6:5, 6:6-18. Thus, a POSITA would have consulted Haba and applied its teachings when faced with the problem of minimizing temperature coefficient of expansion mismatching.

C. *Lin-191*

104. Lin-191 teaches system-in-package or multichip module architectures that incorporate multi-layer chips within a multi-layer polymer structure, supported by on-chip and intra-chip metal bumps together with patterned metal layers. These modules provide electrical connection between multiple semiconductor chips and external circuits via "on-chip metal bumps, the intra-chip metal bumps, and the patterned metal layers." *EX1005* at Abstract. For example, chips are disclosed as being connected through multiple metal interconnects, including "patterned metal layers 2, 3, 4 and 5 and the metal pillars or bumps[.]" *EX1005* at [0462].

105. Lin-191 teaches specific thickness ranges for substrates and polymeric dielectric layers that are used in packaging semiconductor chips. For example, the substrate 110 may have a "thickness T1 between about 10 and about 1,000 micrometers, between 10 and 100 micrometers or between 100 and 500 micrometers." *EX1005* at [0051]. Dielectric or insulating layer such as layer 10 can be formed of "silicon dioxide (SiO2), silicon nitride, silicon oxynitride, silicon carbon nitride, polyimide, epoxy, benzocyclobutane (BCB), polybenzoxazole (PBO), poly-phenylene oxide (PPO), silosane or SU-8 having a suitable thickness,

e.g., between 0.3 and 30 micrometers, and preferably between 1 and 10 micrometers." *EX1005* at [0052]. Additional dielectric layers such as insulating layer 15 are disclosed with thicknesses "between 1 and 20 micrometers, and preferably between 3 and 15 micrometers or between 5 and 10 micrometers[.]" *EX1005* at [0291]. Encapsulation is provided by polymer molding layers such as encapsulating layer 85, which has a thickness "between about 20 and about 500 micrometers, and preferably between 30 and 100 micrometers." *EX1005* at [0109]. Build-up polymer layers including polymer layer 78 are specified at thicknesses "between 5 and 50 micrometers, and preferably between 5 and 15 micrometers or between 5 and 10 micrometers[.]" *EX1005* at [0368]. A "passivation layer 501 over the semiconductor substrate 601" may be formed. *EX1005* at [0552].

106. Lin-191 also describes interconnects and bump structures that connect the layers described above. For example, bumps 24 are described as having a "height greater than 5 micrometers, such as between 5 and 50 micrometers, and preferably between 10 and 20 micrometers," while bumps 14 are larger, with a "height greater than 15 micrometers, such as between 15 and 520 micrometers, and preferably between 20 and 110 micrometers[.]" *EX1005* at [0066], [0099]. At the package level, solder balls for external board connection are described. *EX1005* at [0007], [0048], [0490].

107. Lin-191 incorporates passive devices directly into the package. In one embodiment, a chip "can be replaced by a passive component 67, such as capacitor, inductor or resistor." *EX1005* at [0340]. In another embodiment, discrete passive components 910 are mounted between upper-tier chips, coupled through "multiple solder joints 915[,]" "patterned metal layer 7,", and "bumps 64[.]" *EX1005* at [0364]-[0368]. A polymer layer such as polymer layer 78 can be formed "on the discrete passive components 910." *EX1005* at [0364]-[0368].

108. Lin-191 further discloses multiple semiconductor chips integrated into a single package. These chips "can be a central-processing-unit (CPU) chip designed by x86 architecture, a central-processing-unit (CPU) chip designed by non x86 architectures, such as ARM, Strong ARM or MIPs, a baseband chip, a graphics-processing-unit (GPU) chip, a digital-signal-processing (DSP) chip, a wireless local area network (WLAN) chip, a memory chip, such as flash memory chip, dynamic-random-access-memory (DRAM) chip or statistic-random-access-memory (SRAM) chip, a logic chip, an analog chip, a power device, a regulator, a power management device, a global-positioning-system (GPS) chip, a Bluetooth chip…" *EX1005* at [0240], [0382]. Electrical connections between chips are made through "metal layer 63 of the patterned metal layer 6 and on tops of the metal pillars or bumps 54 and 64[.]" *EX1005* at [0241].

109. Lin-191 discusses the use of the multichip modules for pre-testability capability. Lin-191 explains that wafer level packaging allows for the integration of pre-testability "before being singulated by dicing for final assembly into a chip carrier package[.]" *EX1005* at [0006]. Lin-191 describes that the "testing circuit is either (i) the wafer level testing performed before the chip 700 or 800 is sawed or diced apart from a wafer, or (ii) the package level testing (the final testing) after the chips 700 and 800 are connected to each other" *EX1005* at [0492]. Each chip is equipped with dedicated test structures, as "the chip 700 may include … two testing interface circuits 333a and 333b" while "the chip 800 may include … two testing interface circuits 333c and 333d" *EX1005* at [0462]. These test interfaces may be implemented as scan test circuits where each "of the test interface circuits 333a, 333b, 333c and 333d … can be a scan test circuit … used for scan testing … at wafer level … or at the package level testing (the final testing)[.]" *EX1005* at [0493].

110. I have been informed that for a prior art reference to be proper for use in an obviousness analysis, the reference must be "analogous art" to the claimed invention. I have been informed that a prior art reference is analogous to the claimed invention if the reference is from the same field of endeavor as the claimed invention or if it is reasonably pertinent to the particular problem that the inventor was trying to solve.

111. As discussed above, the field of endeavor of the claimed invention of the ’768 Patent includes semiconductor packaging. *See* ¶¶ 31-33. As demonstrated above, Lin-191 is directed to “system-in packages, or multichip modules… includ[ing] multi-layer chips in a multi-layer polymer structure, on-chip metal bumps on the multi-layer chips, intra-chip metal bumps, in the multi-layer polymer structure, and patterned metal layers in the multi-layer polymer structure.” *EX1005* at [0007], [0003]. Thus, Lin-191 is directed to semiconductor packaging and accordingly is in the same field of endeavor as the claimed invention of the ’768 Patent.

112. Lin-191 is also reasonably pertinent to the problems solved by the inventors of the ’768 Patent. As discussed above, the ’768 Patent is directed to solving the problem of providing chip packages with pre-testability capability. *See* ¶¶ 34-38. As demonstrated above, Lin-191 discloses that “the chip 160 may have built-in self test (BIST) circuits for reducing the testing time for the system-in package or multichip module.” *EX1005* at [0401]. Further, Lin-191 describes test structures such as “testing interface circuits 333a–333d” that can be used for wafer-level or package-level scan testing before or after the chips are diced and packaged. *EX1005* at [0462], [0492]-[0493]. Thus, a POSITA would have consulted Lin-191 and applied its teachings when faced with the problem creating chip packages with

pre-testability capability. *See also EX1005* at [0006], [0105], [0173], [0239], [0401] (all concerned with testing in a chip package).

D. *Yu*

113. Yu describes that a "Package-on-Package (PoP) is an integrated circuit packaging technique to allow vertically combining discrete logic and memory ball grid array (BGA) packages." *EX1010* at 1:49-55. Accordingly, Yu teaches a PoP structure comprising a package 202. *EX1010* at 2:9-10, 2:15-16, 8:26-39. Yu's package 202 comprises a "core material, such as molding compound 18" made of an "epoxy, polyimide, silicone rubber…or a combination thereof" that is cured over a "first die 10[.]" *EX1010* at 2:61-67. Yu's package further comprises a "front side interlayer dielectric (ILD) and redistribution layer (RDL) structure" made of a "first front side metallization layer 20" and a "first ILD layer 22" made of polyimide. *EX1010* at 3:4-22. Additional metallization layers and ILD layers, "such as a second metallization layer 24 and a second ILD layer 26" are formed as part of the front side RDL. *EX1010* at 3:28-32.

114. TMV openings 36 are "formed through the molding compound 18 to the front side metallization layer 20" then a copper "seed layer is deposited…into the TMV openings 36." *EX1010* at 3:56-65. "A conductive material, such as copper" is then deposited on the back side by "electroplating" thereby forming "TMVs 38[.]" *EX1010* at 3:67–4:6. Yu's package 202 additionally includes a "back side ILD and

RDL structure" formed of a "first back side ILD layer 40, a second back side metallization layer 42, a second ILD layer 44, and openings 46 and 48 through the second ILD layer 44 to the second back side metallization layer 42." *EX1010* at 4:7-11. As shown in the figure below, a "second die 52, such as a memory die…is attached through the opening 46 to conductive features in the second back side metallization layer 42, such as by conductive connectors 54, like controlled collapse chip connection (C4) bumps." *EX1010* at 4:30-34. "[C]onductive connectors 58, such as ball grid array (BGA) balls" are formed on package 202 which may be a "lead-free solder." *EX1010* at 4:45-50. Finally, a "third die 62, such as a memory die [is]…attached through the openings 30 to conductive features in the second front side metallization layer 24" also by C4 bumps. *EX1010* at 4:53-60.

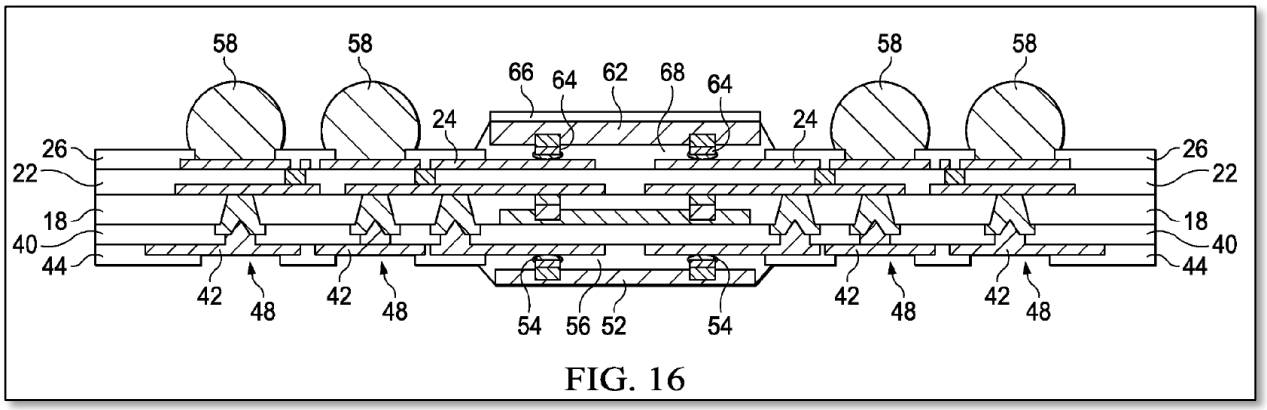


FIG. 16

EX1010 at FIG. 16.

115. The package of FIG. 16 may be stacked alongside additional packages forming the PoP structure:

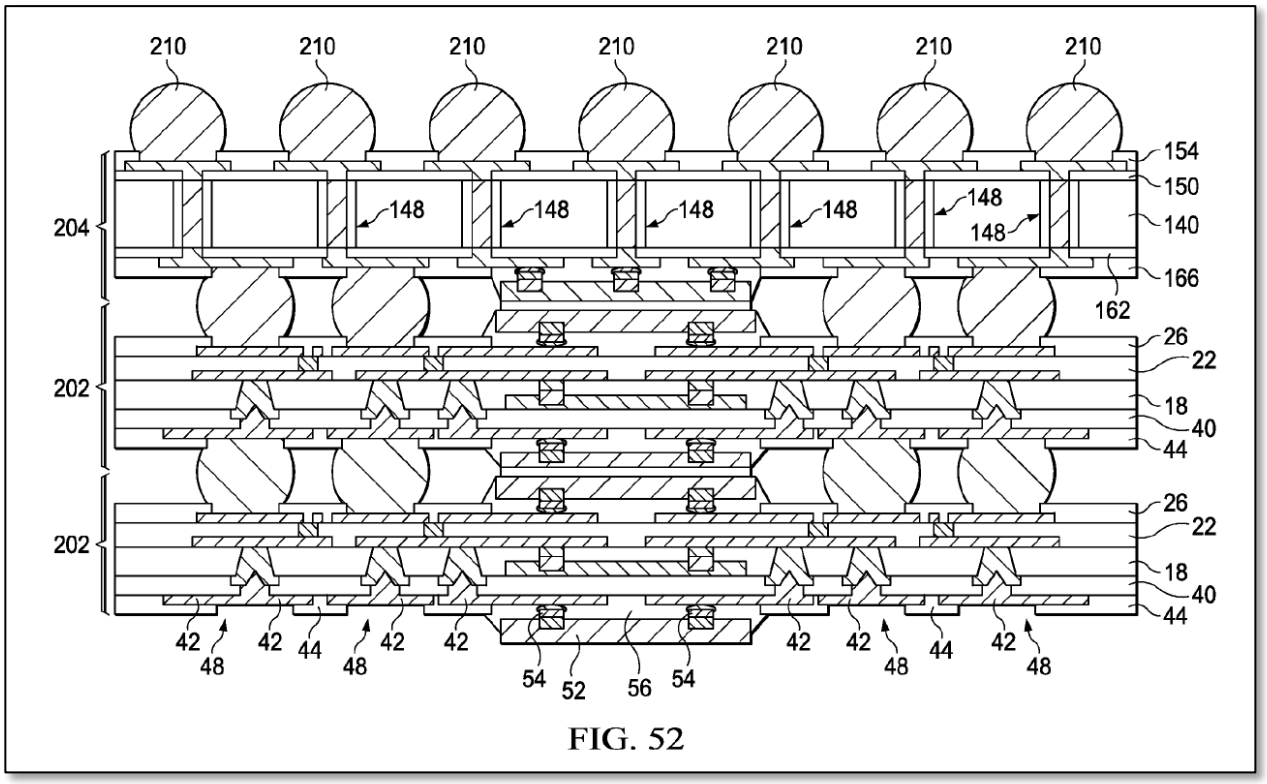


FIG. 52

EX1010 at FIG. 52.

116. In one embodiment, Yu teaches forming an "interposer and a die attached to the interposer" and teaches, with reference to a "substrate 140" used in forming the interposer that "it is believed that using silicon substrates for the interposer may reduce stress because the coefficient of thermal expansion (CTE) mismatch between the silicon substrates and the silicon typically used for the dies is lower than with substrates formed of different materials." *EX1010* at 6:14-26.

117. I have been informed that for a prior art reference to be proper for use in an obviousness analysis, the reference must be "analogous art" to the claimed invention. I have been informed that a prior art reference is analogous to the claimed

invention if the reference is from the same field of endeavor as the claimed invention or if it is reasonably pertinent to the particular problem that the inventor was trying to solve.

118. As discussed above, the field of endeavor of the claimed invention of the '768 Patent includes semiconductor packaging. *See* ¶¶ 31-33. As demonstrated above, Yu is directed to "Package-on-Package (PoP)" structures including "integrated circuit packaging[.]" *EX1010* at 1:49-55, *see also* 1:10-48, 1:63-67. 5:17-20. Thus, Yu is directed to semiconductor chip packaging and accordingly is in the same field of endeavor as the claimed invention of the '768 Patent.

119. Yu is also reasonably pertinent to the problems solved by the inventors of the '768 Patent. As discussed above, the '768 Patent is directed to solving the problem of minimizing temperature coefficient of expansion mismatching. *See* ¶¶ 34-38. As demonstrated above, Yu teaches that "it is believed that using silicon substrates for the interposer may reduce stress because the coefficient of thermal expansion (CTE) mismatch between the silicon substrates and the silicon typically used for the dies is lower than with substrates formed of different materials." *EX1010* at 6:20-26. Thus, a POSITA would have consulted Yu and applied its teachings when faced with the problem of minimizing temperature coefficient of expansion mismatching. Additionally, the '768 Patent is directed to solving the problem creating chip package with pre-testability capability. *See* ¶¶ 34-38. Yu teaches "a

step to test the PoP structure[.]" *EX1010* at 2:17-20. Thus, a POSITA would have consulted Yu and applied its teachings when faced with the problem of creating chip package with pre-testability capability.

E. *Camacho*

120. Camacho teaches that a "need exists for PoP [Package-on-Package] vertical integration compatible with WLSCPs" (wafer level chip scale packge). *EX1006* at [0010], [0008].Camacho teaches techniques for forming through-silicon vias (TSVs) and vertically integrated packages. Specifically, Camacho teaches that "a plurality of vias is formed through semiconductor wafer 120" and that the "vias are filled with Al, Cu, Sn, Ni, Au, Ag, titanium (Ti), W…to form conductive TSV 134." *EX1006* at [0043]. These TSVs provide vertical electrical interconnections between conductive layers, as "conductive layers 130 and 132 are electrically connected by TSV 134." *EX1006* at [0043]. Camacho's TSVs provide a method for establishing reliable electrical pathways through the semiconductor wafer using conductive materials well-known in the art.

121. Camacho further illustrates how stacked dies may be electrically connected using flip-chip technology. As shown in Figure 3d, Camacho describes mounting a "semiconductor die or package 140" to die 122 "in a flipchip arrangement with bumps 142 electrically connected to a conductive layer 130b."

EX1006 at [0044]. This arrangement shows a die-to-die interconnection scheme that leverages solder bumps to form connections to underlying conductive layers.

122. Additionally, Camacho teaches embodiments involving multiple semiconductor chips in stacked configurations. For example, Camacho teaches a "semiconductor die or package 150" that is positioned on top of die 122. *EX1006* at [0047]. Camacho also provides details on the electrical connectivity of the upper die/package. Specifically, Camacho explains that die 150 includes "[c]ontact pads 152…electrically connected to bumps 148, conductive layer 130a, TSVs 134, and conductive layer 132a." *EX1006* at [0047]. Moreover, Camacho discloses earlier embodiments in which contact pads are explicitly described as metal. For instance, with respect to FIGS. 2A–2C, Camacho teaches "contact pads 76" that are "one or more layers…of aluminum (Al), copper (Cu), tin (Sn), nickel (Ni), gold (Au), or silver (Ag)[.]" *EX1006* at [0035].

123. Additionally, Camacho teaches that "the flip chip semiconductor device provides a short electrical conduction path from the active devices on semiconductor die 58 to conduction tracks on PCB 52 in order to…lower capacitance, and improve overall circuit performance." *EX1006* at [0038]. A POSITA would have understood Camacho to be referring to parasitic capacitance, as shortening electrical pathways was known to decrease parasitic capacitance that degrades signal quality.

124. I have been informed that for a prior art reference to be proper for use in an obviousness analysis, the reference must be "analogous art" to the claimed invention. I have been informed that a prior art reference is analogous to the claimed invention if the reference is from the same field of endeavor as the claimed invention or if it is reasonably pertinent to the particular problem that the inventor was trying to solve.

125. As discussed above, the field of endeavor of the claimed invention of the '768 Patent includes semiconductor packaging. *See* ¶¶ 31-33. As demonstrated above, Camacho is directed to the field of semiconductor device packaging, and in particular to wafer level chip scale packages (WLCSPs), through-silicon vias (TSVs), and package-on-package (PoP) vertical interconnections. *EX1006* at [0001], [0008]-[0009]. As explained, "the electrical interconnection between a wafer level chip scale package (WLCSP) containing semiconductor devices on multiple levels (3-D device integration) and external devices can be accomplished with conductive through silicon vias (TSV) or through hole vias (THV)." *EX1006* at [0008], *see also* [0016]. Thus, Camacho is directed to semiconductor chip packaging and accordingly is in the same field of endeavor as the claimed invention of the '768 Patent.

126. Camacho is also reasonably pertinent to the problems solved by the inventors of the '768 Patent. As discussed above, the '768 Patent is directed to solving the problem of the impact of miniaturization of circuit performance. *See* ¶¶

34-38. Camacho is also directed to addressing the problem of the impact of miniaturization on circuit performance, specifically the need for planarization to enable smaller and more densely packed circuit components. Camacho explains that "[d]epositing a thin film of material over an existing pattern can exaggerate the underlying pattern and create a non-uniformly flat surface" and that "a uniformly flat surface is required to produce smaller and more densely packed active and passive components." *EX1006* at [0028]. To address this, Camacho teaches that "planarization can be used to remove material from the surface of the wafer and produce a uniformly flat surface," where the process involves "polishing the surface of the wafer with a polishing pad" and adding an "abrasive material and corrosive chemical" such that "the combined mechanical action of the abrasive and corrosive action of the chemical removes any irregular topography, resulting in a uniformly flat surface." *EX1006* at [0028]. Thus, a POSITA would have consulted Camcho and applied its teachings when faced with the problem of the impact of miniaturization of circuit performance.

127. Additionally, the '768 Patent is directed to solving the problem of parasitic capacitance of interconnections in a chip package. *See* ¶¶ 34-38. As discussed, Camacho is concerned with "lower[ing] capacitance" in a chip package. *See* ¶ 123; *EX1006* at [0038]. Thus, a POSITA would have consulted Camacho and

applied its teachings when faced with the problem of parasitic capacitance of interconnections in a chip package.

VII. SUMMARY OF UNPATENTABILITY

128. I have reproduced the Proposed Grounds of Unpatentability from the Petition for ease of reference:

Grounds	Claims Challenged	35 U.S.C. §	References
1A	1-15, 20	103	Sundaram (EX1004), Haba, (EX1009), and Lin-191 (EX1005)
1B	16-19, 21-28	103	Sundaram and Lin-191
2A	1-3, 5, 7-10, 14-15	103	Haba and Lin-191
2B	4, 6, 11-13	103	Haba, Lin-191, and Sundaram
3A	16-17, 19, 22-28	103	Yu (EX1010) and Lin-191
3B	18, 21	103	Yu, Lin-191, and Camacho (EX1006)
3C	20	103	Yu, Lin-191, and Haba

VIII. OPINIONS REGARDING GROUND 1A: CLAIMS 1-15 AND 20 ARE OBVIOUS OVER SUNDARAM, HABA, AND LIN-191

A. *Claim 1*

1. 1[Pre]: "A chip package comprising"

129. Sundaram teaches various "interconnect structure[s]" to "form a package[.]" *EX1004* at 5:16-19. As shown in FIG. 3 below, Sundaram's interconnect structure comprises an "interposer 105" that "electrically connect[s] the first

electronic device 125 and the second electronic device 130[,]" enabling the "interposer 105 and the package can [*sic*] be one and the same." *EX1004* at 5:45-48, 6:46-48, 7:61-63. The first electronic device 125 "can be single or stacked memory IC devices, and the second electronic device 125 can be a logic IC device or devices." *EX1004* at 6:37-39. ICs (integrated circuits) were known to be formed on semiconductor chips such that Sundaram's interconnect structure and electronic devices 125, 130 collectively form a *chip package*[1]. *See, e.g., EX1133* at 1:14-17 ("…has led to increasingly more complex **integrated circuits being produced** in an increasingly smaller space **on semiconductor chips**.").

[1] Claim language provided in italics. All drawing annotations added. Citations to a claim limitation and/or section number are to the limitations mapping in this Declaration and are incorporated by reference, including the motivations to combine and showing of reasonable expectation of success provided in the cross-referenced section. All reasonable expectations of success include the benefits described for the respective motivation to combine. All emphases added unless otherwise noted.

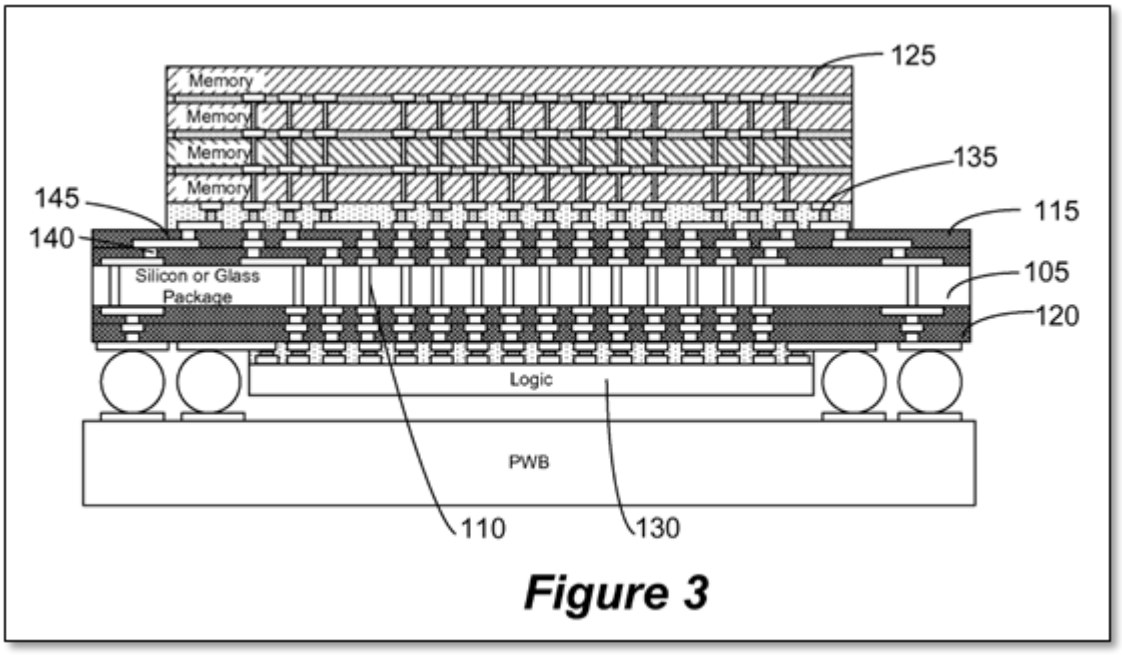


Figure 3

EX1004 at FIG. 3.

2. 1(a): "a first polymer layer having a first surface and a second surface opposite to said first surface,"

130. Sundaram's interconnect structure 100 "comprises an interposer having a first side and a second side" (i.e., *a first surface and a second surface*) and "can be made of… polymer-glass laminates, and **flexible polymers**" such that interposer 105 is a *first polymer layer*. *EX1004* at 2:22-27, 5:54-58. In other words, Sundaram identifies the interposer as a structure defined by two opposed surfaces, with the material of construction being polymeric, reinforced polymeric, or flexible polymer materials, thus teaching the claimed feature of a polymer layer forming part of the chip package.

131. FIG. 3 of Sundaram depicts interposer 105 with a *first surface* and a *second surface opposite to said first surface*. The *second surface* shown in FIG. 3 is *opposite* to the *first surface*, and the interposer functions as a substrate spanning between those opposed sides.

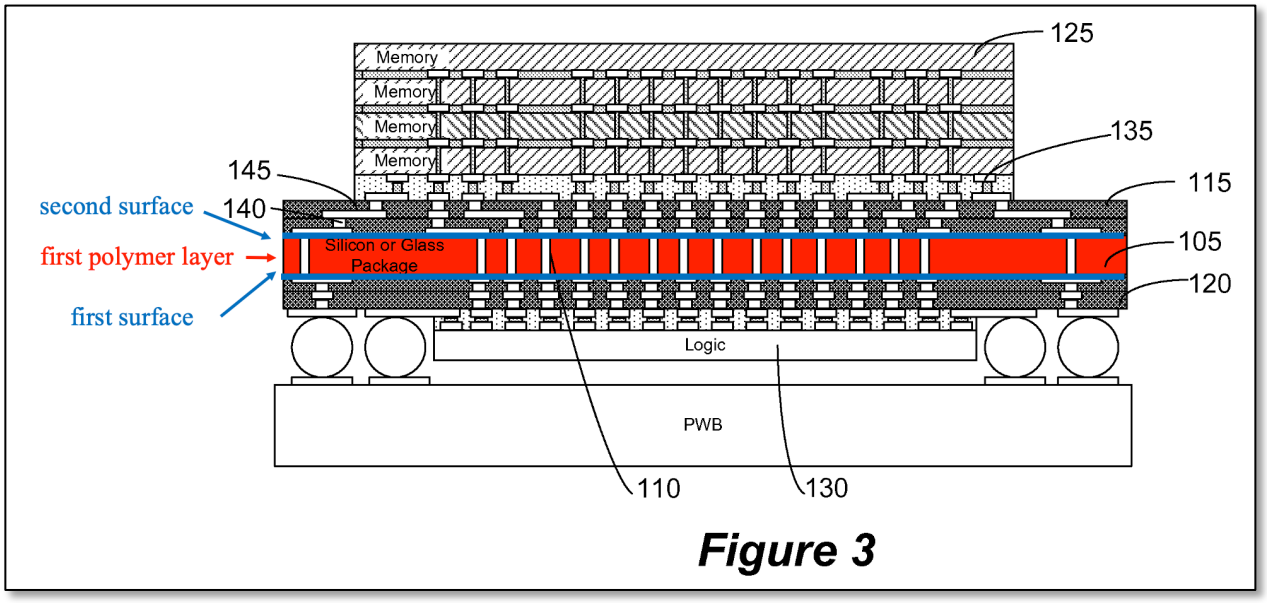


Figure 3

EX1004 at FIG. 3[2].

3. 1(a)(i): "wherein said first surface is substantially parallel to said second surface,"

132. Sundaram's *first surface* and *second surface* are parallel surfaces, as shown below. As such, Sundaram teaches *wherein said first surface is substantially parallel to said second surface*.

[2] Sundaram's original FIG. 3 includes the "Silicon or Glass Package" text; however, as mapped, Sundaram expressly teaches the interposer can be a *polymer*.

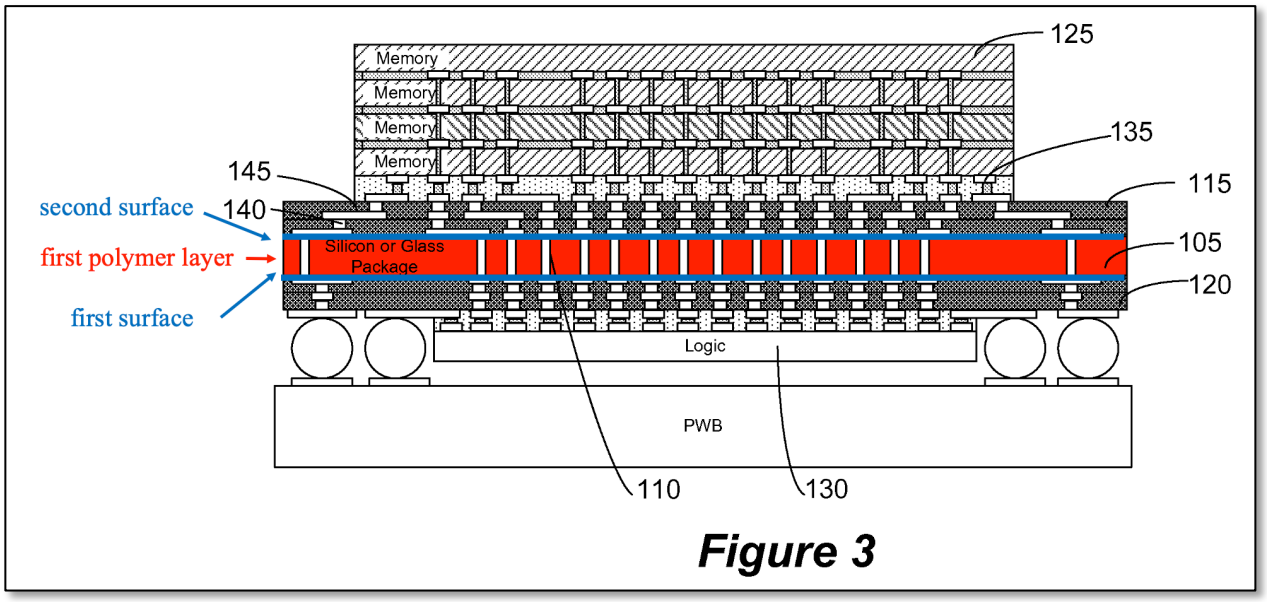


Figure 3

EX1004 at FIG. 3.

4. 1(a)(ii): "wherein said first polymer layer has a thickness between 100 and 300 micrometers and…"

133. Sundaram's interposer (*first polymer layer*) is "about 20 to about 200 micrometers in thickness." *EX1004* at 2:22-25. Because Sundaram teaches a range that overlaps the claimed range, Sundaram teaches or renders obvious Claim 1(a)(ii). Specifically, the claim recites a *thickness between 100 and 300 micrometers*, which overlaps with Sundaram's teaching of 20 to about 200 micrometers, namely the range of 100-200 micrometers within the 20-200 range. Sundaram therefore expressly teaches a thickness, specifically 100-200 micrometers, that is within the claimed range of *between 100 and 300 micrometers*.

134. I also note that the '768 Patent does not ascribe any criticality to the range of 100 and 300 micrometers. That is, the '768 Patent does not provide the

range of 100 and 300 micrometers and then further provide an explanation for why such range is needed, important, or advantageous. Indeed, the '768 Patent describes a variety of ranges, including smaller (20 micrometers) and much larger ranges (2000 micrometers), indicating to a POSITA that the thickness can widely vary and that the thickness is not otherwise critical, further supporting the presumption of obviousness. *See EX1001* at 7:53-57.

5. 1(a)(iii): "[wherein said first polymer layer] has a coefficient of expansion between 3 and 10 ppm/° C.;"

a) Haba's Teachings

135. Haba teaches an "interconnection component 2" having a "plurality of posts 10 within a dielectric layer 20." *EX1009* at 5:23-25. Like Sundaram's interposer 105, Haba's dielectric layer 20 is formed of a polymer. Specifically, dielectric layer 20 "can be formed from, for example, compositions which cure by chemical reaction to form a polymeric dielectric, such as epoxies and polyimides" and "can include particulate materials such as silica[,]" which is similar to Sundaram's interposer 105 being formed of "polymer-glass laminates[.]" *EX1009* at 5:41-44, 5:51-52; *EX1004* at 5:54-56. Notably, Haba expressly teaches that the "CTE [coefficient of thermal expansion] of the material used to form dielectric layer 20 can be in the **range of 8 parts per million per degree Celsius**[,]" which is *between 3 and 10 ppm/° C*. *EX1009* at 5:56-59.

136. Thus, because Haba teaches that the CTE of dielectric layer may be "in the range of 8 parts per million per degree Celsius" and because it was known that epoxy and polyimides (materials that Haba teaches may form dielectric layer 20) were known to have CTE's within the claimed range, Haba teaches [*wherein said first polymer layer*] *has a coefficient of expansion between 3 and 10 ppm/° C.*

b) Motivation to Combine

137. A POSITA would have found it obvious been motivated to modify Sundaram's interposer 105 to have *a coefficient of expansion between 3 and 10 ppm/° C.*, consistent with Haba's teaching. Haba expressly motivates the combination, stating the lower CTE "reduces the difference in the CTE between the interconnection component and…the microelectronic element 66," (a semiconductor chip) which in turn allows "reductions in solder bump sizes…to achieve finer pitch." *EX1009* at 5:67–6:5; 1:19-22. A POSITA would have recognized that Sundaram's interposer 105 serves the same structural role as Haba's interconnection component, i.e., a substrate between semiconductor chips.

138. Haba further motivates the modification by teaching that "when structures within an interconnection component have differing CTEs, the different amounts by which they expand and contract due to changing temperatures can apply stresses" on posts embedded therein which "can lead to delamination or cracking." *EX1009* at 6:6-11. By forming a dielectric layer "with a low-CTE, or one that is

closer to that of the conductive material used to form "posts or pins 10, the structures will expand and contract by closer amounts, thereby reducing the likelihood of bonding interface failures." *EX1009* at 6:14-18.

139. Because Sundaram's through vias 110 (discussed in more detail below at Claims 1(b)-1(b)(i)) and Haba's posts 10 are both made from copper, a POSITA would have recognized the applicability of Haba's teachings of a low-CTE dielectric to Sundaram's interposer 105, and would have been motivated to "reduc[e] to the likelihood of bonding interface failure" by modifying interposer 105 to have a CTE *between 3 and 10 ppm/° C. See* ¶¶ 144-146.

140. Further, Sundaram already contemplates such CTE matching, teaching. that using glass interposer is advantageous for achieving a "silicon-matched" CTE. *EX1004* at 5:62–65. A POSITA would have appreciated that a polymer interposer with Haba's CTE would provide comparable thermal matching while maintaining the flexibility and processability benefits of polymer materials. Thus, based on the combined teachings of Haba and Sundaram, a POSITA would have found it obvious and advantageous to select or formulate a polymer material for interposer 105 having a CTE *between 3 and 10 ppm/°C* to reduce CTE mismatch with Sundaram's semiconductor devices 125 and 130.

141. The combination represents the application of a known technique (forming an interposer or dielectric layer with a low-CTE polymer such as epoxy or

polyimide) to a known device (Sundaram's polymer interposer) to yield predictable results — namely, reduction in solder bump size and reduced likelihood of bonding interface failure, per Haba. *EX1009* at 5:67–6:5; 6:14-18. The modification would have been straightforward because suitable low-CTE polymers were readily available and widely used in semiconductor packaging before the '768 Patent, leading to a reasonable expectation of success. *See* ¶ 57; *see, also., EX1005* at [0596] ("The polymer layer 285 can be a polyimide or epoxy layer having a coefficient of thermal expansion smaller than 15, such as **between 3 and 6, between 2 and 8, between 5 and 10** or between 8 and 15."); *EX1105* at [0006] ("It is known that a film obtained from this polyimide exhibits a very low thermal expansion coefficient (5 to 10 ppm/°C)[.]").

142. Additionally, Sundaram's interposer 105 and Haba's dielectric layer 20 are already formed of similar materials, i.e., polymer with a filler. *EX1004* at 5:54-56 ("The interposer 105 can be made of…polymer glass laminates[.]"); *EX1009* at 5:51-54 ("For example, such additives can include particular materials such as silica…or fibrous reinforcements such as short glass fibers."), 6:24-26 ("Such materials include high filler content epoxy composites, wherein the filler is formed from glass[.]").

143. Thus, a POSITA applying these teachings would have reasonably expected that replacing Sundaram's generic polymer material with a known low-

CTE epoxy or polyimide formulation would predictably enhance reliability without introducing new processing difficulties. Additionally, it was well known that epoxy and polyimide layers were formulated to have a CTE within the claimed range. *See, e.g., EX1005* at [0596] ("The polymer layer 285 can be a polyimide or epoxy layer having a coefficient of thermal expansion smaller than 15, such as **between 3 and 6, between 2 and 8, between 5 and 10** or between 8 and 15."); *EX1105* at [0006] ("It is known that a film obtained from this polyimide exhibits a very low thermal expansion coefficient (5 to 10 ppm/°C)[.]").

6. 1(b): "a first metal plug vertically in a first through via in said first polymer layer,"

144. Sundaram teaches a "plurality of ultra-small through vias 110 can be defined within the interposer 105 such that each of the through vias 110 extends from the first side 115 to the second side 120 of the interposer 105." *EX1004* at 6:6-9. Sundaram's through vias 110 are "metalized with a highly-conductive metal, for example copper." *EX1004* at 6:25-27. Sundaram teaches "through vias 110 can be defined within the interposer" (*in said first polymer layer*) and "can be metalized with a highly-conductive metal." *EX1004* at 6:6-9, 6:25-27, 13:30-34. As shown, through vias 110 are *vertically* through the interposer 105. A first through via 100 (*first metal plug*) is shown below in FIG. 3.

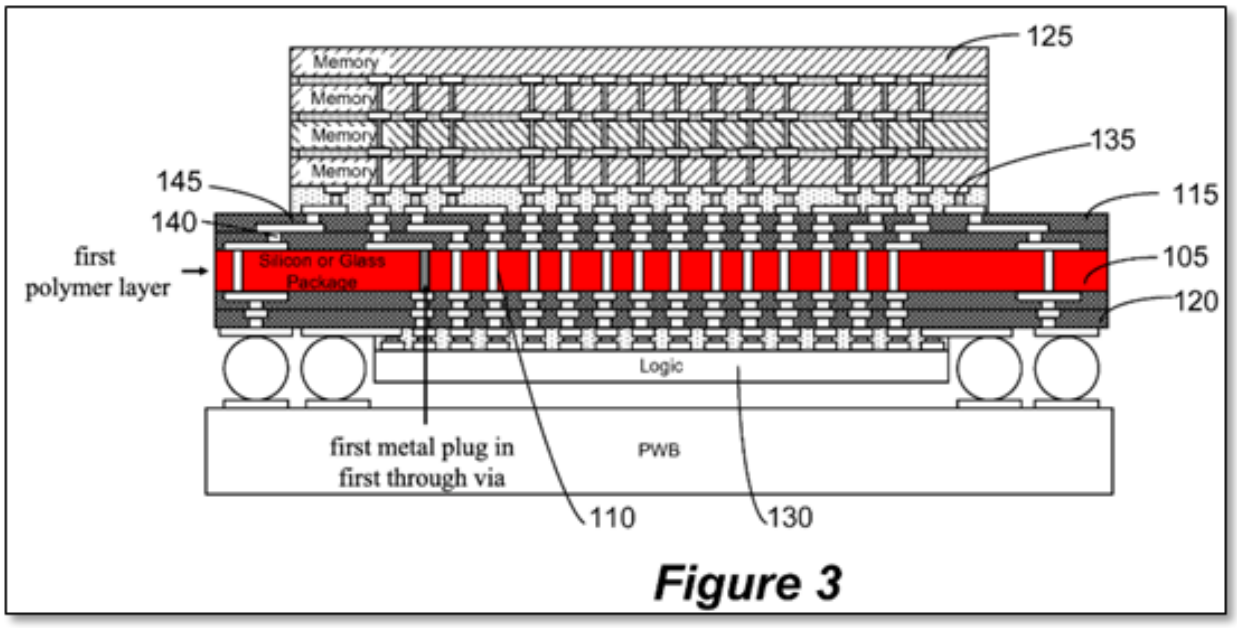


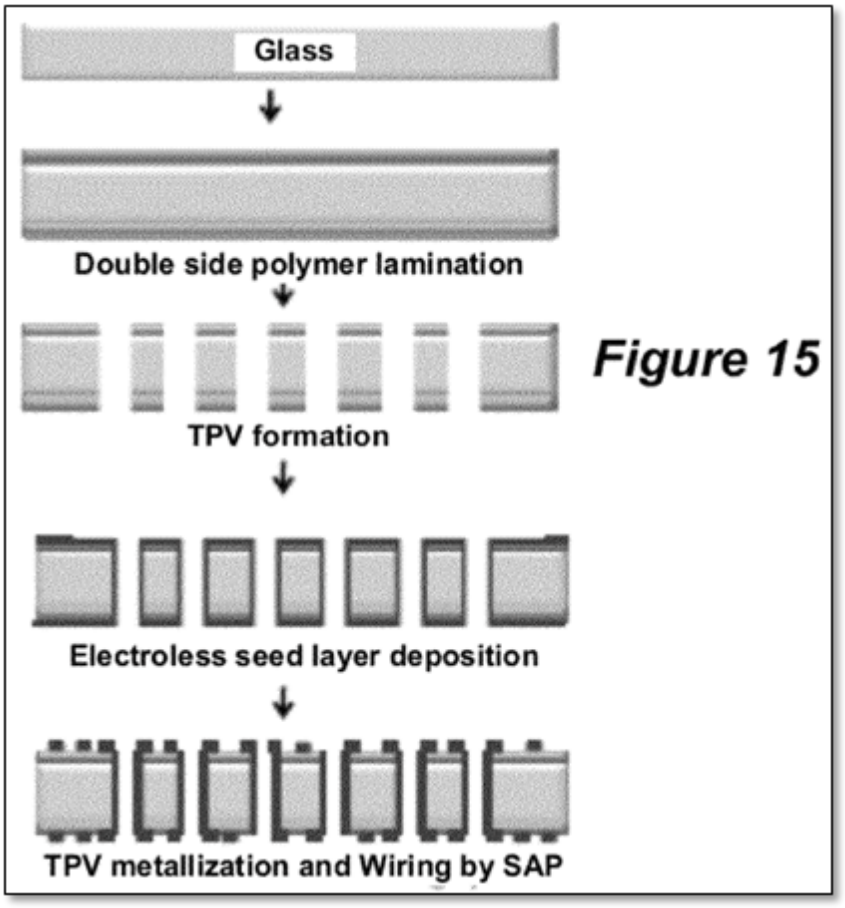
Figure 3

EX1004 at FIG. 3.

7. 1(b)(i): "wherein said first metal plug comprises a first copper layer, wherein the first copper layer contacts with a sidewall of said first through via;"

145. Sundaram teaches the "through vias 110 can be metalized with a highly-conductive metal, for example copper." *EX1004* at 6:25-27. Because the through vias 110 are metalized with copper, through vias 110 comprise a *first copper layer contacting a sidewall* (i.e., sidewall of through via 110 provided by interposer 105) *of one of said plurality of through vias*. In other words, because through vias 110 are metalized with copper, the copper portion *contact[s] a sidewall* of through via 110, because the metallization process deposits copper onto the portion of interposer 105 providing the *sidewall*.

146. For example, as shown in FIGS. 15 and 34, a *first copper layer* is formed on the through vias, for example by "TPV metallization" in FIG. 15 and the "seed repair (Cu electroless)" and "TSV filling" in FIG. 34. *See also EX1004* at 10:26-28 ("Metallization of TPVs…was carried out using copper as metal SAP (semi additive plating) approach.").



EX1004 at FIG. 15.

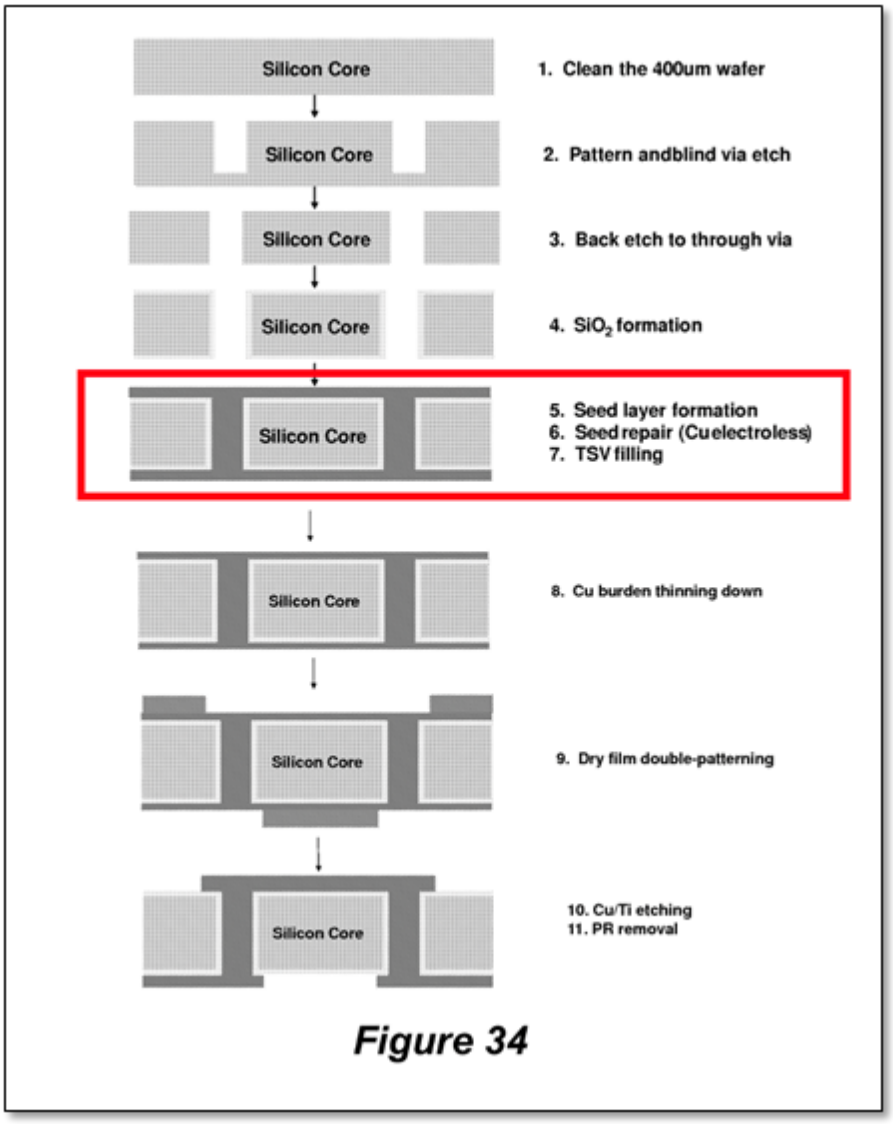


Figure 34

EX1004 at FIG. 34.

8. 1(c): "a second metal plug vertically in a second through via in said first polymer layer,"

147. For the same reasons discussed above at Claim 1(b), a second of Sundaram's through vias 110, shown below, is *a second metal plug vertically in a second through via in said first polymer layer*. *See* ¶ 144.

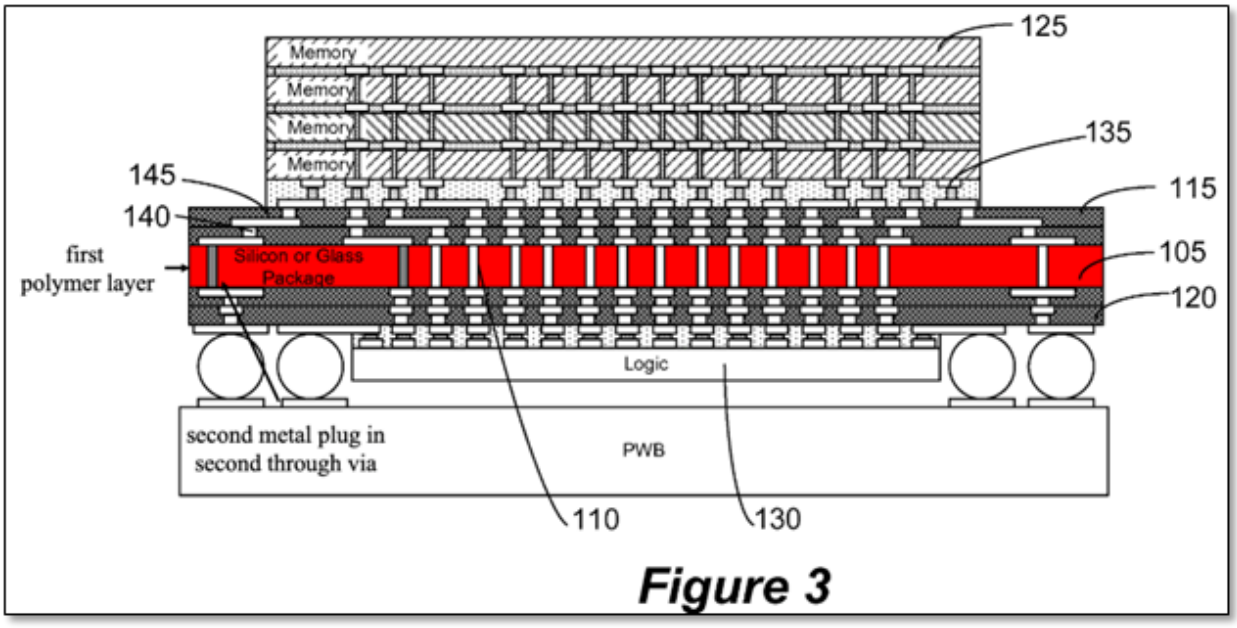


Figure 3

EX1004 at FIG. 3.

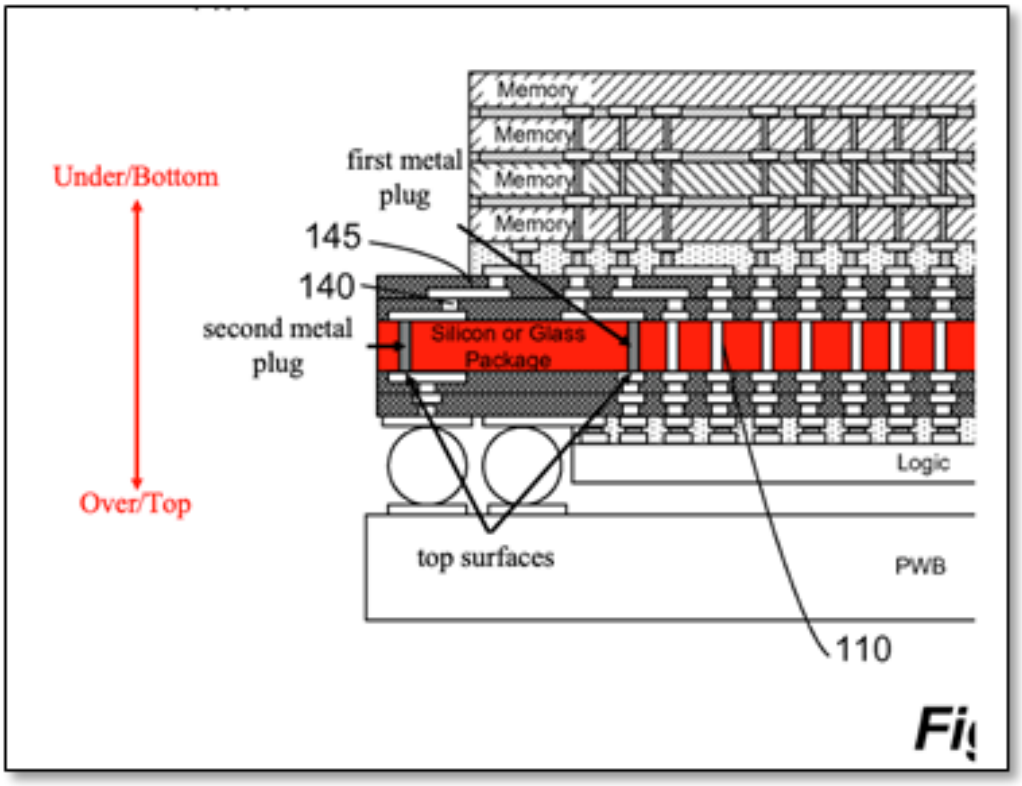
9. 1(c)(i): "wherein said second metal plug comprises a second copper layer,"

148. For the same reasons discussed above a claim 1(b)(i), the *second metal plug comprises a second copper layer*. *See* ¶¶ 145-146.

10. 1(c)(ii): "wherein a top surface of said second metal plug and a top surface of said first metal plug are in the same horizontal plane;"

149. As discussed, Sundaram teaches the "each of the through vias 110" (*first* and *second copper plug[s]*) "extends from the first side 115 to the second side 120 of interposer 105[,]" meaning that each of the through vias 110 have end surfaces *in the same horizontal plane*. *See* ¶ 144; *EX1004* at 6:6-9. The mapped surfaces would be "top" surfaces when the figure is rotated upside down, as the "over" direction is downward as shown in FIG. 3. Thus, as shown below, Sundaram

teaches *wherein a top surface of said second copper plug and a top surface of said first copper plug are in the same horizontal plane.*



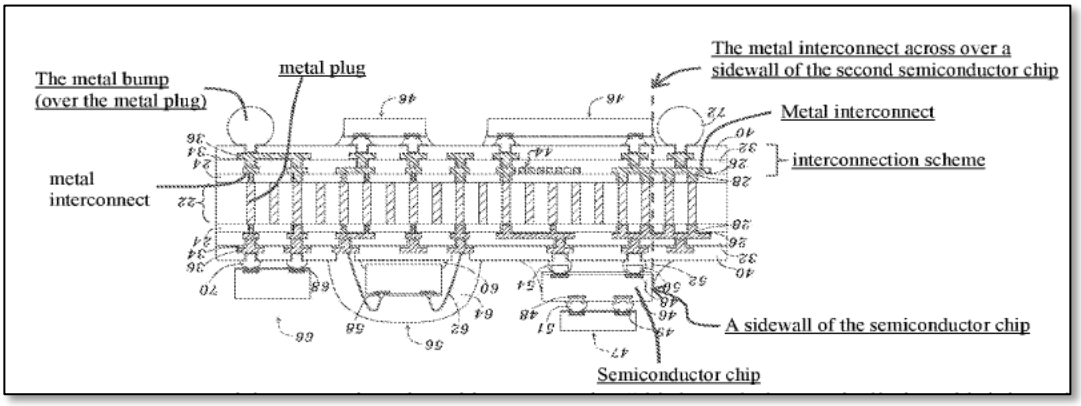
EX1004 at FIG. 3 (excerpt).

11. 1(d): "a first interconnection scheme over said first surface,"

150. I note that various limitations of the Challenged Claims require claim elements to be *over* or *under* with respect to other claim elements. For clarity of mapping, I annotate Sundaram's figures where appropriate indicating the *over* and *under* directions, where *over* is towards the PWB and *under* is away the PWB.

151. I note that the Patent Owner similarly used inverted figures during prosecution of related USPN 11,107,768 to explain the *over*/*under* relationship

between various claim elements. For example, Patent Owner provided an annotated version of FIG. 9x inverted during prosecution as support for "a first metal bump over said first interconnection scheme and said second metal plug[.]" *EX1002* at pp. 537-538, *see also EX1002* at pp. 395-400.



EX1002 at p. 537.

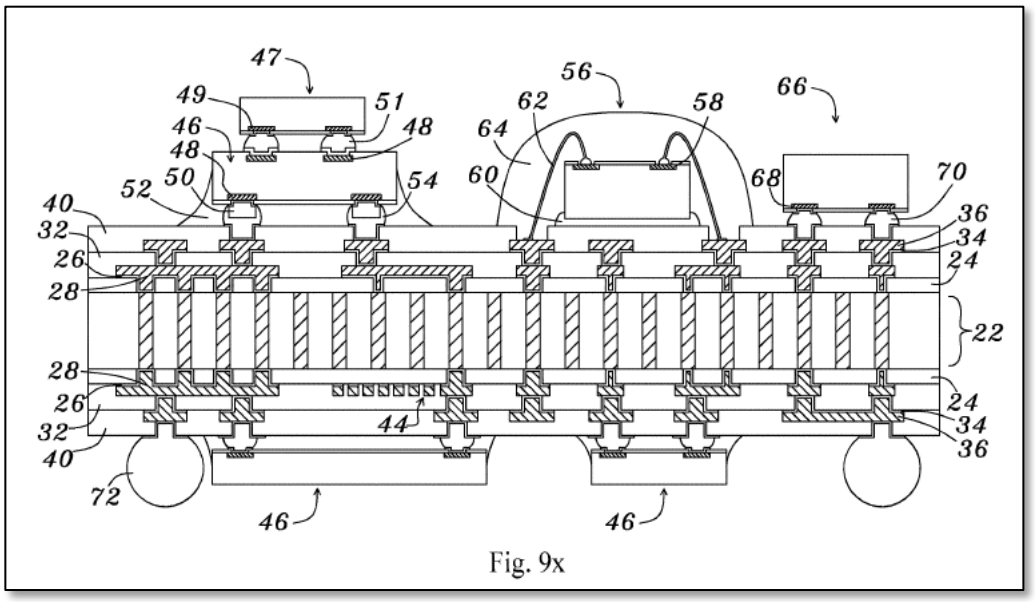


Fig. 9x

EX1001 at FIG. 9x.

152. Illustrated below, Sundaram teaches that "electronic devices having different I/O pad layouts and sizes can also be connected through the use of blind vias 140 and conductor traces 145 defined within **polymer-metal redistribution layers** deposited on the first side 115 and second side 120 of the interposer 105." *EX1004* at 6:62-67. Additionally, Sundaram teaches "die pads 135 that are formed on the first 115 and second sides 120 of interposer 105 can electrically connect devices[.]" *EX1004* at 6:29-31. Per Sundaram, "metallization provides die pad surfaces 135" such that the die pads 135 are *metal*. *EX1004* at 6:22-24. Because the blind vias 140 and conductor traces 145 within polymer-metal redistribution layers connect "electronic devices having different I/O pad layouts and sizes[,]" and because the die pads 135 formed on the second side 120 "electrically connect devices[,]" the vias 140, conductor traces 145, die pads 135, and polymer layer in the "polymer-metal redistribution layer" on second side 120 (*first surface*) are a *first interconnection scheme over said first surface*. In other words, because vias 140 and traces 145 in the polymer layer and die pads 135 connect (i.e., *interconnect[]*) devices 125 and 130, they collectively form an *interconnection scheme*.

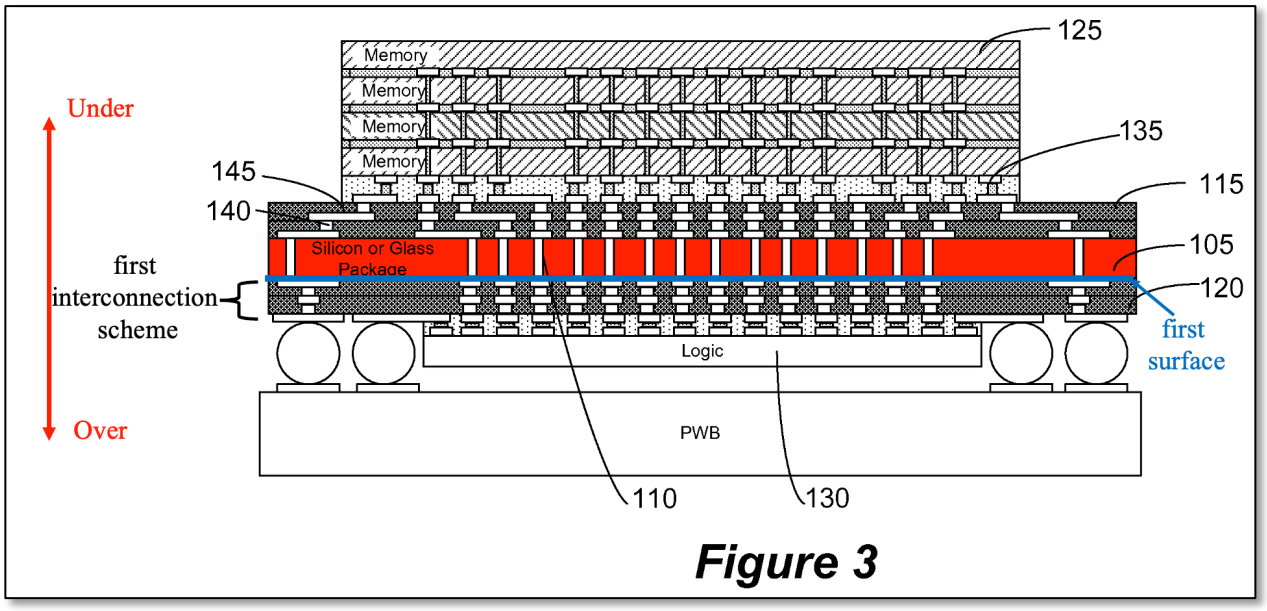


Figure 3

EX1004 at FIG. 3.

12. 1(d)(i): "wherein said first interconnection scheme comprises a first metal interconnect over said first surface, a second metal interconnect over said first surface, a third metal interconnect over said first surface and a second polymer layer over said first, second and third metal interconnects"

153. Because Sundaram teaches that "[m]etallization…on the surface of glass interposer" is done by "using copper as metal and SAP (semi additive plating approach)[,]" a POSITA would understand the blind vias 140 and conductive traces 145 to be the "metal" in the "polymer-metal redistribution layers[.]" *EX1004* at 10:26-28, 9:63-65, FIG. 15, 6:62-67. Semi additive plating was a well-known technique used within a sequential build up (SBU) process flow to form circuitry in chip packages:

> "Circuitry is formed in a **semi-additive** process. The entire polymer surface, both dielectric and via hole walls, is seeded with a conductive

> material in a process derived from conventional circuit board processing, and a thin layer of electroless copper is deposited. A photoresist layer is deposited, patterned, and etched to expose the electroless copper and via holes in the desired circuit pattern. **Electroplated copper is added to the desired finished metal thickness**. Finally, the sacrificial dielectric layer is entirely removed, initial seed metal is stripped, and the SBU substrate is ready for the addition of the next layer pair. The process is repeated for the desired number of layers."

EX1035 at p. 643.

154. Thus, because the blind vias 140 and conductive traces 145 are *metal* and because they connect "electronic devices having different I/O pad layouts and sizes[,]" blind vias 140 and conductive traces 145 are *metal interconnects* of the *first interconnection scheme*. *EX1004* at 6:62-65, 7:4-8. A *first metal interconnect* comprising a trace 145 (longer rectangles in FIG. 3) and a via 140 (shorter rectangles), a *second metal interconnect* comprising another trace 145 and via 140, and a *third metal interconnect* comprising another trace 145 and via 140 in Sundaram's RDL is shown below, along with a *second polymer layer* that is *over said first, second, and third metal interconnects* (the "polymer" of the "polymer-metal redistribution layers."). *EX1004* at 6:62-67. The *second polymer layer* at least includes the below green highlighted layer but may include an additional portion of the RDL (*see* Claim 11, ¶ 238).

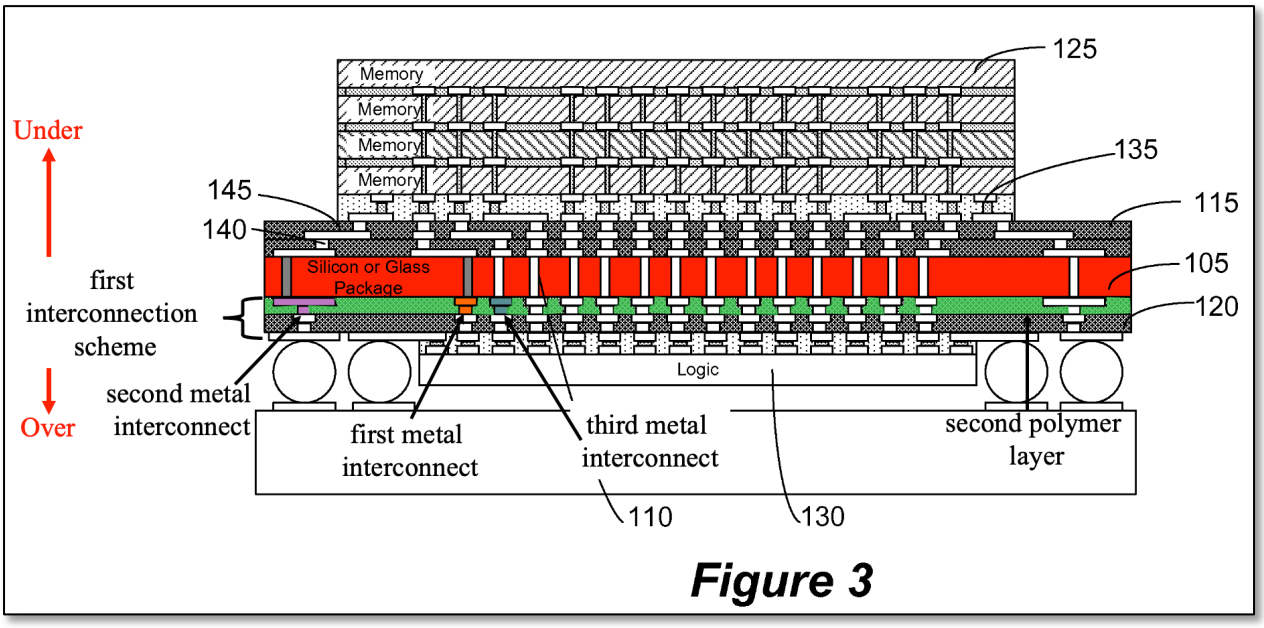


Figure 3

EX1004 at FIG. 3.

155. Alternatively, Sundaram's outermost layer of the RDL is *a second polymer layer* and is *over* the *first/second/third metal interconnects*.

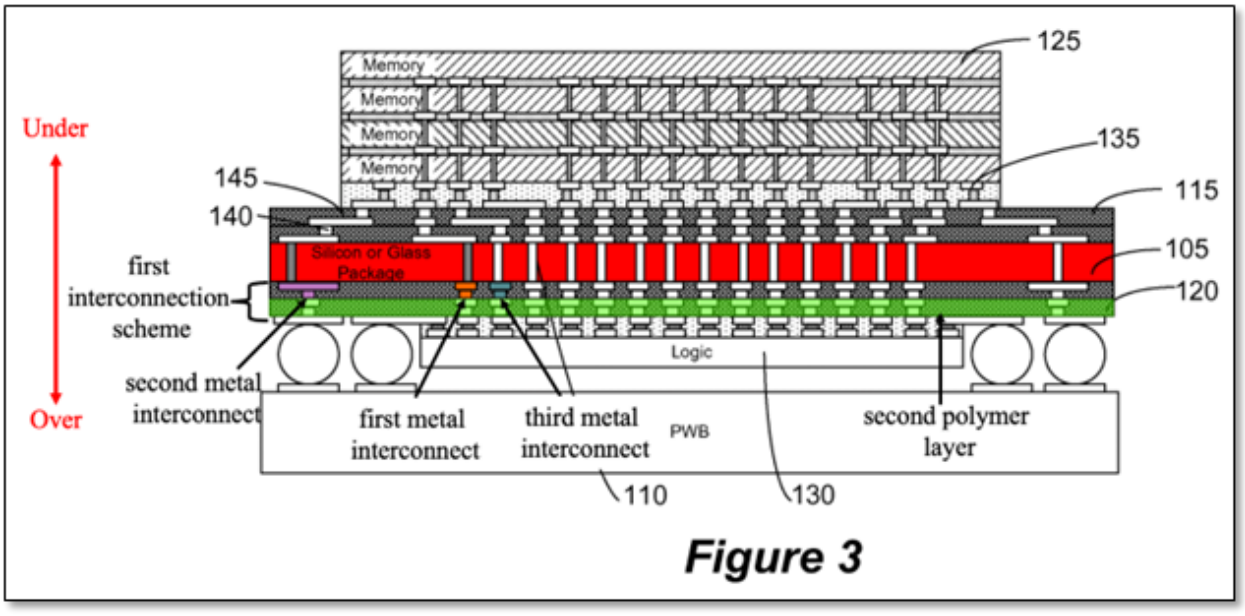
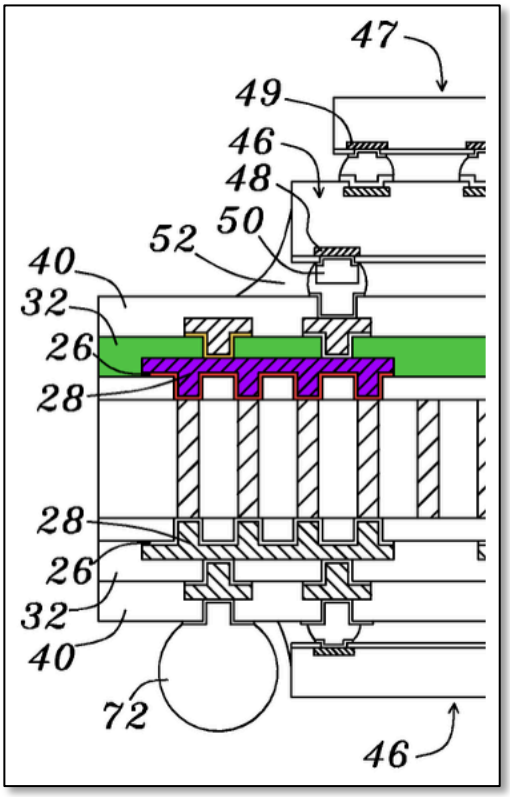


Figure 3

EX1004 at FIG. 3.

156. I note that Sundaram's teaching of the polymer as being over each of the first, second, and third metal interconnect[s] is consistent with what is described by the '768 Patent. Specifically, during prosecution of the '768 Patent, Patent Owner expressly pointed to dielectric layer 72 as being the second polymer layer. *EX1002* at 397.



EX1001 at FIG. 9X (excerpt).

157. As can be seen in the above figure, dielectric layer 32 (the second polymer layer, according to the Patent Owner) is "over" metal layers 26, 28 and partially over metal layer 34, of the metal interconnect. As such, Sundaram's second

polymer layer is over each of the first, second, and third metal interconnect[s] in at least the same way as described by the '768 Patent.

13. 1(d)(ii): "wherein said first metal interconnect is connected to said first metal plug, wherein said second metal interconnect is connected to said second metal plug,"

158. Sundaram teaches the "first electronic device 125 is of a different pad size and configuration then the second electronic device 130, and they are connected with through vias 110, blind vias 140, and conductor traces 145." *EX1004* at 7:4-8. Because devices 125, 130 are connected by blind vias 140, traces 145, and through vias 110, the traces 145 and vias 140 on either side of interposer 105 are connected by vias 110. Thus, as shown below, the *first metal interconnect is connected to said first copper plug* and the *second metal interconnect is connected to said second copper plug*.

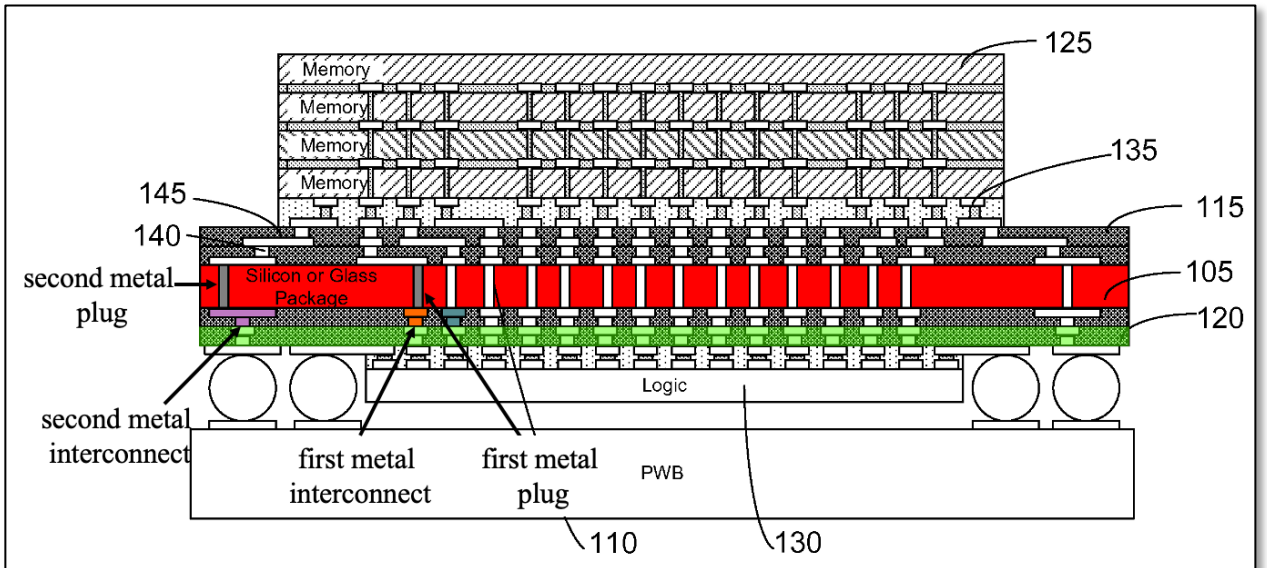


Figure 3

EX1004 at FIG. 3.

14. 1(d)(iii): "wherein said first metal interconnect comprises a first metal layer, a third copper layer on said first metal layer, and a fourth copper layer on said third copper layer"

a) Sundaram's Teachings

159. Sundaram teaches the *first metal interconnect*. *See* ¶¶ 153-154.

b) Lin-191's Teachings

160. Lin-191 teaches an interconnection scheme comprising metal interconnects (patterned metal layers 3). Each of Lin-191's patterned metal layers 3 are a *metal interconnect* because, as I show below, they comprise multiple metal layers and function to connect a semiconductor chip to other structures in Lin-191's multi-chip module. Specifically, Lin-191 teaches that "[e]ach of chips 130 may have one of the metal traces or pads 46 connected to multiple of the metal traces or pads 26 in one or more of the chips 120 through, in sequence,…the patterned metal layer 3[.]" *EX1005* at [0214]. Additionally, Thus, each of Lin-191's patterned metal layers 3 are an *interconnect* at least because they connect chips 130 to chips 120.

161. Lin-191 provides additional specificity to the structure of patterned metal layers 3. Each of patterned metal layers 3 comprises an "adhesion layer 31…formed on the top surfaces 85a of the filling or encapsulating layer 85a[.]" *EX1005* at [0127]. Patterned metal layer 3 further includes a "seed layer 32[,]" and Lin-191 teaches that "when adhesion layer 31 is formed by sputtering a nickel-

containing layer, such as a single layer of nickel…the seed layer 32 can be formed by sputtering a copper layer…on the nickel containing layer." *EX1005* at [0132]. Finally, patterned metal layers 3 comprise "metal layer 33…on the seed layer 32" where "metal layer 33 can be a single layer of copper." *EX1005* at [0133]. Because Lin-191's patterned metal layers 3 include (1) a nickel adhesion layer 31, (2) a copper seed layer 32, and (3) a copper metal layer 33, Lin-191 therefore teaches a metal interconnect comprising *a first metal layer, a third copper layer on said first metal layer, and a fourth copper layer on said third copper layer*, as shown below.

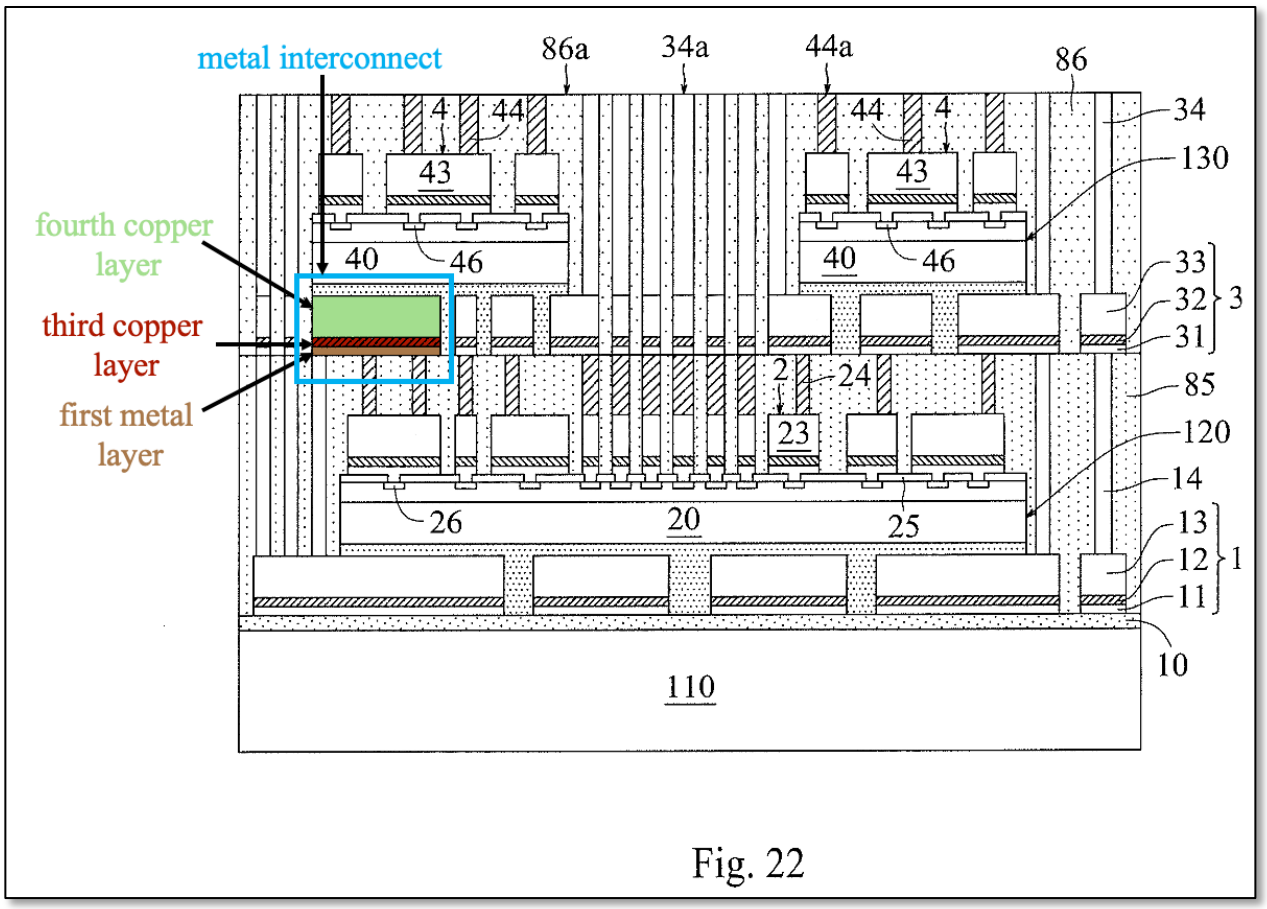


Fig. 22

EX1005 at FIG. 22.

c) Motivation to Combine

162. Based on Lin-191, a POSITA would have found it obvious and been motivated to apply Lin-191's teachings of multiple interconnect layers formed from *metal* and *copper* to Sundaram's *first metal interconnect*, which likewise includes conductor traces 145. *See EX1004* at 6:62-67. A POSITA would have motivated to use such a multi-layer interconnect to leverage the advantages of different materials. For example, Lin-191's nickel adhesion layer 31 would have prevented diffusion of copper into adjacent interconnects, as nickel was known to resist copper diffusion. *EX1040* at Abstract ("The structure comprises a layer of barrier metal, preferably nickel, that resists copper diffusion."). Diffusion of copper out of the interconnects would compromise the mechanical integrity of such copper interconnects, thereby increasing the risk of delamination. Thus, by providing a nickel adhesion layer, the likelihood of delamination is minimized.

163. A POSITA would have also been motivated to include the copper seed layer 32 due to the well-known advantages of seed layers for subsequent electroplating of thicker copper layers (i.e., seed layer 32 provides advantages for the copper metal layer 33 manufacturing process). Specifically, seed layers were known to act as an electrode during the electroplating process, allowing for uniform, void-free electroplated metal to be formed thereon. *EX1104* at 2:46-48 ("The copper seed layer provides an electrode for the subsequent copper electroplating…").

Indeed, it was known that a "missing seed layer" may "lead to a void in the electroplated metal" resulting in an "increase in their resistance and result in poor reliability." *EX1063* at 3:12-16. Accordingly, a POSITA would have been motivated to incorporate Lin-191's copper seed layer into the multi-layer interconnect, to thereby leverage the myriad of other benefits provided by the copper metal layer 33.

164. A POSITA would have been motivated to utilize the *fourth copper layer* (e.g., copper metal layer 33) due to coppers' well-known relatively low electrical resistivity and electromigration resistance. It was known that "as the size and cross-sectional dimensions of electrical interconnects get smaller, resistance increases and electromigration increases. Increased resistance and electromigration are undesirable for a number of reasons. For example, "increased resistance may reduce device drive current, and source/drain current through the device, and may also adversely affect the overall speed and operation of the transistor." *EX1054* at 1:39-46. Copper has a lower resistivity (1.73×10^{-6} ohm-cm at 20°C) compared to other materials, such as aluminum (2.824×10^{-6} ohm-cm at 20°C), as well as a "high immunity to electromigration, high ductility, and high melting point[,]" making it a desirable choice for interconnect material in high-density packaging. *EX1054* at 2:2-14.

165. Indeed, because copper has a relatively low electromigration rate, the likelihood of failures at elevated current densities is reduced. Specifically, it was

known that "high current densities lead to electromigration-caused failures" in integrated circuits. *EX1055* at 1:30-32. Accordingly, a POSITA would have been motivated to choose a material, such as copper due to its lower resistivity, to reduce the risk of "electromigration-caused failures." *EX1055* at 1:30-32. Similarly, because the resistivity of copper is relatively low, the electrical conductivity is relatively high compared to other materials (e.g., aluminum). *EX1056* at [0152] ("In addition, since the electrical conductivity of copper is higher than that of aluminum…"). It was known that in "fabricating semiconductor components, interconnects having a high electrical conductivity…provide the best performance for a signal transmission system." *EX1057* at 1:29-33.

166. Additionally, copper offers superior mechanical reliability and thermal performance compared to alternatives. For example, compared to alternatives (e.g., aluminum), copper was known to have a closer CTE to that of silicon, specifically, the "difference in the coefficient of thermal expansion [] between aluminum (Al) and silicon (Si) is…about 1.46 times larger than the difference in coefficient of thermal expansion [] between copper and silicon. The difference in the coefficient of thermal expansion is the dominant source of strain in a metallic interconnect." *EX1054* at 6:67–7:7. Accordingly, a POSITA would recognize that the use of copper, compared to alternatives such as aluminum, in Sundaram's *first metal interconnect* would advantageously minimize the impact that the difference in CTE

between the *first metal interconnect* and device 130 would have on the mechanical integrity of the *first metal interconnect*.

167. Further, copper was known to have to a high thermal conductivity and, correspondingly, "good heat dissipation characteristic[s]." *EX1106* at 7:51-53. As I described above, enhanced heat dissipation would mitigate processing speed reductions, thereby further incentivizing the use of copper for forming metal interconnects. *See, e.g., EX1082* at 1:40-44 ("For instance, a reduction in the operating temperature of a device such as a typical silicon semiconductor can correspond to an increase in the processing speed, reliability and life expectancy of the device.").

168. Further still, a POSITA would have recognized the use of copper in multi-layer metal interconnects was a well-established industry practice before the '768 Patent. Indeed, it was known that "copper (and its alloys) is becoming the interconnect material of choice" due to the above described advantages as well as the fact that copper "can be deposited at lower temperatures (thereby avoiding deleterious effects on other elements of the integrated circuit) in smaller openings." *EX1107* at 2:20-30. The "lower resistance of copper reduces signal propagation time within the interconnect structures." *EX1107* at 2:30-32. As such, a POSITA would have found it advantageous to apply Lin-191's teaching of copper conductive layers into Sundaram's RDL to enhance electrical performance and process compatibility.

Given the fact that copper was a well-known material for forming metal interconnects with known advantages (described above), the application of Lin-191's copper layers into Sundaram's *first metal interconnect* would have been a straightforward design choice for a POSITA seeking to increase electrical and thermal performance.

169. The combination is the application of a known technique (Lin-191's metal interconnect layers) into a known device (Sundaram's chip package) ready for improvement to yield predictable results, i.e., the predictable result of Sundaram's *first metal interconnect* having metal/copper. The application of Lin-191's teachings would have improved Sundaram's chip package for the reasons set forth above and yielded predictable results at least because copper's use as an interconnect layer material was industry standard. *EX1108* at 2:5-6 ("Copper has become commonly used for some interconnects 311 in integrated circuits, replacing aluminum."); *EX1109* at 1:12-15 ("Copper has become the metal of choice over aluminum in the fabrication of integrated circuits because it has a lower resistance than aluminum and allows for the scaling down of devices."). As such, a POSITA would have been familiar with fabricating metallic interconnects, such as copper traces and vias.

170. The combination would have had a reasonable expectation of success at least because the use of copper in vias, traces, and pads was well established by the time of the '768 Patent, and the techniques for forming such copper

interconnects, such as sputtering an electroplating as taught by Lin-191, were also well known. *EX1005* at [0132], [0134]; *EX1042* at ("…filled with copper typically by an electroplating process, as known to one of ordinary skill in the art of integrated circuit fabrication."); *EX1043* at [0032] ("…variety of different deposition methods known by one of ordinary skill in the art, including but not limited to, CVD, pulsed CVD, PECVD, ALD, PEALD, or sputtering methods."). Further, evidenced by the ubiquitous use of copper in the semiconductor industry for interconnect applications, a POSITA would have had a reasonable expectation of success in applying Lin-191's teachings of a metal/copper interconnect to Haba's traces 30/vias 36. *See, e.g., EX1110* at [0008] ("Metal layers include patterns of conductive material (usually copper)…"); *EX1111* at [0005] ("Today, many integrated circuit chips use copper as the interconnection metal."); *EX1112* at 1:39-41 ("The use of copper has increased in recent years for forming conductive interconnections between individual devices and circuits of chips…". Because the use of copper (1) involves routine manufacturing processes, such as sputtering and electroplating and, (2) leverages a well-known and widely adopted electrically conductive material, a POSITA would have viewed the modification as routine and easily implementable without undue experimentation, leading to a reasonable expectation of success.

15. 1(e): "a first metal bump over said first interconnection scheme and said second metal plug,"

171. Sundaram teaches that "die pads 135 formed on the first 115 and second sides 120 of the interposer 105 can electrically connect devices using…**copper bumps** with solder caps[.]" *EX1004* at 6:29-31. An example of one of Sundaram's copper bumps with solder caps is shown below, which is a *first metal bump* (i.e., because it's made of copper) *over said first interconnection scheme and said second metal plug*.

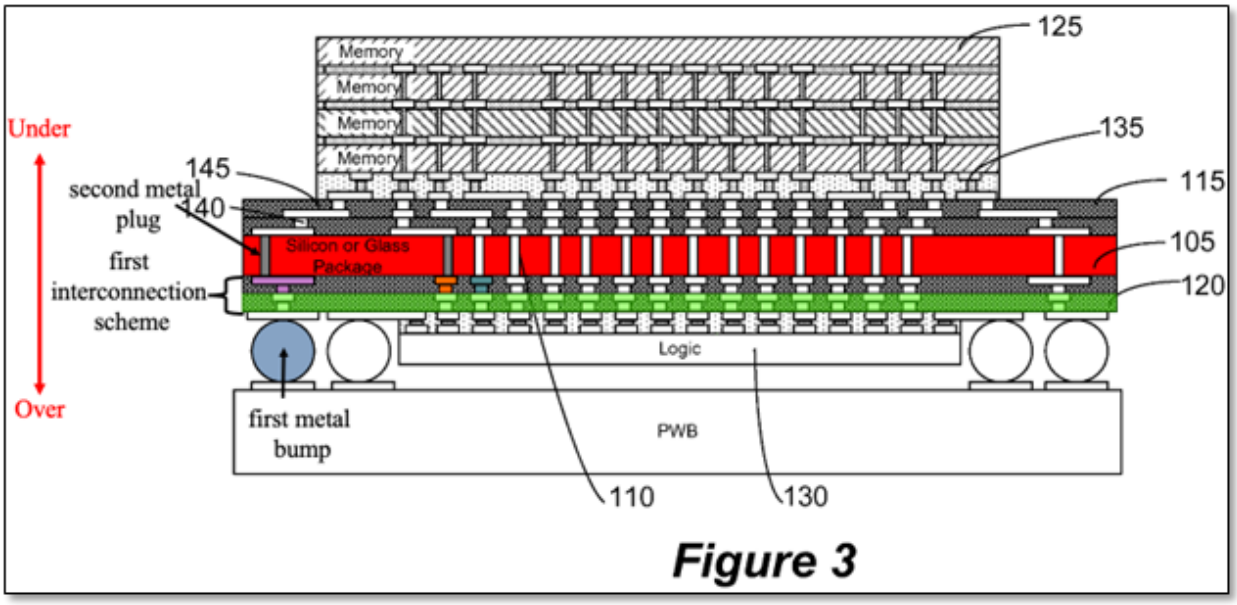


Figure 3

EX1004 at FIG. 3.

16. 1(e)(i): "wherein said first metal bump comprises a tin-containing layer; and"

a) Sundaram's Teachings

172. As discussed above, Sundaram's *first metal bump* is a "copper bump[s] with [] solder cap[]." *EX1004* at 6:29-31. A POSITA would have understood the "solder cap" to be a *tin-containing layer* because "traditional solders are…most

commonly a **tin**-lead alloy (Sn-37% Pb) having about 37% lead in a **tin** base material." *EX1094* at [0003]. Additionally, Sn-based solders were dominant in commercial packages such as those taught by Sundaram. Thus, the context of the chip packages of Sundaram means that "solder" necessarily includes Sn-content, thereby teaching the *tin-containing layer*. A POSITA would have understood Sundaram's disclosure of "solder" to mean the solder contains tin unless stated otherwise. That is, if someone refers to non-tin-containing solder, it would be specified as such because the "default" solder contains tin.

b) Lin-191's Teachings

173. Additionally to Sundaram, Lin-191 teaches a bump with the claimed *tin-containing layer*. Specifically, Lin-191 teaches a system-in-package including "solder bumps or balls 29a" formed by reflowing a "solder layer 29," which is "a single metal layer formed by electroplating… a tin-containing layer." *EX1005* at [0320], [0314]. "For example, the solder layer 29 can be a single metal layer formed by electroplating…a tin-containing layer of a tin-lead alloy, a tin-silver alloy, a tin-silver-copper alloy, or a tin-gold alloy[.]" *EX1005* at [0321].

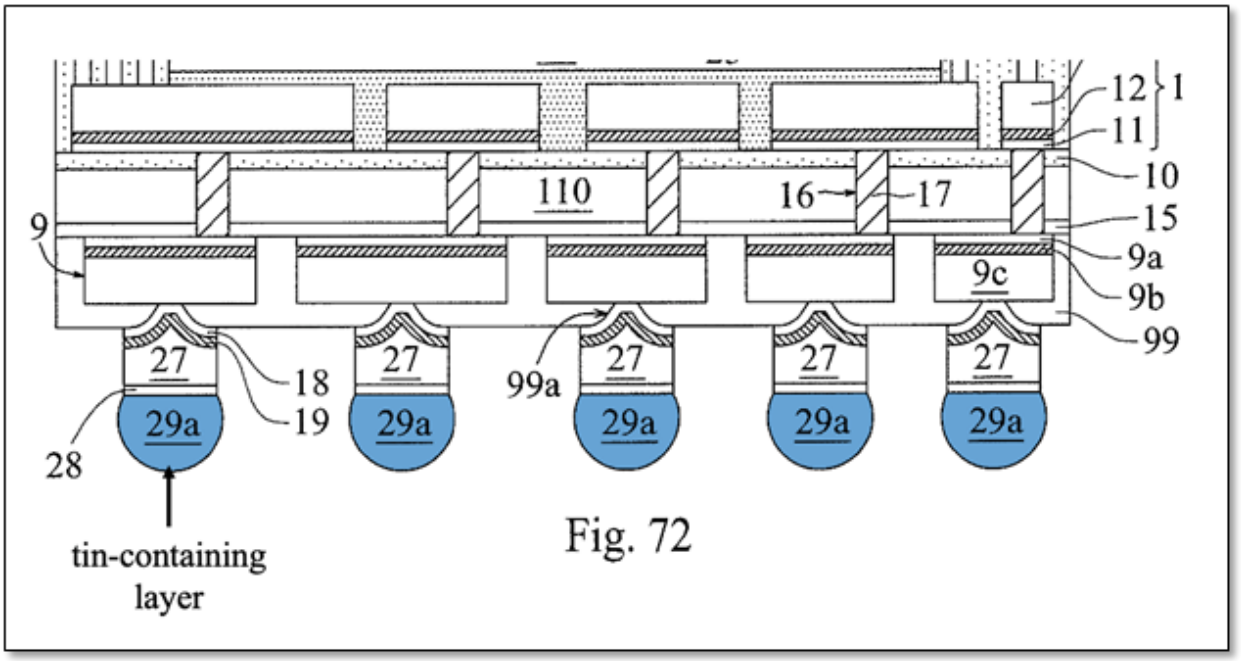


Fig. 72

EX1005 at FIG. 72 (excerpt).

174. Thus, Lin-191's solder layer 29 teaches a metal bump compris[ing] a *tin-containing layer* (solder layer 29).

c) Motivation to Combine

175. A POSITA would have been motivated and found it obvious to apply Lin-191's teachings of a solder bump having a *tin-containing layer* to Sundaram's *first metal bump*. As discussed, Sundaram teaches traditional solder that a POSITA would have understood to contain tin and Lin-191 further discloses a solder layer that is a *tin-containing layer*, further motivating the combination. Lin-191's solder bump or ball 29a would have predictably improved the mechanical connection of Sundaram's first metal bump to die pad 135.

176. Specifically, a POSITA would have appreciated the advantage of a *tin-containing layer*, as tin was known to "wet and spread on a wide range of substrates[,]" which a POSITA would have considered desirable as wettability was an important factor for forming various types of interconnects. *EX1098* at p. 104. Additionally, tin used in limited thickness was known to form IMCs with metals used in electronic assemblies, thereby achieving "good bonding." *EX1099* at p. 20. Tin-containing solder was further known to be advantageous due to tin's "relatively low melting point" which would allow for solder reflow to occur without damaging other components of the chip package unable to withstand high temperatures. *EX1134* at [0026]. Further, "[a]nother advantage is the existence of substantial experience and database in the use of tin solders compiled over a long history." *EX1099* at p. 20. Thus, Lin-191's solder bump or ball 29a having a *tin-containing layer* would have predictably improved the mechanical connection of Sundaram's *first metal bump* to die pad 135 by achieving "good bonding[,]"would have provided the benefit of a low melting point, and would have been a straightforward material choice given the substantial amount of data generated by extensive use. *EX1099* at p. 20.

177. The Sundaram–Lin-191 combination is merely the application of a known technique (a tin-containing solder bump) to a known device (Sundaram's

bump), yielding the predictable result of Sundaram's first metal bump comprising a tin-containing solder layer.

178. Alternatively, substituting Sundaram's solder cap with Lin-191's tin-containing solder bump would have yielded predictable results at least because both serve the same function of connecting interconnects to a PWB/PCB. *See EX1005* at [0324]; *EX1004* at FIG. 3.

179. A POSITA would have had a reasonable expectation of success in combining these teachings because solder bump technology, including the use of tin-based alloys, was well known in the art prior to the '768 Patent. *See* ¶¶ 64-69. Further, methods of forming metal bumps using tin were well known. *See* ¶¶ 71-76.

17. 1(f): "a first semiconductor chip under said first interconnection scheme,"

180. Sundaram teaches a "first electronic device 125" that "can be single or stacked memory IC devices" or "other electronic devices" such as "an image sensor chip." *EX1004* at 6:37-45, FIG. 3, FIG. 33. As shown, Sundaram's first electronic device 125 is a *first semiconductor chip under said first interconnection scheme*.

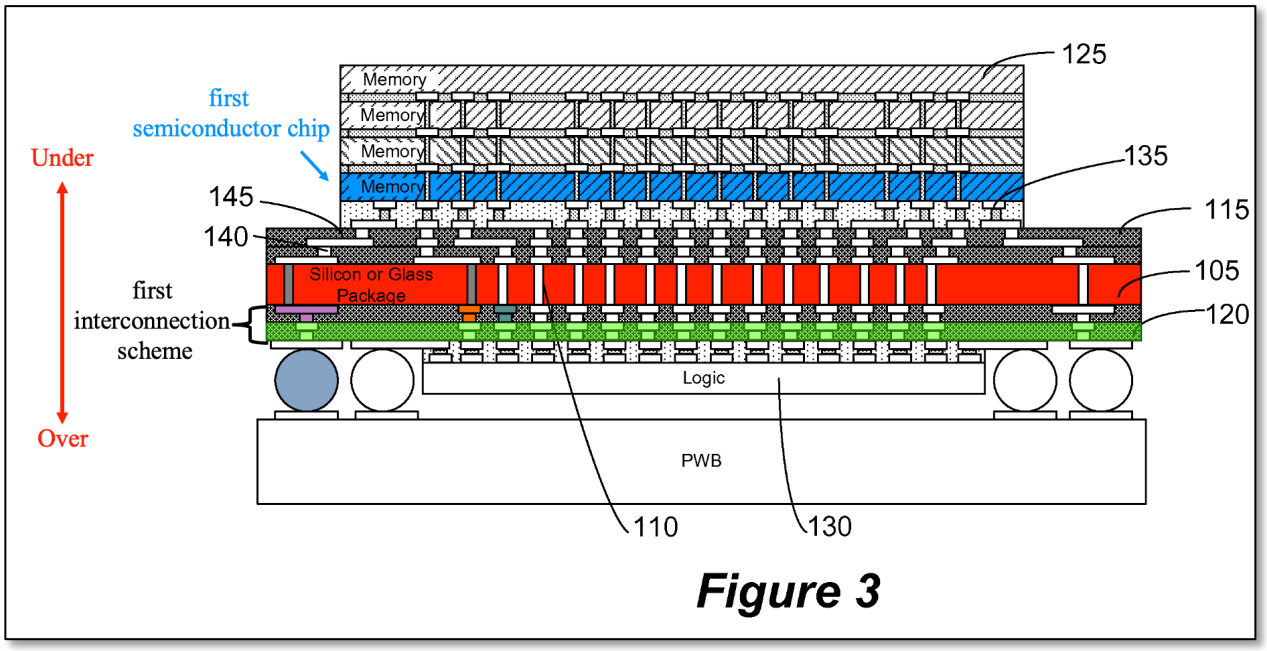


Figure 3

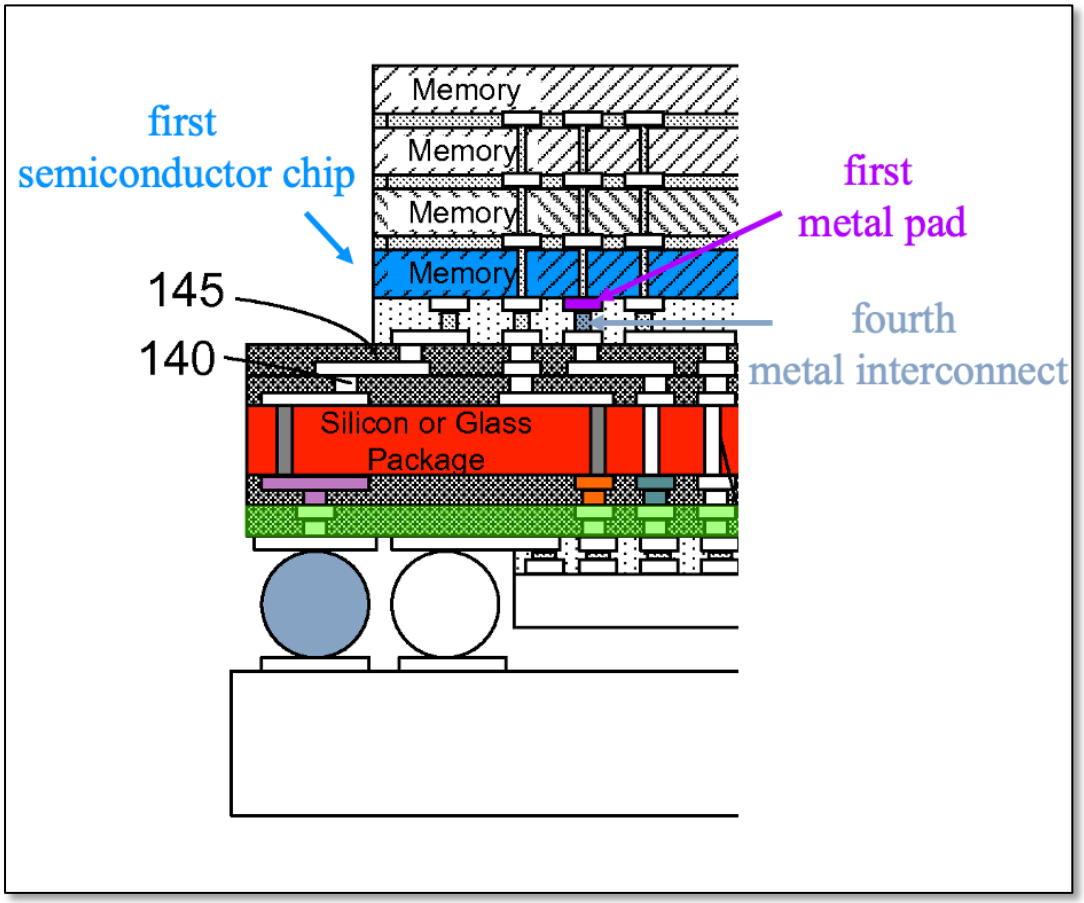
EX1004 at FIG. 3.

18. 1(f)(i): "wherein said first semiconductor chip comprises a fourth metal interconnect on a first metal pad of said first semiconductor chip,"

a) Sundaram's Teachings

181. Sundaram's interposer 105 has die pads 135 where "metallization provides die pad surfaces 135[.]" *EX1004* at 6:23-25. A POSITA would understand that like interposer 105, first electronic device 125 (*first semiconductor chip*) also has die *pad[s]* (one shown in purple below) such that an electrical connection is made between first electronic device 125 and interposer 105. Indeed, it was known that "I/O terminals were traditionally formed by way of metal pads along the periphery of an IC." *EX1095* at 1:24-25. Thus, a POSITA would understand the *pad* (purple) shown in FIG. 3 to be a *first metal pad*. Further, Sundaram teaches "die

pads 135…can electrically connect devices using solder, copper bumps with solder caps, copper to copper bonding," each of which teaches *a fourth metal interconnect* because they "electrically connect devices" and because they are made of *metal* i.e., solder, copper. *EX1004* at 6:29-33. In FIG. 3, below, the *fourth metal interconnect* is depicted as a bump on die pad 135.



EX1004 at FIG. 3.

182. Additionally, or alternatively, FIG. 32 is a "side-by-side configuration" of the interconnect structure, which includes a memory stack where each chip has a *metal pad* on both sides (i.e., top and bottom):

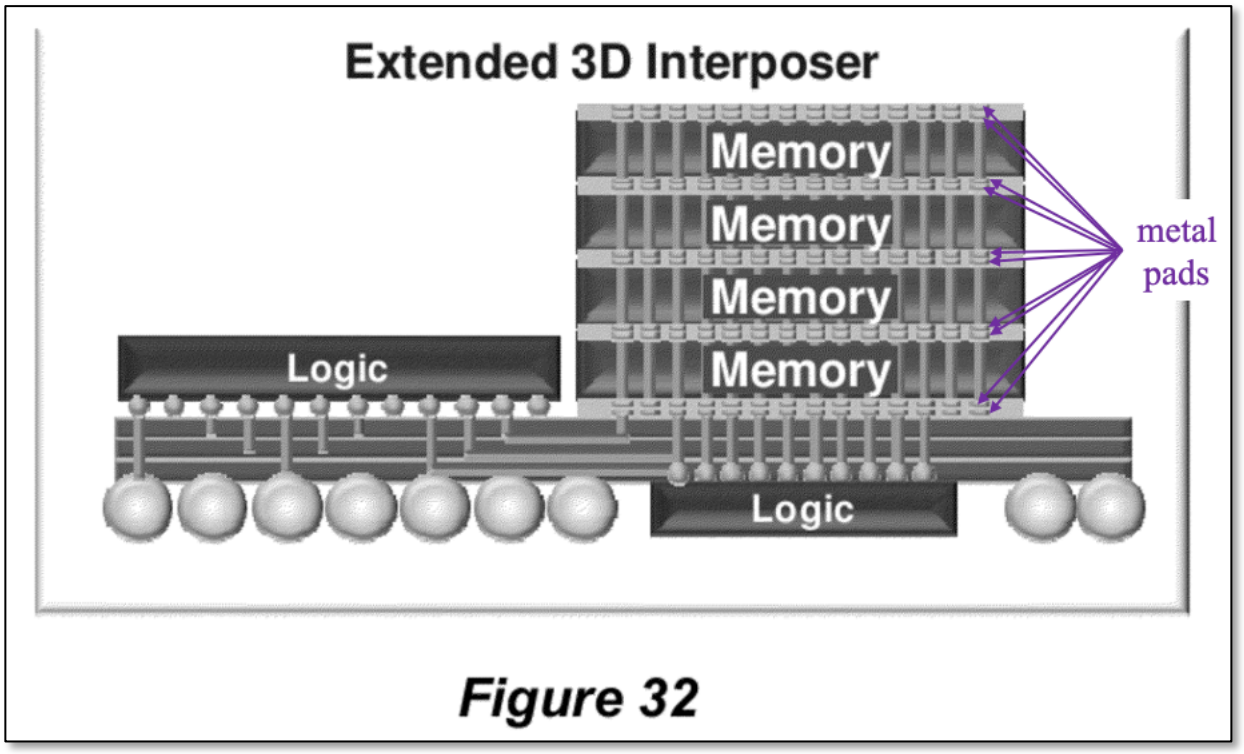
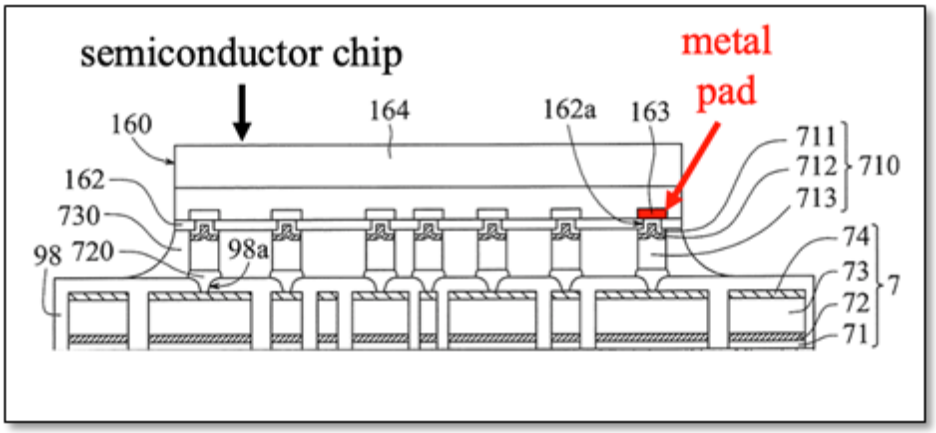


Figure 32

EX1004 at FIG. 32. *See* ¶¶ 184-185, for motivations to combine and reasonable expectation of success.

b) Lin-191's Metal Pad Teachings

183. Additional to Sundaram's teachings, Lin-191 teaches a *metal pad*. Depicted below, Lin-191 teaches a "semiconductor chip 160" comprising "multiple metal traces or pads 163." *EX1005* at [0383]. Lin-191's "metal traces or pads 163" are made of "aluminum" and are connected to "metal pillars or bumps 710[.]" *EX1005* at [0384]. Lin-191's semiconductor chip 160 thus comprises a *metal pad*.



EX1005 at FIG. 71 (excerpt).

c) Motivation to Combine

184. A POSITA would have been motivated and found it obvious to apply Lin-191's teachings of a *metal pad* to Sundaram's *first semiconductor chip*, thereby yielding the predictable result of Sundaram's *first semiconductor chip* (first electronic device 125) having a *metal pad*. Modifying Sundaram's pad to be metal, thereby yielding a *first metal pad*, is merely an implementation detail in Sundaram's overall system, i.e., Lin-191 provides the specificity of a semiconductor contact pad being *metal*. Given that metal contact pads were ubiquitous in semiconductor chips, a POSITA would have been motivated to turn to references teaching materials for contact pads (e.g., Lin-191) to ensure an electrical connection is made between Sundaram's first electronic device 125 and the bump (i.e., by a conductive *metal pad*). *See, e.g., EX1044* at 2:30-33 ("In FIG. 1, a **metal pad** 12 is formed on a semiconductor material 10. Metal pad 12 may be formed from a conductive

metal…") (emphasis added); *EX1045* at [0006] ("FIG. 1 illustrates a portion of flip chip 10 with a solder bump 12 formed on **metal contact pad** 14.") (emphasis added); *EX1046* at [0018] ("Bumps 105 electrically and possibly physically contact the I/O pads (**metal pads**) 103 of the IC chip 100."); *EX1095* at ("I/O terminals were **traditionally** formed by way of **metal pads** along the periphery of an IC.").

185. The combination is application of a known technique (metal pads) to a known device (Sundaram's semiconductor chip) ready for improvement to yield the predictable result of Sundaram's first electronic device 125 having a *first metal pad*, per Lin-191. *EX1005* at [0081]. As I described above, metal contact pads were ubiquitous, so a POSITA would have had a reasonable expectation of success in modifying Sundaram's first electronic device 125 to have *first metal pad*, such as aluminum, per Lin-191.

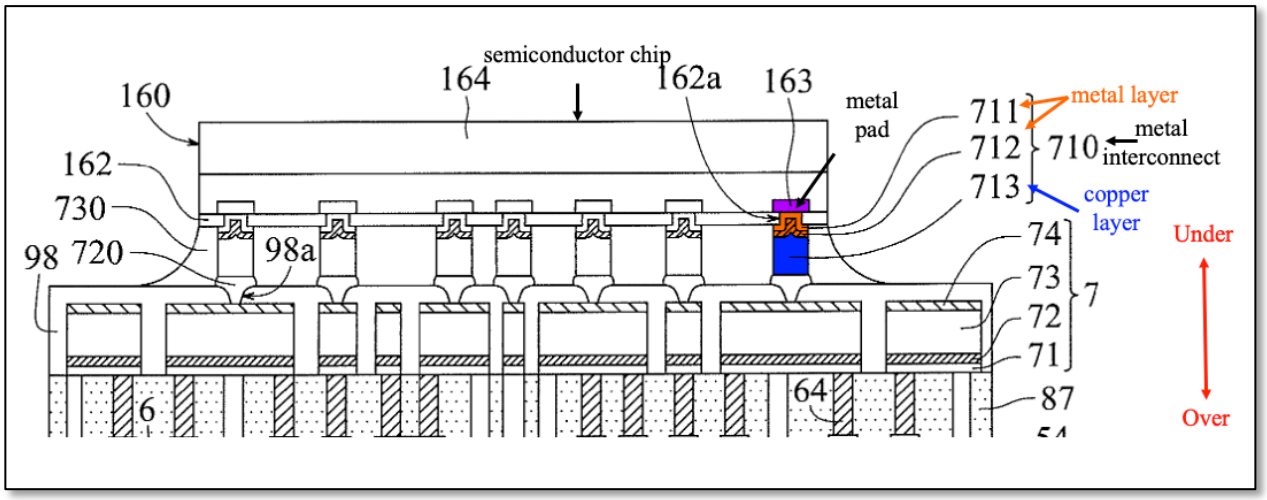
19. 1(f)(ii): "wherein said fourth metal interconnect comprises a second metal layer on said first metal pad and a fifth copper layer over said second metal layer, wherein said fifth copper layer has a thickness between 5 and 30 micrometers,"

a) Lin-191's Teachings

186. Lin-191 teaches "metal pillars or bumps 710" on "metal traces or pads 163" of a semiconductor chip 160, that connect chip 160 to various other structures in Lin-191's multi-chip module thus functioning as a *metal interconnect*. *EX1005* at [0408]. Lin-191's metal pillars or bumps 710 comprise an "adhesion layer 711[,]" a "seed layer 712[,]" and a "metal layer 713[.]" *EX1005* at [0389]. Adhesion layer 711

is formed on a "contact point" of "the metal traces or pads 163[.]" *EX1005* at [0389]. Adhesion layer 711 is "nickel" or "titanium[.]" *EX1005* at [0390], [0394]. Seed layer 712 "can be a copper layer." *EX1005* at [0392]. Thus, the combination of layers 711 and 712 is a *second metal layer on* metal pad 163. That is, because layer 711 is formed on a "contact point" of "metal traces or pads 136" and because both of layers 711 and 712 are *metal*, the mapped combination of layers 711/712 is a *second metal layer on said first metal pad*. *EX1005* at [0389]. The "metal layer 713 can be a single layer of copper" having a thickness "between 2 and 30 micrometers." *EX1005* at [0396]. Lin-191 thus teaches or renders obvious a *fifth copper layer ha[ving] a thickness between 5 and 30 micrometers*.

187. I note that the '768 Patent does not ascribe any criticality to the range of 5 and 30 micrometers. That is, the '768 Patent does not provide the range of 5 and 30 micrometers and then further provide an explanation for why such range is needed, important, or advantageous. Indeed, the '768 Patent describes a variety of ranges, including smaller (between 2 and 5 micrometers) and larger (between 10 and 50 micrometers), indicating to a POSITA that the thickness can vary widely and that the thickness is not otherwise critical. *See EX1001* at 14:15-27.



EX1005 at FIG. 72 (excerpt).

b) Motivation to Combine

188. A POSITA would have found it obvious and been motivated to modify Sundaram's *fourth metal interconnect* per Lin-191's metal pillar or bump 710 (including the thickness of copper layer 713), such that the bump has a *second metal layer* on Sundaram's *first metal pad* and a *fifth copper layer* having a *thickness between 5 and 30 micrometers over* the *third metal layer*. Thus, the combination yields Sundaram's *fourth metal interconnect* having a *second metal layer on said first metal pad and a fifth copper layer over said second metal layer*.

189. A POSITA would have recognized Lin-191's metal pillar or bump 710 would improve metallurgical bonding and enhance reliability by employing a layered structure. Specifically, it was known that multi-layer metal bumps would provide the benefit of "improvement of adhesion of the various overlying layers or the prevention of diffusion of materials between adjacent layers[,]" thereby

improving metallurgical bonding. *EX1022* at 3:49-56. Indeed, it was known that "when a solder bump made of, for example, SnPb, SnAg, SnCu, SnAgCu, SnZn, SnZnBi, SnIn…Sn, which the solder bump is primarily made of, diffuses into the electrode pad and wiring made of Al or Cu," which may result "in electric problems in some cases." *EX1047* at [0003]. "To prevent the diffusion, a UBM [] that is highly effective in preventing solder diffusion is used between the electrode pad and the solder bump." *EX1047* at [0004]. "As a typical example, of the UBM having the barrier capability, Ni…is often used[.]"*EX1047* at [0004]. Therefore, a POSITA would have recognized that a UBM structure, such as Lin-191's metal pillar or bump 710, would improve the connection between Sundaram's *first metal pad* and *fourth metal interconnect* by preventing diffusion of solder material into the *first metal pad*.

190. Additionally, a POSITA would have understood that by employing Lin-191's layered structure the solder joint would have increased resistance to fatigue and stress-induced failure because the copper seed layer would ensure a uniform plating of the thicker copper portion (layer 713) as electroplating copper without a seed layer may "lead to a void in the electroplated metal[,]" thereby compromising mechanical integrity. *EX1063* at 3:12-16. Additionally, a POSITA would have appreciated the advantages of coppers use in interconnects and been motivated to include the *fifth copper layer ha[ving] a thickness between 5 and 30 micrometers* in the *third metal interconnect*. Specifically, copper was known to have "high

immunity to electromigration, high ductility, and high melting point[,]" making it a desirable choice for interconnect material in high-density packaging. *EX1054* at 2:2-14..

191. Thus, the mechanical integrity of Sundaram's *fourth metal interconnect* would be improved by employing such a layered structure, thereby enhancing the reliability of the interconnects, particularly in applications subjected to repeated temperature fluctuations and mechanical stress. As such, the modification of Sundaram's *fourth metal interconnect*, per Lin-191's metal pillar or bump 710, would have been an obvious and advantageous modification to improve long-term solder ball performance.

192. Moreover, a POSITA would have appreciated that the thickness of Lin-191's *third copper layer* (i.e., between "2 and 30 micrometers" which teaches or renders obvious *between 5 and 30 micrometers*) would allow for optimal underfill placement, as demonstrated by Lin-191. *EX1005* at FIG. 72. Specifically, as shown above in FIG. 72, Lin-191's metal pillars or bumps 710 are surrounded by "underfill 730[.]" *EX1005* at [0381]. A POSITA would recognize that Lin-191's thickness of layer 713 (*third metal layer*) allows for ample space for underfill 730 to be placed and would have found that desirable as limited space would prevent proper underfill filling. As shown in FIG. 3, Sundaram already teaches such an underfill between first electronic device 125 and interposer 105 such that applying Lin-191's third

copper layer thickness would have allowed for Sundaram's underfill to be sufficiently deposited. Underfill integrity was an important feature as underfill materials were known to "redistribute the stress caused by CTE mismatch" by "allow[ing] [] stress to be more uniformly spread out over the entire surface of the chip, supporting substrate and solder balls." *EX1135* at 4:34-40. Accordingly, a POSITA would have appreciated that Lin-191's *third copper layer* thickness would achieve proper underfill filling, thereby decreasing CTE mismatch-induced stress to Sundaram's first electronic device 125, *third metal interconnect,* and RDL.

193. A POSITA would have found the modification obvious at least because it is nothing more than the application of a known technique (a layered bump structure) to improve similar structures (Sundaram's chip package, Lin-191's chip package) in a predictable manner. That is, Sundaram's *fourth metal interconnect* is improved in the same way as Lin-191's metal pillar or bump 710. Alternatively, a POSITA would have been motivated to substitute Lin-191's bump structure for Sundaram's *fourth metal interconnect* to obtain the above-described advantages of Lin-191's teachings.

194. A POSITA would have had a reasonable expectation of success in both applying Lin-191's teachings to Sundaram's *fourth metal interconnect* or substituting Lin-191's metal pillar or bump 710 for Sundaram's *fourth metal interconnect*. Indeed, Lin-191 and Sundaram are both directed to semiconductor

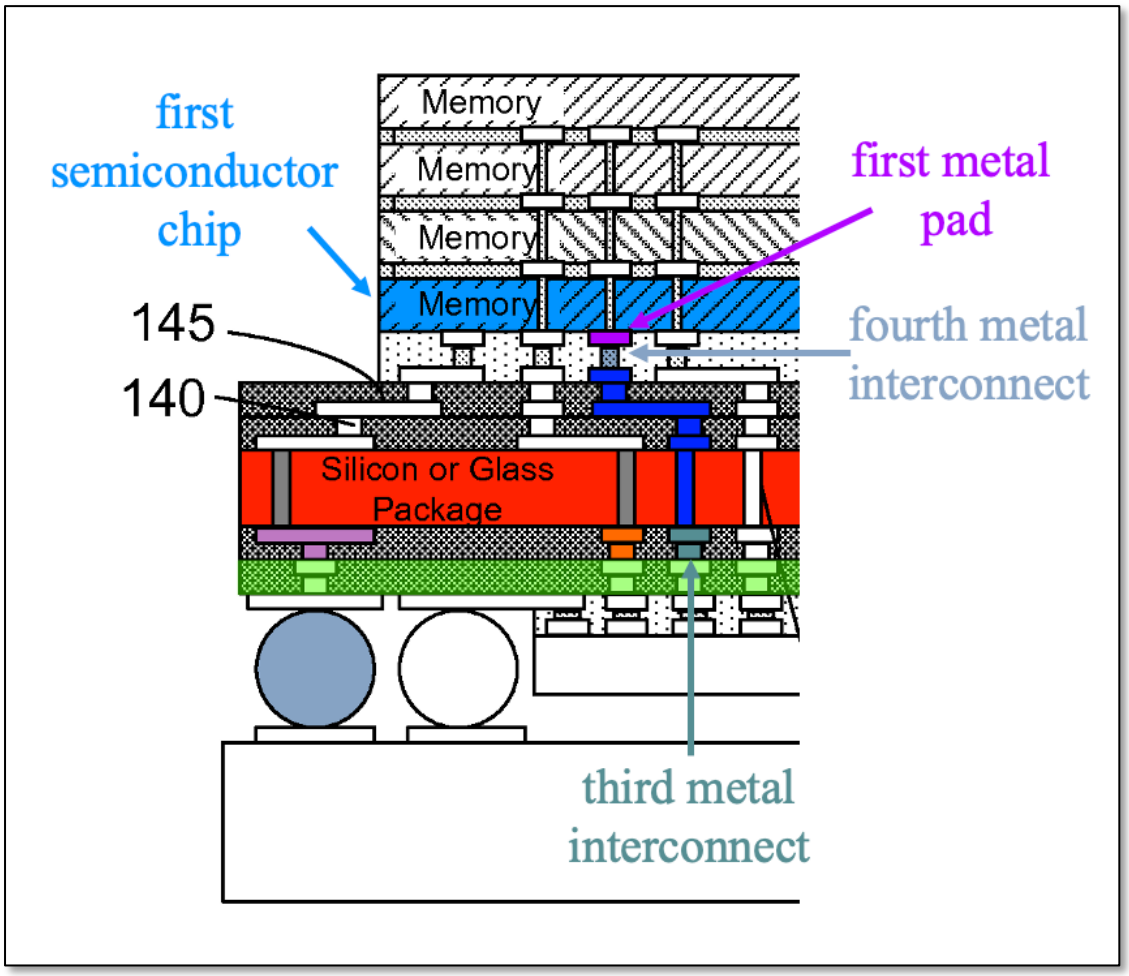
package interconnect technology. Further, bump interconnects were well-known and formed using common manufacturing techniques, such as physical-vapor deposition, sputtering, and electroplating. *EX1005* at [0413], [0420]; *EX1042* at ("…filled with copper typically by an electroplating process, as known to one of ordinary skill in the art of integrated circuit fabrication."); *EX1043* at [0032] ("… a variety of different deposition methods known by one of ordinary skill in the art, including but not limited to, CVD, pulsed CVD, PECVD, ALD, PEALD, or sputtering methods."); ¶¶ 71-76. For example, Lin-191's methods of forming metal or pillar bump 710, such as electroplating, were well-known and well-established, further contributing to a reasonable expectation of success. *EX1005* at [0400].

20. 1(f)(iii): "wherein said fourth metal interconnect is connected to said third metal interconnect."

195. Sundaram's *fourth metal interconnect is connected to said third metal interconnect* through vias 140 and traces 145 and a through via 110. Sundaram teaches that first electronic device 125 (the first semiconductor chip) includes die pads 135 where "metallization provides die pad surfaces 135." *EX1004* at 6:23–25. A POSITA would understand—consistent with industry practice that "I/O terminals were traditionally formed by way of metal pads along the periphery of an IC" (*EX1095* at 1:24–25)—that the *first metal pad* shown in FIG. 3 is connected to die pad 135 by the *fourth metal interconnect*. *EX1004* at 6:29–33 ("die pads 135…can electrically connect devices using solder, copper bumps with solder caps, [or]

copper-to-copper bonding."). Thus, the *fourth metal interconnect* disposed on die pad 135 in FIG. 3 is a metal interconnect that electrically couples device 125 to interposer 105.

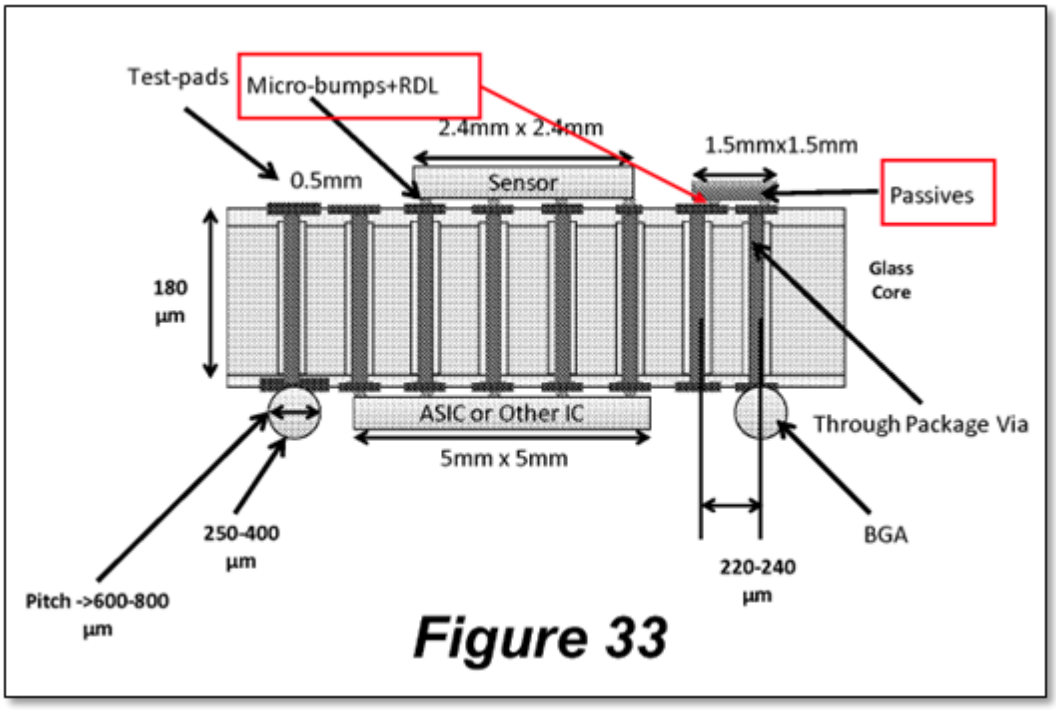
196. From the *fourth metal interconnect*, Sundaram routes electrical connection through the interposer using the conductive pathway highlighted in blue: vias 140 couple the die-pad bump to traces 145, the traces 145 route laterally within the substrate, and a vertical through via 110 then carries the signal to the package's *third* metal interconnect. *EX1004* at FIG. 3. A POSITA would recognize that these elements form a continuous conductive stack from the *fourth metal interconnect* on die pad 135 to the *third metal interconnect*. Accordingly, Sundaram teaches that the *fourth metal interconnect is connected to said third metal interconnect* through vias 140, traces 145, and a through via 110. In my opinion, *connected to* does not require a direct physical connection but is instead met by an electrical connection. This is evidenced by the '768 Patent's descriptions at various spots, e.g., 2:34-36 (connection through a metal bump); 14:28-32 (connection of bumps 50 to layer 36 though layer 54); and 15:50-51 (connection of pads 49 to pads 48 through layer 51). Thus, Sundaram teaches the limitation.



EX1004 at FIG. 3.

B. ***Claim 2: "The chip package of claim 1, further comprising a passive component over said first interconnection scheme and connected to said first interconnection scheme through a solder layer."***

197. Sundaram teaches a *passive component* ("passives") connected to an interposer by "micro-bumps+RDL." *EX1004* at FIG. 33.



EX1004 at FIG. 33.

198. Because Sundaram teaches connecting passives to an "RDL" via "micro-bumps," thus teaches a *passive component* that is *connected to* an *interconnection scheme* (RDL) *through a solder layer* (micro-bumps). Sundaram's "micro-bumps" are a *solder layer* at least because Sundaram teaches that "solder" is used for "electrically connect[ing] device" and because as I described above, solder bumps were known to be formed of *solder layer[s]*. *EX1004* at 6:29-32; ¶¶ 71-76.

a) Motivation to Combine Sundaram's Embodiments

199. Based on the FIG. 33 embodiment, a POSITA would have found it obvious and been motivated to modify Sundaram's chip package to comprise a *passive component over* the *first interconnection scheme* and connected to a metal interconnect through a *solder layer*. In the combination, the *passive component* is

positioned adjacent to FIG. 3's second electronic device 130, therefore *over* the *first interconnection scheme*.

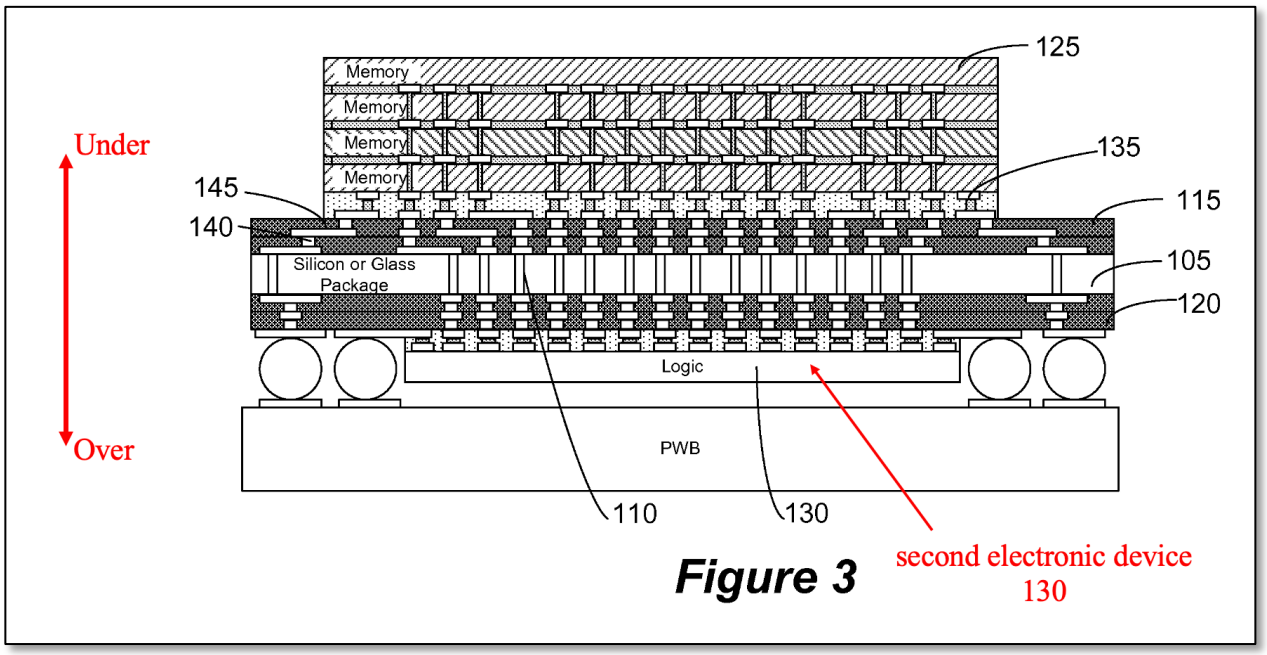


Figure 3

EX1004 at FIG. 3.

200. A POSITA would have appreciated that by connecting a passive component, e.g., a capacitor, over Sundaram's *first interconnection scheme*, Sundaram's chip package would advantageously mitigate signal desynchronization and preserve signal integrity.

201. Passive components, such as capacitors, were known to preserve signal integrity by filtering out noise from signal generated by chips. *See, e.g., EX1048* at [0001] ("Chips such as Application Specific Integrated Circuits [] often include power and ground connections to the circuit board. Capacitors,, often referred to as 'bypass capacitors' or 'decoupling capacitors,' are usually coupled across the power

and ground connections to filter out unwanted electrical noise that may be generated by the power supply. The bypass capacitors may be disposed on the bottom side of circuit board within the footprint of the ASIC.").

202. Indeed, "by use of bypass capacitors on multi-layer printed circuit boards, the total area of the current loop formed by the signal trace and its return current can be minimized. Signal integrity, which is influenced by factors such as impedance, inductive crosstalk to other signals, signal transmission line reflection, and balance, can be improved and noise can be well controlled." *EX1049* at 7:11-19. Additionally, capacitors were known to provide "less noisy power being supplied" to chips in a chip package by "providing a low inductance path between power and ground." *EX1050* at 5:37-41.

203. As such, a POSITA would appreciate both the improvement in signal integrity and reduction in power noise due to the low-inductance path provided by the *passive component*. Further, including a passive component, such as a capacitor, would reduce the impact of high frequency interference (HFI) on digital signals being transmitted between first electronic device 125 (*first semiconductor chip*) and the PWB as well as reduce the negative impact of HFI on power supply lines in Sundaram's chip package, thereby further preserving signal integrity. Specifically, "when events take place that have frequency higher than what can be accommodated by a voltage regulator, noise occurs." *EX1100* at [0004]. A capacitor "works as

backup energy storage" that can "quickly provide the shortfall" if the voltage drops due to such high frequency events. *EX1100* at [0004].

204. The modification is the application of a known technique (implementing a passive component) to a known device (Sundaram's chip package) to yield the predictable result of Sundaram's chip package having a passive component over the *first interconnection scheme*. Further, a POSITA would have had a reasonable expectation of success in including a *passive component* in Sundaram's chip package, because Sundaram already teaches a *passive component* and because soldering passive components into chip packages was a very well-known technique. *See, e.g., EX1051* at FIG. 14, [0093] ("…chip capacitor 213 are provided with a power electrode 214 to be connected to the power internal electrode layer and the power solder bump 217…and the ground solder bump 220."). Furthermore, the inclusion of passive components such as Sundaram's was a ubiquitous practice in chip packaging, thus making the modification simple, straightforward, and routine, thereby further evidencing the reasonable expectation of success. *See, e.g., EX1052* at FIG. 2, [0025] ("The flip-chip BGA package 4 further comprises an RC passive component 41 such as a resist or a capacitor…"); *EX1053* at [0030] ("In some embodiments, electronic components such as the component 180 can comprise passive components (e.g., resistors, capacitors, inductors)…").

C. *Claim 3: "The chip package of claim 1, wherein said first interconnection scheme comprise a fifth metal interconnect across over a sidewall of the first semiconductor chip."*

a) "Fifth Metal Interconnect"

205. As I discussed above at claim 1(d), Sundaram's *first interconnection scheme* comprises die pads 135 that "electrically connect devices" thus functioning as an *interconnect*. *See* ¶ 150. Sundaram additionally teaches "metallization provides die pad surfaces 135" such that the die pads 135 are *metal*. *EX1004* at 6:22-24. FIG. 3 illustrates numerous die pad surfaces. An example one of the many die pad surfaces is identified with reference numeral 135 in FIG. 3. *EX1004* at 6:22-33 (referencing die pads (plural)). However, a POSITA would have understood that FIG. 3 expressly teaches a die pad surface such as the orange-highlighted die pad die pad in the below FIG. 3 at least because of the ubiquity of connecting bumps to pads and because Sundaram labels a similar structure as such. *See* ¶ 65. The die pad 135 shown in orange below is therefore a *fifth metal interconnect* that, like the trace 145 and via 140 making up the *first metal interconnect*, "electrically connect[s]" first and second devices 125, 130. *EX1004* at FIG. 3, 6:29-33; 6:62-67.

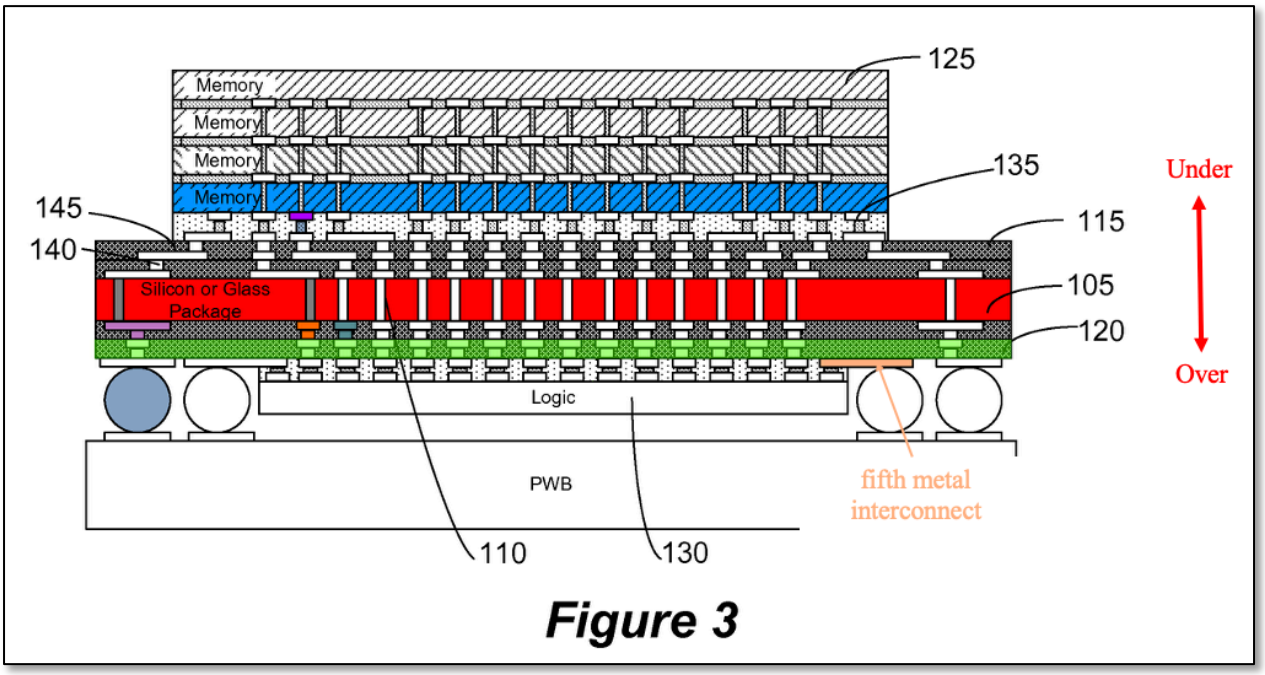
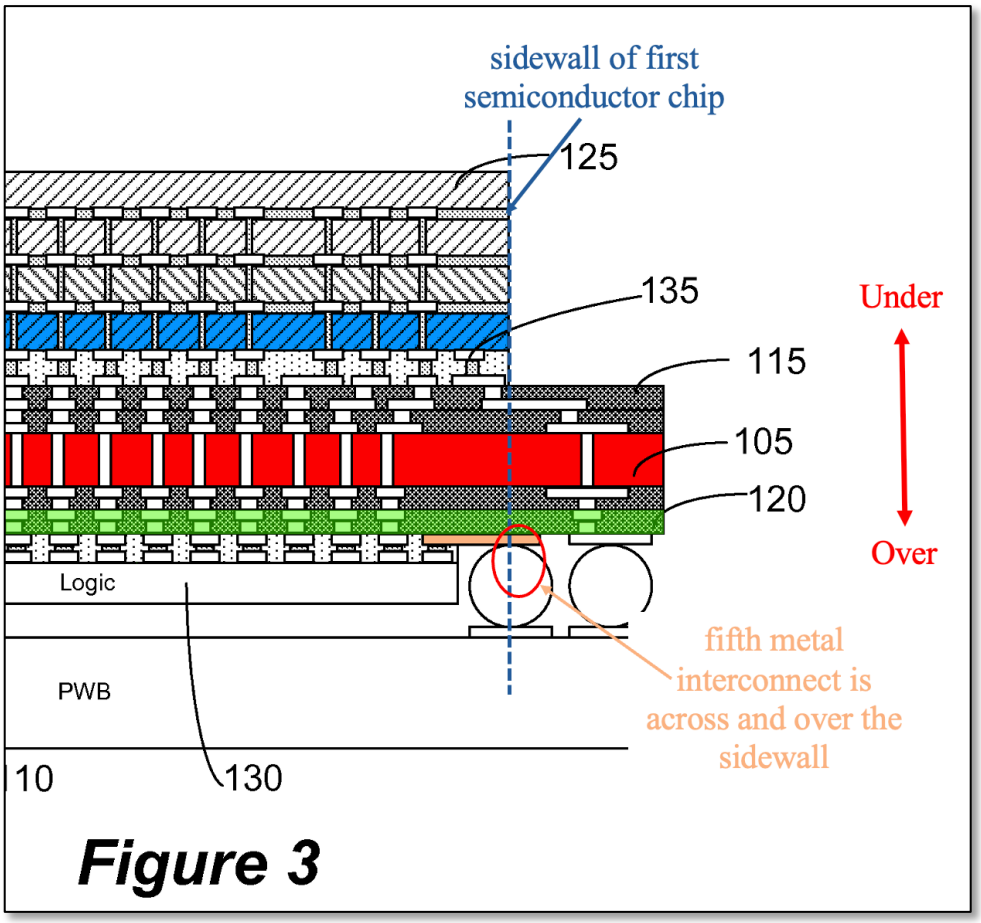


Figure 3

EX1004 at FIG. 3.

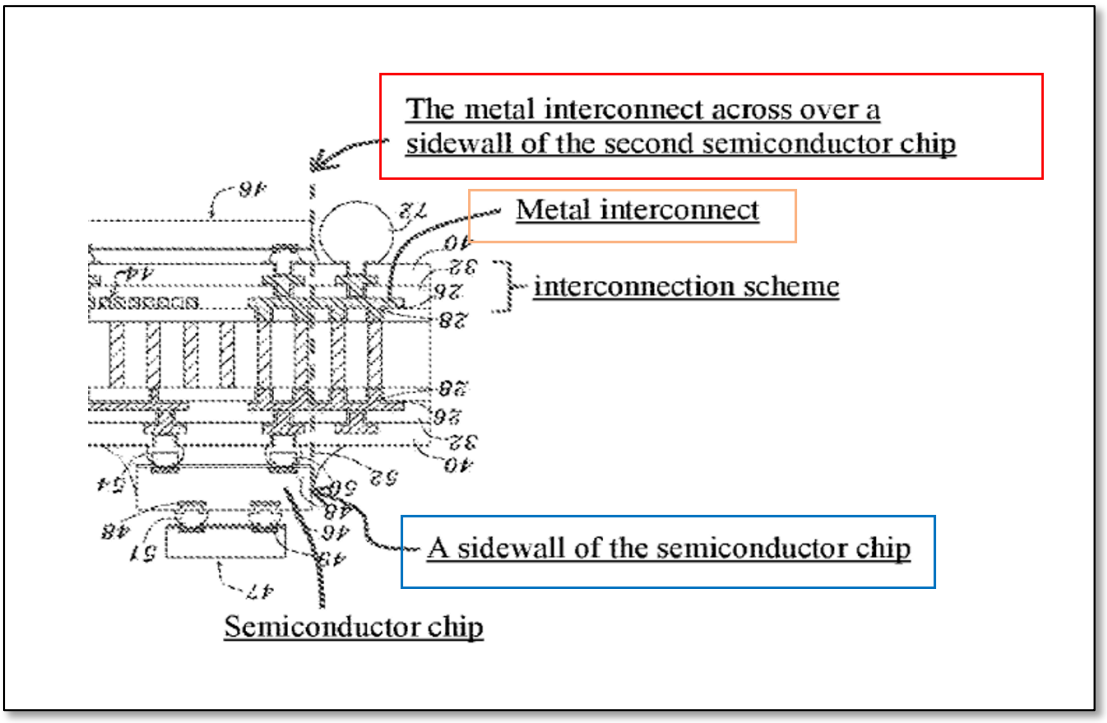
b) "Across Over a Sidewall"

206. The annotated figure below illustrates that the *fifth metal interconnect* is both *across* and *over* a *sidewall* of first electronic device 125 (*first semiconductor chip*). The blue dashed line indicates the *sidewall* of first electronic device 125, namely a boundary thereof. Notably, the *fifth metal interconnect* is positioned in the "over" direction relative to the *sidewall*, as indicated by the red arrow depicting the over/under directions. Additionally, the *fifth metal interconnect* extends laterally (i.e., left/right) to the right past the boundary of the *sidewall*. As such, the *fifth metal interconnect* is both *across* and *over a sidewall of the first semiconductor chip*.



EX1004 at FIG. 3 (excerpt).

207. I note that Sundaram's teachings of the *fifth metal interconnect* being *across* and *over* the *sidewall of the first semiconductor chip* are consistent with an annotated figure that Patent Owner provided during prosecution of '768 Patent, arguing support for this claim limitation. In the figure below, I have shown how the Patent Owner's annotations mirror the above mapping of Sundaram's *fifth metal interconnect*.



EX1002 at p. 537.

D. *Claim 4*

1. Claim 4(a): "The chip package of claim 1, further comprising a second semiconductor chip over said first interconnection scheme,"

208. Shown below, Sundaram teaches a second electronic device 130, which may be a "logic IC device or devices," and is thus a *second semiconductor chip*. *EX1004* at 6:38-39. As shown, Sundaram's *second semiconductor chip* is *over said first interconnection scheme*.

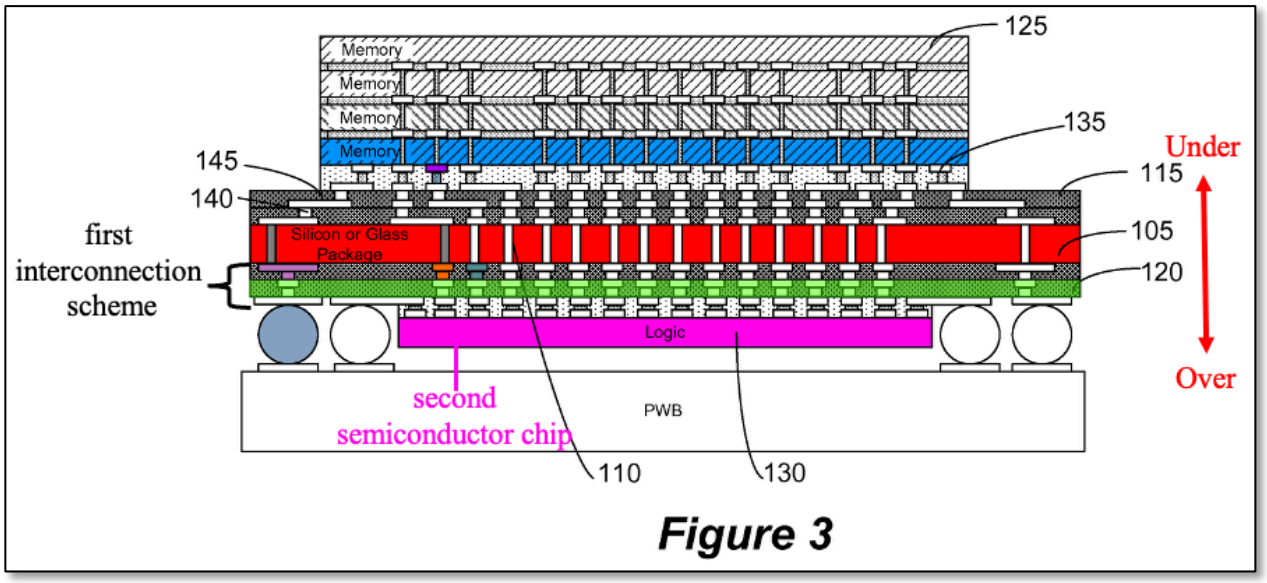
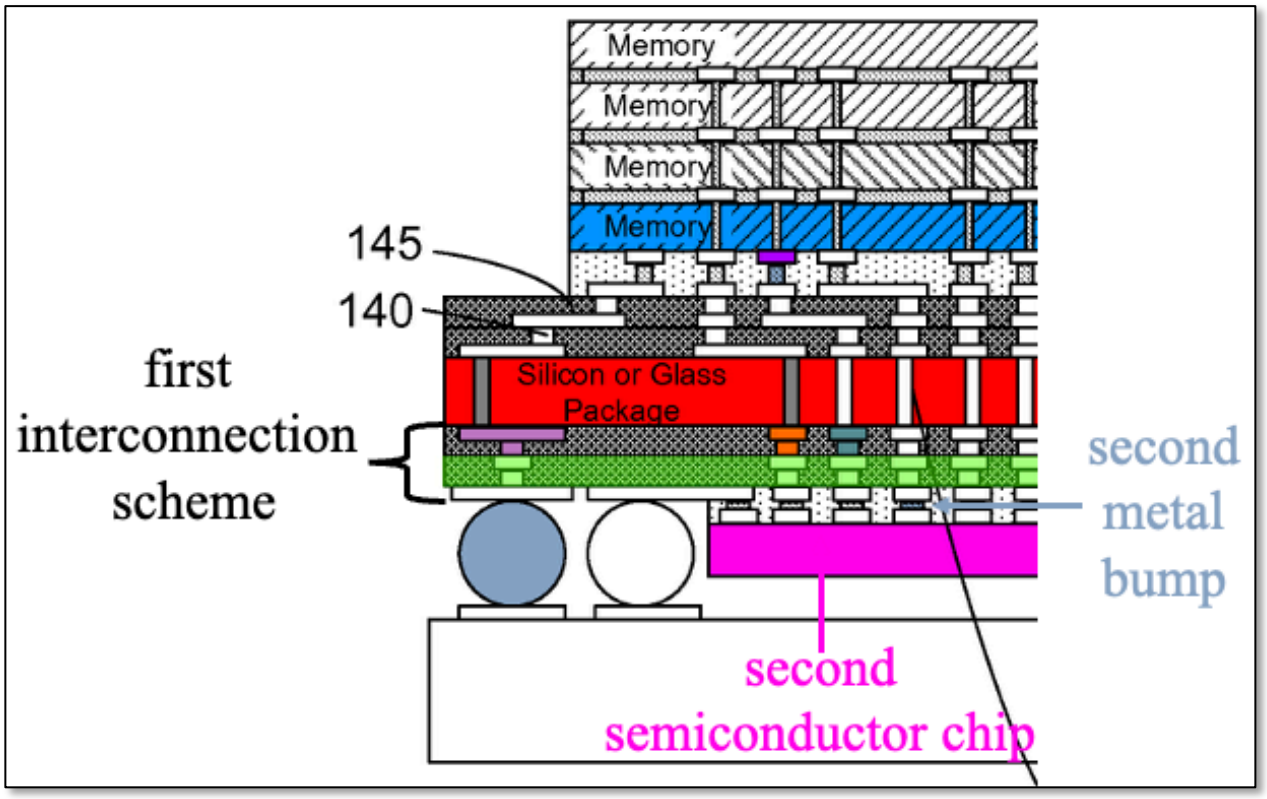


Figure 3

EX1004 at FIG. 3.

2. Claim 4(b): "wherein said second semiconductor chip comprises a second metal bump between said second semiconductor chip and said first interconnection scheme."

209. Recall that Sundaram teaches "die pads 135…can electrically connect devices using solder, copper bumps with solder caps, copper to copper bonding." *EX1004* at 6:29-33. In FIG. 3, below, the *second semiconductor chip* is depicted as being connected to a bump on die pad 135. Because Sundaram teaches "copper bumps with solder caps[,]" the bump on die pad 135 is a *second metal bump*. *EX1004* at 6:29-33. Further, Sundaram's *second metal bump* is shown as *between said second semiconductor chip and said first interconnection scheme*.



EX1004 at FIG. 3 (excerpt).

E. ***Claim 5: "The chip package of claim 1, wherein said first semiconductor chip comprises a central-processing-unit (CPU) circuit block and a graphics-processing-unit (GPU) circuit block."***

a) Lin-191's Teachings

210. Lin-191 teaches semiconductor chips as "system-on chip[s] (SOC) including **a graphics-processing-unit (GPU) circuit block**, a wireless local area network (WLAN) circuit block **and a central-processing-unit (CPU) circuit block**…" *EX1005* at [0106].

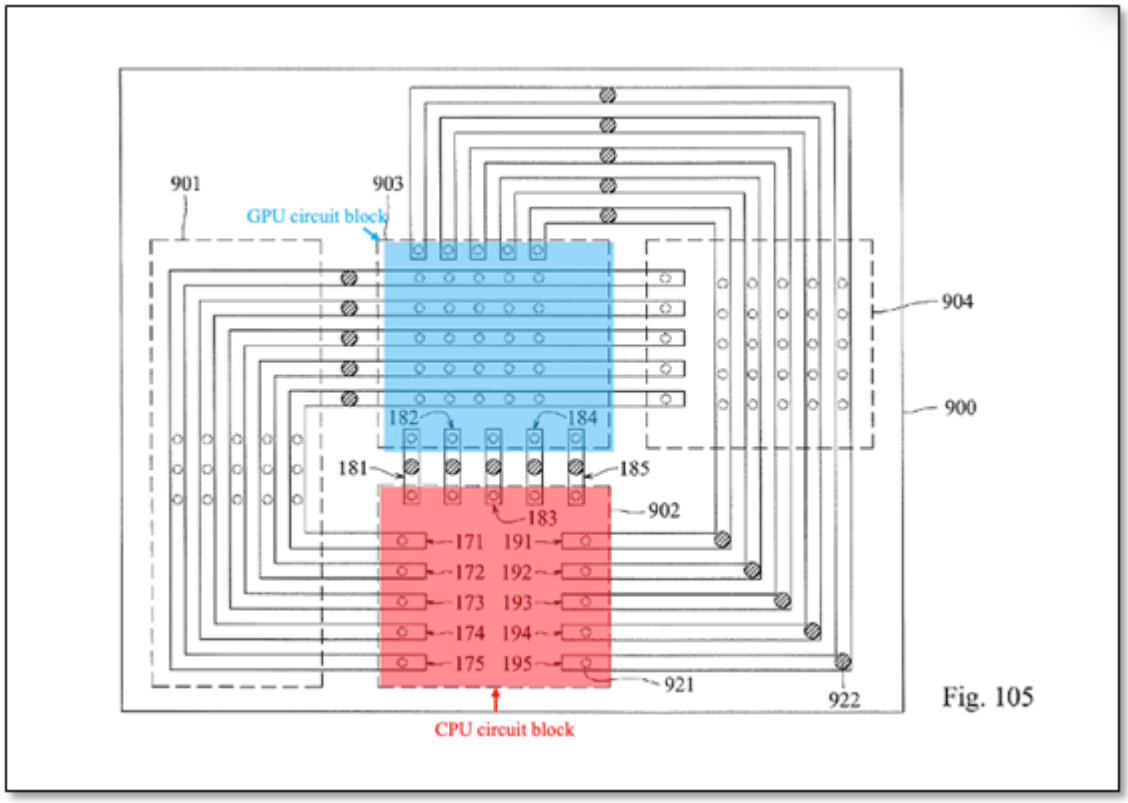


Fig. 105

EX1005 at FIG. 105, [0541], [0543] (describing FIG. 105).

b) Motivation to Combine

211. A POSITA would have found it obvious and been motivated to modify Sundaram's first electronic device 125 to comprise *a CPU circuit block and a GPU circuit block* based on the teachings of Lin-191. The modification would have predictably improved Sundaram first electronic device 125 by providing first electronic device 125 with the ability to perform the functions of both a GPU and a CPU. While Sundaram's FIG.3 depicts device 125 as stacked memory, Sundaram teaches "other electronic devices can also be used as the first electronic device 125." *EX1004* at 6:37-43. Thus, a POSITA would have considered the depicted memory

stack to be merely exemplary and would have been motivated to modify first electronic device 125 to have a CPU and GPU circuit block for applications requiring such processing power. Sundaram teaches "smart and mobile phone applications, including video streaming, 3D graphics, camera-functions, and gaming are driving the demand for logic to memory bandwidth [] at increasing levels without an increase in power consumption," such that a POSITA would have found it obvious to modify Sundaram's chips package, per Lin-191's teachings, to carry out the requisite CPU/GPU tasks for such mobile phone applications. *EX1005* at 1:20-25. Further, Sundaram already contemplates "high power logic component[s]" on device 125's side of interposer 105:

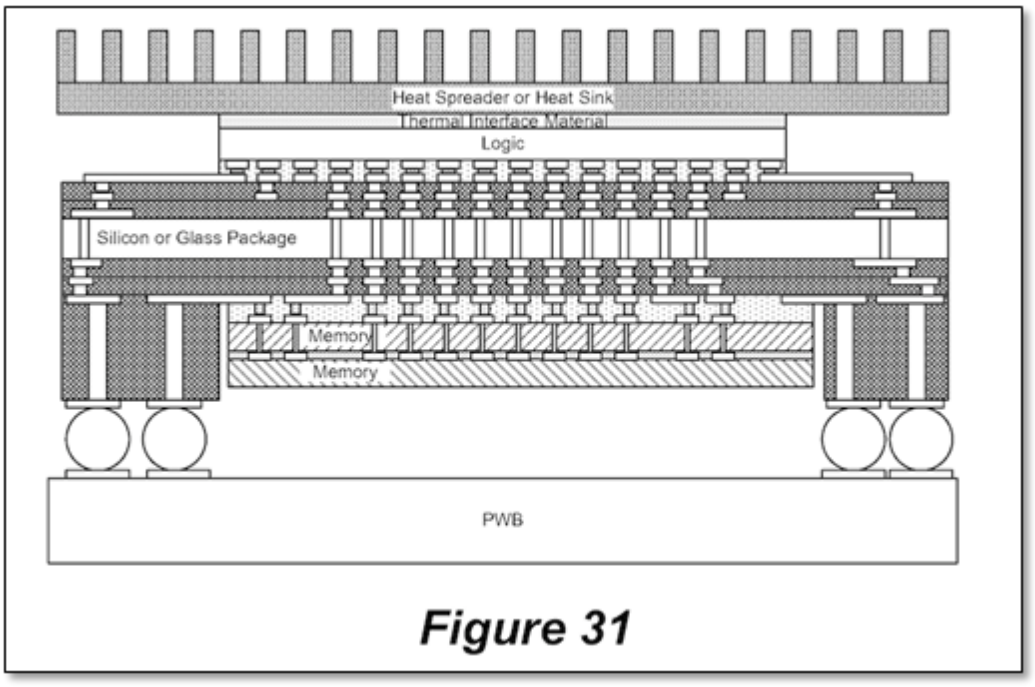


Figure 31

EX1004 at FIG. 31.

212. The Sundaram-Lin-191 combination is the application of a known technique (a semiconductor chip with a CPU circuit block and a GPU circuit block) to a known device (Sundaram's chip package including first electronic device 125) yielding the predictable results of Sundaram first electronic device 125 having both a CPU circuit block and a GPU circuit block. A POSITA would have been motivated to apply Lin-191's teachings based on the desired functionality of Sundaram's chip package, e.g., to obtain the benefits of having a CPU and a GPU on a single chip. As I described above, combined GPU/GPU architectures were known to provide the benefits such as the "opportunity to leverage both the high computational power from GPUs for regular applications and flexible execution from CPUs for irregular workloads" as well bypassing "costly CPU-GPU data transfers[.]" *EX1031* at p. 1-2; ¶ 87. As such, a POSITA would have been motivated to achieve such benefits by implementing Sundaram's first electronic device 125 (*first semiconductor chip*) with *a central-processing-unit (CPU) circuit block and a graphics-processing-unit (GPU) circuit block.*

213. Because chips including both GPU and CPU circuit blocks were well known prior to the '768 Patent, there would have been a reasonable expectation of success. *See, e.g., EX1101* at [0022] ("In one embodiment, the APU 110 may include a general purpose central processing unit (CPU) 130 and a graphics processing unit (GPU) 140 on a same semiconductor die."). Indeed, by the time of the '768 Patent,

AMD and Intel had had both released chips having both GPU and CPU circuit blocks. *See* ¶ 87; *see also EX1102* at p. 1 ("The chip is Intel's first to integrate the graphics processing unit (GPU) on the processor itself.").

F. *Claim 6*

1. Claim 6(a): "The chip package of claim 1, wherein said first semiconductor chip comprises a second metal pad on a top surface of said first semiconductor chip and a third metal pad on a bottom surface of said first semiconductor chip,"

214. Sundaram's first electronic device 125 (*first semiconductor chip*) has pad[s] on the *top* and *bottom* surfaces. Specifically, as shown below, FIG. 3 expressly depicts first electronic device 125 having a *second…pad* and a *third…pad*. A POSITA would have found it obvious that Sundaram's *second…pad* and *third…pad* are *metal pad[s]* because virtually every chip has a metal pad for forming electrical connections and metal pads were ubiquitous. See, e.g., *EX1065* at [0005] ("Refer[ring] to FIG. 1 for a **conventional** electronic component, which includes a chip 1 and a substrate 3. The chip 1 has a plurality of metal pads 2."); *EX1095* at 1:24-25. ("I/O terminals were traditionally formed by way of metal pads along the periphery of an IC."). A *metal pad* on the *top surface* is a *second metal pad* and a *metal pad* on the *bottom surface* is a *third metal pad*, respectively, as shown below in FIG. 3.

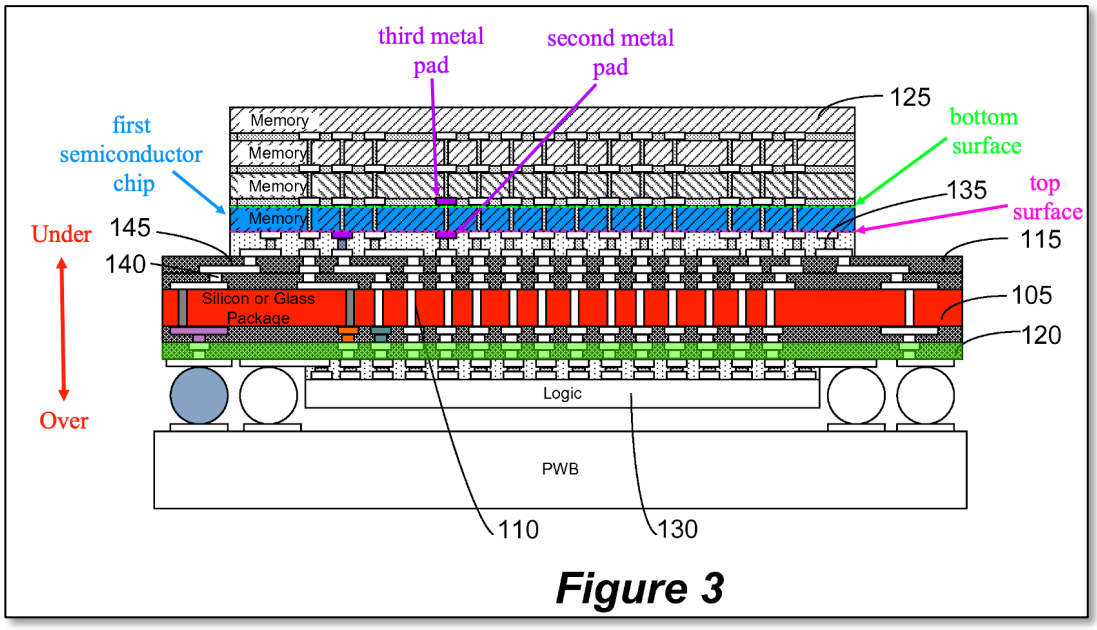


Figure 3

EX1004 at FIG. 3.

215. Additionally to FIG. 3's teachings, Sundaram's FIG. 32 teaches a semiconductor chip having *metal pad[s]* on the *top* and *bottom* surfaces, as shown below. Such teachings further confirm Sundaram's familiarity with forming metal pads on either surface a chip and, as discussed below, a POSITA would have been motivated to apply the teachings of FIG. 32 to FIG. 3.

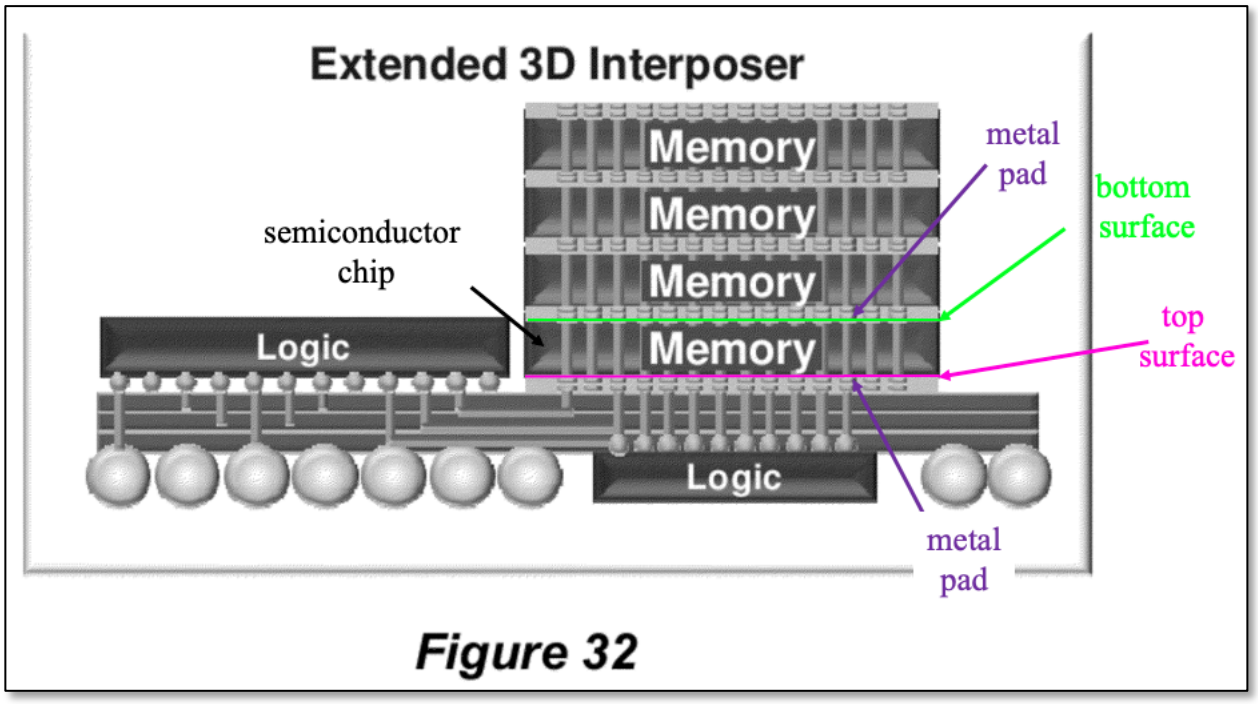


Figure 32

EX1004 at FIG. 32.

216. Given the ubiquity of *metal pad[s]* in semiconductor chips, a POSITA would have found it obvious and been motivated to modify FIG. 3's *first semiconductor chip* to have metal pads on both the top and bottom surfaces, like that of FIG. 32. The modification is a mere implementation detail in Sundaram's FIG. 3 chip stack, as semiconductor chips were conventionally and traditionally manufactured with metal pads on the periphery. *EX1095* at 1:24-25. ("I/O terminals were traditionally formed by way of metal pads along the periphery of an IC."). For the same reasons, i.e., because of the ubiquity and necessity of metal pads, a POSITA would have had a reasonable expectation of success.

2. Claim 6(b): "wherein said second metal pad is connected to said third metal pad through a through-silicon-via metal layer."

217. As shown in Sundaram's FIG. 3, the first semiconductor chip includes an interconnect (shown in orange) extending vertically between the *metal pad[s]* on the *top* and *bottom* surfaces of each stacked memory die. A POSITA would have understood that this vertical interconnect is a *through-silicon-via (TSV) metal layer* connecting the *third metal pad* to the *second metal pad*. TSVs were known to provide vertical electrical connections through a silicon substrate, typically "etched through the silicon wafer and filled with metal." *EX1066* at [0017]. Sundaram's orange interconnect corresponds to this known structure. Furthermore, Sundaram expressly describes devices employing TSVs, stating that "3D ICs with complex and expensive through silicon vias (TSVs)" are used in stacked chip assemblies. *EX1004* at 1:38-41, FIG. 1D. A POSITA would therefore have recognized that the same type of interconnect shown in FIG. 3 of Sundaram's device 125 performs the same TSV function—providing a metal connection through the silicon die between vertically aligned metal pads.

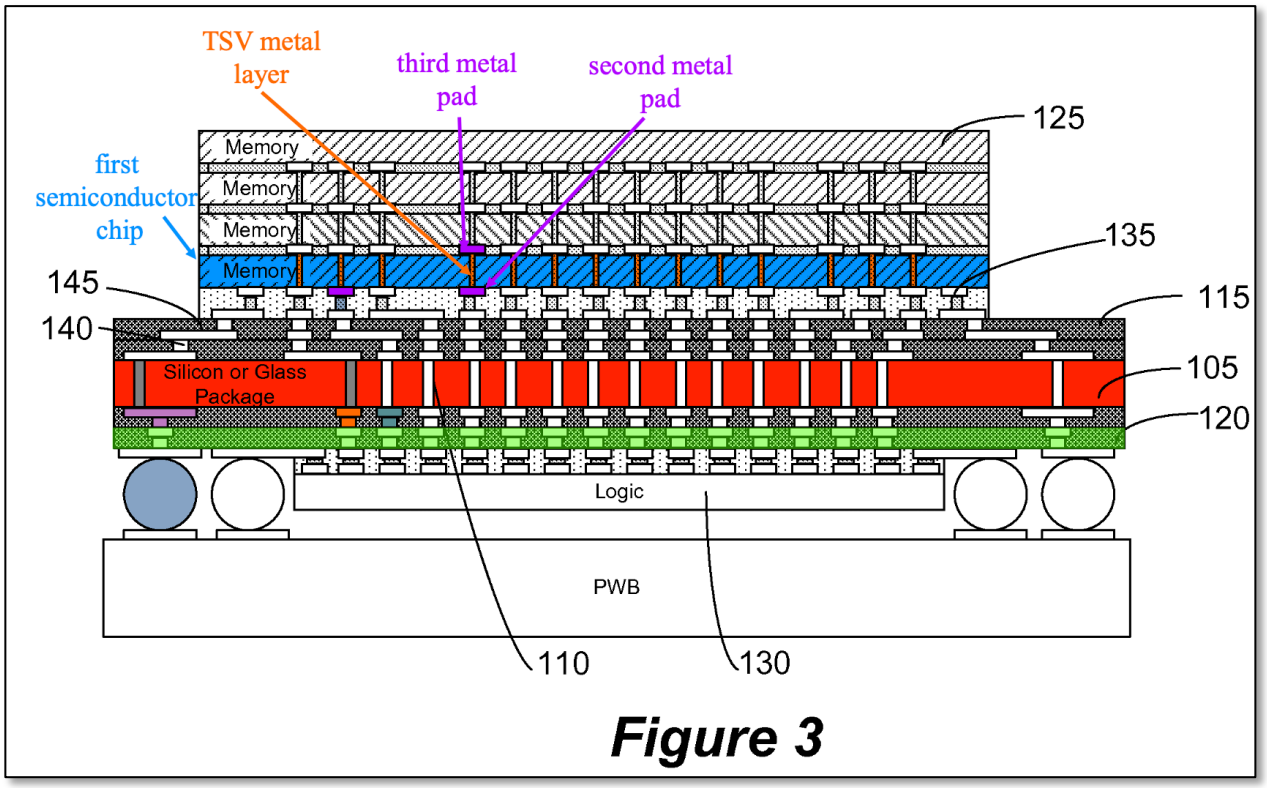


Figure 3

EX1004 at FIG. 3 (excerpt).

218. Sundaram further confirms its use of TSV metal layers in multiple locations. For example, Sundaram describes TSVs formed in "CMOS-grade Si" and filled with copper. *EX1004* at 11:15-20; *see also* 14:13-34, 15:7-8, FIG. 34. These disclosures demonstrate Sundaram's familiarity with and teaching of TSV metal layers connecting metal pads across stacked semiconductor structures. Accordingly, a POSITA would have understood that the orange interconnect structure connecting metal pads in FIG. 3 corresponds to a *TSV metal layer* connecting the *second metal pad* to the *third metal pad*.

219. Sundaram at FIG. 32 further depicts a *TSV metal layer* connecting the *second metal pad* to the *third metal pad*:

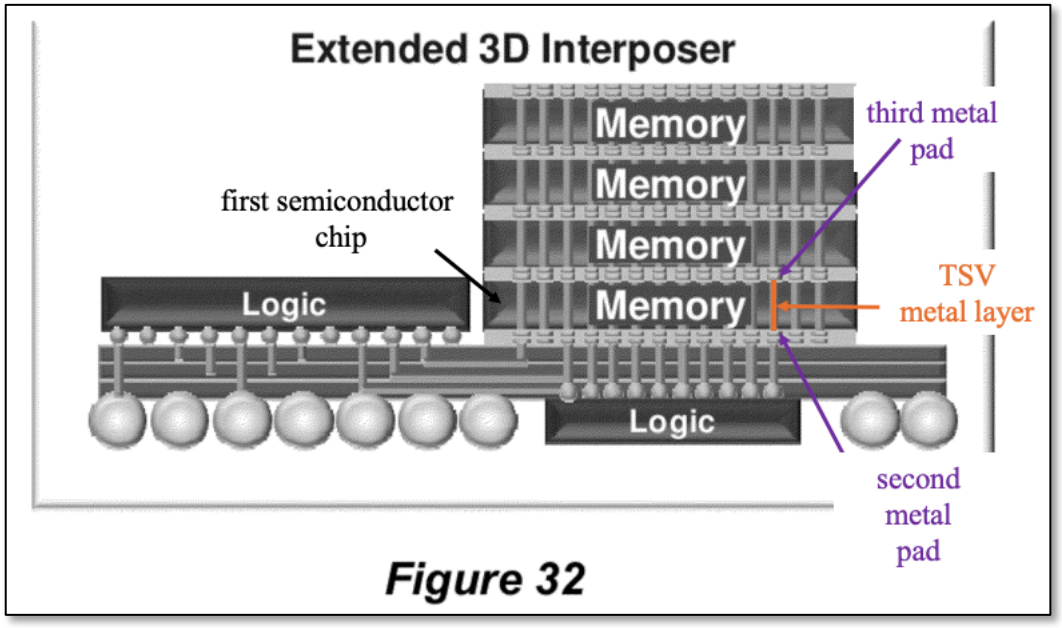


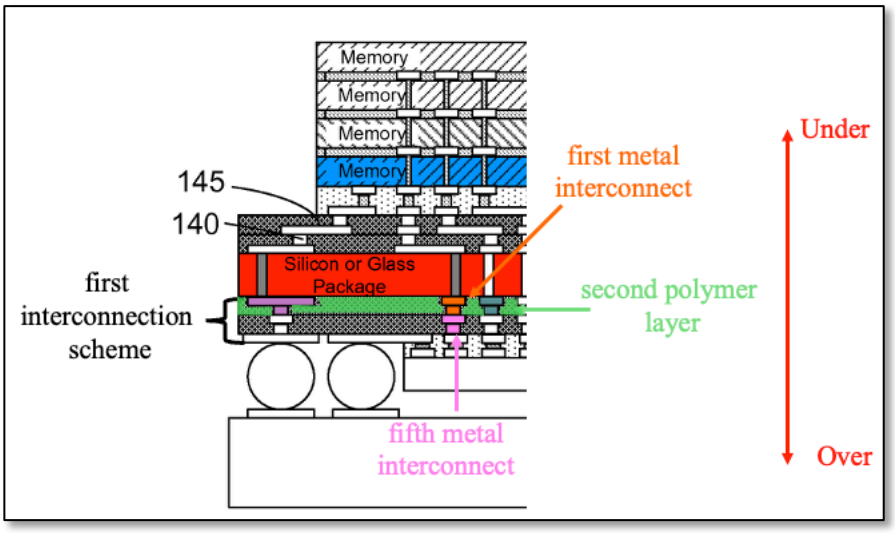
Figure 32

EX1004 at FIG. 32.

G. *Claim 7*

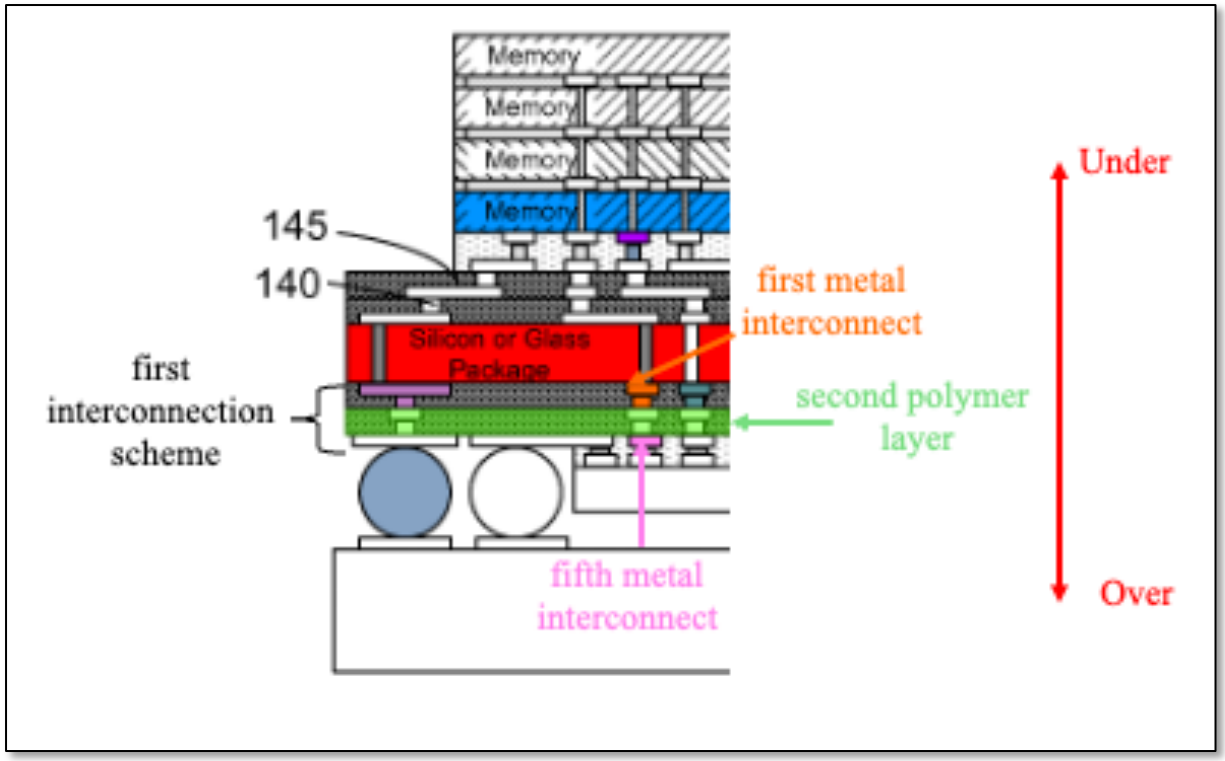
1. Claim 7(a): "The chip package of claim 1, wherein said first interconnection scheme further comprises a fifth metal interconnect over said first metal interconnect and said second polymer layer,"

220. Sundaram's *first interconnection scheme* comprises a *fifth metal interconnect*, namely a blind via 140 and conductor trace 145 that are *over* the via 140 and trace 145 forming the *first metal interconnect*, as shown below. The via 140 and trace 145 are a *metal interconnect* for the same reasons discussed above at Claim 1(d)(i). *See* ¶¶ 153-154.



EX1004 at FIG. 3 (excerpt); ¶ 154.

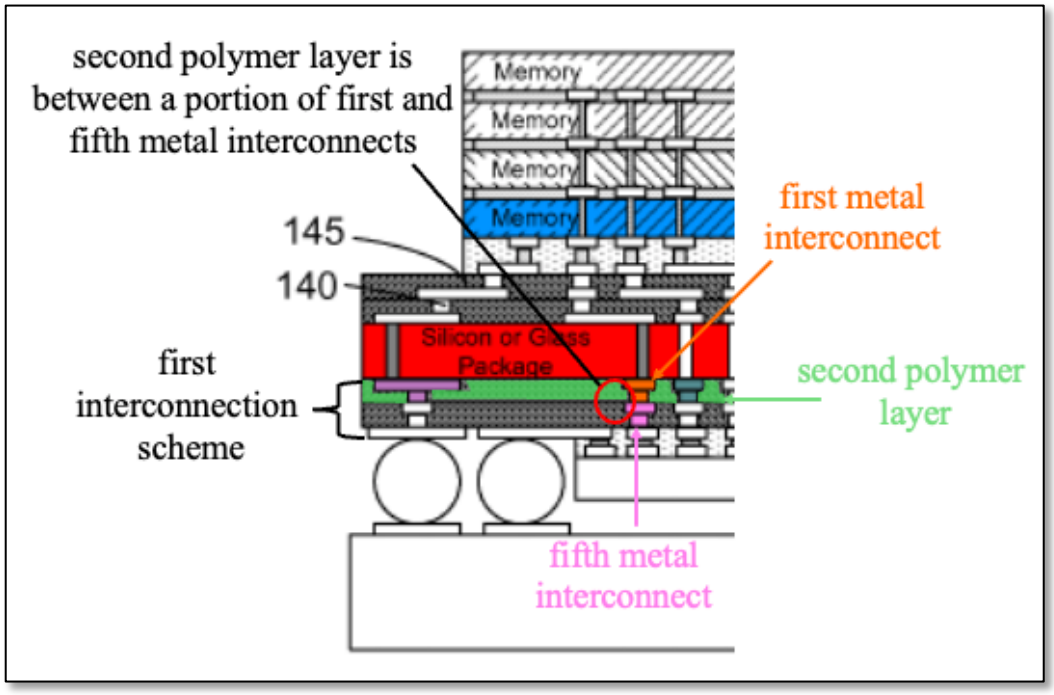
221. Alternatively, Sundaram's die pad 135 is a *fifth metal interconnect* over said *first metal interconnect* and said *second polymer layer*. The die pad 135 is a *metal interconnect* for the same reasons discussed above at Claim 3. *See* ¶ 205.



EX1004 at FIG. 3 (excerpt); ¶ 155.

2. Claim 7(b): "wherein said second polymer is between said first and fifth metal interconnects,"

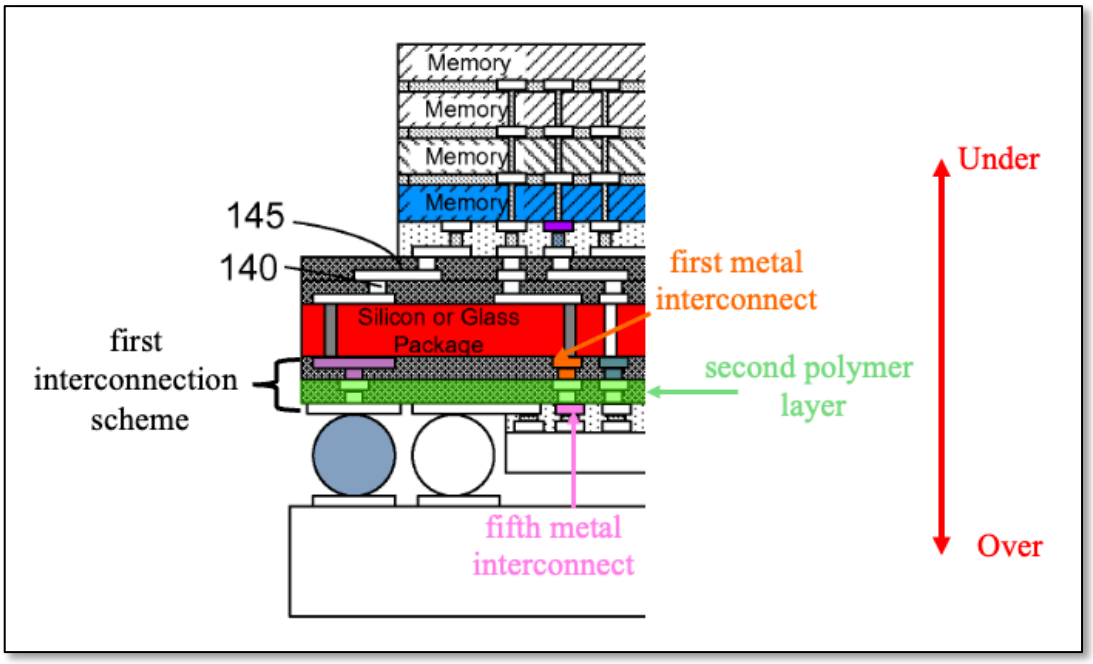
222. Sundaram's *second polymer layer*[3] is *between said first and fifth metal interconnects*, as shown:



EX1004 at FIG. 3 (excerpt); ¶ 154.

223. Alternatively, the *second polymer layer* is between said first and fifth metal interconnects, as shown:

[3] I have been instructed to interpret Claim 7(b)'s *second polymer* as referring to the *second polymer layer* introduced in Claim 1(d)(i).



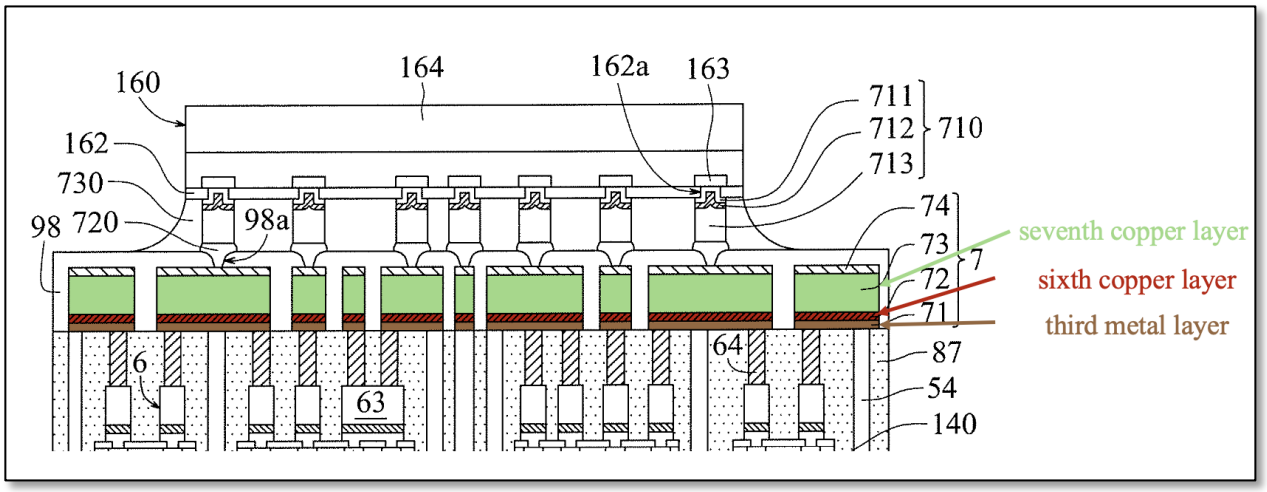
EX1004 at FIG. 3 (excerpt); ¶ 155.

3. Claim 7(c): "wherein said fifth metal interconnect comprises a third metal layer, a sixth copper layer on said third metal layer, and a seventh copper layer on said sixth copper layer."

a) Lin-191's Teachings

224. Lin-191 teaches a multilayered metal interconnect with two copper layers and a metal layer. Specifically, Lin-191 teaches a "patterned metal layer 7" having an "adhesion layer 71, the seed layer 72, the metal layer 73, and the barrier/wetting layer 74" *EX1005* at [0379]. Layer 7 interconnects metal pillars or bumps 64 to various other structures, such "metal pillars or bumps 54" in Lin-191's package and is therefore, like Sundaram's trace 145 and vias 140, a *metal interconnect*. *EX1005* at [0379]. Adhesion layer 71 is a *metal* and is thus a *third metal layer*. *EX1005* at [0260]-[0264]. Seed layer 72 is "a copper layer" on adhesion

layer 71 and is thus a *sixth copper layer on said third metal layer*. *EX1005* at [0261]-[0264]. Metal layer 73 "can be a single metal layer formed by electroplating a copper layer…on the seed layer 72" and is thus a *seventh copper layer on said sixth copper layer*. *EX1005* at [0420]. The barrier/wetting layer 74 is "a single layer of nickel…" *EX1005* at [0375].



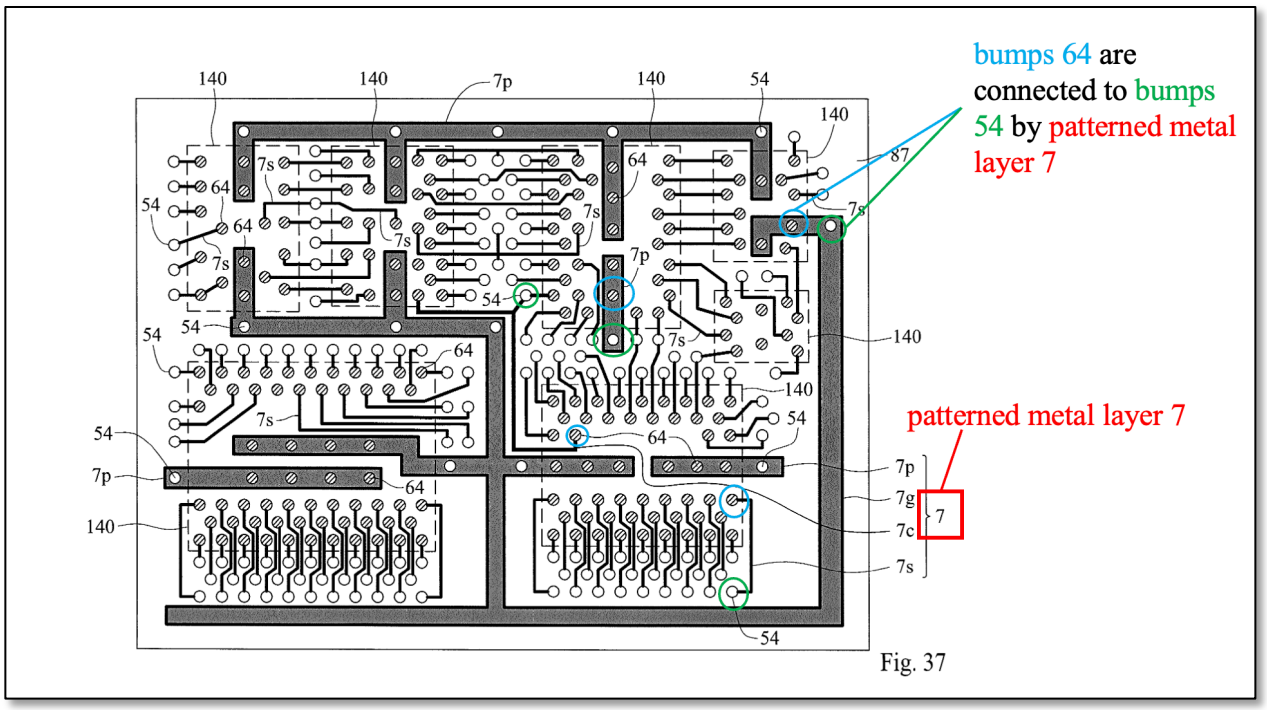
EX1005 at FIG. 72 (excerpt).

b) Motivation to Combine

225. A POSITA would have found it obvious and been motivated to modify Sundaram's *fifth metal interconnect* per Lin-191's teachings of patterned metal layer 7, thus yielding the *fifth metal interconnect compris[ing] a third metal layer, a sixth copper layer on said third metal layer, and a seventh copper layer on said sixth copper layer*.

226. As shown below in FIG. 37, Lin-191 depicts a "schematic top perspective view of the patterned metal layer 7[.]" As shown, the patterned metal

layers 7 makes lateral electrical connections (e.g., from bumps 54 (green) to bumps 64 (blue)). Several representative examples of such lateral electrical connections are annotated below. As such a POSITA would have understood layer 7 as being an RDL. Additionally, because the top view of layer 7 depicts the lateral connections achieved by patterned metal layers 7, Lin-191 thereby demonstrates the applicability to Sundaram's conductor traces 145 and blind vias 140 which likewise make lateral electrical connections (e.g., between pads in the chips to through vias 110), thus motivating the combination. *EX1004* at FIG. 3.



EX1005 at FIG. 37.

227. The modification would have predictably improved Sundaram's chip package by providing a low resistance current path for signals traveling between the

first metal interconnect and the *fifth metal interconnect*. Copper was known for its relatively low electrical resistivity and electromigration resistance. For example, it was known that "as the size and cross-sectional dimensions of electrical interconnects get smaller, resistance increases and electromigration increases. Increased resistance and electromigration are undesirable for a number of reasons. For example, increased resistance may reduce device drive current, and source/drain current through the device, and may also adversely affect the overall speed and operation of the transistor." *EX1054* at 1:39-46. Copper has a lower resistivity (1.73 x 10^{-6} ohm-cm at 20°C) compared to other materials, such as aluminum (2.824 x 10^{-6} ohm-cm at 20°C), as well as a "high immunity to electromigration, high ductility, and high melting point[,]" making it a desirable choice for interconnect material in high-density packaging. *EX1054* at 2:2-14.

228. Indeed, because copper has a relatively low electromigration rate, the risk of failures at elevated current densities is reduced. Specifically, it was known that "high current densities lead to electromigration-caused failures" in integrated circuits. *EX1055* at 1:30-32. Accordingly, a POSITA would have been motivated to choose a material, such as copper due to its lower resistivity, to reduce the risk of "electromigration-caused failures." *EX1055* at 1:30-32. Similarly, because the resistivity of copper is relatively low, the electrical conductivity is relatively high compared to other materials (e.g., aluminum). *EX1056* at [0152] ("In addition, since

the electrical conductivity of copper is higher than that of aluminum…"). It was known that in "fabricating semiconductor components, interconnects having a high electrical conductivity…provide the best performance for a signal transmission system." *EX1057* at 1:29-33.

229. Additionally, the modification would have predictably improved Sundaram's chip package by reducing the risk of delamination between the copper interconnect and the metal layers it interconnects and mitigating diffusion of copper into the metal layers it interconnects, which may negatively impact electrical reliability and ruggedness of the chip package. Specifically, the risk of delamination is reduced because the diffusion of copper out of the interconnects is mitigated by the nickel layers 71 and 74, thereby preventing physical damage to the copper interconnects that leads to delamination. Indeed, the diffusion of copper into adjacent layers is reduced by adhesion layer 71and barrier/wetting layer 74, which are both made of a "single layer of nickel[.]" *EX1005* at [0264], [0375]. As discussed, nickel was known to prevent copper diffusion into adjacent structures. *EX1040* at Abstract ("The structure comprises a layer of barrier metal, preferably nickel, that resists copper diffusion.").

230. The modification is application of a known technique (Lin-191's multi-layer interconnect) to a known device (Sundaram's *fifth metal interconnect*) ready for improvement to yield the predictable result of Sundaram's *fifth metal*

interconnect comprising the layers of Lin-191's layer 7. Further, a POSITA would have had a reasonable expectation of success because Lin-191's layer 7 and Sundaram's *fifth metal interconnect* perform the same function (interconnecting components in a chip package) and because layer 7 is formed using well-known techniques familiar to a POSITA, such as electroplating and sputtering. *EX1005* at [0414]-[0420]; *see, e.g., EX1042* at ("…filled with copper typically by an electroplating process, as known to one of ordinary skill in the art of integrated circuit fabrication."); *., EX1043* at [0032] ("The metal-containing wetting film 104 may be deposited by a variety of different deposition methods known by one of ordinary skill in the art, including but not limited to, CVD, pulsed CVD, PECVD, ALD, PEALD, or sputtering methods."). Additionally, the use of multi-layer interconnects, as demonstrated by both Lin-191 and Sundaram, among other prior art references, was commonplace, further leading to a reasonable expectation of success. *EX1005* at FIG. 84; *EX1004* at FIG. 3; *see also EX1058* at FIGS. 5-6, 8:32-40.

H. *Claim 8: "The chip package of claim 1, further comprising a second interconnection scheme under said first polymer layer and on said second surface."*

231. Sundaram teaches "polymer-metal redistribution layers" are "deposited **on the first side 115** and second side 120 of the interposer 105." *EX1004* at 6:62-67. Die pads 135 are also formed on the first side 115 (*second surface*). Thus, for

the same reasons discussed above at claim 1(c) for the *first interconnection scheme*, Sundaram further teaches a *second interconnection scheme*. *See* ¶ 150. The RDL and die pads 135 on first side 115 is *a second interconnection scheme under said first polymer and on said second surface* because the traces 145 and vias 140 in the RDL "connect" the "electronic devices" 125 and 130 and because die pads 135 "electrically connect devices[]." *EX1004* at 6:62-67, 6:29-31.

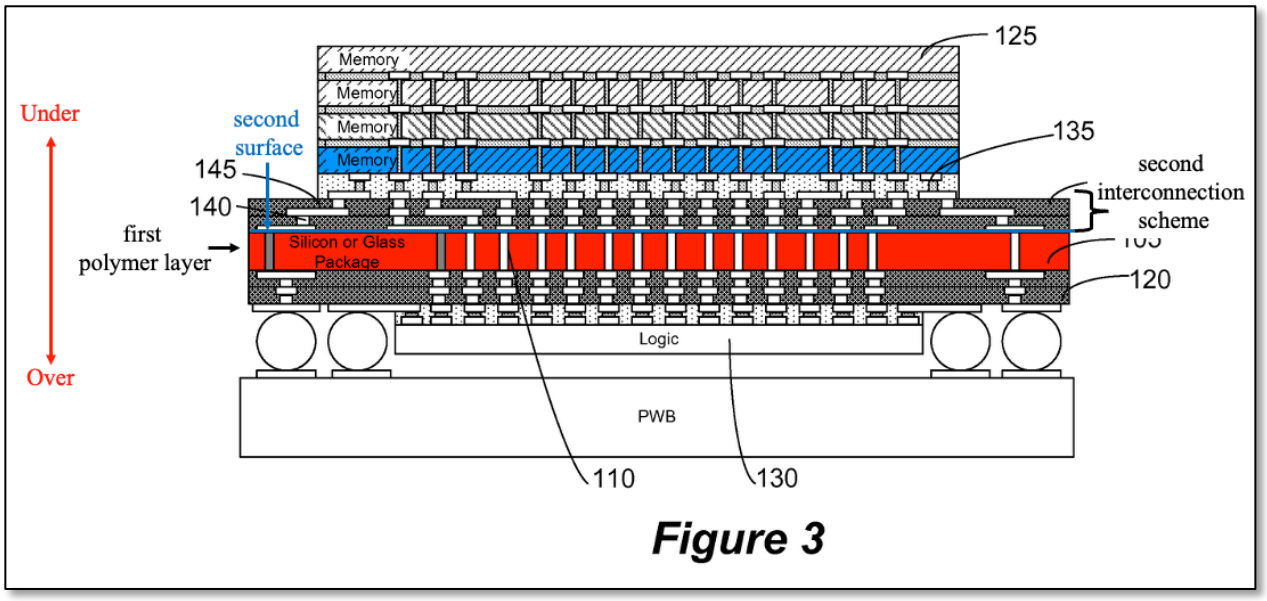


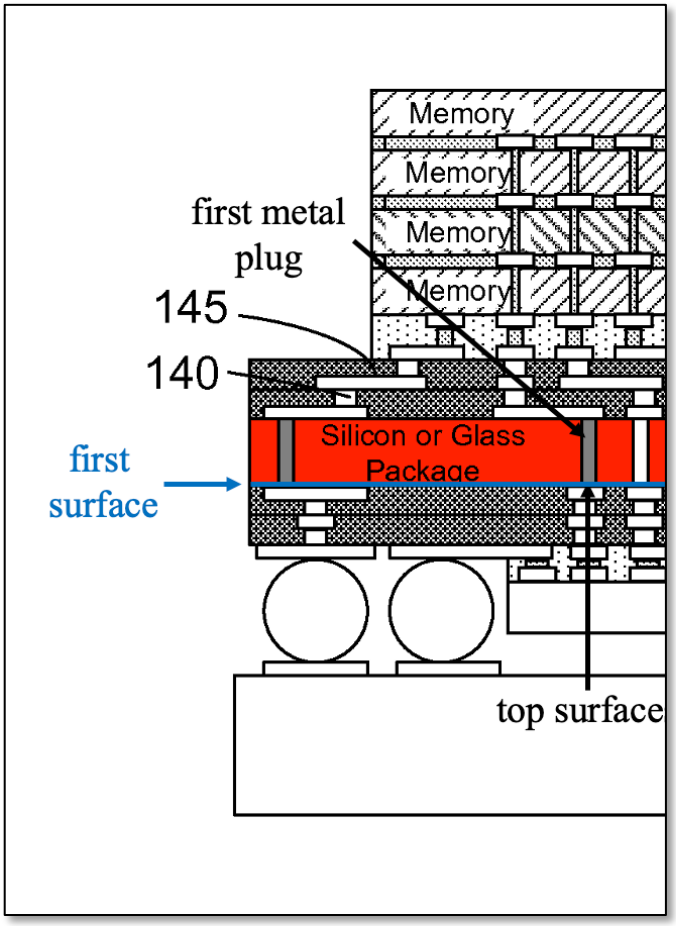
Figure 3

EX1004 at FIG. 3.

I. *Claim 9: "The chip package of claim 1, wherein said first metal plugs has a top surface substantially coplanar with said first surface."*

232. As discussed, Sundaram teaches the "each of the through vias 110" (*first metal plug[s]*) "extends from the first side 115 to the second side 120 of interposer 105[,]" meaning that the through vias 110 have end surfaces that are coplanar with the surfaces of interposer 105. *EX1004* at 6:6-9. Thus, as shown

below, Sundaram *teaches wherein said first metal plugs has a top surface substantially coplanar with said first surface*:



EX1004 at FIG. 3 (excerpt).

J. *Claim 10: "The chip package of claim 1, wherein said first metal pad is an aluminum pad."*

233. Sundaram alone or Sundaram-Lin-191 teaches a *first metal pad*. *See* ¶¶ 181-185. Lin-191, likewise, teaches metal pads 163 that "include **aluminum**." *EX1005* at [0384]. Lin-191 teaches specifically an aluminum metal pad such that a

POSITA would have found it obvious and been motivated to apply Lin-191's aluminum pad teachings to Sundaram's *first metal pad*.

a) Motivation to Combine

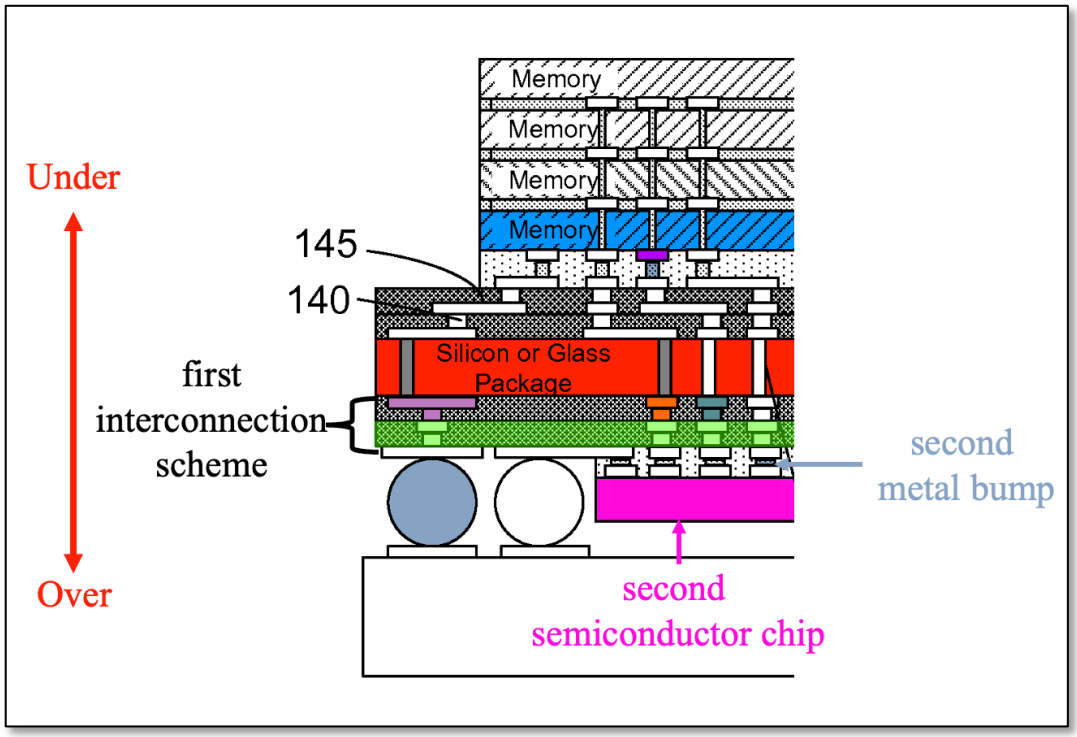
234. A POSITA would have found it obvious and been motivated specifically to implement Sundaram's *first metal pad* as an *aluminum pad* at least because aluminum was a well-known, cost effective, and widely used material for forming contact pads in chips, because it is compatible with established bond wire attachment methods, is consistent with legacy materials used in semiconductor processing, and because methods of forming such aluminum pads were well known. *See, e.g., EX1059* at 3:65–4:2 ("Aluminum is the metal of choice for…bond pad metal in IC devices because of its superior electrical and thermal conductivity, low cost, wire-bondability, and other performance and reliability factors."); *EX1061* at [0012] ("Materials that are commonly used for bond pads include…aluminum[.]"), [0013] ("The conventional processing sequence that is used to create an aluminum bond pad starts with a semiconductor surface…. A layer of Intra Metal Dielectric (IMD) is deposited over the surface, a layer of metal, typically aluminum, is deposited over the surface of the layer of IMD. The layer of metal is patterned and etched typically using a layer of photoresist and conventional methods of photolithography and etching."). The modification is the combination of prior art elements (aluminum pads, chip packages) according to known methods to yield

predictable results i.e., Sundaram's *first metal pad* being made of aluminum. Because aluminum was such a well-known material and because methods of forming aluminum pads were well-known, a POSITA would have had a reasonable expectation of success.

K. *Claim 11*

1. Claim 11(a): "The chip package of claim 1, further comprising a second semiconductor chip over said first interconnection scheme and connected to said first interconnection scheme through a second metal bump"

235. As discussed, Sundaram's second electronic device 130 is a *second semiconductor chip over said first interconnection scheme*. *See* ¶ 208, incorporated herein.

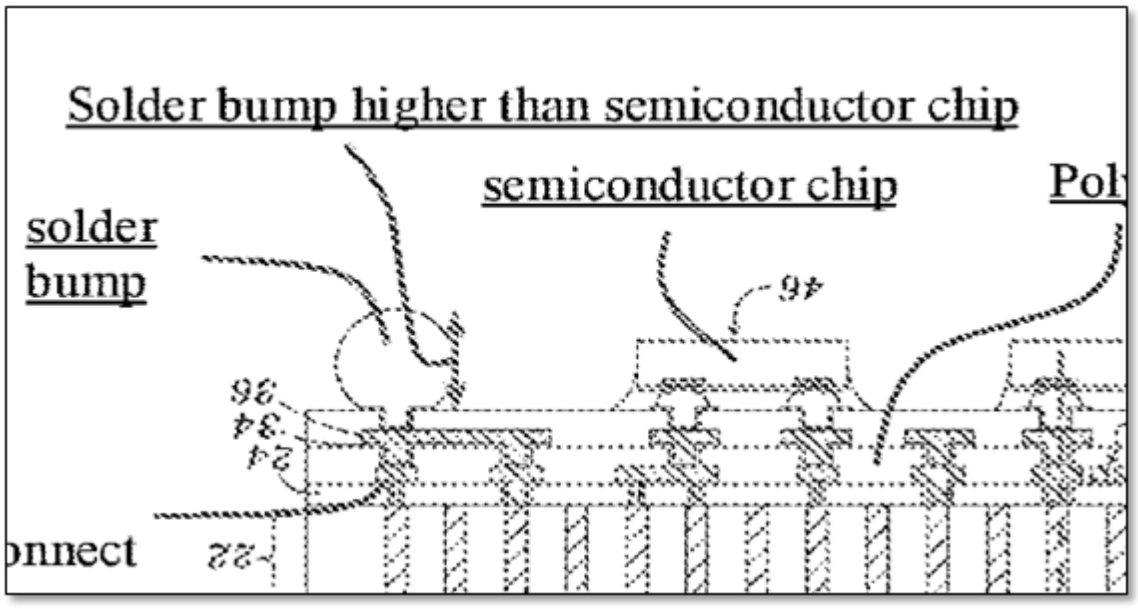


EX1004 at FIG. 3.

236. Further, second electronic device 130 is *connected to said first interconnection scheme through a second metal bump*, as shown in the above figure. *See* ¶ 209, incorporated herein. Indeed, Sundaram teaches "die pads 135…can electrically connect devices using solder, copper bumps with solder caps, copper to copper bonding." *EX1004* at 6:29-33.

2. Claim 11(b): "wherein said second semiconductor chip has a height is between a backside surface of said second semiconductor chip and a top surface of said second polymer layer is smaller than a thickness of said first metal bump."

237. I note that during prosecution of the '768 Patent, the Patent Owner provided an annotated figure arguing support for *a height is between a backside surface of said second semiconductor chip and a top surface of said second polymer layer is smaller than a thickness of said first metal bump*, as shown below.



EX1002 at p. 400.

a) Sundaram's Teachings

238. The *first polymer layer* includes at least the portion described above at Claim 1(c)(i) and further includes the portion highlighted below. *See* ¶ 154. Thus, as shown in FIG. 3, below, Sundaram's device 130 (*second semiconductor chip*) *has a height [that] is between a backside surface of* device 130 *and a top surface of* Sundaram's *first polymer layer*, which is *smaller than thickness* of Sundaram's solder ball (*first metal bump*).

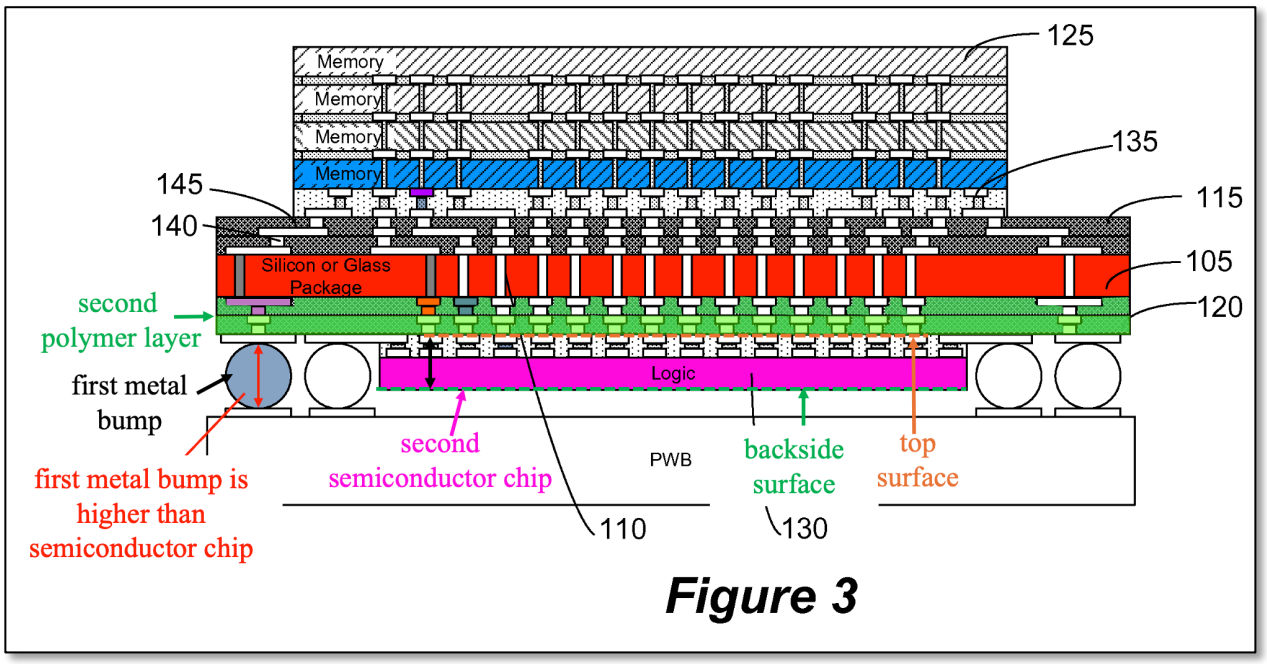


Figure 3

EX1004 at FIG. 3; ¶ 154.

239. Alternatively, Sundaram's *first polymer layer* is as annotated below, which also meets the claim limitation. *See* ¶ 155.

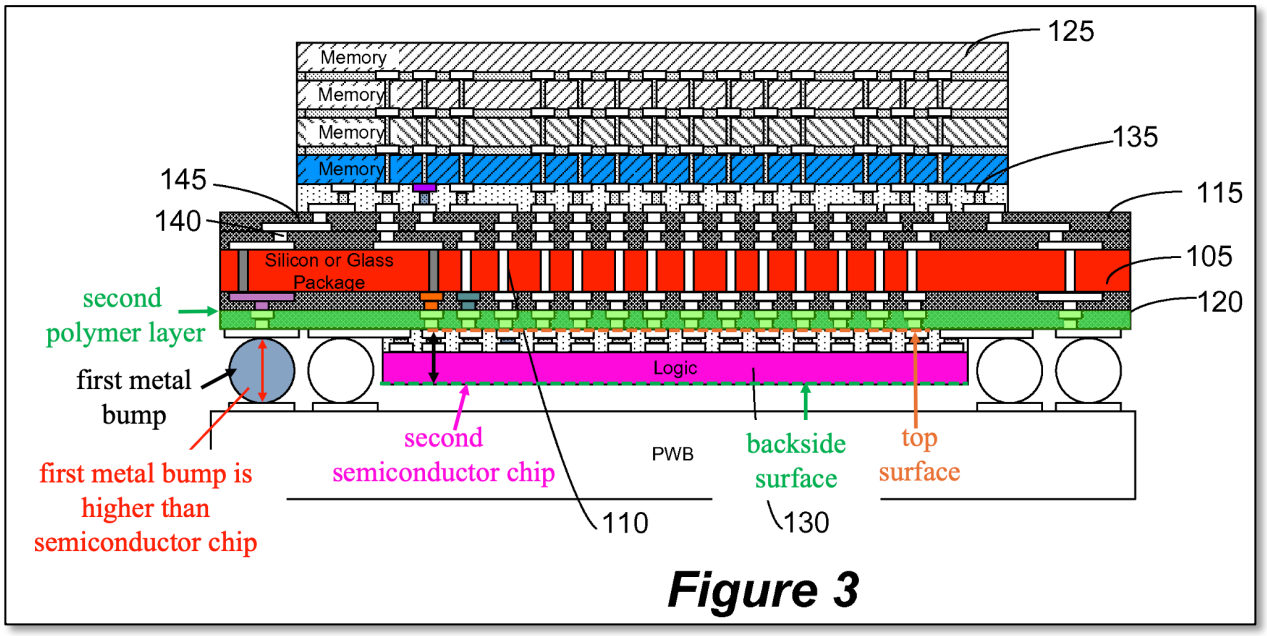


Figure 3

EX1004 at FIG. 3.

L. *Claim 12*

1. Claim 12(a): "The chip package of claim 1, further comprising a second semiconductor chip under said first semiconductor chip,"

240. As shown below, another chip in Sundaram's chip stack 125 is a *second semiconductor chip*. As such, Sundaram teaches a *second semiconductor chip under said first semiconductor chip*. Sundaram's "first electronic device 125 can be…stacked memory IC devices[,]" thus yielding the *second semiconductor chip under said first semiconductor chip*. *EX1004* at 6:37-39.

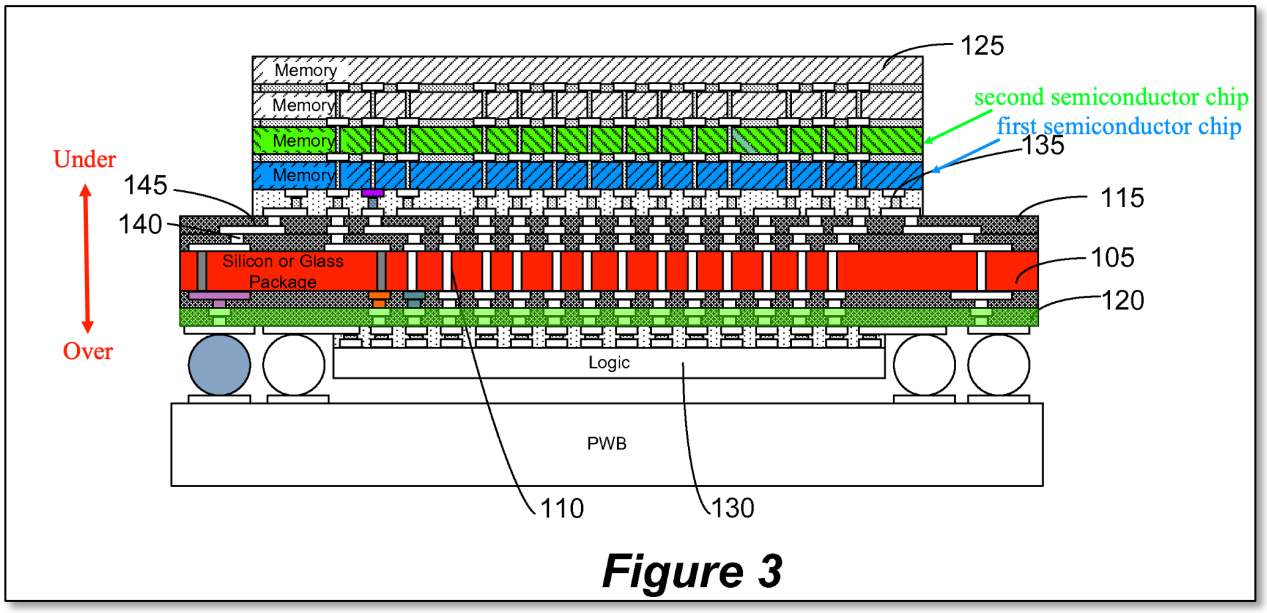


Figure 3

EX1004 at FIG. 3.

2. Claim 12(b): "wherein said first semiconductor chip comprises a second metal pad connected to a third metal pad of said second semiconductor chip through a solder layer, wherein said solder layer between said first and second semiconductor chips."

241. FIG. 32 depicts the *second metal pad* of a first semiconductor chip *connected to a third metal pad* of a *second semiconductor chip*.

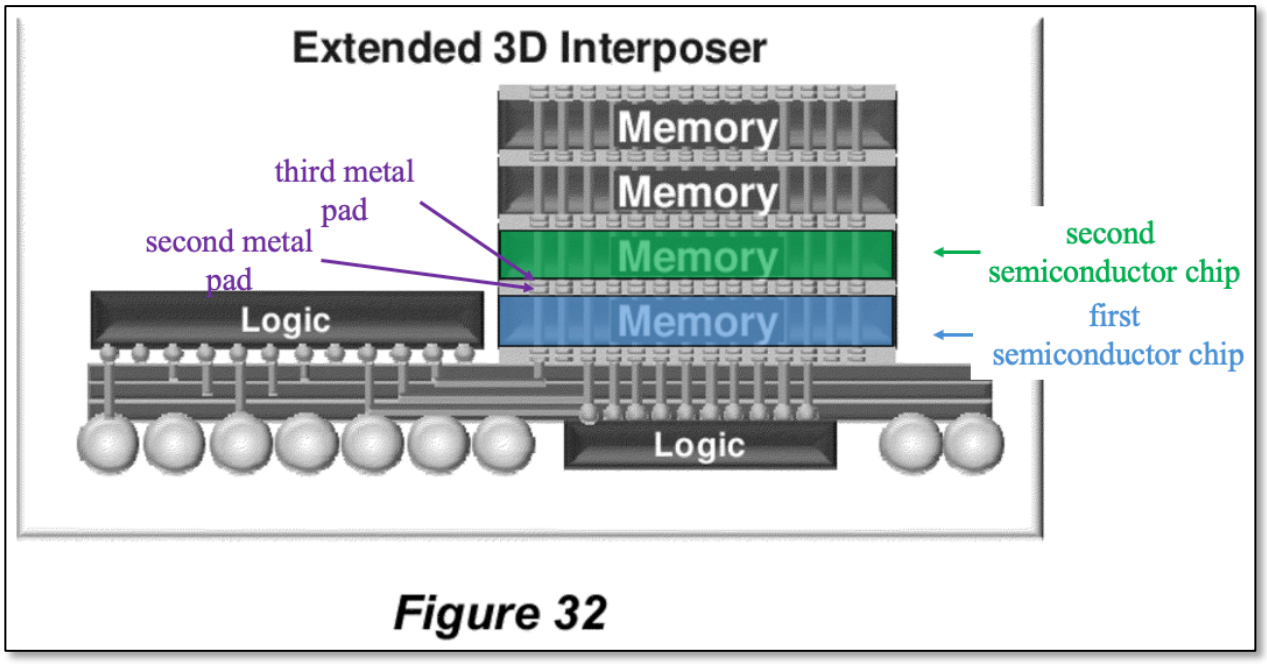


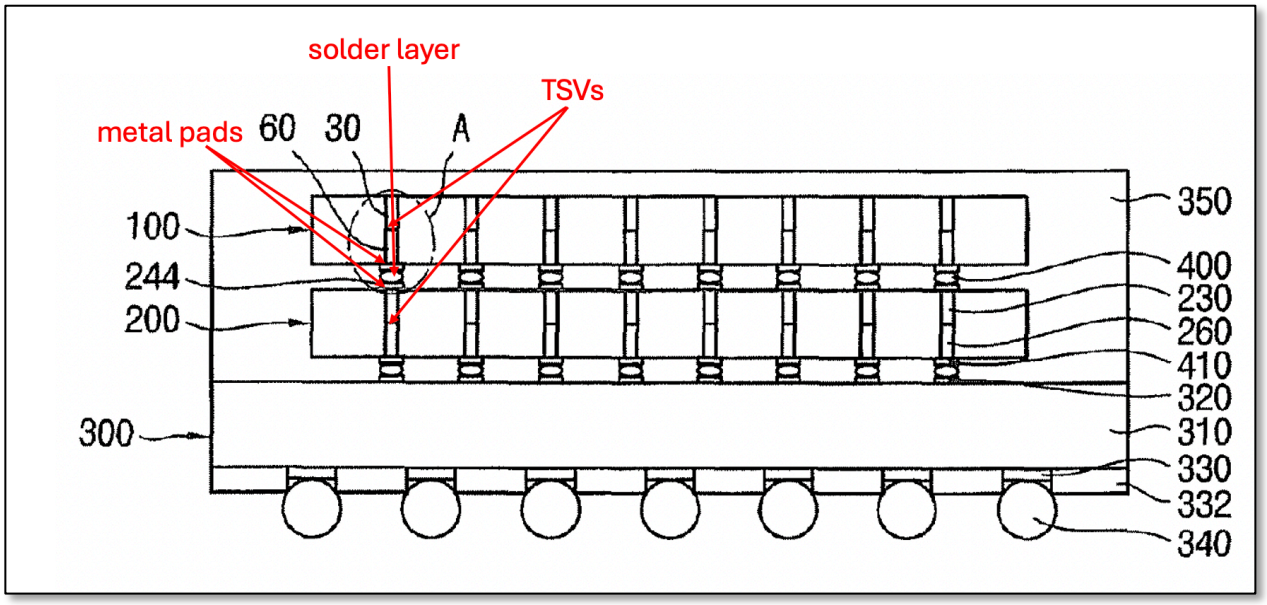
Figure 32

EX1004 at FIG. 32.

242. A POSITA would have been motivated and found it obvious to modify Sundaram's FIG. 3 embodiment so that each chip has top and bottom pads connected to one another as each chip must include pads on its surface to provide connection to other electrical components in the chip package, which would have been an obvious, ubiquitous implementation detail. In doing so, the chip stack of FIG. 3 is modified such that the *first semiconductor chip* has a *second metal pad connected to a third metal pad of* FIG. 3's *second semiconductor chip*. Indeed, semiconductor chips were regularly manufactured with metal pads formed on the periphery. *EX1095* at ("I/O terminals were **traditionally** formed by way of **metal pads** along the periphery of an IC."). Because the standard method of manufacturing chips included forming metal pads along the periphery, a POSITA would have found it

obvious to include metal pads on either surface of each chip in the chip stack of FIG. 3., thereby ensuring electrical communication via such I/O terminals. For the same reason, i.e., because that is how chips were formed, a POSITA would have had a reasonable expectation of success.

243. Sundaram further teaches that "die pads 135 … can electrically connect devices using solder, copper bumps with solder caps …." *EX1004* at 6:29–34. A POSITA would have understood chip pads on devices 125, 130 likewise electrically connect using solder because connecting metal pads using solder bumps was standard practice. For example, Lee depicts a chip stacking in which each chip has its own set of metal pads connecting TSVs through a solder layer:



EX1126 at FIG. 2, 6:16-22, 7:40-42.

244. A POSITA would have found it obvious, been motivated, and had a reasonable expectation of success in combining Sundaram's internal embodiments such that the *first semiconductor chip comprises a second metal pad connected to a third metal pad of said second semiconductor chip through a solder layer, wherein said solder layer between said first and second semiconductor chips*.

245. A POSITA would have recognized that including a solder layer between the metal pads of Sundaram's chip stack would have provided the benefit of self-alignment, thereby reducing the risk of misalignment between the metal pads of the chips. Indeed, it was known when forming metal bumps, "self-alignment" occurs which is "such an effect that the electronic component is lifted by surface tension and stress of the molten solder, and then self-aligns itself on the mounted position on the board by restitution from the stress." *EX1083* at [0003]. A POSITA would have had the knowledge and skillset to successfully implement such solder layers between the metal pads, including any necessary corresponding changes, such as implementing an underfill material which was standard, well-established practice. Additionally, a POSITA would have recognized the modification would have been standard practice, as the alternative to solder-based interconnection between stacked chips was bumpless Cu-Cu hybrid bonding. Bumpless pad-to-pad bonding required more expensive high precision processing to obtain ultra-flat, ultra-clean copper interfaces, and was only used for applications requiring extremely high I/O density.

246. As such, a POSITA would have been motivated to achieve such a benefit (self-alignment) by connecting the *second metal pad* to the *third metal pad* through a *solder layer between said first and second semiconductor chips* The modification is the combination of known prior art elements (solder connections for chip pads) according to known methods to yield predictable results. The modification would have advantageously provided Sundaram with a good electromechanical connection between chips, which would have had a reasonable expectation of success because such was a common method of connecting chips, as described above. *See* ¶ 243; *see also EX1113* at FIG. 3G, [0032]-[0033]. Further, Sundaram already teaches forming solder layers (i.e., "copper bumps with solder caps"), further leading to a reasonable expectation of success. *EX1004* at 6:29-34.

M. *Claim 13*

1. Claim 13(a): "The chip package of claim 1, further comprising a second semiconductor chip under said first semiconductor chip,"

247. *See* Claim 12(a), ¶ 240, incorporated herein.

2. Claim 13(b): "wherein said first semiconductor chip comprises a second metal pad on a top surface of said first semiconductor chip, a third metal pad on a bottom surface of said first semiconductor chip"

248. *See* Claim 6(a), ¶¶ 214-216, incorporated herein.

3. Claim 13(c): "and a through-silicon-via metal layer connects to said second metal pad,"

249. *See* Claim 6(b), ¶¶ 217-219, incorporated herein. Because the *TSV metal layer* connects the *second metal pad* to the *third metal pad*, the *through-silicon-via metal layer connects to said second metal pad*.

4. Claim 13(d): "wherein said third metal pad is connected to a fourth metal pad of said second semiconductor chip."

250. Shown below, Sundaram's *chip package* has a *third metal pad connected to a fourth metal pad of said second semiconductor chip*. Additionally, Sundaram alone or Sundaram-Lin-191 expressly teach the pads being *metal*. *See* ¶¶ 181-185.

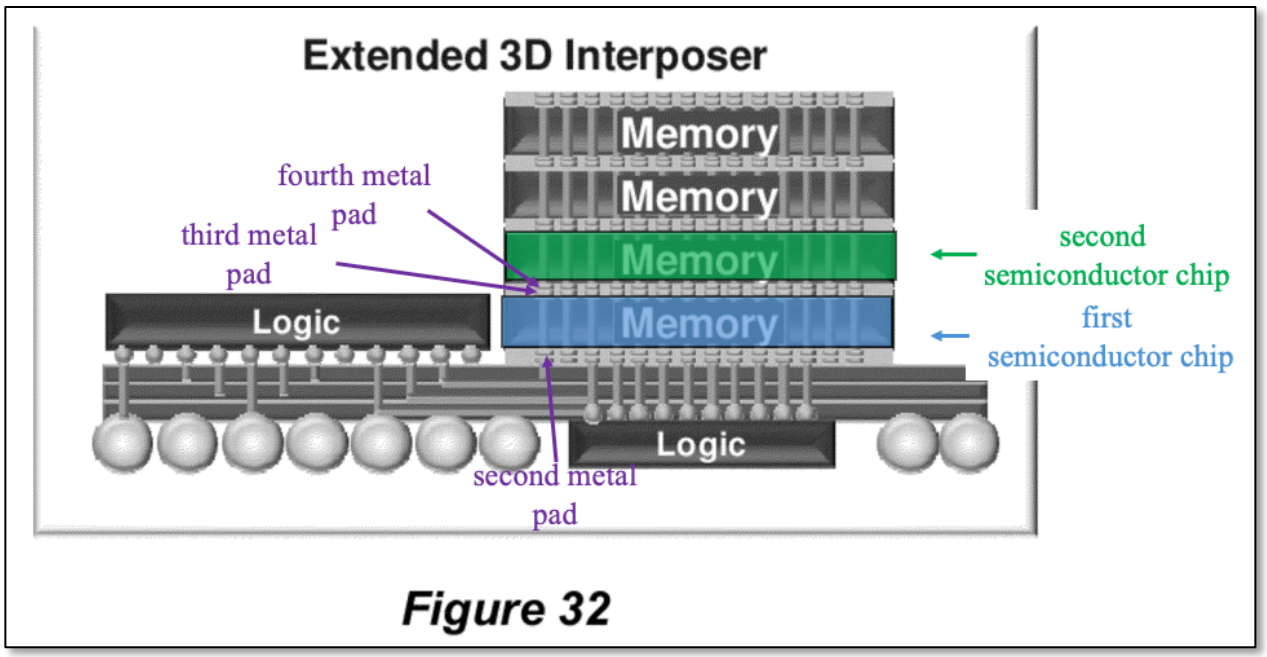


Figure 32

EX1004 at FIG. 32.

251. A POSITA would have found it obvious, been motivated, and had a reasonable expectation of success in combining Sundaram's internal embodiments

so that the *third metal pad* is *connected to a fourth metal pad of the second semiconductor chip*, thereby vertically interconnecting the two chips. The MTCs and reasonable expectation of success from Claim 12(b) are incorporated herein. *See* ¶¶ 244-245.

N. *Claim 14: "The chip package of claim 1, further comprising a third metal plug vertically in a third through via in said first polymer layer, wherein a pitch between said first and third metal plugs is between 200 and 1000 micrometers."*

a) Sundaram's Teachings

252. Shown below, Sundaram teaches *a third metal plug vertically in a third through via in said first polymer layer*, namely a third of through vias 110.

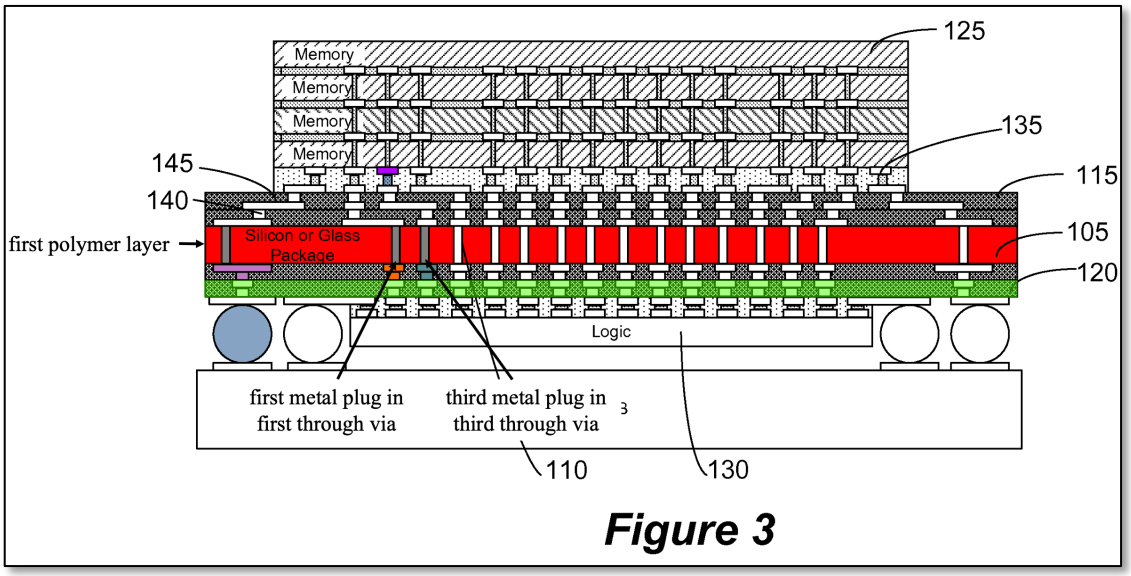


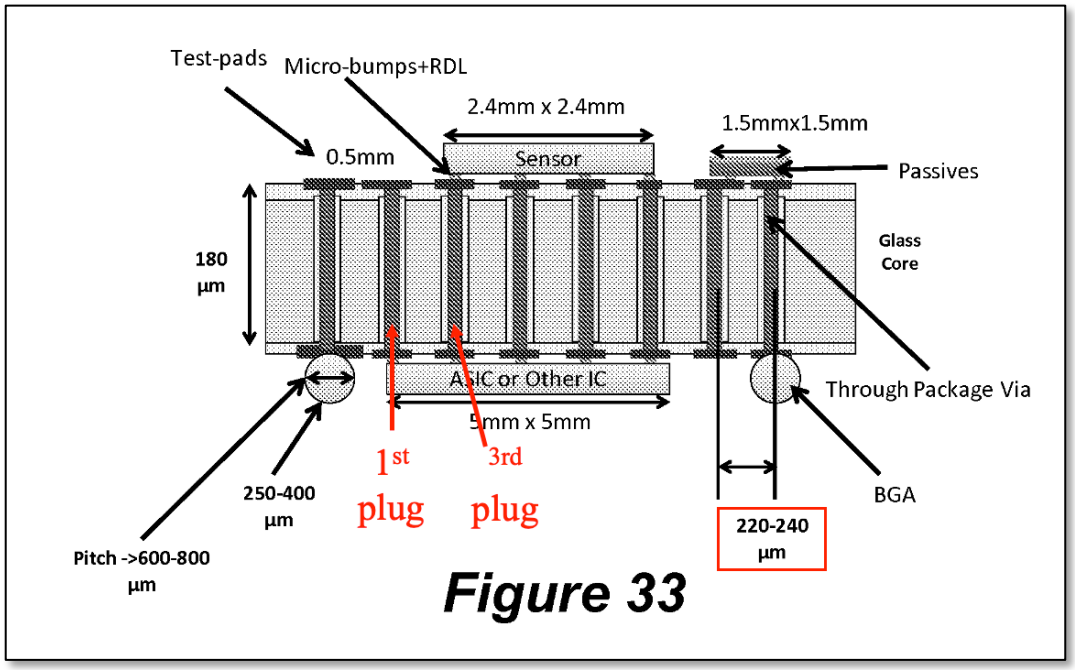
Figure 3

EX1004 at FIG. 3.

253. Sundaram, with respect to FIG. 33, Sundaram teaches through vias having a pitch "220-240 μm[.]" *EX1004* at FIG. 33. As shown, like interposer 105

in FIG. 3, the interposer of FIG. 33 similarly comprises *first* and *third plug[s]* that are adjacent to each other. Because the *pitch* between the *first* and *third plug[s]* is "220-240 µm," Sundaram teaches or renders obvious the claimed range of *between 200 and 1000 micrometers*. *EX1004* at FIG. 33.

254. FIG. 33 is a specific example of a chip package for "a digital camera for cell phones" with a "through-via interconnect density" that is "substantially the same" as "the first electronic device 125 or the second electronic device 130 it connects." *EX1004* at 6:42-50.



EX1004 at FIG. 33.

255. In my opinion, the '768 Patent does not ascribe any criticality the claimed pitch of *between 200 and 1000 micrometers*. That is, the '768 Patent does

not provide the range of 200-1000 micrometers and then further provide an explanation for why such range is needed, important, or advantageous. Indeed, the '768 Patent describes a variety of ranges, including smaller (between 5 and 20 micrometers) and larger (between 500 and 10,000 micrometers), indicating to a POSITA that the thickness can vary widely and that the thickness is not otherwise critical. See *EX1001* at 6:7-15.

b) Motivation to Combine

256. To the extent PO argues Sundaram's FIGS. 3 and 33 are separate embodiments, a POSITA would have found it obvious and been motivated to modify the pitch of Sundaram's through vias 110 (*plurality of copper plugs*) according to the FIG. 33 embodiment such that a *pitch between said first and third copper plugs is between 200 and 1000 micrometers*. The modification is expressly motivated by Sundaram because FIG. 33 enables high bandwidth speeds such as "at least about 10 GB/s" between "an image sensor chip" and an "Asic chip" in a "digital camera for cell phones." *EX1004* at 6:42-45. As acknowledged by Sundaram, a POSITA would have recognized that there was a need "for logic to memory bandwidth (BW) at increasing levels without an increase in power consumption." *EX1004* at 1:22-24. Thus, a POSITA would have been motivated to implement a *pitch between said first and third copper plugs* of *between 200 and 1000 micrometer* to achieve such "high bandwidth speeds." *EX1004* at 6:42-45. The combination is the application of a

known technique (Sundaram's copper plugs having a pitch between *200 and 1000 micrometers*) to a known device (Sundaram's chip package) ready for improvement to yield predictable results. A POSITA would have a reasonable expectation of success at least because the modification would have been simple and straightforward as methods of controlling pitch of copper plugs were well-known and because such a structure was already taught by Sundaram. *EX1004* at FIG. 33.

O. *Claim 15: "The chip package of claim 1, wherein said first metal plug has a thickness between 100 and 300 micrometers."*

257. Sundaram teaches or renders obvious *wherein said first metal plug has a thickness between 100 and 300 micrometers*. As discussed, Sundaram's interposer 105 has a *thickness between 100 and 300 micrometers*. *See* ¶ 133. Sundaram further teaches "through vias 110 can be defined within the interposer 105 such that each of the through vias 110 extends from the first side 115 to the second side 120[.]" *EX1004* at 6:6-9. Because through vias 110 extend from the *first surface* and *second surface* of interposer 105 (*first polymer layer*), through vias 110 (*first metal plug*) have a thickness equal to that of the *first polymer layer* i.e., "20 to about 200 micrometers" which teaches or renders obvious *between 100 and 300 micrometers*. *EX1004* at 2:24-28, FIG. 3.

258. In my opinion, the '768 Patent does not ascribe any criticality the claimed plug thickness of *between 100 and 300 micrometers*. I first note that the Applicant during examination of the'768 Patent stated that the plug thickness is the

same as substrate 20's thickness. *See EX1002* at 535-537. I also note my discussion at ¶ 134 that the '768 Patent does not ascribe any criticality to the claimed substrate thickness. Therefore, because (i) the Applicant stated that the plug thickness was the same as the substrate thickness, and (ii) the '768 Patent does not indicate the substrate thickness is critical, then it is my opinion the plug thickness recited in Claim 15 similarly is not critical.

P. *Claim 20: "The chip package of claim 16, wherein said first polymer layer has a coefficient of expansion between 3 and 10 ppm/°C."*

259. *See* Claim 1(a)(iii), ¶¶ 135-141, incorporated herein.

IX. OPINIONS REGARDING GROUND 1B: 16-19 AND 21-28 ARE OBVIOUS OVER SUNDARAM AND LIN-191

A. *Claim 16*

1. 16(Pre): "A chip package comprising"

260. *See* Claim 1(Pre)[4], ¶ 129, incorporated herein.

[4] I note that numerous claim limitations of later claims are the same or substantially the same as claim limitations from earlier claims. For examples, Claim 16(Pre) is substantially the same as Claim 1(Pre). For each claim limitation that is the same or substantially the same as an earlier claim limitation, I provide a cross-reference citation to my opinions for the earlier claim limitation, which should be understood to incorporate by reference for the later claim limitation.

2. 16(a): "a first polymer layer having a first surface and a second surface opposite to said first surface,"

261. *See* Claim 1(a), ¶¶ 130-131, incorporated herein.

3. 16(a)(i): "wherein said first surface is substantially parallel to said second surface,"

262. *See* Claim 1(a)(i), ¶ 132, incorporated herein.

4. 16(a)(ii): "wherein said first polymer layer has a thickness between 100 and 300 micrometers;"

263. *See* Claim 1(a)(ii), ¶ 133, incorporated herein.

5. 16(b): "a first metal plug vertically in a first through via in said first polymer layer,"

264. *See* Claim 1(b), ¶ 144, incorporated herein.

6. 16(b)(i): "wherein said first metal plug comprises a first copper layer, wherein the first copper layer contacts with a sidewall of said first through via;"

265. *See* Claim 1(b)(i), ¶¶ 145-145, incorporated herein.

7. 16(c): "a second metal plug vertically in a second through via in said first polymer layer,"

266. *See* Claim 1(c), ¶ 147, incorporated herein.

8. 16(c)(i): "wherein said second metal plug comprises a second copper layer,"

267. *See* Claim 1(c)(i), ¶ 148, incorporated herein.

9. 16(c)(ii): "wherein a top surface of said second metal plug and a top surface of said first metal plug are in the same horizontal plane;"

268. *See* Claim 1(c)(ii), ¶ 149, incorporated herein.

10. 16(d): "a first interconnection scheme over said first surface,"

269. *See* Claim 1(d), ¶ 150, incorporated herein.

11. 16(d)(i): "wherein said first interconnection scheme comprises a first metal interconnect over said first surface, a second metal interconnect over said first surface and a second polymer layer over said first and second metal interconnects,"

270. *See* Claim 1(d)(i), ¶¶ 153-155, incorporated herein. For Claim 16, I map a different blind via 140 and conductor trace 145 as the *second metal interconnect*.

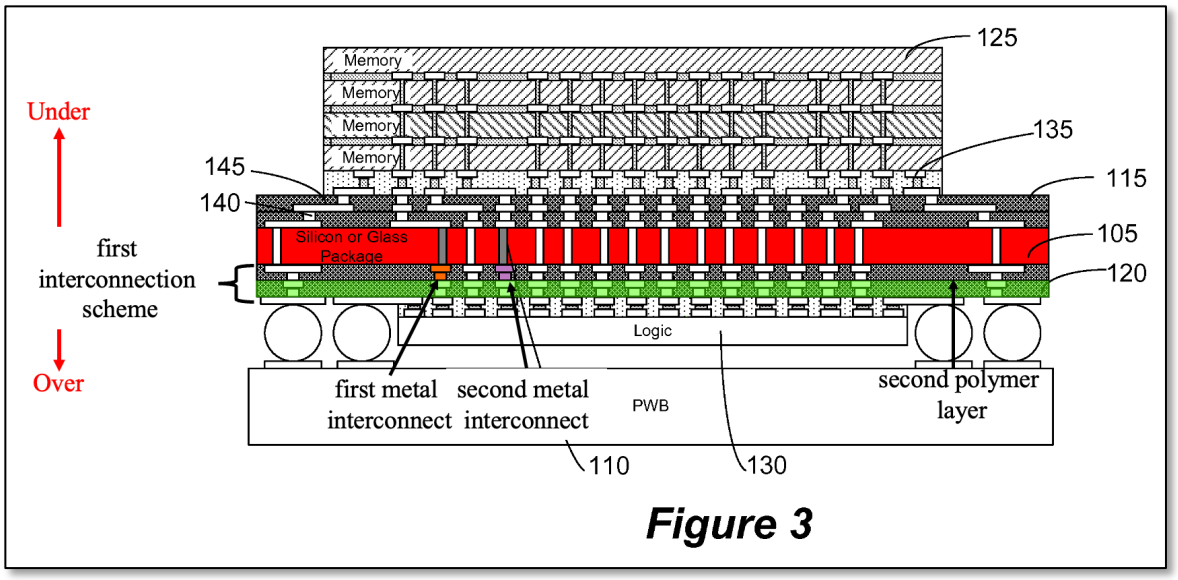


Figure 3

EX1004 at FIG. 3.

12. 16(d)(ii): "wherein said first metal interconnect is connected to said first metal plug,"

271. *See* Claim 1(d)(ii), ¶ 158, incorporated herein.

13. 16(d)(iii): "wherein said first metal interconnect comprises a first metal layer, a third copper layer on said first metal layer, and a fourth copper layer on said third copper layer;"

272. *See* Claim 1(d)(iii), ¶¶ 159-170, incorporated herein.

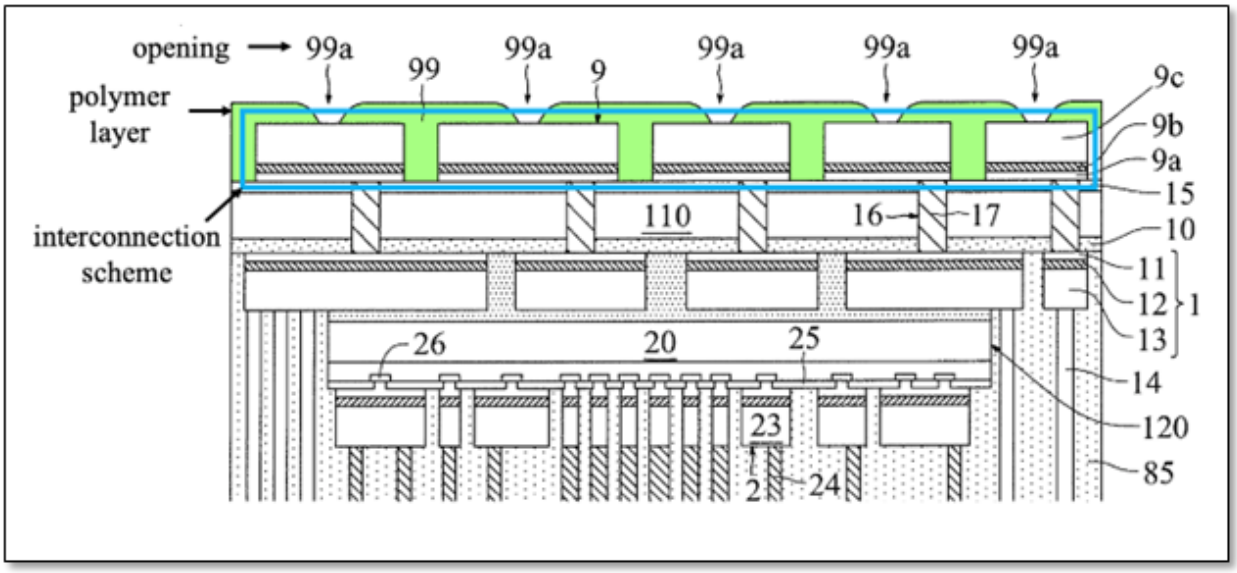
14. 16(e): "a first metal bump over said first interconnection scheme,"

273. *See* Claim 1(e), ¶ 171, incorporated herein.

15. 16(e)(i): "wherein said first metal bump is connected to said first interconnection scheme through a first opening in said second polymer layer,"

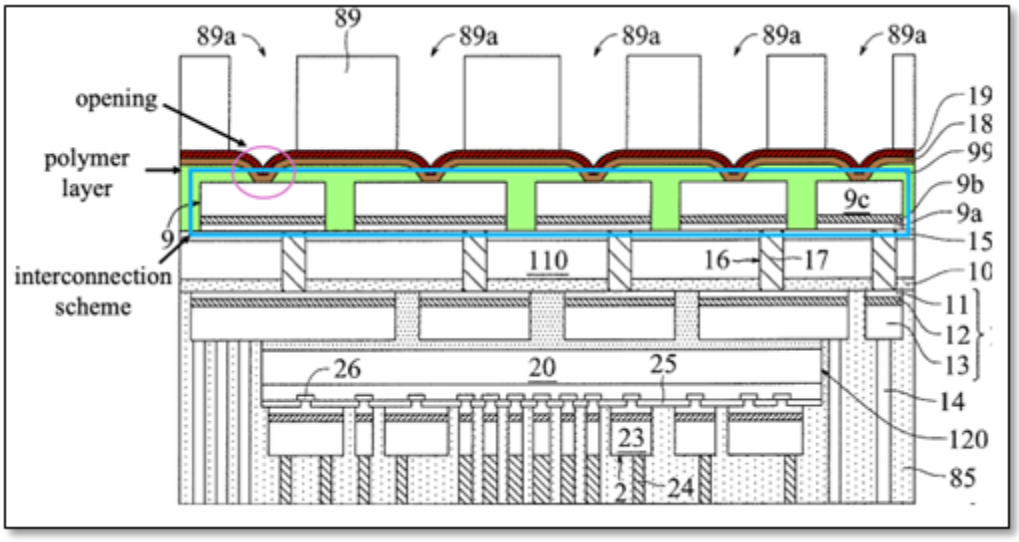
a) Lin-191's Teachings

274. Lin-191 teaches a *metal bump* that is *connected* to an *interconnection scheme through a first opening* in a *polymer layer*. Specifically, Lin-191 teaches solder bumps or balls 29a having a UBM layer that is formed in "openings 99a" of "polymer layer 99." *EX1005* at [0306]-[0324]. Specifically, as shown below, Lin-191's multi-chip module comprises a "patterned metal layer 9" that is, like patterned metal layer 3 described above, an *interconnection scheme*. Indeed, patterned metal layer 9 connects solder bumps or balls 29a to patterned metal layer 1, thus functioning as an *interconnection scheme*. *EX1005* at [0326], FIG. 52. A "polymer layer 99" is formed "on the metal layer 9c of the metal layer 9c of the patterned metal layer 9" then the polymer layer 99 is "patterned…to form multiple openings 99a" thereby "exposing multiple contact points of the metal layer 9c[.] *EX1005* at [0306]. The openings 99a in the polymer layer 99 are shown below:

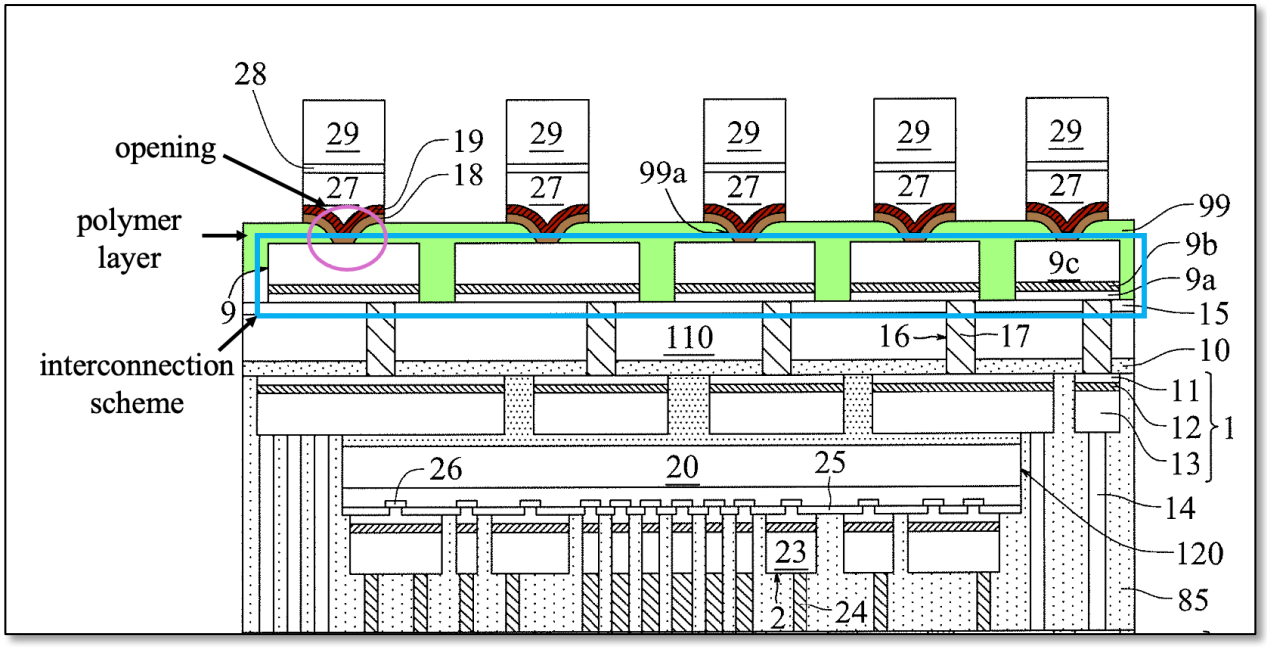


EX1005 at FIG. 48 (excerpt).

275. An "adhesion layer 18…can be formed on the contact points of the metal layer 9c" then a "seed layer 19" is formed on adhesion layer 18. *EX1005* at [0307]. The UBM layer is completed by the formation of metal layer 27 and metal layer 28. *EX1005* at [0314]-[0318], [0323]. Solder bumps or balls 29a are formed by forming a solder layer 29 then reflowing to form the "multiple solid solder bumps or balls 29a." *EX1005* at [032], [0324].



EX1005 at FIG. 49 (excerpt).



EX1005 at FIG. 51 (excerpt).

276. Lin-191's solder bumps or balls 29a are connected to the patterned metal layer 9 (*interconnection scheme*) through the UBM layer. As such, Lin-191 teaches a *metal bump* that is *connected to* an *interconnection scheme through a first opening* (one of openings 99a) in a *polymer layer*.

b) Motivation to Combine

277. A POSITA would have found it obvious and been motivated to modify Sundaram's *first metal bump* to connect to the *first interconnection scheme* through a *first opening in said second polymer layer* based on the teachings of Lin-191. A POSITA would have recognized that the modification would have advantageously improved the mechanical connection between Sundaram's metal bump and the

interconnection scheme because, UBM layers (such as Lin-191's UBM layer) were known to "improve the adhesive strength of solder balls" and to "prevent[] diffusion of unnecessary substances" of solder balls into nearby substrates. *EX1037* at 5:3-5. Further, it was known that when forming recessed bump pads, "the recessed areas of the bump pads are surrounded by the peripheral barriers, thus the embedded, recessed bump bads having peripheral barriers can avoid immersion Sn or solder balls formed on the recessed areas from overflowing, thereby avoiding short circuiting." *EX1114* at [0036].

278. Thus, a POSITA would have recognized that modifying Sundaram to use a UBM layer formed in an opening in Sundaram's *second polymer layer* to electrically connect the *first metal bump* to Sundaram's conductor traces 140 and blind vias 140 would have predictably improved the mechanical connection and avoided short circuiting issues associated with solder ball formation. The modification is the application of a known technique (Sundaram's solder balls connecting through a polymer layer opening) to a known component (Sundaram's chip package) to yield the predictable results of Sundaram's *first metal bump* being connected to the *first interconnection scheme through a first opening in said second polymer layer*.

279. Additionally, Lin-191 teaches well known methods of forming the connection through an *opening* in the *polymer layer*. Specifically, openings in

polymer layers may be formed by "processes of lithographic, light exposure with a 1x stepper" and the UBM layers 18, 19 that are *through* openings 99a are formed by "using a physical vapor deposition (PVD) process, such as sputtering processor or evaporation process, or a chemical-vapor deposition (CVD) process," which were all widely known and used techniques that a POSITA would have been familiar with. *EX1005* at [0306]-[0307]. Because Sundaram already teaches the polymer layer, and because openings in polymer layers and UBM layers were already well-known and formed using conventional manufacturing techniques, a POSITA would have had a reasonable expectation of success.

16. 16(e)(ii): "wherein said first metal bump comprises a tin-containing layer;"

280. *See* Claim 1(e)(i), ¶¶ 172-179, incorporated herein.

17. 16(f): "a second metal bump over said first interconnection scheme,"

281. Sundaram's chip package includes a *second metal bump over said first interconnection scheme*, shown below. The annotated bump is a *second metal bump* for the same reasons described above at Claims 16(e), 1(e), i.e., because it's a "copper bump with [a] solder cap[]." *See* ¶¶ 273, 171; *EX1004* at 6:29-31.

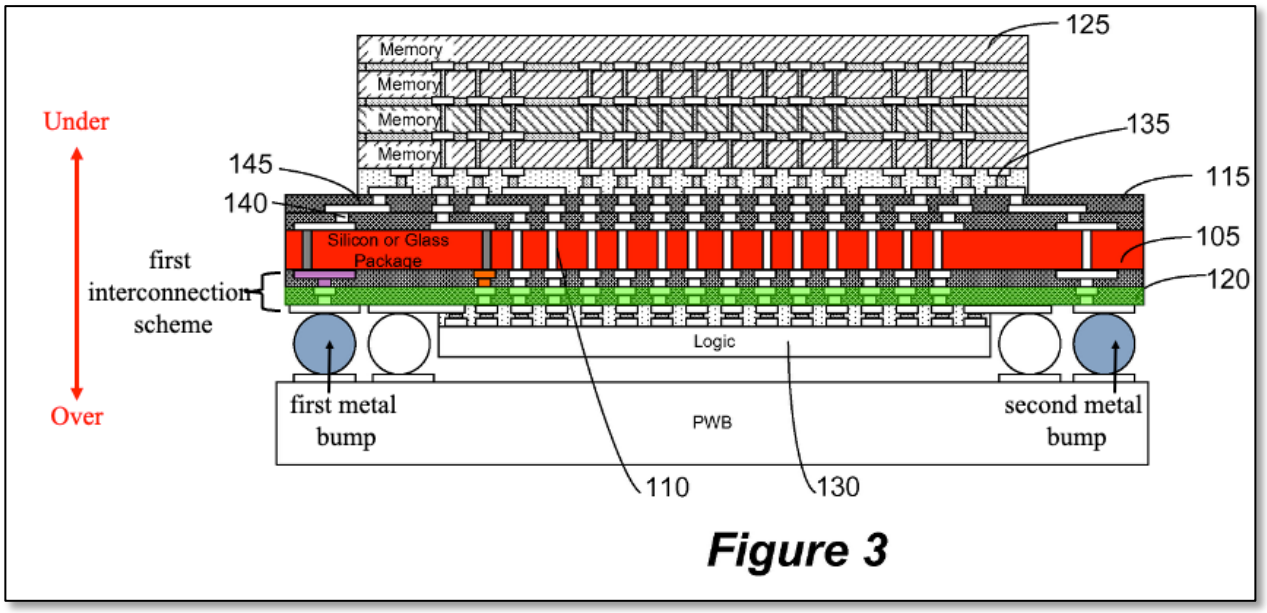


Figure 3

EX1004 at FIG. 3.

18. 16(f)(i): "wherein said second metal bump is connected to said first interconnection scheme through a second opening in said second polymer layer;"

282. For the same reasons described above at Claim 16(e)(i), based on Lin-191's teachings, a POSITA would have found it obvious and been motivated to modify Sundaram's *second metal bump* to be *connected to said first interconnection scheme through a second opening in said second polymer layer*. *See* ¶¶ 274-279, incorporated herein.

19. 16(g): "a first semiconductor chip over said first interconnection scheme and between said first and second metal bumps;"

283. Sundaram teaches that "a second electronic device 130 can be attached to the second side 120 of the interposer 105. In exemplary embodiments… second

electronic device 130 can be a logic IC device or devices." *EX1004* at 6:35-39. Second electronic device 130 is thus a *first semiconductor chip over said first interconnection scheme* and, as shown, is *between said first and second metal bumps*:

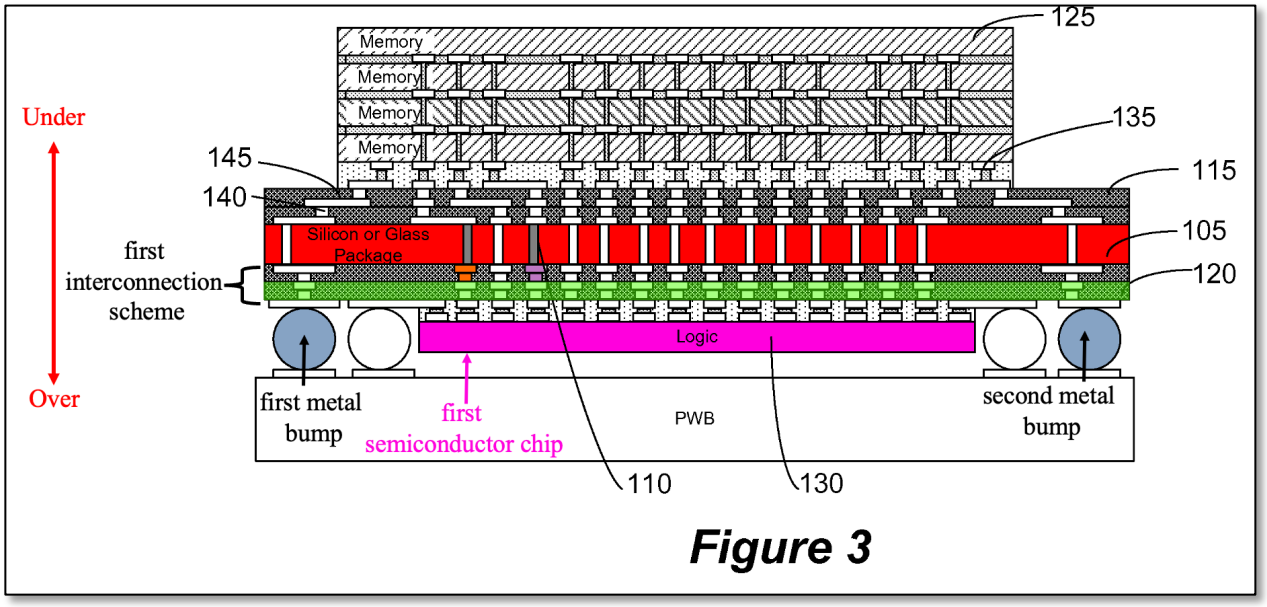


Figure 3

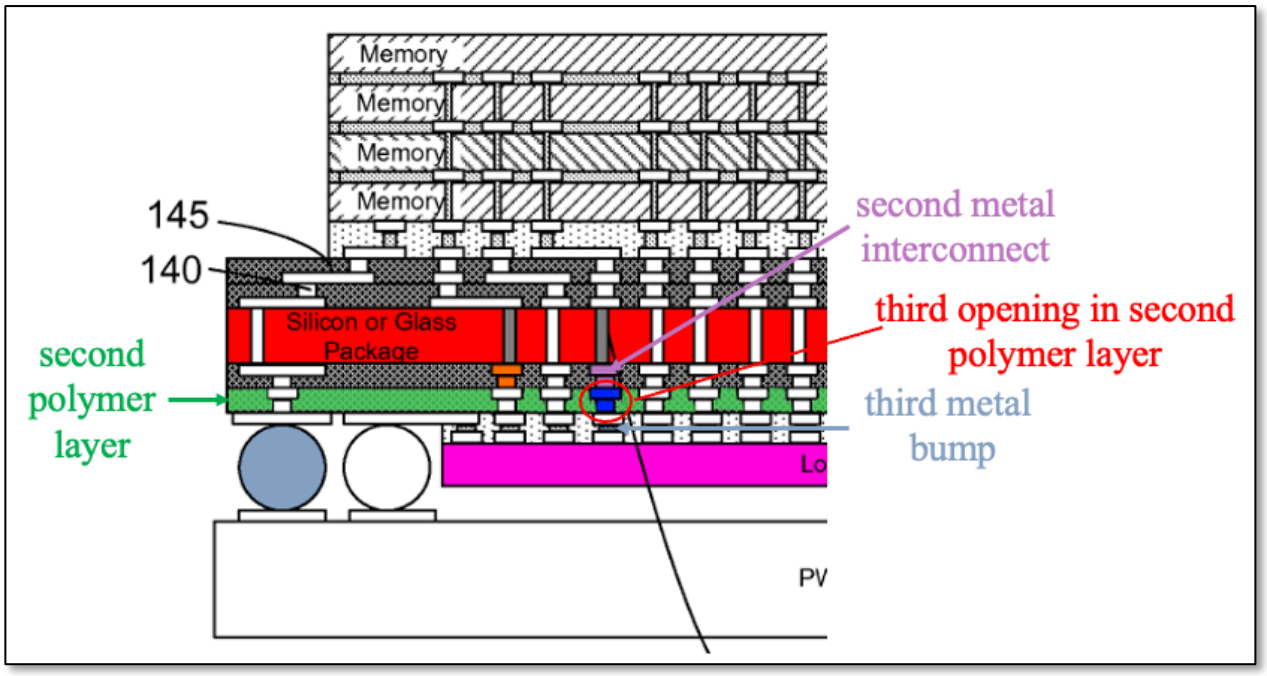
EX1004 at FIG. 3.

20. 16(h): "a third metal bump between said first semiconductor chip and said first interconnection scheme,"

284. *See* Claim 4(b), ¶ 209, incorporated herein. Claim 16(h)'s *third metal bump* corresponds to Claim 4(b)'s *second metal bump*. In other words, the limitations of Claim 16(h) correspond to those of Claim 4(b), including the interrelationship to the claimed components, because they recite the same claimed structure other than the nomenclature of the *second* and *third*.

21. 16(h)(i): "wherein said third metal bump connected to said second metal interconnect through a third opening in said second polymer layer; and"

285. Sundaram's *third metal bump [is] connected to said second metal interconnect* via traces and vias positioned in a *third opening in said second polymer layer*. The traces and vias are in *a third opening* because they are "defined within polymer-metal redistribution layers" meaning there are gaps in the *second polymer layer* that form the *third opening* where the traces and vias are positioned. *EX1004* at 6:62-67;



EX1004 at FIG. 3 (excerpt); 6:29-33, 6:62-67.

22. 16(i): "a second semiconductor chip under said first interconnection scheme and said first semiconductor chip,"

286. Sundaram teaches a "first electronic device 125" that "can be single or stacked memory IC devices" or "other electronic devices" such as "an image sensor chip." *EX1004* at 6:37-45, FIG. 3. Device 125 is thus a *second semiconductor chip*. As shown, the *second semiconductor chip* is *under said first interconnection scheme and said first semiconductor chip*:

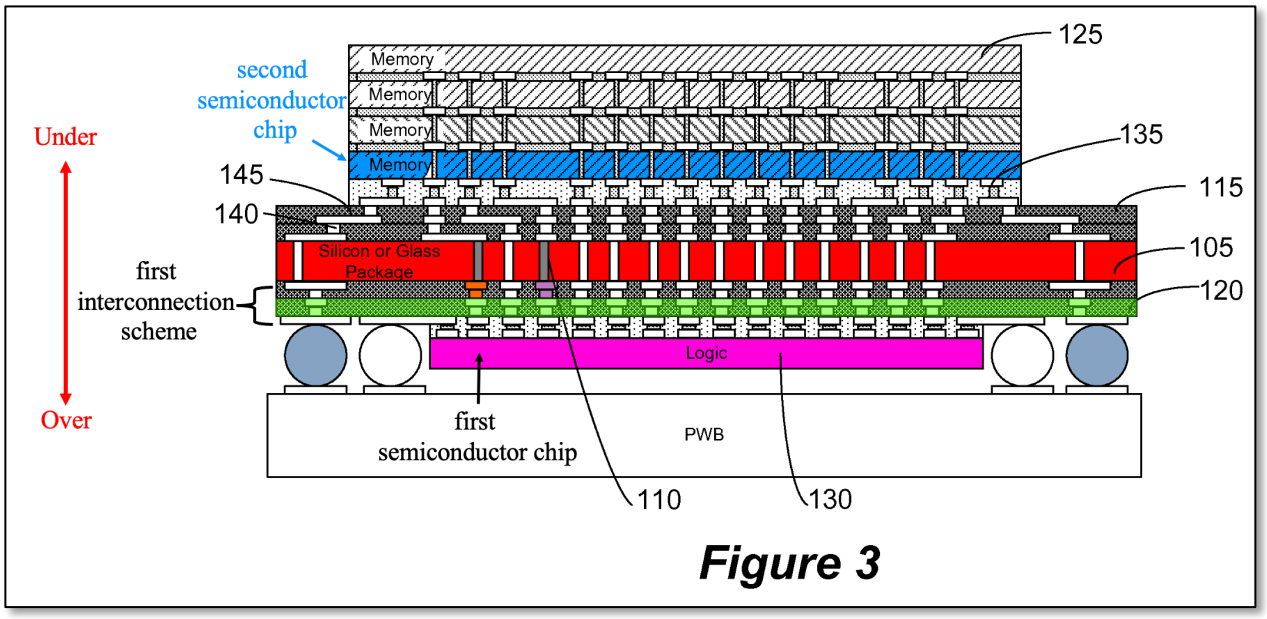


Figure 3

EX1004 at FIG. 3.

23. 16(i)(i): "wherein said first interconnection scheme is between said first and second semiconductor chips,"

287. As I discussed above at claim 16(i), in the Sundaram-Lin combination, the *first semiconductor chip* is *over* the *first interconnection scheme* while the *second semiconductor chip* is *under* the *first interconnection scheme*. *See* ¶ 286. Because (1) the *first semiconductor chip* is *over* the *first interconnection scheme*, and (2), the *second semiconductor chip* is *under* the *first interconnection scheme*, then the *first*

interconnection scheme is between said first and second semiconductor chips, as shown:

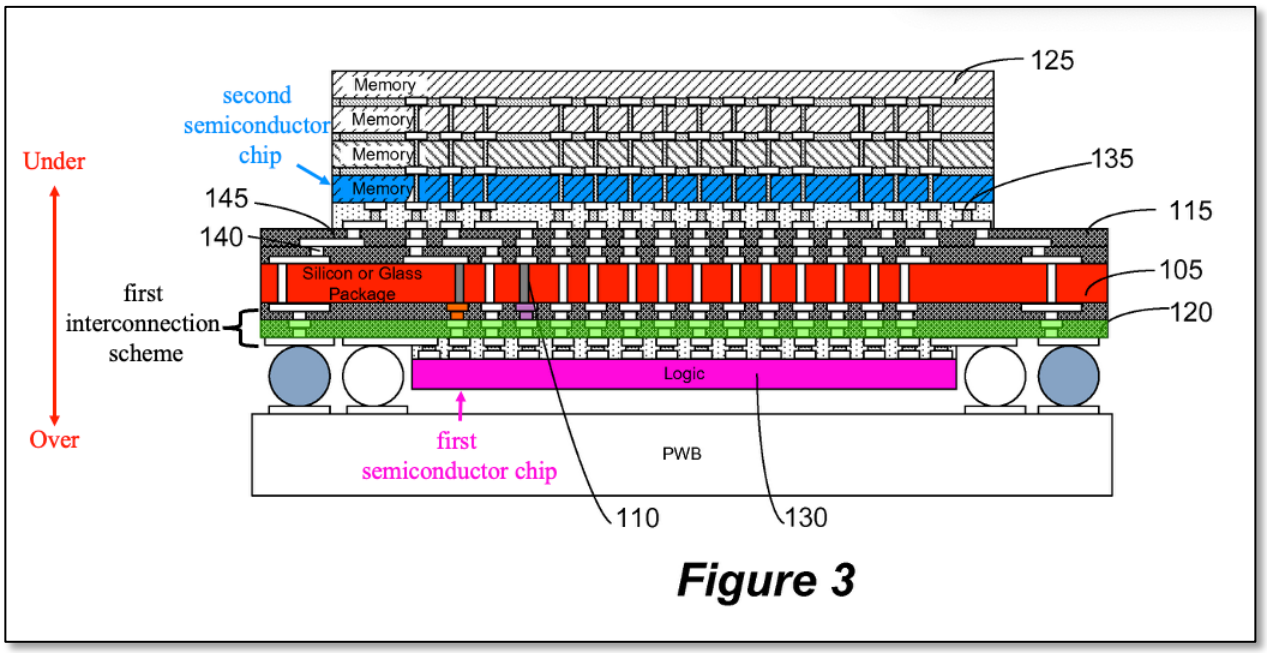


Figure 3

EX1004 at FIG. 3.

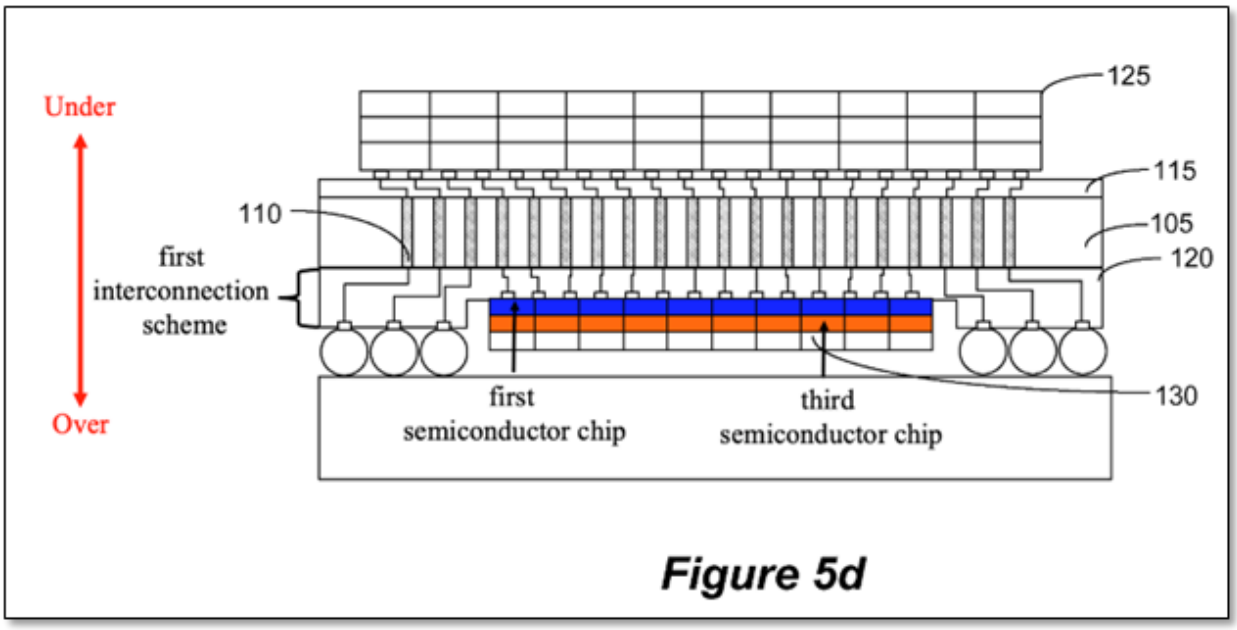
24. 16(i)(ii): "wherein said second semiconductor chip comprises a central-processing-unit (CPU) circuit block and a graphics-processing-unit (GPU) circuit block."

288. *See* Claim 5, ¶¶ 210-213, (teachings, motivation to combine, and reasonable expectation of success incorporated herein). Claim 16(i)(ii)'s *second semiconductor chip* corresponds to Claim 5's *first semiconductor chip*.

B. *Claim 17: "The chip package of claim 16, further comprising a third semiconductor chip over said first interconnection scheme."*

289. Sundaram teaches "third and fourth electronic devices can be stacked on the first 125 and second 130 electronic devices," thus, the fourth electronic device

stacked on the second electronic device 130 is *a third semiconductor chip over said first interconnection scheme*. *EX1004* at 7:16-18. Indeed, the *third semiconductor chip* is shown below in FIG. 5d. Because FIG. 5 "show[s] various exemplary embodiments of the interconnect structure 100," a POSITA would have understood that the stacked chips in second electronic device 130 shown in FIG. 5d represent a *second semiconductor chip over* the *first interconnection scheme* in Sundaram's interconnect structure 100 depicted in FIG. 3. *EX1004* at 7:7-9, 5:45-46, FIG. 3.



EX1004 at FIG. 5d.

C. ***Claim 18: "The chip package of claim 16, wherein said second semiconductor chip comprises a first metal pad on a top surface of said second semiconductor chip and a second metal pad on a bottom surface of said second semiconductor chip, wherein said first metal pad is connected to said second metal pad through a through-silicon-via metal layer."***

290. *See* Claim 6, ¶¶ 214-219, incorporated herein. Claim 18's *second semiconductor chip*, *first metal pad*, and *second metal pad* correspond to Claim 6's *first semiconductor chip*, *second metal pad*, and *third metal pad*, respectively. In other words, the limitations of Claim 18 correspond to those of Claim 6, including the interrelationship of the claimed components because they recite the same claimed structure other than the nomenclature of the *first*, *second*, and *third*.

D. *Claim 19: "The chip package of claim 16, further comprising a third metal plug vertically in a third through via in said polymer layer, wherein a pitch between said first and third metal plugs is between 200 and 1000 micrometers."*

291. *See* Claim 14, ¶¶ 252-256, incorporated herein.

E. *Claim 21*

1. Claim 21(a): "The chip package of claim 16, further comprising a third semiconductor chip under said second semiconductor chip and"

292. *See* Claim 12(a), ¶ 240, incorporated herein. Claim 21's *third semiconductor chip* and *second semiconductor chip* correspond to Claim 12's *second semiconductor chip* and *first semiconductor chip*, respectively. In other words, the limitations of Claim 21(a) correspond to those of Claim 12(a), including the interrelationship of the claimed components, because they recite the same claimed structure other than the nomenclature of *first*, *second*, and *third*.

2. Claim 21(b): "multiple fourth metal bumps between said second and third semiconductor chips,"

293. FIG. 32 teaches *second and third semiconductor chips* having metal pads on either surface.

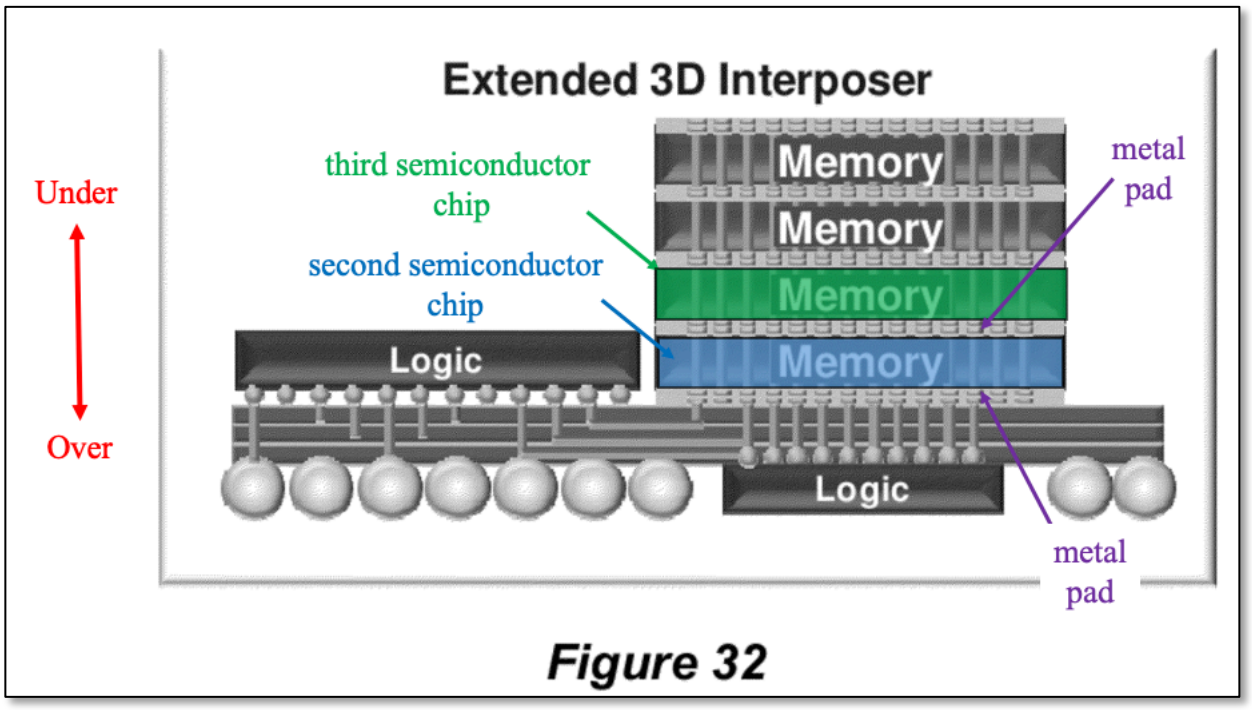


Figure 32

EX1004 at FIG. 32.

294. Sundaram further teaches that "die pads 135 … can electrically connect devices using solder, copper bumps with solder caps …." *EX1004* at 6:29–34. A POSITA would have understood chip pads on devices 125, 130 likewise electrically connect using solder because connecting metal pads using solder bumps was standard practice for the same reasons discussed above at Claim 12(b). *See* ¶ 243. A POSITA would have found it obvious, been motivated, and had a reasonable expectation of success in combining Sundaram's internal embodiments to *connect[] pads* with *multiple fourth metal bumps between said second and third semiconductor*

chips, teaching Claim 21(b). The same MTCs and reasonable expectation of success discussed above apply herein. *See* ¶¶ 244-245, incorporated herein. That is, a POSITA would have recognized that connecting Sundaram's *second and third semiconductor chips* with *multiple fourth metal bumps* would have yielded the same advantages discussed above. *See* ¶¶ 244-245. The modification is the combination of known prior art elements (metal bump connections for chip pads) according to known methods to yield predictable results. The modification would have advantageously provided Sundaram with a good electromechanical connection between chips, which would have had a reasonable expectation of success because such was a common method of connecting chips, as described above. *See* ¶ 243; *see also EX1113* at FIG. 3G, [0032]-[0033]. Further, Sundaram already teaches forming metal bumps (i.e., "copper bumps with solder caps"), further leading to a reasonable expectation of success.

3. Claim 21(c): "wherein said second semiconductor chip comprises a first metal pad on a top surface of said second semiconductor chip and a second metal pad on a bottom surface of said second semiconductor chip,"

295. *See* Claim 6(a), ¶¶ 214-216, incorporated herein. Claim 21(c)'s *second semiconductor chip, first metal pad*, and *second metal pad* correspond to Claim 6(a)'s *first semiconductor chip, second metal pad*, and *third metal pad*, respectively. In other words, the limitations of Claim 21(c) correspond to those of Claim 6(a),

including the interrelationship of the claimed components, because they recite the same claimed structure other than the nomenclature of *first*, *second*, and *third*.

4. Claim 21(d): "wherein said first metal pad is connected to said second metal pad through a through-silicon-via metal layer."

296. *See* Claim 6(b), ¶¶ 217-219, incorporated herein. Claim 21(d)'s *first metal pad* and *second metal pad* correspond to Claim 6(b)'s *second metal pad* and *third metal pad*, respectively. In other words, the limitations of Claim 21(d) correspond to those of Claim 6(b), including the interrelationship of the claimed components, because they recite the same claimed structure other than the nomenclature of nomenclature of *first*, *second*, and *third*.

F. *Claim 22: "The chip package of claim 16, further comprising a passive component over said first surface."*

297. *See* Claim 2, ¶¶ 197-204, incorporated herein. Because, in the combination, the *passive component* is *over* the *first interconnection scheme*, the *passive component* is also *over said first surface*.

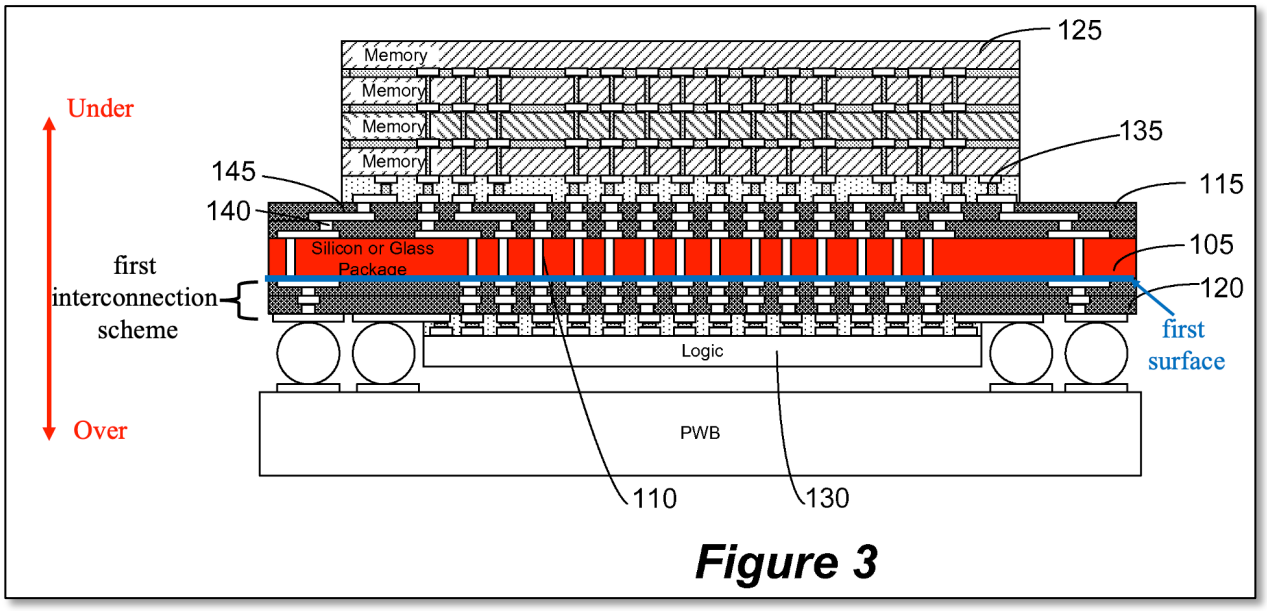


Figure 3

EX1004 at FIG. 3.

G. *Claim 23: "The chip package of claim 16, wherein said first interconnection scheme comprise a third metal interconnect across over a sidewall of the second semiconductor chip."*

298. *See,* Claim 3, ¶¶ 205-207, incorporated herein. Claim 23's the *third metal interconnect* corresponds to Claim 3's *fifth metal interconnect*. In other words, the limitations of Claim 23 correspond to those of Claim 3, including the interrelationship of the claimed components, because they recite the same claimed structure other than the nomenclature of *third* and *fifth*.

H. *Claim 24: "The chip package of claim 16, further comprising a third semiconductor chip under said first interconnection scheme, wherein said third semiconductor chip is a memory chip."*

299. Because Sundaram teaches that the "first electronic device 125 can be…stacked memory IC devices," a second chip in Sundaram's memory chip stack

is a *third semiconductor chip* that *is a memory chip*. *EX1004* at 6:37-38. As shown, the *third semiconductor chip* is *under said first interconnection scheme*:

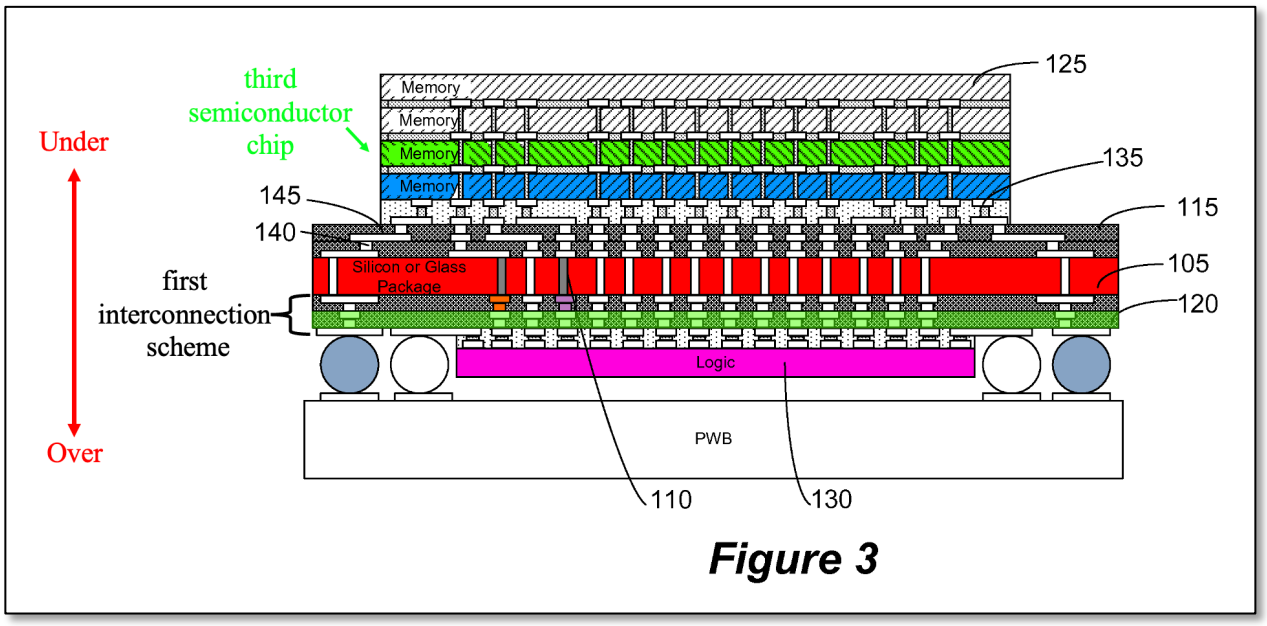


Figure 3

EX1004 at FIG. 3.

I. *Claim 25*

1. Claim 25(a): "The chip package of claim 16, wherein said second semiconductor chip comprises a third metal interconnect on a metal pad of said second semiconductor chip,"

300. See Claim 1(f)(i) ¶¶ 181-185, incorporated herein. Claim 25's *second semiconductor chip* and *third metal interconnect* correspond to Claim 1(f)(i)'s *first semiconductor chip* and *fourth metal interconnect*, respectively. In other words, the limitations of Claim 25(a) correspond to those of Claim 1(f)(i), including the interrelationship of the claimed components, because they recite the same claimed structure other than the nomenclature of *first*, *second*, *third*, and *fourth*.

2. Claim 25(b): "wherein said third metal interconnect comprises a second metal layer on said metal pad and a fifth copper layer over said second metal layer, wherein said fifth copper layer has a thickness between 5 and 30 micrometers,"

301. *See* Claim 1(f)(ii), ¶¶ 186-194, incorporated herein. Claim 25(b)'s *third metal interconnect* corresponds to Claim 1(f)(ii)'s *fourth metal interconnect*. In other words, the limitations of Claim 25(b) correspond to those of Claim 1(f)(ii), including the interrelationship of the claimed components, because they recite the same claimed structure other than the nomenclature of *third* and *fourth*.

3. Claim 25(c): "wherein said third metal interconnect is connected to said a fourth metal interconnect of said first interconnection scheme."

302. *See* Claim 1(f)(iii), ¶¶ 195-196, incorporated herein. Claim 25's *fourth metal interconnect* corresponds to Claim 1(f)(iii)'s *third metal interconnect*, which is part of the *first interconnection scheme*. In other words, the limitations of Claim 25(c) correspond to those of Claim 1(f)(iii), including the interrelationship of the claimed components, because they recite the same claimed structure other than the nomenclature of *third* and *fourth*.

J. *Claim 26: "The chip package of claim 16, wherein a height is between a backside surface of said first semiconductor chip and a top surface of said second polymer layer is smaller than a thickness of said first metal bump."*

303. *See* Claim 11(b), ¶¶ 237-239, incorporated herein. Claim 26's *first semiconductor chip* corresponds to Claim 11's *second semiconductor chip*. In other words, the limitations of Claim 26 correspond to those of Claim 11(b), including the

interrelationship of the claimed components, because they recite the same claimed structure other than the nomenclature of *first* and *second*.

K. *Claim 27: "The chip package of claim 16, wherein said second semiconductor chip is coupled to said first semiconductor chip through said first interconnection scheme."*

304. Sundaram's *second semiconductor chip is coupled to the first semiconductor chip through the first interconnection scheme*, as shown via the path (highlighted in pink) in FIG. 3. The electrical path extends through vias 140 and traces 145, which connects the upper memory stack (first electronic device 125) to the logic device 130 positioned beneath the interposer 105. Sundaram explains that "the interposer 105 and the through vias 110 work to electrically connect the first electronic device 125 and the second electronic device 130, and have substantially the same through-via interconnect density as the first electronic device 125 or the second electronic device 130 it connects." *EX1004* at 6:46-50. Additionally, die pads 135 that are formed on the first 115 and second sides 120 of the interposer 105 can **electrically connect** devices using…copper bumps[.]" *EX1004* at 6:29-33. Thus, the vias 140 and traces 145 on either side of interposer 105 (including those of the *first interconnection scheme*) are connected through a through via 110, and likewise connect to the pads in Sundaram's devices 125, 130, thus forming a continuous conductive path between the first electronic device 125 (*second semiconductor chip*) and second electronic device 130 (*first semiconductor chip*). Sundaram thus teaches

wherein said second semiconductor chip is coupled to said first semiconductor chip through said first interconnection scheme

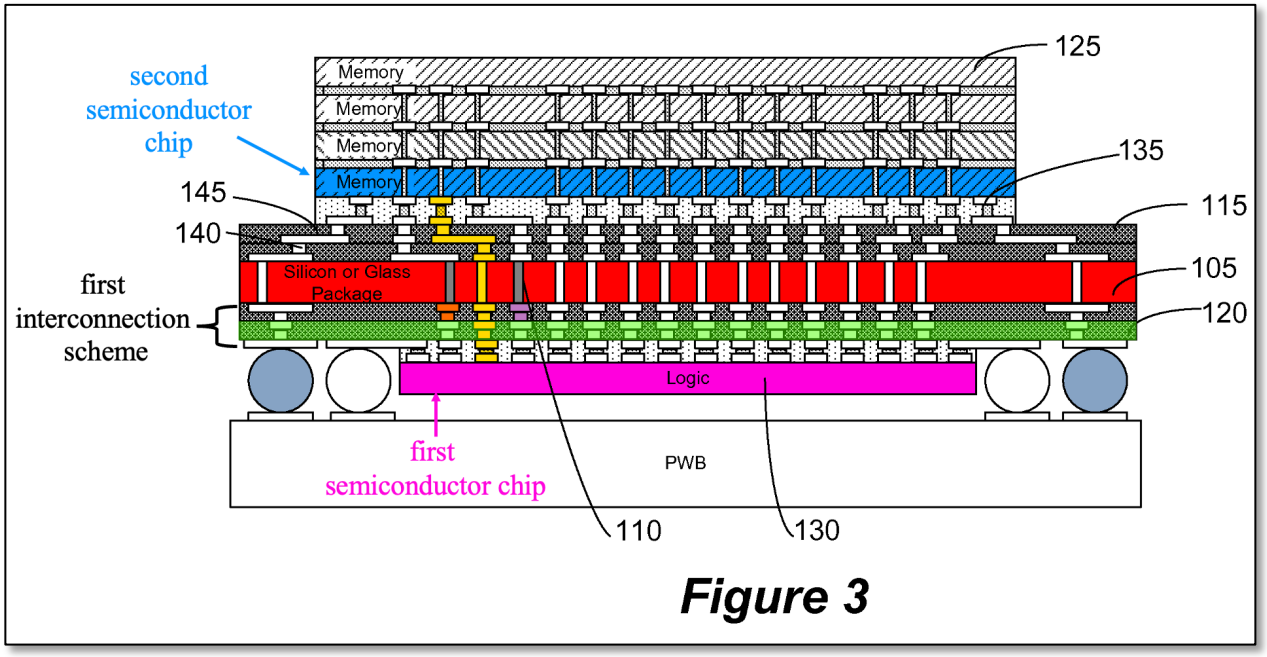


Figure 3

EX1004 at FIG. 3.

L. *Claim 28: "The chip package of claim 16, wherein said first metal plug has a thickness between 100 and 300 micrometers."*

305. *See* Claim 15, ¶¶ 257-258, incorporated herein.

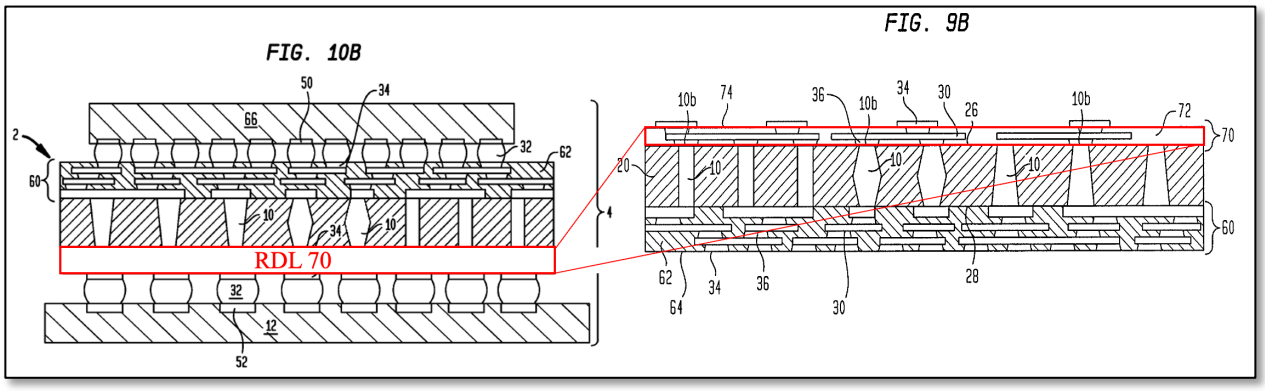
X. OPINIONS REGARDING GROUND 2A: CLAIMS 1-3, 5, 7-10, AND 14-15 ARE OBVIOUS OVER HABA AND LIN-191

A. *Overview of Haba's Figures*

306. I note that the following mapping relies on Haba's FIGS. 9B and 10B. Regarding FIG. 9B, Haba teaches that the "embodiment of [interconnection] component 2 shown in FIG. 9B can be used in an assembly for attachment between a microelectronic element and a PCB in a similar arrangement as shown in FIGS.

10A and 10B…" *EX1009* at 8:12-16. Thus, Haba teaches that like FIG. 10B, the embodiment of FIG. 9B, may include a microelectronic element 66 and printed circuit board (PCB) 12.

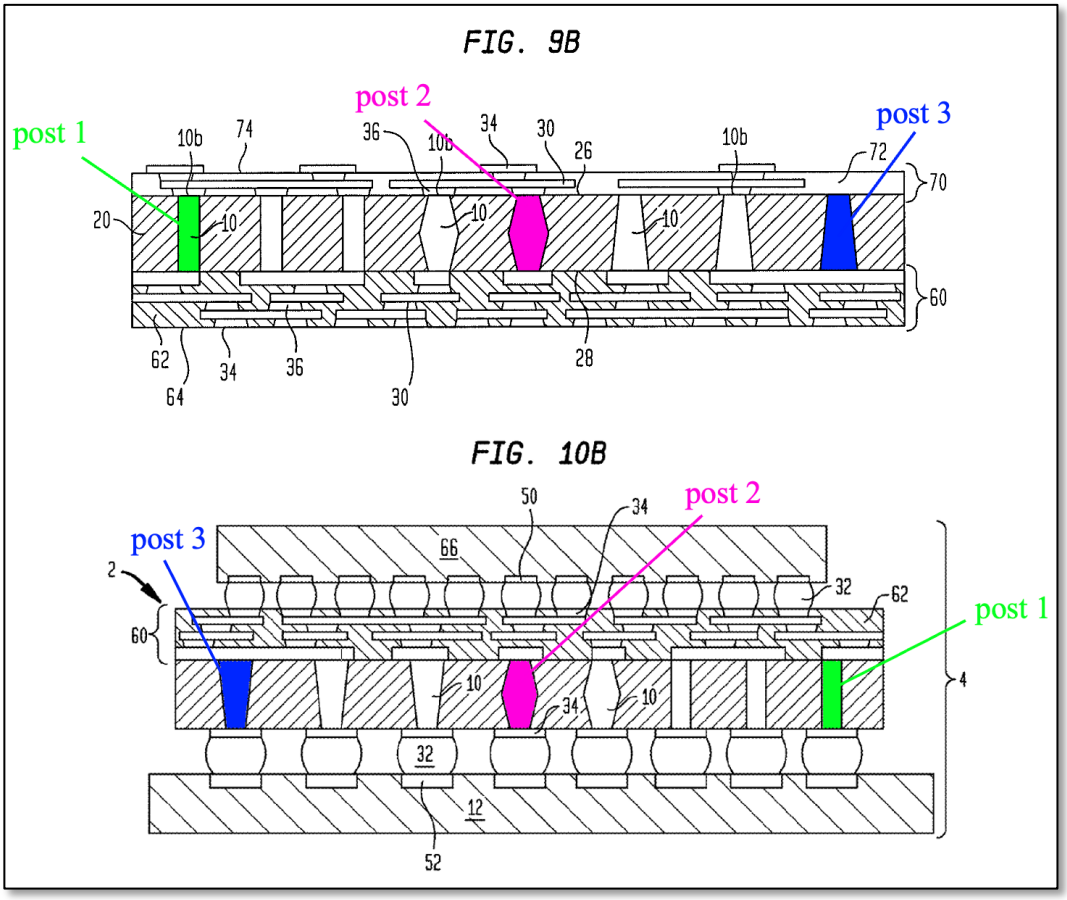
307. I have provided an annotated figure below that depicts the relationship between both figures. Specifically, the mapping provided herein relies on understanding, based on Haba's express teaching, that the redistribution layer 70, including traces 30, vias 36 and redistribution dielectric 72, may be included in the FIG. 10B embodiment. *EX1009* at 8:12-16. Additionally, Haba discloses that FIG. 10B is "inverted with respect to the depiction" of FIG. 9B. *EX1009* at 7:42-56, 5:1-6. Thus, the redistribution layer 70 of FIG. 9B would fit into the FIG. 10B disclosure as follows:



EX1009 at FIGS. 9B, 10B.

308. For further clarification, in the below figure, I have annotated a number like components in each of FIGS. 9B and 10B, which further illustrate the

relationship between each figure. I note that the "posts 10" in each figure orient the reader to the inversion of FIG. 9B relative to FIG. 10B. *EX1009* at 7:42-56, 5:1-6.



EX1009 at FIGS. 9B and 10B.

309. To the extent Patent Owner contends the disclosure in FIG. 10B is a different embodiment from FIG. 9B's disclosure (notwithstanding Haba's express teaching at 8:12-15 that the FIG. 9B interconnection component 2 can be used in the assembly of FIG. 10B), a POSITA would have been motivated and found it obvious to modify FIG. 10B's interconnection component 2 (including as modified by Lin-191) by including Haba's teachings of FIG. 9B's RDL 70. In the modification, RDL

70 is "formed along surface 26" such that pads 34 are on surface 74 of redistribution layer 70, and solder ball 32 attaches to pad 34. *EX1009* at 8:57-59, FIG. 9B.

310. A POSITA would have found it obvious and been motivated to combine Haba's FIGS. 9B and 10B disclosures. First, Haba expressly teaches that "FIGS. 10A and 10B show variations of a microelectronic assembly respectively including interconnection components according to the embodiments of FIGS. 8 and 9A" and that the "embodiment of component 2 shown in FIG. 9B" is usable in "a similar arrangement as shown in FIGS. 10A and 10B[,]" thus providing an express teaching, suggestion, and motivation for the modification. *EX1009* at 5:4-6, 8:12-17. Additionally, the modification is the combination of a known prior art elements according to known methods to yield the predictable result of Haba's FIG. 10B interconnection component comprising FIG. 9B's redistribution layer 70 along surface 26. The modification would have been straightforward and merely required forming RDL 70 on the side of dielectric layer 20 opposite to that of RDL 60. Thus, given that Haba, at FIG. 9B, already teaches forming both RDL 60 and RDL 70 on either side of dielectric layer 20, the modification would have been straightforward. *EX1009* at FIG. 9B.

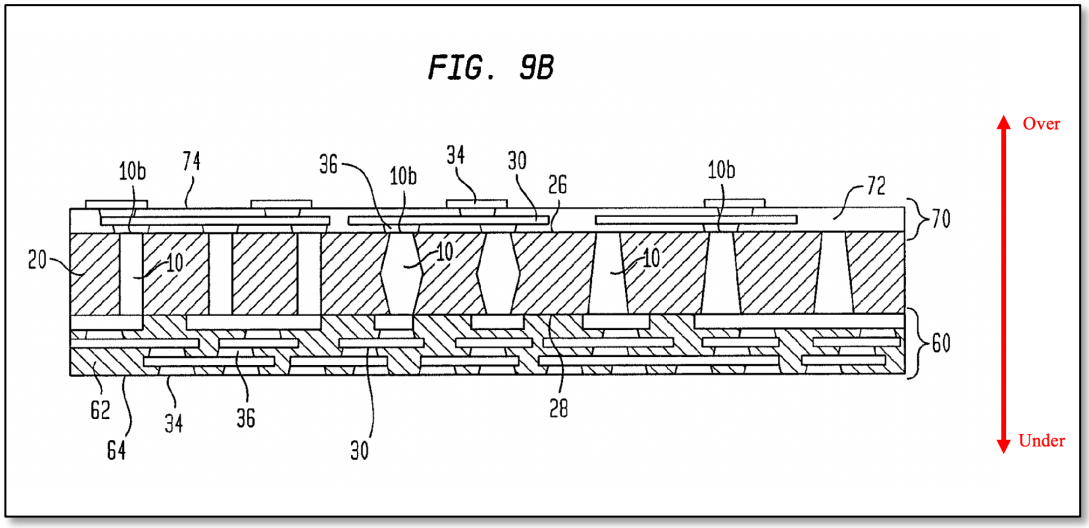
311. Further, the modification is merely the application of a known technique (adding redistribution layer 70 to surface 26) to a known device (the FIG. 10B interconnection component) to yield the predictable result discussed above. The

modification would have advantageously yielded an improved interconnection component 2 that "allow[s] for an even greater difference in pitch between the conductive features of the microelectronic element and the PCB." *EX1009* at 8:12-17. Such a feature (i.e., allowing for a difference in pitch between the conductive features of the microelectronic element and the PCB) would have been advantageous for applications where microelectronic element 66 (semiconductor chip) comprised contacts with a pitch different than that of the PCB. Thus, a microelectronic element 66 would still have the ability to electrically connect to the PCB without having specialized contacts unique to that specific PCB. Accordingly, a more agnostic chip package structure would be provided that would connect to a variety of components having different contact pitches, which was known to be an advantage. *See, e.g., EX1071* at ("By suitable choice of contact elements on both surfaces of the interposer, as can be appreciated, electronic components having different pitch, different lengths, or different contact pads having diverse features may be interconnected…").

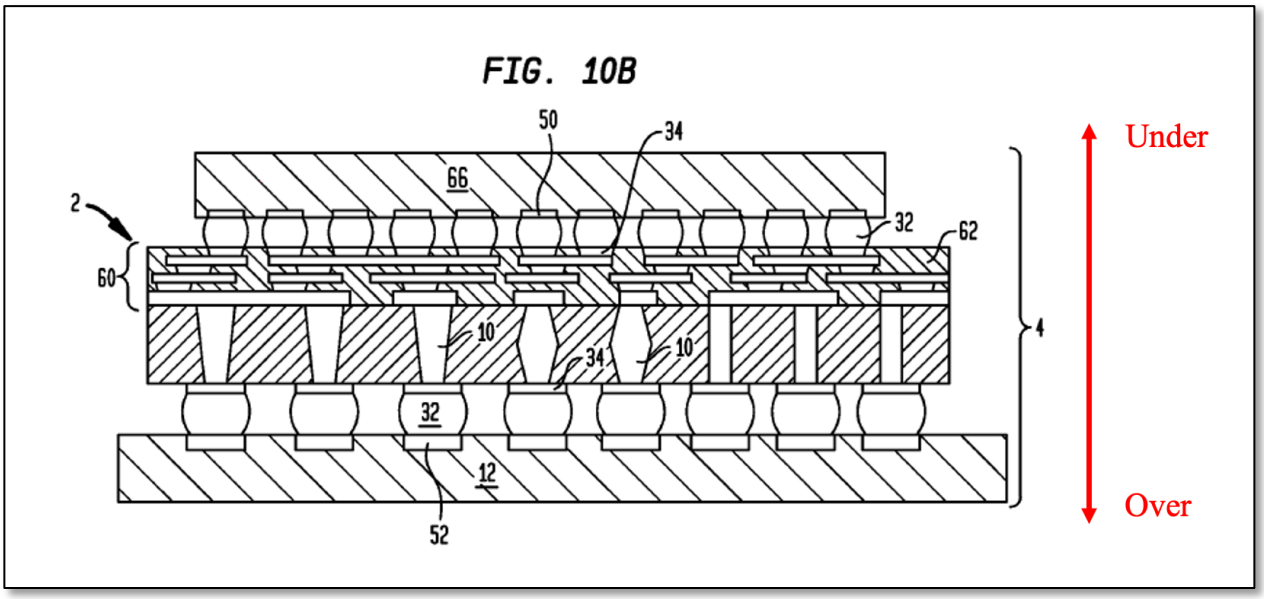
312. Additionally, because the modification is expressly envisioned, if not taught, by Haba and because FIG. 9B already shows forming both RDL 60 and RDL 70 opposite surfaces of on dielectric layer 20, which is the structure achieved in the combination of FIGS 9B and 10B, the modification would have had a reasonable expectation of success. Additionally, formation of redistribution layers for

connecting components in a chip package to a PCB was well known. *See, e.g., EX1078* at [0059] ("The redistribution layer maps the connections provided by the electrically conductive pillars onto a regular array of solder balls (a ball grid array)…for reflow attachment to an appropriately designed printed circuit board.").

313. As with the Sundaram ground, I annotate FIGS. 9B and 10B (and other figures where appropriate) indicating the *over* and *under* directions, where *over* is towards PCB 12 and *under* is away from PCB 12 (FIG. 10B).



EX1009 at FIG. 9B



EX1009 at FIG. 10B

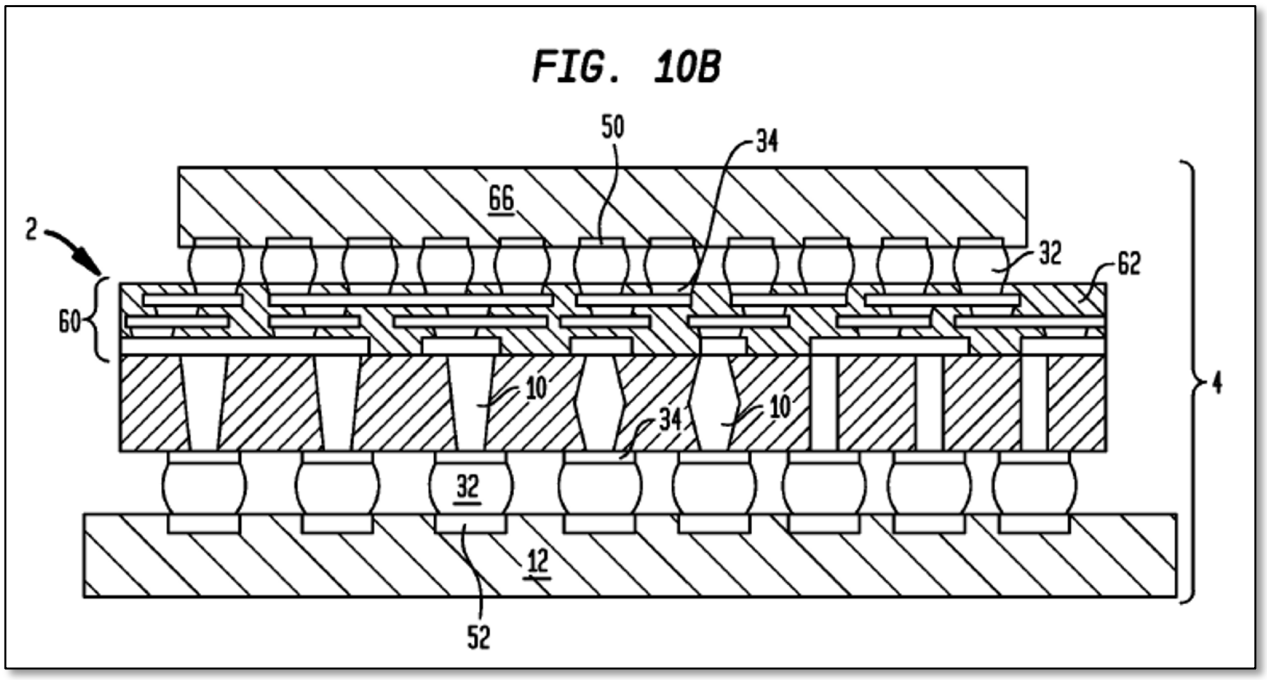
B. *Claim 1*

1. 1[Pre]: "A chip package comprising"

314. Haba teaches that "[m]icroelectronic assemblies generally include one or more **packaged** microelectronic elements such as one or more semiconductor chips mounted on a substrate." *EX1009* at 1:19-22 (emphasis added). As such, Haba recognizes that a *chip package* includes "one or more semiconductor chips" that are "mounted on a substrate." *EX1009* at 1:19-22. Additionally, Haba incorporates in by reference U.S. Patent No. 7,759,782, which expressly teaches that "microelectronic **packages** generally comprise one or more substrates with one or more microelectronic devices such as one or more semiconductor **chips** mounted on such substrates." *EX1084* at 1:22-26. Haba, thus, defines a "microelectronic *package*" as including "one or more substrates" with "one or more semiconductor chips mounted

on such substrates." *EX1084* at 1:22-26. As I will explain below, Haba thus teaches a *chip package*, namely in the form of a microelectronic element 66 (semiconductor chip) mounted to an "interconnection component 2" (substrate).

315. Indeed, Haba specifically teaches a microelectronic assembly including a "microelectronic element 66" (one or more semiconductor chips) that is "flip-chip bonded" to an "interconnection component 2" (substrate), which is, in turn, mounted to a printed circuit board (PCB) 12, thus forming a *chip package*, as shown below in FIG. 10B. *EX1009* at 6:63-66. Indeed, Haba refers to "dielectric layer 20" in interconnection component 2 as a "substrate or interconnect component[,]" thus confirming that together, at least interconnection component 2 and microelectronic element 66 comprise a "microelectronic assembly" (i.e., *chip package*). *EX1009* at 6:19-23, 1:19-22, *see also EX1009* at 2:59-3:3 (discussing a method for forming a "microelectronic assembly"). Additionally, "flip-chip" bonding is a technique regularly used in semiconductor packaging. *See, e.g., EX1085* at 1:16-17 ("Flip chip bonding technology is a **packaging** technique that attaches a die to a carrier."). Thus, by "flip-chip bond[ing]" microelectronic element 66 (one or more semiconductor chips) to interconnection component 2, Haba teaches forming a *chip package*.

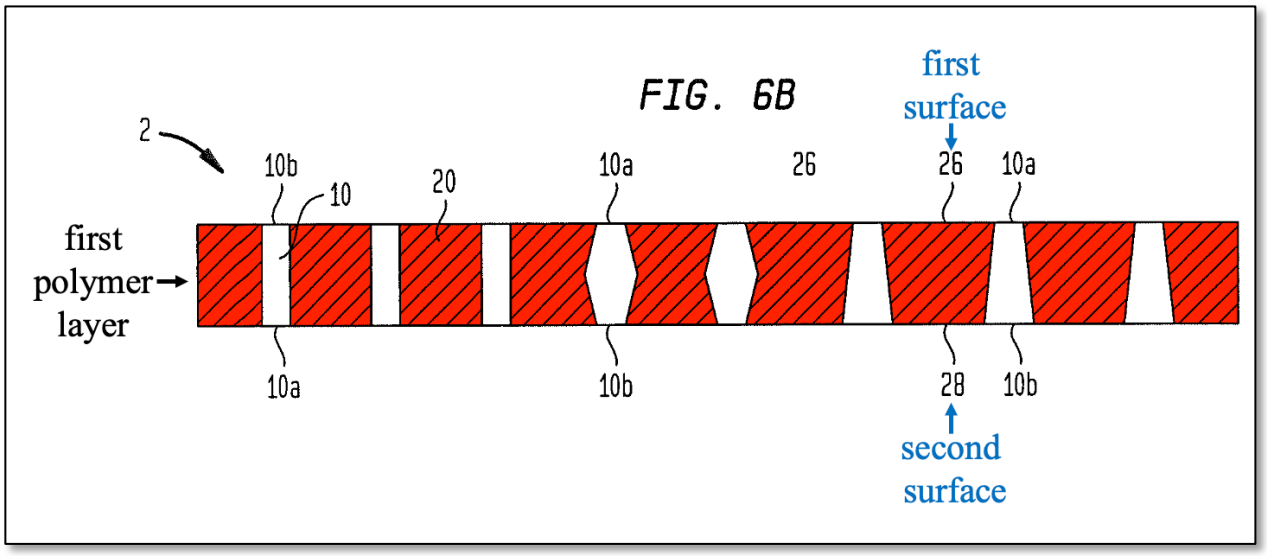


EX1009 at FIG. 10B.

2. 1(a): "a first polymer layer having a first surface and a second surface opposite to said first surface,"

316. As shown below, Haba's interconnection component 2, part of the *chip package*, comprises a dielectric layer 20 that "can be formed from, for example, compositions which cure by chemical reaction to form a **polymeric** dielectric, such as epoxies and polyimides[.]" *EX1009* at 5:41-44. Because Haba teaches that dielectric layer 20 may be formed of "epoxies and polyimides[,]" both examples of a *polymer*, such that a "polymeric dielectric" is formed, Haba thus teaches a *first polymer layer*. *See, e.g., EX1115* at 17:14-25 ("…high temperature polymers such…epoxies[.]"), 12:45 ("For example, polymers, such as some polyimides…").

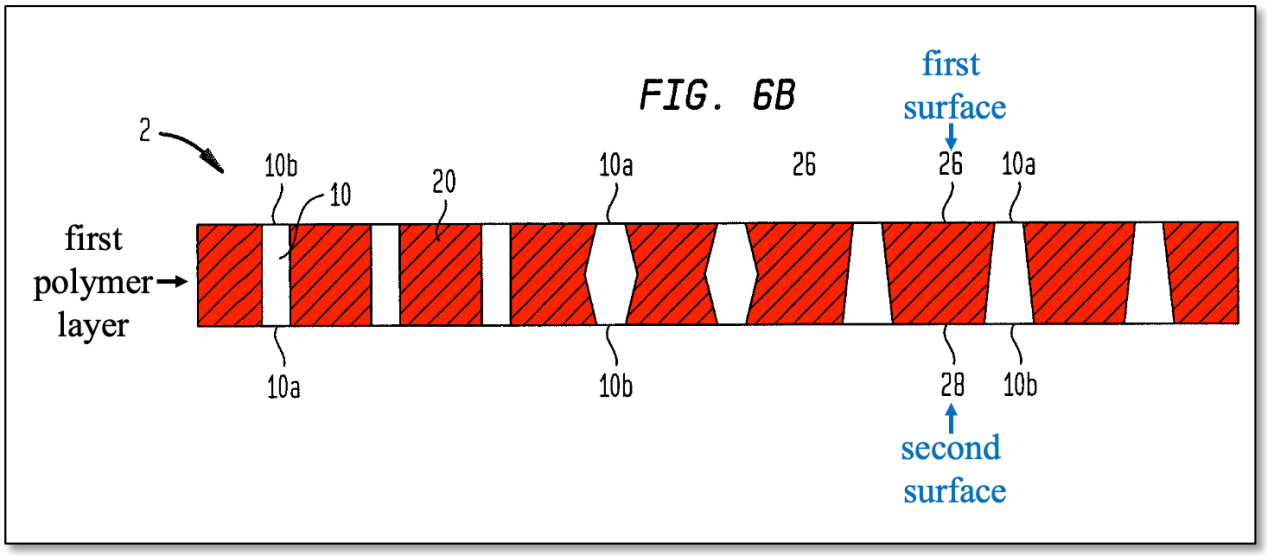
317. Further, the "dielectric layer has first and second opposed surfaces[,]" namely surface 26 (*first surface*) and surface 28 (*second surface*). Because surface 26 and surface 28 are "opposed surfaces[,]" Haba teaches that dielectric layer 20 (*first polymer layer*) has *a first surface* (surface 26) *and a second surface* (surface 28) *opposite to said first surface*.



EX1009 at FIG. 6B.

3. 1(a)(i): "wherein said first surface is substantially parallel to said second surface,"

318. Haba's surfaces 26 and 28 are parallel surfaces, as shown below. As such, Haba teaches *wherein said first surface is substantially parallel to said second surface*.



EX1009 at FIG. 6B.

4. 1(a)(ii): "wherein said first polymer layer has a thickness between 100 and 300 micrometers and…"

319. Dielectric layer 20 has "a thickness of **at least 10 μm** between the first and second surfaces[,]" overlapping with and thus teaching or rendering obvious the claimed range of *between 100 and 300 micrometers*. *EX1009* at 2:34-36.

a) Lin-191's Teachings

320. Lin-191 teaches "system-in-packages or multichip modules (MCMs) that include multi-layer chips in a multi-layer polymer structure[.]" *EX1005* at [0048]. Lin's MCM includes a "substrate 110 [that] can be made of a suitable material, examples of which include…organic polymer." *EX1005* at [0051]. Because, like Haba, Lin-191's substrate 110 is a "polymer substrate", Lin-191's substrate is analogous to Haba's dielectric layer 20, in that both are a *polymer layer*. *EX1005* at [0051].

321. Additionally, Lin-191's substrate 110 includes "multiple through-hole connections 17[,]" which are analogous to Haba's posts 10 (discussed in further detail at claim 1(b)) because they are made of "copper[.]" *EX1005* at [0293], FIG. 52. Thus, like Haba, Lin-191 teaches a polymer layer surrounding copper posts. Thus, a POSITA would have recognized that Lin-191's teachings were relevant to Haba based on the similarities between Haba and Lin-191's polymer layers surrounding copper posts.

322. Finally, Lin-191 teaches that substrate has a "thickness between 10 and 150 micrometers." *EX1005* at [0290]. Similar to my opinions provided for Sundaram for Ground 1A (¶¶ 133-134), Lin-191 teaches or renders obvious the claimed *thickness between 100 and 300 micrometers*. *EX1005* at [0109]-[0111]. Specifically, the claim recites a *thickness between 100 and 300 micrometers*, which overlaps with Lin-191's teaching of 10 to about 150 micrometers, namely the range of 100-150 micrometers within the 10-150 range. Lin-191 therefore teaches a thickness, specifically 100-150 micrometers, that is within the claimed range of *between 100 and 300 micrometers*.

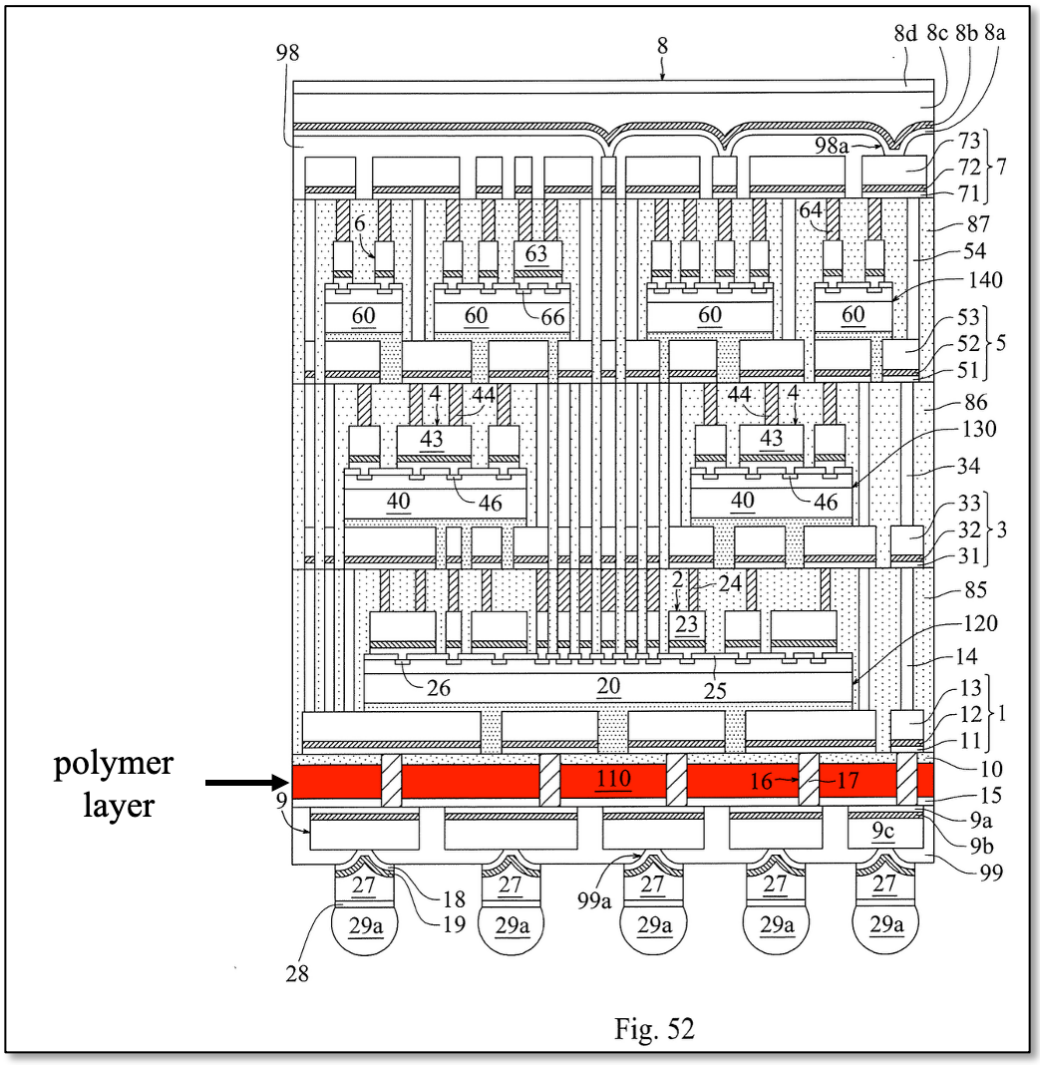


Fig. 52

EX1005 at FIG. 52.

323. Similar to my opinions provided at ¶ 134, I note that the ’768 Patent does not indicate any specific criticality for the claimed range. Therefore, for the reasons provided here and in ¶ 134, it is my opinion a POSITA would have found the claimed range taught or obvious.

b) Motivation to Combine

324. A POSITA would have found it obvious and been motivated to apply Lin-191's teachings of a polymer layer having a *thickness between 100 and 300 micrometers* to Haba's dielectric layer 20 (*first polymer layer*). Lin-191 provides more specificity and optimal ranges for a polymer/dielectric layer that is otherwise taught in Haba as having a thickness of at least 10 microns. *EX1009* at 2:34-36. Selecting a thickness of a substrate would have been a design choice based on factors such as use environment of the package, manufacturability (e.g., layer thickness impacts defect and void formation during production because thinner layers require tighter control of deposition, flow, and planarization processes), and type of chip (e.g., thickness of chip). I note that while at the priority date of the '768 Patent, the industry's trend was to smaller (thinner) packages. However, a POSITA would have appreciated the tradeoff of a slightly larger package size to obtain certain benefits.

325. For example, a POSITA would have recognized that modifying Haba's dielectric layer 20 according to Lin-191's teachings would have provided many benefits. First, such a thickness would have reduced stress and mechanical fatigue that occurs at the interface between Haba's dielectric layer 20 and posts 10. As discussed in further detail below, Haba's posts 10 are surrounded by dielectric layer 20. A POSITA would have recognized that the interface between the copper posts and dielectric layer 20 would have benefitted from a thicker dielectric layer because

the impact of temperature cycling on said interface would have been reduced, resulting in an increased lifetime of the chip package.

326. Specifically, temperature cycling was a common, and necessary, process during chip manufacturing and use, as expressly noted by Haba. See, e.g., *EX1009* at 5:59-63 ("Components such as the interconnection component described herein may be subject to frequent high temperatures and cycling between high and low temperatures during manufacture, testing, or use."). Temperature cycling during processing or chip operation generates a variable mechanical moment about the vertically embedded posts due to the relative expansion of dielectric layer 20 during heating, creating shear stresses at both attachment surfaces. As expressly recognized by Haba, "when structures within an interconnection component have differing CTEs, the different amounts by which they expand and contract due to changing temperatures can apply stresses" between dielectric layer 20 and posts 10. *EX1009* at 6:6-9. Such stresses "can lead to delamination or cracking[.]" *EX1009* at 6:10. As such, a POSITA would have recognized that increasing the thickness of dielectric layer 20 would have reduced the amount of stress placed on copper posts 10 resulting from CTE mismatch, because the thicker the polymer layer (i.e., dielectric layer 20), the more stress is absorbed by dielectric layer 20. Indeed, polymer layers having a thickness between about "30 μm and about 200 μm" (falling within the claimed range) were known to "act[] as an efficient stress buffer." *EX1080* at [0018]. Thus,

with Lin's thicker polymer layer, the range of stress variation (which creates fatigue) is also reduced. Because more stress would be absorbed by the polymer layer, stress leading to "delamination or cracking" at the copper posts 10 would be reduced, thereby extending the lifetime of the chip package because premature failure due to delamination or cracking would be reduced/delayed. As such, when applied to Haba's dielectric layer 20, Lin-191's thickness would enhance the mechanical reliability of Haba's interconnect structure.

327. Second, a POSITA would have recognized that increasing the thickness of dielectric layer 20, per Lin-191, would offer improved thermal management in Haba's chip package. Specifically, a thicker dielectric layer would provide greater thermal buffering between active layers and external environments, because polymer layers, such as those formed of epoxy and polyimide, were known to be insulating. *EX1081* at 2:31-33 ("…the electrically insulating matrix may include at least one of **polyimide**, silicone, **epoxy**…") (emphasis added). Because dielectric layer 20 is formed of such insulating material (e.g., epoxy/polyimide), increasing the thickness would have correspondingly increased the insulation provided by dielectric layer 20, such that heat generated by microelectronic element 66 would be less likely to travel toward PCB 12, thereby enhancing processing speed. *EX1082* at 1:40-44 ("For instance, a reduction in the operating temperature of a device such as a typical silicon

semiconductor can correspond to an increase in the processing speed, reliability and life expectancy of the device.").

328. Third, a POSITA would have appreciated that the slight increase in thickness would have beneficially enabled more layers of interconnection of EMI shielding to be included in Haba's chip package while still maintaining the minimum allowed interlayer spacing and also enabling increased design flexibility, particularly for stacked and multi-chip configuration.

329. To the extent it is argued a POSITA would not have wanted to increase the size of Haba's dielectric layer 20 in view of the industry's trend to smaller packages, a POSITA would have appreciated the benefits of the tradeoff of a slightly larger package size to obtain the benefits of Lin's teachings and the above-discussed advantages. Specifically, a POSITA would have recognized that while slightly increasing the size of Haba's chip package would have correspondingly increased package size, the various advantages of a thicker dielectric layer 20 described above would have outweighed any concerns about the slight increase in package thickness.

330. The Haba-Lin-191 combination is the application of a known technique (a polymer layer with Lin-191's thickness) to a known device (Haba's chip package with dielectric layer 20) ready for improvement to yield predictable results of a dielectric layer with Lin-191's disclosed thickness to obtain the advantages discussed above. Both Haba and Lin-191 teach known structures, i.e., polymer layers

used in chip packages. Specifically, both Haba and Lin-191 teach dielectric polymer layers (dielectric layer 20 in Haba, substrate 110 in Lin-191) included vertical conductors embedded therein (posts 10 in Haba, through-hole connections 17 in Lin-191). Thus, the modification merely involves selecting a known thickness (e.g., thickness between 100 and 300 micrometers) of a polymer layer for a known purpose.

331. Dielectric layer thickness is commonly varied in microelectronic packaging to optimize mechanical, electrical, and/or thermal performance, and both Lin-191 and Haba use conventional materials (i.e., polymers). Thus, because the thickness range is compatible, the materials are similar, and the processing is well understood, a POSITA would have recognized the modification would have been done with predictable results and without undue experimentation. Additionally, Additionally, Lin-191's 10–150 μm thickness reflects a common dielectric layer thickness used for molded and laminated dielectric layers prior to the '768 Patent because polymer layers were commonly manufactured at Lin-191's thickness. *See* ¶¶ 52-53. Thus, the modification would have merely been a routine adjustment to a known tunable parameter.

5. 1(a)(iii): "[wherein said first polymer layer] has a coefficient of expansion between 3 and 10 ppm/° C.;"

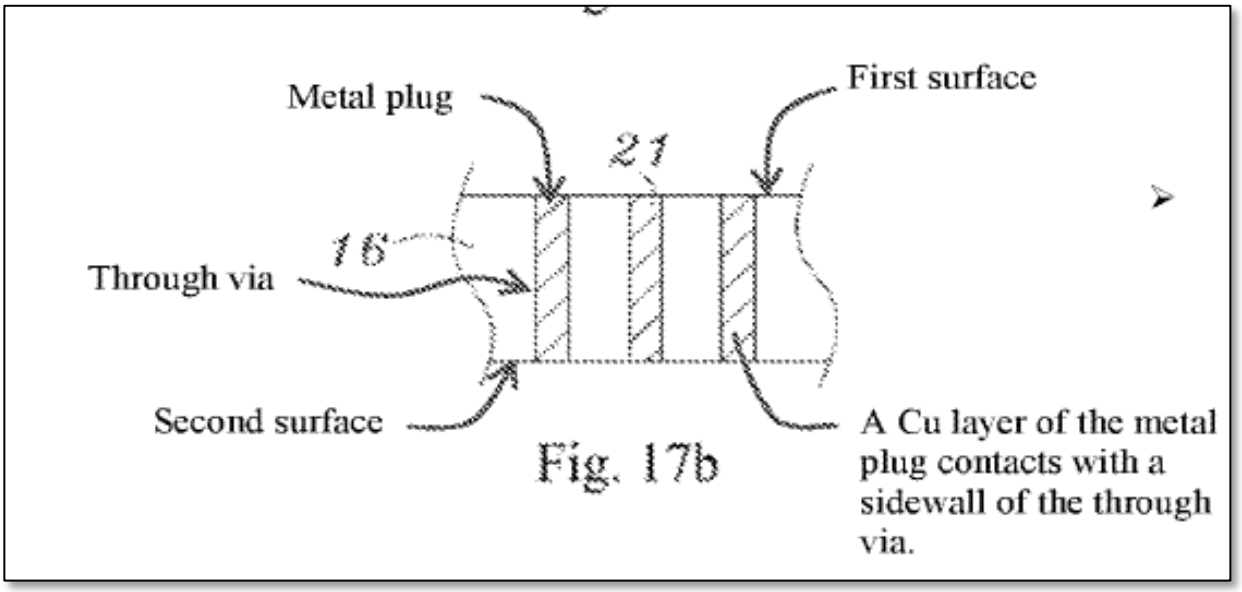
332. Haba expressly teaches that the "CTE [coefficient of thermal expansion] of the material used to form dielectric layer 20 can be in the **range of 8**

parts per million per degree Celsius…or lower." *EX1009* at 5:56-59. *See* ¶¶ 135-136, incorporated herein.

6. 1(b): "a first metal plug vertically in a first through via in said first polymer layer,"

a) The '768 Patent's "through vias"

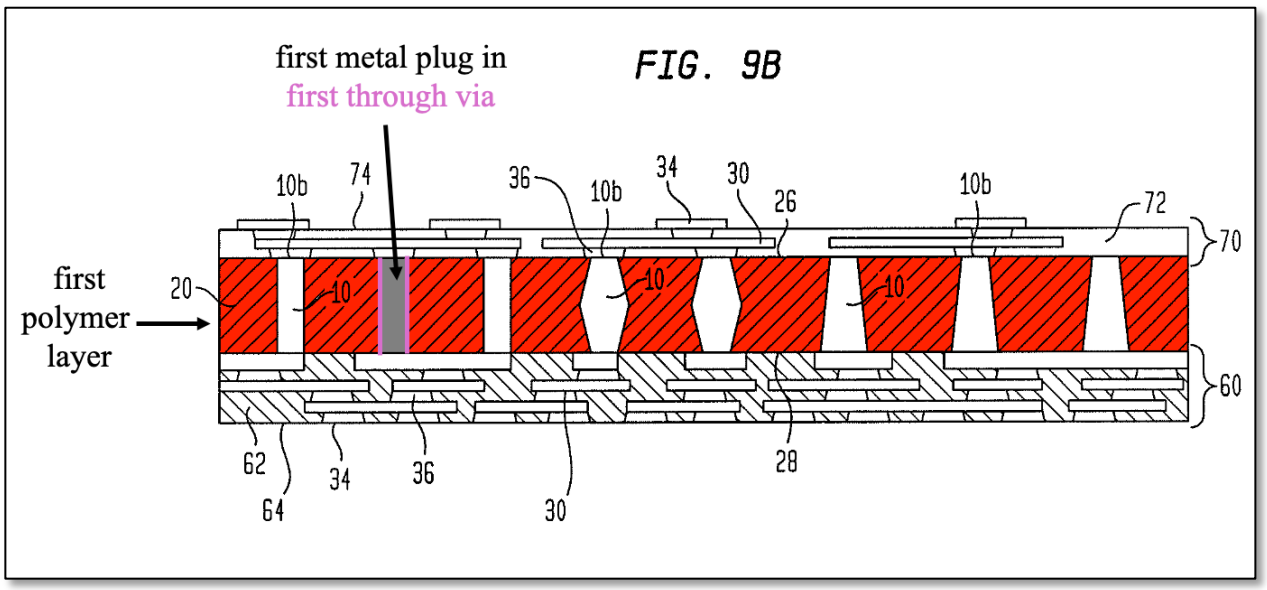
333. I note that during prosecution of the '768 Patent the Patent Owner provided an annotated FIG. 17B illustrating specification support for metal plug 21 being in a *through via*. Specifically, as shown below, the '768 Patent's metal plug 21 is shown as being in a through via within glass layer 16. As I will detail below, Haba's arrangement of posts 10 within dielectric layer 20 mirrors the arrangement depicted in the annotated FIG. 17B.



EX1002 at 537.

b) Haba's Teachings

334. Haba teaches that interconnection component 2 comprises "a **plurality of posts 10** within a dielectric layer 20" wherein "the "posts can be formed at locations facilitating connectivity between elements of a microelectronic assembly." *EX1009* at 5:33-35. The posts 10 "have end surface 10A and 10B" that "are left uncovered by the electric layer 20 on corresponding surface 28 and 26 thereof." *EX1009* at 5:25-30. In other words, posts 10 extend vertically between surface 26 and surface 28 within dielectric layer 20, shown below in FIG. 9B. Haba further teaches that "the posts can be made from copper." *EX1009* at 3:57-58. As such, Haba's posts 10 are *metal plug[s]*. A first post 10 (*first metal plug*) is shown below in FIG. 9B.



EX1009 at FIG. 9B.

335. The *first metal plug* is in a *first through via*, namely the area in Haba's *first polymer layer* where post 10 is located, as shown above. Haba's *through via* is

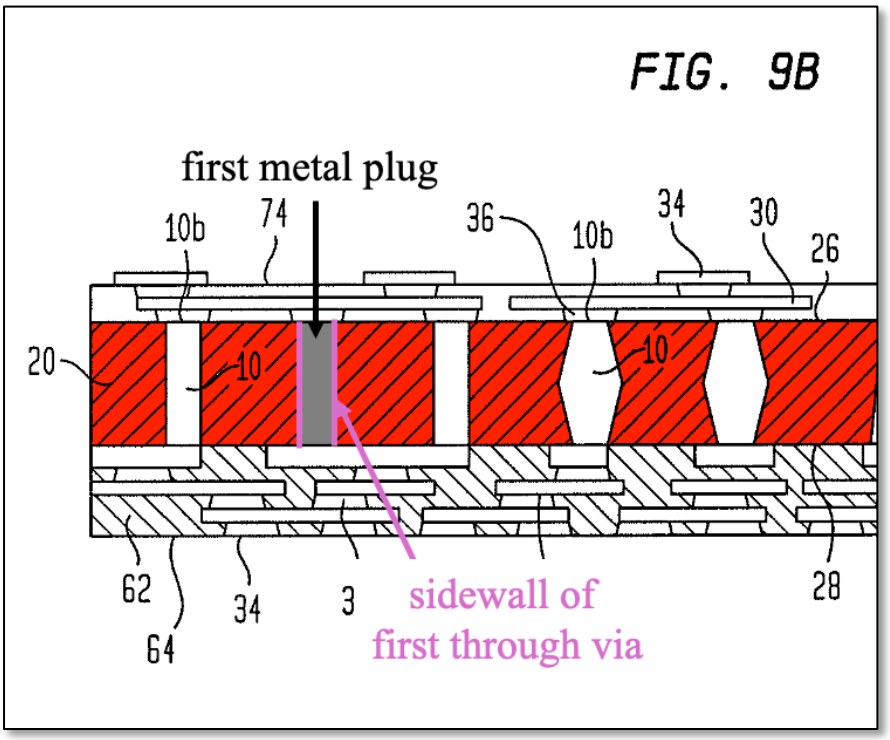
formed by the walls of dielectric layer 20 surrounding the copper post 10. In other words, the walls of dielectric layer 20 surrounding post 10 form a *through via* because they form a passageway (i.e., via) in dielectric layer 20 that extends vertically *through* dielectric layer 20 between surfaces 26, 28, thus, forming a *via* in the dielectric layer 20 in which posts 10 are located. Thus, Haba's post 10 is *a first metal plug vertically in a first through via in said first polymer layer*. Thus, like the '768 Patent, the *through via* is formed by the walls of the polymer layer surrounding the post 10.

336. I note that like the '768 Patent, Haba's metal posts carry current to "facilitat[e] connectivity between elements of a microelectronic assembly." *EX1009* at 5:23-35; *EX1001* at FIG. 9x (illustrating metal plugs connecting metal interconnects).

7. 1(b)(i): "wherein said first metal plug comprises a first copper layer, wherein the first copper layer contacts with a sidewall of said first through via;"

337. As described above, Haba expressly teaches that the "posts can be made from copper[,]" and Haba further teaches that posts 10 "can be fabricated from a single layer of the principal metal (e.g., **Cu** and the like)." *EX1009* at 2:57-58, 10:46-49, *see also* 2:37-38 ("The plurality of posts can be formed from materials such as…copper."). Thus, Haba's *first metal plug comprises a first copper layer*.

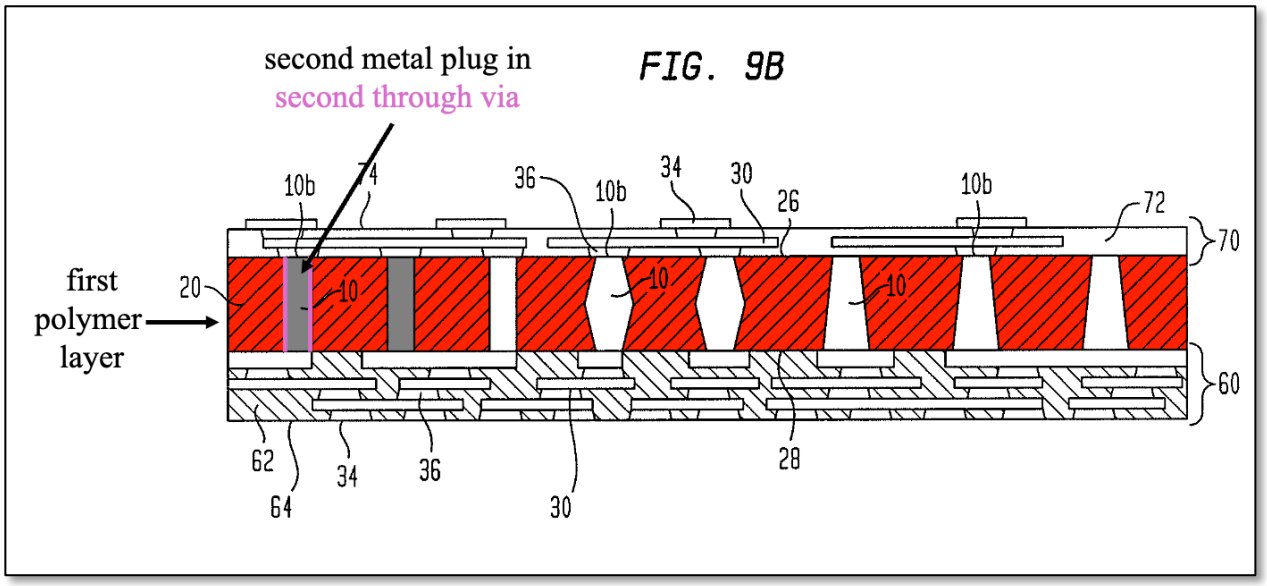
338. Additionally, Haba teaches that "dielectric layer 20 is formed over edge surfaces 14 of posts 10[.]" *EX1009* at 9:29-33. Indeed, the dielectric layer "directly contact[s] the edge surfaces" of posts 10. *EX1009* at 3:36-40, 1:49-50. The portions of dielectric layer 20 contacting edge surfaces 14 of posts 10 is a *sidewall of said first through via*. That is, the *through via* is the opening in dielectric layer 20, and the *through via* has a *sidewall* that forms the boundaries of the *through via*. *See* ¶ 335. Because dielectric layer 20 is formed "over edge surfaces 14 of posts 10[,]" the *sidewall* of the *through via* contacts posts 10. Further, because post 10 comprises *the first copper layer*, the *sidewall* of the *through via* contacts *the first copper layer*. *See* ¶ 337. Therefore, Haba teaches *wherein the first copper layer contacts with a sidewall of said first through via*.



EX1009 at FIG. 9B (excerpt).

8. 1(c): "a second metal plug vertically in a second through via in said first polymer layer,"

339. As discussed, Haba teaches a "plurality of posts 10 within a dielectric layer 20[.]" *See* ¶ 334. A second of Haba's posts 10, shown below, is therefore *a second metal plug vertically in a second through via in said first polymer layer* in the same way as described above at claim 1(b). *See* ¶¶ 334-336.



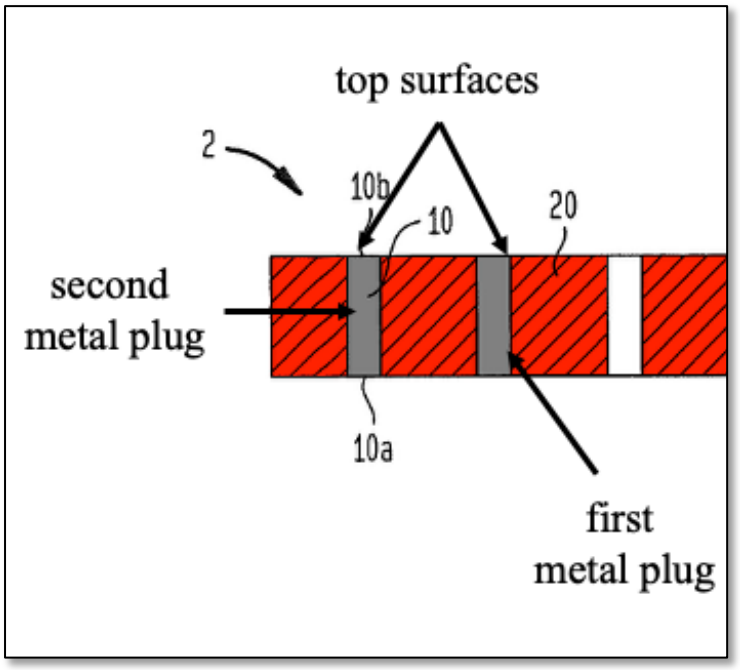
EX1009 at FIG. 9B.

9. 1(c)(i): "wherein said second metal plug comprises a second copper layer,"

340. Each of Haba's posts 10 are made from the same material (i.e., copper, per claim 1(b)(i)), thus Haba teaches that the *second metal plug comprises a second copper layer*. *See* ¶ 337.

10. 1(c)(ii): "wherein a top surface of said second metal plug and a top surface of said first metal plug are in the same horizontal plane;"

341. Haba teaches that surface 26 (*first surface*) is "coplanar with end surfaces 10B of the posts 10." *EX1009* at 10:8-10. Because Haba teaches (1) Posts 10 have end surfaces 10B that coplanar with surface 26, and (2) each post 10 has an end surface 10B, Haba teaches that each end surface 10B is coplanar with surface 26. Because each end surface 26 is coplanar with surface 26, end surface[s] 10B of each post 10 are also coplanar with each other. Because each end surface 10B is coplanar with every other end surface 10B, all end surfaces 10B *are in the same horizontal plane*. Thus, Haba teaches *wherein a top surface of said second metal plug* (end surface 10B of the *second metal plug*) *and a top surface of said first metal plug* (end surface 10B of the *first metal plug*) *are in the same horizontal plane*, as shown below.

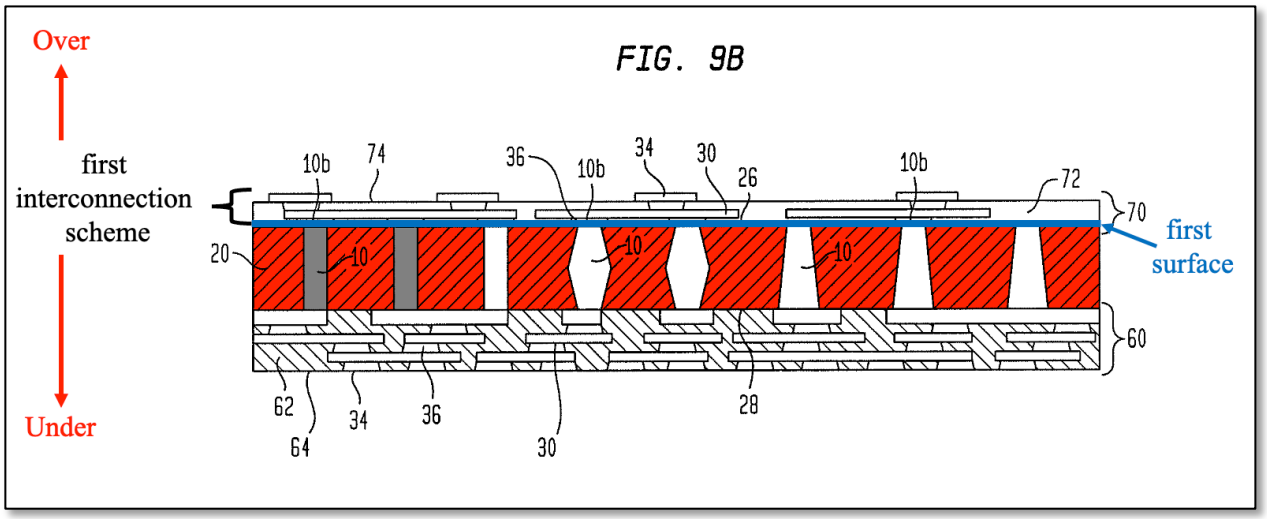


EX1009 at FIG. 6B.

11. 1(d): "a first interconnection scheme over said first surface,"

342. Haba teaches a "redistribution layer 70 formed along surface 26" (*first surface*) of dielectric layer 20. *EX1009* at 7:57-59. Redistribution layer (RDL) 70 "is similar to redistribution layer 60[,]" where RDL 60 comprises "multiple layers of traces 30 [that] are formed with a redistribution dielectric 62" and are "connected, as desired, between layers using conductive vias 36[.]" *EX1009* at 7:59-60, 7:1-8. Thus, like RDL 60, RDL 70 comprises various traces 30 and vias 36, which can be seen in FIG. 9B below. *EX1009* at 7:62-65, *see also* FIGS. 10A-10B. Haba further teaches "contacts or pads 34 [that] overlie portions of outside surface 74" of RDL 70, where "[p]ads 34 are connected to respective ones of end surfaces 10B by traces 30 and additional conductive vias 36 formed within redistribution dielectric 72."

EX1009 at 7:60-65. The collective various traces 30, vias 36, and pads 34 form a *first interconnection scheme*. Additionally, because the traces 30 and vias 36 are formed on surface 26 (*first surface*), and pads 34 "overlie portions of outside surface 74[,]" all of the traces 30, vias 34, and pads 34 are *over said first surface* (surface 26), as shown below. *EX1009* at 7:60-61.



EX1009 at FIG. 9B.

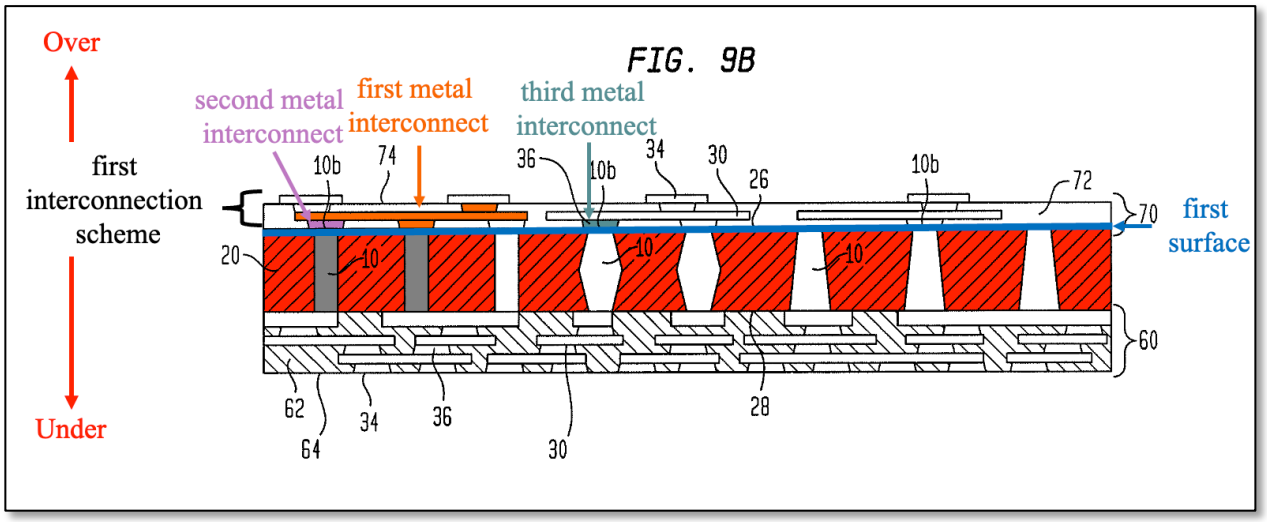
343. The collective various traces 20, vias 36, and pads 34 over surface 26 are an *interconnection scheme* because they collectively allow for "interconnect component 2 to be used to connect to a microelectronic element having a different connection configuration than the configuration of posts 10." *EX1009* at 7:27-31. 7:57-63 ("Redistribution layer 70 is similar to redistribution layer 60…"). Specifically, because "pads 34 are connected to respective ones of end surfaces 10B" of posts 10 by traces 30 and vias 36, the collection of pads 34, traces 30, and vias 36

allow for a microelectronic element to be electrically connected to interconnection component 2. *EX1009* at 7:63-65, 8:12-17 ("The embodiment of component 2 shown in FIG. 9B can be used in an assembly for attachment between a microelectronic element and a PCB in a similar arrangement as shown in FIGS. 10A and 10B, and can allow for an even greater difference in pitch between the conductive features of the microelectronic element and the PCB.").

12. 1(d)(i): "wherein said first interconnection scheme comprises a first metal interconnect over said first surface, a second metal interconnect over said first surface, a third metal interconnect over said first surface and a second polymer layer over said first, second and third metal interconnects"

a) First, Second, and Third Metal Interconnects

344. As described above, Haba's teaches various traces 30, vias 36, and pads 34 that are collectively a *first interconnection scheme*. *See* ¶¶ 342-343. Within the *first interconnection scheme* is *first metal interconnect* comprising the trace 30 and vias 36 that connect a pad 34 to the *first metal plug*, as shown below. *EX1009* at 6:56-62. Described above, Haba teaches that pads 34 "are connected to respective ones of end surfaces 10B by traces 30 and additional conductive vias 36[.]" *EX1009* at 7:60-65. Because the trace 30 and vias 36, shown below, connect contact pad 34 to *the first metal plug*, they are, collectively, a *first…interconnect*. For the same reasons, the vias 36 (pink, teal) are *second* and *third…interconnects*, respectively.



EX1009 at FIG. 9B.

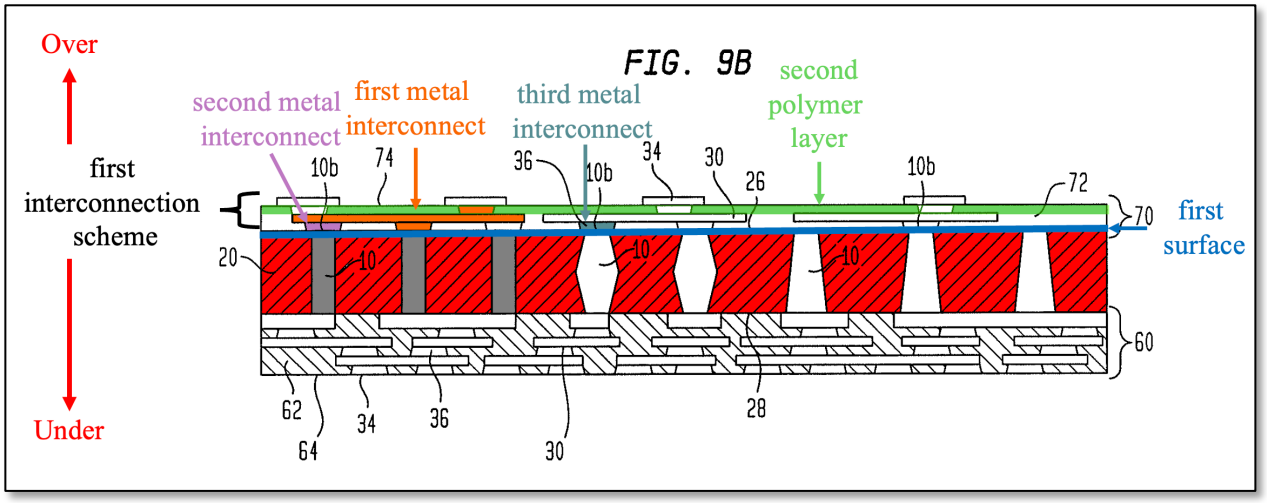
345. Haba additionally teaches that traces 30 are "formed from…metal." *EX1009* at 10:51-52. Further, Haba teaches that vias 36 are also made of metal. Specifically, Haba (1) refers to vias 36 as "wettable contacts[,]" (2) teaches that "wettable **metal** layers or structures…can be wettable contacts[,]" and (3) teaches that "[s]uch wettable metal layers or structures can be made from nickel[.]" *EX1009* at 7:34-36, 6:47-52. Thus, Haba's vias 36 also comprise *metal*, namely nickel. Because traces 30 and vias 36 comprise *metal*, Haba thus teaches that the *first*, *second*, and *third…interconnects*, are each *metal interconnect[s]*.

346. Finally, because Haba's *first*, *second*, and *third metal interconnect[s]* are formed over surface 26 (*first surface*) Haba thus teaches *a first metal interconnect over said first surface, a second metal interconnect over said first surface, a third metal interconnect over said first surface*.

b) Second Polymer Layer

(1) Haba's Teachings

347. Shown in FIG. 9B below, Haba's RDL 70 comprises a *second polymer layer* in the form of at least an uppermost portion of redistribution dielectric 72 that "traces 30 and…vias 36 are formed within." *EX1009* at 7:64-65. The redistribution dielectric is a "dielectric **layer** [formed] along the other surface" of the first dielectric layer 20, i.e., over surface 26. *EX1009* at 2:21-25. Indeed, Haba teaches that "interconnection component 2 can be completed by forming one or more redistribution layers, such as…redistribution layer 70 along surface 26." *EX1009* at 10:14-17. Because RDL 70 comprises redistribution dielectric 72, and because RDL 70 is formed "along surface 26" (i.e., over surface 26), redistribution dielectric 72 is also formed along surface 26 (*first surface*). Haba teaches dielectrics include "liquid-crystal **polymers**" such that dielectric 72 is *a second polymer layer*. *EX1009* at 6:19-26.



EX1009 at FIG. 9B.

348. Regarding RDL 60, Haba teaches that it "can be formed including traces 30 that are formed by etching away selected portions of layer 4 between the desired area for traces 30" then a "portion of redistribution dielectric 62 can then be applied along surface 28 between traces 30, and optionally, over traces 30." *EX1009* at 10:20-27. "Further traces 30 and portions of redistribution dielectric 62 can then be formed along with conductive vias 36 to form a multi-layer redistribution layer 60." *EX1009* at 10:28-31. Because redistribution dielectric 62 is formed between and **over** traces 30, redistribution dielectric 62 is a layer that is *over* the metal interconnects in RDL 60.

349. Because RDL 70 is "similar to redistribution layer 60[,]" a POSITA would understand that redistribution dielectric 72 is similarly formed *over* the traces 30 and vias 36 making up the *first*, *second*, and *third metal interconnects*, such that the upper most portion of redistribution dielectric 72 is a *second…layer* ***over*** *said first, second and third metal interconnects*. *EX1009* at 7:59-60. I note that Haba's teaching of redistribution dielectric 72 as being *over* each of the *first*, *second*, and *third metal interconnect[s]* is consistent with what is described by the '768 Patent. *See* ¶¶ 153-154.

(2) Lin-191's "Polymer" Teachings

350. Additionally or alternatively, shown below in FIG. 12, Lin-191 teaches a *polymer layer*, namely "encapsulating layer 85" which is a "polymer layer, such as epoxy layer, polyimide layer[.]" *EX1005* at [0109]. As shown, encapsulating layer 85 is formed over substrate 110 and *over* an *interconnection scheme* formed by "patterned metal layers 1" which provide "multiple metal interconnects or traces 1a[.]" *EX1005* at [0109].

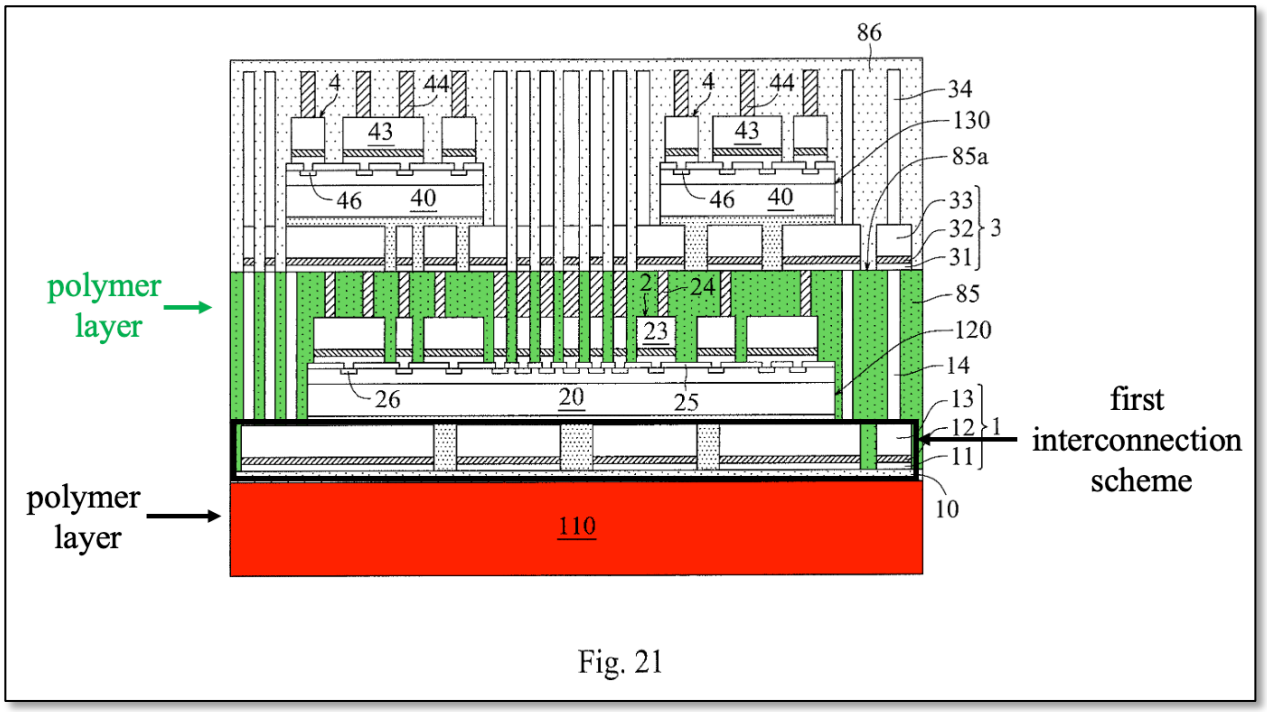


Fig. 21

EX1005 at FIG. 12.

351. Thus, Lin-191 teaches a *second polymer layer* formed *over* an interconnection scheme.

c) Motivation to Combine

352. Based on the teachings of Lin-191, a POSITA would have found it obvious and been motivated to modify Haba's redistribution dielectric (*second…layer*) to be a *polymer*, resulting in a *second polymer layer*. As I discussed above, Haba already teaches that dielectric layer 20 is a *polymer layer*, stating that dielectric layer 20 "can be formed from, for example, compositions which cure by chemical reaction to form a **polymeric** dielectric, such as epoxies and polyimides[.]" *EX1009* at 5:41-44 (emphasis added). *See* ¶ 316. Based on Lin-191's *second polymer layer*, a POSITA would have been motivated to likewise form Haba's redistribution dielectric 72 as a *polymer*, to form a multi-layer polymer interconnection component. That is, a POSITA would have looked to Lin-191's multi-layer polymer structure (encapsulating layer 85 is a *polymer layer* on substrate, which is also made of polymer) and been motivated to modify Haba such that redistribution dielectric 72 is a *second polymer layer* on a *first polymer layer*. *EX1005* at [0051], [0109]. Implementing redistribution dielectric layer 72 as a *polymer*, like Haba's disclosed dielectric layer 20 and Lin-191's layer 85, would have obtained the same advantages as otherwise already achieved with Haba's dielectric layer 20 being a polymer. *EX1009* at 5:41-51, 6:6-26.

353. Specifically, as described above, Haba recognizes that "when structures within an interconnection component have differing CTEs, the different amounts by which they expand and contract due to changing temperatures can apply stresses"

between dielectric layer 20 and posts 10 that leads to "delamination and cracking." *EX1009* at 6:6-10. A POSITA would have recognized that the copper traces 30 in the *metal interconnect[s]* within redistribution dielectric 72 (*second…layer*) would similarly be susceptible to CTE-mismatch stress-induced delamination and cracking, because traces 30 are made from the same material as Haba's posts 10 (copper). *See* ¶ 326. As such, a POSITA would have been motivated to implement redistribution dielectric 72 also as a *second polymer layer* to reduce such delamination and cracking between the copper traces 30 and redistribution dielectric 72, thereby "reducing the likelihood of bonding interface failures" in RDL 70. *EX1009* at 6:17-18. Similarly, a POSITA would have recognized that forming redistribution dielectric 72, like Haba's dielectric layer 20, as a *polymer* would have prevented delamination and cracking between RDL 70 and dielectric layer 20. Particularly, recall that like Haba's dielectric layer 20, Lin's encapsulating layer 86 may also be a "polymer layer, such as epoxy layer, polyimide layer[.]" *EX1005* at [0175]. Thus, delamination and cracking between RDL 70 (comprising redistribution dielectric 72) would be minimized due to CTE-matching between redistribution dielectric 72 and dielectric layer 20.

354. Additionally, a POSITA would have appreciated the electrical insulation that forming redistribution dielectric 72 of a *polymer* would provide, as both epoxy and polyimide are insulating materials. *EX1081* at 2:31-33 ("…the

electrically insulating matrix may include at least one of **polyimide**, silicone, **epoxy**…") (emphasis added). Electrical insulation would have been beneficial in RDL, as it was known that as "the size and spacing between [] electrically conductive interconnect lines decreases, the capacitance between closely spaced interconnects tends to increase, causing a generally commensurate increase in cross talk and power dissipation between adjacent interconnect lines. Cross talk is the signal interference between electrically conductive interconnect lines, which tends to adversely affect signal integrity and signal strength." *EX1086* at [0003]. As such, it was well known that "insulating layers can be formed between adjacent levels of conductors to prevent cross talk and capacitive coupling between conductors." *EX1087* at 2:27-29. Because epoxy and polyimide are both insulating materials, a POSITA would have recognized and appreciated the value of using an insulating *polymer layer* to thereby "prevent cross talk and capacitive coupling between conductors." *Id.*

355. Further, polymer layers were widely known for their flexibility and ease in patterning, thus allowing for complex interconnect structures to be formed therein. *EX1088* at 1:9-12 (Polyimide film is commonly used as a substrate for flexible circuits. Patterning such substrates primarily is accomplished by such process steps as mechanical punching or drilling, laser ablation, and chemical etching. Etched features such as vias or throughholes are commonly present in flexible circuits for reasons of interconnection."). Additionally, due to the mechanical properties of

polymer layers, metal interconnects formed within were protected from mechanical damage, because external forces applied to the chip package would be more easily dissipated by the polymer layer. *See, e.g., EX1089* at 1:20-25 ("In semiconductor devices, polyimide resins having excellent heat resistance and electrical properties as well as excellent mechanical properties have conventionally been used in surface protecting films and interlayer insulating layers."). Accordingly, a POSITA would have been motivated to implement redistribution dielectric 72 as a *polymer* per Lin-191 to thereby achieve the aforementioned benefits.

356. The modification is the application of a known technique (Lin-191's multi-polymer layers) to a known device (Haba's interconnection structure 2) ready for improvement to yield predictable results (e.g., forming dielectric of a material with a CTE closer to that of the surrounding materials to "thereby potentially reduc[e] the likelihood of bonding interface failures"). *EX1009* at 6:14-19. Specifically, forming redistribution dielectric 72 as a *second polymer layer* would have reduced the likelihood of bonding interface failure at both the redistribution dielectric 72-trace 30 interface as well as the redistribution dielectric 72-dielectric layer 20 interface. Further, methods of forming such polymer layers were widely known and well-established, as evidenced by Haba itself forming dielectric layer 20 in "the molding process." *EX1009* at 9:29-31. Lin-191 additionally teaches that a "molding process, a spin coating process, a lamination process, or a printing

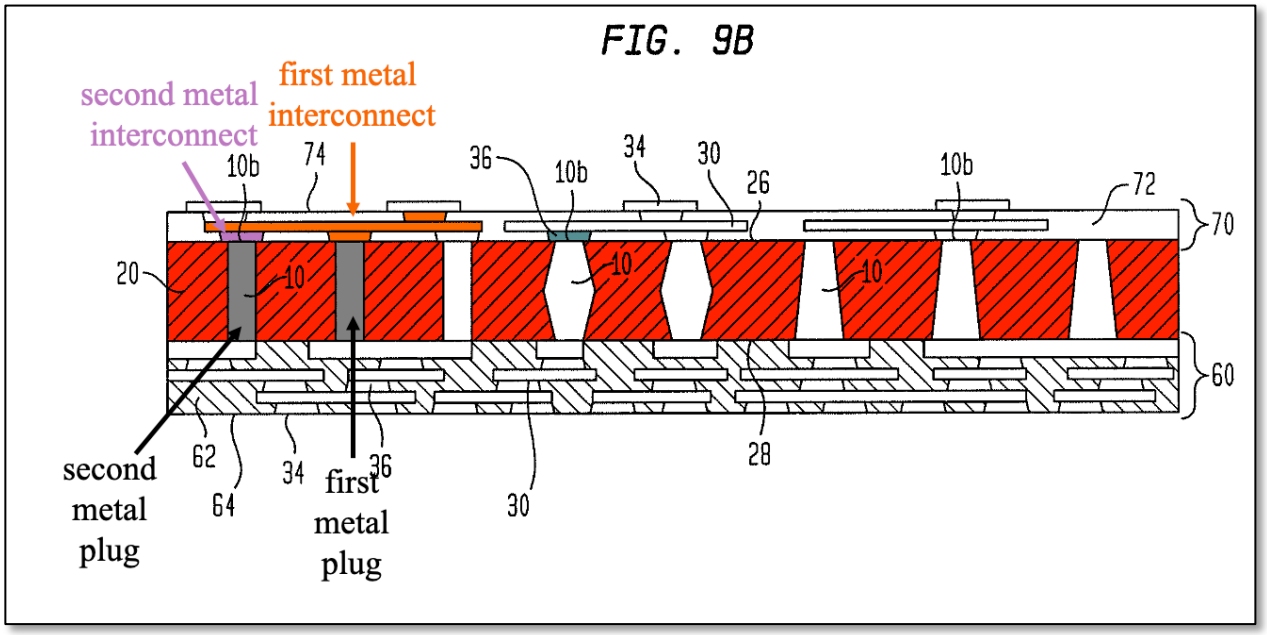
process" may be used to form a polymer layer. *EX1005* at [0109], [0175]. Because forming polymer layers was so well-known, a POSITA would have had a reasonable expectation of success in modifying Haba's redistribution dielectric 72 to be a *second polymer layer*.

13. 1(d)(ii): "wherein said first metal interconnect is connected to said first metal plug, wherein said second metal interconnect is connected to said second metal plug,"

357. As described above, Haba teaches that pads 34 "are connected to respective ones of end surfaces 10B by traces 30 and additional conductive vias 36[.]" *EX1009* at 7:60-65. *See* ¶ 344. Because traces 30 and vias 36 connect pads 34 to end surfaces 10B of posts 10, the trace 30 and vias 36 making up *the first metal interconnect*, are *connected to said first metal plug* (i.e., the first of post 10).

358. Specifically, as mapped above at claim 1(d)(i), Haba's *first metal interconnect* comprises a first via, a trace, and a second via. Because the first via, the trace, and the second via connect post 10 to pad 34, each of the first via, the trace, and the second via (*first metal interconnect*) are also connected to post 10 (*first metal plug*). Indeed, Haba repeatedly teaches that pads 34 are connected to end surfaces of posts 10 through traces 60 and vias 36. *See, e.g., EX1009* at 6:59-62 (As further shown in FIG. 8, wettable contacts can be provided as pads 34 electrically interconnected with end surfaces 10A through traces 30 and other electrically conductive structure, e.g., conductive vias 36."), 7:7-9 ("[T]races 30 are connected,

as desired, between layers using conductive vias 36, which are formed through portions of redistribution dielectric 60."), 6:62-65 ("In one example, traces 30 can electrically connect to and overlie respective end surfaces 10A…"), 7:60-65. For the same reasons, the *second metal interconnect is connected to said second metal plug*.



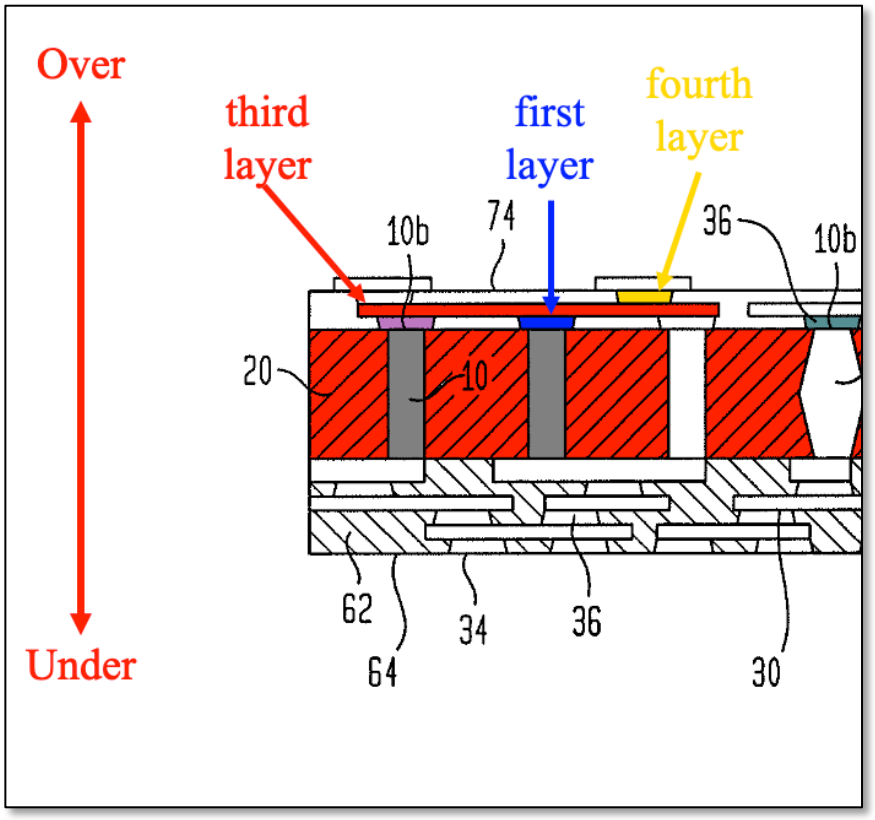
EX1009 at FIG. 9B.

14. 1(d)(iii): "wherein said first metal interconnect comprises a first metal layer, a third copper layer on said first metal layer, and a fourth copper layer on said third copper layer"

359. As I will detail below, Haba's *first metal interconnect* (i.e., the vias and trace connecting to the *first metal plug*) comprises various metal layers, as claimed. Additionally, Lin-191 similarly teaches a metal interconnect with various layers formed of *copper*, as claimed.

a) Haba's Teachings

360. Haba specifically teaches that the *first metal interconnect* comprises a *first…layer* (first via), *a third…layer on said first…layer* (trace on the first via), and *a fourth…layer* (second via) *on said third…layer* (trace):



EX1009 at FIG. 9B.

361. Regarding vias 36 (*first* and *fourth…layers*), recall that Haba teaches vias 36 as being *metal*, namely nickel. *See* ¶ 345. Specifically, Haba teaches that "wettable metal layers or structures can be added to interconnection component 2 that can be wettable contacts for connection to other microelectronic components[,]" where such "wettable metal layers or structures can be made from nickel or Ni–Au…." *EX1009* at 6:47-52. In other words, wettable contacts are formed from

wettable metal layers. Further, Haba refers to vias 36 as "wettable contacts." *EX1009* at 7:34-36 ("…wettable contacts formed by vias 36[.]"). Therefore, because Haba teaches that (1) wettable metal layers are wettable contacts, and (2) wettable contacts are vias, Haba teaches the vias 36 within the *first metal interconnect* are *metal*, thus teaching a *first metal layer*.

b) Lin-191's Teachings and Motivation to Combine

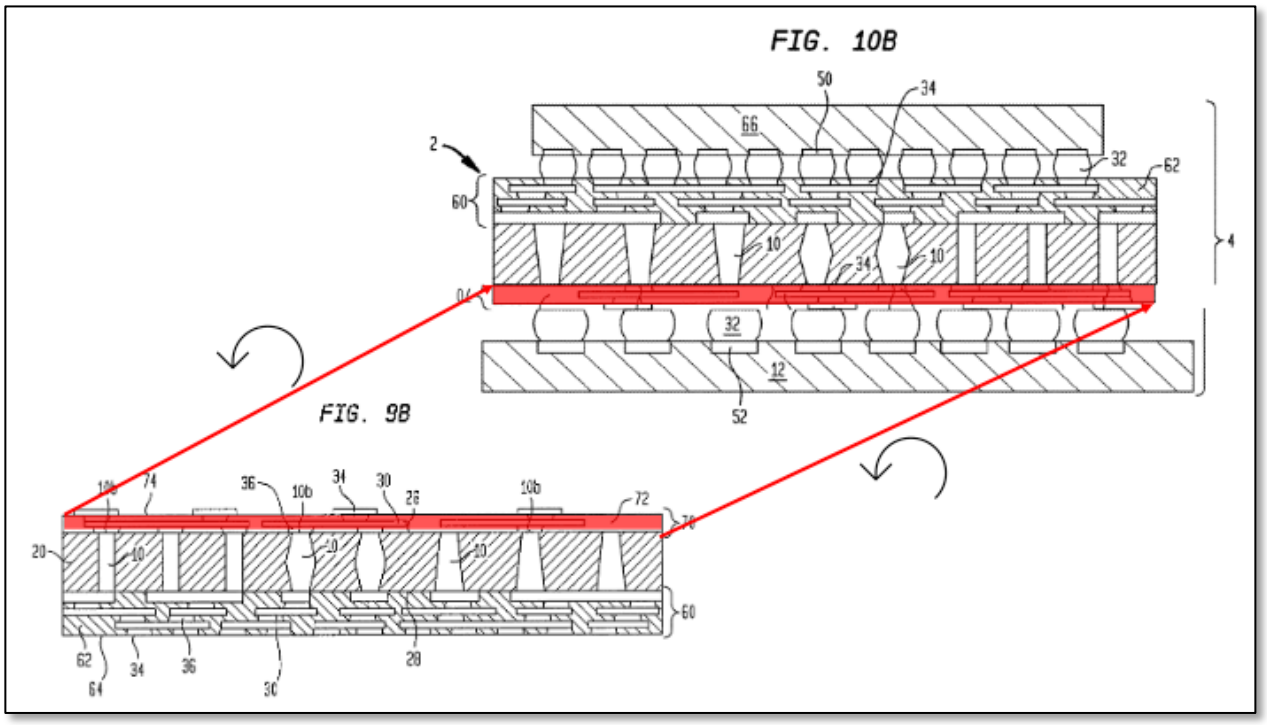
362. *See* ¶¶ 160-161 for Lin-191's teachings, incorporated herein. The MTCs and reasonable expectation of success for modifying Sundaram per Lin-191 apply for the Haba-Lin-191 combination as well. That is, due to the above-described advantages of Lin-191's metal interconnect layers, the application of Lin-191's interconnect to Haba's *first metal interconnect* would have been a straightforward design choice for a POSITA seeking to increase electrical and thermal performance. *See* ¶¶ 162-170, incorporated herein.

15. 1(e): "a first metal bump over said first interconnection scheme and said second metal plug,"

a) Haba's Teachings

363. Recall that a POSITA would have understood that because Haba teaches the "embodiment of component 2 shown in FIG. 9B can be used in an assembly for attachment between a microelectronic element and a PCB in a similar arrangement as shown in FIGS. 10A and 10B[,]" that Haba teaches RDL 70 of FIG. 9B may be included in the FIG. 10B embodiment, such that RDL 70 is positioned

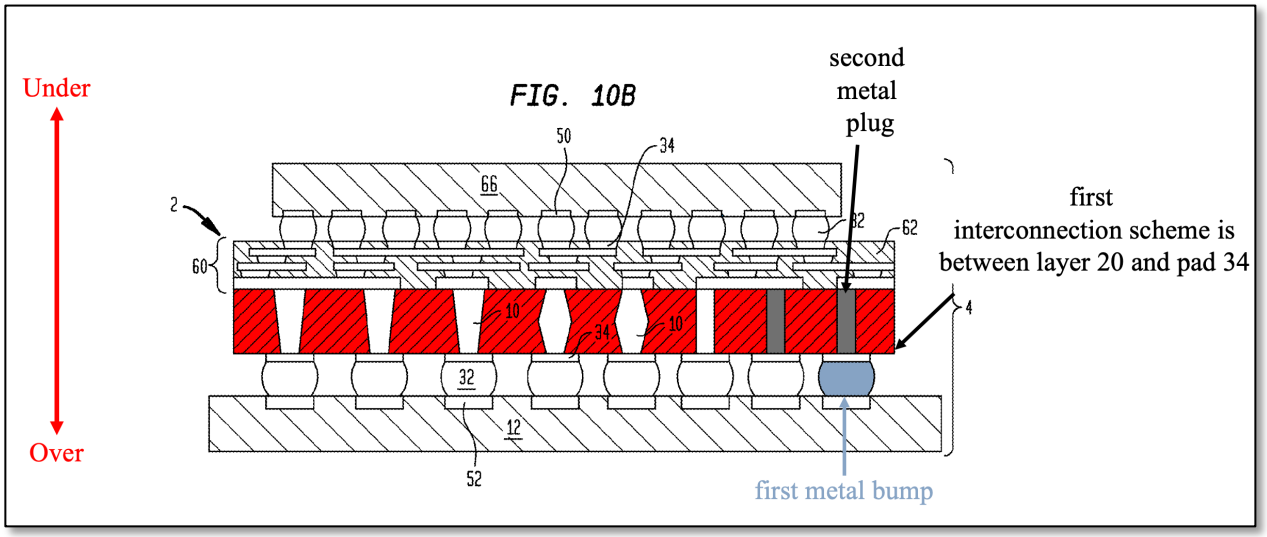
over surface 26, between dielectric layer 20 and PCB 12. Alternatively, a POSITA would have been motivated and found it obvious to modify the FIG. 10B embodiment to include FIG. 9B's RDL 70. *See* ¶¶ 306-312. In other words, "a second redistribution layer 70 formed along surface 26" as shown in FIG. 9B would be similarly formed over the *first surface* in FIG. 10B, shown below.



EX1009 at FIGS. 9B, 10B.

364. Additionally, recall that FIG. 10B is "inverted with respect to the depiction of FIG. 8" and is likewise inverted with respect to FIG. 9B, which depicts "an interconnection component that includes additions to the embodiment of FIG. 8." *EX1009* at 7:42-56, 5:1-3. Thus, in the above image, RDL 70 of FIG. 9B is flipped according to FIG. 10B's inversion relative to FIG. 9B. *See* ¶¶ 307-308.

365. Based on such teachings, i.e., because RDL 70 is positioned in the "under" direction relative to solder balls 32 in FIG. 10B, Haba teaches *a first metal bump over said first interconnection scheme and said second metal plug*, namely a solder ball 32, shown below.



EX1009 at FIG. 10B.

366. Haba teaches that "pads 34 which overlie end surfaces 10B act as wettable contacts for attachment to contacts 52 of PCB 12 using **solder balls 32**." *EX1009* at 7:54-56. Because a POSITA would understand RDL 70 of FIG. 9B to be formed on the *first surface* as shown above in FIG. 10B, each of solder balls 32 are *over said first interconnection scheme*. Specifically, as depicted by the red arrow indicating the over/under directions relative to FIG. 9B, solder balls 32 are *over* where Haba teaches RDL 70 is formed in the FIG. 10B embodiment. Further, the solder ball 32 (*first metal bump*) is *over* the *second metal plug* for the same reason.

367. Accordingly, Haba teaches *a first metal bump over said first interconnection scheme and said second metal plug*.

16. 1(e)(i): "wherein said first metal bump comprises a tin-containing layer; and"

a) Haba's Teachings

368. One of Haba's solder balls 32 is the *first metal bump*. *See* claim 1(e), ¶¶ 363-367. A POSITA would have understood Haba's "solder" to comprise a *tin-containing layer* for the same reasons described above. *See* ¶ 172, incorporated herein.

b) Lin-191's Teachings and Motivation to Combine

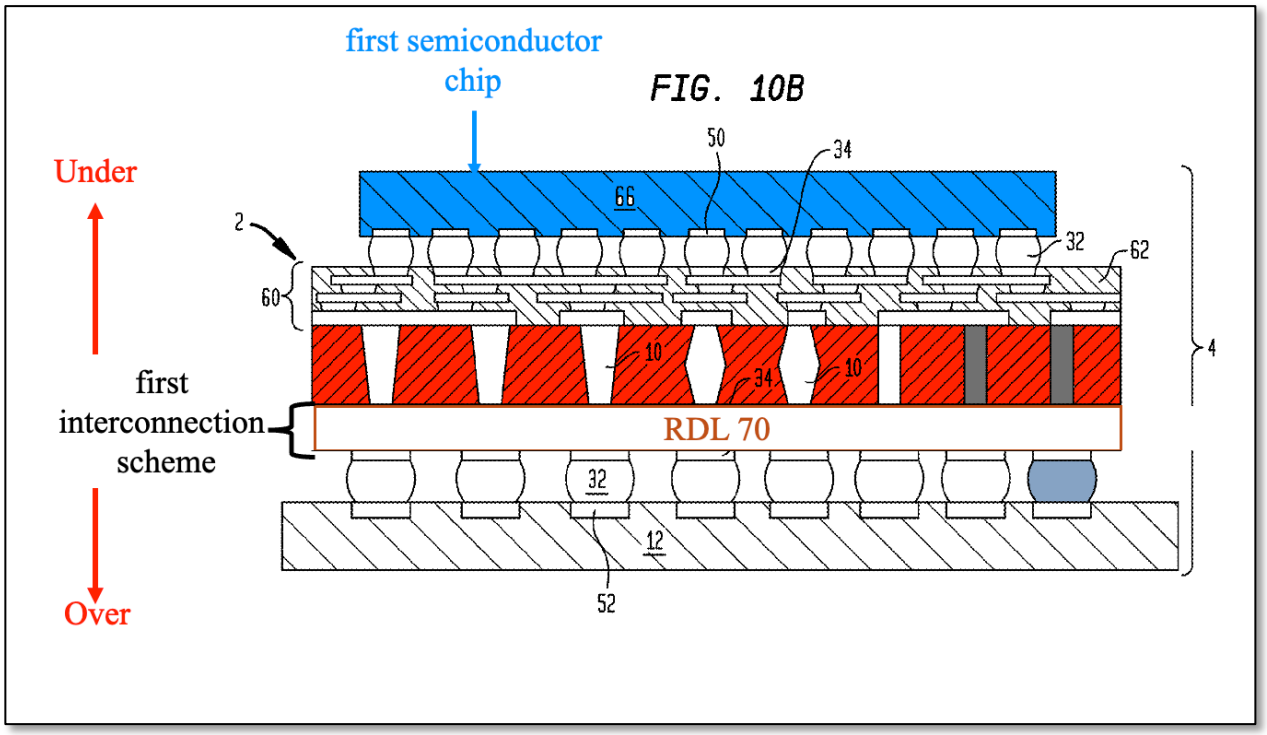
369. Additionally or alternatively to Haba, Lin-191 teaches a "solder layer 29 [that] can be…a **tin-containing layer**[.]" *EX1005* at [0320]. *See* ¶¶ 173-174, incorporated herein. For the same MTCs and with the same reasonable expectation of success, a POSITA would have found it obvious and been motivated to modify Haba's solder ball 32 (*first metal bump*) to comprise a *tin-containing layer*. *See* ¶¶ 175-179.

17. 1(f): "a first semiconductor chip under said first interconnection scheme,"

370. Haba teaches a "microelectronic element 66" which may be "one or more semiconductor chips[.]" *EX1009* at FIG. 10B, 7:42-56, 1:19-22. Haba thus teaches a *first semiconductor chip*.

371. Recall that a POSITA would have understood that because Haba teaches the "embodiment of component 2 shown in FIG. 9B can be used in an assembly for attachment between a microelectronic element and a PCB in a similar arrangement as shown in FIGS. 10A and 10B[,]" that Haba teaches RDL 70 of FIG. 9B may be included in the FIG. 10B embodiment, such that RDL 70 is positioned *over* surface 26, between dielectric layer 20 and PCB 12. *See* ¶¶ 306-307. In other words, "a second redistribution layer 70 formed along surface 26" as shown in FIG. 9B would be similarly formed over the *first surface* in FIG. 10B. Alternatively, POSITA would have found it obvious and been motivated to combine the FIG. 9B and 10B embodiments such that RDL 70 of FIG. 9B is positioned between dielectric layer 20 and PCB 12. *See* ¶¶ 309-312.

372. Because RDL 70 is positioned between dielectric layer 20 and PCB 12, Haba teaches that microelectronic element 66 (*first semiconductor chip*) is *under* RDL 70 and is therefore *under said first interconnection scheme* (i.e., because the *first interconnection scheme* comprising traces 30, vias 36, and pads 34 are in and on RDL 70). *See* claim 1(d), ¶¶ 342-343. That is, as depicted by the red arrow indicating the over/under directions, microelectronic element 66 is *under* where RDL 70 is positioned.



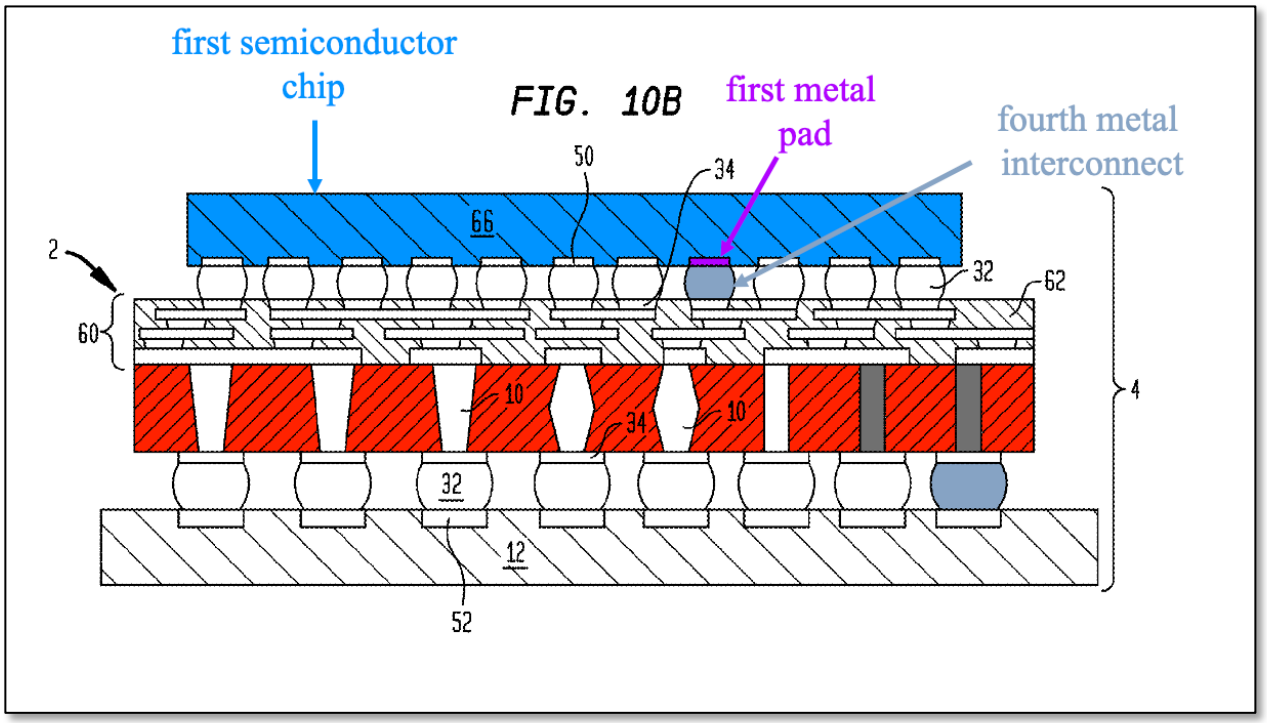
EX1009 at FIG. 10B.

18. 1(f)(i): "wherein said first semiconductor chip comprises a fourth metal interconnect on a first metal pad of said first semiconductor chip,"

a) Haba's Teachings

373. As shown in FIG. 10B, end surfaces 10B of posts 10 "are used to join posts 10 to solder balls 32, which are, in turn, joined to contacts 50 on a microelectronic element 66." *EX1009* at 6:42-44, 7:52-56 (The embodiment of FIG. 10B is similar to that which is shown in FIG. 10A…"). Indeed, contacts 50 of the *first semiconductor chip* "are joined to contacts or pads of interconnection component 2[,]" which, as seen below, is achieved via solder balls 32. *EX1009* at 7:50-51; FIG. 10B.

374. Microelectronic element 66 is therefore connected to RDL 60 via a solder ball 32. Because microelectronic element 66 comprises solder ball 32 which connects microelectronic element 66 to RDL 60, solder ball 32, as depicted below, is a *fourth metal interconnect* that is *on a first…pad* (contact 50) *of said first semiconductor chip*.



EX1009 at FIG. 10B.

375. Further, Haba was familiar with metal pads in chip packaging, teaching that contact pads 34 can be "wettable metal layer or structures[.]" *EX1009* at 6:50-55. As such, a POSITA would have understood contact 50 (*first…pad*) to likewise be metal, as semiconductor chips having *metal* contact pads was standard. *See, e.g., EX1044* at 2:30-33 ("In FIG. 1, a **metal pad** 12 is formed on a semiconductor

material 10. Metal pad 12 may be formed from a conductive metal…"); *EX1045* at [0006] ("FIG. 1 illustrates a portion of flip chip 10 with a solder bump 12 formed on **metal contact pad** 14."); *EX1046* at [0018] ("Bumps 105 electrically and possibly physically contact the I/O pads (**metal pads**) 103 of the IC chip 100."); *EX1095* at ("I/O terminals were **traditionally** formed by way of **metal pads** along the periphery of an IC.").

b) Lin-191's "Metal Pad" Teachings and Motivation to Combine

376. *See* ¶ 183 for Lin-191's teachings, incorporated herein. For the same MTCs and with the same reasonable expectation of success, a POSITA would have found it obvious and been motivated to implement, per Lin-191, Haba's contact 50 (*first…pad*) as *metal*, yielding a *first metal pad*. *See* ¶¶ 184-185.

19. 1(f)(ii): "wherein said fourth metal interconnect comprises a second metal layer on said first metal pad and a fifth copper layer over said second metal layer, wherein said fifth copper layer has a thickness between 5 and 30 micrometers,"

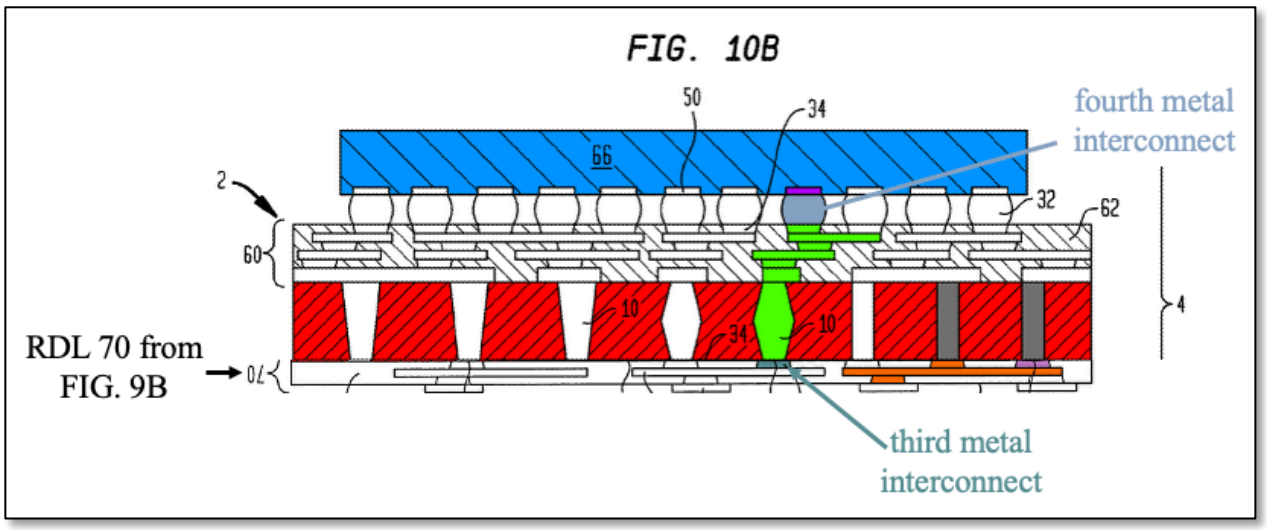
a) Lin-191's Teachings and Motivation to Combine

377. Lin-191 teaches or renders obvious interconnects/bumps with layers/thickness as recited in Claim 1(f)(ii). *See* ¶ 186-187, incorporated herein. A POSITA would have found it obvious and been motivated to, with the same reasonable expectation of success, modify Haba's *fourth metal interconnect*, per Lin-191, to comprise *a second metal layer on said first metal pad and a fifth copper layer over said second metal layer, wherein said fifth copper layer has a thickness*

between 5 and 30 micrometers. As I described above, Lin-191's layered bump structure would improve long-term solder ball performance by preventing unwanted diffusion of materials and improving mechanical integrity of the solder ball. *See* ¶¶ 188-194, incorporated herein. Additionally, the thickness of Lin-191's metal layer 713 (*fifth copper layer*) would have allowed ample space for an underfill material to be positioned between Haba's microelectronic element 66 and RDL, which would have further improved solder ball performance for the same reasons described above. *See* ¶ 192.

20. 1(f)(iii): "wherein said fourth metal interconnect is connected to said third metal interconnect."

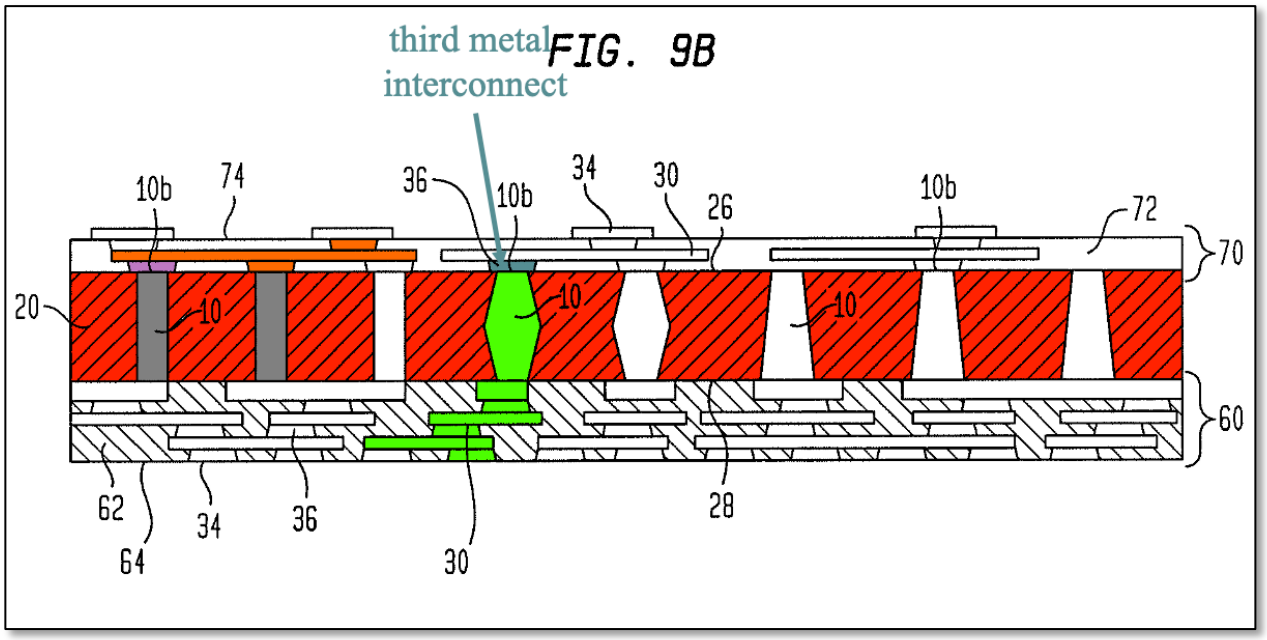
378. Recall that the *fourth metal interconnect* is Haba's solder ball 32, modified per Lin-191, connecting microelectronic element 66 to RDL 60. *See* ¶ 374. Haba's solder ball 32, through RDL 60, is thus connected to a post 10 in dielectric layer 20:



EX1009 at FIG. 10B.

379. Further recall that a POSITA would have understood that because Haba teaches the "embodiment of component 2 shown in FIG. 9B can be used in an assembly for attachment between a microelectronic element and a PCB in a similar arrangement as shown in FIGS. 10A and 10B[,]" that Haba teaches RDL 70 of FIG. 9B may be included in the FIG. 10B embodiment, such that RDL 70 is positioned *over* surface 26, between dielectric layer 20 and PCB 12. *See* ¶¶ 306-307. In other words, "a second redistribution layer 70 formed along surface 26" as shown in FIG. 9B would be similarly formed over the *first surface* in FIG. 10B. Alternatively, POSITA would have found it obvious and been motivated to combine the FIG. 9B and 10B embodiments such that RDL 70 of FIG. 9B is positioned between dielectric layer 20 and PCB 12. *See* ¶¶ 309-312.

380. Because Haba's RDL 70, including the *third metal interconnect*, is formed on *the first surface* of FIG. 10B, the same post 10 identified in the above FIG. 10B is connected to the *third metal interconnect*:



EX1009 at FIG. 9B.

381. Finally, because Haba's solder ball 32 (*fourth metal interconnect*) and Haba's *third metal interconnect* are both connected to the same post 10, Haba teaches *wherein said fourth metal interconnect is connected to said third metal interconnect*.

C. *Claim 2: "The chip package of claim 1, further comprising a passive component over said first interconnection scheme and connected to said first interconnection scheme through a solder layer."*

a) Lin-191's Teachings

382. As discussed in detail herein, Lin-191 teaches two embodiments relevant to Claim 2's mapping, namely the FIG. 55 embodiment and the FIG. 84 embodiment. In the FIG. 55 embodiment, Lin-191 teaches chip 140 "can be replaced by a passive component 67," where the passive component is "connected to the metal

layer 53 of the patterned metal layer 5 **through** two solder joints 68."[5] *EX1005* at [0340], FIG. 55. Shown in FIG. 55 below, Lin-191 teaches a "passive component 67, such as a capacitor, inductor, or resistor." *EX1005* at [0341]. Passive component 67 is "connected to the metal layer 53 of the patterned metal layer 5 through two solder joints 68." *EX1005* at [0340]. Like Lin-191's patterned metal layer 3 discussed above at claim 1(d)(iii), patterned metal layer 5 comprises a nickel "adhesion layer 51", a copper "seed layer 52", and a copper "metal layer 53." *EX1005* at [0198]-[0199], [0214] (layer 5 includes a metal interconnect), *see* ¶ 362. Thus, Lin-191's *passive component* is connected to a metal interconnect in an *interconnection scheme* with the same structure as achieved in the Claim 1(d)(iii) combination. Additionally, Lin-191 provides specificity to solder joint 68, teaching that they "may include bismuth, indium, tin-lead alloy, tin-silver alloy, tin-silver-copper alloy, or tin-gold[,]" thereby teaching a *passive component* connected to a metal interconnect through a *solder layer*. *See* ¶¶ 71-76.

[5] The textual description of FIG. 84 at [0439] does not discuss chip and layers, but Lin-191 states that "[w]hen the same numeral appears in different drawings, it refers to the same or like components or steps." *EX1005* at [0013]. Therefore, Lin-191's discussion of FIG. 55 and chip 140 and layers 5 is applicable to the FIG. 84 embodiment.

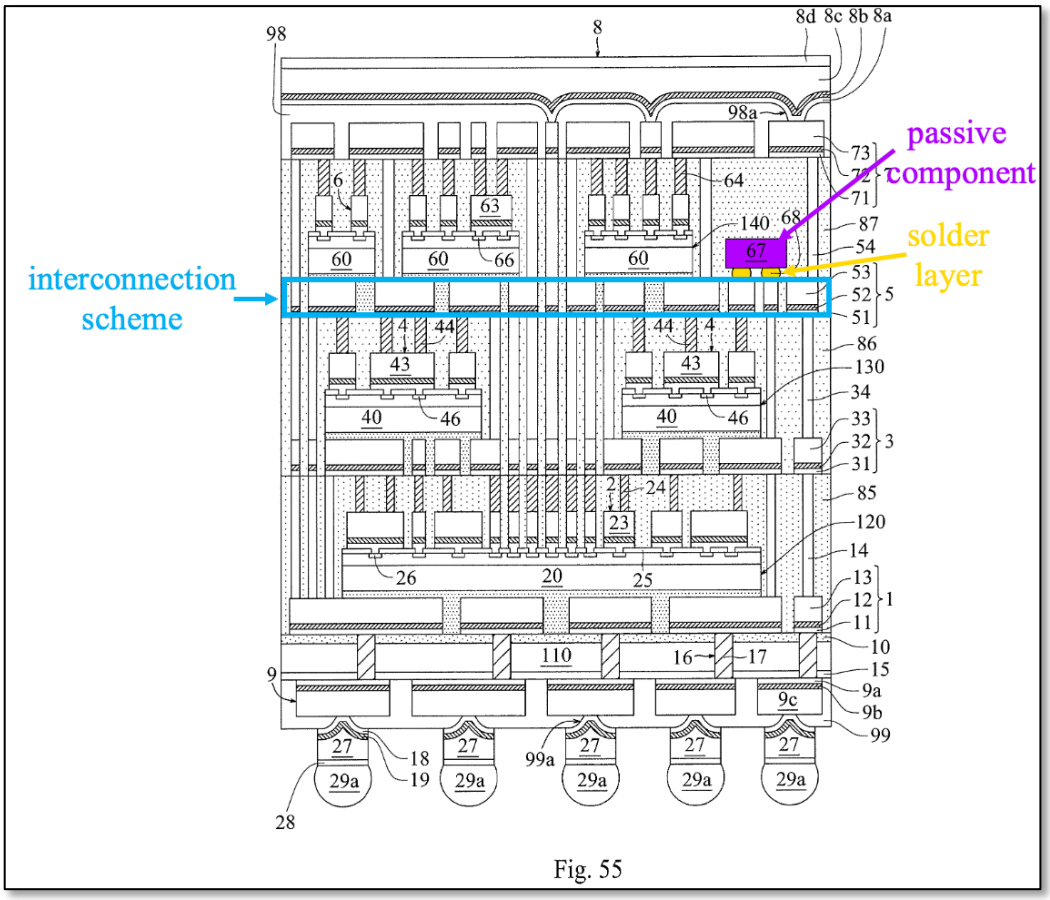


Fig. 55

EX1005 at FIG. 55.

383. In the FIG. 84 embodiment, Lin-191 teaches that chip 140 is *over* and connected to patterned metal layer 5 (an *interconnect* in Lin-191's *interconnection scheme*). *EX1005* at FIG. 84, [0273], [0340]. That is, chip 140 is *over* patterned metal layer 5 because it is towards the solder balls 29a which connect to a PCB and is therefore in the "over" direction as depicted by the red arrow. *EX1005* at [0439].

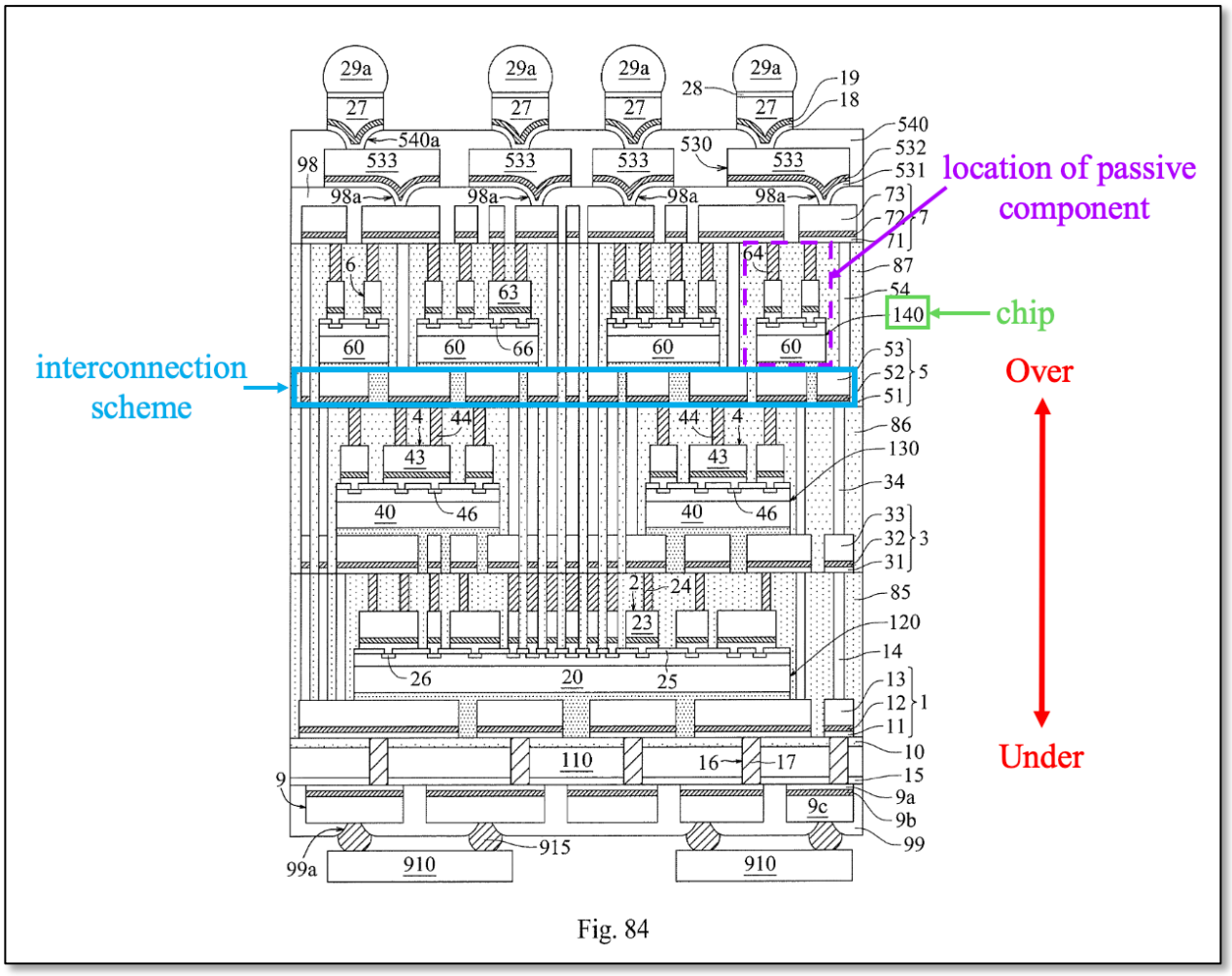


Fig. 84

EX1005 at FIG. 84.

384. Based on Lin-191's express teaching and motivation that "one of the chips 140" can "be replaced by a passive component 67[,]" a POSITA would have found it obvious and been motivated to replace the chip 140 in FIG. 84 with passive component 67, thereby teaching or rendering obvious *passive component* (passive component 67) *over said first interconnection scheme* (layers 5). That is, when chip 140 in FIG. 84 is replaced with passive component 67, the *passive component* is *over* Lin-191's *interconnection scheme* for the same reasons as discussed above for chip

140. *See* ¶ 383. When chip 140 is replaced with passive component 67, a POSITA would have found it obvious to connect passive component to Lin-191's *interconnection scheme* (patterned metal layer 5) through a *solder layer* (solder joints 68) as taught by Lin-191. *See* FIG. 55, [0340] ("The passive component 67 can be connected to the metal layer 53 of the patterned metal layer 5 through two solder joints 68."). A POSITA would have been motivated to position passive component 67 in place of chip 140 because passive components, such as a capacitor, were known to preserve the integrity of signals from various chips travelling to the PCB. *See, e.g., EX1048* at [0001] ("Chips such as Application Specific Integrated Circuits [] often include power and ground connections to the circuit board. Capacitors, often referred to as 'bypass capacitors' or 'decoupling capacitors,' are usually coupled across the power and ground connections to filter out unwanted electrical noise that may be generated by the power supply. The bypass capacitors may be disposed on the bottom side of circuit board within the footprint of the ASIC."). The modification is the application of a known technique (a passive component connected to an interconnection scheme via a solder joint) to a known device (Lin-191's package) to yield the predictable result of Lin-191's FIG. 84 embodiment having a passive component 67 in place of a chip 140.

385. Further, in the modified FIG. 84 embodiment, multiple passive components, namely passive component 67 and passive component 910 are

provided. A POSITA would have found it obvious to include multiple passive components in the chip package at various locations, because such a practice was advantageous for preserving signal integrity throughout the entire chip package. *EX1090* at [0010] ("As the internal circuitry of high performance ICs, such as processors, operates at higher and higher clock frequencies, noise in the power and ground lines increasingly reaches an unacceptable level. This noise can arise due to inductive and capacitive parasitics, for example, as is well known. To reduce such noise, capacitors known as decoupling or by-pass capacitors are often used to provide a stable signal or stable supply of power to the circuitry."). For example, a POSITA would have recognized that positioning passive component 67 in place of chip 140 would preserve the signal integrity of the chip 130 positioned under passive component 67, by filtering out "unwanted electrical noise" from signals traveling from chip 130 toward solder balls 29a, which connect to a printed circuit board. *EX1048* at [0001]; *EX1005* at [0348].

b) Motivation to Combine

386. Based on Lin-191's teachings, a POSITA would have found it obvious and been motivated to modify Haba's chip package to comprise a *passive component* (e.g., passive component 67) *over* the *first interconnection scheme* and connected to a metal interconnect through a *solder layer* (solder joints 68). In the combination, the *passive component* is positioned between dielectric layer 20 and PCB 12, taking

the place of some of solder balls 32, thus parallel to the remaining solder balls 32. A POSITA would have appreciated that by connecting a passive component, e.g., a capacitor, over Haba's RDL 70, Haba's chip package would advantageously preserve the integrity of signals from microelectronic element 66 traveling to the PCB 12. As I described above, passive components, such as capacitors, were known to ensure signal quality and integrity because the capacitor maintains transmission line integrity, thereby suppressing distortion in such signals prior to transmission to the PCB. *See* ¶ 385. Indeed, "by use of bypass capacitors on multi-layer printed circuit boards, the total area of the current loop formed by the signal trace and its return current can be minimized. Signal integrity, which is influenced by factors such as impedance, inductive crosstalk to other signals, signal transmission line reflection, and balance, can be improved and noise can be well controlled." *EX1049* at 7:11-19. Additionally, capacitors were known to provide "less noisy power being supplied" to chips in a chip package by "providing a low inductance path between power and ground." *EX1050* at 5:37-41. As such, a POSITA would appreciate both the improvement in signal integrity and reduction in power noise due to the low-inductance path provided by the *passive component*. Further, including a passive component, such as a capacitor, would reduce the impact of high frequency interference (HFI) on digital signals being transmitted between microelectronic element 66 (*first semiconductor chip*) and PCB 12, as well as reduce the negative

impact of HFI on power supply lines in Haba's chip package, thereby further preserving signal integrity. Specifically, "when events take place that have frequency higher than what can be accommodated by a voltage regulator, noise occurs." *EX1100* at [0004]. A capacitor "works as backup energy storage" that can "quickly provide the shortfall" if the voltage drops due to such high frequency events. *EX1100* at [0004].

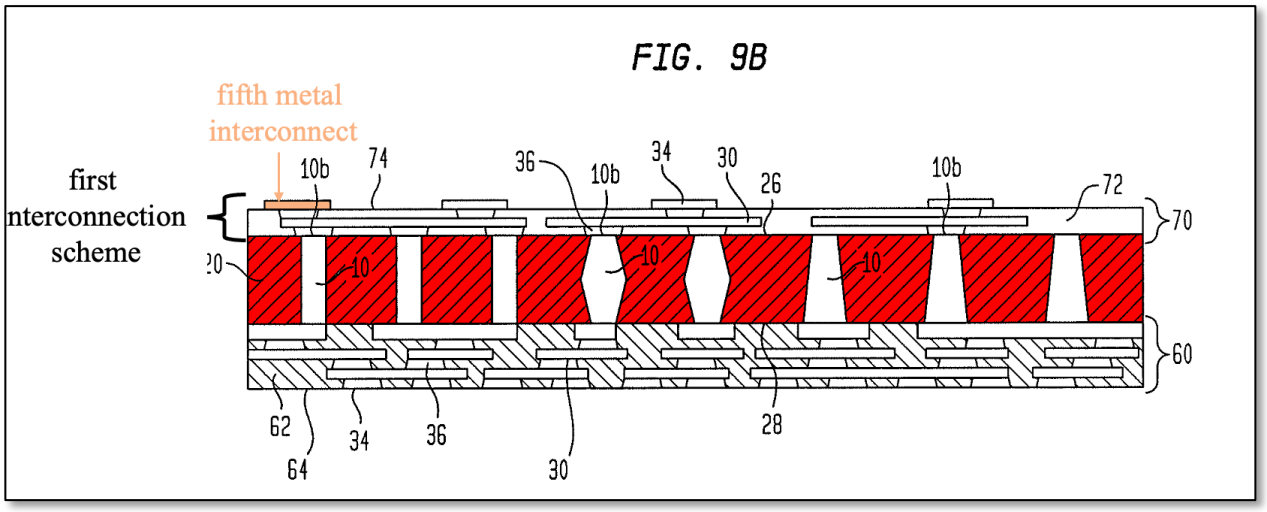
387. The modification is the application of a known technique (implementing a passive component) to a known device (Haba's chip package) to yield the predictable result of Haba's chip package having a passive component. Further, a POSITA would have had a reasonable expectation of success in including a *passive component* in Haba's chip package, because soldering passive components into chip packages was a very well-known technique, as demonstrated by Lin-191 and others. *See, e.g., EX1051* at FIG. 14, [0093] ("…chip capacitor 213 are provided with a power electrode 214 to be connected to the power internal electrode layer and the power solder bump 217…and the ground solder bump 220."), Furthermore, the inclusion of passive components such as Lin-191's was a ubiquitous practice in chip packaging, thus making the modification simple, straightforward, and routine, thereby further evidencing the reasonable expectation of success. *See, e.g., EX1052* at FIG. 2, [0025] ("The flip-chip BGA package 4 further comprises an RC passive component 41 such as a resist or a capacitor…"); *EX1053* at [0030] ("In some

embodiments, electronic components such as the component 180 can comprise passive components (e.g., resistors, capacitors, inductors)…").

D. *Claim 3: "The chip package of claim 1, wherein said first interconnection scheme comprise a fifth metal interconnect across over a sidewall of the first semiconductor chip."*

a) Fifth Metal Interconnect

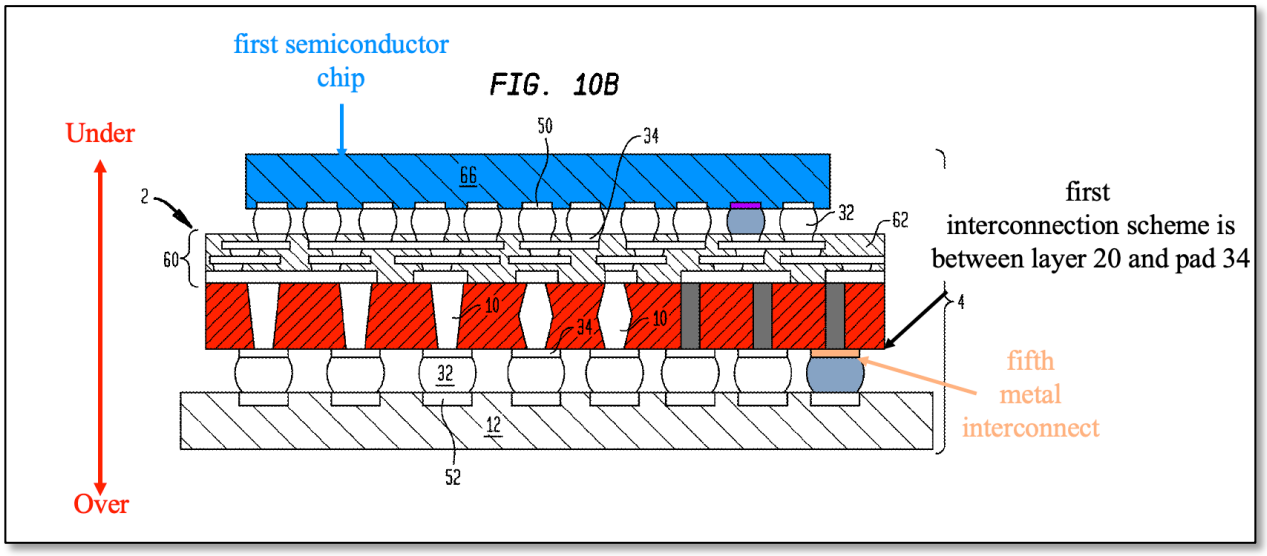
388. Recall that Haba's *first interconnection scheme* comprises various traces 30, vias 36, and pads 34. *See* ¶¶ 342-343. One of Haba's pads 34 is a *fifth metal interconnect* of the *first interconnection scheme* because Haba teaches "pads 34 which overlie end surfaces 10B [and] act as wettable contacts for attachment to contacts 52 of PCB 12 using solder balls 32." *EX1009* at 7:54-56. Recall that Haba teaches that "wettable **metal** layers or structures…can be wettable contacts[,]" and teaches that "[s]uch wettable metal layers or structures can be made from nickel[.]" *EX1009* at 7:34-36, 6:47-52. *See* ¶ 345. Thus, because Haba teaches "pads 34…act as wettable contacts[,]" pads 34 are *metal*, namely "Nickel or Ni–Au[.]" *EX1009* at 6:50-55.



EX1009 at FIG. 9B

389. Further regarding pads 34, Haba teaches "contacts or pads 34 overlie portions of outside surface 74 and are electrically connected to conductive vias 36[.]" *EX1009* at 7:60-63, *see also* 7:62-64 ("Pads 34 are connected to respective ones of end surfaces 10B by traces 30 and additional conductive vias 36 formed within redistribution dielectric 72."). Because pads 34 (1) act as wettable contacts for attachment to contacts 52 of PCB 12, and (2) are electrically connected to traces 30 and vias 36, a pad 34 is, therefore, a *fifth metal interconnect*. In other words, pads 34 connect components of Haba's chip package, such as PCB 12 (via contacts 52) to traces 30 and vias 36, thereby functioning as a *metal interconnect*.

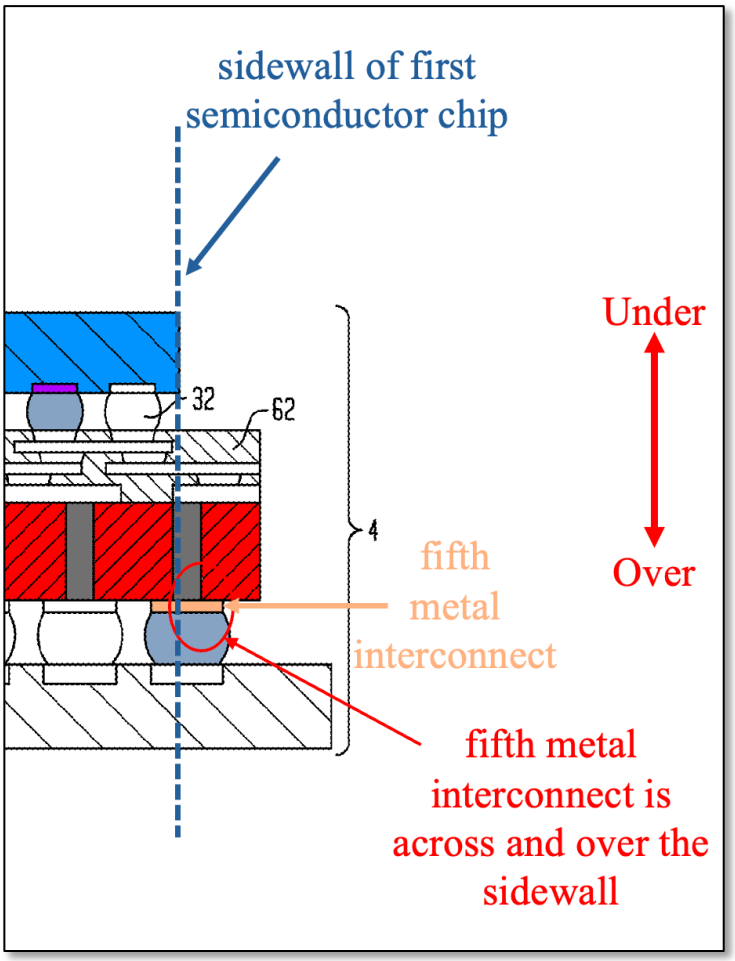
390. The *fifth metal interconnect* is shown in FIG. 10B below, where pad 34 (as identified above in FIG. 9B) is positioned when RDL 70 is included in the FIG. 10B embodiment.



EX1009 at FIG. 10B.

b) Across Over a Sidewall

391. The annotated figure below illustrates that the *fifth metal interconnect* is both *across* and *over* a *sidewall* of microelectronic element 66 (*first semiconductor chip*). The blue dashed line indicates the *sidewall* of microelectronic element 66, namely a boundary thereof. Notably, the *fifth metal interconnect* is positioned in the "over" direction relative to the *sidewall*, as indicated by the red arrow depicting the over/under directions. Additionally, the *fifth metal interconnect* extends laterally (i.e., left/right) to the right past the boundary of the *sidewall*. As such, the *fifth metal interconnect* is both *across* and *over a sidewall of the first semiconductor chip*.

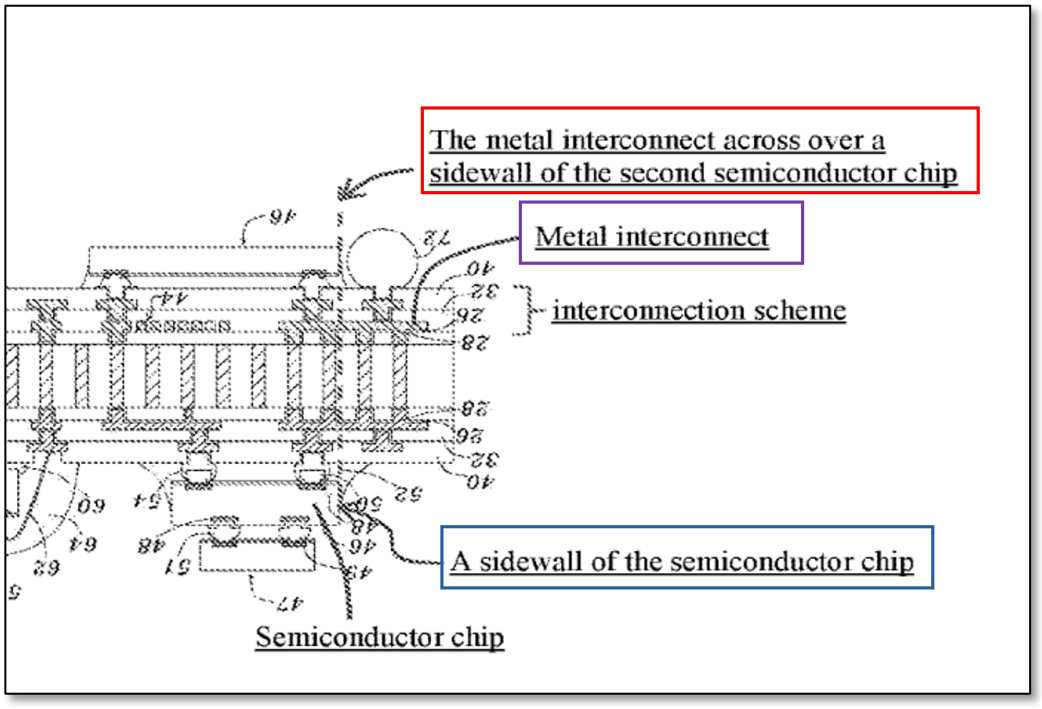


EX1009 at FIG. 10B.

392. Further, even when FIG. 10B of Haba includes RDL 70 of FIG. 9B, the *fifth metal interconnect* still satisfies Claim 3 because RDL 70 is merely positioned under the pads 34 depicted in FIG. 10B such that pads 34 of FIG. 10B are connected to traces 30 in RDL 70. Further, recall that FIG. 10B is "inverted with respect to the depiction" of FIG. 9B. *EX1009* at 7:42-56, 5:1-6; ¶¶ 307-308. Thus, the contact pad 34 in FIG. 9B identified above corresponds to the *fifth metal interconnect* as mapped in FIG. 10B. *See* ¶ 388. Because the *fifth metal interconnect* shown in FIG. 9B

corresponds to the *fifth metal interconnect* in FIG. 10B, when FIG. 10B is modified to include FIG. 9B's RDL 70, the contact pads 34 including the *fifth metal interconnect* is included in the same position depicted in FIG. 10B. Thus, even in the modified FIG. 10B, Haba's *fifth metal interconnect* is *across over a sidewall of the first semiconductor chip*.

393. I note that Haba's teachings of the *fifth metal interconnect* being *across* and *over* the *sidewall of the first semiconductor chip* are consistent with an annotated figure that Patent Owner provided during prosecution illustrating support for this specification. In the figure below, I have shown how the Patent Owner's annotations mirror the above mapping of Haba's *fifth metal interconnect*.



EX1002 at p. 537.

E. ***Claim 5: "The chip package of claim 1, wherein said first semiconductor chip comprises a central-processing-unit (CPU) circuit block and a graphics-processing-unit (GPU) circuit block."***

a) Lin-191's Teachings

394. *See* ¶ 210, incorporated herein.

b) Motivation to Combine

395. The same MTCs and reasonable expectation of success for modifying Sundaram per Lin-191 apply to modifying Haba per Lin-191, e.g., increasing the functionality of Haba's chip package. *See* ¶¶ 211-213, incorporated herein. Additionally, Haba, like Sundaram, contemplates "cellular phones[.]" *EX1009* at 11:35-39.

F. ***Claim 7***

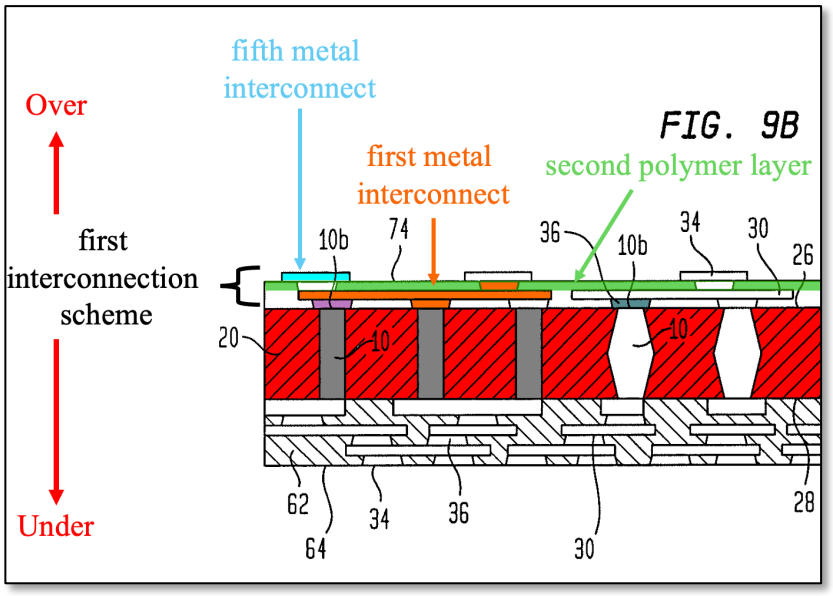
1. Claim 7(a): "The chip package of claim 1, wherein said first interconnection scheme further comprises a fifth metal interconnect over said first metal interconnect and said second polymer layer,"

396. Recall that Haba's *first interconnection scheme* comprises various traces 30, vias 36, and pads 34. *See* ¶¶ 342-343. One of Haba's pads 34 is a *fifth metal interconnect* of the *first interconnection scheme* because Haba teaches "pads 34 which overlie end surfaces 10B [and] act as wettable contacts for attachment to contacts 52 of PCB 12 using solder balls 32." *EX1009* at 7:54-56. Recall that Haba teaches that "wettable **metal** layers or structures…can be wettable contacts[,]" and teaches that "[s]uch wettable metal layers or structures can be made from nickel[.]"

EX1009 at 7:34-36, 6:47-52. *See* ¶ 345. Thus, because Haba teaches "pads 34…act as wettable contacts[,]" pads 34 are *metal*, namely "Nickel or Ni–Au[.]" *EX1009* at 6:50-55.

397. Further regarding pads 34, Haba teaches "contacts or pads 34 overlie portions of outside surface 74 and are electrically connected to conductive vias 36[.]" *EX1009* at 7:60-63, *see also* 7:62-64 ("Pads 34 are connected to respective ones of end surfaces 10B by traces 30 and additional conductive vias 36 formed within redistribution dielectric 72."). Because pads 34 (1) act as wettable contacts for attachment to contacts 52 of PCB 12, and (2) are electrically connected to traces 30 and vias 36, a pad 34 is, therefore, a *fifth metal interconnect*. In other words, pads 34 connect components of Haba's chip package, such as PCB 12 (via contacts 52) to traces 30 and vias 36, thereby functioning as a *metal interconnect*.

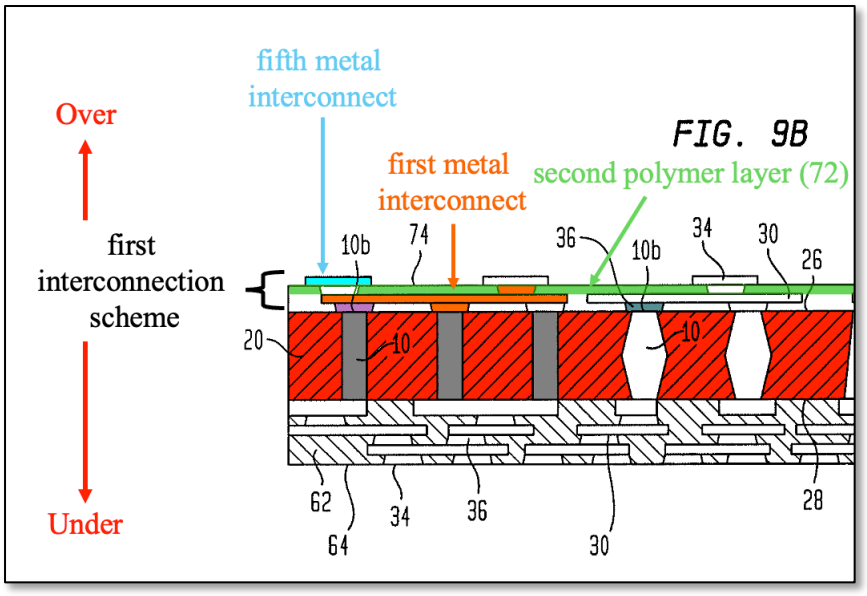
398. As shown, Haba's pad 34 (*fifth metal interconnect*) is on surface 74 of RDL 70 and is, therefore, *over said first metal interconnect and said second polymer layer*, as indicated by the red arrow depicting the over/under directions:



EX1009 at FIG. 9B (excerpt).

2. Claim 7(b): "wherein said second polymer is between said first and fifth metal interconnects,"

399. Haba's redistribution dielectric 72 (*second polymer layer*) is *between said first and fifth metal interconnects*. As shown, at least a portion of the *second polymer layer* is *between said first and fifth metal interconnects*:



EX1009 at FIG. 9B (excerpt).

3. Claim 7(c): "wherein said fifth metal interconnect comprises a third metal layer, a sixth copper layer on said third metal layer, and a seventh copper layer on said sixth copper layer."

a) Lin-191's Teachings

400. Lin-191's teaches a UBM structure comprising the claimed layers. Specifically, adhesion layer 18 is "nickel" and is thus a *third metal layer*, seed layer 19 is formed by "sputtering a copper layer" on layer 18 and is thus *a sixth copper layer on* adhesion layer 18 (i.e., is a *sixth copper layer on said third metal layer*), and "metal layer 27[,]" a "copper layer" is a *seventh copper layer on said sixth copper layer*. *EX1005* at [0308]-[0309], [0313], [0323].

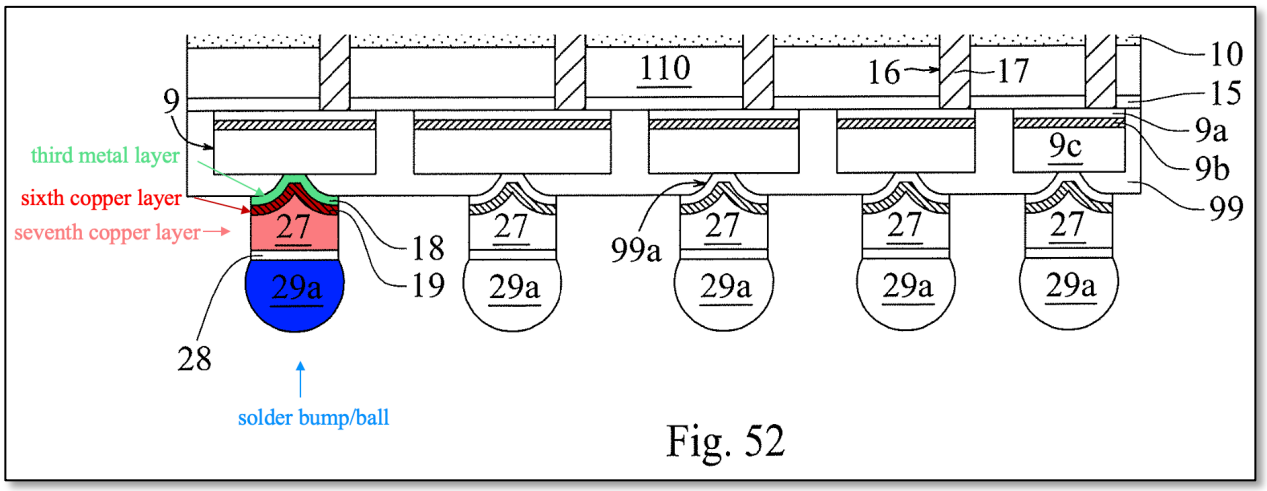


Fig. 52

EX1005 at FIG. 52.

b) Motivation to Combine

401. A POSITA would have found it obvious and been motivated to modify Sundaram's *fifth metal interconnect* (pad 34) per Lin-191's teachings of patterned

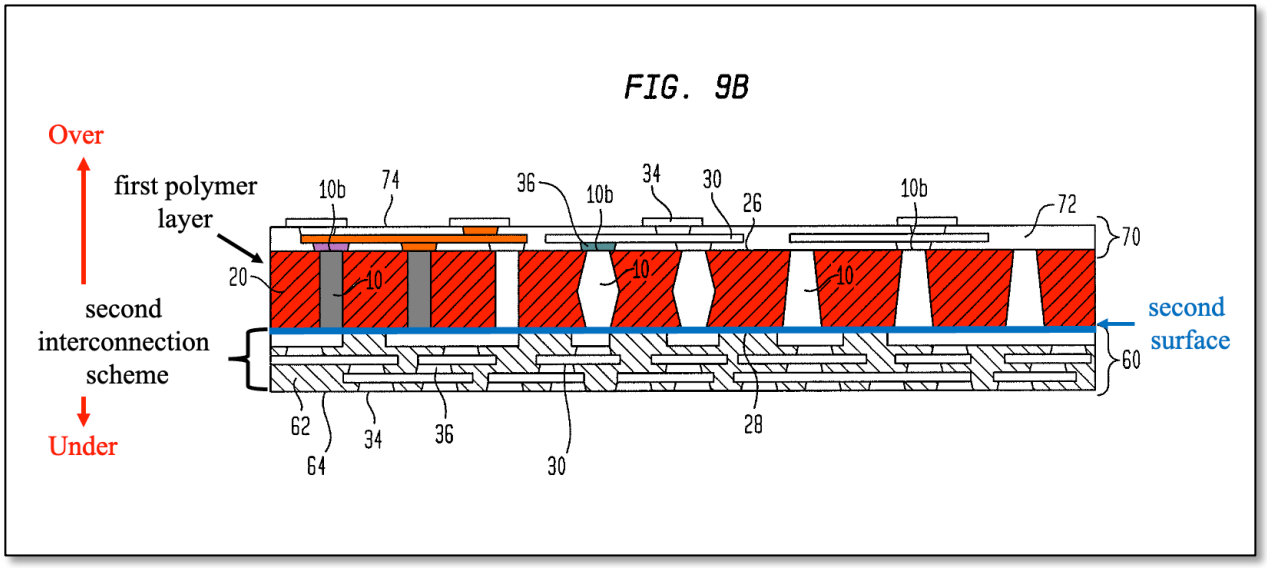
UBM layers, thus yielding the *fifth metal interconnect compris[ing] a third metal layer, a sixth copper layer on said third metal layer, and a seventh copper layer on said sixth copper layer*. The same MTCs and the same reasonable expectation of success described above for Sundaram also apply to Haba. *See* ¶¶ 226-230, incorporated herein. Specifically, the various benefits of copper and nickel described above for Sundaram equally apply to modifying Haba's pad 34. Additionally, because Haba's pad 34 connects to solder ball 32, a POSITA would have found it advantageous to modify the pad 34 to include UBM layers per Lin-191 to improve solder reliability because UBM layers were known to "improve the adhesive strength of solder balls" and to "prevent[] diffusion of unnecessary substances" of solder balls into nearby substrates. *EX1037* at 5:3-5.

G. *Claim 8: "The chip package of claim 1, further comprising a second interconnection scheme under said first polymer layer and on said second surface."*

402. Haba teaches RDL 60, which like RDL 70, comprises various traces 30, vias 36, and pads 34. *EX1009* at FIG. 10B. Indeed, Haba expressly teaches that "traces 30 can electrically connect to an overlie end surfaces 10A…in a redistribution layer 60." *EX1009* at 6:62-65. "The traces 30 are connected, as desired, between layers using conductive vias 36, which are formed through portions of redistribution dielectric layer 60." *EX1009* at 7:7-9. The "posts 10, traces 30 can form an electrical circuit of interconnection component 2." *EX1009* at 7:20-22.

Further, "redistribution layer 60 can allow interconnection component 2 to be used to connect to a microelectronic component having a different connection configuration than the configuration of posts 10." *EX1009* at 7:27-31. Because RDL 60, by vias 36, traces 30, and pads 34 connects interconnection component 2 to other microelectronic components, the traces 30, vias 36, and pads 34 within RDL 60 are a *second interconnection scheme*.

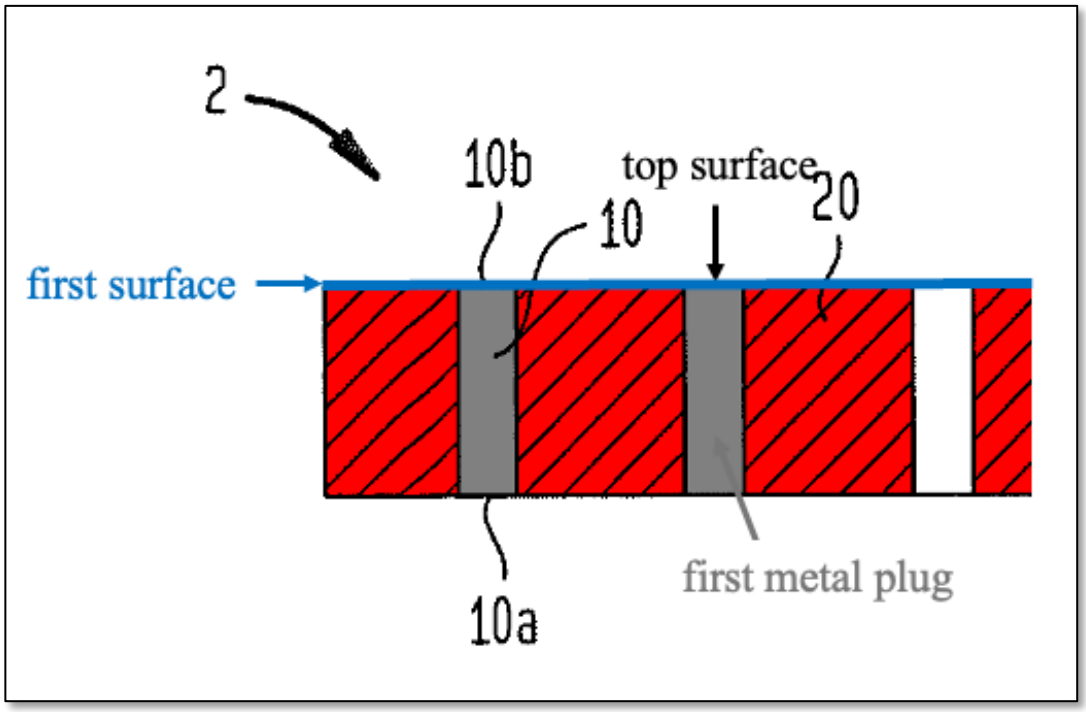
403. Additionally, "redistribution layer 60" is formed "along surface 28" (*second surface*) and is therefore *under said first polymer layer and on said second surface*. *EX1009* at 10:15-16. That is, as shown below, RDL 60 comprising the traces 30 and vias 36 making up the *second interconnection scheme* is *under* dielectric layer 20 (*first polymer layer*) as indicated by the red arrow depicting the over/under directions.



EX1009 at FIG. 9B.

H. *Claim 9: "The chip package of claim 1, wherein said first metal plugs has a top surface substantially coplanar with said first surface."*

404. Haba teaches that the first post 10 (*first metal plug[]*) has a *top surface substantially coplanar with said first surface*, as illustrated below. Recall Haba teaches "a plurality of posts 10 within a dielectric layer 20" comprising "end surfaces 10A and 10B remote from each other with an edge surface 14 extending therebetween." *EX1009* at 5:23-27. Haba further teaches that surface 26 (*said first surface*) is "coplanar with end surfaces 10B of the posts 10." *EX1009* at 10:8-10. As such, surface 10B (*a top surface*) of Haba's *first metal plug[]* is coplanar (*substantially coplanar*) with surface 26 (*said first surface*).



EX1009 at FIG. 9B (excerpt).

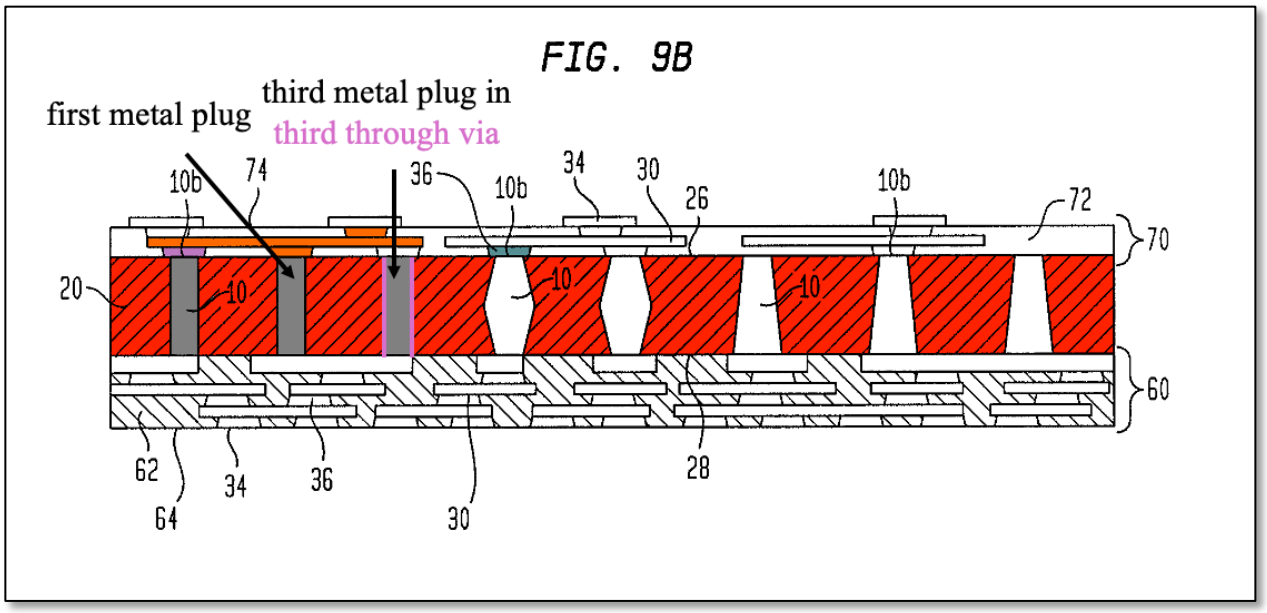
I. ***Claim 10: "The chip package of claim 1, wherein said first metal pad is an aluminum pad."***

a) Lin-191's Teachings and Motivation to Combine

405. *See* ¶ 233 for Lin-191's teachings of an aluminum pad, incorporated herein. The same MTCs and reasonable expectation of success apply to Haba. *See* ¶ 234, incorporated herein.

J. ***Claim 14: "The chip package of claim 1, further comprising a third metal plug vertically in a third through via in said first polymer layer, wherein a pitch between said first and third metal plugs is between 200 and 1000 micrometers."***

406. As discussed, Haba teaches a "plurality of posts 10 within a dielectric layer 20" that are copper (*metal*). *See* ¶ 334. Illustrated below, third of Haba's posts 10 is a *third metal pug* that is *vertically in a third through via in said first polymer layer*.



EX1009 at FIG. 9B.

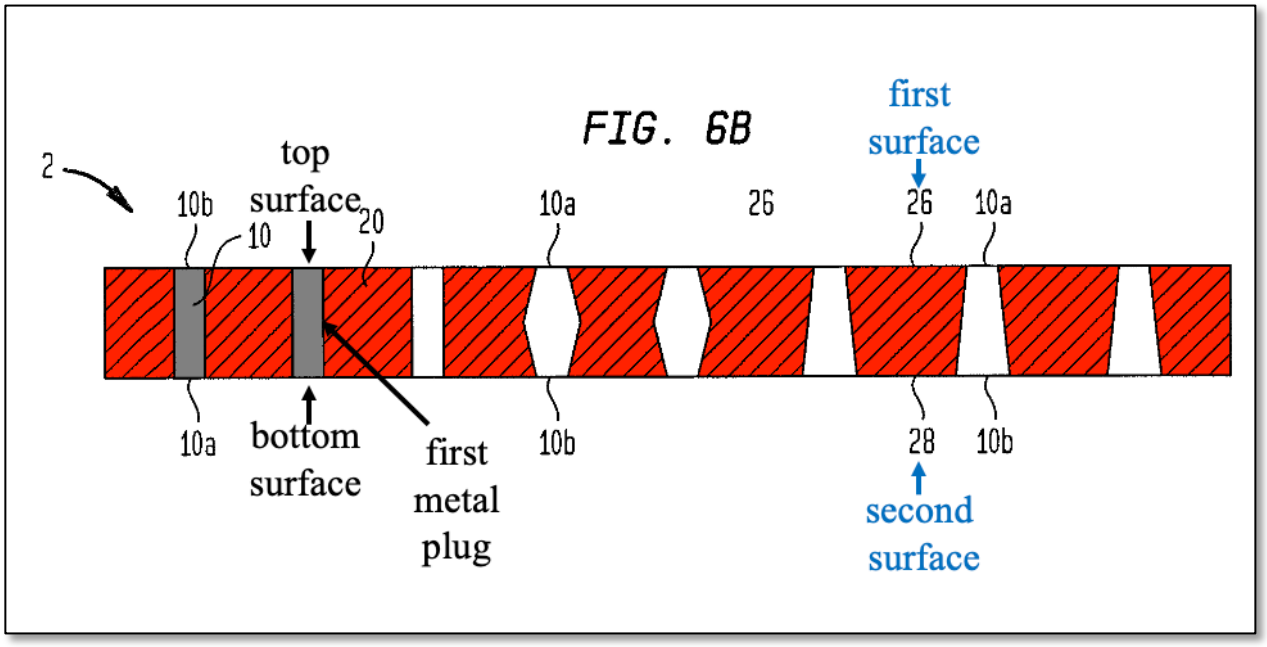
407. Haba further teaches that "posts 10 can be formed at locations facilitating connectivity between elements of a microelectronic assembly. Such posts may have different form factors and be organization, for example, in one or more grid-like patterns having a pitch in a range from 100 to 10000 μm (e.g., **400-650 μm**)." *EX1009* at 5:34-38. Thus, a POSITA would understand that the pitch between Haba's first post 10 (*first metal* plug) and third post 10 (*third metal plug*) is 400-650 μm. Because Haba's pitch of 400-650 μm falls within the claims range of *between 200 and 1000 micrometers*, Haba teaches or renders obvious *wherein a pitch between said first and third metal plugs is between 200 and 1000 micrometers*. As I noted, the '768 Patent does not ascribe criticality to the claimed *pitch*. *See* ¶ 255.

K. *Claim 15: "The chip package of claim 1, wherein said first metal plug has a thickness between 100 and 300 micrometers."*

408. In the combination of Haba-Lin described above, Haba's posts 10, including the first post 10 (*first metal plug*) *has a thickness between 100 and 300 micrometers*. Specifically, at claim 1(a)(ii), Haba's dielectric layer 20 (*first polymer layer*) is modified per Lin to be "between 10 and 150 micrometers." *EX1005* at [0290], *see* ¶¶ 320-331.

409. Further, recall that Haba's posts 10, including the first post 10 (*first metal plug*) has a top surface 10B that is substantially coplanar with surface 26 (*first surface*), where surface 26 is a surface of dielectric layer 20 (*first polymer layer*). *EX1009* at 6:55-58; ¶ 404. Haba's posts 10, including the first post 10 (*first metal*

plug) further comprise a bottom surface 10A that, as shown below, is coplanar with surface 28 (*second surface*) of dielectric layer 20 (*first polymer layer*). *EX1009* at 5:27 ("End surfaces 10A and 10B are left uncovered by the dielectric layer 20 on corresponding surface 28 and 26 thereof.")



EX1009 at FIG. 6B.

410. Because Haba's *first metal plug* has top and bottom surfaces that are coplanar with the first and second surfaces of dielectric layer 20 (*first polymer layer*), the thickness of posts 10, including the first post 10 (*first metal plug*) is equal to the thickness of dielectric layer 20 (*first polymer layer*). Therefore, because post 10 is the same thickness as dielectric layer 20 (*first polymer layer*), and because dielectric layer 20 is modified, per Lin-191, to have a thickness *a thickness between 100 and 300 micrometers*, the first post 10 (*first metal plug*) also *has a thickness between 100*

and 300 micrometers. That is, because Lin-191's range of between 10 and 150 micrometers" teaches or renders obvious *between 100 and 300 micrometers*, and because posts 10 (*first metal plug*) comprise the same thickness range, Haba in view of Lin-191 teaches or renders obvious the *first metal plug* having a *thickness between 100 and 300 micrometers*. *EX1005* at [0290]; ¶¶ 320-322. Further, as I described above, the '768 Patent does not ascribe any criticality to the claimed plug thickness. *See* ¶ 258.

XI. OPINIONS REGARDING GROUND 2B: CLAIMS 4, 6, AND 11-13 ARE OBVIOUS OVER HABA, LIN-191, AND SUNDARAM

A. *Claim 4*

1. 4(a): "The chip package of claim 1, further comprising a second semiconductor chip over said first interconnection scheme,"

a) Sundaram's Teachings

411. As I described above, Sundaram's second electronic device 130 is a *second semiconductor chip over said first interconnection scheme*. *See* ¶ 208, incorporated herein.

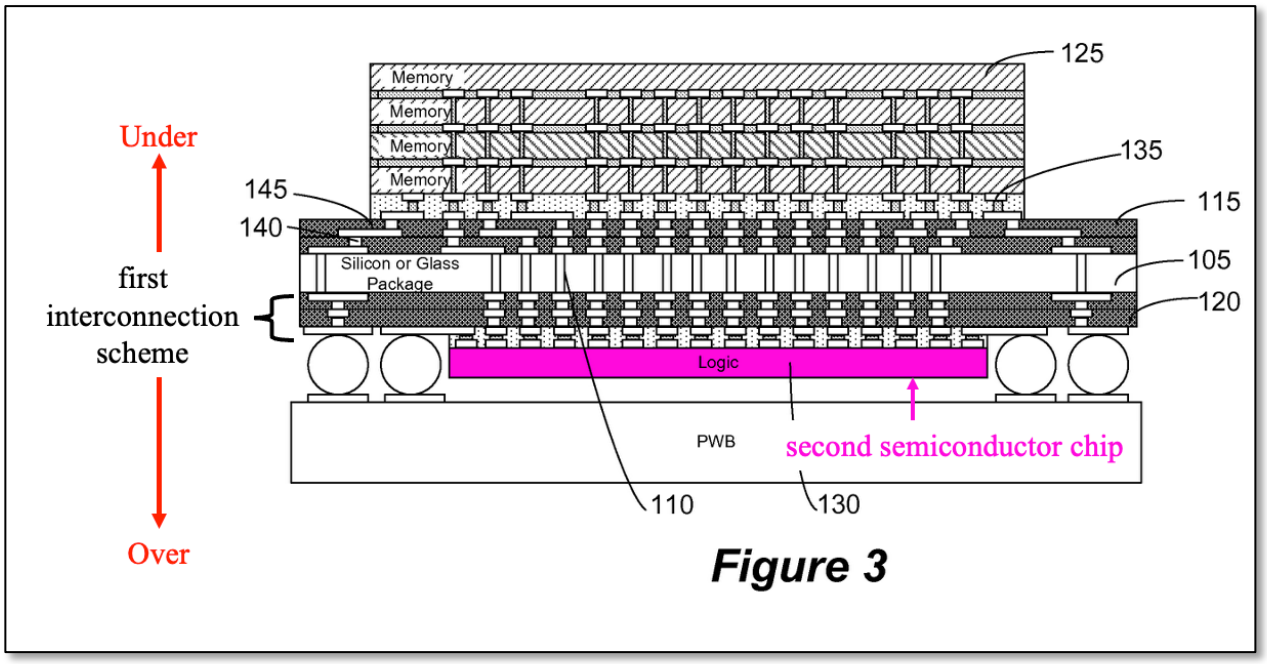


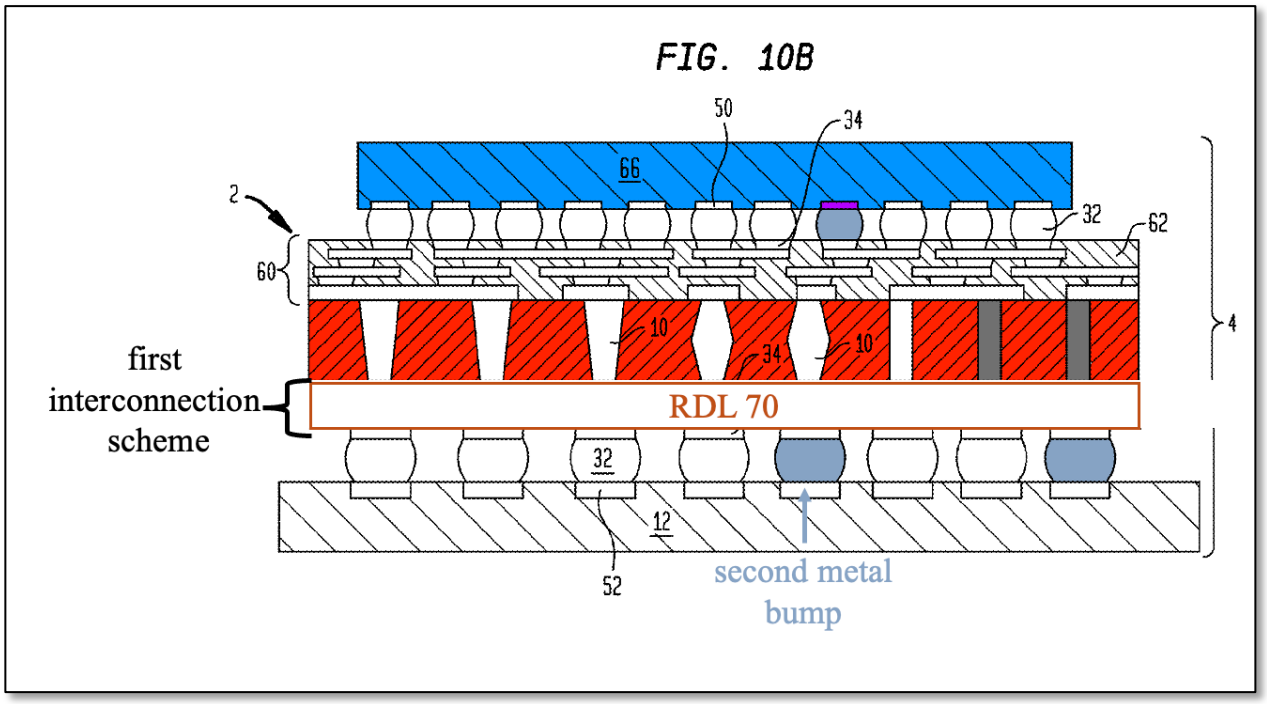
Figure 3

EX1004 at FIG. 3. *See* ¶¶ 414-419 for MTC and reasonable expectation of success.

2. 4(b): "wherein said second semiconductor chip comprises a second metal bump between said second semiconductor chip and said first interconnection scheme."

a) Haba's Teachings

412. For the same reasons discussed above at Claim 1(e), Haba teaches a *second metal bump*. *See* ¶¶ 363-367.



EX1009 at FIG. 10B.

b) Sundaram's Teachings

413. Additionally, or alternatively, Sundaram's device 130 has a *second metal bump between said second semiconductor chip and said first interconnection scheme*. *See* ¶¶ 209. 284, incorporated herein.

3. Motivation to Combine

414. In the Haba-Lin-191 combination, a POSITA would have been motivated and found it obvious, per Sundaram, to include a semiconductor chip *over* Haba's *first interconnection scheme* and connected thereto by a *second metal bump*. Haba already envisions multiple chips in a chip package, incorporating in by reference U.S. Patent No. 7,759,782 that teaches multiple microelectronic elements 906, 908 in a chip package, thus motivating the combination. *EX1084* at 6:56-61,

FIG. 9D. A POSITA would have appreciated that the single microelectronic element 66 (semiconductor chip) depicted in FIG. 10B is merely exemplary and would have found it obvious and been motivated to incorporate additional semiconductor chips into Haba's chip package, for example to add functionality.

415. Additionally, a POSITA would have recognized that positioning a chip between Haba's RDL 70 and PCB 12 would have maximized the use of space in Haba's chip package, because placing a chip in such a location would have added functionality to such space, more so than merely having solder balls 32 there. As such, a POSITA would have been motivated to turn to references like Sundaram, which taught connecting semiconductor chips to RDL's like Sundaram's, which would not have incrased the width of Haba's *chip package* as the chip would be within the same vertical extent of Haba's package by being between RDL 70 and PCB 12.

416. For example, it was common and advantageous to provide a chip package in a package-on-package configuration with a memory chip above an interposer/interconnection scheme and a logic chip below. For example, Sundaram teaches that a "first electronic device 125 can be attached to the first side 115 of the interposer 105 and a second electronic device 130 can be attached to the second side 120 of the interposer 105. In exemplary embodiments, the first electronic device can be single or stacked memory IC devices, and the second electronic device 130 can

be a logic IC device or devices." *EX1009* at [0064], FIGS. 3, 5a-d. *See also EX1091* at [0033] ("Top die 18 and die 146 may be different types of dies. For example, top die 18 may be a logic die, such as a central computing unit (CPU), while die 146 may be a memory die."), FIG. 11; *EX1092* at p. 1397 ("The dominant use of PoP packages is to integrate a high density digital logic device in the bottom (base) package with high capacity combination memory devices (i.e., DRAM and flash) in the top (stacked) package to achieve system size reduction and memory architecture flexibility."). Indeed, this structure was common digital cameras and cell phones before the '768 Patent, and Haba envisions using interconnection component 2 in "cellular telephone[s]." *EX1009* at 11:14-39; *EX1028* at p. 5 ("Digital camera and cell phone applications are currently stacking two packages for logic + memory architectures."). As Haba already teaches a chip (microelectronic element 66) under an interconnection scheme (see, e.g., FIGS. 10A-10B), a POSITA would have found it obvious to modify Haba to include a second chip to complete this common structure.

417. Further, a POSITA would have been motivated and found it obvious to modify Haba such that the *second semiconductor chip* is *over* Haba's *first interconnection scheme* to provide a minimal path length between the *second semiconductor chip* and the PCB 12. Specifically, by positioning the *second semiconductor chip over* the *first interconnection scheme*, signals travelling from

the *second semiconductor chip* and PCB 12 would have a reduced susceptibility to noise due to the physical proximity between the two.

418. The Haba-Lin-191-Sundaram combination is the application of a known technique (Sundaram chip over an RDL) to a known device (Haba's chip package) to yield the predictable result of Haba's chip package having a semiconductor chip over Haba's interconnection scheme.

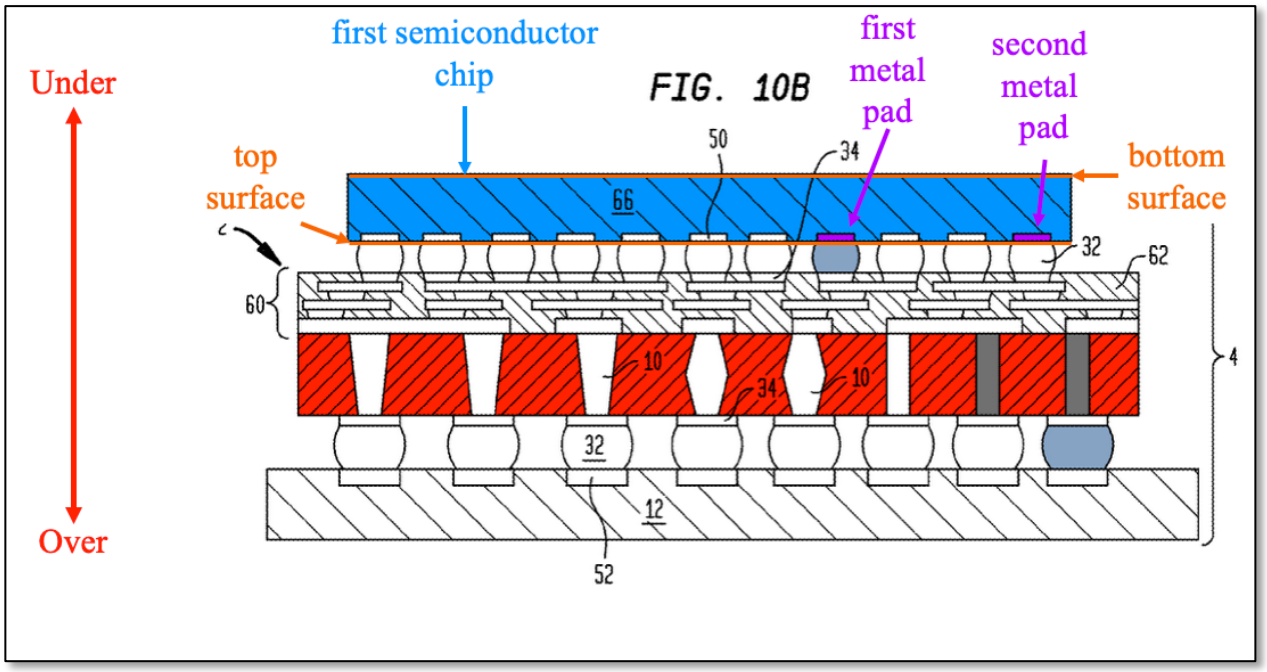
419. A POSITA would have had a reasonable expectation of success in modifying Haba-Lin-191 per Sundaram because Sundaram's configuration represents a well-known method for connecting a chip to an RDL. *See, e.g., EX1091* at FIG. 11.

B. *Claim 6*

1. 6(a): "The chip package of claim 1, wherein said first semiconductor chip comprises a second metal pad on a top surface of said first semiconductor chip and a third metal pad on a bottom surface of said first semiconductor chip,"

a) Haba's Teachings

420. As described at Claim 1(f)(i), the Haba-Lin-191 combination teaches *a first semiconductor chip* having a *first metal pad*. *See* ¶¶ 373-376. For the same reasons, Haba-Lin-191 teaches *a second metal pad on a top surface of said first semiconductor chip*, namely a second contact 50 *on a top* surface microelectronic element 66.



EX1009 at FIG. 10B.

b) Sundaram's Teachings

421. As I described above, Sundaram teaches a *third metal pad on a bottom surface* of a *semiconductor chip*. *See* ¶ 214, incorporated herein.

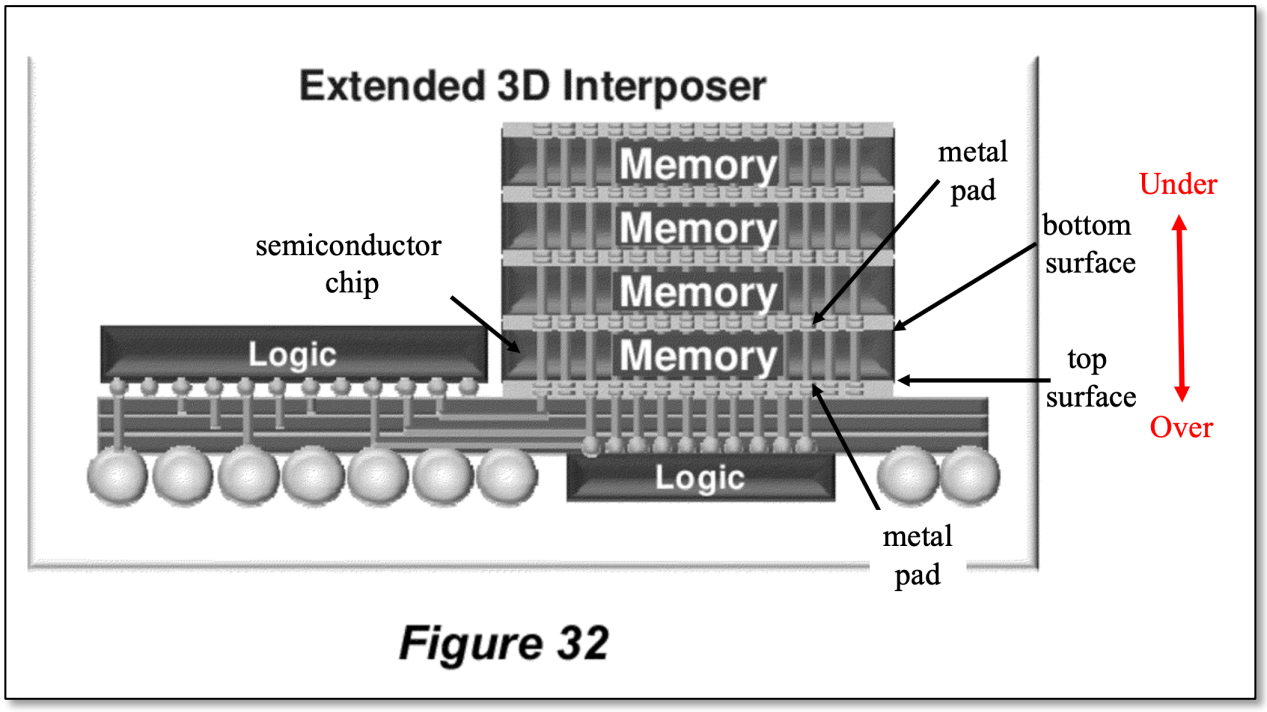


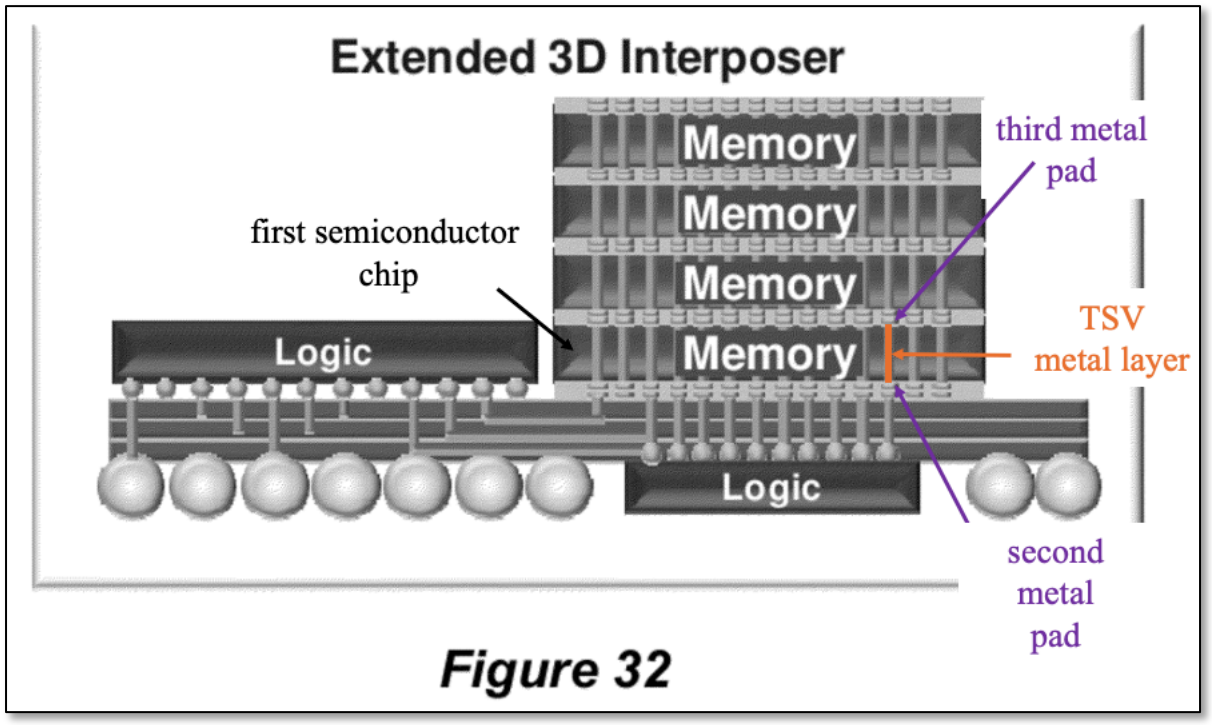
Figure 32

EX1004 at FIG. 32. *See* ¶¶ 423-429 for MTC and reasonable expectation of success.

2. 6(b): "wherein said second metal pad is connected to said third metal pad through a through-silicon-via metal layer."

a) Sundaram's Teachings

422. As I described above, Sundaram teaches a *through-silicon-via metal layer connect[ing]* metal pads on a *semiconductor chip*. *See* ¶¶ 217-219.



EX1004 at FIG. 32.

3. Motivation to Combine

423. A POSITA would have found it obvious and been motivated to modify Haba's microelectronic element 66 (*first semiconductor chip*), per Sundaram, to comprise a *third metal pad* on the *bottom surface* of microelectronic element 66 that is electrically connected to Haba's *second metal pad* on the *top surface through a through-silicon-via metal layer*. Specifically, in the combination, Haba's microelectronic element 66 is modified to have the *third metal pad* and the *through-silicon-via metal layer*.

424. A POSITA would have recognized and appreciated that modifying Haba's microelectronic element 66 according to Sundaram TSV metal layer would

have allowed for additional chips to be easily stacked under microelectronic element 66. Specifically, it was known that TSV's "which are vertical connections 'etched through the silicon wafer and filled with metal'" allows for "the addition of many more pathways between 2D layers" in a chip package." *EX1066* at [0017]. Additionally, by "using TSV technology, 3D ICs can pack a great deal of functionality into a small 'footprint.' In addition, critical electrical paths through the device can be drastically shortened, leading to faster operation." *EX1067* at [0005]. As such, a POSITA would have recognized that by forming a TSV connecting metal pads in Haba's microelectronic element 66 would have allowed for additional chips to be stacked thereon and for "critical electrical paths" to be short, leading to efficient communication between such chips. *EX1067* at [0005].

425. When adding a TSV to Haba's microelectronic element 66, a POSITA would have also found it obvious to include the *third metal pad*, per Sundaram, so that other components of the chip package would electrically connect to the TSV. As such, a POSITA would have recognized that modifying Haba's microelectronic element 66 would similarly allow for additional structures, such as another semiconductor chip, to be connected to the *through-silicon-via metal layer*.

426. Further, as I described above, it was well understood to include multiple chips stacked in a chip package and was expressly envisioned by Haba. *EX1009* at 8:18-40; ¶ 414. A POSITA would have appreciated that modifying Haba's

microelectronic element 66 (*first semiconductor chip*) to have a TSV *metal layer* connecting two metal pads on opposite surfaces was a well-known industry standard for configuring a semiconductor chip to enable chip stacking. Indeed, providing background information on TSVs, Lee-944 states "[t]o electrically connect the stacked semiconductor chips, a through-silicon via (TSV) technique is used. The TSV technique is a three-dimensional package technique that electrically connects the stacked semiconductor chips by forming a small hole in each semiconductor chip and by filling the hole with a metal material. The TSV technique may obviate drawbacks, such as low speed, high power consumption, a large size, etc., of a conventional stack package using a metal wire. The term 'through silicon via' is used for convenience as a recognized term of art." *EX1116* at [0003]. Due to the well-known benefits and recognition of a TSV as a "term of art[,]" a POSITA would have been familiar with such a structure and been motivated to achieve the aforementioned benefits in Haba's chip package. *EX1116* at [0003].

427. As another example, it was common and advantageous to provide a chip package with stacked memory chips connected by a TSV, as demonstrated by Sundaram. *EX1004* at FIG. 3, 6:37-39 ("In exemplary embodiments, the first electronic device 125 can be single or stacked memory IC devices…"), 7:15-23 ("For example, third and fourth electronic devices can be stacked on the first 125 and second 130 electronic devices, respectively to create a 3D configuration. In

stacking embodiments, through vias are defined within the first 125 and second 130 electronic devices, as well as the interposer, to facilitate communication with the third and fourth electronic embodiments.").

428. Because Haba already envisions having multiple chips as part of interconnection component 2, a POSITA would have appreciated that modifying Haba's chip to comprise a TSV connecting metal pads would have allowed for high-density 3D integration, with high speed communication between additional chips. Additionally, a POSITA would have recognized that the modification is nothing more than the application of a known technique (configuring chips with a TSV connecting metal pads) to a known device (Haba's chip package) to yield the predictable result of Haba's chip package having microelectronic element 66 with a TSV, e.g., to connect to other chips in the package.

429. A POSITA would have had a reasonable expectation of success in modifying Haba-Lin-191, per Sundaram because, as I described above, Sundaram's configuration represents a well-known method for enabling chip stacking and TSVs were common in chips by the time of the '768 Patent. *See* ¶¶ 217-218. Additionally, methods of forming both metal pads and TSVs were well known. For example, metal pads may be formed by "patterning with PVD, CVD, sputtering, electrolytic plating, electroless plating." *EX1006* at [0041]; *EX1042* at ("…filled with copper typically by an electroplating process, as known to one of ordinary skill in the art of integrated

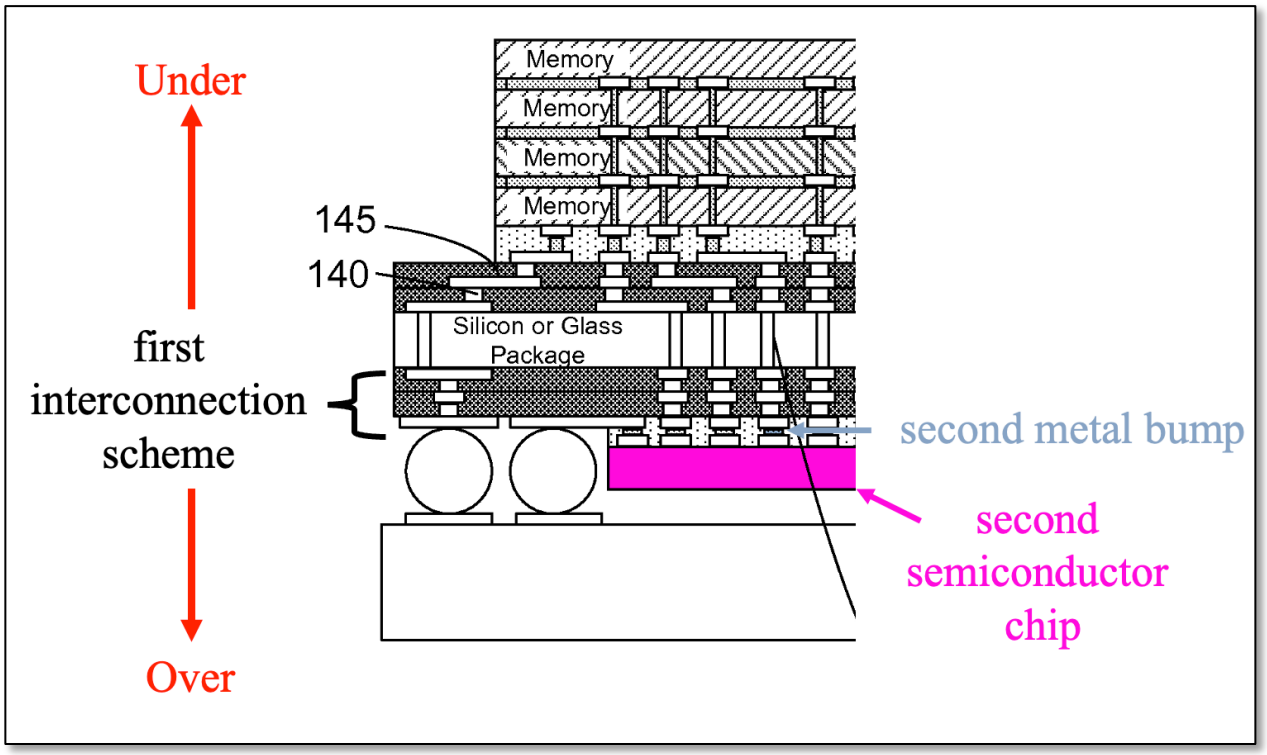
circuit fabrication."); *EX1043* at [0032] ("…variety of different deposition methods known by one of ordinary skill in the art, including but not limited to, CVD, pulsed CVD, PECVD, ALD, PEALD, or sputtering methods."). Further, "PVD, CVD, electrolytic plating, [or] electroless plating process" may be used to form a TSV *metal layer*. *EX1006* at [0043]. As such, the modification would have been simple and straightforward using techniques familiar to a POSITA, thus leading to a reasonable expectation of success.

C. *Claim 11*

1. 11(a): "The chip package of claim 1, further comprising a second semiconductor chip over said first interconnection scheme and connected to said first interconnection scheme through a second metal bump"

a) Sundaram's Teachings

430. As I described above, Sundaram teaches the *second semiconductor chip over said first interconnection scheme* and the *second semiconductor chip* is *connected to said first interconnection scheme through a second metal bump*. *See* ¶¶ 235-236, incorporated herein. Indeed, Sundaram teaches that die pads 135 on interposer 105 "electrically connect devices[,]" such as second electronic device 130, shown below, "using solder, copper bumps with solder caps…" *EX1004* at 6:29-30; FIG. 3. Because device 130 is connected using a "copper bump[] with solder cap[]," Sundaram teaches the *second metal bump*.



EX1004 at FIG. 3 (excerpt).

2. 11(b): "wherein said second semiconductor chip has a height is between a backside surface of said second semiconductor chip and a top surface of said second polymer layer is smaller than a thickness of said first metal bump."

a) Sundaram's Teachings and Motivation to Combine

431. As discussed, Sundaram teaches *wherein said second semiconductor chip has a height is between a backside surface of said second semiconductor chip and a top surface of said second polymer layer is smaller than a thickness of said first metal bump* in the same way as described by the '768 Patent. *See* ¶¶ 237-239, incorporated herein.

432. A POSITA would have found it obvious and been motivated to configure the second semiconductor chip, per Sundaram, such that it *has a height [that] is between a backside surface of said second semiconductor chip and a top surface of said second polymer layer*, that is *smaller than a thickness of said first metal bump*. Specifically, the modification would yield solder balls that are taller than the semiconductor chip to space the semiconductor chip from the PCB. Thus, a POSITA would have recognized that when the height of the second semiconductor chip is less than the height of the first metal bump, the second semiconductor chip would advantageously not impede the connection of Haba's bumps 32 to PCB 12, because solder balls 32 surrounding the periphery of the second semiconductor chip would still connect to PCB 12.

433. Indeed, the height of the second semiconductor chip must be smaller than the thickness of the metal bumps, else the metal bumps would not connect to the PCB. As such, a POSITA would have recognized the modification as an advantageous way of increasing chip density without compromising package size, i.e., adding the *second semiconductor chip* would not increase the package thickness. Indeed, it was known to place a semiconductor chip between layers of a chip package with a smaller height than the surrounding bumps interconnecting the layers, so that the chip would not increase the overall package thickness. *EX1068* at [0046] ("For example, the thickness of substrate 122 can be 0.1 mm, the height of semiconductor

die 124 can be 0.18 mm, and the height of bumps 132 can be 0.3 mm with a 0.5 mm pitch, to yield an overall package height of approximately 0.4 mm. Accordingly, the combined thickness of semiconductor die 124 and the gap is less than or equal to the height of bumps 132 so that the effective die thickness is accommodated within the second level interconnect, and contributes nothing to the overall package thickness ("Z" direction miniaturization."), FIG. 4. Thus, a POSITA would have recognized the modification as an advantageous way of increasing chip density without compromising package size.

434. The modification is the application of a known technique (a chip having a height less than surrounding bumps) to a known device (Haba's chip package) ready for improvement to yield the predictable result of a chip package having two chips without increasing package thickness. Additionally, a POSITA would have had a reasonable expectation of success at least because the modification would have merely required making the solder balls 32 connecting the *second semiconductor chip* to RDL 70 smaller than the others, and methods of controlling solder ball size were well-known. *See, e.g., EX1093* at 4:7-11 ("Furthermore, the actual amount of solder 42 deposited will be a function of the desired end bump size. In other words, in order to form a large solder bump, a greater amount of solder 42 material would be applied to the device than would be applied to form a small bump.") Thus, a

POSITA would have viewed the modification as routine and easily implementable, further contributing to a reasonable expectation of success.

D. ***Claim 12 "The chip package of claim 1, further comprising a second semiconductor chip under said first semiconductor chip, wherein said first semiconductor chip comprises a second metal pad connected to a third metal pad of said second semiconductor chip through a solder layer, wherein said solder layer between said first and second semiconductor chips."***

a) Sundaram's Teachings

435. As discussed, Sundaram teaches Claim 12. *See* ¶¶ 240-245, incorporated herein. A POSITA would have found it obvious and been motivated to modify Haba per Sundaram's teachings of a *second semiconductor chip* (second memory chip) *under* Haba's element 66 (*first semiconductor chip*) and for element 66 to have *a second metal pad connected to a third metal pad via a solder layer*. As I discussed above, a POSITA would have been motivated to incorporate additional chips into Haba's chip package to add functionality. *See* ¶¶ 411-419, incorporated herein.

436. A POSITA would have been motivated to modify Haba per Sundaram's teachings of a *second semiconductor chip* (second memory chip) under Haba's element 66 (first semiconductor chip) and for element 66 to have a *second metal pad connected to a third metal pad via a solder layer.* Haba expressly teaches stacked interconnection structures in which a microelectronic element 66 is joined to an interconnection component 2 by conductive masses such as solder balls 32 formed

on wettable contact surfaces of posts 10. *EX1009* at 6:42–44, 7:50–56; FIG. 10A–B. Haba explains that "the end surfaces 10B of posts 10 are used to join posts 10 to solder balls 32, which are, in turn, joined to contacts 50 on a microelectronic element 66." *EX1009* at 6:42–44, Additionally, "contacts 50 of the microelectronic element 66 are joined to contacts or pads of interconnection component 2." *EX1009* at 7:50–52. Thus, Haba teaches the use of opposing metal pad interfaces (e.g., contact 50 of die 66 and end surface 10B of post 10) joined through solder layers 32 on both the upper and lower sides of the interconnection component, thereby providing metal pad-to-pad continuity through solder interconnects. A POSITA would have recognized that incorporating Sundaram's teaching of a second, memory-type chip beneath the interposer would simply extend Haba's vertically stacked configuration, using the same solder interconnect approach to couple a lower die's top pads to Haba's bottom solder joints (end surface 10B/contact 52). The modification would have been straightforward, predictable, and had a reasonable expectation of success because Haba already provides the wettable metal pad and solder-based interfaces needed for pad-to-pad vertical connection, and contemplates "stacked" interconnection assemblies. *EX1009* at 6:42–44, 7:50–56; 8:18-40; FIG. 10A-B. The modification is the application of a known technique, i.e., Sundaram's teachings of stacking chips using metal pads and solder layers, to a known device, i.e., Haba's

chip package to yield the predictable results of Haba's package having two chips coupled using pads soldered to one another.

E. *Claim 13*

1. 13(a): "The chip package of claim 1, further comprising a second semiconductor chip under said first semiconductor chip,"

a) Sundaram's Teachings

437. As discussed, Sundaram teaches a *second semiconductor chip under* a *first semiconductor chip*. *See* ¶ 247, incorporated herein.

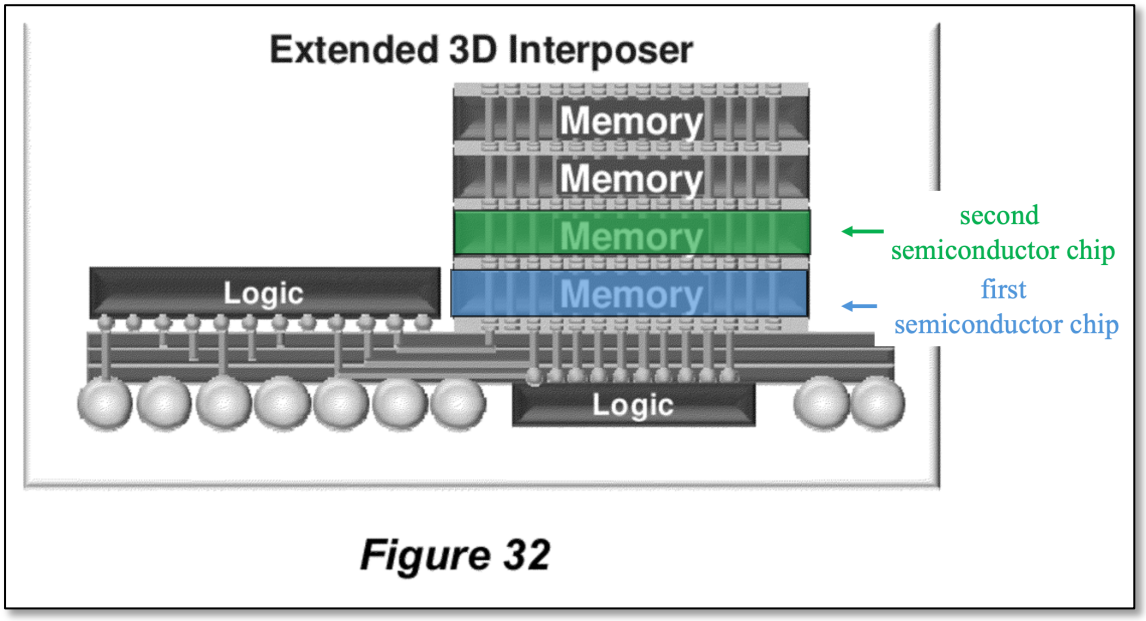


Figure 32

EX1004 at FIG. 32. *See* ¶¶ 441-444 for MTC and reasonable expectation of success.

2. 13(b): "wherein said first semiconductor chip comprises a second metal pad on a top surface of said first semiconductor chip, a third metal pad on a bottom surface of said first semiconductor chip"

a) Sundaram's Teachings

438. *See* ¶ 248, incorporated herein.

3. 13(c): "and a through-silicon-via metal layer connects to said second metal pad,"

439. *See* ¶ 249, incorporated herein.

4. 13(d): "wherein said third metal pad is connected to a fourth metal pad of said second semiconductor chip."

a) Sundaram's Teachings

440. Sundaram *second semiconductor chip* comprises a *fourth metal pad connected to* a pad of Sundaram's *first semiconductor chip*. *See* ¶¶ 250-251, incorporated herein.

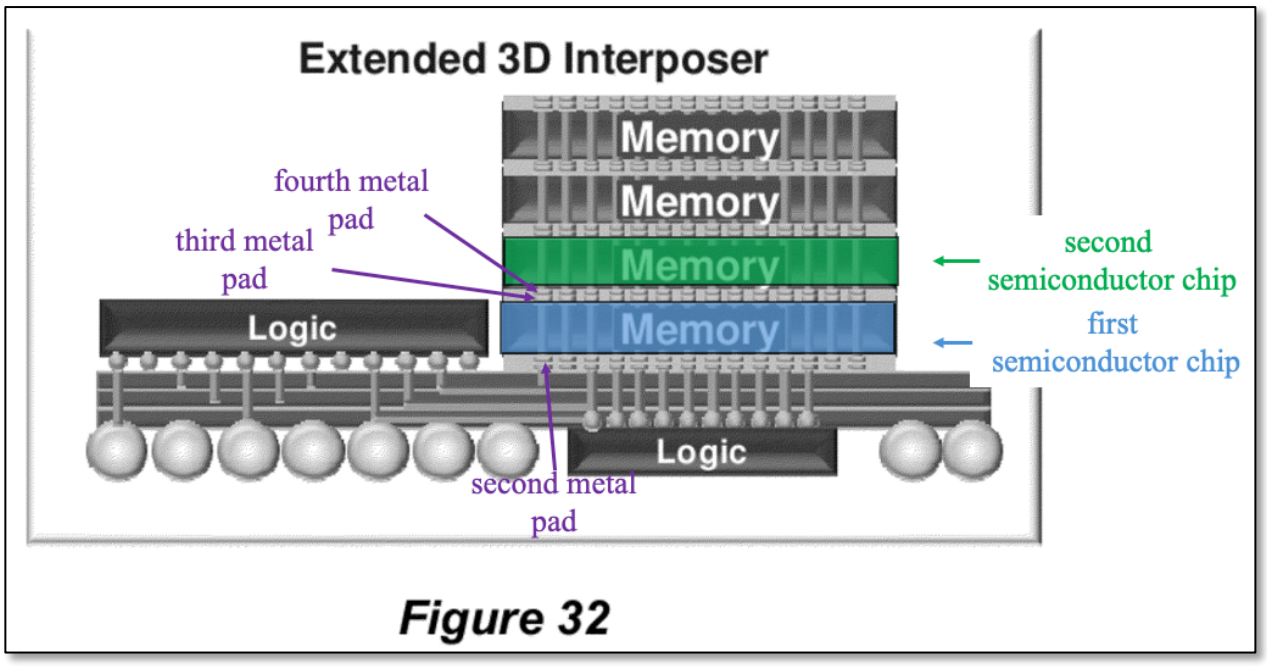


Figure 32

EX1004 at FIG. 32.

5. Motivation to Combine

441. The MTCs and reasonable expectation of success of Claim 6 are incorporated herein. *See* ¶¶ 423-429, incorporated herein. A POSITA would have been further motivated to include a *second semiconductor chip under said first semiconductor chip* in Haba's chip package. As I described above, Haba envisions multiple chips in a chip package, and it was common to do so. *See* ¶ 414; *EX1006* at FIG. 3f; *EX1067* at [0005] ("A three dimensional integrated circuit (3D IC) is a single integrated circuit built by stacking silicon wafers and/or dies and interconnecting them vertically so that they behave as a single device."). A POSITA would have recognized that Sundaram's configuration represents an efficient use of space while maximizing functionality of Haba's chip package because it was known to stack chips vertically so that "they occupy less space." *EX1067* at [0006].

442. That is, stacking chips vertically would allow for increased functionality of Haba's chip package while not increasing the horizontal length of the chip package. Indeed, as described above at claim 6, modifying element 66 to comprise a TSV connecting metal pads would have allowed for high-density 3D integration and high speed communication between chips, and so a POSITA would have found it obvious to modify Haba's chip package to include chip 150 to realize such high-density integration. *See* ¶¶ 424-428.

443. Additionally, a POSITA would have been motivated to connect the *third metal pad* to the *fourth metal pad* each of the *first semiconductor chip* and the

second semiconductor chip would be electrically connected. Metal pads were traditionally used as input/output (I/O) terminals for semiconductor chips, so the modification would have been a straightforward, conventional means of facilitating communication between the stacked chips. *EX1095* at ("I/O terminals were **traditionally** formed by way of **metal pads** along the periphery of an IC.").

444. The modification is the application of a known technique (stacking chips) to a known device (Haba's chip package) to yield the predictable result of a chip package comprising multiple chips. The modification would have been straightforward and merely required forming a TSV connecting metal pads of the *first* and *second semiconductor chips* according to well-known methods. For example, as I described above, methods of forming metal pads such and TSVs, such as PVD, CVD, electrolytic plating, and electroless plating were well-known. *See* ¶ 429. Thus, because such methods were well-known, and because TSVs connecting metal pads in a chip stack was a common structure, a POSITA would have had the skill set to perform the modification with no undue experimentation, leading to a reasonable expectation of success.

XII. OPINIONS REGARDING GROUND 3A: CLAIMS 16-17, 19, 22-28 ARE OBVIOUS OVER YU AND LIN-191

A. *Claim 16*

1. 16(Pre): "A chip package comprising"

445. Yu teaches a "PoP [Package-on-Package] structure" comprising "multiple packages 202," each of which contains one or more semiconductor dies. *EX1010* at 8:35-36. Yu explains the dies may include "a logic circuitry die, a memory die, or any other die," thereby encompassing a variety of semiconductor devices integrated within the stacked package arrangement. *EX1010* at 2:50–51. Yu further defines "Package-on-Package (PoP)" as "an integrated circuit packaging technique to allow vertically combining discrete logic and memory ball grid array (BGA) packages." *EX1010* at 1:49–51.

446. Accordingly, Yu's disclosure of a "PoP structure" comprising "multiple packages 202" and including logic and memory dies teaches *a chip package* in which multiple packaged semiconductor devices are combined into a vertically integrated assembly. *EX1010* at 1:49–51, 2:50–51, 8:35–36.

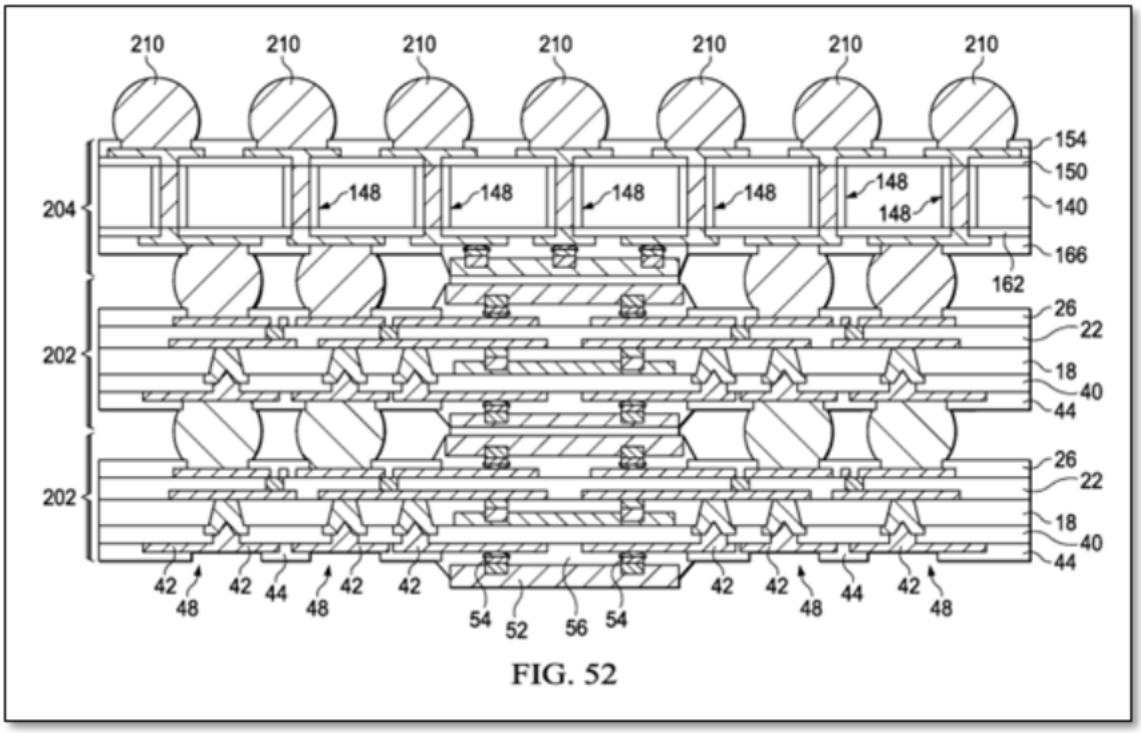


FIG. 52

EX1010 at FIG. 52.

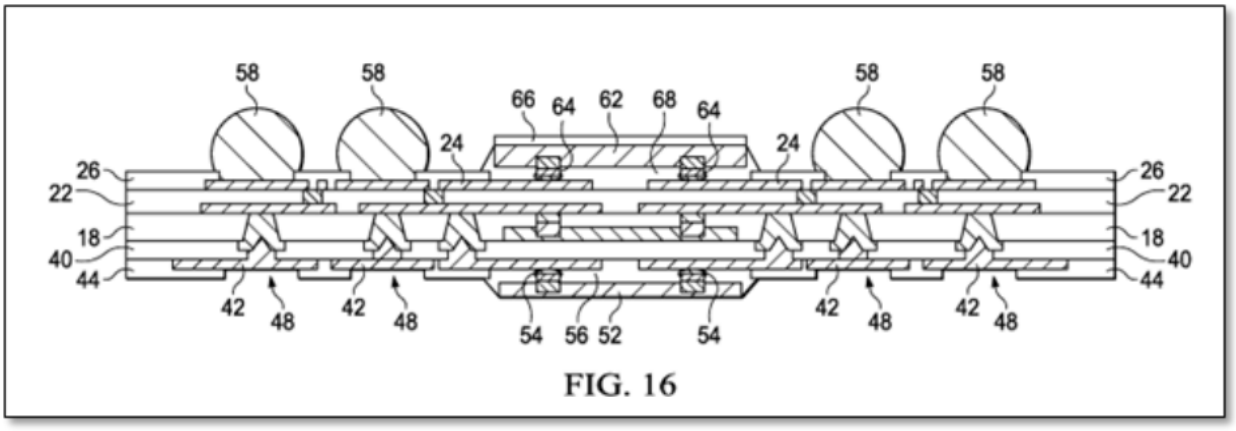


FIG. 16

EX1010 at FIG. 16.

447. Yu's FIG. 52 comprises multiple of the packages 202 shown in FIG. 17. *EX1010* at 8:11-13. The package of FIG. 17 is the same as FIG. 16 except for depicting "pins 70 of a probe card" probing connectors 58 "to test the structure."

EX1010 at 5:4-6. Thus, Yu's FIG. 52 depicts multiple of the packages 202 as depicted in FIG. 16.

448. The hierarchy of figures illustrates a progressive structural relationship: FIG. 16 depicts the core single-package cross-section and FIG. 52 shows multiple such packages stacked in a vertical PoP configuration. Accordingly, Yu's PoP structure, as shown in FIG. 52, comprises multiple chip packages each corresponding to the single-package configuration of FIG. 16, thereby forming a *chip package*. *EX1010* at 1:49–51, 2:50–51, 4:67–5:7, 8:11–13, 8:35–36.

2. 16(a): "a first polymer layer having a first surface and a second surface opposite to said first surface,"

449. As shown below, Yu's package 202 includes "molding compound 18 [that] can be [] epoxy, polyimide, silicone rubber, the like, or a combination thereof," i.e., *a first polymer layer*. *EX1010 at* 2:61-64. Molding compound 18 has *a first surface opposite to a second surface*. Yu identifies molding compound 18 as part of package 202 and depicts the molding compound 18 as a defined, polymer region surrounding the internal components of the package. As shown in Yu's FIG. 16, molding compound 18 includes opposing surfaces, *a first surface and a second surface opposite to said first surface*, that bound the *first polymer layer*.

450. Thus, Yu's molding compound 18 (*first polymer layer*) comprises a *first surface and a second surface opposite to said first surface*.

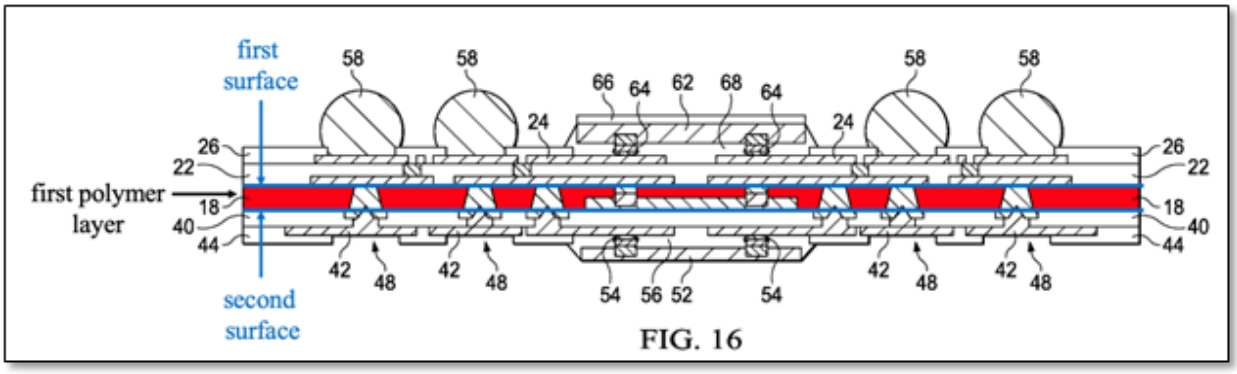


FIG. 16

EX1010 at FIG. 16.

3. 16(a)(i): "wherein said first surface is substantially parallel to said second surface,"

451. Yu's surfaces are parallel surfaces, as shown below. As such, Yu teaches *wherein said first surface is substantially parallel to said second surface.*

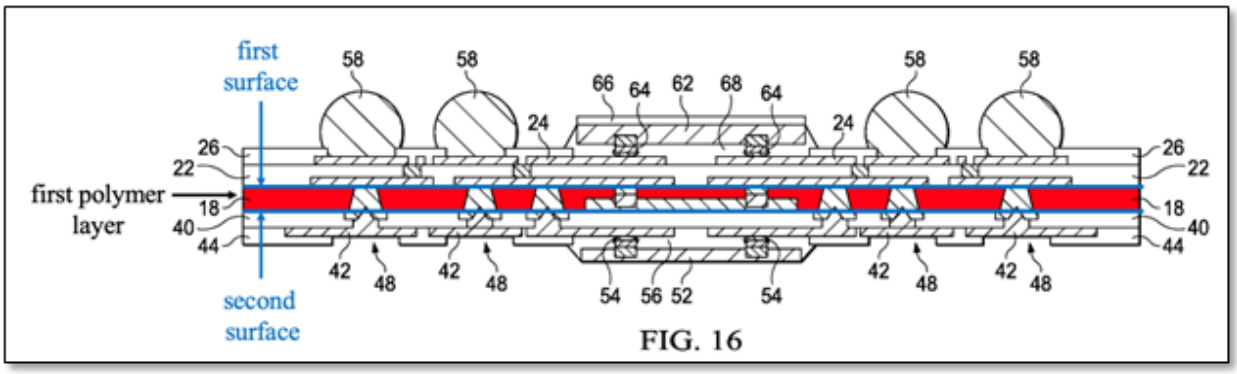


FIG. 16

EX1010 at FIG. 16.

4. 16(a)(ii): "wherein said first polymer layer has a thickness between 100 and 300 micrometers;"

a) Lin-191's Teachings

452. Lin-191 teaches an "encapsulating layer 85" formed "on top[] of the metal pillars or bumps 14," which correspond structurally to conductive vias or posts such as Yu's TMVs (discussed further at Claim 1(b)). *EX1005* at [0109]. Lin-191

explains that the encapsulating layer 85 covers the bumps and the surrounding regions of the substrate to protect and planarize the device structure. *Id*. Because encapsulating layer 85 includes "a polymer layer," it constitutes a polymer layer similar to Yu's molding compound 18, which likewise encapsulates conductive structures within a polymer layer. *Id*.

453. Lin-191's encapsulating layer 85 has a thickness "between about 20 and about 500 micrometers." *EX1005* at [0109]. Similar to my opinions provided for Sundaram for Ground 1A (¶¶ 133-134), Lin-191 renders obvious the claimed *thickness between 100 and 300 micrometers*. *EX1005* at [0109]-[0111]. Because Lin-191 teaches a range ("between about 20 and about 500 micrometers") that includes the narrower claimed range of *between 100 and 300 micrometers*, Lin-191 teaches or renders obvious Claim 16(a)(ii).

454. Additionally or alternatively, Lin-191's encapsulating layer 85 has a *thickness* equal to the combined thickness of layers 1 and metal pillars or bumps 14. Encapsulating layer 85 is "formed…on the metal layer 13 of the patterned metal layer 1," and "top surfaces 14a" of bumps 14 are "substantially coplanar…with a top surface 85a" of layer 85. *EX1005*, [0109-0110], FIG. 12. Thus, as can be seen in FIG. 21 below, encapsulating layer 85's thickness is equivalent to that of layer 1 plus bump 14. Indeed, Lin-191 teaches layer 85 is "ground or polished" such that "top surfaces 14a of" pillars 14 and "top surfaces 24a" of bumps 24 "are substantially

coplanar with…a top surface 85a" of encapsulating layer 85. *EX1005* at [0110]. Pillars 14 have a thickness "between 20 and 110 micrometers[.]" *EX1005* at [0121]. Additionally, pillars 14 are on layer 1, which is formed of adhesion layer 11, seed layer 12, and metal layer 13. *EX1005* at [0075], FIG. 21. Layer 11 has a thickness "less than 1 micrometer, such as between 1 nanometer and 0.5 micrometers," layer 12 has a thickness "less than 1 micrometer, such as between 10 nanometers and 0.8 micrometers," and layer 13 has a thickness "between 3 and 10 micrometers." *EX1005* at [0050], [0060]. Thus, layer 1 plus pillar/bump 14 has a thickness of, at most, 121.3 micrometers (0.5 + 0.8 + 10 + 110) or at least 23.011 micrometers (0.001 + 0.01 +3 + 20). Because layer 85's thickness is the same as the combined thickness of pillars 14 and layer 1, layer 85 thus also has a maximum thickness of 121.3 micrometers, or a minimum thickness of about 23.011 micrometers. *EX1005* at [0050]. Thus, a POSITA would have understood that Lin-191's encapsulating layer 85, like Yu's molding compound 18, is a polymeric solid encapsulant layer of comparable structure and function, disposed over the metal pillars 14 and having a thickness between 23.011 micrometers and 121.3 micrometers, thus teaching or rendering obvious a *thickness between 100 and 300 micrometers*.

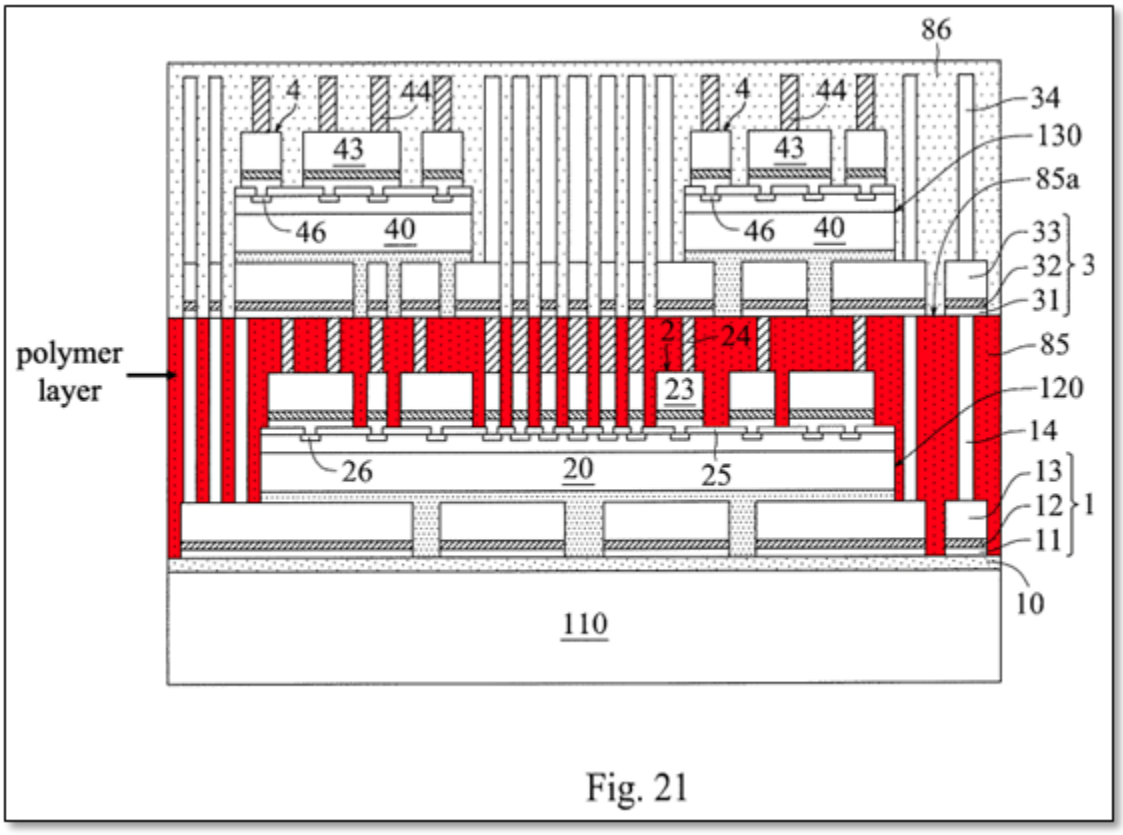


Fig. 21

EX1005 at FIG. 12.

455. Similar to my opinions provided at ¶ 136, I note that the '768 Patent does not indicate any specific criticality for the claimed range. Therefore, for the reasons provided here and in ¶ 136, it is my opinion a POSITA would have found the claimed range obvious.

b) Motivation to Combine

456. A POSITA would have been motivated to apply Lin-191's thickness to Yu's molding compound 18. The modification would have given Yu's molding compound 18 stress buffering capabilities as polymer layers (such as Yu's molding compound 18) having a thickness "between about 30 μm and about 200 μm"

(overlapping with Lin-191's and the claimed range) were known to "act[] as an efficient stress buffer." *EX1080* at [0018]. Stress buffering provided by Yu's molding compound 18 would have been advantageous for a variety of reasons.

457. First, stress buffering provided by Yu's compound 18 and Lin-191's thickness would be beneficial for protecting Yu's die 10 that is in molding compound 18. *EX1010* at 2:61-63, FIG. 2. As demonstrated by Lin-191, the thickness is appropriate for an embedded chip, as encapsulating layer 85 covers chip 120. *EX1005* at FIG. 21. Given that Yu similarly embeds a die 10 in molding compound 18, a POSITA would appreciate that Lin-191's polymer layer thickness would apply to Yu's *first polymer layer*. Given that polymer layers with the claimed thickness were known for embedding chips and buffering stress, a POSITA would appreciate the Yu's die 10 would be protected from stress by molding compound 18, thereby reducing the likelihood of stress-induced damage to die 10. *EX1080* at [0018]. Further, molding/encapsulation layers at the claimed thickness were known to environmentally protect embedded die from "external elements and contaminants." *EX1131* at [0046]; ¶ 54.

458. Additionally, Lin-191's thickness would allow for the opportunity to incorporate metal shielding into Yu's molding compound 18 (*first polymer layer*) which would reduce electromagnetic interference (in the chip package. EMI negatively impacts signal quality in chip packages such that a POSITA would have

found the opportunity to prevent EMI-induced signal degradation. Indeed, ICs were known to "radiate a relatively large amount of electromagnetic energy" that may "interfere with the operation of other devices or circuits in the vicinity of the radiating IC" which prompted the use of "electromagnetic interference (EMI) shielding layer[s]." *EX1136* at 1:28-37, 2:28-30. Such shielding layers were known to be incorporated within and between dielectric layers such that a POSITA would have recognized applying Lin-191's thickness to Yu's molding compound 18 would have advantageously provided the opportunity for such shielding in Yu's package. *See, e.g., EX1137* at 6:1-10, 3:38-41, FIGS. 6-7 (providing a metal power plane 61 (i.e., a shielding layer) that "eliminates crosstalk" within dielectric layers 67, 68).

459. The combination is the application of a known technique (an encapsulant thickness) to a known device (Yu's molding compound 18) ready for improvement to yield predictable results. A POSITA would have had a reasonable expectation of success in applying Lin-191's polymer layer thickness to Yu's compound 18 because the range was a common thickness for molding layers in chip packaging before the '768 Patent. *See* ¶¶ 51-54. Additionally, Lin-191's encapsulating layer 85 is, like Yu's molding compound 18 (*first polymer layer*) formed by a "molding process[.]" *EX1005* at [0109]; *EX1010* at 2:65-66 ("The molding compound 18 can be applied using…compression molding."). Because Lin-191's and Yu's polymer layers are formed using the same process, a POSITA would

have had a reasonable expectation of success in using Yu's molding process to form molding compound 18 according to Lin-191's layer 85 thickness.

5. 16(b): "a first metal plug vertically in a first through via in said first polymer layer,"

460. Yu teaches that "TMV [through molding via] openings 36 are formed through the molding compound 18," and that "a seed layer is deposited … into the TMV openings 36," followed by deposition of a "conductive material." *EX1010* at 3:56–4:6. Yu further discloses that both the seed layer and the conductive material are copper, thereby forming copper-filled through vias within the molding compound. *Id.* As a result, the TMVs 38 shown in Yu correspond to a *first metal plugs* extending *vertically* through the molding compound 18, each positioned within a corresponding TMV opening 36 (via). The copper seed and conductive layers together form solid metallic structures within the through holes, yielding *a first metal plug vertically in a first through via in said first polymer layer*, i.e., the TMV openings 36.

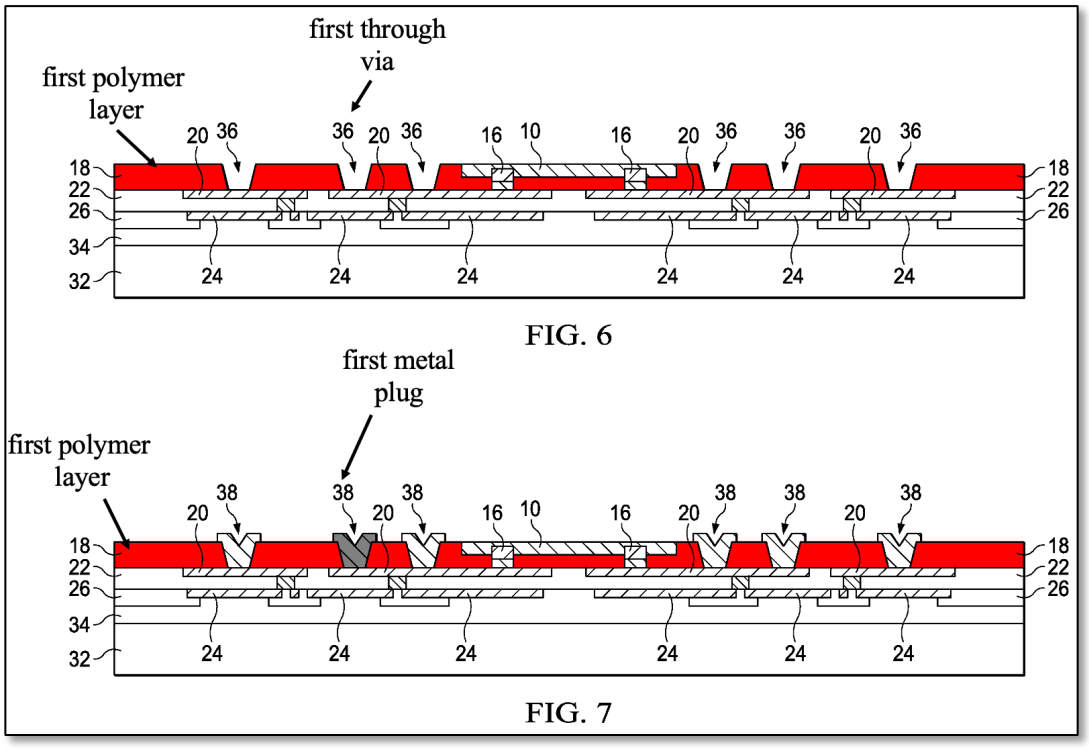


FIG. 6

FIG. 7

EX1010 at FIGS. 6-7.

6. 16(b)(i): "wherein said first metal plug comprises a first copper layer, wherein the first copper layer contacts with a sidewall of said first through via"

461. Yu teaches that a "seed layer is deposited … into the TMV openings 36," and further identifies the seed layer material as copper. *EX1010* at 3:60–64. In Yu, the TMV openings 36 extend through the molding compound 18 to expose the surfaces of underlying conductive regions, and the deposition of the copper seed layer coats the interior surfaces of those openings. *EX1010* at 2:64-3:19; 10:29-33. Thus, the deposited copper seed layer forms a copper layer that contacts the sidewalls of the TMV openings 36. In this way, the copper seed layer of the *first metal plug* is *a first copper layer* that *contacts with a sidewall of said first through*

via. The copper seed layer forms the conductive base upon which additional copper material is subsequently plated to fill the TMV openings 36.

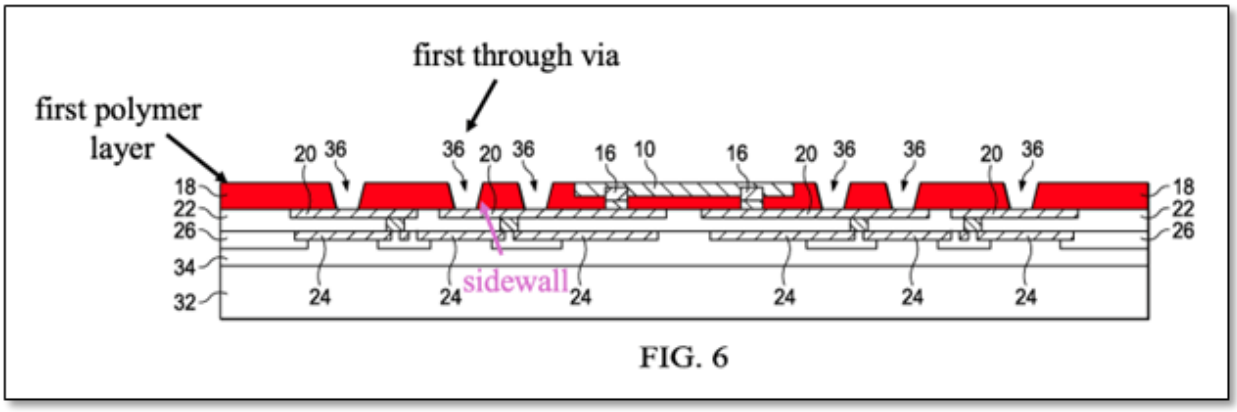


FIG. 6

EX1010 at FIG. 6.

462. I note that Yu's teachings mirror Patent Owner's statements during original prosecution in the'768 Patent, where FIG. 17B is annotated to state "A Cu layer of the metal plug contacts with a sidewall of the through via." *EX1002* at p. 537.

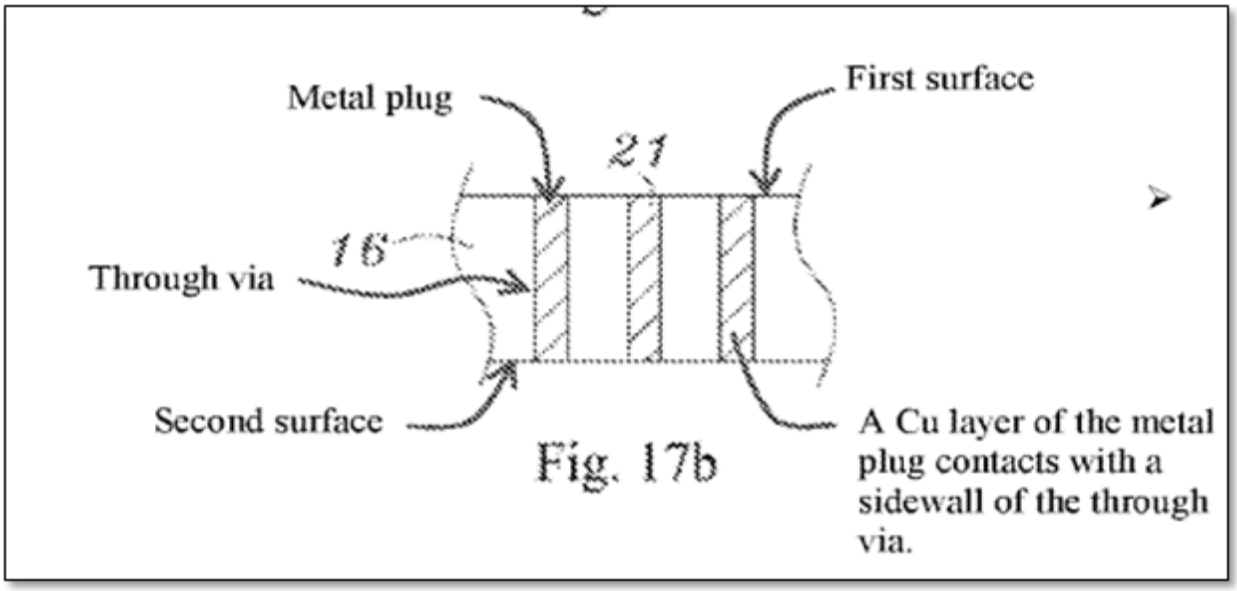


Fig. 17b

EX1002 at p. 537.

7. 16(c): "a second metal plug vertically in a second through via in said first polymer layer,"

463. For the same reasons discussed above regarding the *first metal plug*, a second of Yu's TMVs 38 is a *second metal plug vertically in a second through via in said first polymer layer*, as shown below. *See* ¶ 460.

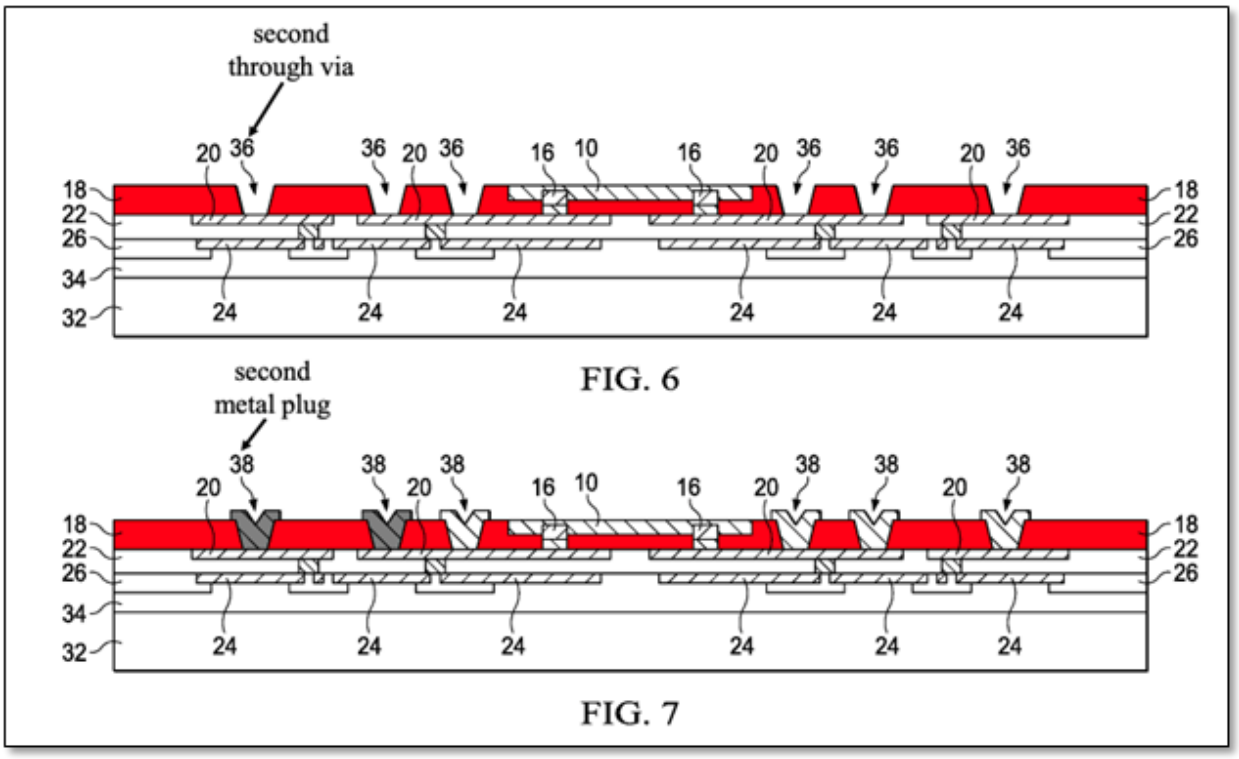


FIG. 6

FIG. 7

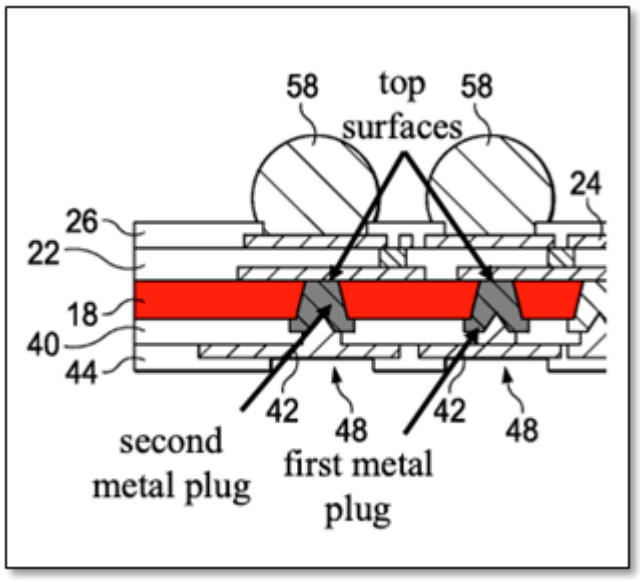
EX1010 at FIGS. 6-7.

8. 16(c)(i): "wherein said second metal plug comprises a second copper layer,"

464. *See* Claim 16(b)(i), ¶¶ 461-462, incorporated herein. Yu teaches plugs comprise a copper seed layer. *EX1010* at 3:60-64.

9. 16(c)(ii): "wherein a top surface of said second metal plug and a top surface of said first metal plug are in the same horizontal plane;"

465. As shown below, the *first* and *second copper plug[s]* comprise *top surface[s]* that *are in the same horizontal plane*. The top surfaces are *in the same horizontal plane* because each top surface is coplanar with the top surface of molding compound 18.



EX1010 at FIG. 16 (excerpt).

10. 16(d): "a first interconnection scheme over said first surface,"

466. Yu teaches a "front side interlayer dielectric (ILD) and redistribution layer (RDL) structure." *EX1010* at 3:4-5. In particular, a seed layer is deposited on the molding compound 18 and patterned to form a "first front-side metallization layer 20." *EX1010* at 3:5-19. A "first ILD layer 22**"** is then deposited over layer 20 and subsequent metallization and ILD layers are formed, including a second

metallization layer 24 and a second ILD layer 26, with openings 28 and 30 formed in the topmost front-side ILD for connectors. *EX1010* at 3:4-19. These layers are all on the molding compound 18 and constitute a *first interconnection scheme* over the *first surface*. *EX1010* at 3:4-19 (front-side ILD/RDL over molding compound 18; first metallization layer 20), 3:20-27 (first ILD layer 22), 3:28-43 (subsequent metallization/ILD including layers 24 and 26; openings 28, 30).

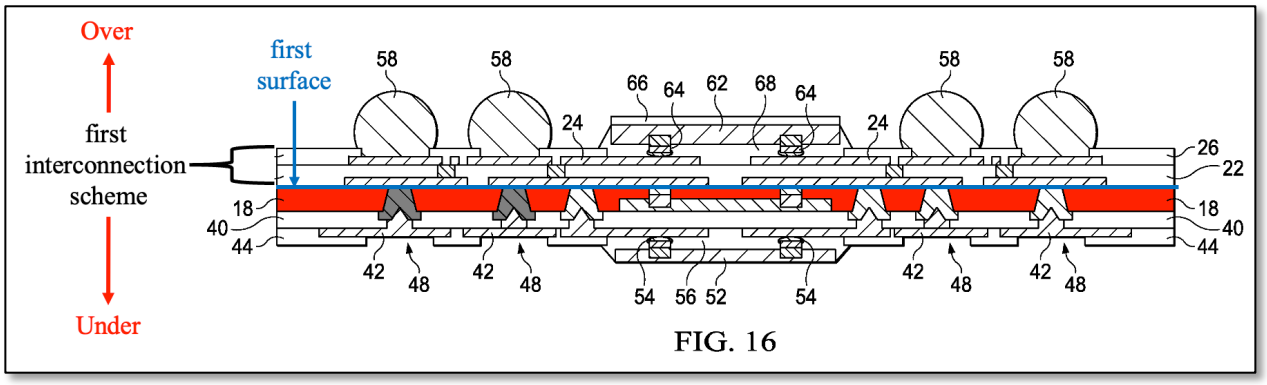


FIG. 16

EX1010 at FIG. 16. I note that metallization layer 20 is assigned a reference numeral in FIGS. 4-7 and 10-11 which depict steps of forming the package 202 of FIG. 16, while the reference numeral for layer 20 in FIG. 16 above is omitted. *See, e.g.,*

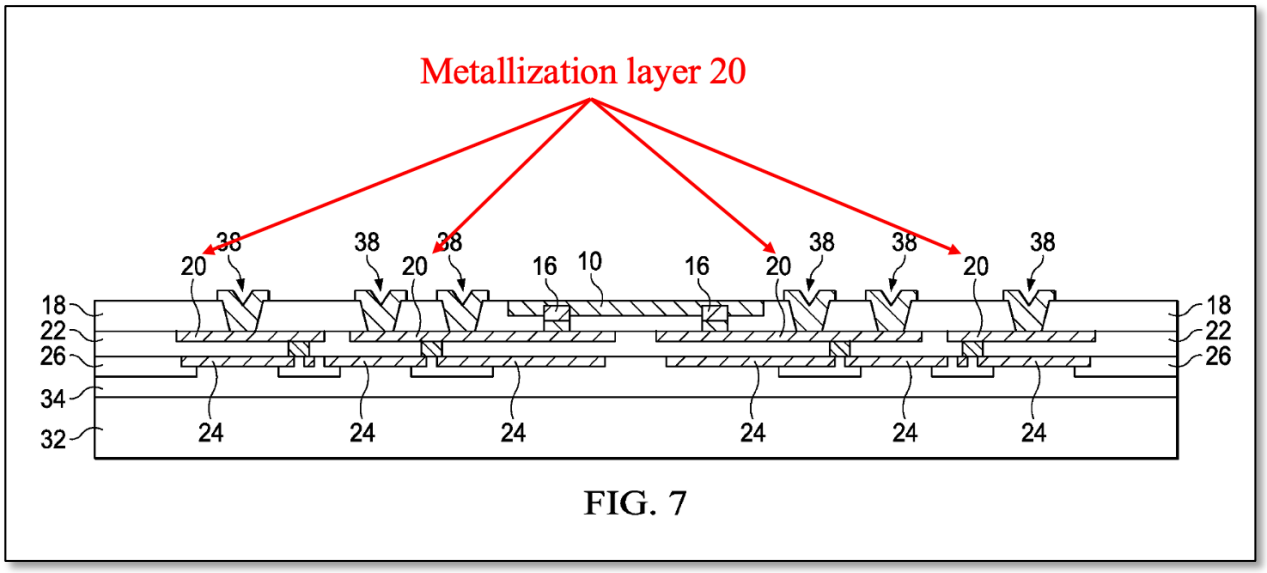


FIG. 7

EX1010 at FIG. 7.

11. 16(d)(i): "wherein said first interconnection scheme comprises a first metal interconnect over said first surface, a second metal interconnect over said first surface and a second polymer layer over said first and second metal interconnects,"

467. Yu teaches that "a seed layer, such as a copper" is "deposited on the molding compound 18" then a "[c]onductive material of the first metallization layer, such as copper… is deposited on the exposed seed layer." *EX1010* at 3:8–18. *EX1010* at 3:8–18. Yu further explains that "the remaining conductive material forms the first front-side metallization layer 20." *EX1010* at 3:18–20. Accordingly, metallization layer 20, which comprises copper, is *a first metal interconnect over said first surface* of molding compound 18 (*first polymer layer*).

468. Yu further discloses additional metallization layers and dielectric layers that together form the complete front-side interconnection scheme. For example, Yu teaches that "[s]ubsequent metallization layers[,]" such as "second metallization

layer 24" are formed "using the same or similar processes" as the first metallization layer 20. *EX1010* at 3:28–32. Metallization layer 24, like metallization layer 20, is thus copper and a portion of second metallization layer 24 is *a second metal interconnect over said first surface.*

469. Yu further teaches that "a first ILD layer 22 is deposited on the front side and over the first metallization layer 20. The first ILD layer 22 may be a polyimide, polybenzoxazole (PBO), benzocyclobutene (BCB), the like, or a combination thereof." *EX1010 at* 3:21–27. Thus, ILD layer 22 comprises a polyimide and is a *polymer*. A "second ILD layer 26" that is "formed using the same" process as ILD layer 22 is also a *polymer*. Because both layers 22, 26 are made of a *polymer*, ILD layer 22 and ILD layer 26 are, collectively, a *second polymer layer*. As shown, Yu's *second polymer layer* is *over said first and second metal interconnects*:

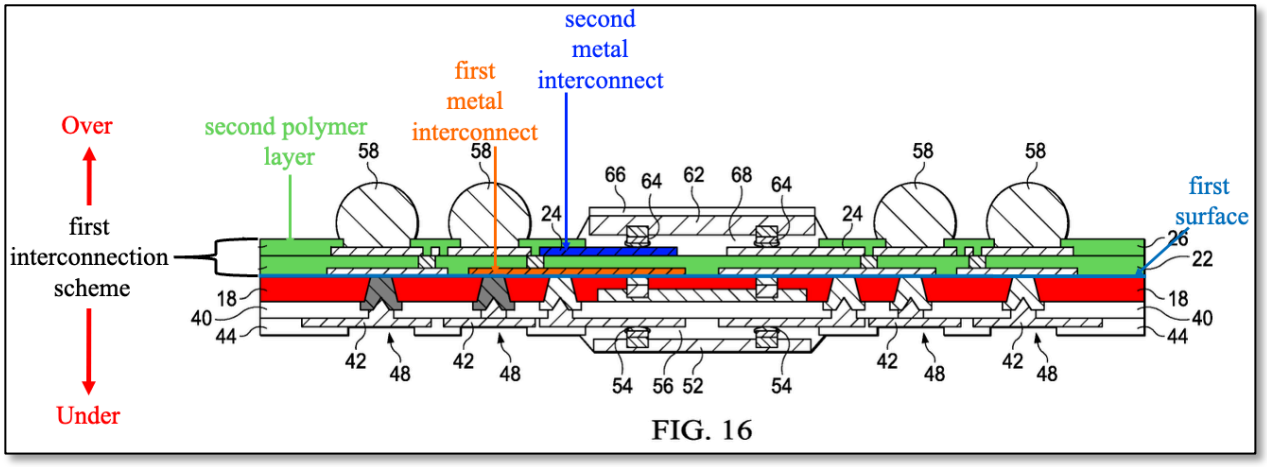


FIG. 16

EX1010 at FIG. 16.

12. 16(d)(ii): "wherein said first metal interconnect is connected to said first metal plug,"

470. As shown below, Yu teaches that "TMV [through molding via] openings 36 are formed through the molding compound 18 to the first front side metallization layer 20," followed by deposition of a seed layer and electroplating of a conductive material such as copper to form TMVs 38. *EX1010* at 3:5-19. The TMVs 38 extend through the molding compound 18 and make electrical contact with the first front-side metallization layer 20. Accordingly, metallization layer 20 (*first metal interconnect*) is *connected to said first metal plug*. In other words, because Yu teaches that the TMV openings 36 are formed to the first front-side metallization layer 20 and subsequently filled with copper to form TMVs 38 in contact with that layer, the *first metal plug* is *connected to* the *first metal interconnect*.

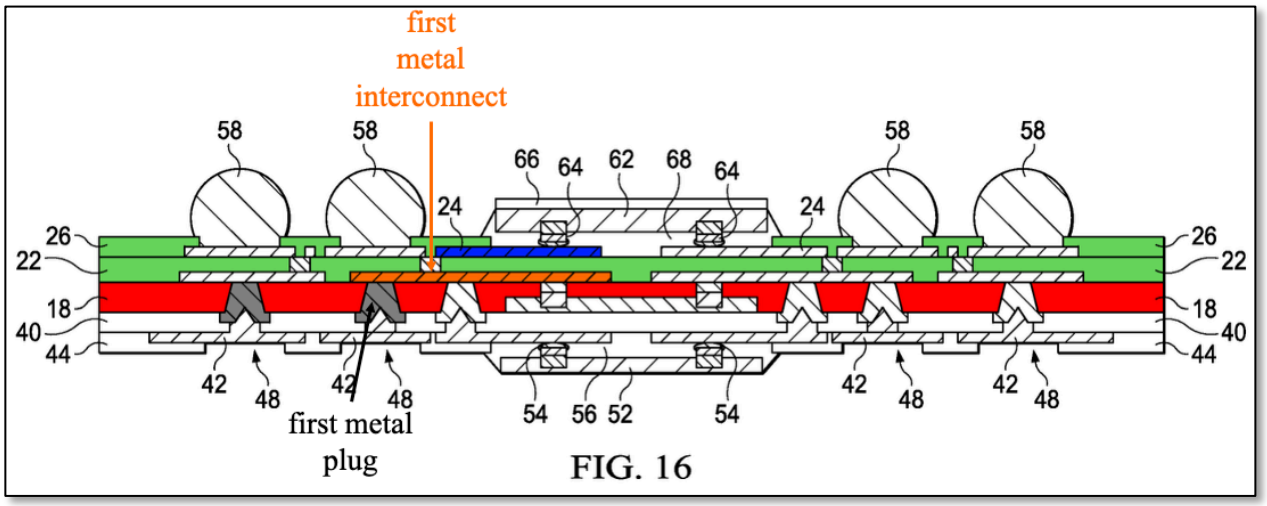


FIG. 16

EX1010 at FIG.16.

13. 16(d)(iii): "wherein said first metal interconnect comprises a first metal layer, a third copper layer on said first metal layer, and a fourth copper layer on said third copper layer;"

471. Metallization layer 20 (*first metal interconnect*) includes a "seed layer, such as **copper**…deposited on the molding compound 18," and a "[c]onductive material…such as **copper**…is deposited on the exposed seed layer, such as by…electroplating" *EX1010* at 3:5-19. Thus, metallization layer 20's copper "seed layer" is *a third copper layer*, and the copper "conductive material" deposited on the seed layer is *a fourth copper layer on* the copper seed layer (*said third copper layer*).

a) Lin-191's Teachings

472. *See* ¶¶ 160-161 for Lin-191's teachings, incorporated herein. Lin-191's adhesion layer 31 is a *first metal layer* with two copper layers formed thereon.

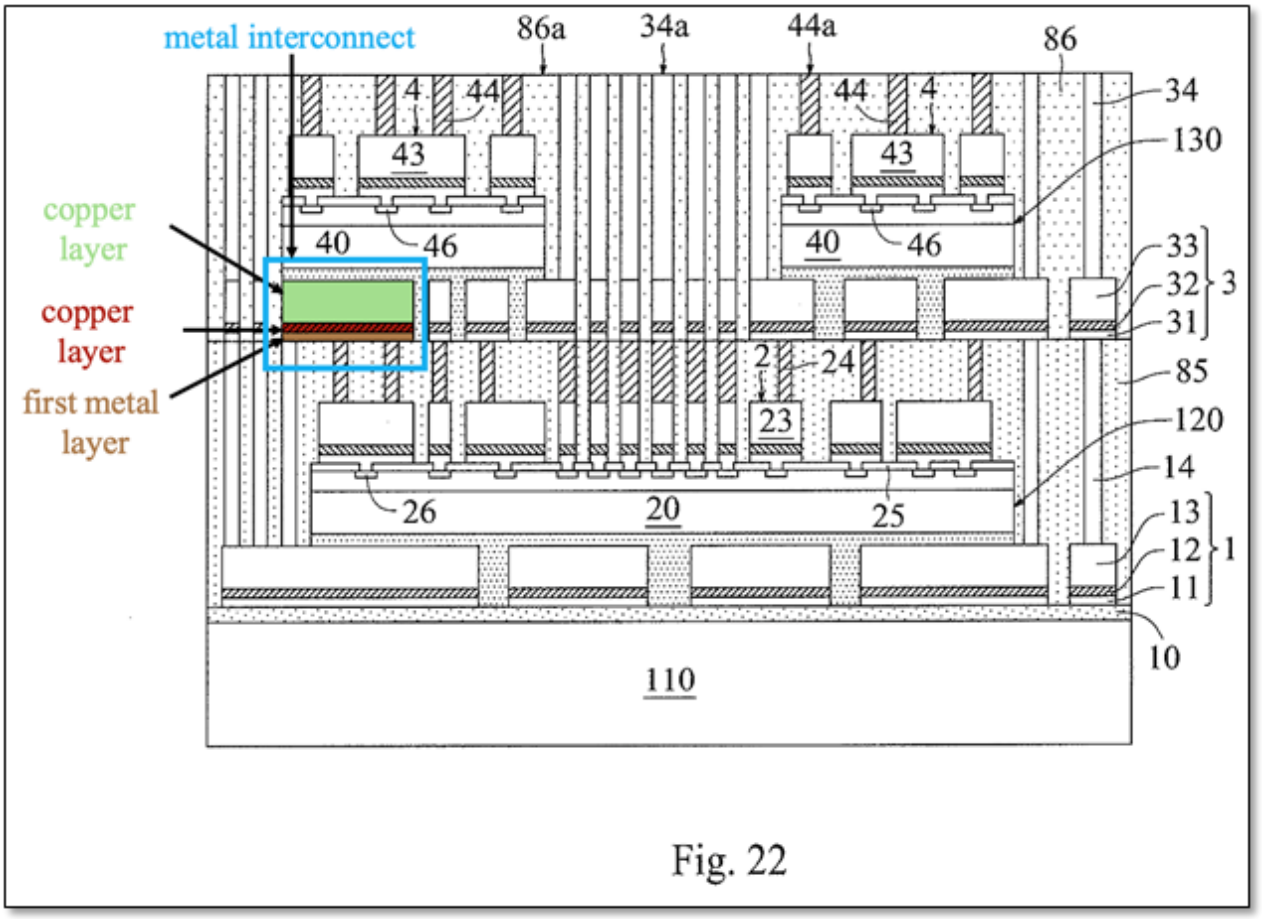


Fig. 22

EX1005 at FIG. 22, [0127].

b) Motivation to Combine

473. The MTCs and reasonable expectation of success for modifying Sundaram per Lin-191 apply for the Yu-Lin-191 combination as well. *See* ¶¶ 162-170. A POSITA would have appreciated the similarities between Yu's and Lin-191's metal interconnects, as like Yu's metallization layer 20 (*first metal interconnect*), Lin-191's metal interconnect comprises a copper seed layer 32 and a copper metal layer 33. *EX1005* at [0127-0128], [0133]. A POSITA would have found it obvious and been motivated to apply Lin-191's three-metal layer interconnect teachings,

including adhesion layer 31 (*first metal layer*) having two copper layers formed thereon to Yu's metallization layer 20 such that the *first metal interconnect comprises a first metal layer, a third copper layer on said first metal layer, and a fourth copper layer on said third copper layer*. The modification would have provided Yu's first metal interconnect with the benefits of Lin-191's adhesion layer 31. As I discussed above, nickel adhesion layers were known to prevent diffusion of copper into adjacent metal interconnects, thereby reducing the risk of delamination. *See* ¶ 162.

474. The combination is the application of a known technique (Lin-191's three-layer metal interconnect) to a known device (Yu's metal interconnect) ready for improvement to yield predictable results, i.e., Yu's metallization layer 20 having a *first metal layer*. There would have been a reasonable expectation of success because Lin-191 teaches forming adhesion layer 31 using manufacturing techniques also taught by Yu such that the modification would have been simple and straightforward. For example, Lin-191 teaches using a "sputtering process[,]" "physical-vapor deposition (PVD) process," and electroplating, which are all techniques taught by Yu. *EX1005* at [0127], [0134]; *EX1010* at 3:5-8 ("A seed layer…is deposited…such as by sputtering or another physical vapor deposition process.), 3:11-14 ("Conductive material…is deposited…such as by…electroplating[.]"). Because Lin-191's multi-layer metal interconnect is formed

using the same techniques that Yu's *first metal interconnect* is formed by, the modification would have merely required forming an additional metal layer (*first metal layer*) using Yu's existing techniques. Accordingly, there would have been a reasonable expectation of success.

14. 16(e): "a first metal bump over said first interconnection scheme,"

475. Yu teaches that "conductive connectors 58, such as ball grid array (BGA) balls," are "formed on the front side of the package in the openings 28." *EX1010* at 4:45–49. Yu further explains that the openings 28 are formed through the topmost ILD layer 26 to expose portions of the "topmost front-side metallization layer, such as the second metallization layer 24," to which the connectors are electrically coupled. *Id*. at 3:31–36. Yu also teaches that the conductive connectors 58 may be "a lead-free solder" i.e., *metal Id*. at 4:47–50. These connectors 58 are positioned on the front side of the package above the multilayer ILD/RDL stack, including metallization layers 20 and 24 and ILD layers 22 and 26, that together form the *first interconnection scheme*. Accordingly, a connector 58 is *a first metal bump over said first interconnection scheme* because Yu expressly teaches that conductive connectors (BGA balls) 58 are formed on the front side of the package and in electrical contact with the upper metallization layer of the interconnection structure.

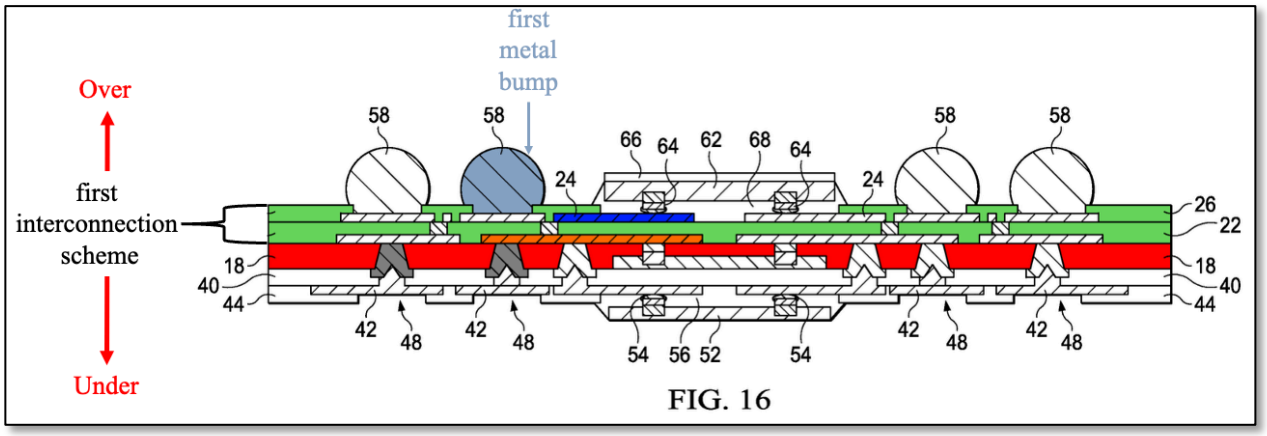


FIG. 16

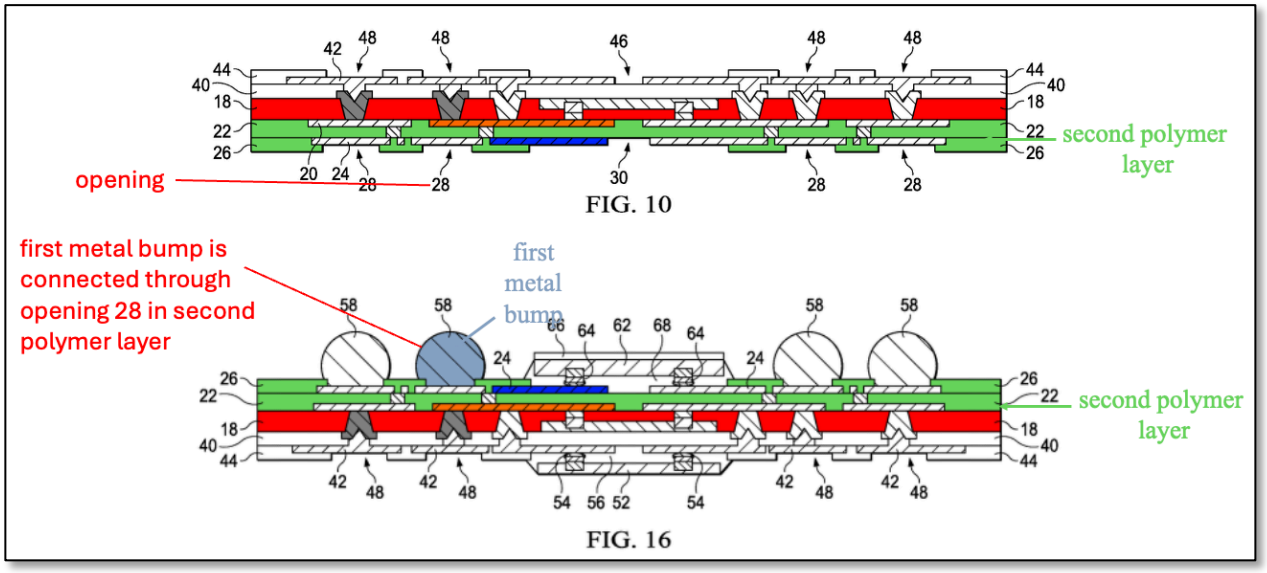
EX1010 at FIG. 16.

15. 16(e)(i): "wherein said first metal bump is connected to said first interconnection scheme through a first opening in said second polymer layer,"

476. Yu teaches that "after forming the topmost ILD layer, the second ILD layer 26 in this embodiment, openings 28 and 30 are formed through the topmost front side ILD layer for connectors coupled between the topmost front side metallization layer, such as the second metallization layer 24, and another package, another die, and/or another substrate." *EX1010* at 3:35-40. Accordingly, Yu identifies openings 28 as vias or through-holes that are patterned into the second ILD layer 26 to expose portions of the underlying metallization layer 24 for electrical connection. The openings are explicitly associated with the subsequent formation of conductive connectors that electrically couple the front-side metallization to external components.

477. Yu further explains that "conductive connectors 58, such as ball grid array (BGA) balls, [are] formed on the front side of the package in the **openings 28**.

Bond pads may be formed in the openings 28 on the front side of the package, and connectors 58 may be formed on the bond pads." *EX1010* at 4:45-48. Thus, each opening 28 in the second ILD layer 26 provides a passage for depositing and connecting the conductive bond pads and solder balls of connector 58 to the underlying copper metallization. As such, the *first metal bump* (connector 58) *is connected to the first interconnection scheme through a first opening* (openings 28) *in said second polymer layer* (second ILD layer 26).



EX1010 at FIGS. 10, 16.

16. 16(e)(ii): "wherein said first metal bump comprises a tin-containing layer;"

478. Yu teaches that "connectors 58 may be lead-free solder." *EX1010* at 4:47–50. A POSITA would have the "lead-free solder" to include tin, since tin-based alloys (for example, SnAg or SnAgCu compositions) were the dominant lead-free materials used in commercial packaging applications. A POSITA would have

understood the Yu's lead-free solder to be a *tin-containing layer* because Sn-based solders were dominant in commercial packages such as those taught by Yu. Thus, the context of the chip packages of Yu means that "solder" necessarily includes Sn-content, thereby teaching the *tin-containing layer*. A POSITA would have understood Yu's disclosure of "lead-free solder" to mean the solder contains tin unless stated otherwise. That is, if someone refers to non-tin-containing solder, it would be specified as such because the "default" solder contains tin.

a) Lin-191's Teachings and MTC

479. Additionally, Lin-191 teaches a metal bump comprising *a tin-containing layer over said second metal layer*. *See* ¶¶ 173-174, incorporated herein. A POSITA would have been motivated, found it obvious, and had a reasonable expectation of success in modifying Yu per Lin-191 for the same reasons discussed for Sundaram-Lin-191. *See* ¶¶ 175-179, incorporated herein. The Yu-Lin-191 combination is application of known technique (Lin-191's solder bump structure) to a known device (Yu's connector 58) ready for improvement to yield predictable results, i.e., Yu's connector 58 comprising a *tin-containing layer*.

17. 16(f): "a second metal bump over said first interconnection scheme,"

480. For the same reasons described above regarding the *first metal bump*, Yu teaches a *second metal bump*, namely another connector 58. *See* ¶ 475. As shown, the *second metal bump* is *over said first interconnection scheme*:

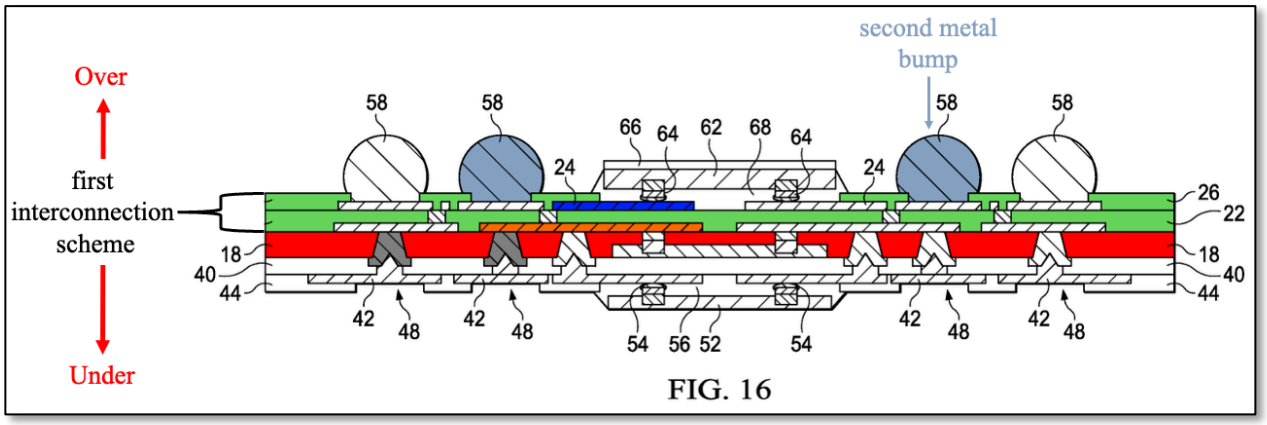
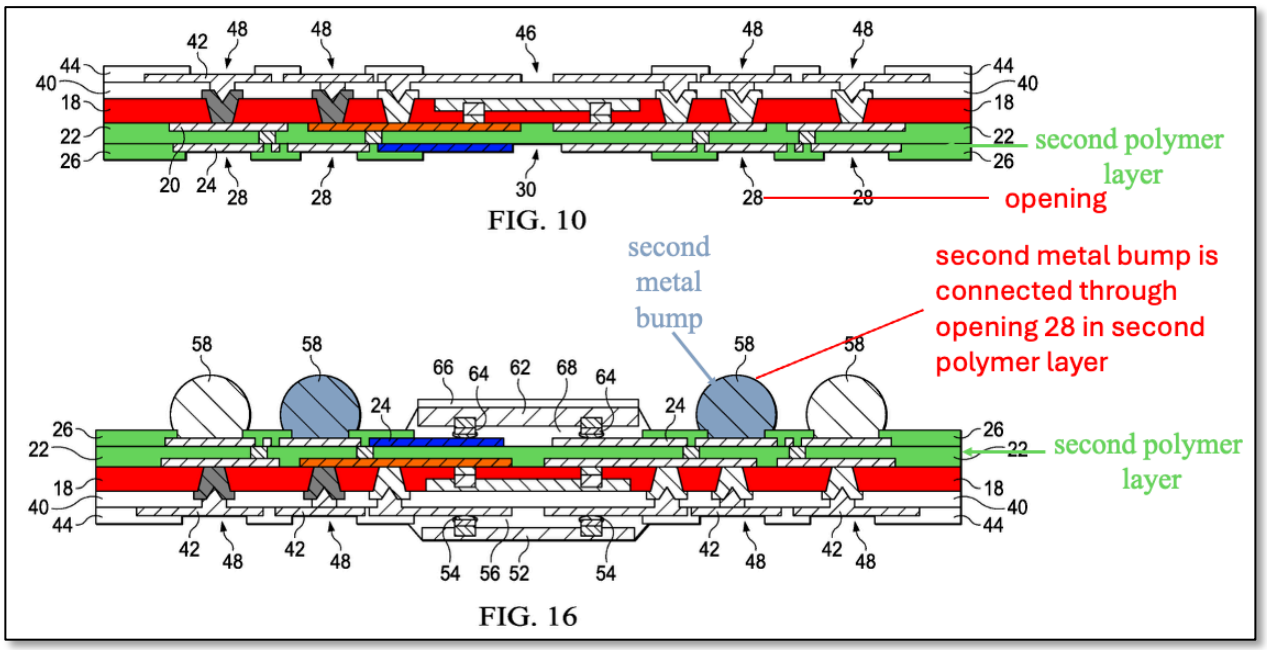


FIG. 16

EX1010 at FIG. 16.

18. 16(f)(i): "wherein said second metal bump is connected to said first interconnection scheme through a second opening in said second polymer layer;"

481. For the same reasons described above at Claim 16(e)(i), based on Yu's teachings, Yu's *second metal bump* (connector 58) *is connected to said first interconnection scheme through a second opening in said second polymer layer*. *See* ¶¶ 476-477.



EX1010 at FIGS. 10, 16.

19. 16(g): "a first semiconductor chip over said first interconnection scheme and between said first and second metal bumps;"

482. Yu's package includes "die 62, such as a memory die" (*first semiconductor chip*) that is "attached…to conductive features in the second front side metallization layer 24." *EX1010* at 4:53-53. As shown, die 62 is positioned *over said first interconnection scheme and between said first and second metal bumps*:

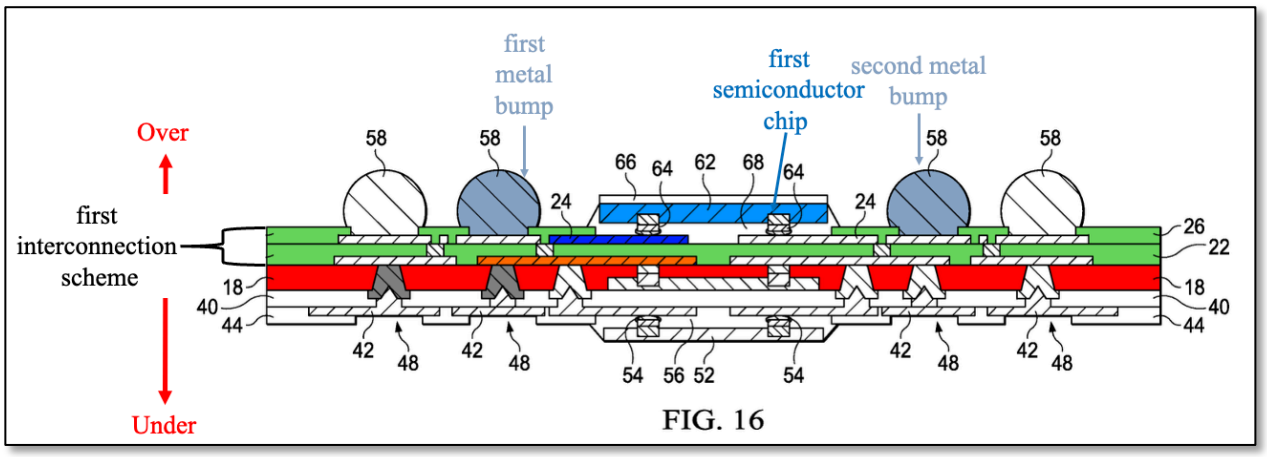


FIG. 16

EX1010 at FIG. 16.

20. 16(h): "a third metal bump between said first semiconductor chip and said first interconnection scheme,"

483. Yu teaches that die 62 is connected through "connectors 64, such as controlled collapse chip connection (C4) bumps," which "attach to the conductive features in the second front-side metallization layer 24." *EX1010* at 4:56-60. A POSITA would recognize that these C4 bump connectors 64 are solder bumps commonly formed from tin-containing alloys (e.g., Sn-Ag-Cu systems) (i.e., *metal*),

consistent with standard C4 bumping processes in semiconductor packaging. *See* ¶ 70.

484. Accordingly, the C4 connector 64 is a *third metal bump* and, as shown, the *third metal bump* is *between said first semiconductor chip and said first interconnection scheme*:

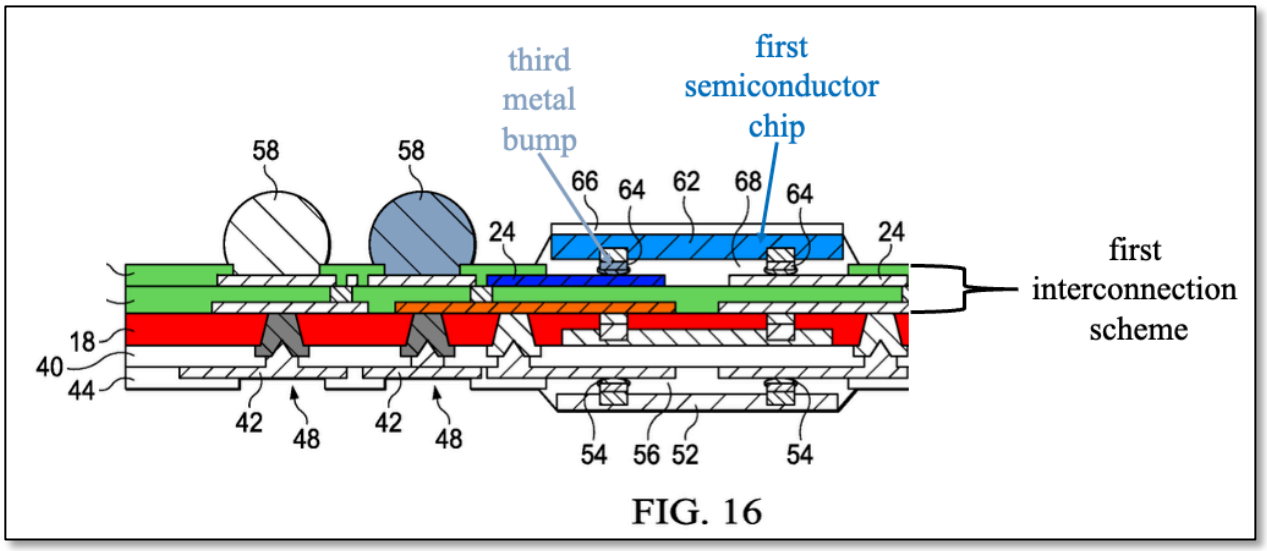


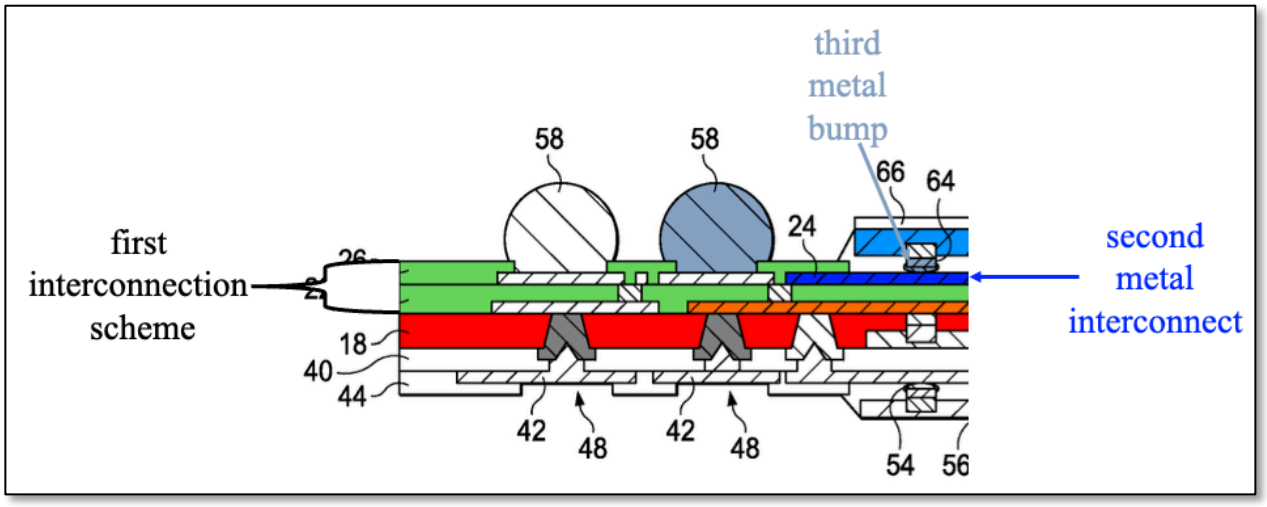
FIG. 16

EX1010 at FIG. 16 (excerpt).

21. 16(h)(i): "wherein said third metal bump connected to said second metal interconnect through a third opening in said second polymer layer; and"

485. Yu teaches that die 62 "is attached…to conductive features in the second front-side metallization layer 24 … by conductive connectors 64, such as C4 bumps." *EX1010* at 5:15-19. Yu further states that "the third die 62 may be attached … by reflowing connectors 64 between the third die 62 and the conductive features in the second front-side metallization layer 24," confirming that the connector 64

electrically connects die 62 to the second metallization layer 24 (i.e., the *second metal interconnect*). *EX1010* at 4:56-60. Accordingly, Yu's *third metal bump* is *connected to said second metal interconnect*:



EX1010 at FIG. 16 (excerpt).

486. Yu further teaches that die 62 is "attached **through the opening 30** to conductive features in …the second front-side metallization layer 24." *EX1010* at 4:54-56. Because connector 64 (*third metal bump*) couples die 62 to layer 24 through opening 30 in the *second polymer layer*, Yu teaches *the third metal bump* is *connected to said second metal interconnect through a third opening* (opening 30) *in said second polymer layer*:

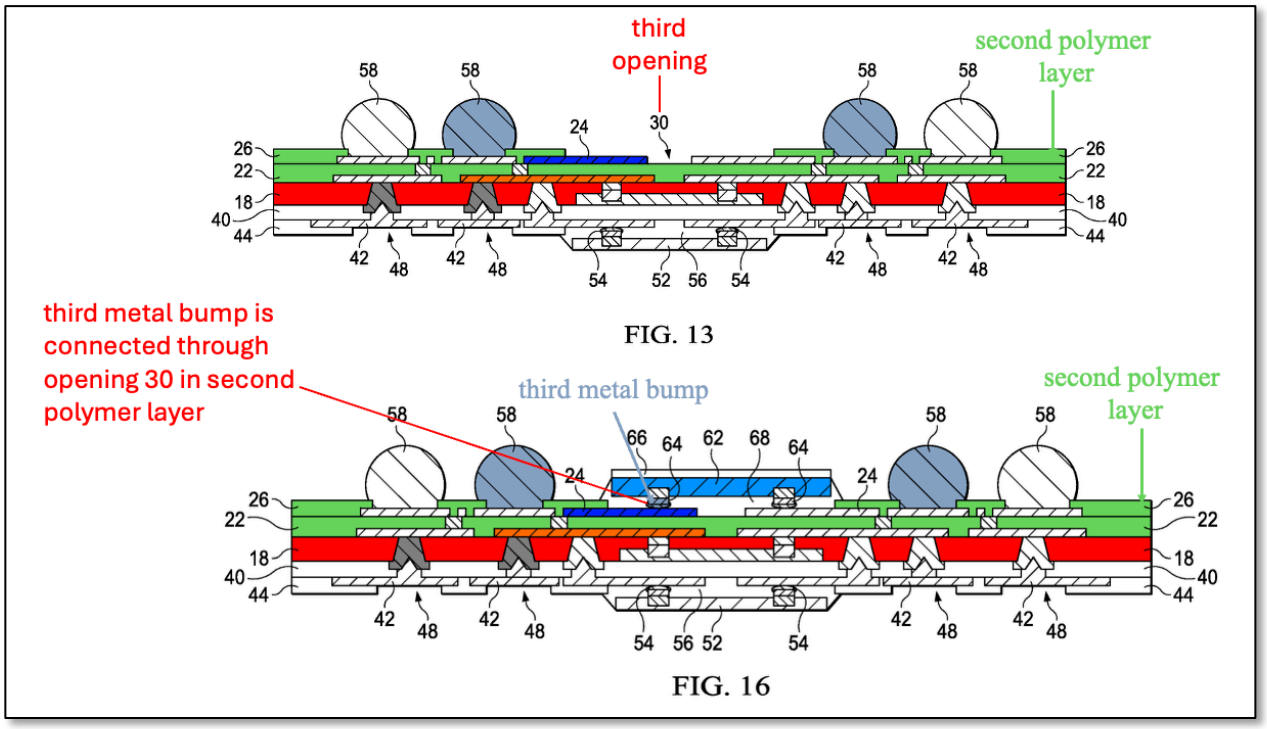


FIG. 13

FIG. 16

EX1010 at FIG. 13, 16.

22. 16(i): "a second semiconductor chip under said first interconnection scheme and said first semiconductor chip,"

487. Yu teaches a "die 52, such as a memory die" that is "attached…to conductive features in the second back side metallization layer 42," such that die 52 is a *second semiconductor chip*. *EX1010* at 4:30-33. Yu's FIG. 16 shows die 52 positioned *under* the *first interconnection scheme* and *under* die 62 (*first semiconductor chip*. Accordingly, Yu teaches a *second semiconductor chip under said first interconnection scheme and said first semiconductor chip*:

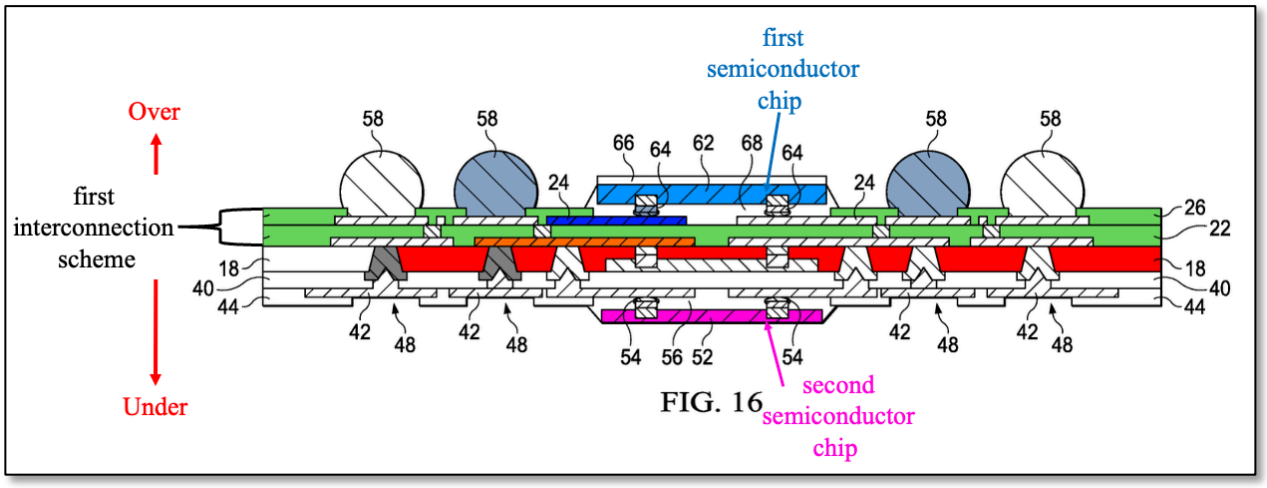


FIG. 16

EX1010 at FIG. 16.

23. 16(i)(i): "wherein said first interconnection scheme is between said first and second semiconductor chips,"

488. As shown below, Yu's *first interconnection scheme is between said first and second semiconductor chips*:

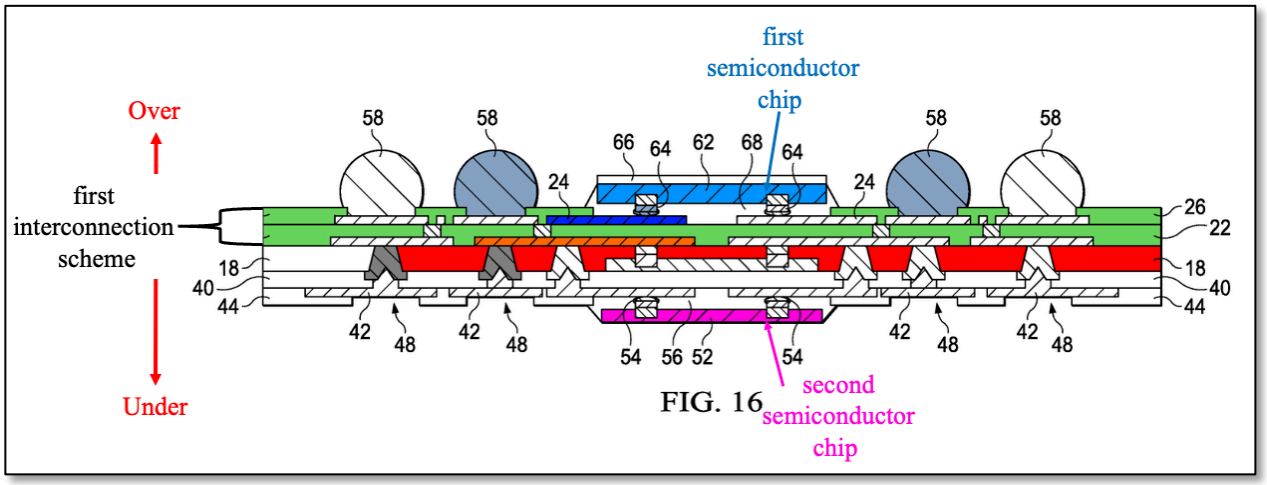


FIG. 16

EX1010 at FIG. 16.

24. 16(i)(ii): "wherein said second semiconductor chip comprises a central-processing-unit (CPU) circuit block and a graphics-processing-unit (GPU) circuit block."

a) Lin-191's Teachings and Motivation to Combine

489. *See* ¶ 210, incorporated herein. The same MTCs and reasonable expectation of success for modifying Sundaram per Lin-191 apply to modifying Yu per Lin-191, e.g., increasing the functionality of Yu's chip package. *See* ¶¶ 211-213, incorporated herein.

B. *Claim 17: "The chip package of claim 16, further comprising a third semiconductor chip over said first interconnection scheme."*

490. As I discussed above, Yu's package 202 as depicted in FIG. 16 is part of FIG. 52's PoP structure (*chip package*). *See* ¶¶ 445-448. As shown, the PoP structure of FIG. 52 includes a package 204 that is positioned over FIG. 16's package 202. *EX1010* at FIG. 52. Package 204 include a "die 174, such as a logic circuitry die" (i.e., a *third semiconductor chip*). As shown, die 174 is positioned *over said first interconnection scheme*:

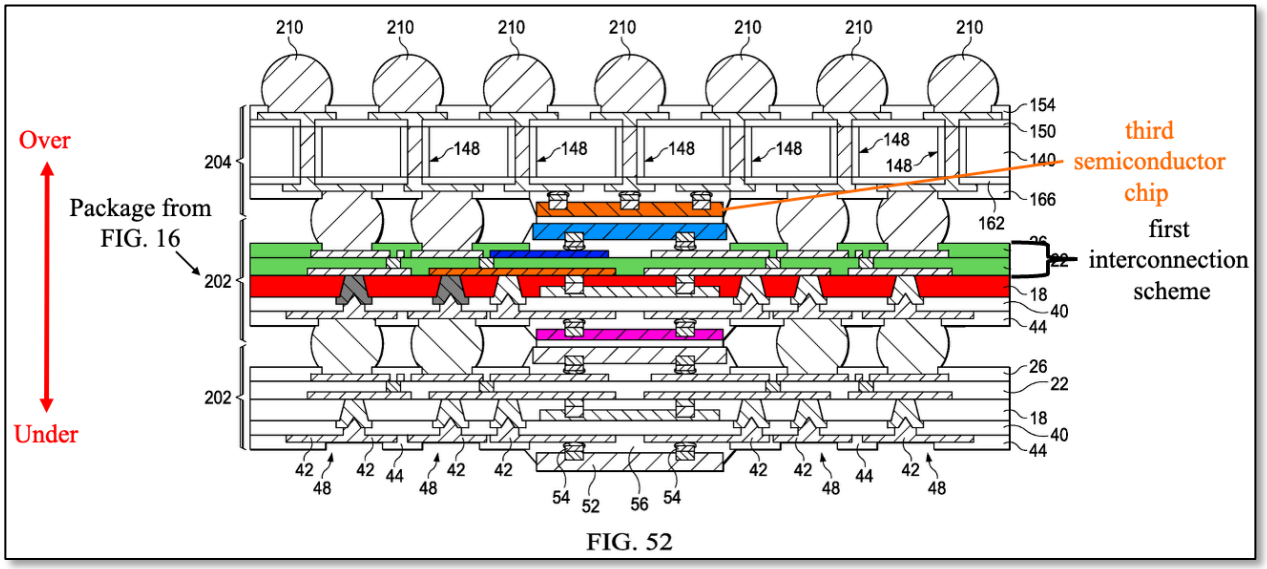


FIG. 52

EX1010 at FIG. 52, 8:35-39 ("FIG. 51 shows that multiple packages 202…can be stacked in the PoP structure. In FIG. 52, connectors 210…[are] formed[.]"), 8:11-12.

C. *Claim 19: "The chip package of claim 16, further comprising a third metal plug vertically in a third through via in said polymer layer, wherein a pitch between said first and third metal plugs is between 200 and 1000 micrometers."*

491. For the same reasons described above regarding the *first metal plug*, another of TMVs 38 is a *third metal plug vertically in third through via in said polymer layer*[6] as shown below:

[6] I have been instructed to interpret Claim 19's *polymer layer* as referring to the *first polymer layer* introduced in Claim 16(a).

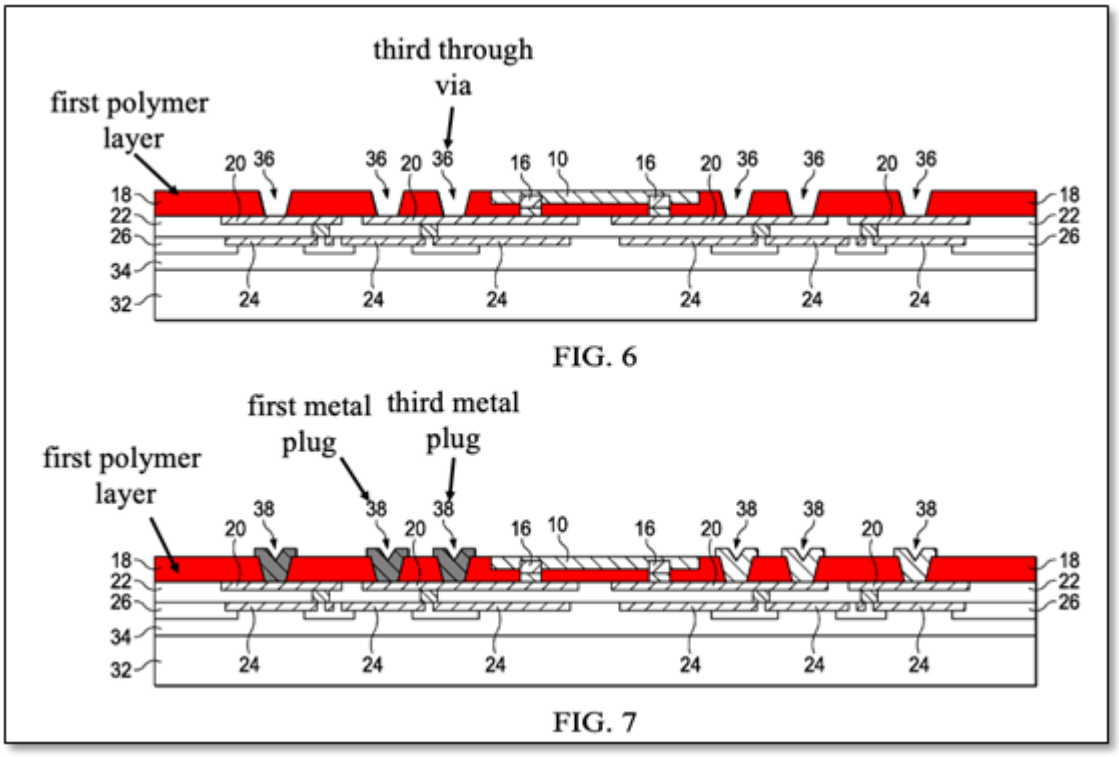


FIG. 6

FIG. 7

EX1010 at FIGS. 6-7; ¶ 460.

a) Lin-191's Teachings and Motivation to Combine

492. As I discussed above, Lin-191 teaches an "encapsulating layer 85" that is analogous to Yu's molding compound 18. *See* ¶ 452. Lin-191 further teaches "metal pillars or bumps 14" in encapsulating layer 85 that, like Yu's TMVs 38, are made of "copper" and interconnect components of a chip package. *EX1005* at [0066], [0086]. The "pitch between neighboring or adjacent pairs of metal pillars or bumps 14" can be "between 100 and 250 micrometers," therefore teaching or rendering obvious *between 200 and 1000 micrometers*. *EX1005* at [0075].

493. I note that the '768 Patent does not indicate any criticality of the claimed pitch. *EX1001* at 6:8-15. That is, the '768 Patent does not provide the range

of 200 and 1000 micrometers and then further provide an explanation for why such range is needed, important, or advantageous. Indeed, the '768 Patent describes a variety of ranges, including smaller (5 micrometers) and much larger values (10000 micrometers), indicating to a POSITA that the thickness can vary widely and that the thickness is not otherwise critical. *See EX1001* at 6:8-15.

494. A POSITA would have found it obvious and been motivated to apply Lin-191's pitch to Yu's *first* and *third copper plug[s]*, which are likewise neighboring/adjacent, as shown above. A pitch *between 200 and 1000 micrometers* was known to enable high bandwidth speeds such as "at least about 10 GB/s" in a "digital camera for cell phones[.]" *EX1004* at 6:42-55, FIG. 33 (showing a pitch of neighboring plugs between 220-240 μm). Yu already contemplates chip packages for use "in the mobile telephone/PDA market." *EX1010* at 1:53-55. Accordingly, a POSITA would have been motivated to implement Lin-191's *pitch* of *between 200 and 1000 micrometers* to Yu's *first* and *third copper plug[s]* which was known to provide benefits in cell phones.

495. The combination is the application of a known technique (Yu's plugs having a pitch between *200 and 1000 micrometers*) to a known device (Yu's chip package) ready for improvement to yield predictable results, i.e., Yu's first and third plugs having a pitch between *200 and 1000 micrometers*. A POSITA would have a reasonable expectation of success at least because the modification would have been

simple and straightforward as methods of controlling pitch of metal plugs were well-known. Indeed, the modification would have merely required forming the openings 36 in which TMVs 38 are formed to have such a pitch, and Yu already teaches a "laser technique or a mechanical process like drilling" is used to form openings 36, thereby leading to a reasonable expectation of success.

496. Additionally, because Yu explicitly discloses forming TMVs using "laser technique[s] or a mechanical process like drilling," both of which allow precise adjustment of via spacing and diameter, the modification would have been easily implementable. *EX1010* at 3:66–4:1. Lin-191's pitch parameters would therefore be directly implemented using Yu's described manufacturing methods without requiring new materials or processes, further leading to a reasonable expectation of success. A POSITA would have viewed the modification as a routine design optimization, applying a known fine-pitch interconnect spacing from Lin-191 to Yu's analogous TMV structure—to achieve predictable improvements in bandwidth density, form factor reduction, and mechanical reliability.

D. *Claim 22: "The chip package of claim 16, further comprising a passive component over said first surface."*

497. *See* Claim 2, ¶¶ 382-387, The motivations to combine Yu with Lin-191 parallel those for Haba-Lin-191. Yu's already teaches "chip resistors" and "chip capacitors," which are *passive component[s]* as described by the '768 Patent. *EX1010* at 1:41-45; *EX1001* at 13:55-57 ("…a passive device 44…such as an

inductor, a capacitor or resistor." Lin-191 teaches connecting *passive component[s]* in a multiple chip package.

498. A POSITA would have been motivated to apply Lin-191's teachings of integrating a *passive component* over Yu's *first surface* because Yu expressly teaches that its "front-side metallization layer 24" routes signals to external packages via connectors 58 and C4 bumps 64. *EX1010* at 5:15-23. Integrating a passive component above that interconnect region would advantageously preserve signal integrity, mitigate crosstalk, and reduce parasitic effects along those same signal paths.

499. The modification represents the application of a known technique (integrated passive component) to a known device (Yu's PoP chip package), yielding predictable improvements in high-frequency performance. It would have had a reasonable expectation of success because passives were already ubiquitous in advanced packaging at the time. A POSITA would thus view the adaptation as simple and straightforward, involving routine implementation of known packaging features for predictable electrical benefits.

E. *Claim 23: "The chip package of claim 16, wherein said first interconnection scheme comprise a third metal interconnect across over a sidewall of the second semiconductor chip."*

500. For the same reasons described above, another portion of metallization layer 20 is *a third metal interconnect* that is part of the *first interconnection scheme*.

See ¶ 467. Further, as shown below, the *third metal interconnect* is both *across* and *over* a *sidewall* of die 52 (*second semiconductor chip*). The blue dashed line indicates the *sidewall* of die 52, namely a boundary thereof. Notably, the *third metal interconnect* is positioned in the "over" direction relative to the *sidewall*, as indicated by the red arrow depicting the over/under directions. Additionally, the *third metal interconnect* extends laterally (i.e., left/right) to the right past the boundary of the *sidewall*. Thus, the *third metal interconnect* is both *across* and *over a sidewall of the second semiconductor chip*.

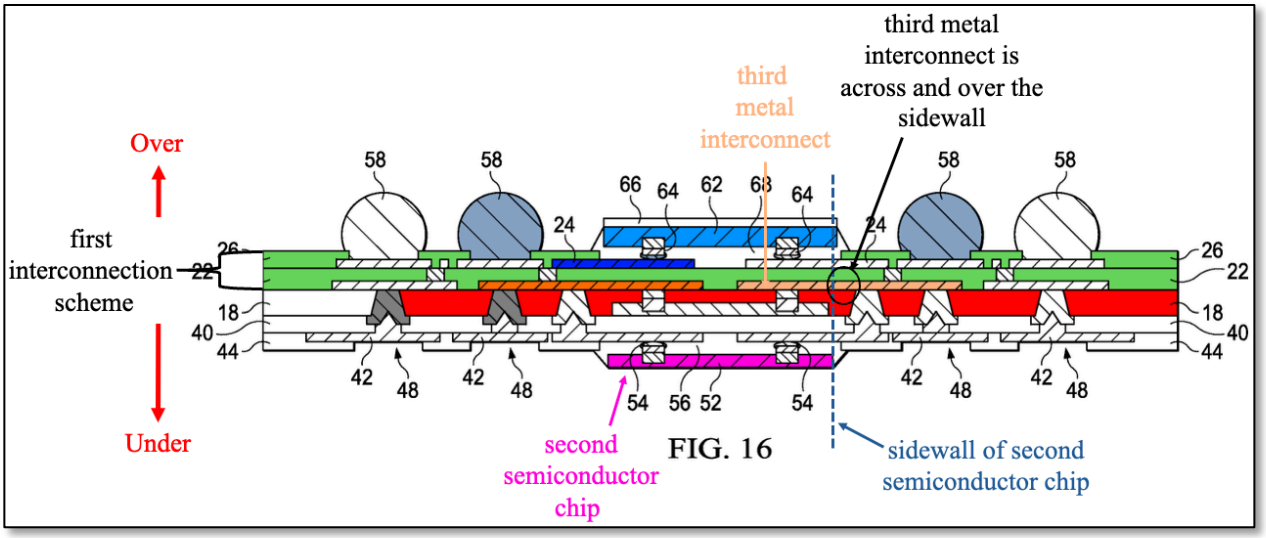
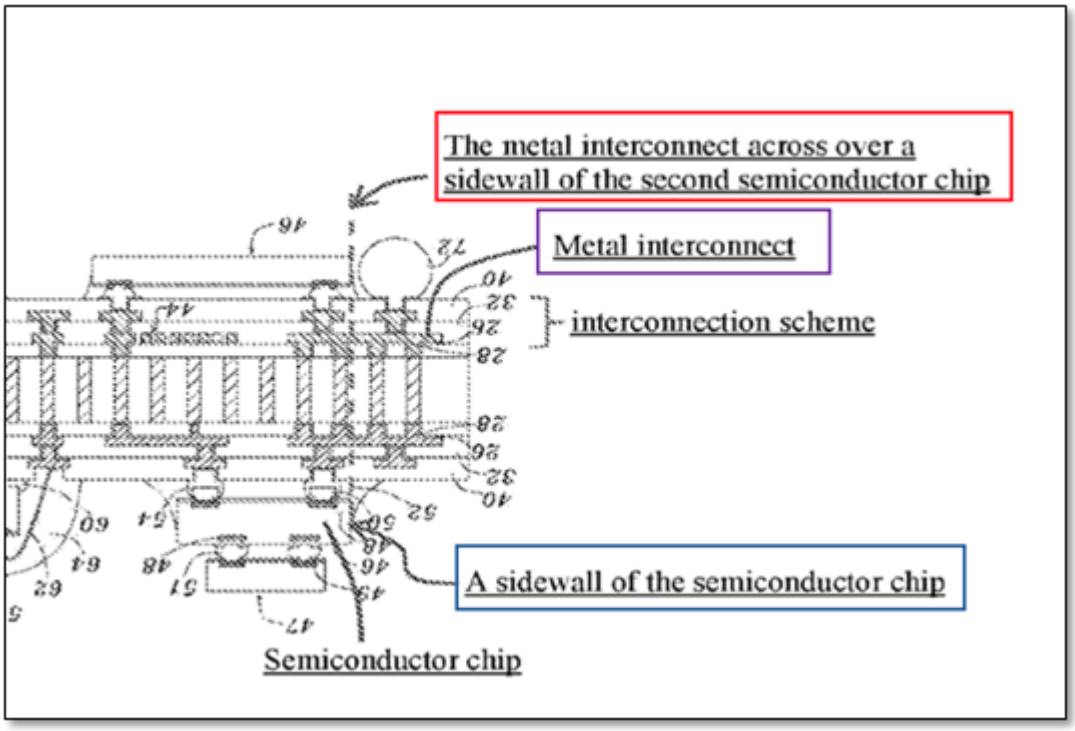


FIG. 16

EX1010 at FIG. 16.

501. I note that Yu's teachings of the *third metal interconnect* being *across* and *over* the *sidewall of the second semiconductor chip* are consistent with an annotated figure that Patent Owner provided during prosecution of the '768 Patent arguing support for this specification. In the figure below, I have shown how the

Patent Owner's annotations mirror the above mapping of Yu's *third metal interconnect*.



EX1002 at 537.

F. *Claim 24: "The chip package of claim 16, further comprising a third semiconductor chip under said first interconnection scheme, wherein said third semiconductor chip is a memory chip."*

502. As I discussed above, Yu's package 202 as depicted in FIG. 16 is part of FIG. 52's PoP structure (*chip package*). *See* ¶¶ 445-448. As shown, the PoP structure of FIG. 52 includes another package 202 that is positioned under FIG. 16's package 202. *EX1010* at FIG. 52. The second package 204 includes another "die 62, such as a **memory die**," i.e., *a third semiconductor chip* that is a *memory chip*. *EX1010* at 4:53-55, 8:35-39 ("FIG. 51 shows that multiple packages 202…can be

stacked in the PoP structure. In FIG. 52, connectors 210…[are] formed[.]"), 8:11-12. As shown, die 62 is positioned *under said first interconnection scheme*:

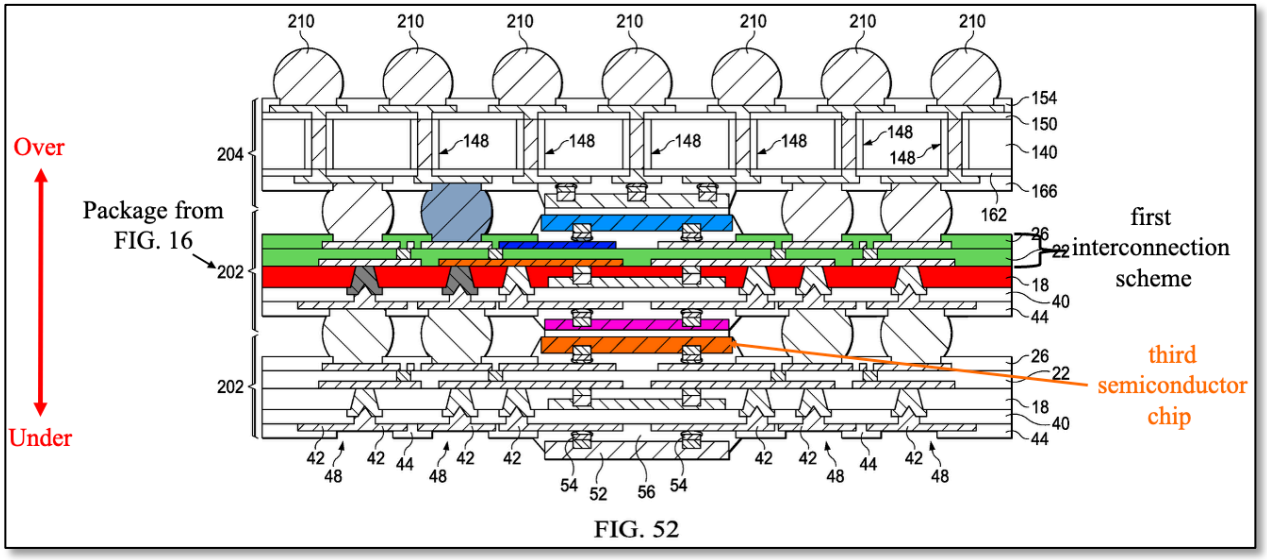


FIG. 52

EX1010 at FIG. 52.

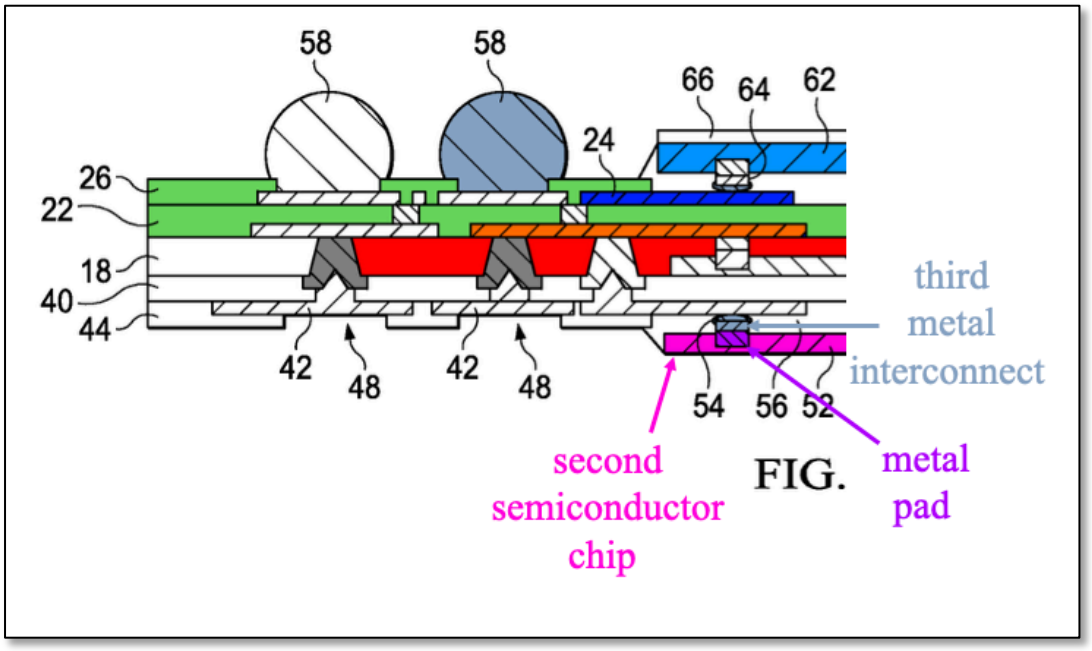
G. *Claim 25*

1. Claim 25(a): "The chip package of claim 16, wherein said second semiconductor chip comprises a third metal interconnect on a metal pad of said second semiconductor chip,"

503. Yu teaches that die 52 "is attached…to conductive features in the second back side metallization layer 42, such as by conductive connectors 54, like controlled collapse chip connection (C4) bumps." *EX1010* at 4:30–34. Connector 54 thus provides the conductive pathway that couples die 52 to metallization layer 42 and functions as *a third metal interconnect on a metal pad of said second semiconductor chip*.

504. Connector 54 is formed on the underside of die 52, establishing both mechanical and electrical contact to the back-side metallization. Yu's reference to "C4 bumps" reflects the standard flip-chip interconnect process in which solder bumps (metal interconnects) are deposited directly on metal bond pads of the semiconductor die. *See* ¶ 70. Accordingly, a POSITA would have understood that Yu's die 52 includes a metal bond pad underlying each C4 bump, since such pads are required for reliable solder attachment and electrical continuity in C4 packaging.

505. Thus, Yu teaches that die 52 comprises *a metal pad* and a connector 54 functioning as *a third metal interconnect on* that *metal pad*. *EX1010* at 4:30–34; FIG. 16.



EX1010 at FIG. 16 (excerpt).

506. A POSITA would have understood the rectangle portion in die 52 to be a *metal pad* of die 52 given that "I/O terminals were traditionally formed by way of metal pads along the periphery of an IC." *EX1095* at 1:24-25. As shown, the C4 bump/connector 54 (*third metal interconnect*) is *on* the *first metal pad*. *EX1010* at 4:30-34.

a) Lin-191's "Metal Pad Teachings and Motivation to Combine

507. In addition to Yu, Lin-191 teaches a semiconductor chip 160 with "metal traces or pads 163" that include "aluminum." *EX1005* at [0384]; *see* ¶¶ 183-185, incorporated herein. A POSITA would have been motivated and found it obvious to apply Lin-191's teachings of a *metal pad* to Yu's *pad*, thereby yielding the predictable result of Yu's *first semiconductor chip* (die 52) having a die *pad* that is *metal*. As I described above, Yu already teaches die 52 comprising connector 54, i.e., the claimed *pad*, and Lin-191 merely provides additional specificity that the pad is *metal*. Modifying Yu's pad to be metal, thereby yielding a *metal pad*, is merely an implementation detail in Yu's overall system, i.e., Lin-191 provides the specificity of a semiconductor contact pad being *metal*. Thus, for the same motivations described above, a POSITA would have been motivated to modify Yu's pad to be a *first metal pad*. *See* ¶¶ 184-185, incorporated herein.

508. The combination is the application of known technique (metal pads) to a known device (Yu's die 52) ready for improvement to the yield predictable result

of Yu's pad being *metal*. *EX1005* at [0081]. As I described above, metal contact pads were ubiquitous, so a POSITA would have had a reasonable expectation of success in modifying Yu's pad to be *metal*, such as aluminum, per Lin-191. *See* ¶¶ 184-185.

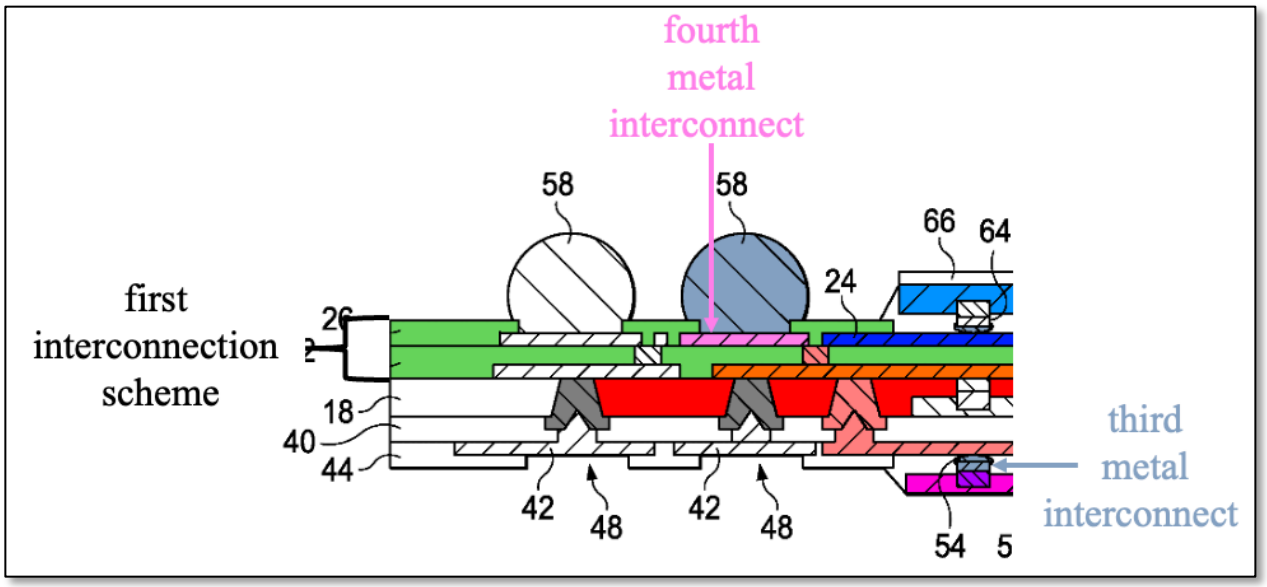
2. Claim 25(b): "wherein said third metal interconnect comprises a second metal layer on said metal pad and a fifth copper layer over said second metal layer, wherein said fifth copper layer has a thickness between 5 and 30 micrometers,"

509. *See* ¶¶ 186-194, incorporated herein. Lin-191 teaches or renders obvious interconnects/bumps with layers/thickness as recited in Claim 25(b). A POSITA would have found it obvious and been motivated to modify Yu's connector 54 for the reasons discussed with respect to Sundaram, i.e., improved metallurgical bonding and increased resistance to fatigue and stress-induced failure. *See* ¶¶ 188-194. Yu, like Lin-191's underfill 730, teaches an underfill material 56 such that the thickness of the *fifth copper layer* would advantageously provide ample space for Yu's underfill material 56 to be positioned. *EX1010* at 4:39-40; *see* ¶ 192. Layered bumps, per Lin-191, were routinely manufactured using techniques contemplated by Yu, leading to a reasonable expectation of success. For example, Lin-191 teaches using a "sputtering process[,]" "physical-vapor deposition (PVD) process," and electroplating, which are all techniques taught by Yu. *EX1005* at [0400], [0413]; *EX1010* at 3:5-8 ("A seed layer…is deposited…such as by sputtering or another physical vapor deposition process.), 3:11-14 ("Conductive material…is deposited…such as by…electroplating[.]"). Accordingly, the modification would

have merely required forming Yu's *third metal interconnect* per Lin-191's structure using techniques already taught by Yu, which would have given a POSITA a reasonable expectation of success.

3. Claim 25(c): "wherein said third metal interconnect is connected to said a fourth metal interconnect of said first interconnection scheme."

510. For the same reasons discussed above regarding the *second metal interconnect*, another portion of metallization layer 24 is a *fourth metal interconnect of said first interconnection scheme*. *See* ¶ 468. As shown, Yu's *third metal interconnect is connected to* the *fourth metal interconnect* by a a portion of metallization layer 42, a TMV 38, the *first metal interconnect,* and a *via*. *EX1010* at 4:7-11, 3:32-35.



EX1010 at FIG. 16 (excerpt).

H. *Claim 26: "The chip package of claim 16, wherein a height is between a backside surface of said first semiconductor chip and a top surface of said second polymer layer is smaller than a thickness of said first metal bump."*

511. Yu's die 62 (*first semiconductor chip*) has *a height* that *is between a backside surface* and a *top surface* of ILD 26 (*second polymer layer*) that *is smaller than a thickness of said first metal bump*, as shown:

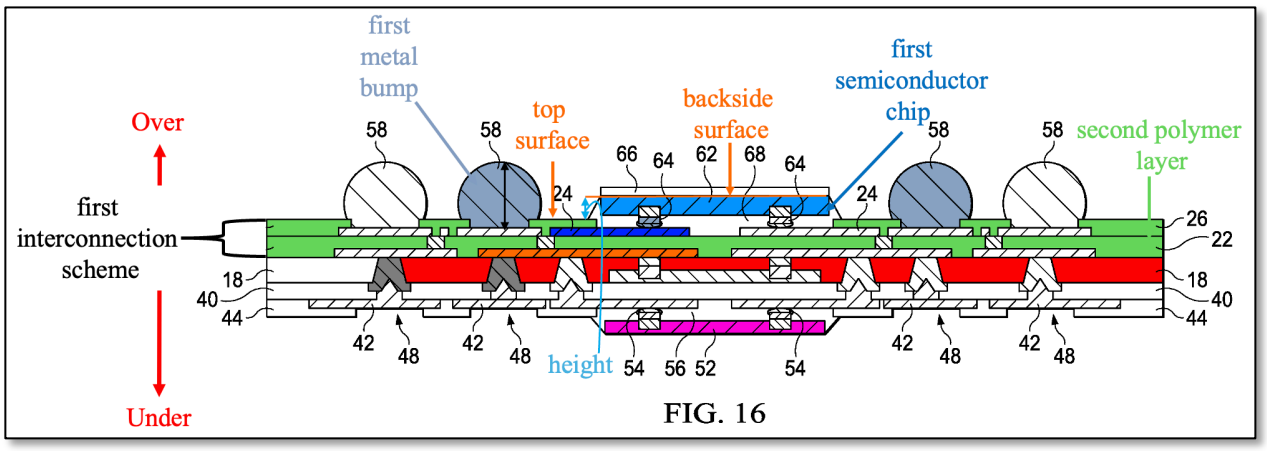
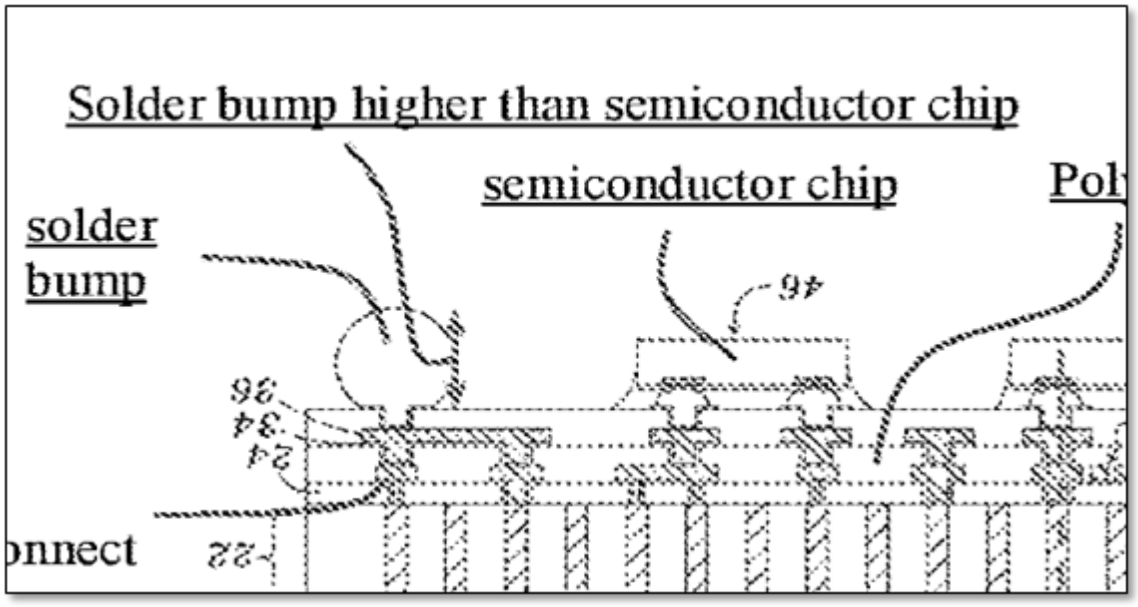


FIG. 16

EX1010 at FIG. 16 (excerpt).

512. Yu's teachings are consistent with the annotated figure provided by Patent Owner during prosecution arguing support for similar claim language.



EX1002 at 400.

I. *Claim 27: "The chip package of claim 16, wherein said second semiconductor chip is coupled to said first semiconductor chip through said first interconnection scheme."*

513. Die 52 (*second semiconductor chip*) is coupled to die 62 (*first semiconductor chip*) through *said first interconnection scheme*, as shown in FIG. 16. Yu expressly teaches that "die 52, such as a memory die, [is] attached to conductive features in the second back side metallization layer 42, such as by conductive connectors 54, like controlled collapse chip connection (C4) bumps". *EX1010* at 4:30-34. The conductive connectors 54 link die 52 to the underlying metallization features of layer 42, which forms part of the package's redistribution structure.

514. Yu further teaches the "back side ILD and RDL structure" includes "a first back side ILD layer 40, a second back side metallization layer 42, and a second ILD layer 44." *EX1010* at 4:7-10. This shows that layer 42 lies within the conductive

routing that continues through the molding compound 18 via the through-mold vias (TMVs 38) formed by depositing a copper seed layer and plating conductive material within "TMV openings 36 … formed through the molding compound 18." *EX1010* at 3:56-60.

515. On the opposite side, Yu describes that "connectors 64" are conductive connectors formed on the front side of the package and that each connector is coupled to conductive features in the second front side metallization layer 24. *EX1010* at 4:53-5:7. These connectors 64 in turn contact die 62, completing an electrical pathway from die 52 through connector 54, metallization layer 42, TMV 38, the first and second metal interconnects (layers 20 and 24), and finally through connector 64 to die 62.

516. Accordingly, Yu teaches that die 52 is coupled to die 62 through said *first interconnection scheme*.

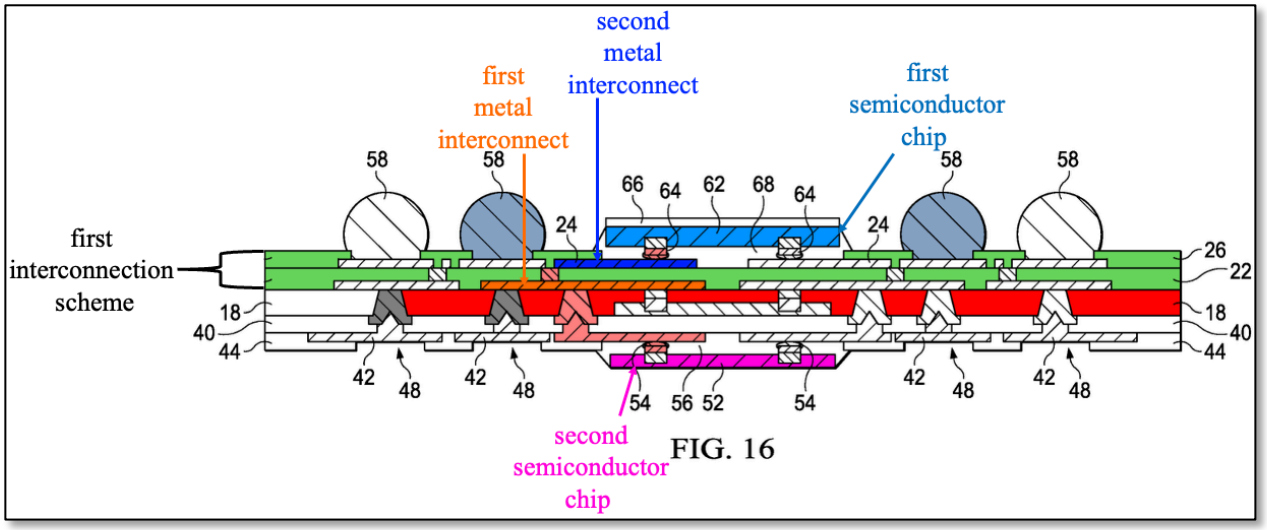


FIG. 16

EX1010 at FIG. 16.

J. *Claim 28: "The chip package of claim 16, wherein said first metal plug has a thickness between 100 and 300 micrometers."*

517. As shown below, Yu's *first metal plug* (TMV 38) extends from either side of the *first polymer layer*. Because the *first polymer layer*, per Claim 16(a)(ii), is *between 100 and 300 micrometers* thick, the *first metal plug* of Yu-Lin-191 has a thickness equal to that of the *first polymer layer,* thus teaching or rendering obvious the claimed *thickness between 100 and 300 micrometers*. *See* ¶¶ 452-457. As discussed, the '768 Patent does not ascribe any criticality to the claimed plug thickness of between 100 and 300 micrometers. *See* ¶ 258.

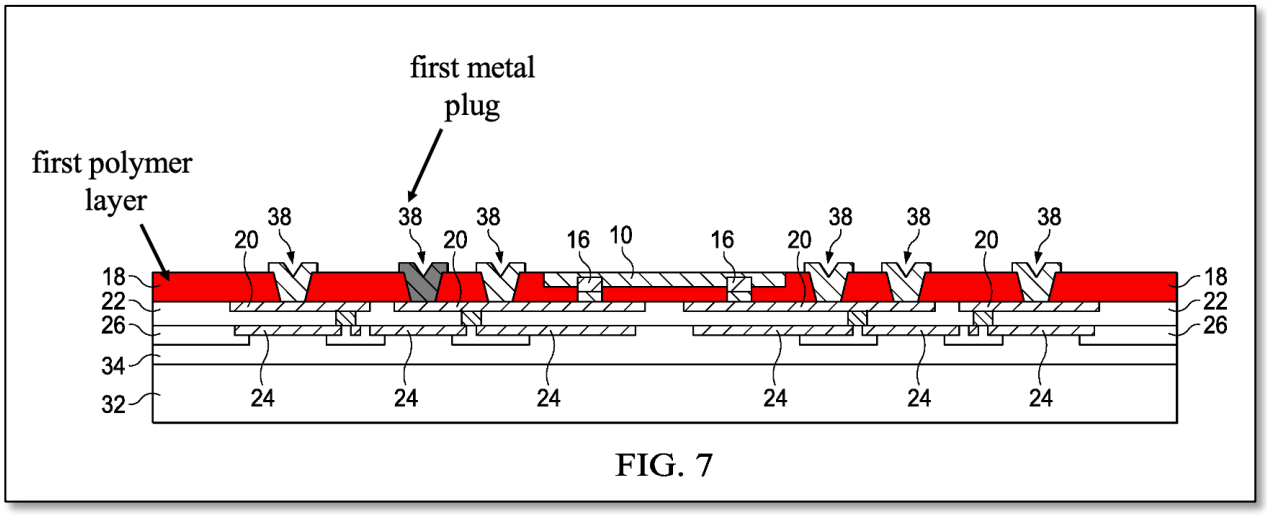


FIG. 7

EX1010 at FIG. 7.

XIII. OPINIONS REGARDING GROUND 3B: CLAIMS 18 AND 21 ARE OBVIOUS OVER YU, LIN-191, AND CAMACHO

A. *Claim 18:*

1. 18(a): "The chip package of claim 16, wherein said second semiconductor chip comprises a first metal pad on a top surface of said second semiconductor chip and a second metal pad on a bottom surface of said second semiconductor chip,"

518. As I discussed above, Yu alone or Yu-Lin-191 teaches that die 52 (*second semiconductor chip*) has a *first metal pad*. *See* ¶¶ 503-508. As shown, Yu's *first metal pad* is *on a top surface of said second semiconductor chip*:

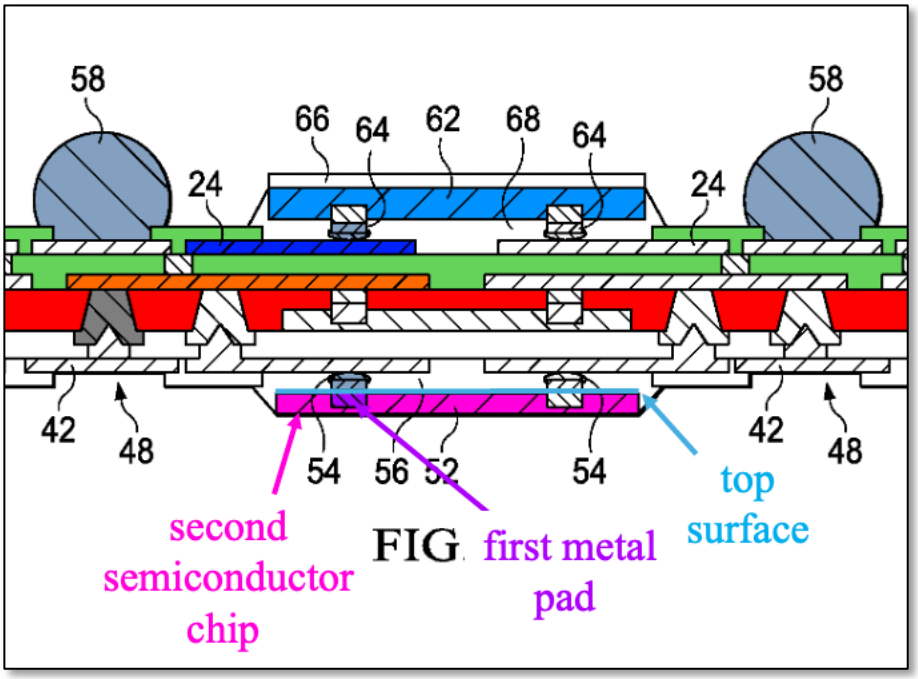
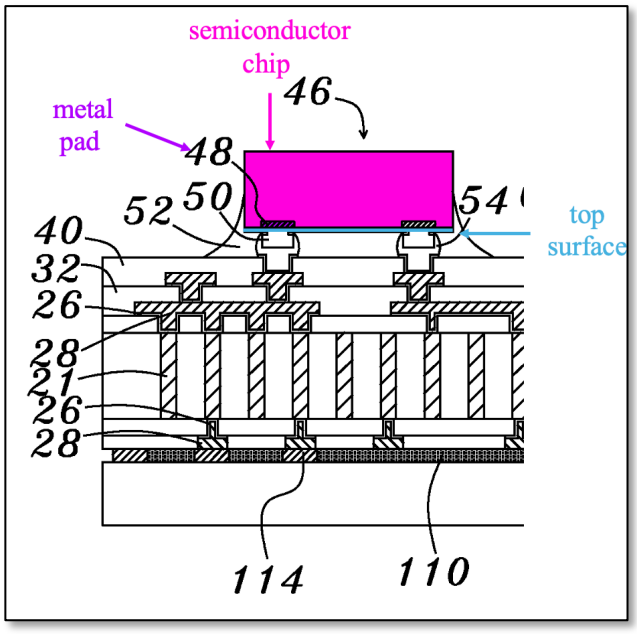


FIG.

EX1010 at FIG. 16 (excerpt).

519. Yu's teachings of a *metal pad* are consistent with the '768 Patent's description of chip 46 comprising metal pad 48. *EX1001* at FIG. 17a, 14:10-14. As shown, Yu's metal pad is similar to the '768 Patent's metal pad 48 on a top surface of chip 46:



EX1001 at FIG. 17a (excerpt).

a) Camacho's "Metal Pad" Teachings

520. Camacho teaches forming a "conductive TSV through a WLSCP [wafer level chip scale package]" semiconductor die. *EX1006* at [0039], [0008], [0010]. An electrically conductive layer 130 is formed over the top active surface of semiconductor die 122[,]" to form "individual portions or sections 130a-130b." *EX1006* at [0041]. Similarly, "an electrically conductive layer 132 is formed over the bottom surface of semiconductor die 122[,]" yielding individual sections 132a-132b. *EX1006* at [0041]. "Conductive layers 130 and 132 can be one or more layers of Al, Cu, Sn, Ni, Au, Ag, or other suitable electrically conductive material" (i.e., *metal*). *EX1006* at [0041]. Because layers 130, 132 are formed "over" their respective surfaces, layers 130, 132 are formed *on* those surfaces, as depicted below

where layers 130, 132 are on either surface of die 122. *EX1006* at [0041]. As such, Camacho teaches a *metal pad on* both the *top* and *bottom* surfaces of semiconductor die 122 (a *semiconductor chip*), thereby yielding *a first metal pad on a top surface of* a chip *and a second metal pad on a bottom surface of* the chip:

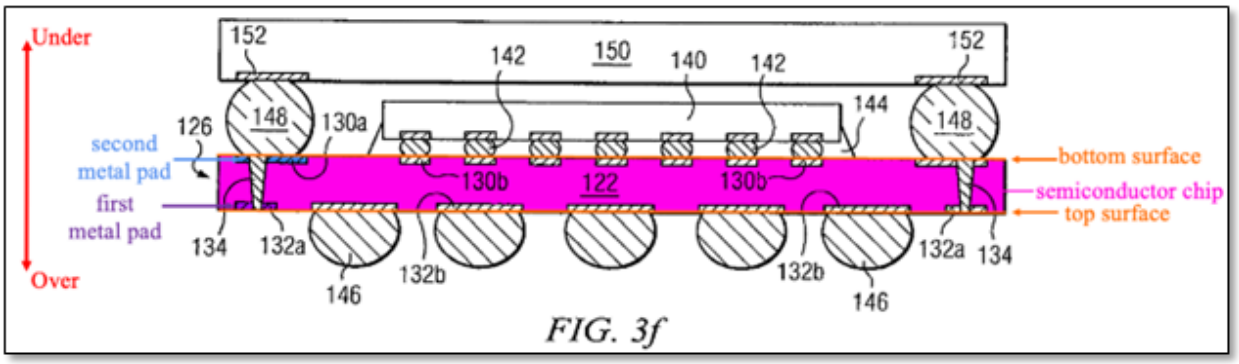


FIG. 3f

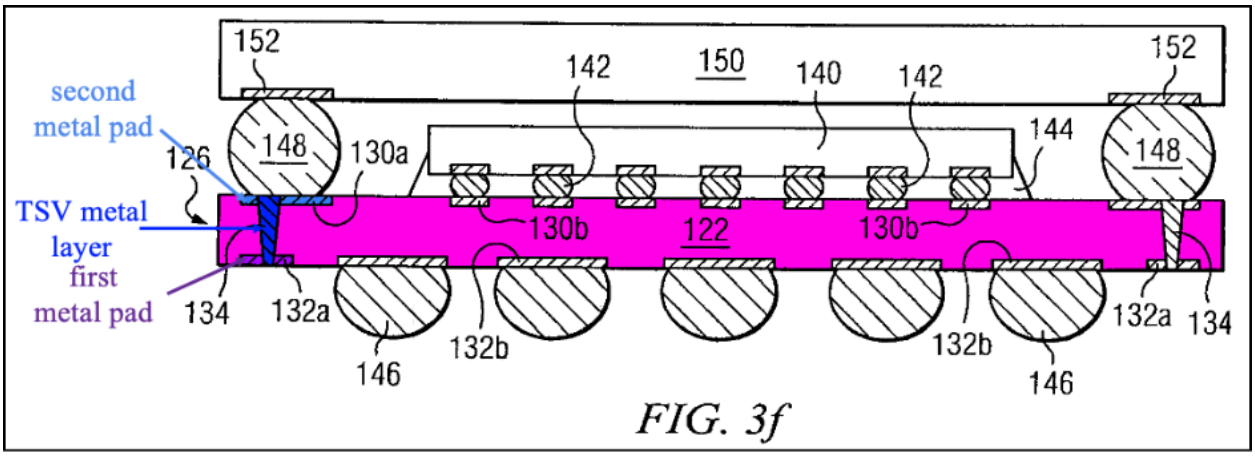
EX1006 at FIG. 3f. MTCs and reasonable expectation of success for combining Yu-Camacho are below. *See* ¶¶ 523-525.

2. 18(b): "wherein said first metal pad is connected to said second metal pad through a through-silicon-via metal layer."

a) Camacho's Teachings

521. Camacho teaches that "a plurality of vias is formed through semiconductor wafer 120" and that those vias "are filled with a conductive material to form conductive TSV 134." *EX1006* at [0043], [0047]. Camacho further explains that "conductive layers 130 and 132 are electrically connected by TSV 134", thereby providing a continuous electrical path vertically through the semiconductor die from the *first metal pad* to the *second metal pad*. *Id* at [0043].

522. Accordingly, Camacho teaches that the *first metal pad* (conductive layer 132a) is *connected to the second metal pad* (conductive layer 130a) through a *through-silicon-via metal layer* (TSV 134):



EX1006 at FIG. 3f.

3. Claim 18 MTC

523. A POSITA would have found it obvious and been motivated to configure Yu's die 52 with a through-silicon-via (TSV) metal layer connecting upper and lower metal pads and to apply Camacho's explicit teachings of conductive pads on both surfaces of a die. Camacho teaches forming "a plurality of vias … through semiconductor wafer 120," which "are filled with a conductive material to form conductive TSV 134," and that "conductive layers 130 and 132 are electrically connected by TSV 134." *EX1006* at [0043], [0047]. These teachings provide a model for inter-die communication through the silicon body itself, rather than solely through peripheral bump connections.

524. In Yu, die 52 is already interconnected vertically within a package structure by being "attached … to conductive features in the second back-side metallization layer 42 … by conductive connectors 54, like C4 bumps" and connected above to another die 62 through metallization and connectors. *EX1010* at 4:30-34. A POSITA would have recognized that integrating Camacho's TSV-based through-die interconnects into Yu's existing stacked-die configuration would further reduce interconnect length and latency while improving electrical performance. Indeed, it was known that by "using TSV technology, 3D ICs can pack a great deal of functionality into a small 'footprint.' Thus, critical electrical paths through the device can be drastically shortened, leading to faster operation." *EX1067* at [0005]. Because TSVs were known for allowing such high-density 3D integration, with low-latency communication (i.e., by shortening electrical paths) between additional chips while preserving package size, the modification would give Yu's die 52 to ability to efficiently communicate through shorter interconnects with another stacked chip, which would provide increased functionality to Yu's chip package.

525. The modification is therefore the application of a known technique (configuring a semiconductor die with a TSV connecting metal pads on opposite surfaces) to a known device (Yu's die 52) ready for improvement to yield the predictable result of a TSV-enabled die capable of efficient communication through shorter interconnects. Modifying Yu's package to stack chips would have been

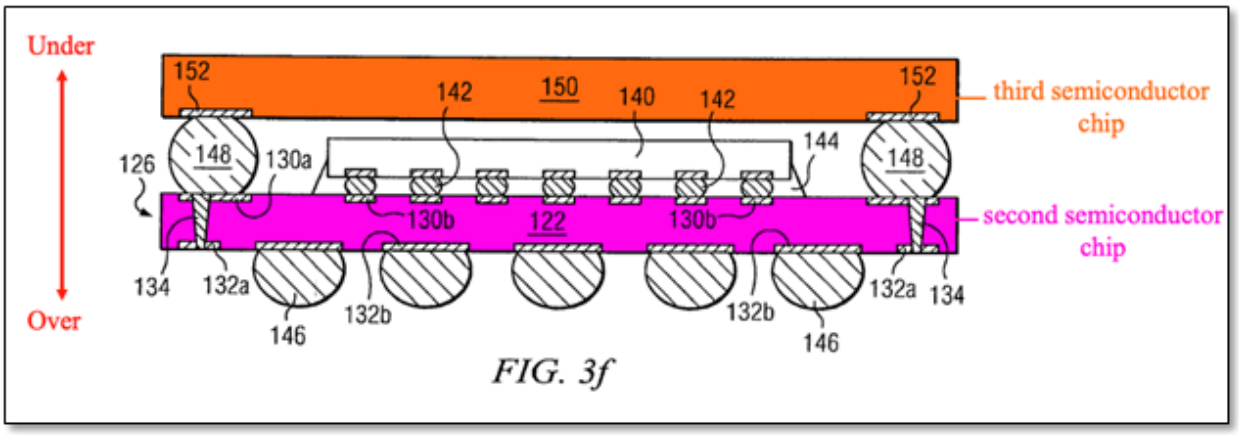
advantageous in increasing package density to increase processing speed or storage capacity and in shortening interconnects between chips in the package. A POSITA would have had a reasonable expectation of success in modifying Yu–Lin-191 per Camacho because Camacho discloses well-established and industry-standard TSV fabrication methods, including forming the vias through the wafer and filling them with conductive materials such as copper or tungsten. *EX1006* at [0043]-[0047]. For example, Camacho teaches well known methods of forming the TSV metal layer, such as "laser drilling," which is a techniques a POSITA would have been familiar with. *EX1006* at [0043]; *EX1128* at 5:32-34 ("…method known to one of ordinary skill in the art, such as by laser drilling[.]"). Moreover, the metal portion of TSV metal layer 134 is formed by "PVD, CVD, electrolytic plating" which are techniques already taught by Yu, further leading to reasonable expectation of success. *EX1010* at 3:5-8 ("A seed layer…is deposited…such as by sputtering or another **physical vapor deposition** process.), 3:11-14 ("Conductive material…is deposited…such as by…electroplating[.]").

B. *Claim 21*

1. Claim 21(a): "The chip package of claim 16, further comprising a third semiconductor chip under said second semiconductor chip and"

526. As shown below, another chip in Camacho's package, die 150 is a *third semiconductor chip*. As such, Camacho teaches a *third semiconductor chip under*

said second semiconductor chip. Camacho explains that die 122 is electrically coupled to the underlying semiconductor package 150 through the lower conductive layer and corresponding solder interconnects, forming a multi-chip or package-on-package (PoP) assembly. *EX1006* at [0045]–[0047], FIG. 3f. Accordingly, Camacho expressly teaches a structure in which the lower semiconductor element (die 150) is disposed *under* another semiconductor die (die 122), and both are electrically interconnected through the conductive structures extending through die 122.



EX1006 at *FIG. 3f.*

2. *Claim 21(b): "multiple fourth metal bumps between said second and third semiconductor chips,"*

527. Camacho's die 150 (*third semiconductor chip*) includes "contact pads 152…electrically connected to bumps 148, conductive layer 130a, TSVs 134, and conductive layer 132a." *EX1006* at [0047]. Bumps 148 are *metal bumps* because "the bump material can be Al, Sn, Ni, Au, Ag, Pb, Bi, Cu, and solder[.]" *EX1006* at

[0046]. Camacho thus teaches *multiple fourth metal bumps* between *semiconductor chips*.

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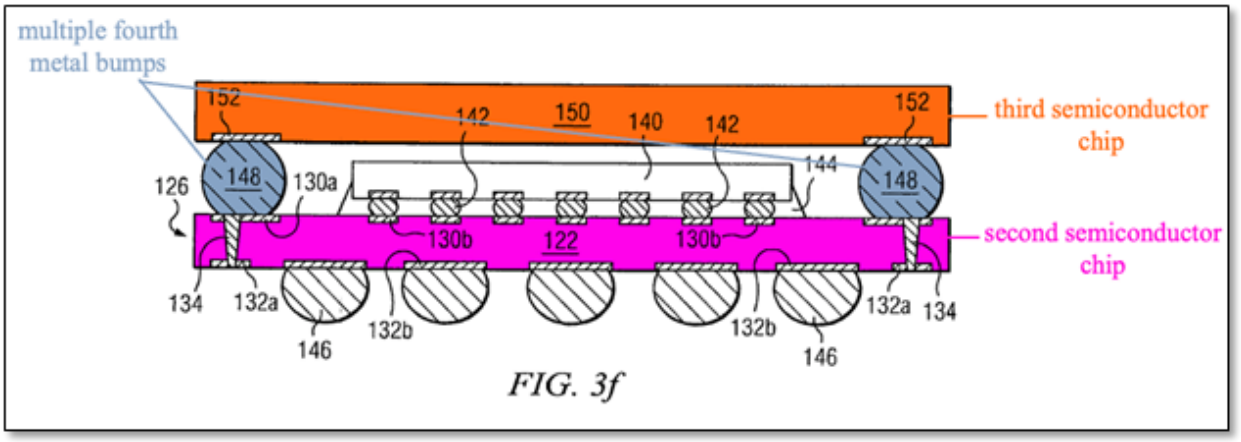


FIG. 3f

EX1006 at FIG. 3f.

3. Claim 21(c): "wherein said second semiconductor chip comprises a first metal pad on a top surface of said second semiconductor chip and a second metal pad on a bottom surface of said second semiconductor chip,"

528. *See* Claim 18(a), ¶¶ 518-520, incorporated herein. Claim 21(c) recites the same limitation as Claim 18(a).

4. Claim 21(d): "wherein said first metal pad is connected to said second metal pad through a through-silicon-via metal layer."

529. *See* Claim 18(b), ¶ 521, incorporated herein. Claim 21(d) recites the same limitation as Claim 18(b).

5. Claim 21 MTC

530. A POSITA would have found it obvious and been motivated to modify Yu's die 52 such that a *first* and *second metal pad* were connected via TSV 134 for the same reasons described at Claim 18. *See* ¶¶ 523-525, incorporated herein.

531. A POSITA would have been further motivated to include Camacho's semiconductor die 150 *under* Yu's modified die 52 by connecting a contact pad (e.g., contact pad 152) in semiconductor die 150 to *multiple fourth metal bumps* positioned on the *first metal pad* of die 52. Thus, in the combination, Yu's die 52 is modified such that the *first metal pad* and *second metal pad* are connected by a TSV (*through-silicon-via metal layer*) therebetween. *Multiple fourth metal bumps* (bumps 148) would be positioned on conductive layers 130a (*second metal pad*), as shown in Camacho, such that die 150 (*third semiconductor chip*) is connected to the *second semiconductor chip* (Yu's die 52). Thus, the arrangement of the combination mirrors Camacho's structure, where semiconductor die 150 is placed under die 122, and connected to conductive layers 130a by bumps 148. *EX1006* at FIG. 3f.

532. A POSITA would have found it obvious and been motivated to include Camacho's *third semiconductor chip* under Yu's *second semiconductor chip*. Yu is already familiar with including a plurality of chips in the package, as illustrated by FIG. 52's PoP structure. *EX1010* at FIG. 52. A POSITA would have appreciated that Camacho's teachings would enable the additional chip to be added to Yu's package without having to add an entire additional package 202. The ability to add just one

additional chip (e.g., Camacho's *third semiconductor chip*) to Yu's package would have been desirable for applications merely requiring just one more chip and avoided a drastic increase in package size (i.e., because one chip would require less space than another package 202). Indeed, stacking chips in a chip package was known to be advantageous because package functionality would be increased "without increasing the footprint, or the area occupied on a circuit board, of the integrated circuit package." *EX1096* at 1:28-31.

533. A POSITA would have further been motivated and found it obvious to include *multiple fourth metal bumps* between the *second* and *third semiconductor chip* such that pads on either chip were electrically connected, as Camacho's bumps 148 "provide vertical, z-direction interconnect" between each die. *EX1006* at [0048]. A POSITA would have appreciated that using solder bumps 148 to connect adjacent chips would have provided the benefit of self-alignment during reflow, thereby reducing the risk of misalignment between the metal pads of the chips. *See* ¶ 245.

534. This modification represents the application of a known 3D-stacking technique to a known interconnect architecture to achieve the predictable result of a chip package comprising multiple vertically stacked semiconductor chips. The modification would have been straightforward and would merely require forming TSVs connecting metal pads and additional solder bumps between the chips using well-known processes taught by Camacho. Camacho teaches forming metal pads

using "PVD, CVD, sputtering, electrolytic plating, [or] electroless plating" and forming TSV metal layers by similar methods. *EX1006* at [0041], [0043]. Further, bumps 148 are formed using "evaporation, electrolytic plating, electroless process, ball drop, or screen printing process" with materials such as "eutectic Sn/Pb, high-lead solder, or lead-free solder." *EX1006* at [0046]. The bump material "is bonded to conductive layer 130a and reflowed by heating the material above its melting point to form spherical balls or bumps 148." *EX1006* at [0046]. Accordingly, a POSITA would have had the requisite skill and would have reasonably expected success in performing this modification without undue experimentation as it would have been simple and straightforward.

XIV. OPINIONS REGARDING GROUND 3C: CLAIM 20 IS OBVIOUS OVER YU, LIN-191, AND HABA

A. *Claim 20: "The chip package of claim 16, wherein said first polymer layer has a coefficient of expansion between 3 and 10 ppm/°C."*

a) Haba's Teachings and Motivation to Combine

535. *See* ¶¶ 135-136 for Haba's Teachings. The same MTCs and reasonable expectation of success for Sundaram-Haba apply for Yu-Haba. *See* ¶¶ 137-143, incorporated herein. The modification would reduce CTE mismatch between Yu's molding compound 18 and chips, which was a known benefit when encapsulating chips. *See* ¶¶ 137. The combination is the application of a known technique (a

polymer interposer with a CTE of 8 ppm/°C) to a known device (Yu's polymer molding compound 18) ready for improvement to yield predictable results.

XV. CONCLUSION

I declare that all statements made herein of my knowledge are true, and that all statements made on information and belief are believed to be true, and that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Date: November 21, 2025 By: 

Dr. Stanley R. Shanfield

Stanley Shanfield



Curriculum Vitae for Stanley Shanfield

Education:

Massachusetts Institute of Technology, Ph.D., Physics, 1981

University of California, Irvine, B.S. Cum Laude, Physics, 1977

Educational Awards:

Outstanding Research Project, U.C. Regents Award, 1977

Phi Beta Kappa, 1977

Four Year Scholarship, Tuition & Research, ERDA/DOE, 1977-1981

Hands-On Professional Expertise:

Semiconductor Physics & Chemistry
Semiconductor Fabrication: Silicon and III-V Materials
Semiconductor Device & Integrated Circuit Engineering
Semiconductor Equipment: Front & Back End
Semiconductor Packaging Design and Manufacturing
Passive Component Design and Manufacturing
RF Design and Fabrication
Digital Design & Fabrication
Semiconductor Manufacturing in Silicon and III-V Materials
MEMS Design and Fabrication: Electrical, Optical, & Sensing Devices
Fiber Optic Device Design and Fabrication
Integrated Optics & Electro-Optical Devices
Plasma Physics

Specialized Training:

Global Positioning Electronics, Systems and Components
Six Sigma Semiconductor Manufacturing
Microwave Engineering
US Patent Law in Technology
Patent Application and Prosecution
Semiconductor Plasma Processing
Thin Film Physics and Technology
MEMS-based Gyroscopes and Accelerometers
Thermoelectric Materials & Technology
Phased Array Radar Engineering
Antennas and Electromagnetic Propagation
Solid State Optical Devices
Fiber Optic Communication System Operation
HALT and HAST Reliability Testing Methods

Professional Experience:

Draper Laboratory Cambridge, MA ***2003 – present***

Division Leader, Advanced Hardware Development
Distinguished Member of Technical Staff
Technical Director

Led division (about 80 staff) in re-invigorating multi-chip integrated circuit module facility, more than doubling associated revenues in two years. By most accounts, made division a viable business & technological entity again. Invented & led implementation of an ultra-miniature electronics fabrication technology which became a top laboratory priority. Led team in realization & fabrication of a newly designed precision MEMS-based gyroscope and associated ASIC. Found funding and led team in developing a miniature power source with energy density at least two orders of magnitude higher than any source previously built. Developed fabrication technology for semiconductor-based low phase noise oscillator design, allowing for receiver operation with extremely low signal strength. Many awards received, most recently, the Draper 2010 Distinguished Performance Award, and 2010 Best Patent Award.

Clarendon Photonics Newton, MA ***2001 – 2003***

Director, Packaging & Integration

30 person photonic chip startup with $18 million 2nd round funding. Invented and productized new, low cost and reliable semiconductor processing, packaging and pig-tailing technology for optical add-drop multiplexer. Established assembly and packaging process, and developed control electronics. Partner with Micron Technologies, using their R&D semiconductor facility.

AXSUN Technologies Bedford/Billerica, MA ***1999 – 2001***

Vice President, Operations
1999 – 2000

Initially three staff members with $6 million funding. Designed, fabricated and productized AXSUN's micro-electromechanical (MEM) Fabry-Perot optical filter. Patents granted on semiconductor processing and control electronics. Completed facility and semiconductor processing design, then completely equipped. Raised 2nd round funding for $36 million. Established process and fabrication facility in Belfast, Northern Ireland for producing thick oxide silicon-on-insulator material.

Director, Manufacturing & Wafer Fab Technology **2000 – 2001**

After 3rd round funding, led device manufacturing, creating wafer fab and assembly infrastructure; hired 70+ people, led production. Delivered first generation product for revenue to multiple customers. Converted pure technology to dominant company revenue with high yield.

Company purchased by Volcano Technologies, San Diego.

Raytheon Corporation Lexington/Andover, MA ***1985 - 1999***

Manager, Semiconductor Operations **1996 – 1999**

Built and led a 300 employee, $60 million revenue 24/7 semiconductor development and manufacturing operation resulting from the consolidation of a number of smaller organizations. Key player in technological development and recipient of Raytheon's 6 Sigma Leadership training. Decision maker in Texas Instrument group acquisition, providing significant expert opinion on semiconductor and design facilities. Obtained state-of-art yields using best available steppers, deep reactive ion etching, plasma assisted CVD, and ion-implantation equipment, and disciplined design-for steppers, deep reactive ion etching, plasma assisted CVD, and ion-implantation equipment, and disciplined design-for-manufacturing
circuit design and layout methodology.

Research Laboratory Manager **1992 – 1996**

Leader of a 90 employee development and contract research organization in high performance semiconductor devices and circuits, measurement, assembly and wafer fab. Led a team which invented and implemented a major revenue generating technology (.$100 million) based on semiconductor device development (pseudomorphic high electron mobility transistor). Increased outside research funding by 50% in 3 years through superior technical performance relative
to competitors.

Section Manager, Semiconductors & ICs **1985 – 1992**

Led a MM-Wave Circuit and Module Development program over 2 years, leading to production win of a satellite terminal electronics generating $320 million in sales. Developed processes for fabricating high power, high frequency multi-function integrated circuits, and combining high performance digital and analog devices in a single integrated circuit.

Spire Corporation Bedford, MA ***1981 – 1984***

Staff Scientist
Senior Staff Scientist

Developed new methods for low temperature deposition of plasma-assisted CVD epitaxial silicon. Wrote joint papers with MIT professor, and had process adopted by equipment manufacturers. Built, operated and characterized ion-assisted deposition system for making coating for semiconductor and machine tool industries. Process eventually purchased by Kennametal, Inc.

Publications

Restricted Publications & Reports

Process Sequence for Formation of Ultra-High Density Multi-Chip Modules:
A high yield, low cost method for creating a system-in-a-package consisting of numerous semiconductor die, passive components, and sensors. Process formed basis for new (2008) facility.

Design and Method of Fabrication of Ultra-High Density Radioisotope Power Source:
In test, a miniature power source that achieves energy density more than 1000X the best chemical battery. Method uses planar semiconductor processing of bulk thermoelectric materials.

Design and Method of Achieving Extremely Low Crystal Oscillator Phase Noise:
Method developed for very low power refrigeration of quartz or sapphire crystal resonators, resulting in extremely low phase noise oscillators. The low phase noise allows extremely high sensitivity in digital receivers, including GPS receivers, leading to use in extremely low signal conditions.

Design, Evaluation & Production of MEMS-based Fabry-Perot Interferometer:
Design and method for ultra-compact spectral analyzer made using semiconductor and optical thin film processing.

Design & Evaluation of Ultra-Fast Control Electronics for Integrated Optical Multiplexer:
Design and performance evaluation of silicon-based integrated optical multiplexer using chip-based local heating

Design and Fabrication of Q-band MILSTAR Communications Terminal Transmitter:
Record power and efficiency 44 GHz transmitter design using new transistor design, and combined waveguide

Key Publications (selected)

Process Characterization of PSG and BPSG Plasma Deposition, J. Electrochem. Soc., Volume 131, Issue 9, pp. 2202-2203

A double-recessed Al0.24GaAs/In0.16GaAs pseudomorphic HEMT for Ka- and Q-band power Applications, Electron Device Letters, IEEE, Volume 14, Issue 9, pp. 456 - 458

Formation of Thick Metal Structures on GaAs MMICs Using Image Reversal Lithography and Evaporated Metal Deposition, J. Electrochem. Soc., Volume 136, Issue 9, pp. 2687-2690

Contact Hole Etching in Load-Locked Hexagonal Reactive Ion Etch System, J. Electrochem. Soc., Vol. 131, No. 8, 1984

An AlGaAs/InGaAs pseudomorphic high electron mobility transistor with Improved Breakdown Voltage for X and Ku-band power applications, Microwave Theory and Techniques, IEEE Transactions on, Volume 41, Issue 5, May 1993, pp. 752 - 759

Hot-electron-induced Degradation of Metal-Semiconductor Field-Effect Transistors, Integrated Circuit Symposium, 1994. Technical Digest 1994., 16th Annual Volume , Issue , 16-19 Oct. 1994, pp. 259

Ion Beam Deposition of Cubic Boron Nitride, J. Vac. Sci. Technol. A Volume 1, Issue 2, pp. 323-325

Patents

US Patent 6504235 - **Passivation layer and process for semiconductor devices**
Method of coating semiconductor devices that prevented parametric shift in electrical performance. Solved key processing problem.

US Patent 4440108 - **Ion Beam Deposition Apparatus**
Design of equipment for deposition of thin films in the presence of ion bombardment. System produced thin films of interest for mechanical, electrical and optical properties and was sold as an equipment product.

US Patent 6525880 - **Integrated Tunable Fabry-Perot filter and Method of Making Same**

Design and method for fabricating very small, very high performance variable optical filter using semiconductor fabrication technology. In current use in fiber optical networks, chemical sensors, and 3-D medical imaging applications.

US Patent 5175020 - **Boron Nitride Films and Process of Making Same**
Ion assisted deposition of ultra-hard cubic boron nitride films for semiconductor and machine tool applications. Significant use in both areas.

US Patent 4526673 - **Coating Method**
Method for deposition of thin films used in semiconductor device fabrication. Method based on direct control of the kinetics of thin film deposition.

US Patent 7727806 - **Systems and Methods for High Density Multi-Component Modules**
Method for fabrication of electronic modules using multiple thinned integrated circuits, patterned multi-level interconnects, passive electronic components, and sensors

US Patent Application 2009/TBD - **Devices, systems, and methods for controlling the temperature of resonant elements**
Devices and systems for achieving low phase noise crystal oscillators using unique low power thermoelectric structures

Expert Witness Experience:

See attachment

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Email: shanfield@alum.mit.edu