UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY LTD.,

and

APPLE INC.,

Petitioners

v.

MYW SEMITECH, LLC,

Patent Owner

Inter Partes Review Case No. IPR2026-00065
U.S. Patent No. 11,107,768

PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 11,107,768

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I. INTRODUCTION

IPR is requested of Claims 1-28 of USPN 11,107,768. The '768 Patent claims a chip package comprising various well-known components of semiconductor and chip packaging designs. Neither the claimed components nor the claimed configuration of the components is new or non-obvious.

II. LEVEL OF SKILL OF A PERSON HAVING ORDINARY SKILL IN THE ART

A POSITA at the time of the '768 Patent would have had at least a bachelor's degree in electrical engineering, materials science, or physics (or an equivalent degree), and at least two years of experience in semiconductor design or semiconductor manufacturing. A master's degree or Ph.D. in a relevant field may substitute for some work experience or vice versa. Additional education or experience might substitute for the above requirements.

III. REQUIREMENTS UNDER 37 C.F.R. § 42.104

A. Grounds for Standing Under 37 C.F.R. § 42.104(a)

Petitioners certify the '768 Patent is eligible for IPR.

B. Identification of Challenge Under 37 C.F.R. § 42.104(b)

Petitioners request the Challenged Claims be found unpatentable on the following grounds[1]:

[1] All references qualify as prior art under at least one of pre-AIA §§ 102(a)-(b), (e).

Grounds	Claims Challenged	35 U.S.C. §	References
1A	1-15, 20	103	Sundaram (EX1004), Haba, (EX1009), and Lin-191 (EX1005)
1B	16-19, 21-28	103	Sundaram and Lin-191
2A	1-3, 5, 7-10, 14-15	103	Haba and Lin-191
2B	4, 6, 11-13,	103	Haba, Lin-191, and Sundaram
3A	16-17, 19, 22-28	103	Yu (EX1010) and Lin-191
3B	18, 21	103	Yu, Lin-191, and Camacho (EX1006)
3C	20	103	Yu, Lin-191, and Haba

C. Claim Construction Under 37 C.F.R. § 42.104(b)(3)

For this IPR only, claim construction is unnecessary because, as set forth herein, the prior art falls within the indisputable scope of the Challenged Claims under any reasonable construction (including any proposed in litigation).

IV. SHOWING OF ANALOGOUS, PRIOR ART

The prior art is analogous to the claimed invention of the ’768 Patent. The prior art is from the same field of endeavor of the ’768 Patent, namely semiconductor packaging. *EX1001*, 1:24-67, 3:32-35, 14:10-11; *EX1004*, 1:33-42, 5:16-19, 7:61-67; *EX1005*, [0003], [0007]; *EX1006*, [0001], [0008]-[0009]; *EX1009*, 1:18-28, 8:18-40; *EX1010*, Abstract, 1:10-55, 1:63-67, 4:17-20; *EX1003*, ¶¶31-33, 93, 102, 111, 118, 125.

The prior art is also reasonably pertinent to at least one purported problem identified in the '768 Patent, namely:

(A) Minimizing temperature coefficient of expansion mismatching; *EX1001*, 1:58-64; *EX1004*, 5:62-63; *EX1009*, 1:53-55, 3:36-38, 5:55–6:5, 6:6-18; *EX1010*, 6:20-26;

(B) Creating chip packages with pre-testability capability; *EX1001*, 1:58-64; *EX1004*, 7:41-43, 2:34-35; *EX1005*, [0006], [0105], [0173], [0239], [0401], [0462], [0492-0493]; *EX1010*, 2:17-20;

(C) The impact of miniaturization on circuit performance; *EX1001*, 1:31-35; *EX1004*, 1:15-32, 2:21–3:6; *EX1006*, [0028]; and/or

(D) Parasitic capacitance of interconnections in a chip package; *EX1001*, 1:32-37; *EX1006*, [0038]; *EX1003*, ¶¶34-38, 94, 103, 112, 119, 126-127.

V. GROUND 1A: CLAIMS 1-15 AND 20 ARE OBVIOUS OVER SUNDARAM, HABA, AND LIN-191

A. Claim 1

1. 1(Pre)

Sundaram teaches a *chip package*[2] formed by an "interconnect structure [] compris[ing] an interposer 105" that interconnects a "first electronic device 125"

[2] Claim language provided in italics. All drawing annotations added. Citations to a claim limitation and/or section number are to the limitations mapping in this Petition

and a "second electronic device 130." *EX1004*, 5:45-58, 6:34-46 (devices 125, 130 are chips), FIG. 33. The interconnect structure "enables the interposer 105 and the **package** can [*sic*] be one and the same." *EX1004*, 7:61-63.

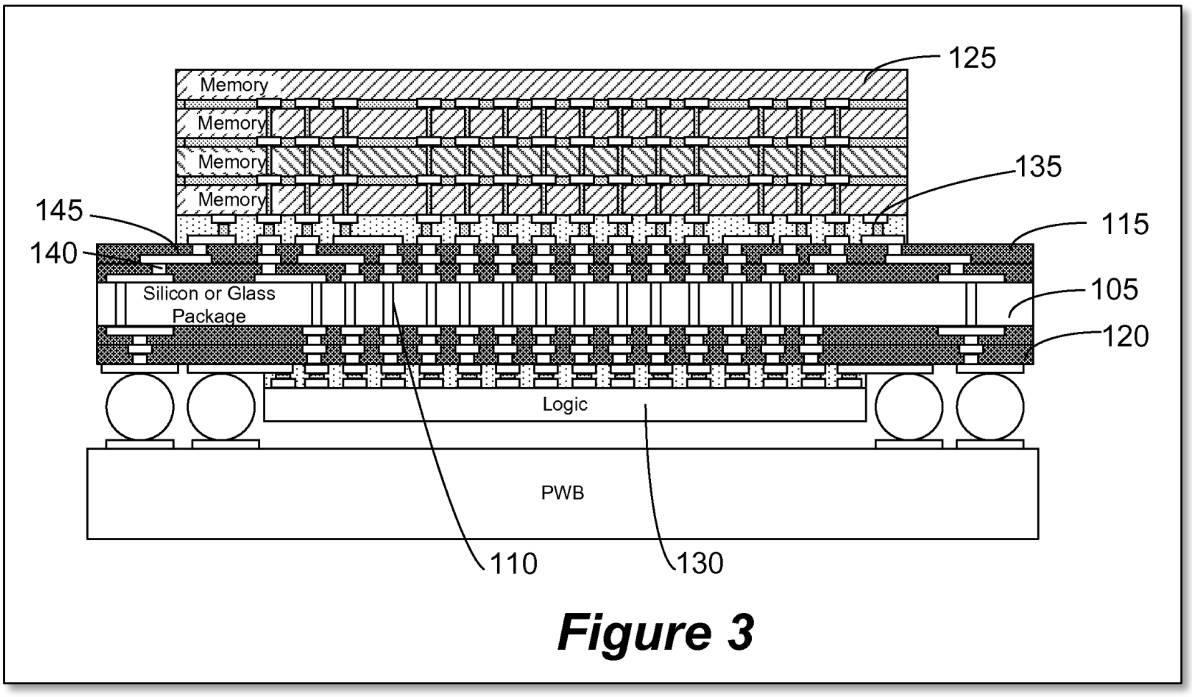


Figure 3

EX1004, FIG. 3; *EX1003*, ¶129.

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and are incorporated by reference, including the motivations to combine (MTC) and showing of reasonable expectation of success (REOS) provided in the cross-referenced section. All REOS include the benefits described for the respective MTC. All emphases added unless otherwise noted.

2. 1(a)

Sundaram's interconnect structure "comprises an interposer having a first side and a second side" (*a first surface and a second surface*) and is "made of…flexible **polymers**" such that interposer 105 is a *first polymer layer*. *EX1004*, 2:22-27, 5:54-58. Sundaram's *second surface* is *opposite to said first surface*:

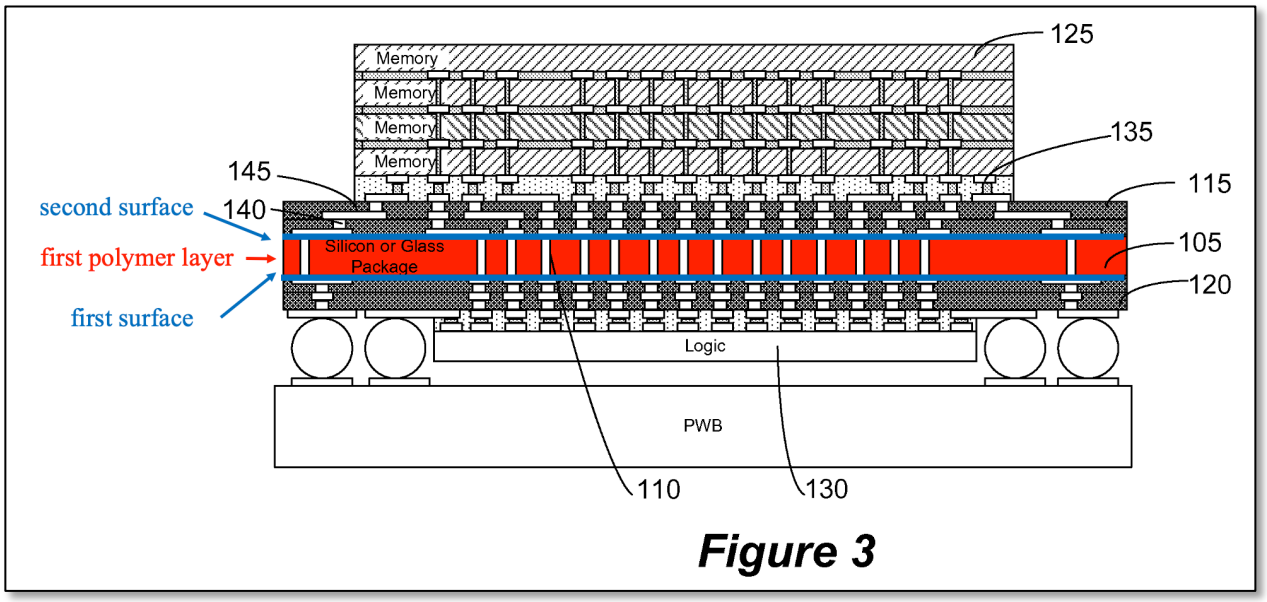


Figure 3

EX1004, FIG. 3[3]; *EX1003*, ¶¶130-131.

3. 1(a)(i)

Sundaram's *first surface is substantially parallel to said second surface.*

[3] Sundaram's original FIG. 3 includes the "Silicon or Glass Package" text; however, as mapped, Sundaram expressly teaches the interposer can be a *polymer*.

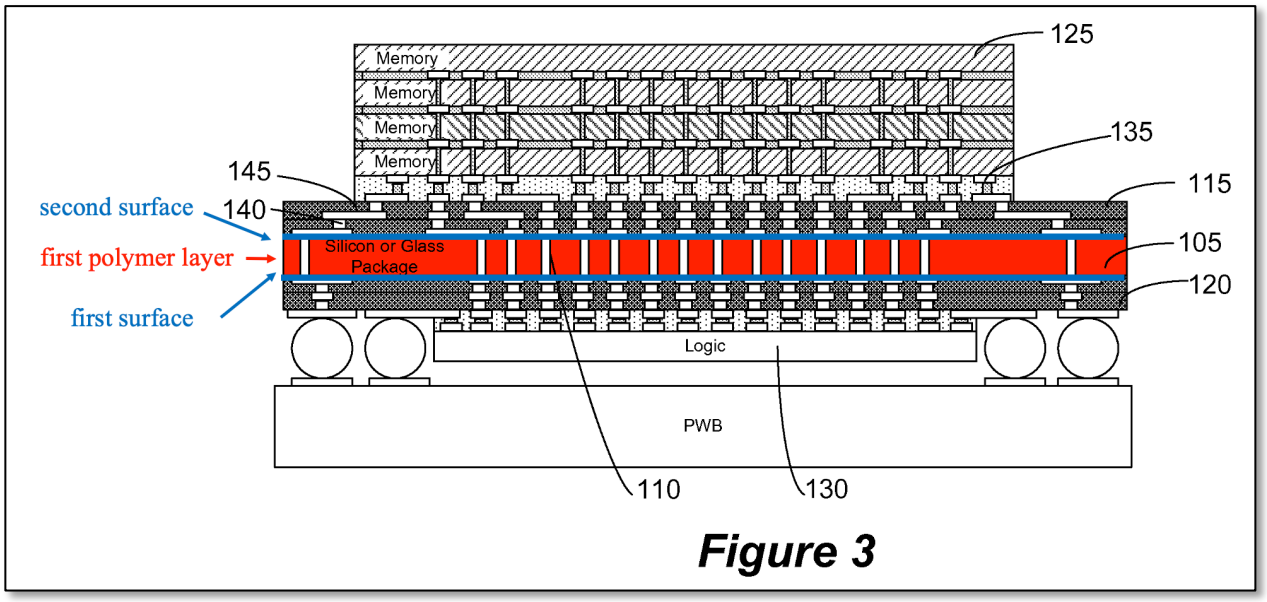


Figure 3

EX1004, FIG. 3; *EX1003*, ¶132.

4. 1(a)(ii)

Sundaram teaches or renders obvious the claimed thickness. Sundaram teaches interposer 105 (*first polymer layer*) is "about 20 to about 200 micrometers in thickness," overlapping with the claimed *thickness* range. *EX1004*, 2:22-25, 14:34-36. The '768 Patent does not ascribe any criticality to the claimed *thickness between 100 and 300 micrometers*. Instead, the '768 Patent describes smaller (20 micrometers) and much larger values (2000 micrometers), indicating to a POSITA the thickness varies widely and is not otherwise critical. *EX1001*, 7:53-57; *EX1003*, ¶¶133-134; *Clearvalue, Inc. v. Pearl River Polymers, Inc.*, 668 F.3d 1340, 1345 (Fed. Cir. 2012) (finding the prior art reference's teaching of "150 ppm or less" anticipated claimed "less than or equal to 50 ppm" where the challenged patent did

not indicate criticality of the claimed range); MPEP 2131.03(II); *UCB Inc., et al. v. Actavis Labs. UT, Inc., et al.*, 65 F.4th 679, 689-90 (Fed. Cir. 2023) ("A presumption of obviousness applies '[w]here a claimed range overlaps with a range disclosed in the prior art.'" (quoting *Ormco Corp. v. Align Tech., Inc*., 463 F.3d 1299, 1311 (Fed. Cir. 2006)); MPEP 2144.05.

5. 1(a)(iii)

a) Haba's Teachings

Haba teaches an "interconnection component 2" that "include[s] a dielectric layer 20 that is made from a material having a low coefficient of thermal expansion…in the range of **8 parts per million per degree Celsius**." *EX1009*, 5:55-59; MPEP 2131.03(I). Dielectric layer 20 is "a polymeric dielectric," and thus is a *polymer layer*, like Sundaram's interposer 105. *EX1009* 5:41-44; *EX1003*, ¶¶135-136.

b) MTC

A POSITA would have been motivated and found obvious to modify Sundaram per Haba's teachings of a polymer layer with a coefficient of thermal expansion (CTE) of 8 ppm/°C. *EX1003*, ¶137. Haba expressly motivates the combination, teaching "the difference in the CTE between the interconnection component and…the microelectronic element 66 can be reduced to a more manageable quantity," enables "reductions in solder bump sizes…to achieve finer pitch." *EX1009*, 5:67-6:5. Haba's microelectronic element 66 is a "semiconductor

chip[]"; thus, a POSITA would have found it advantageous to modify Sundaram's interposer 105 to have a low CTE to likewise reduce the difference in CTE between interposer 105 and Sundaram's electronic devices (chips) 125, 130. *EX1009*, 1:19-23; *EX1003*, ¶¶138-139.

Sundaram also motivates the combination, teaching a "silicon-matched" CTE is advantageous for an interposer. *EX1004*, 2:4-6. A POSITA would have found obvious modifying Sundaram's polymer interposer 105 to have a CTE closely matched to the silicon chips, per Haba. *EX1003*, ¶140.

The combination is the application of a known technique (a polymer interposer with a CTE of 8 ppm/°C) to a known device (Sundaram's polymer interposer) to yield predictable results, and there would have been a REOS because the use of low CTE polymers as interposers was well known, including those with vertical interconnects therein. *EX1003*, ¶¶141-143.

6. 1(b)

Sundaram teaches *a first metal plug vertically in a first through via*, i.e., copper metalized through vias 110, where the copper metallization forms *metal plug[s]* in *through vias*. Sundaram teaches "through vias 110 can be defined within the interposer" (*in said first polymer layer*) and "metalized with a highly-conductive **metal**." *EX1004*, 6:6-9, 6:25-27, 13:30-34. Through vias 110 are *vertical[]*:

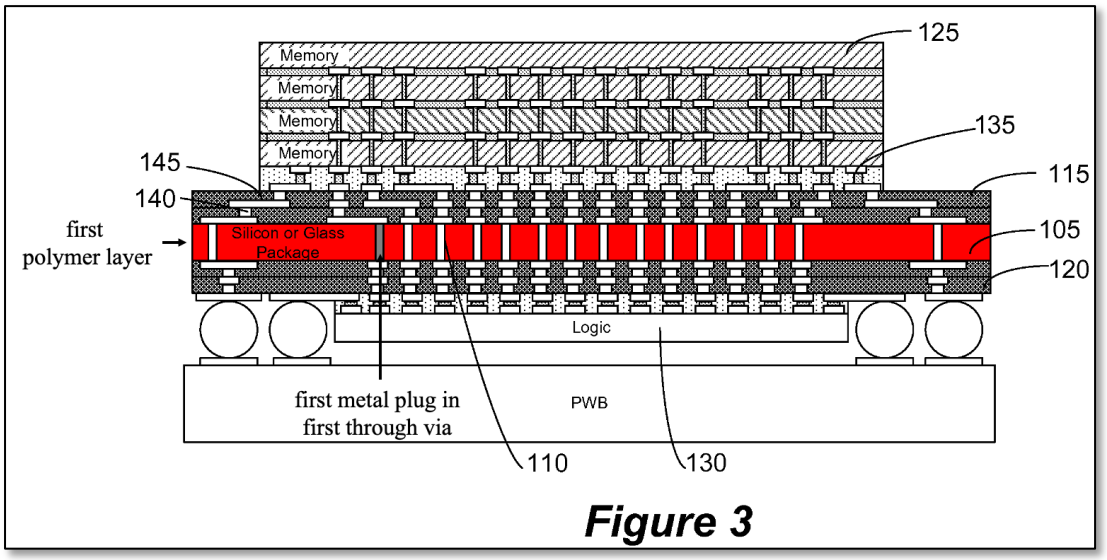


Figure 3

EX1004, FIG. 3; *EX1003*, ¶144.

7. 1(b)(i)

Sundaram teaches "metaliz[ing]" through vias 110 with **copper** such that the *first metal plug* comprises a *first copper layer* (the metalized copper) that *contacts with a sidewall* of a through via 110. *EX1004*, 6:22-27, 13:30-34; *EX1003*, ¶¶145-146.

8. 1(c)

A second metal plug vertically in a second through via in said first polymer layer is shown below.

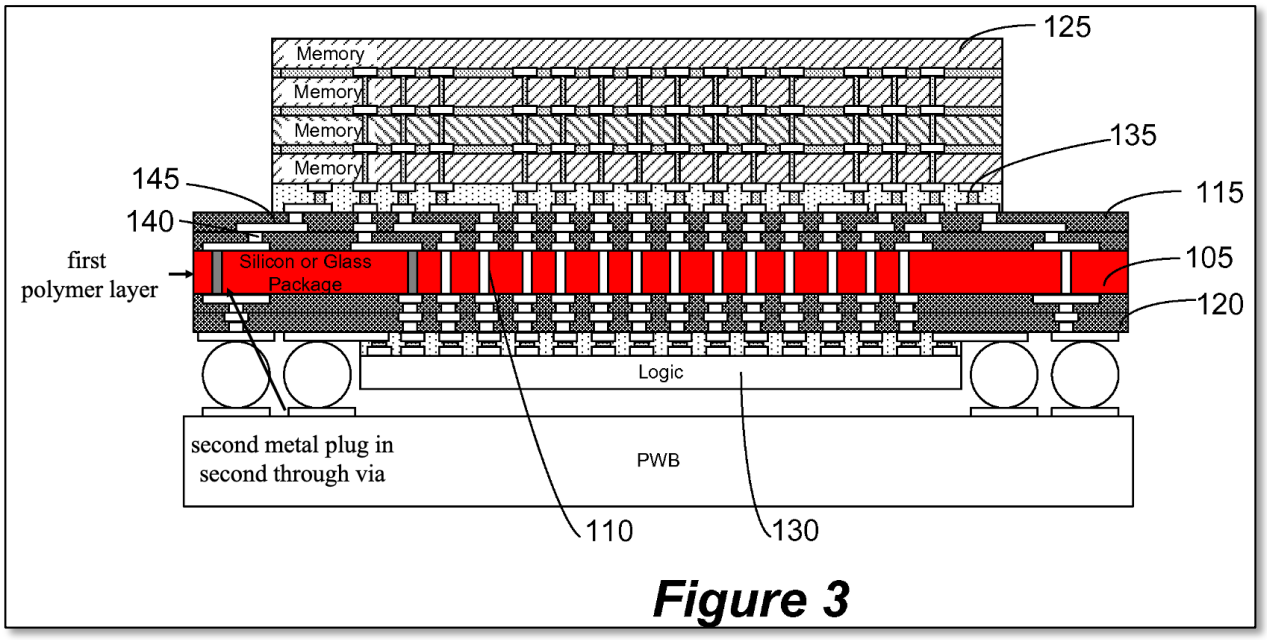


Figure 3

EX1004, FIG. 3; *EX1003*, ¶147.

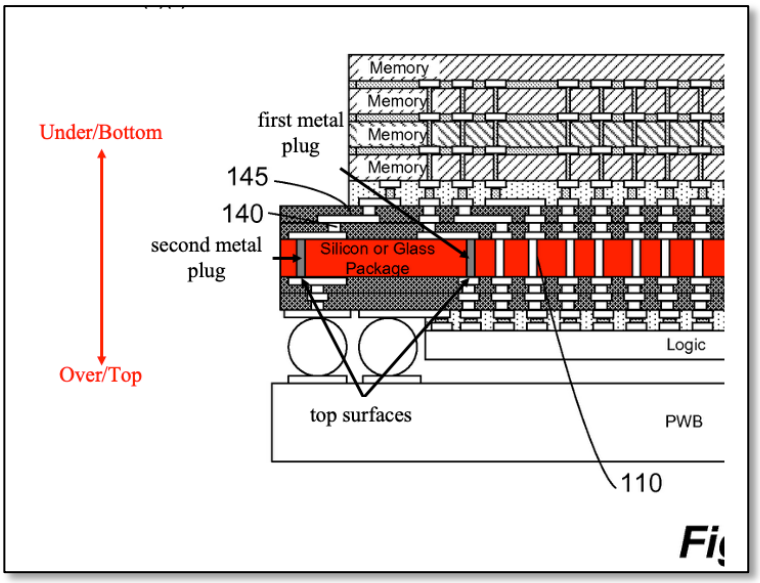
9. 1(c)(i)

Section V.A.7, reciting corresponding limitations[4]. *EX1003*, ¶148.

10. 1(c)(ii)

The *first* and *second metal plug[s]* have *top surface[s] in the same horizontal plane*. The mapped surfaces are "top" surfaces when the figure is rotated upside down.

[4] The "first" copper layer is recited in 1(b)(i).



EX1004, FIG. 3 (excerpt). Section V.A.11 (discussing *over/under* directions); *EX1003*, ¶149.

11. 1(d)

Sundaram teaches "polymer-metal redistribution layers" are "deposited on the first side 115 and second side 120 of the interposer 105" and include "blind vias 140 and conductor traces 145[.]" *EX1004*, 6:62-67. Electronic devices 125, 130 "are connected with through vias 110, blind vias 140, [] conductor traces 145," and "die pads 135" formed *over said first surface*. *EX1004*, 7:4-8, 6:29-33. Blind vias 140, conductor traces 145, pads 135, and the polymer in the polymer-metal redistribution layer (RDL) form *a first interconnection scheme over*[5] *said first surface*.

[5] Each reference's figures indicate the *over/under* direction where appropriate. The *over* direction is towards the PWB. *EX1003*, ¶150. PO similarly used inverted

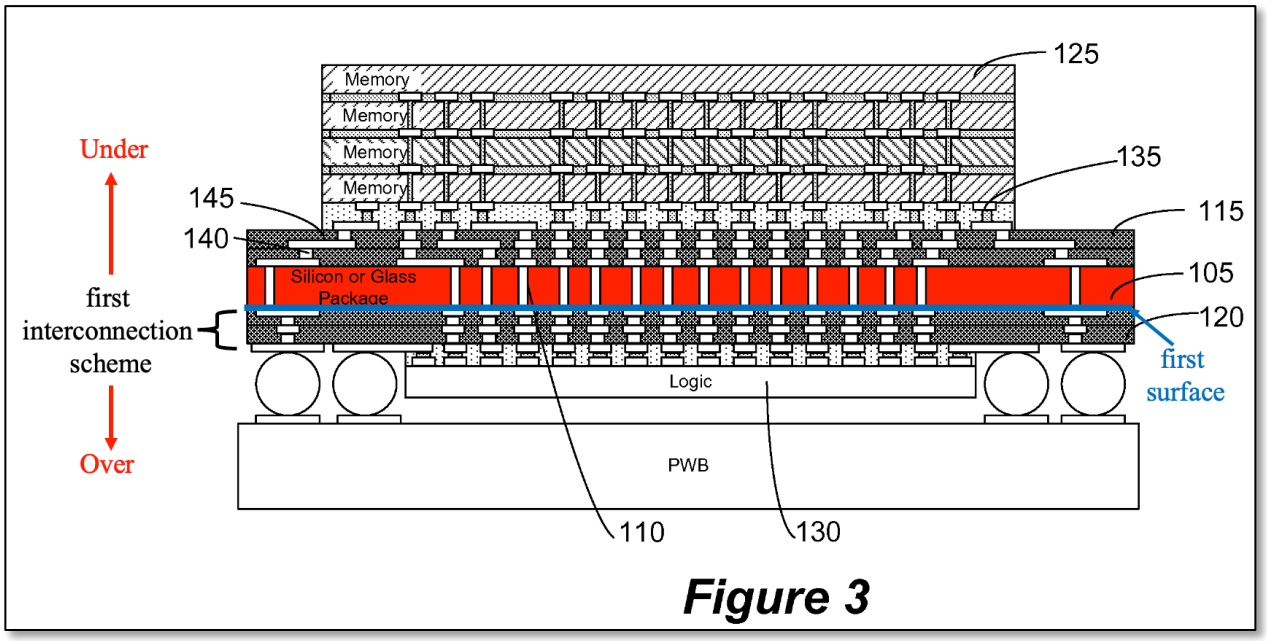


Figure 3

EX1004, FIG. 3; *EX1003*, ¶152.

12. 1(d)(i)

The "blind vias 140" and "conductor traces 145" are the "metal" in Sundaram's "polymer-metal redistribution layers" such that vias 140 and traces 145 are *metal interconnects* of the *first interconnection scheme*. *EX1004*, 6:62-7:8. Shown below in Sundaram's RDL are a *first metal interconnect* comprising a first trace 145 (longer rectangles in FIG. 3) and a first via 140 (shorter rectangles); a

---

figures during prosecution to explain the *over/under* relationship between various claim elements. *Compare EX1001*, FIG. 9t *with EX1002*, 395-400, 537-538; *EX1003*, ¶151.

second metal interconnect comprising a second trace 145 and via 140; and *a third metal interconnect* comprising a third trace 145 and via 140. *EX1003*, ¶¶153-154. Each *interconnect* is *over said first surface*. Further depicted is *second polymer layer over said first, second and third metal interconnects* (the "polymer" of the "polymer-metal redistribution layers."). *EX1004*, 6:62-67; *EX1003*, ¶¶156-157 (discussing '768 Patent's prosecution history). The *second polymer layer* at least includes the below highlighted layer but may include an additional portion of the RDL (*see* Claim 11, Section V.K).

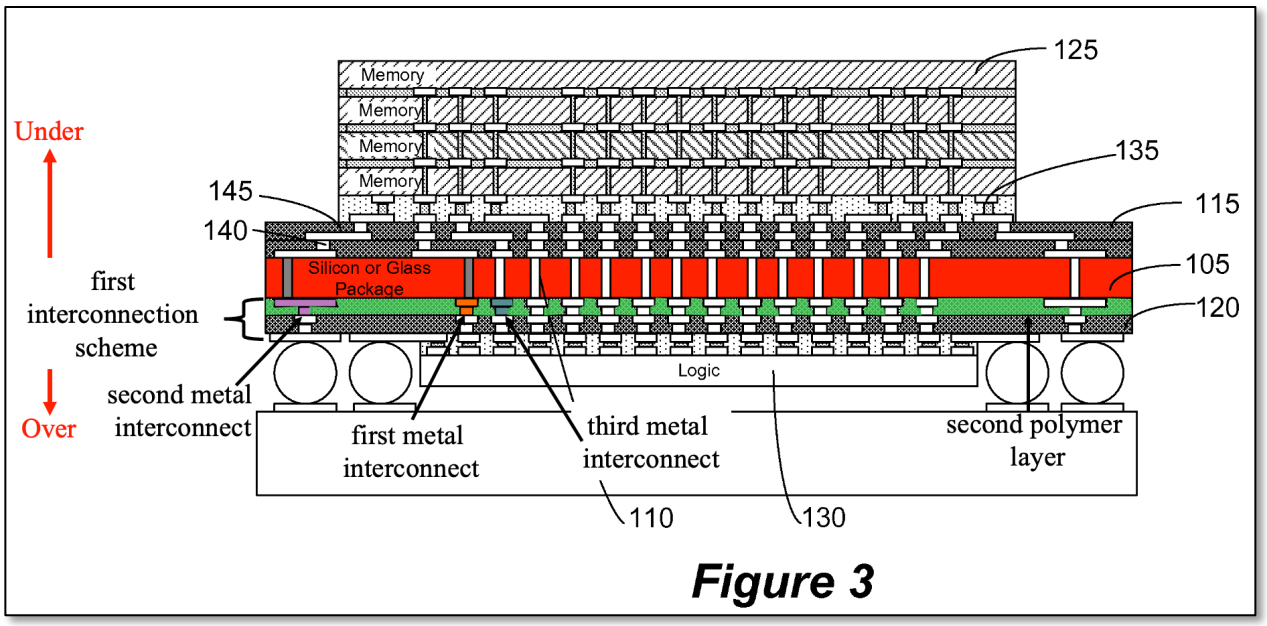


Figure 3

EX1004, FIG. 3.

Alternatively, the *second polymer layer* is the outermost portion of the RDL.

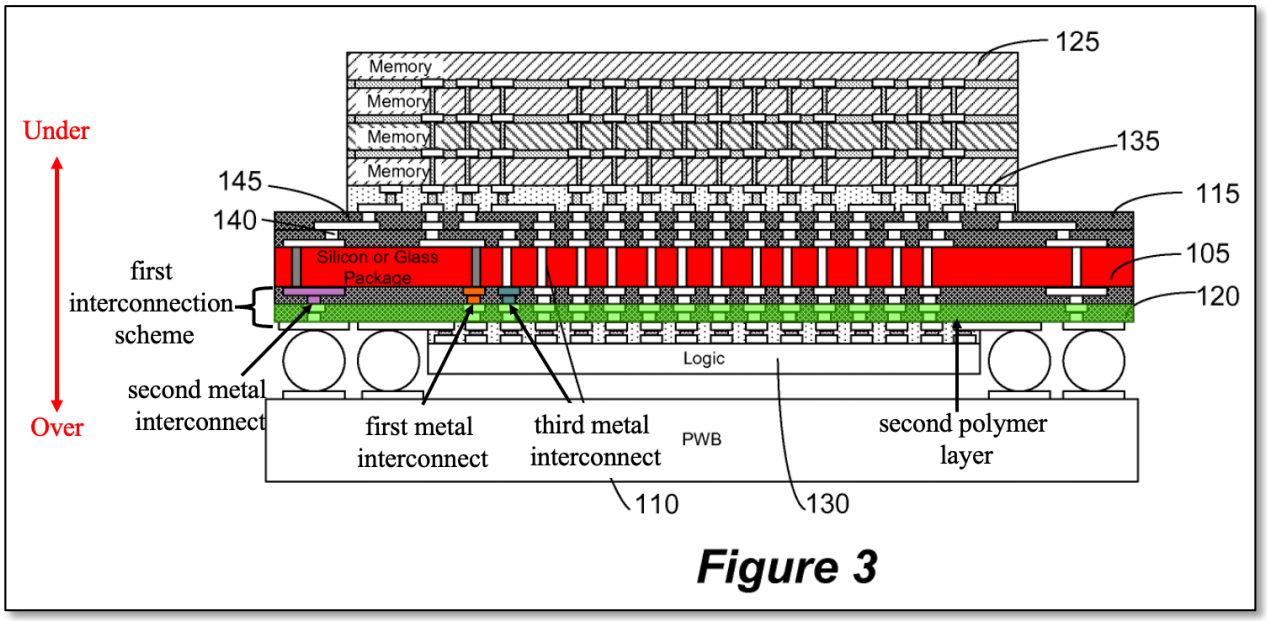


Figure 3

EX1004, FIG. 3; *EX1003*, ¶155.

13. 1(d)(ii)

The *first* and *second metal interconnect[s]* are *connected to* the *first* and *second metal plug[s]*, respectively, as shown below, such that devices 125, 130 "are connected with through vias, 110, blind vias 140, and conductor traces 145." *EX1004*, 7:4-9.

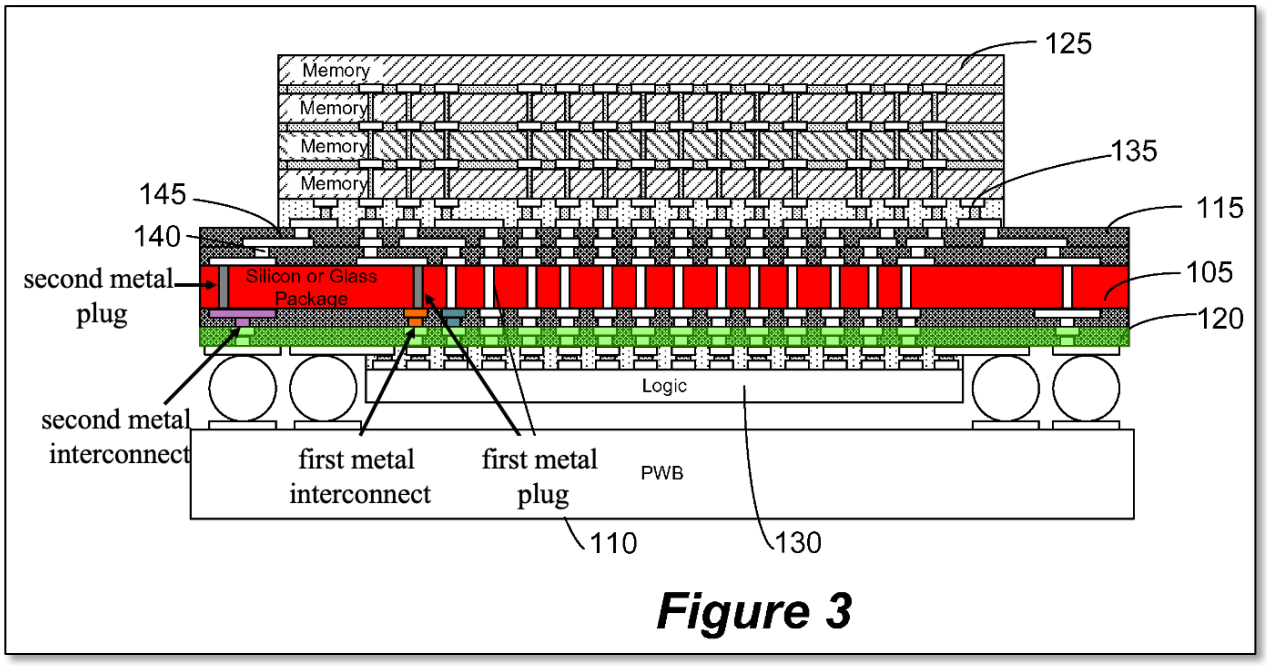


Figure 3

EX1004, FIG. 3; *EX1003*, ¶158.

14. 1(d)(iii)

a) Lin-191's Teachings

Lin-191 teaches a multi-layered metal interconnect ("patterned metal layer 3") with an adhesion layer 31 (*first metal layer*); a copper seed layer 32 *on* adhesion layer 31 (*third copper layer*); and a metal layer 33 *on* seed layer 32 (*fourth copper layer*). *EX1005*, [0148]. Layer 3 "connect[s]" bumps 34 to bumps 14, 24 such that layer 3 is *a metal interconnect*. *EX1005*, [0148]. Adhesion layer 31 includes "nickel;" seed layer 32 includes "**copper**"; and metal layer 33 includes "**copper**." *EX1005*, [0128], [0133].

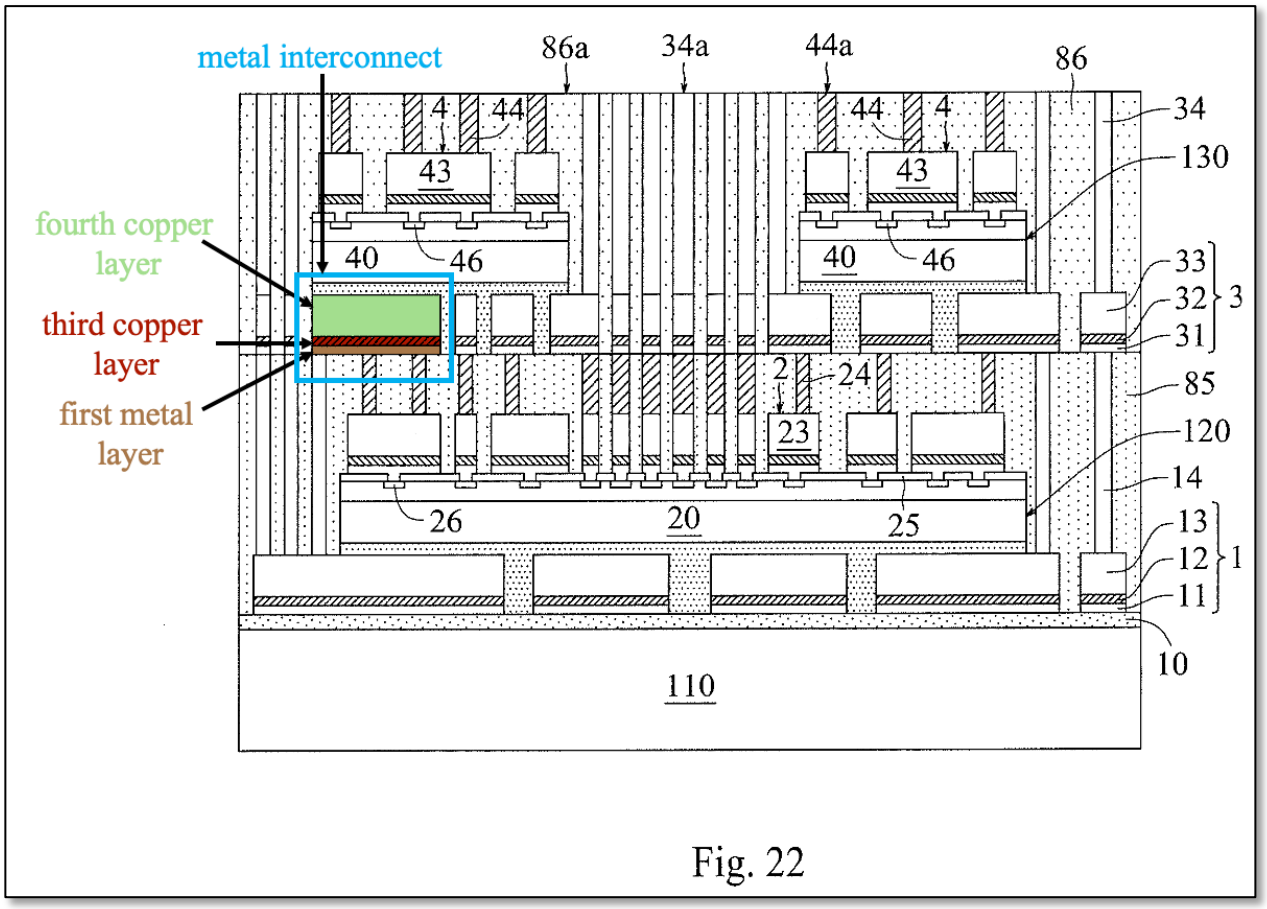


Fig. 22

EX1005, FIG. 22; *EX1003*, ¶¶160-161.

b) MTC

A POSITA would have been motivated and found obvious to apply Lin-191's teachings of multi-layered metal interconnect layers including *metal* and *copper* layers to Sundaram's *metal interconnect* that likewise includes conductor traces (*EX1004*, 6:62-67), yielding Sundaram's *first metal interconnect* comprising the claimed layers. *EX1003*, ¶162. A POSITA would have understood that Lin-191's multi-layered copper structure corresponds to sequentially deposited seed and

plating layers formed during electroplating, providing adhesion to the underlying metal layer and buildup of conductor thickness. *EX1003*, ¶163.

A POSITA would have been motivated to utilize a multi-layered metal interconnect structure to leverage the advantages of different materials. *EX1003*, ¶¶163-168. Nickel layer 31 advantageously mitigates copper diffusion out of the metal interconnect, reducing void formation. *Id*. Copper also has well-known benefits, including electrical conductivity and electromigration resistance, that are desirable for interconnect material in high-density packaging. *Id*. Copper has a lower electromigration rate than conventional conductive materials (e.g., aluminum), reducing failures occurring at elevated temperature and high current density. *Id*. The electrical conductivity of copper is also superior to other metals (e.g., aluminum), enabling faster signal transmission and lower power dissipation. *Id*.

The combination is the application of a known technique (Lin-191's multi-layered metal interconnect layers) to a known device (Sundaram's *chip package* that includes a metal interconnect) ready for improvement to yield predictable results, i.e., the predictable result of Sundaram's *metal interconnect* having metal/copper. *EX1003*, ¶169..

The combination would have had a REOS at least because the use of multi-layered metal interconnect including copper in vias, traces, and pads was well established by the time of the '768 Patent, and the electroplating techniques taught

by Lin-191 are directly applicable to Sundaram's interconnection component. *EX1005*, [0133]; *EX1004*, 10:36-39; *EX1003*, ¶170.

15. 1(e)

Sundaram teaches *a first metal bump over said first interconnection scheme and said second metal plug*, namely, a "copper **bump**[] with solder cap[]" that "electrically connect[s] devices." *EX1004*, 6:29-32.

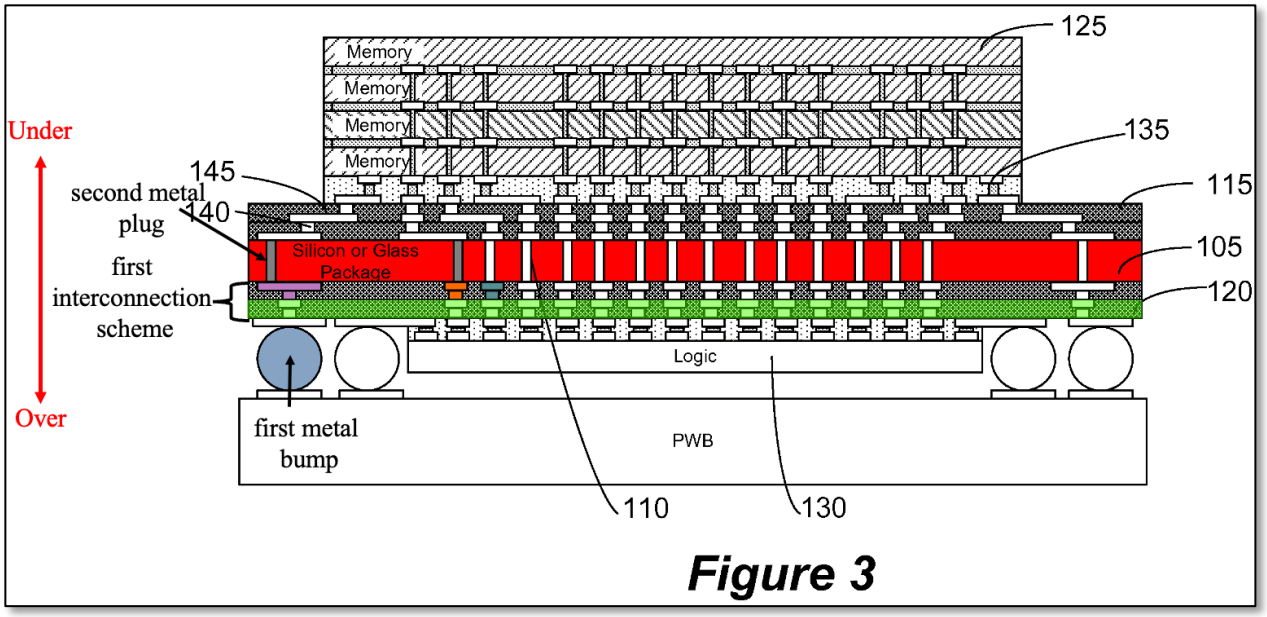


Figure 3

EX1004, FIG. 3; *EX1003*, ¶171.

16. 1(e)(i)

Sundaram's "copper bumps with solder caps" teach *a tin-containing layer* (the solder cap) as a POSITA would have understood solder to include tin. *EX1004*, 6:29-32. Sundaram thus teaches this limitation. *EX1003*, ¶172.

a) Lin-191's Teachings

Additionally or alternatively to Sundaram, Lin-191 teaches a *bump* with a *tin-containing layer*. Specifically, Lin-191 teaches "solder bumps or balls 29a" formed by reflowing a "solder layer 29," which is "a single metal layer formed by electroplating…**a tin-containing layer**."

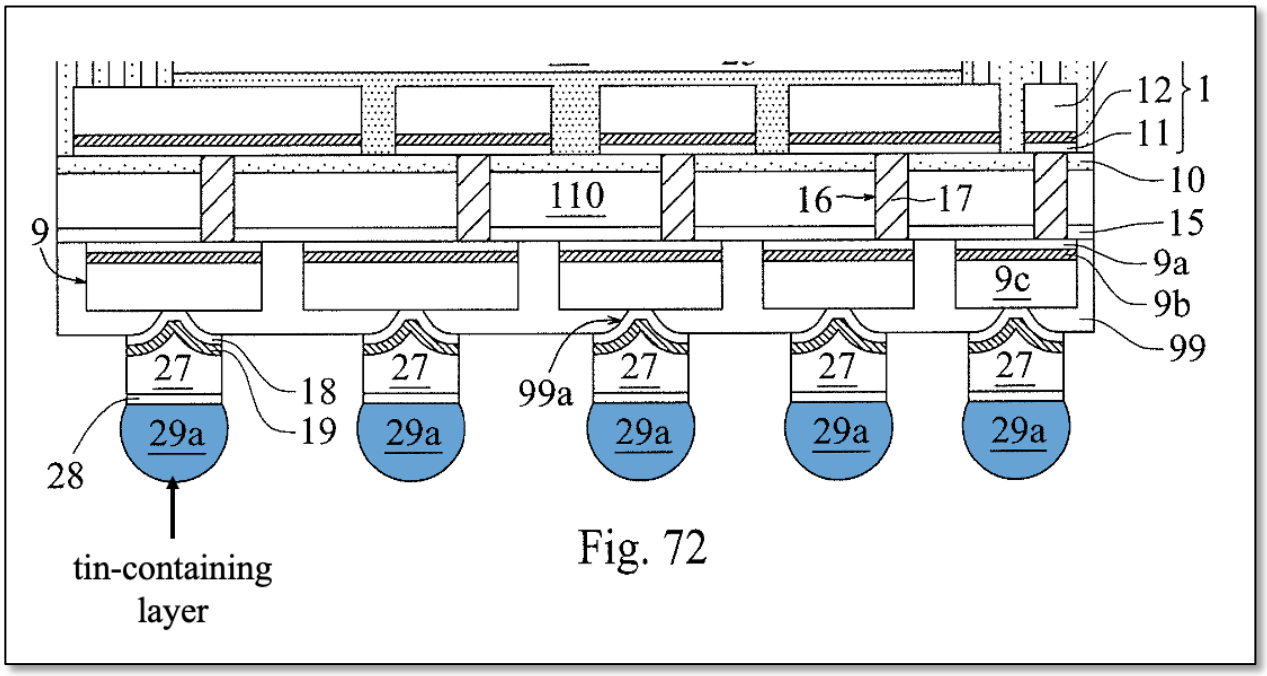


Fig. 72

EX1005, FIG. 72 (excerpt); *EX1003*, ¶¶173-174.

b) MTC

A POSITA would have been motivated and found obvious to apply Lin-191's teachings of a metal bump having *a tin-containing layer* to Sundaram's copper bumps with solder caps. *EX1003*, ¶175. Tin was known to advantageously "wet and spread on a wide range of substrate," motivating the combination. *EX1098*, 104; *EX1005*, [0323], [0437]; *EX1003*, ¶176.

The Sundaram-Lin-191 combination is the application of a known technique (Lin-191's bump structure) to a known device (Sundaram's bump) ready for improvement to yield predictable results. *EX1003*, ¶177. Alternatively, the Sundaram-Lin-191 combination is the simple substitution of Lin-191's solder bump structure for Sundaram's "copper bumps with solder caps." *EX1004*, 6:29-33; EX1003, ¶178.

A POSITA would have had a REOS in either applying Lin-191's teachings to Sundaram's bump or substituting Sundaram's bump with Lin-191's bump at least because such a modification/substitution would have involved the application of well-known manufacturing techniques well within the skill of a POSITA. *EX1003*, ¶179.

17. 1(f)

Sundaram's first electronic device 125 "can be…stacked memory IC devices" such that a memory chip of the stack is *a first semiconductor chip under said first interconnection scheme*. *EX1004*, 6:34-46.

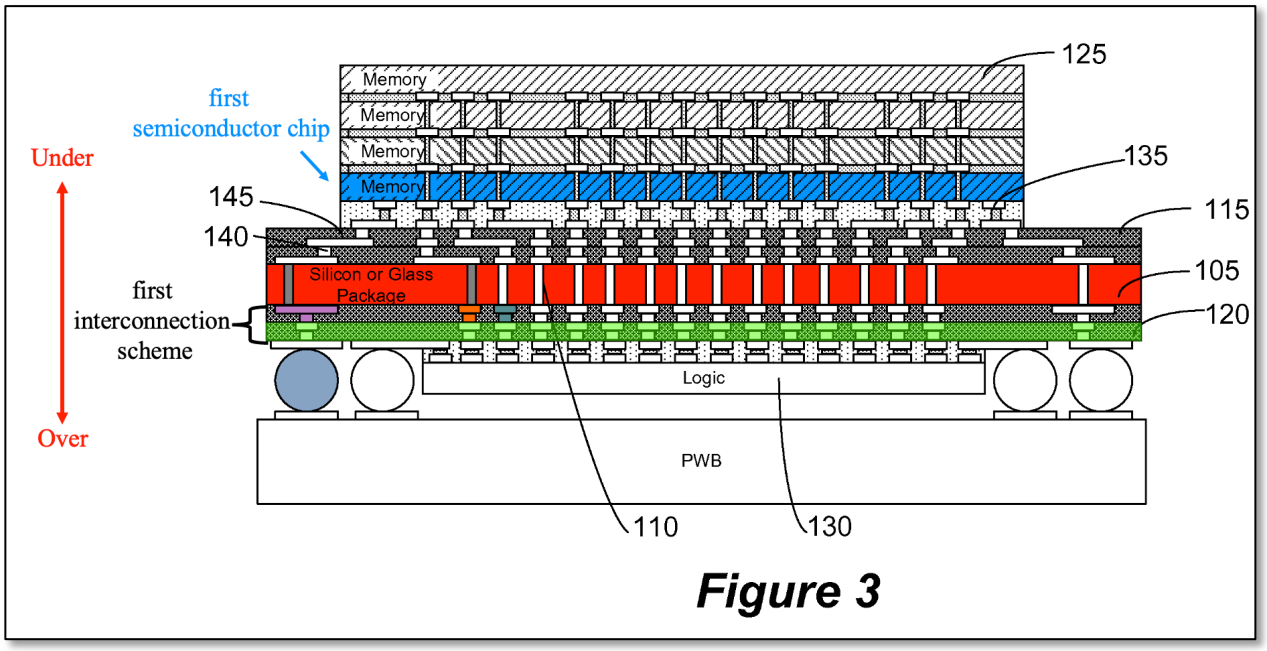
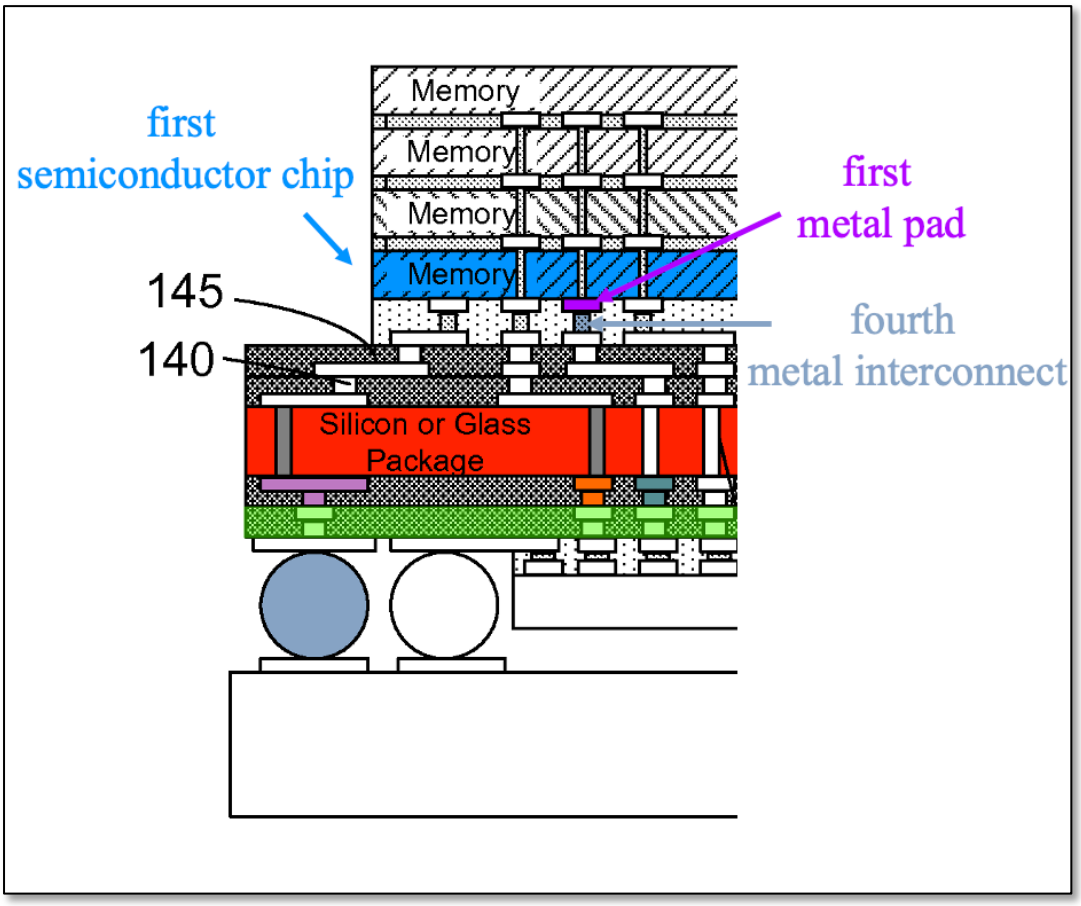


Figure 3

EX1004, FIG. 3; *EX1003*, ¶180.

18. 1(f)(i)

Interposer 105 has die pads 135 where "metallization provides die pad surfaces 135[.]". *EX1004*, 6:23-25. A POSITA would understand that device 125 also has die pads such that an electrical connection is made between interposer 105 and device 125, thus teaching the *first semiconductor chip* having a *first metal pad*. *EX1003*, ¶181. "[D]ie pads 135…can electrically connect devices using solder, copper bumps with solder caps, copper to copper bonding," each of which teaches *a fourth metal interconnect*. *EX1004*, 6:29-33. In FIG. 3, the *fourth metal interconnect* is a bump on die pad 135.



EX1004, FIG. 3 (excerpt).

Additionally or alternatively, FIG. 32 is a "side-by-side configuration" of the interconnect structure, which includes a memory stack where each chip has a *metal pad*:

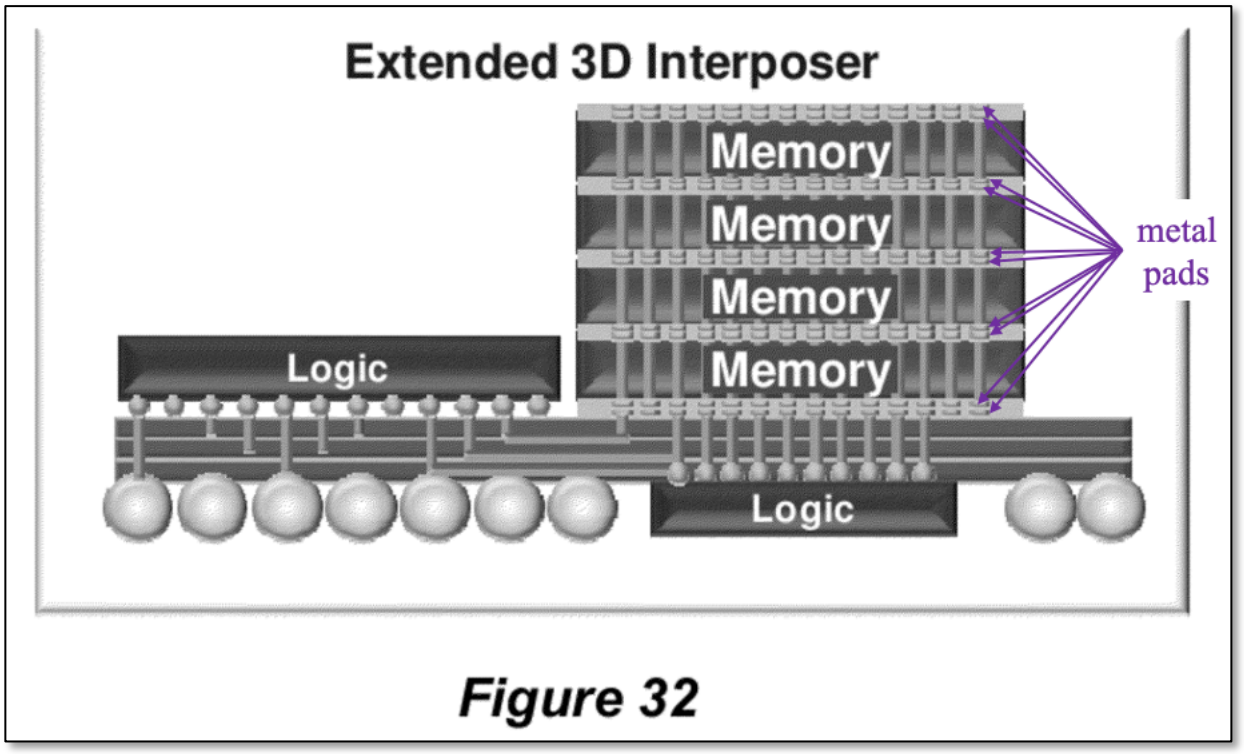
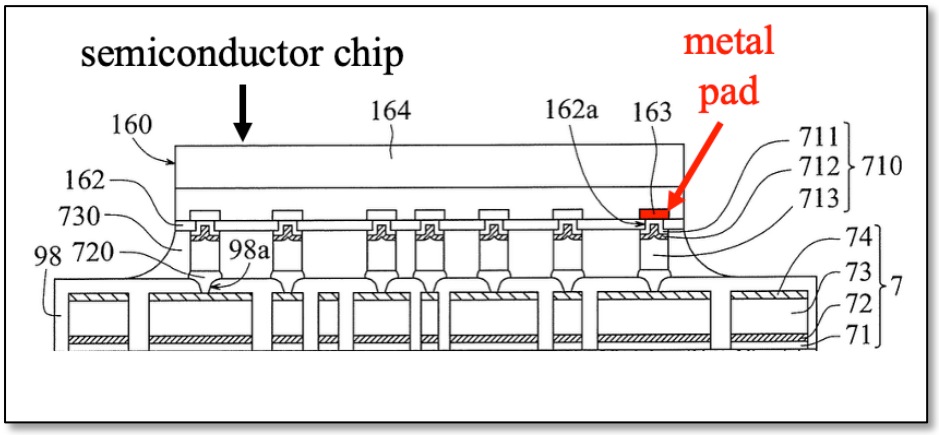


Figure 32

EX1004, FIG. 32, 4:26-27, 7:56-59; *EX1003*, ¶182. MTCs and REOS are below for modifying Sundaram's chip to have a *metal pad* incorporated. Section V.A.18.b.

a) Lin-191's "Metal Pad" Teachings

Additionally or alternatively to Sundaram's teachings, Lin-191 teaches a semiconductor chip 160 with "**metal** traces or **pads** 163" that include "aluminum." *EX1005*, [0384].



EX1005, FIG. 71 (excerpt); *EX1003*, ¶183.

b) MTC

A POSITA would have been motivated and found obvious to modify Sundaram per Lin-191's metal-pad teachings. *EX1003*, ¶184. The modification is an implementation detail in Sundaram's chip package, and the combination is the application of a known technique (metal pads) to a known device (Sundaram's semiconductor chip having die pads) ready for improvement to yield the predictable result of Sundaram's device 125 having a *first metal pad*. *EX1005,* [0081]; *EX1003*, ¶¶184-185. Because chips having metal pads is ubiquitous and essential for interconnecting the chip to other components, the modification has an REOS. *Id.*

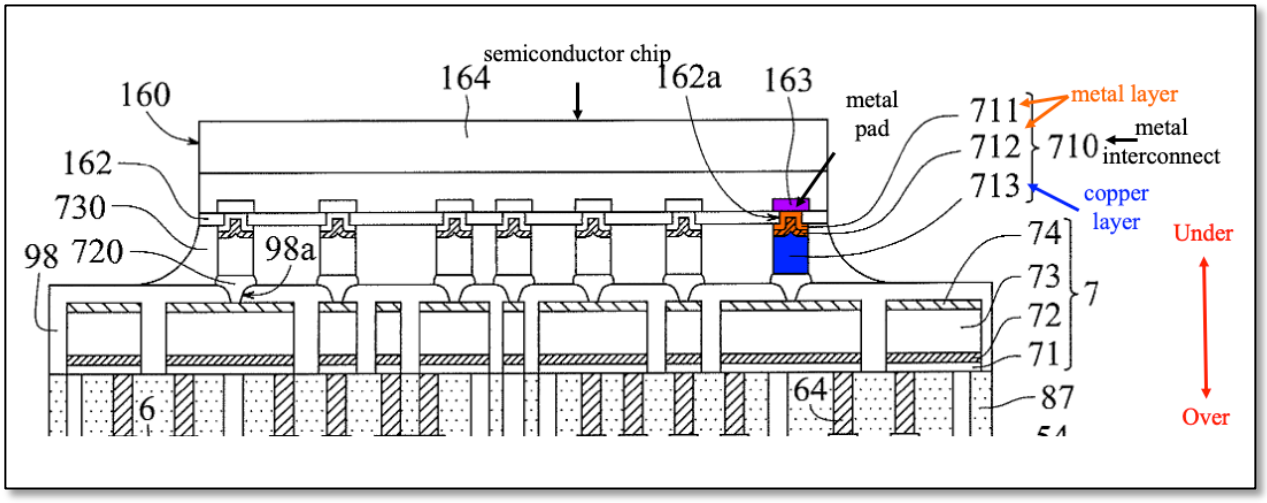
19. 1(f)(ii)

a) Lin-191's Teachings

Lin-191 teaches metal bumps 710 *on* "the metal traces or pads 163" of chip 160 and teaches bumps 710 *interconnect* chip 160 to another chip 140 such that

bumps 710, like Sundaram's copper bumps, are *metal interconnect[s]*. *EX1005*, [0406]; *EX1003*, ¶186.

Bumps 710 include an "adhesion layer 711 under the contact points…of the metal traces or pads 163…a seed layer 712 under the adhesion layer 711, and a metal layer 713 under the seed layer[.]" *EX1005*, [0389]. Adhesion layer 711 includes "nickel" or "titanium." *EX1005*, [0390]. Seed layer 712 "can be a copper layer." *EX1005*, [0392]. Thus, the combination of layers 711 and 712 is a *second metal layer on* metal pad 163. *EX1003*, ¶186. Metal layer 713 is "a single **copper** layer having a thickness…between 2 and 30 micrometers;" thus, it is a *copper layer* that teaches or renders obvious *a thickness between 5 and 30 micrometers*. *EX1005*, [0396]; Section V.A.4 (supporting caselaw); *EX1003*, ¶187 (citing *EX1001*, 14:15-27 and opining no criticality of the claimed copper thickness).



EX1005, FIG. 72 (excerpt); *EX1003*, ¶187.

b) MTC

A POSITA would have been motivated and found obvious to modify Sundaram's bump per Lin-191's layered bump teachings (including the thickness of copper layer 713), where the bump has a metal layer on a metal pad and a copper layer over the metal layer. *EX1003*, ¶¶188-193.

A POSITA would have recognized that Lin-191's metal bump provides improved metallurgical bonding and increased resistance to fatigue and stress-induced failure by employing a layered structure. *EX1003*, ¶189. This multi-layer configuration would reduce the risk of intermetallic formation at critical interfaces, mitigate electromigration, and better absorb mechanical strain during thermal cycling. *EX1003*, ¶¶189-190 Further, the mechanical integrity and reliability of Sundaram's bumps would be improved, particularly in applications subject to repeated temperature fluctuations and mechanical stress, improving long-term bump performance. *EX1003*, ¶191.

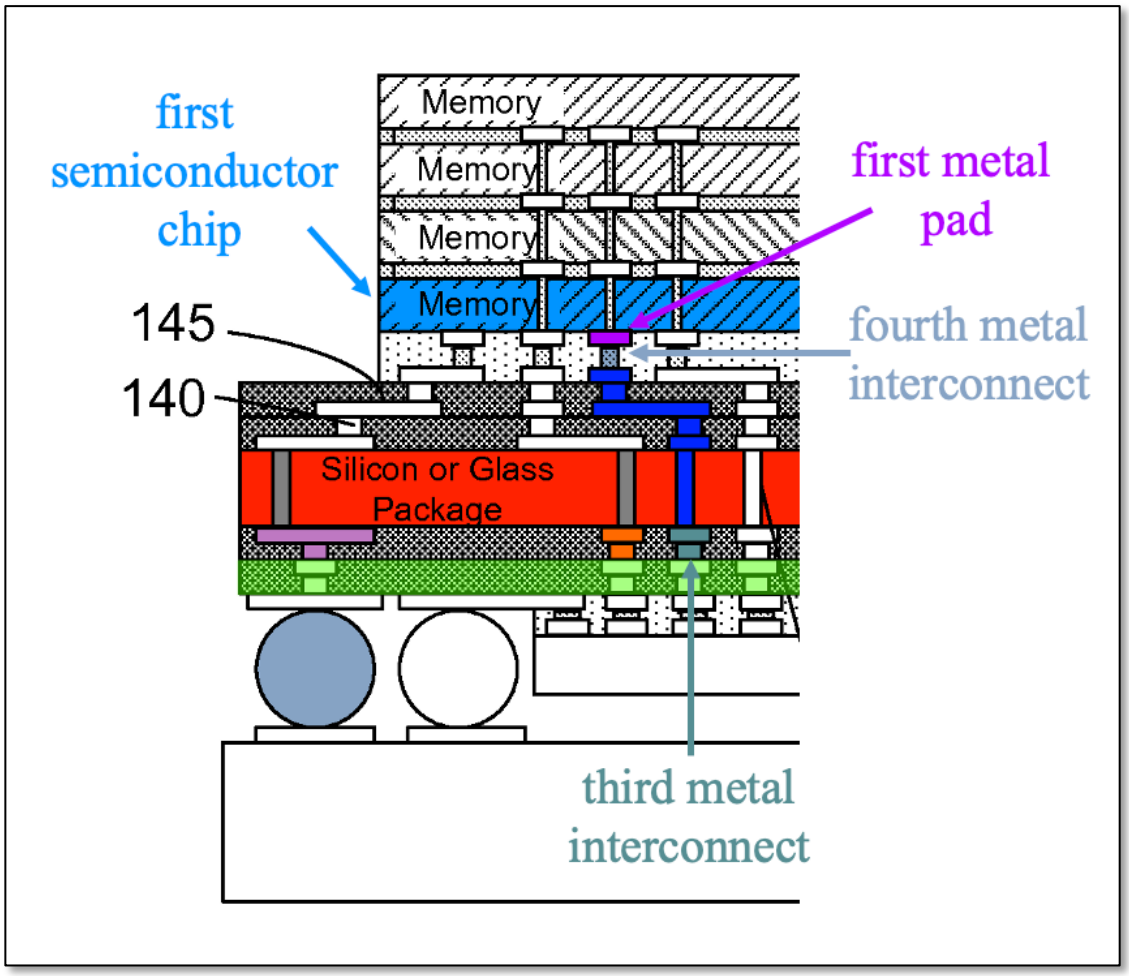
The combination is the application of known techniques to known devices to yield predictable results, i.e., predictably improving Sundaram's copper bump in the same way as Lin-191's bump. *EX1003*, ¶193. Alternatively, a POSITA would have been motivated to substitute Lin-191's bump structure for Sundaram's bump to obtain the above-described advantages of Lin-191's teachings. *Id*.

A POSITA would have had a REOS in either applying Lin-191's teachings to Sundaram's bump or substituting Lin-191's bump for Sundaram's similar bump, as both Lin-191 and Sundaram address semiconductor interconnect technology and because bump interconnects were well-known and fabricated using common manufacturing techniques taught by both Lin-191 and Sundaram. *Compare EX1005,* [0400] *with EX1004*, 6:22-29, 10:26-29; *EX1003*, ¶194.

20. 1(f)(iii)

Sundaram's *fourth metal interconnect is connected to*[6] *said third metal interconnect* through vias 140 and traces 145 and a through via 110.

[6] Petitioners note *connected to* does not require a direct physical connection but is met by an electrical connection. *See, e.g., EX1001*, 2:34-36, 14:28-32, 15:50-51; *EX1003*, ¶196.



EX1004, FIG. 3; *EX1003*, ¶¶195-196.

B. Claim 2

Sundaram teaches a *passive component* ("passives") connected to an interposer by "micro-bumps+RDL", thus teaching a *passive component over* and *connected to* an *interconnection scheme* (RDL) *through a solder layer* (micro-bumps). The micro-bumps are a *solder layer* because Sundaram teaches devices are connected using "solder, copper bumps with solder caps…" *EX1004*, 6:29-32.

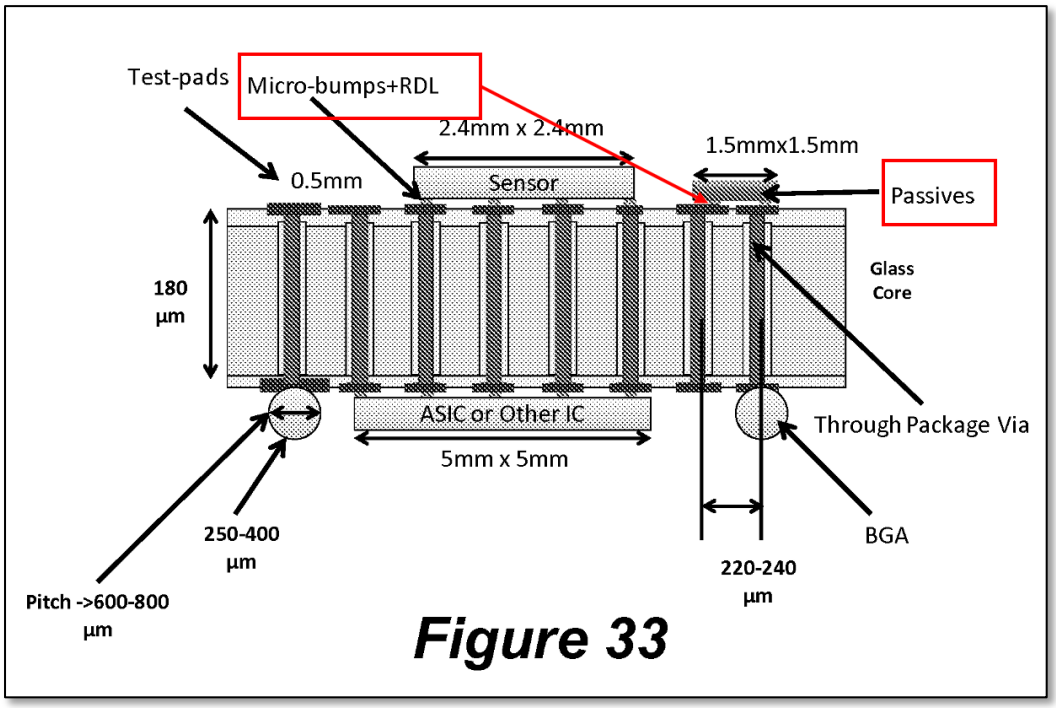


Figure 33

EX1004, FIG. 33; *EX1003*, ¶¶197-198.

a) MTC Sundaram's Embodiments

Based on FIG. 33's embodiment, a POSITA would have found obvious and been motivated to include a *passive component over* and *connected to* Sundaram *first interconnection scheme through a solder layer*, e.g., adjacent to FIG. 3's electronic device 130. *EX1003*, ¶¶199-200. Connecting a passive component, e.g., a capacitor, over Sundaram's *first interconnection scheme* would advantageously mitigate signal desynchronization and preserve signal integrity. *Id*. Capacitors in chip packages was a well-known technique to ensure signal quality and integrity because capacitors establish a transmission line signal path, thereby maintaining signal integrity when interconnecting with the PWB (printed wiring board). *EX1003*,

¶¶201-203. A POSITA would have been motivated to connect the passive component using a *solder layer* because they were ubiquitous for electrically connecting devices in chip packages. *Id*.

The modification is the application of a known technique (a passive component connected by a solder layer) to a known device (Sundaram's *chip package*) to yield the predictable result of Sundaram's *chip package* having a passive component over the RDL and connected thereto. *Id*. A POSITA would have had a REOS in modifying Sundaram's FIG. 3 embodiment based on FIG. 33's teachings because solder bonded passives were commonplace before the '768 Patent, making the modification simple and straightforward. *EX1003*, ¶204.

C. Claim 3

Sundaram's *first interconnection scheme* comprises a *fifth metal interconnect*, namely a die pad. *EX1004*, 6:22-25; Section V.A.11. Sundaram teaches "metallization provides die pad surfaces 135" on "the second side 120 of the interposer 105," which "electrically connect devices," and are therefore *metal interconnect[s]*. *EX1003*, ¶205. FIG. 3 illustrates numerous die pad surfaces. An example one of the many die pad surfaces is identified with reference numeral 135 in FIG. 3. *EX1004*, 6:22-33 (referencing die pads (plural)). A POSITA would have understood FIG. 3 expressly teaches a die pad, such as the orange-highlighted die pad, at least because of the ubiquity of connecting bumps to pads. *EX1003*, ¶205.

The orange-highlighted die pad is part of the *first interconnection scheme*. *EX1004*, 6:22-33.

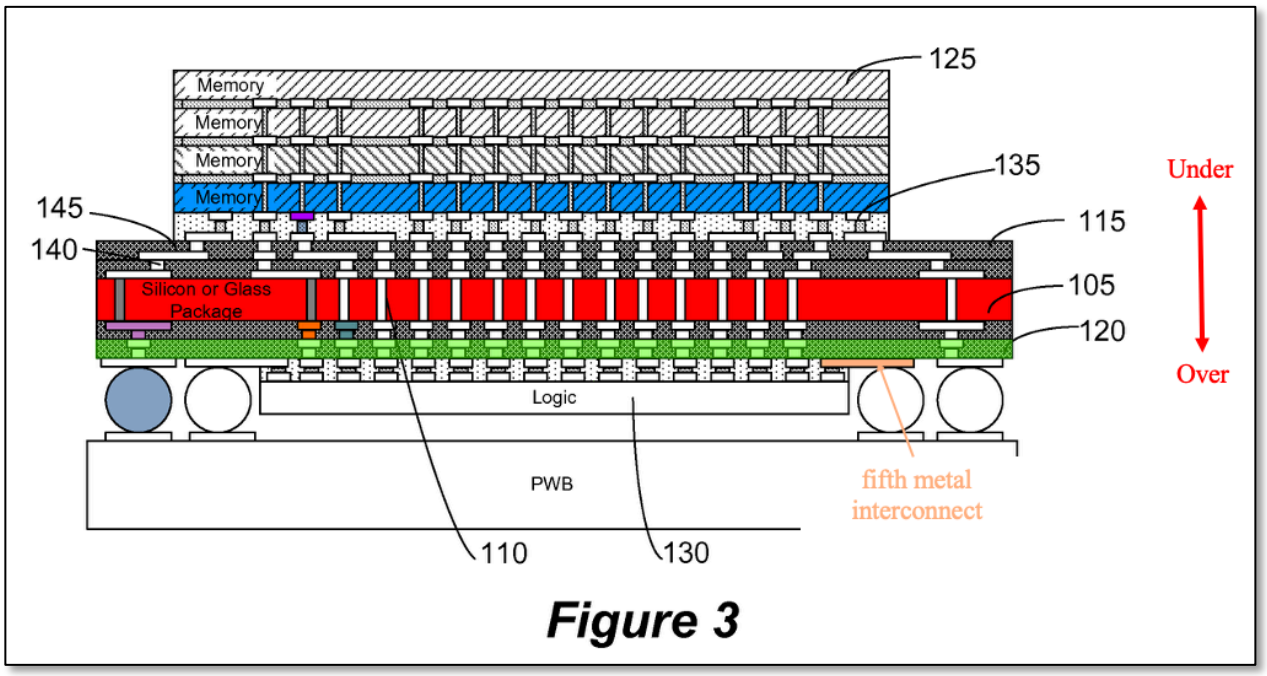
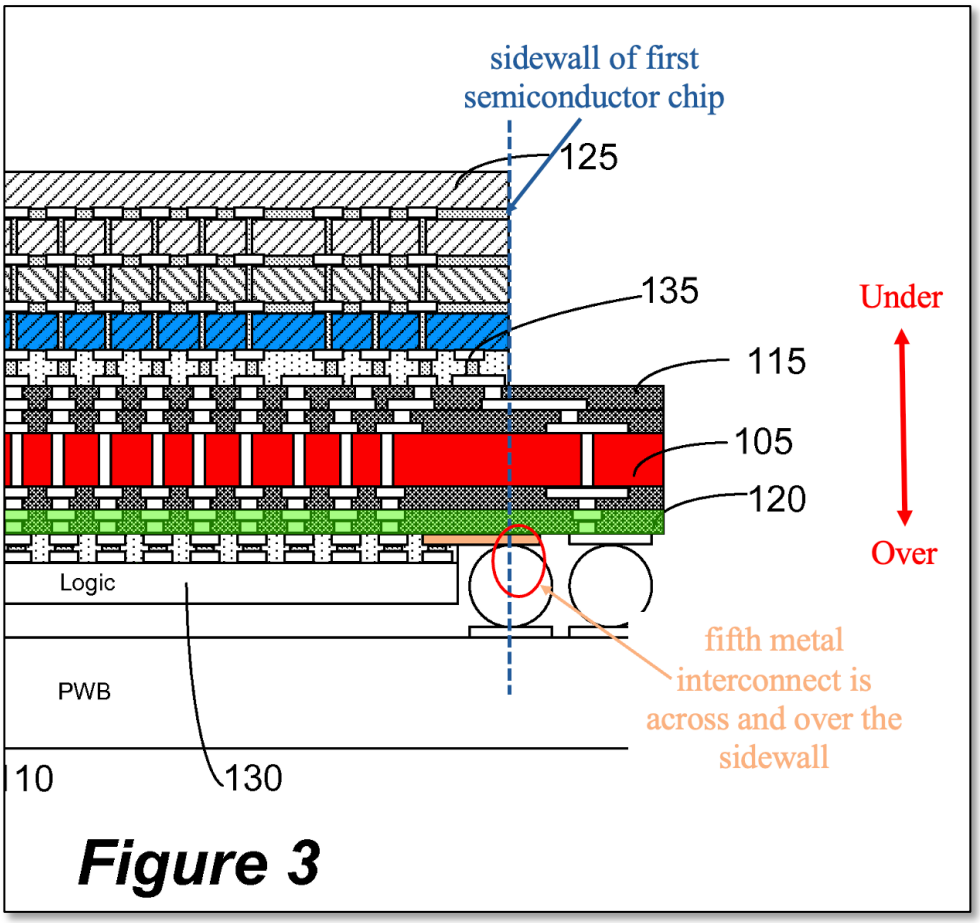


Figure 3

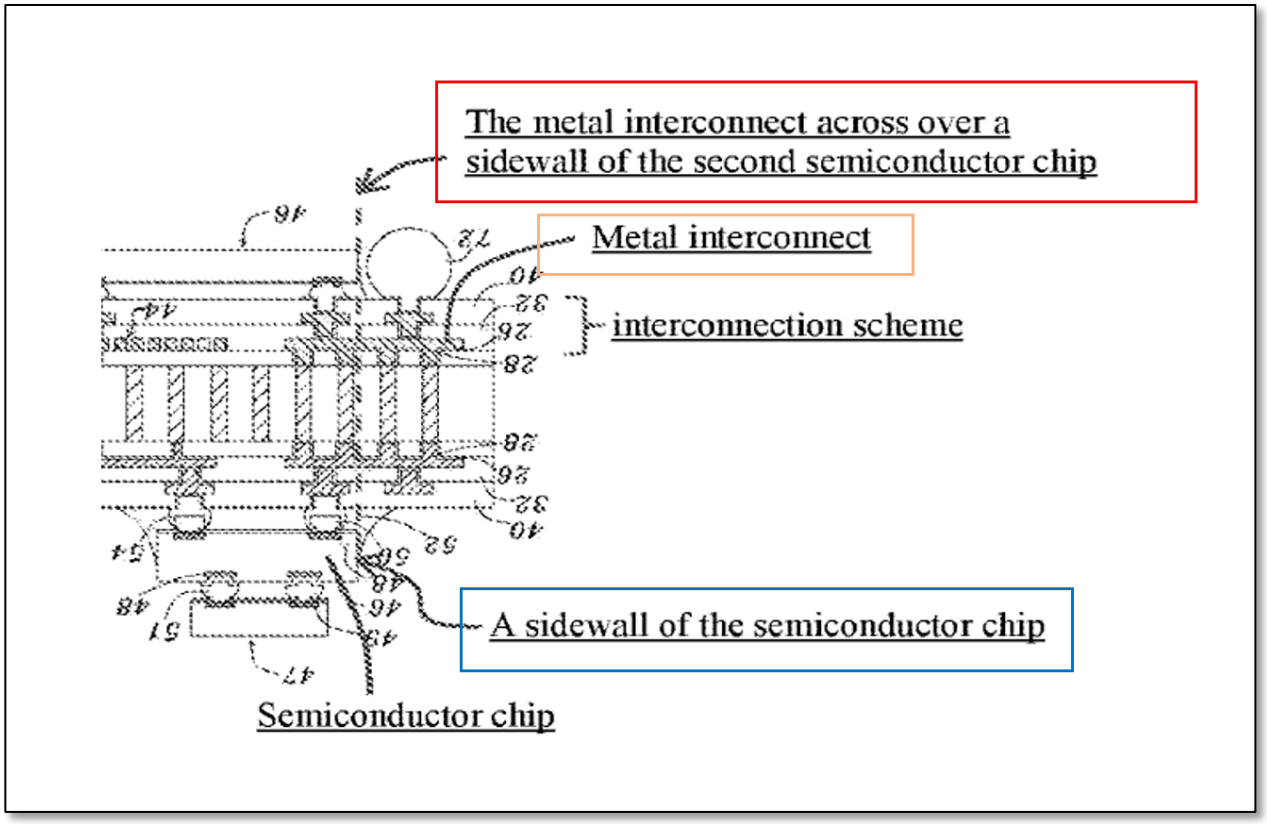
EX1004, FIG. 3.

Sundaram further teaches the orange-highlighted die pad is *across over a sidewall of* device 125 as the orange-highlighted die pad is positioned on the opposite side of interposer 105 from device 125's *sidewall* (*over*) and comprises a portion extending laterally beyond device 125's *sidewall* (*across*). *EX1003*, ¶206; *Regents of Univ. of California v. Satco Prods., Inc.*, No. 2023-1356, 2024 WL 4972639 (Fed. Cir. Dec. 4, 2024) ("[P]atent drawings may be useful in shedding light about the general shapes and relative sizes of elements of the claimed invention, as well as their spatial relations to one another."); *Mahle Behr Charleston Inc. v. Catalano*, IPR2023-00861, Paper 15, at 6-7 (PTAB Apr. 5, 2024) (Director Review).



EX1004, FIG. 3 (excerpt).

During original prosecution, PO provided an annotated figure arguing specification support for this limitation, similar to Sundaram's orange-highlighted pad relative to device 125.



EX1002, 537; *EX1003*, ¶207.

D. Claim 4

1. 4(a)

Sundaram teaches "a second electronic device 130…attached to the second side 120 of the interposer 105," i.e., a *second semiconductor chip over said first interconnection scheme*:

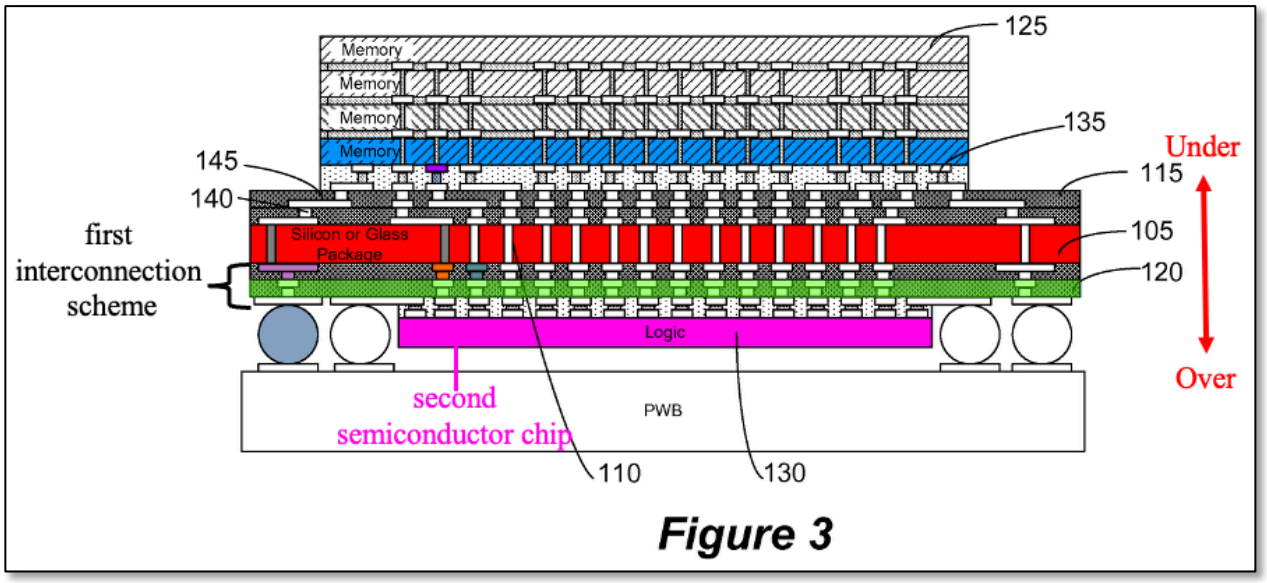
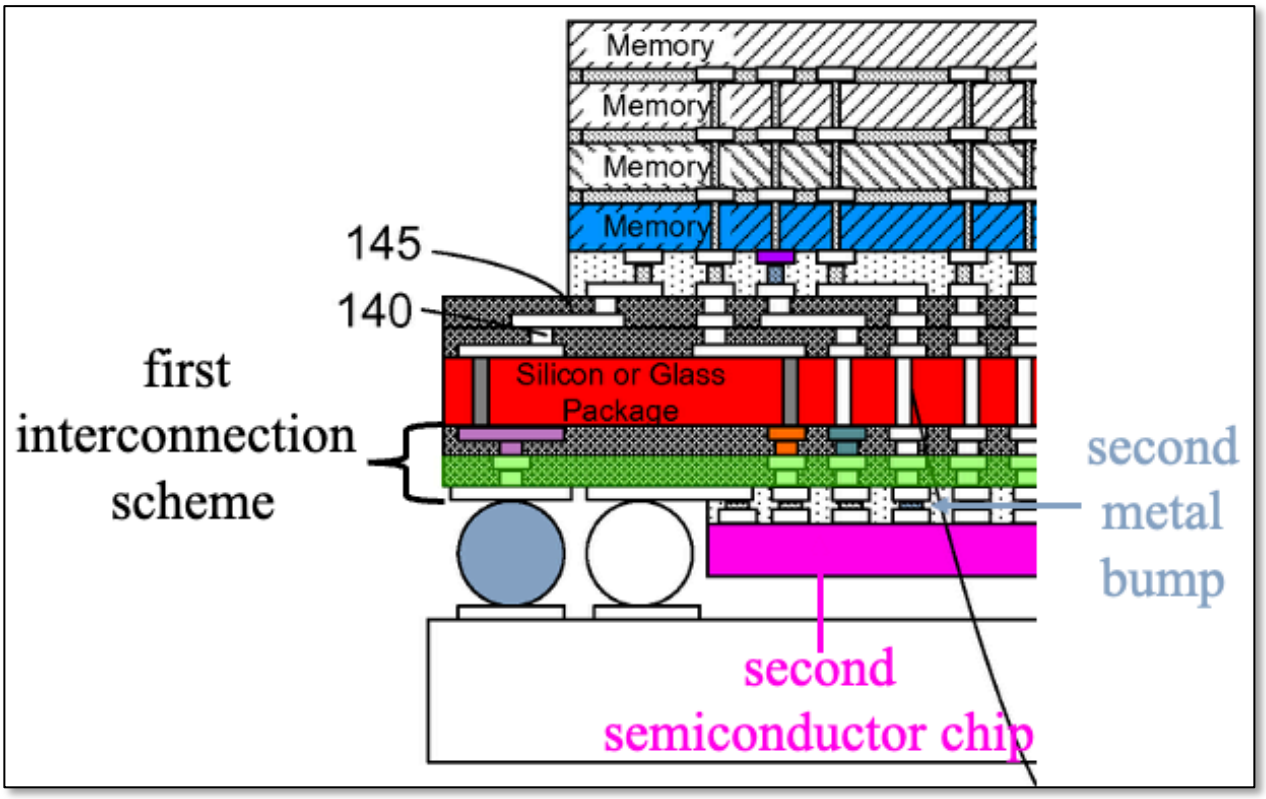


Figure 3

EX1004, FIG. 3, 6:34-36; *EX1003*, ¶208.

2. 4(b)

Device 130 *comprises a second metal bump between* it and *said first interconnection scheme*. *EX1004*, 6:29-33 ("The die pads 135 that are formed on…the interposer 105 can electrically connect devices using…copper **bumps**[.]").



EX1004, FIG. 3 (excerpt); *EX1003*, ¶209.

E. Claim 5

a) Lin-191's Teachings

Lin-191 teaches semiconductor chips as "system-on chip[s] (SOC) including **a graphics-processing-unit (GPU) circuit block**…**and a central-processing-unit (CPU) circuit block**…" *EX1005*, [0106].

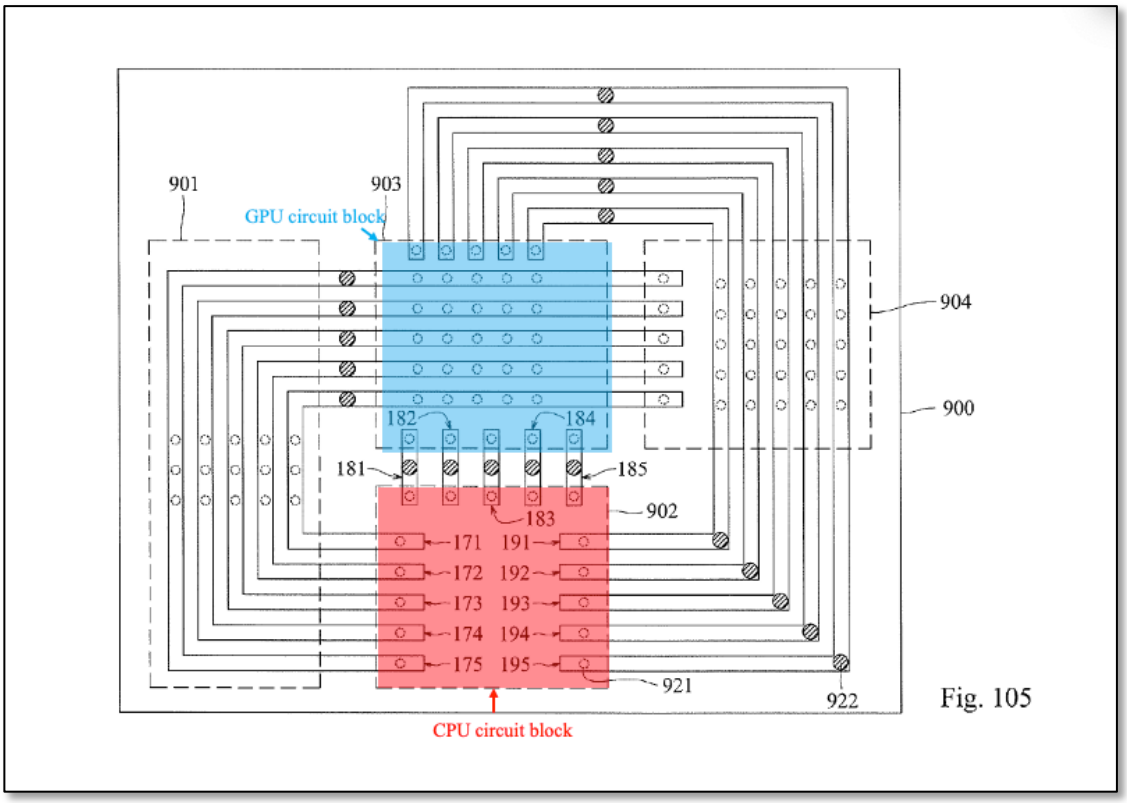


Fig. 105

EX1005, FIG. 105, [0541], [0543]; *EX1003*, ¶210.

b) MTC

A POSITA would have been motivated and found obvious to modify device 125 per Lin-191 to include *a CPU circuit block and a GPU circuit block*. *EX1003*, ¶211. While Sundaram's FIG. 3 depicts device 125 as stacked memory, Sundaram teaches device 125 can be "other electronic devices[.]" *EX1004*, 6:37-43; *EX1003*, ¶211. Indeed, Sundaram discloses "mobile phone applications, including video streaming, 3D graphics, camera-functions, and gaming" and contemplates "high power logic component[s]" for device 125's side of interposer 105:

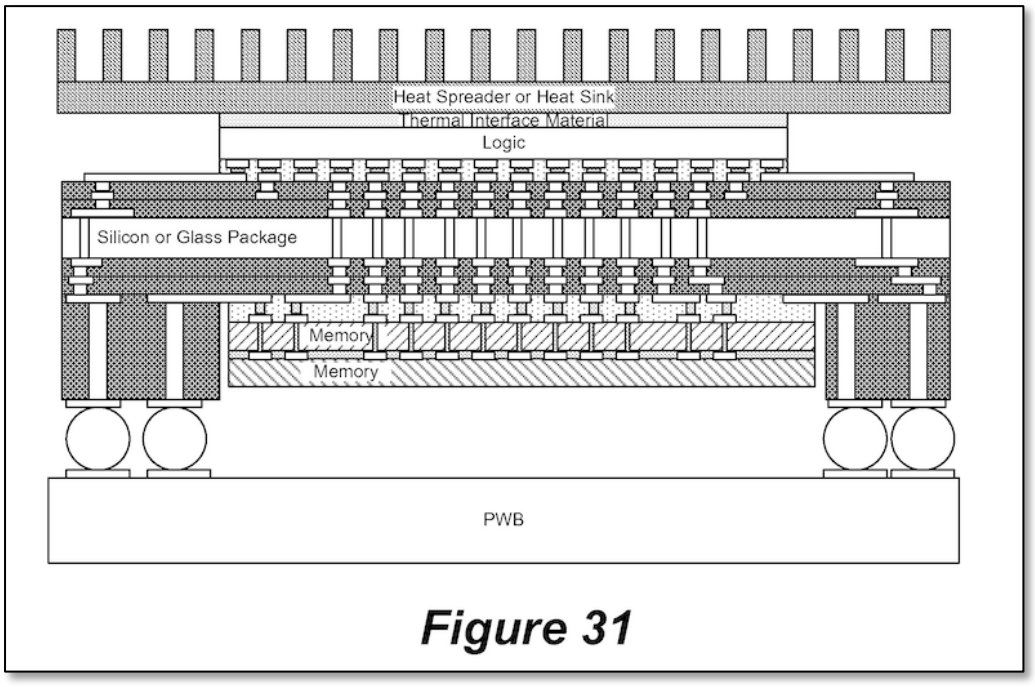


Figure 31

EX1004, 1:20-25, 6:19-22, FIG. 31. The combination would have predictably improved Sundaram's *chip package* by providing it with increased capabilities, i.e., to carry out the functions of both a CPU and a GPU. *EX1003*, ¶211.

The combination is the application of a known technique (a chip with GPU and CPU circuit blocks) to a known device (Sundaram's *chip package*) yielding the predictable results of device 125 having both CPU and GPU circuit blocks. Further, the modification is an implementation detail a POSITA would have found obvious given Sundaram's teachings of phone applications. *EX1003*, ¶212.

SoCs that included CPUs and GPUs were well-known before the time of the '768 Patent, leading to a REOS. *EX1003*, ¶213.

F. Claim 6

1. 6(a)

Sundaram illustrates *a second metal pad on a top surface* and a *third metal pad on a bottom surface* of device 125 in FIGS. 3 and 32. Sundaram alone or Sundaram-Lin-191 teaches semiconductor chips with *metal pad[s]*. Section V.A.18.

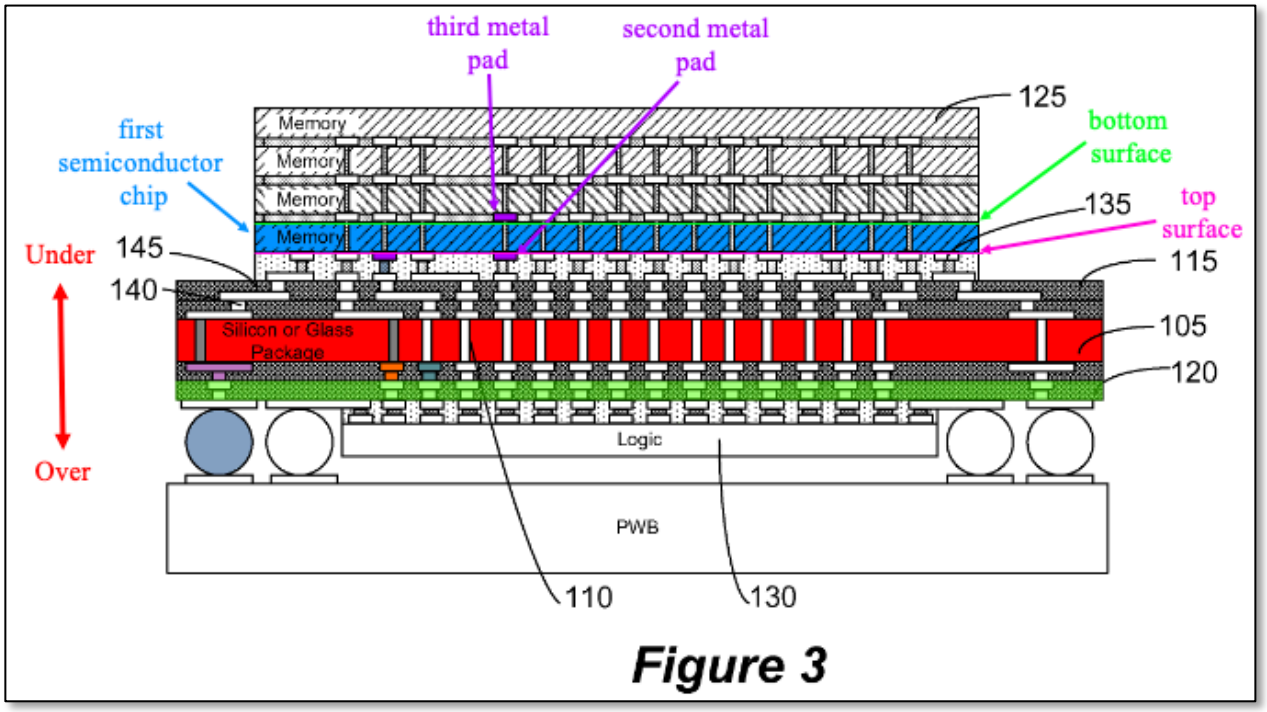


Figure 3

EX1004, FIG. 3.

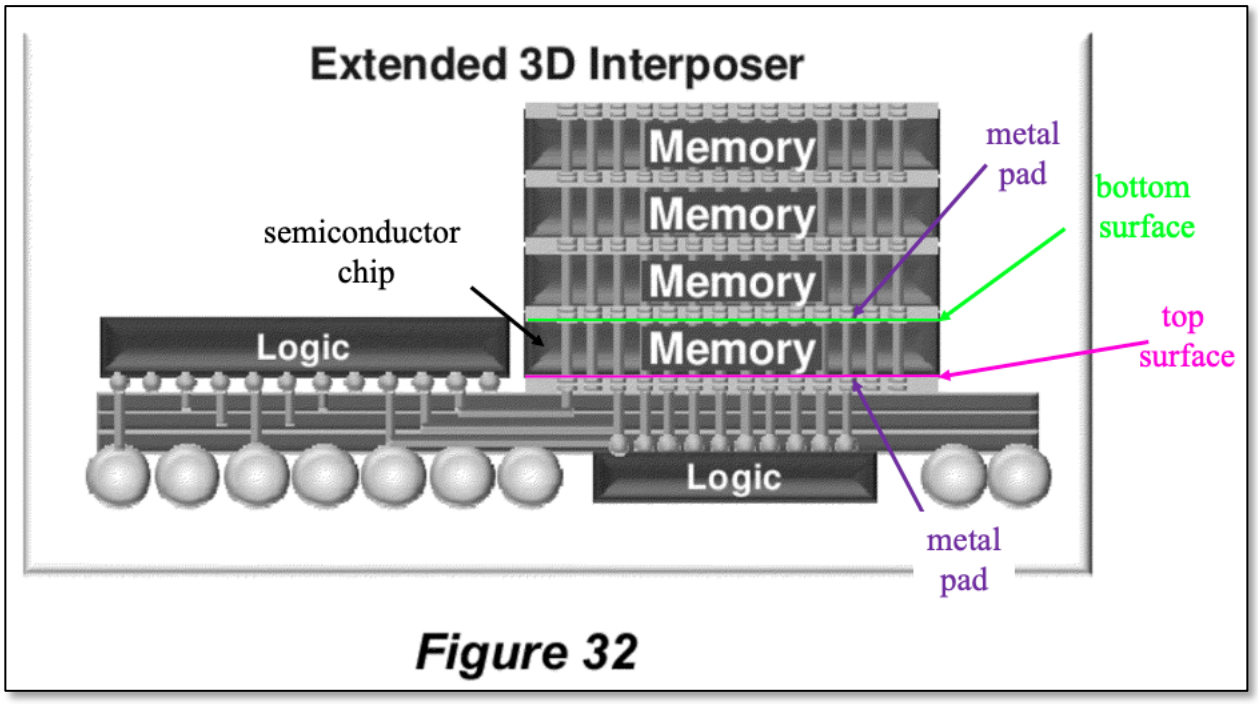


Figure 32

EX1004, FIG. 32. A POSITA would have found obvious, been motivated, and had a REOS in modifying FIG. 3's *first semiconductor chip* to have *metal* pads on both top and bottom surfaces, which would have been an obvious, ubiquitous implementation detail to connect the chips to other devices. *EX1003*, ¶¶214-216.

2. 6(b)

Sundaram depicts TSV (*through-silicon-via*) layers in FIGS. 3, 32 and teaches TSVs with "plate[d] copper," i.e., *TSV metal layers*. *EX1004*, 15:7-8. Sundaram's *second metal pad is connected to said third metal pad through a TSV metal layer*:

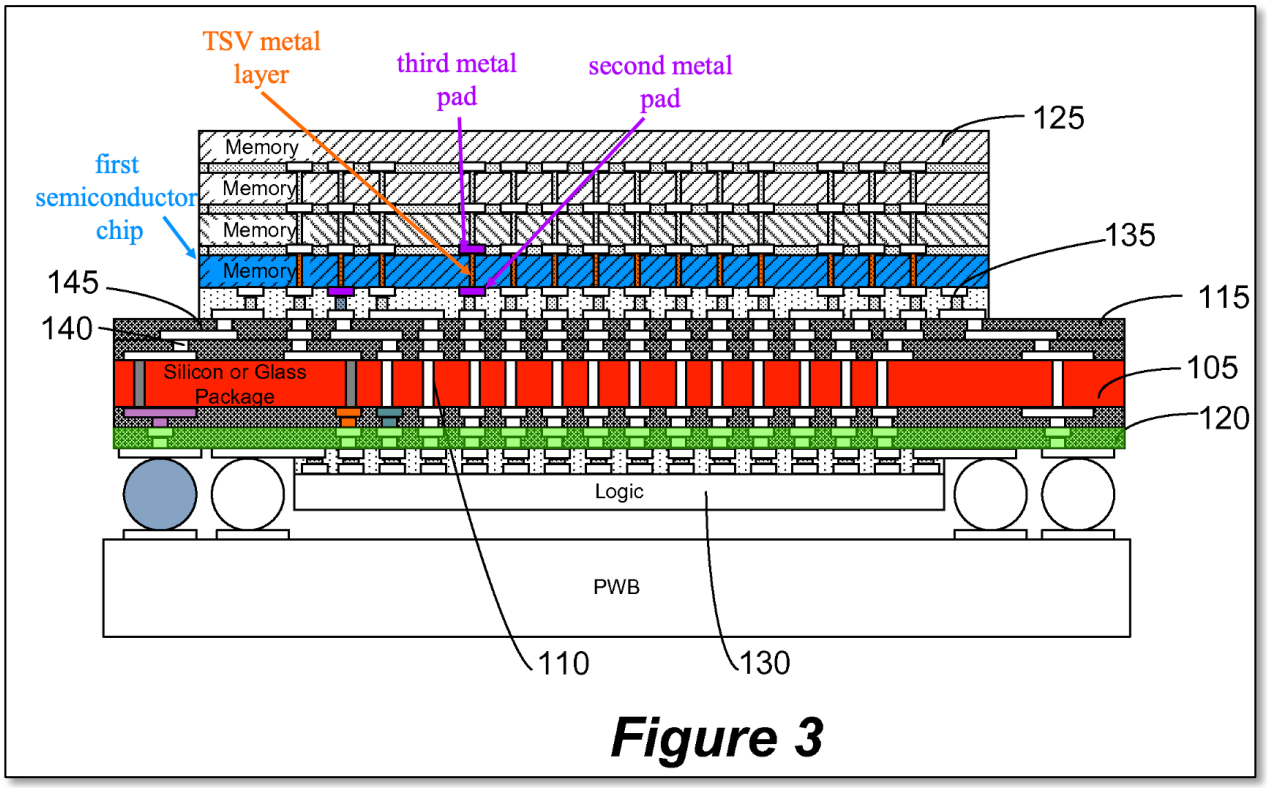


Figure 3

EX1004, FIG. 3.

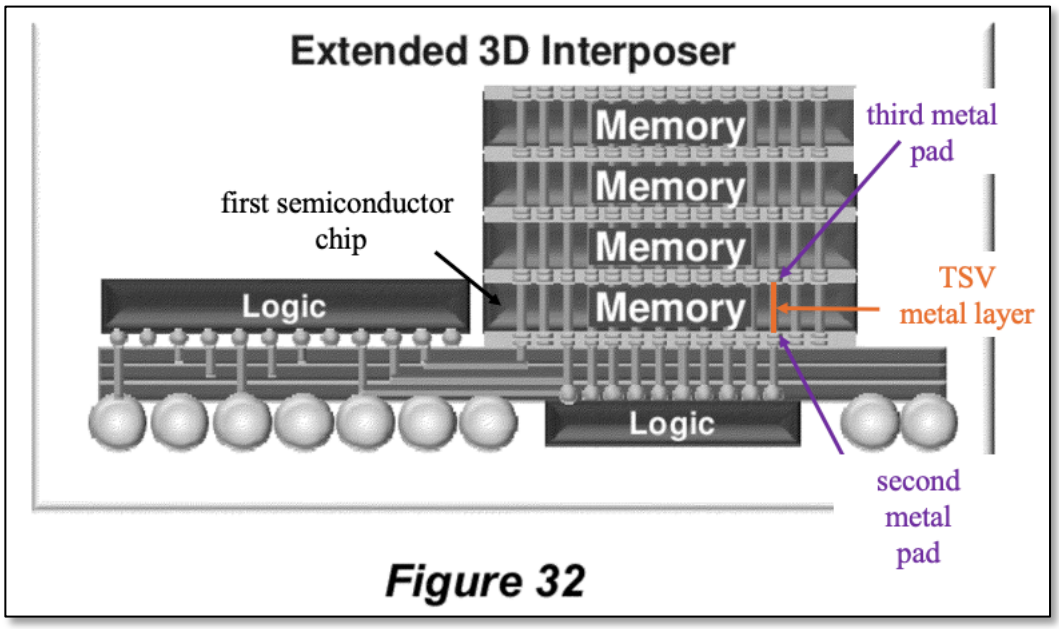


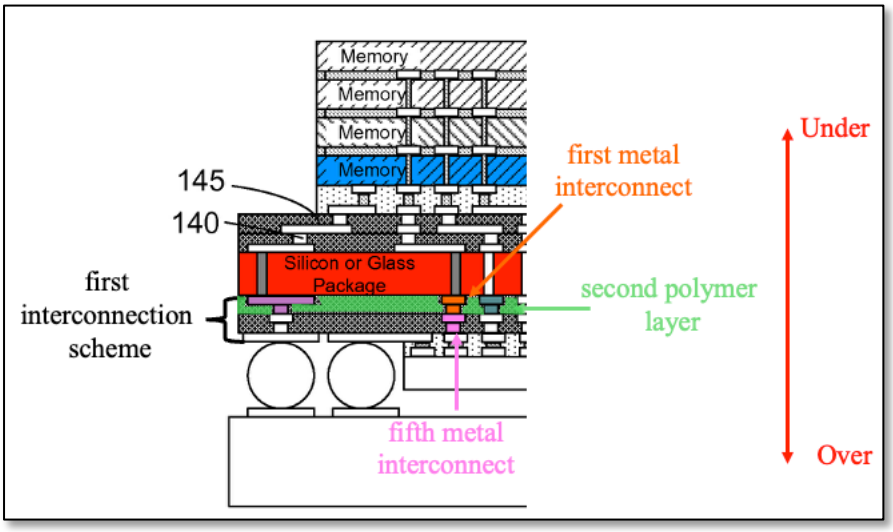
Figure 32

EX1004, FIG. 32; *EX1003*, ¶¶217-219.

G. Claim 7

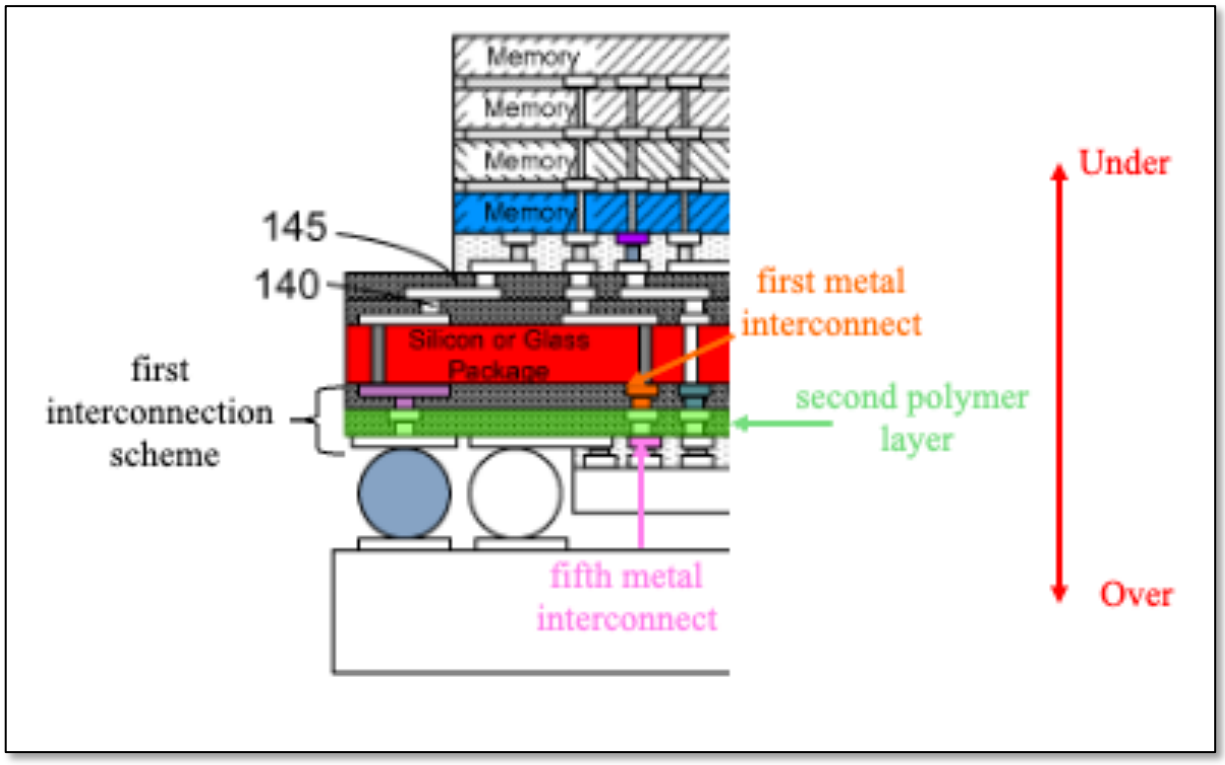
1. 7(a)

A blind via 140 and conductor trace 145 *over* the via 140 of the *first metal interconnect* (Section V.A.12) is a *fifth metal interconnect over said second polymer layer*:



EX1004, FIG. 3 (excerpt); *EX1003*, ¶220.

Alternatively, die pad 135 is a *fifth metal interconnect over said first metal interconnect and said second polymer layer*.

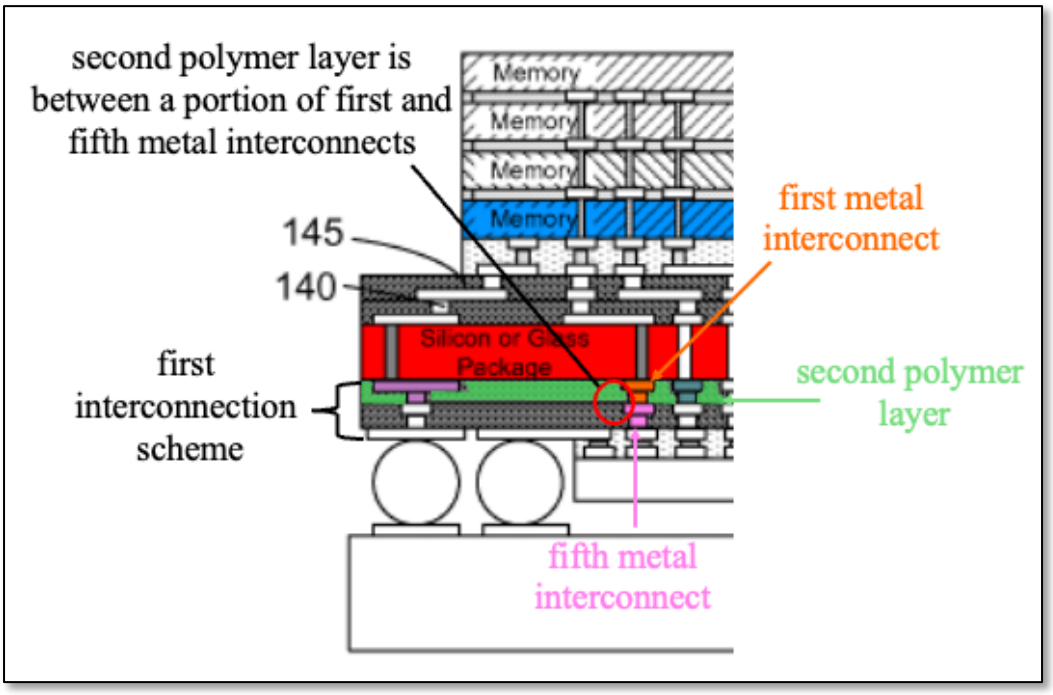


EX1004, FIG. 3 (excerpt); *EX1003*, ¶221.

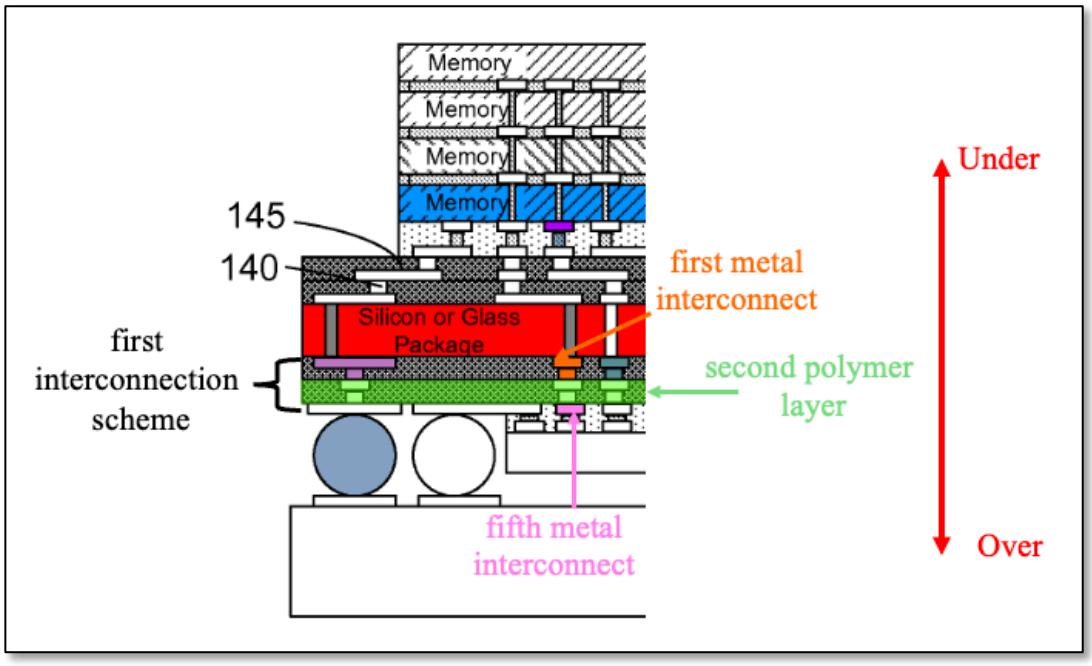
2. 7(b)

Under either mapping of the *fifth metal interconnect* and *second polymer layer*, Sundaram's *second polymer layer*[7] is *between said first and fifth metal interconnects*:

[7] Petitioners interpret Claim 7(b)'s *second polymer* as referring to Claim 1(d)(i)'s *second polymer layer*.



EX1004, FIG. 3 (excerpt).

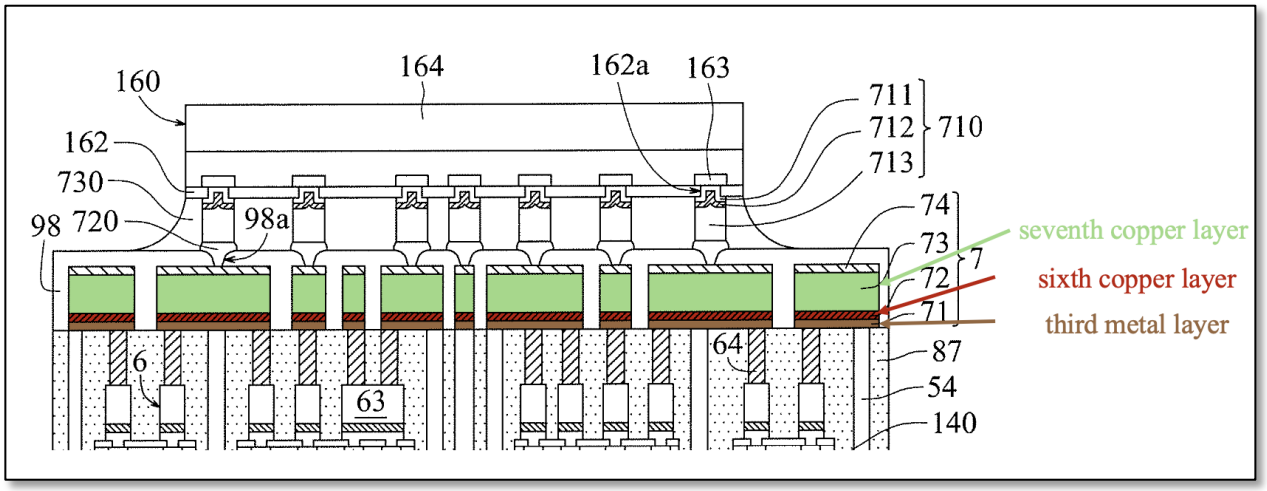


EX1004, FIG. 3 (excerpt); *EX1003*, ¶¶222-223.

3. 7(c)

a) Lin-191's Teachings

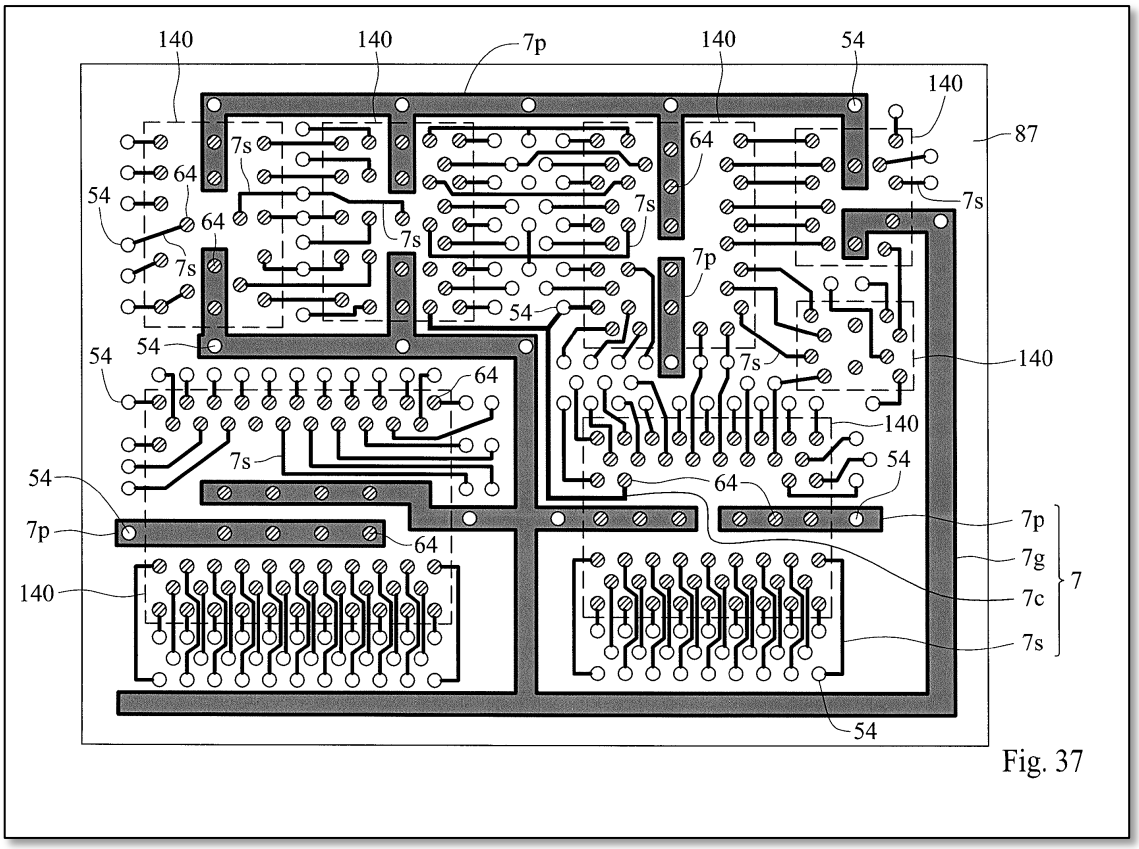
Lin-191 teaches a multilayered metal interconnect with two copper layers and a metal layer, i.e., a "patterned metal layer 7" having "adhesion layer 71, the seed layer 72," and "metal layer 73." *EX1005,* [0379]. Layer 7 interconnects metal bumps 64 to other structures in Lin-191's package and, therefore, is a *metal interconnect*. *EX1005*, [0379]. Adhesion layer 71 is a *metal* (e.g., titanium or nickel) and is thus a *third metal layer*. *EX1005,* [0260]-[0264]. Seed layer 72 is "a copper layer" on adhesion layer 71, i.e., a *sixth copper layer on said third metal layer*. *EX1005*, [0261]-[0264]. Metal layer 73 is "a copper layer…on the seed layer 72," i.e., a *seventh copper layer on said sixth copper layer*. *EX1005*, [0420].



EX1005, FIG. 72 (excerpt); *EX1003*, ¶224.

b) MTC

A POSITA would have been motivated and found obvious to apply Lin-191's teachings of patterned metal layer 7 to Sundaram's via 140 and trace 145 or die pad 135 forming the *fifth metal interconnect*. *EX1003*, ¶¶225-229. Lin-191's FIG. 37 illustrates "a schematic top perspective view of the patterned metal layer 7," and, as shown, layer 7 makes lateral electrical connections (e.g., from bump 54 to bump 64) such that a POSITA would have understood layer 7 as being an RDL, like Sundaram's RDL.



EX1005, FIG. 37, [0017], [0272-0273]; *EX1003*, ¶226.

The modification would have advantageously provided a low resistance current path for signals traveling between the *first metal interconnect* and *fifth metal interconnect*. *EX1003*, ¶¶227-228. Desirably, copper (layers 72, 73) has low resistivity, high conductivity, and high immunity to electromigration. *Id.* The modification would have advantageously reduced delamination and copper diffusion, both which negatively impact electrical reliability and ruggedness of the chip package. *EX1003*, ¶229.

The modification is the application of a known technique (Lin-191's multi-layer metal interconnect) to a known component (Sundaram's *fifth metal interconnect*) ready for improvement to yield the predictable result of Sundaram's *fifth metal interconnect* comprising the layers of Lin-191's layer 7. *EX1003*, ¶230. There would have been a REOS as layered interconnects were commonplace and because Lin-191's layer 7 is an RDL, and Sundaram's similar RDL is being modified per layer 7's teachings. *Id*.

H. Claim 8

Sundaram teaches "polymer-metal redistribution layers" are "deposited **on the first side 115**…of the interposer 105" and that die pads 135 are formed on first side 115. *EX1004*, 6:62-67; 6:29-31. The RDL and die pads 135 on first side 115 form *a second interconnection scheme under said first polymer layer and on said*

second surface because the RDL "connect[s]" the "electronic devices" 125 and 130. *Id*.

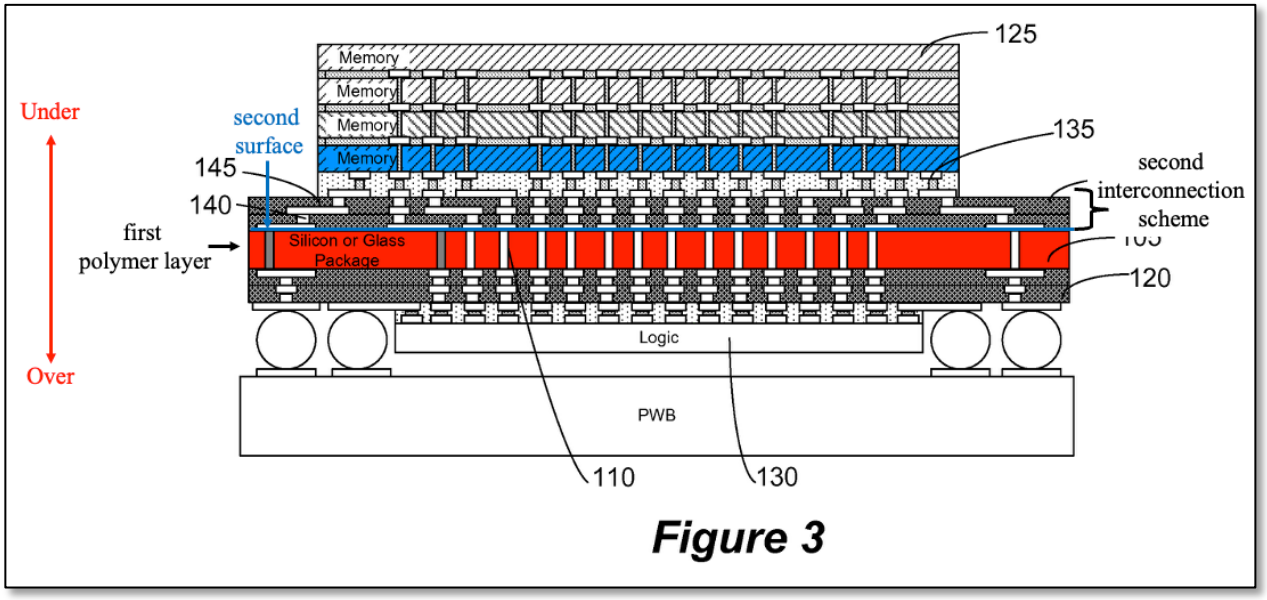
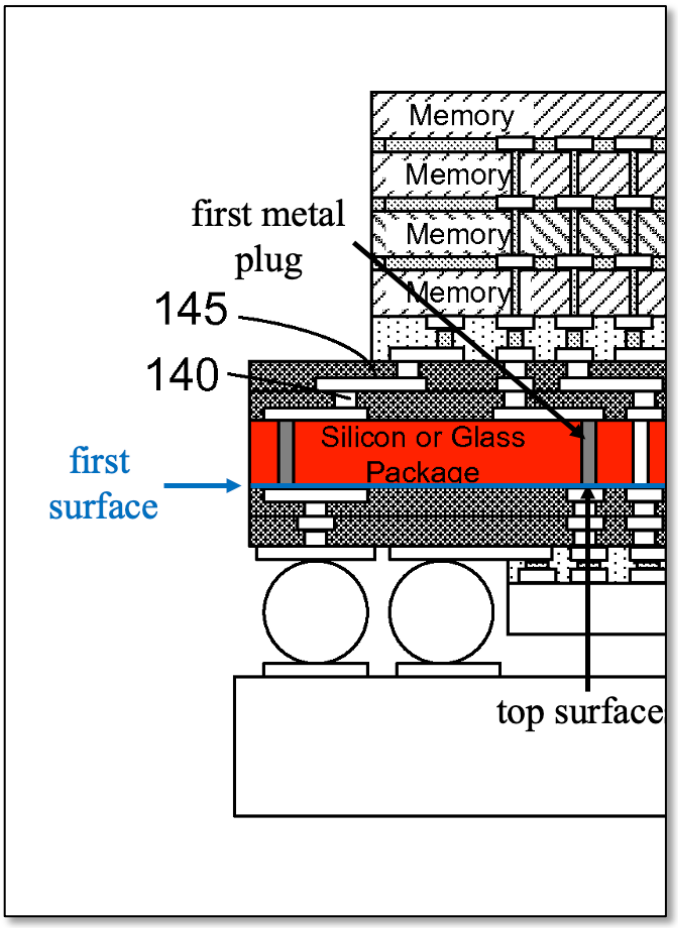


Figure 3

EX1004, FIG. 3; *EX1003*, ¶231.

I. Claim 9

Through vias 110 (*metal plug[s]*) "extend from the first side 115 to the second side 120" such that *a top surface* of the *first metal plug* is *coplanar with said first surface* (side 120). *EX1004*, 6:6-9.



EX1004, FIG. 3 (excerpt); *EX1003*, ¶232.

J. Claim 10

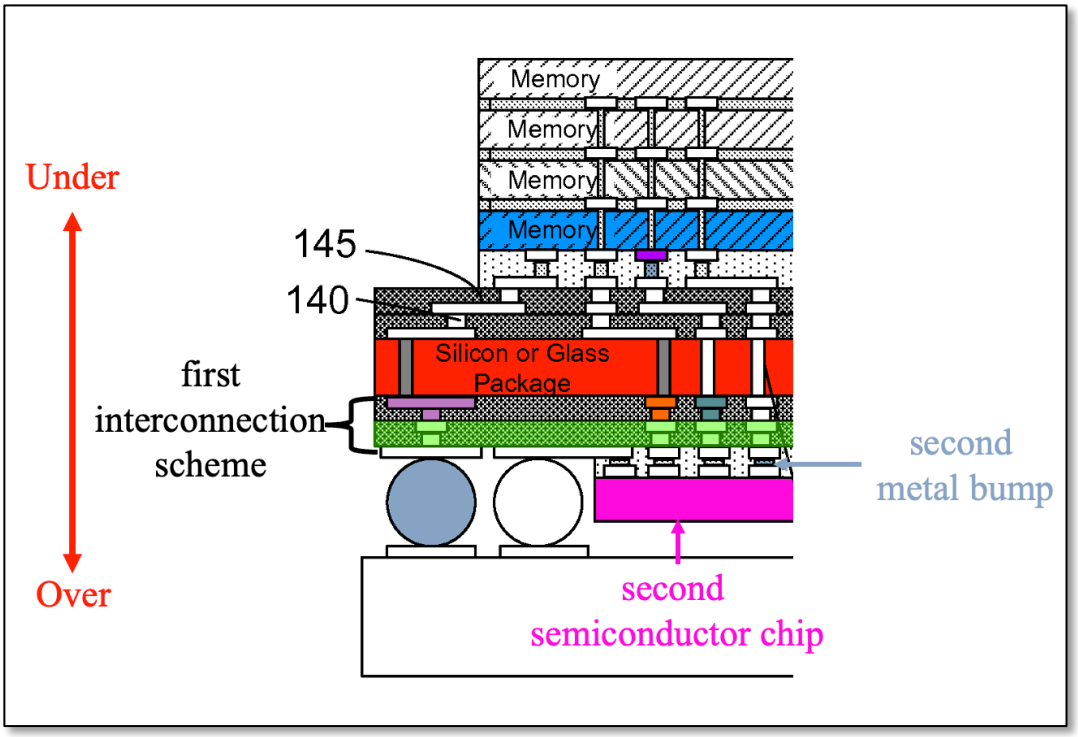
Lin-191 teaches "**aluminum**" metal pads 163. *EX1005*, [0384]. Aluminum was a well-known and widely used material for forming contact pads in chips, as it is compatible with established bond wire attachment methods, low cost, and consistent with legacy materials used in semiconductor processing, motivating the combination. *EX1003*, ¶¶233-234. Aluminum would have been a cost-effective and commonly-used choice to form Sundaram's pad and had a REOS. *Id*. The

modification is combination of prior art elements according to known methods to yield predictable results. *Id*.

K. Claim 11

1. 11(a)

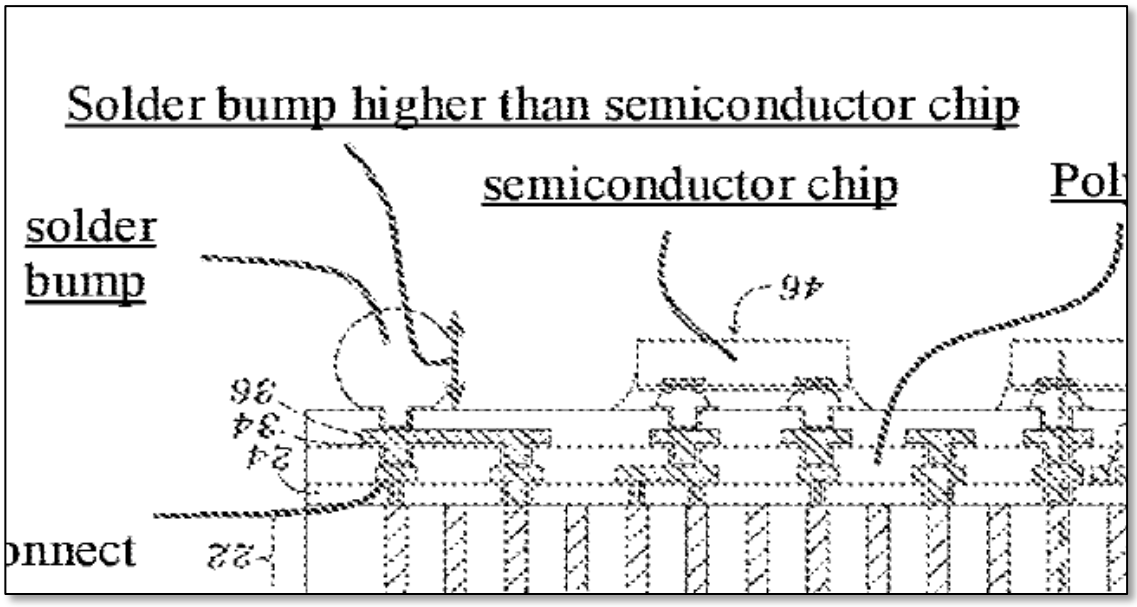
Section V.D. Device 130 *is over said first interconnection scheme and connected* thereto *through a second metal bump*.



EX1004, FIG. 3 (excerpt), 6:29-33; *EX1003*, ¶¶235-236.

2. 11(b)

During original prosecution, PO filed an Amendment with an annotated figure arguing specification support for 11(b)'s claim language:



EX1002, 400; *EX1003*, ¶237.

Sundaram's *second polymer layer* includes at least the portion described at Claim 1(d)(i) and further includes the portion highlighted below. Section V.A.12. Shown in FIG. 3, device 130 *has a height [that] is between a backside surface of* device 130 *and a top surface of said second polymer layer*, which is *smaller than thickness* of Sundaram's *first metal bump*.

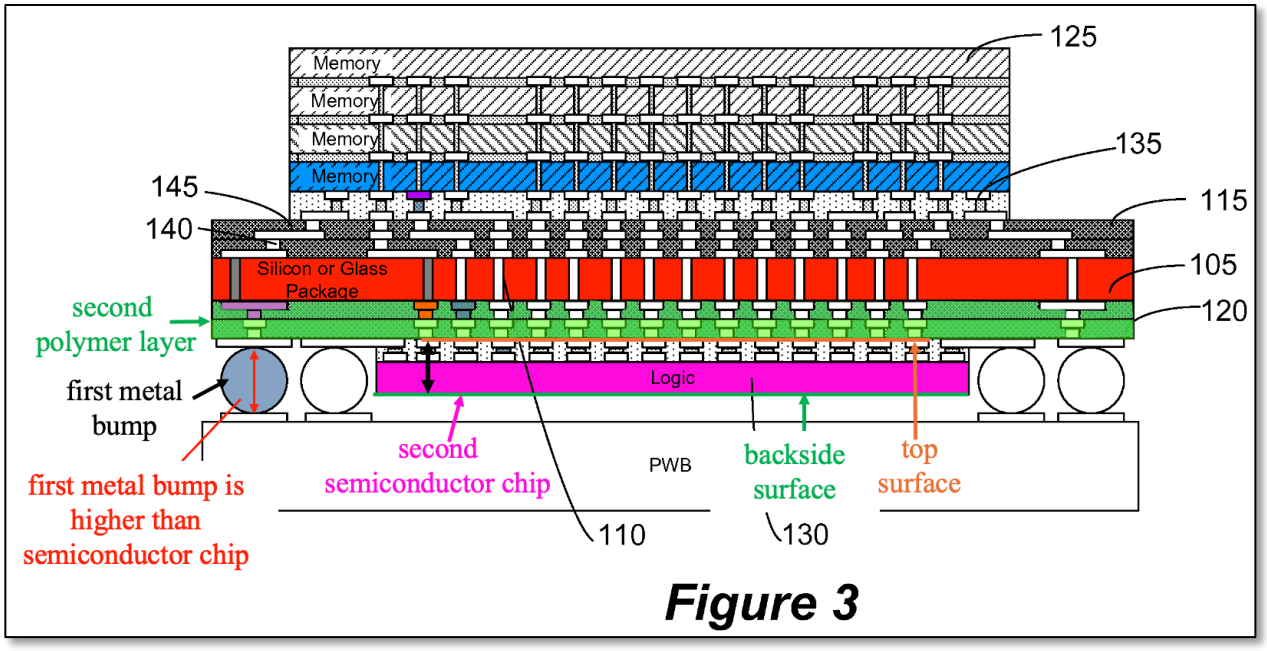


Figure 3

EX1004, FIG. 3; *EX1003*, ¶238; Section V.C (relevant caselaw).

Alternatively, Sundaram's *second polymer layer* is as annotated below, which also meets the claim limitation.

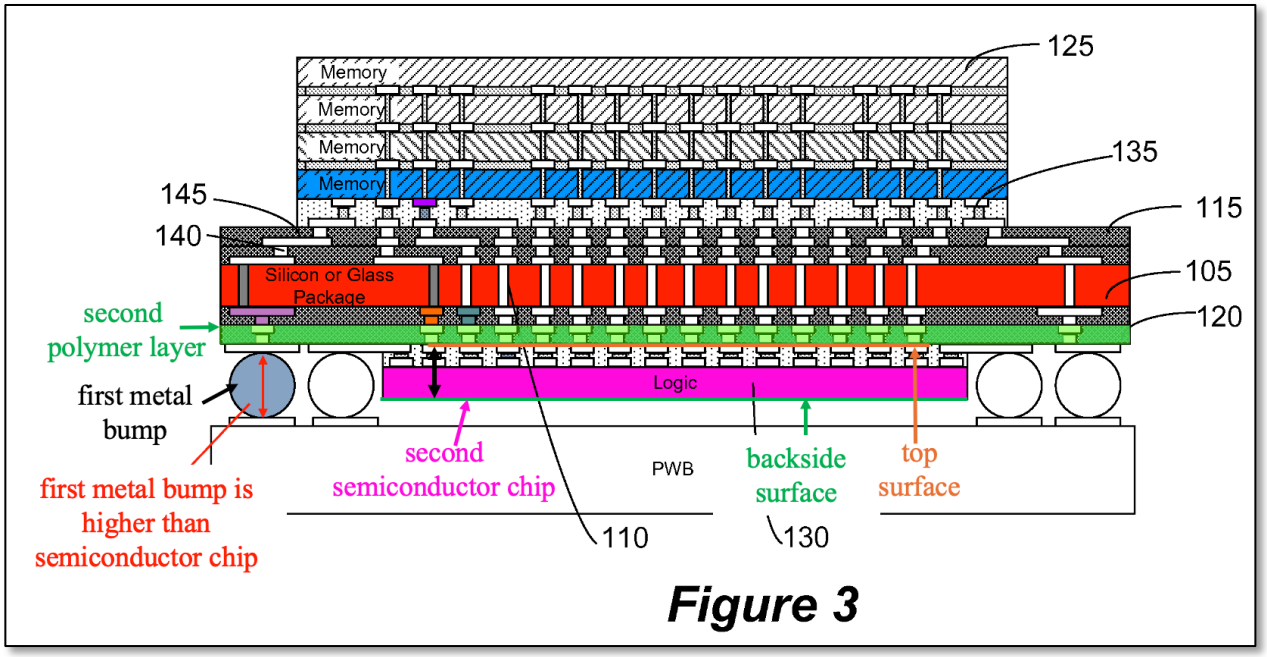


Figure 3

EX1004, FIG. 3; *EX1003*, ¶239.

L. Claim 12

1. 12(a)

Another chip in Sundaram's chip stack is *a second semiconductor chip under said first semiconductor chip*.

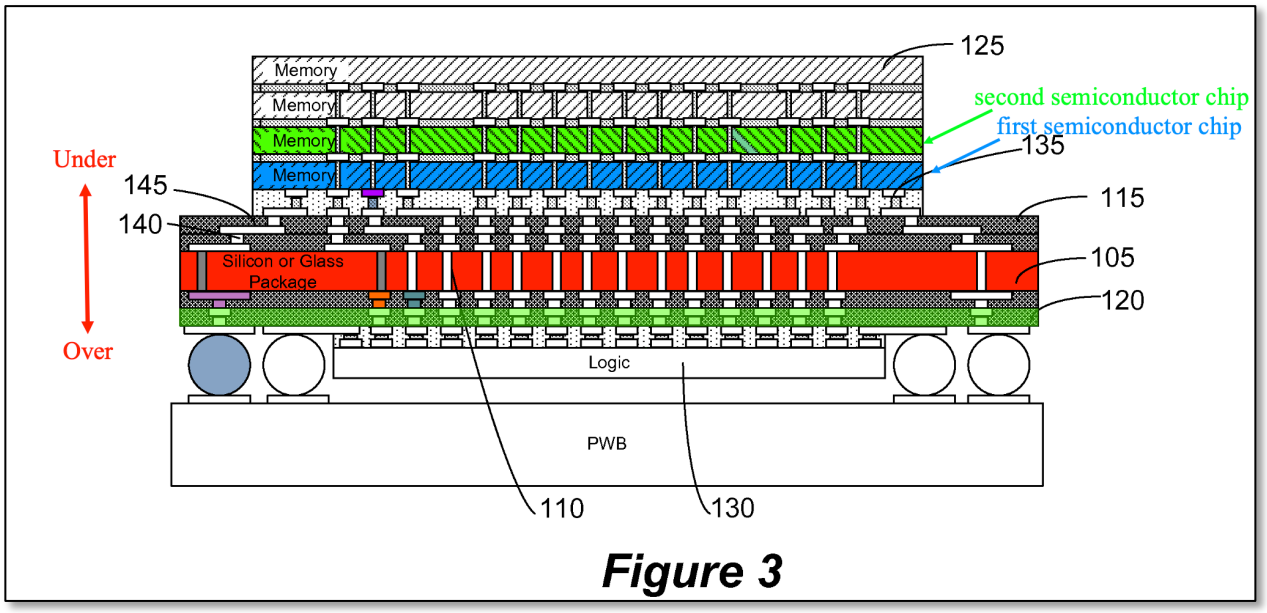


Figure 3

EX1004, FIG. 3; *EX1003*, ¶240.

2. 12(b)

FIG. 32 depicts a *second metal pad* of a *first semiconductor chip connected to a third metal pad* of a *second semiconductor chip*.

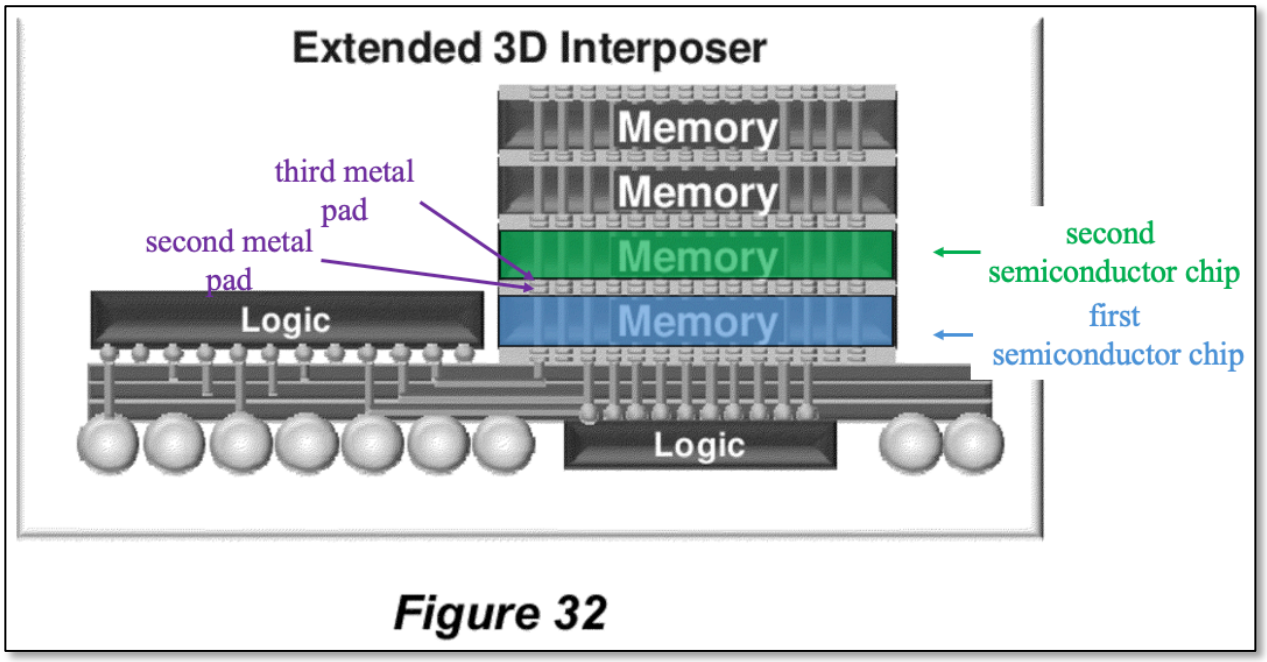


Figure 32

EX1004, FIG. 32. A POSITA would have been motivated, found obvious, and had a REOS in modifying Sundaram's FIG. 3 embodiment so that each chip has top and bottom pads connected to one another as each chip must include pads on its surface to provide connection to other electrical components in the chip package. *EX1003*, ¶¶241-242. The modification would have been an obvious, ubiquitous implementation detail, so that FIG. 3's *first semiconductor chip* has a *second metal pad connected to a third metal pad of* FIG. 3's *second semiconductor chip*. *Id*.

Sundaram teaches "die pads 135…can electrically connect devices using **solder**, copper bumps with **solder** caps…." *EX1004*, 6:29-34. A POSITA would have understood chip pads on devices 125, 130 likewise electrically connect using solder. *EX1003*, ¶243. A POSITA would have found obvious, been motivated, and had a REOS in combining Sundaram's internal embodiments to *connect[]* Sundaram-Lin-191's *second metal pad* and *third metal pad through a solder layer between said first and second semiconductor chips*, teaching Claim 12(b). *EX1003*, ¶¶244-245. The modification is the combination of known prior art elements (solder connections for chip pads) according to known methods to yield predictable results and would have advantageously provided Sundaram with a good electromechanical connection between chips, which would have had a REOS because this was a common method of connecting chips. *EX1003*, ¶246.

M. Claim 13

1. 13(a)

Section V.L.1.

2. 13(b)

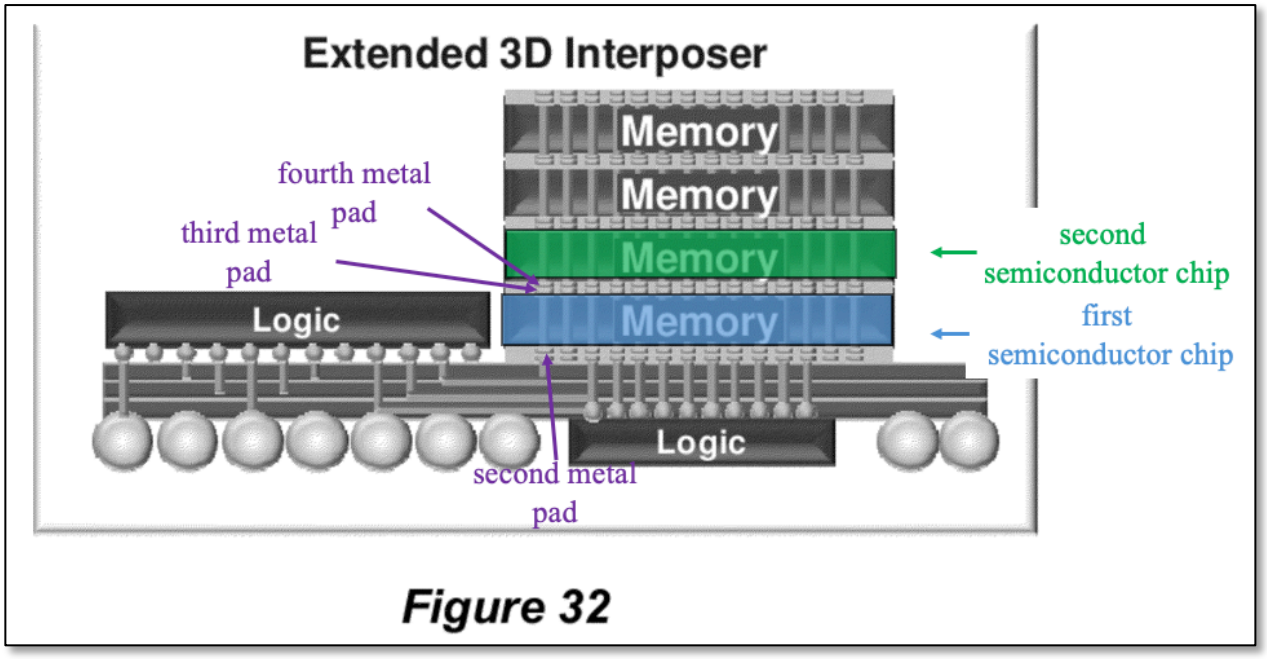
Section V.F.1.

3. 13(c)

Section V.F.2, reciting corresponding limitations. *EX1003*, ¶249.

4. 13(d)

FIG. 32 teaches a *third metal pad connected to a fourth metal pad of said second semiconductor chip*. Section V.A.18 (*metal pad* teachings).

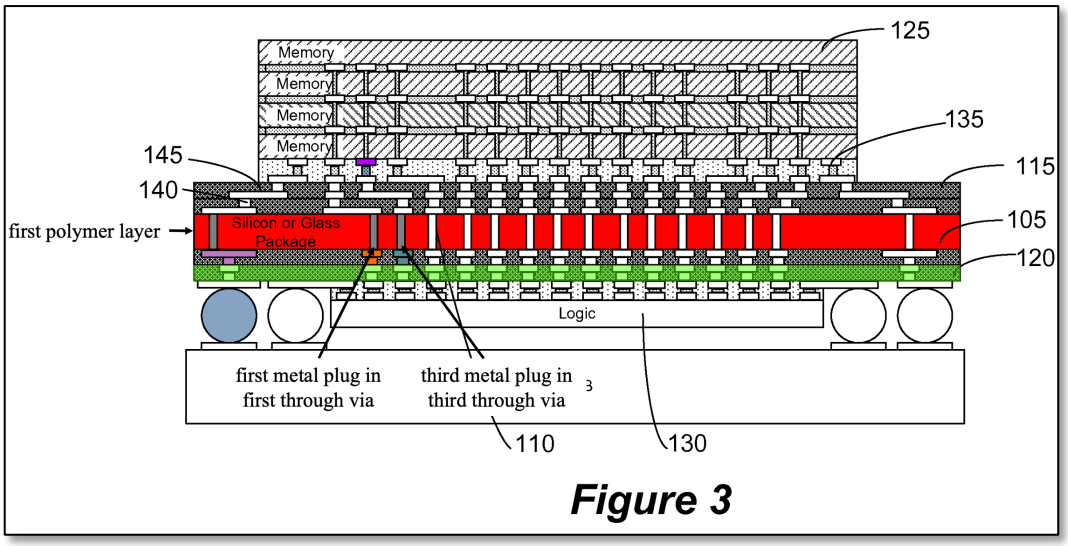


EX1004, FIG. 32.

A POSITA would have found obvious, been motivated, and had a REOS in combining Sundaram's internal embodiments so that the *first semiconductor chip* had *second* and *third metal pad[s]*, with the *third metal pad connected to a fourth metal pad* of the *second semiconductor chip* to interconnect the two chips. *EX1003*, ¶¶250-251; Section V.L.2.

N. Claim 14

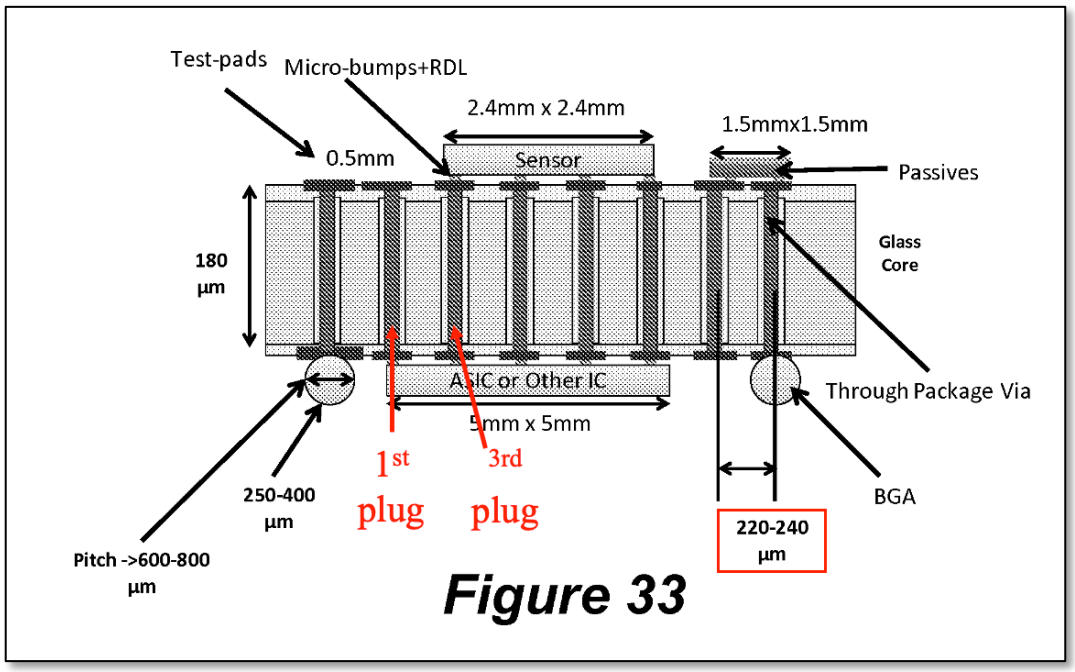
Sundaram teaches or renders obvious a *third metal plug vertically in a third through via in said first polymer layer*:



EX1004, FIG. 3.

FIG. 33 teaches through vias having a pitch between "220-240 mm," falling within the claimed range of *between 200 and 1000 micrometers*. *EX1004*, FIG. 33. *EX1003*, ¶¶252-254. FIG. 33 is a chip package for "a digital camera for cell phones"

with a "through-via interconnect density" that is "substantially the same" as devices 125, 130. *EX1004*, 6:42-50.



EX1004, FIG. 33.

The '768 Patent does not ascribe any criticality to the claimed range of between 200 and 1000 micrometers. *EX1001*, 6:7-15; Section V.A.4 (supporting caselaw); *EX1003*, ¶255.

a) MTC Sundaram's Embodiments

A POSITA would have found obvious and been motivated to modify the pitch of through vias 110 per FIG. 33's teachings. *EX1003*, ¶256. The modification is expressly motivated by Sundaram because FIG. 33 enables high bandwidth speeds between "an image sensor chip" and an "Asic chip" in a "digital camera for cell phones." *EX1004*, 6:42-45; *EX1003*, ¶256.

The combination is the application of a known technique (FIG. 33's *pitch*) to a known device (FIG. 3's *chip package*) ready for improvement to yield predictable results. *EX1003*, ¶256. A POSITA would have a REOS at least because the modification would have been simple and straightforward as methods of controlling pitch were well-known. *Id*.

O. Claim 15

Sundaram teaches or renders obvious Claim 15. Sundaram's interposer has a thickness "about 20 to about 200 micrometers." *EX1004*, 2:22-25; Section V.A.4 (supporting caselaw); *EX1003*, ¶¶257-258; (citing *EX1002*, 535-537 opining no criticality of claimed plug thickness because Applicant argued plug thickness was the same as the substrate's thickness). Through vias 110 "extend[] from the first side 115 to the second side 120 of interposer 105" such that the thickness of the through via (*first metal plug*) is equal to the thickness of the interposer, i.e., *between 100 and 300 micrometers*. *EX1004*, 6:6-9.

P. Claim 20

Sections V.A.5, VI.A.

VI. GROUND 1B: CLAIMS 16-19, 21-28 ARE OBVIOUS OVER SUNDARAM AND LIN-191

A. Claim 16

1. 16(Pre)

Section V.A.1.

2. 16(a)

Section V.A.2.

3. 16(a)(i)

Section V.A.3.

4. 16(a)(ii)

Section V.A.4.

5. 16(b)

Section V.A.6.

6. 16(b)(i)

Section V.A.7.

7. 16(c)

Section V.A.8.

8. 16(c)(i)

Section V.A.9.

9. 16(c)(ii)

Section V.A.10.

10. 16(d)

Section V.A.11.

11. 16(d)(i)

Section V.A.12. For Claim 16, Petitioners map a different via 140 and trace 145 as the *second metal interconnect*.

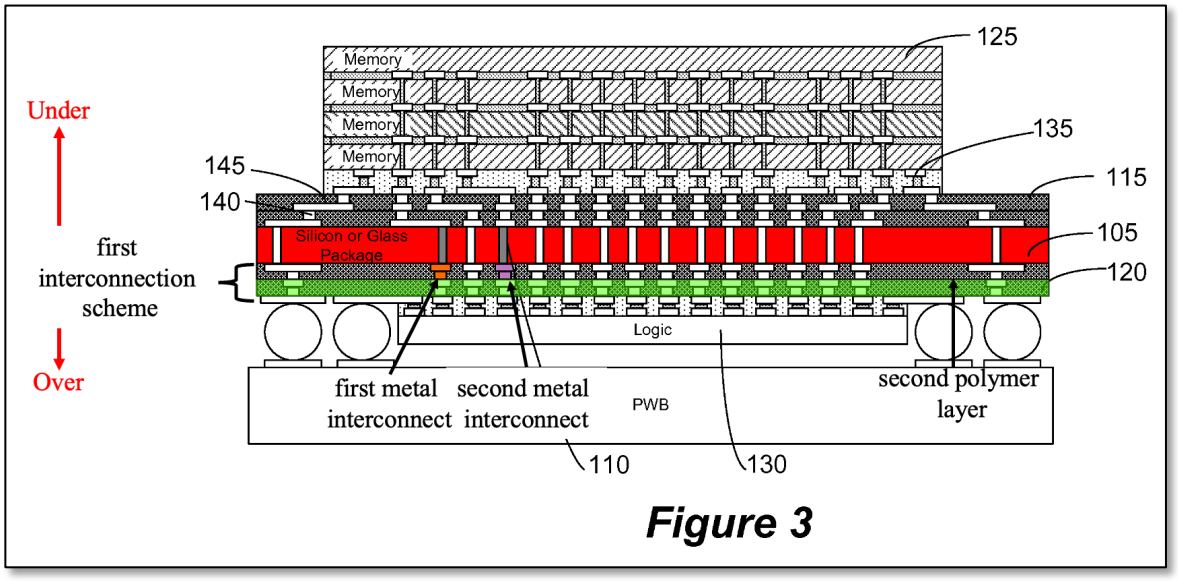


Figure 3

EX1004, FIG. 3; *EX1003*, ¶270.

12. 16(d)(ii)

Section V.A.13.

13. 16(d)(iii)

Section V.A.14.

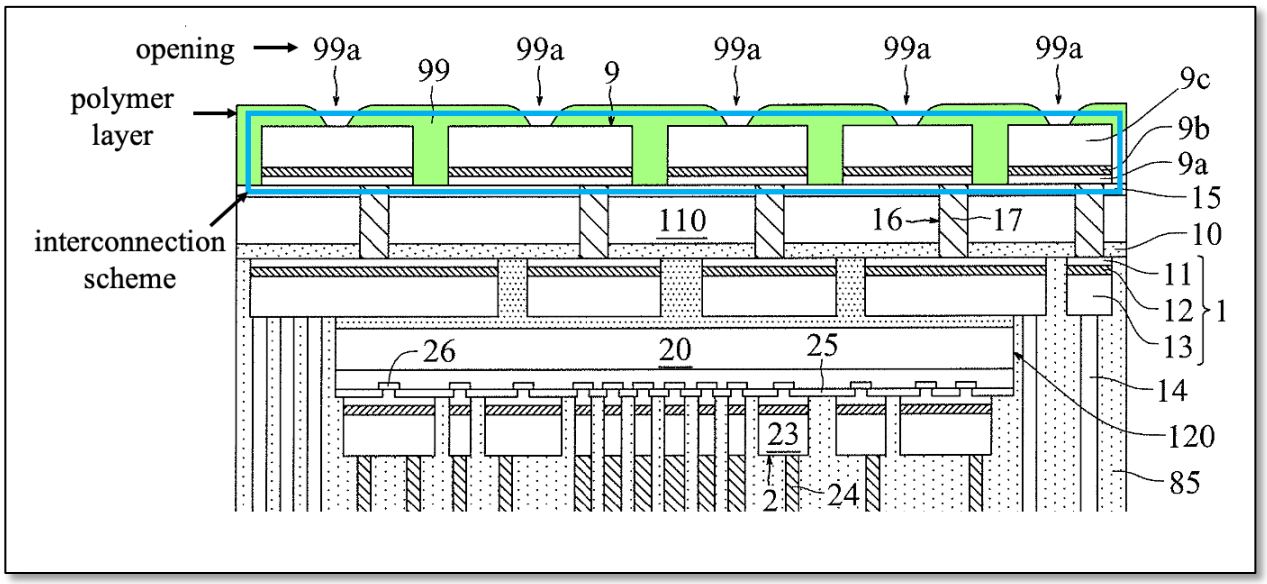
14. 16(e)

Section V.A.15.

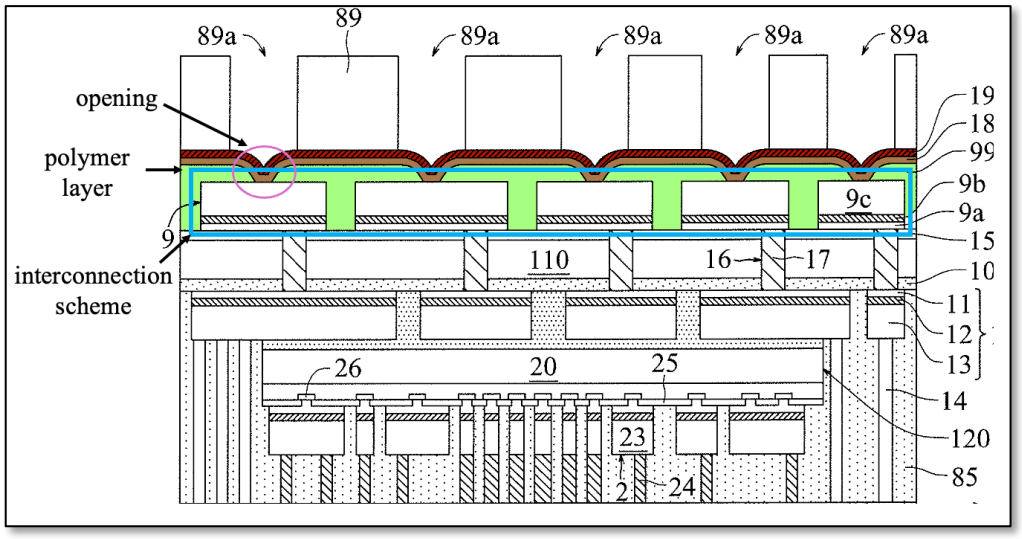
15. 16(e)(i)

a) Lin-191's Teachings

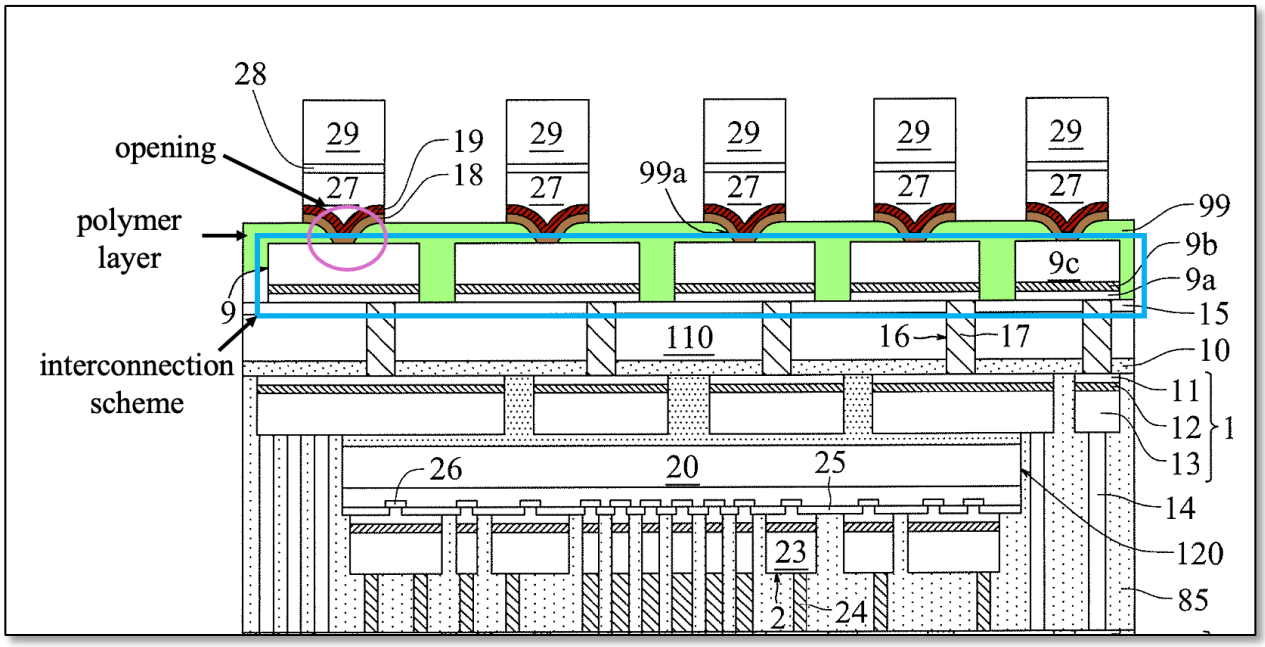
Lin-191 teaches *metal bump[s]* having UBM layers. *EX1005*, [0323]. The UBM layer is formed in "**openings 99a** in the polymer layer 99," one of which is *an opening in a polymer layer*. *EX1005*, [0306-0323]. The UBM layer is "formed on the contact points of the metal layer 9c" of patterned metal layer 9, which is an *interconnection scheme*, because like patterned metal layer 3, each layer 9 interconnects other components in Lin-191's package (Section V.A.14). Thus, Lin-191 teaches metal bumps connected to interconnection schemes through openings in a polymer layer. .



EX1005, FIG. 48 (excerpt). Shown in FIGS. 49 and 51, adhesion layer 18 and seed layer 19 are formed in openings 99a, followed by layers 27, 28 to complete the UBM layer. *EX1005*, [0306-0323].



EX1005, FIG. 49 (excerpt).



EX1005, FIG. 51 (excerpt); ¶¶274-276.

b) MTC

A POSITA would have been motivated and found obvious to modify Sundaram's copper bumps (*metal bumps*) to connect to the *interconnection scheme* via *a first opening in said second polymer layer* per Lin-191. *EX1003*, ¶¶277-278. The modification would have improved the mechanical connection between Sundaram's copper bumps and *interconnection scheme*. *Id*. Recessed pads, such as Lin-191's UBM layer, were known to avoid short circuiting issues. *EX1003*, ¶¶277-278; *see also EX1027*, [0036].

The combination is the application of a known technique (Lin-191's bumps in polymer layer openings) to a known device (Sundaram's copper bumps) to yield the predictable results of Sundaram's bumps being connected to the interconnection scheme via an opening in the RDL. *EX1003*, ¶278. Because Lin-191 teaches well-known manufacturing techniques for forming UBM layers already contemplated by Sundaram a POSITA would have had a REOS. *Compare EX1005*, [0306-0323] *with EX1004*, 14:52-24, 14:62-15:11; *EX1003*, ¶279. Furthermore, UBM layers were commonplace in chip packaging before the '768 Patent such that the modification would have been simple and straightforward, *EX1003*, ¶279.

16. 16(e)(ii)

Section V.A.16.

17. 16(f)

Sundaram teaches *a second metal bump over said first interconnection scheme*:

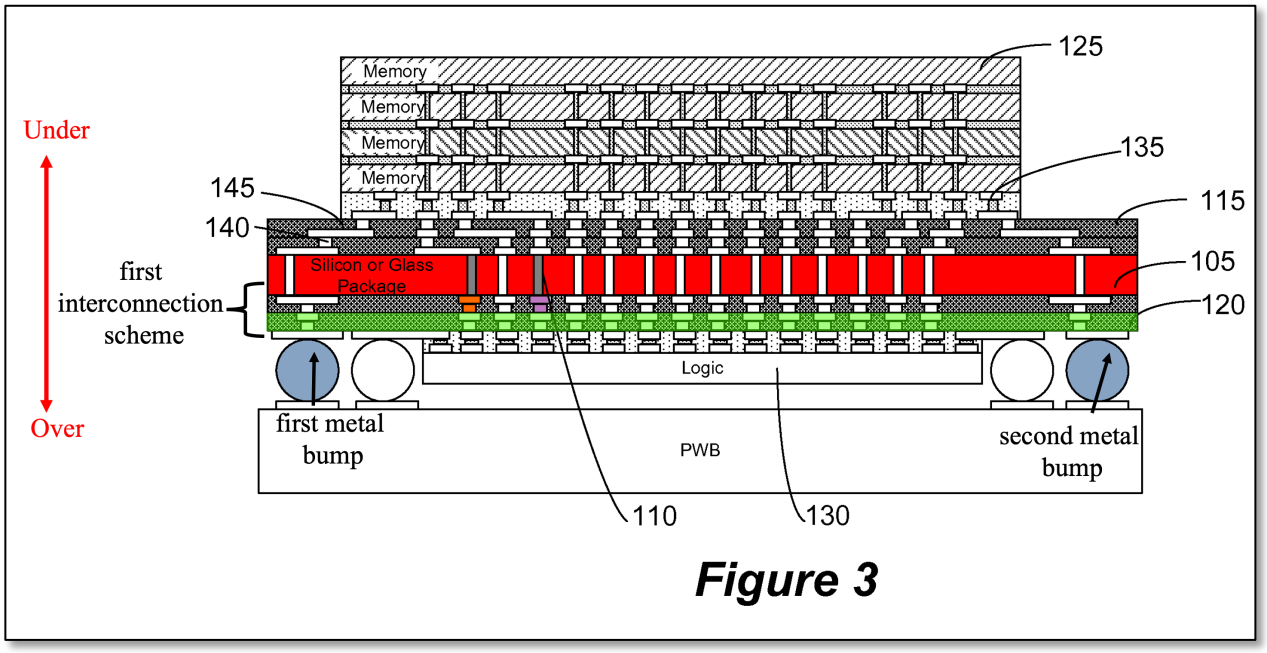


Figure 3

EX1004, FIG. 3; *EX1003*, ¶281.

18. 16(f)(i)

Section VI.A.15, reciting corresponding limitations; *EX1003*, ¶282.

19. 16(g)

Device 130 is *a first semiconductor chip over said first interconnection scheme and between said first and second metal bumps*:

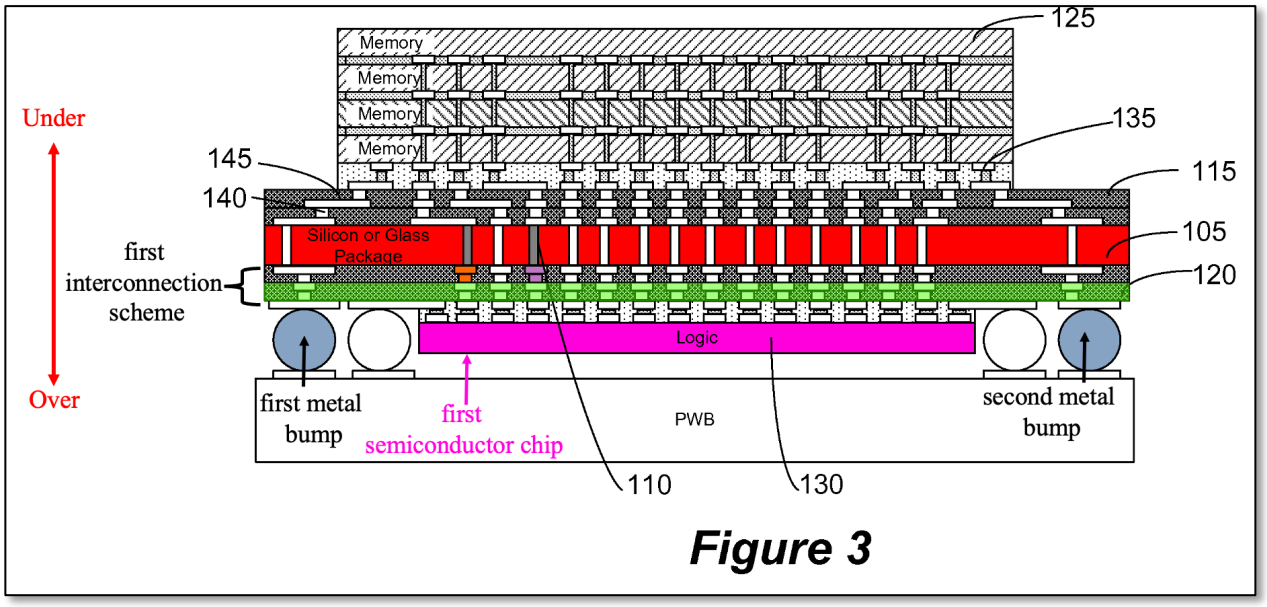


Figure 3

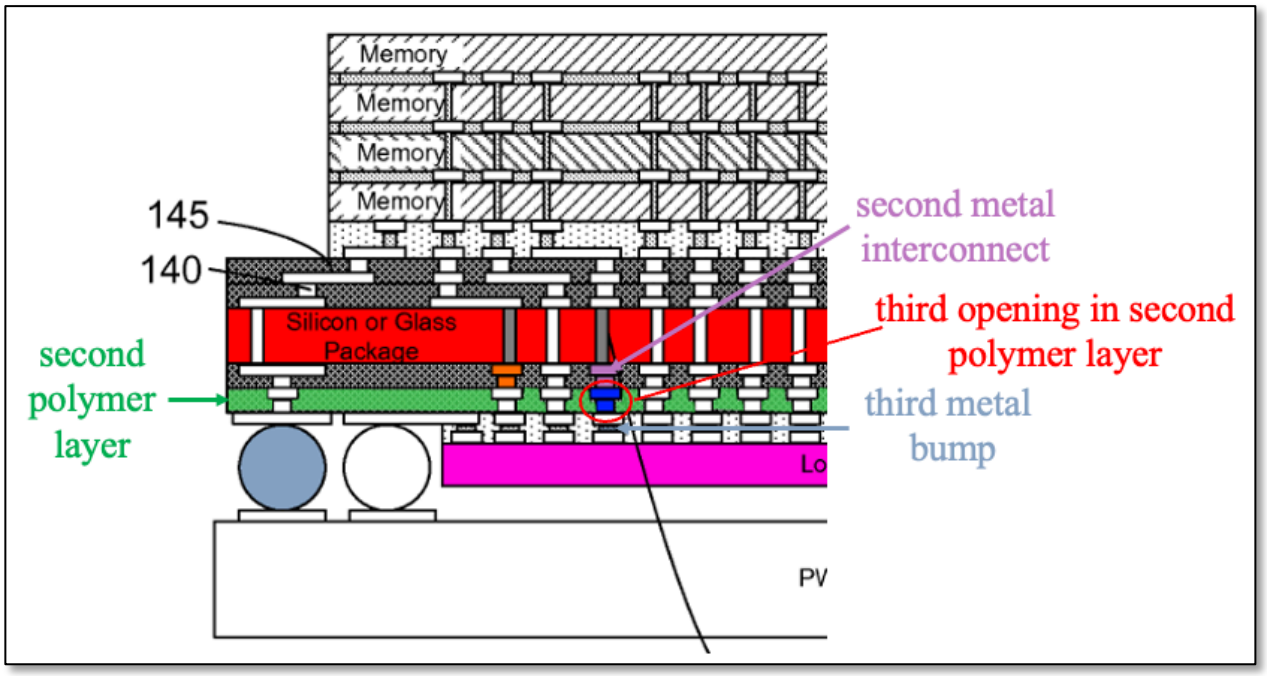
EX1004, FIG. 3; *EX1003*, ¶283

20. 16(h)

Section V.D.2, reciting corresponding limitations. *EX1003*, ¶284.

21. 16(h)(i)

Sundaram's *third metal bump [is] connected to said second metal interconnect* via traces and vias positioned in a *third opening in said second polymer layer*. The traces and vias are in *a third opening* because they are "defined within polymer-metal redistribution layers." *EX1004*, 6:62-67; *EX1003*, ¶285.



EX1004, FIG. 3 (excerpt).

22. 16(i)

Device 125 is *a second semiconductor chip under said first interconnection scheme and said first semiconductor chip*:

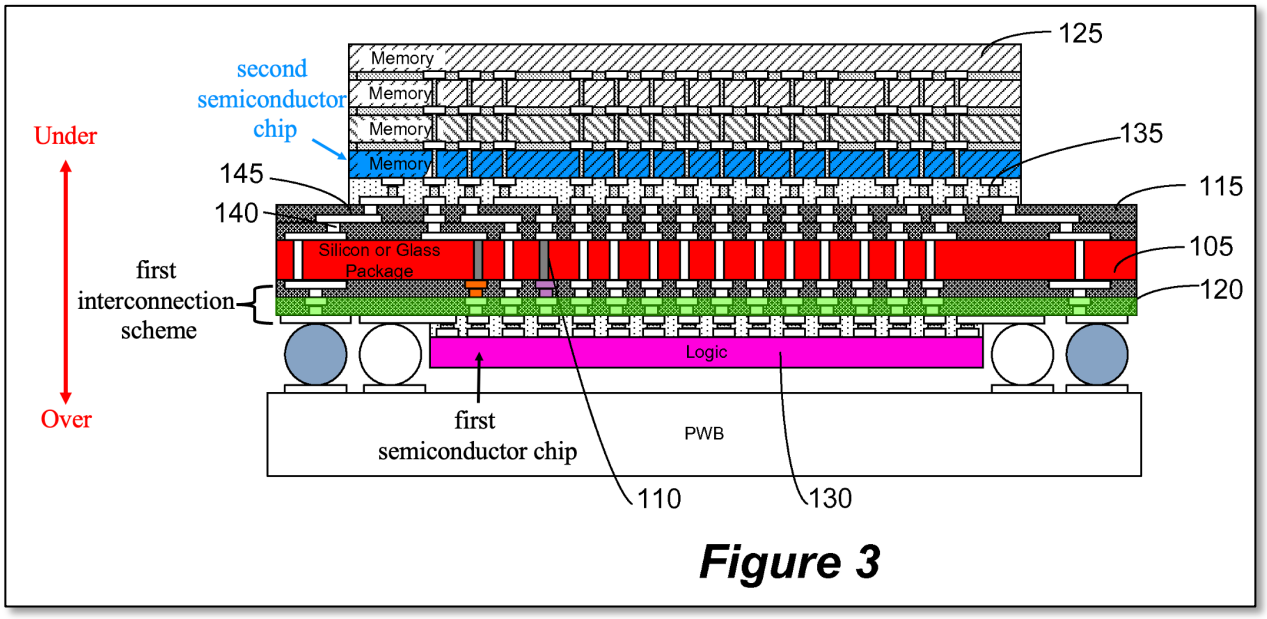


Figure 3

EX1004, FIG. 3; *EX1003*, ¶286.

23. 16(i)(i)

Sundaram's *first interconnection scheme is between said first and second semiconductor chips*:

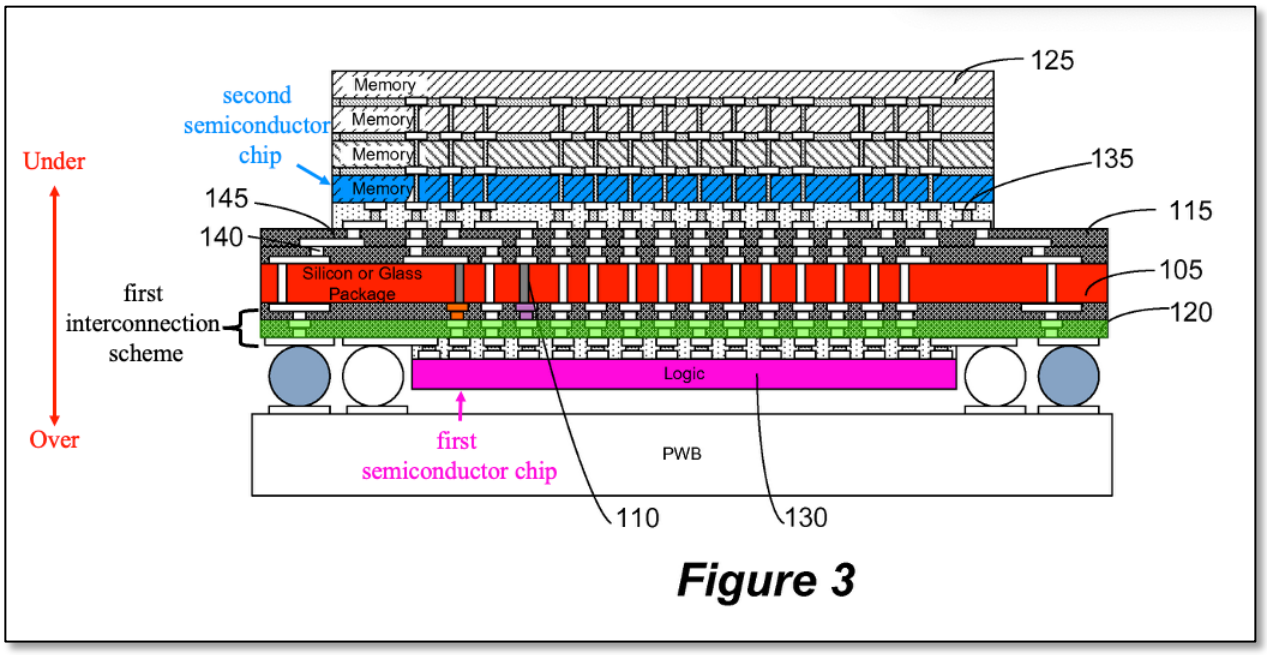


Figure 3

EX1004, FIG. 3; ¶287.

24. 16(i)(ii)

Section V.E, reciting corresponding limitations. *EX1003*, ¶288.

B. Claim 17

Sundaram teaches "third and fourth electronic devices can be stacked on the first 125 and second 130 electronic devices"; thus, the fourth electronic device stacked on second device 130 is *a third semiconductor chip over said first interconnection scheme*. *EX1004*, 7:16-18.

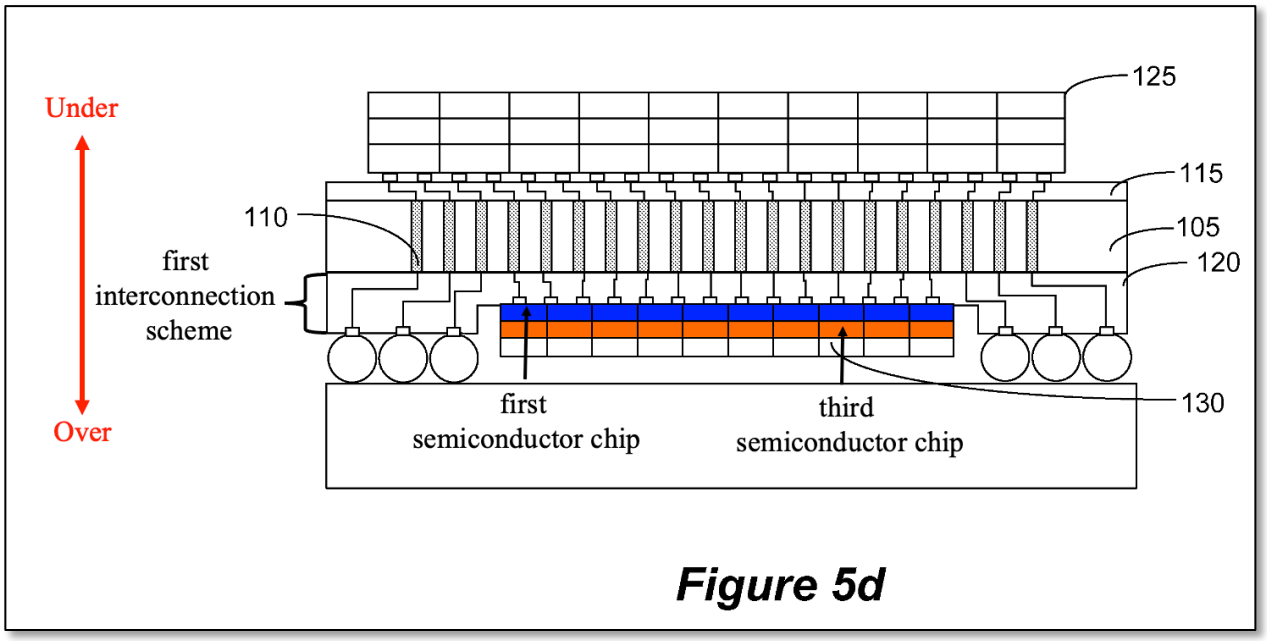


Figure 5d

EX1004, FIG. 5d; *EX1003*, ¶289.

C. Claim 18

Section V.F, reciting corresponding limitations. *EX1003*, ¶290.

D. Claim 19

Section V.N.

E. Claim 21

1. 21(a)

Section V.L.1, reciting corresponding limitations. *EX1003*, ¶292.

2. 21(b)

FIG. 32 teaches *second and third semiconductor chips* having metal pads on either surface.

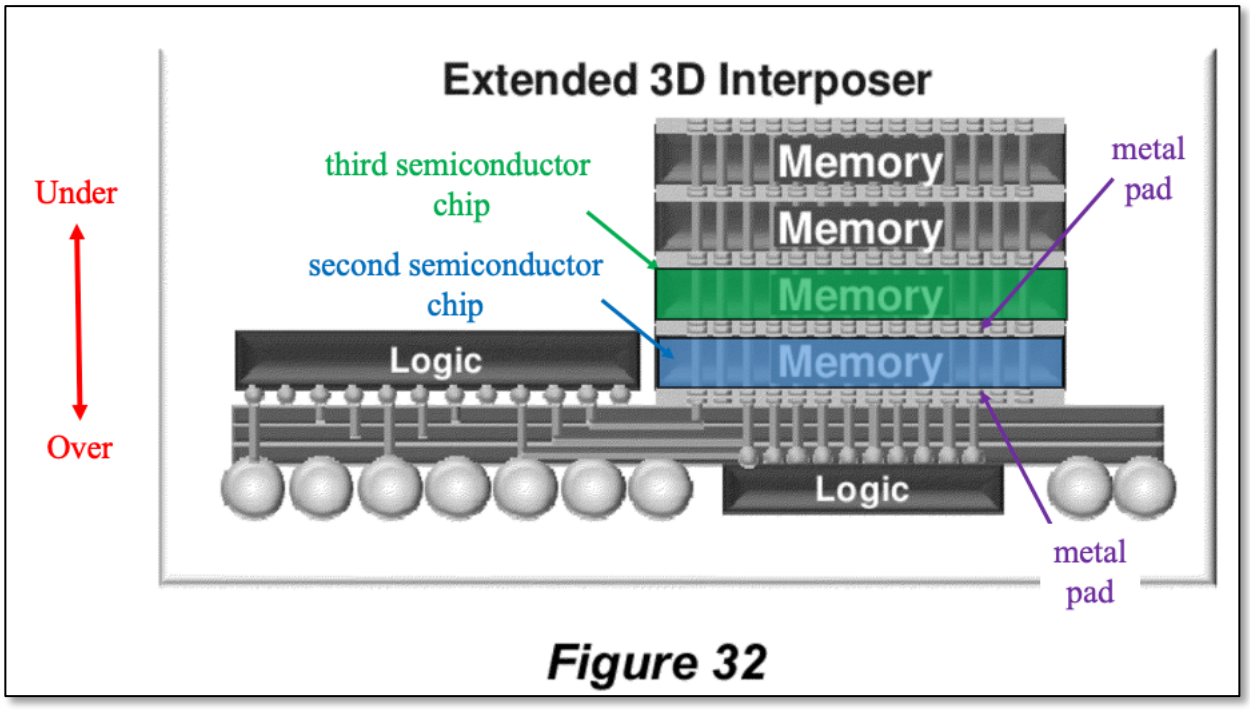


Figure 32

EX1004, FIG. 32.

Sundaram teaches "die pads 135…can electrically connect devices using solder, **copper bumps** with solder caps," and a POSITA would have understood chip pads on devices 125, 130 to likewise electrically connect using copper bumps. *EX1004*, 6:29-34; Section V.L.2; *EX1003*, ¶¶293-294. A POSITA would have found obvious and been motivated in combining Sundaram's internal embodiments to *connect[] pads* with *multiple fourth metal bumps between said second and third semiconductor chips*, teaching Claim 21(b). *Id*. The modification is the combination of known prior art elements (metal bump connections for chip pads) according to known methods to yield predictable results. *Id.* The modification would have advantageously provided Sundaram with a good electromechanical connection

between chips, which would have had a REOS because such was a common method of connecting chips. *Id.*

3. 21(c)

Section V.F.1, reciting corresponding limitations. *EX1003*, ¶295.

4. 21(d)

Section V.F.2, reciting corresponding limitations. *EX1003*, ¶296.

F. Claim 22

Sundaram teaches *a passive component over* Sundaram's first interconnection scheme. Section V.B. Sundaram's first interconnection scheme is *over said first surface*; thus, Sundaram teaches Claim 22.

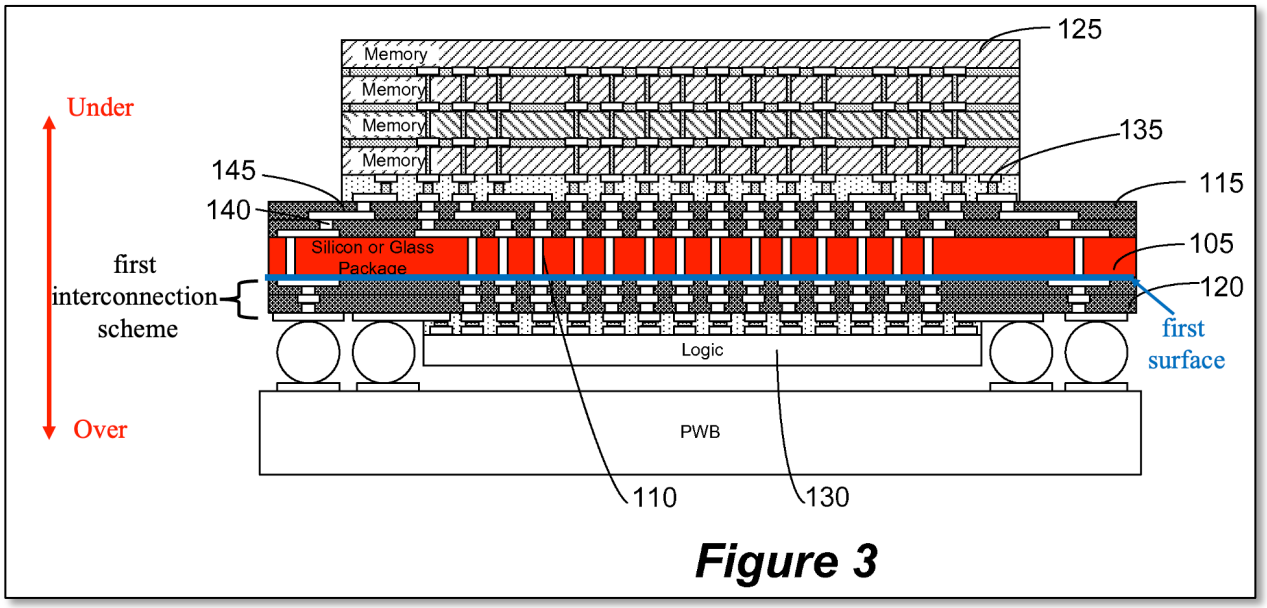


Figure 3

EX1004 at FIG. 3; *EX1003*, ¶297.

G. Claim 23

Section V.C, reciting corresponding limitations. *EX1003*, ¶298.

H. Claim 24

A second chip in Sundaram's memory stack is *a third semiconductor chip under said first interconnection scheme* and is *a memory chip*:

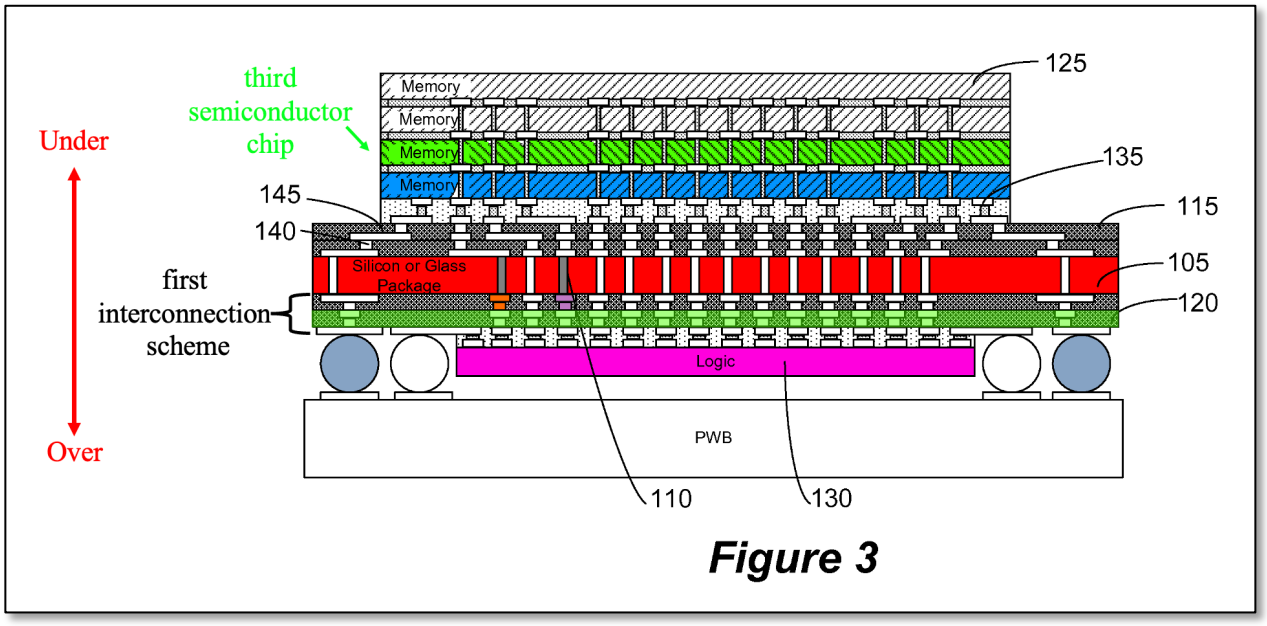


Figure 3

EX1004, FIG. 3, 6:37-38; *EX1003*, ¶299.

I. Claim 25

1. 25(a)

Section V.A.18, reciting corresponding limitations. *EX1003*, ¶300.

2. 25(b)

Section V.A.19, reciting corresponding limitations. *EX1003*, ¶301.

3. 25(c)

Section V.A.20, reciting corresponding limitations. *EX1003*, ¶302.

J. Claim 26

Section V.K.2, reciting corresponding limitations. *EX1003*, ¶303.

K. Claim 27

Sundaram's *second semiconductor chip is coupled to said first semiconductor chip through said first interconnection scheme* via the path, which includes vias 140 and traces 145 in the *first interconnection scheme*.

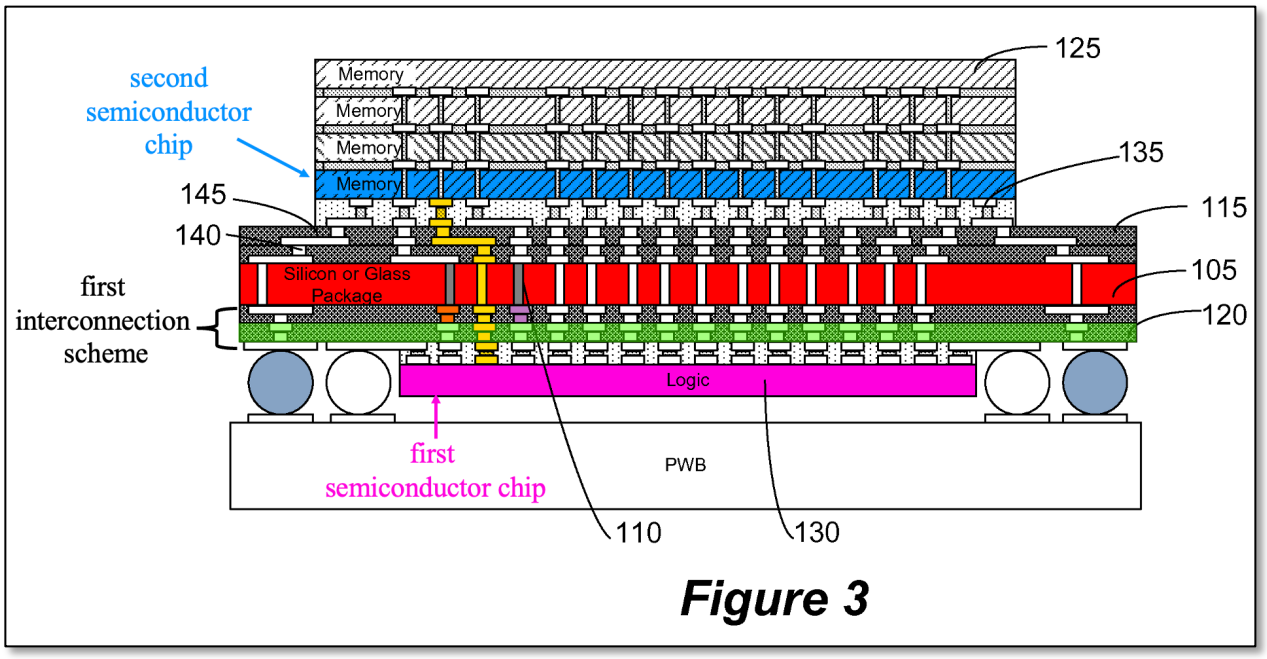


Figure 3

EX1004, FIG. 3; *EX1003*, ¶304.

L. Claim 28

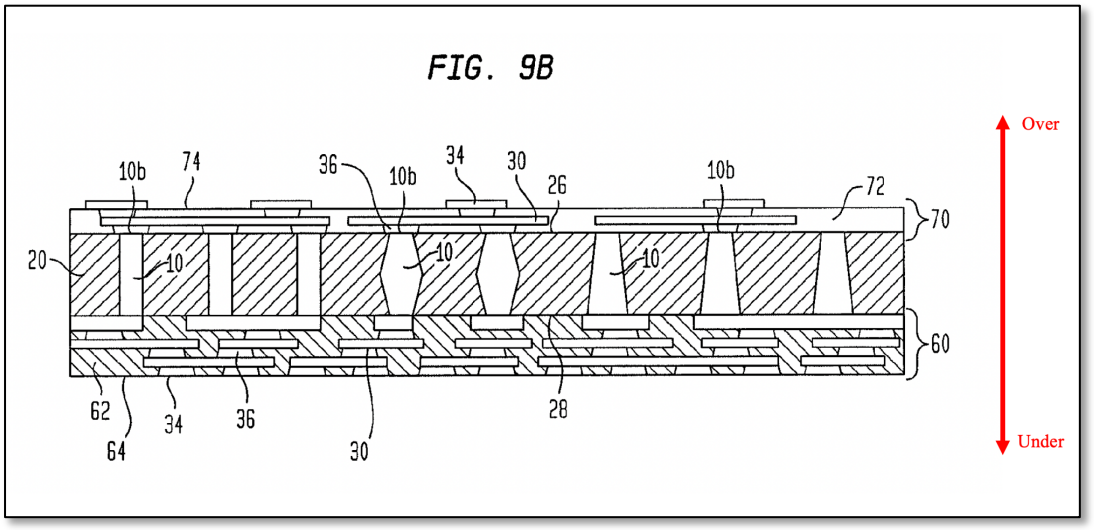
Section V.O.

VII. GROUND 2A: CLAIMS 1-3, 5, 7-10, AND 14-15 ARE OBVIOUS OVER HABA AND LIN-191

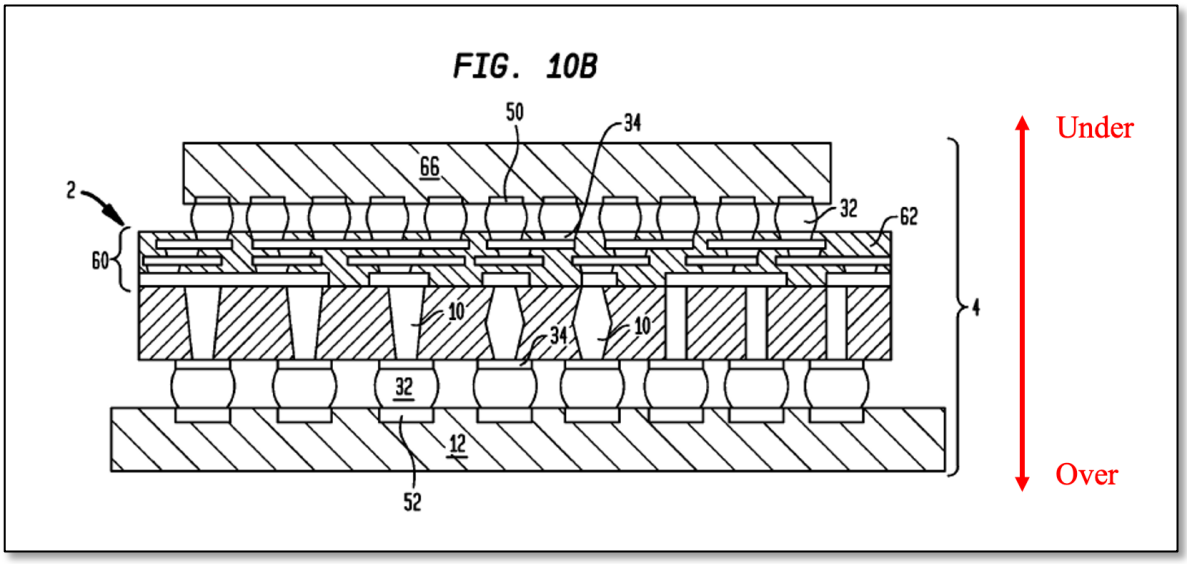
A. Overview of Haba's Figures

Petitioners' mapping relies on Haba, FIGS. 9B and 10B, where the "embodiment of [interconnection] component 2 shown in FIG. 9B can be used…in a similar arrangement as shown in FIGS. 10A and 10B," and FIG. 10B is "inverted

with respect to" FIG. 9B. *EX1009*, 8:12-15, 7:42-56, 5:1-6; *EX1003*, ¶¶306-313 (opining Haba teaches or renders obvious FIG. 9B's components usable in FIGS. 10A-10B).



EX1009, FIG. 9B.

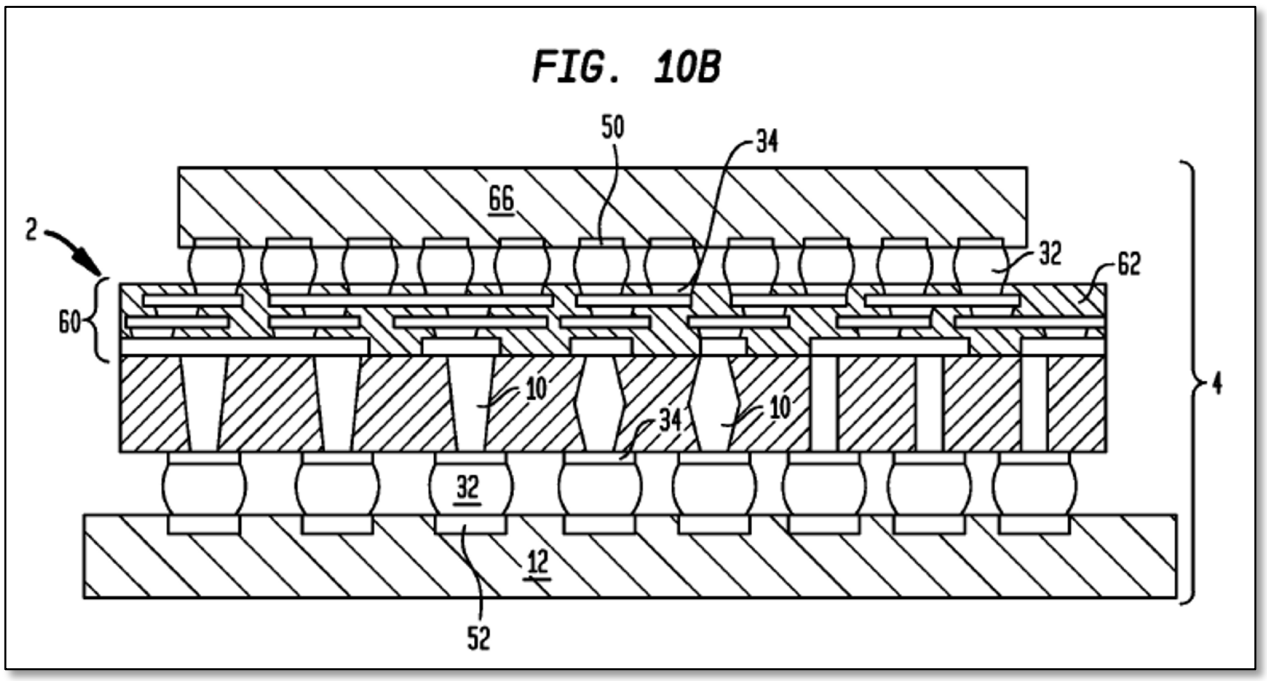


EX1009, FIG. 10B.

B. Claim 1

1. 1(Pre)

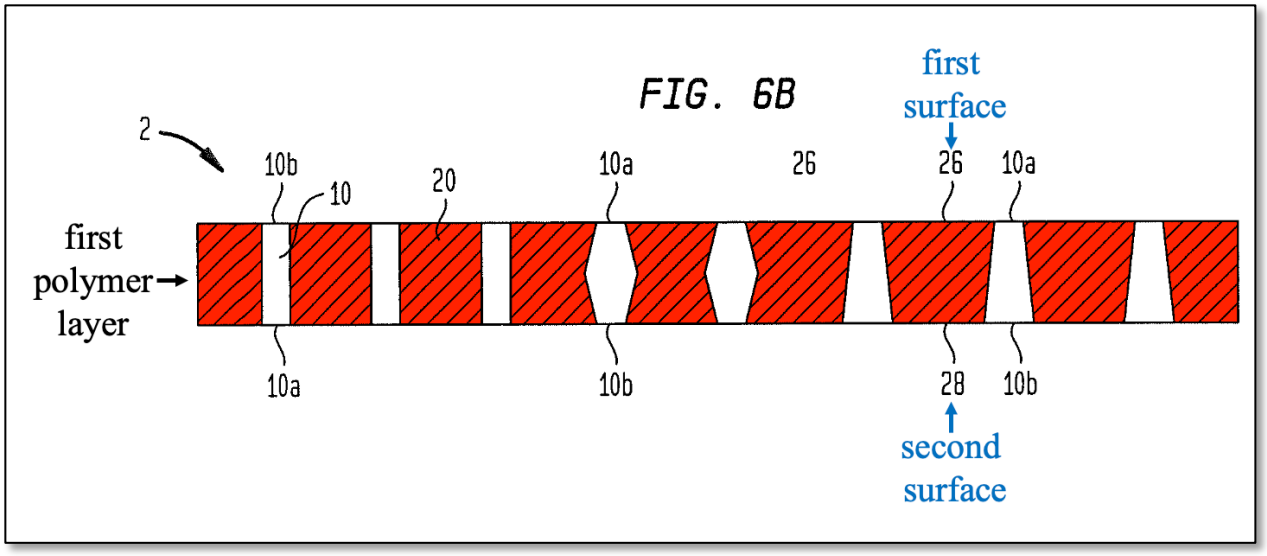
Haba teaches a *chip package* including, at least in part, a "microelectronic assembly" that "include[s] a microelectronic element" and "an interconnection component." *EX1009*, 4:40-45, 11:3-9. Haba's microelectronic assemblies "include…**packaged** microelectronic elements such as…semiconductor **chips** mounted on a substrate." *EX1009*, 1:19-21. A microelectronic element 66 (semiconductor chip) is mounted on interconnection component 2 (a substrate) forming a *chip package*, which is "flip-chip bonded" to a PCB. *EX1009*, 5:63-67, 2:59-3:3, 6:19-23.



EX1009, FIG. 10B; *EX1003*, ¶¶314-315.

2. 1(a)

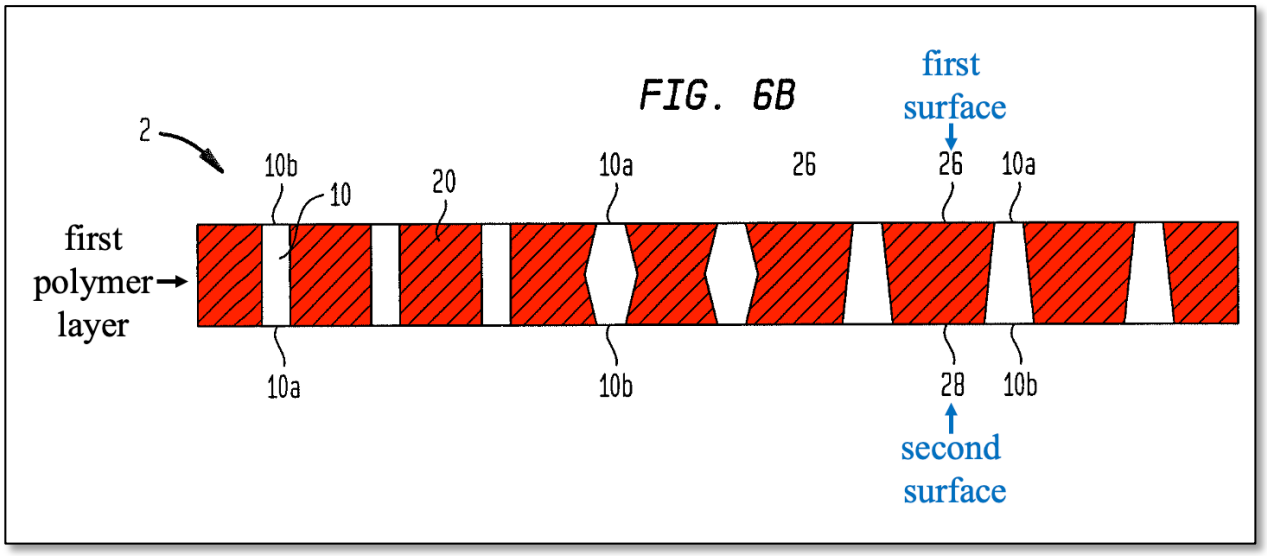
Interconnection component 2 includes dielectric layer 20 (*a first polymer layer*) having surface 26 (*first surface*) *opposite to* surface 28 (*second surface*). *EX1009*, 1:51-52 ("The dielectric layer has first and second **opposed** surfaces…"), 3:40-42, 5:22-29, 5:41-44. Layer 20 is "a **polymeric** dielectric, such as epoxies and polyimides." *EX1009*, 5:41-44, 6:19-23.



EX1009, FIG. 6B; *EX1003*, ¶¶316-317.

3. 1(a)(i)

Surface 26 *is substantially parallel* to surface 28. *EX1009*, 1:51-52.



EX1009, FIG. 6B; *EX1003*, ¶318.

4. 1(a)(ii)

Dielectric layer 20 has "a thickness of **at least 10 mm** between the first and second surfaces[,]" overlapping with and thus teaching or rendering obvious the claimed range of *between 100 and 300 micrometers*. *EX1009*, 2:34-36; *EX1003*, ¶319.

a) Lin-191's Teachings

Additionally or alternatively to Haba, Lin-191 teaches or renders obvious a *thickness between 100 and 300 micrometers*. Lin-191 teaches "a polymer substrate [110]." *EX1005*, [0051]. Copper "through-hole connections" are in substrate 110, which are analogous to Haba's posts (discussed at Claim 1(b)). *EX1005*, [0292-0293]. Substrate 110 is therefore a *first polymer layer* like Haba's dielectric layer 20. Substrate 110 has "thickness between 10 and 150 micrometers," which overlaps

with the claimed range, thus teaching or rendering obvious *between 100 and 300 micrometers*. *EX1005* at [0290]. *See* Section V.A.4 (supporting caselaw and discussion of the '768 Patent not ascribing criticality to Claim 1(a)(ii)'s range); *EX1003*, ¶323.

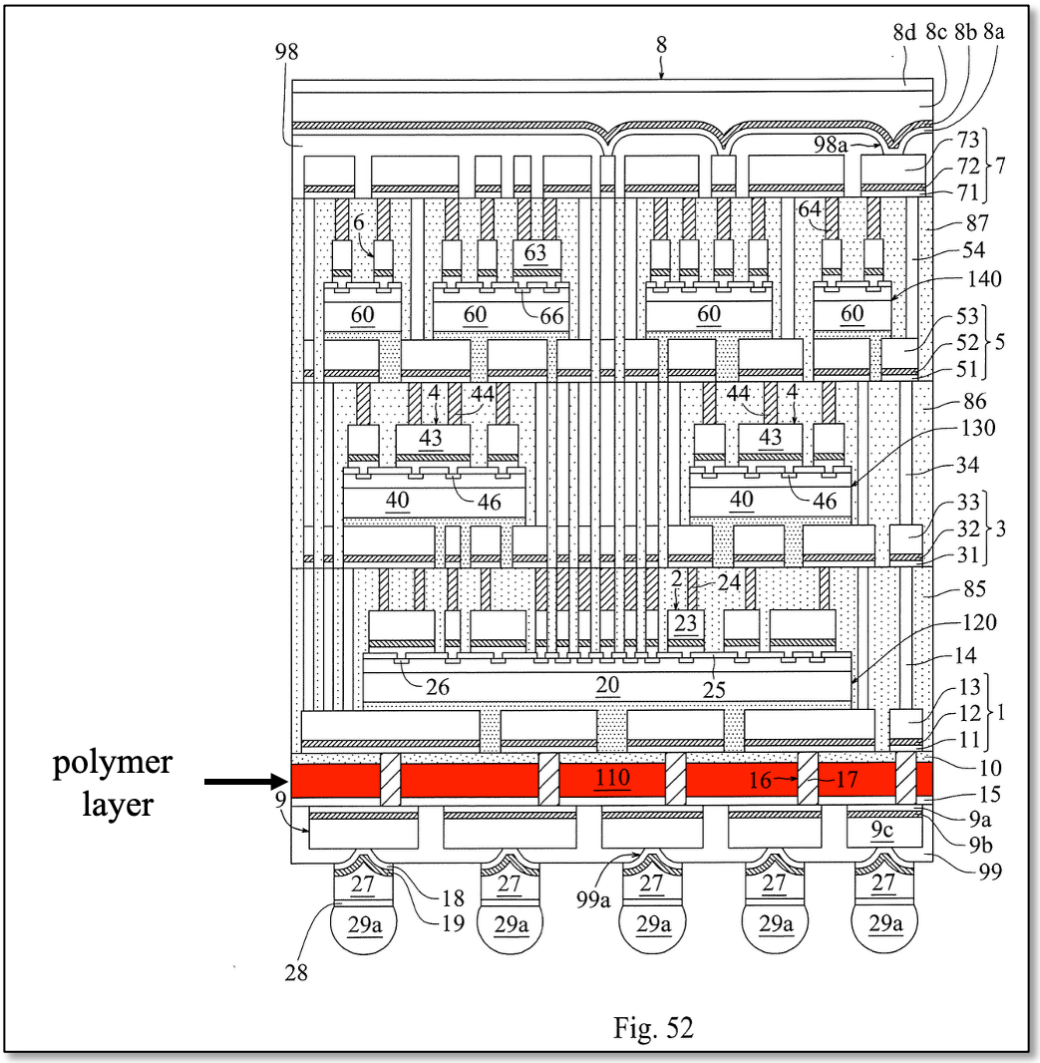


Fig. 52

EX1005, FIG. 52; *EX1003*, ¶¶320-322.

b) MTC

Lin-191 provides more specificity and optimal ranges for a polymer/dielectric layer than is otherwise taught in Haba as having a thickness of at least 10 microns. Selecting a thickness of a substrate would have been a design choice based on factors such as use environment of the package, manufacturability (e.g., layer thickness impacts defect and void formation), and type of chip (e.g., high vs low power chips generate varying degrees of heat). *EX1003*, ¶¶324-328. While, the industry's trend was to smaller (thinner) packages, a POSITA would have appreciated the tradeoff of a slightly larger package size to obtain certain benefits. *EX1003*, ¶329.

A POSITA would have been motivated and found obvious to apply Lin-191's specific thickness to Haba's polymer layer to reduce stress and mechanical fatigue occurring between Haba's posts and dielectric layer. *EX1003*, ¶¶325-326. Utilizing Lin-191's substrate thickness improves thermal management in chip packages as thicker dielectric layers provide greater thermal buffering between active layers and external environments. *EX1003*, ¶327. The thickness increase would enable more layers of interconnection or EMI shielding to be included while maintaining the minimum allowed interlayer spacing, increasing design flexibility. *EX1009*, 8:18-40; *EX1003*, ¶328.

The Haba-Lin-191 combination is the application of a known technique to a known device ready for improvement to yield predictable results. *EX1003*, ¶330. A

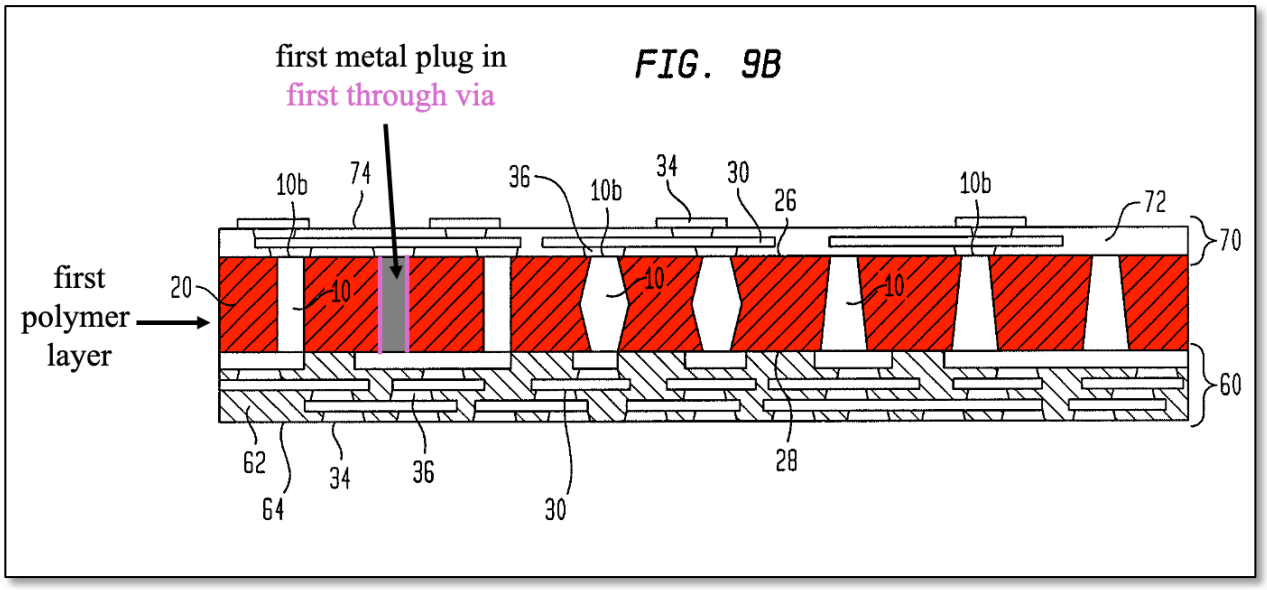
POSITA would have had a REOS because no change in processing would be required, only a routine adjustment to a known tunable parameter (thickness), and polymer interposers were commonly manufactured to the claimed thickness. *EX1003*, ¶331.

5. 1(a)(iii)

Section V.A.5.a.

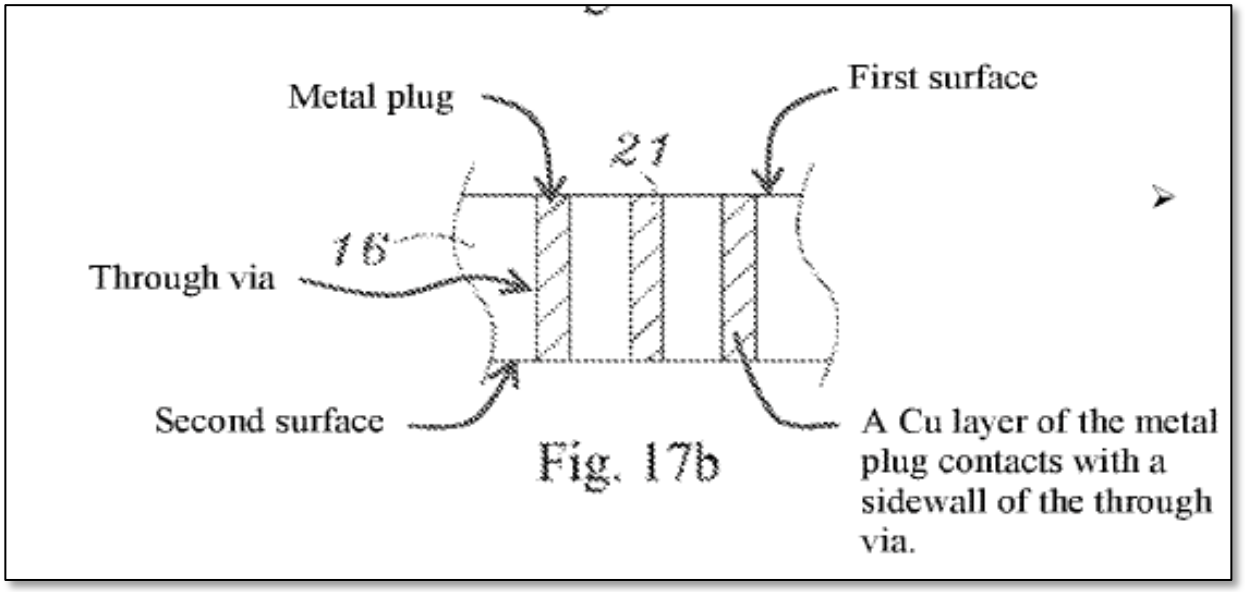
6. 1(b)

Interconnection component 2 includes "posts 10 within a dielectric layer 20" for "facilitating connectivity between elements," where posts 10 are "copper." *EX1009,* 5:23-35, 3:57-58. Each post is a *metal plug* and has "end surfaces 10A and 10B remote from each other with an edge surface 14 extending therebetween" such that posts 10 are *vertical[]…in said first polymer layer*. *EX1009*, 5:26-27. FIG. 9B shows a first post 10 in *a first through via*, i.e., the passageway in layer 20 in which post 10 is located:



EX1009, FIG. 9B; *EX1003*, ¶¶334-336.

During original examination in a Preliminary Amendment filed 5/25/2021, PO provided an annotated FIG. 17B illustrating specification support for the plugs 21 being within through vias, similar to Haba's arrangement of posts 10.

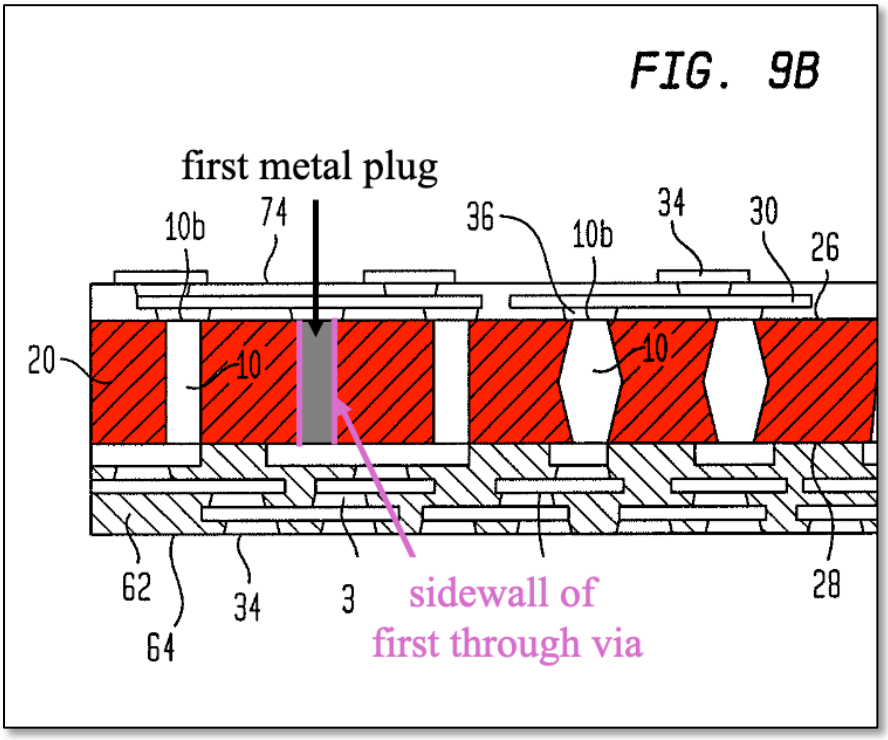


EX1002, 537; *EX1003*, ¶333.

7. 1(b)(i)

Haba's posts are "copper" and "fabricated from a **single layer** of the principal metal" thus *compris[ing] a first copper layer*. *EX1009*, 3:57-58, 9:14-18, 10:46-49.

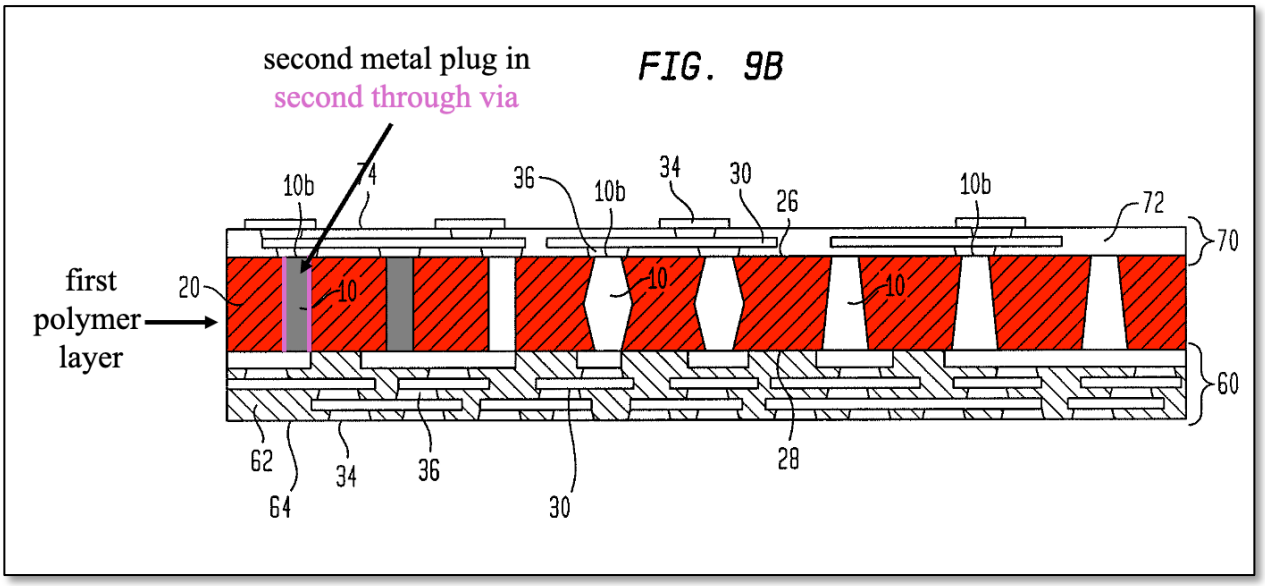
Dielectric layer 20 "contact[s] the edge surfaces…of the posts." *EX1009*, 1:49-51, 3:36-40, 9:29-30. Thus, post 10 has a *first copper layer contact[ing] a sidewall of said first through via*, mirroring PO's statements during original prosecution. *EX1002*, 537.



EX1009, FIG. 9B (excerpt); *EX1003*, ¶337-338.

8. 1(c)

Haba teaches a second post 10 *vertically in a second through via in said first polymer layer*:



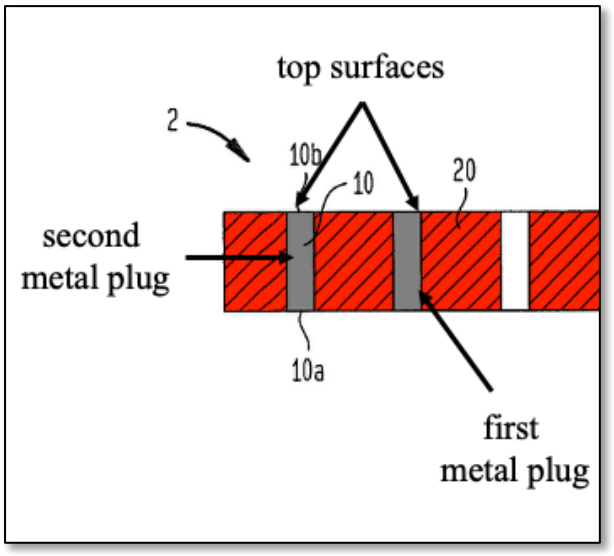
EX1009, FIG. 9B; *EX1003*, ¶339.

9. 1(c)(i)

Section VII.B.7.

10. 1(c)(ii)

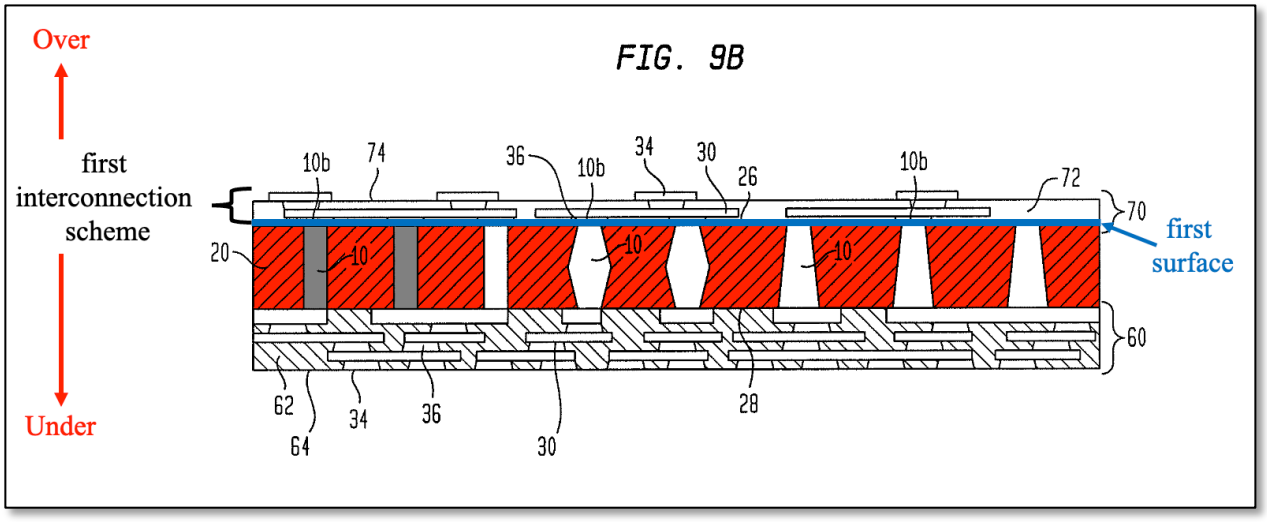
Surface 26 is "**coplanar** with end surfaces 10B of the posts." *EX1009*, 10:8-10. End surfaces 10B are *top surface[s]* and *in the same horizontal plane* because they are coplanar.



EX1009, FIG. 6B (excerpt); *EX1003*, ¶341.

11. 1(d)

Haba teaches *a first interconnection scheme over* surface 26 formed by metal traces 30, vias 36 in RDL 70, and pads 34 over RDL 70. *EX1009*, 6:59-7:11, FIG. 8; Section V.A.11, footnote 5.



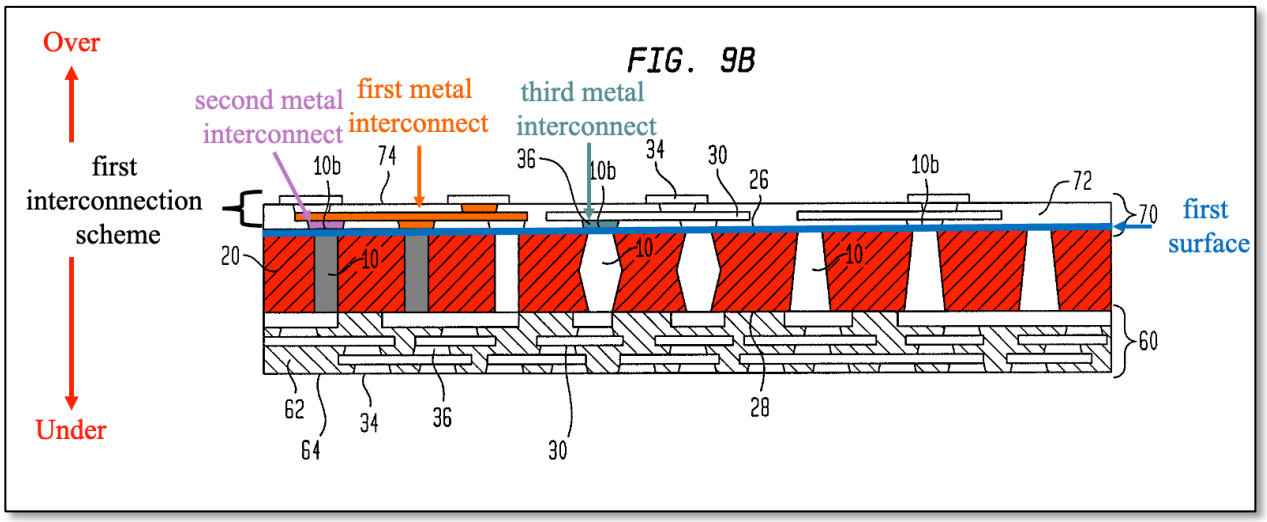
EX1009, FIG. 9B.

Interconnection component 2 "**connect[s]** to a microelectronic component" via RDL 70. *EX1009*, 7:27-31, 7:57-63. Thus, because traces 30, vias 36, and pads 34 interconnect interconnection component 2 to other microelectronic components, they collectively form *an interconnection scheme*. *EX1003*, ¶342-343.

12. 1(d)(i)

a) First, Second, and Third Metal Interconnects

Haba teaches a *first metal interconnect over* surface 26, formed by metal traces 30 and vias 36 in RDL 70. *EX1009*, 6:59-62, 7:63-65. Traces 30 are "wettable **metal** layers." *EX1009*, 6:47-62, 10:51-52, 10:20-23, 7:34-37. *Second* and *third metal interconnect[s]* are formed from vias 36 (pink, blue-green).



EX1009, FIG. 9B; *EX1003*, ¶344.

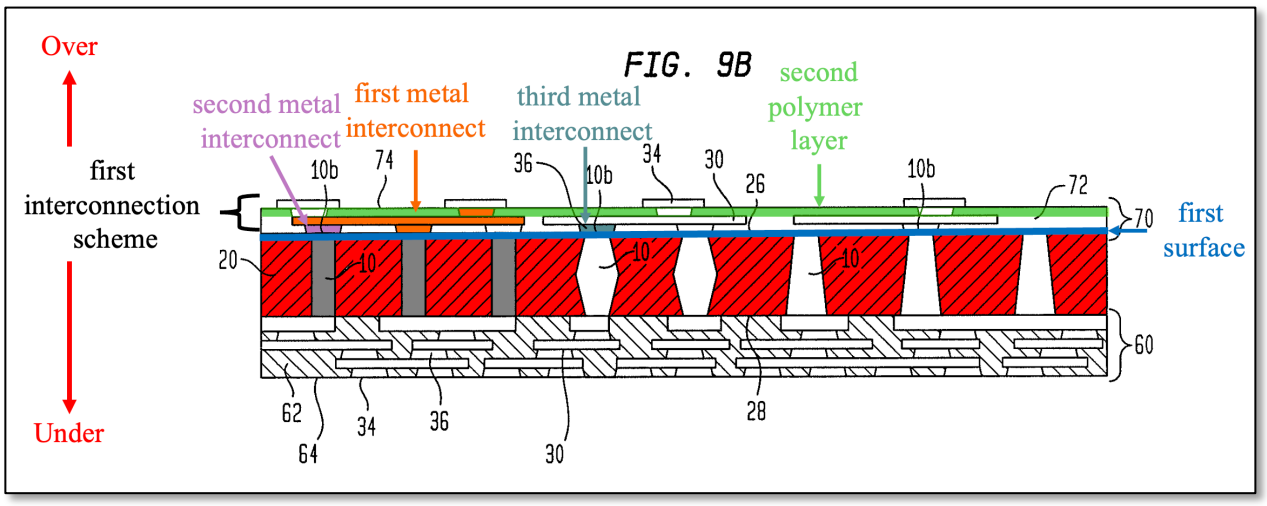
Haba teaches vias 36 are metal. Specifically, Haba teaches "wettable metal layers or structures can be added to interconnection component 2 that can be wettable contacts for connection to other microelectronic components." *EX1009*, 6:47-50.

Therefore, Haba teaches wettable metal layers are wettable contacts. Haba then teaches "wettable contacts formed by vias 36[.]" *EX1009*, 7:34-36. Because Haba teaches (1) wettable metal layers are wettable contacts, and (2) wettable contacts are vias, Haba teaches vias are *metal interconnects*. *EX1003*, ¶¶345-346.

b) "Second Polymer Layer"

(1) Haba's Teachings

Haba teaches a *second polymer layer*, namely an uppermost portion of redistribution dielectric 72. RDL 70 includes "redistribution dielectric 72" that traces 30 and vias 36 are "formed within." *EX1009*, 7:63-65. Dielectric 72 is a "dielectric **layer** [formed] along the other surface" of dielectric layer 20, i.e., *over* surface 26. *EX1009*, 2:21-25. Haba teaches dielectrics include "liquid-crystal **polymers**" such that dielectric 72 is *a polymer layer*. *EX1009*, 6:19-26; *EX1003*, ¶347.



EX1009, FIG. 9B.

Dielectric 72 is *over* the interconnects because RDL 70 is formed by applying dielectric 72 "between traces 30 and, optionally, over traces 30" where "[f]urther traces 30 and portions of redistribution dielectric [] can then be formed[.]" *EX1009*, 10:20-31; *EX1003*, ¶¶348-349 (discussing '768 Patent's prosecution history).

(2) Lin-191's "Polymer" Teachings

Additionally or alternatively, Lin-191 teaches a *second* ***polymer*** *layer*, namely "encapsulating layer 85…formed over the substrate 110," which is "a polymer layer." *EX1005*, [0109].

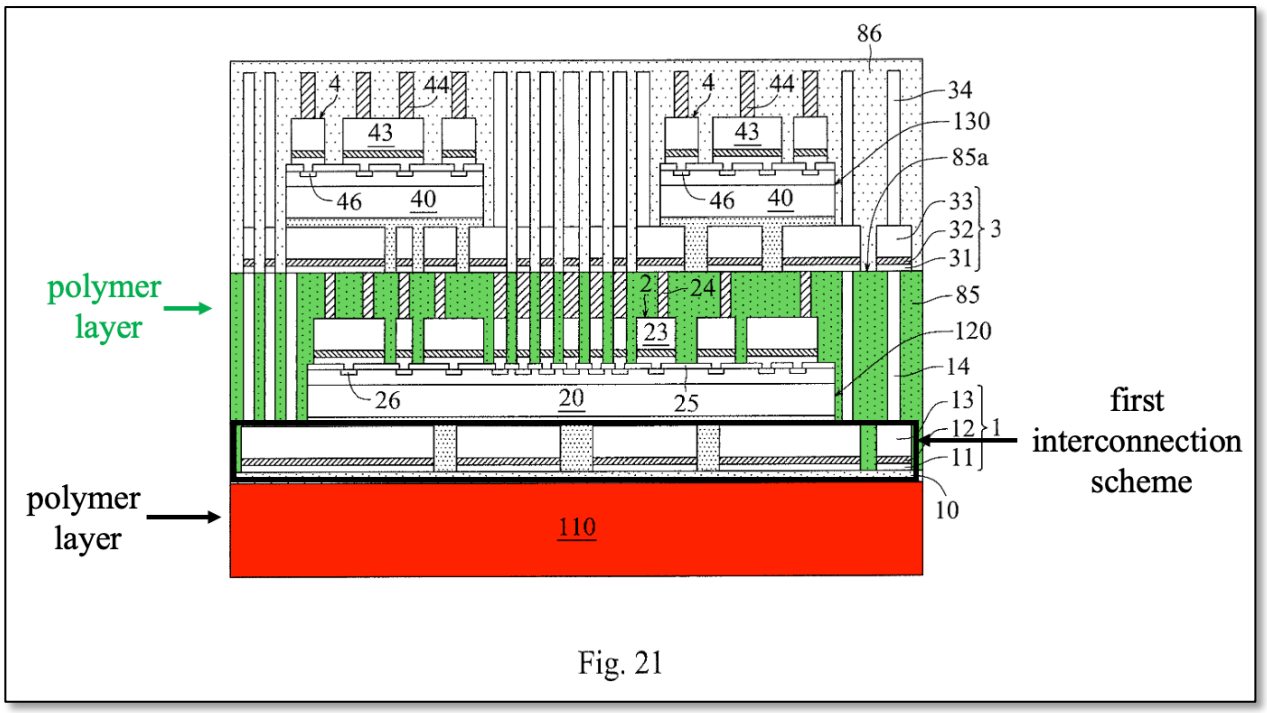


Fig. 21

EX1005, FIG. 12. Like Haba's dielectric 72, Lin-191's layer 85 is *over* an *interconnection scheme* formed by patterned metal layers 1. *EX1003*, ¶¶350-351.

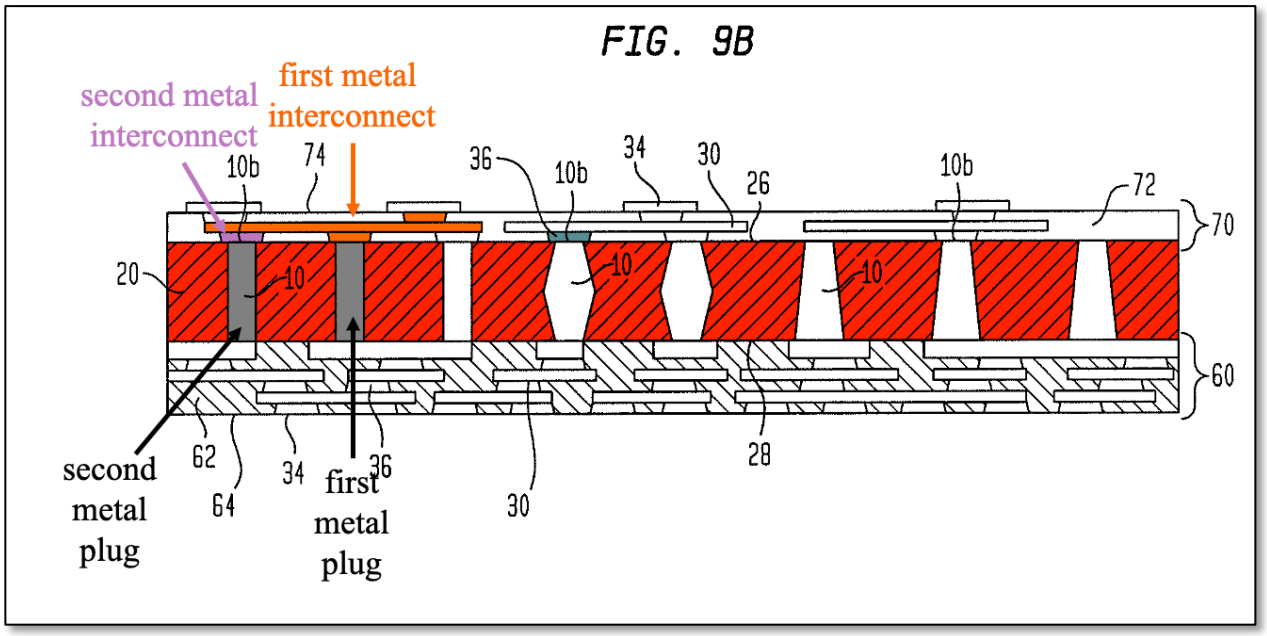
(3) MTC

A POSITA would have been motivated and found obvious to modify Haba's dielectric 72 to be *polymer* per Lin-191. *EX1003*, ¶¶352-355. Haba teaches **dielectric** layer 20 is a polymer. *EX1009*, 5:41-44. A POSITA would have found obvious to likewise form **dielectric** 72 from a polymer to form a multi-layer polymer interconnection component. *EX1003*, ¶¶352-355. Forming dielectric 72 as a *polymer* would have obtained the same advantages already achieved with layer 20 being a polymer, e.g., preventing delamination and cracking between RDL 70 and layer 20. *EX1009*, 5:41-51, 6:6-26; *EX1003*, ¶¶352-355.

The combination is the application of a known technique (Lin-191's multi-polymer layers) to a known device (Haba's interconnection component 2) ready for improvement to yield predictable results. *EX1009*, 6:14-19; *EX1003*, ¶356. There would have been a REOS because polymer RDLs were well known. *EX1003*, ¶356.

13. 1(d)(ii)

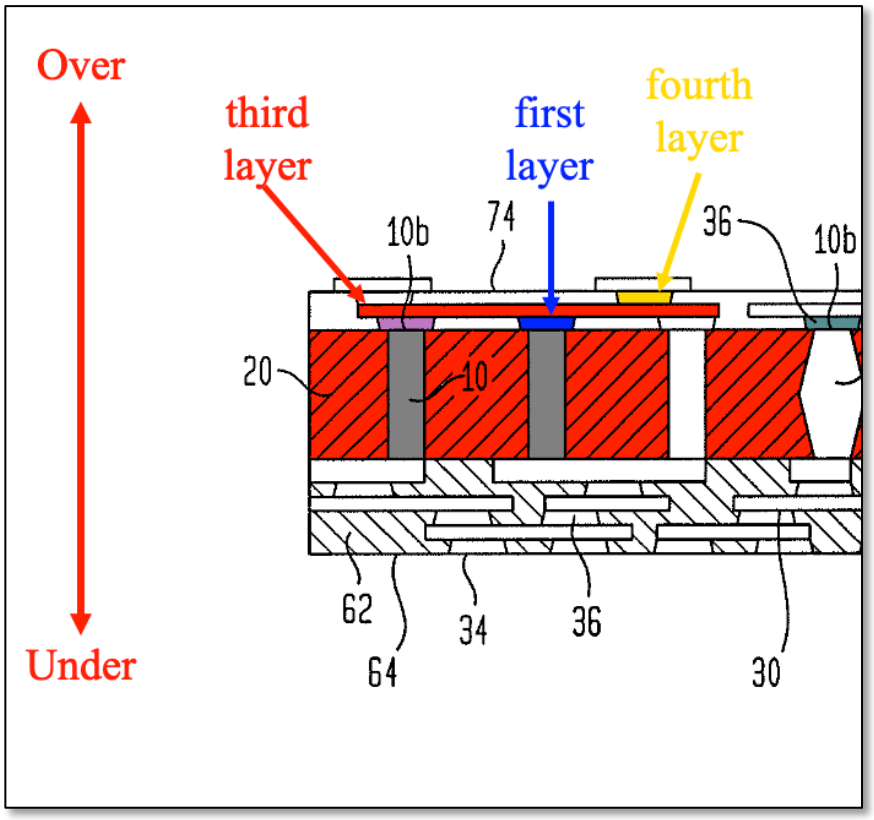
Haba's *first metal interconnect* comprises via 36 overlying first post 10 such that via 36 *is connected* to first post 10 (*first metal plug*) by via 36 contacting post 10. *EX1009*, 6:59-62. Haba's *second metal interconnect* is via 36 overlying and contacting second post 10 (*second metal plug*) such that via 36 *is connected* to the post 10.



EX1009, FIG. 9B; *EX1003*, ¶¶357-358.

14. 1(d)(iii)

Haba's *first metal interconnect* comprises a *first…layer* (first via), *a third…layer on said first…layer* (trace on the first via), and *a fourth…layer* (second via) *on said third…layer* (trace):



EX1009, FIG. 9B (excerpt).

Haba teaches vias 36 are *metal*, thereby teaching *a first metal layer* (via 36). Section VII.B.12.a; *EX1003*, ¶¶359-361.

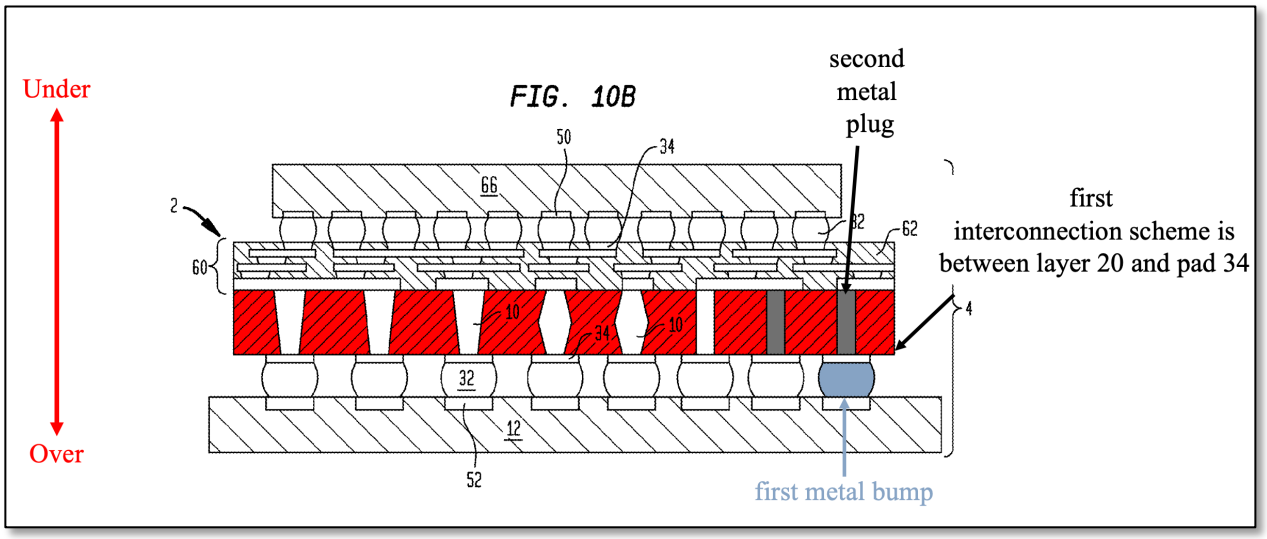
a) Lin-191's Teachings and MTC

Additionally or alternatively, Lin-191 teaches the claimed *layer[s]*. Section V.A.14. The MTCs and REOS for modifying Sundaram per Lin-191 apply for the Haba-Lin-191 combination. *Id*. The application of Lin-191's copper layers to Haba's interconnection component would have been a straightforward design choice for a POSITA seeking to increase electrical and thermal performance. *EX1003*, ¶362. The combination is the application of a known technique (Lin-191's metal interconnect

layers) to a known device (Haba's interconnection component) ready for improvement to yield predictable results. *Id*.

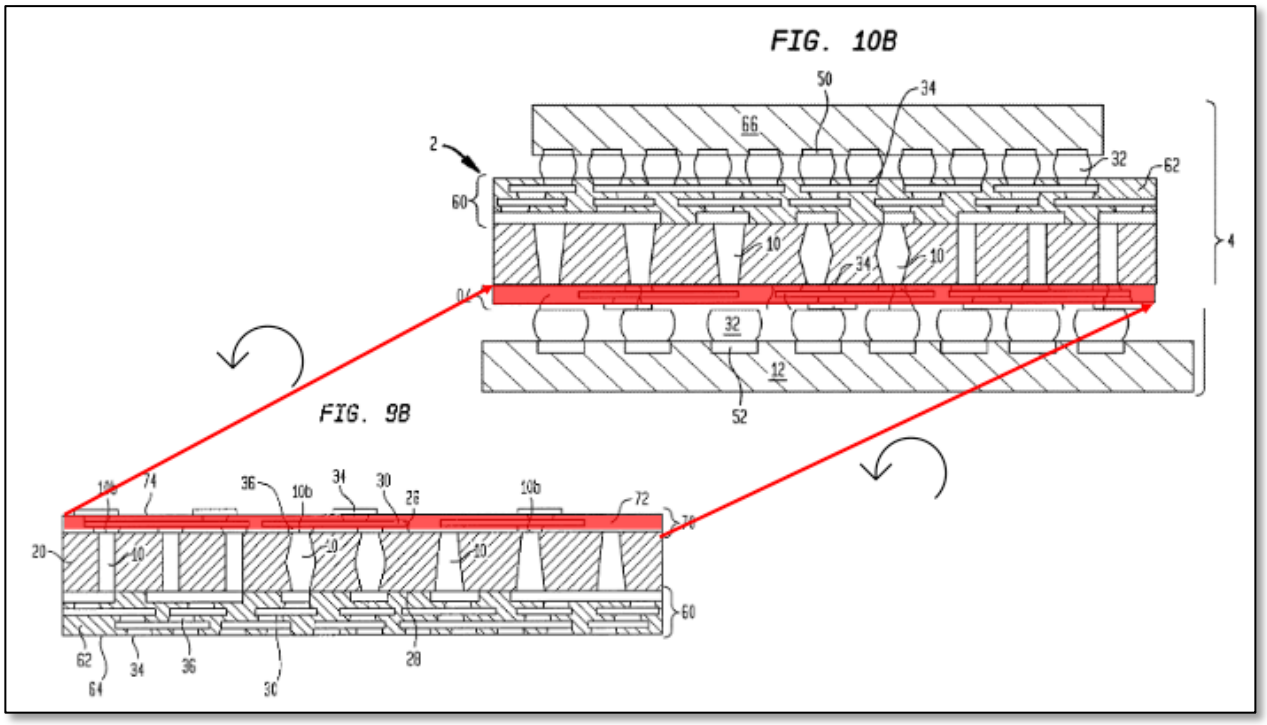
15. 1(e)

Haba teaches solder balls 32 (*a first metal bump*), which is *over said first interconnection scheme and said second metal plug*.



EX1009, FIG. 10B; *EX1003*, ¶¶365-367.

While FIG. 9B's RDL 70 is not depicted in FIG. 10B, Haba teaches FIG. 9B's component 2 is usable "in a similar arrangement as shown in FIGS. 10A and 10B…" *EX1009*, 8:12-15. Thus, a POSITA would have understood FIG. 10B's interconnection component to include RDL 70 as shown in FIG. 9B. *EX1009*, 7:57-59.



EX1009, FIGS. 9B, 10B (RDL 70 inverted according to FIG. 10B's inversion relative to FIG. 9B); *EX1003*, ¶¶363-365.

Accordingly, Haba teaches solder ball 32 is *over said first interconnection scheme*, i.e., over RDL 70. *EX1003*, ¶¶363-367.

16. 1(e)(i)

Haba's teachings of **solder** balls teach *a tin-containing layer* because solder contains tin. *EX1003*, ¶368.

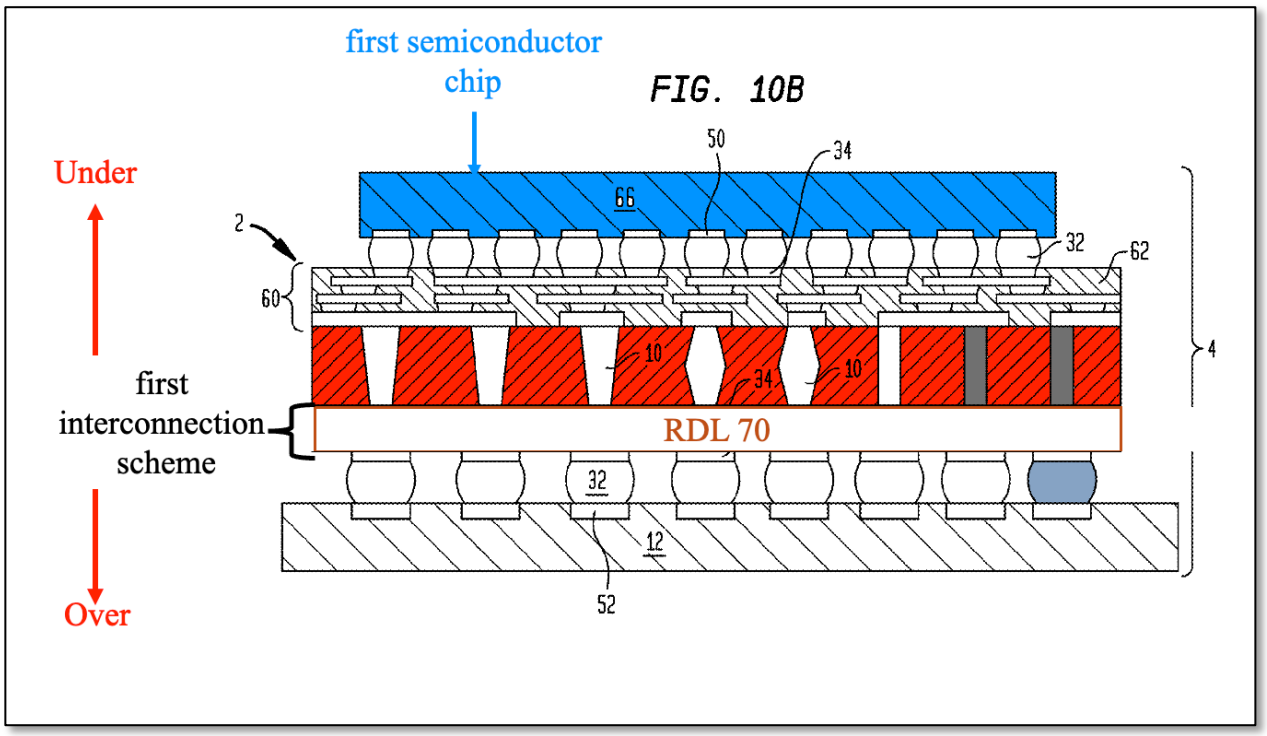
a) Lin-191's Teachings and MTC

Additionally or alternatively to Haba, Lin-191 teaches *a tin-containing layer*. Section V.A.16.a-b. A POSITA would have found obvious, been motivated, and had

a REOS in modifying Haba per Lin-191 for the same reasons described for Sundaram-Lin-191. *Id.*; *EX1003*, ¶369.

17. 1(f)

Haba teaches microelectronic element 66 is "one or more **semiconductor chips**[.]" *EX1009*, 7:42-56, 1:19-22. Microelectronic element 66 (*first semiconductor chip*) is *under* RDL 70, and thus, *under said first interconnection scheme*. *EX1009*, 7:57-59.

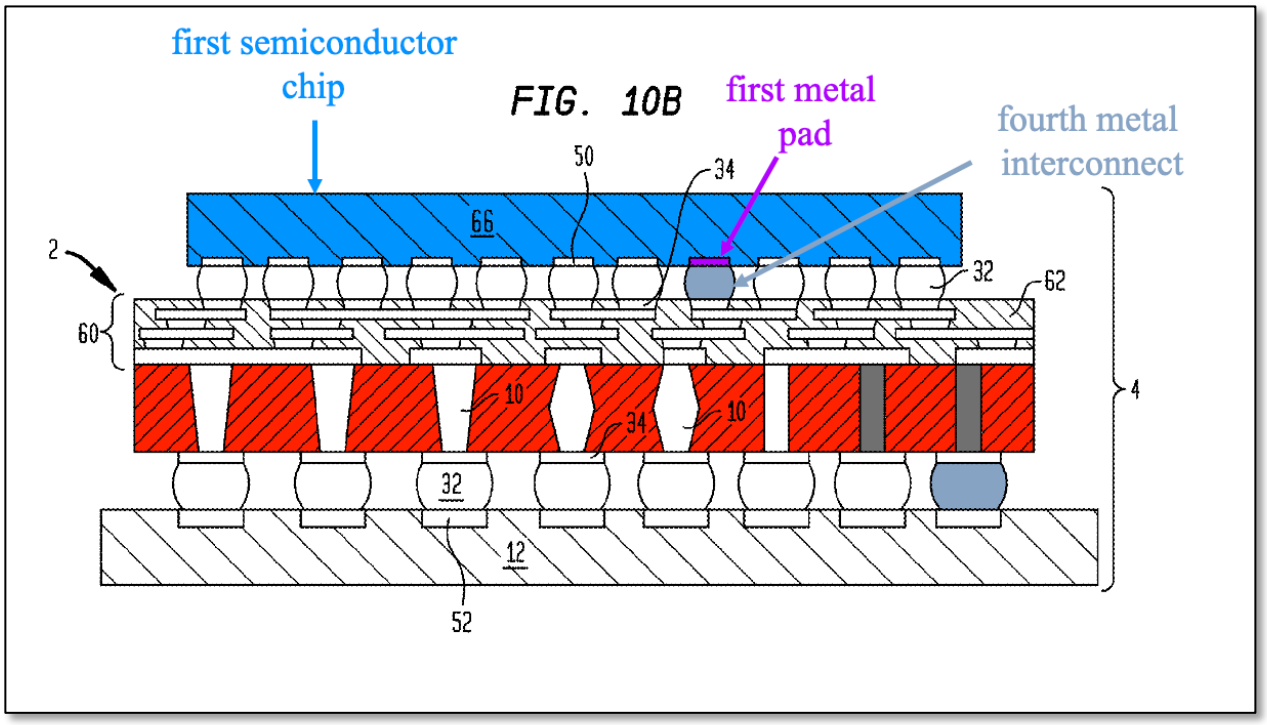


EX1009, FIG. 10B; *EX1003*, ¶¶370-372.

18. 1(f)(i)

Microelectronic element 66 electrically connects to RDL 60 via solder ball 32, which is attached to contact 50 (*a first metal pad*), such that solder ball 32 is *a*

fourth metal interconnect that is *on a first pad* of microelectronic element 66 (*first semiconductor chip*). *EX1009*, 7:45-48; *EX1003*, ¶¶373-375. Haba discloses "contact pads 34" are "wettable **metal** layer or structures." *EX1009*, 6:50-55. A POSITA would have understood contact 50 to likewise be *metal*. *EX1003*, ¶¶373-375.



EX1009, FIG. 10B.

a) Lin-191's "Metal Pad" Teachings and MTC

Section V.A.18. The Haba-Lin-191 combination an implementation detail in Haba's chip package as Lin-191 provides the specificity of a metal contact pad to the extent that PO argues not provided by Haba. *EX1003*, ¶376. The same MTC and REOS for Sundaram-Lin-191 apply for Haba-Lin-191. Section V.A.18.b.

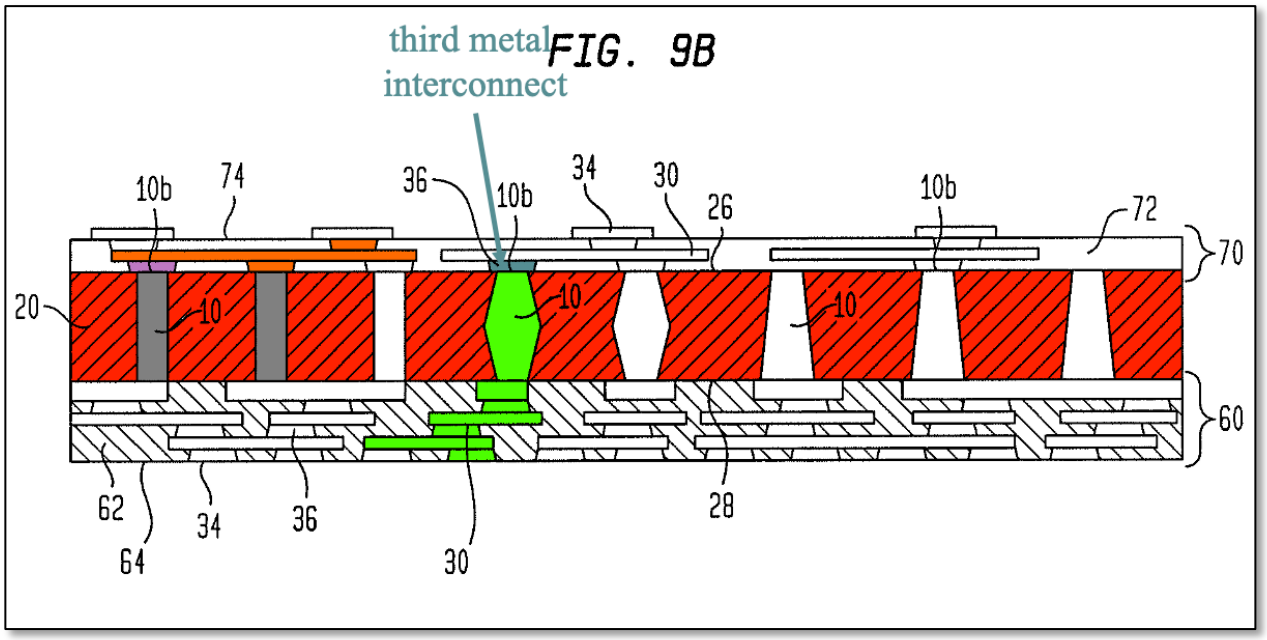
19. 1(f)(ii)

Lin-191 teaches or renders obvious interconnects/bumps with layers/thickness as recited in Claim 1(f)(ii). Section V.A.19. A POSITA would have been motivated, found obvious, and had a REOS in modifying Haba per Lin-191 for the same reasons discussed for Sundaram-Lin-191, i.e., to advantageously improve long-term solder ball performance. *Id*.; *EX1003*, ¶377.

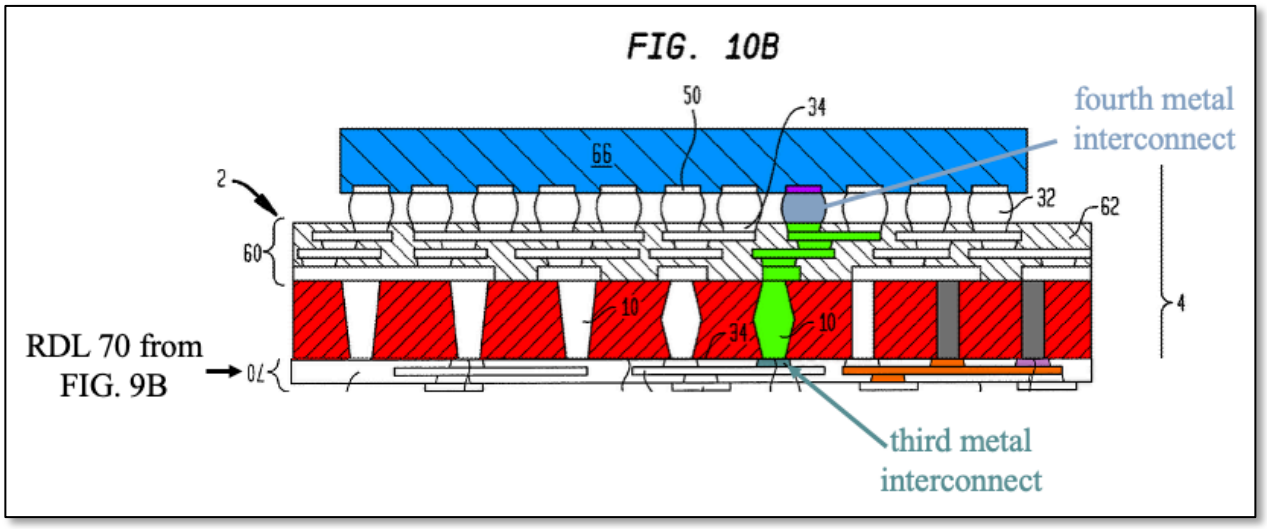
20. 1(f)(iii)

Solder ball 32 (*fourth metal interconnect*) *is connected to* Haba's *third metal interconnect* via RDL 60, which connects solder ball 32 to post 10 in layer 20. *EX1009*, 7:27-31, FIG. 10B. Post 10 is connected to the *third metal interconnect* in RDL 70, thereby connecting the *third* and *fourth metal interconnects*. *EX1009*, 7:57-62, 5:33-35, FIG. 9B; *EX1003*, ¶¶378-381.

Annotated FIG. 9B illustrates Haba's *third metal interconnect*, a post, and traces and vias in RDL 60 (green) while annotated FIG. 10B illustrates the *fourth metal interconnect* and the traces and vias connecting the *fourth metal interconnect* to that same post when RDL 70 is positioned in FIG. 10B.



EX1009, FIG. 9B.



EX1009, FIG. 10B; *EX1003*, ¶¶378-381.

C. Claim 2

a) Lin-191's Teachings

Lin-191 discloses two embodiments relevant to Claim 2's mapping. Lin-191 teaches chip 140 is "replaced by a passive component 67" that is "connected to the

metal layer 53 of the patterned metal layer 5 **through** two solder joints 68." *EX1005*, [0340], FIG. 55. Patterned metal layers 5 are *an interconnection scheme* because they include a "metal **interconnect** or trace…" *EX1005*, [0214]. As shown and otherwise expressly taught at [0341], passive component 67 is connected to the *interconnection scheme* (layer 5) *through a solder layer* (solder joint 68).

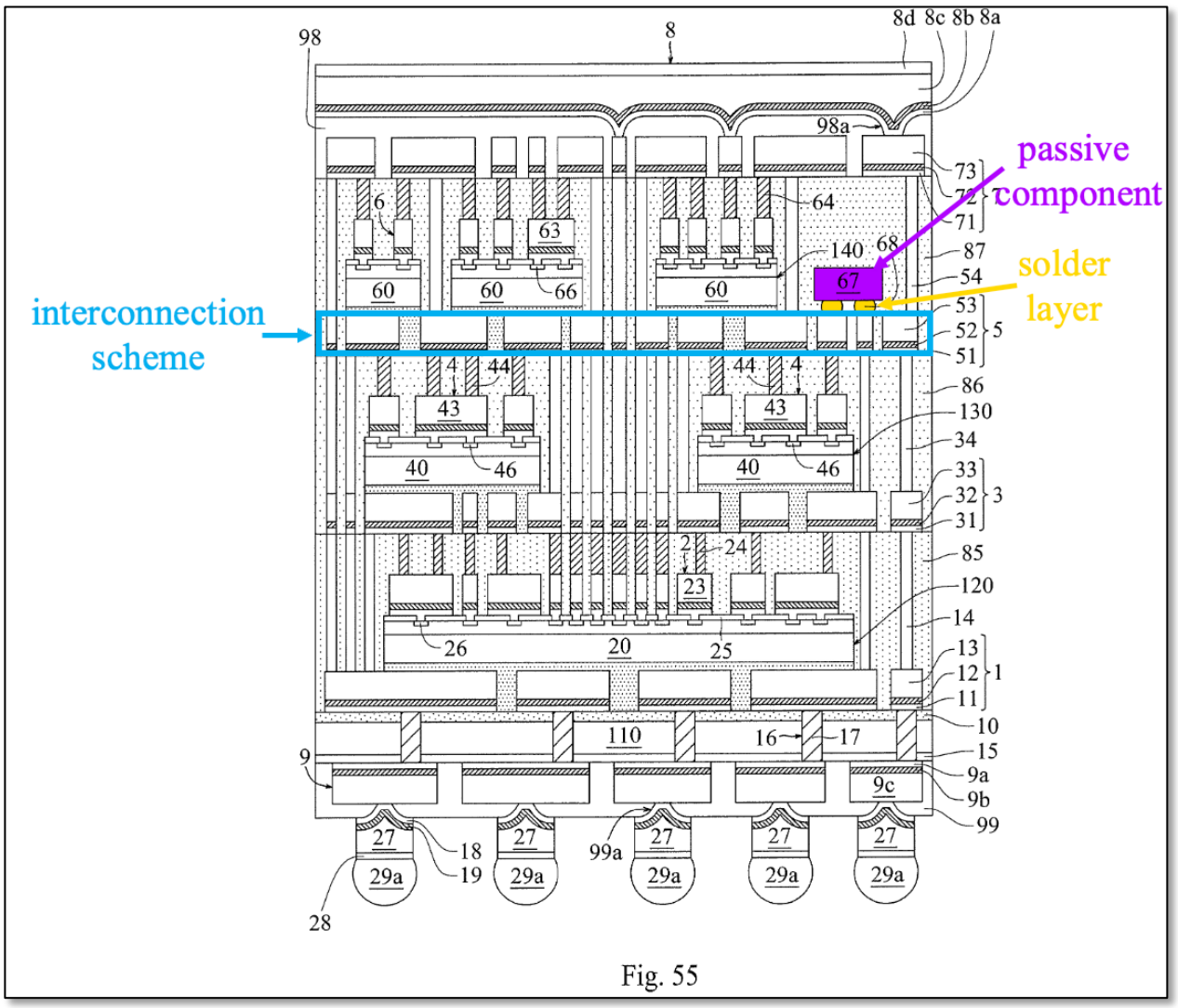


Fig. 55

EX1005, FIG. 55; *EX1003*, ¶382.

In FIG. 84's embodiment, chip 140 is *over* and connected to patterned metal layer 5:

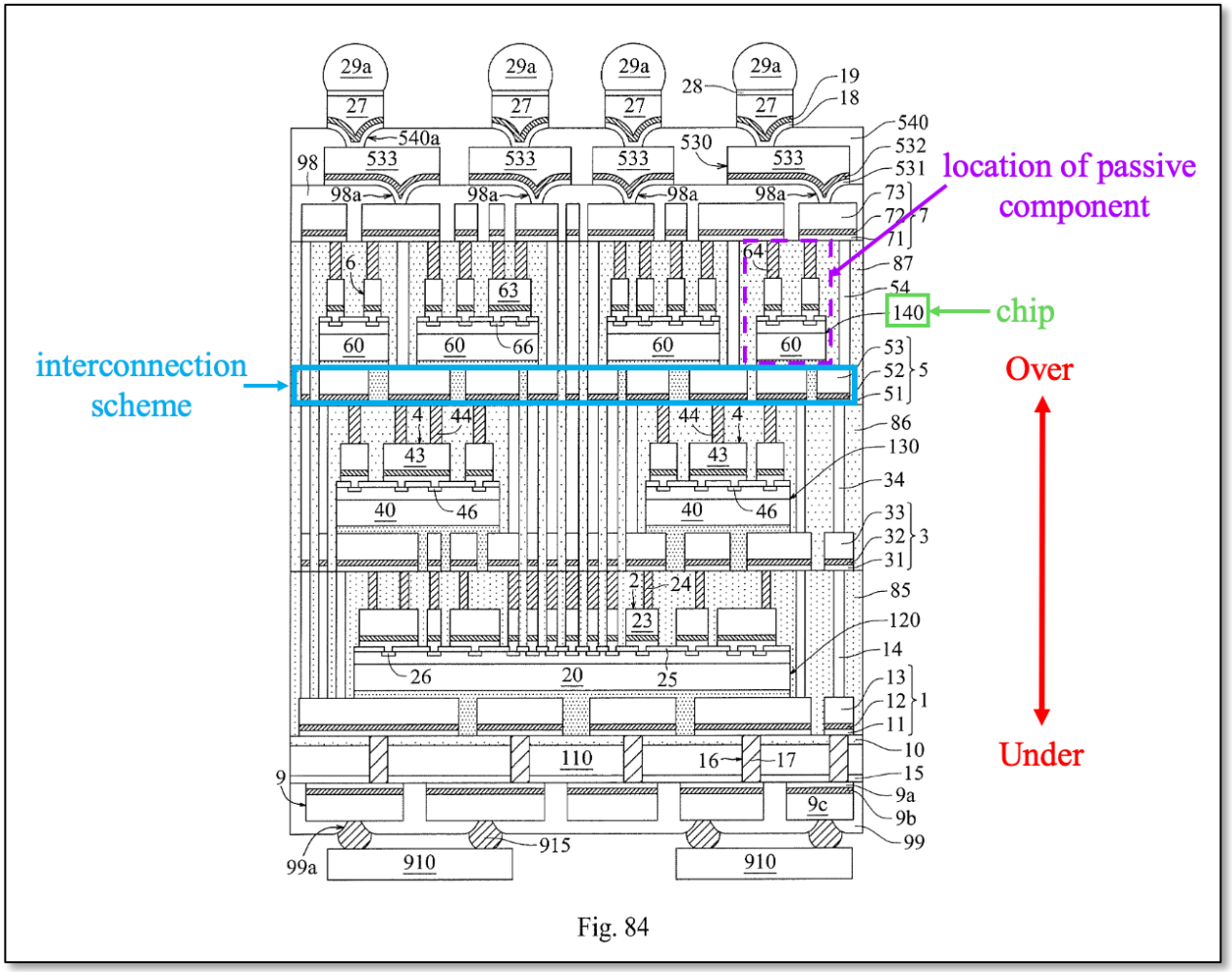


Fig. 84

EX1005, FIG. 84, [0273], [0340-0341]; *EX1003*, ¶383.

Lin-191 expressly discloses replacing chip 140 with passive component 67. *EX1005*, [0340]. Accordingly, Lin-191 teaches or renders obvious passive component 67 *over said first interconnection scheme* (layers 5). Upon replacing chip 140 with passive component 67, passive component 67 is connected to an

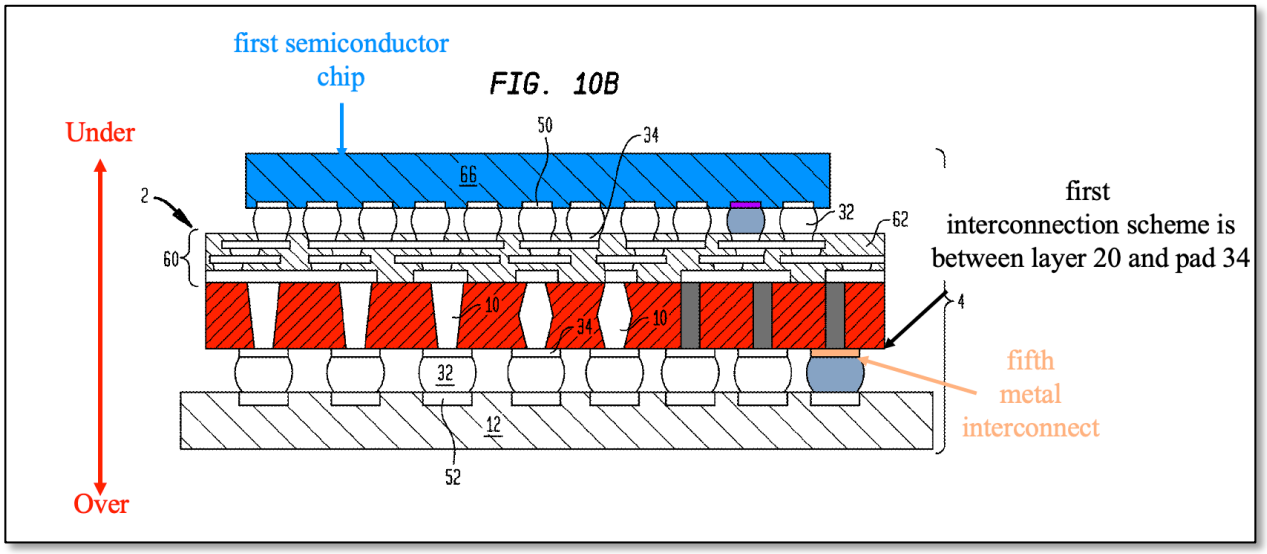
interconnection scheme through a *solder layer* (solder joints 68), as shown in FIG. 55. *EX1005*, [0340]; *EX1003*, ¶384. To the extent there is any dispute regarding Lin-191's express disclosure of replacing chip 140 with passive component 67, a POSITA would have found this same structure obvious in view of the same disclosures because the modification is the application of a known technique (a passive component connected to an interconnection scheme via a solder joint) to a known device (Lin-191's package) to yield the predictable result of Lin-191's FIG. 84 embodiment having a passive component 67 in place of a chip 140. *EX1003*, ¶384.

b) MTC

A POSITA would have been motivated and found obvious to modify Haba per Lin-191 such that a *passive component* was connected to a metal interconnect in Haba's *first interconnection scheme through a solder layer*. *EX1003*, ¶386. Connecting a passive component, e.g., a capacitor, over RDL 70 would advantageously mitigate signal desynchronization and preserve signal integrity. *Id*. The modification is the application of a known technique (passive component) to a known device (Haba's chip package) to yield predictable results. *EX1003*, ¶387 . A POSITA would have had a REOS because soldering passive components into chip packages was a well-established industry practice before the '768 Patent. *Id.*

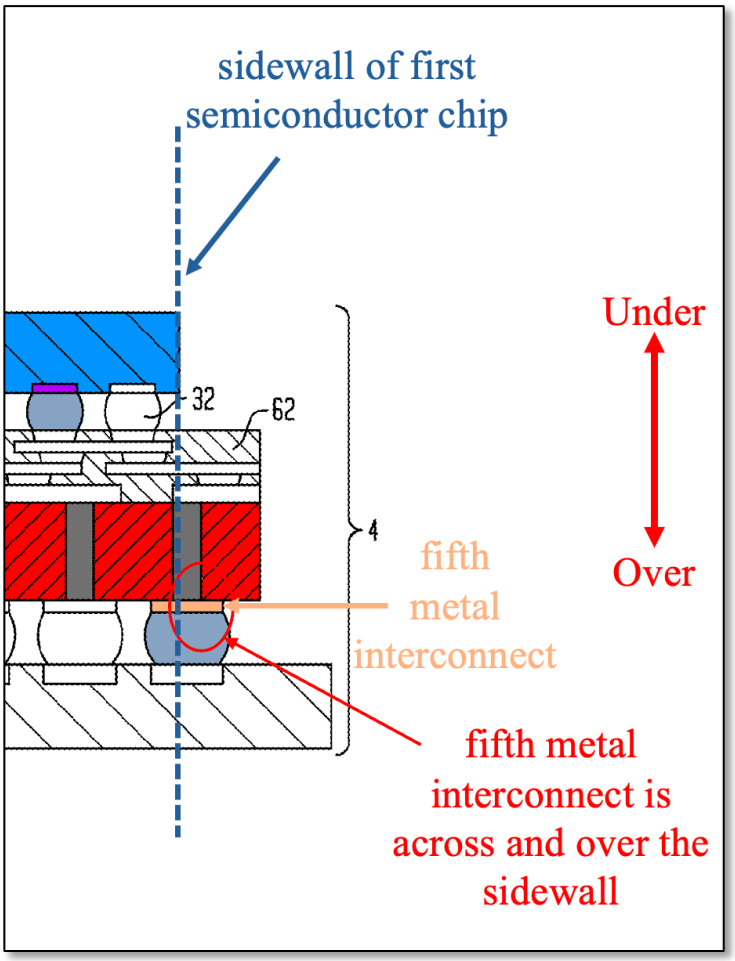
D. Claim 3

Haba's *first interconnection scheme* comprises a *fifth metal interconnect*, i.e., contact pad 34.



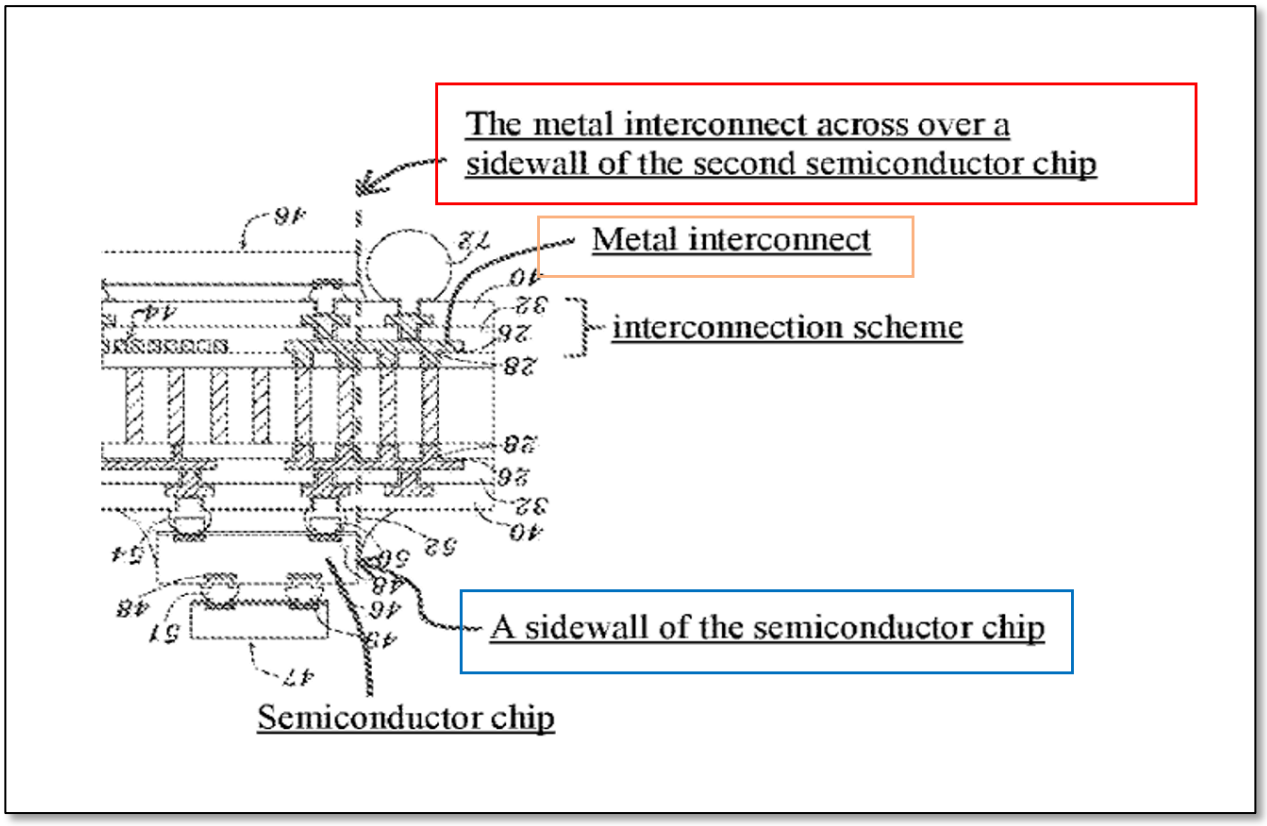
EX1009, FIG. 10B; 8:12-17; Section VII.B.15 (discussing RDL 70 in FIG. 10B); *EX1003*, ¶¶388-390.

Pad 34 is *over* a sidewall of element 66 because it is positioned on the opposite side of layer 20 (*over*) from element 66's *sidewall*. Additionally, pad 34 comprises a portion extending laterally beyond the *sidewall*; thus, pad 34 is *across* the *sidewall*.



EX1009, FIG. 10B; *EX1003*, ¶¶391-392.

Haba's teachings mirrors PO's statements regarding *across over* made in original prosecution:



EX1002, 537; Section V.C; *EX1003*, ¶393.

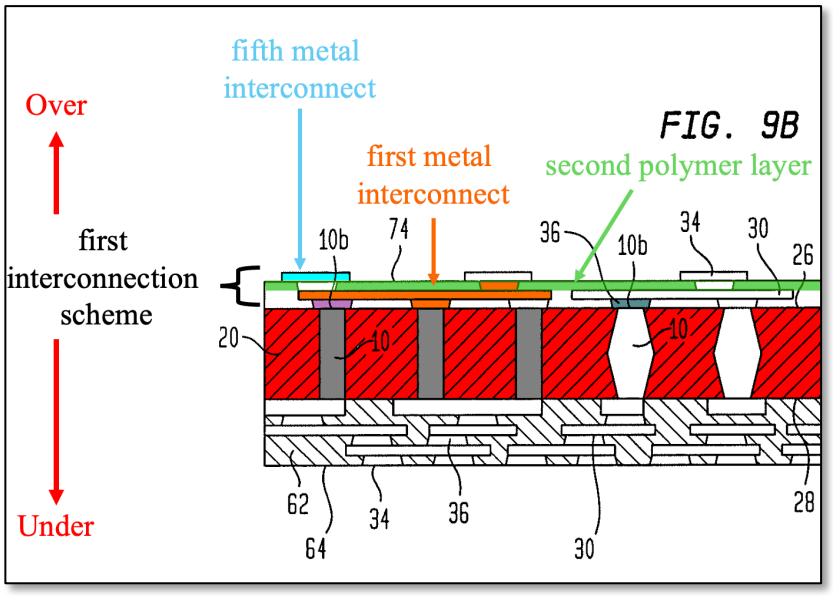
E. Claim 5

The same MTCs and REOS for modifying Sundaram per Lin-191 apply to Haba-Lin-191, e.g., increasing the functionality of Haba's *chip package*. Section V.E; *EX1003*, ¶¶394-395.

F. Claim 7

1. 7(a)

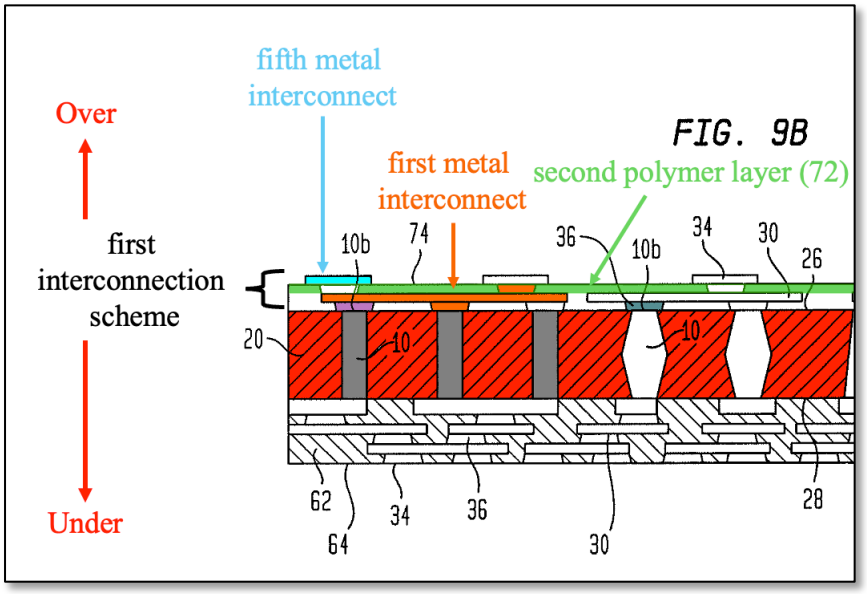
Pad 34 is a *fifth metal interconnect* on surface 74 and, therefore, *over said first metal interconnect and said second polymer layer*. Sections VII.B.11, VII.B.18 (pads 34 are *metal*).



EX1009, FIG. 9B (excerpt); *EX1003*, ¶¶396-398.

2. 7(b)

Redistribution dielectric 72 is *between said first and fifth metal interconnects*:



EX1009, FIG. 9B (excerpt); *EX1003*, ¶399.

3. 7(c)

a) Lin-191's Teachings and MTC

Lin-191's UBM layer teaches the claimed layers, where adhesion layer 18 is a *third metal layer,* seed layer 19 is *a sixth copper layer on* adhesion layer 18, and metal layer 27 is a *seventh copper layer* on seed layer 19. *EX1005*, [0308-0309], [0313], [0323]; Section V.G.3.

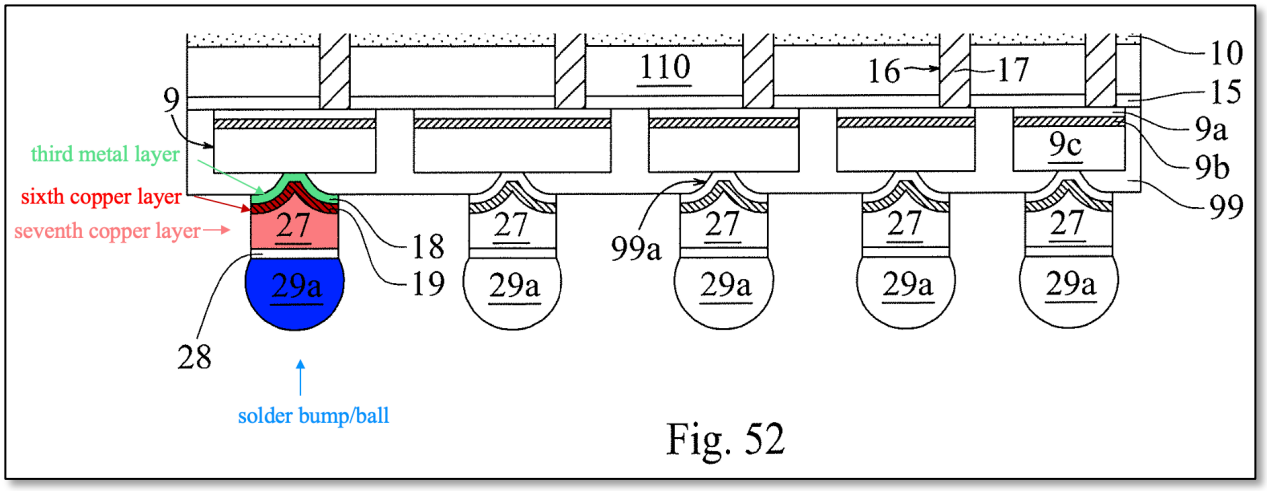


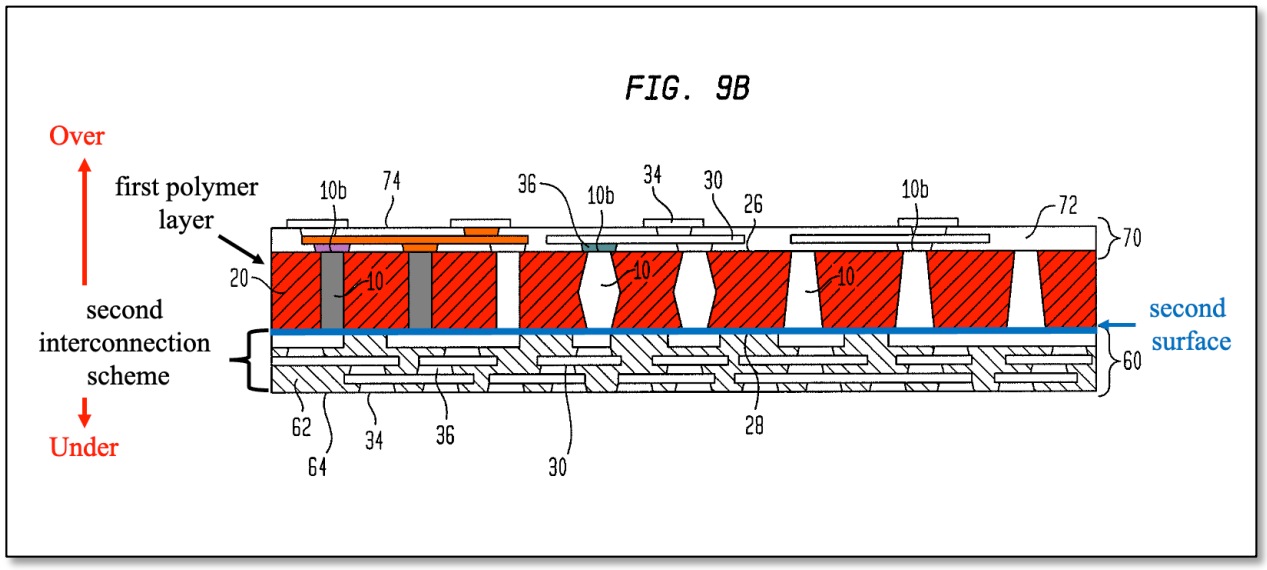
Fig. 52

EX1005 at FIG. 52; *EX1003,* ¶400.

A POSITA would have found obvious, been motivated, and had a REOS in modifying Haba's pad 34 for the same reasons discussed for modifying Sundaram's similar pad 135. Section V.G.3.b. Because pad 34 connects to solder ball 32, a POSITA would have found it advantageous to modify pad 34 to include UBM layers to improve solder reliability. *EX1003*, ¶401.

G. Claim 8

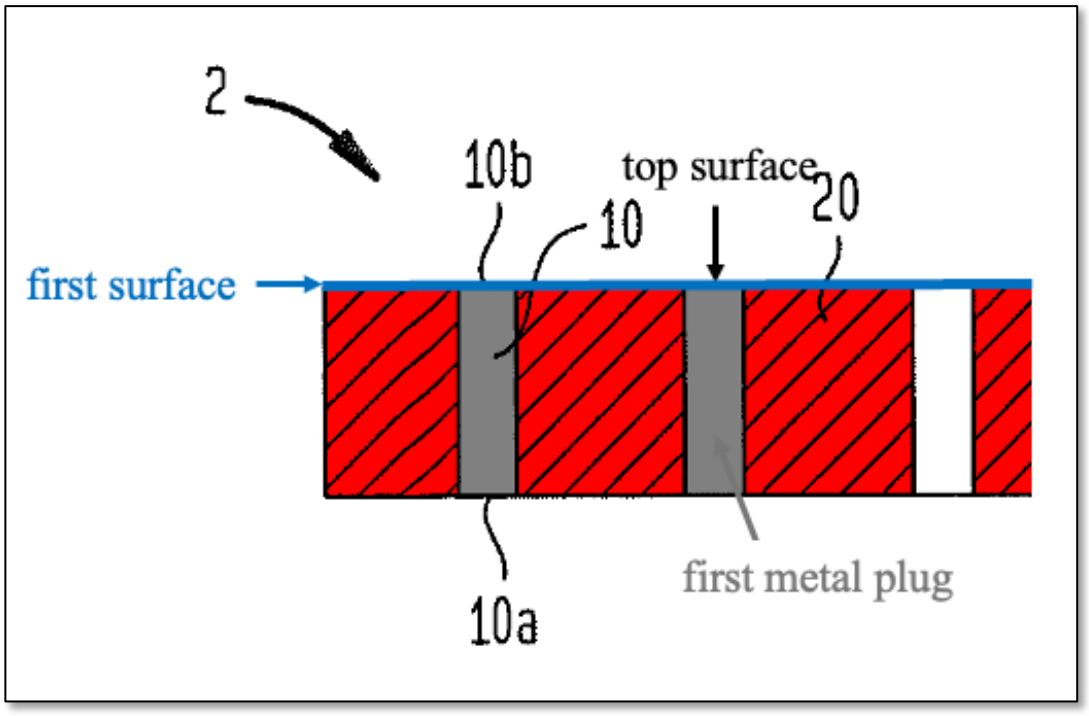
Haba teaches a *second interconnection scheme on* surface 28 (*second surface*) formed by traces 30, vias 36, and pads 34 in RDL 60. Because Haba's RDL 60 is on surface 28, the RDL 60 is *under* dielectric layer 20 (*first polymer layer*).



EX1009, FIG. 9B; *EX1003*, ¶¶402-403.

H. Claim 9

Surface 26 is "**coplanar** with end surfaces 10B of the posts 10." *EX1009*, 10:8-10. Thus, surface 10B (*a top surface*) of post 10 (*first metal plug[]*) is *substantially coplanar* with surface 26.



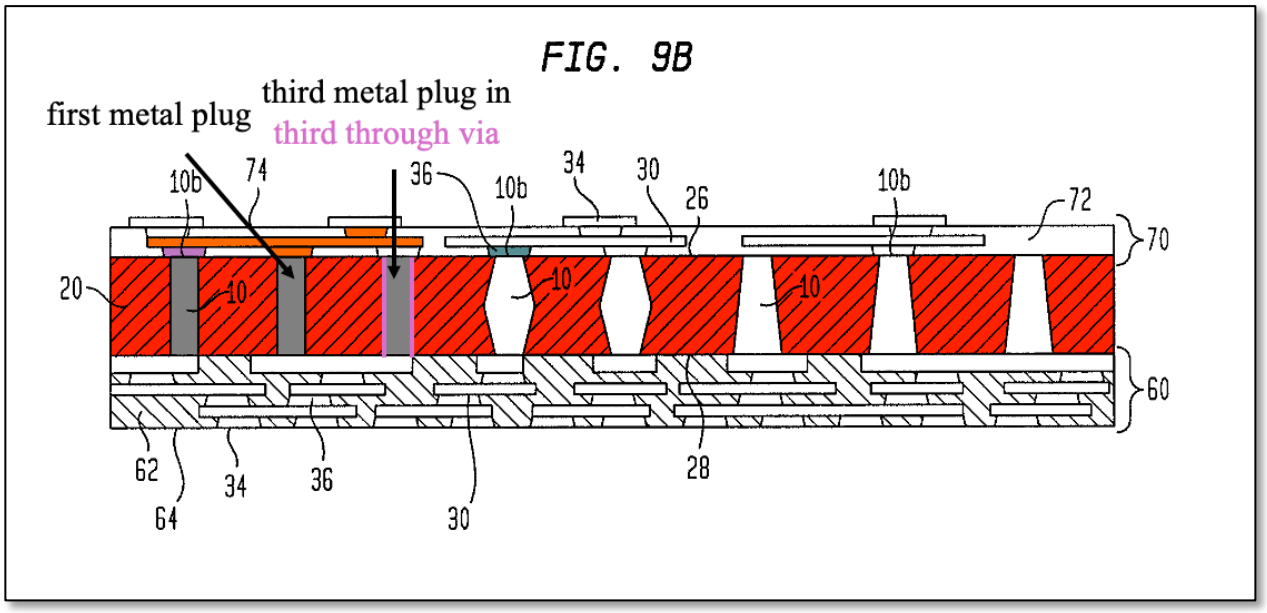
EX1009, FIG. 6B (excerpt); *EX1003*, ¶404.

I. Claim 10

Section V.J. The same MTCs and REOS apply.

J. Claim 14

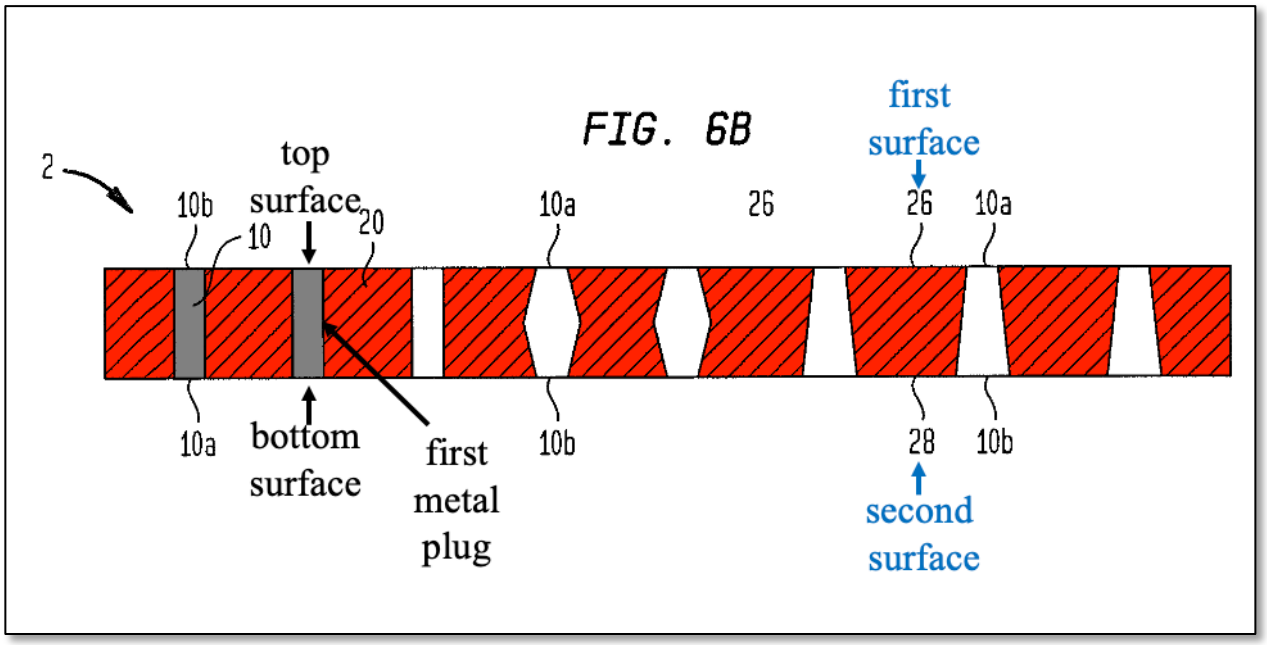
Haba teaches a third post 10 *vertically in a third through via in said first polymer layer*.



EX1009, FIG. 9B. Posts 10 have "a pitch" of "**400-650** mm" teaching or rendering obvious the claimed range. *EX1009*, 5:34-38; *EX1003*, ¶¶406-407; Section V.N.

K. Claim 15

Haba teaches or renders obvious layer 20 having the claimed *thickness*. Section VII.B.4. Additionally or alternatively, layer 20 is modified, per Lin-191, to be "between about 10 and 150 micrometers." *EX1005*, [0290]. Sections VII.B.4.a-b. Post 10 is embedded within layer 20 and has surfaces 10A, 10B coplanar with surfaces 26, 28 such that post 10 has a *thickness* equal to the thickness of layer 20, i.e., at least 10 mm or 10-150 micrometers, thus teaching or rendering obvious the claimed range.



EX1009, FIG. 6B, 10:8-13; *EX1003*, ¶¶408-410; Sections V.A.4, V.O, VII.A.4.

VIII. GROUND 2B: CLAIMS 4, 6, 11-13 ARE OBVIOUS OVER HABA, LIN-191, AND SUNDARAM

A. Claim 4

1. 4(a)

a) Sundaram's Teachings

Device 130 is *a second semiconductor chip over said first interconnection scheme*. Section V.D.1.

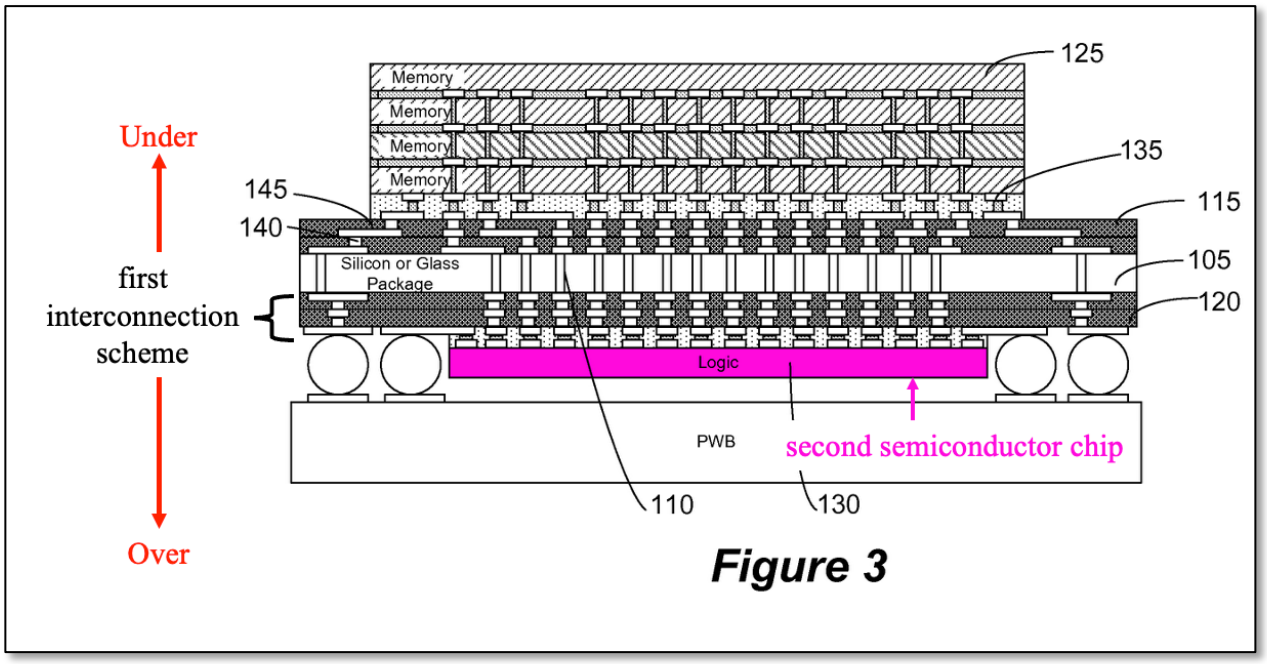


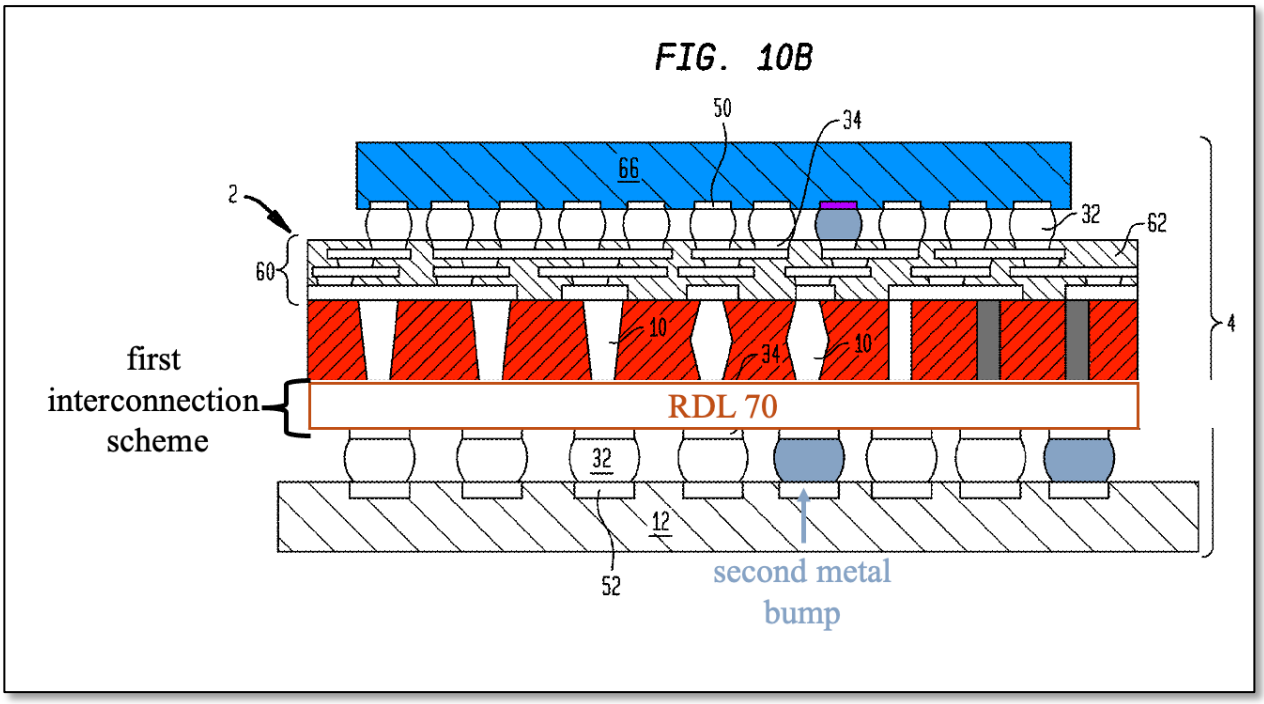
Figure 3

EX1004, FIG. 3. Section VIII.A.3 (MTC and REOS); *EX1003*, ¶411.

2. 4(b)

a) Haba's Teachings

Haba teaches *a second metal bump* (solder ball 32).



EX1009, FIG. 10B; *EX1003*, ¶412.

b) Sundaram's Teachings

Additionally, or alternatively, device 130 teaches Claim 4(b). Section V.D.2; *EX1003*, ¶413.

3. Claim 4 MTC

A POSITA would have been motivated and found obvious to include a semiconductor chip *over* Haba's *first interconnection scheme* to incorporate additional chips to add functionality as it was well-understood and envisioned by Haba to have multiple chips in a chip package. *EX1009*, 8:18-40, 1:20-21; *EX1003*, ¶¶414-417.

Placing a chip between RDL 70 and PCB 12 (*over said first interconnection scheme*) advantageously maximizes space and provides a shorter path length to the

PCB. *EX1003*, ¶415.Connecting the *second semiconductor chip* to RDL 70 using micro-bumps (per Sundaram) would beneficially maintain the connection between solder balls 32 and PCB 12 without increasing the overall width of Haba's *chip package*. *Id*.

The combination is the application of a known technique (a chip connected by bumps between an interposer and a PCB/PWB) to a known device (Haba's *chip package*) to yield the predictable result of Haba's *chip package* having a semiconductor chip over the interconnection scheme. *EX1003*, ¶418.

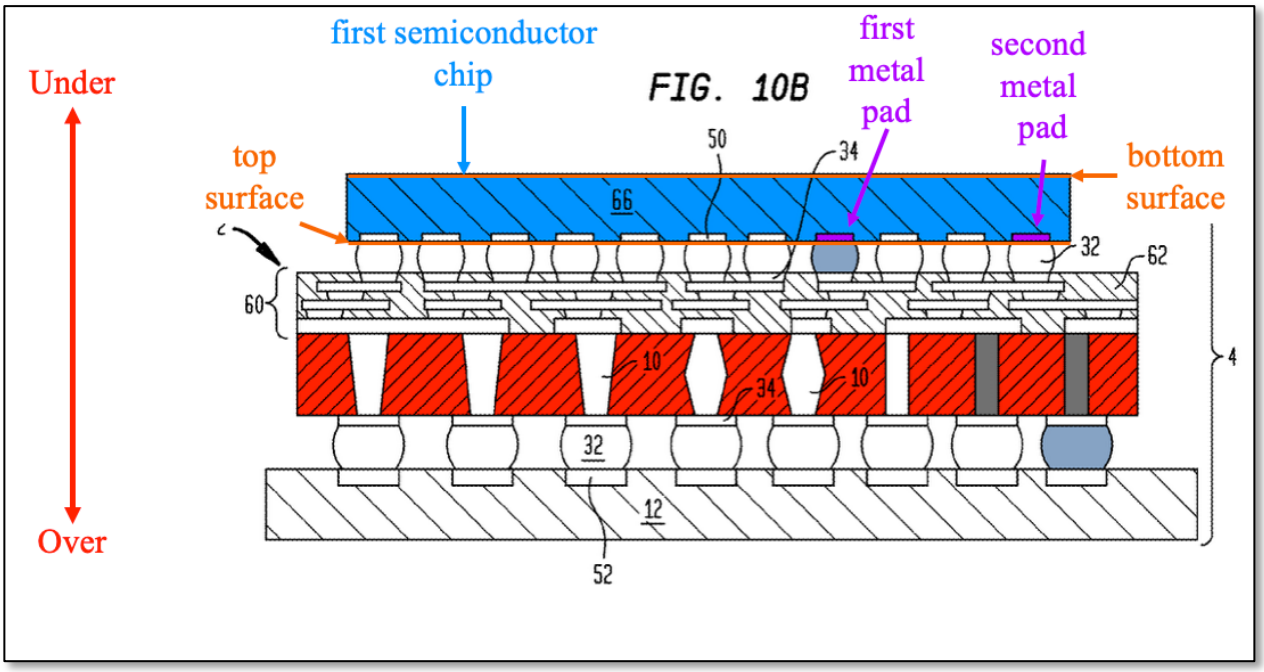
There is a REOS because chip packages with chips on both sides of an interposer were well-known and straightforward to manufacture. *EX1003*, ¶419.

B. Claim 6

1. 6(a)

a) Haba's Teachings

A second contact 50 is *a second metal pad on a top surface of said first semiconductor chip*. Section VII.B.18.



EX1009, FIG. 10B; *EX1003*, ¶420.

b) Sundaram's Teachings

Sundaram teaches *a third metal pad on a bottom surface* of a *semiconductor chip*. Section V.F.1.

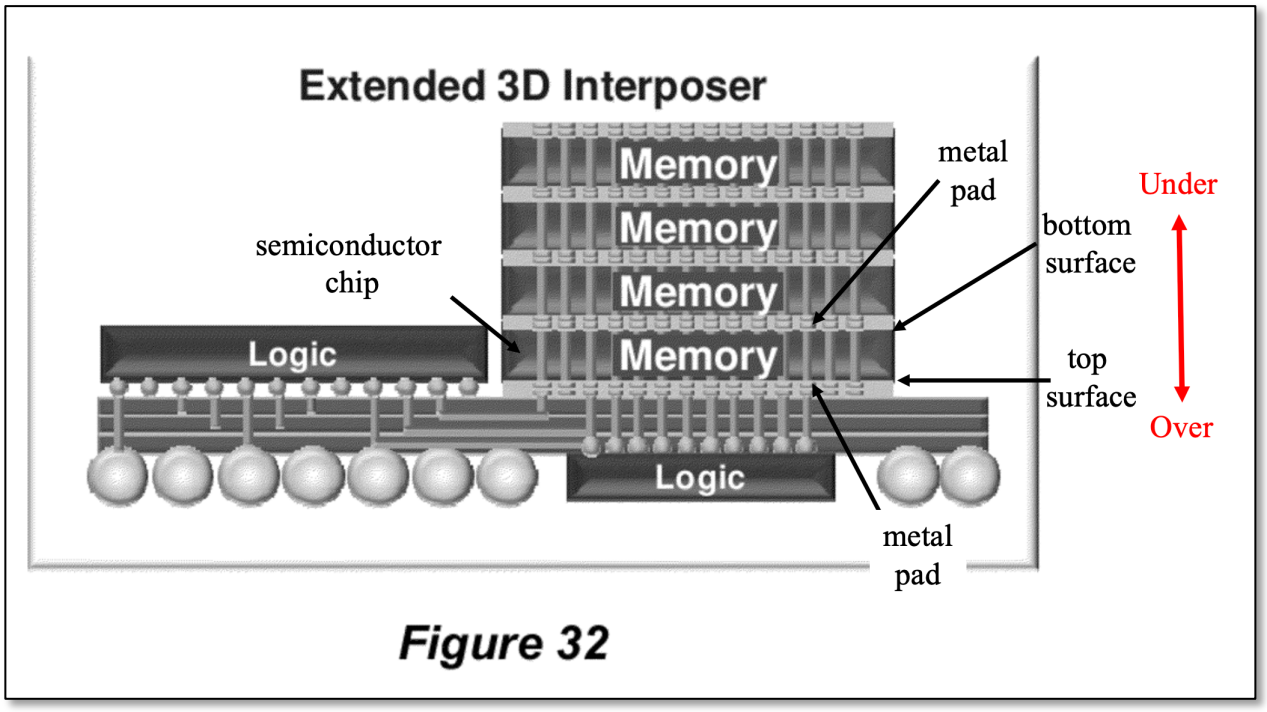


Figure 32

EX1004, FIG. 32. Section VIII.B.3 (MTC and REOS); *EX1003*, ¶421.

2. 6(b)

Sundaram teaches *TSV metal layer[s] connect[ing]* pads on a *semiconductor chip.* Section V.F.2.

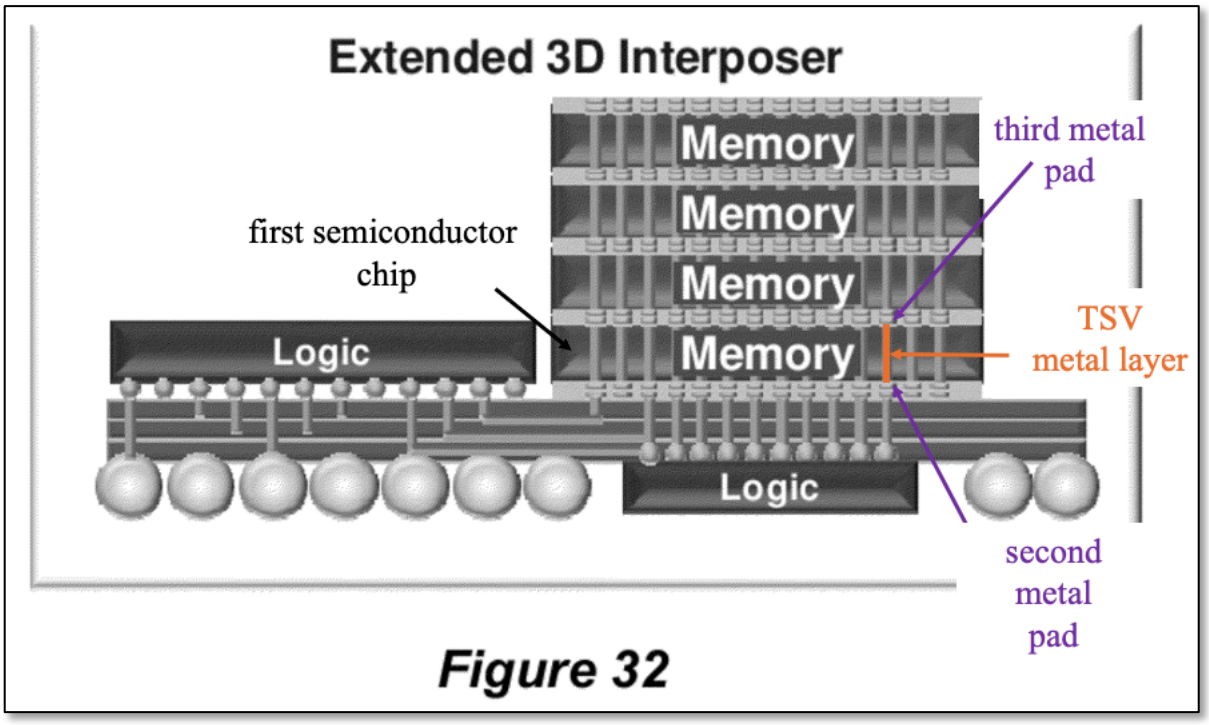


Figure 32

EX1004, FIG. 32; *EX1003,* ¶422.

3. Claim 6 MTC

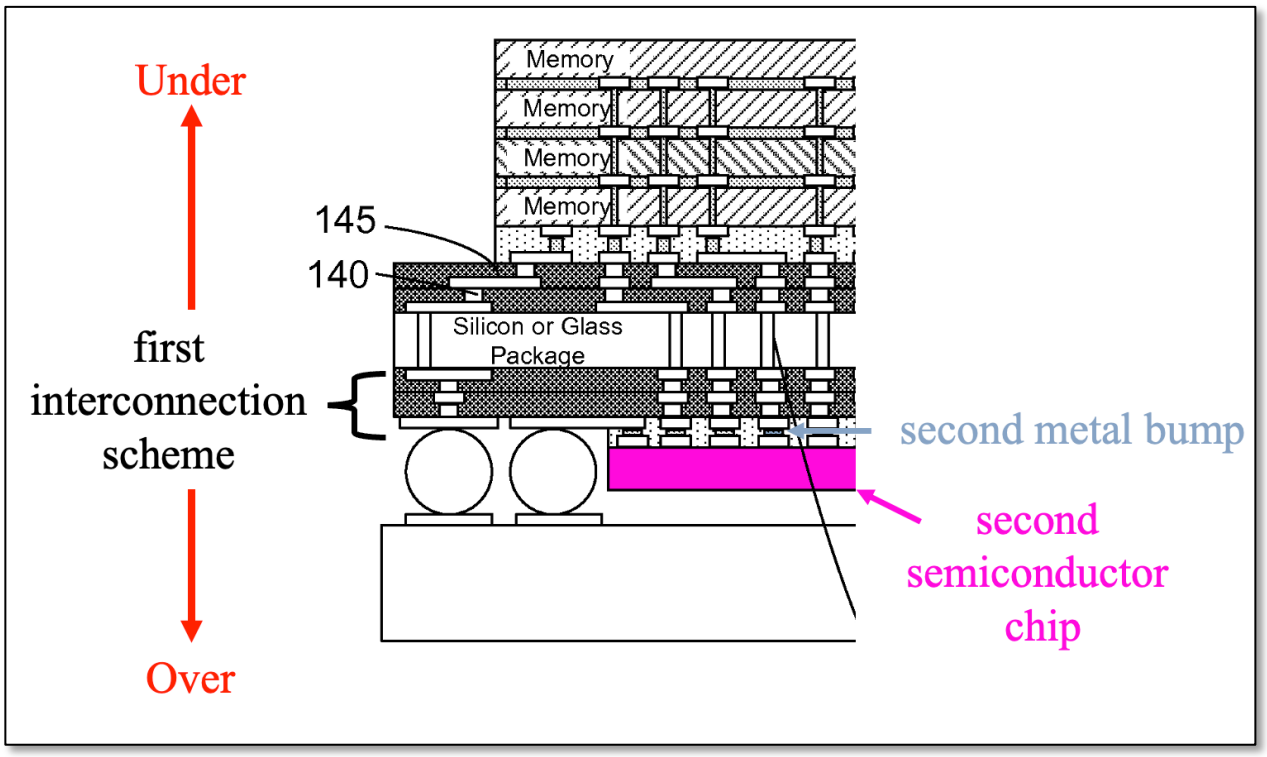
A POSITA would have found obvious and been motivated to modify Haba per Sundaram such that a *third metal pad* is on the *bottom surface* of element 66 to electrically connect to Haba's *second metal pad through a through-silicon-via metal layer*. *EX1003*, ¶423. The modification would have advantageously enabled additional semiconductor chips to be incorporated and connected to element 66. *EX1003*, ¶¶424-426. A POSITA would have found obvious to also modify element 66 to have a *third metal pad* enabling other components in the chip package to connect to the TSV. *EX1003*, ¶425.

The modification is the application of a known technique (chips with TSVs connecting metal pads) to a known device (Haba's *chip package*) to yield the predictable result of Haba's chip element 66 having a TSV to connect to other chips in the package. *EX1003*, ¶428. A POSITA would have had a REOS because chips with TSVs were well-known and routinely manufactured. *EX1003*, ¶429.

C. Claim 11

1. 11(a)

Sundaram teaches Claim 11(a). Sections VIII.A, V.K.1. Sundaram's *second metal bump connect[s]* the *second semiconductor chip to said first interconnection scheme*. *EX1004,* 6:29-33; *EX1003*, ¶430.



EX1004, FIG. 3 (excerpt).

2. 11(b)

Sundaram teaches Claim 11(b). Section V.K.2. A POSITA would have found obvious and been motivated to modify Haba's *chip package* with a *second semiconductor chip* having a *height* as claimed so the *second semiconductor chip* would advantageously not impede the connection of Haba's bumps 32 to PCB 12. *EX1003*, ¶¶431-434.

D. Claim 12

a) Sundaram's Teachings and MTC

Sundaram teaches Claim 12. Section V.L. A POSITA would have found obvious and been motivated to modify Haba per Sundaram's teachings of a *second semiconductor chip under* a *first chip* that has *a second metal pad connected to a third metal pad via a solder layer*. *EX1003*, ¶435. A POSITA would have been motivated to incorporate additional chips into Haba's *chip package* to add functionality. Sections VIII.A, VIII.D.

The modification is the application of a known technique (stacking chips using metal pads and solder layers) to a known device (Haba's *chip package*) ready for improvement to yield predictable results. *EX1003*, ¶436. There would have been a REOS because the modification would have been straightforward and only required forming metal pads on semiconductor chips and connecting them using a solder layer. *Id*.

E. Claim 13

1. 13(a)

Sundaram teaches a *second semiconductor chip under a first semiconductor chip*. Section V.M.1.

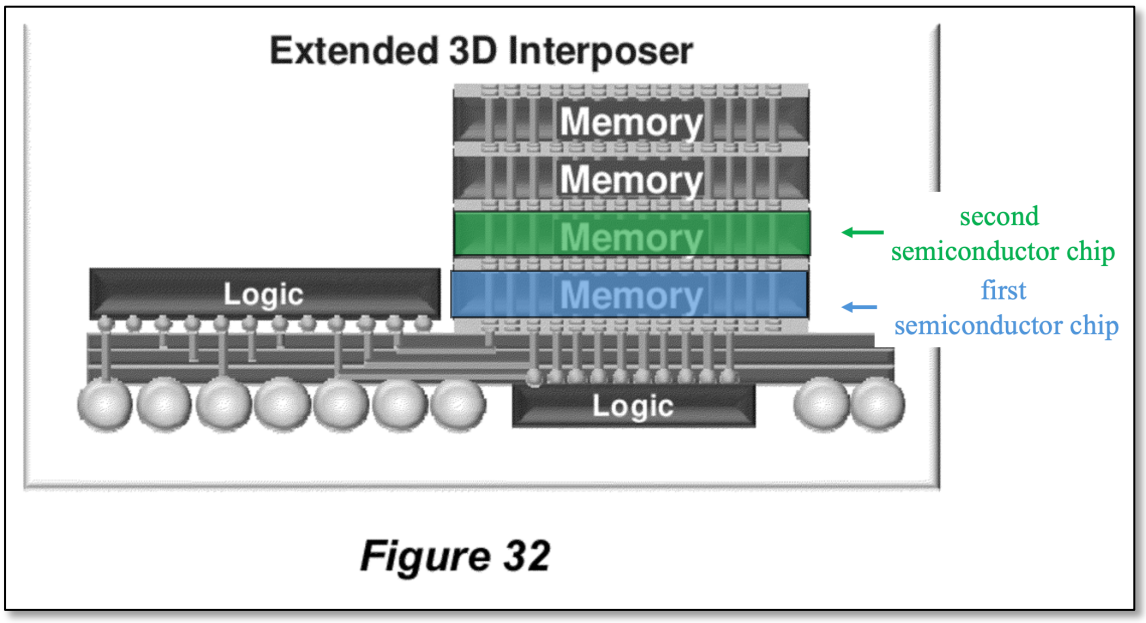


Figure 32

EX1004, FIG. 32; Section VIII.E.5 (MTC and REOS); *EX1003*, ¶437.

2. 13(b)

Section VIII.B.1.

3. 13(c)

Section VIII.B.2.

4. 13(d)

Sundaram's *second semiconductor chip* comprises a *fourth metal pad connected to* a *third metal pad*. Section V.M.4.

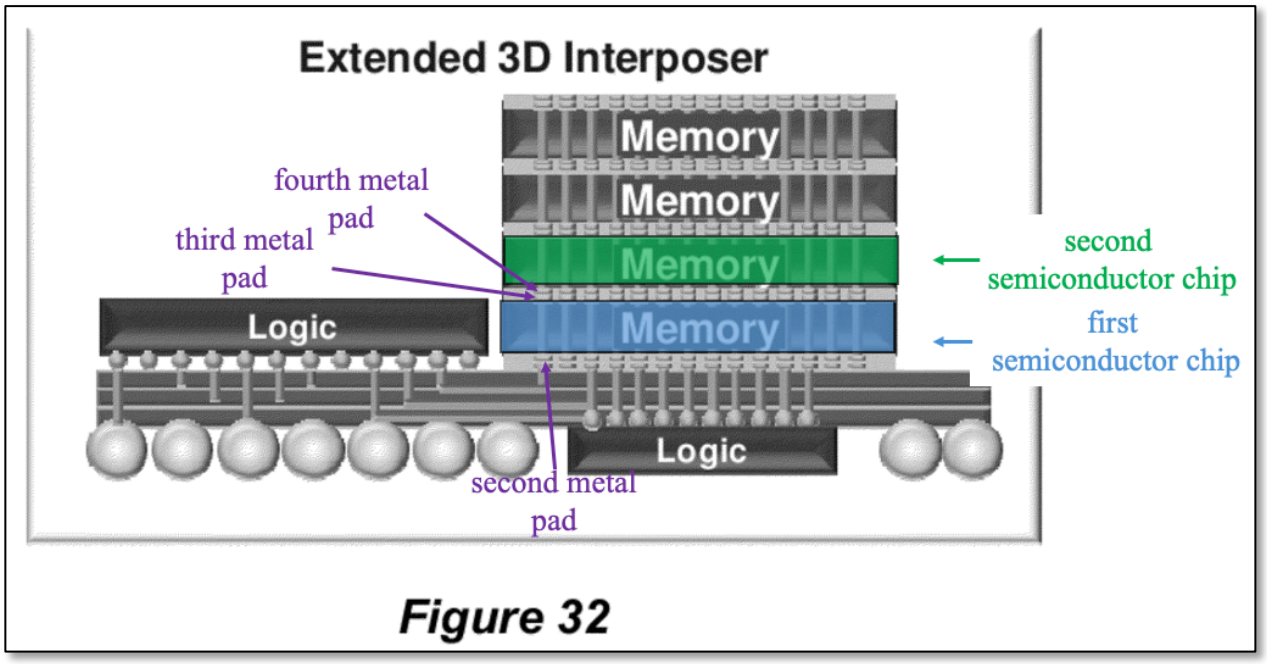


Figure 32

EX1004, FIG. 32; *EX1003*, ¶440.

5. Claim 13 MTC

Section VIII.B.3 (Claim 6's MTC and REOS). A POSITA would have been motivated to modify Haba's to include *a second semiconductor chip under said first semiconductor chip* to efficiently use space and increase functionality of Haba's chip package. *EX1003*, ¶¶441-443.

The modification is the application of a known technique (stacking chips) to a known device (Haba's *chip package*) to yield the predictable result of multiple chips connected via TSVs. *EX1003*, ¶444. The modification would have been straightforward and merely required forming a TSV connecting metal pads and had a REOS. *Id*.

IX. GROUND 3A: CLAIMS 16-17, 19, AND 22-28 ARE OBVIOUS OVER YU AND LIN-191

A. Claim 16

1. 16(Pre)

Yu teaches a "PoP [Package-on-Package] structure" comprising "multiple packages 202", which includes dies (e.g., "a logic circuitry die, a memory die, or any other die") such that the PoP structure is a *chip package*. *EX1010*, 8:35-36, 2:50-51, 1:49-51; *EX1003*, ¶¶445-446.

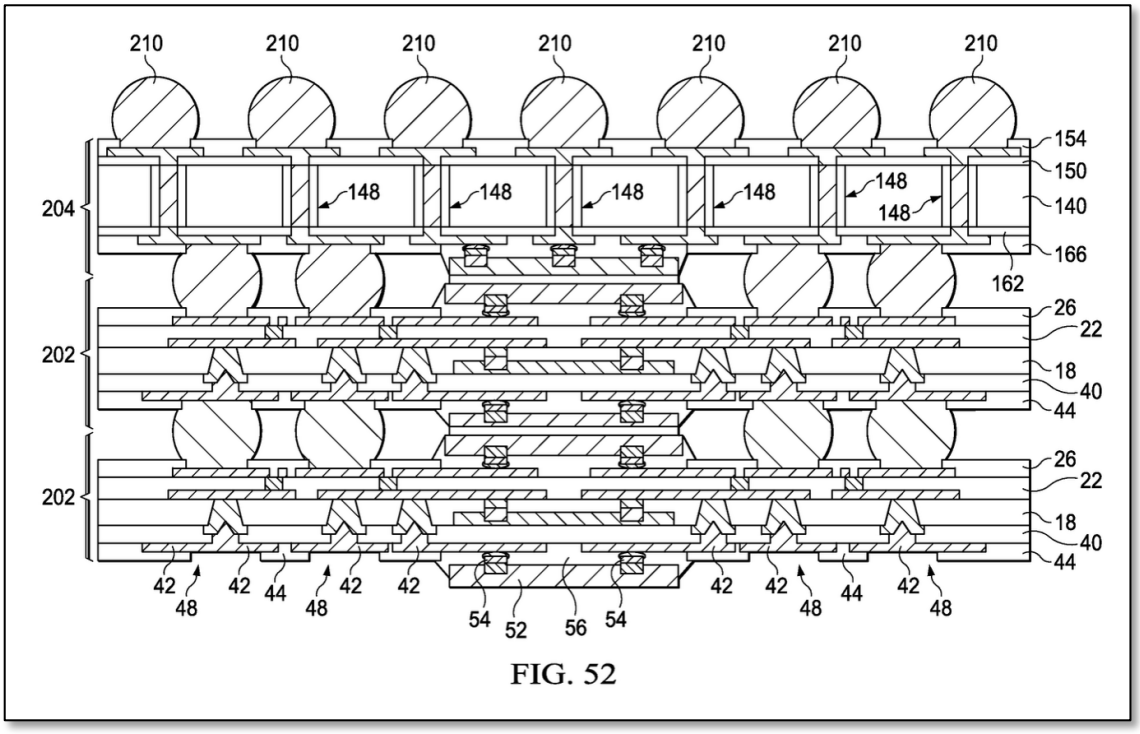


FIG. 52

EX1010, FIG. 52.

One of the packages 202 in Yu's *chip package* is shown in FIG. 16:

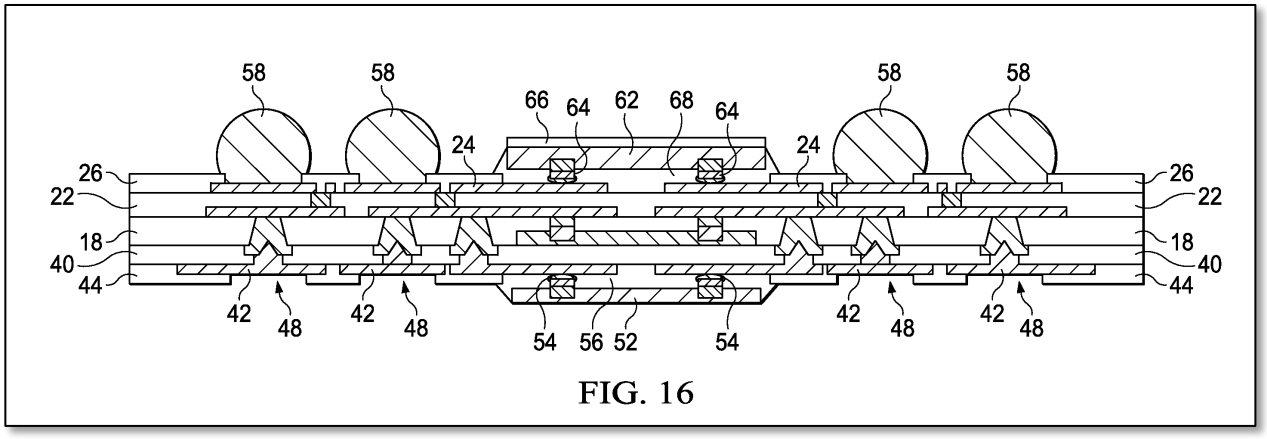


FIG. 16

EX1010, FIG. 16, 8:11-13, 4:67-5:7 (describing relationship between FIGS. 16, 52); *EX1003*, ¶¶447-448.

2. 16(a)

Yu's package includes "molding compound 18 [that] can be [] epoxy, polyimide," i.e., *a first polymer layer*, which has *a first surface opposite to a second surface*:

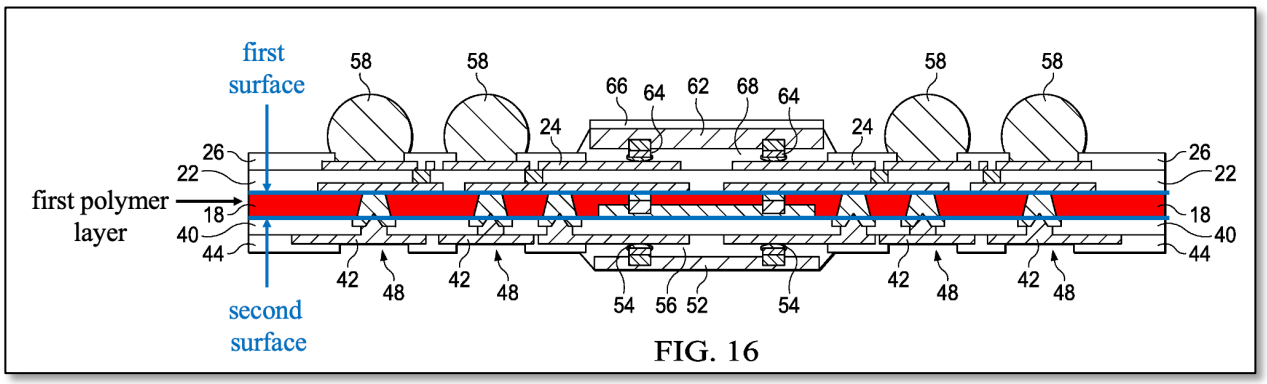


FIG. 16

EX1010, FIG. 16, 2:61-64; *EX1003*, ¶¶449-450.

3. 16(a)(i)

The *first surface is substantially parallel to said second surface*:

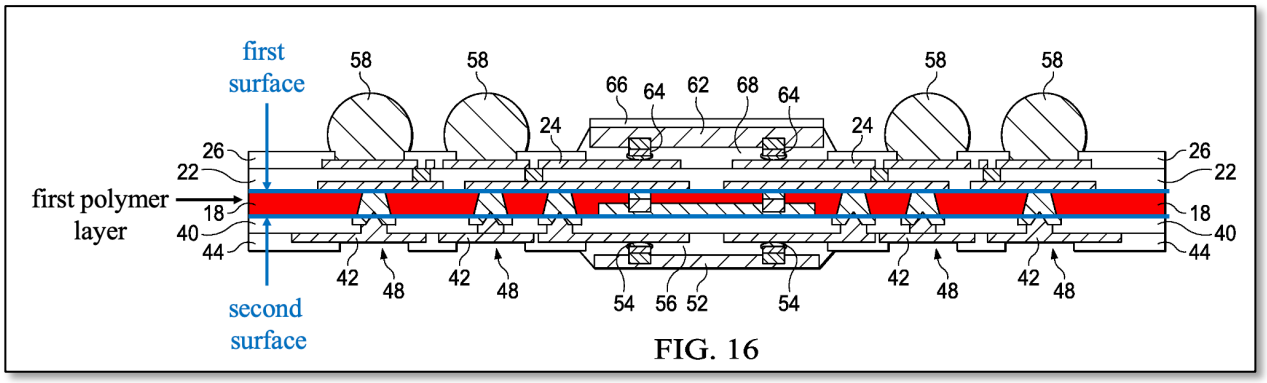


FIG. 16

EX1010, FIG. 16; *EX1003*, ¶451.

4. 16(a)(ii)

a) Lin-191's Teachings

Lin-191 teaches or renders obvious Claim 16(a)(ii).

Lin-191's package includes "encapsulating layer 85" formed "on…metal pillars or bumps 14" (analogous to Yu's through mold vias (TMVs), discussed at Claim 16(b)). *EX1005*, [0109]. Layer 85 includes "a polymer layer" such that layer 85 is a *first polymer layer*, similar to Yu's molding compound 18. *Id*. Encapsulating layer 85 has a thickness "between about 20 and about 500 micrometers" encompassing the claimed *thickness between 100 and 300 micrometers*. *EX1005*, [0109-0111]; *EX1003*, ¶¶452-453. Because Lin-191 teaches a range of 20-500 micrometers that includes the narrower claimed range of *100-300 micrometers*, Lin-191 teaches or renders obvious Claim 16(a)(ii). Section V.A.4 (supporting caselaw and discussion of '768 Patent not ascribing criticality to the claimed *thickness*); *EX1003*, ¶455.

Additionally or alternatively, layer 85 has a *thickness* equivalent to the combined thickness of layers 1 and bump 14 because layer 85 is "formed…on the metal layer 13 of the patterned metal layer 1," and "top surfaces 14a" of bumps 14 are "substantially coplanar…with a top surface 85a" of layer 85. *EX1005*, [0109-0110], FIG. 12. Lin-191 teaches bumps 14 are "between 20 and 110 micrometers"; layer 11 is "between 1 nanometer and 0.5 micrometers"; layer 12 is "between 10 nanometers and 0.8 micrometers"; and layer 13 is "between 3 and 10 micrometers." *EX1005*, [0121], [0050], [0060]. Thus, Lin-191 teaches layer 85 has a *thickness* between 23.011 micrometers and 121.3 micrometers, overlapping with and teaching or rendering obvious the claimed *thickness*. *EX1003*, ¶454.

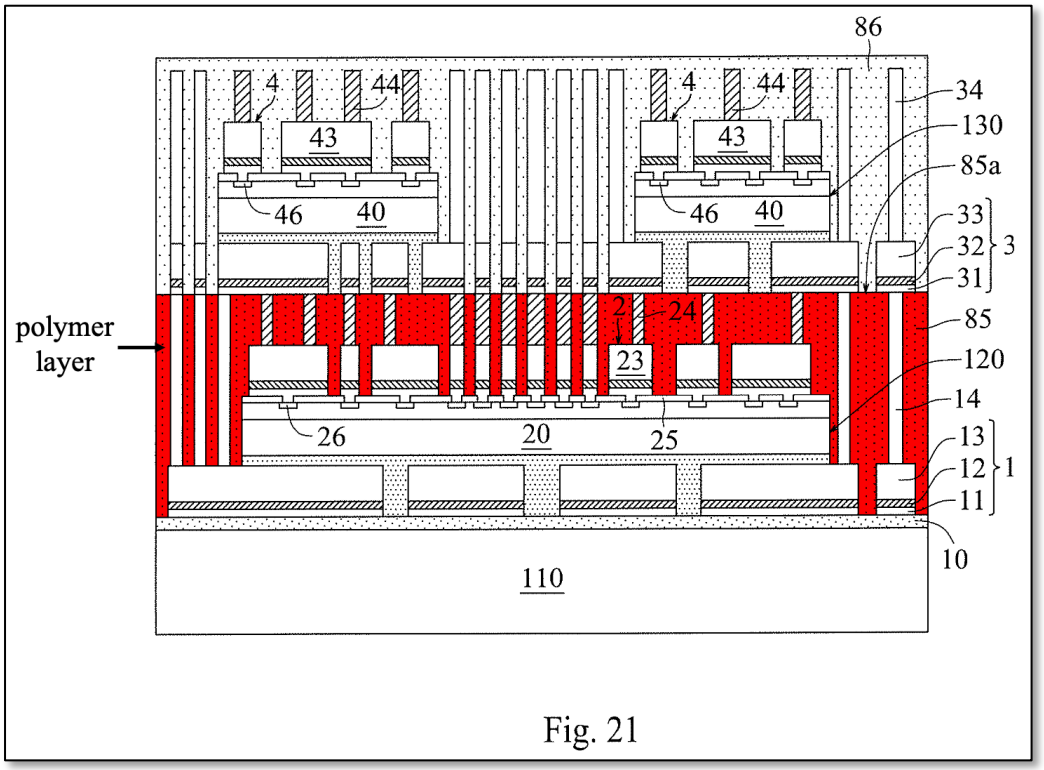


Fig. 21

EX1005, FIG. 12.

b) MTC

A POSITA would have been motivated and found obvious to apply Lin-191's thickness to Yu's molding compound 18 to advantageously provide stress buffering to protect Yu's die 10 embedded in molding compound 18, as Lin-191's thickness was known be appropriate for embedded chip architecture. *EX1003*, ¶¶456-457. Additionally, Lin-191's thickness would desirably allow for the opportunity to incorporate shielding layers. *EX1003*, ¶¶458-459.

The Yu-Lin-191 combination is the application of a known technique to a known device ready for improvement to yield predictable results. *EX1003*, ¶459. A POSITA would have had a REOS because Lin-191's thickness was a common thickness for molding/encapsulation layers before the '768 Patent. *Id*.

5. 16(b)

Yu teaches metal through molding vias (TMVs), each of which is a *metal plug*. Specifically, Yu teaches "TMV openings 36 are formed through the molding compound 18," and a "seed layer is deposited…into the TMV openings 36," followed by deposition of a "conductive material," forming TMVs 38. *EX1010*, 3:56-4:6. Both the seed layer and the conductive material are "copper" (*metal*). *Id*. Thus, a TMV 38 is a *first metal plug…in a first through via in said first polymer layer*. TMV 38 extends from Yu's *first surface* to the *second surface* such that TMV 38 is *vertical*.

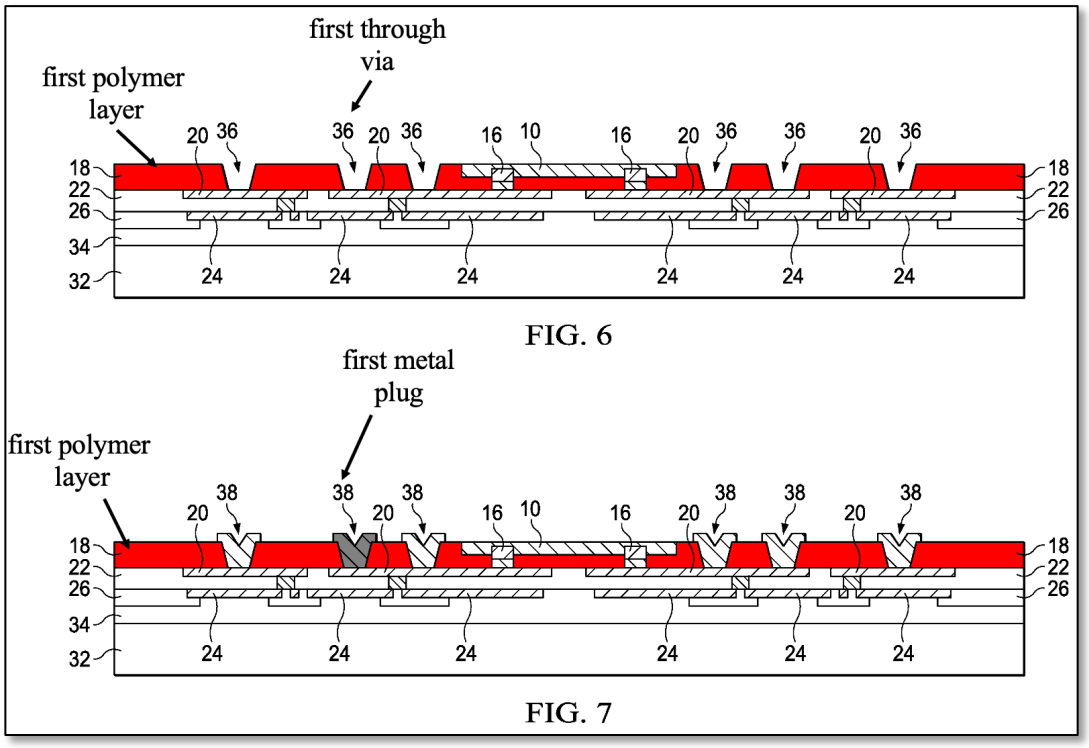


FIG. 6

FIG. 7

EX1010, FIGS. 6-7; *EX1003*, ¶460.

6. 16(b)(i)

TMV 38's copper seed layer "deposited…into the TMV opening[] 36" is *a first copper layer* that *contacts with a sidewall of said first through via*. *EX1010*, 3:60-64; *EX1003*, ¶¶461-462.

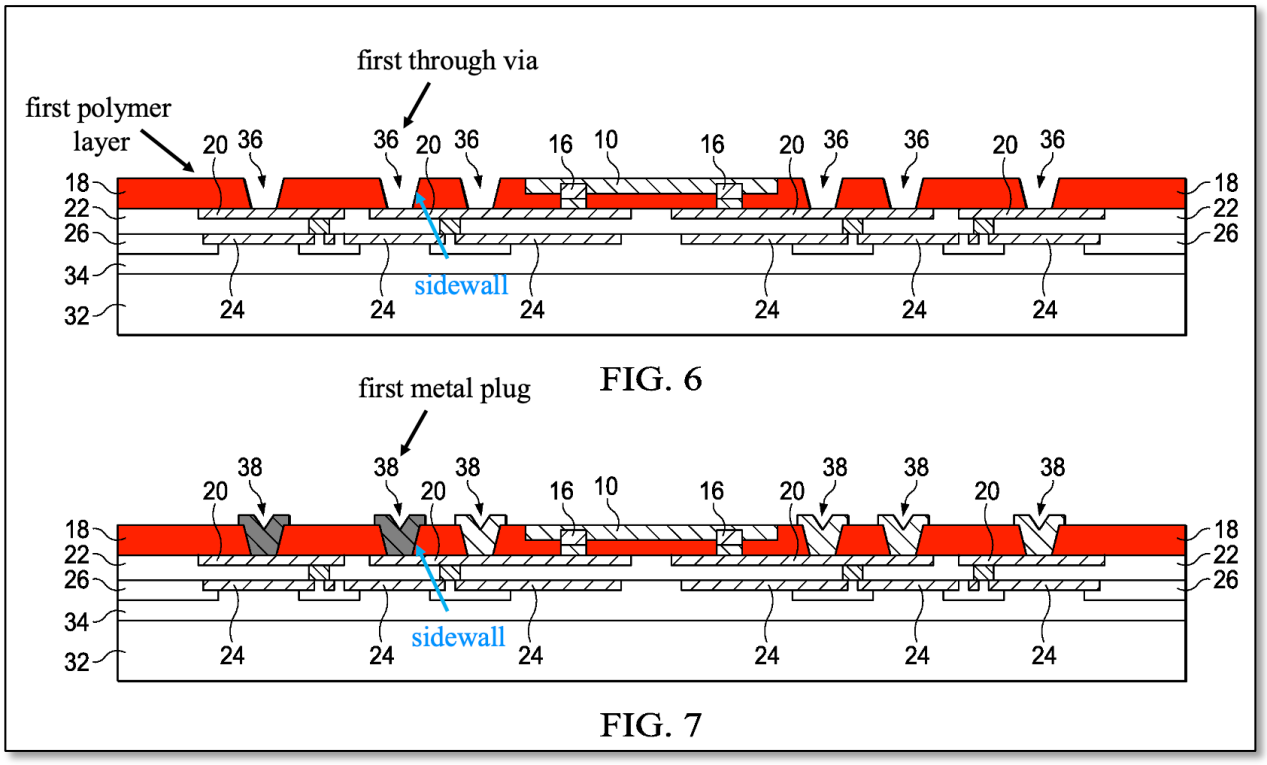


FIG. 6

FIG. 7

EX1010, FIGS. 6-7.

7. 16(c)

A second TMV 38 *vertically in a second through via in said first polymer layer* is shown below:

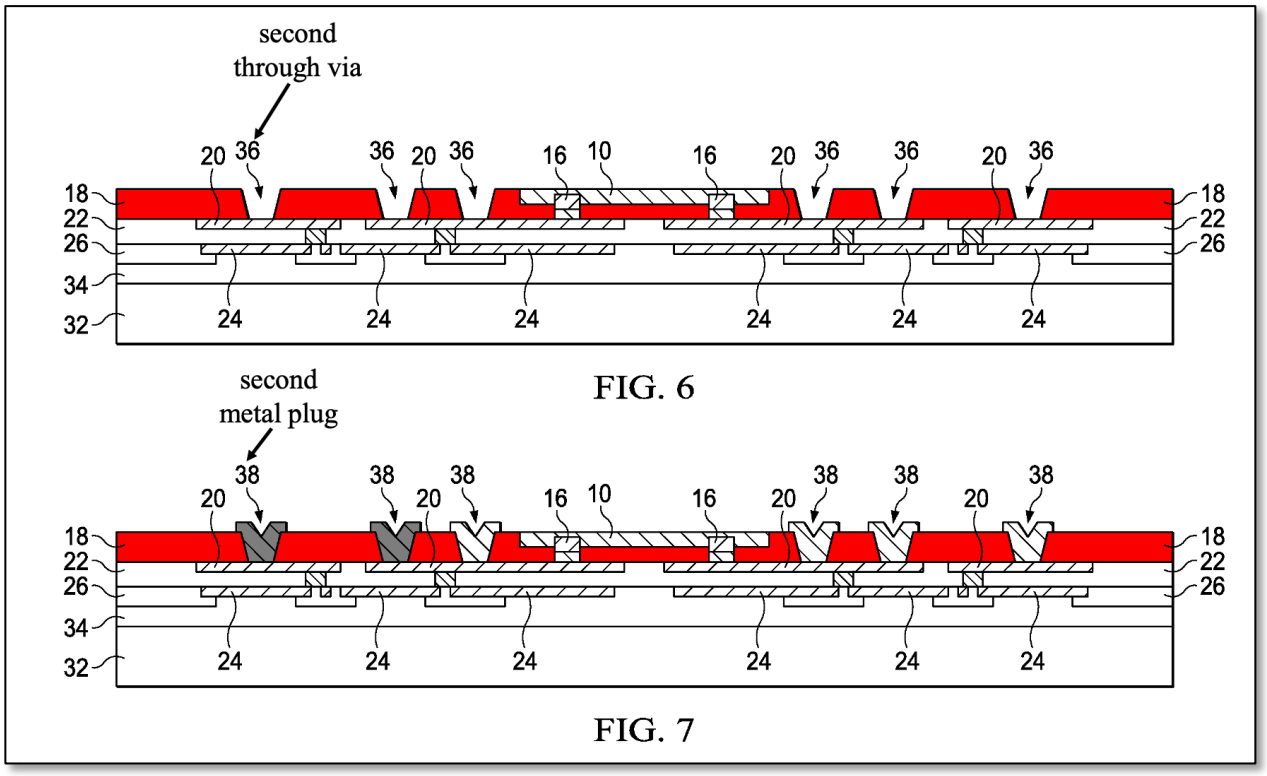


FIG. 6

FIG. 7

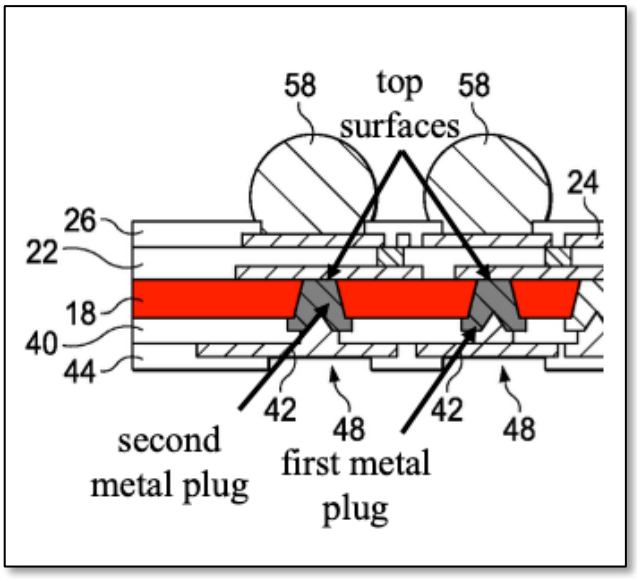
EX1010, FIGS. 6-7; *EX1003*, ¶463.

8. 16(c)(i)

Section IX.A.6. Yu teaches plugs comprise a copper seed layer. *EX1010*, 3:60-64.

9. 16(c)(ii)

The *first* and *second metal plug[s]* comprise *top surface[s]* that *are in the same horizontal plane*:



EX1010, FIG. 16; *EX1003*, ¶465.

10. 16(d)

Yu teaches a "front side interlayer dielectric (ILD) and redistribution layer (RDL) structure" that are collectively *a first interconnection scheme over said first surface* because the structure "electrically couple[s]" components in Yu's *package*. *EX1010*, 3:4-15. The ILD/RDL structure includes a "first front side metallization layer 20," a "first ILD layer 22," "a second metallization layer 24 and a second ILD layer 26." *EX1010*, 3:16-32, FIGS. 4, 7 (describing and showing the formation of layer 20 as in FIG. 16).

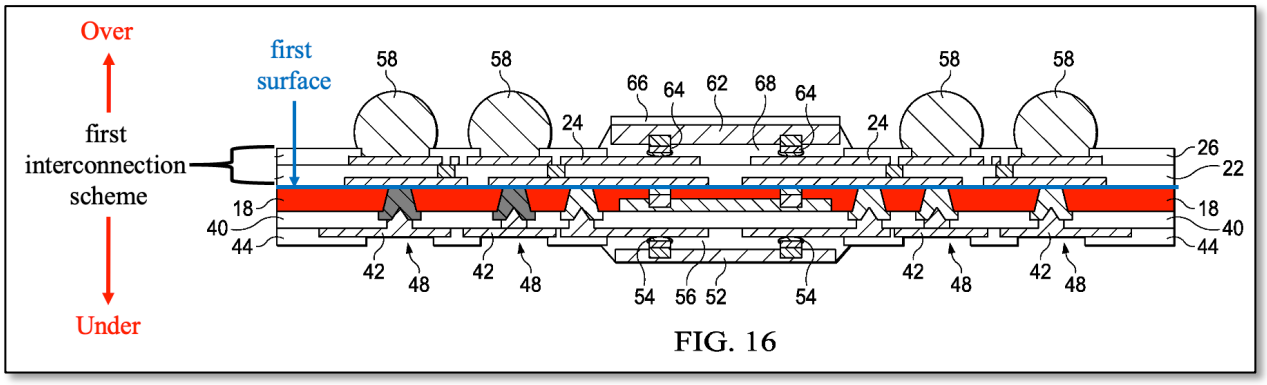


FIG. 16

EX1010, FIG. 16; *EX1003*, ¶466; Section V.A.11, footnote 5.

11. 16(d)(i)

Metallization layer 20 comprises "copper," and a portion of layer 20 is, therefore, *a first metal interconnect*. *EX1010*, 3:10-19. Metallization layer 24 is formed "using the same" process as layer 20 (i.e., with copper); thus, a portion of layer 24 is a *second metal interconnect*. *EX1010*, 3:328-32. Both layers 20, 24 are *over said first surface* as shown below. ILD layers 22, 26 comprise "polyimide" and are, collectively, *a second polymer layer over* metallization layers 20, 24:

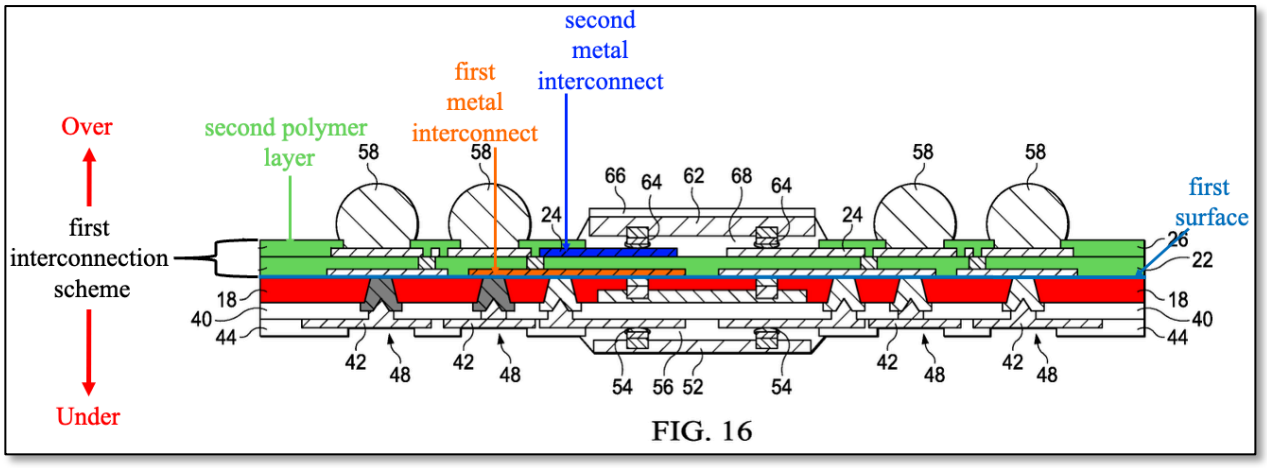


FIG. 16

EX1010, FIG. 16, 3:20-43; *EX1003*, ¶¶467-470.

12. 16(d)(ii)

Yu's *first metal interconnect is connected to said first metal plug* as "TMV openings 36 are formed through the molding compound 18 to the first front side metallization layer 20," followed by formation of TMVs 38 via electroplating. *EX1010*, 3:56-4:6.

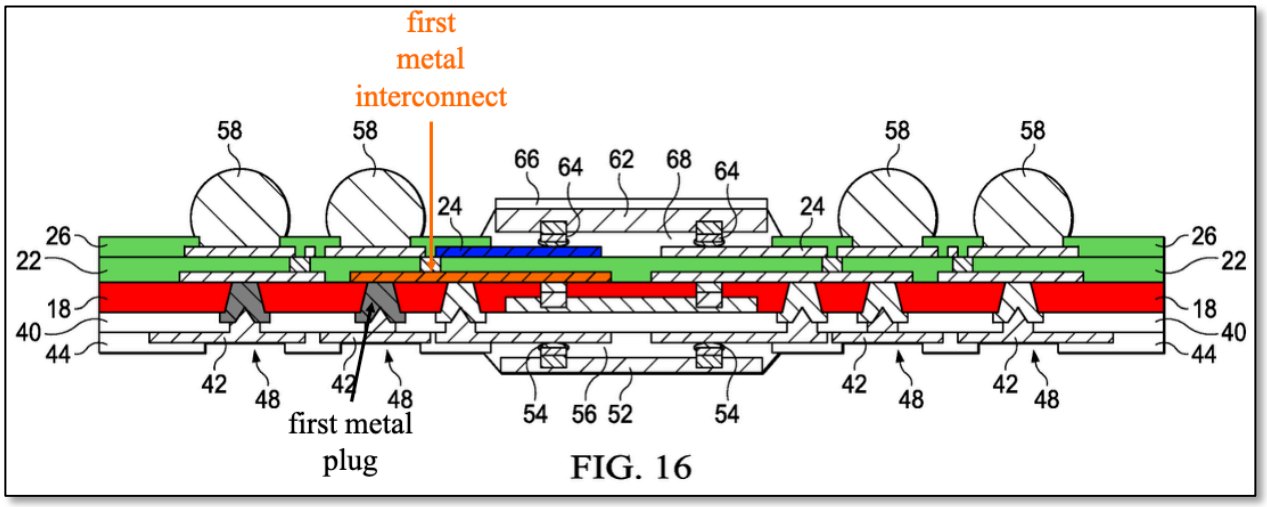


FIG. 16

EX1010, FIG. 16; *EX1003*, ¶471.

13. 16(d)(iii)

Metallization layer 20 includes a "seed layer, such as **copper**…deposited on the molding compound 18," and a "[c]onductive material…such as **copper**…is deposited on the seed layer." *EX1010*, 3:5-19. Thus, metallization layer 20's copper "seed layer" is *a third copper layer*, and the copper "conductive material" deposited on the seed layer is *a fourth copper layer on* the copper seed layer. *EX1003*, ¶472.

a) Lin-191's Teachings

Section V.A.14. Lin-191's adhesion layer 31 is a *first metal layer* with two copper layers formed thereon.

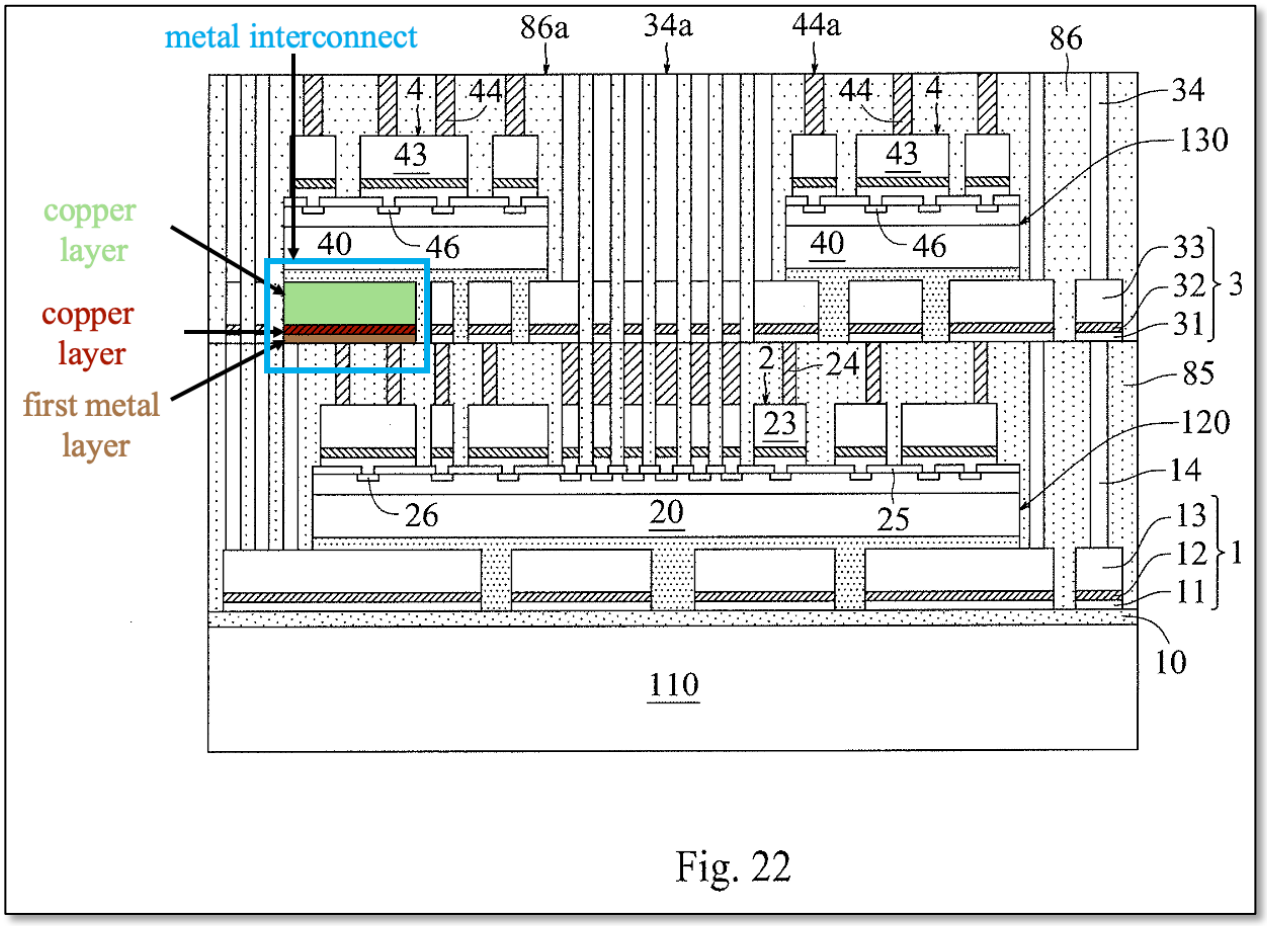


Fig. 22

EX1005, FIG. 22, [0127]; *EX1003*, ¶473.

b) MTC

Section V.A.14. The MTCs and REOS for modifying Sundaram per Lin-191 apply for the Yu-Lin-191 combination. Like Yu's *first metal interconnect*, Lin-191's metal interconnect comprises a copper seed layer 32 and a copper metal layer 33. *EX1005*, [0127-0128], [0133]. Thus, a POSITA would have been motivated and

found obvious to apply Lin-191's three-metal layer interconnect teachings to Yu's *first metal interconnect*, yielding the claimed *layer[s]* to obtain the benefits of Lin-191's adhesion layer 31. *EX1003*, ¶474. The combination is the application of a known technique (Lin-191's three-layer metal interconnect) to a known device (Yu's metal interconnect) ready for improvement to yield predictable results. *EX1003*, ¶475. There would have been a REOS because Lin-191 teaches forming adhesion layer 31 using manufacturing techniques also taught by Yu making the modification would have been simple and straightforward. *Compare EX1005*, [0127] *with EX1010,* 3:5-16; *EX1003*, ¶475.

14. 16(e)

Yu teaches "conductive connectors 58, such as ball grid array (BGA) balls" are formed "on the front side of the package in the openings 28" and "formed on [] bond pads." *EX1010*, 4:45-49. A connector 58 is *a first metal bump over said first interconnection scheme*.

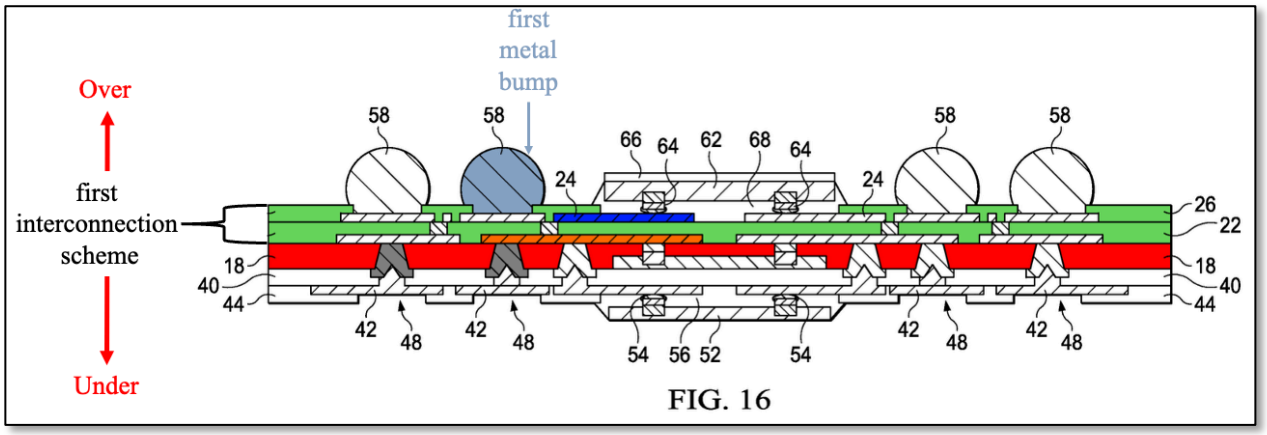
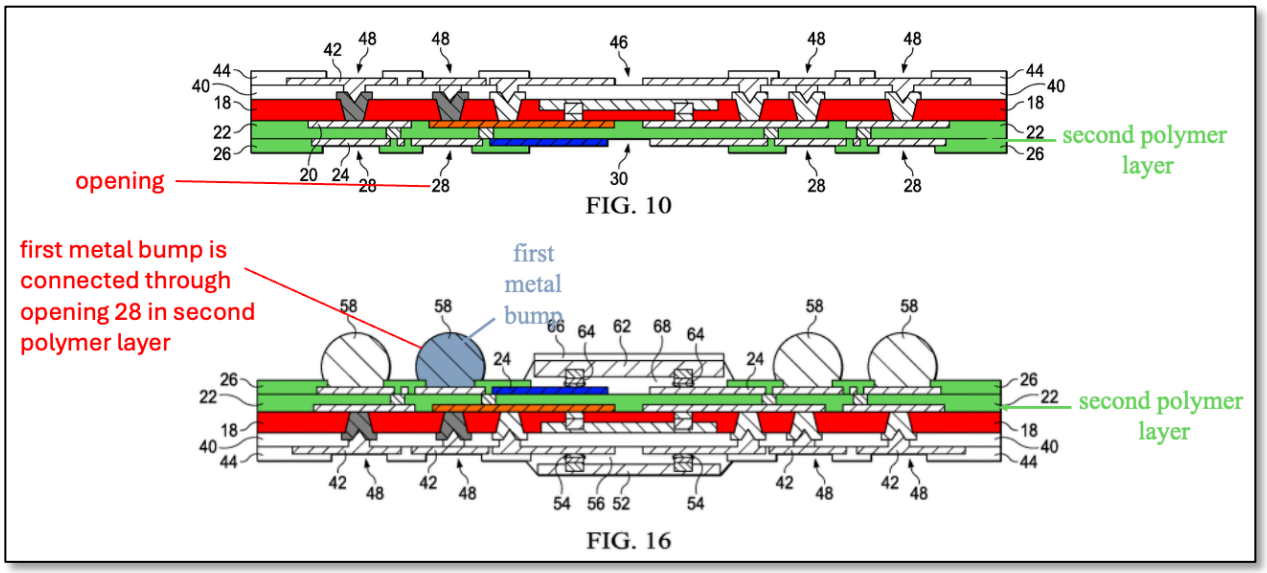


FIG. 16

EX1010, FIG. 16; *EX1003*, ¶476.

15. 16(e)(i)

Connector 58 is *connected to said first interconnection scheme* "through opening 28" in "second ILD layer 26" (*a first opening in said second polymer layer*). *EX1010*, 3:35-39, 4:45-49; *EX1003*, ¶477-478.



EX1010, FIGS. 10, 16.

16. 16(e)(ii)

Connectors 58 are "lead-free solder." *EX1010*, 4:47-50. A POSITA would have understood lead-free solder to include *tin*. *EX1003*, ¶479. Thus, Yu teaches *a tin-containing layer. Id*.

a) Lin-191's Teachings and MTC

Additionally, or alternatively, Lin-191 teaches Claim 16(e)(ii). Sections VI.A.16, V.A.16.a-b. A POSITA would have been motivated, found obvious, and had a REOS for modifying Yu-Lin-191 as discussed for Sundaram-Lin-191. *Id.* The

Yu-Lin-191 combination is application of known technique (Lin-191's solder bump structure) to a known device (Yu's connector/BGA ball 58) ready for improvement to yield predictable results. *EX1003*, ¶480.

17. 16(f)

Yu teaches a *second metal bump* (second connector/BGA ball 58) *over said first interconnection scheme*:

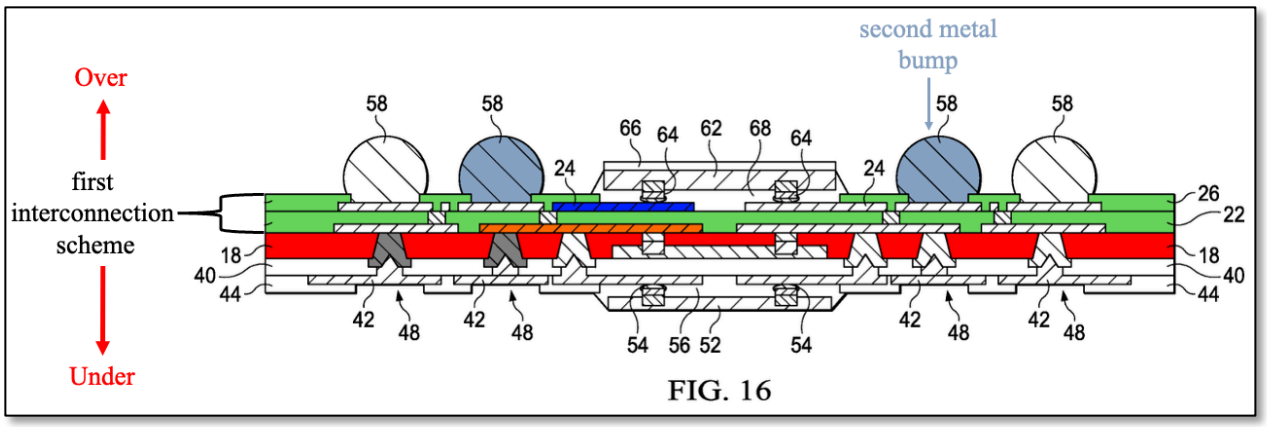
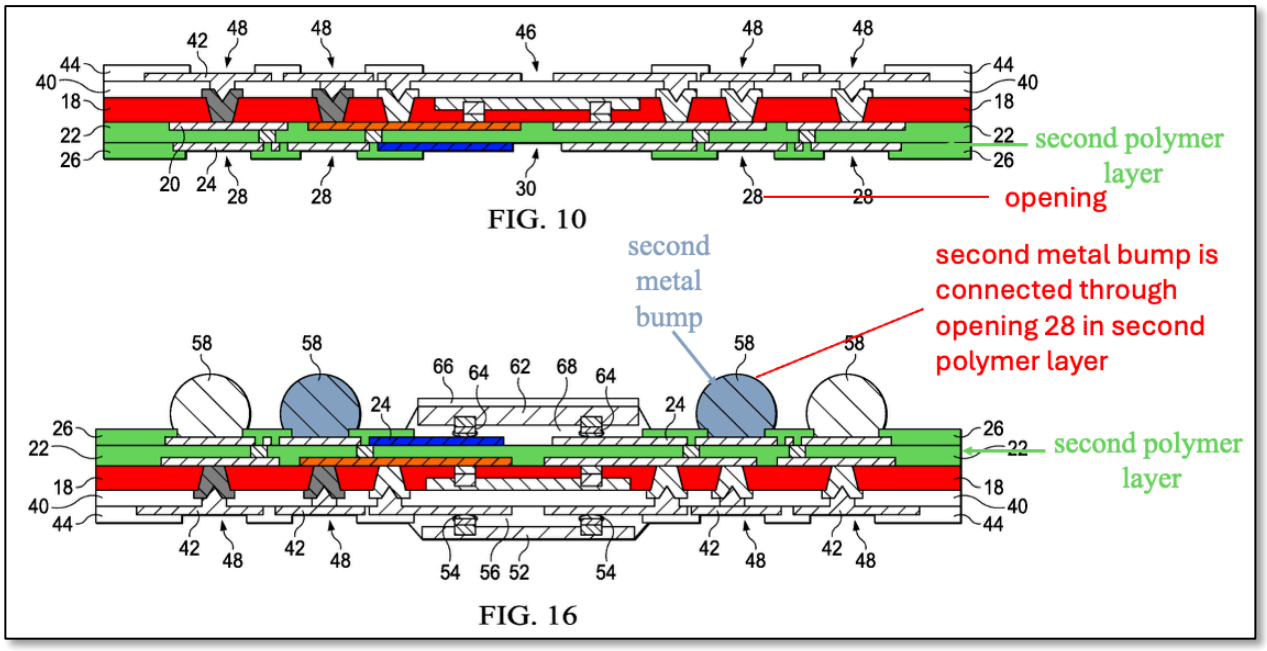


FIG. 16

EX1010, FIG. 16; *EX1003*, ¶481.

18. 16(f)(i)

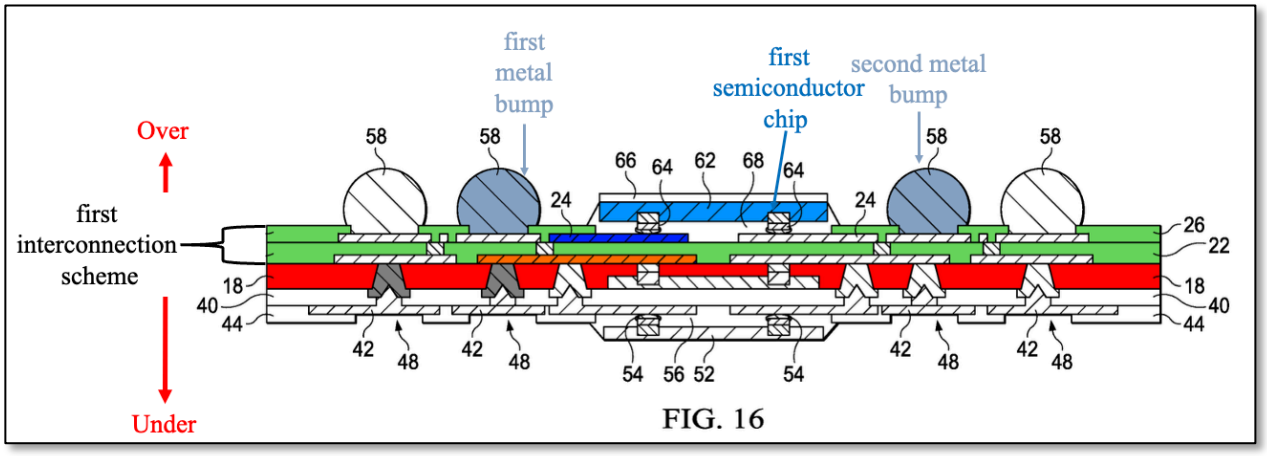
Section IX.A.15, reciting corresponding limitations. *EX1003*, ¶482.



EX1010, FIGS. 10, 16.

19. 16(g)

Yu's package includes "die 62," i.e., *a first semiconductor chip over said first interconnection scheme and between said first and second metal bumps. EX1010*, 4:53-58.



EX1010, FIG. 16; *EX1003*, ¶483.

20. 16(h)

Die 62 is "attached…to conductive features in the second front side metallization layer 24" by "connectors 64," which are "C4 bumps." *EX1010*, 4:53-58. C4 bumps are solder bumps, i.e., *metal bumps*. *EX1003*, ¶484. A connector 64 is a *third metal bump between said first semiconductor chip and first interconnection scheme*:

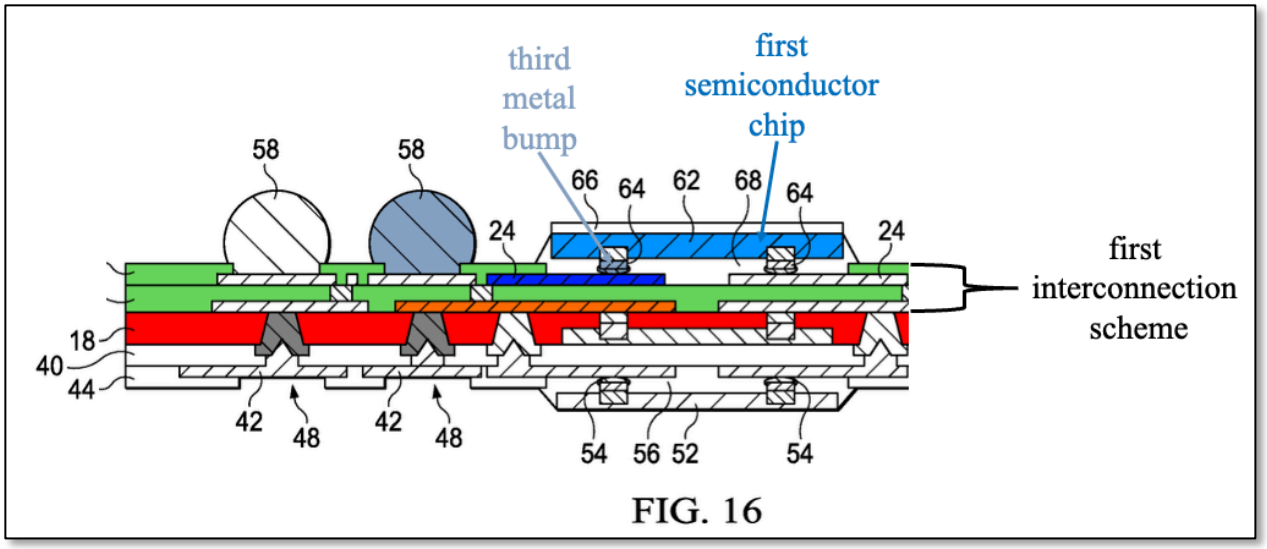
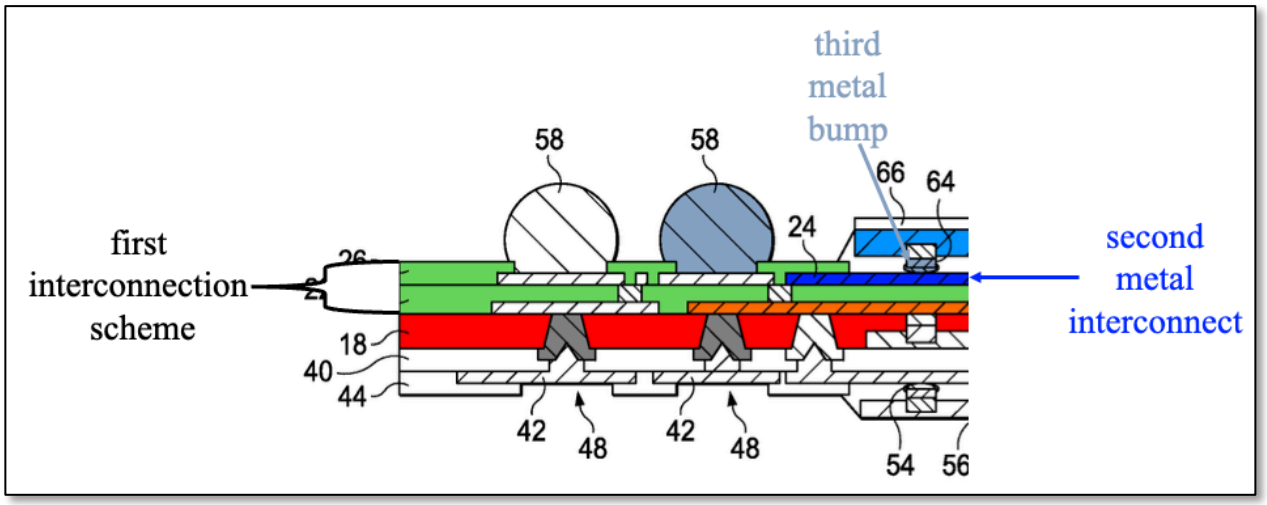


FIG. 16

EX1010, FIG. 16 (excerpt); *EX1003*, ¶¶484-485.

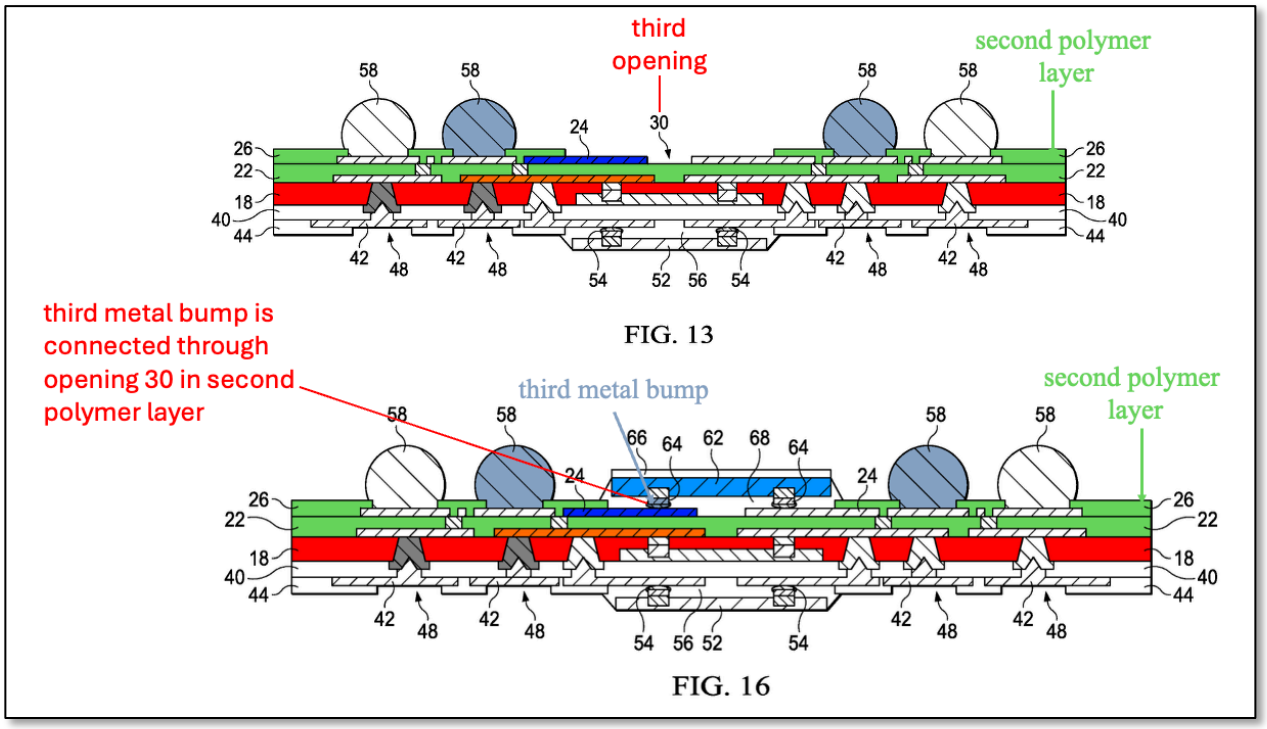
21. 16(h)(i)

Connector 64 is connected to "conductive features in the second front metallization layer 24," i.e., to *said second metal interconnect*. *EX1010*, 4:57-60.



EX1010, FIG. 16 (excerpt); *EX1003*, ¶486.

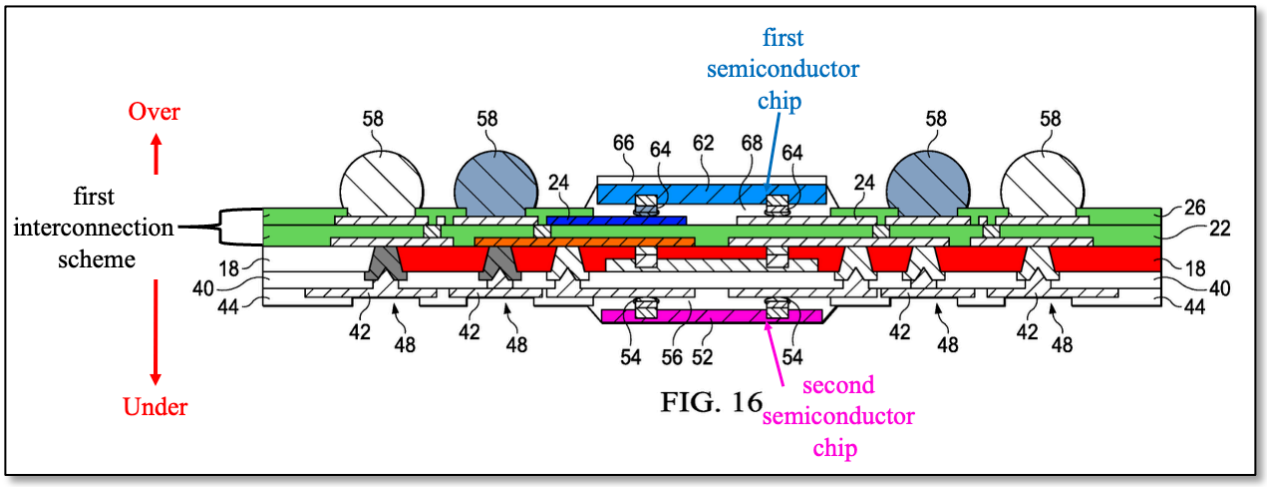
Die 62 is connected "through the opening 30" in ILD layer 22 (a *third opening in said second polymer layer*). *EX1010*, 3:35-41, 4:53-56. Because the *third metal bump* connects die 62 to the *second metal interconnect* and die 62 is connected through the *third opening*, the *third metal bump* is *connected through a third opening in said second polymer layer*:



EX1010, FIGS. 13, 16, 3:35-41, 4:53-56; *EX1003*, ¶487.

22. 16(i)

Yu's package additionally includes "die 52," which is *a second semiconductor chip under first interconnection scheme and said first semiconductor chip*. *EX1010*, 4:30-36.



EX1010, FIG. 16; *EX1003*, ¶488.

23. 16(i)(i)

Yu's *first interconnection scheme is between said first and second semiconductor chips*:

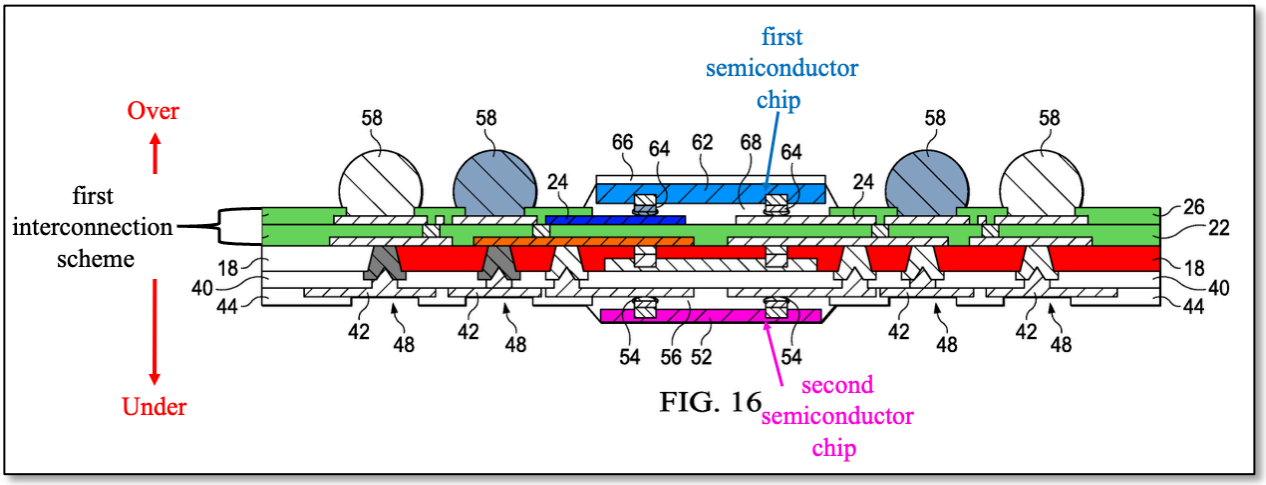


FIG. 16

EX1010, FIG. 16; *EX1003*, ¶489.

24. 16(i)(ii)

Section V.E., reciting corresponding limitations. The same MTC and REOS for Sundaram-Lin-191 apply to Yu-Lin-191, i.e., the modification would advantageously increase the functionality of Yu's package. *EX1003,* ¶490.

B. Claim 17

FIG. 16's package is part of FIG. 52's PoP structure (*chip package*). Section IX.A.1. The PoP structure includes another package 204 over FIG. 16's package 202, which includes a logic die 174, i.e., *a third semiconductor chip over said first interconnection scheme*.

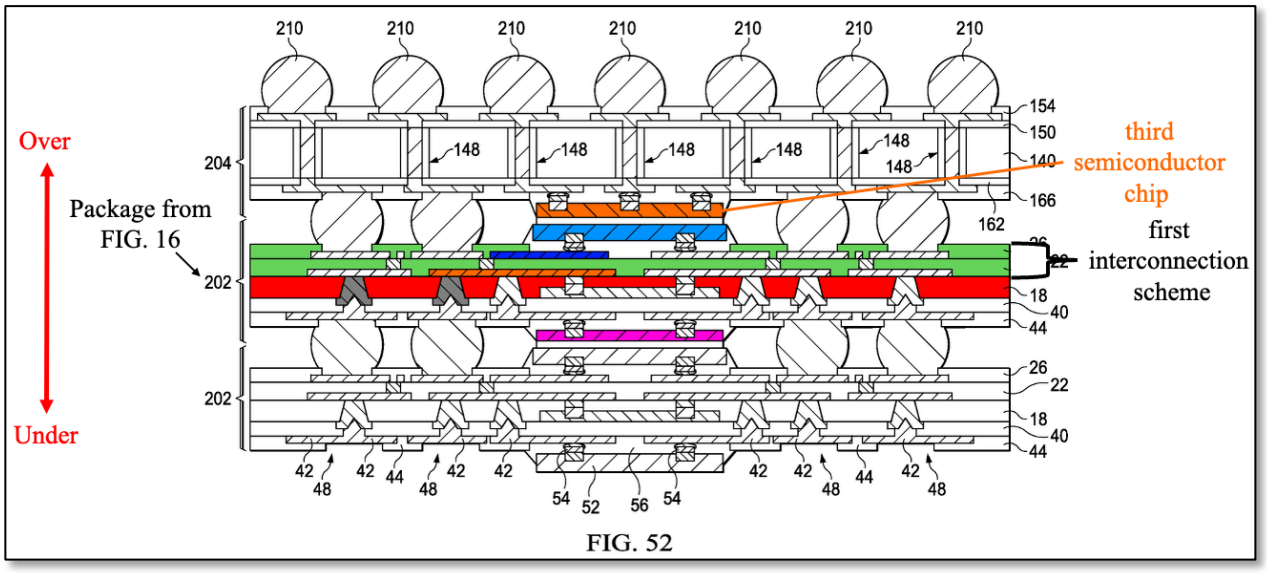


FIG. 52

EX1010, FIG. 52, 7:44-45, 8:35-39, 8:11-12; *EX1003*, ¶491.

C. Claim 19

Yu teaches a third TMV 38 *vertically in a third through via in said polymer layer*[8] :

[8] Petitioners interpret Claim 19's *polymer layer* as referring to Claim 16(a)'s *first polymer layer*.

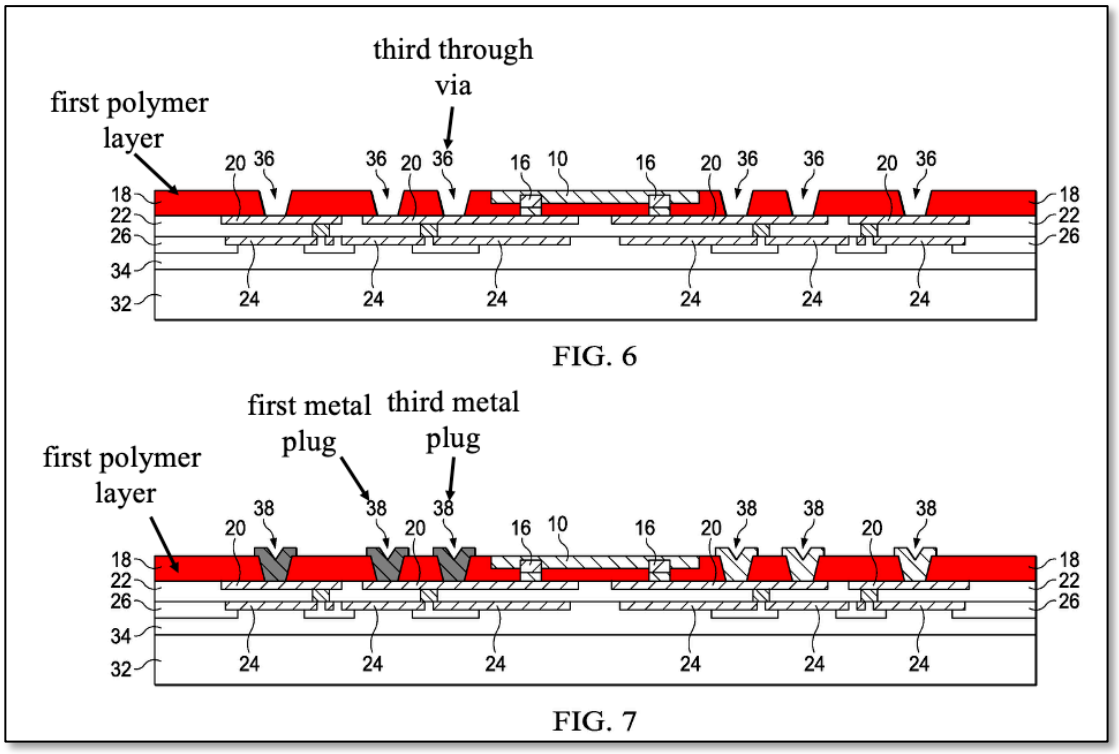


FIG. 6

FIG. 7

EX1010, FIGS. 6-7; *EX1003*, ¶492.

a) Lin-191's Teachings and MTC

Lin-191's layer 85 includes metal bumps 14 having a "pitch…between 100 and 250 micrometers," overlapping with and teaching or rendering obvious the claimed range. *EX1005*, [0075]; Section V.A.4 (supporting caselaw); *EX1003*, ¶494 (citing *EX1001*, 6:8-15 and opining no criticality of the claimed pitch).

A POSITA would have found obvious and been motivated to apply Lin-191's pitch to Yu's *first* and *third metal plug[s]* as a pitch *between 200 and 1000 micrometers* was known to enable high bandwidth speeds such as "at least about 10 GB/s" in a "digital camera for cell phones," which Yu expressly contemplates *EX1004*, 6:42-45; *EX1010*, 1:53-55; *EX1003*, ¶¶495-496. The combination is the

application of a known technique (Lin-191's pitch) to a known device (TMVs 38) ready for improvement to yield predictable results. *EX1003*, ¶497. A POSITA would have a REOS because the modification would have been simple and straightforward as methods of controlling pitch were well-known. *Id*.

D. Claim 22

Section VII.C. The MTCs and REOS for modifying Haba per Lin-191 apply for the Yu-Lin-191 combination. Additionally, Yu teaches "chip resistors" and "chip capacitors," i.e., *passive component[s]*. *EX1010*, 1:41-45. The modification is the application of a known technique (*passive component*) to a known device (Yu's *chip package*) to yield predictable results and would have had a REOS due to the ubiquity of passives in chip packages, making the modification simple and straightforward. *EX1003*, ¶¶498-500.

E. Claim 23

Another portion of metallization layer 20 is *a third metal interconnect*, which is *over* a sidewall of die 52 because it is positioned on the opposite side of molding compound 18 (*over*) from die 52's *sidewall*. Additionally, metallization layer 20 comprises a portion extending laterally beyond the *sidewall*; thus, it is *across* the *sidewall*.

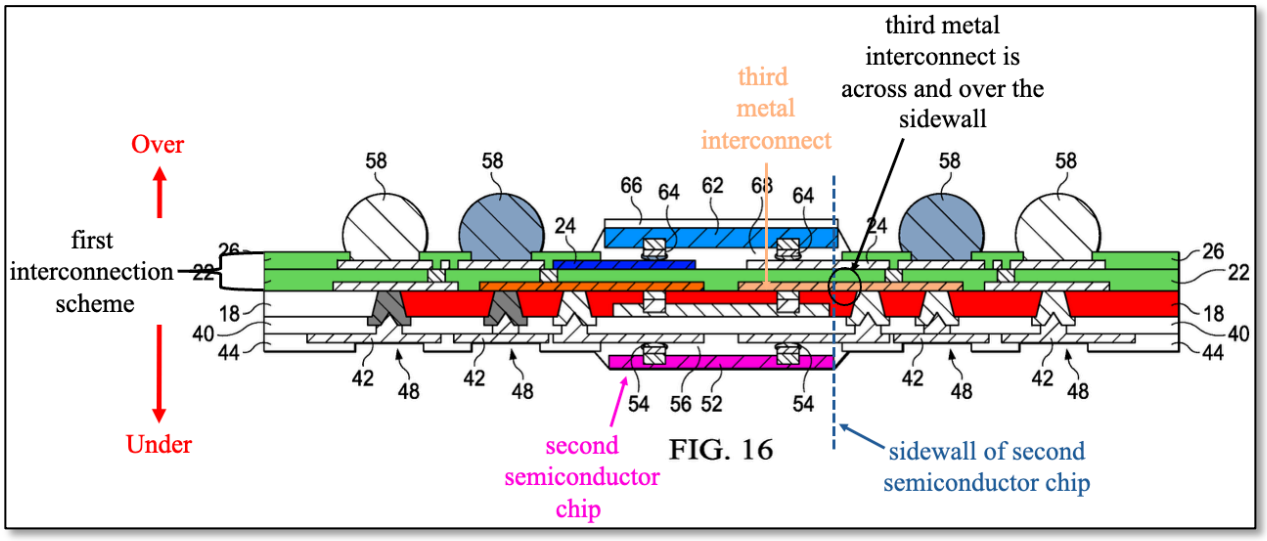
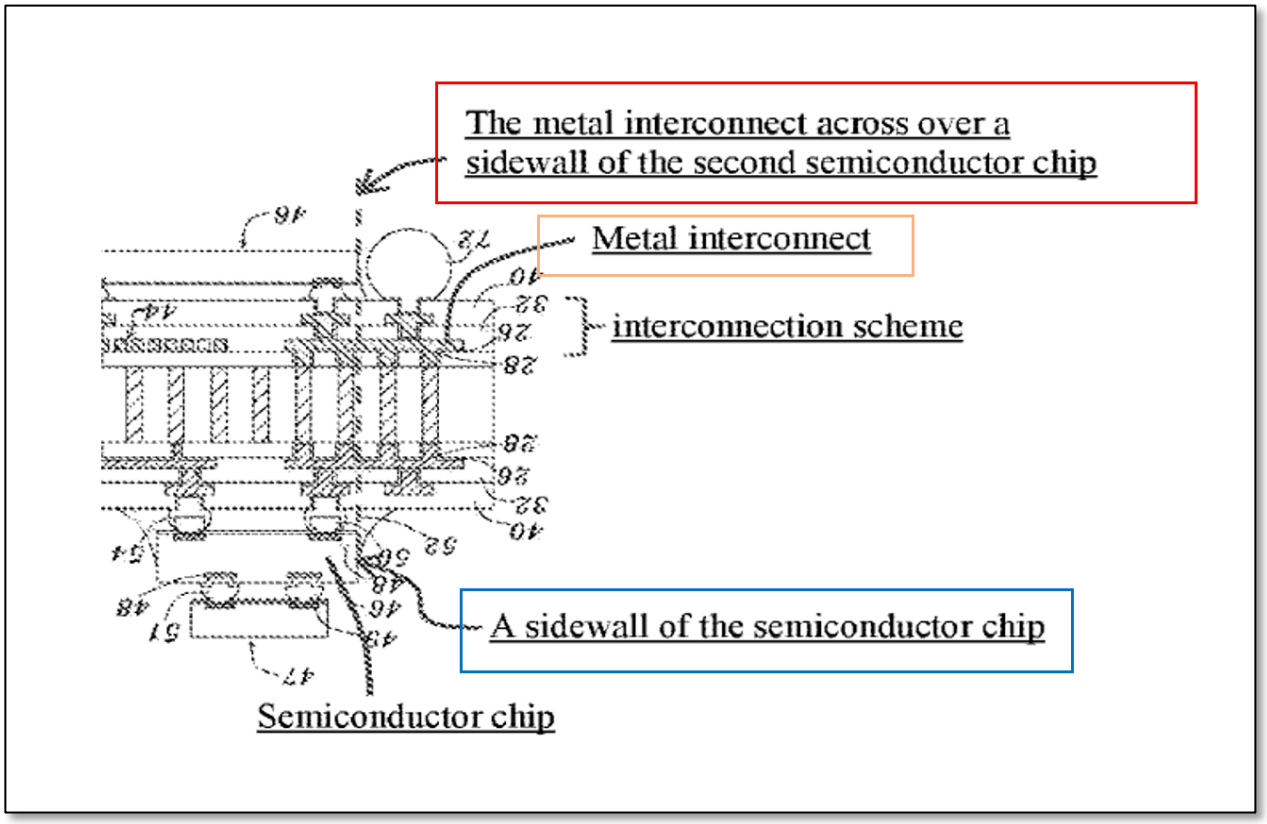


FIG. 16

EX1010, FIG. 16; *EX1003*, ¶501.



EX1002, 537[9]. Section V.C; *EX1003*, ¶502.

[9] Annotated figure that PO argues supports Claim 23's language.

F. Claim 24

Yu's PoP structure (*chip package*) includes another package 202 under FIG. 16's package 202, which includes another "die 62, such as a **memory die**," i.e., *a third semiconductor chip under said first interconnection scheme* that is a *memory chip*. *EX1010*, 4:53-55, 8:35-39, 8:11-12.

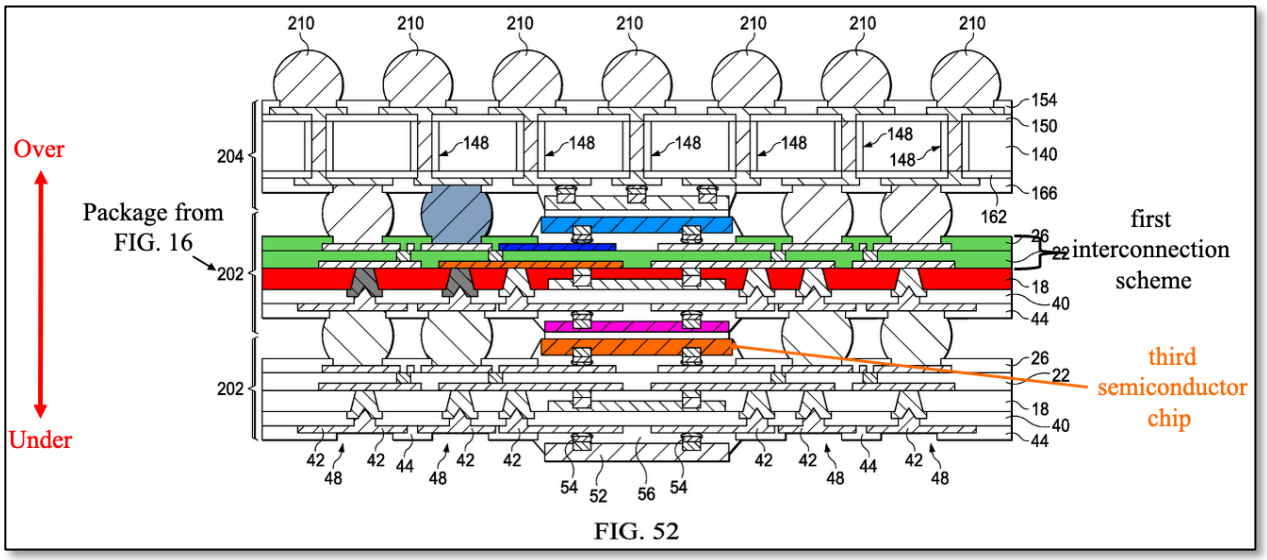


FIG. 52

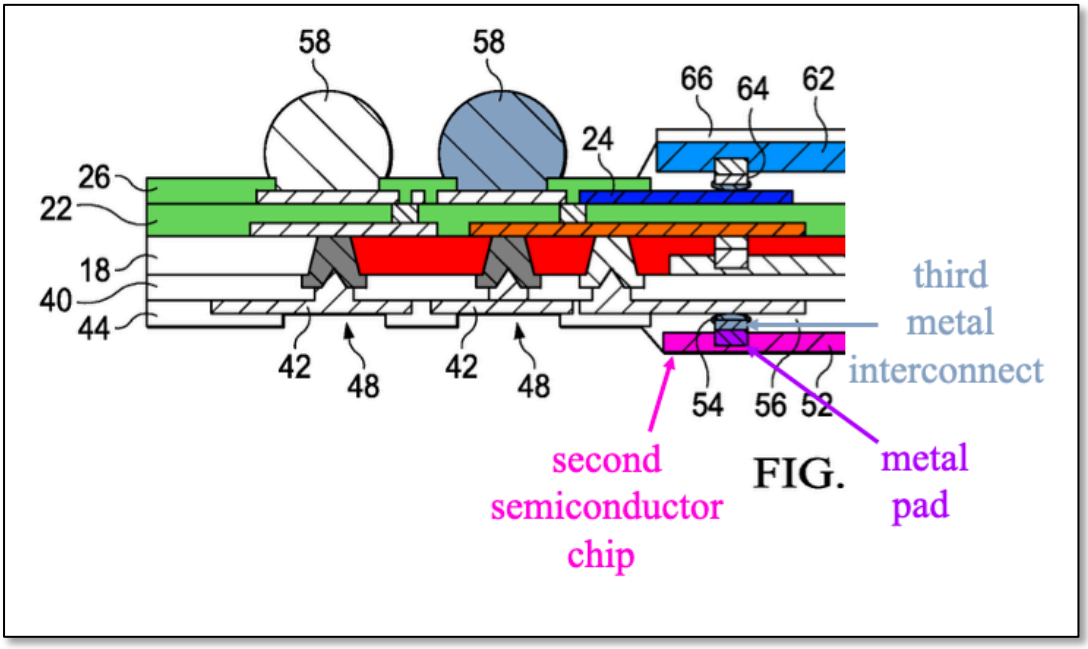
EX1010, FIG. 52; *EX1003*, ¶503.

G. Claim 25

1. 25(a)

Die 52 is attached to "metallization layer 42…by conductive connectors 54." *EX1010*, 4:30-34. A connector 54 is *a third metal interconnect* because it connects die 52 "to conductive features" in layer 42. *Id.* A POSITA would have understood die 52 includes die pads (unlabeled) such that an electrical connection is made between die 52 and other devices (e.g., die 62), thus teaching the *metal pad of said*

second semiconductor chip. *EX1003*, ¶¶504-507; *EX1129*, 1:9-26. The connector 54 is *on* the die pad of die 52:



EX1010, FIG. 16 (excerpt); *EX1003*, ¶¶504-507.

a) Lin-191's "Metal Pad" Teachings and MTC

Additionally, or alternatively, Lin-191 teaches *metal pads*. Section V.A.18.a. Lin-191 teaches an implementation detail of Yu's die pads such that there would have been a motivation and REOS for modifying Yu. *EX1003,* ¶¶508-509. The combination is the application of known technique (metal pads) to a known device (die 52) ready for improvement to yield predictable results. *Id*.

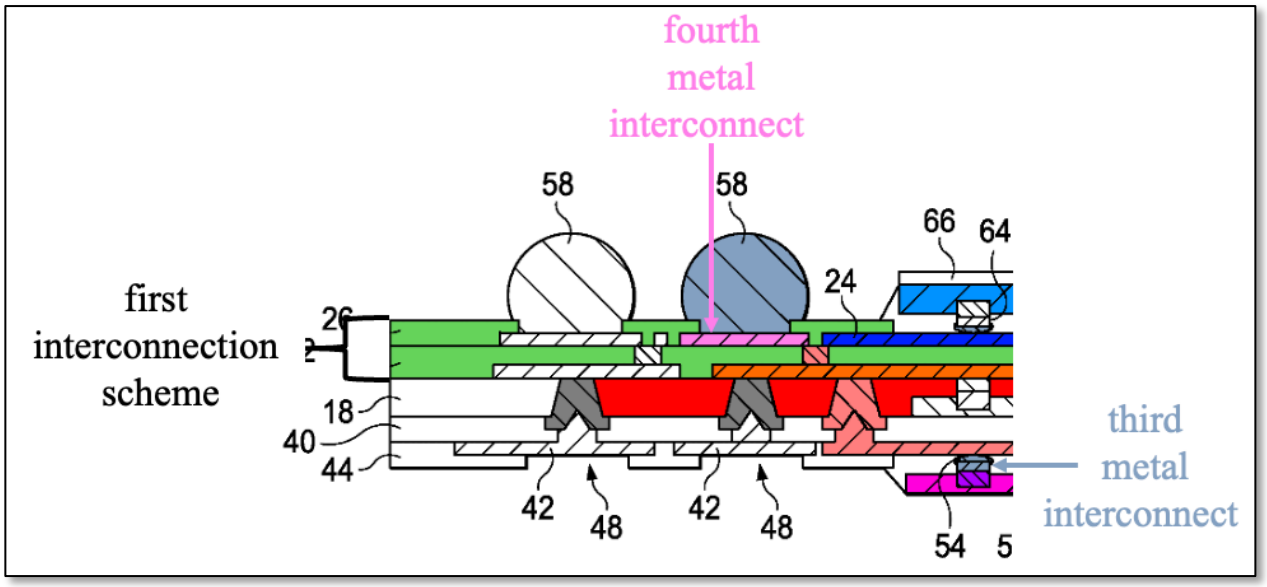
2. 25(b)

Lin-191 teaches or renders obvious interconnects/bumps with layers/thickness as recited. Section V.A.19. A POSITA would have found obvious

and been motivated to modify Yu's connector to improve metallurgical bonding and increase resistance to fatigue and stress-induced failure. *EX1003*, ¶510. Layered bumps were routinely manufactured using techniques contemplated by Yu, leading to a REOS. *Compare EX1005*, [0400] *with EX1010*, 3:11-14; *EX1003*, ¶510.

3. 25(c)

Yu's *third metal interconnect is connected to* another portion of metallization layer 24 (*fourth metal interconnect*) through a portion of metallization layer 42, a TMV 38, the *first metal interconnect,* and a *via*. *EX1010*, 4:7-11, 3:32-35.



EX1010, FIG. 16 (excerpt); *EX1003*, ¶511.

H. Claim 26

Yu's *first semiconductor chip* has a *height* that *is between a backside surface and a top surface* of ILD 22, 26, which *is smaller than a thickness of said first metal*

bump, similar to PO's annotated figure relied on during original prosecution to support the claim language.

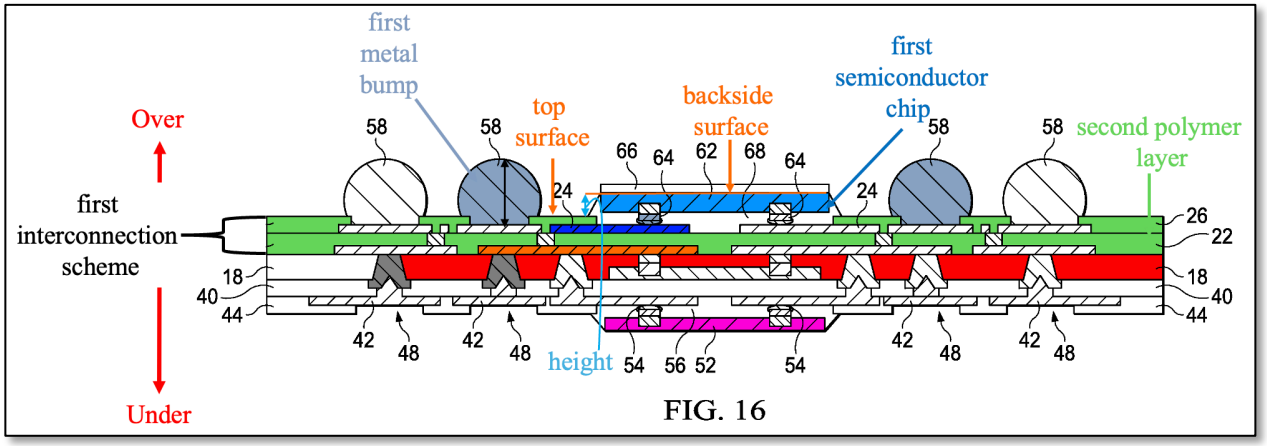
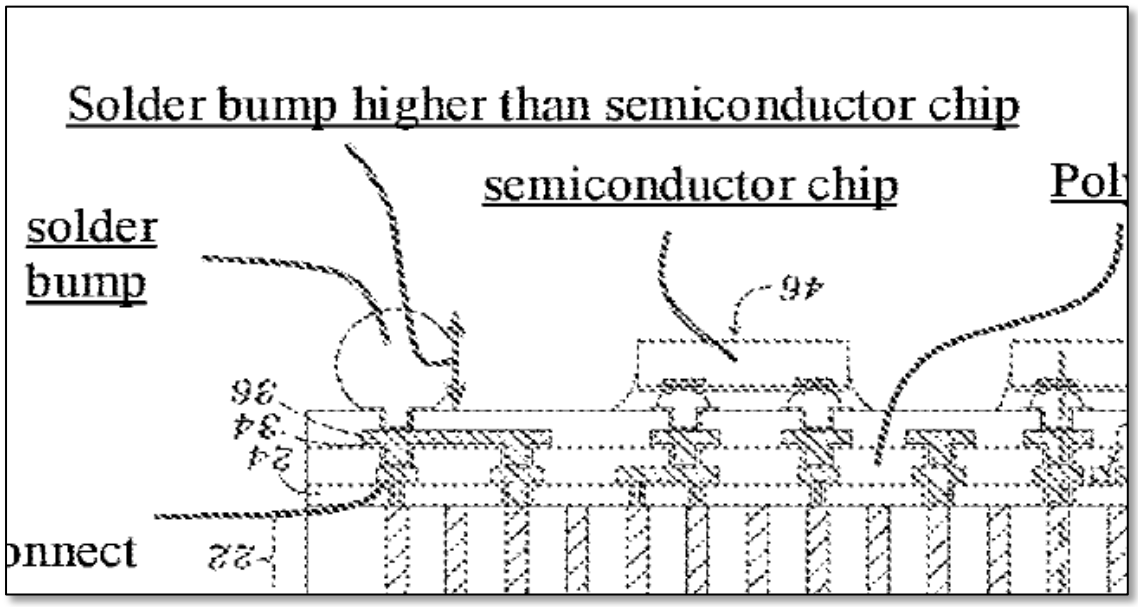


FIG. 16

EX1010, FIG. 16 (excerpt); Section V.C (supporting caselaw); *EX1003*, ¶512.



EX1002, 400; *EX1003*, ¶513.

I. Claim 27

Die 52 (*second semiconductor chip*) is *coupled to* die 62 (*first semiconductor chip*) *through said first interconnection scheme*. Specifically, die 52 is connected to

die 62 through connector 54, layer 42, a TMV, the first and second metal interconnects, then to another connector 64 connected to die 62. *EX1010*, 4:30-38, 4:53-50, 3:32-35.

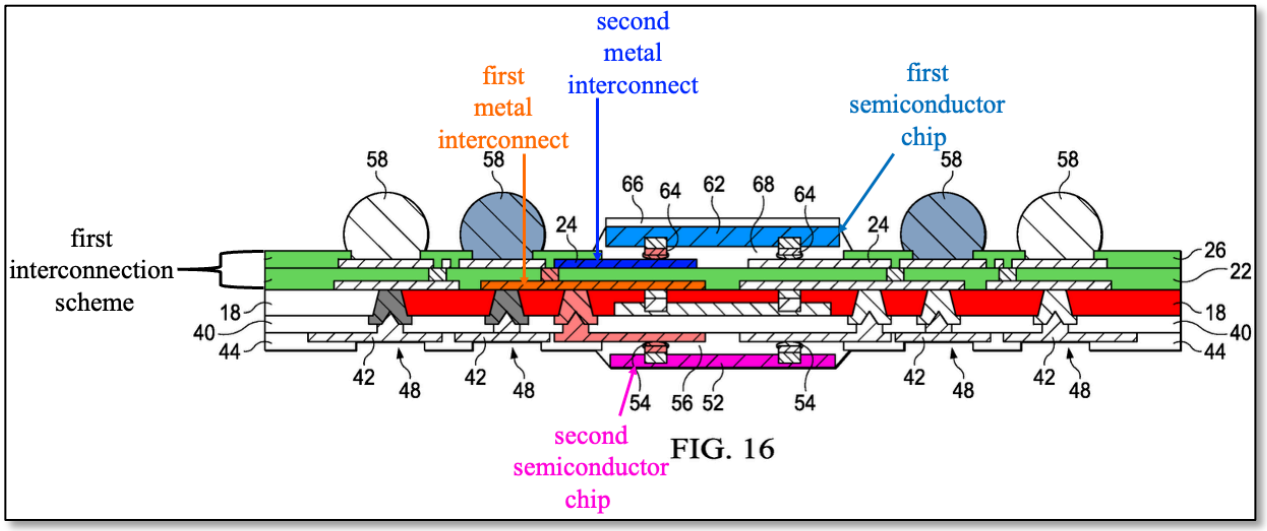


FIG. 16

EX1010, FIG. 16 (excerpt); *EX1003*, ¶¶514-517.

J. Claim 28

TMVs 38 (*first metal plug*) extend from either surface of the molding compound 18. At Claim 16(a)(ii), molding compound 18 is modified per Lin-191 to be *between about 100 and 300 micrometers*. Section IX.A.4. Because the *first metal plug has a thickness* approximately equal to that of molding compound 18, Yu-Lin-191 teaches or renders obvious Claim 28. *EX1003*, ¶518; Sections V.A.4, V.O., IX.A.4.

X. GROUND 3B: CLAIMS 18 AND 21 ARE OBVIOUS OVER YU, LIN-191, AND CAMACHO

A. Claim 18

1. 18(a)

Yu's alone or Yu-Lin-191 teaches *a first metal pad*. Section IX.G.1. Die 52's *first metal pad* is *on a top surface*:

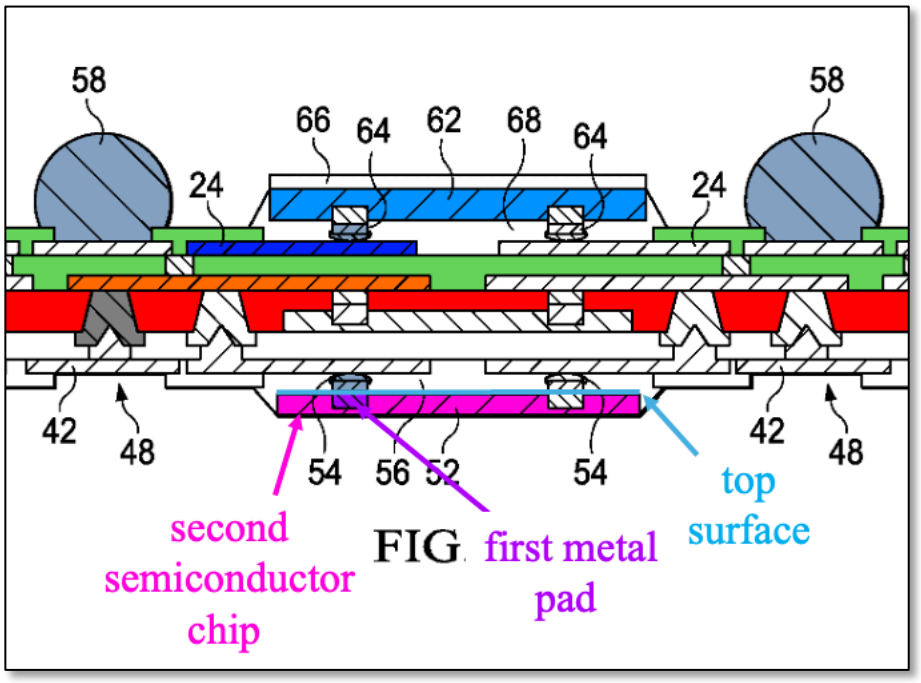
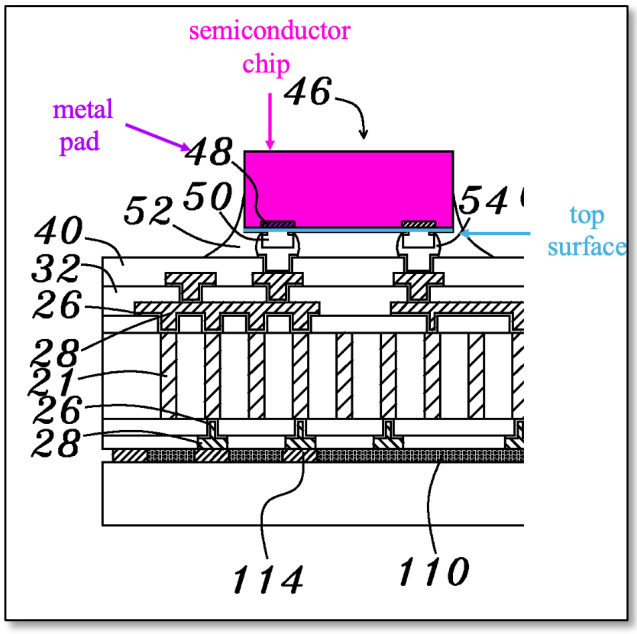


FIG.

EX1010, FIG. 16 (excerpt); *EX1003*, ¶519.

Yu's teachings are similar to the '768 Patent's depiction of a metal pad on a top surface:



EX1001, FIG. 17a (excerpt); *EX1003*, ¶520.

a) Camacho's "Metal Pad" Teachings

Camacho teaches a "conductive TSV through a" semiconductor die 122. *EX1006*, [0039], [0008], [0010]. An "electrically conductive layer 130 is formed **over** the top" of die 122, and "electrically conductive layer 132 is formed **over** the bottom surface of semiconductor die 122.". *EX1006*, [0041]. Layers 130, 132 are aluminum. *Id*. Thus, a layer section 132 is *a first metal pad on a top surface* of a chip, and a layer section 130 is *a second metal pad on a bottom surface of* the chip.

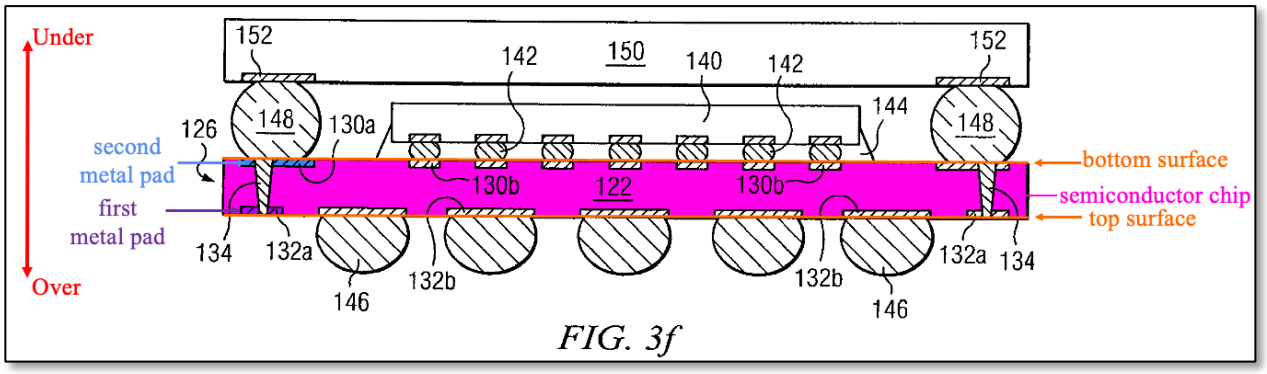


FIG. 3f

EX1006, FIG. 3f. Section X.A.3 (MTC and REOS); *EX1003*, ¶521.

2. 18(b)

a) Camacho's Teachings

Camacho teaches *metal* "conductive TSV[s] 134" that "electrically connect[]" layers, 130, 132. *EX1006*, [0043], [0047]. Thus, Camacho teaches layer 132a *is connected to* layer 130a *through a through-silicon-via metal layer* (TSV 134).

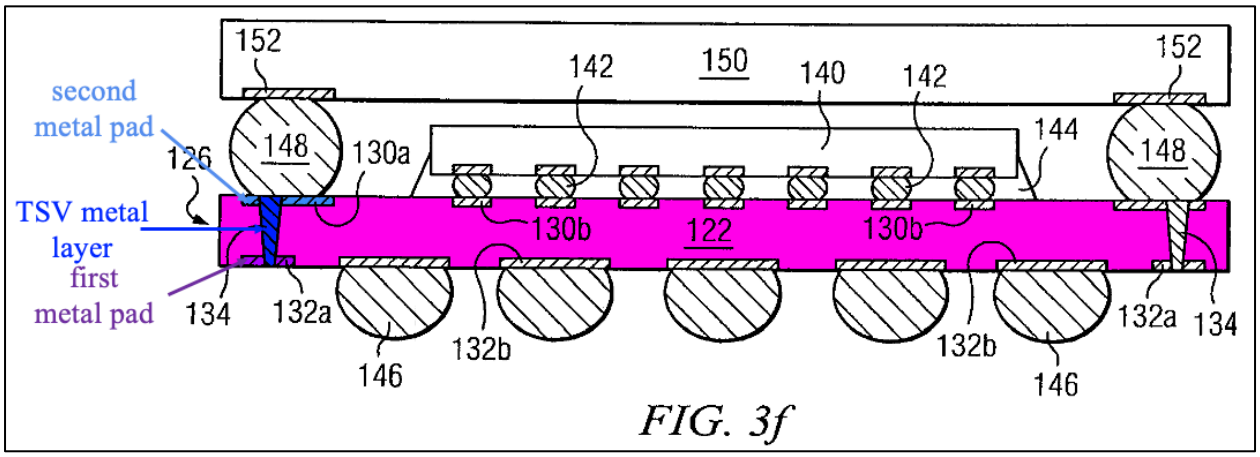


FIG. 3f

EX1006, FIG. 3f; *EX1003*, ¶¶522-523.

3. Claim 18 MTC

A POSITA would have found obvious and been motivated to configure Yu's die 52 with a TSV metal layer connecting metal pads on both surfaces of die to provide Yu with the TSV advantages previously discussed. Sections VIII.B.3, VIII.E.5. The modification is the application of a known technique (chips with TSVs connecting metal pads) to a known device (Yu's die) to yield the predictable result of die 52 having a TSV connecting pads on either side. *EX1003*, ¶¶524-526. A POSITA would have had a REOS because Camacho's teachings represent well-known methods for chip stacking using TSVs, which was commonplace by the time of the '768 Patent. *EX1003*, ¶526.

B. Claim 21

1. 21(a)

a) Camacho's Teachings

Camacho teaches a die 150 *under* die 122, i.e., *a third semiconductor chip under said second semiconductor chip*. *EX1003*, ¶527.

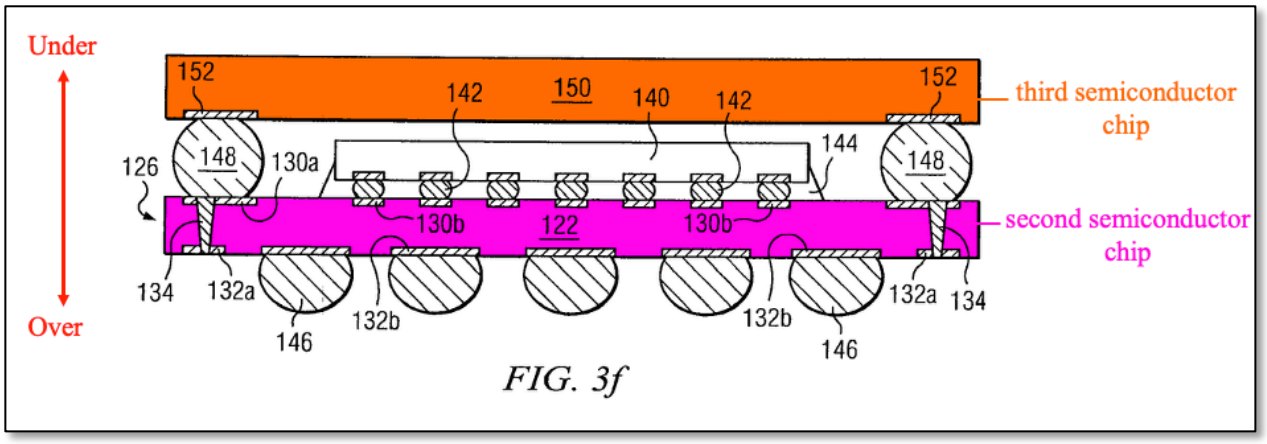


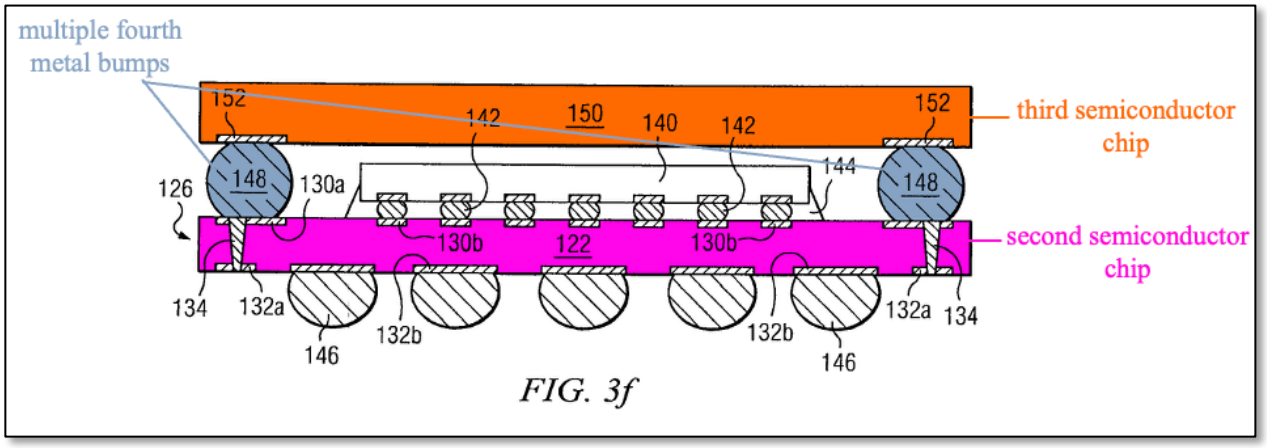
FIG. 3f

EX1006, FIG. 3f.

2. 21(b)

a) Camacho's Teachings

Die 150 connects to die 122 through *multiple fourth metal bumps*, namely "Al" bumps 148 *between* dies 122, 150. *EX1006*, FIG. 3f, [0046], [0048].



EX1006, FIG. 3f; *EX1003*, ¶528.

3. 21(c)

Section X.A.1, reciting corresponding limitations. *EX1003*, ¶529.

4. 21(d)

Section X.A.2, reciting corresponding limitations. *EX1003*, ¶530.

5. Claim 21 MTC

Section X.A.3 (MTCs and REOS for modifying Yu's *second semiconductor chip* to have metal pads connected via TSVs).

Further, modifying Yu with a *third semiconductor chip under* Yu's die 52 and connected thereto by *multiple fourth metal bumps* (Camacho's bumps 148)

positioned on the *first metal pad* would have advantageously maximized package space. *EX1003*, ¶¶532-534. The modification is the application of a known technique (stacking chips) to a known device (Yu's *chip package*) to yield the predictable result of a chip package comprising multiple connected chips, which would have had a REOS because the modification would have been simple and straightforward. *EX1003*, ¶535.

XI. GROUND 3C: CLAIM 20 IS OBVIOUS OVER YU, LIN-191, AND HABA

A. Claim 20

a) Haba's Teachings and MTC

Section V.A.5. The same MTCs and REOS for Sundaram-Haba apply for Yu-Haba. The modification would reduce CTE mismatch between Yu's molding compound 18 and chips, which was a known benefit when encapsulating chips. *EX1003*, ¶536. The combination is the application of a known technique (a polymer with a CTE of 8 ppm/°C) to a known device (Yu's polymer molding compound 18) to yield predictable results. *Id*.

XII. CONCLUSION

For the foregoing reasons, Petitioners respectfully request *inter partes* review of the Challenged Claims.

Respectfully submitted,

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APPLE INC.

XIII. MANDATORY NOTICES UNDER 37 C.F.R. § 42.8(A)(1)

A. Real Parties-In-Interest

Petitioners Taiwan Semiconductor Manufacturing Company Limited and Apple Inc. are the real parties-in-interest. 37 C.F.R. § 42.8(b)(1).

B. Related Matters

The '768 Patent is presently the subject of a patent infringement lawsuit filed against Petitioner, Apple Inc., in the United States District Court for the District of Delaware. *MYW Semitech, LLC v. Apple Inc.*, Case No. 1:25-cv-00504.

C. Lead and Back-Up Counsel

Petitioners provide the following designation and service information for lead and back-up counsel. 37 C.F.R. §§ 42.8(b)(3) and (b)(4).

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D. 37 C.F.R. § 42.8(b)(4) – Service Information

Please address all correspondence to the lead and back-up counsel as shown above. Petitioners consent to electronic service by e-mail at the e-mail addresses provided above.

CLAIM LISTING APPENDIX
U.S. Patent No. 11,107,768 for Claims 1-28

Claim Designation	Claim Language
Claim 1(Pre)	A chip package comprising:
Claim 1(a)	a first polymer layer having a first surface and a second surface opposite to said first surface,
Claim 1(a)(i)	wherein said first surface is substantially parallel to said second surface,
Claim 1(a)(ii)	wherein said first polymer layer has a thickness between 100 and 300 micrometers and
Claim 1(a)(iii)	has a coefficient of expansion between 3 and 10 ppm/° C.;
Claim 1(b)	a first metal plug vertically in a first through via in said first polymer layer,
Claim 1(b)(i)	wherein said first metal plug comprises a first copper layer, wherein the first copper layer contacts with a sidewall of said first through via;
Claim 1(c)	a second metal plug vertically in a second through via in said first polymer layer,
Claim 1(c)(i)	wherein said second metal plug comprises a second copper layer,
Claim 1(c)(ii)	wherein a top surface of said second metal plug and a top surface of said first metal plug are in the same horizontal plane;
Claim 1(d)	a first interconnection scheme over said first surface,
Claim 1(d)(i)	wherein said first interconnection scheme comprises a first metal interconnect over said first surface, a second metal interconnect over said first surface, a third metal interconnect over said first surface and a second polymer layer over said first, second and third metal interconnects,
Claim 1(d)(ii)	wherein said first metal interconnect is connected to said first metal plug, wherein said second metal interconnect is connected to said second metal plug,
Claim 1(d)(iii)	wherein said first metal interconnect comprises a first metal layer, a third copper layer on said first metal layer, and a fourth copper layer on said third copper layer;
Claim 1(e)	a first metal bump over said first interconnection scheme and said second metal plug,
Claim 1(e)(i)	wherein said first metal bump comprises a tin-containing layer; and

Claim Designation	Claim Language
Claim 1(f)	a first semiconductor chip under said first interconnection scheme,
Claim 1(f)(i)	wherein said first semiconductor chip comprises a fourth metal interconnect on a first metal pad of said first semiconductor chip,
Claim 1(f)(ii)	wherein said fourth metal interconnect comprises a second metal layer on said first metal pad and a fifth copper layer over said second metal layer, wherein said fifth copper layer has a thickness between 5 and 30 micrometers,
Claim 1(f)(iii)	wherein said fourth metal interconnect is connected to said third metal interconnect.
Claim 2	The chip package of claim 1, further comprising a passive component over said first interconnection scheme and connected to said first interconnection scheme through a solder layer.
Claim 3	The chip package of claim 1, wherein said first interconnection scheme comprise a fifth metal interconnect across over a sidewall of the first semiconductor chip.
Claim 4(a)	The chip package of claim 1, further comprising a second semiconductor chip over said first interconnection scheme,
Claim 4(b)	wherein said second semiconductor chip comprises a second metal bump between said second semiconductor chip and said first interconnection scheme.
Claim 5	The chip package of claim 1, wherein said first semiconductor chip comprises a central-processing-unit (CPU) circuit block and a graphics-processing-unit (GPU) circuit block.
Claim 6(a)	The chip package of claim 1, wherein said first semiconductor chip comprises a second metal pad on a top surface of said first semiconductor chip and a third metal pad on a bottom surface of said first semiconductor chip,
Claim 6(b)	wherein said second metal pad is connected to said third metal pad through a through-silicon-via metal layer.
Claim 7(a)	The chip package of claim 1, wherein said first interconnection scheme further comprises a fifth metal interconnect over said first metal interconnect and said second polymer layer,
Claim 7(b)	wherein said second polymer is between said first and fifth metal interconnects,

Claim Designation	Claim Language
Claim 7(c)	wherein said fifth metal interconnect comprises a third metal layer, a sixth copper layer on said third metal layer, and a seventh copper layer on said sixth copper layer.
Claim 8	The chip package of claim 1, further comprising a second interconnection scheme under said first polymer layer and on said second surface.
Claim 9	The chip package of claim 1, wherein said first metal plugs has a top surface substantially coplanar with said first surface.
Claim 10	The chip package of claim 1, wherein said first metal pad is an aluminum pad.
Claim 11(a)	The chip package of claim 1, further comprising a second semiconductor chip over said first interconnection scheme and connected to said first interconnection scheme through a second metal bump,
Claim 11(b)	wherein said second semiconductor chip has a height is between a backside surface of said second semiconductor chip and a top surface of said second polymer layer is smaller than a thickness of said first metal bump.
Claim 12(a)	The chip package of claim 1, further comprising a second semiconductor chip under said first semiconductor chip,
Claim 12(b)	wherein said first semiconductor chip comprises a second metal pad connected to a third metal pad of said second semiconductor chip through a solder layer, wherein said solder layer between said first and second semiconductor chips.
Claim 13(a)	The chip package of claim 1, further comprising a second semiconductor chip under said first semiconductor chip,
Claim 13(b)	wherein said first semiconductor chip comprises a second metal pad on a top surface of said first semiconductor chip, a third metal pad on a bottom surface of said first semiconductor chip
Claim 13(c)	and a through-silicon-via metal layer connects to said second metal pad,
Claim 13(d)	wherein said third metal pad is connected to a fourth metal pad of said second semiconductor chip.
Claim 14	The chip package of claim 1, further comprising a third metal plug vertically in a third through via in said first polymer layer, wherein a pitch between said first and third metal plugs is between 200 and 1000 micrometers.

Claim Designation	Claim Language
Claim 15	The chip package of claim 1, wherein said first metal plug has a thickness between 100 and 300 micrometers.
Claim 16(Pre)	A chip package comprising:
Claim 16(a)	a first polymer layer having a first surface and a second surface opposite to said first surface,
Claim 16(a)(i)	wherein said first surface is substantially parallel to said second surface,
Claim 16(a)(ii)	wherein said first polymer layer has a thickness between 100 and 300 micrometers;
Claim 16(b)	a first metal plug vertically in a first through via in said first polymer layer,
Claim 16(b)(i)	wherein said first metal plug comprises a first copper layer, wherein the first copper layer contacts with a sidewall of said first through via;
Claim 16(c)	a second metal plug vertically in a second through via in said first polymer layer,
Claim 16(c)(i)	wherein said second metal plug comprises a second copper layer,
Claim 16(c)(ii)	wherein a top surface of said second metal plug and a top surface of said first metal plug are in the same horizontal plane;
Claim 16(d)	a first interconnection scheme over said first surface,
Claim 16(d)(i)	wherein said first interconnection scheme comprises a first metal interconnect over said first surface, a second metal interconnect over said first surface and a second polymer layer over said first and second metal interconnects,
Claim 16(d)(ii)	wherein said first metal interconnect is connected to said first metal plug,
Claim 16(d)(iii)	wherein said first metal interconnect comprises a first metal layer, a third copper layer on said first metal layer, and a fourth copper layer on said third copper layer;
Claim 16(e)	a first metal bump over said first interconnection scheme,
Claim 16(e)(i)	wherein said first metal bump is connected to said first interconnection scheme through a first opening in said second polymer layer,
Claim 16(e)(ii)	wherein said first metal bump comprises a tin-containing layer;
Claim 16(f)	a second metal bump over said first interconnection scheme,

Claim Designation	Claim Language
Claim 16(f)(i)	wherein said second metal bump is connected to said first interconnection scheme through a second opening in said second polymer layer;
Claim 16(g)	a first semiconductor chip over said first interconnection scheme and between said first and second metal bumps;
Claim 16(h)	a third metal bump between said first semiconductor chip and said first interconnection scheme,
Claim 16(h)(i)	wherein said third metal bump connected to said second metal interconnect through a third opening in said second polymer layer; and
Claim 16(i)	a second semiconductor chip under said first interconnection scheme and said first semiconductor chip,
Claim 16(i)(i)	wherein said first interconnection scheme is between said first and second semiconductor chips,
Claim 16(i)(ii)	wherein said second semiconductor chip comprises a central-processing-unit (CPU) circuit block and a graphics-processing-unit (GPU) circuit block.
Claim 17	The chip package of claim 16, further comprising a third semiconductor chip over said first interconnection scheme.
Claim 18	The chip package of claim 16, wherein said second semiconductor chip comprises a first metal pad on a top surface of said second semiconductor chip and a second metal pad on a bottom surface of said second semiconductor chip, wherein said first metal pad is connected to said second metal pad through a through-silicon-via metal layer.
Claim 19	The chip package of claim 16, further comprising a third metal plug vertically in a third through via in said polymer layer, wherein a pitch between said first and third metal plugs is between 200 and 1000 micrometers.
Claim 20	The chip package of claim 16, wherein said first polymer layer has a coefficient of expansion between 3 and 10 ppm/°C.
Claim 21(a)	The chip package of claim 16, further comprising a third semiconductor chip under said second semiconductor chip and
Claim 21(b)	multiple fourth metal bumps between said second and third semiconductor chips,

Claim Designation	Claim Language
Claim 21(c)	wherein said second semiconductor chip comprises a first metal pad on a top surface of said second semiconductor chip and a second metal pad on a bottom surface of said second semiconductor chip,
Claim 21(d)	wherein said first metal pad is connected to said second metal pad through a through-silicon-via metal layer.
Claim 22	The chip package of claim 16, further comprising a passive component over said first surface.
Claim 23	The chip package of claim 16, wherein said first interconnection scheme comprise a third metal interconnect across over a sidewall of the second semiconductor chip.
Claim 24	The chip package of claim 16, further comprising a third semiconductor chip under said first interconnection scheme, wherein said third semiconductor chip is a memory chip.
Claim 25(a)	The chip package of claim 16, wherein said second semiconductor chip comprises a third metal interconnect on a metal pad of said second semiconductor chip,
Claim 25(b)	wherein said third metal interconnect comprises a second metal layer on said metal pad and a fifth copper layer over said second metal layer, wherein said fifth copper layer has a thickness between 5 and 30 micrometers,
Claim 25(c)	wherein said third metal interconnect is connected to said a fourth metal interconnect of said first interconnection scheme.
Claim 26	The chip package of claim 16, wherein a height is between a backside surface of said first semiconductor chip and a top surface of said second polymer layer is smaller than a thickness of said first metal bump.
Claim 27	The chip package of claim 16, wherein said second semiconductor chip is coupled to said first semiconductor chip through said first interconnection scheme.
Claim 28	The chip package of claim 16, wherein said first metal plug has a thickness between 100 and 300 micrometers.

APPENDIX OF EXHIBITS

Exhibit 1001	U.S. Patent No. 11,107,768
Exhibit 1002	File History of the '768 Patent
Exhibit 1004	U.S. Patent No. 9,167,694 to Sundaram, et al.
Exhibit 1005	U.S. Patent Publication No. 2010/0290191 to Lin, et al.
Exhibit 1006	U.S. Patent Publication No. 2011/0215458 to Camacho, et al.
Exhibit 1007-1008	Intentionally left blank
Exhibit 1009	U.S. Patent No. 8,709,933 to Haba, et al.
Exhibit 1010	U.S. Patent No. 9,123,763 to Yu, et al.
Exhibit 1011	Intentionally left blank
Exhibit 1012	Andrea Chen, et al. *Semiconductor Packaging Materials Interaction and Reliability*, CRC Press, 2012
Exhibit 1013	Philip Garrou, et al., *RDL: an integral part of today's advanced packaging technologies*, Solid State Technology, May 2011
Exhibit 1014	U.S. Patent No. 8,780,576 to Haba, et al.
Exhibit 1015	U.S. Patent No. 7,902,648 to Lee
Exhibit 1016	U.S. Patent No. 7,964,961 to Lee, et al.
Exhibit 1017	U.S. Patent No. 7,241,641 to Savastiouk, et al.
Exhibit 1018	U.S. Patent Publication No. 2005/0110168 to Chuang
Exhibit 1019	U.S. Patent Publication No. 2011/0026232 to Lin, et al.
Exhibit 1020	U.S. Patent No. 5,086,558 to Grube, et al.
Exhibit 1021	U.S. Patent Publication No. 2011/0193219 to Lai, et al.
Exhibit 1022	U.S. Patent No. 6,818,545 to Lee, et al.
Exhibit 1023	U.S. Patent No. 6,974,659 to Su, et al.
Exhibit 1024	U.S. Patent Publication No. 2006/0175686 to Murata, et al.
Exhibit 1025	U.S. Patent Publication No. 2012/0098124 to Wu, et al.
Exhibit 1026	U.S. Patent No. 8,193,604 to Lin et al.
Exhibit 1027	U.S. Patent Publication No. 2004/0203224 to Halahan, et al.
Exhibit 1028	Philip Garrou, *Introduction to 3D Integration,* Handbook of 3D integration: Volumes 1 and 2, Technology and Application of 3D Integrated Circuits, 2012
Exhibit 1029	U.S. Patent Publication No. 2003/0068877 to Kinsman
Exhibit 1030	U.S. Patent Publication No. 2010/0246152 to Lin, et al.
Exhibit 1031	Yi Yang, et al, *CPU-Assisted GPGPU on Fused CPU-GPU Architectures,* IEEE Xplore
Exhibit 1032-1034	Intentionally left blank

Exhibit 1035	E.D. Blackshear, et al., *The evolution of build-up package technology and its design challenges*, International Business Machines Corporation, 2005
Exhibit 1036	Intentionally left blank
Exhibit 1037	U.S. Patent No. 7,374,969 to Cho, et al.
Exhibit 1038	Intentionally left blank
Exhibit 1039	Intentionally left blank
Exhibit 1040	U.S. Patent No. 6,619,538 to Test, et al.
Exhibit 1041	Intentionally left blank
Exhibit 1042	U.S. Patent No. 6,831,003 to Huang, et al.
Exhibit 1043	U.S. Patent Publication No. 2009/0226611 to Suzuki, et al.
Exhibit 1044	U.S. Patent No. 6,077,726 to Mistry, et al.
Exhibit 1045	U.S. Patent Publication No. 2010/0244245 to Pendse, et al.
Exhibit 1046	U.S. Patent Publication No. 2012/0206160 to Wu, et al.
Exhibit 1047	U.S. Patent Publication No. 2009/0174052 to Sogawa, et al.
Exhibit 1048	U.S. Patent Publication No. 2013/0100624 to Carpenter, et al.
Exhibit 1049	U.S. Patent No. 7,047,515 to Vitek, et al.
Exhibit 1050	U.S. Patent No. 8,116,097 to Love, et al.
Exhibit 1051	U.S. Patent Publication No. 2009/0237900 to Origuchi, et al.
Exhibit 1052	U.S. Patent Publication No. 2005/0002167 to Hsuan, et al.
Exhibit 1053	U.S. Patent Publication No. 2008/0067695 to Chow, et al.
Exhibit 1054	U.S. Patent No. 6,489,240 to Iacoponi, et al.
Exhibit 1055	U.S. Patent No. 6,578,178 to Mau
Exhibit 1056	U.S. Patent Publication No. 2012/0001190 to Okabe, et al.
Exhibit 1057	U.S. Patent No. 7,307,348 to Wood, et al.
Exhibit 1058	U.S. Patent No. 8,138,014 to Chi, et al.
Exhibit 1059	U.S. Patent No. 6,506,672 to Dagenais, et al.
Exhibit 1060	Intentionally left blank
Exhibit 1061	U.S. Patent Publication No. 2009/0261473 to Lee, et al.
Exhibit 1062	Intentionally left blank
Exhibit 1063	U.S. Patent No. 6,812,143 to Lane, et al.
Exhibit 1064	Intentionally left blank
Exhibit 1065	U.S. Patent Publication No. 2011/0147950 to Tai, et al.
Exhibit 1066	U.S. Patent Publication No. 2009/0070727 to Solomon
Exhibit 1067	U.S. Patent Publication No. 2012/0098114 to Ishibashi
Exhibit 1068	U.S. Patent Publication No. 2011/0074028 to Pendse
Exhibit 1069-1070	Intentionally left blank
Exhibit 1071	U.S. Patent No. 7,649,368 to Eldridge, et al.

Exhibit 1072-1077	Intentionally left blank
Exhibit 1078	U.S. Patent Publication No. 2012/0139068 to Stacey
Exhibit 1079	Intentionally left blank
Exhibit 1080	U.S. Patent Publication No. 2012/0319251 to Yu, et al.
Exhibit 1081	U.S. Patent No. 7,838,759 to Alley, et al.
Exhibit 1082	U.S. Patent No. 6,982,874 to Smalc, et al.
Exhibit 1083	U.S. Patent Publication No. 2009/0166069 to Kinoshita
Exhibit 1084	U.S. Patent No. 7,759,782 to Haba, et al.
Exhibit 1085	U.S. Patent No. 6,946,727 to Ho, et al.
Exhibit 1086	U.S. Patent Publication No. 2003/0013298 to May
Exhibit 1087	U.S. Patent No. 5,834,945 to Akram, et al.
Exhibit 1088	U.S. Patent No. 6,611,046 to Yang
Exhibit 1089	U.S. Patent No. 7,638,254 to Hattori, et al.
Exhibit 1090	U.S. Patent Publication No. 2005/0156280 to Patel, et al.
Exhibit 1091	U.S. Patent Publication No. 2011/0215470 to Chen, et al.
Exhibit 1092	Moody Dreiza, et al., *High Density PoP (Package-on-Package) and Package Stacking Development*, Electronic Components and Technology Conference, 2007
Exhibit 1093	U.S. Patent No. 6,107,180 to Munroe, et al.
Exhibit 1094	U.S. Patent Publication No. 2011/0210283 to Ramirez, et al.
Exhibit 1095	U.S. Patent No. 6,452,502 to Dishongh, et al.
Exhibit 1096	U.S. Patent No. 6,344,401 to Lam.
Exhibit 1097	Richard K. Ulrich, et al., *Advanced Electronic Packaging,* IEEE Press Series on Microelectrical Systems, 2006
Exhibit 1098	Mulugeta Abtew, et al., *Lead-free Solders in Microelectronics*, Materials Science and Engineering, 2000
Exhibit 1099	Karl J. Puttlitz, et al., *Handbook of Lead-Free Solder Technology for Microelectronic Assemblies*, 2005
Exhibit 1100	U.S. Patent Publication No. 2013/0309832 to Cheng, et al.
Exhibit 1101	U.S. Patent Publication No. 2013/0151869 to Steinman, et al.
Exhibit 1102	Linely Gwennap, *Sandy Bridge Spans Generations: Intel Focuses on Graphics, Multimedia in New Processor Design*, Microprocessor, 2010
Exhibit 1103	Intentionally left blank
Exhibit 1104	U.S. Patent No. 6,710,447 to Nogami.
Exhibit 1105	U.S. Patent Publication No. 2011/0059305 to Kaneya, et al.
Exhibit 1106	U.S. Patent No. 7,057,896 to Matsuo, et al.
Exhibit 1107	U.S. Patent No. 7,777,333 to Bachman, et al.

Exhibit 1108	U.S. Patent No. 7,095,105 to Cherukuri, et al.
Exhibit 1109	U.S. Patent No. 7,423,347 to Chen, et al.
Exhibit 1110	U.S. Patent Publication No. 2008/0128891 to Ziglioli, et al.
Exhibit 1111	U.S. Patent Publication No. 2008/0042280 to Lin, et al.
Exhibit 1112	U.S. Patent No. 7,923,836 to Farooq, et al.
Exhibit 1113	U.S. Patent Publication No. 2005/0121711 to Pogge, et al.
Exhibit 1114	U.S. Patent Publication No. 2012/0313240 to Cheng, et al.
Exhibit 1115	U.S. Patent No. 7,262,444 to Fillion, et al.
Exhibit 1116	U.S. Patent Publication No. 2013/0037944 to Lee, et al.
Exhibit 1117-1125	Intentionally left blank
Exhibit 1126	U.S. Patent No. 8,592,988 to Lee, et al.
Exhibit 1127	Intentionally left blank
Exhibit 1128	U.S. Patent No. 6,528,179 to Jimarez, et al.
Exhibit 1129	U.S. Patent No. 6,468,413 to Fanti, et al.
Exhibit 1130	U.S. Patent No. 8,132,775 to Goldmann.
Exhibit 1131	U.S. Patent Publication No. 2011/0186977 to Chi, et al.
Exhibit 1132	U.S. Patent No. 7,169,627 to Duh, et al.
Exhibit 1133	U.S. Patent No. 6,614,243 to Klehn, et al.
Exhibit 1134	U.S. Patent Publication No. 2009/0162622 to Van Veen, et al.
Exhibit 1135	U.S. Patent No. 6,570,259 to Alcoe, et al.
Exhibit 1136	U.S. Patent No. 7,741,567 to Beddingfield, et al.
Exhibit 1137	U.S. Patent No. 6,407,341 to Anstrom, et al.

CERTIFICATION OF WORD COUNT

The undersigned certifies pursuant to 37 C.F.R. § 42.24 that the foregoing Petition for *Inter Partes* Review, excluding any table of contents, mandatory notices under 37 C.F.R. § 42.8, certificates of service or word count, or appendix of exhibits, contains 13,759 words according to the word-processing program used to prepare this document (Microsoft Word).

Dated: November 21, 2025

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CERTIFICATE OF SERVICE ON PATENT OWNER
UNDER 37 C.F.R. § 42.105

Pursuant to 37 C.F.R. §§ 42.6(e) and 42.105(b), the undersigned certifies that on November 21, 2025, a complete and entire copy of this Petition for *Inter Partes* Review and Exhibits were provided via Federal Express to the Patent Owner by serving the correspondence address of record for the '768 Patent:

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