

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TAIWAN SEMICONDUCTOR
MANUFACTURING COMPANY LTD. and APPLE INC.
Petitioners

v.

MYW SEMITECH, LLC,
Patent Owner

U.S. Patent No. 11,107,768
Issue Date: August 31, 2021

Title: CHIP PACKAGE

Inter Partes Review No. IPR2026-00065

PATENT OWNER'S RESPONSE

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PATENT OWNER'S EXHIBIT LIST

Exhibit No.	Description
2001	U.S. Patent No. 9,615,453
2002	Information Disclosure Statement for U.S. Application No. 17/929,180 dated December 21, 2023
2003	[SEALED] Email chain between Richard Juang, counsel for MYW Semitech, and Daniel Richards, counsel for Apple Inc., regarding production of materials
2004	[SEALED] Defendant Apple Inc.'s First Supplemental Responses to Plaintiff MYW Semitech, LLC's First Set of Interrogatories (Nos. 1-12)
2005	[SEALED] Email chain between Richard Juang, counsel for MYW Semitech, and Daniel Richards, counsel for Apple Inc., regarding availability of source code
2006	[SEALED] Email chain between Richard Juang and Peter Yang, counsel for TSMC, regarding inventorship.
2007	Oral Order for Motion to Stay Pending <i>Inter Partes</i> Review, <i>MYW Semitech, LLC v. Apple Inc.</i> , 1-25-cv-00504 (DDE) Dkt. 68 (January 21, 2026)
2008	Stipulation and [Proposed] Order to Amend Scheduling Order, <i>MYW Semitech, LLC v. Apple Inc.</i> , 1-25-cv-00504 (DDE) Dkt. 58 (December 3, 2025)
2009	Apple Inc.'s Infringement Contentions, <i>MYW Semitech, LLC v. Apple Inc.</i> , 1-25-cv-00504 (DDE) (January 9, 2026)
2010	Agreed Stipulation Regarding the Discovery of Electronically Stored Information, <i>MYW Semitech, LLC v. Apple Inc.</i> , 1-25-cv-00504 (DDE) Dkt. 39 (October 14, 2025)
2011	Revision to Rules of Practice Before the Patent Trial and Appeal

	Board, 90 Fed. Reg. 48,335 (proposed Oct. 17, 2025) (to be codified at 37 C.F.R. pt. 42).
2012	Declaration of Richard Juang
2013	Default Protective Order
2014	Apple Inc.’s Proposed Constructions in <i>MYW Semitech, LLC v. Apple Inc.</i> , C.A. No. 25-504-RGA-EGT (Feb. 12, 2026)
2015	Joint Claim Construction Chart in <i>MYW Semitech, LLC v. Apple Inc.</i> , C.A. No. 25-504-RGA-EGT (Feb. 26, 2026)
2016	Defendant Apple Inc.’s Answering Claim Construction Brief
2017	Defendant Apple Inc.’s Initial Invalidity Contentions (Cover Document)
2018	Declaration of Professor David S. Ricketts
2019	CV of Professor David S. Ricketts
2020	Deposition Transcript of Stanley Shanfield, Ph. D., dated July 14, 2026.
2021	<i>Coefficient of Thermal Expansion (CTE)</i> , BYU Integr. Microfabrication Lab, https://cleanroom.byu.edu/cte_materials (last visited Aug. 6, 2026).
2022	Rogers Corp., <i>ULTRALAM® 3000 Liquid Crystalline Polymer Circuit Material</i> , Double-Clad Laminates, Data Sheet No. RF1.3000, Publication No. 92-125 (rev. May 10, 2011).
2023	Yoon, J., Shin, T., Kim, D. et al. Enhancing bonding strength of the electroplated Cu pillars for semiconductor package by controlling grain orientation. <i>Sci Rep</i> 16, 9814 (2026).

I. INTRODUCTION

The claims of the '768 Patent are directed to specific configurations of semiconductor chip packages. These specific configurations are necessary and beneficial in order to minimize the size of the semiconductor chip packages while ensuring the highest possible performance. EX1001 ['768 Patent], 1:24-41.

Because the claimed configurations are detailed and specific, none of the asserted references teach or suggest the claimed invention, either alone or in combination. The Petition relies on combinations of five different references. But even then, the proposed combinations do not map to the claimed configurations. As a result, the Petition's mapping to the claims distorts the references relied upon or maps the references inconsistently within the same challenged claim. For example, the Petition alleges Sundaram's figure 3 memory chip is the claimed semiconductor chip and that the memory chip comprises solder bumps that are allegedly the claimed fourth metal interconnect. But the solder bumps disclosed in Sundaram are external to said memory chip. Thus, Sundaram's memory chip does not "comprise" the solder bumps as required by the claims.

Similarly, claim 1(f)(ii) requires a "fourth metal interconnect comprises a second metal layer on said first metal pad and a fifth copper layer over said second metal layer, wherein said fifth copper layer has a thickness between 5 and 30 micrometers." EX1001 ['768 Patent], cl. 1. Because none of the metal layers

disclosed in the prior art meet this limitation, the Petition attempts to combine multiple discrete layers from Lin-191 into a single layer.

The other primary references in grounds 2A through 3C—Haba and Yu—have similar deficiencies. For example, the alleged fourth metal interconnects in Haba are, like Sundaram, are located external to the alleged semiconductor chip; thus, Haba’s alleged semiconductor chip does not comprise a fourth metal interconnect as required by the claims. For Yu, Petitioners allege the same conductive pathway in Yu is simultaneously the claimed “first metal interconnect” and the claimed “second metal interconnect.” But because the claims require a first and second interconnect, a single conductive pathway cannot serve as both. And both grounds attempt to supply missing limitations using the same flawed mapping to Lin-191.

For these and the other reasons described in more detail below, the Petition fails to demonstrate by a preponderance of the evidence that any challenged claim is unpatentable.

II. BACKGROUND

A. Procedural History

Patent Owner (“PO”) is asserting the ’768 Patent (along with U.S. Patent Nos. 11,538,763 (“the ’763 Patent”) and 11,894,306 (“the ’306 Patent”)) against

Petitioner Apple in *MYW Semitech, LLC v. Apple Inc.*, Case No. 1:25-cv-00504. (D. Del. 2025). That case was filed on April 24, 2025.

On November 21, 2025, Petitioners filed this IPR, along with IPR2026-00066 and IPR2026-00067 challenging the '763 and '306 Patents, respectively. The district court litigation was stayed on June 16, 2026 pending resolution of these IPRs.

B. The '768 Patent

The '768 Patent was filed as application No. 16/752,650 on January 26, 2020. It is a continuation of application No. 15/261,956, filed on September 11, 2016, now Patent No. 10,622,310, which is a continuation-in-part of application No. 14/036,256, filed on September 25, 2013, now Patent No. 9,615,453. The '768 Patent claims priority to provisional application No. 61/705,649, filed on September 26, 2012, and provisional application No. 62/219,249, filed on September 16, 2015.

The '768 Patent discloses a “method and structure to manufacture a glass substrate” and a “chip building a system on the glass substrate.” *See* EX1001, 1:18-19. EX2018 [Ricketts Decl.], ¶¶67-72. The glass substrate comprises “multiple metal conductors through in said glass substrate and multiple metal bumps are between said glass substrate and said display panel substrate, wherein said one of said metal conductors is connected to one of said contact pads through one of said

metal bumps.” *Id.*, Abstract. In certain embodiments, the invention may use polymer layers in addition to glass layers (*see id.*, 6:18-46), or “the glass layer [] may be replaced by a polymer layer.” *Id.*, 7:42-43. “When the polymer layer [is] cured to a solid state, then the polymer layer has a coefficient of expansion between 3 and 10 ppm/°C.” *Id.*, 7:43-45.

The ’768 Patent has 2 independent claims (1 and 16) and 26 claims that depend from claims 1 and 16. The claims are directed to chip packages using polymer layers with specific layouts of metal plugs and interconnects. EX2018 [Ricketts Decl.], ¶¶ 73-75.

C. Petitioners’ Cited References

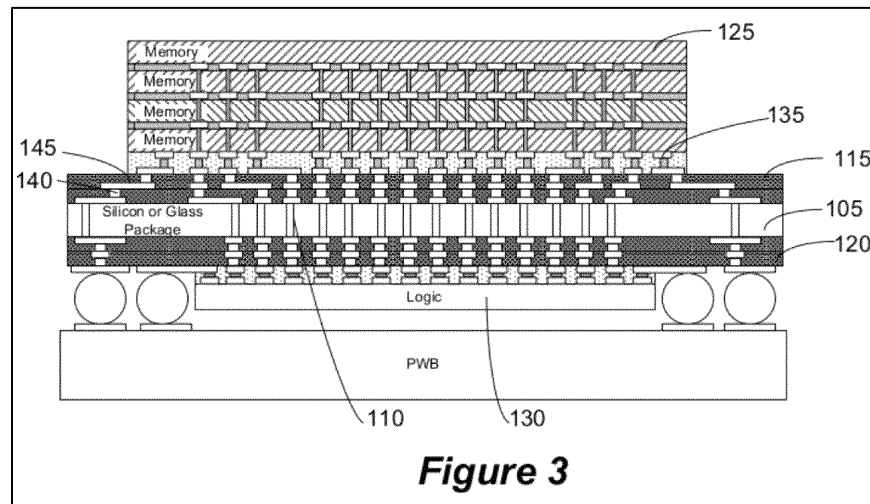
The Petition advances the following seven grounds:

Grounds	Claims Challenged	35 U.S.C. §	References
<u>1A</u>	1-15, 20	103	Sundaram (EX1004), Haba, (EX1009), and Lin-191 (EX1005)
<u>1B</u>	16-19, 21-28	103	Sundaram and Lin-191
<u>2A</u>	1-3, 5, 7-10, 14-15	103	Haba and Lin-191
<u>2B</u>	4, 6, 11-13,	103	Haba, Lin-191, and Sundaram
<u>3A</u>	16-17, 19, 22-28	103	Yu (EX1010) and Lin-191
<u>3B</u>	18, 21	103	Yu, Lin-191, and Camacho (EX1006)
<u>3C</u>	20	103	Yu, Lin-191, and Haba

Pet., 2.

1. Sundaram (EX1004)

Sundaram is directed to a 3D interconnect structure comprising an ultra-thin interposer having a plurality of ultra-high density through-via interconnections defined therein. EX1004, Abstract. Sundaram figure 3 (relied on in the Petition) shows Sundaram's interconnect structure comprising an interposer defining a plurality of through visas:

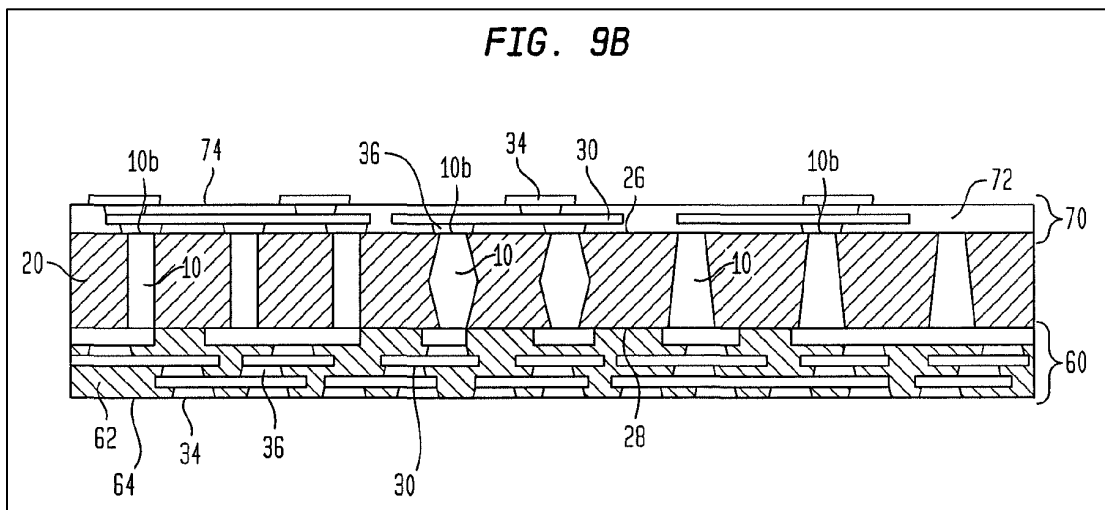


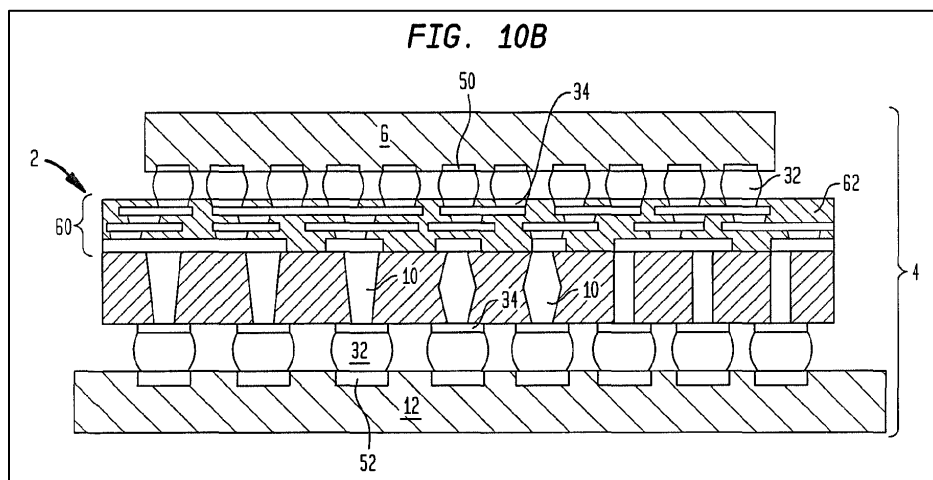
Id., Fig. 3. “[T]he interconnect structure comprises an interposer 105 having a first side 115 and a second side 120.” *Id.*, 5:47-48. “A plurality of ultra-small through vias 110 can be defined within the interposer 105 such that each of the through vias 110 extends from the first side 115 to the second side 120 of the interposer 105.” *Id.*, 6:6-9. These “through vias 110 are ultra-small and can range from about 1-25 micrometers in diameter at about 3-50 micrometers in pitch.” *Id.*,

6:11-13. “A first electronic device 125 can be attached to the first side 115 of the interposer 105 and a second electronic device 130 can be attached to the second side 120 of the interposer 105.” *Id.*, 6:34-36. “[E]lectronic devices having different I/O pad layouts and sizes can also be connected through the use of blind vias 140 and conductor traces 145 defined within polymer-metal redistribution layers deposited on the first side 115 and second side 120 of the interposer 105.” *Id.*, 6:62-67.

2. Haba (EX1009)

Haba discloses a method for making an interconnection component including forming a plurality of metal posts extending away from a reference surface. EX1009, Abstract. The Petition relies on Haba figures 9B and 10B:





Id., figures 9B, 10B. Haba figure 9B discloses “interconnection component 2 having a second redistribution layer 70 formed along surface 26” in addition to redistribution layer 60. *Id.*, 7:57-59.

Haba figure 10B is a “variation[] of a microelectronic assembly respectively including interconnection components according to the embodiments of FIGS. 8 and 9A.” *Id.*, 5:4-6. Fig. 10A discloses that “microelectronic element 6 has contacts 50 having a smaller pitch than the pitch of contacts 52 on printed circuit board (“PCB”) 12.” *Id.*, 7:45-47. “FIG. 10B is similar to that which is shown in 10A, except that pads 34 which overlie end surfaces 10B act as wettable contacts for attachment to contacts 52 of PCB 12 using solder balls 32.” *Id.*, 7:53-56. Haba figure 10B lacks the second redistribution layer 70 of figure 9B.

3. Lin-191 (EX1005)

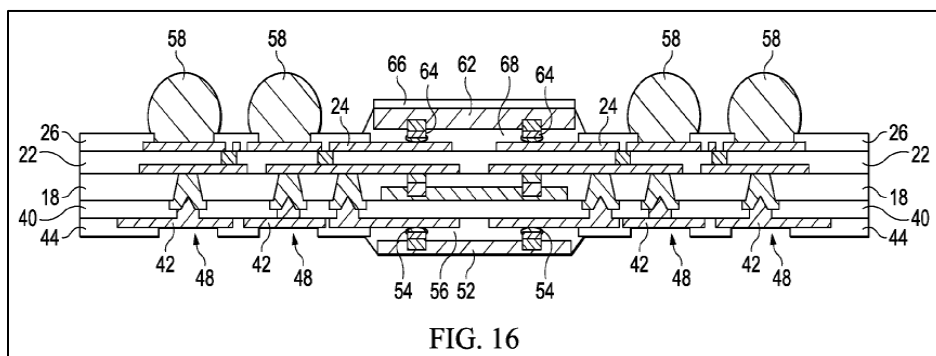
Lin-191 discloses “system-in packages” comprising multi-layer chips in a multi-layer polymer structure. EX1005, Abstract. Lin-191 explains that:

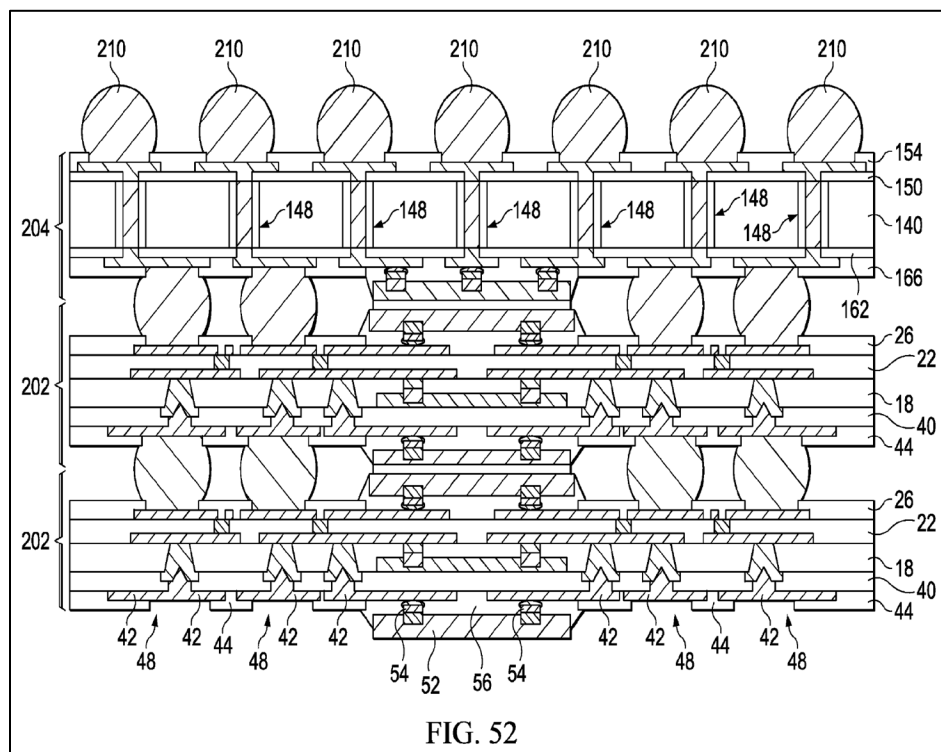
System-in packages, or multichip modules, are described which can include multi-layer chips in a multi-layer polymer structure, on-chip metal bumps on the multi-layer chips, intra-chip metal bumps in the multi-layer polymer structure, and patterned metal layers in the multi-layer polymer structure. The multi-layer chips in the multi-layer polymer structure can be connected to each other or to an external circuit through the on-chip metal bumps, the intra-chip metal bumps and the patterned metal layers. The system-in packages can be connected to external circuits through solder bumps, meal bumps or wirebonded wires.

Id.

4. Yu (EX1010)

Yu discloses a package-on-package (POP) structure having at least one package comprising one die being disposed in a core material between first and second surfaces of the core material. EX1010, Title. The Petition relies primarily on Yu figures 16 and 52:





Id., figures 16, 52. Yu provides limited discussion of these figures. Yu figure 16 is an “example of a second portion of a process for forming a package according to an embodiment.” *Id.*, 2:1-3. Yu explains that “In FIG. 16, an underfill material 68, such as liquid epoxy, deformable gel, silicon rubber, the like, or a combination thereof, is dispensed and cured between the third die 62 and the front side of the package, such as between the third die 62 and the second metallization layer 24.” *Id.*, 4:67-5:4.

Yu figure 52 shows a “step to form electrical connectors on the PoP structure of FIG. 51.” *Id.*, 2:15-16. “In FIG. 52, connectors 210, such as BGA balls, formed

coupled to a metallization layer on a front side of the interposer of the interposer package 204, similar to FIG. 50.” *Id.*, 8:36-39.

III. LEVEL OF ORDINARY SKILL

Petitioners allege the following level of ordinary skill:

A person of ordinary skill in the art (“POSITA”) relating to the subject matter of the ’750 patent as of the Critical Date would have had a bachelor’s degree in Computer Engineering, Electrical Engineering, Computer Science, or a comparable field and at least two years of experience related to computer architecture. AMD1003, ¶¶27–28. Additional experience could substitute for a formal degree or formal training (and *vice versa*). *Id.*

Pet., 1. For the purposes of this POR, PO does not dispute Petitioners’ level of ordinary skill. EX2018 [Ricketts Decl.], ¶¶44-45.

IV. CLAIM CONSTRUCTION

Petitioners allege that claim construction is unnecessary for this IPR. Pet., 2. For the purposes of this POR, PO does not believe any claims need to be construed. EX2018 [Ricketts Decl.], ¶46.

V. PETITIONERS FAIL TO DEMONSTRATE BY A PREPONDERANCE OF THE EVIDENCE THAT ANY OF THE CHALLENGED CLAIMS ARE UNPATENTABLE

The claims of the ’768 Patent are directed to specific configurations of semiconductor materials useful for semiconductor chip packages. The Petition fails

to demonstrate that any of the prior art, either alone or in combination, discloses the specific configurations required by the claims. For example, the Petition alleges Sundaram's figure 3 memory chip is the claimed semiconductor chip and that the memory chip comprises solder bumps that are allegedly the claimed fourth metal interconnect. But the solder bumps disclosed in Sundaram are external to said memory chip. Thus, Sundaram's memory chip does not "comprise" the solder bumps as required by the claims.

Similarly, claim 1(f)(ii) requires "fourth metal interconnect comprises a second metal layer on said first metal pad and a fifth copper layer over said second metal layer." EX1001 ['768 Patent], cl. 1. Because none of the metal layers disclosed in the prior art meet this limitation, the Petition attempts to combine multiple discrete layers from Lin-191 into a single layer.

The other primary references in grounds 2A through 3C—Haba and Yu—have similar deficiencies. For example, the alleged fourth metal interconnects in Haba are, like Sundaram, located external to the alleged semiconductor chip; thus, Haba's alleged semiconductor chip does not comprise a fourth metal interconnect. For Yu, Petitioner alleges the same interconnect in Yu is simultaneously the claimed "first metal interconnect" and the claimed "second metal interconnect." And both grounds attempt to supply missing limitations using the same flawed mapping to Lin-191 described above. For the reasons described detail below, the

Petition fails to demonstrate by a preponderance of the evidence that any challenged claim is unpatentable.

A. Grounds 1A and 1B

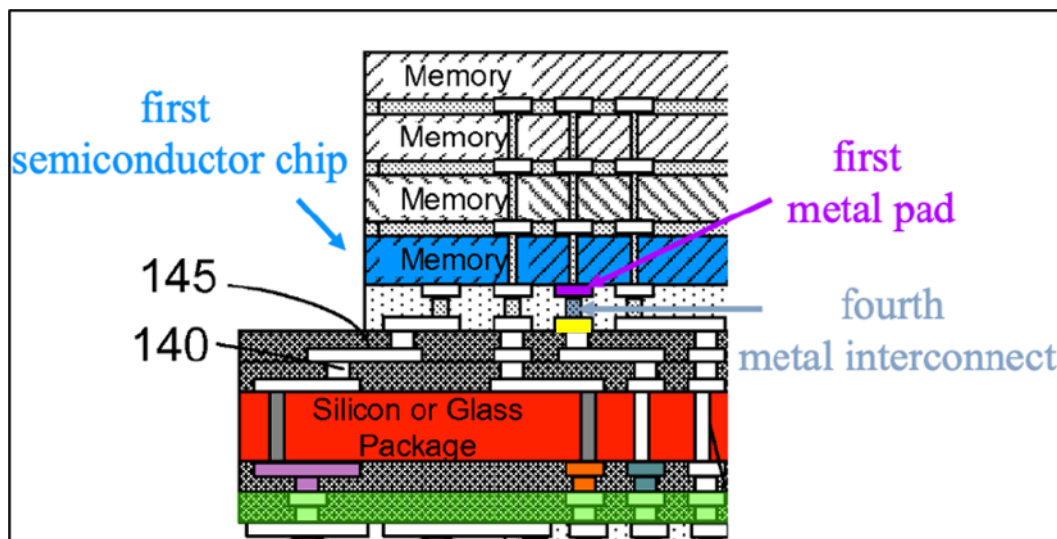
Grounds 1A-1B challenge claims 1-28. Pet., 2.

1. Sundaram and Lin-191 Fail To Teach Or Suggest Limitation 1(f)(i)

a) Sundaram’s memory chip does not comprise a “fourth metal interconnect on a first metal pad of said first semiconductor chip.”

Limitation 1(f)(i) requires that the “first semiconductor chip comprises a fourth metal interconnect.” EX1001 [’768 Patent], cl. 1. This limitation is not disclosed by Sundaram because Sundaram’s alleged semiconductor chip does not comprise or include Sundaram’s alleged fourth metal interconnect.

Petitioners argue that Sundaram’s figure 3 ““die pads 135...can electrically connect devices using solder, copper bumps with solder caps, copper to copper bonding,’ each of which teaches *a fourth metal interconnect*” and that ““[i]n FIG. 3, the fourth metal interconnect is a bump on die pad 135.” Pet., 21. (citing EX1004, 6:29-33.) That is, the Petition alleges (below) that the solder/bumps (gray) (located on top of the die pad 135 (yellow) of interposer 105) is the claimed “fourth metal interconnect”:



Pet., 21-22 (excerpting and annotating EX1004 [Sundaram], Fig. 3).

The structure the Petition identifies as the claimed “first semiconductor chip” (blue) does not comprise the alleged “fourth metal interconnect” (bump/solder shown in gray). This is because the bumps/solder (gray) are not part of the memory – the alleged “first semiconductor chip” (shown in blue). EX2018 [Ricketts Decl.], ¶87.

Instead, the bumps (or solder) (the alleged “fourth metal interconnect”) are formed *on the die pad 135 of the interposer 105*. Sundaram specifically states that the die pads 135 are associated *with the interposer 105*: “[t]he through vias 110 can be metalized in such a way that the metallization provides die pad surfaces 135 that correspond to each of the vias 110 on both the first side 115 and the second side 120 of the interposer 105.” EX1004 [Sundaram], 6:23-25; *see also* EX1004, 6:29-

33. Thus, Sundaram's bumps/solder are part of or associated with the interposer 105, not the alleged "first semiconductor chip." EX2018 [Ricketts Decl.], ¶¶88-89; EX1009 [Haba], 6:39-47; 7:42-56; 8:27-29; 11:33-35.

Limitation 1(f)(i) requires a "fourth metal interconnect on a first metal pad of said first semiconductor chip." EX1001 ['768 Patent], cl. 1. Sundaram's solder or bumps are formed on a die pad of the interposer 105, not on a metal pad of the semiconductor chip. The Petition identifies the electronic device 125 as the claimed first semiconductor chip. Pet., 20. Thus, the Petition places the alleged "fourth metal interconnect" on the interposer 105 and the alleged "first metal pad" on the alleged semiconductor chip. EX2018 [Ricketts Decl.], ¶90.

Sundaram does not describe the pads or interconnects of electronic device 125 at all. EX2018 [Ricketts Decl.], ¶91. The Petition does not identify any disclosure of those structures and certainly does not explain the component shown in purple above or what it is made of. *Id.* The Petition states instead that "[a] POSITA would understand that device 125 also has die pads such that an electrical connection is made between interposer 105 and device 125." Pet., 21. But Sundaram does not actually teach or suggest that device 125 has die pads; instead, Petitioners rely on a POSITA to supply this missing limitation. Petitioners may not rely on background knowledge of a POSITA to supply this limitation. *See* Memorandum from Coke Morgan Stewart, Acting Dir., U.S. Patent & Trademark

Off., on Enforcement and Non-Waiver of 37 C.F.R. § 42.104(b)(4) and Permissible Uses of General Knowledge in *Inter Partes* Reviews (July 31, 2025).¹

The Sundaram passage the Petition relies on is directed to the interposer. Pet., 21 (citing Sundaram, 6:29-33). Sundaram states that “[t]he die pads 135 that are formed on the first 115 and second sides 120 of the interposer 105 can electrically connect devices using solder, copper bumps with solder caps, copper to copper bonding, adhesive bonding, metallurgical bonding, non-conductive bonding, or combinations thereof.” EX1004 [Sundaram], 6:29-33. That sentence lists alternative methods for joining a device to the die pads of the interposer 105. EX2018 [Ricketts Decl.], ¶92. It does not describe any structure formed on electronic device 125 or the memory shown in blue above, and it does not describe the layered construction required by limitation 1(f)(ii).

Thus, the Petition’s combination of Sundaram and Lin-191 fails because it does not teach or suggest the “first semiconductor chip comprises a fourth metal interconnect.”

¹ *Available at*

https://www.uspto.gov/sites/default/files/documents/aapa_memo_final__signed.pdf

b) Lin-191 does not teach or suggest limitation 1(f)(1)

Petitioners do not allege that Lin-191 teaches or suggests the “first semiconductor chip comprises a fourth metal interconnect.” EX1001 [’768 Patent], cl. 1. Although Petitioners includes a short section on Lin-191 for Ground 1A limitation 1(f)(i), those sentences are directed to the claimed “metal pad,” not the claimed “fourth metal interconnect.” Pet., 23-24. The section does not allege Lin-191 teaches or suggests the “first semiconductor chip comprises a fourth metal interconnect.” EX2018 [Ricketts Decl.], ¶94. Thus, Lin-191 does not remedy the deficiency in Sundaram.

c) The Petitioner’s motivation to combine Lin-191 and Sundaram is conclusory

The Petitioner’s motivation to combine Lin-191 and Sundaram for limitation 1(f)(i) is ostensibly because the modification “is the application of a known technique (metal pads) to a known device (Sundaram’s semiconductor chip having die pads) ready for improvement to yield the predictable result of Sundaram’s device 125 having a first metal pad.” Pet. 24. This statement offers no substantive explanation as to why Sundaram’s metal pad (shown in purple above) required the application of the Lin-191’s metal pad teachings. EX2018 [Ricketts Decl.], ¶95. It presupposes that one would modify Sundaram without identifying any issues, shortcomings, or reasons to combine the references.

Further Sundaram and Lin-191 reflect fundamentally different engineering approaches to building a multi-chip structure, and a POSITA in 2012 would not have been motivated to merge them. EX2018 [Ricketts Decl.], ¶96. Lin-191 teaches a chip-first, tier-by-tier build in which the substrate is a work-in-progress rather than a finished component: chips carrying on-chip metal bumps are adhered to the substrate, encapsulated, and then polished or ground to expose the bumps before interconnections are formed, with the sequence repeated for each successive tier. EX1005, ¶[0009]. Consistent with that approach, Lin-191 does not form its through-substrate connections until late in the process — substrate 110 is first thinned to as little as 1 to 10 micrometers by mechanical grinding or chemical-mechanical polishing of its backside, EX1005, ¶[0290], and only then are through holes 16 and through-hole connections 17 formed from that newly exposed surface. EX1005, ¶¶[0292]–[0293]; EX2018 [Ricketts Decl.], ¶96.

Sundaram proceeds in the opposite order and for the opposite reason. EX2018 [Ricketts Decl.], ¶96. Sundaram builds and electrically verifies its interposer *before* any die is attached, and describes this chip-last sequence as the mechanism by which its structure “alleviates the Known Good Die (KGD) concerns in 3DIC integration.” EX1004 [Sundaram], 7:51-56, FIG. 6 (steps 605, 610, 615). Sundaram’s claims reinforce that its interposer is meant to be a

completed, verifiable article, requiring test pads on both sides to permit testing of devices attached to either side. EX1004 [Sundaram], cl. 21–22.

A POSITA seeking the benefits Sundaram describes would have understood that those benefits depend on the interposer being finished and tested before die attachment, and would therefore have seen no advantage in placing that interposer into Lin-191's process, where the substrate is deliberately left unfinished and is subsequently thinned, ground, and metallized from the backside after the chips are already in place. EX2018 [Ricketts Decl.], ¶96. The features a POSITA would have been looking to Sundaram for—through-vias, redistribution layers, and test pads—are the same features Lin-191's later processing steps would have been expected to disturb, and a POSITA would not have expected the combined arrangement to retain them or to function as Sundaram describes. *Id.* Conversely, a POSITA starting from Lin-191 and reordering its process to preserve Sundaram's pre-tested interposer would have had to abandon the tiered, chip-first integration that Lin-191 identifies as its contribution, including the high routing density between chips that Lin-191 attributes to its fine-pitched on-chip and intra-chip metal bumps. EX1005 [Lin-191], ¶¶[0010]–[0011]. A POSITA would not have had a reason to make either change, nor a reasonable expectation that the resulting structure would work as either reference intends. EX2018 [Ricketts Decl.], ¶96.

**2. Sundaram and Lin-191 Do Not Teach Or Suggest
Limitation 1(f)(ii)**

The Petition relies solely on Lin-191 for limitation 1(f)(ii). Pet., 24-25. As discussed below, Lin-191 does not teach or suggest this limitation.

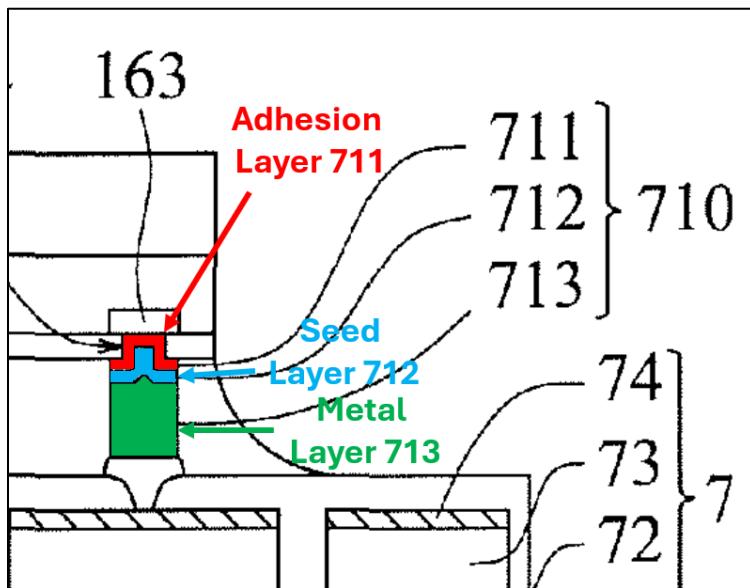
a) Lin-191 does not teach or suggest “said fourth metal interconnect.”

As discussed in §V.A.1.a above, the Petition fails to demonstrate that Sundaram teaches or suggests a “first semiconductor chip compris[ing] a fourth metal interconnect” because Sundaram’s memory chip does not comprise the solder/bumps alleged to be the claimed “said fourth metal interconnect.” *Supra*, §V.A.1.a.

Although the Petition alleges Lin-191’s bumps 710 are metal interconnects for limitation 1(f)(ii) (Pet., 24-25), the Petition does not rely on Lin-191 as teaching or suggesting that Sundaram’s first semiconductor chip comprises the claimed fourth metal interconnect, cl. 1(f)(i). *Id.* The Petition’s treatment of Lin-191 for limitation 1(f)(i) is directed to the claimed “metal pad,” stating only that “Lin-191 teaches a semiconductor chip 160 with ‘metal traces or pads 163’ that include ‘aluminum.’” Pet., 23-24 (emphasis removed). Thus, Lin-191 does not remedy the deficiency in Sundaram identified above. EX2018 [Ricketts Decl.], ¶¶98-99.

b) Lin-191 does not teach or suggest limitation 1(f)(ii)

Lin-191 does not disclose “a second metal layer on said first metal pad” as required by limitation 1(f)(ii). EX1001 [’768 Patent], cl. 1. The Petition alleges that “the combination of layers 711 and 712 [in Lin-191 Fig. 72] is a *second metal layer on metal pad 163.*” Pet., 25 (emphasis in original). But as Petitioners admit, adhesion layer 711 and seed layer 712 in Lin-191 figure 72 are *two different layers*:



EX1005 [Lin-191], Fig. 72 (excerpted and annotated); *see also* [0389] (“metal layer 713 under the seed layer 712 and over the solder joints 720.”); (“a seed layer 712 under the adhesion layer 711”). EX2018 [Ricketts Decl.], ¶¶100-101. The Petitioner even identified them as separate layers in 1(d)(iii). Pet., 15.

Petitioner combines layers 711 and 712 because the claim language requires that a second metal layer is on the first metal pad and that a copper layer is over the second metal layer. The alleged first metal pad is metal pad 163. But only adhesive layer 711 is on the metal pad 163 and the alleged copper layer 713 is over seed layer 712, not the adhesive layer 711. Thus, if layers 711 and 712 are not one layer, the claim limitation is not met. But, according to Petitioner's own admission, layers 711 and 712 are not the same layer. Ricketts Decl.], ¶102. Thus, Lin-191 fails to disclose "a second metal layer on said first metal pad and a fifth copper layer over said second metal layer."

A POSITA would not consider Lin-191's adhesion layer 711 and seed layer 712 to be a single layer. EX2018 [Ricketts Decl.], ¶103. Lin-191 does not refer to adhesion layer 711 and seed layer 712 as a single layer. EX1005 [Lin-191], [0389]-[0400]. Instead, Lin-191 is clear that adhesion layer 711 and seed layer 712 are two different layers made of different materials serving different purposes. EX1005 [Lin-191], [0389] ("a seed layer 712 under the adhesion layer 711"), Fig. 72 (excerpted and annotated), EX2018 [Ricketts Decl.], ¶103. A POSITA would understand an adhesion layer as a layer made to allow materials that are not compatible (in adhesion) to adhere to one another. *Id.* For example, Lin-191 explains that adhesion layer 711 is made of "titanium, a titanium-tungsten alloy, titanium nitride, chromium, tantalum, tantalum nitride, nickel or nickel vanadium"

and has a thickness of “less than 1 micrometer, such as between 1 nanometer and 0.5 micrometers.” EX1005 [Lin-191], [0390]. Conversely, Lin-191 explains that seed layer 712 is made of different materials (“copper, silver, gold, nickel or titanium-copper alloy”) having a different thickness (“less than 1 micrometer, such as between 10 nanometers and 0.8 micrometers.”). *Id.* Thus, a POSITA would understand that adhesion layer 711 and seed layer 712 are two different layers. *Id.*, EX2018 [Ricketts Decl.], ¶¶103-105.

Petitioners combination of adhesion layer 711 and seed layer 712 into a single layer is inconsistent with its own arguments elsewhere in the Petition where Petitioners recognize adhesion layers and seed layers constitute two different layers. For example, limitation 1(d)(iii) requires “said first metal interconnect comprises a first metal layer, a third copper layer on said first metal layer, and a fourth copper layer on said third copper layer.” EX1001 [’768 Patent], cl. 1. Petitioners allege Lin-191 figure 22’s adhesion layer 31 is the claimed “first metal layer” and seed layer 32 as the claimed “third copper layer.” Pet., 15. Thus, Petitioners allege for limitation 1(d)(iii) that Lin-191 discloses adhesion layers and seed layers as separate layers and accordingly map them to different claimed layers. Petitioners’ attempt to combine separate adhesion layers and seed layers for limitation 1(f)(ii) contradicts this mapping. EX2018 [Ricketts Decl.], ¶¶106-110;

See also Pet., 130. Petitioners' hindsight combination of two materially different semiconductor layers to arrive at a single claimed layer must be rejected.

For these reasons, the layout of the chip package claimed at '768 patent claim 1 is different than the layout of the semiconductors described in Lin-191. EX2018 [Ricketts Decl.], ¶111. Because of this, the Petition fails to map Lin-191 to limitation 1(f)(ii). Because neither Sundaram nor Lin-191 teaches or suggests limitation 1(f)(ii), the Petition fails to prove that claim 1 (or the claims depending therefrom) are unpatentable.

3. There is No Motivation to Combine Sundaram and Lin-191.

The Petition advances a separate motivation to combine for limitation 1(f)(ii), distinct from the motivation it advances for limitation 1(f)(i). Pet., 26. The Petition asserts that "Lin-191's metal bump provides improved metallurgical bonding and increased resistance to fatigue and stress-induced failure by employing a layered structure," and that the configuration "would reduce the risk of intermetallic formation at critical interfaces, mitigate electromigration, and better absorb mechanical strain during thermal cycling." *Id.* (citing EX1003 [Shanfield Decl.], ¶¶189-191).

Nothing in Lin-191 suggests adhesion layer 711 and seed layer 712 provide improved metallurgical bonding, increased resistance to fatigue or stress-induced

failure, reduced intermetallic formation, mitigation of electromigration, or improved absorption of mechanical strain during thermal cycling. EX2018 [Ricketts Decl.], ¶113. Lin-191 describes those layers structurally and by material and thickness, and does not attribute the asserted advantages to them. EX1005 [Lin-191], [0389]-[0400]; EX2018 [Ricketts Decl.], ¶113.

The asserted motivation to combine also presupposes a bump structure in Sundaram to be modified. The Petition describes the combination as “modify[ing] Sundaram’s bump per Lin-191’s layered bump teachings.” Pet., 26. As discussed above, Sundaram does not describe the construction of any bump on electronic device 125. EX2018 [Ricketts Decl.], ¶114. A POSITA could not modify a structure that the reference does not describe, and the Petition does not explain what would be modified. *Id.*

A POSITA would not be motivated to combine Sundaram and Lin-191. EX2018 [Ricketts Decl.], ¶115. The Petition has not shown that a POSITA would have looked to Lin-191’s adhesion-layer/seed-layer/electroplated-layer bump structure to modify the bump on Sundaram die pad 135. *Id.* A POSITA would have known that an adhesion or diffusion-barrier layer, such as the titanium or nickel adhesion layer 711 that Lin-191 describes, is needed only in particular circumstances: where copper would otherwise diffuse into an adjacent, dissimilar metal; where copper would otherwise diffuse into an oxide or other inorganic

dielectric; or where copper does not otherwise bond adequately to the material beneath it. *Id.* The Petition does not show that any of these circumstances exists in Sundaram. *Id.*

The Petition's description of this combination confirms that Sundaram's bump is copper. EX2018 [Ricketts Decl.], ¶116. The Petition states that Lin-191's bumps 710, "like Sundaram's copper bumps, are metal interconnect[s]." Pet., 25; EX1003 [Shanfield Decl.], ¶186. The Petition's stated motivation for adding Lin-191's layered structure is that it would provide "improved metallurgical bonding and increased resistance to fatigue and stress-induced failure," would "reduce the risk of intermetallic formation at critical interfaces," and would "mitigate electromigration" and "better absorb mechanical strain during thermal cycling." Pet., 26; EX1003 [Shanfield Decl.], ¶¶188-191. This rationale does not identify any specific diffusion, oxide, or adhesion problem with Sundaram's own copper bump on die pad 135 that Lin-191's layers would remedy. EX2018 [Ricketts Decl.], ¶116.

Sundaram indicates that no such problem exists at die pad 135. EX2018 [Ricketts Decl.], ¶117. Sundaram states that the through vias forming die pad 135 "can be metalized with a highly-conductive metal, for example copper," and "can also be metalized with a polymer liner or a metal seeding liner." EX1004 [Sundaram], 6:22-29. Sundaram identifies these as its metallization options for die

pad 135 and the vias beneath it, and none of them includes a separate adhesion or diffusion-barrier metal layer such as titanium or nickel. EX2018 [Ricketts Decl.], ¶117.

Sundaram elsewhere confirms that it recognizes when such a barrier layer is needed, and that die pad 135 is not an instance of it. EX2018 [Ricketts Decl.], ¶118. In describing an alternative single-crystal-silicon-interposer embodiment, Sundaram describes forming “about 30 nanometer (nm) Ti (barrier for Cu diffusion into SiO₂) and about 1 μm thick copper seed layer” on a silicon wafer coated with a “SiO₂ dielectric isolation layer.” EX1004 [Sundaram], 14:58-66. Sundaram states that this titanium layer is a “barrier for Cu diffusion into SiO₂” — that is, a layer used specifically to prevent copper from diffusing into an inorganic oxide dielectric. *Id.* Sundaram further states that its “novel polymer liner approach is presented to replace the current combination of SiO₂ and diffusion barriers used in the processing of CMOS-based silicon interposers.” *Id.*, 13:5-7 This confirms that Sundaram ties the need for a titanium diffusion barrier to a specific combination — copper deposited on an SiO₂ dielectric in a silicon interposer — and presents its own polymer-based approach as an alternative that avoids that combination. EX1004 [Sundaram], 14:58-66; EX2018 [Ricketts Decl.], ¶118.

Thus, die pad 135 is part of interposer 105, Sundaram’s glass-and-polymer interposer, not the alternative single-crystal silicon interposer in which Sundaram

describes using a titanium barrier against SiO₂. EX1004 [Sundaram], 14:58-66; EX2018 [Ricketts Decl.], ¶119. The Petition has not shown that copper at die pad 135 would diffuse into an adjacent dissimilar metal, would diffuse into an oxide or other inorganic dielectric, or would not otherwise bond adequately to the material beneath it. EX2018 [Ricketts Decl.], ¶119. Absent such a showing, a POSITA would not have understood Lin-191's adhesion-layer teaching to apply to die pad 135's bump, and the Petition's generic reliability rationale does not establish that a POSITA would have been motivated to add it.

4. Sundaram Does Not Teach or Suggest a Polymer Interposer Having the Claimed Thickness

Independent claims 1 and 16 of the '768 patent recite a "first polymer layer" having "a thickness between 100 and 300 micrometers." EX1001 ('768 Patent), cls. 1(a)(ii), 16(a)(ii). Sundaram provides a POSITA with no basis to select a polymer interposer having a thickness between 100 and 300 micrometers.

Sundaram describes the thickness of interposer 105 without reference to any material. Sundaram states that interposer 105 "is ultra-thin and is less than about 100 micrometers in thickness," that "[i]n exemplary embodiments, the interposer 105 is less than about 800 micrometers in thickness, and more specifically about 20-100 micrometers in thickness," and that "[i]n preferred embodiments, the interposer is about 30 micrometers in thickness." EX1004 [Sundaram], 5:48-54.

Only afterward does Sundaram identify candidate materials, stating that interposer 105 “can be made of many substrate materials, for example, glass, silicon, ceramic, polymer-glass laminates, and flexible polymers.” *Id.*, 5:54-58; EX2018 [Ricketts Decl.], ¶121. Thus, Sundaram does not tie any of these thickness values to a polymer interposer, and the sole material Sundaram identifies as preferred, and the only one to which it attributes the advantages it seeks, is glass. *Id.*, 5:58-67; EX2018 [Ricketts Decl.], ¶121. The thicknesses listed at Sundaram 14:34-36 appear under the heading “Single Crystal Silicon Interposer Examples.” The passages describes a *single crystal silicon* interposer, not a polymer interposer. EX1004 [Sundaram], 14:6-10; EX2018 [Ricketts Decl.], ¶121.

Nothing in Sundaram discloses an interposer comprising a “polymer layer [having] a thickness between 100 and 300 micrometers” as required by claims 1 and 16. Therefore, Sundaram does not teach or suggest a polymer interposer having the thickness range recited in challenged claims 1 and 16.

5. The Petition’s Rationale For Combining Sundaram, and Haba For Limitation 1(a)(iii) Fails

Independent claims 1 of the ’768 patent recite a “first polymer layer” having “a coefficient of expansion between 3 and 10 ppm/°C.” EX1001 [’768 Patent],

1(a)(iii). Dependent claim 20 contains the same limitation² The Petition relies on Haba (EX1009) alone for this limitation because Haba discloses a polymer having a CTE of “in the range of 8 parts per million per degree Celsius.” Pet., 7, 58; EX1009 [Haba], 5:55-59.

The Petition’s inclusion of Haba is hindsight. The Petition’s motivation to combine Haba’s polymer with Sundaram is that “a POSITA would have found it advantageous to modify Sundaram’s interposer 105 to have a low CTE to likewise reduce the difference in CTE between interposer 105 and Sundaram’s electronic devices (chips) 125, 130.” Pet., 7-8. But Sundaram already discloses interposers (namely, glass) having CTEs in between the claimed 3 and 10 ppm/°C:

TABLE 1

	Young’s Modulus (GPa)	Poisson’s Ratio	CTE (ppm/° C.)	Stress free Temp. (° C.)
Glass 1	77	0.22	3.8	25
Glass 2	71	0.24	8.5	25
Polymer 1	1.83	0.3	67	232
Polymer 2	6.9	0.3	31	120
Copper	121	0.3	17.3	25

EX1004 [Sundaram], 8:61-62 (showing CTEs for glass of 3.8 and 8.5 ppm/°C);

² While independent claim 16 does not include the CTE limitation, claim 20 depends from claim 16 and recites “said first polymer layer has a coefficient of expansion between 3 and 10 ppm/°C.”

EX2018 [Ricketts Decl.], ¶¶124-125.

The Petition relies on Sundaram's teaching that a "silicon-matched" coefficient of thermal expansion is advantageous for an interposer. Pet., 8 (citing EX1004 [Sundaram], 2:4-6). Sundaram makes that statement about glass, not polymers. EX2018 [Ricketts Decl.], ¶¶126-127. Sundaram states that "[g]lass presents several advantages, namely, silicon-matched coefficient of thermal expansions (CTE), excellent surface flatness, dimensional stability, high electrical resistivity, and thin and large panel availability." EX1004 [Sundaram], 5:62-67. Sundaram does not attribute a silicon-matched coefficient of thermal expansion to any polymer. EX2018 [Ricketts Decl.], ¶126.

The polymers Sundaram itself discloses do not have coefficients of expansion within the claimed range. EX2018 [Ricketts Decl.], ¶127. The materials table in Sundaram reports coefficients of thermal expansion for two polymers substantially above the claimed range of 3 to 10 ppm/°C, while the two glasses reported are within it:

TABLE 1

	Young's Modulus (GPa)	Poisson's Ratio	CTE (ppm/° C.)	Stress free Temp. (° C.)
Glass 1	77	0.22	3.8	25
Glass 2	71	0.24	8.5	25
Polymer 1	1.83	0.3	67	232
Polymer 2	6.9	0.3	31	120
Copper	121	0.3	17.3	25

EX1004 [Sundaram], 8:58-65; *See also id.*, 12:5-12 (Sundaram Table 3 showing CTE of 31 for polymer).

Thus, a POSITA following Sundaram's teaching that a silicon-matched coefficient of expansion is advantageous would select one of the materials Sundaram identifies as having that property (such as glass), and Sundaram identifies none of its polymers as having it. EX2018 [Ricketts Decl.], ¶127.

The Petition relies on Haba's dielectric layer 20 as "a polymeric dielectric" having a coefficient of thermal expansion "in the range of 8 parts per million per degree Celsius." Pet., 7 (citing EX1009 [Haba], 5:41-44, 5:55-59). But Haba's dielectric layer 20 is not an ordinary polymer. EX2018 [Ricketts Decl.], ¶128. Haba describes it as a material selected for low thermal expansion and identifies candidates including "low temperature co-fired ceramic, liquid crystal polymer, glass, and high filler-content epoxy." EX1009 [Haba], cl. 5. Achieving a coefficient of expansion of 8 ppm/°C or lower in a polymer requires a specifically engineered

material, such as a liquid crystal polymer or a highly filled epoxy, and is not a property of polymers generally. EX2018 [Ricketts Decl.], ¶128.

The Petition therefore does not propose using a material that Sundaram discloses. It proposes replacing the interposer material of Sundaram's preferred embodiment with a different, specifically engineered polymer drawn from Haba. But the Petition does not explain why a POSITA seeking a silicon-matched coefficient of expansion would take that path rather than use one of the glasses that Sundaram identifies as already having that property. EX2018 [Ricketts Decl.], ¶129.

Petitioners argue that "Haba expressly motivates the combination, teaching 'the difference in the CTE between the interconnection component and...the microelectronic element 66 can be reduced to a more manageable quantity,' enables 'reductions in solder bump sizes...to achieve finer pitch.'" Pet., 7. But, as explained above, a POSITA reading Sundaram would choose Sundaram's glass material for the interposer since those glass interposers have a CTE of between 3.8 and 8.5 ppm/°C, which matches silicon, while the CTEs of the polymers disclosed in Sundaram are much higher in the range of 31-67 ppm/°C. The Petition provides no rationale for using lower CTE polymers that are not disclosed in Sundaram, especially given that the preferred glass interposers in Sundaram already have "silicon-matched" CTEs.

Moreover, the modification the Petition proposes would not accomplish the purpose the Petition gives for it. Replacing Sundaram's preferred glass interposer with Haba's polymer would increase, rather than decrease, the difference in CTE between the silicon devices in Sundaram and Sundaram's glass interposer because Sundaram's glass CTE of 3.8 ppm/°C is closer to the CTE of silicon than the polymer disclosed in Haba. EX2018 [Ricketts Decl.], ¶¶130-146. Accordingly, the Petition's rationale for combining Sundaram and Haba for limitation 1(a)(iii) fails.

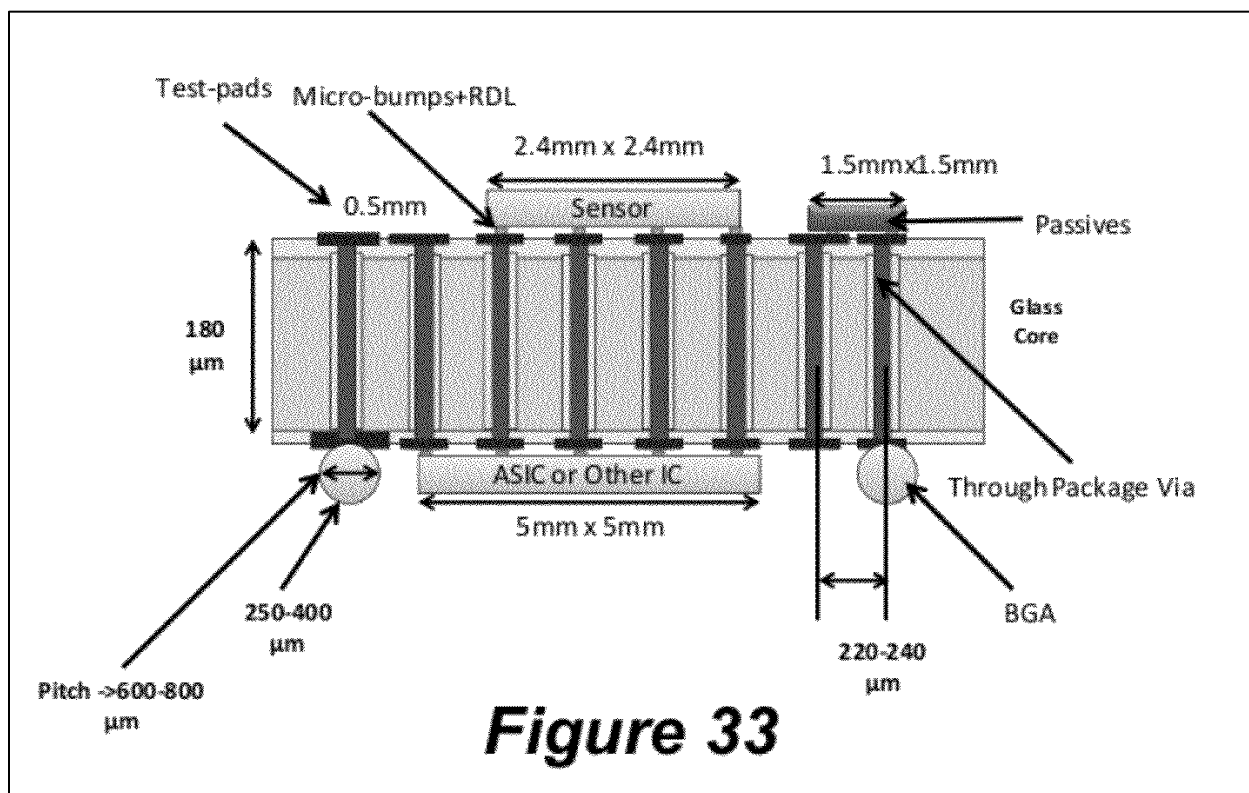
**6. Sundaram Does Not Support the Petition's
Motivation to Combine for Claims 2 and 22**

Claim 2 requires "a passive component over said first interconnection scheme and connected to said first interconnection scheme through a solder layer." EX1001 ['768 Patent], cl. 2. Claim 22 similarly requires "a passive component over said first surface." *Id.*, cl. 22. The Petition relies on Sundaram's figure 33 for the proposition that a passive component can be connected to an interposer's redistribution layer through a solder-based connection, and then proposes relocating that passive component into Sundaram's figure 3 embodiment relied on for the remaining limitations of claim 1. Pet., 28-30, 70 (referring back to claim 2); EX1003 [Shanfield Decl.], ¶¶197-199, 297.

The Petition states that "[b]ased on FIG. 33's embodiment, a POSITA would have found obvious and been motivated to include a *passive component over* and

connected to Sundaram first interconnection scheme through a solder layer, e.g., adjacent to FIG. 3's electronic device 130." Pet., 29-30; EX1003 [Shanfield Decl.], ¶¶199-200.

Sundaram's figure 33 does not support that placement. EX2018 [Ricketts Decl.], ¶¶147-149. Figure 33 depicts a glass core with an image sensor chip and associated test-pads and micro-bumps-and-RDL structure on one side, and an "ASIC or Other IC" on the opposite side, with BGA solder balls formed beneath the ASIC for connection to the next-level board:



EX1004 [Sundaram], Fig. 33; 6:42-45 (describing "an image sensor chip on one side and an Asic chip on the other side of the interposer, as illustrated in FIG. 33").

The convention the Petition applies is that “over” refers to the direction toward the printed wiring board (“PWB”) and “under” refers to the direction away from the PWB. Pet., 11; EX1003 [Shanfield Decl.], ¶150; EX2018 [Ricketts Decl.], ¶¶149-150. Because the BGA solder balls that connect to the PWB are formed on the ASIC side of figure 33, a POSITA would understand the ASIC side of figure 33 to be the “over” side and the sensor side to be the “under” side—consistent with the Petition’s mapping elsewhere of the analogous ASIC-type device (device 130) and sensor-type device (device 125) in the figure 3 embodiment:

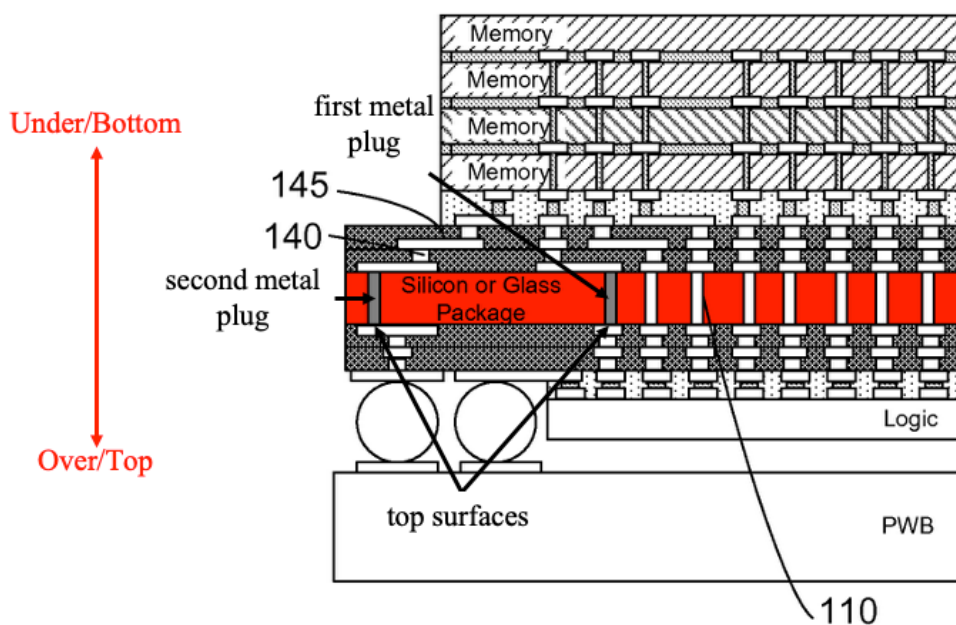
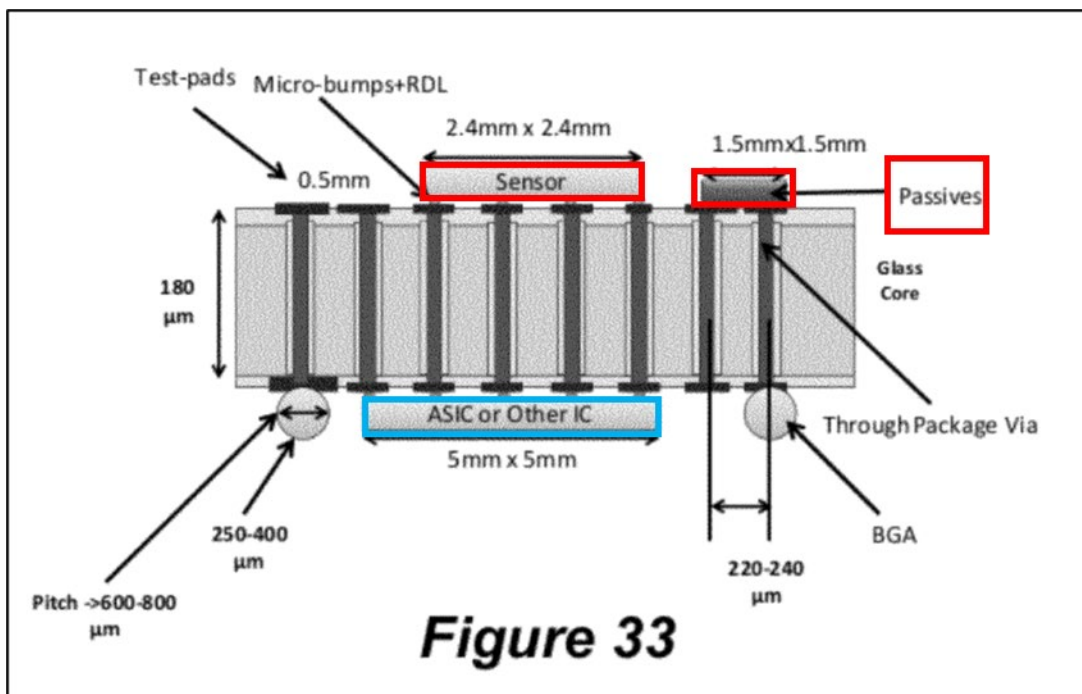


Fig.

Pet., 11 (annotating and excerpting EX1004 [Sundaram], Fig. 3). *See also* EX1004 [Sundaram], 6:37-45 (device 125 as an image sensor chip, device 130 as the

logic/ASIC device); EX2018 [Ricketts Decl.], ¶149.

FIG. 33, however, shows the “Passives” element positioned on the sensor side of the structure — immediately adjacent to the “Sensor” and its micro-bumps-and-RDL connection — not on the ASIC/BGA side:



EX1004 [Sundaram], Fig. 33. Thus, Sundaram’s own drawing places its passive component on the “under” side of the structure, i.e., the side away from the PWB, and not “over” the interconnection scheme that connects to the PWB. EX2018 [Ricketts Decl.], ¶150.

This is the opposite of where the Petition proposes to place the corresponding element in the figure 3 combination. EX2018 [Ricketts Decl.], ¶151. The Petition places its combined passive component “adjacent to FIG. 3’s

electronic device 130,” which Dr. Shanfield elsewhere maps to the ASIC-type, PWB-facing side of the figure 3 structure. Pet., 29-30; EX1003 [Shanfield Decl.], ¶199; see also Pet., 33; *id.*, ¶207 (mapping device 130 as the second semiconductor chip over the first interconnection scheme, i.e., on the PWB-facing side of the structure). Thus, the Petition thus takes the general teaching of figure 33—that a passive component can be soldered to an RDL — but relocates that passive component to the side of the structure opposite to where Sundaram actually discloses it, without identifying any disclosure in Sundaram that supports placing a passive component on the device-130/over side rather than the device-125/under side depicted in figure 33. EX2018 [Ricketts Decl.], ¶151.

A POSITA reading Sundaram figure 33 would understand Sundaram’s own teaching to place the passive component on the side of the package furthest from the board-level connection—for example, to keep the board-side footprint clear for the BGA array, or to position the passive nearer the sensor and its associated fine-pitch redistribution circuitry. EX2018 [Ricketts Decl.], ¶152. The Petition provides no reasoning for why a POSITA would instead have placed the passive component on the opposite, PWB-facing side of the package as the Petition proposes. *Id.* Because the Petition’s sole evidentiary basis for the claimed placement is figure 33, and figure 33 shows the passive component on the side opposite to where the Petition places it, the Petition has not shown that a POSITA would have been

motivated to place a passive component “over said first interconnection scheme” as claim 2 requires, nor has it shown a reasonable expectation of success in doing so.

Id.

Thus, the Petition fails to prove by a preponderance of the evidence that claim 2, or claim 22, is unpatentable in grounds 1A and 1C.

7. Sundaram, Haba, and Lin-191 Fail to Teach Or Suggest Claim 5

Claim 5 requires “a first semiconductor chip compris[ing] a central-processing-unit (CPU) circuit block and a graphics-processing-unit (GPU) circuit block.” EX1001 [’768 Patent], cl. 5. Sundaram does not disclose a central-processing-unit circuit block or a graphics-processing-unit circuit block, and Petitioners therefore rely exclusively on Lin-191. Pet., 35.

The Petition states that although “Sundaram’s FIG. 3 depicts device 125 as stacked memory, Sundaram teaches device 125 can be ‘other electronic devices,’” and that Sundaram discloses “‘mobile phone applications, including video streaming, 3D graphics, camera-functions, and gaming’ and contemplates ‘high power logic component[s]’” for device 125’s side of interposer 105. Pet., 36 (citing EX1003 [Shanfield Decl.], ¶211).

This rationale is inconsistent with the architecture Sundaram describes. EX2018 [Ricketts Decl.], ¶¶154-156. Sundaram pairs a memory device on one side

of its interposer with a logic device on the other: “the first electronic device 125 can be single or stacked memory IC devices, and the second electronic device 130 can be a logic IC device or devices.” EX1004 [Sundaram], 6:38-89. The purpose of that arrangement is to provide very high bandwidth between a logic device and a memory device across a short, dense interconnect. EX2018 [Ricketts Decl.], ¶156.

Placing a central-processing-unit circuit block and a graphics-processing-unit circuit block on device 125 would place logic circuitry on both sides of the interposer and would remove the memory device that Sundaram’s architecture is designed to serve. EX2018 [Ricketts Decl.], ¶157. Sundaram’s references to mobile phone applications and to high power logic components describe the demands that motivate Sundaram’s logic-to-memory architecture; they do not suggest converting the memory side of that architecture into a second logic device. *Id.* For this reason, and for the reasons discussed above, a POSITA would not have been motivated to combine Lin-191 and Sundaram to arrive at claim 5. *Id.*

8. Sundaram, Haba and Lin-191 Fail To Teach Or Suggest Claim 20

Like Claim 1(a)(iii), Claim 20 requires “[t]he chip package of claim 16, wherein said first polymer layer has a coefficient of expansion between 3 and 10 ppm/°C.” The Petition’s discussion of Ground 1A Claim 20 states only “Sections V.A.5, VI.A.” Pet., 58 Those sections discuss Ground 1A claim 1(a)(iii) and

Ground 1B claim 16. Pet., 7, 59-67. For the reasons discussed above at §V.A.5 for claim 1(a)(iii), *supra*, a POSITA would not have combined Sundaram and Haba in the manner the Petition proposes. EX2018 [Ricketts Decl.], ¶¶158-159.

9. Sundaram and Lin-191 Do Not Teach or Suggest Claim 25

The Petition’s analysis of Ground 2A claim 25(b) refers back to section V.A.19, without elaboration. §V.A.19 of the Petition discusses Ground 1A limitation 1(f)(ii). Pet., 24-27, 143. Limitation 1(f)(ii) is substantively similar to claim 25. EX1001 [’768 Patent], cls. 1(f)(ii), 25; Accordingly, claim 25 fails for the same reasons as limitation 1(f)(ii). *Supra*, §V.A.2; EX2018 [Ricketts Decl.], ¶¶160-162.

B. Grounds 2A and 2B

Grounds 2A and 2B collectively challenge claims 1-15.

1. The Petition Identifies Two Different Structures as the Same Claimed “Fourth Metal Interconnect”

Claim 1 recites a “fourth metal interconnect” in limitation 1(f)(i), and then refers back to “said fourth metal interconnect” in limitation 1(f)(ii). Limitation 1(f)(i) requires that “said first semiconductor chip comprises a fourth metal interconnect on a first metal pad of said first semiconductor chip.” EX1001 [’768 Patent], cl. 1. Limitation 1(f)(ii) then requires that “said fourth metal interconnect comprises a second metal layer on said first metal pad and a fifth copper layer over

said second metal layer, wherein said fifth copper layer has a thickness between 5 and 30 micrometers.” *Id.* A POSITA would understand that “said fourth metal interconnect” in limitation 1(f)(ii) refers to the same structure recited in limitation 1(f)(i), and that a single structure must therefore satisfy both limitations. EX2018 [Ricketts Decl.], ¶165.

In Ground 2A, the Petition does not identify a single structure that satisfies both limitations. EX2018 [Ricketts Decl.], ¶166. For limitation 1(f)(i), the Petition states that Haba’s “solder ball 32 is a fourth metal interconnect that is on a first pad of microelectronic element 66 (first semiconductor chip).” Pet., 92-93; (citing EX1009 [Haba], 7:45-48, Fig. 3) (emphasis removed). For limitation 1(f)(ii), the Petition states that “Lin-191 teaches or renders obvious interconnects/bumps with layers/thickness as recited in Claim 1(f)(ii),” and cross-references Section V.A.19 of the Petition. Pet., 94. Section V.A.19 relies on the layered structure of Lin-191’s metal pillars or bumps 710 — an adhesion layer 711, a seed layer 712, and a metal layer 713. Pet., 24-25; EX1005 [Lin-191], [0389].

Haba’s solder ball 32 and Lin-191’s metal pillars or bumps 710 are two different structures. EX2018 [Ricketts Decl.], ¶167. Haba’s solder ball 32 is a mass of solder. *Id.*; EX1009 [Haba], 6:42-47. It does not comprise an adhesion layer, and it does not comprise a copper layer having a thickness between 5 and 30 micrometers. EX2018 [Ricketts Decl.], ¶167. Lin-191’s metal pillar or bump 710 is

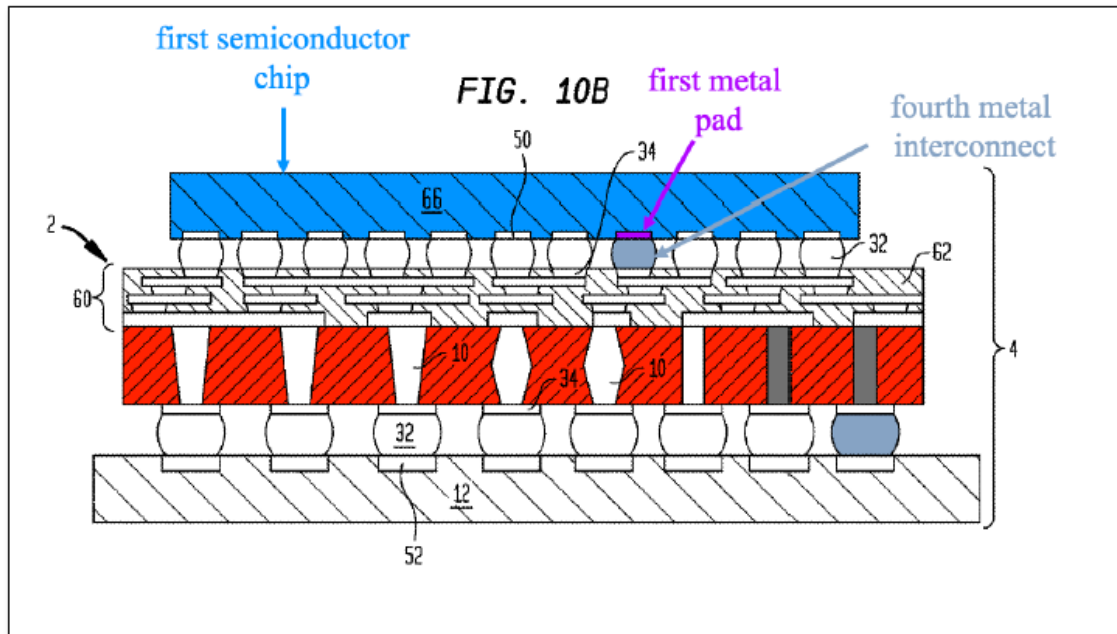
not a solder ball; Lin-191 describes the metal pillars or bumps 710 as bonded to separate solder joints 720. EX1005 [Lin-191], [0389]; EX2018 [Ricketts Decl.], ¶167. Thus, the Petition’s mapping therefore requires “said fourth metal interconnect” to be a solder ball for purposes of limitation 1(f)(i) and a plated copper interconnect for purposes of limitation 1(f)(ii). EX2018 [Ricketts Decl.], ¶167. A POSITA would not understand a single claimed structure to be both. *Id.*

Thus, Ground 2A fails to prove that limitation 1(f)(i) and (1)(f)(ii) are unpatentable.

2. Haba and Lin-191 Do Not Teach Or Suggest Limitation 1(f)(i)

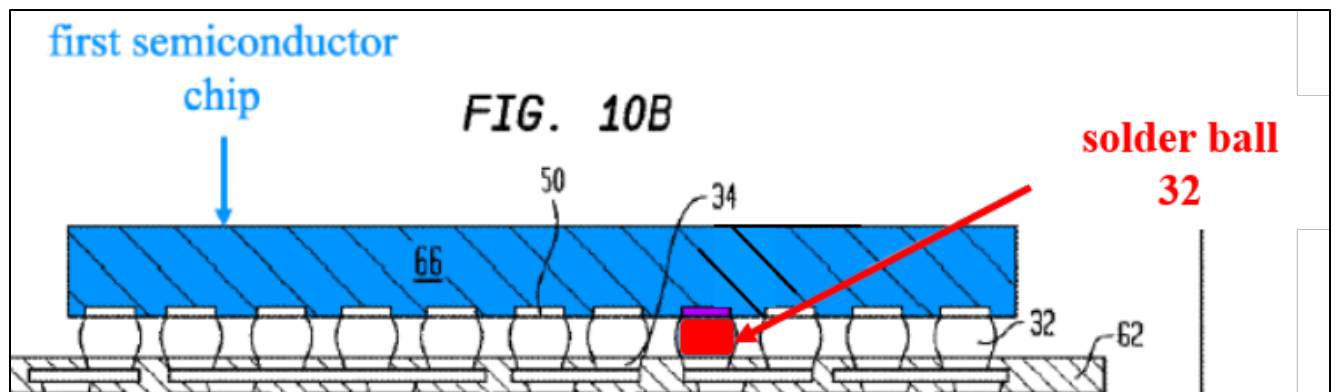
a) Haba does not teach or suggest this limitation because Haba’s microelectronic element 66 does not comprise Haba’s solder ball 32

Limitation 1(f)(i) requires that the “first semiconductor chip comprises a fourth metal interconnect.” EX1001 [’768 Patent], cl. 1. As shown below, the Petition alleges Haba’s microelectronic element 66 is the claimed “first semiconductor chip” and Haba’s solder ball 32 is the claimed “fourth metal interconnect”:



Pet., 92-93 (annotating EX1009 [Haba], Fig. 10B); EX2020 [Shanfield Dep. Tr.], 63:5-64:10.

As is clear from the Petition's annotation of Haba figure 10, and emphasized in the annotation below, Haba's solder ball 32 is not part of microelectronic element 66:



EX1009 [Haba], Fig. 10B (excerpted and annotated); EX2018 [Ricketts Decl.], ¶¶173-174. Instead, it is solder added outside microelectronic element 66³ to attach microelectronic element 66 to interconnection component 2. EX1009 [Haba], 7:52-56 (“end surfaces 10B are used to join posts 10 to solder balls 32, which are, in turn, joined to contacts 50 on a microelectronic element [66].”); EX2018 [Ricketts Decl.], ¶174.

As Haba explains, “[m]icroelectronic assemblies generally include one or more packaged micro-electronic elements such as one or more semiconductor chips mounted on a substrate.” EX1009 [Haba], 1:19-22. Haba consistently treats the microelectronic element, the contacts of that element, and the material used to join the element to another component as separate things. EX2018 [Ricketts Decl.], ¶175.

Haba’s own claims reflect that separation. EX2018 [Ricketts Decl.], ¶176. Claim 2 recites a microelectronic assembly in which “the element contacts are joined with the first wettable contacts through masses of conductive bonding material.” EX1009 [Haba], cl. 2. Claim 21 similarly recites an assembly in which

³ Haba’s specification and original figures discuss microelectronic element 6, not 66. However, a January 2, 2018 certificate of correction changed “6” to “66”.

EX1009 [Haba], p. 17.

“at least some of the element contacts of the microelectronic element are joined to the first wettable contacts of the interconnection component through conductive masses.” *Id.*, cl. 21. Thus, a POSITA would understand from these recitations that Haba treats the microelectronic element and its element contacts as one structure, and the conductive bonding masses that join that element to the interconnection component as a separate structure. EX2018 [Ricketts Decl.], ¶176.

Haba also describes solder ball 32 as an interchangeable bonding material rather than a structure of the microelectronic element. Haba states that “[o]ther materials can be used in place of solder balls 32 to join features of the components of the assembly such as tin indium or a conductive matrix.” EX1009 [Haba], 6:44-47. A POSITA would not understand a bonding material that may be replaced by “a conductive matrix” to be a part of the semiconductor chip being bonded. EX2018 [Ricketts Decl.], ¶177.

For these reasons, Haba’s microelectronic element 66 does not “comprise” solder ball 32. MPEP § 2111.03 (“The transitional term ‘comprising,’ which is synonymous with ‘including,’ ‘containing,’ or ‘characterized by,’ ...”). Solder ball 32 is a separate component from microelectronic element 66, and microelectronic element 66 does not include or contain, and is not characterized by, solder ball 32. EX2018 [Ricketts Decl.], ¶¶178-179.

Accordingly, the Petition's combination of Haba and Lin-191 fails because it does not teach or suggest the "first semiconductor chip comprises a fourth metal interconnect."

b) Lin-191 does not teach or suggest this limitation

Petitioners do not allege that Lin-191 teaches or suggests the claimed "first semiconductor chip comprises a fourth metal interconnect." Pet., 21-23; EX1001 [’768 Patent], cl. 1(f)(i). Although Petitioners includes two sentences on Lin-191 for Ground 2A limitation 1(f)(1), those sentences are directed to the claimed "metal pad," not the claimed "fourth metal interconnect." Pet., 93. The Petition's analysis states "Section V.A.18," possibly intending to refer back to §V.A.18 of the Petition for support. *Id.* But section V.A.18's discussion of Lin-191 only refers to the "metal pad" limitation, stating that "Lin-191 teaches a semiconductor chip 160 with 'metal traces or pads 163' that include 'aluminum.'" Pet., 23; EX2018 [Ricketts Decl.], ¶180. It does not allege Lin-191 teaches or suggests the "first semiconductor chip comprises a fourth metal interconnect." *Id.* Thus, Lin-191 does not remedy the deficiency in Haba.

c) The Petition Provides No Rationale for Combining Haba with Lin-191

"[T]here must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." *KSR Int'l Co. v.*

Teleflex Inc., 550 U.S. 398, 418 (2007) (quoting *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006)). Obviousness “cannot be sustained by mere conclusory statements.” *Id.* “The mere fact that these possible arrangements existed in the prior art does not provide a reason [for combining two references] ... [a] reason for combining must exist.” *Virtek Vision Int'l ULC v. Assembly Guidance Sys.*, 97 F.4th 882, 887-888 (Fed. Cir. 2024) (reversing PTAB finding of obviousness because only conclusory rationales for combining were provided).

The Petition’s rationale for combining Lin-191 with Haba for limitation 1(f)(i) (below) must be rejected because it is conclusory and lacks any articulated reasoning or rational underpinning:

a) Lin-191’s “Metal Pad” Teachings and MTC

Section V.A.18. The Haba-Lin-191 combination an implementation detail in Haba’s chip package as Lin-191 provides the specificity of a metal contact pad to the extent that PO argues not provided by Haba. *EX1003*, ¶376. The same MTC and REOS for Sundaram-Lin-191 apply for Haba-Lin-191. Section V.A.18.b.

Pet., 93. The first and last sentence (“Section V.A.18” and “Section V.A.18.b”) possibly intend to refer back to those sections of the Petition for support. *See* Pet., 26. While Section V.A.18.b discusses why a POSITA would allegedly combine *Sundaram* and Lin-191, Section V.A.18.b ***does not mention Haba, let alone why a POSITA would allegedly combine Haba and Lin-191.*** EX2018 [Ricketts Decl.],

¶181. Thus, it cannot serve as articulated reasoning or a rational underpinning for why a POSITA would allegedly combine Haba and Lin-191.

The second sentence states “[t]he Haba-Lin-191 combination an implementation detail in Haba’s chip package as Lin-191 provides the specificity of a metal contact pad to the extent that PO argues not provided by Haba.” Pet., 93. But this sentence does not make grammatical sense. To the extent a meaning can be discerned, it appears to imply that the rationale for adding Lin-191’s contact 50 to Haba is because the claimed metal pad is “not provided by Haba.” *Id.*; EX2018 [Ricketts Decl.], ¶182. This is the definition of hindsight. It provides no rationale for why a POSITA would be motivated to combine Lin-191’s contact 50 with Haba. *Virtek*, 97 F.4th at 887-888.

The third sentence states “[t]he same MTC and REOS for Sundaram-Lin-191 apply for Haba-Lin-191.” *Id.* Again, this conclusory statement refers to the Petition’s rationale for combining Sundaram and Lin-191, which makes no mention of Haba. EX2018 [Ricketts Decl.], ¶183.

The Petition cites paragraph 376 of Dr. Shanfield’s declaration in support. Pet., 93. That paragraph similarly refers back to Dr. Shanfield’s motivation to combine ***Sundaram*** and Lin-191, stating “[f]or the same MTCs and with the same reasonable expectation of success, a POSITA would have found it obvious and been motivated to implement, per Lin-191, Haba’s contact 50 (*first...pad*) as *metal*,

yielding a *first metal pad*.” EX1003 [Shanfield Decl.], ¶376. But neither paragraph 376 nor Dr. Shanfield’s analysis of the motivation to combine Sundaram and Lin-191 contains any analysis of why a POSITA would allegedly be motivated to combine **Haba** and Lin-191. EX2018 [Ricketts Decl.], ¶184. Because the Petition’s motivation to combine Haba and Lin-191 consists entirely of conclusory statements lacking any articulated reasoning with rational underpinnings to support a conclusion of obviousness, the Petition’s rationale for combining Haba and Lin-191 fails.

3. Haba and Lin-191 Do Not Teach Or Suggest Limitation 1(f)(ii)

a) Lin-191 does not teach or suggest “said fourth metal interconnect.”

The Petition relies solely on Lin-191 for limitation 1(f)(ii). Pet., 94. The entirety of the Petition’s explanation is that “Lin-191 teaches or renders obvious interconnects/bumps with layers/thickness as recited in Claim 1(f)(ii),” citing Section V.A.19 of the Petition. *Id.*

The Petition’s reliance on Lin-191 for limitation 1(f)(ii) does not cure the deficiency discussed above for 1(f)(i). EX2018 [Ricketts Decl.], ¶¶186-187. The structure the Petition identifies as the claimed “fourth metal interconnect” for limitation 1(f)(i) is Haba’s solder ball 32, and the structure on which it relies for limitation 1(f)(ii) is Lin-191’s metal pillar or bump 710. The Petition therefore

does not identify any single structure that is both the “fourth metal interconnect” of limitation 1(f)(i) and “said fourth metal interconnect” of limitation 1(f)(ii).

Because neither Haba nor Lin-191 teach or suggest limitation 1(f)(ii), the Petition fails to prove by a preponderance of the evidence that claim 1 (or the claims depending therefrom) are unpatentable.

4. Lin-191 does not teach “a second metal layer on said first metal pad” or a fifth copper layer of the claimed thickness

For the reasons discussed above in connection with Ground 1A (*supra*, §V.A.2.b), the Petition does not show “a second metal layer on said first metal pad” as required by limitation 1(f)(ii). EX2018 [Ricketts Decl.], ¶188.

The Petition also does not identify a “fifth copper layer over said second metal layer” because it does not identify a “second metal layer” in Lin-191” for the reasons discussed above. *Supra*, §V.A.2.b; EX1005 [Lin-191], [0396]; EX2018 [Ricketts Decl.], ¶189. Because neither Haba nor Lin-191 teaches or suggests limitation 1(f)(ii), the Petition fails to prove by a preponderance of the evidence that claim 1, or the claims depending therefrom, are unpatentable.

5. Haba and Lin-191 Do Not Teach or Suggest Claim 2’s “Passive Component ... Over Said First Interconnection Scheme”

Claim 2 requires “a passive component over said first interconnection scheme and connected to said first interconnection scheme through a solder layer.”

EX1001 ['768 Patent], cl. 2. For Ground 2A, the Petition relies on two different figures of Lin-191 for this limitation: figure 55, for the teaching that a chip can be replaced with a passive component connected through solder joints, and figure 84, for the position of that substitution relative to Haba's structure. Pet., 96-98; EX1003 [Shanfield Decl.], ¶¶382-386. The Petition states that connecting a passive component "over RDL 70 would advantageously mitigate signal desynchronization and preserve signal integrity," Pet., 98; *see also* EX1003 [Shanfield Decl.], ¶386.

Lin-191 does not support this mapping, for at least three reasons. EX2018 [Ricketts Decl.], ¶¶191-198. First, figure 55 is expressly tied to a different embodiment than figure 84. Lin-191 states that "FIG. 55 demonstrates another system-in package or multichip module according to another embodiment of the present disclosure. In this embodiment, one of the chips 140 in the system-in package or multichip module illustrated in FIG. 52 can be replaced by a passive component 67...." Further, "[t]he passive component 67 can be connected to the metal layer 53 of the patterned metal layer 5 through two solder joints 68." Pet., 96; EX1005 [Lin-191], [0340]. Thus, Lin-191 itself identifies the embodiment to which figure 55's substitution teaching applies—the figure 52 embodiment. *Id.* The Petition's reliance on Lin-191's general statement that "the same numeral appears in different drawings" to import figure 55's teaching into the separate figure 84 embodiment (EX1003 [Shanfield Decl.], ¶382 n.5) does not override Lin-191's

own express statement that the figure 55 substitution belongs to the figure 52 embodiment. EX2018 [Ricketts Decl.], ¶192.

Second, even if a POSITA imported figure 55's substitution concept into figure 84, the chip 140 that Lin-191 describes in the figure 84 embodiment does not connect to patterned metal layer 5 the way figure 52/55's chip 140 does. Lin-191 states that "[t]hrough one or more metal pillars or bumps 64, each of the chips 140 can be connected to... the patterned metal layer 7," and that "[e]ach of the chips 140 has one of the metal traces or pads 66 connected to one or more of the metal traces or pads 46 in one or more of the chips 130 through, in sequence, the patterned metal layer 6, one of the metal pillars or bumps 64, the patterned metal layer 7... one or more of the metal pillars or bumps 54, the patterned metal layer 5, one or more of the metal pillars or bumps 44, and the patterned metal layer 4." Pet., 97; EX1005 [Lin-191], [0273]. This passage demonstrates that the chips 140 relevant to the figure 84 family connect directly to patterned metal layer 7 through metal pillars or bumps 64, and that patterned metal layer 5 is a separate, more remote layer reached only after passing through metal layer 7 and additional metal pillars or bumps 54. EX2018 [Ricketts Decl.], ¶193. Thus, a component occupying chip 140's position in this embodiment would connect to layer 7, not layer 5. *Id.*

This sequence also defeats the Petition's "over" mapping. EX2018 [Ricketts Decl.], ¶¶194, 196. The Petition applies a convention under which "over" refers to

the direction toward the printed circuit board and “under” refers to the direction away from it. Pet., 97; EX1003 [Shanfield Decl.], ¶383. Because patterned metal layer 5 lies further along the conductive path toward the package’s lower metal layers and, ultimately, its board-level connections than patterned metal layer 7 and the chips 140 that connect to it, a POSITA would understand a component in chip 140’s position to be on the chip side of patterned metal layer 5, not on the side of patterned metal layer 5 that faces the circuit board. EX2018 [Ricketts Decl.], ¶194. Thus, the Petition has not shown that a passive component substituted for chip 140 in the figure 84 embodiment would be “over” patterned metal layer 5. EX2018 [Ricketts Decl.], ¶194.

Third, and independently, neither figure 55, nor figure 84, nor any other portion of Lin-191 that the Petition cites, teaches, or suggests replacing a solder ball with a passive component. EX2018 [Ricketts Decl.], ¶197. Lin-191’s actual teaching is a substitution of a chip for a passive component at a chip-attach location — the figure 52/55 embodiment replaces chip 140, which Lin-191 elsewhere describes as having “first and second terminals” landing on discrete contact points of an interconnection scheme, with passive component 67, which likewise has “first and second terminals” landing on the same type of contact points. EX1005 [Lin-191], [0340]-[0341]. This is a substitution of one two-

terminal device for another two-terminal device at the same type of attachment location. EX2018 [Ricketts Decl.], ¶197.

The Petition's proposed modification of Haba is a different substitution. EX2018 [Ricketts Decl.], ¶198. As discussed above, the Petition states only that connecting a passive component over RDL 70 would preserve signal integrity. Pet., 98. Haba's solder balls 32 are individual, single-node connectors that each carry a dedicated electrical path from one of Haba's pads 34 to a corresponding one of PCB 12's contacts 52. EX1009 [Haba], 7:54-56. Removing one of those individual connectors and replacing it with a two-terminal passive component is not the same kind of substitution as replacing an entire chip, with its own independent set of terminals and conductive paths, with a passive component having a comparable set of terminals. EX2018 [Ricketts Decl.], ¶198. Lin-191 does not teach, suggest, or provide any reasoning that would have led a POSITA to remove one of an array of single-node board-level solder balls and replace it with a two-terminal passive component. *Id.* A POSITA would not have found it obvious to do so, and the Petition identifies no motivation, teaching, or suggestion — in Lin-191 or otherwise — for that specific substitution, nor does it explain how a two-terminal passive component would be expected to function in place of a single-node solder ball, or where the passive component's second terminal would connect. *Id.*

Thus, the Petition has not shown that Haba and Lin-191 in Ground 2A teach or suggest claim 2.

6. The Petition Fails To Prove Haba and Lin-191 Render Claim 5 Unpatentable

Claim 5 recites “The chip package of claim 1, wherein said first semiconductor chip comprises a central-processing-unit (CPU) circuit block and a graphics-processing-unit (GPU) circuit block.” EX1001 [’786 patent], cl. 1.

Petition Ground 2A states as follows for claim 5:

E. Claim 5

The same MTCs and REOS for modifying Sundaram per Lin-191 apply to Haba-Lin-191, e.g., increasing the functionality of Haba’s *chip package*. Section V.E; EX1003, ¶¶394-395.

Pet., 101. The Petition fails because it does not “specify where each element of the claim is found in the prior art patents or printed publications relied upon.” 37 C.F.R. § 42.104(b)(4). The Petition does not identify whether or to what extent it relies on Haba or Lin-191 as disclosing this limitation. EX2018 [Ricketts Decl.], ¶201. That is, the Petition is unclear what structure in Haba or in Lin-191 the Petition contends corresponds to the central-processing-unit circuit block and the graphics-processing-unit circuit block recited in claim 5, or whether the Petition relies on Haba, on Lin-191, or on both for that limitation. *Id.*

Moreover, the Petition’s motivation to combine and reasonable expectation of success also fail because they refer back to the motivation to combine *Sundaram* and Lin-191 rather than *Haba* and Lin-191. There is no discussion at Section V.E of why a POSITA would be motivated to “increase[e] the functionality of Haba’s chip package.” The Shanfield declaration at paragraphs 394 and 395 merely repeats the conclusory statement from the Petition and adds that “Haba, like Sundaram, contemplates ‘cellular phones[.]’” EX1003 [Shanfield Decl.], ¶395. But it provides no explanation for why this would motivate a POSITA to combine Lin-191 and Haba or why the POSITA would have a reasonable expectation of success in doing so. EX2018 [Ricketts Decl.], ¶¶202-203. Accordingly, the Petition fails to demonstrate that claim 5 is unpatentable over Haba and Lin-191.

7. The Petition Fails to Prove Haba and Lin-191 Render Claim 10 Unpatentable

The Petition also fails to demonstrate how Haba and Lin-191 render claim 10 unpatentable. Claim 10 recites “The chip package of claim 1, wherein said first metal pad is an aluminum pad. The Petition’s entire explanation is below:

I. Claim 10

Section V.J. The same MTCs and REOS apply.

Pet., 105. “Section V.J” is Ground 1A’s analysis of claim 10 for *Sundaram* and Lin-191. The Petition does not explain how *Haba* and Lin-191 allegedly teach or

suggest claim 10, nor what the motivation to combine or reasonable expectation of success are in combining Haba and Lin-191. The Petition's citation to Section V.J refers back to the Petition's discussion of how Sundaram and Lin-191 allegedly teach or suggest claim 10. *Id.*, 48-49. Section V.J makes no mention of Haba, let alone discuss why a POSITA would be motivated to combine Haba and Lin-191, or have a reasonable expectation of success in doing so. *Id.* 37 C.F.R. § 42.104(b)(4); EX2018 [Ricketts Decl.], ¶¶211. Accordingly, the Petition fails to prove that claim 10 is unpatentable over Haba and Lin-191.

C. Grounds 3A-3C

Grounds 3A-3C challenge claims 16-28. Pet., 2.

1. Yu and Lin-191 Do Not Teach Or Suggest a “Second Metal Interconnect”

Claim 16(d)(i) recites that a “first interconnection scheme comprises a first metal interconnect ..., a second metal interconnect ..., wherein said first metal interconnect is connected to said first metal plug.” Ex. 1001, 24:45-54. Thus, the claim requires both a first metal interconnect and a second metal interconnect—that is, the claim requires two separate interconnects. EX2018 [Ricketts Decl.], ¶¶213.

The '768 Patent distinguishes the metal interconnects of an interconnection scheme by the conductive path each provides, and not by vertical position within a

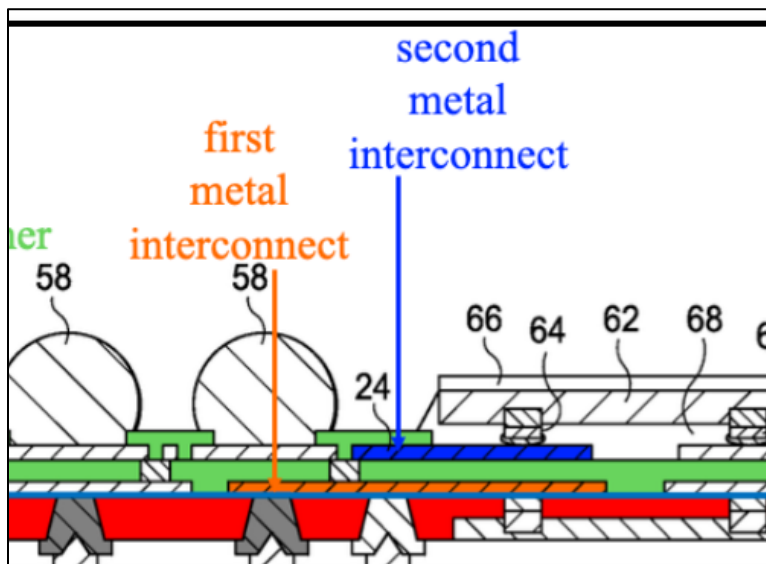
single conductive path. EX2018 [Ricketts Decl.], ¶214. Claim 1 illustrates that usage. Claim 1 recites that “said first metal interconnect is connected to said first metal plug, wherein said second metal interconnect is connected to said second metal plug.” EX1001 [’768 Patent], cl. 1. Thus, a POSITA would understand from that recitation that the first and second metal interconnects of the first interconnection scheme are separate conductive paths, each routing to a different metal plug, rather than two vertically stacked portions of one path. EX2018 [Ricketts Decl.], ¶214. A POSITA would understand the terms “first metal interconnect” and “second metal interconnect” to carry the same meaning in claim 16 as in claim 1, and would understand claim 16 to require two separate conductive paths within the first interconnection scheme. EX2018 [Ricketts Decl.], ¶¶214-218.

The Petition’s mapping is also inconsistent with claim 16(d)(i)’s requirement of “a second polymer layer over said first and second metal interconnects.” EX1001 [’768 Patent], cl. 16. EX2018 [Ricketts Decl.], ¶219. The Petition states that “ILD layers 22, 26 comprise ‘polyimide’ and are, collectively, a second polymer layer over metallization layers 20, 24.” Pet., 127.

ILD layer 22 and ILD layer 26 are two separate layers, not one layer. EX2018 [Ricketts Decl.], ¶220. Yu describes ILD layer 22 as deposited “over the first metallization layer 20”, and describes the second metallization layer 24 and the second ILD layer 26 as formed afterward. EX1010 [Yu], 3:20-32. Thus, ILD

layer 22 lies beneath the second metallization layer 24 and is therefore not over the structure the Petition identifies as the claimed second metal interconnect. EX2018 [Ricketts Decl.], ¶220. Further, a POSITA would not understand two dielectric layers at different levels of a build-up structure, separated by a metallization layer, to be a single polymer layer over both metallization layers. EX2018 [Ricketts Decl.], ¶220.

Instead of identifying a first metal interconnect and a second metal interconnect as the claim requires, the Petition cites different parts of the same interconnect as satisfying both claim limitations. EX2018 [Ricketts Decl.], ¶221. Below is the highlighted and annotated figure from the Petition identifying the alleged first and second metal interconnects:



Pet., 127 (annotating EX1010 [Yu], Fig. 16). The orange layer (Yu's first metallization layer 20) is the alleged "first metal interconnect" and the blue layer

(Yu's second metallization layer 24) is the alleged "second metal interconnect."

But these layers are connected together by the unlabeled and uncolored metal material disposed between the orange and blue layers.⁴ EX2018 [Ricketts Decl.], ¶221. Thus, the orange and blue layers are two portions of a single conductive path through the interconnection scheme, and are not two separate metal interconnects.

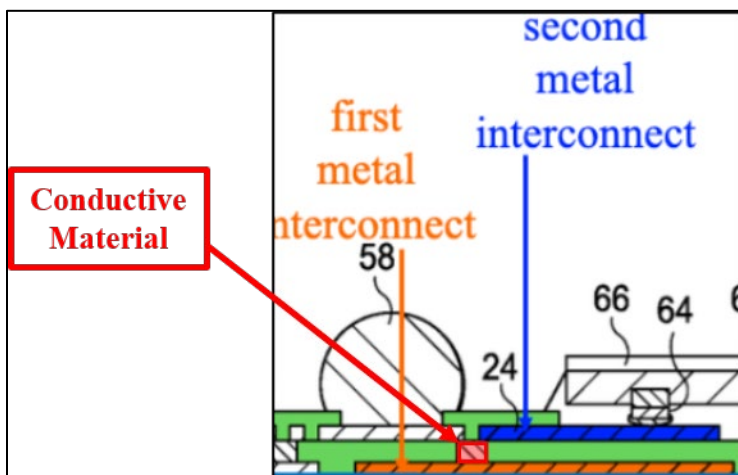
Id.

Yu describes metallization layers 20 and 24 as successive levels of a single redistribution structure on the front side of the package. EX2018 [Ricketts Decl.], ¶221. Yu states that the first front side metallization layer 20 is formed, and that "[a] first ILD layer 22 is deposited on the front side and over the first metallization layer 20." EX1010 [Yu], 3:20-21. Yu then states that "[o]penings may be formed through the first ILD layer 22 to the first metallization layer 20," and that subsequent metallization layers and ILD layers, "such as a second metallization layer 24 and a second ILD layer 26, may be formed using the same or similar processes as discussed with regard to the first metallization layer 20 and the first

⁴ In fact, for dependent claim 27, the Petition relies on the fact that what it identifies as the "first metal interconnect" is directly electrically connected to what it identifies as the "second metal interconnect." Pet., 145-46; EX[Ricketts Decl.], ¶225.

ILD layer 22.” *Id.*, 3:25-32. Yu further states that “[c]onductive material deposited during the formation of a subsequent metallization layer may be deposited in openings of the previously formed ILD layer to electrically couple respective metallization layers.” *Id.*, 3:32-35.

The Petition relies on Yu Fig. 16 for this limitation. Pet., 127. Yu Fig. 16 depicts conductive material occupying the openings in the first ILD layer 22 and joining the first metallization layer 20 to the second metallization layer 24:



Pet., 127 (annotating EX1010 [Yu], Fig. 16):

The conductive material occupying the openings in the first ILD layer 22 joins the first metallization layer 20 and the second metallization layer 24 into a single conductive path. EX2018 [Ricketts Decl.], ¶¶222-223. The Petition identifies the claimed “first metal interconnect” as a portion of metallization layer 20 (highlighted in orange above) and the claimed “second metal interconnect” as a portion of metallization layer 24 (highlighted in blue above. Those two portions are

not separate conductive paths. They are an upper and a lower portion of the same path, and a signal entering one passes directly into the other. EX2018 [Ricketts Decl.], ¶223.

That is not what claim 16 requires. As discussed above, the '768 Patent distinguishes the first and second metal interconnects of an interconnection scheme as separate conductive paths. The Petition has identified a single conductive path in Yu and labeled two portions of it as the claimed “first” and “second” metal interconnects. EX2018 [Ricketts Decl.], ¶224. Thus, the Petitioners does not identify the two metal interconnects that claim 16 requires in Yu.

The Petition’s treatment of dependent claim 27 confirms this. EX2018 [Ricketts Decl.], ¶225. For claim 27, the Petition relies on the fact that what it identifies as the “first metal interconnect” is directly electrically connected to what it identifies as the “second metal interconnect.” Pet., 145-46. This reliance confirms that the two structures the Petition has identified lie on a single conductive path. *Id.*

The conductive material deposited in the openings in the first ILD layer 22 connects the first metallization layer 20 to the second metallization layer 24. When Petitioners identify the claimed “first metal interconnect” as corresponding to the portion of metallization layer 20 (highlighted in orange above) and the claimed “second metal interconnect” as corresponding to the portion of metallization layer

24 (highlighted in blue above), Petitioners are identifying two layers of the same metal interconnect. EX2018 [Ricketts Decl.], ¶226. Thus, Petitioners have failed to identify the claimed “first” and “second” metal interconnects. Petitioners have at best identified *one* metal interconnect.

2. Yu and Lin-191 Do Not Teach or Suggest Limitation 16(d)(iii)

Limitation 16(d)(iii) requires that “said first metal interconnect compris[es] a first metal layer, a third copper layer on said first metal layer, and a fourth copper layer on said third copper layer.” EX1001 [’768 Patent], cl. 16(d)(iii). The Petition relies on Yu’s own description of metallization layer 20: “Metallization layer 20 includes a ‘seed layer, such as copper...deposited on the molding compound 18,’ and a ‘[c]onductive material...such as copper...is deposited on the seed layer.’” Pet., 128 (quoting EX1010 [Yu], 3:5-19). The Petition maps Yu’s copper seed layer as the claimed “third copper layer” and Yu’s copper conductive material as the claimed “fourth copper layer.” *Id.*; EX1003 [Shanfield Decl.], ¶¶471-2.

Yu’s description of metallization layer 20, as quoted by the Petition, discloses two layers: a copper seed layer and copper conductive material electroplated onto that seed layer. EX1010 [Yu], 3:5-19. Yu states that the seed layer is deposited “on the molding compound 18”—that is, directly on a dielectric surface, with no intervening layer described. *Id.*; EX2018 [Ricketts Decl.], ¶227-

228. Yu's own teaching therefore does not disclose the claimed "first metal layer," which limitation 16(d)(iii) requires to underlie the third copper layer. *Id.*

The Petition does not explain why its stated rationale for adding an adhesion layer applies to the interface Yu discloses. EX2018 [Ricketts Decl.], ¶229. The Petition's rationale is directed to a metal-to-metal interface. The Petition states that "Lin-191's multi-layered copper structure corresponds to sequentially deposited seed and plating layers formed during electroplating, providing adhesion to the underlying metal layer and buildup of conductor thickness." Pet., 16-17 (citing EX1003 [Shanfield Decl.], ¶ 163). The Petition further states that "[n]ickel layer 31 advantageously mitigates copper diffusion out of the metal interconnect, reducing void formation." Pet., 17 (citing EX1003 [Shanfield Decl.], ¶¶163-168). Dr. Shanfield likewise states that "Lin-191's nickel adhesion layer 31 would have prevented diffusion of copper into adjacent interconnects, as nickel was known to resist copper diffusion." EX1003 [Shanfield Decl.], ¶162.

The interface Yu describes is not the interface those statements address. EX2018 [Ricketts Decl.], ¶230. In Yu, the seed layer of metallization layer 20 is deposited directly on molding compound 18, an organic encapsulant, and there is no adjacent metal interconnect at that interface into which copper could diffuse. EX1010 [Yu], 3:5-19. Whether an adhesion or barrier layer is used at a given interface depends on the specific materials involved, and the Petition offers no

reason directed to a copper-to-organic interface. EX2018 [Ricketts Decl.], ¶230. Yu describes its metallization process—including the composition and deposition of both the seed layer and the conductive material formed on it—in detail, and does not describe any adhesion or barrier layer as part of that process. *Id.*; EX1010 [Yu], 3:5-19.

To supply a first metal layer that Yu itself does not disclose or require, the Petition turns to a different reference. The Petition states that “Lin-191’s adhesion layer 31 is a first metal layer with two copper layers formed thereon,” Pet., 129 (citing EX1005 [Lin-191], Fig. 22, [0127]), and that a POSITA would have been motivated “to apply Lin-191’s three-metal layer interconnect teachings to Yu’s first metal interconnect, yielding the claimed layer[s] to obtain the benefits of Lin-191’s adhesion layer 31.” Pet., 129-130; EX1003 [Shanfield Decl.], ¶¶473-474; EX2018 [Ricketts Decl.], ¶231.

The Petition does not explain how Lin-191’s adhesion layer 31 is to be incorporated into Yu’s own, already fully-described deposition sequence for metallization layer 20. EX2018 [Ricketts Decl.], ¶232. Lin-191’s adhesion layer 31, together with its own seed layer 32 and metal layer 33, is itself a complete, three-layer interconnect structure within Lin-191’s own package. EX1005 [Lin-191], [0127]-[0128], [0133]. Yu, however, already describes metallization layer 20 as beginning with a copper seed layer deposited directly on the molding

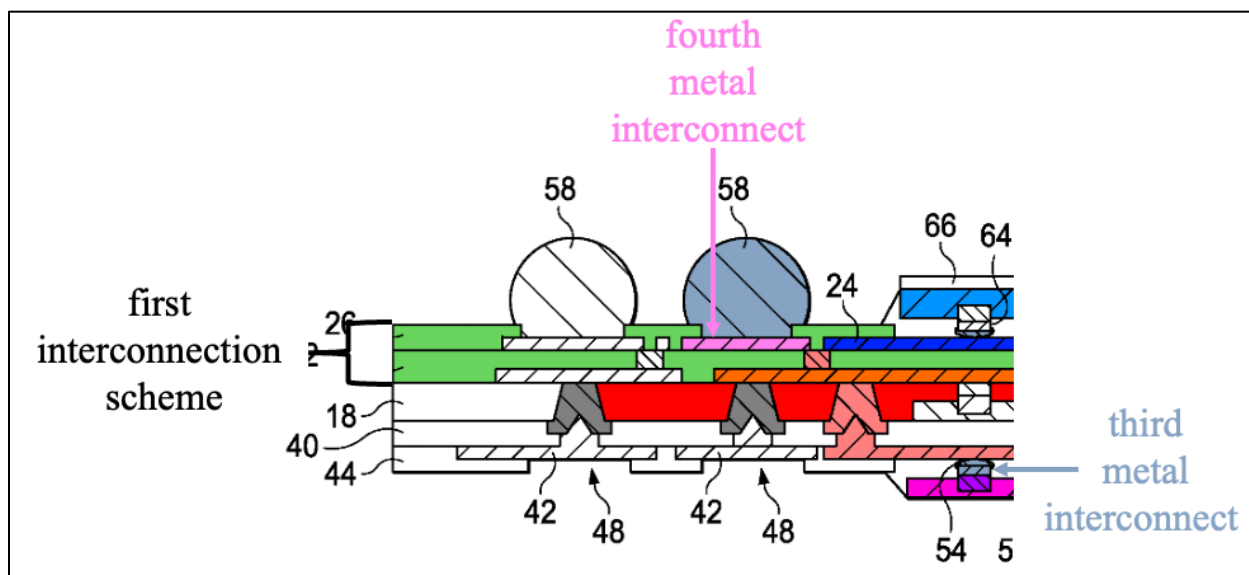
compound, with no adhesion layer beneath it. EX1010 [Yu], 3:5-19. The Petition's proposal to "apply" Lin-191's three-layer teaching to Yu's already-complete two-layer structure does not explain whether a POSITA would insert Lin-191's adhesion layer 31 between the molding compound and Yu's existing seed layer, substitute Lin-191's entire three-layer stack for Yu's seed layer, or make some other modification, nor does it explain why a POSITA would depart from Yu's own express disclosure that the seed layer is deposited directly on the molding compound. EX2018 [Ricketts Decl.], ¶232.

The Petition also does not explain why a POSITA would have understood Yu's own two-layer metallization structure to require modification at all. EX2018 [Ricketts Decl.], ¶233. Yu presents its seed-layer/electroplated-copper sequence as a complete process for forming metallization layer 20, without describing any deficiency that an added adhesion layer would remedy. EX1010 [Yu], 3:5-19. The Petition's stated motivation—that the modification would provide "the benefits of Lin-191's adhesion layer 31," (Pet., 129-130)—does not identify any problem with Yu's own structure that those benefits would address, nor explain why a POSITA would modify an already complete, fully-disclosed interconnect structure to import an additional layer from an unrelated reference. EX2018 [Ricketts Decl.], ¶233.

Thus, the Petition has not shown that Yu and Lin-191 teach or suggest limitation 16(d)(iii), and therefore has not shown that claim 16, or the claims depending therefrom, are unpatentable on this ground.

3. Claim 25: Yu and Lin-191 Do Not Teach Or Suggest a “Fourth Metal Interconnect”

Claim 25 recites in part “wherein said third metal interconnect is connected to said a fourth metal interconnect of said first interconnection scheme.” The Petition alleges “another portion of metallization layer 24” in Yu figure 33 (highlighted in purple below) is the claimed “fourth metal interconnect”:

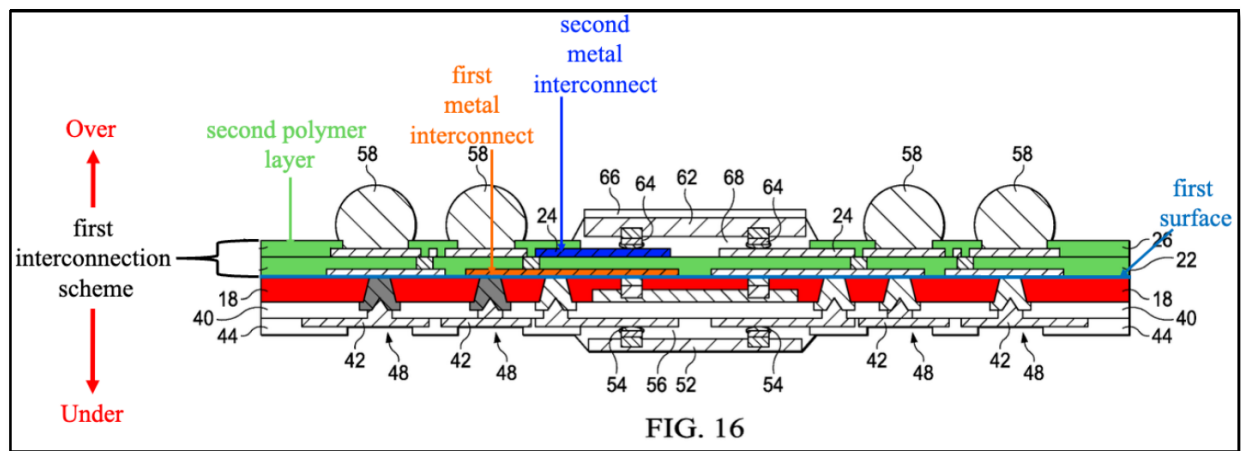


Pet., 144 (annotating EX1010 [Yu] Fig. 16).

Claim 16, from which claim 25 depends, recites a first metal interconnect and a second metal interconnect of the first interconnection scheme, and does not recite a third or fourth metal interconnect of that scheme. EX1001 [’768 Patent], cl.

16. A POSITA would understand the “fourth metal interconnect of said first interconnection scheme” recited in claim 25 to be a metal interconnect distinct from the first and second metal interconnects recited in claim 16. EX2018 [Ricketts Decl.], ¶236.

The portion of Yu’s metallization layer 24 that Petitioners allege is the “fourth metal interconnect” is part of the same metallization layer 24 that Petitioners allege is the “second metal interconnect.” EX2018 [Ricketts Decl.], ¶237. Below is the image taken from page 127 of the Petition showing what the Petition identifies as the “first” and “second” metal interconnects:



Pet., 127.

The Petition therefore identifies two different portions of the same metallization layer 24 as two different claimed interconnects — the “second metal interconnect” and the “fourth metal interconnect.” Two portions of a single metallization layer, lying on the same conductive path, are not two metal

interconnects. EX2018 [Ricketts Decl.], ¶238. The “first metal interconnect,” the “second metal interconnect” and the “fourth metal interconnect” must be different interconnects, and the Petition does not identify the claimed “fourth metal interconnect.” *Id.*

Claim 25 further requires that the “third metal interconnect compris[e] a second metal layer on said metal pad and a fifth copper layer over said second metal layer, wherein said fifth copper layer has a thickness between 5 and 30 micrometers.” EX1001 [’768 Patent], cl. 25. This limitation is materially the same as limitation 1(f)(ii) of claim 1. *Id.*, cl. 1. For the reasons discussed above in connection with Grounds 1A and 2A, Lin-191 does not disclose a single “second metal layer” on the metal pad, and does not direct a POSITA to a copper layer having a thickness between 5 and 30 micrometers. EX1005 [Lin-191], [0389]-[0390], [0396]; EX2018 [Ricketts Decl.], ¶239.

The Petition’s own description of claim 25 confirms that the structures it identifies lie on a single conductive path. EX2018 [Ricketts Decl.], ¶240. The Petition states that “Yu’s third metal interconnect is connected to another portion of metallization layer 24 (fourth metal interconnect) through a portion of metallization layer 42, a TMV 38, the first metal interconnect, and a via.” Pet., 144. That path runs through the structure the Petition identifies as the first metal interconnect and arrives at another portion of the same metallization layer 24 that

the Petition identifies as the second metal interconnect. EX2018 [Ricketts Decl.], ¶240.

Accordingly, the Petition fails to identify the claimed “fourth metal interconnect.”

D. The Petition Fails Because It Contradictorily Characterizes the Asserted Reference

Because the prior art does not teach or suggest the architecture recited in the challenged claims, the Petition’s arguments internally contradicts themselves, relying on the same disclosure from the asserted references to satisfy distinct and incompatible limitations. As one example below, the Petition alleges Lin-191’s adhesion layer and seed layer collectively constitute a single metal layer for some claim limitations, but elsewhere argues that Lin-191’s adhesion layer and seed layer constitute separate metal layers for other limitations. *See, e.g., supra*, §V.A.2.b. As another example, the Petition flips the frame of reference (i.e., changes “over” to “under”) depending on the limitation and the reference’s disclosure. *See, e.g., supra*, §V.A.6; V.B.5. In each case, the Petition argues contradictory positions, often for the same claim and same ground.

Petitioners at all times bear the burden to prove unpatentability by a preponderance of the evidence. 35 U.S.C. §316(e); *Dynamic Drinkware, LLC v. Nat’l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015). Petitioners cannot

satisfy this burden when their own internal mappings of the asserted references directly contradict one another. Thus, the Petition fails for this additional reason.

VI. CONCLUSION

For at least the foregoing reasons, Petitioners have failed to demonstrate by a preponderance of the evidence that any challenged claim is unpatentable.

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CERTIFICATE OF COMPLIANCE

Pursuant to 37 C.F.R. § 42.24(d), Patent Owner certifies that this Patent Owner Response has 13,375 words as counted by the word-processing system used to prepare this document. This word count complies with the 14,000 word limit under 37 C.F.R. § 42.24(b)(1).

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CERTIFICATE OF SERVICE

The undersigned hereby certifies that the foregoing PATENT OWNER'S RESPONSE was served electronically via email on August 7, 2026, on the following counsel of record for Petitioners:

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