UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TAIWAN SEMICONDUCTOR
MANUFACTURING COMPANY LTD. and APPLE INC.,
Petitioners,

v.

MYW SEMITECH, LLC,
Patent Owner.

Case No. IPR2026-00065
U.S. Patent No. 11,107,768

DECLARATION OF DAVID S. RICKETTS

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PATENT OWNER'S EXHIBIT LIST

Exhibit No.	Description
2001	U.S. Patent No. 9,615,453
2002	Information Disclosure Statement for U.S. Application No. 17/929,180 dated December 21, 2023
2003	[SEALED] Email chain between Richard Juang, counsel for MYW Semitech, and Daniel Richards, counsel for Apple Inc., regarding production of materials
2004	[SEALED] Defendant Apple Inc.'s First Supplemental Responses to Plaintiff MYW Semitech, LLC's First Set of Interrogatories (Nos. 1-12)
2005	[SEALED] Email chain between Richard Juang, counsel for MYW Semitech, and Daniel Richards, counsel for Apple Inc., regarding availability of source code
2006	[SEALED] Email chain between Richard Juang and Peter Yang, counsel for TSMC, regarding inventorship.
2007	Oral Order for Motion to Stay Pending *Inter Partes* Review, *MYW Semitech, LLC v. Apple Inc.*, 1-25-cv-00504 (DDE) Dkt. 68 (January 21, 2026)
2008	Stipulation and [Proposed] Order to Amend Scheduling Order, *MYW Semitech, LLC v. Apple Inc.*, 1-25-cv-00504 (DDE) Dkt. 58 (December 3, 2025)
2009	Apple Inc.'s Infringement Contentions, *MYW Semitech, LLC v. Apple Inc.*, 1-25-cv-00504 (DDE) (January 9, 2026)
2010	Agreed Stipulation Regarding the Discovery of Electronically Stored Information, *MYW Semitech, LLC v. Apple Inc.*, 1-25-cv-00504 (DDE) Dkt. 39 (October 14, 2025)

2011	Revision to Rules of Practice Before the Patent Trial and Appeal Board, 90 Fed. Reg. 48,335 (proposed Oct. 17, 2025) (to be codified at 37 C.F.R. pt. 42).
2012	Declaration of Richard Juang
2013	Default Protective Order
2014	Apple Inc's Proposed Constructions in *MYW Semitech, LLC v. Apple Inc.*, C.A. No. 25-504-RGA-EGT (Feb. 12, 2026)
2015	Joint Claim Construction Chart in *MYW Semitech, LLC v. Apple Inc.*, C.A. No. 25-504-RGA-EGT (Feb. 26, 2026)
2016	Defendant Apple Inc.'s Answering Claim Construction Brief
2017	Defendant Apple Inc.'s Initial Invalidity Contentions (Cover Document)
2018	Declaration of Professor David S. Ricketts
2019	CV of Professor David S. Ricketts
2020	Deposition Transcript of Stanley Shanfield, Ph. D., dated July 14, 2026.
2021	*Coefficient of Thermal Expansion (CTE)*, BYU Integr. Microfabrication Lab, https://cleanroom.byu.edu/cte_materials (last visited Aug. 6, 2026).
2022	Rogers Corp., *ULTRALAM® 3000 Liquid Crystalline Polymer Circuit Material*, Double-Clad Laminates, Data Sheet No. RF1.3000, Publication No. 92-125 (rev. May 10, 2011).
2023	J. Yoon et al, "Enhancing bonding strength of the electroplated Cu pillars for semiconductor package by controlling grain orientation," Scientific Reports (2026).

I have personal knowledge of the facts set forth in this declaration and, if called to testify as a witness, would testify under oath as follows:

I. BACKGROUND

1. I have been retained as an expert by MYW Semitech, LLC ("Semitech") in the above-captioned matter (IPR2026-00065).

2. I have been asked by Semitech to provide my expert opinion regarding the patentability of claims 1-28 of U.S. Patent No. 11,107,768 ("the '768 Patent") in view of the grounds asserted in IPR2026-00065. For the reasons set forth below, it is my opinion that claims 1-28 of the '768 Patent are patentable over the grounds asserted in IPR2026-00065.

II. PROFESSIONAL QUALIFICATIONS

3. I am currently Full Professor of Electrical and Computer Engineering at North Carolina State University ("NCSU"), a position I have held since 2012. In this position, I conduct research and teach undergraduate and graduate students in the field of electrical and computer engineering. My professional career spans approximately three decades and encompasses both industry and academic experience in the design, development, testing, and management of power electronics and power conversion systems, including uninterruptible power supplies ("UPS"), AC-DC converters, DC-DC converters, DC-AC converters,

battery charging and battery management systems, and power management integrated circuits ("ICs").

4. The courses I teach at NCSU include Advanced Analog Integrated Circuit ("IC") Design, Radio System Design, Analog Circuit Laboratory, and Power Management IC Design. My Power Management IC Design course addresses the design and analysis of power conversion circuits and the integrated circuits that control them, including the converter topologies, control circuits, feedback systems, and protection circuits that are foundational to AC-DC and DC-DC power conversion products. In teaching these courses, I instruct students in the same fundamental principles of power conversion, regulation, and control that I applied throughout my industry career designing UPS systems and power converters.

5. At NCSU, I lead a research group that conducts research on and designs electrical and electronic circuits, including millimeter wave and microwave circuits and systems, radio frequency identification ("RFID") circuits, wireless power transfer circuits, power management controllers, DC-DC and AC-DC converters, analog circuits, and radio frequency ("RF") circuits. A substantial portion of my research program is devoted to power electronics and power conversion. I lead research in power electronics and power conversion integrated

circuits, and my group designs power management systems that include both integrated circuits and discrete power converters. This work involves the same classes of circuits found in commercial power conversion products, including switching converters, rectification circuits, regulation and control loops, and battery charging circuitry.

6. My research group at NCSU also designs microcontroller-based Bluetooth systems and other mixed-signal RF/digital systems. This work requires the integration of digital control, embedded firmware, and analog and power circuitry within a single system, which is the same engineering discipline required to design microcontroller-supervised power conversion products such as UPS systems, battery chargers, and power management controllers.

7. Prior to my current position, I served as an Assistant Professor of Electrical and Computer Engineering and Assistant Professor of Materials Science and Engineering at Carnegie Mellon University from 2006 to 2012, where I likewise conducted research and taught in the areas of circuits and systems.

8. I received my B.S. and M.S. degrees in Electrical Engineering from Worcester Polytechnic Institute in Worcester, Massachusetts, in 1995 and 1997, respectively. I received my Ph.D. in Electrical Engineering from Harvard University in Cambridge, Massachusetts, in 2006.

9. Throughout my doctoral studies and academic career, I have personally worked hands-on in the cleanroom and semiconductor fabrication facilities at Harvard University, Carnegie Mellon University, and North Carolina State University. In these facilities, I fabricated, processed, and characterized semiconductor devices and nanoscale structures, gaining direct experience with semiconductor processing techniques, including lithography, thin-film deposition, etching, surface preparation, and metrology, as well as the handling, mounting, and characterization of semiconductor die and wafers.

10. Prior to entering academia, I spent approximately eight years as an engineer in private industry, holding several engineering and managerial positions in which I developed, and oversaw the development of, electrical and electronic circuits, including those related to power transfer, power conversion, and semiconductor design in wired and wireless circuits and systems. The core of my industry career was the design and development of power conversion products — in particular, uninterruptible power supplies and the AC-DC, DC-DC, and DC-AC converters within them, as well as the power management integrated circuits that control such converters.

11. From 1995 to 1999, I held positions as an engineer and senior engineer at American Power Conversion ("APC"), which at the time was one of

the world's leading manufacturers of uninterruptible power supplies. At APC, I personally designed AC-DC and DC-DC converters for use in APC's UPS products.

12. As a design engineer at APC, I designed and tested complete uninterruptible power supply products. The UPS products I worked on were complex, multi-converter power systems: each contained an AC-DC converter to rectify and convert incoming AC line power, a DC-AC converter (inverter) to synthesize AC output power from the internal battery, DC-DC conversion stages, and an embedded microcontroller that supervised the operation of the system, including monitoring line conditions, managing the transfer between line power and battery power, controlling battery charging, and implementing protection functions. My work on these products encompassed circuit design, prototyping, testing, and validation of the power conversion stages and their interaction with the supervisory microcontroller.

13. Through this work at APC, I gained direct, hands-on experience with the full range of engineering issues involved in AC-DC converter design, including rectification, power factor considerations, switching converter topologies, transformer and magnetics design, feedback and regulation, component selection

and stress analysis, thermal design, protection circuitry, and safety and regulatory requirements applicable to products that connect to the AC mains.

14. While at APC, I also headed the battery technology group. Batteries are the energy storage element at the heart of every UPS, and the charging, monitoring, and health assessment of the battery are central to UPS product performance and reliability. In leading the battery technology group, I developed models for battery health that could be adapted into microcontroller-based systems, allowing a UPS or similar product to assess the condition of its battery in real time using its embedded controller. This work required detailed understanding of battery charging circuits and algorithms, battery discharge behavior, and the integration of battery management functions into microcontroller firmware and supervisory control.

15. From 1999 to 2001, I held a position as a Principal Consultant at Renaissance Design, Inc., where I designed power management ICs. Power management ICs are the integrated circuits that implement the control, regulation, drive, and protection functions of power converters, including AC-DC and DC-DC converters and battery chargers. In this role I was responsible for circuit design at the silicon level for such devices.

16. From 2000 to 2002, I held a position as Manager of New Product Development at ON Semiconductor Corp., a major manufacturer of power management semiconductors. In that position, I was responsible for six product development teams and oversaw the development of over twenty power management ICs in bipolar, CMOS, and BiCMOS technologies. The products developed under my direction included controllers for power conversion applications. My group designed power management controllers and built application boards for battery chargers and buck converters. Buck converters are a fundamental class of DC-DC converter, and battery charger circuits are a core building block of battery-powered and battery-backed products, including UPS systems, portable power products, and consumer electronics.

17. In overseeing these product development teams at ON Semiconductor, my responsibilities extended beyond circuit design to the full product development cycle for power management semiconductors, including product definition, design reviews, silicon validation, application board development and bench evaluation, and support of customers designing the ICs into end products such as battery chargers and DC-DC converter power stages.

18. From 2002 to 2003, I held the position of Advanced System Engineering Manager at ON Semiconductor Corp., where I directed a team of

system engineers developing multi-phase power management ICs for Intel and AMD microprocessors. Multi-phase power management ICs control multi-phase buck (DC-DC) converters that deliver tightly regulated, high-current power to microprocessors, and their design requires expertise in converter topology, current sharing and balancing among phases, feedback control, and transient response.

19. Taken together, my industry experience includes the design and testing of complete UPS products; the design of the AC-DC, DC-DC, and DC-AC converter stages within such products; leadership of battery technology development, including battery charging and microcontroller-based battery health monitoring; the silicon-level design of power management ICs; and the management of engineering teams developing power management controllers, battery chargers, and DC-DC converter products.

20. My academic research and teaching have continued and deepened this expertise. At NCSU, my group designs power management systems, including integrated circuits as well as discrete power converters, and designs microcontroller-based systems in which embedded controllers supervise analog and power circuitry — the same architecture used in UPS systems, battery chargers, and other microcontroller-supervised power conversion products.

21. A substantial portion of my academic research has been devoted to nanofabrication and nanoscale devices — that is, the fabrication, characterization, and application of structures and devices with dimensions on the nanometer scale. At Carnegie Mellon University, I led research on Tip-directed, Field-emission Assisted Nanofabrication ("TFAN") as part of the DARPA Tip-Based Nanofabrication (TBN) program, in collaboration with Professors Bain, Carley, Davis, Fedder, Sitti, and Islam. This research used tip-directed, field-emission-assisted chemical vapor deposition (CVD) for the precise fabrication of structures on the nanometer scale, in which device geometry is determined by probe manipulation and controlled energy delivery at the probe tip, enabling control of the length, width, orientation, and height of nanoscale structures during fabrication. The work included the deposition of silicon nanowires by using field-emitted electrons to locally crack adsorbed silane (SiH_4) and disilane (Si_2H_6), and methods for localized surface preparation, including targeted desorption of hydrogen on hydrogen-terminated silicon substrates to localize silane adsorption. This research required extensive hands-on work with scanning tunneling microscopes (STM), atomic force microscopes (AFM), ultra-high vacuum systems, and semiconductor surface preparation and characterization.

22. My nanofabrication research has resulted in numerous peer-reviewed publications and presentations. Representative journal publications relating to nanofabrication and nanoscale devices include:

- W. Hu, J. Bain and D. S. Ricketts, "An AFM/STM multi-mode nanofabrication approach allowing in situ surface modification and characterization," Micro and Nano Letters, vol. 8, pp. 43–46, Jan. 2013.
- W. Hu, J. A. Bain and D. S. Ricketts, "In-situ quantification of electrical isolation in STM-fabricated TiOx nanostructures," Micro and Nano Letters, vol. 7, no. 4, pp. 334–336, Apr. 2012.
- O. Ozcan, W. Hu, M. Sitti, J. Bain, and D. S. Ricketts, "Investigation of tip current and normal force measured simultaneously during local oxidation of titanium using dual-mode scanning probe microscopy," Micro & Nano Letters, vol. 9, no. 5, pp. 332–336, May 2014.
- D. S. Ricketts, J. A. Bain, Y. Luo, S. Blanton, K. Mai and G. K. Fedder, "Enhancing CMOS using nanoelectronic devices, a perspective on hybrid integrated systems," Proceedings of the IEEE, vol. 98, no. 12, pp. 2061–2075, Dec. 2010.

- M. E. Karagozler, S. C. Goldstein and D. S. Ricketts, "Scalable self-assembly process for the fabrication of sub-millimetre three-dimensional cylindrical tubes," IET Micro & Nano Letters, vol. 11, no. 1, pp. 4–8, 2016.
- R. S. Friedman, M. C. McAlpine, D. S. Ricketts, D. Ham, and C. M. Lieber, "High-speed integrated nanowire circuits," Nature, vol. 434, p. 1085, Apr. 2005.

23. Representative peer-reviewed conference publications and presentations relating to nanofabrication and nanomanufacturing include:

- J. R. Smith, W. Hu, Y.-Y. Dang, O. Ozcan, M. Sitti, J. A. Bain, D. S. Ricketts, and R. Davis, "Scanning Probe Nanomanufacturing on Si: Surface Characterization of the Process Technique," Materials Research Symposium, paper G1.5, Nov. 2010.
- J. R. Smith, W. Hu, Y. Y. Dang, O. Ozcan, M. Sitti, J. Bain, R. Davis and D. S. Ricketts, "Writing Si nanowires on Si (100) with an STM tip: surface preparation and initial results," Materials Research Symposium, M11.50, Boston, MA, Nov. 2009.

- J. R. Smith, et al. (with D. S. Ricketts), Proc. SPIE 7637, Alternative Lithographic Technologies II, 76371D (2010) (scanning-probe-based nanofabrication on silicon).
- W. Hu, J. Gu, Z. George and D. S. Ricketts, "Directed scanning probe nanomanufacturing of lateral Ti-TiO2-Ti junctions for low capacitance MIM rectenna diodes," Micro and Nano Engineering Conf., Berlin, Sept. 2011.
- W. Hu, Y. Tang, Y. Zhang, J. Gu, S. Tamaru, J. A. Bain, L. R. Carley, R. F. Davis, G. K. Fedder and D. S. Ricketts, "Ti/TiO2 nanodevice fabrication using compliant probes and CMOS probe-arrays," Technologies for Future Micro-Nano Manufacturing, Napa Valley, CA, Aug. 2011.
- W. Hu, S. Tamaru, J. A. Bain and D. S. Ricketts, "High Current Pulse Generation for Thermal Surface Modification using Standard STM," Int. Conf. Electron, Ion, Photon Beam Technology and Nanofabrication, May 2011.
- J. R. Smith, D. S. Ricketts and J. A. Bain, "Localized thermal modification of surfaces via pulsed electron bombardment from an

STM tip," Int. Conf. Electron, Ion, Photon Beam Technology and Nanofabrication, May 2011.

- W. Hu, J. A. Bain and D. S. Ricketts, "In-situ characterization using AFM probes in multiple modes," Int. Conf. Electron, Ion, Photon Beam Technology and Nanofabrication, May 2012.
- O. Ozcan, W. Hu, M. Sitti, J. A. Bain and D. S. Ricketts, "Experimental Investigation of Force, Conduction and Growth in Nano-oxidation using scanning probe microscopy," Enabling Nanomanufacturing for Rapid Innovation, Aug. 2013 (Best Poster).
- D. S. Ricketts, T. Schlesinger, Y. Luo and J. Bain, "Materials and Devices for Hybrid CMOS Circuits: Expanding the Functionality of Nanoscale CMOS," Nano-DDS Conference, Ft. Lauderdale, FL, Oct. 2009 (Invited).

24. During my doctoral research at Harvard University, I collaborated with the research group of Professor Charles Lieber, a leading group in nanowire synthesis, on the design and characterization of high-speed integrated nanowire circuits. This work, published in Nature (R. S. Friedman, M. C. McAlpine, D. S. Ricketts, D. Ham, C. M. Lieber, "High-speed integrated nanowire circuits," Nature, vol. 434, p. 1085, Apr. 2005), demonstrated integrated circuits built from

semiconductor nanowires and required detailed understanding of nanoscale semiconductor devices, their fabrication, and their integration into functional circuits.

25. My research has also included nanoscale magnetic and spintronic devices, including spin-torque nano-oscillators and magnetic tunnel junctions with dimensions below 30 nanometers. This work was supported in part by my 2008 DARPA Young Faculty Award, "Spin-torque Oscillators for Spectrum-Agile RF," and involved the fabrication and characterization of nanoscale magnetic devices, including spin-transfer-torque switching of magnetic tunnel junctions using conductive atomic force microscopy. Representative publications include: S. Tamaru and D. S. Ricketts, "Measurement of ultra-low power oscillators using adaptive drift cancellation with applications to nano-magnetic spin torque oscillators," Review of Scientific Instruments, vol. 84, p. 054704, May 2013; E. R. Evarts, L. Cao, D. S. Ricketts, N. D. Rizzo, J. A. Bain, and S. A. Majetich, "Spin transfer torque switching of magnetic tunnel junctions using a conductive atomic force microscope," Applied Physics Letters, vol. 95, 132510 (2009); E. R. Evarts, L. Cao, D. S. Ricketts, N. D. Rizzo, J. A. Bain, and S. A. Majetich, "Characterization of conducting atomic force microscopy for use with magnetic tunnel junctions," IEEE Transactions on Magnetics, vol. 46, no. 6, pp. 1741–1744,

June 2010; and E. R. Evarts, et al., "Spin Torque Switching of 26 nm Diameter Magnetic Tunnel Junction Using a Conductive Atomic Force Microscope," Conference on Magnetism and Magnetic Materials, paper FC-13, Nov. 2010.

26. I have been recognized as a leader in the field of nanofabrication and nanomanufacturing. I served as Technical Program Chair of the Enabling Nanomanufacturing for Rapid Innovation TRC/NSF Workshop in August 2013, and delivered the keynote address, "Enabling Rapid Innovation in Nanomanufacturing," at the ENRI NSF workshop in Napa, California in August 2013. I served as Session Chair for Nanotechnology at the CMOS Emerging Technologies Conference (Banff, Canada, 2009) and at the NANO-DDS conference (2011). I have also given invited presentations on nanofabrication at the National Institute of Standards and Technology (NIST) ("Tip-directed, Field-assisted Nanofabrication," Mar. 2011), Zyvex Corp. ("Tip-assisted, field emission nanofabrication," Apr. 2010), Worcester Polytechnic Institute ("Tip-assisted Nanofabrication," Mar. 2010), and the Army Research Laboratory ("Nanoscale magnetics for integrated power conversion and RF," Jan. 2011).

27. In recognition of my research, I received the National Science Foundation Faculty Early Career Development (CAREER) Award, one of the

NSF's most prestigious awards in support of early-career faculty, as well as the DARPA Young Faculty Award (2008).

28. My research has also encompassed advanced semiconductor packaging at the micro- and nanoscale. As part of the DARPA Efficient Linearized All-Silicon Transmitter ICs ("ELASTx") program — a program directed at developing monolithic, high power-added-efficiency, high-linearity, millimeter-wave silicon-based transmitter ICs — I designed and built 100 GHz integrated packaging using liquid crystal polymer (LCP) substrates of 25 μm thickness, solder microbumps, and multi-layer metal interconnect. This advanced 3D packaging work involved semiconductor die mounting on substrates, including the use of solder balls and microbumps, and required detailed understanding of semiconductor die attachment, interconnect design, substrate materials, and the assembly and integration of semiconductor die into packaged systems.

29. I have published at least 49 academic journal papers, as shown in my curriculum vitae, relating to various topics including millimeter wave and microwave circuits and systems, RFID circuits, wireless power transfer circuits, analog circuits, and RF circuits.

30. I have also authored at least 78 conference articles, as shown in my curriculum vitae, relating to various topics including millimeter wave and

microwave circuits and systems, RFID circuits, wireless power transfer circuits, analog circuits, and RF circuits.

31. In sum, I have approximately three decades of combined industry and academic experience in power electronics and power conversion, with particular depth in uninterruptible power supplies, AC-DC and DC-DC converter design, battery charging and battery management, and the power management integrated circuits that control such systems, as well as in analog, RF, and microcontroller-based mixed-signal systems, and in semiconductor fabrication, nanofabrication, nanoscale devices, and advanced semiconductor packaging.

32. My curriculum vitae, which includes a complete list of my qualifications and publications, is being filed as Exhibit 2019 in this IPR.

III. MATERIAL CONSIDERED

33. In preparing this declaration, I have reviewed the public papers and exhibits filed in this IPR to date, including the specification, claims and prosecution history of the ’768 Patent, the references asserted in the Petition, and the exhibits filed concurrently with this Declaration as part of the Patent Owner Response.

IV. LEGAL STANDARDS

34. I am not an attorney, and I have not independently researched the law. MYW's counsel has explained certain legal principles to me that I have relied on in forming my opinions set forth in this declaration. I have applied these legal principles in arriving at my opinions expressed in this declaration. They are set forth below.

35. I have been informed and understand that an invention cannot be patented if the subject matter as a whole would have been obvious to a person of ordinary skill in the art at the time of the invention. Also, while the prior art is compared to each claim on an element-by-element basis, the claimed invention as a whole must have been obvious to one of ordinary skill in order for a claim to be invalid.

36. I understand that the fundamental question in analyzing obviousness is whether, at the time of the invention, the subject matter of the claimed invention as a whole would have been obvious to a person of ordinary skill in the art to which the subject matter pertains, taking into account: (a) the scope and content of the prior art; (b) the differences between the prior art and the claims at issue; (c) the level of ordinary skill in the art; and (d) any objective indicia of non-obviousness referred to as secondary considerations. The secondary considerations

may include: (1) a long-felt but unmet need in the prior art that was satisfied by the claimed invention; (2) the failure of others; (3) skepticism; (4) commercial success of a product covered by the patent; (5) industry praise of the claimed invention; and (6) copying of the invention.

37. A combination of prior art references must teach or suggest all of the recited limitations of the claim for the invention to be found obvious.

38. It is important in the obviousness inquiry to identify whether a reason existed at the time of the invention that would have motivated a person of ordinary skill in the art in the relevant field to combine or modify the prior art references in the manner proposed by the petitioner so as to arrive at the claimed invention. Put another way, a finding of obviousness should be supported by an apparent reason to combine or modify the prior art references as proposed by the petitioner.

39. It is important in the obviousness inquiry to understand how the combination of references is supposed to work. An explanation of the operation of the combined references is often a prerequisite to showing that a person of ordinary skill in the art would have had an apparent reason to make the proposed combination and would have had a reasonable expectation of success.

40. A finding of obviousness requires the additional showing that a person of ordinary skill at the time of the invention would have selected and combined

those prior art elements in the normal course of research and development to yield the claimed invention. In addition, a person of ordinary skill in the art should have had a reasonable expectation of success in combining the references as proposed.

41. In assessing obviousness, one must consider both the ordinary creativity and common sense of the person of ordinary skill in the art. I understand that in *inter partes* reviews, it is impermissible for common sense to be applied to fill gaps in prior art that fails to teach or suggest a limitation of the claim.

42. Multiple references can be combined, with one another and/or with the knowledge of a person of ordinary skill in the art, in rendering a claim obvious. However, obviousness cannot be established by simply demonstrating that each element was independently known in the prior art. Rather, it may be necessary to identify a reason, such as a teaching, suggestion, or motivation, which would have prompted a person of ordinary skill in the art to combine the elements in the way the claimed invention does.

43. Obviousness cannot be established through hindsight. That means the claimed invention cannot be used as a roadmap to combine elements from different pieces of prior art, or different embodiments of a single prior art reference, to create the claimed invention. The claimed invention as a whole must be compared to the prior art as a whole, and one must avoid aggregating pieces of prior art

through hindsight that would not have been combined absent the patent inventor's insight.

V. LEVEL OF ORDINARY SKILL IN THE ART

44. Petitioners allege the following level of ordinary skill:

> A POSITA at the time of the '768 Patent would have had at least a bachelor's degree in electrical engineering, materials science, or physics (or an equivalent degree), and at least two years of experience in semiconductor design or semiconductor manufacturing. A master's degree or Ph.D. in a relevant field may substitute for some work experience or vice versa. Additional education or experience might substitute for the above requirements.

Pet., 1. For the purposes of this declaration, I have applied Petitioners' level of ordinary skill.

45. For purposes of this declaration, I have applied a priority date of September 26, 2012. My opinions in this declaration regarding a POSITA assume a POSITA as of September 26, 2012. As of September 26, 2012, I was at least a POSITA.

VI. CLAIM CONSTRUCTION

46. Petitioners allege that claim construction is unnecessary for this IPR. Pet., 2. For the purposes of this POR, I do not believe any claims need to be construed.

VII. TECHNOLOGY BACKGROUND

47. The following discussion reflects background knowledge and understanding that a POSITA would have possessed as of the priority date, based on my own education, training, and experience in the field of semiconductor design and packaging.

48. Though advances in transistor scaling have dramatically increased the computational capability of integrated circuits, no semiconductor chip operates in isolation. Every chip must communicate with the world outside it—with sensors, memory, other processors, power management circuitry, antennas, displays, or other semiconductor devices. Reliably transmitting electrical signals, power, and heat between the circuits on a chip and its external environment has long been one of the most critical aspects of semiconductor packaging.

49. Semiconductor packaging serves primarily as a protective enclosure that provides electrical connections between a chip and the outside world. Over time, packaging has grown into a sophisticated engineering discipline that materially affects electrical performance, power efficiency, thermal management, manufacturing cost, and overall system capability. As transistor dimensions have continued to shrink while system complexity has increased, conventional packaging approaches reached practical and economic limits, which motivated the

development of more advanced packaging technologies, including flip-chip assembly, wafer-level packaging, chiplet architectures, and three-dimensional integration.

50. One of the earliest, and still widely used, methods of connecting an integrated circuit to external circuitry is wire bonding. In wire bonding, the semiconductor die is mounted on a carrier substrate having relatively coarse conductive traces, and fine gold, aluminum, or copper wires are bonded between bond pads located around the perimeter of the die and corresponding traces on the substrate. Wire bonding became a mainstay of the industry because of its low production cost and high manufacturing yield.

51. Because wire bonds can only be formed to bond pads located around the edges of a die, the number of external connections that can be achieved scales approximately with the die's perimeter rather than its area. Since transistor count scales with die area while the number of available bond pads scales with perimeter, larger and more complex chips eventually became limited by the number of available input/output ("I/O") connections rather than by transistor density.

52. Wire bonds are also typically several millimeters long, and the inductance of a conductor of that length limits the speed, or bandwidth, of the signal that can be carried to and from the chip. Wire bonds are further susceptible

to mechanical vibration and to thermal fatigue and stress incurred during encapsulation. Although wire bonding remains highly reliable for many applications, these characteristics make it increasingly disadvantageous for extremely high-frequency or high-power devices.

53. To address these limitations, the industry developed flip-chip packaging. Rather than wiring only the perimeter of the die, flip-chip technology fabricates solder bumps directly across the active surface of the chip. The die is then mounted face-down, or "flipped," onto the package substrate, so that connections are distributed across the entire surface of the chip rather than confined to its edges. Because the achievable I/O count in a flip-chip design scales with chip area rather than perimeter, flip-chip packaging affords substantially higher interconnection density than wire bonding.

54. In a typical flip-chip implementation, solder bumps—commonly lead/tin alloy bumps formed on aluminum bond pads on the chip, sometimes referred to in the industry as C4 ("Controlled Collapse Chip Connection") bumps—are reflowed to bond the chip face-down, along the shortest available path, to the package substrate. Because the resulting interconnects are far shorter than wire bonds, flip-chip bumps introduce substantially less parasitic inductance, enabling higher-speed signaling, and their shorter current paths and greater areal

density reduce voltage drop and improve power distribution to increasingly power-hungry integrated circuits.

55. Flip-chip assemblies are also frequently underfilled: after the die is bonded, a polymer material—typically an epoxy resin loaded with fine silica or ceramic filler particles—is dispensed into the gap between the die and the substrate. Once cured, the underfill forms a rigid mechanical support around the solder bumps that improves the assembly's resistance to thermal and mechanical stress.

56. Notwithstanding these advantages, flip-chip packaging presents its own challenges. Pre-bond testability and post-bond visual inspection of the concealed solder joints are difficult, and because the chip, the solder bumps, and the package substrate are typically composed of different materials having different coefficients of thermal expansion ("CTE," sometimes also referred to as "TCE"), repeated thermal cycling can fatigue and eventually fracture the solder joints unless the materials in the assembly are reasonably well CTE-matched.

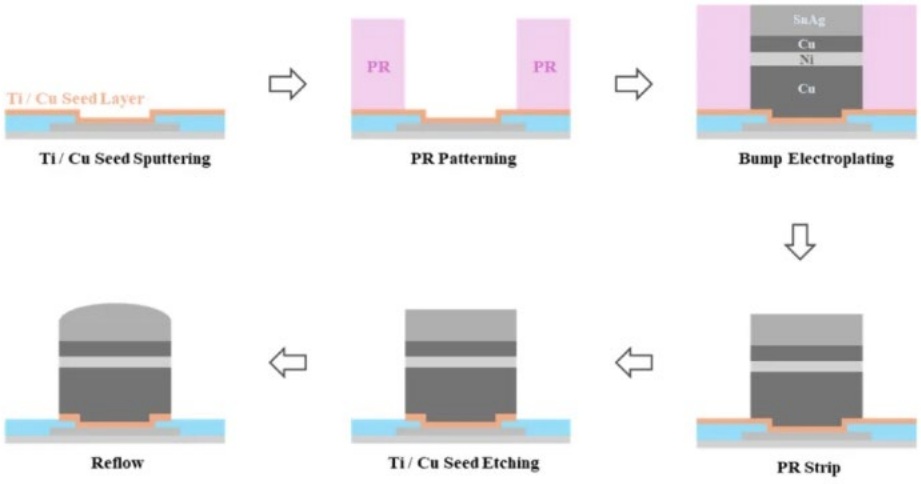
57. Flip-chip packaging also did not eliminate every interconnect bottleneck. As integrated circuits came to require thousands of signal connections among processors, memory, analog circuitry, and power-management circuitry, conventional printed circuit board ("PCB") technology was unable to keep pace

with the interconnect density achievable on the chips themselves. Adding routing layers to a PCB increases both its thickness and the signal propagation delay between chips—a particular concern for high-speed communication between a processor and memory operating at multi-gigahertz clock frequencies.

58. To reduce interconnect length and increase routing density beyond what a conventional PCB can offer, the industry developed interposer-based, or "2.5D" integration, in which multiple dies are mounted side by side on an interposer rather than directly on a PCB. Because an interposer can be fabricated using photolithography and thin-film metallization, it supports far finer routing pitches than a PCB. Silicon has traditionally been used as an interposer material, although other materials—including glass—have also been used as interposer substrates, offering potential advantages such as lower material cost and, depending on composition, a CTE that can be closely matched to silicon.

59. Dies are typically attached to an interposer using copper pillar bumps, or "microbumps," which are generally smaller than conventional C4 solder bumps and are fabricated differently. Whereas a C4 bump is composed primarily of solder, a copper pillar consists mainly of electroplated copper with only a thin solder cap. Electroplating is an electrochemical process used to create the bulk part of the pillar. In this process all dies on a wafer are first covered by a uniform

conductor layer, connected to a voltage source and immersed into an electrolyte containing copper ions. Copper ions receive electrons form copper atom on the surface of the wafer. The thin conductive layer is called a seed layer and is removed from the wafer after the process is completed. The process of the copper bump formation is schematically shown below. EX2023.



60. Formation of a copper pillar directly on a bare dielectric, or on a dissimilar metal such as an aluminum bond pad, is often preceded by depositing a thin titanium, or similar, adhesion layer and a thin copper seed layer, on which the pillar is then electroplated. Sometimes a third layer containing TiN or TaN is added in between the adhesion and seed layers to block the Cu from unwanted diffusion in the material underneath. Deposition of adhesion, barrier and seed layers is an example of a broader family of wafer-level microfabrication. Although

these layers may be deposited using the same technique, their metal composition and purpose is distinctively different. The choice of layers in such a sequence is typically driven by the specific materials present at the interface being built—for example, the poor adhesion of copper to a bare dielectric or oxide surface, or the tendency of certain dissimilar metal pairs, such as aluminum and copper.

61. These are real, well-studied phenomena, but they are specific to the particular materials being joined at a given interface—they are not a universal property of every metal-to-metal or metal-to-substrate contact. Where the metal already present at an interface is the same metal being added—for example, copper deposited on, or reflowed against, a surface that is already copper—neither the adhesion concern nor the interdiffusion concern described above is presented in the same way. In these cases, there is only a need for the seed layer because copper adheres readily to copper and there is no dissimilar-metal pair to interdiffuse.

62. Attaching a solder ball or solder bump to a metal pad is, in any event, a different kind of joining process altogether, with a different bonding mechanism than a thin film seeking to mechanically adhere to whatever lies beneath it. A solder joint forms when molten solder wets the pad and reacts with it, and that reaction is itself the bond. Where the pad is copper, tin-based solder reacts with the copper to form one or more copper-tin intermetallic compounds—principally

Cu_6Sn_5, and, with additional time or temperature, Cu_3Sn—at the solder-to-pad interface. The presence of that intermetallic layer is recognized in the industry as the evidence that a genuine metallurgical solder joint has been made. A solder ball or solder bump accordingly does not need a separate adhesion layer to bond to a copper pad. Forming that intermetallic bond to the copper is the result of reflowing solder against it, not a failure mode to be engineered around.

63. Beyond 2.5D integration, the industry has also developed true three-dimensional die stacking, in which multiple chips are stacked vertically and interconnected using through-silicon vias ("TSVs")—vertical conductive structures that extend completely through a silicon die. Because the resulting interconnects between stacked dies are extremely short, 3D stacking offers the highest interconnect bandwidth among the packaging approaches described above.

64. Advanced packaging techniques of this kind, however, introduce their own engineering challenges. Chief among them is heat removal: in a conventional package, heat generated by the die flows in a relatively direct path to a heat spreader. In a stacked or interposer-based assembly, however, internal dies have more limited cooling paths, and dies positioned closer to the heat spreader can thermally shield those farther away.

65. A related challenge is that advanced packages combine many different materials—semiconductor, metal, polymer, ceramic, and, in some instances, glass—at different locations within the same assembly. Different materials expand and contract by different amounts as temperature changes. Because integrated circuits are predominantly fabricated in silicon, it is generally desirable for the other materials in a package to have a CTE reasonably close to that of silicon. A significant CTE mismatch between adjoining materials can cause delamination, warping, or bowing and, as noted above, can fatigue and crack solder interconnects over repeated thermal cycling. This is one of the reasons that underfill materials are often loaded with silica or ceramic filler—to bring the underfill's effective CTE closer to that of the surrounding materials it contacts.

VIII. THE '768 PATENT

66. The '768 Patent was filed on January 26, 2020 as U.S. Patent Application No. 16/752,650. The '768 Patent also claims priority to provisional application No. 61/705,649, filed on September 26, 2012, and provisional application No. 62/219,249, filed on September 16, 2015. EX-1001, 1-2. For the purposes of this declaration, I have applied a priority date of September 26, 2012.

A. Specification

67. I have reviewed the patent specification along with the claims. The '768 Patent discloses a "method and structure to manufacture a glass substrate" and a "chip building a system on the glass substrate." *See* EX1001, 1:18-19. The glass substrate comprises "multiple metal conductors through in said glass substrate and multiple metal bumps are between said glass substrate and said display panel substrate, wherein said one of said metal conductors is connected to one of said contact pads through one of said metal bumps." *Id.*, Abstract. In certain embodiments, the invention may use polymer layers in addition to glass layers (see id., 6:18-24), or "the glass layer [ ] may be replaced with a polymer layer." *Id.*, 7:42-43. "When the polymer layer [is] cured to a solid state, then the polymer layer has a coefficient of expansion between 3 and 10 ppm/°C." *Id.*, 7:43-45.

B. Prosecution History

68. I have reviewed the prosecution history of the '768 Patent. EX-1002. Based on my review, I understand that the '768 Patent was filed as application No. 16/752,650 on January 26, 2020. It is a continuation of application No. 15/261,956, filed on September 11, 2016, now Patent No. 10,622,310, which is a continuation-in-part of application No. 14/036,256, filed on September 25, 2013, now Patent No. 9,615,453. The '768 Patent claims priority to provisional application No.

61/705,649, filed on September 26, 2012, and provisional application No. 62/219,249, filed on September 16, 2015.

69. As I reviewed the prosecution history, I have seen that that after several preliminary amendments, on February 21, 2020, the examiner issued a non-final rejection of all pending claims based on Gong (US 2013/0049217) in view of Lin (US 2009/0155959), along with several tertiary and quaternary references. EX1002 [File History], 254-271.

70. Further, I have also seen that on November 5, 2020, the applicant filed a response to the office action. The applicant significantly amended pending claims 21-40 and added new dependent claims 41-46. *Id.*, 411-420. On April 26, 2021, the examiner issued a notice of allowance. *Id.*, 444-451. The examiner found that the added limitations "are material to the inventive concept of the application in hand to forming a polymer interconnect with sufficient coefficient of expansion to enable holes and other features formed inside with improved chemical durability, strength and optical properties." *Id.*, 450.

71. As prosecution progressed, on May 25, 2021, the applicant submitted a request for continued examination, adding the limitation "wherein said first polymer layer has a thickness between 100 and 300 micrometers and has a coefficient of expansion between 3 and 10 ppml°C: wherein said first polymer

layer has a thickness between 100 and 300 micrometers and has a coefficient of expansion between 3 and 10 ppml°C" among other amendments. *Id.*, 487. On June 22, 2021, the examiner issued a notice of allowance, finding the claims allowable because "the closest prior art does not appear to disclose, alone or in combination, the limitations of material and structure of the chip package in combination with the other required elements of [independent] claim 21 or 31." *Id.*, 551.

72. Lastly, on June 24, 2021, the applicant submitted a second request for continued examination amending dependent claims 37 and 43. *Id.*, 590-597. On July 9, 2021, the examiner issued a notice of allowance. After an amendment after allowance to correct formal matters in the claims without changing their scope, the patent issued on August 31, 2021.

C. Claims of the '768 Patent

73. Claim 1 of the '768 patent recites a chip package whose elements, read together, describe a single integrated architecture: a low-expansion polymer core carrying copper through-conductors, planarized to a common plane so that a thin-film interconnection scheme can be fabricated across it, which scheme simultaneously receives a flip-chip semiconductor die through the die's thick-copper pad interconnect and routes the die's signals through the through-conductors to solderable, tin-containing bumps for the next assembly level. The

claim is properly understood as this combination, not as a collection of independent components.

74. The specification discloses this claimed architecture. For example, the claimed first polymer layer is substrate 20 (FIGS. 6a–6j, 7n) having a thickness of 100–300 micrometers. The polymer, when cured, has "a coefficient of expansion between 3 and 10 ppm/° C." ('768 patent, col. 7–8.) The first and second metal plugs are the copper plugs 21 formed from traces 6 molded through the polymer layer, the copper contacting the sidewall of the through via formed around it (FIGS. 6g–6j, 8a), with plug top surfaces rendered coplanar by planarization (FIG. 8b). The first interconnection scheme is the build-up structure of dielectric layers 24/32/40 and metal layers 26/28/34/36 (FIGS. 9a–9r), whose claimed tri-layer construction — a first metal layer, a third copper layer thereon, and a fourth copper layer thereon — corresponds to the adhesion/barrier layer 90, copper seed layer 92, and electroplated copper layer 94 of the damascene process (FIGS. 10h–10j), with the disclosed polymer dielectrics (polyimide, BCB, PBO, epoxy) supplying the second polymer layer. The first metal bump is bump 72, first type (FIGS. 9u–9v), whose solder layer 67 of tin-silver, tin-silver-copper, gold-tin, or tin-bismuth alloy is the claimed tin-containing layer, positioned over the interconnection scheme on the axis of the plug that carries the die's signal to it. The first semiconductor chip is

flip-chip die 46 (FIG. 9t; mounted on the opposite face of substrate 20 from bumps 72 per FIG. 9w, matching the claimed over/under orientation), whose claimed fourth metal interconnect is the specification's structure 50 on metal pad 48: an adhesion/barrier layer (the claimed second metal layer) and an electroplated copper layer of "between 5 and 30 micrometers" — verbatim the claimed range — connected to the third metal interconnect (metal layer 36) through openings 40a.

75. The interdependence of the elements confirms that the claim must be considered as a whole. The claimed invention resides in their combination, and the claim limitations take their meaning from other limitations: e.g., the core's 3–10 ppm/°C expansion coefficient is significant because a silicon die and copper-laden interconnection scheme are bonded across it, addressing the thermal-expansion-mismatch and solder-fatigue problem the specification itself identifies (col. 1–2); the plugs' coplanarity is significant because the micron-scale interconnection scheme must span both plugs at once; the scheme's barrier/seed/electroplate copper construction is the means of building fine-pitch wiring on that polymer surface; the tin-capped bump sits over the second plug because the plug is the die's conduit outward; and the die's 5–30 micrometer copper interconnect is the die-side counterpart that mates with the scheme. The specification presents the same interdependence as part of a fabrication sequence — forming the cored substrate

(FIG. 6), planarizing it (FIG. 8), building the interconnection scheme upon it (FIGS. 9a–9r), attaching the die to it (FIG. 9t), and bumping it (FIGS. 9u–9w).

IX. OVERVIEW OF THE ALLEGED PRIOR ART

A. Sundaram (EX1004)

76. Sundaram is directed to a 3D interconnect structure comprising an ultra-thin interposer having a plurality of ultra-high density through-via interconnections defined therein. EX1004, Abstract. Sundaram Figure 3 (relied on in the Petition) shows Sundaram's interconnect structure comprising an interposer defining a plurality of through vias.

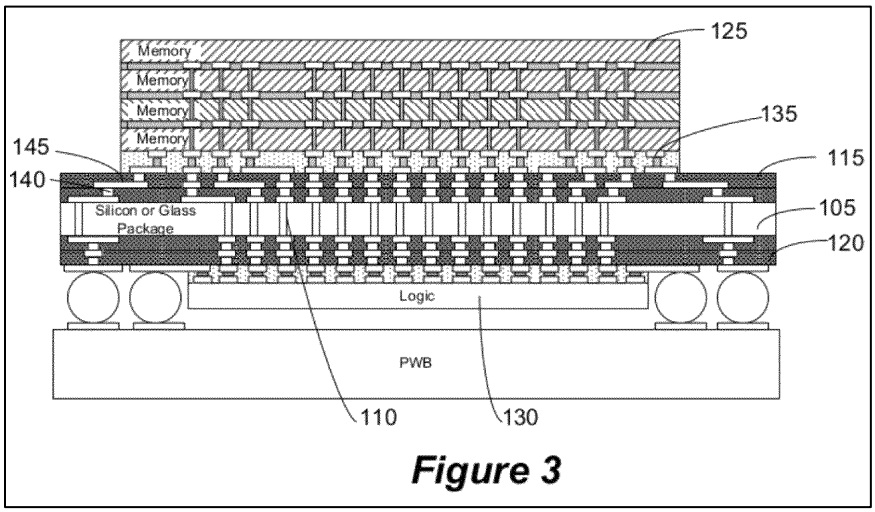


Figure 3

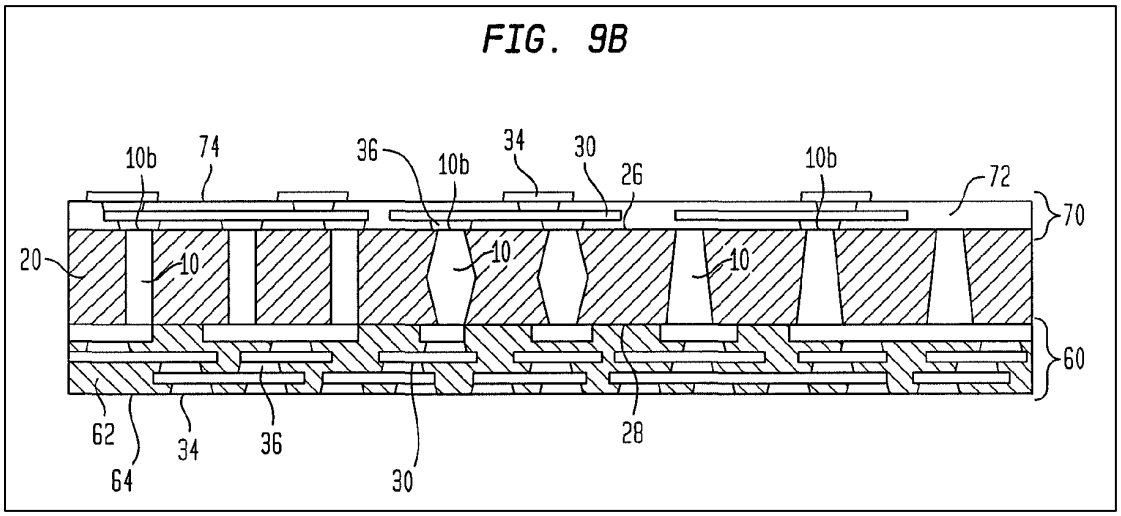
Id., Fig. 3. "[T]he interconnect structure comprises an interposer 105 having a first side 115 and a second side 120." *Id.*, 5:47-48. "A plurality of ultra-small through vias 110 can be defined within the interposer 105 such that each of the through vias 110 extends from the first side 115 to the second side 120 of the interposer 105." *Id.*,

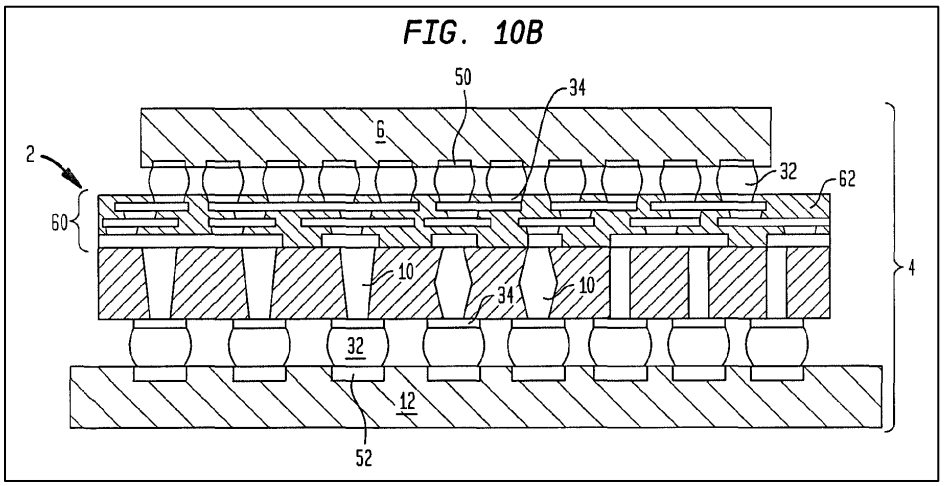
6:6-9. These "through vias 110 are ultra-small and can range from about 1-25 micrometers in diameter at about 3-50 micrometers in pitch." *Id.*, 6:11-13. "A first electronic device 125 can be attached to the first side 115 of the interposer 105 and a second electronic device 130 can be attached to the second side 120 of the interposer 105." *Id.*, 6:34-36. "[E]lectronic devices having different I/O pad layouts and sizes can also be connected through the use of blind vias 140 and conductor traces 145 defined within polymer-metal redistribution layers deposited on the first side 115 and second side 120 of the interposer 105." *Id.*, 6:62-67.

B. Haba (EX1009)

77. Haba discloses a method for making an interconnection component including forming a plurality of metal posts extending away from a reference surface. EX1009, Abstract. The Petition relies on Haba Fig. 9B and 10B.

FIG. 9B





Id., Figs. 9B, 10B. Haba Fig. 9B discloses "interconnection component 2 having a second redistribution layer 70 formed along surface 26" in addition to redistribution layer 60. *Id.*, 7:57-59.

78. Haba Fig. 10B is a "variation[ ] of a microelectronic reductions in solder bump sizes at the bonding interface to assembly respectively including interconnection components according to the embodiments of FIGS. 8 and 9A." *Id.*, 5:4-6. Fig. 10A discloses that "microelectronic element 6 has contacts 50 having a smaller pitch than the pitch of contacts 52 on printed circuit board ("PCB") 12." *Id.*, 7:45-47. "FIG. 10B is similar to that which is shown in 10A, except that pads 34 which overlie end surfaces 10B act as wettable contacts for attachment to contacts 52 of PCB 12 using solder balls 32." *Id.*, 7:53-56. Haba Fig. 10B lacks the second redistribution layer 70 of Fig. 9B.

C. Lin-191 (EX1005)

79. Lin-191 discloses "system-in packages" comprising multi-layer chips in a multi-layer polymer structure. EX1005, Abstract. Lin-191 explains that:

> System-in packages, or multichip modules, are described which can include multi-layer chips in a multi-layer polymer structure, on-chip metal bumps on the multi-layer chips, intra-chip metal bumps in the multi-layer polymer structure, and patterned metal layers in the multi-layer polymer structure. The multi-layer chips in the multi-layer polymer structure can be connected to each other or to an external circuit through the on-chip metal bumps, the intra-chip metal bumps and the patterned metal layers. The system-in packages can be connected to external circuits through solder bumps, meal bumps or wirebonded wires.

Id.

D. Yu (EX1010)

80. Yu discloses a package-on-package (POP) structure having at least one package comprising one die being disposed in a core material between first and second surfaces of the core material. EX1010, Title. The Petition relies primarily on Yu Figs. 16 and 52.

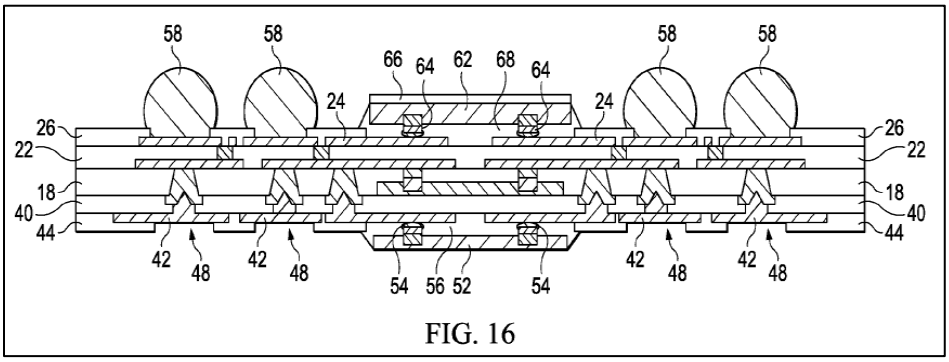


FIG. 16

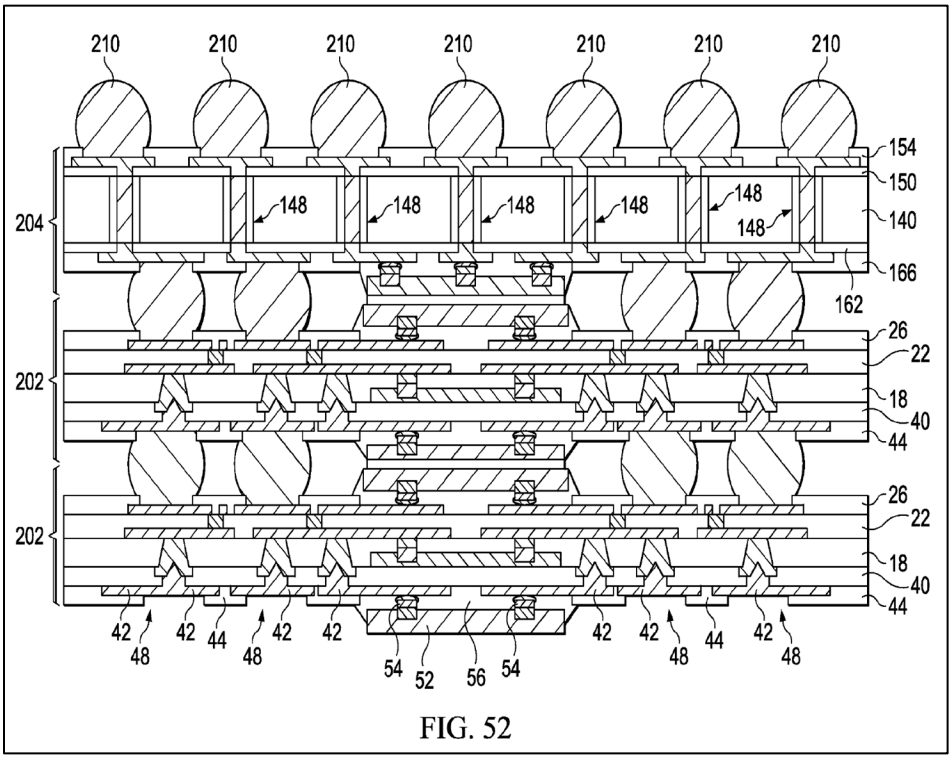


FIG. 52

Id., Figs. 16, 52. Yu provides limited discussion of these figures. Yu Fig. 16 is an "example of a second portion of a process for forming a package according to an embodiment." *Id.*, 1:65-67. Yu explains that "In FIG. 16, an underfill material 68, such as In FIG. 16, an underfill material 68, such as liquid epoxy, deformable gel, silicon rubber, the like, or a combination thereof, is dispensed and cured between the

third die 62 and the front side of the package, such as between the third die 62 and the second metallization layer 24." *Id.*, 4:67-5:4.

81. Yu Fig. 52 shows "step to form electrical connectors on the PoP structure of FIG. 51." *Id.*, 2:15-16. "In FIG. 52, connectors 210, such as BGA balls, formed coupled to a metallization layer on a front side of the interposer of the interposer package 204, similar to FIG. 50." *Id.*, 8:36-39.

X. CLAIMS

82. I understand that the '768 Patent has 2 independent claims (1 and 16) and 26 dependent claims. The claims are directed to chip packages using polymer layers with specific layouts of metal plugs and interconnects. Representative independent claim 1 is reproduced below.

Claim	Claim Language
1(Pre)	A chip package comprising:
1A	a first polymer layer having a first surface and a second surface opposite to said first surface , wherein said first surface is substantially parallel to said second surface , wherein said first polymer layer has a thickness between 100 and 300 micrometers and has a coefficient of expansion between 3 and 10 ppm / °C.;
1B	a first metal plug vertically in a first through via in said first polymer layer, wherein said first metal plug comprises a first copper layer, wherein the first copper layer contacts with a sidewall of said first through via;
1C	a second metal plug vertically in a second through via in said first polymer layer, wherein said second metal plug comprises a second

	copper layer, wherein a top surface of said second metal plug and a top surface of said first metal plug are in the same horizontal plane;
1D	a first interconnection scheme over said first surface, wherein said first interconnection scheme comprises a first metal interconnect over said first surface, a second metal interconnect over said first surface, a third metal interconnect over said first surface and a second polymer layer over said first, second and third metal interconnects, wherein said first metal interconnect is connected to said first metal plug, wherein said second metal interconnect is connected to said second metal plug, wherein said first metal interconnect comprises a first metal layer, a third copper layer on said first metal layer, and a fourth copper layer on said third copper layer;
1E	a first metal bump over said first interconnection scheme and said second metal plug, wherein said first metal bump comprises a tin-containing layer; and
1F	a first semiconductor chip under said first interconnection scheme, wherein said first semiconductor chip comprises a fourth metal interconnect on a first metal pad of said first semiconductor chip, wherein said fourth metal interconnect comprises a second metal layer on said first metal pad and a fifth copper layer over said second metal layer, wherein said fifth copper layer has a thickness between 5 and 30 micrometers, wherein said fourth metal interconnect is connected to said third metal interconnect.

XI. PETITIONERS FAIL TO DEMONSTRATE THAT ANY OF THE CHALLENGED CLAIMS ARE UNPATENTABLE

83. I have reviewed the Petition and understand that the Petition advances the following seven grounds:

Grounds	Claims Challenged	35 U.S.C. §	References
1A	1-15, 20	103	Sundaram (EX1004), Haba, (EX1009), and Lin-191 (EX1005)
1B	16-19, 21-28	103	Sundaram and Lin-191
2A	1-3, 5, 7-10, 14-15	103	Haba and Lin-191
2B	4, 6, 11-13,	103	Haba, Lin-191, and Sundaram
3A	16-17, 19, 22-28	103	Yu (EX1010) and Lin-191
3B	18, 21	103	Yu, Lin-191, and Camacho (EX1006)
3C	20	103	Yu, Lin-191, and Haba

A. Grounds 1A and 1B

84. Ground 1A relies on Sundaram, Haba and Lin-191, and challenges claims 1-15 and 20. Ground 1B relies on Sundaram and Lin-191 only, and challenges claims 16-19 and 21-28. Pet., 2.

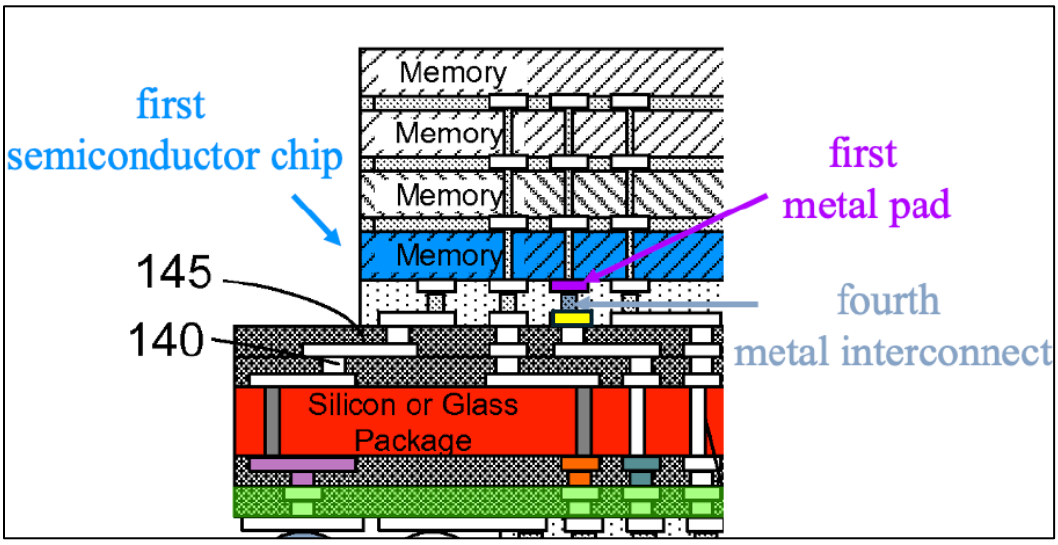
1. Sundaram and Lin-191 Fail to Teach or Suggest a "First Semiconductor Chip Comprises a Fourth Metal Interconnect" or "Fourth Metal Interconnect on a First Metal Pad of Said First Semiconductor Chip."

a. Sundaram's memory chip does not comprise a fourth metal interconnect or fourth metal interconnect on a first metal pad of said first semiconductor chip.

85. Limitation 1(f)(i) requires that the "first semiconductor chip comprises a fourth metal interconnect." EX1001 ['768 Patent], cl. 1. This

limitation is not disclosed by Sundaram because Sundaram' alleged semiconductor chip does not comprise or include Sundaram's alleged fourth metal interconnect.

86. Petitioners argue that Sundaram Fig. 3's "'die pads 135 [that are formed on the first 115 and second sides 120 of the interposer 105] can electrically connect devices using solder, copper bumps with solder caps, copper to copper bonding,' each of which teaches a fourth metal interconnect." Pet., 21. (citing EX1004, 6:29-33.). In particular, the Petition states that "[i]n FIG. 3, the fourth metal interconnect is a bump on die pad 135." Pet., 21. That is, as shown below, the Petition alleges that the solder/bumps (gray) (located on top of the die pad 135 (yellow) of interposer 105) is the claimed "fourth metal interconnect":



Pet., 21-22 (excerpting and annotating EX1004 [Sundaram] Fig. 3; I have added the yellow annotation showing die pad 135).

87. The structure the Petition identifies as the claimed "first semiconductor chip" (blue) does not comprise the alleged "fourth metal interconnect" (bump/solder shown in gray). This is because the bumps/solder (gray) are not part of the memory (blue) – the alleged "first semiconductor chip" (shown in blue).

88. Instead, the bumps (or solder) (the alleged "fourth metal interconnect") are formed *on the die pad 135 of the interposer 105* to electrically connect devices to the interposer 105. EX1004, 6:29-33. And Sundaram specifically states that the die pads 135 are associated *with the interposer 105*: "[t]he through vias 110 can be metalized in such a way that the metallization provides die pad surfaces 135 that correspond to each of the vias 110 on both the first side 115 and the second side 120 of the interposer 105." EX1004 [Sundaram], 6:23-25; *see also* EX1004, 6:29-33. Thus, Sundaram's bumps/solder are part of or associated with the interposer 105, not the alleged "first semiconductor chip."

89. Indeed, Haba (a reference on which Petitioners rely) demonstrates that solder/bumps (as described in Sundaram) are not considered part of the alleged "first semiconductor chip." Instead, solder/bumps (as described in Sundaram) are structures that are separate from a semiconductor chip and that are used to connect other components to contacts/pads of the semiconductor chip. EX1009 [Haba],

6:39-47 ("In the interconnection component of FIG. 8 end surfaces 10B can be wettable contacts *used to connect posts 10 to another component using solder balls or other conductive materials*. For example, in FIG. 10A, *end surfaces 10B are used to join posts 10 to solder balls 32, which are, in turn, joined to contacts 50 on a microelectronic element 6*. Other materials can be used in place of solder balls 32 to join features of the components of the assembly such as tin indium or a conductive matrix."); 7:42-56 ("As shown in FIGS. 10A and 10B, interconnect component 2 in either of the forms shown 9 and 10A, respectively, can be used to connect two components with respective contacts having different pitches or other different configurations. In the example shown in FIG. 10A microelectronic element 6 has contacts 50 having a smaller pitch than the pitch of contacts 52 on printed circuit board ("PCB") 12. Contacts 52 of PCB 12 are joined to end surfaces 10B, which act as wettable contacts therefor, and contacts 50 of microelectronic element 50 are joined to vias pads 34 of interconnection component 2, which is inverted with respect to the depiction of FIG. 8. The embodiment shown in FIG. 10B is similar to that which is shown in 10A, except that *pads 34 which overlie end surfaces 10B act as wettable contacts for attachment to contacts 52 of PCB 12 using solder balls 32*."); 8:27-29 ("For example, an interconnection component can be disposed on and connected to a PCB that includes an electrically conductive

EMI shield. The *end surfaces of the posts can then be solder bonded to contact pads of the PCB* with the EMI shield being ball-bonded to a peripheral trace of the interconnection component for grounding to the shield."); 11:33-35 ("Further, *circuit panel 96* can be of a similar structure to PCB having contacts 52 thereon, and *can connect to interconnection component 2 using solder balls 32 or the like*."). *See also* Section X.B.3 below.

90. Limitation 1(f)(i) requires "wherein said first semiconductor chip comprises a fourth metal interconnect on a first metal pad of said first semiconductor chip." EX1001 ['768 Patent], cl. 1. Based on Sundaram's disclosure, bump/solder (gray) is formed on a die pad 135 of the interposer 105 and, thus, is not on a metal pad of the semiconductor chip. The Petition identifies the "first metal pad" as the component shown in purple above and memory (blue) of electronic device 125 as the claimed "first semiconductor chip." Pet., 20. Sundaram (and the Petition) therefore places the alleged "fourth metal interconnect" on the interposer 105 and the alleged "first metal pad" on the alleged semiconductor chip. Thus, the alleged "fourth metal interconnect" is not on the alleged "first metal pad." The alleged "fourth metal interconnect" is on the die pad 135 (yellow) of the interposer 105. In addition, the "first semiconductor chip" does not comprise a fourth metal interconnect because the memory (the alleged

semiconductor chip) does not comprise the bump/solder (gray) (the alleged fourth metal interconnect) – the bump/solder (gray) is part of the interposer.

91. The mismatch described above – the alleged "fourth metal interconnect" on the interposer 105 and the alleged "first metal pad" on the alleged semiconductor chip – follows at least partially from the fact that Sundaram does not describe the pads or interconnects of electronic device 125. The Petition does not identify any disclosure of those structures and certainly does not explain the component shown in purple above or what it is made of. The Petition states instead that "[a] POSITA would understand that device 125 also has die pads such that an electrical connection is made between interposer 105 and device 125." Pet., 21. That is an assumption about what a device would have, not a teaching of Sundaram.

92. The Sundaram passage that the Petition relies on is directed to the interposer. Sundaram states that "[t]he die pads 135 that are formed on the first 115 and second sides 120 of the interposer 105 can electrically connect devices using solder, copper bumps with solder caps, copper to copper bonding, adhesive bonding, metallurgical bonding, non-conductive bonding, or combinations thereof." EX1004 [Sundaram], 6:29-33. That sentence lists methods for joining a device to the die pads *of the interposer*. It does not describe any structure formed

on electronic device 125 or the memory shown in blue above, and it does not describe the layered construction required by limitation 1(f)(ii).

93. The Petition's combination of Sundaram and Lin-191 fails because it does not teach or suggest the "first semiconductor chip comprises a fourth metal interconnect" or "fourth metal interconnect on a first metal pad of said first semiconductor chip."

b. Lin-191 does not teach or suggest limitation 1(f)(1).

94. Petitioners do not adequately allege that Lin-191 teaches or suggests the "first semiconductor chip comprises a fourth metal interconnect." EX1001 ['768 Patent], cl. 1. Although Petitioners include a section on Lin-191 for Ground 1A limitation 1(f)(1), the statements in that section are directed to the claimed "metal pad," not the claimed "fourth metal interconnect." Pet., 23-24. The section does not allege Lin-191 teaches or suggests the "first semiconductor chip comprises a fourth metal interconnect."

c. The Petition's motivation to combine Lin-191 and Sundaram is conclusory and wrong.

95. According to the Petitioners, there is a motivation to combine Lin-191 and Sundaram because the modification "is the application of a known technique (metal pads) to a known device (Sundaram's semiconductor chip having die pads) ready for improvement to yield the predictable result of Sundaram's device 125

having a first metal pad." Pet. 24. This statement offers no substantive explanation as to why the structure (shown in purple above) required the application of the Lin-191's metal pad teachings. It presupposes that one would modify Sundaram without identifying any issues, shortcomings, or reasons to combine the references.

96. Sundaram and Lin-191 reflect fundamentally different engineering approaches to building a multi-chip structure, and a POSITA would not have been motivated to merge them. Lin-191 teaches a chip-first, tier-by-tier build in which the substrate is a work-in-progress rather than a finished component: chips carrying on-chip metal bumps are adhered to the substrate, encapsulated, and then polished or ground to expose the bumps before interconnections are formed, with the sequence repeated for each successive tier. EX1005, ¶[0009]. Consistent with that approach, Lin-191 does not form its through-substrate connections until late in the process — substrate 110 is first thinned to as little as 1 to 10 micrometers by mechanical grinding or chemical-mechanical polishing of its backside, EX1005, ¶[0290], and only then are through holes 16 and through-hole connections 17 formed from that newly exposed surface. EX1005, ¶¶[0292]–[0293]. Sundaram proceeds in the opposite order and for the opposite reason. Sundaram builds and electrically verifies its interposer *before* any die is attached, and describes this chip-last sequence as the mechanism by which its structure "alleviates the Known

Good Die (KGD) concerns in 3DIC integration." EX1004, 7:51-53, FIG. 6 (steps 605, 610, 615). Sundaram's claims reinforce that its interposer is meant to be a completed, verifiable article, requiring test pads on both sides to permit testing of devices attached to either side. EX1004, cl. 21–22. A POSITA seeking the benefits Sundaram describes would have understood that those benefits depend on the interposer being finished and tested before die attachment, and would therefore have seen no advantage in placing that interposer into Lin-191's process, where the substrate is deliberately left unfinished and is subsequently thinned, ground, and metallized from the backside after the chips are already in place. The features a POSITA would have been looking to Sundaram for — its through-vias, its redistribution layers, and its test pads — are the same features Lin-191's later processing steps would have been expected to disturb. A POSITA would not have expected the combined arrangement to retain them or to function as Sundaram describes. Conversely, a POSITA starting from Lin-191 and reordering its process to preserve Sundaram's pre-tested interposer would have had to abandon the tiered, chip-first integration that Lin-191 identifies as its contribution, including the high routing density between chips that Lin-191 attributes to its fine-pitched on-chip and intra-chip metal bumps. EX1005, ¶¶[0010]–[0011]. A POSITA would not have had a reason to make either change, nor a reasonable expectation that the

resulting structure would work as either reference intends. In my view, there is no evidence that a POSITA would have a reason to combine the references.

2. Sundaram and Lin-191 Do Not Teach "Wherein Said Fourth Metal Interconnect Comprises a Second Metal Layer on Said First Metal Pad and a Fifth Copper Layer Over Said Second Metal Layer, Wherein Said Fifth Copper Layer Has a Thickness Between 5 and 30 Micrometers."

97. The Petition relies solely on Lin-191 for limitation 1(f)(ii). Pet., 24-25. In my view, as discussed below, Lin-191 does not teach this limitation.

a. Lin-191 does not teach or suggest "said fourth metal interconnect."

98. As discussed above, the Petition fails to demonstrate that Sundaram teaches a "first semiconductor chip compris[ing] a fourth metal interconnect" because Sundaram's memory chip does not comprise the solder/bumps alleged to be the claimed "said fourth metal interconnect."

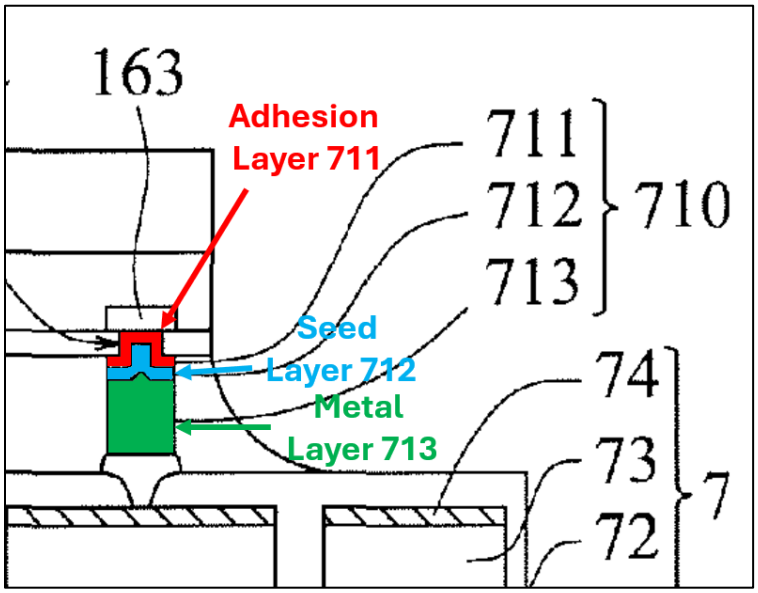
99. Although the Petition alleges Lin-191's bumps 710 are metal interconnects for limitation 1(f)(ii) (Pet., 24-25), the Petition does not rely on Lin-191 as teaching or suggesting that Sundaram's first semiconductor chip comprises the claimed fourth metal interconnect, cl. 1(f)(i). *Id.* The Petition's treatment of Lin-191 for limitation 1(f)(i) is directed to the claimed "metal pad," stating only that "Lin-191 teaches a semiconductor chip 160 with 'metal traces or pads 163'

that include 'aluminum.'" Pet., 23-24. Lin-191 therefore does not remedy the deficiency in Sundaram that I have identified above.

b. Lin-191 does not teach or suggest "a second metal layer on said first metal pad and a fifth copper layer over said second metal layer."

100. The Petition's mapping of limitation 1(f)(ii) is inconsistent with the Petition's own mapping of limitation 1(d)(iii). Claim 1 recites a three-layer interconnect in limitation 1(d)(iii) and a two-layer interconnect in limitation 1(f)(ii). Petitioners assert that Lin-191's adhesion layer and seed layer are *two* *separate* layers for limitation 1(d)(iii). But, when it comes to limitation 1(f)(ii), Petitioners asserts that the adhesion layer and seed layer are *one* layer. Those two positions cannot both be correct.

101. The Petition errs in its assertions that "the combination of layers 711 and 712 [in Lin-191 Fig. 72] is a second metal layer on metal pad 163." Pet., 25 (emphasis in original). In other words, in view of Lin-191's configuration, the Petition errs in asserts that two layers 711 and 712 are one layer – "a second metal layer." Based on Petitioners' own position regarding limitation 1(d)(iii), adhesion layer 711 and seed layer 712 in Lin-191 Fig. 72 are two different layers, not one layer.



EX1005 [Lin-191], Fig. 72 (excerpted and annotated), [0389] ("metal layer 713 under the seed layer 712 and over the solder joints 720."); ("a seed layer 712 under the adhesion layer 711"). The Petitioners specifically identified an adhesion layer and a seed layer as separate layers in analyzing 1(d)(iii). (Pet. 15).

102. Notably, Petitioners combine layers 711 and 712 because the claim language requires that a second metal layer is on the first metal pad and that a copper layer is over the second metal layer. The alleged first metal pad is metal pad 163. Adhesive layer 711 is on the metal pad 163 and the alleged copper layer 713 is over seed layer 712, not the adhesive layer 711. Thus, if layers 711 and 712 are not one layer, under Petitioners' apparent view, the claim limitation is not met. But, according to Petitioner's own admission, layers 711 and 712 are not the same

layer. Thus, Lin-191 fails to disclose "a second metal layer on said first metal pad and a fifth copper layer over said second metal layer."

103. In view of Lin-191's configuration and Petitioners' admission, a POSITA would not consider Lin-191's adhesion layer 711 and seed layer 712 to be a single layer. Lin-191 does not refer to adhesion layer 711 and seed layer 712 as a single layer. EX1005 [Lin-191], [0389]-[0400]. Instead, adhesion layer 711 and seed layer 712 are two different layers made of different materials serving different purposes. EX1005 [Lin-191], [0389] ("a seed layer 712 under the adhesion layer 711"), Fig. 72 (excerpted and annotated). A POSITA would understand an adhesion layer as a layer made to allow materials that are not compatible (in adhesion) to adhere to one another. This is a common occurrence in microfabrication where dissimilar materials are deposited on one another. An example is copper deposited on aluminum pads. *Id*., [0059]. For example, Lin-191 explains that adhesion layer 711 is made of "titanium, a titanium-tungsten alloy, titanium nitride, chromium, tantalum, tantalum nitride, nickel or nickel vanadium" and has a thickness of "less than 1 micrometer, such as between 1 nanometer and 0.5 micrometers." EX1005 [Lin-191], [0390]. Conversely, Lin-191 explains that seed layer 712 is made of different materials ("copper, silver, gold, nickel or titanium-copper alloy") having a different thickness ("less than 1 micrometer, such

as between 10 nanometers and 0.8 micrometers."). *Id.* Thus, according to Lin-191's configuration, a seed layer is used for a starting layer for electroplating. *Id*., [0058].

104. The materials that Lin-191 specifies for an adhesion layer 711 are metals and compounds selected for adhesion and diffusion barrier performance rather than for conductivity. EX1005 [Lin-191], [0390]. Lin-191 uses these materials because, for example, copper does not adhere well to, and can diffuse into, the underlying dielectric or pad material.

105. The separate seed layer in Lin-191 is present for a different reason. Electroplating requires a continuous conductive surface from which the plated metal can nucleate and grow, and the seed layer supplies that surface. This is why Lin-191 specifies seed layer 712 as "copper, silver, gold, nickel or titanium-copper alloy" — metals selected for their compatibility with the metal to be plated. EX1005 [Lin-191], [0390]. The materials Lin-191 specifies for the adhesion layer would not serve as a plating seed, and the copper and noble metals it specifies for the seed layer would not provide the adhesion and barrier function.

106. Petitioners combination of adhesion layer 711 and seed layer 712 into a single layer is inconsistent with Petitioners' own arguments elsewhere in the Petition where Petitioners assert that an adhesion layer and seed layer constitute

two different layers. For example, limitation 1(d)(iii) requires "said first metal interconnect comprises a first metal layer, a third copper layer on said first metal layer, and a fourth copper layer on said third copper layer." EX1001 ['768 Patent], cl. 1. Petitioners rely on Lin-191 Fig. 22's adhesion layer 31 as the claimed "first metal layer" and seed layer 32 as the claimed "third copper layer." Pet., 15. Thus, Petitioners asserts that Lin-191 discloses adhesion layers and seed layers as separate layers and accordingly maps them to different claimed layers. Petitioners' attempt to combine separate adhesion layers and seed layers for limitation 1(f)(ii) is not consistent with Petitioners' other mapping.

107. The Petition also treats Lin-191's adhesion, seed, and metal layers as three separate claimed layers elsewhere in Ground 1A, and does so using the same Figure 72 on which it relies for limitation 1(f)(ii). For element 7(c), the Petition states that Lin-191 "teaches a multilayered metal interconnect with two copper layers and a metal layer, i.e., a 'patterned metal layer 7' having 'adhesion layer 71, the seed layer 72,' and 'metal layer 73.'" Pet., 44 (citing EX1005 [Lin-191], [0379]).

108. The Petition then maps each of those layers to a separate claimed layer: "Adhesion layer 71 is a metal (e.g., titanium or nickel) and is thus a third metal layer. Seed layer 72 is 'a copper layer' on adhesion layer 71, i.e., a sixth

copper layer on said third metal layer. Metal layer 73 is 'a copper layer…on the seed layer 72,' i.e., a seventh copper layer on said sixth copper layer." Pet., 44.

109. I also note that the Petition elsewhere describes this construction as "Lin-191's three-metal layer interconnect" and as "Lin-191's three-layer metal interconnect." Pet., 130. Based on Petitioners' own statements, a POSITA would understand Lin-191's adhesion layer, seed layer, and metal layer to be three layers, and would not understand an adhesion layer and a seed layer together to be a single layer.

110. Petitioners' position that "the combination of layers 711 and 712 is a second metal layer on metal pad 163" (Pet., 25) merges what Petitioners identify as two distinct layers into one claimed layer, which is inconsistent with Petitioners' own mapping of limitation 1(d)(iii).

111. For these reasons, the structure of the chip package claimed at '768 patent claim 1 is different than the structure of the semiconductors described in Lin-191. Because of this, the Petition fails to map Lin-191 to limitation 1(f)(ii). Because neither Sundaram nor Lin-191 teaches or suggests limitation 1(f)(ii), the Petition fails to prove that claim 1 (or the claims depending therefrom) are unpatentable.

3. There is No Motivation to Combine Sundaram and Lin-191.

112. The Petition advances a separate motivation to combine for limitation 1(f)(ii), distinct from the motivation it advances for limitation 1(f)(i). Pet., 26. The Petition asserts that "Lin-191's metal bump provides improved metallurgical bonding and increased resistance to fatigue and stress-induced failure by employing a layered structure," and that the configuration "would reduce the risk of intermetallic formation at critical interfaces, mitigate electromigration, and better absorb mechanical strain during thermal cycling." *Id.* (citing EX1003 [Shanfield Decl.], ¶¶189-191).

113. I have reviewed Lin-191 and have not located any statement that demonstrates to a POSITA that Lin-191's adhesion layer 711 and seed layer 712 provide increased resistance to fatigue or stress-induced failure, reduced intermetallic formation, mitigation of electromigration, or improved absorption of mechanical strain during thermal cycling. Lin-191 describes those layers structurally and by material and thickness, and does not attribute the asserted advantages to them. EX1005 [Lin-191], [0389]-[0400].

114. Petitioners' asserted motivation also presupposes a bump structure in Sundaram to be modified. The Petition describes the combination as "modify[ing] Sundaram's bump per Lin-191's layered bump teachings." Pet., 26. As discussed

above, Sundaram does not describe the construction of any bump on electronic device 125. A POSITA could not modify a structure that the reference does not describe, and the Petition does not explain what would be modified.

115. A POSITA would not be motivated to combine Sundaram and Lin-191. The Petition has not shown that a POSITA would have looked to Lin-191's adhesion-layer/seed-layer/electroplated-layer bump structure to modify the bump on die pad 135 of Sundaram. A POSITA would have known that an adhesion or diffusion-barrier layer, such as the titanium or nickel adhesion layer 711 that Lin-191 describes, is needed only in particular circumstances, for example: where copper would otherwise diffuse into an adjacent, dissimilar metal; where copper would otherwise diffuse into an oxide or other inorganic dielectric; or where copper does not otherwise bond adequately to the material beneath it. The Petition does not show that any of these circumstances exists in Sundaram.

116. The Petition's own description of this combination confirms that Sundaram's own bump is copper. The Petition states that Lin-191's bumps 710, "like Sundaram's copper bumps, are metal interconnect[s]." Pet., 25; EX1003 [Shanfield Decl.], ¶186. The Petition's stated motivation for adding Lin-191's layered structure is that it would provide "improved metallurgical bonding and increased resistance to fatigue and stress-induced failure," would "reduce the risk

of intermetallic formation at critical interfaces," and would "mitigate electromigration" and "better absorb mechanical strain during thermal cycling." Pet., 26; EX1003 [Shanfield Decl.], ¶¶188-191. This rationale does not identify any specific diffusion, oxide, or adhesion problem with Sundaram's own copper bump on die pad 135 that Lin-191's layers would remedy. Moreover, electronic device 125 is not described structurally at all, because Sundaram pertains to the interposer not the electronic device 125.

117. Sundaram's own disclosure indicates that no such problem exists at die pad 135. Sundaram states that the through vias forming die pad 135 "can be metalized with a highly-conductive metal, for example copper," and "can also be metalized with a polymer liner or a metal seeding liner." EX1004 [Sundaram], 6:22-29. Sundaram identifies these as its metallization options for die pad 135 and the vias beneath it, and none of them includes a separate adhesion or diffusion-barrier metal layer such as titanium or nickel.

118. Sundaram confirms that when such a barrier layer is needed, die pad 135 is not an instance of it. In describing an alternative single-crystal-silicon-interposer embodiment, Sundaram describes forming "about 30 nanometer (nm) Ti (barrier for Cu diffusion into SiO2) and about 1 um thick copper seed layer" on a silicon wafer coated with a "SiO2 dielectric isolation layer." EX1004 [Sundaram],

14:58-66. Sundaram states that this titanium layer is a "barrier for Cu diffusion into SiO2" — that is, a layer used specifically to prevent copper from diffusing into an inorganic oxide dielectric. *Id.* Sundaram further states that its "novel polymer liner approach is presented to replace the current combination of SiO2 and diffusion barriers used in the processing of CMOS-based silicon interposers." *Id.* This confirms that Sundaram ties the need for a titanium diffusion barrier to a specific combination — copper deposited on an SiO2 dielectric in a silicon interposer — and presents its own polymer-based approach as an alternative that avoids that combination.

119. Die pad 135 belongs to interposer 105, Sundaram's glass-and-polymer interposer, not the alternative single-crystal silicon interposer in which Sundaram describes using a titanium barrier against SiO_2. The Petition has not shown that copper at die pad 135 would diffuse into an adjacent dissimilar metal, would diffuse into an oxide or other inorganic dielectric, or would not otherwise bond adequately to the material beneath it. Absent such a showing, a POSITA would not have understood Lin-191's adhesion-layer teaching to apply to die pad 135's bump, and the Petition's generic reliability rationale does not establish that a POSITA would have been motivated to add it.

4. Sundaram Does Not Teach or Suggest a Polymer Interposer Having the Claimed Thickness.

120. Independent claims 1 and 16 of the '768 patent recite a "first polymer layer" having "a thickness between 100 and 300 micrometers." EX1001 ('768 Patent), cls. 1(a)(ii), 16(a)(ii). Sundaram provides a POSITA with no basis to select a polymer interposer having a thickness between 100 and 300 micrometers.

121. Sundaram describes the thickness of interposer 105 without reference to any material. Sundaram states that "the interposer being about 20 to about 200 micrometers in thickness," interposer 105 "is ultra-thin and is less than about 100 micrometers in thickness," that "[i]n exemplary embodiments, the interposer 105 is less than about 800 micrometers in thickness, and more specifically about 20-100 micrometers in thickness," and that "[i]n preferred embodiments, the interposer is about 30 micrometers in thickness." EX1004, 2:22-25, 5:48-54. Sundaram identifies candidate materials, stating that interposer 105 "can be made of many substrate materials, for example, glass, silicon, ceramic, polymer-glass laminates, and flexible polymers." *Id.*, 5:54-58. But Sundaram does not tie any of these thickness values to a polymer interposer. Indeed, the sole material Sundaram identifies as preferred, and the only one to which it attributes the advantages it seeks, is glass, not polymer. *Id.*, 5:58-67. With regard to 14:34-36, this passage

appears under the heading "Single Crystal Silicon Interposer Examples." The passages describes a *single crystal silicon* interposer, not a polymer interposer. EX1004 [Sundaram], 14:6-10.

122. [Intentionally omitted].

123. Therefore, the passages the Petition cites do not describe interposer 105, and Sundaram does not attribute any thickness to a polymer interposer. The Petition has not identified a disclosure in Sundaram of a polymer interposer having a thickness between 100 and 300 micrometers.

5. The Petition's Rationale for Combining Sundaram, and Haba for Limitation 1(a)(iii) Fails.

124. Independent claim 1 of the '768 patent recites a "first polymer layer" having "a coefficient of expansion between 3 and 10 ppm/°C." EX1001 ['768 Patent], 1(a)(iii). Dependent claim 20 contains the same limitation. The Petition relies on Haba (EX1009) alone for this limitation because Haba discloses a polymer having a CTE of "in the range of 8 parts per million per degree Celsius." Pet., 7, 58; EX1009 [Haba], 5:55-59.

125. The Petition's motivation to combine Haba's polymer with Sundaram is that "a POSITA would have found it advantageous to modify Sundaram's interposer 105 to have a low CTE to likewise reduce the difference in CTE between interposer 105 and Sundaram's electronic devices (chips) 125, 130." Pet.,

7-8. Sundaram identifies specific materials for use in Sundaram's architecture. The materials Sundaram identifies as having a coefficient of expansion within the claimed range of 3 to 10 ppm/°C, however, are glasses, not polymers.

TABLE 1

	Young's Modulus (GPA)	Poisson's Ratio	CTE (ppm/° C.)	Stress free Temp. (° C.)
Glass 1	77	0.22	3.8	25
Glass 2	71	0.24	8.5	25
Polymer 1	1.83	0.3	67	232
Polymer 2	6.9	0.3	31	120
Copper	121	0.3	17.3	25

EX1004 [Sundaram], 8:61-62 (showing CTEs for glass of 3.8 and 8.5 ppm/°C.)

126. I have reviewed the Petition's reliance on Sundaram's teaching that a "silicon-matched" coefficient of thermal expansion is advantageous for an interposer. Pet., 8 (citing EX1004 [Sundaram], 2:4-6). Sundaram makes that statement about glass, not polymers. Sundaram states that "[g]lass presents several advantages, namely, silicon-matched coefficient of thermal expansions (CTE), excellent surface flatness, dimensional stability, high electrical resistivity, and thin and large panel availability." EX1004 [Sundaram], 5:62-67. Sundaram does not attribute a silicon-matched coefficient of thermal expansion to any polymer.

127. The polymers Sundaram itself discloses do not have coefficients of expansion within the claimed range. With regard to polymers, the materials table in

Sundaram reports coefficients of thermal expansion of 31 and 67 ppm/°C – substantially above the claimed range of 3 to 10 ppm/°C. EX1004 [Sundaram], 8:61-62. A POSITA following Sundaram's teaching that a silicon-matched coefficient of expansion is advantageous would select one of the materials Sundaram identifies as having that property, and Sundaram identifies none of its polymers as having it.

128. I have reviewed the Petition's reliance on Haba's dielectric layer 20 as "a polymeric dielectric" having a coefficient of thermal expansion "in the range of 8 parts per million per degree Celsius." Pet., 7 (citing EX1009 [Haba], 5:41-44, 5:55-59). Haba's dielectric layer 20 is not an ordinary polymer. Haba describes it as a material selected for low thermal expansion and identifies candidates including "low temperature co-fired ceramic, liquid crystal polymer, glass, and high filler-content epoxy." EX1009 [Haba], cl. 5. Achieving a coefficient of expansion of 8 ppm/°C or lower in a polymer requires a specifically engineered material, such as a liquid crystal polymer or a highly filled epoxy, and is not a property of polymers generally. Rogers 3000 ultram product, for example, is a liquid crytsal polymer with at CTE of 17-150 ppm/°C. EX2022.

129. The Petition therefore does not propose using a material that Sundaram discloses. It proposes replacing the interposer material of Sundaram

with a different, specifically engineered polymer to be used in the specific configuration of Haba. The Petition does not explain why a POSITA seeking a silicon-matched coefficient of expansion would take that path rather than use one of the glasses that Sundaram identifies as already having that property.

130. The modification the Petition proposes would not accomplish the purpose the Petition gives for it. The Petition states that "a POSITA would have found it advantageous to modify Sundaram's interposer 105 to have a low CTE to likewise reduce the difference in CTE between interposer 105 and Sundaram's electronic devices (chips) 125, 130." Pet., 7-8. The relevant comparison is therefore between the coefficient of expansion of the interposer material and that of the semiconductor chips mounted to it.

131. Sundaram's electronic devices 125 and 130 are integrated circuit devices, which a POSITA would understand to be formed in silicon. EX1004 [Sundaram], 6:37-39 (describing device 125 as "single or stacked memory IC devices" and device 130 as "a logic IC device or devices"). A POSITA would understand silicon to have a coefficient of thermal expansion of approximately 2.6 to 3.0 ppm/°C. *See* EX2021.

132. Replacing Sundaram's preferred glass with a material of the kind Haba describes would increase, not reduce, that difference. Sundaram reports a

coefficient of thermal expansion of 3.8 ppm/°C for one of the two glasses in its materials table. EX1004 [Sundaram], 8:61-62, Table 1. That value is within approximately 1 ppm/°C of silicon, which is what Sundaram means when it states that glass presents the advantage of "silicon-matched coefficient of thermal expansions (CTE)." *Id.*, 5:62-67. The Petition characterizes Haba's dielectric layer 20 as having a coefficient of thermal expansion "in the range of 8 parts per million per degree Celsius." Pet., 7. A material at approximately 8 ppm/°C differs from silicon by approximately 5 ppm/°C, which is roughly five times the difference presented by Sundaram's 3.8 ppm/°C glass.

133. Using Haba's polymer in Sundaram's interposer would also place the interposer outside the range of materials Sundaram specifies. Sundaram states that "the interposer 105 is made of glass or any other substrate with a thermal conductivity as low as about 5 W/mK or as high as about 125 W/mK, or higher, as in the case of silicon." EX1004 [Sundaram], 5: 58-62. A POSITA would understand that statement to set a lower bound of approximately 5 W/mK on the thermal conductivity of the interposer material.

134. The polymers Haba identifies do not meet that lower bound. Haba identifies its dielectric layer as capable of being formed from "low temperature co-fired ceramic, liquid crystal polymer, glass, and high filler-content epoxy," and the

Petition relies on Haba's description of the layer as "a polymeric dielectric." EX1009 [Haba], cl. 5, 5:41-44; Pet., 7. Liquid crystal polymers and filled epoxies of the kind Haba describes have thermal conductivities substantially below 5 W/mK. For example, materials that I have worked with, including Roger's liquid crystal polymer have thermal coefficient of 0.2W/mK. *See* EX2022.

135. Thermal performance is not incidental to Sundaram's structure. Sundaram states that its vias "are electrically and thermally conducting, and are distributed within the interposer such that they provide localized thermal isolation or thermal conduction between the first and second electronic devices," and Sundaram devotes figures to "a thermally managed interconnect structure of the present invention for both a low and high power logic component." EX1004 [Sundaram], 6:19-22 (describing FIGS. 30 and 31). Sundaram also lists "thermal manageable" among the properties of its structure. *Id.*, 2: 15-18. A POSITA would not have selected an interposer material falling below the thermal conductivity range Sundaram specifies, because doing so would compromise a function Sundaram treats as central to its design.

136. The Petition therefore has not shown that its proposed modification would reduce the difference in coefficient of expansion between the interposer and the chips. Measured against Sundaram's preferred glass, the modification makes

that difference larger. A POSITA seeking to reduce the difference in coefficient of expansion between the interposer and the chips would retain Sundaram's glass rather than replace it with Haba's dielectric material.

137. Haba's low coefficient of expansion dielectric cannot be separated from the process by which Haba forms it or from the geometry that process requires. Haba forms its posts first and then molds the dielectric around them. Haba states that "posts 10 can be formed on rigid metal layer 4" by plating or by "etching posts 10 from a solid layer of metal 6," and that thereafter "dielectric layer 20 is formed over edge surfaces 14 of posts 10 … [i]n the molding process, [where] a flowable composition is introduced in the desired locations and cured to form the dielectric layer." EX1009 [Haba], 9:9-10, 9:17, 9:29-33.

138. Haba describes that molding step in terms of fluid flow. Haba states that "[t]he molding composition can be injected through at least one opening, or gate, in the counter element," and that "[s]lots can further be used as escape passages for trapped air, and can also vent excess material of the molding composition." *Id.*, 9:44-46. A POSITA would understand that a process of this kind requires spaces between the features being encapsulated that are large enough for a viscous composition to flow through and for displaced air to escape, and that the achievable feature size and spacing are limited accordingly.

139. Haba's disclosed geometry reflects those limits. Haba describes the end surfaces of its posts as "generally selected in a range from about 50 to 1000 μm, for example, 200-300 μm," arranged "in one or more grid-like patterns having a pitch in a range from 100 to 10000 μm (e.g., 400-650 μm)." EX1009 [Haba], 5: 22-38. Haba's dielectric layer thickness is also set by that geometry, because the molded layer is formed with "a surface 26 coplanar with end surfaces 10B of the posts" and "a surface 28 … coplanar with end surfaces 10A of the posts 10." *Id.*, 9: 10:8-13. A POSITA would understand the thickness of Haba's dielectric layer and the height of Haba's posts to be the same dimension.

140. Sundaram forms its interconnections in the opposite way, and at a far finer scale. Sundaram's through vias 110 are formed into a solid substrate and then metalized: the through vias "can be metalized with a highly-conductive metal, for example copper," and "can also be metalized with a polymer liner or a metal seeding liner." EX1004 [Sundaram], 6:25-29. Sundaram describes forming those vias by laser ablation, reporting "excimer laser via formation on ultrathin glass substrates" and a mask projection technique by which "[m]ore than one thousand uniform vias at a pitch of 30 μm were obtained simultaneously in one laser ablation process." *Id.*, 9:8-36.

141. That process is what permits Sundaram's interconnect density. Sundaram states that its "through vias 110 are ultra-small and can range from about 1-25 micrometers in diameter at about 3-50 micrometers in pitch," and that in exemplary embodiments they are "about 1-20 micrometers in diameter at about 3-40 micrometers in pitch." EX1004 [Sundaram], 6:11-15. Haba's posts are roughly an order of magnitude larger in both dimensions than Sundaram's vias: Haba's example post end surfaces of 200-300 micrometers at a pitch of 400-650 micrometers compare with Sundaram's example vias of 1-20 micrometers at a pitch of 3-40 micrometers.

142. Sundaram's stated advantage depends on that density. Sundaram states that the interposer "has the same or substantially the same through-via interconnect density as the first and second electronic devices it connects," and that this "enables the first 125 and second 130 electronic devices to communicate at bandwidth speeds of at least about 10 GB/s." EX1004 [Sundaram], 6:50-53. Sundaram further identifies coarse-pitch carriers as the problem its structure is meant to solve, explaining that "organic, ceramic, and glass carriers having conductive through vias have been described in prior art, however, they do not operate at high bandwidths because of coarse pitch and long interconnections." *Id.*, 2:6-9.

143. A POSITA therefore would not have looked to Haba's molded dielectric layer as a material for Sundaram's interposer 105. Haba's dielectric is a molded encapsulant formed around a coarse grid of pre-formed posts, and its material, its thickness, and its feature spacing are products of that process. Sundaram's interposer is a solid substrate into which ultra-small vias are ablated at a pitch roughly an order of magnitude finer than disclosed in Haba. Adopting Haba's molded dielectric approach in Sundaram would sacrifice the through-via density on which Sundaram's stated bandwidth advantage depends, and would produce the coarse-pitch carrier that Sundaram identifies as deficient in the prior art.

144. Sundaram does more than describe a finer geometry than Haba. It identifies structures of Haba's kind as the deficiency its invention is meant to overcome. In its discussion of the prior art, Sundaram states that "organic, ceramic, and glass carriers having conductive through vias have been described in prior art, however, they do not operate at high bandwidths because of coarse pitch and long interconnections." EX1004 [Sundaram], 2:6-9. Sundaram then states that its own structure "achieves the same ultra high density of interconnections at ultra short lengths, very similar to TSVs within the logic and memory devices." *Id.*

145. Haba's interconnection component is a carrier of the kind Sundaram criticizes. Haba's conductive elements are posts with end surfaces of "about 50 to 1000 μm, for example, 200-300 μm," arranged at "a pitch in a range from 100 to 10000 μm (e.g., 400-650 μm)." EX1009 [Haba], 5: 30-38. A POSITA would characterize that geometry as coarse pitch, and would recognize it as the arrangement Sundaram states does "not operate at high bandwidths."

146. A POSITA reading Sundaram would therefore be discouraged from adopting Haba's approach in Sundaram's interposer. Sundaram's stated purpose is to achieve through-via density comparable to that of the chips it connects, and it identifies coarse pitch as the reason prior art carriers fail to do so. Sundaram directs a POSITA away from the structure the Petition proposes to import.

6. Sundaram Does Not Support the Petition's Motivation to Combine for Claim 2's "Passive Component … Over Said First Interconnection Scheme."

147. Claim 2 requires "a passive component over said first interconnection scheme and connected to said first interconnection scheme through a solder layer." EX1001 ['768 Patent], cl. 2. The Petition relies on Sundaram's FIG. 33 for the proposition that a passive component can be connected to an interposer's redistribution layer through a solder-based connection. Pet., 28-30. The Petition then proposes relocating that passive component into the FIG. 3 embodiment relied

on for the remaining limitations of claim 1. *Id*.; EX1003 [Shanfield Decl.], ¶¶197-199.

148. The Petition states that "[b]ased on the FIG. 33 embodiment, a POSITA would have found it obvious and been motivated to modify Sundaram's chip package to comprise a passive component over the first interconnection scheme and connected to a metal interconnect through a solder layer," and that "[i]n the combination, the passive component is positioned adjacent to FIG. 3's second electronic device 130, therefore over the first interconnection scheme." Pet., 29-30; EX1003 [Shanfield Decl.], ¶¶199-200.

149. Sundaram's FIG. 33 does not support that placement. FIG. 33 depicts a glass core with an image sensor chip and associated test-pads and micro-bumps-and-RDL structure on one side, and an "ASIC or Other IC" on the opposite side, with BGA solder balls formed beneath the ASIC for connection to the next-level board. EX1004 [Sundaram], Fig. 33; 6:42-45 (describing "an image sensor chip on one side and an Asic chip on the other side of the interposer, as illustrated in FIG. 33"). The convention Dr. Shanfield applies throughout his declaration is that "over" refers to the direction toward the printed wiring board ("PWB") and "under" refers to the direction away from the PWB. Pet., 11; EX1003 [Shanfield Decl.], ¶150. Because the BGA solder balls that connect to the PWB are formed on

the ASIC side of FIG. 33, a POSITA would understand the ASIC side of FIG. 33 to be the "over" side and the sensor side to be the "under" side — using Dr. Shanfield's own mapping elsewhere of the analogous ASIC-type device (device 130) and sensor-type device (device 125) in the FIG. 3 embodiment. See EX1004 [Sundaram], 6:37-45 (device 125 as an image sensor chip, device 130 as the logic/ASIC device).

150. FIG. 33, however, shows the "Passives" element positioned on the sensor side of the structure — immediately adjacent to the "Sensor" and its micro-bumps-and-RDL connection — not on the ASIC/BGA side. EX1004 [Sundaram], Fig. 33. Sundaram's own drawing therefore places its passive component on the "under" side of the structure, i.e., the side away from the PWB, and not "over" the interconnection scheme that connects to the PWB.

151. This is the opposite of where the Petition proposes to place the corresponding element in the FIG. 3 combination. The Petition places its combined passive component "adjacent to FIG. 3's second electronic device 130," which Dr. Shanfield elsewhere maps to the ASIC-type, PWB-facing side of the FIG. 3 structure. Pet., 29-30; EX1003 [Shanfield Decl.], ¶199; see also Pet., 33; *id.*, ¶208 (mapping device 130 as the second semiconductor chip over the first interconnection scheme, i.e., on the PWB-facing side of the structure). The Petition

thus takes the general teaching of FIG. 33 — that a passive component can be soldered to an RDL — but relocates that passive component to the side of the structure opposite to where Sundaram actually discloses it. The Petition does sowithout identifying any disclosure in Sundaram that supports placing a passive component on the device-130/over side rather than the device-125/under side depicted in FIG. 33.

152. A POSITA reading FIG. 33 would understand Sundaram's own teaching to place the passive component on the side of the package furthest from the board-level connection — for example, to keep the board-side footprint clear for the BGA array, or to position the passive nearer the sensor and its associated fine-pitch redistribution circuitry. The Petition provides no reasoning, let alone reasoning grounded in Sundaram's own disclosure, for why a POSITA would instead have placed the passive component on the opposite, PWB-facing side of the package as the Petition proposes. Because the Petition's sole evidentiary basis for the claimed placement is FIG. 33, and FIG. 33 shows the passive component on the side opposite to where the Petition places it, the Petition has not shown that a POSITA would have been motivated to place a passive component "over said first interconnection scheme" as claim 2 requires, nor has it shown a reasonable expectation of success in doing so.

153. For these reasons, in my opinion the Petition fails to prove that claim 2, or claim 22 (which recites the same limitation with respect to claim 16), is unpatentable over Sundaram, Haba, and Lin-191, or over Sundaram and Lin-191.

7. Sundaram, Haba, and Lin-191 Fail to Teach Claim 5.

154. Claim 5 requires "a first semiconductor chip compris[ing] a central-processing-unit (CPU) circuit block and a graphics-processing-unit (GPU) circuit block." EX1001 ['768 Patent], cl. 5. Sundaram does not disclose a central-processing-unit circuit block or a graphics-processing-unit circuit block, and Petitioners therefore rely exclusively on Lin-191. Pet., 35.

155. I have reviewed the Petition's motivation to combine for claim 5. The Petition states that although "Sundaram's FIG. 3 depicts device 125 as stacked memory, Sundaram teaches device 125 can be 'other electronic devices,'" and that Sundaram discloses "mobile phone applications, including video streaming, 3D graphics, camera-functions, and gaming" and contemplates "high power logic component[s]" for device 125's side of interposer 105. Pet., 36 (citing EX1003 [Shanfield Decl.], ¶211).

156. This rationale is inconsistent with the architecture Sundaram describes. Sundaram pairs a memory device on one side of the interposer with a logic device on the other: "the first electronic device 125 can be single or stacked

memory IC devices, and the second electronic device 130 can be a logic IC device or devices." EX1004 [Sundaram], 6:38-39. The purpose of that arrangement is to provide very high bandwidth between a logic device and a memory device across a short, dense interconnect.

157. Placing a central-processing-unit circuit block and a graphics-processing-unit circuit block as part of device 125 would place logic circuitry on both sides of the interposer and would remove the memory device that Sundaram's architecture is designed to serve. Sundaram's references to mobile phone applications and to high power logic components describe the demands that motivate Sundaram's logic-to-memory architecture. Thus, these references do not suggest converting the memory side of that architecture into a second logic device. For this reason, and for the reasons discussed above, a POSITA would not have been motivated to combine Lin-191 and Sundaram to arrive at claim 5.

8. Sundaram, Haba and Lin-191 Fail To Teach Or Suggest Claim 20.

158. Claim 20 requires "[t]he chip package of claim 16, wherein said first polymer layer has a coefficient of expansion between 3 and 10 ppm/°C." EX1001 ['768 Patent], cl. 20. The Petition's discussion of Ground 1A claim 20 states only "Sections V.A.5, VI.A." Pet., 58. Those are the sections of the Petition addressing Ground 1A limitation 1(a)(iii) and Ground 1B claim 16. Pet., 7, 59-67.

159. Claim 20, like limitation 1(a)(iii), requires that the recited coefficient of expansion be a property of the first polymer layer. The materials that Sundaram identifies as having coefficients of expansion within the claimed range are glass, not polymer, and Sundaram identifies glass as its preferred interposer material precisely because of its silicon-matched coefficient of thermal expansion. EX1004 [Sundaram], 5:62-67. The polymers disclosed in Sundaram have coefficients of expansion in the range of approximately 31 to 67 ppm/°C, well outside the claimed range. *Id.*, 8:61-62, Table 1. The Petition does not explain why a POSITA seeking a low coefficient of expansion would have departed from Sundaram's preferred glass interposer in favor of a polymer, and then looked to a further reference to supply a polymer having an atypically low coefficient of expansion. For the reasons discussed above, a POSITA would not have combined Sundaram and Haba in the manner the Petition proposes. *See also* Section XI.A.5.

9. Sundaram and Lin-191 Do Not Teach or Suggest Claim 25.

160. Claim 25 depends from claim 16 and requires that "said third metal interconnect compris[e] a second metal layer on said metal pad and a fifth copper layer over said second metal layer, wherein said fifth copper layer has a thickness between 5 and 30 micrometers." EX1001 ['768 Patent], cl. 25(b). For this limitation, the Petition states that "Claim 25(b)'s third metal interconnect

corresponds to Claim 1(f)(ii)'s fourth metal interconnect," and that "the limitations of Claim 25(b) correspond to those of Claim 1(f)(ii), including the interrelationship of the claimed components, because they recite the same claimed structure other than the nomenclature of third and fourth." EX1003 [Shanfield Decl.], ¶301. The Petition's own showing for claim 25(b) is limited to a cross-reference to its limitation 1(f)(ii) analysis: "Section V.A.19, reciting corresponding limitations." Pet., 71 (citing EX1003 [Shanfield Decl.], ¶301, which in turn incorporates id., ¶¶186-194 by reference).

161. Claim 25(b) is materially the same as limitation 1(f)(ii) of claim 1, and the Petition's own cross-reference confirms that it relies on the identical Lin-191 mapping discussed above — combining Lin-191's adhesion layer 711 and seed layer 712 into a single claimed "second metal layer." For the reasons discussed above in connection with limitation 1(f)(ii), Lin-191 does not disclose "a second metal layer on said metal pad and a fifth copper layer over said second metal layer." The Petition's mapping of layers 711 and 712 as a single layer for claim 25(b) is inconsistent with the Petition's own mapping of the three-layer structure in limitation 1(d)(iii) and element 7(c).

162. For these reasons, in my opinion the Petition has not shown that Sundaram and Lin-191 teach or suggest claim 25.

B. Grounds 2A and 2B

163. I have reviewed the Petition and grounds 2A and 2B collectively challenge claims 1-15. Ground 2A (Haba and Lin-191) challenges independent claim 1 and dependent claims 2-3, 5, 7-10 and 14-15. Pet., 2. Ground 2B (Haba, Lin-191, and Sundaram) challenges claims 4, 6, and 11-13 that depend from claim 1. Pet., 2. Ground 2B uses the same prior art combination (Haba, Lin-191 and Sundaram) as Ground 1A, but with Haba instead of Sundaram as the primary reference. Neither Ground 2A nor Ground 2B challenge independent claim 16 or any of its dependent claims 17-28.

164. For the reasons discussed below, the combination of Haba, Lin-191, and Sundaram fail to render any of claims 1-15 unpatentable.

1. The Petition Identifies Two Different Structures as the Same Claimed "Fourth Metal Interconnect."

165. Claim 1 recites the "fourth metal interconnect" – once, in limitation 1(f)(i), and then refers back to that same structure in limitation 1(f)(ii). Limitation 1(f)(i) requires that "said first semiconductor chip comprises a fourth metal interconnect on a first metal pad of said first semiconductor chip." Limitation 1(f)(ii) then requires that "*said* fourth metal interconnect comprises a second metal layer on said first metal pad and a fifth copper layer over said second metal layer, wherein said fifth copper layer has a thickness between 5 and 30 micrometers."

EX1001 ['768 Patent], cl. 1. A POSITA would understand that "said fourth metal interconnect" in limitation 1(f)(ii) refers to the same structure recited in limitation 1(f)(i), and that the same structure must therefore satisfy both limitations.

166. In Ground 2A, the Petition does not identify the same structure that satisfies both limitations. For limitation 1(f)(i), the Petition states that "solder ball 32 is a fourth metal interconnect that is on a first pad of microelectronic element 66 (first semiconductor chip)." Pet., 92. For limitation 1(f)(ii), the Petition states that "Lin-191 teaches or renders obvious interconnects/bumps with layers/thickness as recited in Claim 1(f)(ii)," and cross-references Section V.A.19 of the Petition. Pet., 94. Section V.A.19 relies on the layered structure of Lin-191's metal pillars or bumps 710 — an adhesion layer 711, a seed layer 712, and a metal layer 713. Pet., 24-25; EX1005 [Lin-191], [0389].

167. Those are two different structures, and neither is the other. Haba's solder ball 32 is a mass of solder. It does not comprise an adhesion layer, and it does not comprise a copper layer having a thickness between 5 and 30 micrometers. Lin-191's metal pillar or bump 710, on the other hand, is not a solder ball. Lin-191 describes the metal pillars or bumps 710 as bonded to separate solder joints 720. EX1005 [Lin-191], [0389]. The Petition's mapping therefore requires "said fourth metal interconnect" to be a solder ball for purposes of limitation 1(f)(i)

and a plated copper interconnect for purposes of limitation 1(f)(ii). A POSITA would not understand a single claimed structure to be both.

168. Even if Haba's microelectronic element 66 were understood to comprise solder ball 32, the Petition still would not have shown that the structure it identifies as the claimed fourth metal interconnect satisfies limitation 1(f)(ii).

2. [Intentionally omitted].

169. [Intentionally omitted].

170. [Intentionally omitted].

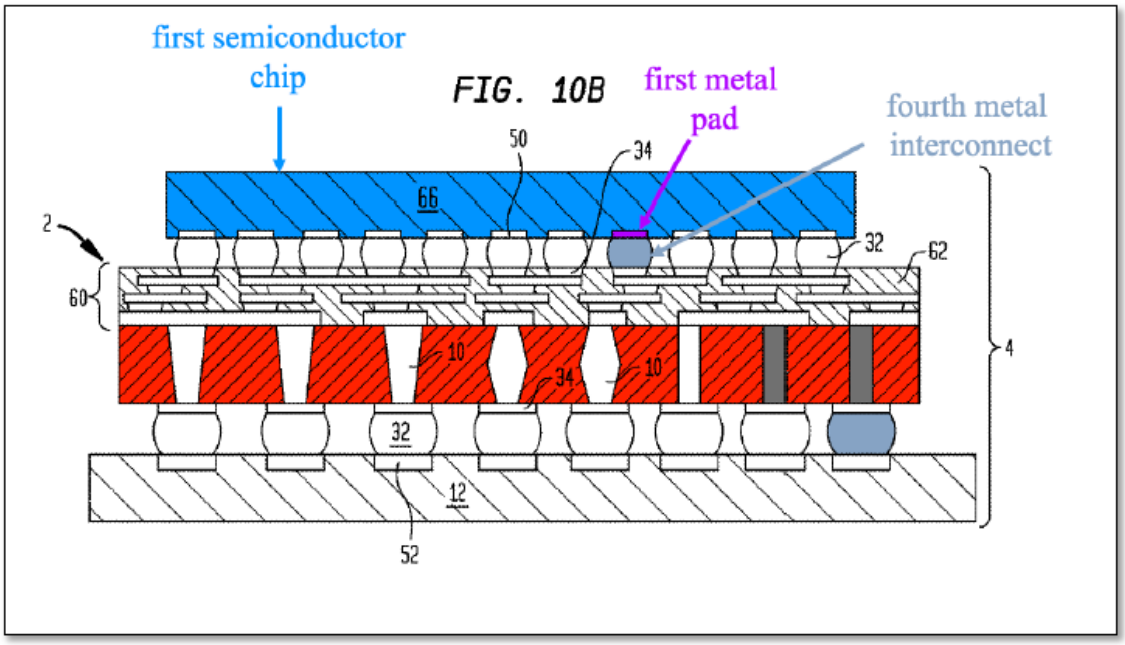
171. [Intentionally omitted].

172. [Intentionally omitted].

3. Haba and Lin-191 Do Not Teach Or Suggest a "First Semiconductor Chip Comprises a Fourth Metal Interconnect."

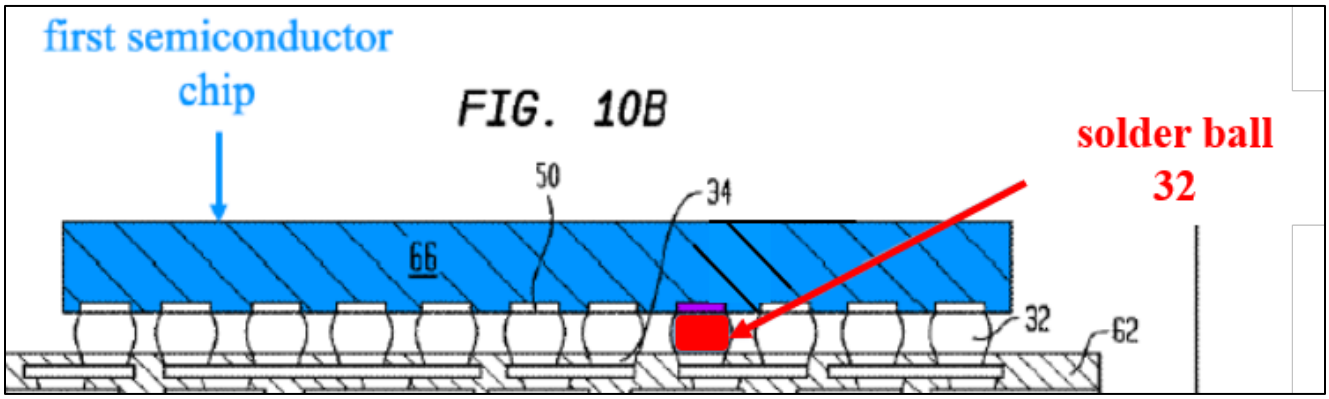
A. Haba does not teach or suggest this limitation because Haba's microelectronic element 66 does not comprise Haba's solder ball 32.

173. Limitation 1(f)(i) requires that the "first semiconductor chip comprises a fourth metal interconnect." EX1001 ['768 Patent], cl. 1. The Petition alleges Haba's microelectronic element 66 is the claimed "first semiconductor chip" and Haba's solder ball 32 is the claimed "fourth metal interconnect":



Pet., 92-93 (annotating EX1009 [Haba], Fig. 10B). EX2020 [Shanfield Dep. Tr.], 63:5-64:10.

174. The Petition's own annotation of Haba Fig. 10 (and Haba's disclosure) demonstrates that Haba's solder ball 32 is not part of microelectronic element 66.



EX1009 [Haba], Fig. 10B(excerpted and annotated). Instead, it is solder added outside microelectronic element 66 to attach microelectronic element 66 to interconnection component 2. EX1009 [Haba], 7:52-56 ("end surfaces 10B are used to join posts 10 to solder balls 32, which are, in turn, joined to contacts 50 on a microelectronic element [66].").[1]

175. As Haba explains, "[m]icroelectronic assemblies generally include one or more packaged micro-electronic elements such as one or more semiconductor chips mounted on a substrate." EX1009 [Haba], 1:19-22. Haba consistently treats the microelectronic element, the contacts of that element, and the material used to join the element to another component as separate things.

176. Haba's own claims reflect that separation. Claim 2 recites a microelectronic assembly in which "the element contacts are joined with the first wettable contacts through masses of conductive bonding material." EX1009 [Haba], cl. 2. Claim 21 similarly recites an assembly in which "at least some of the element contacts of the microelectronic element are joined to the first wettable

[1] Haba's specification and original figures discuss microelectronic element 6, not 66. However, a January 2, 2018 certificate of correction changed "6" to "66". EX1009 [Haba], p. 17.

contacts of the interconnection component through conductive masses." Id., cl. 21. A POSITA would understand from these recitations that Haba treats the microelectronic element and the conductive bonding masses (solder ball) (that join that element to the interconnection component) as a separate structure.

177. Haba also describes solder ball 32 as an interchangeable bonding material rather than a structure of the microelectronic element. Haba states that "[o]ther materials can be used in place of solder balls 32 to join features of the components of the assembly such as tin indium or a conductive matrix." EX1009 [Haba], 6:44-47. A POSITA would not understand a bonding material that may be replaced by "a conductive matrix" to be a part of the semiconductor chip being bonded.

178. For these reasons, Haba's microelectronic element 66 does not "comprise" solder ball 32. Solder ball 32 is a separate component from microelectronic element 66, and microelectronic element 66 does not include or contain, and is not characterized by, solder ball 32.

179. The component Petitioners allege is Haba's "fourth metal interconnect" is not part of the component Petitioners allege is Haba's "first semiconductor chip." The Petition's combination of Haba and Lin-191 does not teach the "first semiconductor chip comprises a fourth metal interconnect."

B. Lin-191 does not teach or suggest this limitation.

180. Petitioners include two sentences on Lin-191 for Ground 2A limitation 1(f)(1). Those sentences are directed to the claimed "metal pad," not the claimed "fourth metal interconnect." Pet., 93. The Petition's analysis states "Section V.A.18," possibly intending to refer back to §V.A.18 of the Petition for support. *Id.* But section V.A.18 only refers to the "metal pad" limitation, stating that "Lin-191 teaches a semiconductor chip 160 with 'metal traces or pads 163' that include 'aluminum.'" Pet., 23. It does not allege Lin-191 teaches or suggests the "first semiconductor chip comprises a fourth metal interconnect." Thus, Lin-191 does not remedy the deficiency in Haba.

C. The Petition Provides No Rationale For Combining Haba With Lin-191 and There is No Motivation to Combine.

181. The Petition's rationale for combining Lin-191 with Haba for limitation 1(f)(i) (below) lacks the appropriate articulated reasoning or rational underpinning.

> **a) Lin-191's "Metal Pad" Teachings and MTC**
>
> Section V.A.18. The Haba-Lin-191 combination an implementation detail in Haba's chip package as Lin-191 provides the specificity of a metal contact pad to the extent that PO argues not provided by Haba. *EX1003*, ¶376. The same MTC and REOS for Sundaram-Lin-191 apply for Haba-Lin-191. Section V.A.18.b.

Pet., 93. The first and last sentence ("Section V.A.18" and "Section V.A.18.b") possibly intend to refer back to those sections of the Petition for support. *See* Pet., 26. Though Section V.A.18.b discusses why a POSITA would allegedly combine Sundaram and Lin-191, Section V.A.18.b does not mention Haba, let alone why a POSITA would allegedly combine Haba and Lin-191. Thus, it cannot serve as articulated reasoning or a rational underpinning for why a POSITA would allegedly combine Haba and Lin-191.

182. The second sentence states "[t]he Haba-Lin-191 combination an implementation detail in Haba's chip package as Lin-191 provides the specificity of a metal contact pad to the extent that PO argues not provided by Haba." Pet., 93, Based on my reading, it appears to imply that the rationale for adding Lin-191's contact 50 to Haba is because the claimed metal pad is "not provided by Haba." *Id.* The Petitioners provide no rationale for why a POSITA would be motivated to combine Lin-191's contact 50 with Haba.

183. The third sentence states "[t]he same MTC and REOS for Sundaram-Lin-191 apply for Haba-Lin-191." *Id.* Again, this statement refers to the Petition's rationale for combining Sundaram and Lin-191, which makes no mention of Haba.

184. The Petition cites to paragraph 376 of Dr. Shanfield's declaration in support. Pet., 93. That paragraph refers back to Dr. Shanfield's motivation to

combine Sundaram and Lin-191, stating "[f]or the same MTCs and with the same reasonable expectation of success, a POSITA would have found it obvious and been motivated to implement, per Lin-191, Haba's contact 50 (first…pad) as metal, yielding a first metal pad." EX1003 [Shanfield Decl.], ¶376. But neither paragraph 376 nor Dr. Shanfield's analysis of the motivation to combine Sundaram and Lin-191 contains any analysis of why a POSITA would allegedly be motivated to combine Haba and Lin-191. The Petition's motivation to combine Haba and Lin-191 consists entirely of conclusory statements lacking any articulated reasoning with rational underpinnings to support a conclusion of obviousness.

185. In Section XI.B.6, paragraph 203 below, I provide additional analysis as to why a POSITA would not be motivated to combine Haba and Lin-191.

4. Haba and Lin-191 Do Not Teach "Wherein Said Fourth Metal Interconnect Comprises a Second Metal Layer On Said First Metal Pad and a Fifth Copper Layer Over Said Second Metal Layer, Wherein Said Fifth Copper Layer Has a Thickness Between 5 and 30 Micrometers."

a. Lin-191 does not teach "said fourth metal interconnect."

186. The Petition relies solely on Lin-191 for limitation 1(f)(ii). Pet., 94. The Petition's explanation is that "Lin-191 teaches or renders obvious interconnects/bumps with layers/thickness as recited in Claim 1(f)(ii)," citing Section V.A.19 of the Petition. Id.

187. The Petition's reliance on Lin-191 for limitation 1(f)(ii) does not cure the deficiency discussed above. The structure the Petition identifies as the claimed "fourth metal interconnect" for limitation 1(f)(i) is Haba's solder ball 32, and the structure on which it relies for limitation 1(f)(ii) is Lin-191's metal pillar or bump 710. Solder balls and pillar or bumps are not the same structures. The Petition therefore does not identify any single structure that is both the "fourth metal interconnect" of limitation 1(f)(i) and "said fourth metal interconnect" of limitation 1(f)(ii).

b. Lin-191 does not teach "a second metal layer on said first metal pad" or a fifth copper layer of the claimed thickness.

188. For the reasons discussed above in connection with Ground 1A, the Petition does not show "a second metal layer on said first metal pad" as required by limitation 1(f)(ii).

189. Because the Petition does not identify a "second metal layer" in Lin-191 as limitation 1(f)(ii) requires, it also does not identify a "fifth copper layer over said second metal layer." The thickness the Petition ascribes to Lin-191's metal layer 713 therefore does not establish the limitation. Because neither Haba nor Lin-191 teaches or suggests limitation 1(f)(ii), the Petition fails to prove that claim 1, or the claims depending therefrom, are unpatentable .

5. Haba and Lin-191 Do Not Teach or Suggest Claim 2's "Passive Component ... Over Said First Interconnection Scheme."

190. Claim 2 requires "a passive component over said first interconnection scheme and connected to said first interconnection scheme through a solder layer." EX1001 ['768 Patent], cl. 2. For Ground 2A, the Petition relies on two different figures of Lin-191 for this limitation: FIG. 55, for the teaching that a chip can be replaced with a passive component connected through solder joints, and FIG. 84, for the position of that substitution relative to Haba's structure. Pet., 96-98; EX1003 [Shanfield Decl.], ¶¶382-386. The Petition states that connecting a passive component "over RDL 70 would advantageously mitigate signal desynchronization and preserve signal integrity," Pet., 98, and Dr. Shanfield's declaration elaborates that, in the combination, the passive component is "positioned between dielectric layer 20 and PCB 12, taking the place of some of solder balls 32, thus parallel to the remaining solder balls 32." EX1003 [Shanfield Decl.], ¶386.

191. Lin-191 does not support this mapping, for three reasons.

192. First, FIG. 55 is expressly tied to a different embodiment than FIG. 84. Lin-191 states that "FIG. 55 demonstrates another system-in package or multichip module according to another embodiment of the present disclosure. In this embodiment, one of the chips 140 in the system-in package or multichip

module illustrated in FIG. 52 can be replaced by a passive component 67... The passive component 67 can be connected to the metal layer 53 of the patterned metal layer 5 through two solder joints 68." Pet., 96; EX1005 [Lin-191], [0340]. Lin-191 itself identifies the embodiment to which FIG. 55's substitution teaching applies — the FIG. 52 embodiment — rather than leaving that substitution open to be imported into any other embodiment sharing the numeral "140." The Petition's reliance on Lin-191's general statement that "the same numeral appears in different drawings" to import FIG. 55's teaching into the separate FIG. 84 embodiment (EX1003 [Shanfield Decl.], ¶382 n.5) does not override Lin-191's own express statement that the FIG. 55 substitution belongs to the FIG. 52 embodiment.

193. Second, even if a POSITA imported FIG. 55's substitution concept into FIG. 84, the chip 140 that Lin-191 actually describes in the FIG. 84 family of embodiments does not connect to patterned metal layer 5 the way FIG. 52/55's chip 140 does. Lin-191 states that "[t]hrough one or more metal pillars or bumps 64, each of the chips 140 can be connected to... the patterned metal layer 7," and that "[e]ach of the chips 140 has one of the metal traces or pads 66 connected to one or more of the metal traces or pads 46 in one or more of the chips 130 through, in sequence, the patterned metal layer 6, one of the metal pillars or bumps 64, the patterned metal layer 7... one or more of the metal pillars or bumps 54, the

patterned metal layer 5, one or more of the metal pillars or bumps 44, and the patterned metal layer 4." Pet., 97; EX1005 [Lin-191], [0273]. This passage shows that the chips 140 relevant to the FIG. 84 family connect directly to patterned metal layer 7 through metal pillars or bumps 64, and that patterned metal layer 5 is a separate, more remote layer reached only after passing through metal layer 7 and additional metal pillars or bumps 54. A component occupying chip 140's position in this embodiment would connect to layer 7, not layer 5.

194. This sequence also defeats the Petition's "over" mapping. Dr. Shanfield applies a convention under which "over" refers to the direction toward the printed circuit board and "under" refers to the direction away from it. EX1003 [Shanfield Decl.], ¶383 (stating that "chip 140 is over patterned metal layer 5 because it is towards the solder balls 29a which connect to a PCB"). Because patterned metal layer 5 lies further along the conductive path toward the package's lower metal layers and, ultimately, its board-level connections than patterned metal layer 7 and the chips 140 that connect to it, a POSITA would understand a component in chip 140's position to be on the chip side of patterned metal layer 5, not on the side of patterned metal layer 5 that faces the circuit board. The Petition has therefore not shown that a passive component substituted for chip 140 in the FIG. 84 embodiment would be "over" patterned metal layer 5.

195. [Intentionally omitted].

196. I have also reviewed Dr. Shanfield's citation to Lin-191 [0439] for his statement that "chip 140 is over patterned metal layer 5 because it is towards the solder balls 29a which connect to a PCB." EX1003 [Shanfield Decl.], ¶383. Paragraph [0439] does not support that statement. Paragraph [0439] states that, "[a]lternatively, referring to FIG. 84... multiple discrete (preformed) passive components 910, such as capacitors, inductors or resistors, are mounted on the contact points, exposed by the openings 99a in the polymer layer 99, of the metal layer 9c through multiple solder joints 915," and that the resulting structure "can be connected to a mother board, a printed circuit board, a metal substrate, a glass substrate or a ceramic substrate using the solder bumps or balls 29a." EX1005 [Lin-191], [0439]. This paragraph does not mention chip 140, patterned metal layer 5, passive component 67, or solder joints 68 at all. It describes a different, unrelated teaching: discrete passive components 910 mounted on metal layer 9c through solder joints 915. Paragraph [0439] provides no support for the Petition's assertion that chip 140 is positioned "over" patterned metal layer 5 in the FIG. 84 embodiment.

197. Third, neither FIG. 55 nor FIG. 84, nor any other portion of Lin-191 that the Petition cites, teaches, or suggests replacing a solder ball with a passive

component. Lin-191's actual teaching is a substitution of a chip for a passive component at a chip-attach location — the FIG. 52/55 embodiment replaces chip 140, which Lin-191 elsewhere describes as having "first and second terminals" landing on discrete contact points of an interconnection scheme, with passive component 67, which likewise has "first and second terminals" landing on the same type of contact points. EX1005 [Lin-191], [0340]-[0341]. That is a substitution of one two-terminal device for another two-terminal device at the same type of attachment location.

198. The Petition's proposed modification of Haba is a different substitution. As discussed above, the Petition states only that connecting a passive component over RDL 70 would preserve signal integrity, Pet., 98, though Dr. Shanfield's declaration states that, in the combination, the passive component "is positioned between dielectric layer 20 and PCB 12, taking the place of some of solder balls 32, thus parallel to the remaining solder balls 32." EX1003 [Shanfield Decl.], ¶386. Haba's solder balls 32 are individual, single-node connectors that each carry a dedicated electrical path from one of Haba's pads 34 to a corresponding one of PCB 12's contacts 52. EX1009 [Haba], 7:54-56. Removing one of those individual connectors and replacing it with a two-terminal passive component is not the same kind of substitution as replacing an entire chip (with its

own independent set of terminals and conductive paths) with a passive component having a comparable set of terminals. Lin-191 does not teach, suggest, or provide any reasoning that would have led a POSITA to remove one of an array of single-node board-level solder balls and replace it with a two-terminal passive component. A POSITA would not have found it obvious to do so, and the Petition identifies no motivation, teaching, or suggestion — in Lin-191 or otherwise — for that specific substitution. Nor does the Petition explain how a two-terminal passive component would be expected to function in place of a single-node solder ball, or where the passive component's second terminal would connect.

199. For these reasons, in my opinion the Petition has not shown that Haba and Lin-191 teach or suggest claim 2, or claim 22 (which recites the same limitation with respect to claim 16).

6. The Petition Fails To Prove Haba and Lin-191 Render Claim 5 Unpatentable.

200. Petition Ground 2A states as follows for claim 5:

> **E. Claim 5**
>
> The same MTCs and REOS for modifying Sundaram per Lin-191 apply to Haba-Lin-191, e.g., increasing the functionality of Haba's *chip package*. Section V.E; *EX1003*, ¶¶394-395.

Pet., 101.

201. A POSITA could not determine what structure in Haba or in Lin-191 the Petition contends corresponds to the central-processing-unit circuit block and the graphics-processing-unit circuit block recited in claim 5, or whether the Petition relies on Haba, on Lin-191, or on both for that limitation.

202. Further, the Petition's motivation to combine and reasonable expectation of success refer back to the motivation to combine Sundaram and Lin-191 rather than Haba and Lin-191. There is no discussion at Section V.E of why a POSITA would be motivated to "increas[e] the functionality of Haba's chip package." The Shanfield declaration at paragraphs 394 and 395 repeats the statement from the Petition and adds that "Haba, like Sundaram, contemplates 'cellular phones[.]'" EX1003 [Shanfield Decl.], ¶395. But it provides no explanation for why this would motivate a POSITA to combine Lin-191 and Haba or why the POSITA would have a reasonable expectation of success in doing so.

203. A POSITA would not combine Haba and Lin-191. Haba describes its posts as unitary metal bodies: they "can be monolithically formed such as by plating a conductive metal on an electrical commoning layer... or by etching posts 10 from a solid layer of metal 6 disposed on an etch-stop layer 4b," EX1009, [9:13–18], and in a further embodiment "can be fabricated from a single layer of the principal metal (e.g., Cu and the like)." EX1009, [10:45–49]. Haba's summary

likewise describes forming the posts "by etching a solid metal layer to remove metal from areas outside the posts." EX1009, 2:46-50. Lin-191's adhesion layer 61 and seed layer 62 are a different kind of structure altogether — sputtered and plated thin films, each under a micrometer thick, deposited over the passivation layer 65 and onto the metal pads 66 of a semiconductor chip as part of post-passivation, wafer-level processing. EX1005, ¶¶[0219], [0226]–[0227]. Haba's component contains no chip, no passivation layer, and no chip pads, and is built by molding a dielectric around preformed posts rather than by depositing films on a wafer. A POSITA would have understood that Lin-191's layers presuppose a chip surface Haba does not present, and that adding them to Haba's posts would displace the unitary, etched-from-solid-metal construction Haba consistently describes. Nor does Lin-191 speak to the problem Haba set out to solve — reducing CTE mismatch so that the posts do not "become detached from within the molded dielectric layer during use," EX1009, 6:11-14 — as Lin-191 nowhere identifies CTE, stress, or interface failure as considerations bearing on its metal bump structures. A POSITA seeking to improve Haba would have found nothing in Lin-191 directed to that objective.

7. Haba and Lin-191 Do Not Teach or Suggest Claim 3 or Claim 7(c).

204. Claim 3 requires that "said first interconnection scheme comprise a fifth metal interconnect across over a sidewall of the first semiconductor chip," and claim 7(c) further requires that "said fifth metal interconnect compris[e] a third metal layer, a sixth copper layer on said third metal layer, and a seventh copper layer on said sixth copper layer." EX1001 ['768 Patent], cls. 3, 7(c). For Ground 2A, the Petition maps the fifth metal interconnect to Haba's pad 34 and relies on the same Lin-191 three-layer structure discussed above — adhesion layer 18, seed layer 19, and metal layer 27 — for the required three-layer construction.103; EX1003 [Shanfield Decl.], ¶¶400-401 (citing EX1005 [Lin-191], [0308]-[0309], [0313], [0323]).

205. As discussed above, Lin-191's adhesion layer 18/seed layer 19/metal layer 27 sequence is a sputtered under-bump metallization structure, formed as an additional stack on top of an already-complete patterned metal layer 9 (itself composed of adhesion layer 9a, seed layer 9b, and metal layer 9c), for the purpose of preparing that layer's contact points for solder ball attachment. EX1005 [Lin-191], [0294]-[0296], [0300]-[0301], [0305]-[0307]. This is a wafer-level bump-formation sequence, not a description of a package-level redistribution pad.

206. Haba's pad 34 is not the kind of structure this sequence is designed for. Haba's pad 34 is a wettable contact formed from an already-existing, etched copper structure. Haba discloses that its posts are "made from copper" and that its redistribution-layer traces 30, of which pad 34 can be a portion, "can be formed by etching away selected portions of layer 4," the same rigid metal layer the copper posts are formed from. EX1009 [Haba], cl. 6; 9:65-67, 10:20-24. Haba separately discloses that, where additional wettability is desired, "wettable metal layers or structures can be added to interconnection component 2... made from nickel or Ni—Au, or organic solderable preservative ('OSP')." EX1009 [Haba], 7:47-51. A POSITA would recognize nickel, Ni-Au, and OSP as the same class of surface finish used in printed-circuit and package-level fabrication to prepare an already-formed bulk copper pad for solder attachment — applied directly to the copper by a thin electroless, for example, without any sputtered adhesion layer or seed layer.

207. The Petition does not explain why a POSITA, starting from Haba's own already-disclosed nickel, Ni-Au, or OSP treatment for pad 34, would instead have looked to Lin-191's more elaborate sputtered adhesion-layer/seed-layer/electroplated-metal three-layer sequence — a sequence developed to prepare a semiconductor die's own bond pad for a new solder bump. The Petition states that "[b]ecause pad 34 connects to solder ball 32, a POSITA would have found it

advantageous to modify pad 34 to include UBM layers to improve solder reliability."103; EX1003 [Shanfield Decl.], ¶401. This does not address the fact that Haba's own disclosure already provides a solution to the same solder-reliability and wettability concern, using a different and simpler class of treatment than the one Lin-191 discloses. The Petition does not explain why a POSITA would have been motivated to depart from Haba's own disclosed approach in favor of Lin-191's.

208. In Section XI.B.6, paragraph 203 below, I provide additional analysis as to why a POSITA would not be motivated to combine Haba and Lin-191.

209. For these reasons, the Petition has not shown that Haba and Lin-191 teach or suggest claim 3 or claim 7(c).

210. I note that my opinions regarding claim 3 and claim 7(c) differ between Ground 1A and Ground 2A, because the Petition relies on different structures in each. For Ground 1A, the Petition maps Sundaram's die pad 135 as the fifth metal interconnect and relies on Lin-191's patterned metal layer 7 for its layer structure. For Ground 2A, the Petition maps Haba's contact pad 34 and relies on a different Lin-191 structure. Pet., 43-45, 99. Each mapping fails for reasons particular to the structure the Petition has selected.

8. The Petition Fails to Prove Haba and Lin-191 Render Claim 10 Unpatentable.

211. The Petition also fails to demonstrate how Haba and Lin-191 render claim 10 unpatentable. The Petition's entire explanation is below:

> **I. Claim 10**
>
> Section V.J. The same MTCs and REOS apply.

Pet., 105. "Section V.J" is Ground 1A's analysis of claim 10 for Sundaram and Lin-191. The Petition does not explain how Haba and Lin-191 allegedly teach or suggest claim 10, nor what the motivation to combine or reasonable expectation of success are in combining Haba and Lin-191. The Petition's citation to Section V.J refers back to the Petition's discussion of how Sundaram and Lin-191 allegedly teach or suggest claim 10. *Id.*, 48-49. Section V.J makes no mention of Haba, let alone discuss why a POSITA would be motivated to combine Haba and Lin-191, or have a reasonable expectation of success in doing so. *Id*. Accordingly, the Petition fails to prove that claim 10 is unpatentable over Haba and Lin-191.

C. Grounds 3A-3C

212. Grounds 3A-3C challenge independent claim 16 and its dependent claims 17-28. Pet., 2. These grounds do not challenge claims 1-15.

1. Yu and Lin-191 Do Not Teach Or Suggest a "Second Metal Interconnect."

213. Claim 16 recites that a "first interconnection scheme comprises a first metal interconnect …, a second metal interconnect …, wherein said first metal interconnect is connected to said first metal plug." Ex. 1001, 24:45-54. The claim requires both a first metal interconnect and a second metal interconnect—that is, the claim requires two separate interconnects.

214. The '768 Patent distinguishes the metal interconnects of an interconnection scheme by the conductive path each provides, and not by vertical position within a single conductive path. Claim 1 illustrates that usage. Claim 1 recites that "said first metal interconnect is connected to said first metal plug, wherein said second metal interconnect is connected to said second metal plug." EX1001 ['768 Patent], cl. 1. A POSITA would understand from this recitation that the first and second metal interconnects of the first interconnection scheme are separate conductive paths, each routing to a different metal plug, rather than two vertically stacked portions of one conductive path.

215. Claim 16 does not separately recite a connection between the second metal interconnect and the second metal plug. However, a POSITA would understand the terms "first metal interconnect" and "second metal interconnect" to

carry the same meaning in claim 16 as in claim 1, and would understand claim 16 to require two separate conductive paths within the first interconnection scheme.

216. I note that the '768 Patent recites that one metal interconnect is connected to another. Claim 1 recites that "said fourth metal interconnect is connected to said third metal interconnect." EX1001 ['768 Patent], cl. 1. Claim 25 recites that "said third metal interconnect is connected to said a fourth metal interconnect of said first interconnection scheme." *Id.*, cl. 25. Those recitations, however, simply cover the situation where two separate metal interconnects (with separate conductive paths) may be connected to one another.

217. Each of those recitations describes a connection between an interconnect of a semiconductor chip and an interconnect of the first interconnection scheme. In claim 1, the fourth metal interconnect is a structure of the first semiconductor chip and the third metal interconnect is a structure of the first interconnection scheme. *Id.*, cl. 1. In claim 25, the third metal interconnect is a structure of the second semiconductor chip and the fourth metal interconnect is "of said first interconnection scheme." *Id.*, cl. 25. Each recitation therefore describes a connection made across the interface between a chip and the interconnection scheme on which it is mounted.

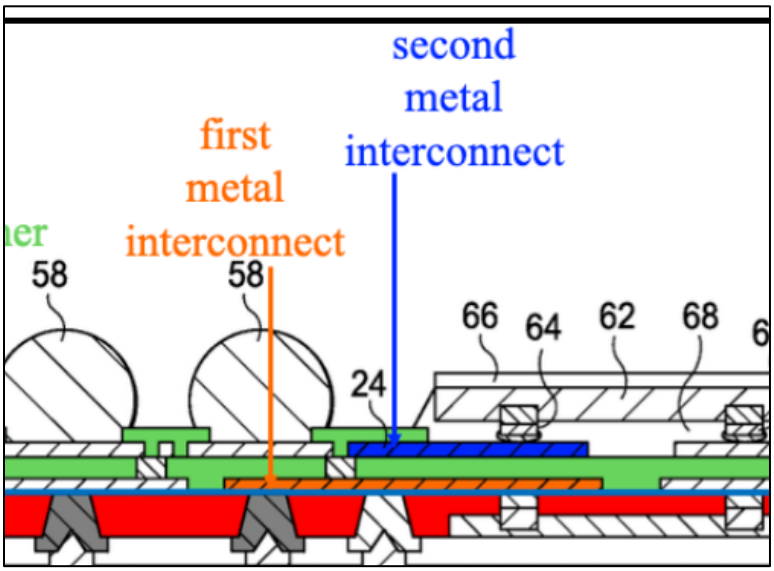
218. The ’768 Patent does not recite two metal interconnects of the same interconnection scheme as connected to one another. Where the patent describes an additional interconnect of the first interconnection scheme positioned above another, it recites no connection between them. Claim 7, for example, recites “a fifth metal interconnect over said first metal interconnect and said second polymer layer, wherein said second polymer is between said first and fifth metal interconnects.” *Id.*, cl. 7. A POSITA would understand from this usage that the first and second metal interconnects of the first interconnection scheme are separate conductive paths within that scheme. A POSITA would not understand two successive levels of a single path through the scheme to be the first and second metal interconnects that claim 16 requires.

219. The Petition’s mapping is also inconsistent with claim 16’s requirement of “a second polymer layer over said first and second metal interconnects.” EX1001 [’768 Patent], cl. 16. The Petition states that “ILD layers 22, 26 comprise ‘polyimide’ and are, collectively, a second polymer layer over metallization layers 20, 24.” Pet., 127.

220. ILD layer 22 and ILD layer 26 are two separate layers, not one layer. Yu describes ILD layer 22 as deposited over the first metallization layer 20, and describes the second metallization layer 24 and the second ILD layer 26 as formed

afterward. EX1010 [Yu], 3:20-32. ILD layer 22 lies beneath the second metallization layer 24 and is therefore not over the structure the Petition identifies as the claimed second metal interconnect. A POSITA would not understand two dielectric layers at different levels of a build-up structure, separated by a metallization layer, to be a single polymer layer over both metallization layers.

221. Instead of identifying a first metal interconnect and a second metal interconnect as the claim requires, the Petition identifies two portions of the same conductive path as satisfying both limitations. Below is the highlighted and annotated figure from the Petition identifying the alleged first and second metal interconnects.



Pet., 127 (annotating EX1010 [Yu], Fig. 16). The orange layer (Yu's alleged first metallization layer 20) is the alleged "first metal interconnect" and the blue layer

(Yu's alleged second metallization layer 24) is the alleged "second metal interconnect." But these layers are connected together by the unlabeled and uncolored metal material disposed between the orange and blue layers. The orange and blue layers are two portions of a *single* conductive path through the interconnection scheme, and are not the two separate metal interconnects of the first interconnection scheme that claim 16 requires. Yu describes metallization layers 20 and 24 as successive levels of a single redistribution structure on the front side of the package. Yu states that the first front side metallization layer 20 is formed, and that "[a] first ILD layer 22 is deposited on the front side and over the first metallization layer 20." EX1010 [Yu], 3:20-21. Yu then states that "[o]penings may be formed through the first ILD layer 22 to the first metallization layer 20," and that subsequent metallization layers and ILD layers, "such as a second metallization layer 24 and a second ILD layer 26, may be formed using the same or similar processes as discussed with regard to the first metallization layer 20 and the first ILD layer 22." *Id*., 3:25-32. Yu further states that "[c]onductive material deposited during the formation of a subsequent metallization layer may be deposited in openings of the previously formed ILD layer to electrically couple respective metallization layers." *Id*.

222. I recognize that Yu describes these steps permissively. However, the figure on which the Petition relies depicts conductive material occupying the openings in the first ILD layer 22 and joining the first metallization layer 20 to the second metallization layer 24. Pet., 127 (annotating EX1010 [Yu], Fig. 16). My opinions below address the structure that the Petition has identified in that figure.

223. The conductive material occupying the openings in the first ILD layer 22 joins the first metallization layer 20 and the second metallization layer 24 into a single conductive path. The Petition identifies the claimed "first metal interconnect" as a portion of metallization layer 20 (highlighted in orange above) and the claimed "second metal interconnect" as a portion of metallization layer 24 (highlighted in blue above). Those two portions are not separate conductive paths. They are an upper and a lower portion of the same path, and a signal entering one passes directly into the other.

224. This is not what claim 16 requires. As discussed above, the '768 Patent distinguishes the first and second metal interconnects of an interconnection scheme as separate conductive paths. The Petition has identified a single conductive path in Yu and labeled two portions of it as the claimed "first" and "second" metal interconnects. Petitioners therefore have not identified the two metal interconnects that claim 16 requires.

225. The Petition's treatment of dependent claim 27 confirms this. For claim 27, the Petition relies on the fact that what it identifies as the "first metal interconnect" is directly electrically connected to what it identifies as the "second metal interconnect." Pet., 145-46. That reliance confirms that the two structures the Petition has identified lie on a single conductive path

226. The conductive material deposited in the openings in the first ILD layer 22 connects the first metallization layer 20 to the second metallization layer 24. When Petitioners identify the claimed "first metal interconnect" as corresponding to the portion of metallization layer 20 (highlighted in orange above) and the claimed "second metal interconnect" as corresponding to the portion of metallization layer 24 (highlighted in blue above), Petitioners are identifying two layers of the same metal interconnect. Thus, Petitioners do not identify the claimed "first" and "second" metal interconnects. Petitioners have only identified one metal interconnect.

2. Yu and Lin-191 Do Not Teach or Suggest Limitation 16(d)(iii).

227. Limitation 16(d)(iii) requires that "said first metal interconnect compris[e] a first metal layer, a third copper layer on said first metal layer, and a fourth copper layer on said third copper layer." EX1001 ['768 Patent], cl. 16(d)(iii). For this limitation, the Petition relies on Yu's own description of

metallization layer 20: "Metallization layer 20 includes a 'seed layer, such as copper…deposited on the molding compound 18,' and a '[c]onductive material…such as copper…is deposited on the seed layer.'" Pet., 128 (quoting EX1010 [Yu], 3:5-19). The Petition maps Yu's copper seed layer as the claimed "third copper layer" and Yu's copper conductive material as the claimed "fourth copper layer." Id.; EX1003 [Shanfield Decl.], ¶472.

228. Yu's own description of metallization layer 20, as quoted by the Petition, discloses only two layers: a copper seed layer and copper conductive material electroplated onto that seed layer. EX1010 [Yu], 3:5-19. Yu states that the seed layer is deposited "on the molding compound 18" – that is, directly on a dielectric surface, with no intervening layer described. *Id.* Yu's own teaching therefore does not disclose the claimed "first metal layer," which limitation 16(d)(iii) requires to underlie the third copper layer.

229. The Petition does not explain why its stated rationale for adding an adhesion layer applies to the interface Yu discloses. The Petition's rationale is directed to a metal-to-metal interface. The Petition states that "Lin-191's multi-layered copper structure corresponds to sequentially deposited seed and plating layers formed during electroplating, providing adhesion to the underlying metal

layer and buildup of conductor thickness." Pet., 16-17 (citing EX1003 [Shanfield Decl.], ¶ 163). The Petition further states that "[n]ickel layer 31 advantageously mitigates copper diffusion out of the metal interconnect, reducing void formation." Pet., 17 (citing EX1003 [Shanfield Decl.], ¶ ¶ 163-168). Dr. Shanfield likewise states that "Lin-191's nickel adhesion layer 31 would have prevented diffusion of copper into adjacent interconnects, as nickel was known to resist copper diffusion." EX1003 [Shanfield Decl.], ¶ 162.

230. The interface Yu describes is not the interface those statements address. In Yu, the seed layer of metallization layer 20 is deposited directly on molding compound 18, an organic encapsulant, and there is no adjacent metal interconnect at that interface into which copper could diffuse. EX1010 [Yu], 3:5-19. Whether an adhesion or barrier layer is used at a given interface depends on the specific materials involved, and the Petition offers no reason directed to a copper-to-organic interface. Yu describes its metallization process — including the composition and deposition of both the seed layer and the conductive material formed on it — in detail, and does not describe any adhesion or barrier layer as part of that process. *Id.*

231. To supply a first metal layer that Yu itself does not disclose or require, the Petition turns to a different reference. The Petition states that "Lin-191's

adhesion layer 31 is a first metal layer with two copper layers formed thereon," Pet., 129 (citing EX1005 [Lin-191], Fig. 22, [0127]), and that a POSITA would have been motivated "to apply Lin-191's three-metal layer interconnect teachings to Yu's first metal interconnect, yielding the claimed layer[s] to obtain the benefits of Lin-191's adhesion layer 31." Pet., 129-130; EX1003 [Shanfield Decl.], ¶¶473-474.

232. There is no motivation to combine Yu and Lin-191. Indeed, the Petition does not explain how Lin-191's adhesion layer 31 is to be incorporated into Yu's own, already fully-described deposition sequence for metallization layer 20. Lin-191's adhesion layer 31, together with its own seed layer 32 and metal layer 33, is itself a complete, three-layer interconnect structure within Lin-191's own package. EX1005 [Lin-191], [0127]-[0128], [0133]. Yu, however, already describes metallization layer 20 as beginning with a copper seed layer deposited directly on the molding compound, with no adhesion layer beneath it. EX1010 [Yu], 3:5-19. The Petition's proposal to "apply" Lin-191's three-layer teaching to Yu's already-complete two-layer structure does not explain whether a POSITA would insert Lin-191's adhesion layer 31 between the molding compound and Yu's existing seed layer, substitute Lin-191's entire three-layer stack for Yu's seed layer, or make some other modification. Nor does the Petition explain why a

POSITA would depart from Yu's own express disclosure that the seed layer is deposited directly on the molding compound.

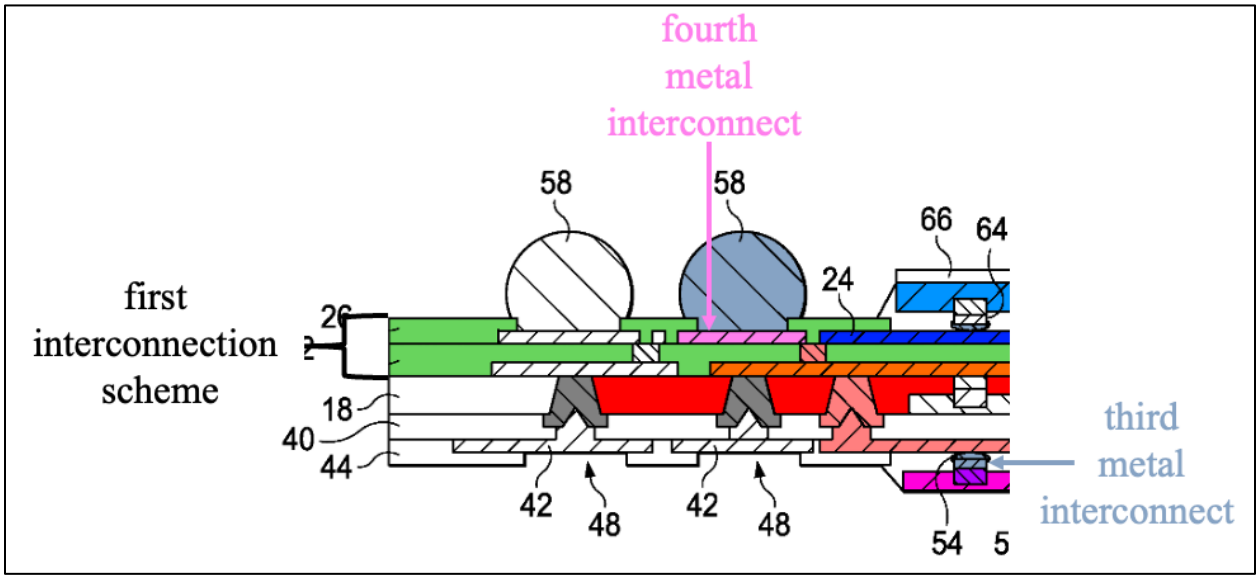
233. There is no reason why a POSITA would have understood Yu's own two-layer metallization structure to require modification at all. Yu presents its seed-layer/electroplated-copper sequence as a complete process for forming metallization layer 20, without describing any deficiency that an added adhesion layer would remedy. EX1010 [Yu], 3:5-19. The Petition's stated motivation — that the modification would provide "the benefits of Lin-191's adhesion layer 31," Pet., 129-130 — does not identify any problem with Yu's own structure that those benefits would address, nor does it explain why a POSITA would modify an already complete, fully-disclosed interconnect structure to import an additional layer from an unrelated reference.

234. For these reasons, in my opinion the Petition has not shown that Yu and Lin-191 teach or suggest limitation 16(d)(iii), and therefore has not shown that claim 16, or the claims depending therefrom, are unpatentable on this ground.

3. Claim 25: Yu and Lin-191 Do Not Teach Or Suggest a "Fourth Metal Interconnect."

235. Claim 25 recites in part "wherein said third metal interconnect is connected to said a fourth metal interconnect of said first interconnection scheme." The Petition alleges "another portion of metallization layer 24" in Yu Fig. 16

(excerpted and highlighted in purple below) is the claimed "fourth metal interconnect."



Pet., 144 (annotating EX1010 [Yu] Fig. 16).

236. I note that claim 16, from which claim 25 depends, recites a first metal interconnect and a second metal interconnect of the first interconnection scheme, and does not recite a third or fourth metal interconnect of that scheme. EX1001 ['768 Patent], cl. 16. A POSITA would understand the "fourth metal interconnect of said first interconnection scheme" recited in claim 25 to be a metal interconnect distinct from the first and second metal interconnects recited in claim 16.

237. The portion of Yu's metallization layer 24 that Petitioners allege is the "fourth metal interconnect" is part of the same metallization layer 24 that

Petitioners allege is the "second metal interconnect." Below is the image taken from page 127 of the Petition showing what the Petition identifies as the "first" and "second" metal interconnects.

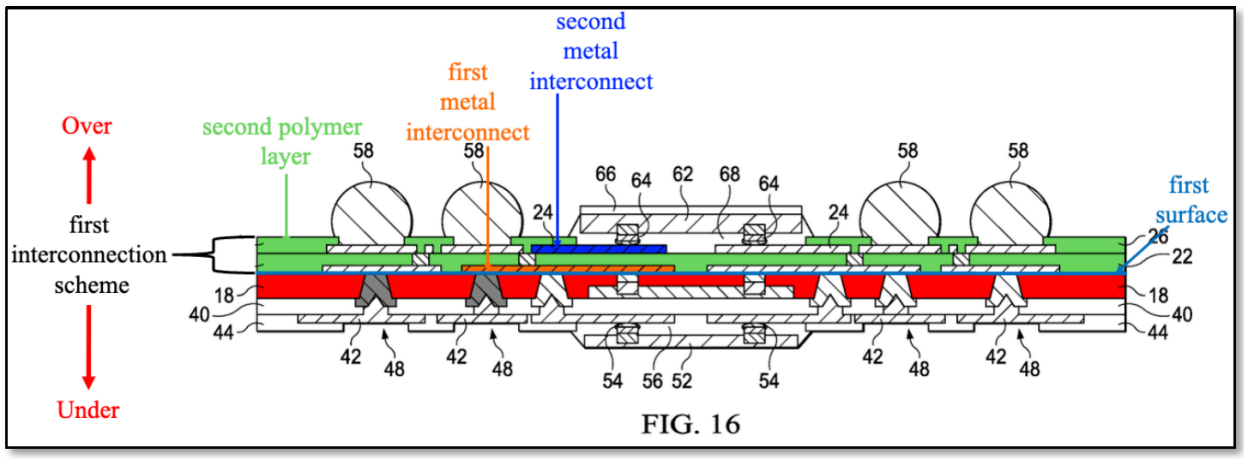


FIG. 16

Pet., 127.

238. The Petition therefore identifies two different portions of the *same* metallization layer 24 as two different claimed interconnects — the "second metal interconnect" and the "fourth metal interconnect." Two portions of a single metallization layer, lying on the same conductive path within the first interconnection scheme, are not two of the separate metal interconnects of that scheme. The "first metal interconnect," the "second metal interconnect" and the "fourth metal interconnect" must be different interconnects, and the Petition does not identify the claimed "fourth metal interconnect."

239. Claim 25 further requires that the "third metal interconnect compris[e] a second metal layer on said metal pad and a fifth copper layer over said second metal layer, wherein said fifth copper layer has a thickness between 5 and 30 micrometers." EX1001 ['768 Patent], cl. 25. This limitation is materially the same as limitation 1(f)(ii) of claim 1. For the reasons discussed above in connection with Grounds 1A and 2A, in my opinion Lin-191 does not disclose a single "second metal layer" on the metal pad, and the Petition therefore does not identify a "fifth copper layer over said second metal layer" of the claimed thickness. EX1005 [Lin-191], [0389]-[0390].

240. The Petition's own description of claim 25 confirms that the structures it identifies lie on a single conductive path. The Petition states that "Yu's third metal interconnect is connected to another portion of metallization layer 24 (fourth metal interconnect) through a portion of metallization layer 42, a TMV 38, the first metal interconnect, and a via." Pet., 144. That path runs through the structure the Petition identifies as the first metal interconnect and arrives at another portion of the same metallization layer 24 that the Petition identifies as the second metal interconnect.

XII. CONCLUSION

241. For at least the foregoing reasons, Petitioners have failed to demonstrate by a preponderance of the evidence that any challenged claim is unpatentable.

I, Dr. David S. Ricketts PhD, do hereby declare and state, that all statements are made herein of my own knowledge are true and that all statements made on information and belief are believed to be true. I am over the age of 21 and am competent to make this declaration. These statements were made with the knowledge that willful false statements are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Dated: August 7, 2026

David Ricketts

Dr. David S. Ricketts