

REDISTRIBUTION LAYERS

RDL: an integral part of today's advanced packaging technologies

EXECUTIVE OVERVIEW

Redistribution technology was developed out of necessity to allow fan-in area array packaging (bumping) to take hold when very few chips were being designed for area array. In the intervening years it has been instrumental in developing many of the newer packaging technologies such as wafer-level packaging (WLP), fan-out packaging, and TSV-based interposers and chip stacks.

The concept of flip-chip (FC) can be traced back to what IBM called "controlled collapse chip connection" (C-4) in the late 1960s. It has always been clear that FC is a superior interconnect based on size, I/O density, electrical and thermal performance. However, during the 1960s-1980s, the technology was mainly confined to high end main frame computer companies because the CTE mismatch between Si and PWB laminate required that FC use expensive ceramic packaging.

For FC to find widespread acceptance by those interested in miniaturized portable products such as lap tops, cell phones, pagers, camcorders etc., reliable lower cost FC processes were needed. In the early 1990s, IBM Japan reported that FC chips could be reliably attached directly to PWB laminate if the chips were underfilled. Unitive and Flip Chip Technologies (FCT) subsequently developed lower cost UBMs, lower cost solder deposition technologies (FCT - stencil printing; Unitive - plating) and redistribution (RDL). The FCT and Unitive technologies were licensed by all the key assembly houses including ASE, Amkor, STATSChipPAC and SPIL, as they initiated production in the early 2000s. This brought flip-chip technology to the masses.

RDL

The lack of area array designed chips was a major impediment to the early use of FC. RDL addressed this issue (Fig. 1) – defined by the addition of metal and dielectric layers onto the surface of the wafer to re-route the I/O layout into a new, looser pitch footprint. Such redistribution requires thin film polymers (BCB, PI or newer polymers such as Asahi Glass ALX) and metallization (Al or Cu) to reroute the peripheral pads to an area array configuration.

The redistribution trace can be fabricated directly on the primary passivation (SiN or SiON) or can be routed over a second layer of polymer to add additional compliancy.

It was widely assumed at the time that RDL was a stopgap measure

and its use would quickly diminish as chip designs migrated to area array. Indeed, RDL is used very little for bumped chips today (estimated at <5% of bumped chips by Amkor and FCI) but as we shall see, it has found a home in other advanced packaging technologies.

To incorporate high I/O FC devices onto a standard PWB, one was still required to use a

package, such as a BGA, to serve as an interposer, matching the chip I/O pitch with the pitch on the PWB.

It was discovered, however, that in low I/O devices, RDL could relax the I/O pitch on the chip and allow direct attachment to the PWB. To mitigate CTE stresses and avoid the use of underfill (slows throughput), larger diameter solder balls (250µm+ diameter) were used for this packaging. This low cost solution proved to be reliable for up to 5mm chips. This concept was first proposed by Sandia Labs in 1994 and called the mini BGA. The first commercialization of such a product was the FCT Ultra CSP, which was introduced in 1998. Soon afterward, Unitive came out with its Xtreme CSP. Over time, the nomenclature for such structures changed from mini-BGA, to wafer-level chip scale package "WL-CSP," to the simpler, wafer-level package "WLP" [1,2].

Fan-out packaging

In the early 2000s the question became how to use the WLP concept when larger numbers of I/O were required or how to maintain the same I/O and pitch during a die shrink. So called "fan-out" packaging (vs. traditional WLP, which is now called fan-in since all the I/O have to fit within the dimensions of the die) was developed to deal with this issue.

Infineon's embedded wafer-level BGA (eWLB) and Freescale's redistribution chip package (RCP) are two examples of fan-out WLP that have received significant industry attention. Infineon has licensed eWLB to STMicro, STATSChipPAC, and ASE. Freescale has licensed the RCP process to Nepes.

In the eWLB process a carrier wafer is laminated to dicing tape and known good die (KGD) are placed face down to create a "reconfigured wafer." This wafer is then compression molded to encapsulate it and the wafer carrier and tape are removed. The molding compound is used to carry the fan-out area and to protect the chip backside. An RDL (Fig. 2) is created on the now exposed die faces, the I/O are rerouted, solder balls are placed, and the die are singulated.

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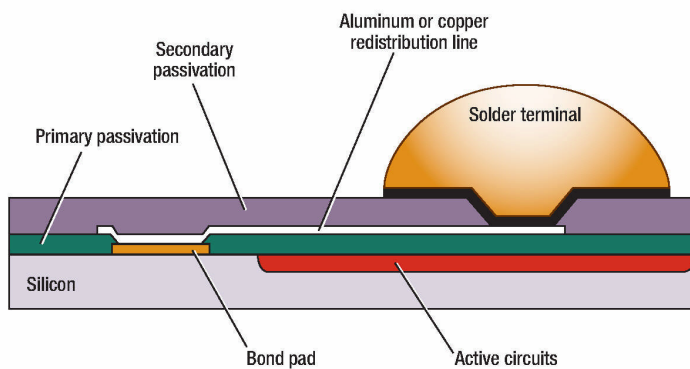


Figure 2. Examples of advanced packaging technologies using RDL.

3D stacking with TSV

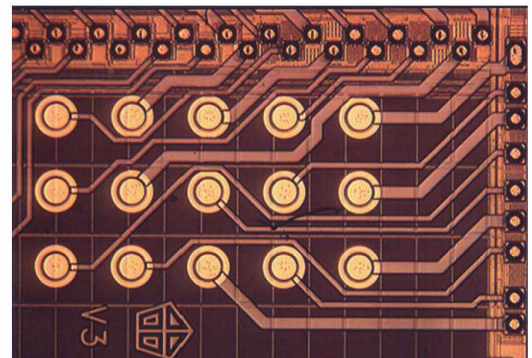
For the last few decades, IC technology has used shrinking gate dimensions and decreasing operating voltage to improve gate switching delay and thus device performance. As we look beyond the 32nm node, we find that fewer and fewer foundries/IDMs can afford to put <45nm generations of technology into place. In addition, further scaling has resulted in increased line resistance and capacitance for the smaller cross-section wires. Options to improve performance, at a reasonable cost, have become limited.

One solution that has been proposed is 3D Integration, where multiple layers of planar devices are stacked and interconnected through the silicon [3]. The resulting decreased chip area results in much shorter global interconnect, which results in less power required to drive signals the shorter distance.

Once the infrastructure is in place, it is hoped that 3D IC technology will reduce both risk and cost through economic benefits such as: a) reducing the time it takes to design and verify chips at the most advanced nodes; b) allowing the use of older analog IP blocks rather than having to develop new IP blocks at the most advanced process nodes; and c) allowing the mixing of normally incompatible technologies (heterogeneous integration).

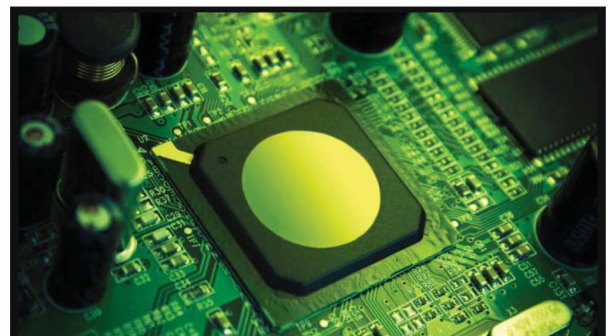
Three-dimensional technology can enable the integration of current off-chip memory (like L2 cache) onto the processor chip, thereby eliminating some of the slower and higher-power off-chip buses to off-chip memory and replacing them with high-bandwidth, low-latency vertical interconnections. In addition, on-chip memory (embedded) can be fabricated on a separate layer and bonded to the logic functions. Both of these options improve access latency, the former reducing interconnect length from tens of millimeters to tens of microns, and the latter allowing optimization of memory processing on a separate layer.

The key enablers of 3D include: 1) fabrication of the through silicon vias; 2) thinning the die/wafers to 50µm or less; 3) align and bond the die/wafers, usually through some form of metal-metal bonding. TSVs will be manufactured either in the fab/foundry during back end of line (vias middle), or after the die has been completed from the back side of the wafer (vias last-backside) by the foundry or OSAT (outsourced semiconductor and test). Backside TSV processing includes insulation and metallization of the TSV, backside RDL and bump placement. For the TSV last-backside processes, OSATs can use their standard polymer-based RDL processes, with minor alterations, to fabricate these structures. An example of this is STMicro's



300mm CMOS image sensor line in Crolle.

While stacking of die, such as memory, is made easier by having identical I/O, stacking other chips will require an I/O interface standardization that is not yet in place. In order to mate such die, silicon interposers with RDL (single or double-sided) are used. It is expected that interposers will function as a stop gap until standardization is in place to allow full wafer/die stacking. Recent commercialization announcements of 3D stacked memory have come from Elpida and Samsung. Product announcements using interposers have come from Xilinx (TSMC manufacturing the interposer) and IBM fabricating interposer-based modules for Semtech.



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Conclusion

While the initial use of RDL for fan-in die bumping has indeed diminished over the years since its inception, RDL technology has been instrumental in the development of many advanced packaging technologies such as fan-in and fan-out WLP, and TSV applications such as CMOS image sensor packaging, silicon interposers for 3D integration, and 3D integration with backside TSV.

Acknowledgments

Ultra CSP is a trademark of Flip Chip Technologies, and Xtreme CSP is a trademark of Unitive.

References

1. P. Garrou, "Wafer Level Packaging has Arrived," Semiconductor Int., Vol. 23, no. 12, 2000, p. 119.
2. P. Garrou, "Wafer Level Chip Scale Packaging (WL-CSP): An Overview," IEEE Trans. Advanced Packaging, Vol. 23, 2000, p. 198.
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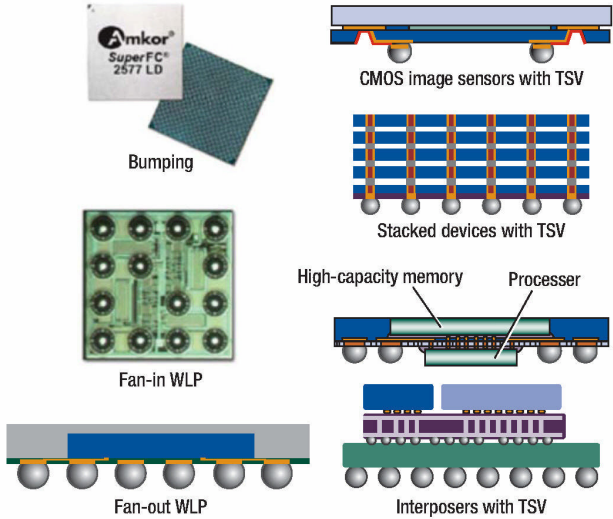


Figure 1. Bumping RDL.

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