UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY LTD.,

and

APPLE INC.,

Petitioners

v.

MYW SEMITECH, LLC,

Patent Owner

Inter Partes Review Case No. IPR2026-00066

U.S. Patent No. 11,538,763

DECLARATION OF STANLEY SHANFIELD, PH.D.

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4. 18(a)(ii): "wherein said solid layer has a thickness between 100 and 300 micrometers;" 192

5. *18(a)(iii): "wherein said solid layer comprises a first region and a second region between said first region and an edge of said solid layer;"* *192*

6. *18(b): "a plurality of metal conductors in said second region of said solid layer respectively,"* *192*

7. *18(b)(i): "wherein one of said plurality of metal conductors comprises a copper portion and a first metal layer covering a sidewall of said copper portion, wherein said copper portion has a diameter in a direction between 50 and 200 micrometers and greater than a thickness of said first metal layer in said direction,"* *192*

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12. *18(c)(iii): "wherein said first metal interconnect comprises a first copper layer;"* *197*

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9. 1(b)(ii): "wherein said first region has a width in a direction greater than a shortest distance between said sidewall of one of said plurality of through vias and said edge of said solid layer in said direction and greater than a pitch between two neighboring copper plugs of said plurality of copper plugs;"....242

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Claim 1:

Claim 1(Pre): A chip package comprising:

Claim 1(a): a solid layer having a first surface and a second surface opposite to said first surface,

Claim 1(a)(i): wherein said first surface is substantially parallel to said second surface,

Claim 1(a)(ii): wherein said solid layer comprises a compound of silicon and oxygen,

Claim 1(a)(iii): wherein said solid layer has a thickness between 100 and 300 micrometers,

Claim 1(a)(iv): wherein said solid layer comprises a first region and a second region between said first region and an edge of said solid layer;

Claim 1(b): a plurality of copper plugs in a plurality of through vias in said second region of said solid layer respectively,

Claim 1(b)(i): wherein one of said plurality of copper plugs comprises a first copper layer contacting a sidewall of one of said plurality of through vias,

Claim 1(b)(ii): wherein said first region has a width in a direction greater than a shortest distance between said sidewall of one of said plurality of through vias and said edge of said solid layer in said direction and greater than a pitch between two neighboring copper plugs of said plurality of copper plugs;

Claim 1(c): a first interconnection scheme over said first surface,

Claim 1(c)(i): wherein said first interconnection scheme comprises a first metal interconnect over said first surface, a second metal interconnect over said first surface and a first polymer layer over said first and second metal interconnects,

Claim 1(c)(ii): wherein said first metal interconnect is connected to a first copper plug of said plurality of copper plugs, wherein said second metal interconnect is connected to a second copper plug of said plurality of copper plugs,

Claim 1(c)(iii): wherein said first metal interconnect comprises a first metal layer and a second copper layer over said first metal layer,

Claim 1(c)(iv): wherein a top surface of said second copper plug and a top surface of said first copper plug are substantially in the same horizontal plane;

Claim 1(d): a first metal bump over said first interconnection scheme,

Claim 1(d)(i): wherein said first metal bump comprises a second metal layer and a tin-containing layer over said second metal layer; and

Claim 1(e): a first semiconductor chip under said first interconnection scheme,

Claim 1(e)(i): wherein said first semiconductor chip comprises a third metal interconnect on a first metal pad of said first semiconductor chip,

Claim 1(e)(ii): wherein said third metal interconnect comprises a third metal layer on said first metal pad and a third copper layer over said third metal layer, wherein said third copper layer has a thickness between 5 and 30 micrometers.

Claim 2:

The chip package of claim 1, further comprising a passive component over said first interconnection scheme and connected to said first interconnection scheme through a solder layer.

Claim 3:

The chip package of claim 1, wherein said first interconnection scheme comprise a fourth metal interconnect across over a sidewall of the first semiconductor chip.

Claim 4:

Claim 4(a): The chip package of claim 1, further comprising a second semiconductor chip over said first interconnection scheme,

Claim 4(b): wherein said second semiconductor chip comprises a second metal bump between said second semiconductor chip and said first interconnection scheme.

Claim 5:

The chip package of claim 1, wherein said first semiconductor chip comprises a central-processing-unit (CPU) circuit block and a graphics-processing-unit (GPU) circuit block.

Claim 6:

Claim 6(a): The chip package of claim 1, further comprising a second semiconductor chip under said first semiconductor chip,

Claim 6(b): wherein said first semiconductor chip comprises a second metal pad on a top surface of said first semiconductor chip, a third metal pad on a bottom surface of said first semiconductor chip

Claim 6(c): a through-silicon-via metal layer connects to said second metal pad,

Claim 6(d): wherein said third metal pad is connected to a fourth metal pad of said second semiconductor chip.

Claim 7:

Claim 7(a): The chip package of claim 1, wherein said first interconnection scheme further comprises a fourth metal interconnect over said first metal interconnect and said first polymer layer,

Claim 7(b): wherein said first polymer is between said first and fourth metal interconnects,

Claim 7(c): wherein said fourth metal interconnect comprises a fourth metal layer, a fourth copper layer on said fourth metal layer, and a fifth copper layer on said fourth copper layer**.**

Claim 8:

The chip package of claim 1, further comprising a second interconnection scheme under said solid layer and on said second surface.

Claim 9:

The chip package of claim 1, wherein said first metal pad is an aluminum pad.

Claim 10:

The chip package of claim 1, wherein said solid layer further comprises a third region opposite to said second region, wherein said third region is between said first region and another edge of said solid layer, wherein said plurality of copper plugs in said plurality of through vias in said third region respectively.

Claim 11:

The chip package of claim 1, wherein said first copper plug has a thickness between 100 and 300 micrometers.

Claim 12:

The chip package of claim 1, wherein said plurality of copper plugs comprise a third copper plug vertically in one of said plurality of through vias in said solid layer, wherein a pitch between said first and third copper plugs is between 200 and 1000 micrometers.

Claim 13:

The chip package of claim 1, wherein said second region is a rectangle region and surrounding said first region.

Claim 14:

Claim 14(a): The chip package of claim 1, further comprising a second semiconductor chip over said first interconnection scheme and connected to said first interconnection scheme through a second metal bump,

Claim 14(b): wherein said second semiconductor chip has a height is between a backside surface of said second semiconductor chip and a top surface of said first polymer layer is smaller than a thickness of said first metal bump.

Claim 15:

The chip package of claim 1, wherein no any copper plug in said first region.

Claim 16:

The chip package of claim 1, further comprising a second semiconductor chip under said first interconnection scheme next to said first semiconductor chip.

Claim 17:

The chip package of claim 1, wherein said compound comprises a SiO2 compound.

Claim 18:

Claim 18(Pre): A chip package comprising:

Claim 18(a): a solid layer having a first surface and a second surface opposite to said first surface,

Claim 18(a)(i): wherein said solid layer comprises a compound of silicon and oxygen,

Claim 18(a)(ii): wherein said solid layer has a thickness between 100 and 300 micrometers,

Claim 18(a)(iii): wherein said solid layer comprises a first region and a second region between said first region and an edge of said solid layer;

Claim 18(b): a plurality of metal conductors in said second region of said solid layer respectively,

Claim 18(b)(i): wherein one of said plurality of metal conductors comprises a copper portion and a first metal layer covering a sidewall of said copper portion, wherein said copper portion has a diameter in a direction between 50 and 200 micrometers and greater than a thickness of said first metal layer in said direction,

Claim 18(b)(ii): wherein said first region has a width in said direction greater than a shortest distance between a sidewall of one of said plurality of metal conductors and said edge of said solid layer in said direction and greater than a pitch between two neighboring metal conductors of said plurality of metal conductors;

Claim 18(c): a first interconnection scheme over said first surface,

Claim 18(c)(i): wherein said first interconnection scheme comprises a first metal interconnect over said first surface and a first polymer layer over said first metal interconnect,

Claim 18(c)(ii): wherein said first metal interconnect is connected to a first metal conductor of said plurality of metal conductors,

Claim 18(c)(iii): wherein said first metal interconnect comprises a first copper layer;

Claim 18(d): a second interconnection scheme under said second surface,

Claim 18(d)(i): wherein said second interconnection scheme comprises a second metal interconnect under said second surface and a second polymer layer under said second metal interconnect,

Claim 18(d)(ii): wherein said second metal interconnect is connected to a second metal conductor of said plurality of metal conductors,

Claim 18(d)(iii): wherein said second metal interconnect comprises a second copper layer; and

Claim 18(e): a first semiconductor chip under said first interconnection scheme,

Claim 18(e)(i): wherein said first semiconductor chip comprises a first metal bump on a first metal pad of said first semiconductor chip,

Claim 18(e)(ii): wherein said first metal bump comprises a third copper layer with a thickness between 5 and 30 micrometers,

Claim 18(e)(iii): wherein said first semiconductor chip is connected to a third metal interconnect of said second interconnection scheme through said first metal bump.

Claim 19:

The chip package of claim 18, wherein said compound comprises a SiO2 compound.

Claim 20:

The chip package of claim 18, further comprising a first passive component under said first interconnection scheme.

Claim 21:

The chip package of claim 18, wherein said first semiconductor chip comprises a central-processing-unit (CPU) circuit block and a graphics-processing-unit (GPU) circuit block.

Claim 22:

The chip package of claim 18, wherein said first metal layer is a silver-containing layer.

Claim 23:

The chip package of claim 18, wherein said solid layer further comprises a third region opposite to said second region, wherein said third region is between said first region and another edge of said solid layer, wherein said plurality of metal conductors in said third region.

I, Stanley Shanfield, declare as follows:

I. INTRODUCTION

1. I have been retained by counsel for Petitioners as a technical expert in the above-captioned case. Specifically, I have been asked to render certain options regarding the IPR petition with respect to U.S. Patent No. 11,538,763 (the "'763 Patent"). I understand that the Challenged Claims are 1-23, and my opinions are limited to those claims. A true and correct copy of my Curriculum Vitae, which provides further details about my background and experience, is appended to this Declaration.

A. *Educational Background and Professional Experience*

2. In 1977, I received a B.S. Degree in Physics *cum laude* from the University of California, Irvine. I received a Ph.D. in Physics from Massachusetts Institute of Technology in 1981.

3. After obtaining my Ph.D. in 1981, I was a Staff Scientist at Spire Corporation in Bedford, Massachusetts. From 1985-1999, I worked at Raytheon Corporation. As staff and later as section manager, among many other projects, I developed reactive ion etching (RIE) processes for patterning dielectrics (silicon dioxide, silicon nitride, silicon oxynitride, etc.), conductive layers (aluminum-copper, copper-silicon, W-silicide, TaN, doped polysilicon, etc.) and organic layers

(photoresist, polyimide, etc.). In 1996, I became the Manager of Semiconductor Operations at Raytheon. As Manager, I built and led a 300-employee, $60 million revenue-generating semiconductor development, commercial system design, and electronic module manufacturing operation. I worked directly with engineers in the selection, installation, and optimization of several chemo-mechanical polishing systems (CMP), including analysis of operational maintenance and performance monitoring. The manufacturing facility eventually used multiple production CMP systems, and I directly participated in establishing the required metrology (optical thickness monitoring) for maintaining polishing uniformity standards.

4. In 1999, I was a co-founder and became Vice President of Operations at AXSUN Technologies in Bedford/Billerica, Massachusetts and later became Director of Manufacturing and Wafer Fab Technology.

5. In 2003, I joined the Draper Laboratory in Cambridge, Massachusetts. Currently, I am the Division Leader of Advanced Hardware Development, with around 80 staff members; a Distinguished Member of Technical Staff; and Technical Director. I led the Advanced Hardware Development division in relaunching a multi-chip integrated circuit module facility. The laboratory has acquired several semiconductor-grade CMP systems for the purpose of fabricating multi-chip modules and for planarization operations in MEMS devices, and I have been

involved in their operation and optimization. I invented and led the implementation of an ultra-miniature electronics fabrication technology. I also developed fabrication technology for semiconductor-based low-phase noise oscillator design. I have received many awards at Draper, including the 2010 Distinguished Performance Award and the 2010 Best Patent Award.

6. During the 1990's I developed early stacked-chip plastic packages while working for Raytheon. Additionally, I have led the implementation and qualification of MCM-D (multi-chip module – deposited) technology for military and space applications during my time at Draper Labs. Also during my time at Draper Labs, I have (1) developed improved fabrication and test methods for advanced multichip modules using ceramic and glass packages, (2) led efforts involving die thinning, copper interconnect plating, and component stacking at multiple interconnect levels, (3) managed thermo-mechanical modeling efforts to assess packaging reliability under demanding conditions, and (4) oversaw a large team of next-gen multichip module process development at Draper (2010-2015). Additionally, I am an inventor on U.S. Patent No. 7,727,806 which is directed to systems and methods for high density multi-component modules.

B. ***Materials Considered***

7. I have relied upon my education, knowledge, and experience with semiconductor chip packaging, as well as the other materials as discussed in this declaration in forming my opinions.

8. In developing my opinions, I have considered the following materials:

Exhibit 1001	U.S. Patent No. 11,538,763
Exhibit 1002	File History of the '763 Patent
Exhibit 1004	U.S. Patent No. 9,167,694 to Sundaram, et al.
Exhibit 1005	U.S. Patent Publication No. 2010/0290191 to Lin, et al.
Exhibit 1006	U.S. Patent Publication No. 2011/0215458 to Camacho, et al.
Exhibit 1007	U.S. Patent No. 9,679,863 to Lin, et al.
Exhibit 1008	U.S. Patent Publication 2011/0266691 to Lin, et al.
Exhibit 1009	Intentionally left blank
Exhibit 1010	U.S. Patent No. 9,123,763 to Yu, et al.
Exhibit 1011	U.S. Patent Publication 2014/0035935 to Shenoy, et al.
Exhibit 1012	Andrea Chen, et al. *Semiconductor Packaging Materials Interaction and Reliability*, CRC Press, 2012
Exhibit 1013	Philip Garrou, et al., *RDL: an integral part of today's advanced packaging technologies*, Solid State Technology, May 2011

Exhibit 1014	U.S. Patent No. 8,780,576 to Haba, et al.
Exhibit 1015	U.S. Patent No. 7,902,648 to Lee
Exhibit 1016	U.S. Patent No. 7,964,961 to Lee, et al.
Exhibit 1017	U.S. Patent No. 7,241,641 to Savastiouk, et al.
Exhibit 1018	U.S. Patent Publication No. 2005/0110168 to Chuang
Exhibit 1019	U.S. Patent Publication No. 2011/0026232 to Lin, et al.
Exhibit 1020	U.S. Patent No. 5,086,558 to Grube, et al.
Exhibit 1021	U.S. Patent Publication No. 2011/0193219 to Lai, et al.
Exhibit 1022	U.S. Patent No. 6,818,545 to Lee, et al.
Exhibit 1023	U.S. Patent No. 6,974,659 to Su, et al.
Exhibit 1024	U.S. Patent Publication No. 2006/0175686 to Murata, et al.
Exhibit 1025	U.S. Patent Publication No. 2012/0098124 to Wu, et al.
Exhibit 1026	U.S. Patent No. 8,193,604 to Lin et al.
Exhibit 1027	U.S. Patent Publication No. 2004/0203224 to Halahan, et al.
Exhibit 1028	Philip Garrou, *Introduction to 3D Integration,* Handbook of 3D integration: Volumes 1 and 2, Technology and Application of 3D Integrated Circuits, 2012
Exhibit 1029	U.S. Patent Publication No. 2003/0068877 to Kinsman

Exhibit 1030	U.S. Patent Publication No. 2010/0246152 to Lin, et al.
Exhibit 1031	Yi Yang, et al, *CPU-Assisted GPGPU on Fused CPU-GPU Architectures,* IEEE Xplore
Exhibit 1032	File History of U.S. Patent No. 11,107,768
Exhibit 1033	U.S. Patent No. 4,863,773 to Rousseau, et al.
Exhibit 1034	U.S. Patent No. 6,365,265 to Tose, et al.
Exhibit 1035	E.D. Blackshear, et al., *The evolution of build-up package technology and its design challenges*, International Business Machines Corporation, 2005
Exhibit 1036	Intentionally Left Blank
Exhibit 1037	U.S. Patent No. 7,374,969 to Cho, et al.
Exhibit 1038	U.S. Patent No. 7,199,036 to Chan, et al.
Exhibit 1039	U.S. Patent No. 8,158,508 to Lin, et al.
Exhibit 1040	U.S. Patent No. 6,619,538 to Test, et al.
Exhibit 1041	U.S. Patent Publication No. 2011/0101523 to Hwang, et al.
Exhibit 1042	U.S. Patent No. 6,831,003 to Huang, et al.
Exhibit 1043	U.S. Patent Publication No. 2009/0226611 to Suzuki, et al.
Exhibit 1044	U.S. Patent No. 6,077,726 to Mistry, et al.

Exhibit 1045	U.S. Patent Publication No. 2010/0244245 to Pendse, et al.
Exhibit 1046	U.S. Patent Publication No. 2012/0206160 to Wu, et al.
Exhibit 1047	U.S. Patent Publication No. 2009/0174052 to Sogawa, et al.,
Exhibit 1048	U.S. Patent Publication No. 2013/0100624 to Carpenter, et al.
Exhibit 1049	U.S. Patent No. 7,047,515 to Vitek, et al.
Exhibit 1050	U.S. Patent No. 8,116,097 to Love, et al.
Exhibit 1051	U.S. Patent Publication No. 2009/0237900 to Origuchi, et al.
Exhibit 1052	U.S. Patent Publication No. 2005/0002167 to Hsuan, et al.
Exhibit 1053	U.S. Patent Publication No. 2008/0067695 to Chow, et al.
Exhibit 1054	U.S. Patent No. 6,489,240 to Iacoponi, et al.
Exhibit 1055	U.S. Patent No. 6,578,178 to Mau
Exhibit 1056	U.S. Patent Publication No. 2012/0001190 to Okabe, et al.
Exhibit 1057	U.S. Patent No. 7,307,348 to Wood, et al.
Exhibit 1058	U.S. Patent No. 8,138,014 to Chi, et al.
Exhibit 1059	U.S. Patent No. 6,506,672 to Dagenais, et al.
Exhibit 1060	U.S. Patent No. 8,518,798 to Graetz
Exhibit 1061	U.S. Patent Publication No. 2009/0261473 to Lee, et al.
Exhibit 1062	U.S. Patent No. 6,440,289 to Woo, et al.

Exhibit 1063	U.S. Patent No. 6,812,143 to Lane, et al.
Exhibit 1064	U.S. Patent Publication No. 2012/0145552 to Nagai, et al.
Exhibit 1065	U.S. Patent Publication No. 2011/0147950 to Tsi, et al.
Exhibit 1066	U.S. Patent Publication No. 2009/0070727 to Solomon
Exhibit 1067	U.S. Patent Publication No. 2012/0098114 to Ishibashi
Exhibit 1068	U.S. Patent Publication No. 2011/0074028 to Pendse
Exhibit 1069	U.S. Patent No. 7,485,955 to Kang, et al.
Exhibit 1070	U.S. Patent Publication No. 2012/0104623 to Pagaila, et al.
Exhibit 1071	Intentionally left blank
Exhibit 1072	U.S. Patent No. 7,772,880 to Solomon
Exhibit 1073	U.S. Patent No. 7,989,270 to Huang, et al.
Exhibit 1074	U.S. Patent Publication No. 2011/0304999 to Yu, et al
Exhibit 1075	U.S. Patent Publication No. 2009/0117327 to Takada
Exhibit 1076	U.S. Patent Publication No. 2005/0081744 to Klocke, et al.,
Exhibit 1077	U.S. Patent No. 6,291,082 to Lopatin
Exhibit 1078	Intentionally left blank
Exhibit 1079	Intentionally left blank
Exhibit 1080	U.S. Patent Publication No. 2012/0319251 to Yu, et al.

Exhibit 1081-1089	Intentionally left blank
Exhibit 1090	U.S. Patent Publication No. 2005/0156280 to Patel, et al.
Exhibit 1091-1092	Intentionally left blank
Exhibit 1093	U.S. Patent No. 6,107,180 to Munroe, et al.
Exhibit 1094	U.S. Patent Publication No. 2011/0210283 to Ramirez, et al.
Exhibit 1095	U.S. Patent No. 6,452,502 to Dishongh, et al.
Exhibit 1096	U.S. Patent No. 6,344,401 to Lam.
Exhibit 1097	Richard K. Ulrich, et al., *Advanced Electronic Packaging,* IEEE Press Series on Microelectrical Systems, 2006
Exhibit 1098	Mulugeta Abtew, et al., *Lead-free Solders in Microelectronics*, Materials Science and Engineering, 2000
Exhibit 1099	Karl J. Puttlitz, et al., *Handbook of Lead-Free Solder Technology for Microelectronic Assemblies*, 2005
Exhibit 1100	U.S. Patent Publication No. 2013/0309832 to Cheng, et al.
Exhibit 1101	U.S. Patent Publication No. 2013/0151869 to Steinman, et al.

Exhibit 1102	Linely Gwennap, *Sandy Bridge Spans Generations: Intel Focuses on Graphics, Multimedia in New Processor Design*, Microprocessor, 2010
Exhibit 1103	U.S. Patent No. 6,330,164 to Khandros, et al.
Exhibit 1104	U.S. Patent No. 6,710,447 to Nogami.
Exhibit 1105-1126	Intentionally left blank
Exhibit 1127	U.S. Patent No. 8,238,113 to Iihola, et al.
Exhibit 1128	Intentionally left blank
Exhibit 1129	U.S. Patent No. 6,468,413 to Fanti, et al.
Exhibit 1130	U.S. Patent No. 8,132,775 to Goldmann.
Exhibit 1131	U.S. Patent Publication No. 2011/0186977 to Chi, et al.
Exhibit 1132	U.S. Patent No. 7,169,627 to Duh, et al.
Exhibit 1133	U.S. Patent No. 6,614,243 to Klehn, et al.
Exhibit 1134	U.S. Patent Publication No. 2009/0162622 to Van Veen, et al.
Exhibit 1135	U.S. Patent No. 6,570,259 to Alcoe, et al.
Exhibit 1136	U.S. Patent No. 7,741,567 to Beddingfield, et al.
Exhibit 1137	U.S. Patent No. 6,407,341 to Anstrom, et al.

9. I have considered these materials from the viewpoint of a POSITA as of the priority date of the ’763 Patent. For the purposes of this declaration, I have been asked to assume that the priority date of the ’763 Patent is September 26, 2012. I note that my opinions provided in this Declaration are made from the perspective of a POSITA as of this priority date of the ’763 Patent unless expressly stated otherwise. To the extent that I use any verb tense in this Declaration that is present tense (e.g., “a POSITA would understand” instead of “a POSITA would have understood”), such verb tense should be understood to be my opinion as of the ’763 Patent’s priority date (again, unless expressly stated otherwise). I merely use the present verb tense for ease of reading.

II. OVERVIEW AND LEGAL STANDARDS

10. In formulating my opinions, I have been instructed to apply certain legal standards. I am not a lawyer. I do not offer any testimony regarding what the law is. Instead, the following sections summarize the law as I have been instructed to apply it in formulating and rendering my opinions found later in this declaration. I understand that, in an *inter partes* review (“IPR”) proceeding, patent claims may be deemed unpatentable if it is shown that they are anticipated or rendered obvious in view of the prior art. I understand that prior art in an IPR review is limited to patents or printed publications that predate the priority date of the patent at issue. I

understand that questions of claim clarity (definiteness) and enablement cannot be considered as a ground for considering the patentability of a claim in these proceedings.

A. *Person of Ordinary Skill in the Art*

11. I understand that the ’763 Patent, the record of the proceedings at the Patent Office (which I understand is called the “File History” or “Prosecution History”), and the teachings of the prior art are evaluated from the perspective of a person of ordinary skill in the art (“POSITA”). I understand that the factors considered in determining the ordinary level of skill in the art may include: (i) the levels of education of the inventor; (ii) the types of problems encountered in the art; (iii) prior art solutions to those problems; (iv) the rapidity with which innovations are made; (v) the sophistication of the technology; and (vi) the educational level of persons working in the field.

12. I understand that a person of ordinary skill in the art is not a specific real individual, but rather a hypothetical individual having the qualities reflected by the factors above. The hypothetical person is presumed to have the same level of skill as the typical practitioner of the art and is presumed to have knowledge of all prior art in the relevant field. I understand that the inventor’s actual knowledge or

lack of knowledge of prior art reference is irrelevant to the obviousness determination.

B. *Obviousness*

13. I understand that a claim may be invalid under 35 U.S.C. § 103(a) if the subject matter described by the claim as a whole would have been "obvious" to a POSITA in view of a single or combination of prior art references at the time the claimed invention was made. I further understand that a POSITA is assumed to know and to have all relevant prior art in the field of endeavor covered by the patent-in-suit and all analogous prior art. I understand that obviousness in an IPR review proceeding is evaluated using a preponderance of the evidence standard, which means that the claims must be more likely obvious than nonobvious.

14. I also understand that an obviousness determination includes the consideration of various factors including: (1) the scope and content of the prior art, (2) the differences between the prior art and the claim at issue, and (3) the level of ordinary skill in the pertinent art. I understand that secondary considerations of non-obviousness such as commercial success, long-felt but unresolved needs, failure of others, and so forth may be assessed as well. I have been informed that an obviousness analysis must consider the full scope of the claims to avoid impermissibly using hindsight to invalidate a patent.

15. In considering whether certain prior art renders a particular patent claim obvious, I have been informed that I can consider the scope and content of the prior art, including the fact that a POSITA would regularly look to the disclosures in patents, trade publications, journal articles, conference papers, industry standards, product literature and documentation, texts describing competitive technologies, requests for comment published by standard setting organizations, and materials from industry conferences, as examples.

16. I have been informed that for a prior art reference to be proper for use in an obviousness analysis, the reference must be "analogous art" to the claimed invention. A reference is analogous art if: (1) the reference is from the same field of endeavor as the claimed invention (even if it addresses a different problem); or (2) the reference is reasonably pertinent to the problem faced by the inventor (even if it is not in the same field of endeavor as the claimed invention). For a reference to be "reasonably pertinent" to the problem, it must logically have commended itself to an inventor's attention in considering the problem. In determining whether a reference is reasonably pertinent, one should consider the problem faced by the inventor, as reflected either explicitly or implicitly, in the specification. I believe that the documents I considered in forming my opinions in this IPR are well within the

range of documents a POSITA would have consulted to address the type of problems described in the Challenged Claims.

17. I have been informed that to establish that a claimed invention was obvious based on a combination of prior art elements, an articulation of the reason(s) why a claimed invention would have been obvious must be provided. Specifically, I have been informed that the prior art, either as a single reference or a combination of multiple items of prior art, renders a patent claim obvious when there was an apparent reason for a POSITA, at the time of the invention, to combine or modify the prior art. Rationales for combining or modifying the prior art include, but are not limited to, any of the following: (A) combining prior art methods according to known methods to yield predictable results; (B) substituting one known element for another to obtain predictable results; (C) using a known technique to improve a similar device in the same way; (D) applying a known technique to a known device ready for improvement to yield predictable results; (E) trying a finite number of identified, predictable potential solutions, with a reasonable expectation of success; (F) identifying that known work in one field of endeavor may prompt variations of it for use in either the same field or a different one based on design incentives or other market forces if the variations are predictable to one of ordinary skill in the art; or (G) identifying an explicit teaching, suggestion, or motivation in the prior art that

would have led one of ordinary skill to modify the prior art reference or to combine the prior art references to arrive at the claimed invention.

18. I have also been informed that where there is a motivation to combine, claims may be rejected as obvious provided a POSITA would have had a reasonable expectation of success regarding the proposed combination. I have also been informed that common sense may be considered. Common sense teaches that familiar items may have obvious uses beyond their primary purposes. I have been informed that if the combination was obvious to try (regardless of whether it was actually tried) or leads to anticipated success, then it is likely the result of ordinary skill and common sense rather than non-obvious innovation.

19. I have been informed that the existence of an explicit teaching, suggestion, or motivation to combine known elements of the prior art is a sufficient, but not a necessary, condition to a finding of obviousness. In determining whether the subject matter of a patent claim is obvious, neither the particular motivation nor the avowed purpose described in the patent-in-suit controls. I have been further informed that the obviousness analysis may consider the effects of demands known to the technological community or present in the marketplace and the background knowledge possessed by a POSITA. These issues may be considered to determine

whether there was an apparent reason to combine the known elements in the fashion claimed by the patent.

20. I have been informed that it is improper to combine references where the references teach away from their combination. A reference may be said to teach away when a POSITA, upon reading the reference, would be discouraged from following the path set out in the reference, or would be led in a direction divergent from the path that was taken by the patent applicant. I have also been informed that a reference does not teach away if it merely expresses a general preference for an alternative invention but does not criticize, discredit, or otherwise discourage investigation into the invention claimed.

21. I am informed that even if a case of obviousness is established, the final determination of obviousness must also consider "secondary considerations" if presented. Secondary considerations include: (a) commercial success of a product due to the merits of the claimed invention; (b) a long-felt, but unsatisfied need for the invention; (c) failure of others to find the solution provided by the claimed invention; (d) deliberate copying of the invention by others; (e) unexpected results achieved by the invention; (f) praise of the invention by others skilled in the art; (g) lack of independent simultaneous invention within a comparatively short space of time; and (h) teaching away from the invention in the prior art.

22. I have been further informed that secondary considerations evidence is only relevant if the offering party establishes a connection, or nexus, between the evidence and the claimed invention. The nexus cannot be based on prior art features. The establishment of a nexus is a question of fact. While I understand that Patent Owner here has not offered any secondary considerations at this time, I will supplement my opinions should Patent Owner raise secondary considerations during the course of this proceeding.

C. *Claim Construction*

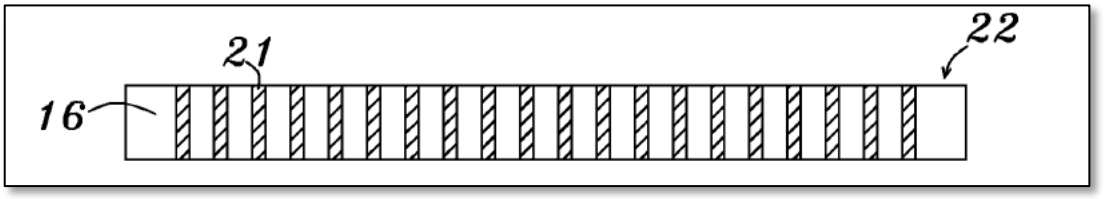
23. I understand that the claim terms in an IPR proceeding are construed according to their plain and ordinary meaning as understood in light of the claim language, the patent's description, and the prosecution history viewed from the perspective of a POSITA. I further understand that where a patent defines claim language, the definition of the patent controls, even if there are other definitions that might be understood by those working in the art.

III. OVERVIEW OF THE '763 PATENT

A. *Summary of the '763 Patent*

24. The '763 Patent describes a chip package having a "second substrate 22" with an "amorphous solid glass layer/body 16 and multiple metal plugs 21" wherein the "amorphous solid glass layer/body 16 having a top surface and an

opposing bottom surface and the metal plugs 21 extending through the amorphous solid glass layer/body 16 beginning at the top surface and ending at the bottom surface." *EX1001* at 11:3-11.



EX1001 at FIG. 8a.

25. The '763 Patent further describes the metal plugs are "formed from metal traces 6." *EX1001* at 7:66–8:1. To obtain the plugs, the metal traces 6 are (1) stretched (6:1-8, FIG. 6a); (2) placed in a mold (6:34-40, FIG. 6d); (3) a polymer is filled into the mold (6:54-60, 7:45-48); and (4) cut into "multiple first substrates 20," which comprises "multiple seconds substrates 22" that each have "multiple metal plugs 21." *EX1001* at 7:54-67, FIGS. 6j-6k.

26. As shown below in FIG. 9b, a "first dielectric layer 24" that may be a "polymer (such as polyimide…)" is formed "formed on the top surface of the first substrate 20." *EX1001* at 11:41-49. "Multiple openings 24a are formed in the first dielectric layer 24 to expose the metal plugs 21" by "etching." *EX1001* at 11:55-58.

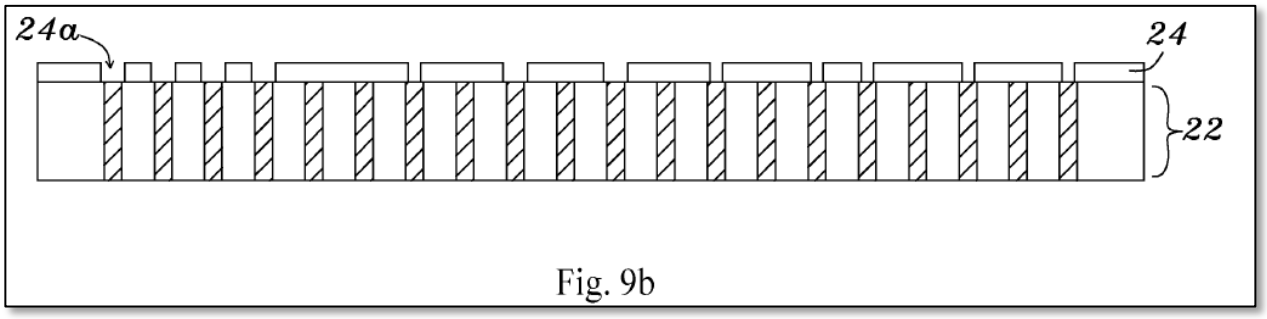
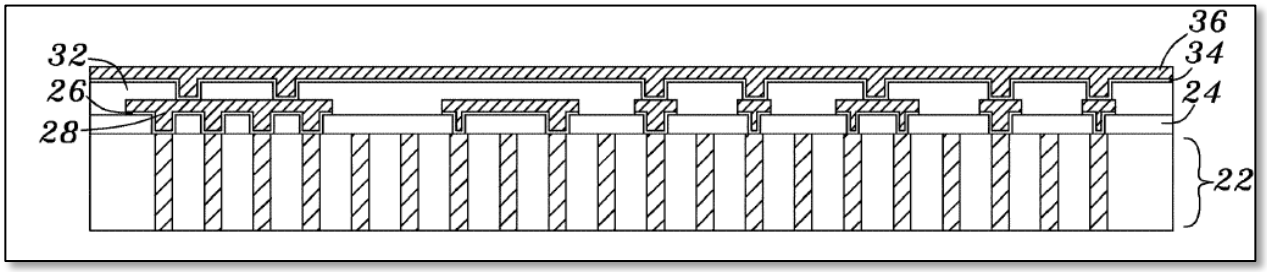


Fig. 9b

EX1001 at FIG. 9b.

27. A "first metal layer 26 is formed on the first dielectric layer 24, on the metal plugs 21 and in the openings 24" that "may include an adhesion/barrier layer, such as a layer of titanium…" *EX1001* at 11:62-64. Next, a "second metal layer 28 is formed on the first metal layer 26" that "maybe comprises copper." *EX1001* at 12:7-9. A "second dielectric layer 32 is formed on the first dielectric layer 24 and on the second metal layer 28" that may be "a polymer[.]" *EX1001* at 12:32-39. Multiple "openings 32a are formed in the second dielectric layer 32 to expose the second metal layer 28" then a "third metal layer 34 is formed on the second dielectric layer 32, on the second metal layer 28 and in the openings 32a." *EX1001* at 12:47-56. A "fourth metal layer 36 is formed on the third metal layer 34." *EX1001* at 12:66-67.



EX1001 at FIG. 9k.

28. A "third dielectric layer 40 is formed on the second dielectric layer 32 and on the fourth metal layer 36" that may be a "polymer[.]" *EX1001* at 13:25-31. Multiple "openings 40a are formed in the third dielectric layer 40 to expose the fourth metal layer 36" then a "protecting layer 42 is formed in the openings 40a, on the third dielectric layer 40 and on the fourth metal layer 36[.]" *EX1001* at 13:46-48. Multiple "chips 46 and chips 56" are "set up over the third dielectric layer 40 through a flip-chip package process" where the "chip 46 comprises multiple metal pads 48 and multiple metal bumps 50 formed on the metal pads 48." *EX1001* at 13:60-62, 14:12-15.

29. The '763 Patent further describes a "metal bump 72" that may have "an adhesion/barrier metal layer 61…a metal seed layer 63 formed on the adhesion/barrier metal layer 61, an electroplated metal layer 65 formed on the metal seed layer 63 and a solder layer 67 formed on the electroplated metal layer 65." *EX1001* at 14:57-63. The "electroplated metal layer 65 comprises a copper layer" and the "solder layer 67 can be formed" of "gold-tin alloy, tin-silver alloy, tin-silver copper alloy, indium, tin-bismuth allow or other lead-free alloy." *EX1001* at 15:1-4.

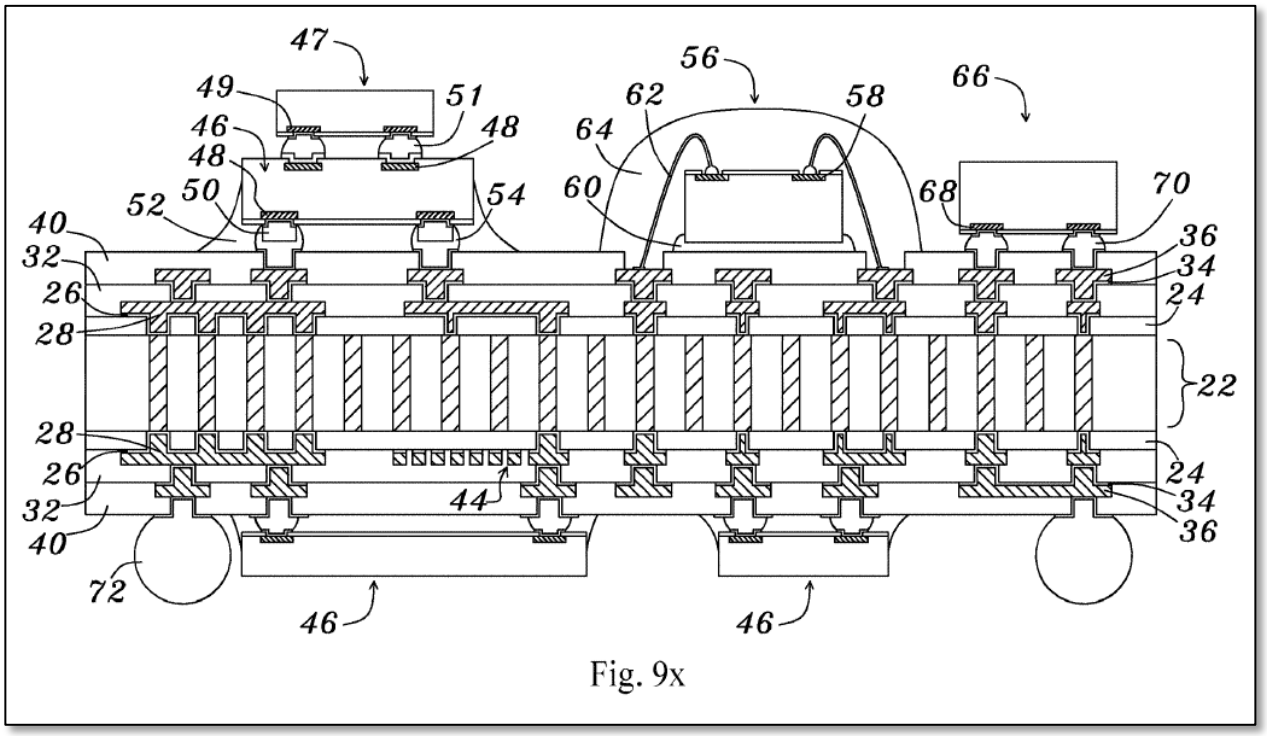


Fig. 9x

EX1001 at FIG. 9x.

30. As I will explain in detail below, there is nothing novel about the disclosure or claims of the ‘763 Patent. The claims as a whole recite a litany of claim elements that were both well-known on their own and well-known in combination with other recited claim elements. For example, the claims recite well-known features such as metal interconnects, copper plugs, semiconductor chips, and metal bumps, all of which were commonplace in chip packages before well before the ’763 Patent. Furthermore, the claimed region[s] and relative distances of the region[s] describe a fan-out chip package, which was a common chip package type before the ’763 Patent.

B. *Field of Endeavor*

31. I have been informed that the field of endeavor of the claimed invention can be determined by reference to explanations of the invention's subject matter in the patent application, including the embodiments, function, and structure of the claimed invention.

32. The '763 Patent, titled "Chip Package" generally relates to semiconductor packaging. *EX1001* at Title. The '763 Patent describes that "microelectronic devices have a tendency to be minimized and thinned with its functional development and a semiconductor package mounted on a mother board is also following the tendency in order to realize a mounting of high integration" *EX1001* at 1:26-31. The described embodiments "illustrates a cross-section view of multiple chips and a 3D-IC package…" *EX1001* at 3:34-37. Additionally, the '763 Patent describes that "chips 46 are set up…through a flip-chip package process." *EX1001* at 14:12-13.

33. Further still, the '763 Patent expressly places its work in the context of flip-chip technology, explaining that "flip-chip technology fabricates bumps… on Al pads of chip and interconnects the bumps directly to the package media" and that this arrangement provides "the highest density of interconnection to the device and a very low inductance interconnection to the package" *EX1001* at 1:49-65. For these

reasons, a POSITA would understand that the field of endeavor of the ‘763 Patent includes semiconductor packaging. *EX1001* at 1:27-67.

C. *Problem Solved by the Inventors of the ‘763 Patent*

34. I have been informed that a prior art reference is “reasonably pertinent” if a POSITA would have consulted it and applied its teachings when faced with the problem(s) that the inventor was trying to solve. As such, I have been asked to analyze the ’763 Patent and determine the problem(s) that the inventors were trying to solve.

35. The ’763 Patent recognizes the problem of "TCE (Temperature Coefficient of Expansion) matching to avoid solder bump fatigue [is] still [a] challenge[]" *EX1001* at 1:58-64. Thus, a POSITA would have understood the ‘763 Patent is directed, in part, to solving the problem of minimizing temperature coefficient of expansion mismatching in semiconductor packages.

36. The ’763 Patent also explains that "pre-testability, post-bonding visual inspection… [is] still [a] challenge[]" *EX1001* at 1:61-62. Thus, a POSITA would have understood the ‘763 Patent to be directed, in part, to solving the problem of creating chip packages with pre-testability capability.

37. Further, the ’763 Patent states that “with the further miniaturization of the IC” there is “an increasingly negative impact on the circuit performance.”

EX1001 at 1:37-38. Thus, a POSITA would have understood the '763 Patent to be directed, in part, to solving the problem the impact of miniaturization on circuit performance.

38. Additionally, the '763 Patent describes that "parasitic capacitance and resistance of the metal interconnections increase, which degrades the chip performance significantly." *EX1001* at 1:38-40. Thus, a POSITA would have understood the '763 Patent to be directed, in part, to solving the problem the impact of parasitic capacitance of interconnections in a semiconductor chip.

IV. LEVEL OF ORDINARY SKILL

39. Based on my review and analysis of the '763 Patent, the cited prior art, and the ordinary skill factors described in this section, a POSITA in the field of the '763 Patent at the time of the earliest possible priority date (September 26, 2012) would have had a at least a bachelor's degree in electrical engineering, materials science, or physics (or an equivalent degree), and at least two years of experience in semiconductor design or semiconductor manufacturing. A master's degree or Ph.D. in a relevant field may substitute for some work experience or vice versa. Additional education or experience might substitute for the above requirements. When I refer to the understanding of a POSITA, I am referring to the understanding of such a person as of September 26, 2012.

V. OVERVIEW OF THE TECHNOLOGY

40. I was asked to briefly summarize the background of the prior art from the standpoint of a person having ordinary skill in the art prior to September 26, 2012. As explained below, the chip packaging technology described by the '763 Patent was based on well-known packaging techniques and chip package structures. Thus, the techniques discussed in the '763 Patent were well-known and conventional prior to the invention of the '763 Patent.

A. *History of Chip Packaging*

41. Chip packaging technology was known and widely used well before the priority date of the '763 Patent. In fact, semiconductor chip packaging had been in development at least 40 years in advance of the 2012 priority date of the '763 Patent with the 1960s seeing "rapid proliferation of new packages for ICs" as a response to the development of silicon planar technology and higher pin count versions of early metal can packages. *EX1097* at p. 8. Additionally, "[p]ackaging costs also received considerable attention during the 1960s while the industry was deciding which package or packages would become standard[.]" along with "early attempts to develop a low-cost, hermetic package[.]" *EX1097* at p. 11, *see also EX1012* at p. 4. Subsequently, plastic packaging, more specifically, the plastic version of the dual

in-line packaging (DIP) family was "introduced in the early 1970s[.]" *EX1012* at p. 4.

42. Eventually, "the early 1990s saw the emergence of both pin grid array (PGA) and ball grid array (BGA) packages" responsive to the ultimate goal for high-performance electronic systems to "pack devices as close together as possible in order to minimize circuit path length." *EX1097* at p. 12. "MCM technology, still a viable technology today, played a major role in the evolution of multichip packaging in the 1990s, which includes three-dimensional (3D) stacking of ICs within a single package[.]" *EX1097* at p. 15.

43. Traditional wire bonding techniques were eventually replaced with flip-chip package technology, "[n]amely, the chip is not wire bonded for interconnect but instead flipped face-to-face with the substrate surface—hence the name *flip chip*—and the interconnection between the die and substrate is made through an array of bumps that are placed on the bonding pads of the die surface." *EX1012* at p. 18.

44. "The concept of flip-chip (FC) can be traced back to what IBM called 'controlled collapse chip connection' (C-4) in the late 1960s. It has always been clear that FC is a superior interconnect based on size, I/O density, electrical and thermal performance. However, during the 1960s-1980s, the technology was mainly

confined to high end main frame computer companies because the CTE mismatch between Si and PWB laminate required that FC use expensive ceramic packaging." *EX1013* at p. 1.

45. "For FC to find widespread acceptance by those interested in miniaturized portable products such as lap tops, cell phones, pagers, camcorders etc., reliable lower cost FC processes were needed. In the early 1990s, IBM Japan reported that FC chips could be reliably attached directly to PWB laminate if the chips were underfilled. Unitive and Flip Chip Technologies (FTC) subsequently developed lower cost UBMs [(under bump metallization)], lower cost solder deposition technologies (FCT – stencil printing; Unitive – plating) and redistribution (RDL). The FCT and Unitive technologies were licensed by all the key assembly houses… as they initiated production in the early 2000s. This brought flip-chip technology to the masses." *EX1013* at p. 1.

46. Flip chip packages were recognized as providing a number of benefits and solutions, namely, "for low to high pin count, high electrical performance demands from high-end memory, ASICs, and microprocessor applications where high frequency and high speed are required." *EX1012* at p. 18.

47. In particular, it was known that "[f]lip-chip interconnections allow better electrical performance through lower inductances due to the shorter electrical

path between the chip and the substrate. The array of bumps under the chip also allows the die to shrink in size, which can reduce wafer cost. The flip-chip structure also allows you to make power and ground connections to internal points on a die, resulting in better chip performance. To increase thermal performance, optional heat spreaders can be attached on the backside of the flipped die." *EX1012* at p. 18.

B. *Interposers and Dielectric Materials*

48. "Interconnection components, such as interposers are used in electronic assemblies to facilitate connection between components with different connection configurations or to provide needed spacing between components in a microelectronic assembly. Interposers can include a dielectric element [electrically insulating] in the form of a sheet or layer of dielectric material having numerous conductive traces extending on or within the sheet or layer. The traces can be provided in one level or in multiple levels throughout a single dielectric layer, separated by portions of dielectric material within the layer." *EX1014* at 1:5-14. Within chip packages, such as a BGA package, an interposer was known to be used for "matching the chip I/O pitch with the pitch on the PWB." *EX1013* at p. 1.

49. "Conventionally, semiconductor dice have been packaged in plastic or, less commonly, in ceramic packages." *EX1015* at 1:50-51. Therefore, materials such as plastic (i.e., polymer) and ceramic were known and commonly used within the

field of chip packaging. In particular, polymer materials, such as, epoxy and polyimide, as well as ceramic materials, such as, silica (silicon dioxide), were commonly used as dielectric/insulation layers within interposer structures for chip packaging. *See, e.g., EX1016* at 23:10-13 (providing epoxy or polyimide as options for "insulating layers 320 and 330"); *EX1016* at 24:1-10 (specifying that the substrate 300 (BGA) may be a "glass fiber reinforced epoxy" or alternatively, a "ceramic substrate").

50. "Packages may support, protect, and dissipate heat from semiconductor dice. Packages may also provide external connective elements for providing power and signal distribution to and from semiconductor dice, as well as for facilitating electrical testing, such as burn-in testing and circuit evaluation, of semiconductor dice prior to or after assembly thereof with higher level components, such as carrier substrates or circuit boards." *EX1015* at 1:51-58. Thus, it would have been understood that a polymer substrate layer would have a suitable thickness to support and protect the coupled semiconductor devices, as well as to support mechanical processes such as drilling to form vias or "receptacles." Specifically, Lee teaches "[s]ubstrates 12 that are formed from resins, or polymers, may have receptacles 11 formed therein by mechanical processes, such as drilling (including laser drilling), punching, milling, or die cutting." *EX1015* at 8:38-41.

51. Savastiouk teaches a silicon substrate of an interposer with a thickness that "can be 100 μm or less." *EX1017* at 4:32-34. Savastiouk also suggests a larger thickness by specifying "silicon substrate 140 can be thicker than described above[.]" *EX1017* at 4:47-50. Therefore, in light of the teachings of Savastiouk interposer substrates were known to include thicknesses of at least 100 μm.

52. Further, it was known to provide interposers with materials other than silicon. Specifically, polymer-based interposers such as epoxy substrates with thicknesses within the range of 100 to 300 μm were known. Specifically, Lee-961 teaches "[t]he substrate 300 may be a ball grid array (BGA) substrate with a thickness [] of between 200 and 2,000 μm. Alternatively, **the substrate 300 may be a glass fiber reinforced epoxy based substrate with a thickness [] of between 200 and 2,000 μm**. Alternatively, the substrate 300 may be a silicon substrate with a thickness [] of between 200 and 2,000 μm. Alternatively, the substrate 300 may be a ceramic substrate with a thickness t15 of between 200 and 2,000 μm. Alternatively, the substrate 300 may be an organic substrate with a thickness t15 of between 200 and 2,000 μm." *EX1016* at 24:1-10 (emphasis added.) Similarly, Haba-576 teaches "**First support portion 12 can, in some embodiments, have a thickness between 50 μm and up to 300 μm**, although a greater thickness is possible. First support portion 12 can be of a dielectric material, **such as a polymeric resin material, for**

example polyimide, glass, or fiber-reinforced epoxy." *EX1014* at 7:24-29 (emphasis added).

53. Additionally, Haba-576 teaches that "first support portion 12 further includes an inside surface 16 that is generally parallel to outside surface 14 and spaced apart therefrom to define a thickness of first support portion 12," where "in an embodiment, first support portion 12 has a thickness of at least 5 μm" and "can, in some embodiments, have a thickness between 50 μm and up to 300 μm … [and] can be of a dielectric material such as a polymeric resin material, for example polyimide, glass, or fiber-reinforced epoxy" *EX1014* at 7:20-29. Haba-576 further teaches that "[f]irst in-process unit 10A includes first support portion 12 having first conductive vias 122 formed therein and first dielectric layer 52 formed over inside surface 16 of first support portion 12." *EX1014* at 15:9-12. Thus, it was known that polymer layers, such as the first support portion 12 of Haba-576 could be fabricated at least up to 300 μm, while still supporting structures such as conductive vias 122.

54. Dielectric materials such as polymers were also used to form chip packages with dies/chip embedded in the dielectric layer. For example, Chi-977 teaches a chip package having a "semiconductor die 138" and an "encapsulant or molding compound 148 [that] is deposited over die 138." *EX1131* at [0046]. The encapsulant 148 "can be a polymer composite material, such as epoxy resin with

filler, epoxy acrylate with filler, or polymer with proper filler." *EX1131* at [0046]. As shown below, a plurality of "conductive pillars 156" are formed in encapsulant 148 having "a height ranging from 20-200 micrometers (μm)." *EX1131* at [0048]. As shown, the encapsulant/molding compound 148 has a height equal to the conductive pillars, demonstrating that dielectric/polymer layers were known to be formed at such a height. *EX1131* at FIG. 4. Further, dielectric/polymer layers having Chi-977's thickness were known to "environmentally protect[] the semiconductor device from external elements and contaminants." *EX1131* at [0046].

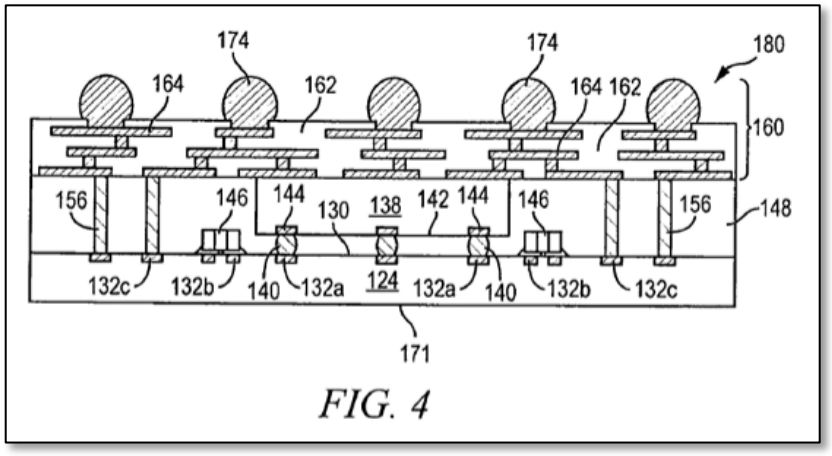


FIG. 4

EX1131 at FIG. 4.

C. *Coefficient of Thermal Expansion*

55. The problem of mismatch of the coefficient of thermal expansion between packaging materials was well known. In particular, it was well known that "The thermal expansion mismatch between the chip and underfill causes stress

concentrations in certain locations, like at a die corner. As the crack propagates during continued stressing, the crack opens up the chip–underfill interface or another weakened section, causing either interconnect fatigue or an electrical failure in the chip's dielectric." *EX1012* at p. 45. As a result of this understanding, temperature cycling tests were typically employed in evaluating package reliability. "The purpose of temperature cycling is to check on package integrity in spite of the coefficient of thermal expansion mismatches between the various materials and their respective interfaces within the plastic package[.]" and that "[a]ll the components—the semiconductor chip, the metal lead frame or organic substrate, the polymer-based molding compound or die attach adhesive—within a package will likely have very different expansion and contraction rates while being heated or otherwise thermally stressed[.]" *EX1012* at p. 48-52. "Temperature cycling and thermal shock are the cause of numerous failure modes in semiconductor packages. Some of these modes include broken bond wire or lifted bonds from pads, solder joint/bump/ball fatigue (an example of which is shown in Figure 5.5), cracked molding compound, and the aforementioned interface delamination. *EX1012* at p. 54.

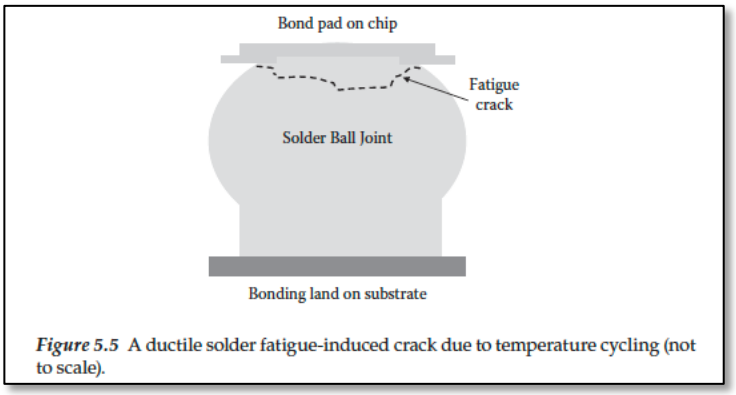


Figure 5.5 A ductile solder fatigue-induced crack due to temperature cycling (not to scale).

EX1012 at FIG. 5.5.

56. It was known that while "epoxy alone has a very high coefficient of thermal expansion, around 80 × 10–6/ºC, compared to the silicon chip or copper lead frame or organic substrate[.]" (*EX1012* at p. 68) there were known techniques to reduce the coefficient of thermal expansion to more closely match that of silicon. Notably, "[f]illing the epoxy with silica filler brings down the thermal expansion coefficient into the teens, which would match the lead frame or substrate but would still be high compared to silicon. Using biphenyl or similar epoxy types allows more filler to be added and brings the coefficient down to the high single digits but still not as low as silicon, which is about 3 × 10–6/ºC." *EX1012* at p. 68.

57. Chuang teaches "a low-CTE packaging material for assembling a semiconductor die into a package[.]" *EX1018* at [0004]. Specifically, Chuang suggests that "[a] low-CTE die attach material 318 preferably comprises an epoxy with a negative-CTE filler, such as zirconium tungstate (ZrWOs), halfnium tungstate

(HfWOs), or a solid solution of zirconium and halfnium tungstate (Zos HfsWOs). Filler materials have a lower CTE than the packaging material in which they are mixed. This is generally done to more closely approximate the CTE of a silicon die, which may be about 3 ppm/C." *EX1018* at [0019]. Thus, it was well understood that low-CTE polymer-based materials, such as a filled epoxy, could be used as a packaging material to more closely match the coefficient of thermal expansion of silicon.

D. ***Through Vias and Metal Plugs***

58. It was widely known that through vias could be disposed through an interposer substrate to provide a conductive path between the top and bottom of the interposer substrate. For example, Savastiouk teaches that "silicon substrate 140 includes metalized through-silicon vias 330 that pass between the top and bottom surfaces of substrate 140. Conductive paths are provided from contact pads 136C at the top of the interposer to contact pads 340 at the bottom of the interposer through the vias 330." *EX1017* at 4:51-56.

59. Vias were also known to be used in non-silicon interposers. For example, Haba-576 teaches a first support portion 12, which "can be a dielectric material. Such as a polymeric resin material, for example polyimide, glass, or fiber-reinforced epoxy[.]" (*EX1014* at 7:26-29) and further that "[t]he interposer can also

include conductive elements such as conductive vias extending through the layer of dielectric material to interconnect traces in different levels." *EX1014* at 1:14-17.

60. Through vias were metalized with materials such as copper to provide electrically conductive paths through an interposer. For example, Haba teaches that "first conductive vias 22 are of a conductive material such as metal including copper, gold, nickel, aluminum, etc." *EX1014* at 7:44-47. Additionally, Savastiouk teaches that "[c]onductive paths are provided from contact pads 136C at the top of the interposer to contact pads 340 at the bottom of the interposer through the vias 330." *EX1017* at 4:54-56; *see also I.D*, 5:54-61, 7:58-59.

61. It was commonly understood that metal plugs could be positioned in vias. Specifically, Lin-232 teaches "The layers 52, 54 and 56 in the through vias 170 v compose multiple metal plugs (or metal vias) 5 p in the through vias 170v, including metal plugs (or metal vias) 5a, 5b, 5c, 5d, 5e and 5f in the through vias 170a, 170b, 170c, 170d, 170e and 170f as shown in FIG. 23, respectively." *EX1019* at [0141].

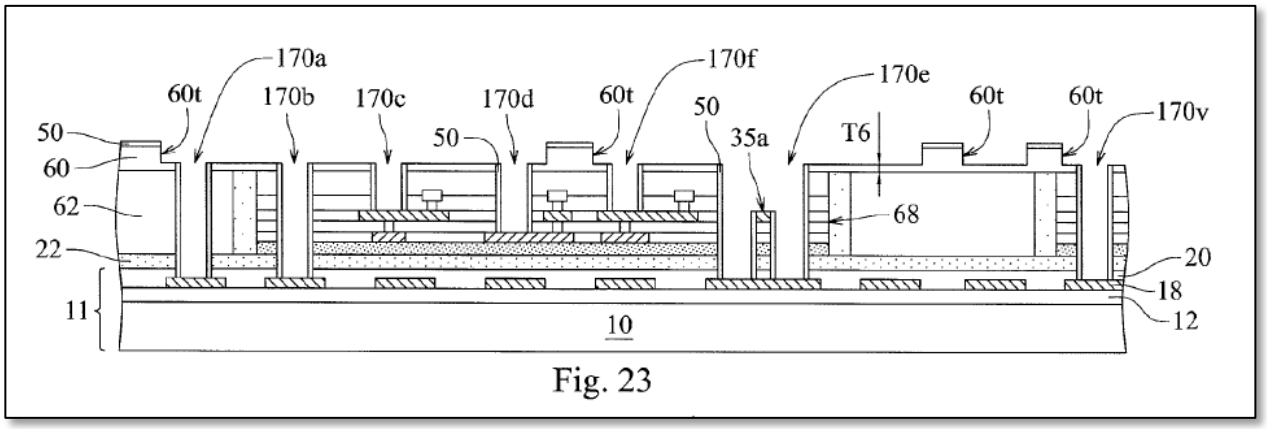


Fig. 23

EX1019 at FIG. 23.

62. Additionally, it was well known that the vias could be positioned into a pattern to match a contact pattern of a respective chip. For example, Grube teaches placing chips upon an interposer sheet with "each chip being positioned on a conforming via pattern[.]" *EX1020* at Abstract. The via patterns are taught as "conforming to the contact patterns of the chips." *EX1020* at 2:42-47.

63. Similarly, via patterns could be arranged in other specific geometries, such as along the perimeter of the substrate. For example, Figure 3.5 of Chen, shown below, illustrates a ball grid array with respective solder balls coupled to vias arranged along the perimeter of the package with an open central region most clearly illustrated in the bottom view.

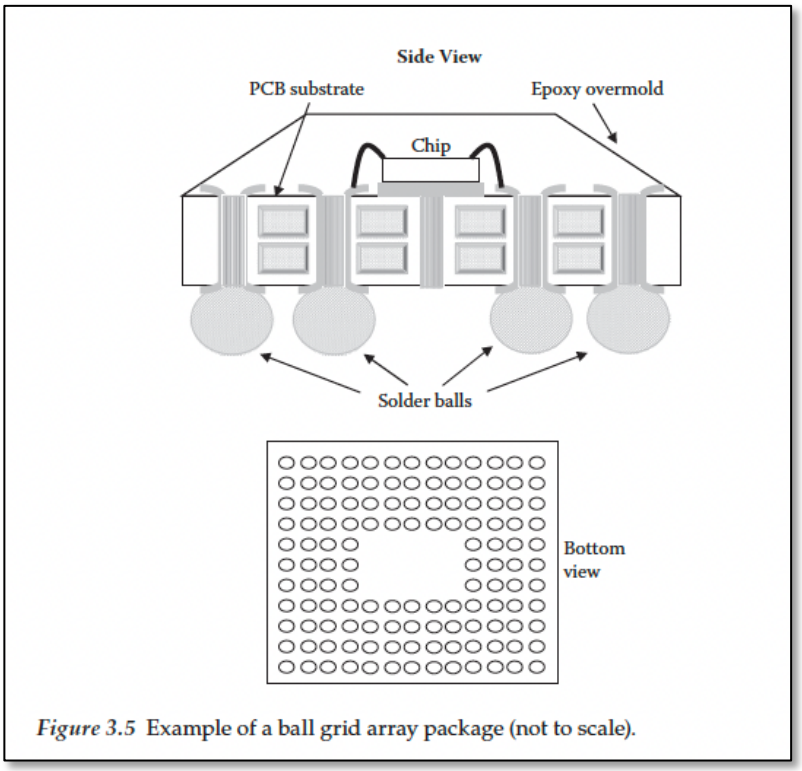


Figure 3.5 Example of a ball grid array package (not to scale).

EX1012 at Figure 3.5, p. 29.

E. *Solder Bumps*

64. Within chip packaging solder bumps were widely used as an interconnection means between packaging components prior to September 26, 2012. Specifically, Chen teaches "[w]afer bumping is necessary to create an electrical and physical connection between a chip and a substrate in lieu of wire bonding. This method is used in flip-chip packaging and in wafer-level chip scale packaging." *EX1012* at p. 121. Additionally, Chen illustrates an exemplary flip-chip interconnect including a solder bump.

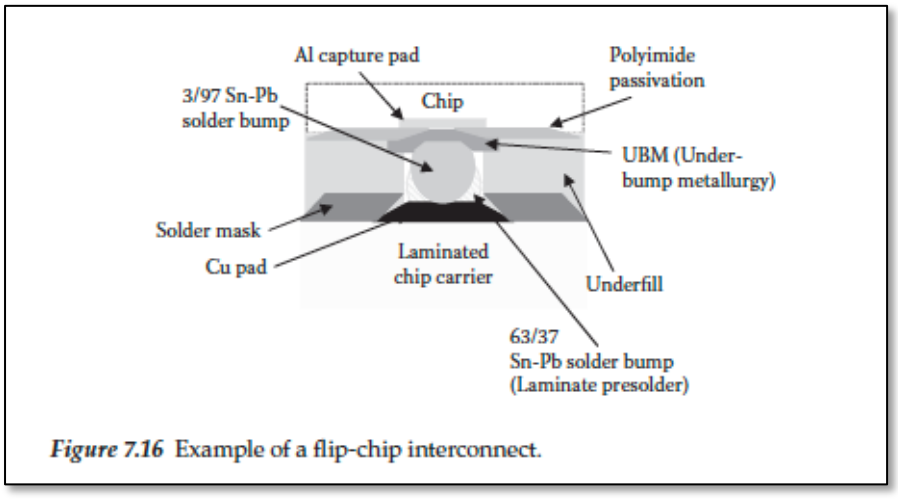


Figure 7.16 Example of a flip-chip interconnect.

EX1012 at FIG. 7.16, p. 122.

65. As shown in the above image, solder bumps were formed on the metal pads of a chip (an "Al capture pad" in the above image). Indeed, in flip-chip packaging "solder bumps are firstly formed on the metal pad of a chip" then the chip "is put on a substrate" and the solder bumps "are aligned with pads of the substrate, and the chip and substrate are processed by means of heat treatment of reflow." *EX1132* at 1:40-45. "After the solder [is] melted, it forms a ball by means of surface tension, such that the connection between the chip and the substrate is complete." *EX1132* at 1:44-47.

66. It was well known that solder contained "pure tin, a tin-silver alloy, a tin-lead alloy or a tin silver-copper alloy[.] *EX1016* at 46:5-7. Additionally, referring to the European Union's RoHS (Restriction of Hazardous Substances) directive made effective in 2006, "with RoHS and other 'green' initiatives, there is the move

toward Pb-free solders and alternate bump metallurgies." *EX1012* at p. 123. Thus, motivation was present at least as early as 2006 to replace traditional lead-based solders with lead-free solder compositions, such as those taught by Lai, which contained tin (Sn). Specifically, Lai teaches a lead-free solder system with a lead-free solder layer 22 that "is SnAg with Ag content being controlled lower than 1.6 weight percent (wt%)." *EX1021* at [0022].

67. Additionally, it was known that solder bump structures could include multiple layers. For example, Lee'545 teaches a solder bump structure having layers including: barrier layers that "are typically used to prevent diffusion of an interconnect metal into surrounding layers of dielectric and silicon[.]" *EX1022* at 8:42-44; a pillar metal layer, notably, "a layer 38 of pillar metal has been deposited (electroplated) over the surface of the layer 36 of barrier material[.]" *EX1022* at 9:61-63; and an under-bump-metallurgy layer with "Layer 40 of UBM, typically of nickel and of a thickness between about 1 and 10 μm, is electroplated over the layer 38 of pillar metal." *EX1022* at 10:19-21.

68. Multiple layers of distinct compositions were known to provide benefits within solder bump structures, such as "the improvement of adhesion of the various overlying layers or the prevention of diffusion of materials between adjacent layers." *EX1022* at 3:49-56.

69. "The conductive bumps formed or placed on the bond pads fulfill several important electrical and mechanical functions. For one thing, it would be physically necessary to create a mechanical and electrical interconnect between the thin, recessed aluminum IC pads to a substrate land. Another issue is that connecting solder directly to aluminum is very tricky at best, but a thin metal layer would probably end up "leached" or dissolved by solder. A sandwich of various metallic layers, usually called the under-bump metallization or UBM, could prevent any material diffusion that would adversely affect the integrity of the connection. The bumps also insured a controlled gap between chip and substrate. If the chip and substrate were touching or nearly so, any CTE mismatch could result in high stress concentrations. By adding a gap, the bumps provide some stress relief." *EX1012* at p. 122.

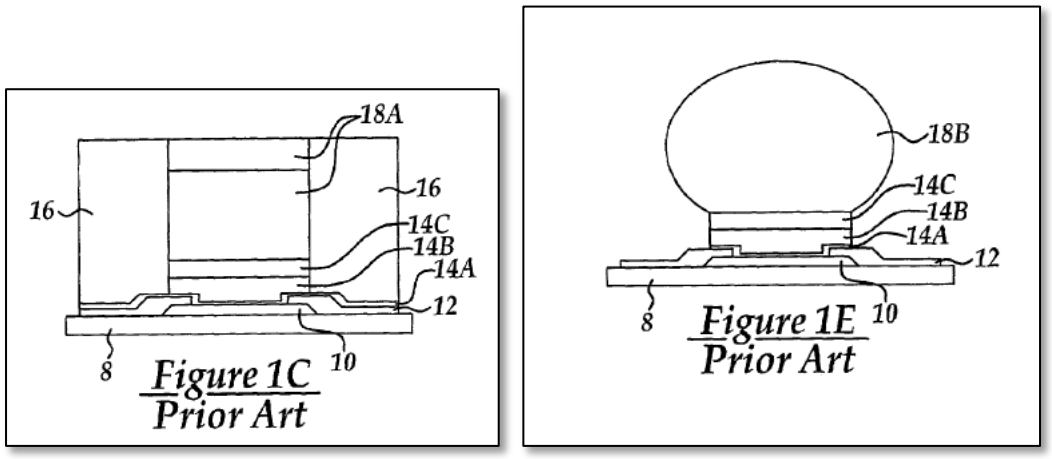
70. A common type of solder bump was known as 'Controlled Collapse Chip Connection" or "C4" bumps. The "basic idea of C4 is to connect chips (semiconductor devices), chip packages, or such other units by means of solder bumps between two surfaces of the units." *EX1129* at 1:9-17. The "tiny bumps of electrically conductive solder bridge the gaps between respective pairs of metal pads on the units being connected. Each pad has a corresponding pad on the other unit's surface; the pad arrangements are mirror images. As the units are pressed together

and heated the solder bumps on the pads of the first unit are contacted with corresponding conductive pads (having no bumps) on the second unit and reflowed, partially collapsing the solder bumps and making connections between respective pads" *EX1129* at 1:17-26. Conventionally, C4 bumps are "made from lead tin solder" but "lead-free requirements" required manufactures to "implement new ways to produce chip to substrates joints. For example, solder interconnects consisting of tin/copper, tin/silver and SAC alloys have been used as a replacement for leaded solder interconnects." *EX1130* at 1:15-31.

F. ***Methods of Forming Solder Bumps***

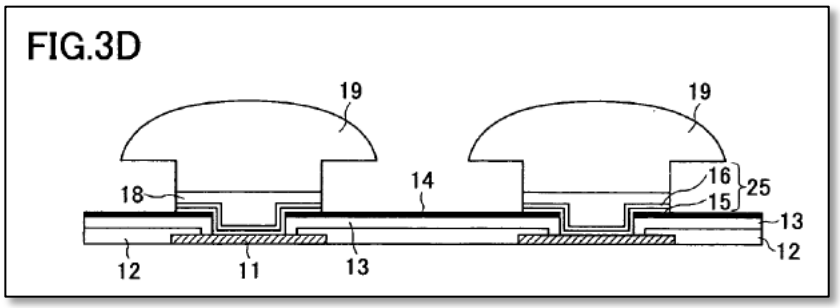
71. As I will detail herein, solder bumps/balls were typically formed by depositing layer(s) of solder material then performing a reflow step to form a spherical bump/ball geometry. For example, as shown below in FIG. 1C, a "column of solder material 18A may either be deposited in layers, for example, a layer of Pb followed by a layer of Sn, the solder material layers later being formed into a homogenous solder during a first reflow process[.]" *EX1023* at 2:45-39. "If the column of solder material is inhomogenous…a first reflow process is typically performed to harden the printed solder paste and form a homogenous column (plug) of solder material confined by the photoresist layer 16[.]" *EX1023* at 2:42-48. After

the photoresist layer 16 is removed, the "solder column 18 is then heated to reflow to form a solder bump 18B…as shown in FIG. 1E." *EX1023* at 2:55-57.

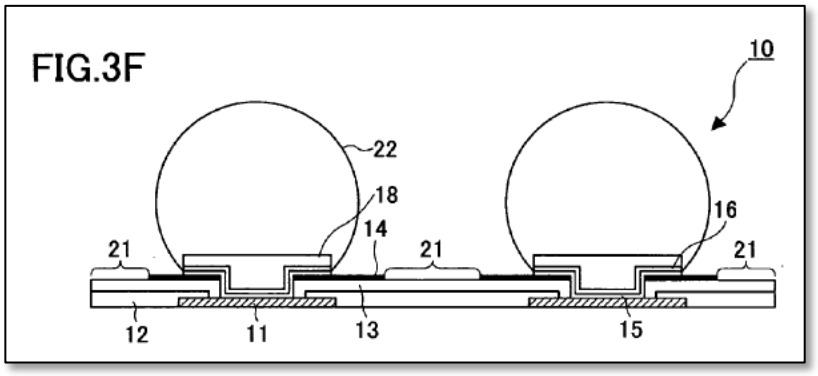


EX1023 at FIGS. 1C, 1E.

72. As another example, a solder bump may be formed by "plating" a "solder layer 19" that may be "an appropriate material, such as Sn/Cu, Sn/Ag, Sn/Ag/Cu, or Pb/Sn" in and on a resist 17. *EX1024* at [0046]; FIG. 3C. As shown below, in FIG. 3D, the "resist 17 may be removed" then "as illustrated in FIG. 3F, a "reflow treatment is performed to form a bump 22[.]" *EX1024* at [0049].



EX1024 at FIG. 3D.



EX1024 at FIG. 3F.

73. Wu-124 also demonstrates how solder balls/bumps are formed. Specifically, "as shown in FIG. 2C, a metallization layer 22 and a **solder material layer 24** are successfully formed in the opening 21" of a masker layer 20. "The solder material 24 is "electroplated within the opening 21 of the mask layer 20," and as a result "the solder material layer retains a pillar shape within the opening 21." *EX1025* at [0018]-[0019] (emphasis added).

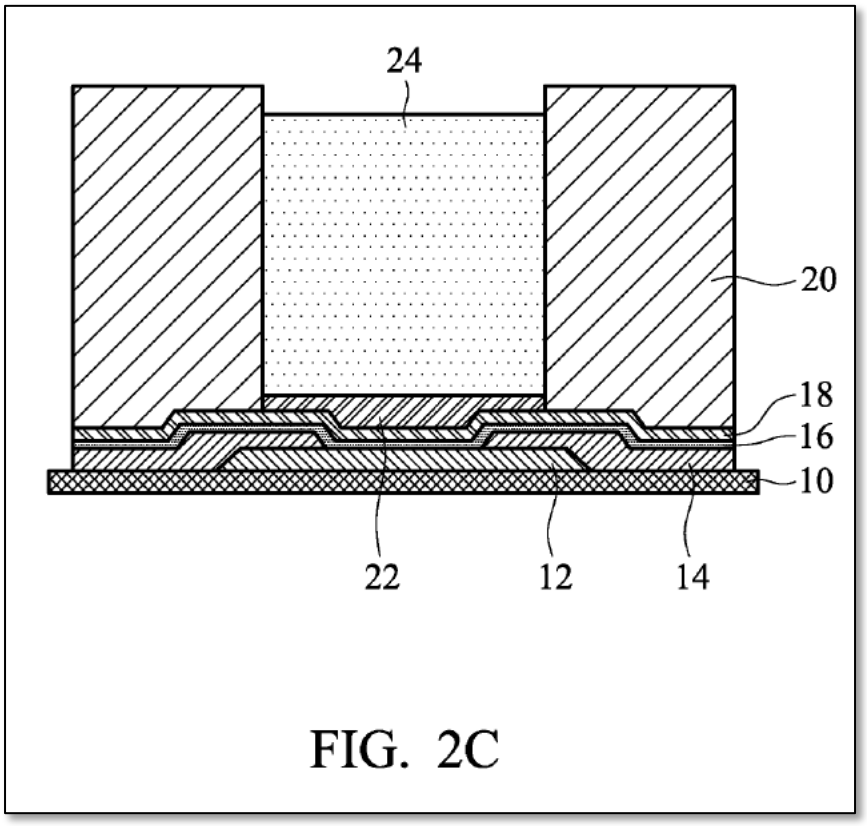


FIG. 2C

*EX1025*at FIG. 2C.

74. The "mask layer 20 is then removed" and, as shown in FIG. 2F, a "thermal reflowing process is performed on the solder material layer 24, forming a hemi-sphere-shaped solder bump 24a." *EX1025* at [0021].

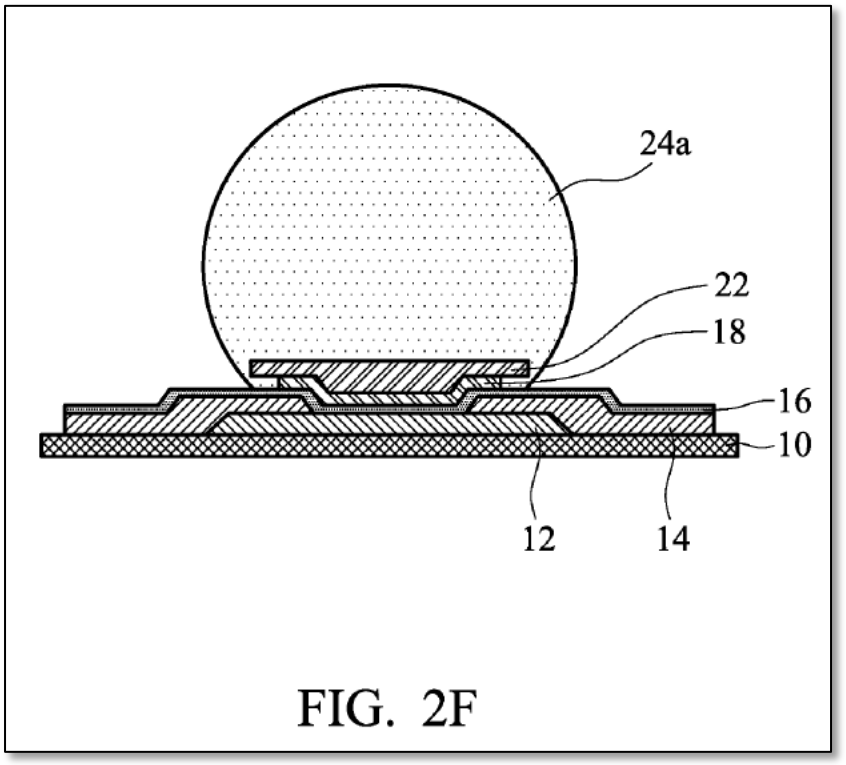


FIG. 2F

EX1025 at FIG. 2F.

75. To control the size of the solder ball, it was known that "the actual amount of solder [] deposited will be a function of the desired end bump size. In other words, in order to form a large solder bump, a greater amount of solder [] material would be applied to the device than would be applied to form a small bump." *EX1093* at 4:7-11.

76. Each of the above examples illustrate the process of forming solder bump/ball and particularly demonstrate that to form a solder bump/ball, a layer or layers of solder material (i.e., solder layers) are deposited, that are then subjected to a reflow treatment, thereby forming the bump/ball geometry. *See also EX1005* at

[0324] ("…the **solder layer** is reflowed to form multiple solid solder bumps or balls 29a[.]") (emphasis added). The formation of solder bumps/balls via solder layers becomes relevant to the mapping of claims 2 and 12, reciting a "solder layer."

G. *Interconnection Schemes and Redistribution Layers*

77. Interconnection schemes, such as those utilizing redistribution layers were well known and widely used prior to the '763 Patent. For example, Lin-604 teaches "[a]n RDL interconnection is formed over a surface of core 744. RDL interconnection may include passive circuitry as well, such as capacitor, resistor and inductor. As an example, insulation layer 747 is deposited over core 744 and patterned to expose metal layer 748. Metal layer 749 is deposited over insulation layer 747 and provides for re-routing electrical connections over a surface of core 744 within semiconductor package 700." *EX1026* at 17:24-31.

78. The metal layers of an interconnection could be formed of copper and that a dielectric layer could be formed of a polymer, such as polyimide, among other suitable materials. Specifically, Savastiouk teaches "[m]etal layers 136 (FIG. 7) and dielectric layers 144 are deposited on the interposer wafer and patterned to provide interconnects and, possibly, other elements as described above. In some embodiments, metal 136 is copper and dielectric 144 is polyimide, but other materials can also be used. Some or all of dielectric layers 144 can be silicon dioxide,

photosensitive benzocyclobutene (BCB), polybenzoxazole (PBO), or other materials." *EX1017* at 6:18-26.

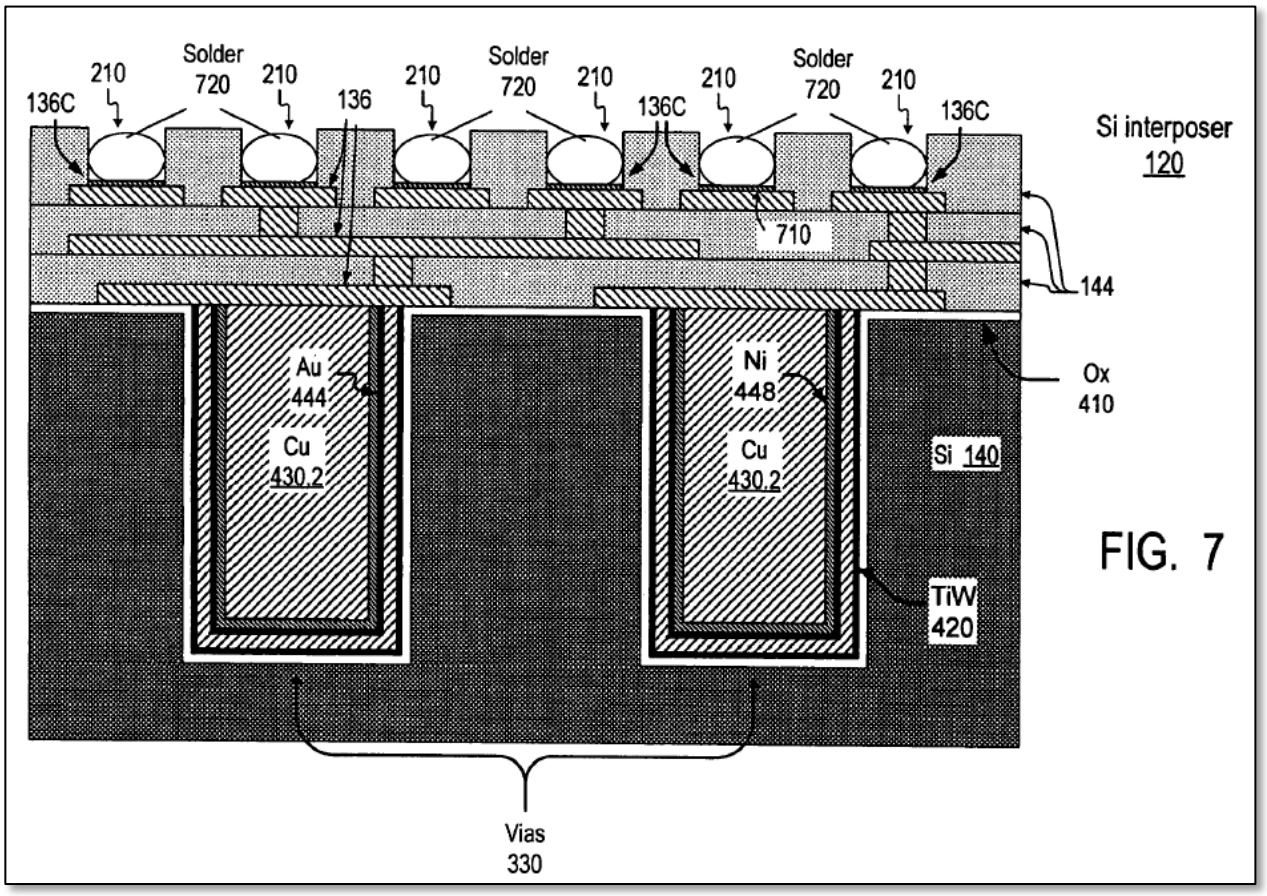
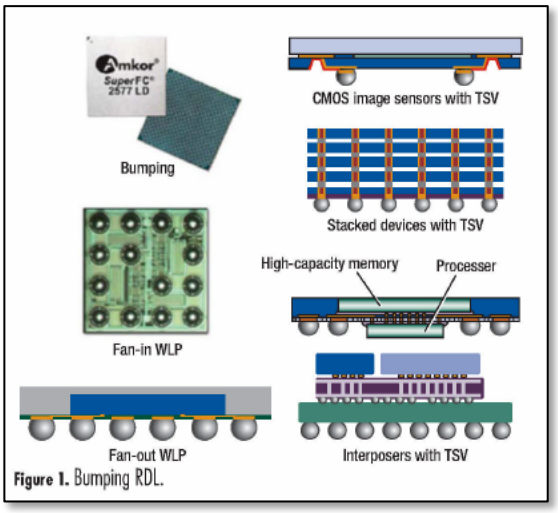


FIG. 7

EX1017 at FIG. 7.

79. Further still, prior to the '763 Patent, it was well known that conductive metals, such as copper, were suitable as metallization for providing electrical conductivity to make electrical connections within a redistribution layer. For example, Garrou teaches "[t]he lack of area array designed chips was a major impediment to the early use of FC. RDL addressed this issue (**Fig. 1**) − defined by

the addition of metal and dielectric layers onto the surface of the wafer to re-route the I/O layout into a new, looser pitch footprint. Such redistribution requires thin film polymers (BCB, PI or newer polymers such as Asahi Glass ALX) and metallization (Al or Cu) to reroute the peripheral pads to an area array configuration." *EX1013* at p. 1.



EX1013 at FIG. 1.

80. At the time of the '763 Patent, a number of manufacturing methods were known and widely used for providing interconnect structures. For example, Halahan teaches "electroplating and electroless plating of conductive materials into openings[.]" where the plated materials are "used to form through hole interconnects in integrated circuits." *EX1027* at [0001]. Specifically, Halahan teaches "Dielectric 120 is deposited in the openings by chemical vapor deposition (CVD) or thermal oxidation. Metal 130 is sputtered on dielectric 120. Metal 140 is electrodeposited

(electroplated) to fill up the openings." *EX1027* at [0002]. Halahan further teaches that "[m]etal 140 increases the mechanical strength of the structure and improves heat dissipation." *EX1027* at [0003]. Notably, Halahan lists advantages of electroplating as "high throughput and low tool cost" with electroless plating having "similar advantages." *EX1027* at [0005].

H. *Semiconductor Chips*

81. Semiconductor chips were widely used well in advance of the '763 Patent. Specifically, semiconductor chips, such as integrated circuits, were known to be coupled using chip packaging techniques such as flip-chip packaging as noted above. For example, Savastiouk teaches attachment of integrated circuits to other substrates in which "Integrated circuit dies ('chips') can be attached to a lead frame and then packaged in a ceramic or plastic carrier. The leads of the lead frame can then be soldered to a printed circuit board (PCB). Alternatively, the chip can be soldered directly to the PCB ('flip chip' packaging). The flip chip packaging reduces the package size and shortens the electrical connections between the die and the PCB." *EX1017* at 1:26-32.

82. It was also known that packaging techniques could be used to couple multiple chips into a single package. For example, Savastiouk teaches coupling IC dies 124.1, 124.2, and 124.3 onto a single interposer 120. Specifically, Savastiouk

teaches "FIGS. 13–14 illustrate a possible manufacturing sequence with multiple die levels 124.1, 124.2, 124.3 attached to the packaging substrate." *EX1017* at 10:22-24. The attachment of dies 124.1, 124.2, and 124.3 is further illustrated in FIG. 13 of Savastiouk shown below with multiple die levels stacked vertically over the interposer 120.

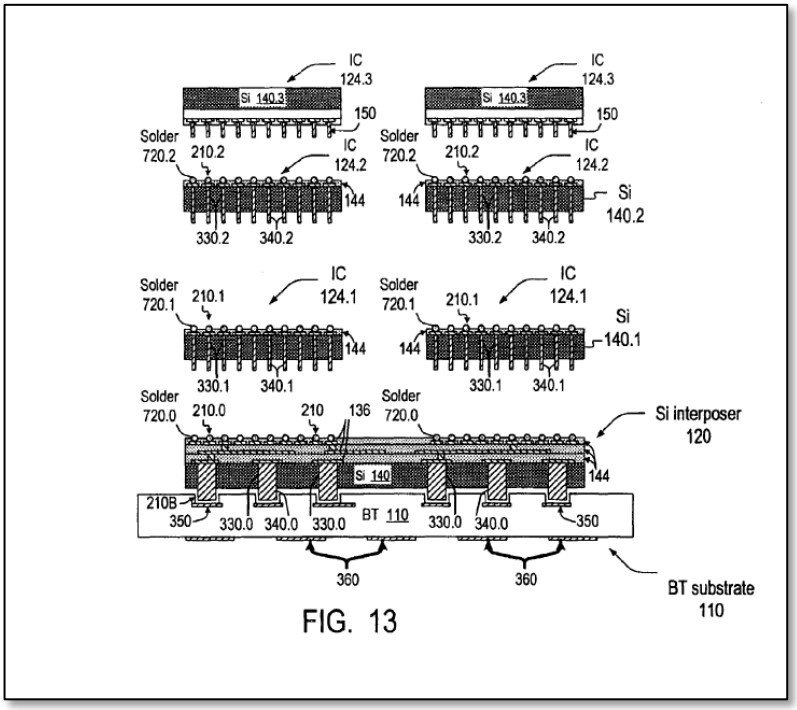


FIG. 13

EX1017 at FIG. 13.

83. Further, Garrou teaches that "[i]ntegrating chips vertically in a single package multiplies the amount of silicon that can be crammed in a given package footprint, conserving hand held device real estate. At the same time, it enables shorter chip to chip routing, which speeds communication between them. Another

benefit is the simplification of board assembly because there are fewer components to be placed on the board." *EX1028* at p. 4. Thus, a variety of benefits of vertically integrating chips was known.

84. In addition to vertically stacking chips, it was well known that integrated circuit chips could be attached on opposing sides of an interposer or circuit board. For example, Kinsman teaches attaching integrated circuits to opposing sides of a dielectric circuit board. "One way to satisfy the demand for increased integrated circuit density is to attach integrated circuits to opposing sides of a dielectric circuit board. A technique developed by the semiconductor industry to couple integrated circuits positioned on opposite sides of a circuit board to each other has been the creation of conductive vias through circuit boards. FIG. 1 is a partial isometric view of a circuit board 1 comprising a substrate 8 with holes 10 extending through its thickness 11 in any desired arrangement according to the prior art. The substrate 8 may comprise a BT or FR dielectric core, and the methods used to make the holes 10 include drilling, etching and laser ablation." *EX1029* at [0003]. Thus, it was known that multiple semiconductor chips, such as integrated circuits, could be coupled to opposing sides of a substrate to increase integrated circuit density.

85. Savastiouk also suggests attaching integrated circuit structures on opposing sides of substrate by stating that PCB 130, which is positioned beneath

interposer 120 on an opposing side of integrated circuit dies 124 can be "replaced with another integrated circuit structure (a die or a wafer)." *EX1017* at 3:22-23; *see also I.D.* at FIGs. 2 and 3.

86. It was well known that semiconductor chips could include processing units such as central processing units and graphics processing units. More specifically, packaged systems included multiple distinct processing units. For example, Lin'152 teaches a system-on chip (SOC) including both a graphics processing unit and a central processing unit. "[A] system-on chip (SOC) including a graphics-processing-unit (GPU) circuit block, a wireless local area network (WLAN) circuit block and a central-processing-unit (CPU) circuit block designed by x86 architecture or by non x86 architectures, but not including any baseband circuit block," *EX1030* at [1000].

87. Integration of central processing units and graphics processing units on a single chip, as well as the benefits associated with such integration, were well known in advance of the '763 Patent. For example, it was known as early as 2011 that the "integration trend of CMOS devices has led to fused architectures, in which the central processing units (CPUs) and graphics processing units (GPUs) are integrated onto the same chip." *EX1031* at p. 1. "Recent examples include Intel's sandy bridge [21], on which CPUs and GPUs are on one chip with a shared on-chip

L3 cache, and AMD accelerated processing unit (APU) [26] on which both on-chip CPUs and GPUs share the same off-chip memory [19].” *EX1031* at p. 1. Such combined GPU/GPU architectures were known to provide benefits such as the “opportunity to leverage both the high computational power from GPUs for regular applications and flexible execution from CPUs for irregular workloads” as well as bypassing “costly CPU-GPU data transfers[.]” *EX1031* at p. 1-2.

88. It was known that semiconductor chips may also comprise various insulating (dielectric) materials with interconnection structures therein that were used to connect such chips to each other and to chip packages. For example, Savastiouk teaches that “[e]ach die 124.1 has one or more metalized through vias 330.1 formed in the die’s semiconductor substrate 140.1 (e.g. monocrystalline silicon). Each via 330.1 passes between the top and bottom surfaces of substrate 140.1. Conductive paths are provided from contact pads at the top of each die 124.1 to contact pads 340.1 at the bottom of the die through the vias 330.1. Contact pads 340.1 protrude out of the respective vias 330.1. The dies 124.1 can be manufactured using the same techniques as described above for interposer 120 (involving the wafer thinning to expose the contact pads 340.1). Each die may have the same general structure as interposer 120 in FIGS. 10–12. Of course, the circuitry in dies 124.1 does not have to be identical to the interposer circuitry, and different dies 124.1 may

differ from each other. Also, contact pads 340.1 may have smaller dimensions, and may be placed closer to each other, as they do not have to meet the BT substrate dimension requirements. Pads 340.1 can be copper/nickel/gold structures as in FIG. 12, or they can be made from other materials. The metal in vias 330.1 is insulated from substrate 140.1 by a dielectric 410 (FIG. 12)." *EX1017* at 10:30-50. Additionally, Savastiouk teaches that "[d]ies 124.2 may be similar to dies 124.1. Dies 124.2 include metalized vias 330.2 in semiconductor substrates 140.2, and contact pads 340.2 protruding out of the vias on the bottom." *EX1017* at 10:62-65.

VI. SUMMARY OF THE PRIOR ART REFERENCES

A. *Sundaram*

89. Sundaram describes "various 3D packaging schemes" such as "a system-in-package (SIP) structure[,]" a "package-on-package (POP) structure[,]" a "face-to-face (F2F) structure[,]" and a "logic bottom stack [] structure." *EX1004* at 1:33-42 Sundaram further describes that "multi-die stacking with TSVs imposes great challenges in forming TSVs within complementary metal oxide semiconductor (CMOS) chips, power delivery, testability, reliability, and thermal management of the logic chip, all of which remain major barriers in achieving high bandwidth for 3D ICs." *EX1004* at 2:1-6. Sundaram teaches various "interposer interconnect structure[s]" and explains "embodiments of the present invention provide a testable

interposer interconnect structure[.]" *EX1004* at 2:24-67. The term "interposer interconnect structure" may "refer to connecting devices to form a package[.]" *EX1004* at 5:16-19

90. As shown below in FIG. 3, Sundaram teaches an "interconnect structure 100" having an "interposer 105" with a "first side 115 and a second side 120." *EX1004* at 5:46-48. Interposer 105 "can be made of many substrate materials, for example, glass, silicon, ceramic, polymer-glass laminates, and flexible polymers." *EX1004* at 5:54-56. There are a "plurality of small through vias 110…within the interposer 105" that "extends from the first side 115 to the second side 120." *EX1004* at 6:6-9. Sundaram's "through vias 110 can be metalized in such a way that the metallization provides die pad surfaces 135 that correspond to each of the vias 110" where the metallization material is "a highly-conductive metal, for example copper." *EX1005* at 6:22-27.

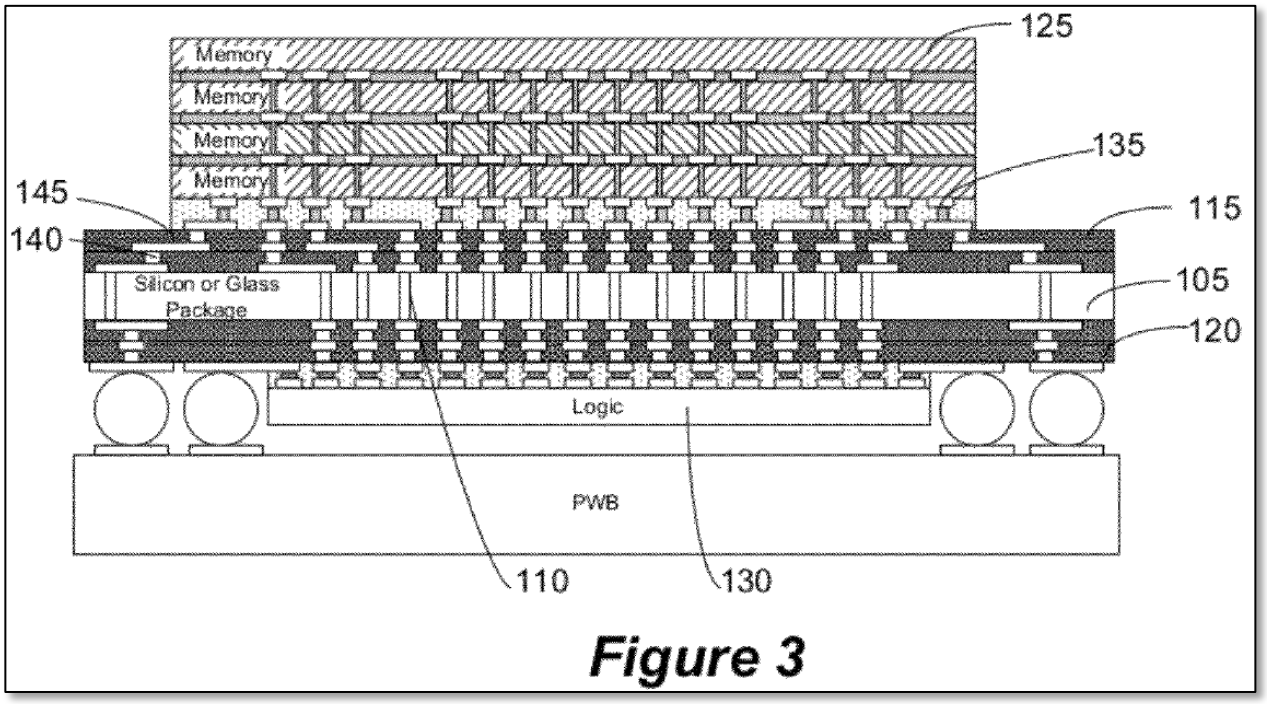


Figure 3

EX1004 at FIG. 3.

91. As shown above, a "first electronic device 125 can be attached to the first side 115 of the interposer 105 and a second electronic device 130 can be attached to the second side 120 of the interposer 105." *EX1004* at 6:34-36. first electronic device 125 "can be single or stacked memory IC devices, and the second electronic device 130 can be a logic IC device or devices." *EX1004* at 6:37-39. Though "other electronic devices can also be used as the first electronic device 125 and/or the second electronic device 130." *EX1004* at 6:39-42. Interposer 105 and through vias 110 "work to electrically connect the first electronic device 125 and second electronic device 130." *EX1004* at 6:46-50. Additionally, as shown above,

Sundaram's interconnect structure 100 comprises "blind vias 140 and conductor traces 145 defined within polymer-metal redistribution layers deposited on the first side 115 and second side 120 of interposer 105." *EX1004* at 6:62-67. Sundaram's teachings allow for the "interposer 105 and the package [sic] can be one and the same." *EX1004* at 7:61-67.

92. I have been informed that for a prior art reference to be proper for use in an obviousness analysis, the reference must be "analogous art" to the claimed invention. I have been informed that a prior art reference is analogous to the claimed invention if the reference is from the same field of endeavor as the claimed invention or if it is reasonably pertinent to the particular problem that the inventor was trying to solve.

93. As discussed above, the field of endeavor of the claimed invention of the '763 Patent includes semiconductor packaging. *See* ¶¶ 31-33. As demonstrated above, Sundaram is directed to "interposer interconnect structure[s]" which may "refer to connecting devices to form a package[.]". *EX1004* at 5:16-19. Thus, Sundaram is directed to semiconductor chip packaging and accordingly is in the same field of endeavor as the claimed invention of the '763 Patent.

94. Sundaram is also reasonably pertinent to the problems solved by the inventors of the '763 Patent. As discussed above, the '763 Patent is directed to

minimizing temperature coefficient of expansion mismatching. *See* ¶¶ 34-38. Sundaram teaches that "[g]lass presents several advantages, namely, silicon-matched coefficient of thermal expansions (CTE)[.]" *EX1004* at 5:62-63. Thus, a POSITA would have consulted Sundaram and applied its teachings when faced with the problem of minimizing temperature coefficient of expansion mismatching. Additionally, the '763 Patent is directed to creating chip packages with pre-testability capability. *See* ¶¶ 34-38. Sundaram is concerned with the "testability" of 3D ICs and provides a "testable interposer interconnect structure." *EX1004* at 7:41-43, 2:34-35. Thus, a POSITA would have consulted Sundaram and applied its teachings when faced with the problem of creating chip packages with pre-testability capability. Finally, the '763 Patent is concerned with the impact of miniaturization on circuit performance. *See* ¶¶ 34-38. Sundaram is likewise concerned with "ultra-fine pitch and ultra-short interconnections" in chip packages and associated "challenges[.]" *EX1004* at 1:65–2:20, *see also* 1:15-32, 2:21–3:6. Thus, a POSITA would have consulted Sundaram and applied its teachings when faced with the problem of the impact of miniaturization on circuit performance.

B. *Lin-191*

95. Lin-191 teaches system-in-package or multichip module architectures that incorporate multi-layer chips within a multi-layer polymer structure, supported

by on-chip and intra-chip metal bumps together with patterned metal layers. These modules provide electrical connection between multiple semiconductor chips and external circuits via "on-chip metal bumps, the intra-chip metal bumps and the patterned metal layers." *EX1005* at Abstract. For example, chips are disclosed as being connected through multiple metal interconnects, including "patterned metal layers 2, 3, 4 and 5 and the metal pillars or bumps[.]" *EX1005* at [0462].

96. Lin-191 teaches specific thickness ranges for substrates and polymeric dielectric layers that are used in packaging semiconductor chips. For example, the substrate 110 may have a "thickness T1 between about 10 and about 1,000 micrometers, between 10 and 100 micrometers or between 100 and 500 micrometers." *EX1005* at [0051]. Dielectric or insulating layer 10 can be formed of "silicon dioxide (SiO_2), silicon nitride, silicon oxynitride, silicon carbon nitride, polyimide, epoxy, benzocyclobutane (BCB), polybenzoxazole (PBO), poly-phenylene oxide (PPO), silosane or SU-8 having a suitable thickness, e.g., between 0.3 and 30 micrometers, and preferably between 1 and 10 micrometers." *EX1005* at [0052]. Additional dielectric layers such as insulating layer 15 are disclosed with thicknesses "between 1 and 20 micrometers, and preferably between 3 and 15 micrometers or between 5 and 10 micrometers[.]" *EX1005* at [0291]. Encapsulation is provided by polymer molding layers such as encapsulating layer 85, which has a

thickness "between about 20 and about 500 micrometers, and preferably between 30 and 100 micrometers." *EX1005* at [0109]. Build-up polymer layers including polymer layer 78 are specified at thicknesses "between 5 and 50 micrometers, and preferably between 5 and 15 micrometers or between 5 and 10 micrometers[.]" *EX1005* at [0368]. A "passivation layer 501 over the semiconductor substrate 601" may be formed. *EX1005* at [0552].

97. Lin-191 also describes interconnects and bump structures that connect the layers described above. For example, bumps 24 are described as having a "height greater than 5 micrometers, such as between 5 and 50 micrometers, and preferably between 10 and 20 micrometers," while bumps 14 are larger, with a "height greater than 15 micrometers, such as between 15 and 520 micrometers, and preferably between 20 and 110 micrometers[.]" *EX1005* at [0066], [0099]. At the package level, solder balls for external board connection are described. *EX1005* at [0007], [0048], [0490].

98. Lin-191 incorporates passive devices directly into the package. In one embodiment, a chip "can be replaced by a passive component 67, such as capacitor, inductor or resistor." *EX1005* at [0340]. In another embodiment, discrete passive components 910 are mounted between upper-tier chips, coupled through "multiple solder joints 915[,]" "patterned metal layer 7,", and "bumps 64[.]" *EX1005* at

[0364]-[0368]. A polymer layer such as polymer layer 78 can be formed "on the discrete passive components 910." *EX1005* at [0368].

99. Lin-191 further discloses multiple semiconductor chips integrated into a single package. These chips "can be a central-processing-unit (CPU) chip designed by x86 architecture, a central-processing-unit (CPU) chip designed by non x86 architectures, such as ARM, Strong ARM or MIPs, a baseband chip, a graphics-processing-unit (GPU) chip, a digital-signal-processing (DSP) chip, a wireless local area network (WLAN) chip, a memory chip, such as flash memory chip, dynamic-random-access-memory (DRAM) chip or statistic-random-access-memory (SRAM) chip, a logic chip, an analog chip, a power device, a regulator, a power management device, a global-positioning-system (GPS) chip, a Bluetooth chip…" *EX1005* at [0240], [0382]. Electrical connections between chips are made through "metal layer 63 of the patterned metal layer 6 and on tops of the metal pillars or bumps 54 and 64[.]" *EX1005* at [0241].

100. Lin-191 discusses the use of the multichip modules for pre-testability capability. Lin-191 explains that wafer level packaging allows for the integration of pre-testability "before being singulated by dicing for final assembly into a chip carrier package[.]" *EX1005* at [0006]. Lin-191 describes that the "testing circuit is either (i) the wafer level testing performed before the chip 700 or 800 is sawed or

diced apart from a wafer, or (ii) the package level testing (the final testing) after the chips 700 and 800 are connected to each other" *EX1005* at [0492]. Each chip is equipped with dedicated test structures, as "the chip 700 may include … two testing interface circuits 333a and 333b" while "the chip 800 may include … two testing interface circuits 333c and 333d" *EX1005* at [0462]. These test interfaces may be implemented as scan test circuits where each "of the test interface circuits 333a, 333b, 333c and 333d … can be a scan test circuit … used for scan testing … at wafer level … or at the package level testing (the final testing)[.]" *EX1005* at [0493].

101. I have been informed that for a prior art reference to be proper for use in an obviousness analysis, the reference must be "analogous art" to the claimed invention. I have been informed that a prior art reference is analogous to the claimed invention if the reference is from the same field of endeavor as the claimed invention or if it is reasonably pertinent to the particular problem that the inventor was trying to solve.

102. As discussed above, the field of endeavor of the claimed invention of the '763 Patent includes semiconductor packaging. *See* ¶¶ 31-33. As demonstrated above, Lin-191 is directed to "system-in packages, or multichip modules… includ[ing] multi-layer chips in a multi-layer polymer structure, on-chip metal bumps on the multi-layer chips, intra-chip metal bumps, in the multi-layer polymer

structure, and patterned metal layers in the multi-layer polymer structure." *EX1005* at [0007], [0003]. Thus, Lin-191 is directed to semiconductor packaging and accordingly is in the same field of endeavor as the claimed invention of the '763 Patent.

103. Lin-191 is also reasonably pertinent to the problems solved by the inventors of the '763 Patent. As discussed above, the '763 Patent is directed to solving the problem of providing chip packages with pre-testability capability. *See* ¶¶ 34-38. As demonstrated above, Lin-191 discloses that "the chip 160 may have built-in self test (BIST) circuits for reducing the testing time for the system-in package or multichip module." *EX1005* at [0401]. Further, Lin-191 describes test structures such as "testing interface circuits 333a–333d" that can be used for wafer-level or package-level scan testing before or after the chips are diced and packaged. *EX1005* at [0462], [0492]-[0493]. Thus, a POSITA would have consulted Lin-191 and applied its teachings when faced with the problem creating chip packages with pre-testability capability. *See also EX1005* at [0006], [0105], [0173], [0239], [0401] (all concerned with testing in a chip package).

C. *Lin-863*

104. Lin-863 is directed to "a semiconductor device and method of forming an interconnect substrate for a Fo-WLCSP" (fan-out wafter level chip scale

package). *EX1007* at 1:7-10, 2:14-15. Lin-863 teaches that "a need exists to reduce CTE mismatch between the encapsulant and substrate in a Fo-WLCSP" because "CTE mismatch…causes stress during thermal cycling, leading to defects and higher manufacturing costs." *EX1007* at 2:29-30, 2:23-25.

105. Accordingly, Lin-863 teaches "an interconnect substrate with conductive TMV for a Fo-WLCSP" *EX1007* at 3:31-32. As shown below, Lin-863's interconnect substrate includes a "TMV interconnect substrate 220 with conductive layer 222" that is "formed over encapsulant 226 and conductive TMV 225 formed through the encapsulant[.]" *EX1007* at 12:34-38. There are a "plurality of openings 228 [] formed in encapsulant for disposing of semiconductor die 124" which is then covered with "an encapsulant or molding compound 236[.]" *EX1007* at 12:40-42, 12:61-62. An "electrically conductive layer or RDL 242 is formed over insulating layer 240 and conductive layer 222" made of "Al, Cu, Sn, Ni, Au, Ag, or other suitable electrically conductive material." *EX1007* at 13:21-26. Additionally, an "electrically conductive bump material" is formed that "can be Al, Sn, Ni, Au, Ag, Pb, Bi, Cu, solder, and combinations thereof[.]" *EX1007* at 14:17-22. FIG. 9a below shows a "cross-sectional view of Fo-WLCSP 262 after singulation" and FIG. 9b shows a "plan view[.]" *EX1007* at 14:45-46, 14:51.

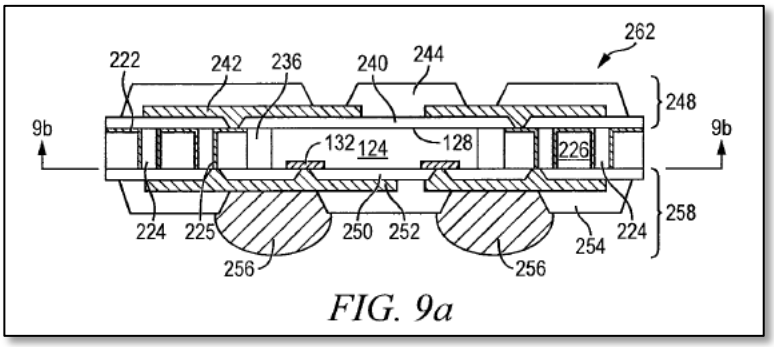


FIG. 9a

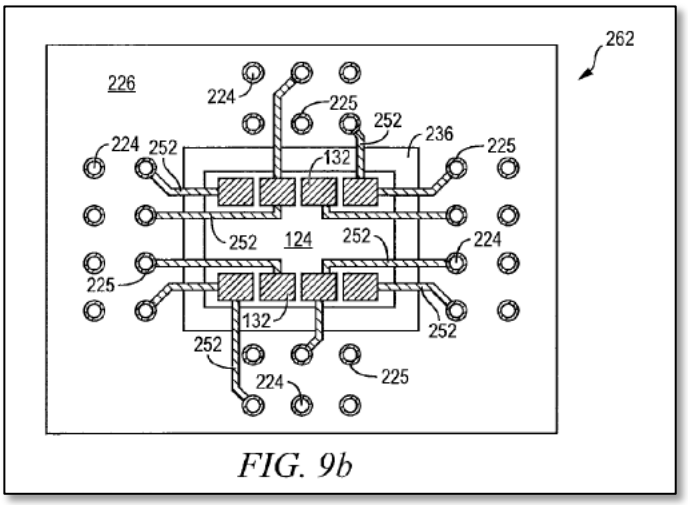


FIG. 9b

EX1007 at FIGS. 9a-b.

106. I have been informed that for a prior art reference to be proper for use in an obviousness analysis, the reference must be "analogous art" to the claimed invention. I have been informed that a prior art reference is analogous to the claimed invention if the reference is from the same field of endeavor as the claimed invention or if it is reasonably pertinent to the particular problem that the inventor was trying to solve.

107. As discussed above, the field of endeavor of the claimed invention of the '763 Patent includes semiconductor packaging. *See* ¶¶ 31-33. As demonstrated above, Lin-863 is directed to an "interconnect substrate for a Fo-WLCSP." *EX1007* at 1:7-10, 1:14–2:25. Thus, Lin-863 is directed to semiconductor chip packaging and accordingly is in the same field of endeavor as the claimed invention of the '763 Patent.

108. Lin-863 is also reasonably pertinent to the problems solved by the inventors of the '763 Patent. As discussed above, the '763 Patent is directed to solving the problem of minimizing temperature coefficient of expansion mismatching. *See* ¶¶ 34-38. As demonstrated above, Lin-863 is concerned with the "CTE mismatch between the encapsulant and substrate in a Fo-WLCSP." *EX1007* at 2:29-30, 11:20-46, 12:11-32, 14:43-65. Thus, a POSITA would have consulted Lin-863 and applied its teachings when faced with the problem of minimizing temperature coefficient of expansion mismatching.

D. *Lin-691*

109. Lin-691 teaches that "among the efforts for reducing the size of integrated circuits and reducing RC delay, three-dimensional integrated circuits (3DIC) and stacked dies are commonly used." *EX1008* at [0002]. Thus, "[t]hrough-substrate vias (TSVs)" are commonly "used in 3DIC and stacked dies." *EX1008* at

[0002]. Lin-691 acknowledges that "there are two commonly used approaches for forming TSVs, via-first approach and via-last approach." *EX1008* at [0003]. However, both approaches suffer from problems such as "copper popping and metal-1 to metal-2 bridging" in the via-first, and "less efficient power connection[,]" resulting in high "resistances of the power paths[,]" for via-last. *EX1008* at [0003]-[0004]. To address these issues, Lin-691 teaches forming a TSV having a "diffusion barrier layer 54…[that] is blanket formed, covering the sidewalls and bottom of TSV opening 44." *EX1008* at [0019]. "Next, a thin seed layer (not shown) may be blanket formed on diffusion barrier layer 54." *EX1008* at [0019]. The seed layer may include "metals such as silver, gold, aluminum, and combinations thereof may also be included." *EX1008* at [0019].

110. "In FIG. 7, a metallic material is filled into openings 44…forming TSV 60[,]" shown below. *EX1008* at [0021]. The "filling material includes copper or copper alloys, although other metals, such as aluminum, silver, gold, and combinations thereof may be used." *EX1008* at [0021].

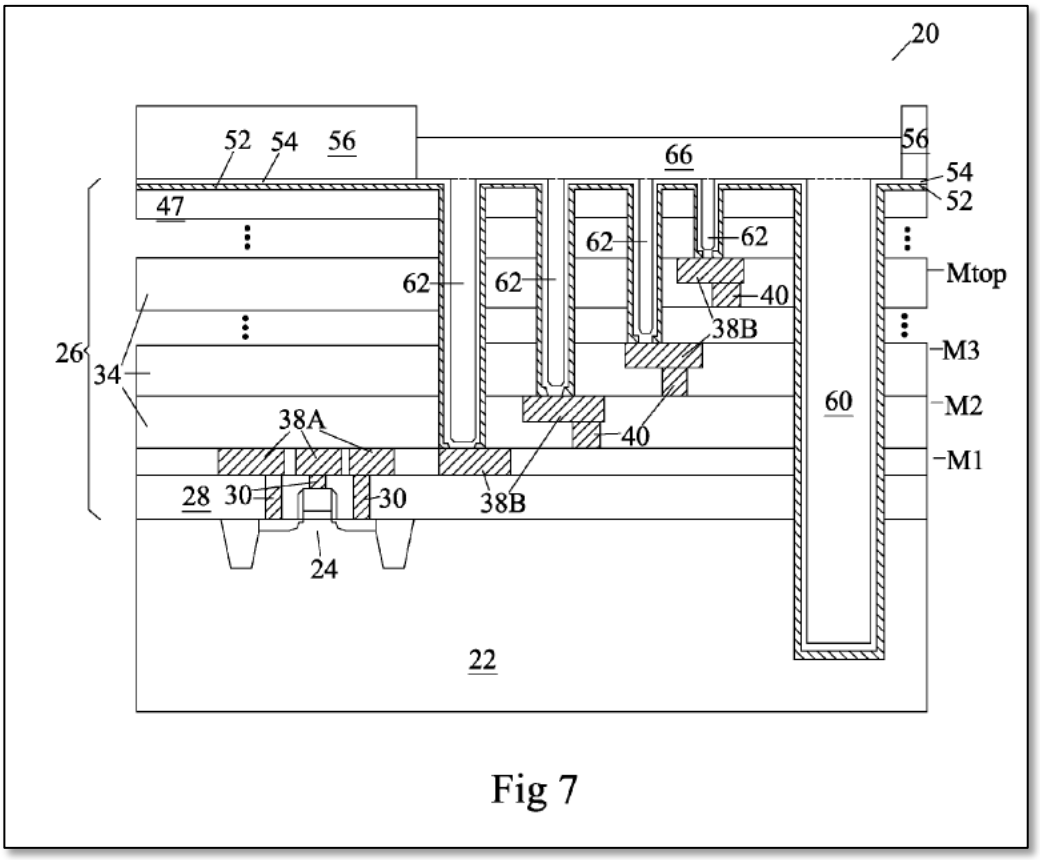


Fig 7

EX1008 at FIG. 7.

111. I have been informed that for a prior art reference to be proper for use in an obviousness analysis, the reference must be "analogous art" to the claimed invention. I have been informed that a prior art reference is analogous to the claimed invention if the reference is from the same field of endeavor as the claimed invention or if it is reasonably pertinent to the particular problem that the inventor was trying to solve.

112. As discussed above, the field of endeavor of the claimed invention of the '763 Patent includes semiconductor packaging. *See* ¶¶ 31-33. As demonstrated

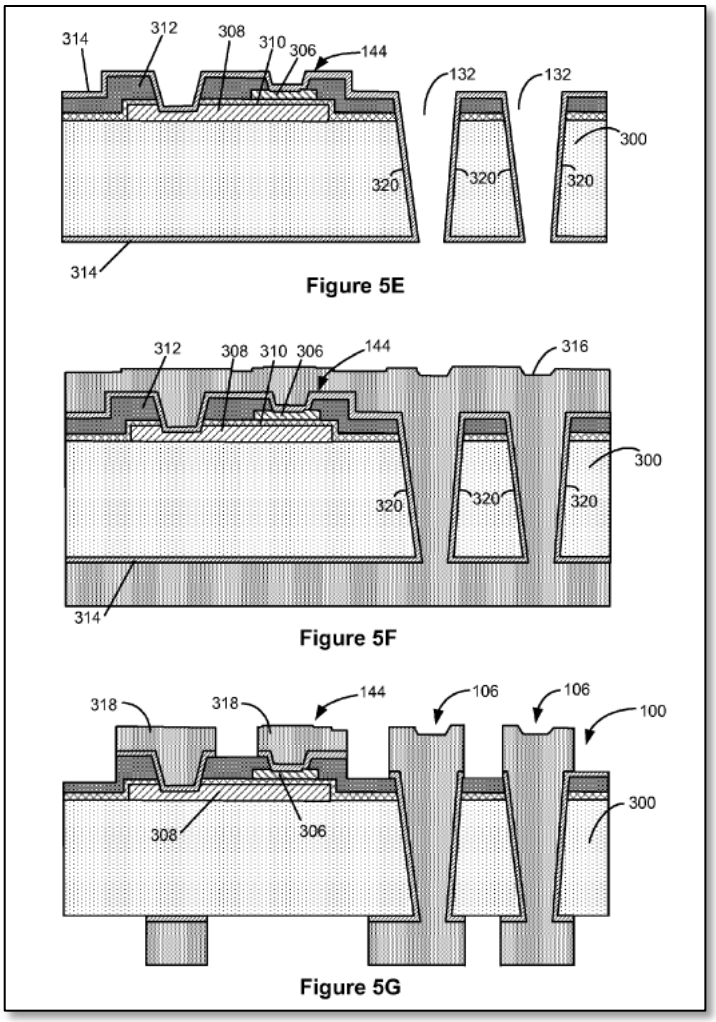
above, Lin-691 is directed to "three-dimensional integrated circuit (3DIC) and stacked dies." *EX1008* at [0002]. Thus, Lin-691 is directed to semiconductor chip packaging and accordingly is in the same field of endeavor as the claimed invention of the '763 Patent.

113. Lin-691 is also reasonably pertinent to the problems solved by the inventors of the '763 Patent. As discussed above, the '763 Patent is directed to solving the problem of the impact of miniaturization on circuit performance. *See* ¶¶ 34-38. As demonstrated above, Lin-691 is concerned with the "efforts for reducing the size of integrated circuits" including problems such as "copper popping and metal-1 to metal-2 bridging" and high "resistances of the power paths." *EX1008* at [0002]-[0004]. Thus, a POSITA would have consulted Lin-691 and applied its teachings when faced with the problem of the impact of miniaturization on circuit performance.

E. *Shenoy*

114. Shenoy is directed to "packaging of devices and more particularly to glass via bars for interconnecting multiple layers, substrates or components of a package." *EX1011* at [0001]. Shenoy teaches a "glass substrate after through-glass via hole sidewall and surface metallization." *EX1011* at [0055]. A "seed layer may be deposited by a process such as PVD, CVD, ALD, or an electroless plating

process" where the seed layer includes "Ag[.]" *EX1011* at [0054]. The seed layer 314 is depicted below. The "through-glass via holes are filled by electroplating" and "can include Cu[.]" *EX1011* at [0054]. The plated metal 316, shown below, "fills the through-glass via holes 132" and "covers the conformal seed layer 314." *EX1011* at [0055]. The plated metal 316 "can be patterned in a subsequent operation, as shown in FIG. 5G." *EX1011* at [0055].



EX1011 at FIGS. 5E-G.

115. Shenoy further teaches that in "some implementations, the glass substrate can have a coefficient of thermal expansion (CTE) matched to the CTE of another component of a package, or between the CTEs of two or more components of a package. For example, a glass substrate can have a relatively low CTE of about 3.4 ppm/ °C. matched to silicon, a relatively high CTE of about 10 ppm/ °C. matched close to a printed circuit board or mold compound, or a CTE between those components." *EX1011* at [0042].

116. I have been informed that for a prior art reference to be proper for use in an obviousness analysis, the reference must be "analogous art" to the claimed invention. I have been informed that a prior art reference is analogous to the claimed invention if the reference is from the same field of endeavor as the claimed invention or if it is reasonably pertinent to the particular problem that the inventor was trying to solve.

117. As discussed above, the field of endeavor of the claimed invention of the '763 Patent includes semiconductor packaging. *See* ¶¶ 31-33. As demonstrated above, Shenoy is directed to "packaging of devices and more particularly to glass via bars for interconnecting multiple layers, substrates or components of a package" and also teaches embodiments that can be sued in "stacked three-dimensional (3-D) packages." *EX1011* at [0001], [0029]-[0030]. Thus, Shenoy is directed to

semiconductor chip packaging and accordingly is in the same field of endeavor as the claimed invention of the '763 Patent.

118. Shenoy is also reasonably pertinent to the problems solved by the inventors of the '763 Patent. As discussed above, the '763 Patent is directed to solving the problem of minimizing temperature coefficient of expansion mismatching. *See* ¶¶ 34-38. As demonstrated above, Shenoy teaches that "the glass substrate can have a coefficient of thermal expansion (CTE) matched to the CTE of another component of a package[.]" *EX1011* at [0042]. Thus, a POSITA would have consulted Shenoy and applied its teachings when faced with the problem of minimizing temperature coefficient of expansion mismatching.

F. *Yu*

119. Yu describes that a "Package-on-Package (PoP) is an integrated circuit packaging technique to allow vertically combining discrete logic and memory ball grid array (BGA) packages." *EX1010* at 1:49-55. Accordingly, Yu teaches a PoP structure comprising a package 202. *EX1010* at 2:9-10, 2:15-16, 8:26-39. Yu's package 202 comprises a "core material, such as molding compound 18" made of an "epoxy, polyimide, silicone rubber…or a combination thereof" that is cured over a "first die 10[.]" *EX1010* at 2:61-67. Yu's package further comprises a "front side interlayer dielectric (ILD) and redistribution layer (RDL) structure" made of a "first

front side metallization layer 20" and a "first ILD layer 22" made of polyimide. *EX1010* at 3:4-22. Additional metallization layers and ILD layers, "such as a second metallization layer 24 and a second ILD layer 26" are formed as part of the front side RDL. *EX1010* at 3:28-32.

120. TMV (through mold via) openings 36 are "formed through the molding compound 18 to the first front side metallization layer 20" then a copper "seed layer is deposited…into the TMV openings 36." *EX1010* at 3:56-65. "A conductive material, such as copper" is then deposited on the back side by "electroplating" thereby forming "TMVs 38[.]" *EX1010* at 3:67–4:6. Yu's package 202 additionally includes a "back side ILD and RDL structure" formed of a "first back side ILD layer 40, a second back side metallization layer 42, a second ILD layer 44, and openings 46 and 48 through the second ILD layer 44 to the second back side metallization layer 42." *EX1010* at 4:7-11. As shown in the figure below, a "second die 52, such as a memory die…is attached through the opening 46 to conductive features in the second back side metallization layer 42, such as by conductive connectors 54, like controlled collapse chip connection (C4) bumps." *EX1010* at 4:30-34. "[C]onductive connectors 58, such as ball grid array (BGA) balls" are formed on package 202 which may be a "lead-free solder." *EX1010* at 4:45-50. Finally, a "third die 62, such

as a memory die [is]…attached through the opening 30 to conductive features in the second front side metallization layer 24" also by C4 bumps. *EX1010* at 4:53-60.

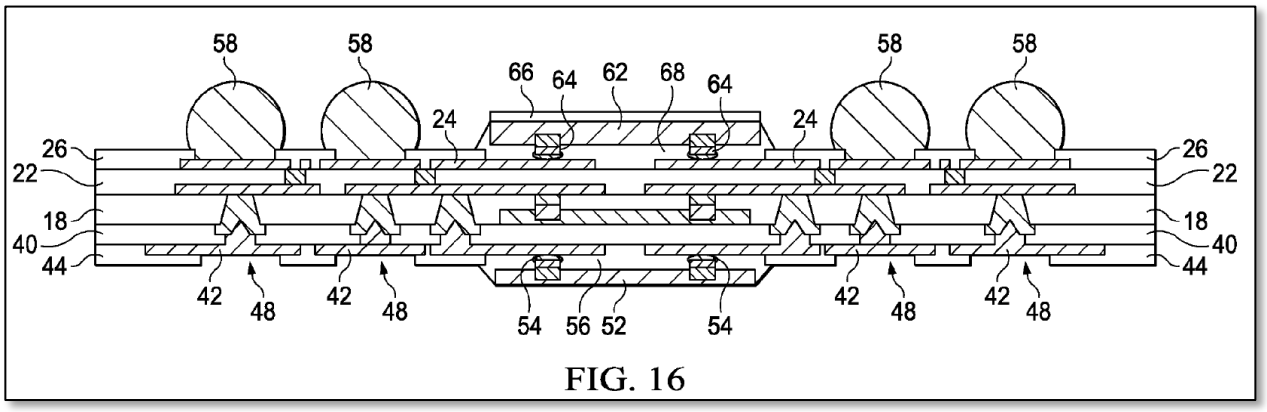


FIG. 16

EX1010 at FIG. 16.

121. The package of FIG. 16 may be stacked alongside additional packages forming the PoP structure:

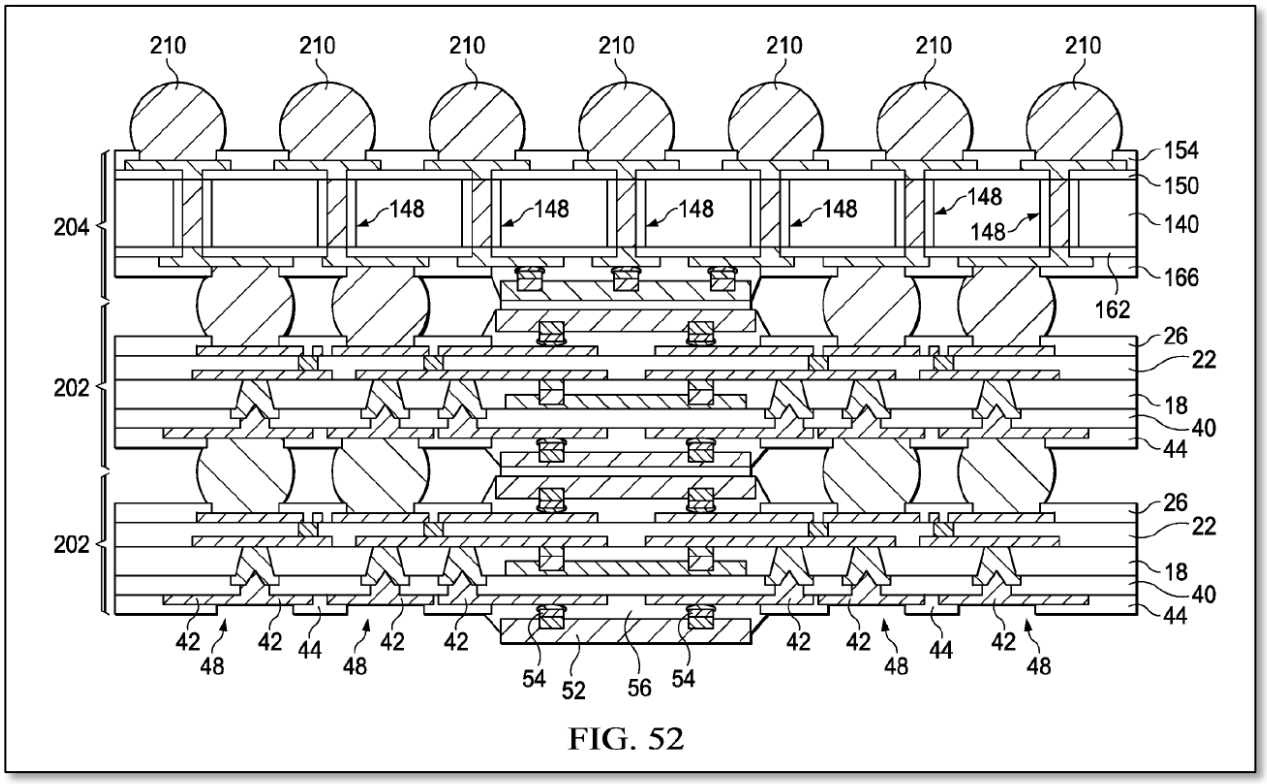


FIG. 52

EX1010 at FIG. 52.

122. In one embodiment, Yu teaches forming an "interposer and a die attached to the interposer" and teaches, with reference to a "substrate 140" used in forming the interposer that "it is believed that using silicon substrates for the interposer may reduce stress because the coefficient of thermal expansion (CTE) mismatch between the silicon substrates and the silicon typically used for the dies is lower than with substrates formed of different materials." *EX1010* at 6:14-26.

123. I have been informed that for a prior art reference to be proper for use in an obviousness analysis, the reference must be "analogous art" to the claimed invention. I have been informed that a prior art reference is analogous to the claimed

invention if the reference is from the same field of endeavor as the claimed invention or if it is reasonably pertinent to the particular problem that the inventor was trying to solve.

124. As discussed above, the field of endeavor of the claimed invention of the '763 Patent includes semiconductor packaging. *See* ¶¶ 31-33. As demonstrated above, Yu is directed to "Package-on-Package (PoP)" structures including "integrated circuit packaging[.]" *EX1010* at 1:49-55, *see also* 1:10-48, 1:63-67, 4:17-20. Thus, Yu is directed to semiconductor chip packaging and accordingly is in the same field of endeavor as the claimed invention of the '763 Patent.

125. Yu is also reasonably pertinent to the problems solved by the inventors of the '763 Patent. As discussed above, the '763 Patent is directed to solving the problem of minimizing temperature coefficient of expansion mismatching. *See* ¶¶ 34-38. As demonstrated above, Yu teaches that "it is believed that using silicon substrates for the interposer may reduce stress because the coefficient of thermal expansion (CTE) mismatch between the silicon substrates and the silicon typically used for the dies is lower than with substrates formed of different materials." *EX1010* at 6:20-26. Thus, a POSITA would have consulted Yu and applied its teachings when faced with the problem of minimizing temperature coefficient of expansion mismatching. Additionally, the '763 Patent is directed to solving the problem

creating chip package with pre-testability capability. *See* ¶¶ 34-38. Yu teaches "a step to test the PoP structure[.]" *EX1010* at 2:17-20. Thus, a POSITA would have consulted Yu and applied its teachings when faced with the problem of creating chip package with pre-testability capability.

VII. SUMMARY OF UNPATENTABILITY

126. I have reproduced the Proposed Grounds of Unpatentability from the Petition for ease of reference:

Grounds	Claims Challenged	35 U.S.C. §	References
1A	1-12, 14, 16-21, 23	103	Sundaram (EX1004) and Lin-191 (EX1005)
1B	13, 15	103	Sundaram, Lin-191, and Lin-863 (EX1007)
1C	22	103	Sundaram, Lin-191, and Lin-691 (EX1008)
1D	22	103	Sundaram, Lin-191, and Shenoy (EX1011)
2A	1-5, 7-12, 14-15, 17	103	Yu (EX1010) and Lin-191
2B	6, 16, 18-21, 23	103	Yu, Lin-191, and Sundaram
2C	13	103	Yu, Lin-191, and Lin-863

VIII. OPINIONS REGARDING GROUND 1A: CLAIMS 1-12, 14, 16-21, AND 23 ARE OBVIOUS OVER SUNDARAM AND LIN-191

A. *Claim 1*

1. 1(Pre): "A chip package comprising"

127. Sundaram teaches various "interconnect structure[s]" to "form a package[.]" *EX1004* at 5:16-19. As shown in FIG. 3 below, As shown in FIG. 3 below, Sundaram's interconnect structure comprises an "interposer 105" that "electrically connect[s] the first electronic device 125 and the second electronic device 130[,]" enabling the "interposer 105 and the package can [*sic*] be one and the same." *EX1004* at 5:45-48, 6:46-48, 7:61-63. The first electronic device 125 "can be single or stacked memory IC devices, and the second electronic device 125 can be a logic IC device or devices." *EX1004* at 6:37-39. ICs (integrated circuit) were known to be formed on semiconductor chips such that Sundaram's interconnect structure and electronic devices 125, 130 collectively form a *chip package*[1]. *See, e.g., EX1133*

[1] Claim language provided in italics. All drawing annotations added. Citations to a claim limitation and/or section number are to the limitations mapping in this Declaration and are incorporated by reference, including the motivations to combine and showing of reasonable expectation of success provided in the cross-referenced

at 1:14-17 ("…has led to increasingly more complex **integrated circuits being produced** in an increasingly smaller space **on semiconductor chips**.").

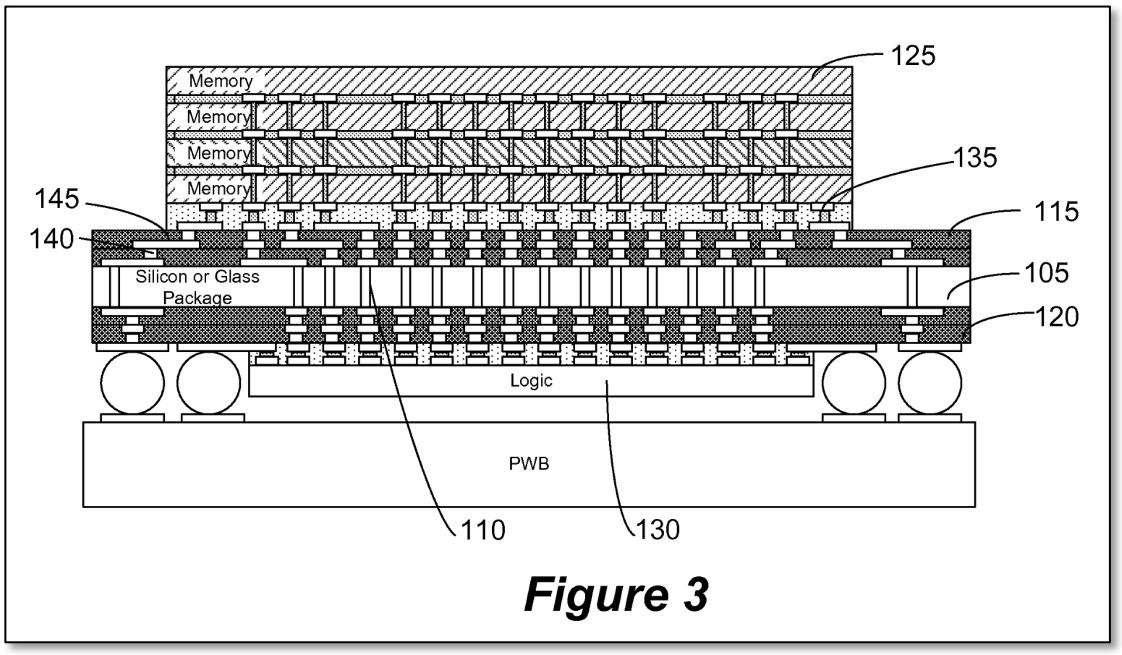


Figure 3

EX1004 at FIG. 3.

2. 1(a): "a solid layer having a first surface and a second surface opposite to said first surface,"

128. Sundaram's *chip package* (interconnect structure) comprises an "interposer 105 having a first side and a second side" (*a first surface and a second surface*) and is "made of…glass" or "polymer-glass laminates[.]" *EX1004* at 2:22-

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section. All reasonable expectations of success include the benefits described for the respective motivation to combine. All emphases added unless otherwise noted.

27, 5:54-58. Because interposer 105 is "made of…glass" or "polymer-glass laminates[,]" interposer is a *solid layer*. I note that the '763 Patent describes that a "glass layer 16 refers to an amorphous **solid**" and the "material of glass layer 16 may be…boro-silicate glass[.]" *EX1001* at 7:12-14. As discussed below at Claim 1(a)(ii), Sundaram teaches that interposer 105 (*solid layer*) comprises "glass," such as "borosilicate glass[.]" *EX1004* at 5:54-58, 9:14-16; ¶ 131. Thus, Sundaram's interposer 105 is a *solid layer* in at least the same way as described by the '763 Patent.

129. Additionally, Sundaram's interposer 105 (*solid layer*) comprises a *first surface and a second surface*. As shown in the image below, Sundaram's *second surface* is *opposite to said first surface*.

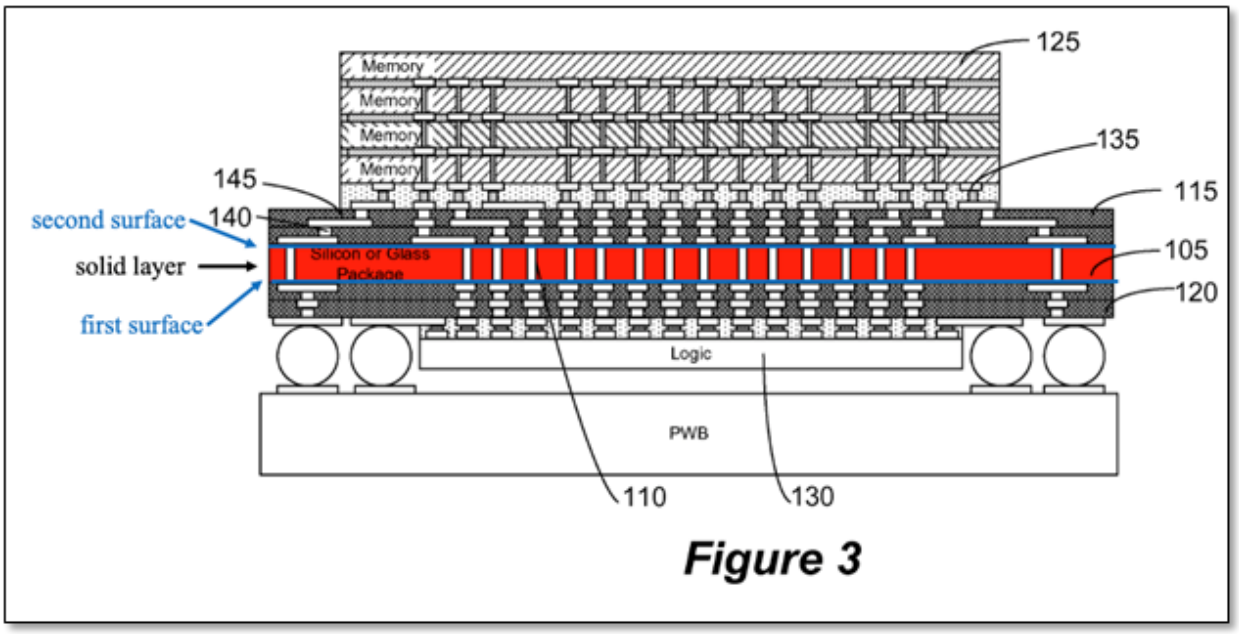


Figure 3

EX1004 at FIG. 3.

3. 1(a)(i): "wherein said first surface is substantially parallel to said second surface,"

130. Sundaram's *first surface* and *second surface* are parallel surfaces, as shown below. As such, Sundaram teaches *wherein said first surface is substantially parallel to said second surface*.

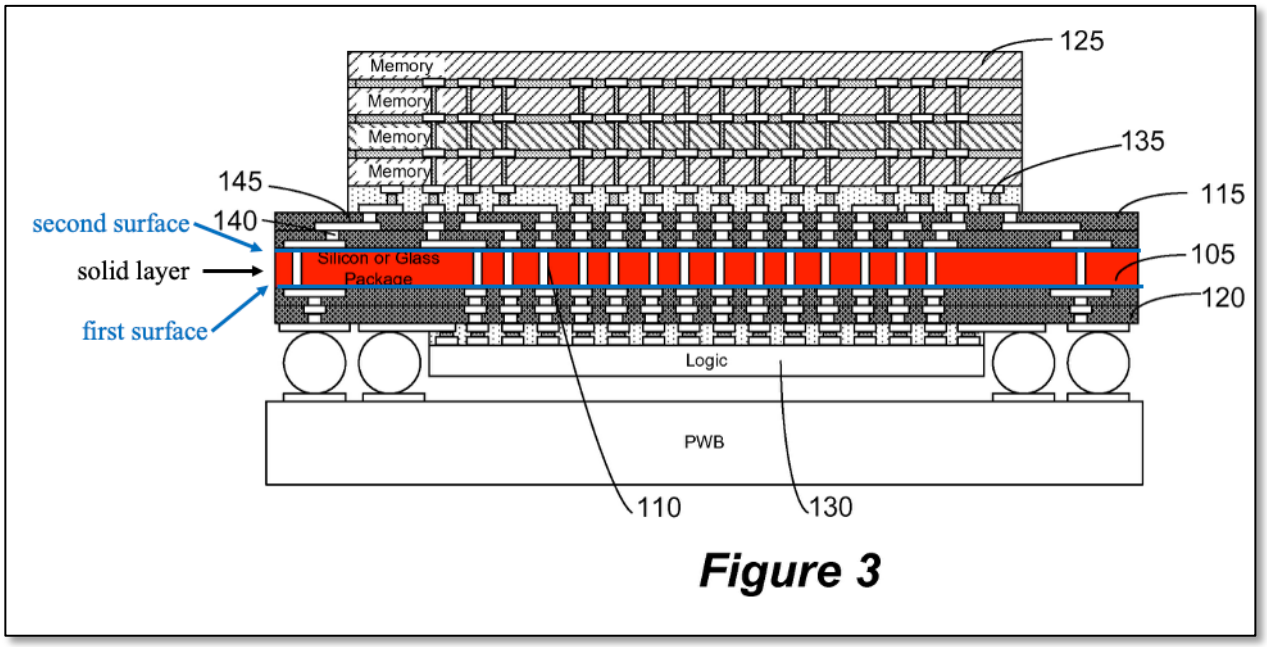


Figure 3

EX1004 at FIG. 3.

4. 1(a)(ii): "wherein said solid layer comprises a compound of silicon and oxygen,"

131. Sundaram's interposer 105 comprises "glass," such as "borosilicate glass" which is *a compound of silicon and oxygen*. *EX1004* at 5:54-58, 9:14-16; *EX1033* at 3:23-24 ("a borosilicate glass (**SiO_2**-B_2O_3)."); *EX1034* at 2:52-53 ("…the borosilicate glass powder contains **SiO_2**, B_2O_3, and K_2O[.]").

132. Alternatively, Sundaram teaches an interposer 105 comprises a "silicon core" with an "**SiO_2** dielectric isolation layer" as shown below in FIG. 34. *EX1004* at 5:54-58, 14:58-62.

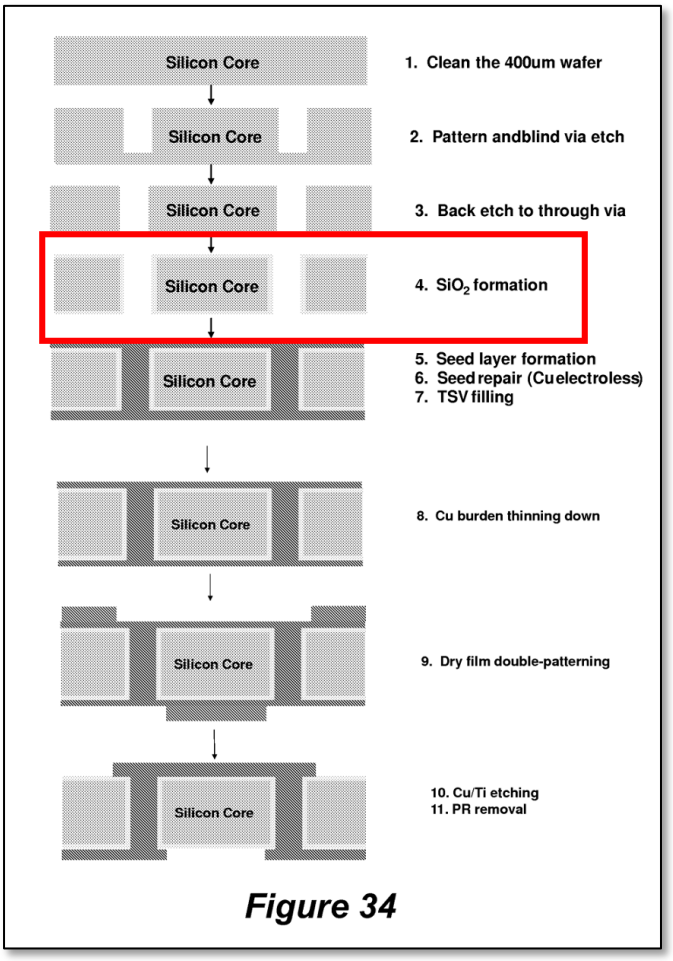


Figure 34

EX1004 at FIG. 34.

5. 1(a)(iii): "wherein said solid layer has a thickness between 100 and 300 micrometers,"

133. Sundaram's interposer (*solid layer*) is "about 20 to about 200 micrometers in thickness." *EX1004* at 2:22-25. Because Sundaram teaches a range that overlaps the claimed range, Sundaram teaches or renders obvious Claim 1(a)(iii). Specifically, the claim recites a *thickness between 100 and 300 micrometers*, which overlaps with Sundaram's teaching of 20 to about 200

micrometers, namely the range of 100-200 micrometers within the 20-200 range. Sundaram therefore expressly teaches a thickness, specifically 100-200 micrometers, that is within the claimed range of *between 100 and 300 micrometers* to thereby teach or render obvious Claim 1(a)(iii).

134. Additionally, Sundaram teaches an embodiment where a glass interposer has a thickness of 175 micrometers, which is a specific point within the claimed range of *between 100 and 300 micrometers*, further teaching the claimed range. *EX1004* at 9:14-16, FIG. 13. The FIG. 13 embodiment, like FIG. 3, is made of glass (e.g., "borosilicate glass") such that a POSITA would have recognized the applicability of the FIG. 13 embodiment to FIG. 3. *EX1004* at 9:14-16, 5:54-55. That is, a POSITA would have recognized that because FIG. 13 and FIG. 3's interposer are made of the same material (glass) that the specific thickness of 175 μm, which is within the thickness range of 20-200 μm, was an applicable example of a specific thickness at which FIG. 3's interposer 105 would be formed. *EX1004* at 9:14-16, 2:22-25.

135. I also note that the '763 Patent does not ascribe any criticality to the range of 100 and 300 micrometers. That is, the '763 Patent does not provide the range of 100 and 300 micrometers and then further provide an explanation for why such range is needed, important, or advantageous. Indeed, the '763 Patent describes

a variety of ranges, including smaller (20 micrometers) and much larger values (2000 micrometers), indicating to a POSITA that the thickness can vary widely and that the thickness is not otherwise critical. *See EX1001* at 7:54-60.

6. 1(a)(iv) "wherein said solid layer comprises a first region and a second region between said first region and an edge of said solid layer;"

136. As shown below, Sundaram's *solid layer* (interposer 105) comprises a *first region* (green) and a *second region* (blue). The *second region*, as shown, is *between said first region and an edge* (purple line) *of said solid layer*.

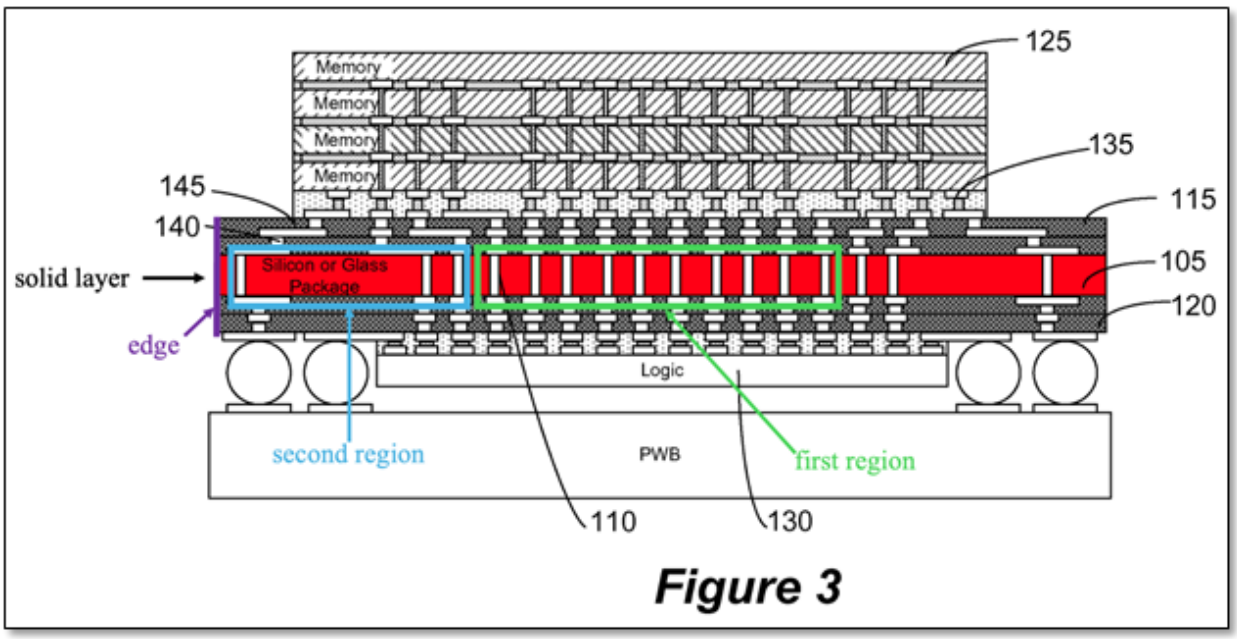


Figure 3

EX1004 at FIG. 3.

7. 1(b): "a plurality of copper plugs in a plurality of through vias in said second region of said solid layer respectively,"

137. Sundaram teaches a "plurality of ultra-small through vias 110 can be defined within the interposer 105 such that each of the through vias 110 extends from the first side 115 to the second side 120 of the interposer 105." *EX1004* at 6:6-9. Sundaram's through vias 110 are "metalized with a highly-conductive metal, for example **copper**." *EX1004* at 6:25-27. Because through vias 110 are "metalized with…copper[,]" Sundaram's through vias 110 are a *plurality of copper plugs in a plurality of through vias*. Further, the indicated through vias 110, as depicted below, are *in said second region of said solid layer respectively*.

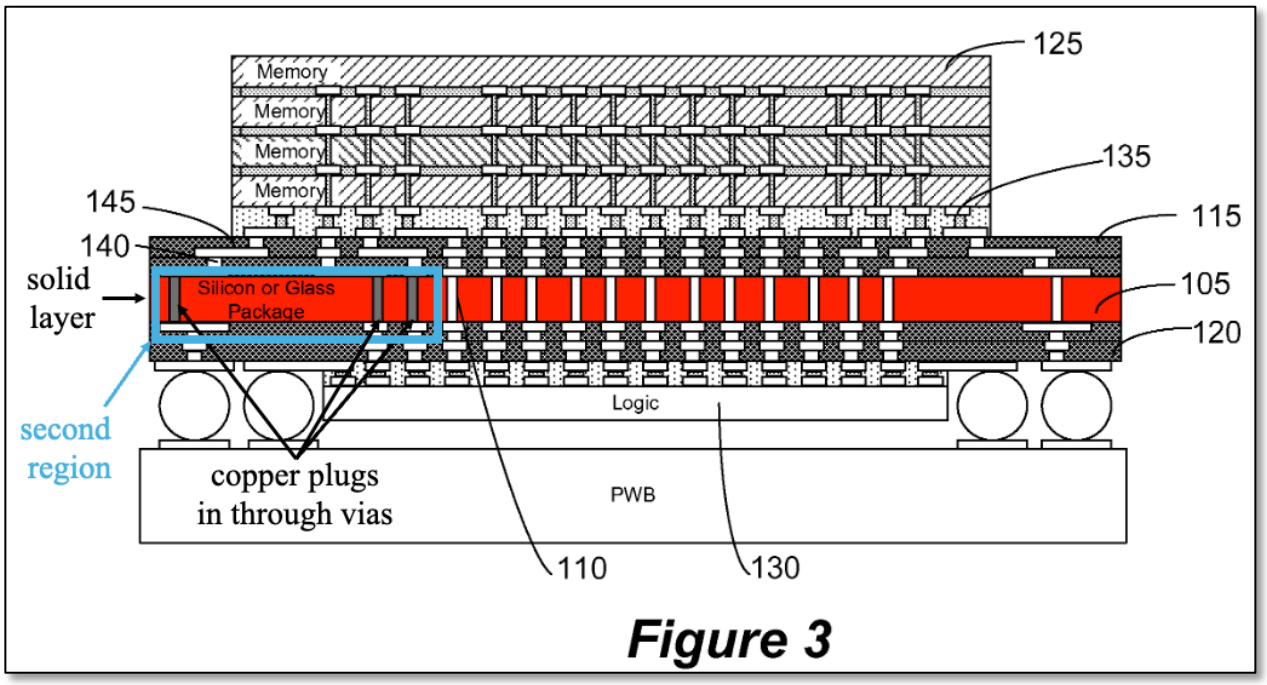


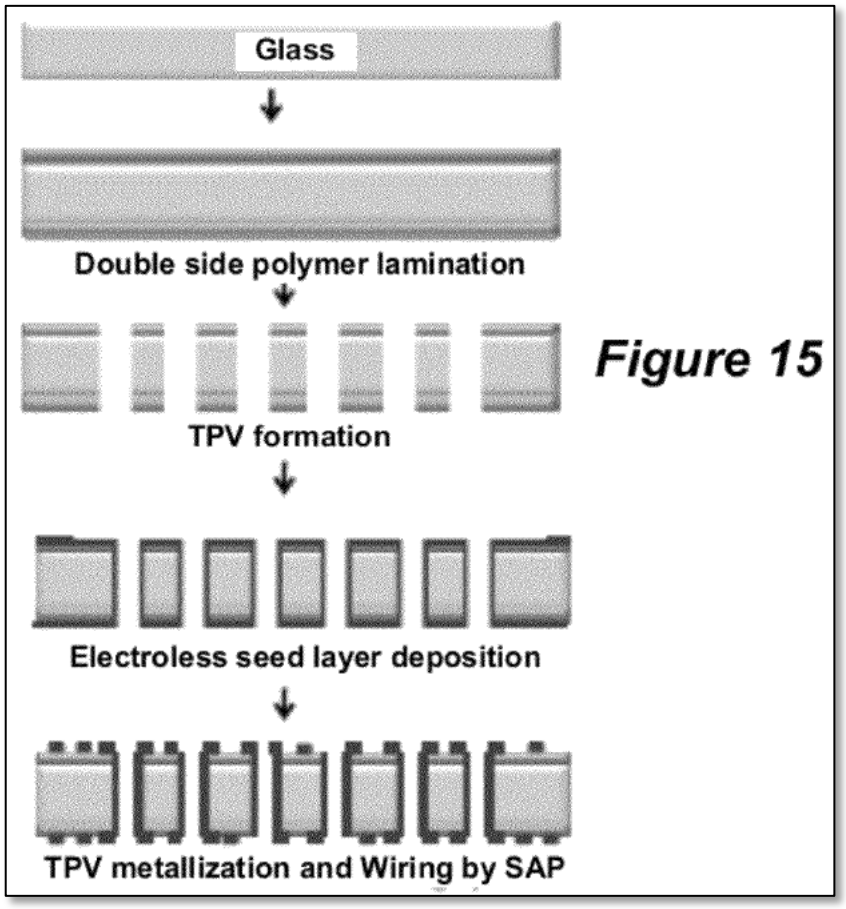
Figure 3

EX1004 at FIG. 3.

8. 1(b)(i): "wherein one of said plurality of copper plugs comprises a first copper layer contacting a sidewall of one of said plurality of through vias,"

138. Sundaram teaches the "through vias 110 can be metalized with a highly-conductive metal, for example copper." *EX1004* at 6:25-27. Because the through vias 110 are metalized with copper, through vias 110 comprise a *first copper layer contacting a sidewall* (i.e., sidewall of through via 110 provided by interposer 105) *of one of said plurality of through vias*. In other words, because through vias 110 are metalized with copper, the copper portion *contact[s] a sidewall* of through via 110, because the metallization process deposits copper onto the portion of interposer 105 providing the *sidewall*.

139. For example, as shown in FIGS. 15 and 34, a *first copper layer* is formed on the through vias, for example by "TPV metallization" in FIG. 15 and the "seed repair (Cu electroless)" and "TSV filling" in FIG. 34. *See also EX1004* at 10:26-28 ("Metallization of TPVs…was carried out using copper as metal SAP (semi additive plating) approach.").



EX1004 at FIG. 15.

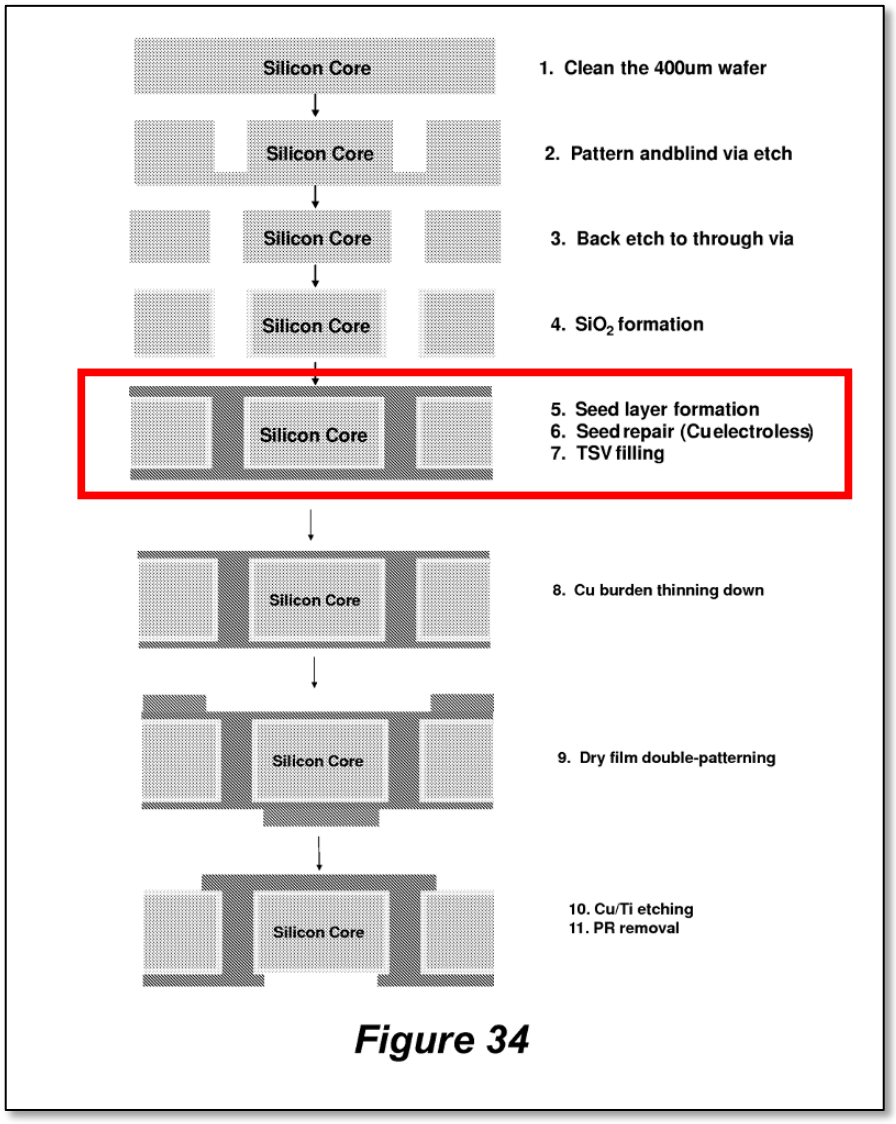


Figure 34

EX1004 at FIG. 34.

9. 1(b)(ii): "wherein said first region has a width in a direction greater than a shortest distance between said sidewall of one of said plurality of through vias and said edge of said solid layer in said direction and greater than a pitch between two neighboring copper plugs of said plurality of copper plugs;"

140. As shown below, Sundaram's *first region has a width in a direction* (denoted D1). The width D1 is *greater than a shortest distance between said sidewall of one of said plurality of through vias and said edge of said solid layer in said direction* (denoted D2). As shown D1 is *greater than* D2. Additionally, Sundaram teaches a *pitch between two neighboring copper plugs of said plurality of copper plugs* (denoted D3). As shown, D1 is *greater than* D3. Thus, Sundaram teaches *wherein said first region has a width in a direction greater than a shortest distance between said sidewall of one of said plurality of through vias and said edge of said solid layer in said direction and greater than a pitch between two neighboring copper plugs of said plurality of copper plugs*.

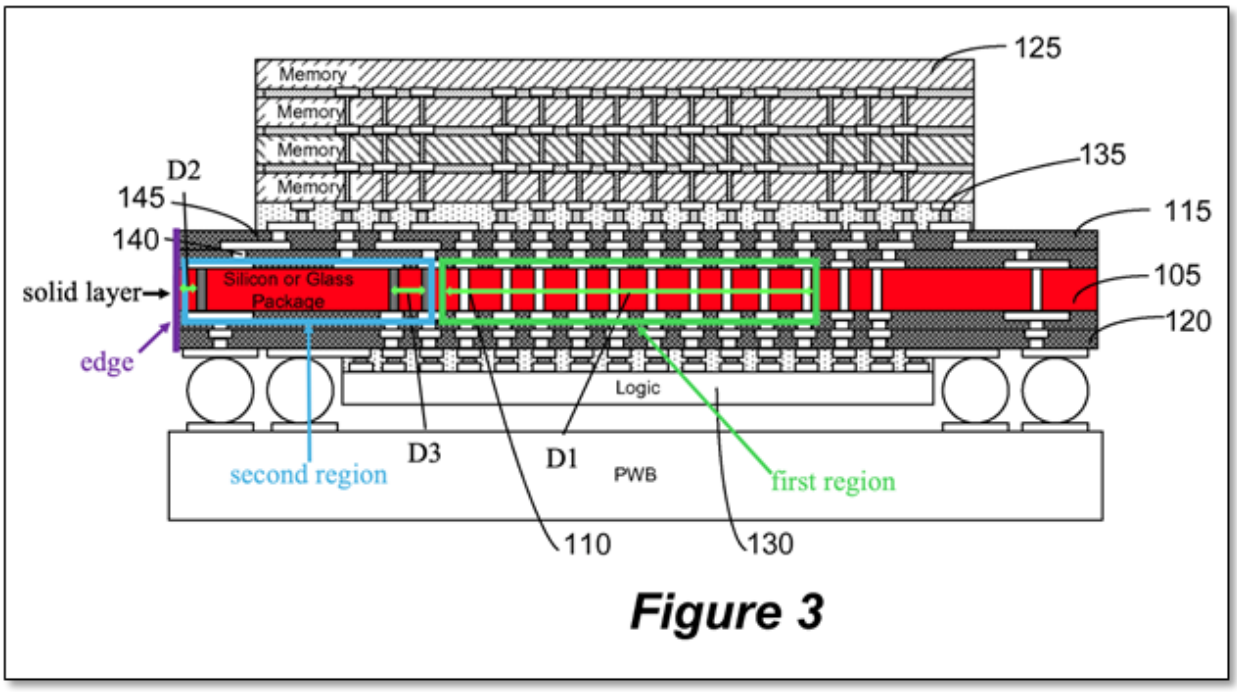


Figure 3

EX1004 at FIG. 3.

141. I note that annotated FIG. 6l provided by PO during original examination is below, which Applicant argued illustrates the claimed *width*, *shortest distance*, and *pitch*. As shown above, Sundaram's *first* and *second* regions mirror this arrangement. The claimed *regions* are not described in the '763 Patent's written description. Applicant relied solely on Applicant-annotated FIG. 6l.

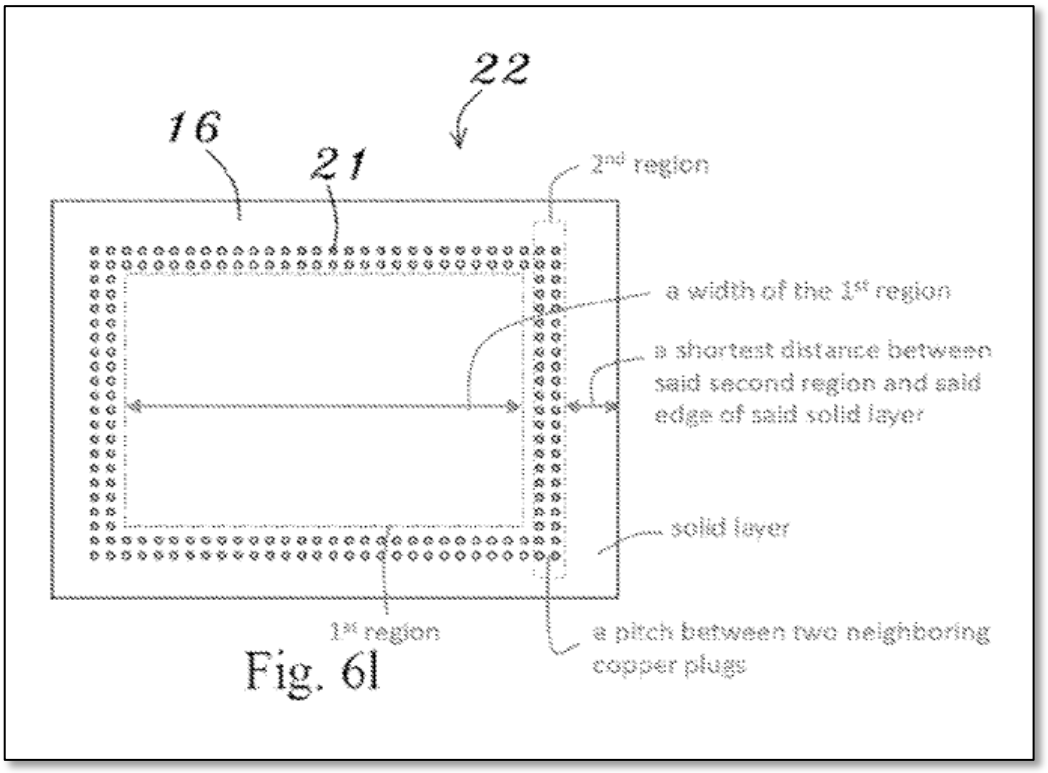


Fig. 6l

EX1002 at p. 272.

10. 1(c): "a first interconnection scheme over said first surface,"

142. Illustrated below, Sundaram teaches that "electronic devices having different I/O pad layouts and sizes can also be connected through the use of blind

vias 140 and conductor traces 145 defined within **polymer-metal redistribution layers** deposited on the first side 115 and second side 120 of the interposer 105." *EX1004* at 6:62-67. Additionally, Sundaram teaches "die pads 135 that are formed on the first 115 and second sides 120 of interposer 105 can electrically connect devices[.]" *EX1004* at 6:29-31. Because the blind vias 140 and conductor traces 145 within polymer-metal redistribution layers connect "electronic devices having different I/O pad layouts and sizes[,]" and because the die pads 135 formed on the second side 120 "electrically connect devices[,]" the vias 140, conductor traces 145, die pads 135, and polymer layer in the "polymer-metal redistribution layer" on second side 120 (*first surface*) are *a first interconnection scheme over said first surface*. In other words, because vias 140 and traces 145 in the polymer layer and die pads 135 connect (i.e., *interconnect[]*) devices 125 and 130, they collectively form an *interconnection scheme*.

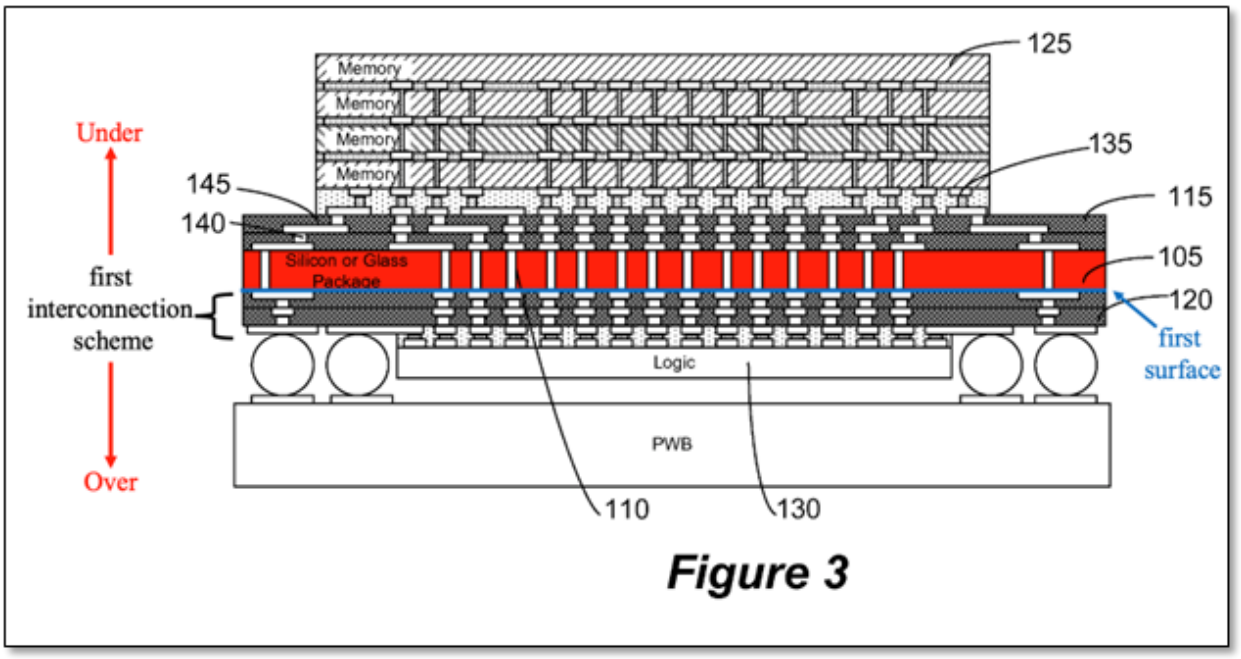
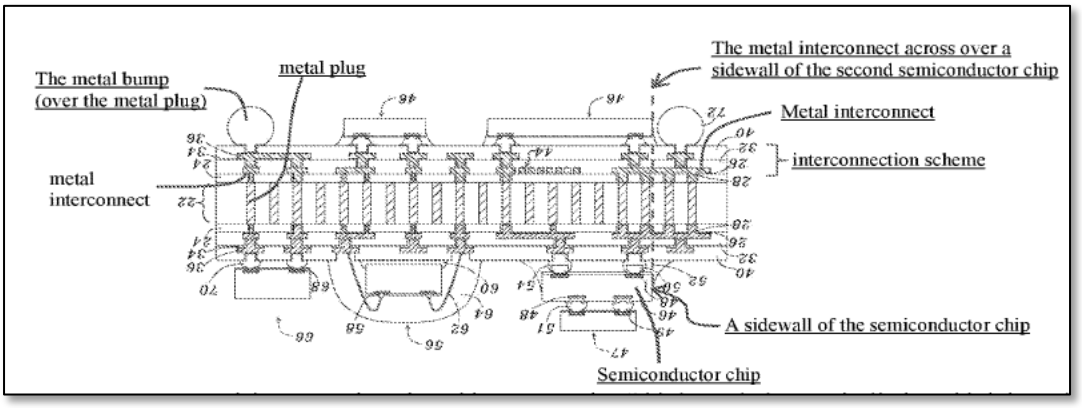


Figure 3

EX1004 at FIG. 3.

143. I note that the *over* and *under* directions are annotated on each figure where appropriate and kept consistent throughout the mappings. Particularly, the *over* direction is towards Sundaram's PWB (printed wiring board), as depicted above. The Patent Owner similarly used inverted figures during original prosecution of the '763 Patent's parent patent (USPN 11,107,768 (the '768 Patent)) to explain the *over/under* relationship between various claim elements. For example, Patent Owner provided an annotated version of FIG. 9x inverted during prosecution. *EX1032* at pp. 537-538, *see also EX1032* at pp. 395-400.



EX1032 at p. 537.

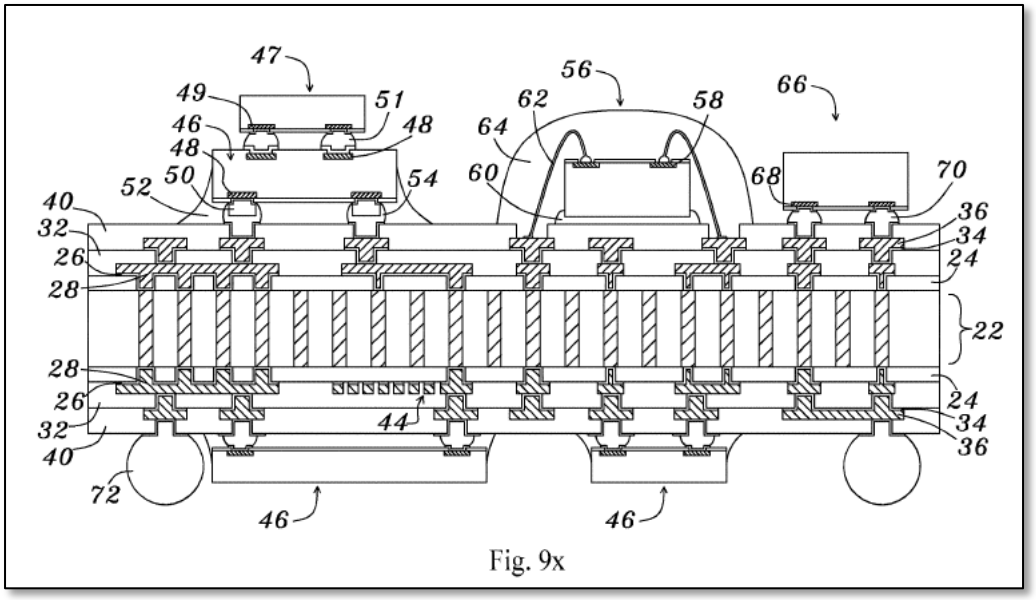


Fig. 9x

EX1001 at FIG. 9x.

11. 1(c)(i): "wherein said first interconnection scheme comprises a first metal interconnect over said first surface, a second metal interconnect over said first surface and a first polymer layer over said first and second metal interconnects,"

144. Because Sundaram teaches that "[m]etallization…on the surface of glass interposer" is done by "using copper as metal and SAP (semi additive plating

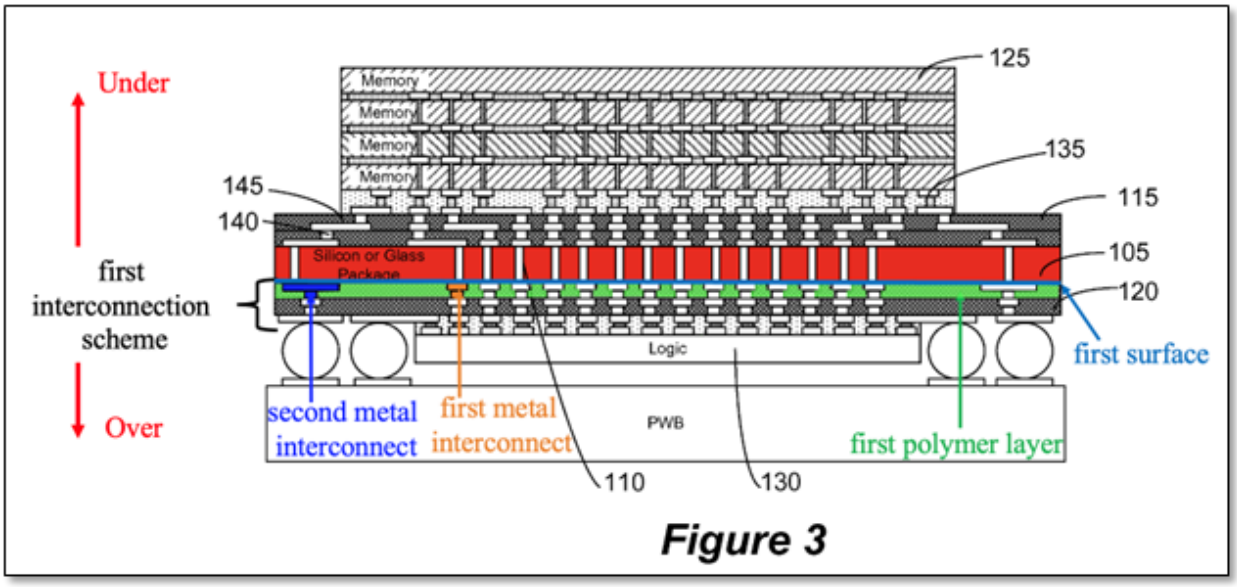
approach)[,]" a POSITA would understand the blind vias 140 and conductive traces 145 to be the "metal" in the "polymer-metal redistribution layers[.]" *EX1004* at 10:26-28, 9:63-65, FIG. 15, 6:62-67. Semi additive plating was a well-known technique used within a sequential build up (SBU) process flow to form circuitry in chip packages:

> "Circuitry is formed in a **semi-additive** process. The entire polymer surface, both dielectric and via hole walls, is seeded with a conductive material in a process derived from conventional circuit board processing, and a thin layer of electroless copper is deposited. A photoresist layer is deposited, patterned, and etched to expose the electroless copper and via holes in the desired circuit pattern. **Electroplated copper is added to the desired finished metal thickness**. Finally, the sacrificial dielectric layer is entirely removed, initial seed metal is stripped, and the SBU substrate is ready for the addition of the next layer pair. The process is repeated for the desired number of layers."

EX1035 at p. 643.

145. Thus, because the blind vias 140 and conductive traces 145 are *metal* and because they connect "electronic devices having different I/O pad layouts and sizes[,]" blind vias 140 and conductive traces 145 are *metal interconnects* of the *first interconnection scheme*. *EX1004* at 6:62-65, 7:4-8. A *first metal interconnect* comprising a trace 145 (longer rectangles in FIG. 3) and a via 140 (shorter rectangles) and a *second metal interconnect* comprising another trace 145 and via

140 in Sundaram's RDL is shown below, along with a *first polymer layer* that is *over said first and second metal interconnects* (the "polymer" of the "polymer-metal redistribution layers."). *EX1004*, 6:62-67. The *first polymer layer* at least includes the below green highlighted layer but may include an additional portion of the RDL (*see* Claim 14).



EX1004 at FIG. 3.

146. Alternatively, Sundaram's outermost layer of the RDL is *a first polymer layer* and is *over* the *first/second metal interconnects*.

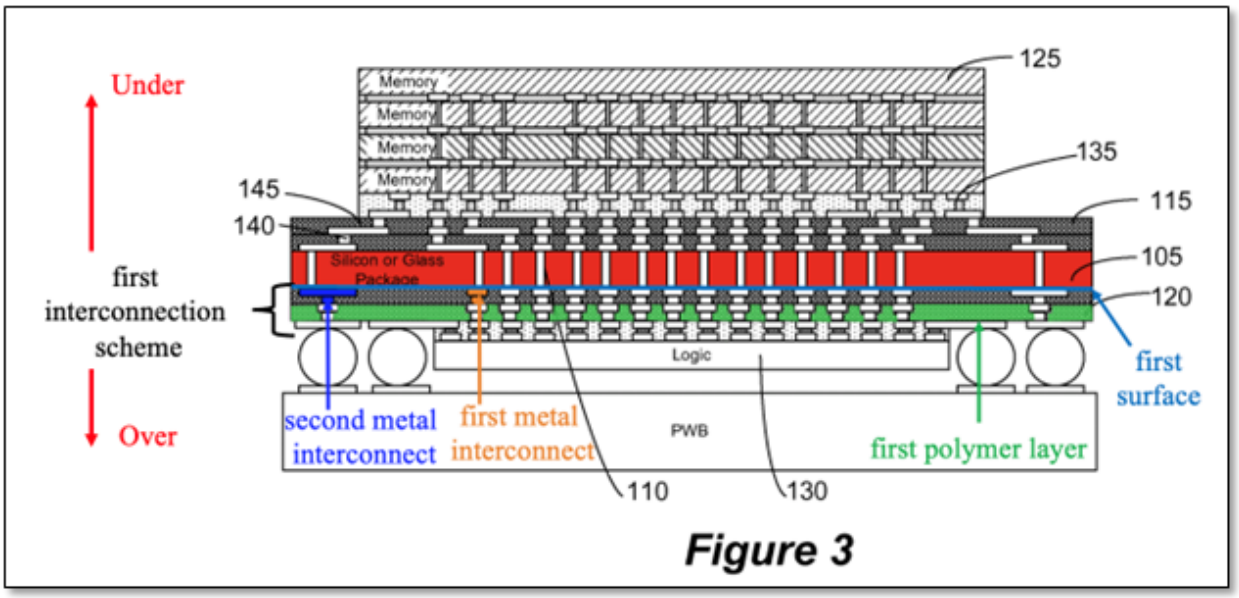
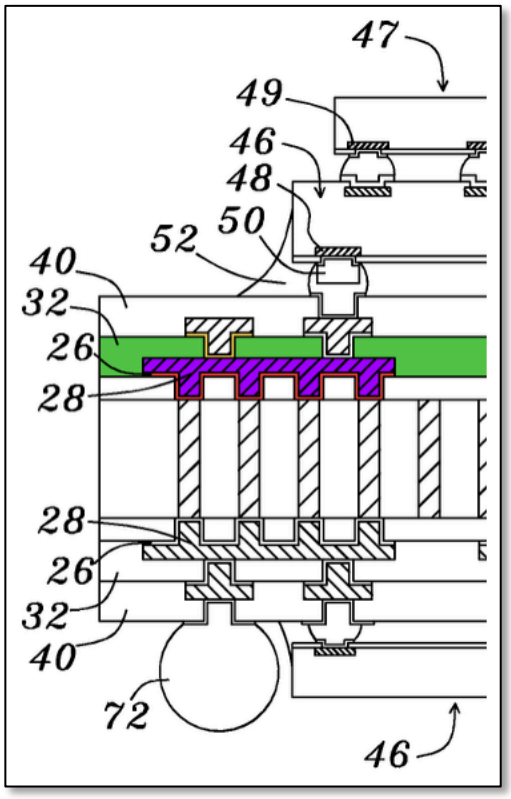


Figure 3

EX1004 at FIG. 3. I note that Sundaram's teaching of the polymer as being over each of the first and second metal interconnects is consistent with what is described by the related '768 Patent. Specifically, during prosecution of the '768 Patent, Patent Owner expressly pointed to dielectric layer 72 as being the second polymer layer. *EX1032* at 397. As can be seen in the below figure, dielectric layer 32 (the second polymer layer, according to the Patent Owner) is "over" metal layers 26, 28 and partially over metal layer 34, of the metal interconnect. As such, Sundaram's second polymer layer is over each of the first, second, and third metal interconnect[s] in at least the same way as described by the '768 Patent.



EX1001 at FIG. 9X (excerpt).

12. 1(c)(ii): "wherein said first metal interconnect is connected to a first copper plug of said plurality of copper plugs, wherein said second metal interconnect is connected to a second copper plug of said plurality of copper plugs,"

147. Sundaram teaches the "first electronic device 125 is of a different pad size and configuration than the second electronic device 130, and they are connected with through vias 110, blind vias 140, and conductor traces 145." *EX1004* at 7:4-8. Because devices 125, 130 are connected by blind vias 140, traces 145, and through vias 110, the traces 145 and vias 140 on either side of interposer 105 are connected by vias 110. Thus, as shown below, the *first metal interconnect is connected to a*

first copper plug of the said plurality of copper plugs, and the *second metal interconnect is connected to a second copper plug of the said plurality of copper plugs*.

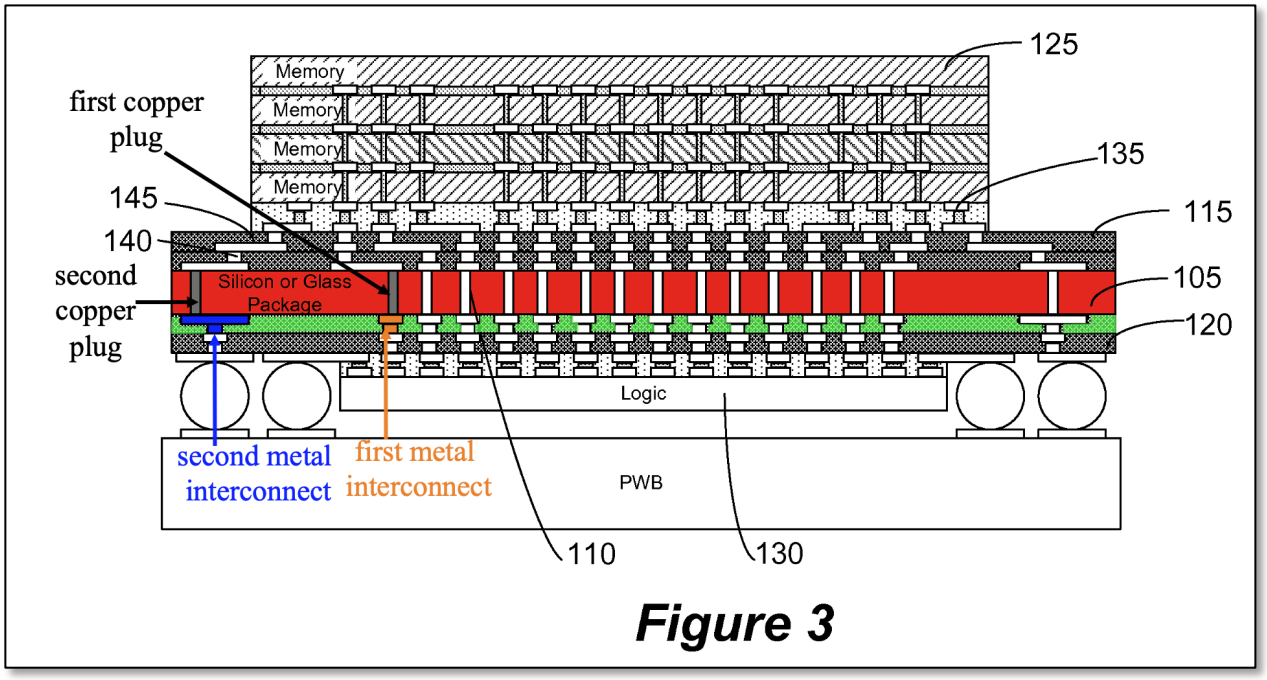


Figure 3

EX1004 at FIG. 3.

13. 1(c)(iii): "wherein said first metal interconnect comprises a first metal layer and a second copper layer over said first metal layer;"

148. As I described above, the blind vias 140 and conductor traces 145 are the "metal" in the "polymer-metal redistribution layers." *See* ¶ 144. Additionally, as shown in FIG. 15, Sundaram expressly teaches a *first metal layer* formed by "direct metallization using wet electroless copper deposition" and *a second copper layer*

over said first metal layer formed by "semi-additive plating" using "copper as metal." *EX1004* at 9:61-65, 10:26-28. The *first metal layer* is provided by the electroless copper seed layer that is shown on the top of glass interposer in FIG. 15 and the *second copper layer* is shown as the SAP wiring on top of the copper seed layer.

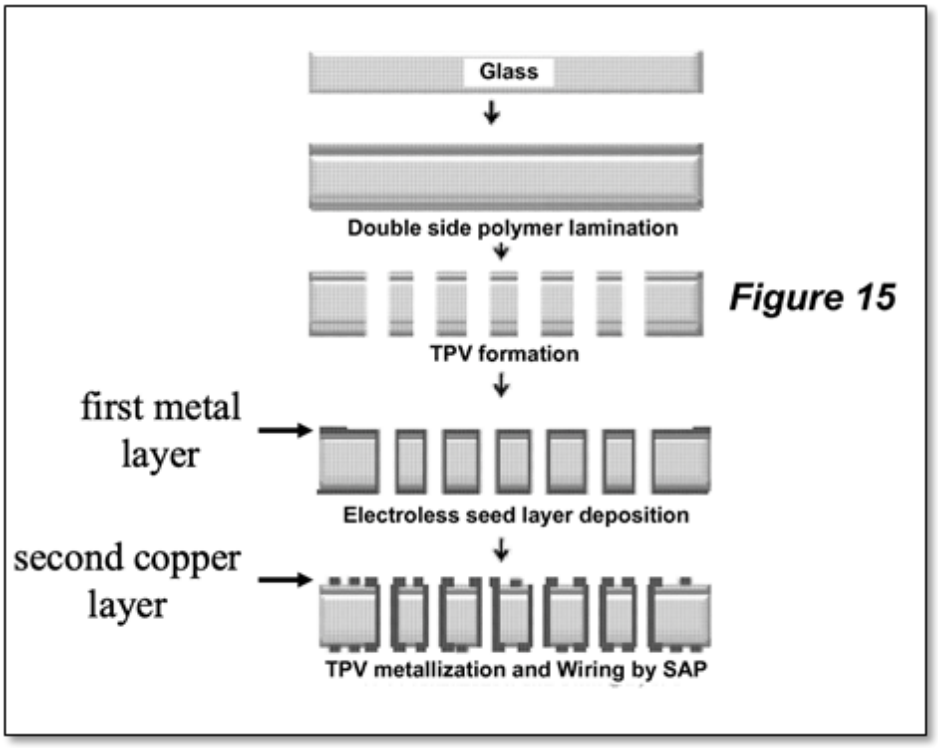


Figure 15

EX1004 at FIG. 15.

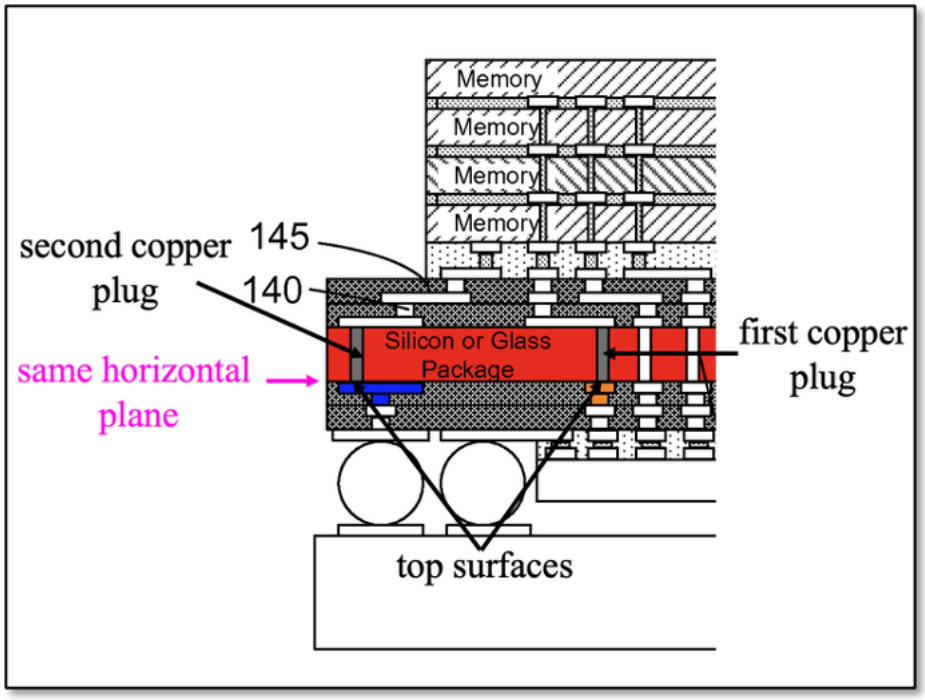
149. To the extent it is argued FIGS. 3 and 15 are separate embodiments, a POSITA would have been motivated and found it obvious to modify Sundaram's vias 110 in FIG. 3 per FIG. 15's SAP teachings. As discussed, Sundaram teaches interposer 105 in which vias 110 are formed is glass. Because glass is an insulator,

a POSITA would have in fact understood it to be necessary to use a seed layer in order to grow the second copper layer via electroplating, as an electrode is needed for uniform formation of an electroplated copper layer. *EX1104* at 2:46-48 ("The copper seed layer provides an electrode for the subsequent copper electroplating…"). Indeed, it was known that a "missing seed layer" may "lead to a void in the electroplated metal" resulting in an "increase in their resistance and result in poor reliability." *EX1063* at 3:12-16. Thus, there would have been ample motivation to modify FIG. 3 per FIG. 15's teachings. Furthermore, a POSITA would have had a reasonable expectation of success because both FIG. 15 and FIG. 3 have the same substrate material, i.e., glass and because the use of metallic seed layers for plating metal interconnects was commonplace. *EX1004* at 10:9-15, 8:1, 5:54-59; *see, e.g.*, *EX1005* at [0057], [0060].

14. 1(c)(iv): "wherein a top surface of said second copper plug and a top surface of said first copper plug are substantially in the same horizontal plane;"

150. As discussed, Sundaram teaches the "each of the through vias 110" (*first* and *second copper plug[s]*) "extends from the first side 115 to the second side 120 of interposer 105[,]" meaning that each of the through vias 110 have an end surface *substantially in the same horizontal plane*. *See* ¶ 137. Thus, as shown below,

Sundaram teaches *wherein a top surface of said second copper plug and a top surface of said first copper plug are in the same horizontal plane.*



EX1004 at FIG. 3.

15. 1(d): "a first metal bump over said first interconnection scheme"

151. Sundaram teaches that "die pads 135 formed on the first 115 and second sides 120 of the interposer 105 can electrically connect devices using…**copper bumps** with solder caps[.]" *EX1004* at 6:29-31. An example of one of Sundaram's copper bumps with solder caps is shown below, which is a *first metal bump* (i.e., because it is made of copper) *over said first interconnection scheme*.

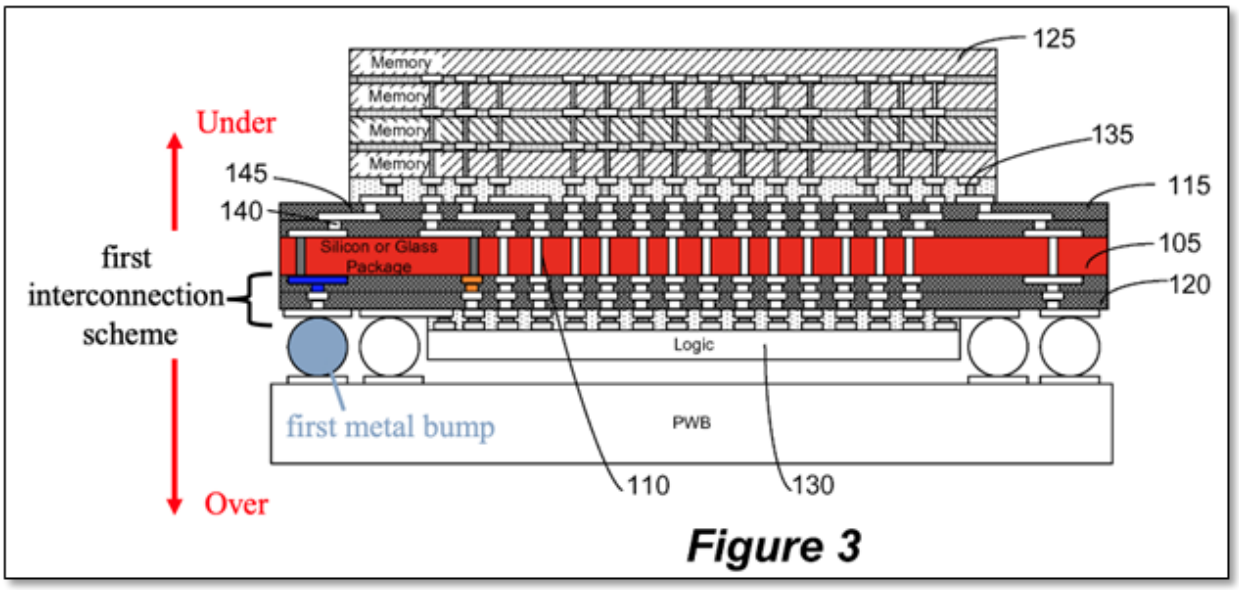


Figure 3

EX1004 at FIG. 3.

16. 1(d)(i): "wherein said first metal bump comprises a second metal layer and a tin-containing layer over said second metal layer; and"

152. As discussed above, Sundaram's *first metal bump* is a "copper bump[s] with [] solder cap[]." *See* ¶ 151; *EX1004* at 6:29-31. Thus, Sundaram's *first metal bump comprises a second metal layer* (the copper bump). A POSITA would have further understood the "solder cap" to be a *tin-containing layer* because "traditional solders are…most commonly a **tin**-lead alloy (Sn-37% Pb) having about 37% lead in a **tin** base material." *EX1094* at [0003]. Additionally, Sn-based solders were dominant in commercial packages such as those taught by Sundaram. Thus, the context of the chip packages of Sundaram means that "solder" necessarily includes Sn-content, thereby teaching the *tin-containing layer*. A POSITA would have

understood Sundaram's disclosure of "solder" to mean the solder contains tin unless stated otherwise. That is, if someone refers to non-tin-containing solder, it would be specified as such because the "default" solder contains tin.

a) Lin-191's Teachings

153. Additionally or alternatively to Sundaram's teachings, Lin-191 teaches a *bump* with the claimed layers. Specifically, Lin-191 teaches a system-in-package including "solder bumps or balls 29a" formed by reflowing a "solder layer 29," which is "**a tin-containing layer**" formed "on the "metal layer 28." *EX1005* at [0320]. Layer 28, along with "adhesion layer 18, the seed layer 19, and metal layer[]27…compose an under bump metallurgic (UBM) layer." *EX1005* at [0323]. Layers 18, 19, are *metal*. *EX1005* at [0308]. The UBM layer is, collectively, a *second metal layer* and layer 29 is the *tin-containing layer*.

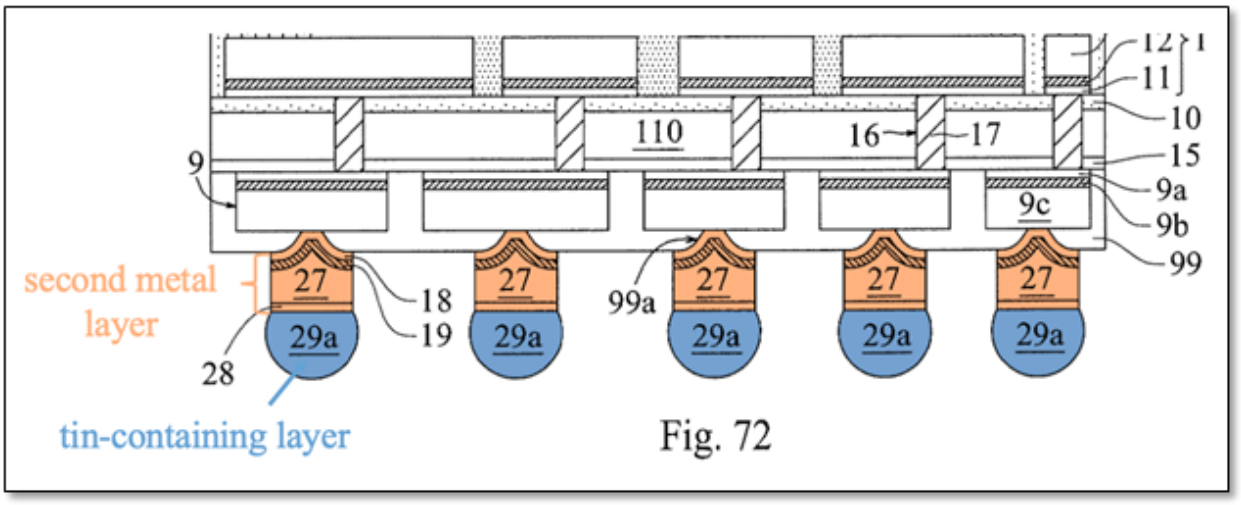


Fig. 72

EX1005 at FIG. 72 (excerpt).

154. Thus, Lin-191 teaches a *metal bump compris[ing] a second metal laye*r (UBM) and a *tin-containing layer* (solder layer 29) *over said second metal layer*.

b) Motivation to Combine

155. A POSITA would have been motivated and found it obvious to apply Lin-191's teachings of a metal bump having a *tin-containing layer over a second metal layer* to Sundaram's *first metal bump*. As discussed, Sundaram teaches traditional solder that a POSITA would have understood to contain tin and Lin-191 further discloses a solder layer that is a *tin-containing layer*, further motivating the combination. A POSITA would have appreciated the advantage of a *tin-containing layer*, as tin was known to "wet and spread on a wide range of substrates[,]" which a POSITA would have considered desirable as wettability was an important factor for forming various types of interconnects. *EX1098* at p. 104. Additionally, tin used in limited thickness was known to form IMCs with metals used in electronic assemblies, thereby achieving "good bonding." *EX1099* at p. 20. Tin-containing solder was further known to be advantageous due to tin's "relatively low melting point" which would allow for solder reflow to occur without damaging other components of the chip package unable to withstand high temperatures. *EX1134* at [0026]. Further, "[a]nother advantage is the existence of substantial experience and database in the use of tin solders compiled over a long history." *EX1099* at p. 20.

Thus, Lin-191's solder bump or ball 29a having a *tin-containing layer* would have predictably improved the mechanical connection of Sundaram's *first metal bump* to die pad 135 by achieving "good bonding[,]" would have provided the benefit of a low melting point, and would have been a straightforward material choice given the substantial amount of data generated by extensive use. *EX1099* at p. 20.

156. Further, a POSITA would have been motivated to implement Lin-191's UBM layers as UBM layers were known to "improve the adhesive strength of solder balls" and to "prevent[] diffusion of unnecessary substances" of solder balls into nearby substrates. *EX1037* at 5:3-5. For example, Lin-191's UBM structure includes an adhesion layer 18 that may be "chromium" or a "titanium-tungsten alloy[,]" which were known materials for use in UBM structures that "improve the adhesion and reliability of solder bumps." *EX1038* at 2:24-29; *EX1005* at [0308], [0311].

157. Further, regarding the copper layer 27 in Lin-191's UBM structure, copper was known to have "good conductivity and good ductility" which provides "improved thermal performance by counteracting thermal stress[,]" thus further motivating the combination. *EX1039* at 13:38-41. Metal layer 28 which may be made of "nickel" would allow a POSITA to leverage the aforementioned advantage of copper layer 27, while minimizing the risk of copper diffusion into the solder balls. Indeed, nickel was known to prevent copper diffusion into adjacent structures.

EX1040 at Abstract ("The structure comprises a layer of barrier metal, preferably nickel, that resists copper diffusion."). A POSITA would have been familiar with the issue of copper diffusing into adjacent structures, such as solder balls. Indeed, it was known that "when used with Sn solder material, sufficient Cu diffusion from Cu pillar bump into the solder forms thick IMC [(Inter Metallic Compound)] such as Cu_6Sn_5 and Cu_3Sn through the reaction between the diffused Cu and Sn in the solder. Thick IMC layers reduce mechanical strength of the Cu pillar bump because the IMC layers are brittle." *EX1041* at [0005]. Further, "IMC formation will cause bump crack or unwanted stress" and "the thicker IMC also results in poor adhesion." *EX1041* at [0005]. As such, a POSITA would have wanted to prevent such loss of mechanical strength that leads to joint failure (i.e., by cracking or unwanted stress) and been motivated to include nickel layer 28 to prevent copper diffusion contributing to such issues.

158. The Sundaram-Lin-191 combination is merely the application of a known technique (Lin-191's solder bump structure) to a known device (Sundaram's bump) ready for improvement to yield the predictable result of Sundaram's *first metal bump* being formed with Lin-191's solder bump structure including *a tin-containing layer over [a] second metal layer*.

159. Alternatively, the Sundaram-Lin-191 combination is the simple substitution of Lin-191's solder bump structure, including the *tin-containing layer over said second metal layer*, for Sundaram's *first metal bump*. The substitution would have yielded predictable results at least because Lin-191's solder ball structure (i.e., solder ball 29a and UBM layers) and Sundaram's metal bump both serve the same function i.e., connecting interconnects to a PWB/PCB. *EX1005* at [0324]; *EX1004* at FIG. 3. Additionally, Lin-191 teaches forming the solder bump structure using well-known manufacturing techniques, such as electroplating. *EX1005* at [0320-0324].

160. A POSITA would have had a reasonable expectation of success in either applying Lin-191's teachings to Sundaram's *first metal bump* or substituting Sundaram's *first metal bump* with Lin-191's structure at least because such a modification/substitution would have involved the application of well-known manufacturing techniques well within the skill of a POSITA. For example, sputtering, electroplating, and reflowing, taught by Lin-191 to form solder ball 29a and UBM layers were well-known techniques that a POSITA would have been familiar with. *See, e.g., EX1005* at [0309]-[0320], [0323]; *EX1042* at ("…filled with copper typically by an electroplating process, as known to one of ordinary skill in the art of integrated circuit fabrication."); *EX1043* at [0032] ("…variety of different

deposition methods known by one of ordinary skill in the art, including but not limited to, CVD, pulsed CVD, PECVD, ALD, PEALD, or sputtering methods."); ¶¶ 71-75. Because Sundaram and Lin-191's solder ball structures perform similar functions and because standard techniques were used to form Lin-191's solder ball and UBM layers, a POSITA would have had a reasonable expectation of success. Moreover, metal bump technology, including layered bump structures, were commonplace prior to the '763 Patent, thereby further contributing to a reasonable expectation of success. *See* ¶¶ 67-69.

17. 1(e): "a first semiconductor chip under said first interconnection scheme,"

161. Sundaram teaches a "first electronic device 125" that "can be… stacked memory IC devices" such that a memory chip of the stack is *a first semiconductor chip under said first interconnection scheme. EX1004* at 6:37-45, FIG. 3, FIG. 33. As shown, Sundaram's first electronic device 125 is a *first semiconductor chip under said first interconnection scheme*.

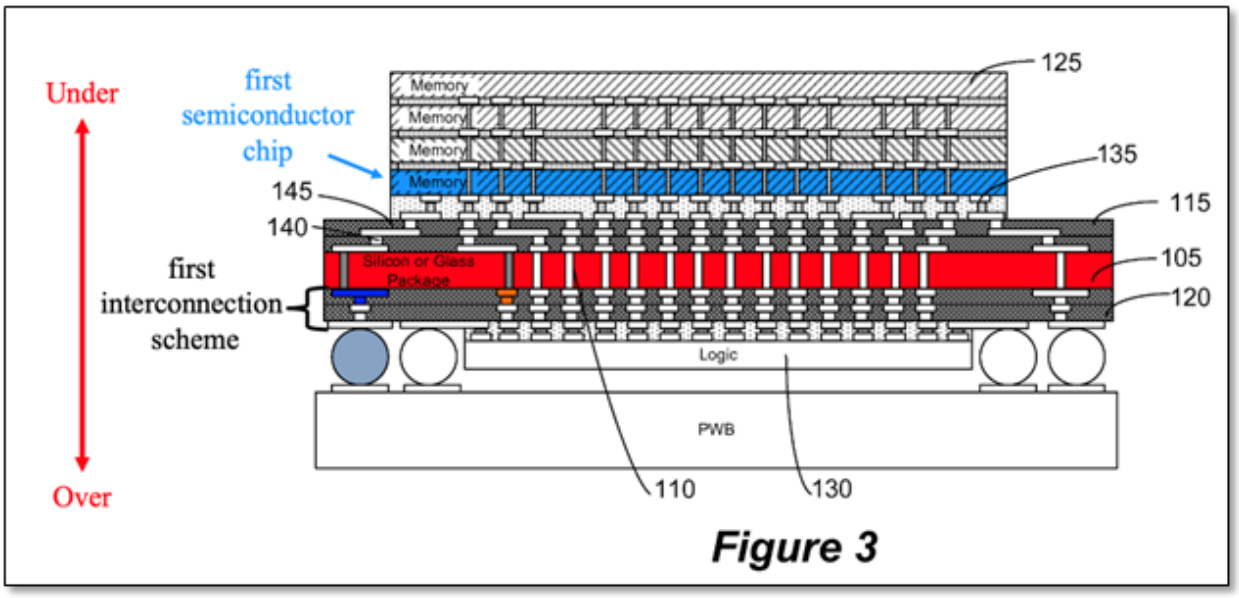


Figure 3

EX1004 at FIG. 3.

18. 1(e)(i): "wherein said first semiconductor chip comprises a third metal interconnect on a first metal pad of said first semiconductor chip,"

162. Sundaram's interposer 105 has die pads 135 where "metallization provides die pad surfaces 135[.]" *EX1004* at 6:23-25. A POSITA would understand that, like interposer 105, first electronic device 125 (*first semiconductor chip*) also has die *pad[s]* (one shown in purple below) such that an electrical connection is made between first electronic device 125 and interposer 105. Indeed, it was known that "I/O terminals were traditionally formed by way of metal pads along the periphery of an IC." *EX1095* at 1:24-25. Thus, a POSITA would understand the *pad* (purple) shown in FIG. 3 to be a *first metal pad*. Further, Sundaram teaches "die pads 135…can electrically connect devices using solder, copper bumps with solder

caps, copper to copper bonding," each of which teaches *a third metal interconnect* because they "electrically connect devices" and because they are made of *metal* i.e., solder, copper. *EX1004* at 6:29-33. In FIG. 3, below, the *third metal interconnect* is depicted as a bump on the metal pad.

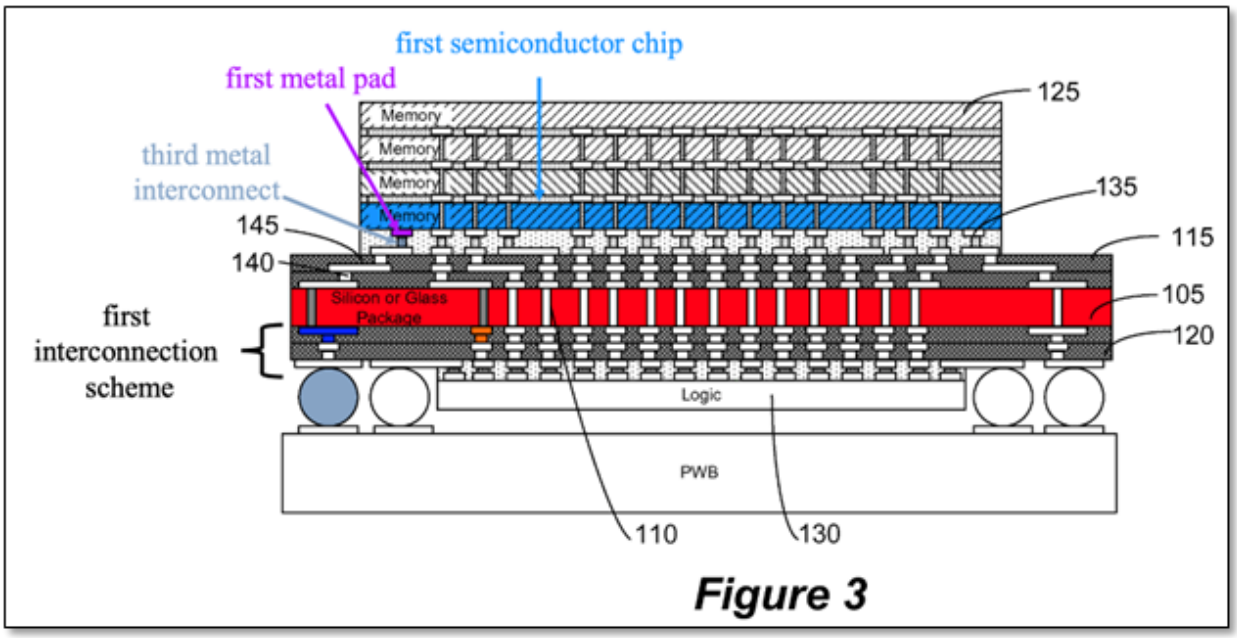


Figure 3

EX1004 at FIG. 3.

163. Sundaram further depicts such *metal pad[s]* in FIG. 32, which shows a "side-by-side configuration" of the interconnect structure wherein each chip in the memory chip stack comprises a metal pad on both top and bottom. *EX1004* at 4:26-27, 7:56-59.

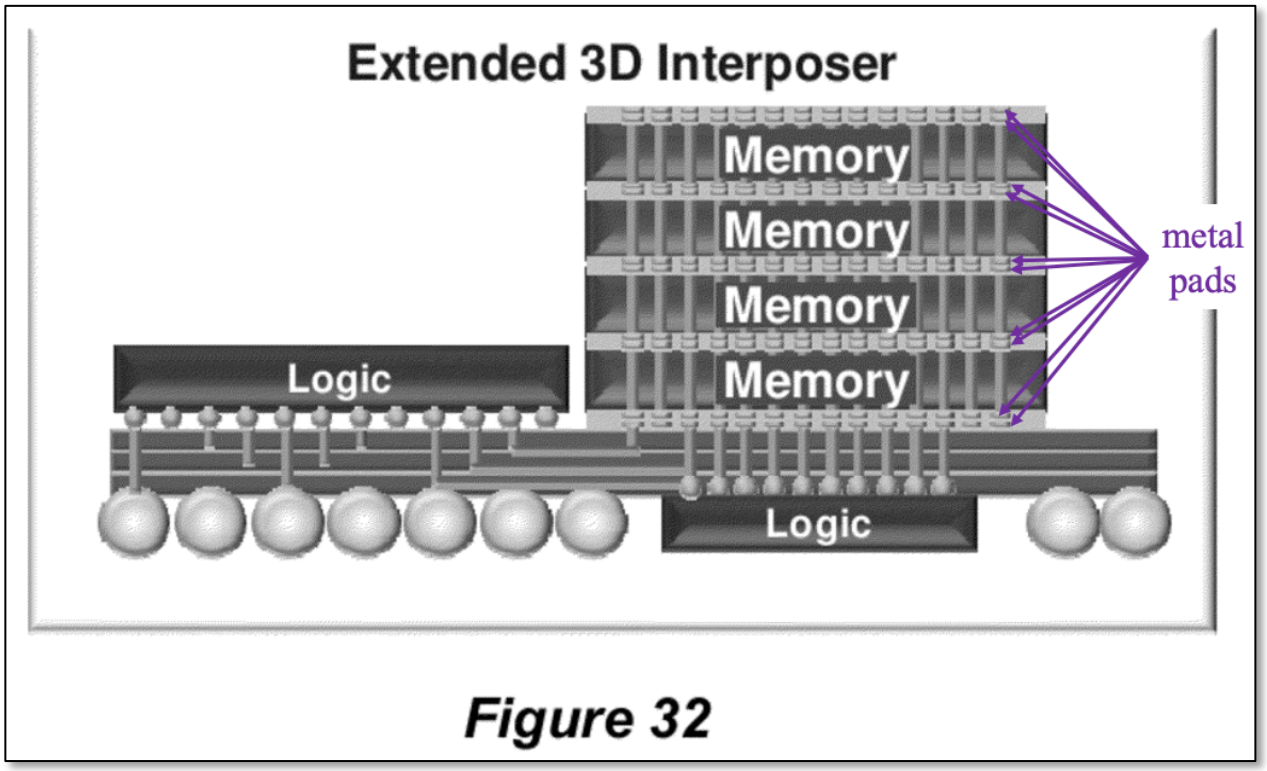
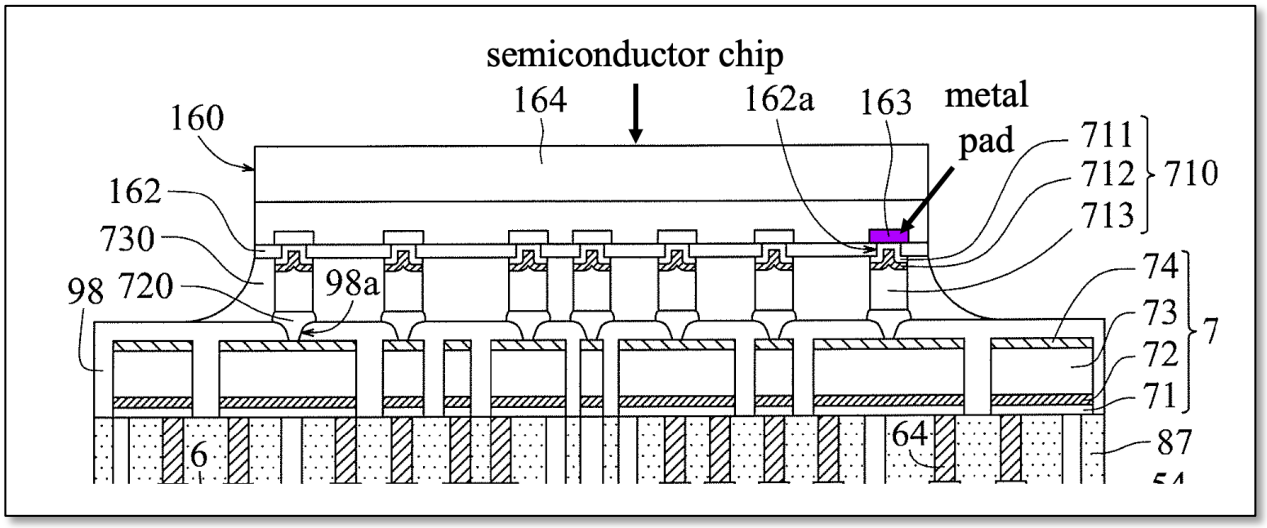


Figure 32

EX1004 at FIG. 32. The below MTC and reasonable expectation of success for modifying Sundaram's chip to have a *metal pad* and are incorporated herein. *See* ¶¶ 165-166.

a) Lin-191's Metal Pad Teachings

164. Additionally or alternatively to Sundaram's teachings of a *first metal pad*, Lin-191 teaches a *metal pad*. Depicted below, Lin-191 teaches a "semiconductor chip 160" comprising "multiple metal traces or pads 163." *EX1005* at [0383]. Lin-191's "metal traces or pads 163" are made of "aluminum" and are connected to "metal pillars or bumps 710[.]" *EX1005* at [0384]. Lin-191's semiconductor chip 160 thus comprises a *metal pad*.



EX1005 at FIG. 71 (excerpt).

b) Motivation to Combine

165. A POSITA would have been motivated and found it obvious to apply Lin-191's teachings of a *metal pad* to Sundaram's *first semiconductor chip*, thereby yielding the predictable result of Sundaram's *first semiconductor chip* (first electronic device 125) having a *metal pad*. Modifying Sundaram's pad to be metal, thereby yielding a *first metal pad*, is merely an implementation detail in Sundaram's overall system, i.e., Lin-191 provides the specificity of a semiconductor contact pad being *metal*. Given that metal contact pads were ubiquitous in semiconductor chips, a POSITA would have been motivated to turn to references teaching materials for contact pads (e.g., Lin-191) to ensure an electrical connection is made between Sundaram's first electronic device 125 and the bump (i.e., by a conductive *metal*

pad). *See, e.g., EX1044* at 2:30-33 ("In FIG. 1, a **metal pad** 12 is formed on a semiconductor material 10. Metal pad 12 may be formed from a conductive metal…") (emphasis added); *EX1045* at [0006] ("FIG. 1 illustrates a portion of flip chip 10 with a solder bump 12 formed on **metal contact pad** 14.") (emphasis added); *EX1046* at [0018] ("Bumps 105 electrically and possibly physically contact the I/O pads (**metal pads**) 103 of the IC chip 100."); *EX1095* at ("I/O terminals were **traditionally** formed by way of **metal pads** along the periphery of an IC.").

166. The combination is application of a known technique (metal pads) to a known device (Sundaram's semiconductor chip) ready for improvement to yield the predictable result of Sundaram's first electronic device 125 having a *first metal pad*, per Lin-191. *EX1005* at [0081]. As I described above, metal contact pads were ubiquitous and necessary for forming interconnections between the chip and other components, so a POSITA would have had a reasonable expectation of success in modifying Sundaram's first electronic device 125 to have *first metal pad*, such as aluminum, per Lin-191. *See* ¶ 165.

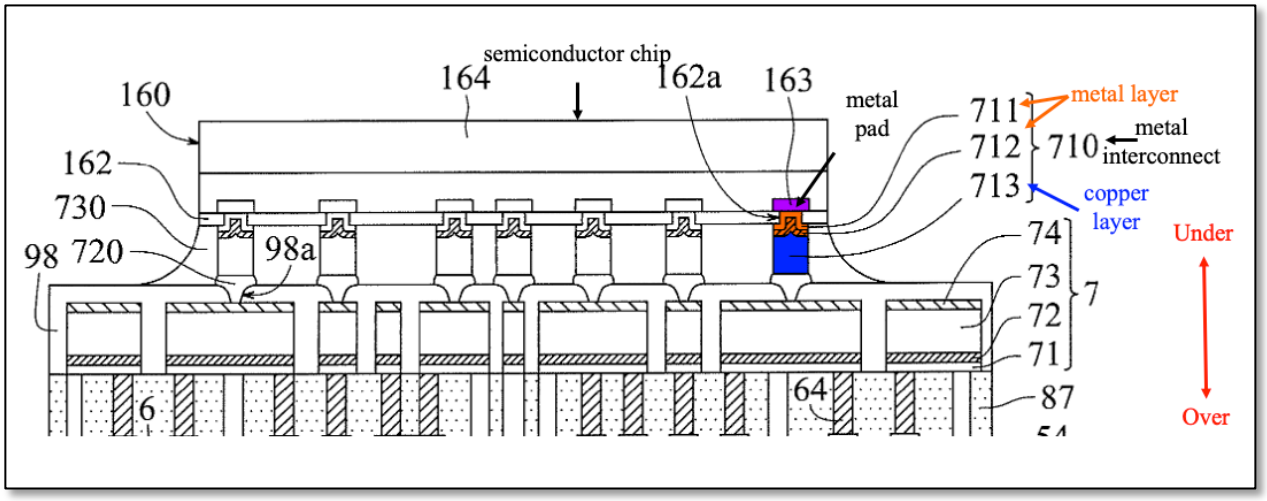
19. 1(e)(ii): "wherein said third metal interconnect comprises a third metal layer on said first metal pad and a third copper layer over said third metal layer, wherein said third copper layer has a thickness between 5 and 30 micrometers."

a) Lin-191's Teachings

167. Lin-191 teaches "metal pillars or bumps 710" on "metal traces or pads 163" of a semiconductor chip 160, that connect chip 160 to various other structures in Lin-191's multi-chip module thus functioning as a *metal interconnect*. *EX1005* at [0408]. Lin-191's metal pillars or bumps 710 comprise an "adhesion layer 711[,]" a "seed layer 712[,]" and a "metal layer 713[.]" *EX1005* at [0389]. Adhesion layer 711 is formed on a "contact point" of "the metal traces or pads 163[.]" *EX1005* at [0389]. Adhesion layer 711 is "nickel" or "titanium[.]" *EX1005* at [0390], [0394]. Seed layer 712 "can be a copper layer." *EX1005* at [0392]. Thus, the combination of layers 711 and 712 is a *second metal layer on* metal pad 163. That is, because layer 711 is formed on a "contact point" of "metal traces or pads 136" and because both of layers 711 and 712 are *metal*, the mapped combination of layers 711/712 is a *second metal layer on said first metal pad*. *EX1005* at [0389]. The "metal layer 713 can be a single layer of copper" having a thickness "between 2 and 30 micrometers." *EX1005* at [0396]. Lin-191 thus teaches or renders obvious a *third copper layer ha[ving] a thickness between 5 and 30 micrometers*.

168. I note that the '763 Patent does not ascribe any criticality to the range of 5 and 30 micrometers. That is, the '763 Patent does not provide the range of 5 and 30 micrometers and then further provide an explanation for why such range is needed, important, or advantageous. Indeed, the '763 Patent describes a variety of

ranges, including smaller (between 2 and 5 micrometers) and larger (between 10 and 50 micrometers), indicating to a POSITA that the thickness can vary widely and that the thickness is not otherwise critical. *See EX1001* at 14:17-29.



EX1005 at FIG. 72 (excerpt).

b) Motivation to Combine

169. A POSITA would have found it obvious and been motivated to modify Sundaram's *third metal interconnect* per Lin-191's metal pillar or bump 710 (including the thickness of copper layer 713), such that the bump has a *third metal layer* on Sundaram's *first metal pad* and a *third copper layer* having a *thickness between 5 and 30 micrometers over* the *third metal layer*. Thus, the combination yields Sundaram's *third metal interconnect* having *a third metal layer over said first metal pad and a third copper layer over said third metal layer*.

170. A POSITA would have recognized Lin-191's metal pillar or bump 710 would improve metallurgical bonding and enhance reliability by employing a layered structure. Specifically, it was known that multi-layer metal bumps would provide the benefit of "improvement of adhesion of the various overlying layers or the prevention of diffusion of materials between adjacent layers[,]" thereby improving metallurgical bonding. *EX1022* at 3:49-56. Indeed, it was known that "when a solder bump made of, for example, SnPb, SnAg, SnCu, SnAgCu, SnZn, SnZnBi, SnIn…Sn, which the solder bump is primarily made of, diffuses into the electrode pad and wiring made of Al or Cu," which may result "in electric problems in some cases." *EX1047* at [0003]. "To prevent the diffusion, a UBM [] that is highly effective in preventing solder diffusion is used between the electrode pad and the solder bump," i.e., reducing the risk of intermetallic formation. *EX1047* at [0004]. "As a typical example, of the UBM having the barrier capability, Ni…is often used." *EX1047* at [0004]. Therefore, a POSITA would have recognized that a UBM structure, such as Lin-191's metal pillar or bump 710, would improve the connection between Sundaram's *first metal pad* and *third metal interconnect* by preventing diffusion of solder material into the *first metal pad*.

171. Additionally, a POSITA would have understood that by employing Lin-191's layered structure the solder joint would have increased resistance to fatigue

and stress-induced failure because the copper seed layer would ensure a uniform plating of the thicker copper portion (layer 713) as electroplating copper without a seed layer may "lead to a void in the electroplated metal[,]" thereby compromising mechanical integrity. *EX1063* at 3:12-16. Additionally, a POSITA would have appreciated the advantages of copper use in interconnects and been motivated to include the *third copper layer ha[ving] a thickness between 5 and 30 micrometers* in the *third metal interconnect*. Specifically, copper was known to have "high immunity to electromigration, high ductility, and high melting point[,]" making it a desirable choice for interconnect material in high-density packaging. *EX1054* at 2:2-14.

172. Thus, the mechanical integrity of Sundaram's *third metal interconnect* would be improved by employing such a layered structure, thereby enhancing the reliability of the interconnects, particularly in applications subjected to repeated temperature fluctuations and mechanical stress. As such, the modification of Sundaram's *third metal interconnect*, per Lin-191's metal pillar or bump 710, would have been an obvious and advantageous modification to improve long-term solder ball performance.

173. Moreover, a POSITA would have appreciated that the thickness of Lin-191's *third copper layer* (i.e., between "2 and 30 micrometers" which teaches or

renders obvious *between 5 and 30 micrometers*) would allow for optimal underfill placement, as demonstrated by Lin-191. *EX1005* at FIG. 72. Specifically, as shown above in FIG. 72, Lin-191's metal pillars or bumps 710 are surrounded by "underfill 730[.]" *EX1005* at [0381]. A POSITA would recognize that Lin-191's thickness of layer 713 (*third metal layer*) allows for ample space for underfill 730 to be placed and would have found that desirable as limited space would prevent proper underfill filling. As shown in FIG. 3, Sundaram already teaches such an underfill between first electronic device 125 and interposer 105 such that applying Lin-191's third copper layer thickness would have allowed for Sundaram's underfill to be sufficiently deposited. Underfill integrity was an important feature as underfill materials were known to "redistribute the stress caused by CTE mismatch" by "allow[ing] [] stress to be more uniformly spread out over the entire surface of the chip, supporting substrate and solder balls." *EX1135* at 4:34-40. Accordingly, a POSITA would have appreciated that Lin-191's *third copper layer* thickness would achieve proper underfill filling, thereby decreasing CTE mismatch-induced stress to Sundaram's first electronic device 125, *third metal interconnect,* and RDL.

174. A POSITA would have found the modification obvious at least because it is nothing more than the application of a known technique (a layered bump structure) to improve similar structures (Sundaram's chip package, Lin-191's chip

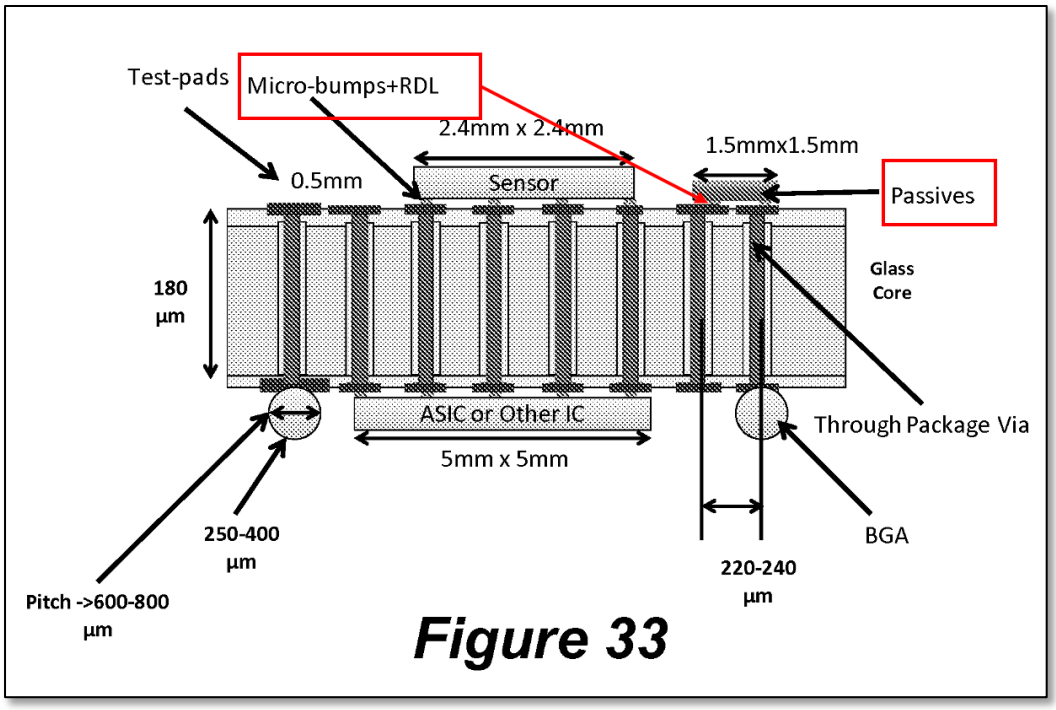
package) in a predictable manner. That is, Sundaram's *third metal interconnect* is improved in the same way as Lin-191's metal pillar or bump 710. Alternatively, a POSITA would have been motivated to substitute Lin-191's bump structure for Sundaram's *third metal interconnect* to obtain the above-described advantages of Lin-191's teachings.

175. A POSITA would have had a reasonable expectation of success in both applying Lin-191's teachings to Sundaram's *third metal interconnect* or substituting Lin-191's metal pillar or bump 710 for Sundaram's *third metal interconnect*. Indeed, Lin-191 and Sundaram are both directed to semiconductor package interconnect technology. Further, bump interconnects were well-known and formed using common manufacturing techniques, such as physical-vapor deposition, sputtering, and electroplating. *EX1005* at [0413], [0420]; *EX1042* at ("…filled with copper typically by an electroplating process, as known to one of ordinary skill in the art of integrated circuit fabrication."); *EX1043* at [0032] ("… a variety of different deposition methods known by one of ordinary skill in the art, including but not limited to, CVD, pulsed CVD, PECVD, ALD, PEALD, or sputtering methods."); ¶¶ 71-75. For example, Lin-191's methods of forming metal or pillar bump 710, such as electroplating, were well-known and well-established, further contributing to a reasonable expectation of success. *EX1005* at [0400].

B. *Claim 2: "The chip package of claim 1, further comprising a passive component over said first interconnection scheme and connected to said first interconnection scheme through a solder layer."*

1. Sundaram's Teachings

176. Sundaram teaches a *passive component* ("passives") connected to an interposer by "micro-bumps+RDL" thus teaching a *passive component* that is *connected to an interconnection scheme* (RDL) *through a solder layer* (micro-bumps). *EX1004* at FIG. 33.



EX1004 at FIG. 33, 6:29-22 .

177. Because Sundaram teaches connecting passives to an "RDL" via "micro-bumps," Sundaram thus teaches a *passive component* that is *connected to* an *interconnection scheme* (RDL) *through a solder layer* (micro-bumps). Sundaram's

"micro-bumps" are a *solder layer* at least because Sundaram teaches that "solder" is used for "electrically connect[ing] device" and because as I described above, solder bumps were known to be formed of *solder layer[s]*. *EX1004* at 6:29-32; *See* ¶¶ 71-75.

2. Motivation to Combine Sundaram's Embodiments

178. Based on the FIG. 33 embodiment, a POSITA would have found it obvious and been motivated to modify Sundaram's chip package to comprise a *passive component over* the *first interconnection scheme* and connected to a metal interconnect through a *solder layer*. In the combination, the *passive component* is positioned adjacent to FIG. 3's second electronic device 130, therefore *over* the *first interconnection scheme*.

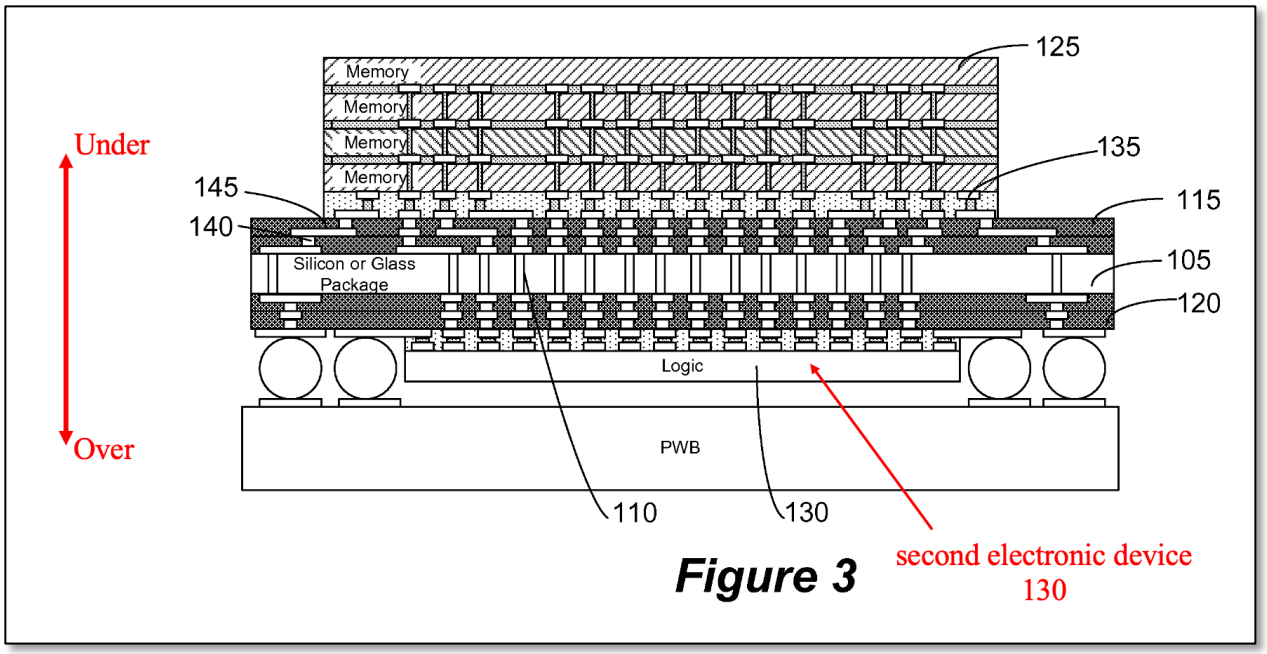


Figure 3

EX1004 at FIG. 3.

179. A POSITA would have appreciated that by connecting a passive component, e.g., a capacitor, over Sundaram's *first interconnection scheme*, Sundaram's chip package would advantageously mitigate signal desynchronization and preserve signal integrity.

180. Passive components, such as capacitors, were known to preserve signal integrity by filtering out noise from signal generated by chips. *See, e.g., EX1048* at [0001] ("Chips such as Application Specific Integrated Circuits [] often include power and ground connections to the circuit board. Capacitors, often referred to as 'bypass capacitors' or 'decoupling capacitors,' are usually coupled across the power and ground connections to filter out unwanted electrical noise that may be generated by the power supply. The bypass capacitors may be disposed on the bottom side of circuit board within the footprint of the ASIC.").

181. Indeed, "by use of bypass capacitors on multi-layer printed circuit boards, the total area of the current loop formed by the signal trace and its return current can be minimized. Signal integrity, which is influenced by factors such as impedance, inductive crosstalk to other signals, signal transmission line reflection, and balance, can be improved and noise can be well controlled." *EX1049* at 7:11-19. Additionally, capacitors were known to provide "less noisy power being supplied"

to chips in a chip package by "providing a low inductance path between power and ground[,]" thereby supporting a transmission line signal path that preserves signal integrity when interconnecting with the PWB (printed wiring board). *EX1050* at 5:37-41.

182. As such, a POSITA would appreciate both the improvement in signal integrity and reduction in power noise due to the low-inductance path provided by the *passive component*. Further, including a passive component, such as a capacitor, would reduce the impact of high frequency interference (HFI) on digital signals being transmitted between first electronic device 125 (*first semiconductor chip*) and the PWB as well as reduce the negative impact of HFI on power supply lines in Sundaram's chip package, thereby further preserving signal integrity. Specifically, "when events take place that have frequency higher than what can be accommodated by a voltage regulator, noise occurs." *EX1100* at [0004]. A capacitor "works as backup energy storage" that can "quickly provide the shortfall" if the voltage drops due to such high frequency events. *EX1100* at [0004].

183. The modification is the application of a known technique (implementing a passive component) to a known device (Sundaram's chip package) to yield the predictable result of Sundaram's chip package having a passive component over the *first interconnection scheme*. Further, a POSITA would have

had a reasonable expectation of success in including a *passive component* in Sundaram's chip package, because Sundaram already teaches a *passive component* and because soldering passive components into chip packages was a very well-known technique. *See, e.g., EX1051* at FIG. 14, [0093] ("…chip capacitor 213 are provided with a power electrode 214 to be connected to the power internal electrode layer and the power solder bump 217…and the ground solder bump 220."). Furthermore, the inclusion of passive components such as Sundaram's was a ubiquitous practice in chip packaging, thus making the modification simple, straightforward, and routine, thereby further evidencing the reasonable expectation of success. *See, e.g., EX1052* at FIG. 2, [0025] ("The flip-chip BGA package 4 further comprises an RC passive component 41 such as a resist or a capacitor…"); *EX1053* at [0030] ("In some embodiments, electronic components such as the component 180 can comprise passive components (e.g., resistors, capacitors, inductors)…").

C. *Claim 3: "The chip package of claim 1, wherein said first interconnection scheme comprise a fourth metal interconnect across over a sidewall of the first semiconductor chip."*

184. As I discussed above at claim 1(e)(i), Sundaram's *first interconnection scheme* comprises die pads 135 that "electrically connect devices" thus functioning as an *interconnect*. *See* ¶ 142. Sundaram additionally teaches "metallization provides

die pad surfaces 135" such that the die pads 135 are *metal*. *EX1004* at 6:22-24. FIG. 3 illustrates numerous die pad surfaces, with one of the many die pad surfaces being identified with reference numeral 135 in FIG. 3. *EX1004* at 6:22-33 (referencing die pads (plural)). However, a POSITA would have understood that FIG. 3 expressly teaches a die pad surface such as the orange-highlighted die pad in the below FIG. 3 at least because of the ubiquity of connecting bumps to pads and because Sundaram labels a similar structure as such. *See* ¶ 65. The die pad 135 shown in orange below is therefore a *fourth metal interconnect* that, like the trace 145 and via 140 making up the *first metal interconnect*, "electrically connect[s]" first and second devices 125, 130. *EX1004* at FIG. 3, 6:29-33; 6:62-67.

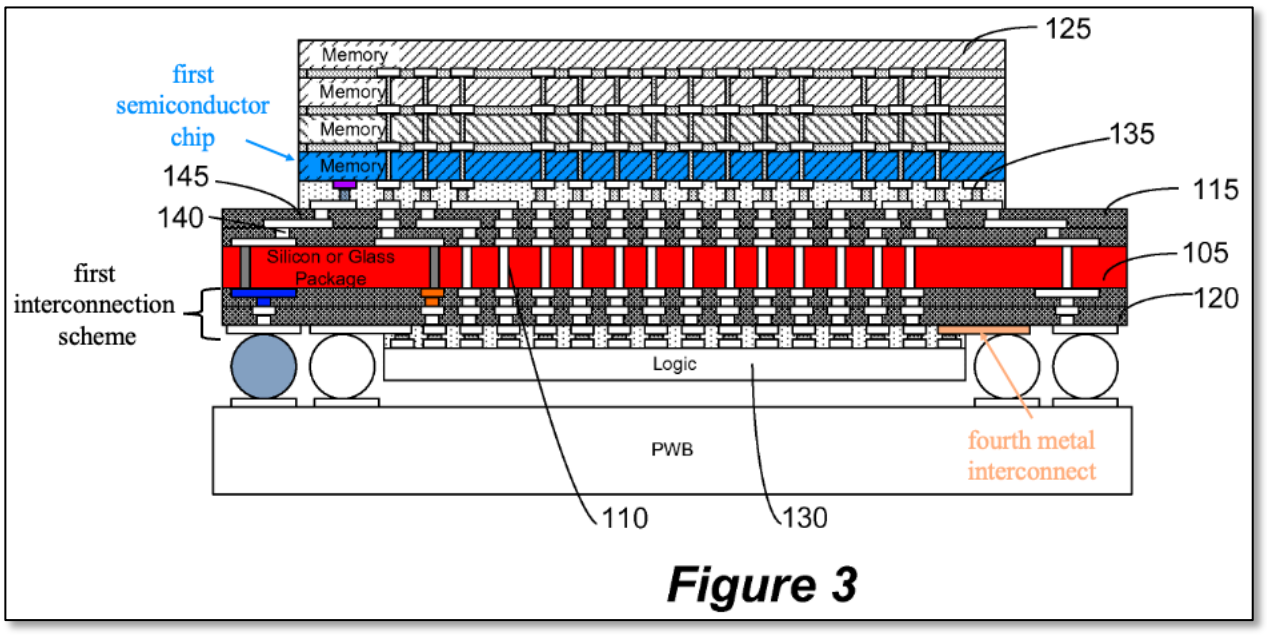
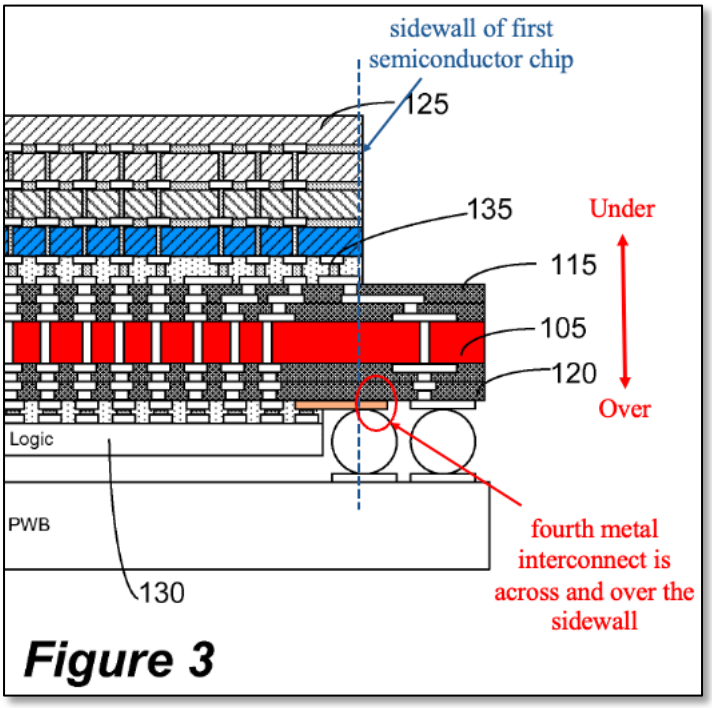


Figure 3

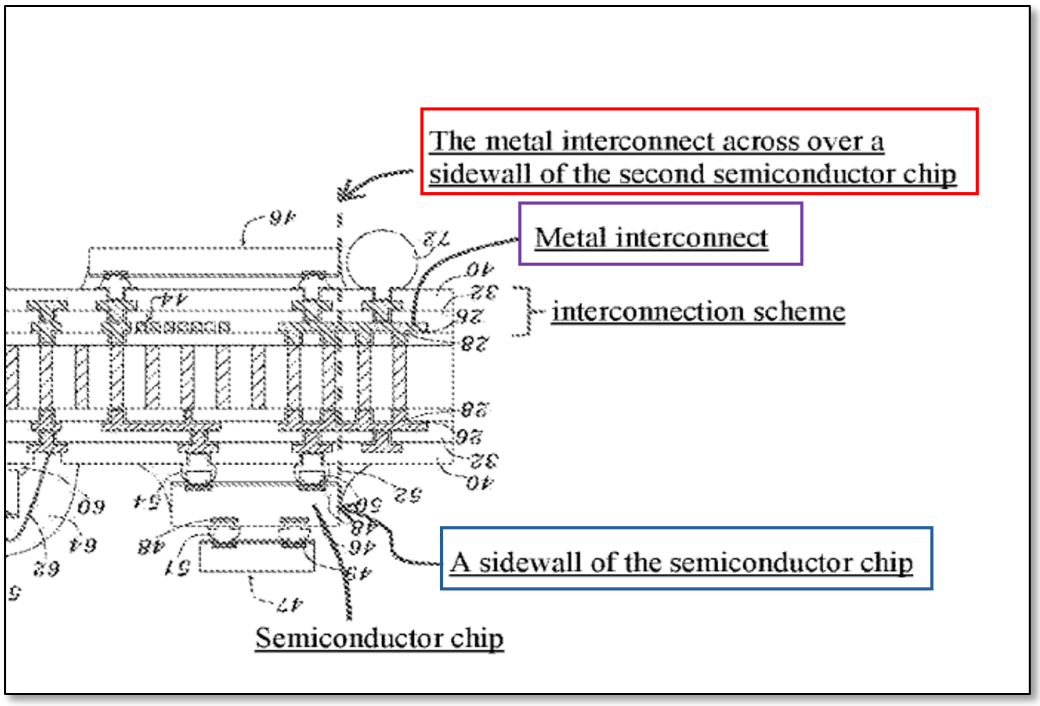
EX1004 at FIG. 3.

185. The annotated figure below illustrates that the *fourth metal interconnect* is both *across* and *over* a *sidewall* of first electronic device 125 (*first semiconductor chip*). The blue dashed line indicates the *sidewall* of first electronic device 125, namely a boundary thereof. Notably, the *fourth metal interconnect* is positioned in the "over" direction relative to the *sidewall*, as indicated by the red arrow depicting the over/under directions. Additionally, the *fourth metal interconnect* extends laterally (i.e., left/right) to the right past the boundary of the *sidewall*. As such, the *fourth metal interconnect* is both *across* and *over a sidewall of the first semiconductor chip*.



EX1004 at FIG. 3 (excerpt).

186. I note that Sundaram's teachings of the *fourth metal interconnect* being *across* and *over* the *sidewall of the first semiconductor chip* are consistent with an annotated figure that Patent Owner provided during prosecution of the related '768 Patent, arguing support for this limitation. In the figure below, I have shown how the Patent Owner's annotations mirror the above mapping of Sundaram's *fourth metal interconnect*.

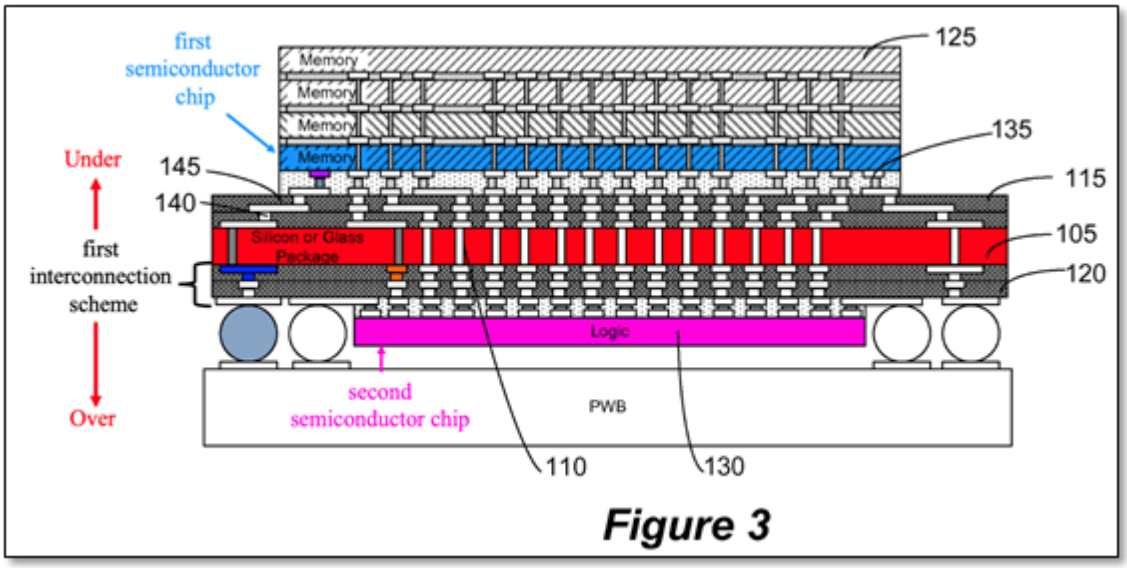


EX1032 at p. 537.

D. *Claim 4:*

1. 4(a): "The chip package of claim 1, further comprising a second semiconductor chip over said first interconnection scheme,"

187. Shown below, Sundaram teaches a second electronic device 130 which may be a "logic IC device or devices" and is "attached to the second side 120 of interposer 105" and is thus a *second semiconductor chip*. *EX1004* at 6:38-39. As shown, Sundaram's *second semiconductor chip* is *over said first interconnection scheme*.

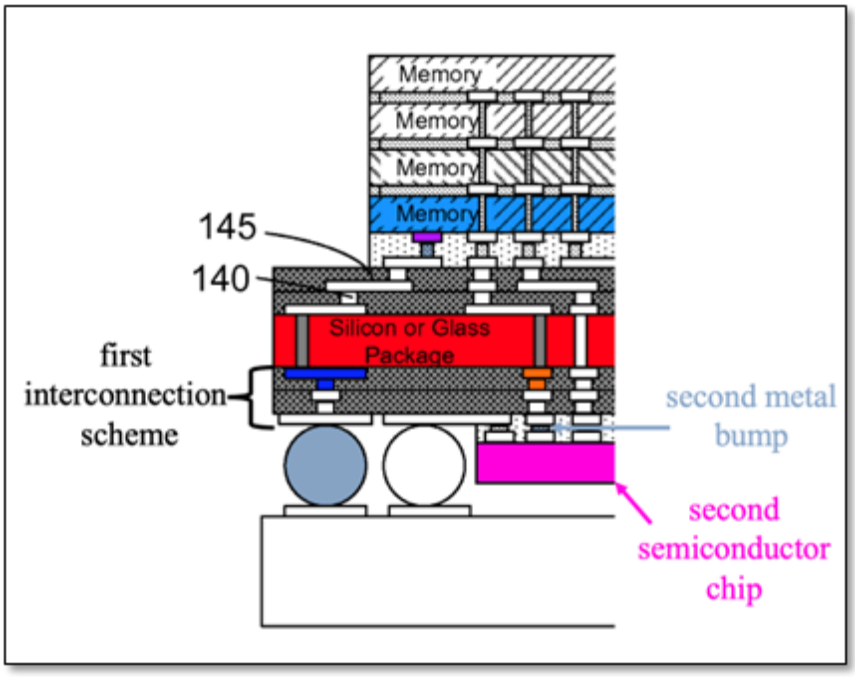


EX1004 at FIG. 3.

2. 4(b): "wherein said second semiconductor chip comprises a second metal bump between said second semiconductor chip and said first interconnection scheme."

188. Recall that Sundaram teaches "die pads 135…can electrically connect devices using solder, copper bumps with solder caps, copper to copper bonding." *EX1004* at 6:29-33. In FIG. 3, below, the *second semiconductor chip* is depicted as being connected to a bump on die pad 135. Because Sundaram teaches "copper

bumps with solder caps[,]" the bump on die pad 135 is a *second metal bump*. *EX1004* at 6:29-33. Further, Sundaram's *second metal bump* is shown as *between said second semiconductor chip and said first interconnection scheme*.



EX1004 at FIG. 3 (excerpt).

E. *Claim 5: "The chip package of claim 1, wherein said first semiconductor chip comprises a central-processing-unit (CPU) circuit block and a graphics-processing-unit (GPU) circuit block."*

a) Lin-191's Teachings

189. Lin-191 teaches semiconductor chips as "system-on chip[s] (SOC) including **a graphics-processing-unit (GPU) circuit block**, a wireless local area network (WLAN) circuit block **and a central-processing-unit (CPU) circuit block**…" *EX1005* at [0106], *see also* [0541], [0543].

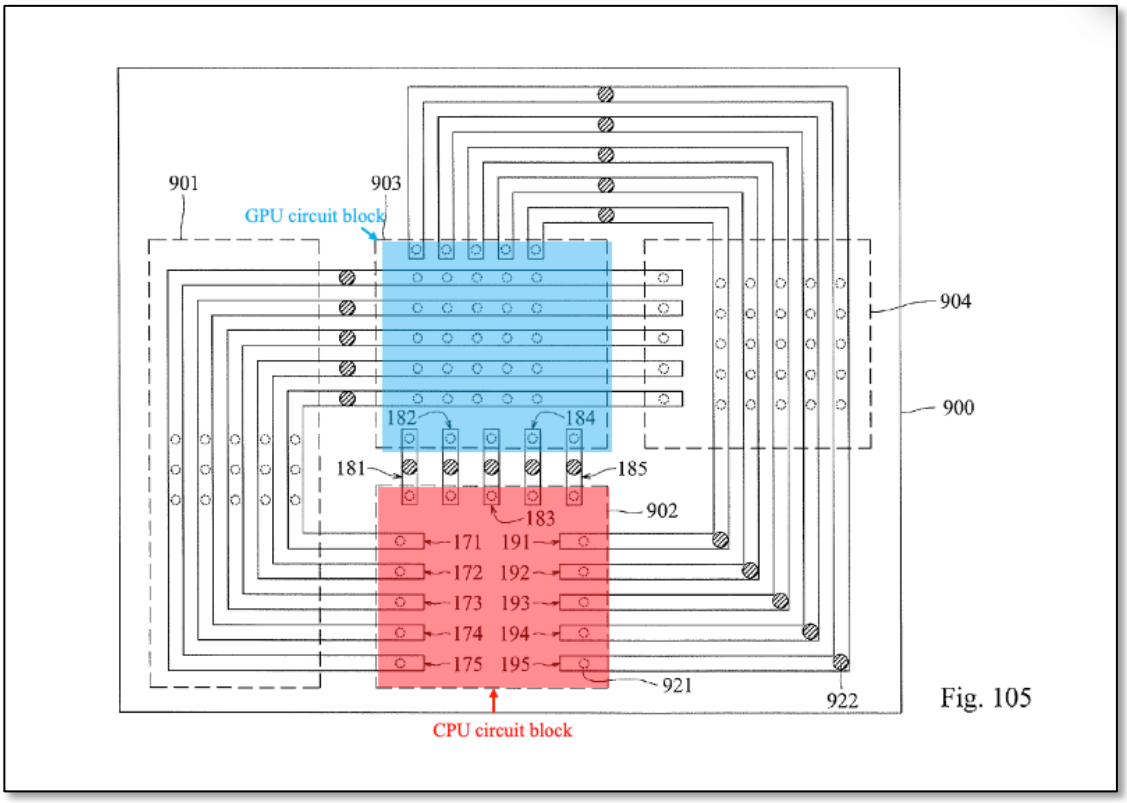


Fig. 105

EX1005 at FIG. 105, [0541], [0543] (describing FIG. 105).

b) Motivation to Combine

190. A POSITA would have found it obvious and been motivated to modify Sundaram's first electronic device 125 to comprise *a CPU circuit block and a GPU circuit block* based on the teachings of Lin-191. The modification would have predictably improved Sundaram first electronic device 125 by providing first electronic device 125 with the ability to perform the functions of both a GPU and a CPU. While Sundaram's FIG.3 depicts device 125 as stacked memory, Sundaram teaches "other electronic devices can also be used as the first electronic device 125."

EX1004 at 6:37-43. Thus, a POSITA would have considered the depicted memory stack to be merely exemplary and would have been motivated to modify first electronic device 125 to have a CPU and GPU circuit block for applications requiring such processing power. Sundaram teaches "smart and mobile phone applications, including video streaming, 3D graphics, camera-functions, and gaming are driving the demand for logic to memory bandwidth [] at increasing levels without an increase in power consumption," such that a POSITA would have found it obvious to modify Sundaram's chips package, per Lin-191's teachings, to carry out the requisite CPU/GPU tasks for such mobile phone applications. *EX1005* at 1:20-25. Further, Sundaram already contemplates "high power logic component[s]" on device 125's side of interposer 105:

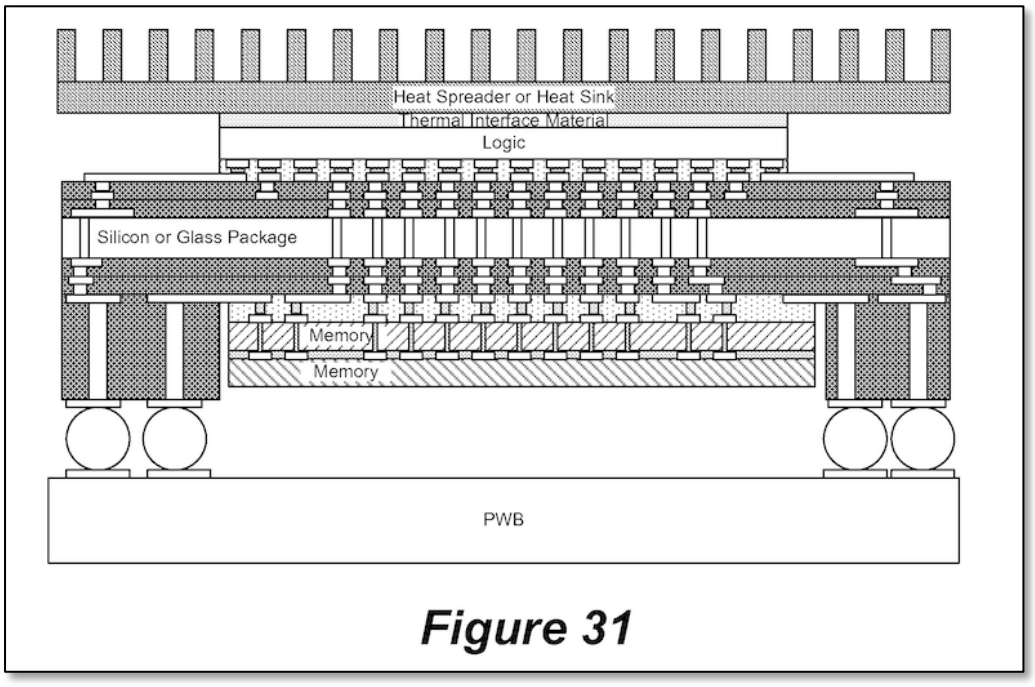


Figure 31

EX1004 at FIG. 31.

191. The Sundaram-Lin-191 combination is the application of a known technique (a semiconductor chip with a CPU circuit block and a GPU circuit block) to a known device (Sundaram's chip package including first electronic device 125) yielding the predictable results of Sundaram first electronic device 125 having both a CPU circuit block and a GPU circuit block. A POSITA would have been motivated to apply Lin-191's teachings based on the desired functionality of Sundaram's chip package, e.g., to obtain the benefits of having a CPU and a GPU on a single chip. As I described above, combined CPU/GPU architectures were known to provide the benefits such as the "opportunity to leverage both the high computational power from GPUs for regular applications and flexible execution from CPUs for irregular workloads" as well bypassing "costly CPU-GPU data transfers[.]" *EX1031* at p. 1-2.¶¶ 86-87. As such, a POSITA would have been motivated to achieve such benefits by implementing Sundaram's first electronic device 125 (*first semiconductor chip*) with *a central-processing-unit (CPU) circuit block and a graphics-processing-unit (GPU) circuit block.*

192. Because chips including both GPU and CPU circuit blocks were well known prior to the '763 Patent, there would have been a reasonable expectation of success. *See, e.g., EX1101* at [0022] ("In one embodiment, the APU 110 may include

a general purpose central processing unit (CPU) 130 and a graphics processing unit (GPU) 140 on a same semiconductor die."). Indeed, by the time of the '763 Patent, Indeed, by the time of the '763 Patent, AMD and Intel had both released chips having both GPU and CPU circuit blocks. *See* ¶¶ 86-87; *see also EX1102* at p. 1 ("The chip is Intel's first to integrate the graphics processing unit (GPU) on the processor itself.")

F. *Claim 6:*

1. 6(a): "The chip package of claim 1, further comprising a second semiconductor chip under said first semiconductor chip,"

193. As shown below, another chip in Sundaram's chip stack 125 is a *second semiconductor chip*. As such, Sundaram teaches a *second semiconductor chip under said first semiconductor chip*. Sundaram's "first electronic device 125 can be…stacked memory IC devices[,]" thus yielding the *second semiconductor chip under said first semiconductor chip*. *EX1004* at 6:37-39.

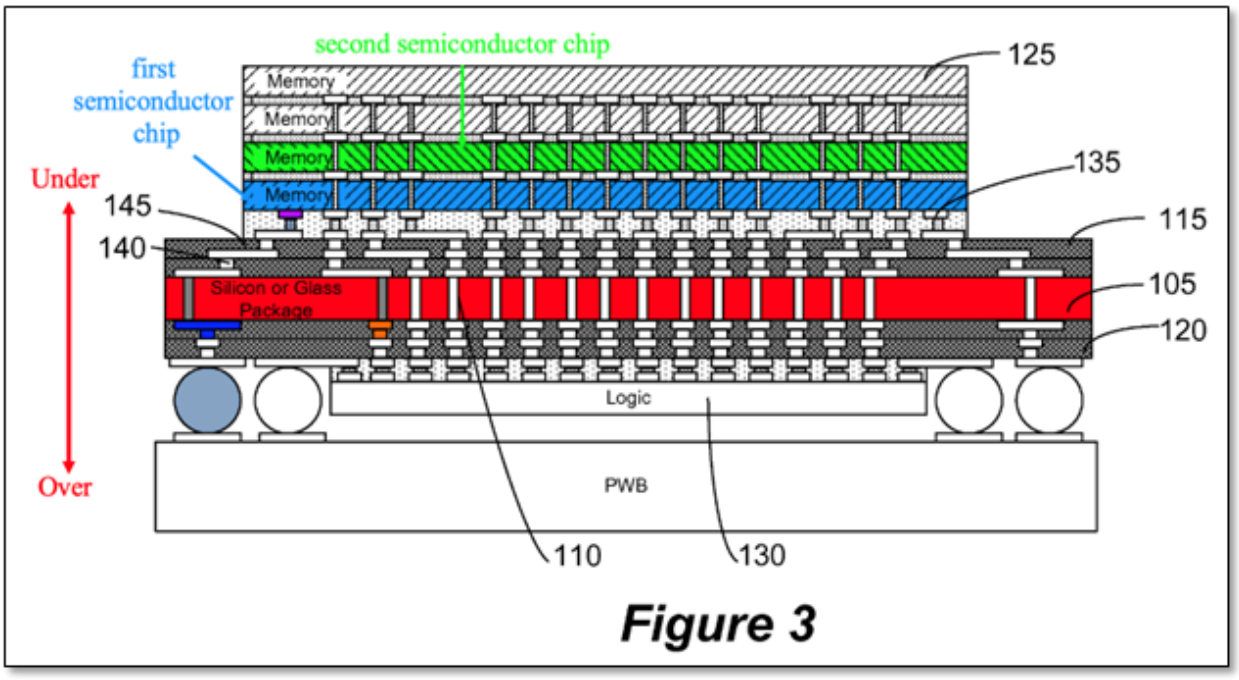


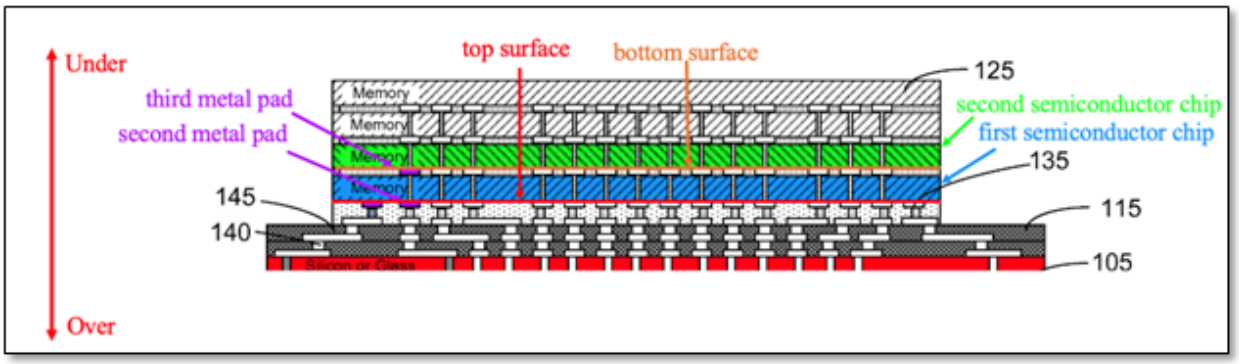
Figure 3

EX1004 at FIG. 3.

2. 6(b): "wherein said first semiconductor chip comprises a second metal pad on a top surface of said first semiconductor chip, a third metal pad on a bottom surface of said first semiconductor chip and"

194. Sundaram's first electronic device 125 (*first semiconductor chip*) has *pad[s]* on the top and bottom surfaces. Specifically, as shown below, FIG. 3 expressly depicts first electronic device 125 having a *second…pad* and a *third…pad*. A POSITA would have found it obvious that Sundaram's *second…pad* and a *third…pad* are *metal pad[s]* because virtually every chip has a metal pad for forming electrical connections and metal pads were ubiquitous. *See, e.g., EX1065* at [0005] ("Refer[ring] to FIG. 1 for a **conventional** electronic component, which includes a chip 1 and a substrate 3. The chip 1 has a plurality of **metal pads** 2."); *EX1095* at

1:24-25. ("I/O terminals were **traditionally** formed by way of **metal pads** along the periphery of an IC."). *See also* ¶ 165. A *metal pad* on the *top surface* is a *second metal pad* and a *metal pad* on the *bottom surface* is a *third metal pad*, respectively, as shown below in FIG. 3.



EX1004 at FIG. 3.

195. Alternatively or additionally, FIG. 32 depicts a chip stack similar to FIG. 3's where each chip has a distinct metal pad. A POSITA would have found it obvious, been motivated, and had a reasonable expectation of success in modifying FIG. 3's chip stack per FIG. 32's to provide each chip with its own set of pads so that each chip has top and bottom pads connected to one another as each chip must include pads on its surface to provide connection to other electrical components in the chip package. The modification is a straightforward implementation detail to FIG. 3's chip stack.

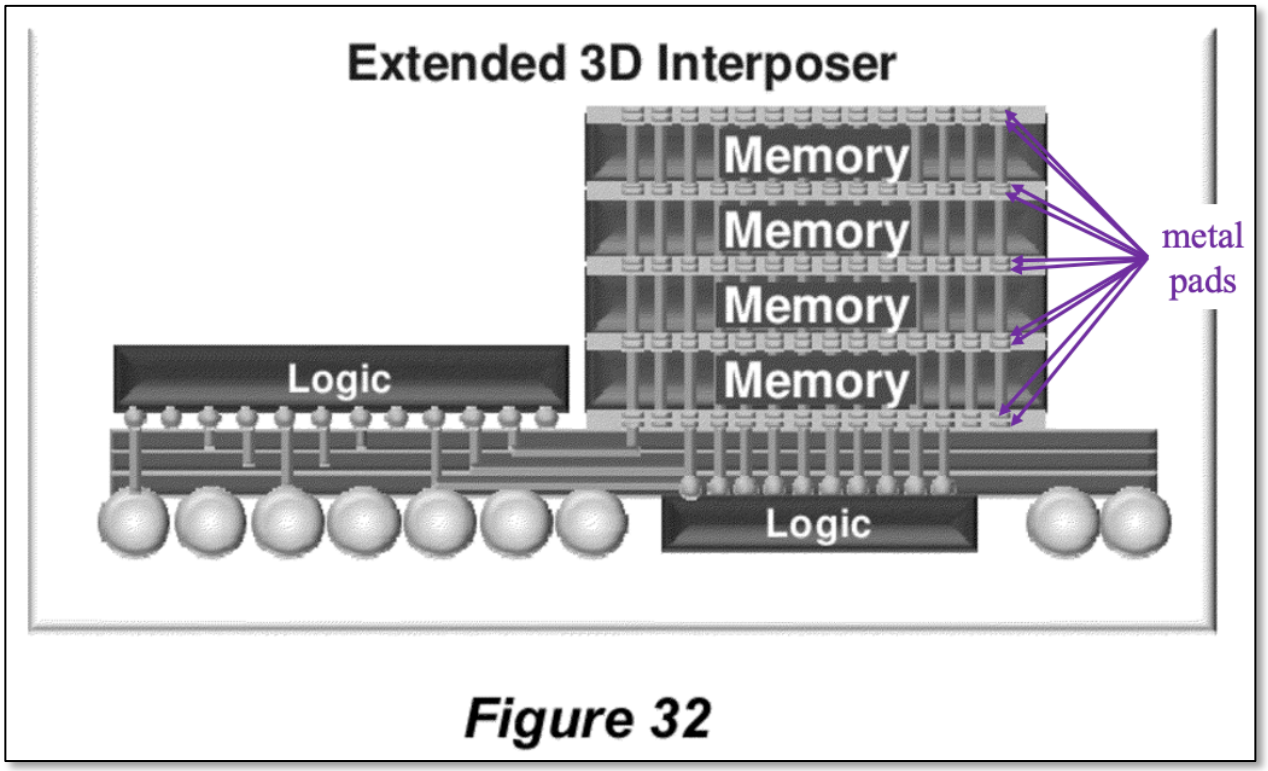


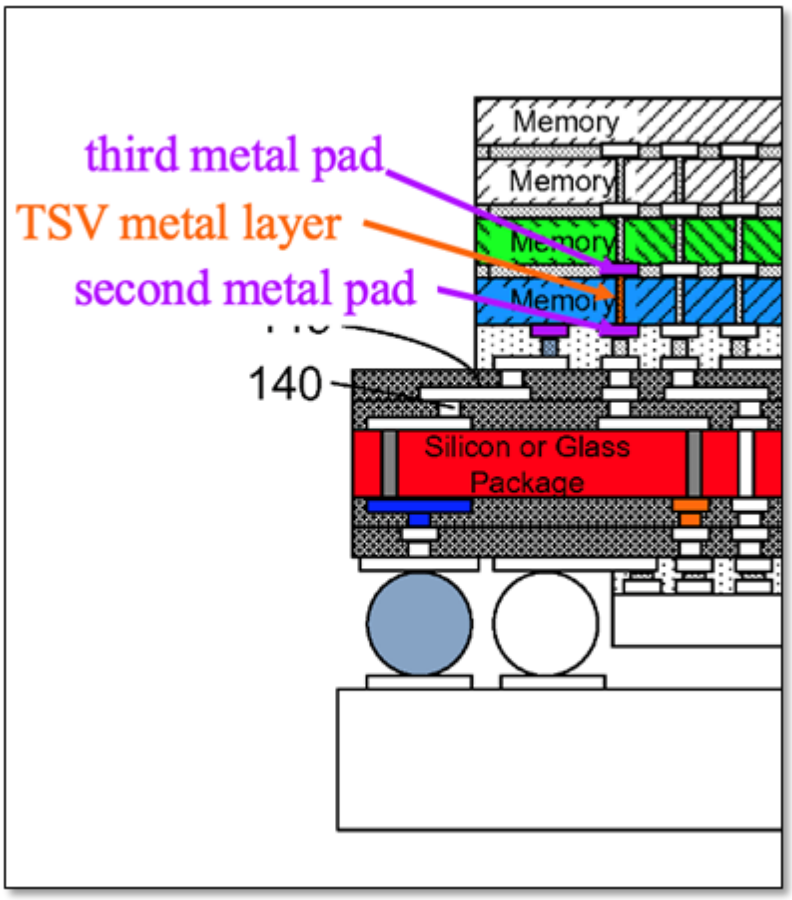
Figure 32

EX1004 at FIG. 32.

3. 6(c): "a through-silicon-via metal layer connects to said second metal pad,"

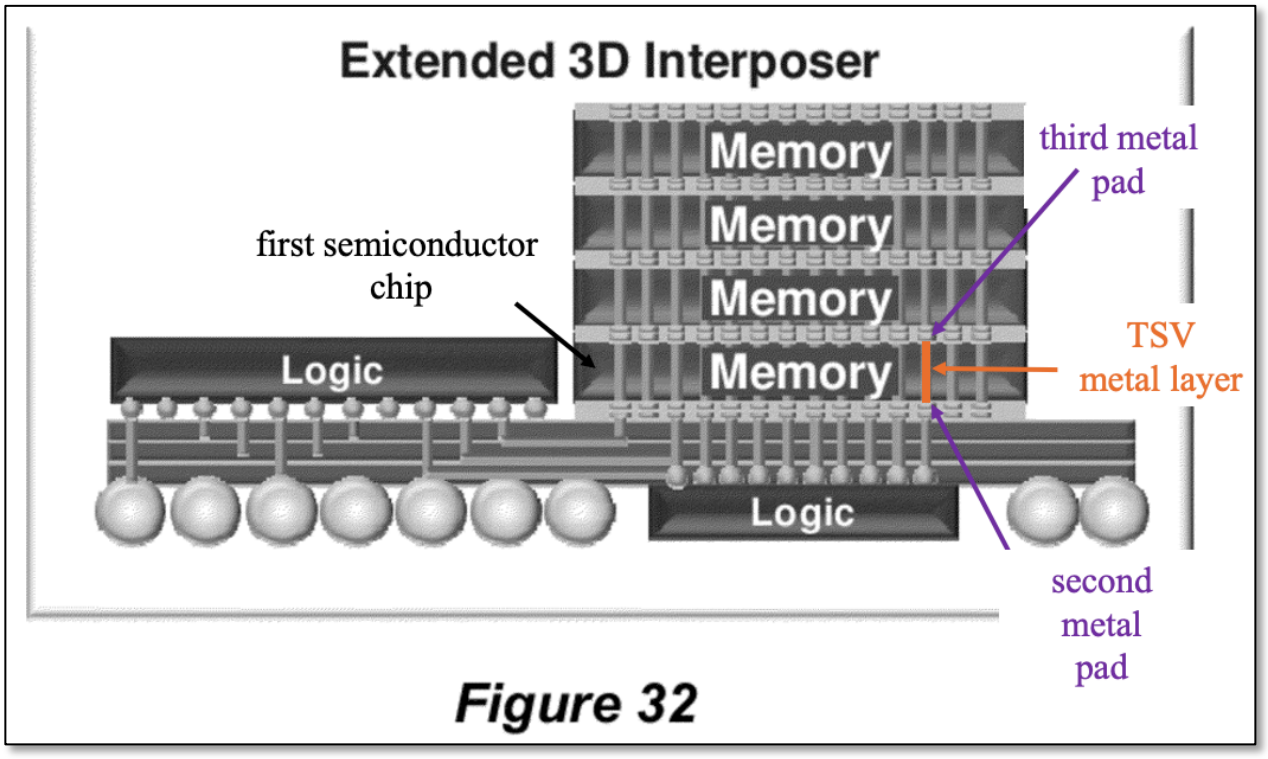
196. As shown, Sundaram's *first semiconductor chip* comprises an interconnect (orange) connecting pads on the top and bottom surfaces of each memory chip, which a POSITA would have understood as being a *through-silicon-via metal layer* that connects the *third metal pad* to the *second metal pad*. A POSITA would have understood Sundaram's orange interconnect to be a *TSV metal layer* because as I described above, TSVs were known to be "vertical connections 'etched through the silicon wafer and filled with metal." *EX1066* at [0017]. Sundaram was

familiar with TSV metal layers connecting metal pads, referring to the logic chip structure in FIG. 1d as having "TSVs[.]" *EX1004*, 1:39-42, 1:62-67. Accordingly, a POSITA would have understood the similar structure shown in device 125 of FIG. 3 to also be a TSV.



EX1004 at FIG. 3 (excerpt).

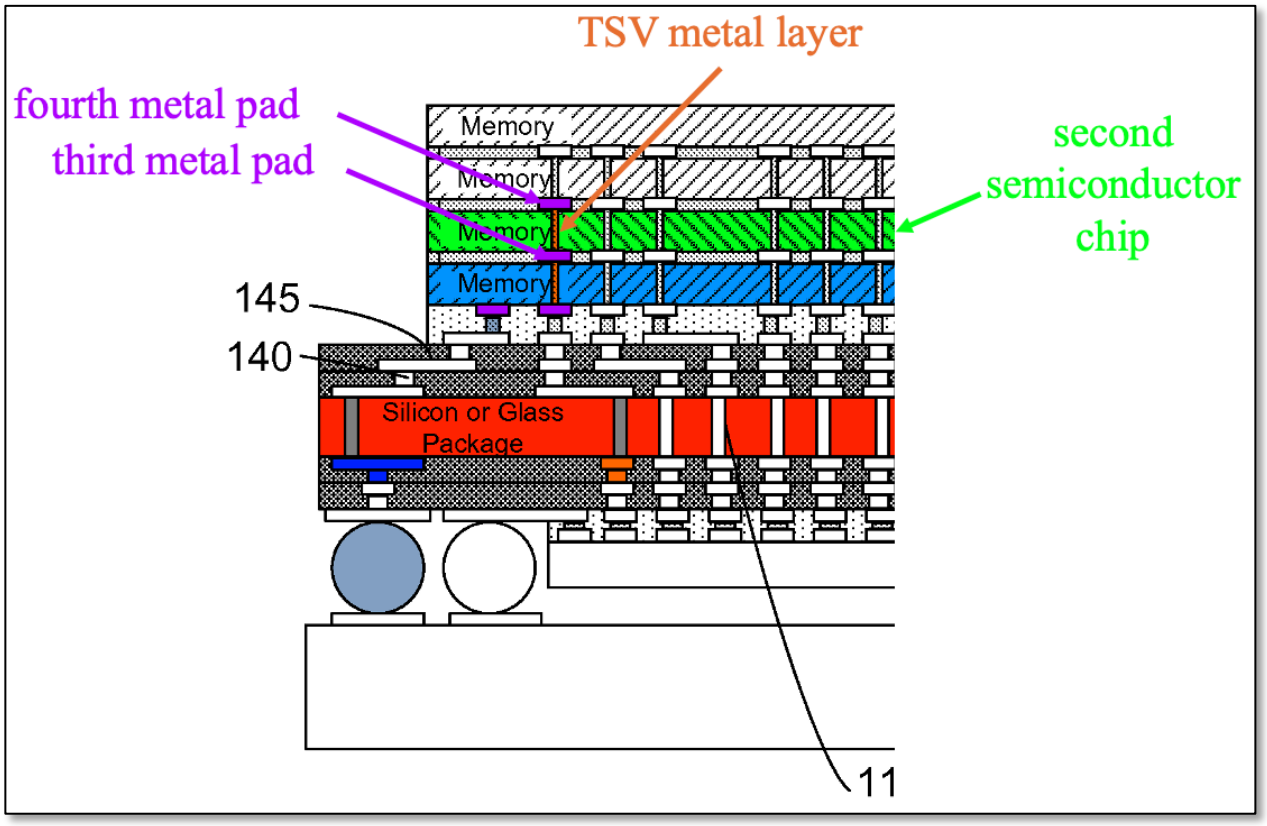
197. Sundaram's FIG. 32 similarly depicts a TSV metal layer connecting metal pads:



EX1004 at FIG. 32.

4. 6(d): "wherein said third metal pad is connected to a fourth metal pad of said second semiconductor chip."

198. As shown below, Sundaram's *third metal pad is connected to a fourth metal pad of said second semiconductor chip* through another TSV metal layer.



EX1004 at FIG. 3 (excerpt).

199. As shown, Sundaram at FIG. 32 also teaches a third metal pad of a first chip connected to a fourth metal pad of a second semiconductor chip.

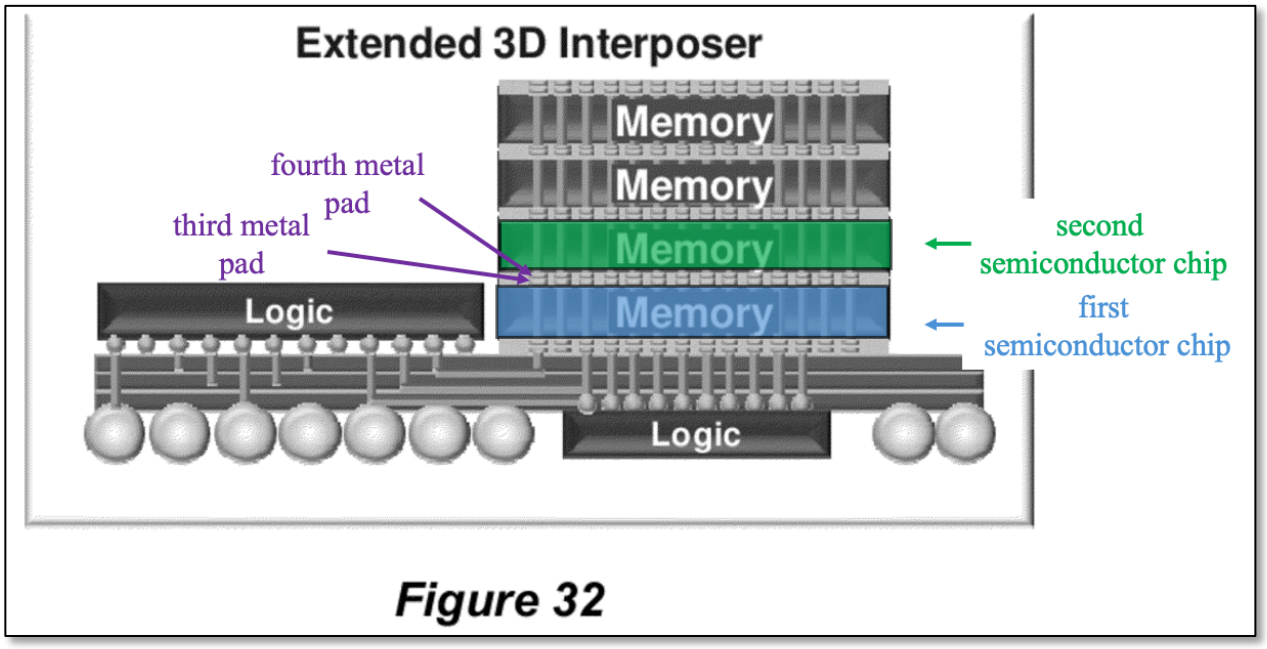


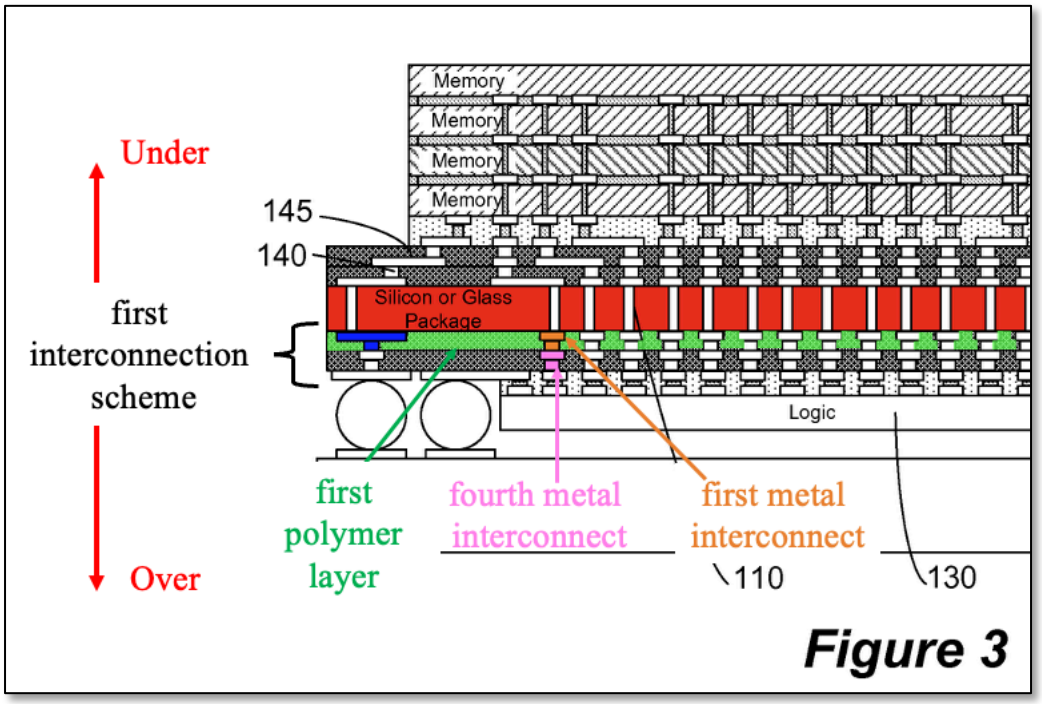
Figure 32

EX1004, FIG. 32.

G. *Claim 7:*

1. 7(a): "The chip package of claim 1, wherein said first interconnection scheme further comprises a fourth metal interconnect over said first metal interconnect and said first polymer layer,"

200. Sundaram's *first interconnection scheme* comprises a *fourth metal interconnect*, namely a blind via 140 and conductor trace 145 that are *over* the via 140 and trace 145 forming the *first metal interconnect* and *said first polymer layer*, as shown below. The blind via 140 and conductor trace 145 are a *metal interconnect* for the same reasons described above. *See* ¶¶ 144-145.



EX1004 at FIG. 3 (excerpt); ¶ 145.

201. Alternatively, Sundaram's die pad 135 is a *fourth metal interconnect* over said *first metal interconnect* and said *first polymer layer*:

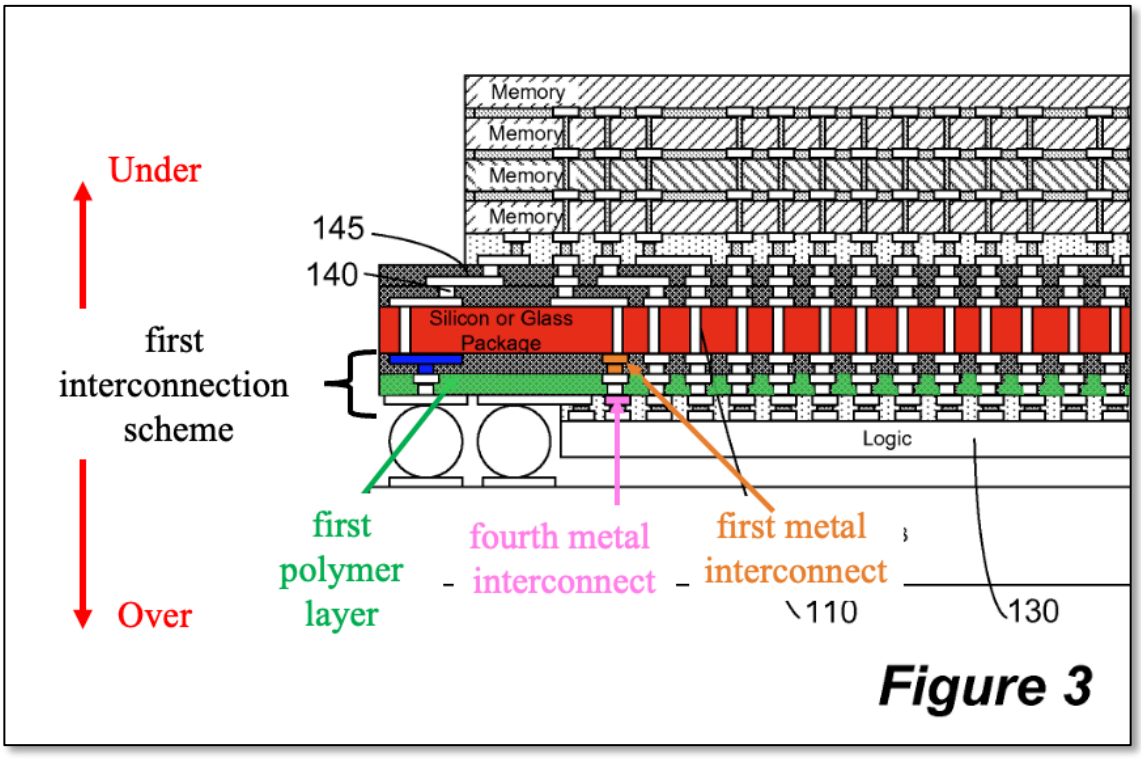


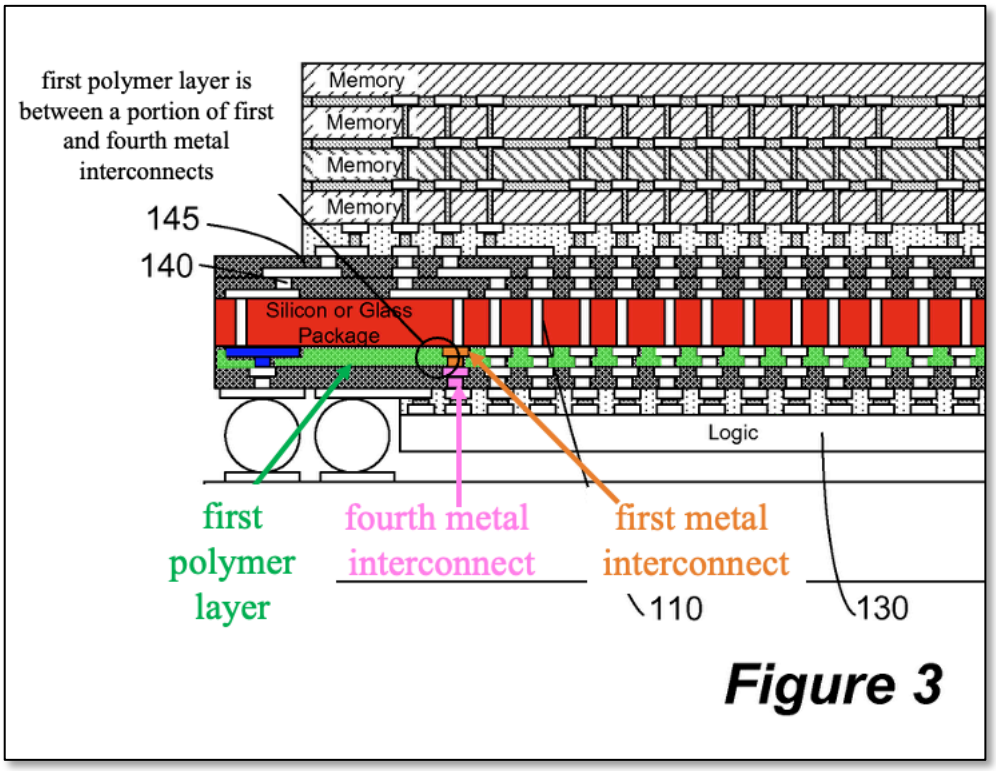
Figure 3

EX1004 at FIG. 3 (excerpt); ¶ 146.

2. 7(b): "wherein said first polymer[2] is between said first and fourth metal interconnects,"

202. Under either mapping of the *fourth metal interconnect* and the *first polymer layer,* Sundaram's *first polymer layer* is *between said first and fourth metal interconnects*, as shown:

[2] I have been instructed to interpret Claim 7(b)'s *first polymer* as referring to the *first polymer layer* introduced in Claim 1(c)(i).



EX1004 at FIG. 3 (excerpt); ¶ 145.

203. Alternatively, the *first polymer layer is between said first and fourth metal interconnects*, as shown:

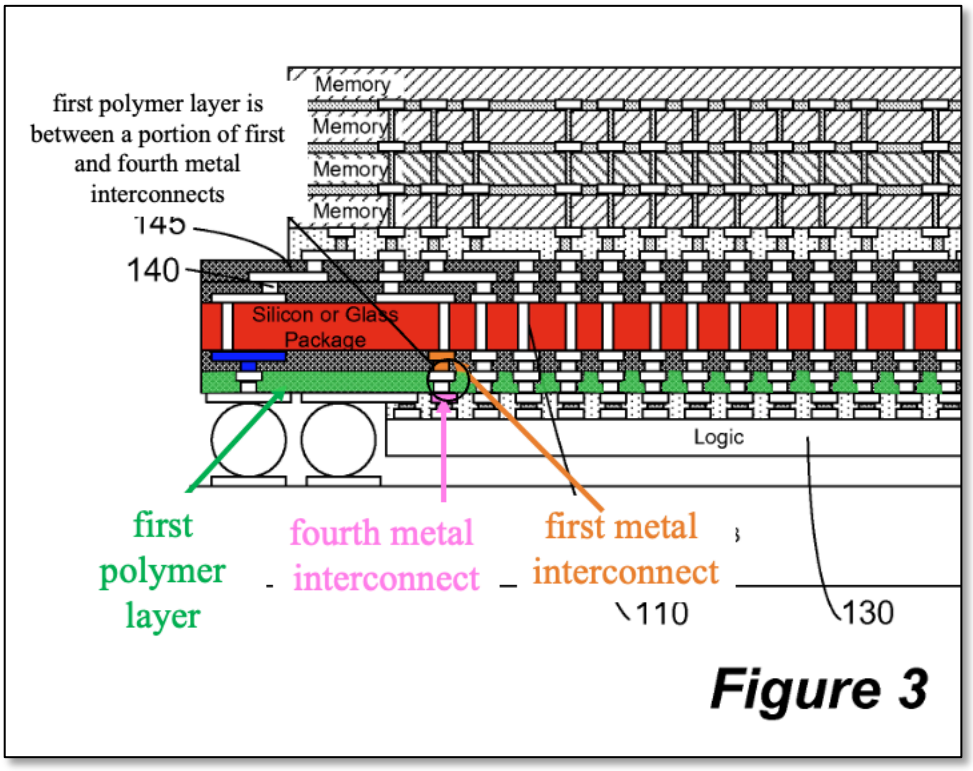


Figure 3

EX1004 at FIG. 3 (excerpt) ; ¶ 146.

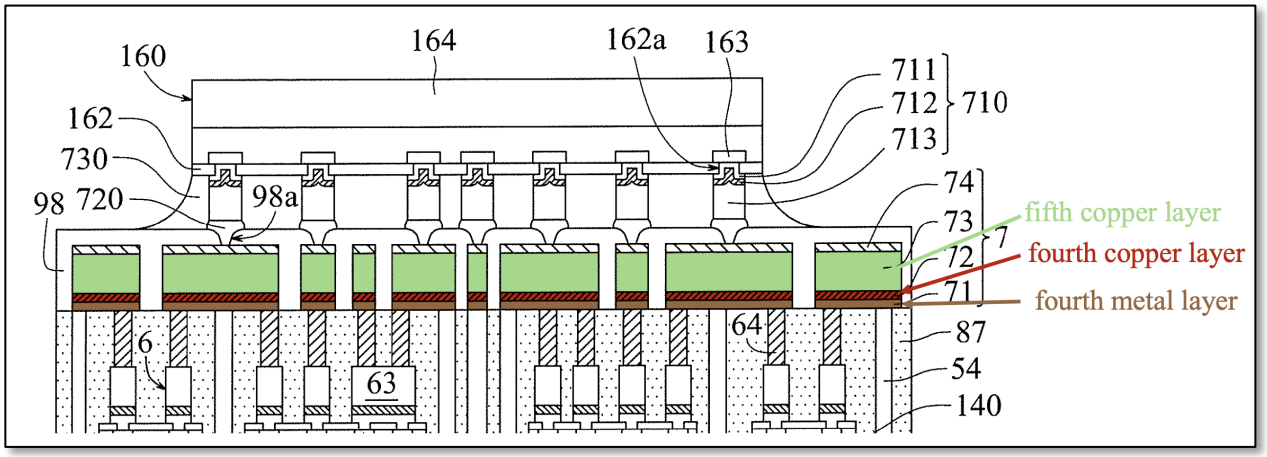
3. 7(c): "wherein said fourth metal interconnect comprises a fourth metal layer, a fourth copper layer on said fourth metal layer, and a fifth copper layer on said fourth copper layer."

204. *See* ¶¶ 148-149, mapping Sundaram's multi-layer interconnect teachings. Sundaram's copper seed layer is a *fourth copper layer* and Sundaram's copper layer formed by SAP is a *fifth copper layer*.

a) Lin-191's Teachings

205. Additionally, Lin-191 teaches a multilayered metal interconnect with two copper layers and a metal layer. Specifically, Lin-191 teaches a "patterned metal layer 7" having an "adhesion layer 71, the seed layer 72, the metal layer 73, and the

barrier/wetting layer 74" *EX1005* at [0379]. Layer 7 interconnects metal pillars or bumps 64 to various other structures, such "metal pillars or bumps 54" in Lin-191's package and is therefore, like Sundaram's trace 145 and vias 140, a *metal interconnect*. *EX1005* at [0379]. Adhesion layer 71 is a *metal* (e.g., titanium or nickel) and is thus a *fourth metal layer*. *EX1005* at [0260]-[0264]. Seed layer 72 is "a copper layer" on adhesion layer 71 and is thus a *fourth copper layer on said fourth metal layer*. *EX1005* at [0261]-[0264]. Metal layer 73 "can be… a copper layer…on the seed layer 72" and is thus a *fifth copper layer on said fourth copper layer*. *EX1005* at [0420].



EX1005 at FIG. 72 (excerpt).

b) Motivation to Combine

206. A POSITA would have found it obvious and been motivated to modify Sundaram's *fourth metal interconnect* per Lin-191's teachings of patterned metal

layer 7, thus yielding the *fourth metal interconnect compris[ing] a fourth metal layer, a fourth copper layer on said fourth metal layer, and a fifth copper layer on said fourth copper layer*.

207. As shown below in FIG. 37, Lin-191 depicts a "schematic top perspective view of the patterned metal layer 7[.]" As shown, the patterned metal layers 7 makes lateral electrical connections (e.g., from bumps 54 (green) to bumps 64 (blue)). Several representative examples of such lateral electrical connections are annotated below. As such a POSITA would have understood layer 7 as being an RDL. Additionally, because the top view of layer 7 depicts the lateral connections achieved by patterned metal layers 7, Lin-191 thereby demonstrates the applicability to Sundaram's conductor traces 145 and blind vias 140 which likewise make lateral electrical connections (e.g., between pads in the chips to through vias 110), thus motivating the combination. *EX1004* at FIG. 3.

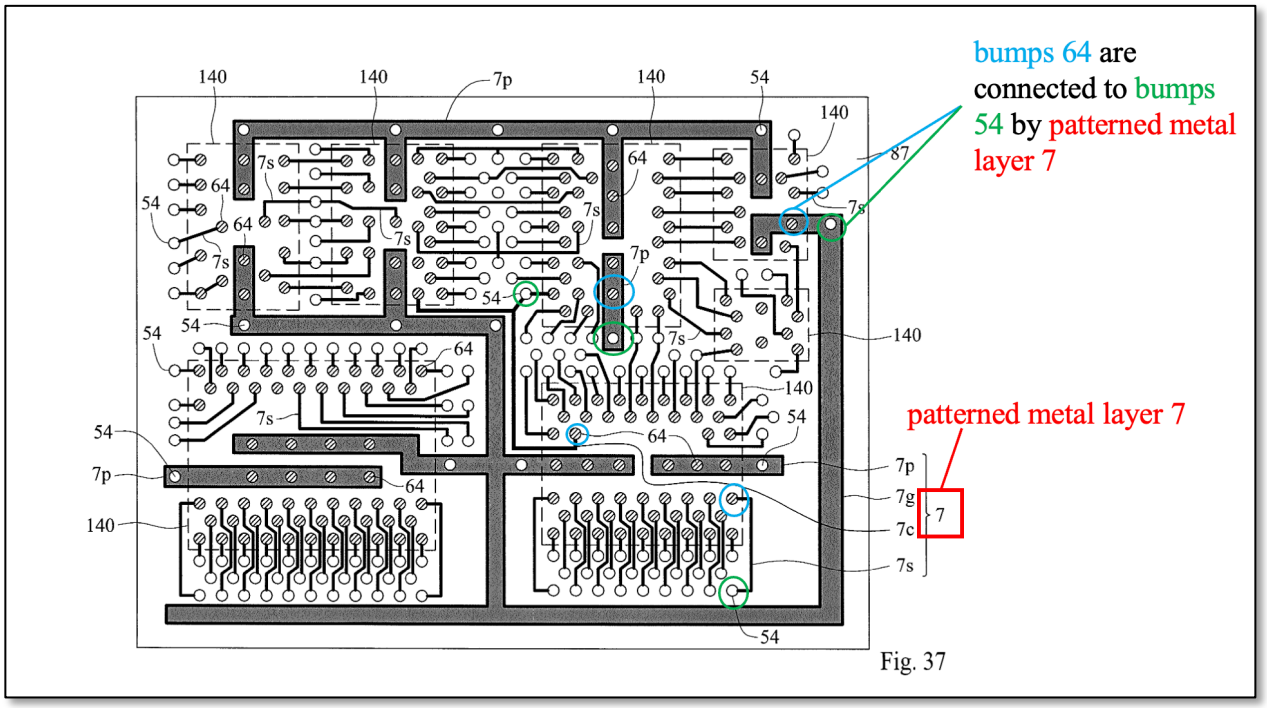


Fig. 37

EX1005 at FIG. 37.

208. The modification would have predictably improved Sundaram's chip package by providing a low resistance current path for signals traveling between the *first metal interconnect* and the *fourth metal interconnect*. Copper was known for its relatively low electrical resistivity and electromigration resistance. For example, it was known that "as the size and cross-sectional dimensions of electrical interconnects get smaller, resistance increases and electromigration increases. Increased resistance and electromigration are undesirable for a number of reasons. For example, increased resistance may reduce device drive current, and source/drain current through the device, and may also adversely affect the overall speed and

operation of the transistor." *EX1054* at 1:39-46. Copper has a lower resistivity (1.73 x 10^{-6} ohm-cm at 20°C) compared to other materials, such as aluminum (2.824 x 10^{-6} ohm-cm at 20°C), as well as a "high immunity to electromigration, high ductility, and high melting point[,]" making it a desirable choice for interconnect material in high-density packaging. *EX1054* at 2:2-14.

209. Indeed, because copper has relatively low electromigration rate, the risk of failures at elevated current densities is reduced. Specifically, it was known that "high current densities lead to electromigration-caused failures" in integrated circuits. *EX1055* at 1:30-32. Accordingly, a POSITA would have been motivated to choose a material, such as copper due to its lower resistivity, to reduce the risk of "electromigration-caused failures." *EX1055* at 1:30-32. Similarly, because the resistivity of copper is relatively low, the electrical conductivity is relatively high compared to other materials (e.g., aluminum). *EX1056* at [0152] ("In addition, since the electrical conductivity of copper is higher than that of aluminum…"). It was known that in "fabricating semiconductor components, interconnects having a high electrical conductivity…provide the best performance for a signal transmission system." *EX1057* at 1:29-33.

210. Additionally, the modification would have predictably improved Sundaram's chip package by reducing the risk of delamination between the copper

interconnect and the metal layers it interconnects and mitigating diffusion of copper into the metal layers it interconnects, which may negatively impact electrical reliability and ruggedness of the chip package. Specifically, the risk of delamination is reduced because the diffusion of copper out of the interconnects is mitigated by the nickel layers 71 and 74, thereby preventing physical damage to the copper interconnects that leads to delamination. Indeed, the diffusion of copper into adjacent copper layers is reduced by adhesion layer 71and barrier/wetting layer 74, which are both made of a "single layer of nickel[.]" *EX1005* at [0264], [0375]. As discussed, nickel was known to prevent copper diffusion into adjacent structures. *EX1040* at Abstract ("The structure comprises a layer of barrier metal, preferably nickel, that resists copper diffusion.").

211. The modification is application of a known technique (Lin-191's multi-layer interconnect) to a known device (Sundaram's *fourth metal interconnect*) ready for improvement to yield the predictable result of Sundaram's *fourth metal interconnect* comprising the layers of Lin-191's layer 7. Further, a POSITA would have had a reasonable expectation of success because Lin-191's layer 7 and Sundaram's *fourth metal interconnect* perform the same function (interconnecting components in a chip package) and because layer 7 is formed using well-known techniques familiar to a POSITA, such as electroplating and sputtering. *EX1005* at

[0414]-[0420]; *see, e.g., EX1042* at ("…filled with copper typically by an electroplating process, as known to one of ordinary skill in the art of integrated circuit fabrication."); *., EX1043* at [0032] ("The metal-containing wetting film 104 may be deposited by a variety of different deposition methods known by one of ordinary skill in the art, including but not limited to, CVD, pulsed CVD, PECVD, ALD, PEALD, or sputtering methods."). Additionally, the use of multi-layer interconnects, as demonstrated by both Lin-191 and Sundaram, among other prior art references, was commonplace, further leading to a reasonable expectation of success. *EX1005* at FIG. 84; *EX1004* at FIG. 3; *see also EX1058* at FIGS. 5-6, 8:32-40.

H. *Claim 8: "The chip package of claim 1, further comprising a second interconnection scheme under said solid layer and on said second surface."*

212. Sundaram teaches "polymer-metal redistribution layers" are "deposited **on the first side 115** and second side 120 of the interposer 105." *EX1004* at 6:62-67. Die pads 135 are also formed on the first side 115 (*second surface*). Thus, for the same reasons discussed above at claim 1(c) for the *first interconnection scheme*, Sundaram further teaches a *second interconnection scheme*. *See* ¶ 142. The RDL and die pads 135 on first side 115 is *a second interconnection scheme under said solid layer and on said second surface* because the traces 145 and vias 140 in the RDL

"connect" the "electronic devices" 125 and 130 and because die pads 135 "electrically connect devices[]." *EX1004* at 6:62-67, 6:29-31.

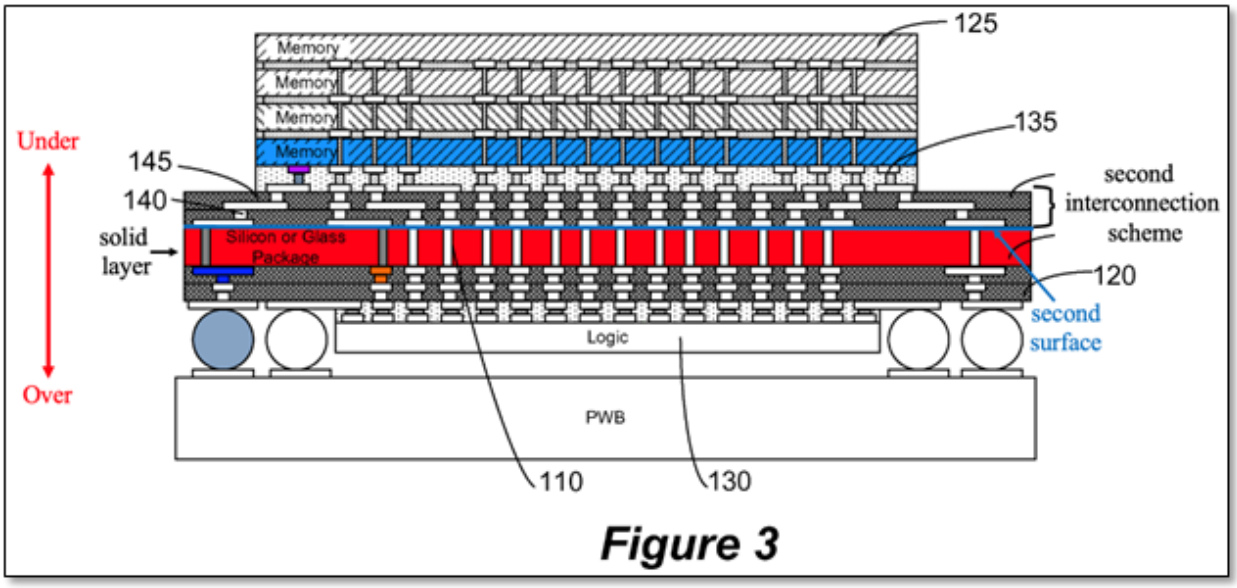


Figure 3

EX1004 at FIG. 3.

I. *Claim 9: "The chip package of claim 1, wherein said first metal pad is an aluminum pad"*

213. Sundaram alone or Sundaram-Lin-191 teaches a *first metal pad*. *See* ¶¶ 162-166. Lin-191, likewise, teaches metal pads 163 that "include **aluminum**." *EX1005* at [0384].

214. Metal pads are used for interconnecting chips to other components, where metal is used for the connection because it provides low resistance. Lin-191 teaches specifically a metal pad that is aluminum such that a POSITA would have found it obvious and been motivated to apply Lin-191's *aluminum pad* teachings to

Sundaram's *first metal pad*. A POSITA would have found it obvious and been motivated specifically to implement Sundaram's *first metal pad* as an *aluminum pad*. at least because aluminum was a well-known, cost effective, and widely used material for forming contact pads in chips, because it is compatible with established bond wire attachment methods, is consistent with legacy materials used in semiconductor processing, and because methods of forming such aluminum pads were well known. *See, e.g., EX1059* at 3:65–4:2 ("Aluminum is the metal of choice for…bond pad metal in IC devices because of its superior electrical and thermal conductivity, low cost, wire-bondability, and other performance and reliability factors."); *EX1061* at [0012] ("Materials that are commonly used for bond pads include…aluminum[.]"), [0013] ("The conventional processing sequence that is used to create an aluminum bond pad starts with a semiconductor surface…. A layer of Intra Metal Dielectric (IMD) is deposited over the surface, a layer of metal, typically aluminum, is deposited over the surface of the layer of IMD. The layer of metal is patterned and etched typically using a layer of photoresist and conventional methods of photolithography and etching."). The modification is the combination of prior art elements (aluminum pads, chip packages) according to known methods to yield predictable results i.e., Sundaram's *first metal pad* being made of aluminum. Because aluminum was such a well-known material and because methods of forming

aluminum pads were well-known, a POSITA would have had a reasonable expectation of success.

J. ***Claim 10: "The chip package of claim 1, wherein said solid layer further comprises a third region opposite to said second region, wherein said third region is between said first region and another edge of said solid layer, wherein said plurality of copper plugs in said plurality of through vias in said third region respectively."***

215. Sundaram teaches interposer 105 (*solid layer*) comprises a *third region*[3], shown below, which is on the *opposite* side of the *first region* than the *second region* and is, therefore, *opposite to said second* region. The *third region* is *between said first region* (green) *and another edge* (pink line on right-hand side) *of said solid layer*. Additionally, the *third region* comprises *copper plugs* in *through vias* (through vias 110), as shown. *EX1004* at 6:6-9 ("A plurality of ultra-small through vias 110 can be defined within the interposer 105…").

[3] The *third region* is not described in the '763 Patent's specification but was introduced by Applicant during original prosecution. *EX1002* at 351-360. Applicant relied solely on FIG. 6l to support the *third region*.

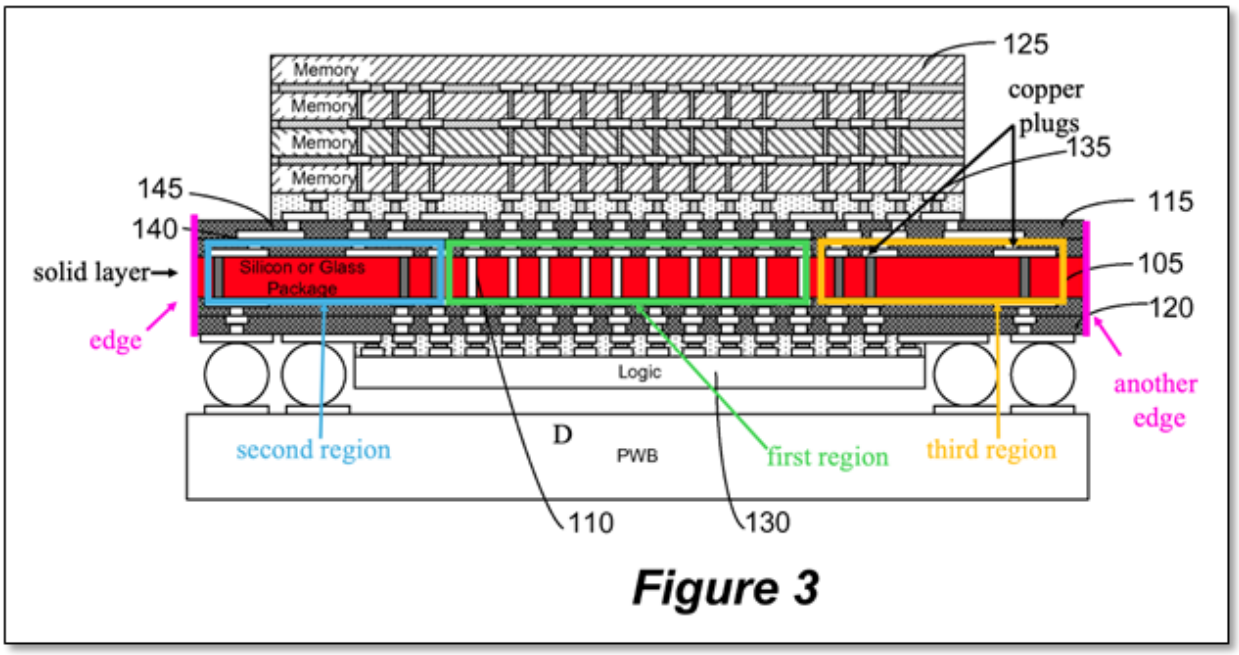


Figure 3

EX1004 at FIG. 3.

K. *Claim 11: "The chip package of claim 1, wherein said first copper plug has a thickness between 100 and 300 micrometers."*

216. Sundaram teaches or renders obvious *wherein said first copper plug has a thickness between 100 and 300 micrometers*. As discussed, Sundaram's interposer 105 has a *thickness between 100 and 300 micrometers*. *See* Claim 1(a)(iii), ¶ 133. Sundaram further teaches "through vias 110 can be defined within the interposer 105 such that each of the through vias 110 extends from the first side 115 to the second side 120[.]" *EX1004* at 6:6-9. Because through vias 110 extend from the *first surface* and *second surface* of interposer 105 (*solid layer*), through vias 110 (*first copper plug*) have a thickness equal to that of the *solid layer* i.e., "20 to about

200 micrometers" which teaches or renders obvious *between 100 and 300 micrometers*. *EX1004* at 2:24-28, FIG. 3.

217. In my opinion, the '763 Patent does not ascribe any criticality the claimed plug thickness of *between 100 and 300 micrometers*. I first note that the Applicant during examination of the related '768 Patent stated that the plug thickness is the same as substrate 20's thickness. *See EX1032* at 535-537. I also note my discussion at ¶ 135 that the '763 Patent does not ascribe any criticality to the claimed substrate thickness. Therefore, because (i) the Applicant stated that the plug thickness was the same as the substrate thickness, and (ii) the '763 Patent does not indicate the substrate thickness is critical, then it is my opinion the plug thickness recited in Claim 11 similarly is not critical.

L. *Claim 12: "The chip package of claim 1, wherein said plurality of copper plugs comprise a third copper plug vertically in one of said plurality of through vias in said solid layer, wherein a pitch between said first and third copper plugs is between 200 and 1000 micrometers."*

218. Shown below, Sundaram teaches that the *plurality of copper plugs comprise a third copper plug vertically in one of said plurality of through vias in said solid layer*, namely a third of through vias 110. The third through via 110 is a *third copper plug* for the same reasons discussed above. *See* ¶ 137.

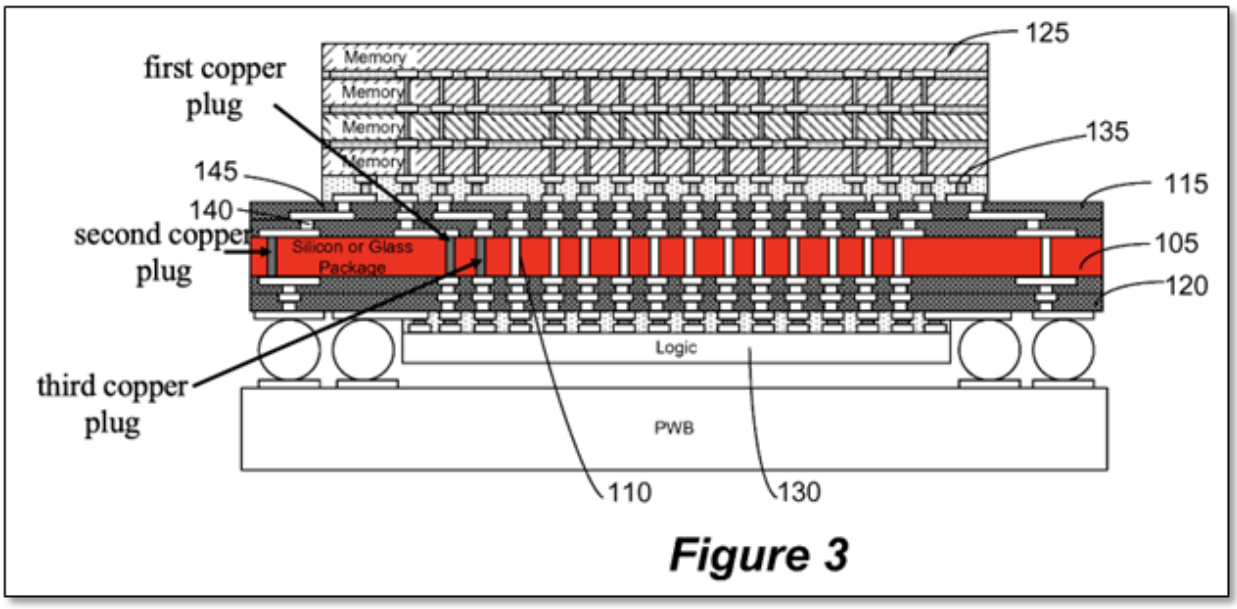
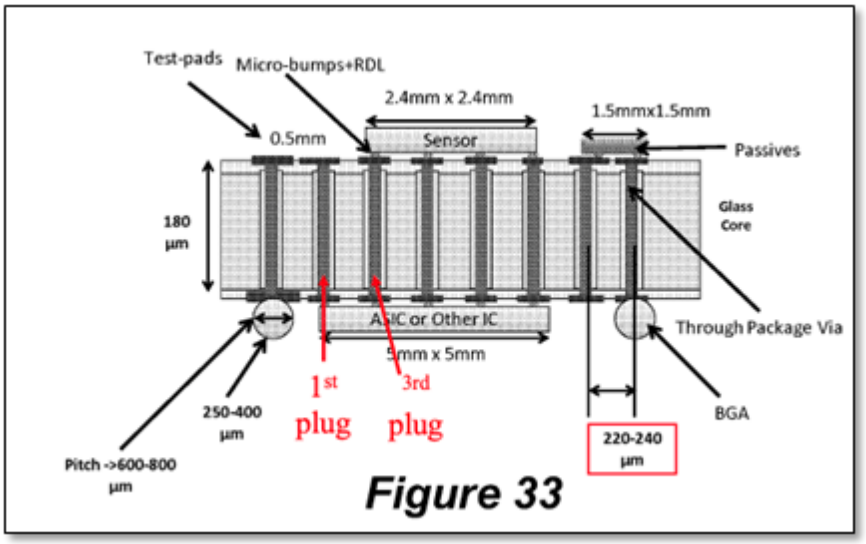


Figure 3

EX1004 at FIG. 3.

219. With respect to FIG. 33, Sundaram teaches through vias having a pitch "220-240 μm.]" *EX1004* at FIG. 33. As shown, like interposer 105 in FIG. 3, the interposer of FIG. 33 similarly comprises *first* and *third plug[s]* that are adjacent to each other. Because the *pitch* between the *first* and *third plug[s]* is "220-240 μm," Sundaram teaches or renders obvious the claimed range of *between 200 and 1000 micrometers*. *EX1004* at FIG. 33.

220. FIG. 33 is a specific example of a chip package for "a digital camera for cell phones" with a "through-via interconnect density" that is "substantially the same" as "the first electronic device 125 or the second electronic device 130 it connects." *EX1004* at 6:42-50.



EX1004 at FIG. 33.

221. In my opinion, the '763 Patent does not ascribe any criticality the claimed pitch of between 200 and 1000 micrometers. That is, the '763 Patent does not provide the range of 200-1000 micrometers and then further provide an explanation for why such range is needed, important, or advantageous. Indeed, the '763 Patent describes a variety of ranges, including smaller (between 5 and 20 micrometers) and larger (between 500 and 10,000 micrometers), indicating to a POSITA that the thickness can vary widely and that the thickness is not otherwise critical. See *EX1001* at 6:11-18.

a) Motivation to Combine

222. To the extent PO argues Sundaram's FIGS. 3 and 33 are separate embodiments, a POSITA would have found it obvious and been motivated to modify

the pitch of Sundaram's through vias 110 (*plurality of copper plugs*) according to the FIG. 33 embodiment such that a *pitch between said first and third copper plugs is between 200 and 1000 micrometers*. The modification is expressly motivated by Sundaram because FIG. 33 enables high bandwidth speeds such as "at least about 10 GB/s" between "an image sensor chip" and an "Asic chip" in a "digital camera for cell phones." *EX1004* at 6:42-45. As acknowledged by Sundaram, a POSITA would have recognized that there was a need "for logic to memory bandwidth (BW) at increasing levels without an increase in power consumption." *EX1004* at 1:22-24. Thus, a POSITA would have been motivated to implement a *pitch between said first and third copper plugs* of *between 200 and 1000 micrometer* to achieve such "high bandwidth speeds." *EX1004* at 6:42-45. The combination is the application of a known technique (Sundaram's copper plugs having a pitch between *200 and 1000 micrometers*) to a known device (Sundaram's chip package) ready for improvement to yield predictable results. A POSITA would have a reasonable expectation of success at least because the modification would have been simple and straightforward as methods of controlling pitch of copper plugs were well-known and because such a structure was already taught by Sundaram. *EX1004* at FIG. 33.

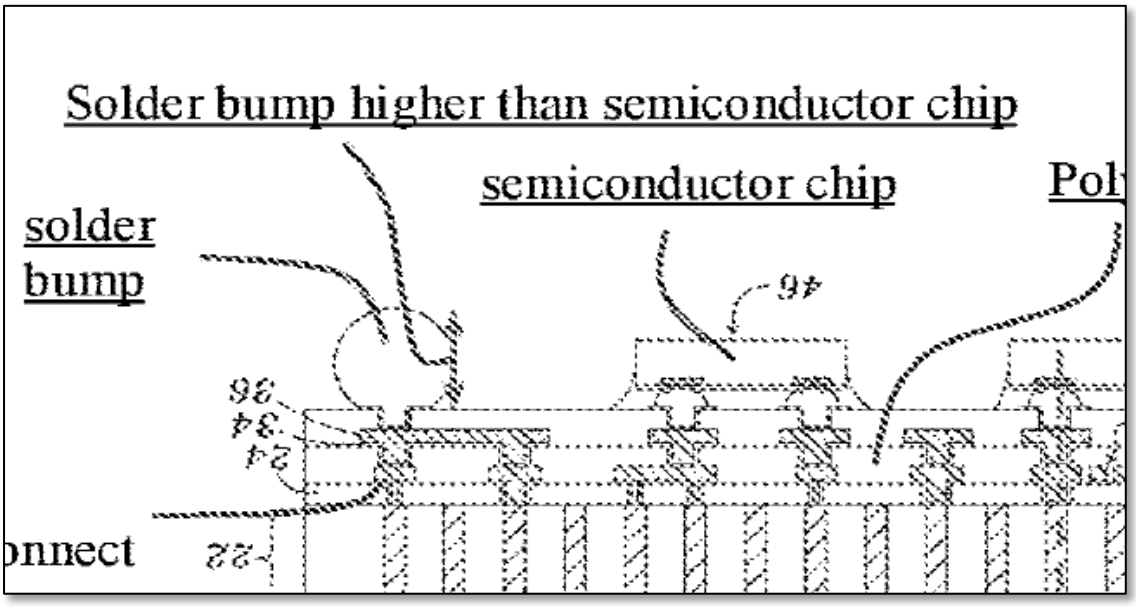
M. ***Claim 14:***

1. 14(a): "The chip package of claim 1, further comprising a second semiconductor chip over said first interconnection scheme and connected to said first interconnection scheme through a second metal bump,"

223. *See* Claim 4(a)-(b), ¶¶ 187-188, incorporated herein. The *second metal bump* discussed at Claim 4(b) connects the *second semiconductor chip* to the *first interconnection scheme* because Sundaram teaches "die pads 135…can **electrically connect** devices using solder, **copper bumps** with solder caps, copper to copper bonding." *EX1004* at 6:29-33.

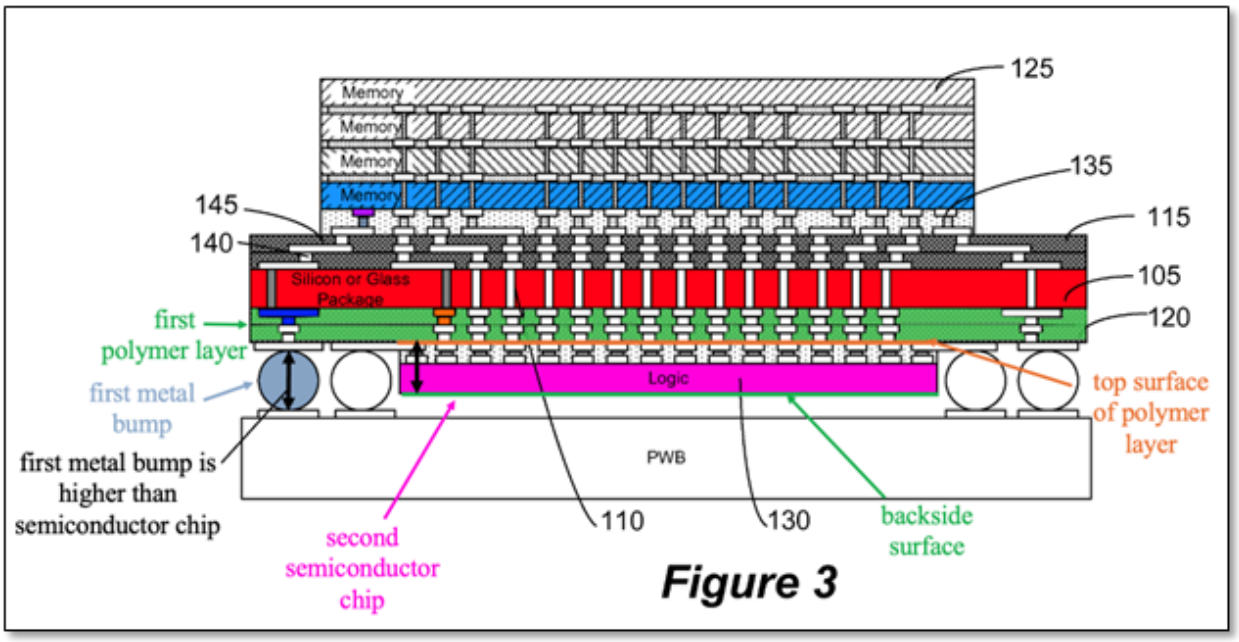
2. 14(b): "wherein said second semiconductor chip has a height is between a backside surface of said second semiconductor chip and a top surface of said first polymer layer is smaller than a thickness of said first metal bump."

224. I note that during prosecution of the related '768 Patent, the Patent Owner provided an annotated figure illustrating support for *a height is between a backside surface of said second semiconductor chip and a top surface of said second polymer layer is smaller than a thickness of said first metal bump*, as shown below.



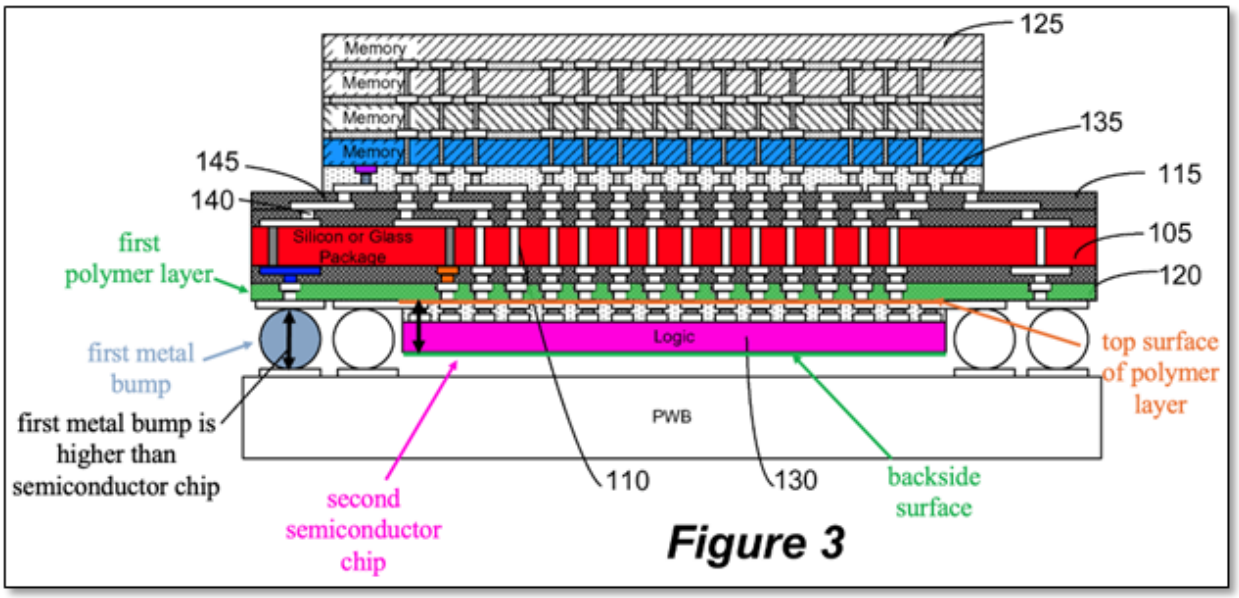
EX1032 at p. 400.

225. The *first polymer layer* includes at least the portion described above at Claim 1(c)(i) and further includes the portion highlighted below. Shown in FIG. 3, below, Sundaram's device 130 (*second semiconductor chip*) *has a height [that] is between a backside surface of* device 130 *and a top surface of* Sundaram's *first polymer layer*, which is *smaller than thickness* of Sundaram's solder ball (*first metal bump*).



EX1004 at FIG. 3. *See* ¶ 145.

226. Alternatively, Sundaram's *first polymer layer* is as annotated below, which also meets the claim limitation because Sundaram's device 130 (*second semiconductor chip*) *has a height [that] is between a backside surface of* device 130 *and a top surface of* Sundaram's *first polymer layer*, which is *smaller than thickness* of Sundaram's solder ball (*first metal bump*).



EX1004 at FIG. 3. *See* ¶ 146.

N. *Claim 16: "The chip package of claim 1, further comprising a second semiconductor chip under said first interconnection scheme next to said first semiconductor chip."*

227. Sundaram teaches the "3D interposer…[is] scalable for increased number of dies, not only above and below the interposer but also side by [side.]" *EX1004* at 7:56-59, 4:26-27. As shown below, Sundaram's side-by-side configuration teaches *a second semiconductor chip under said first interconnection scheme next to said first semiconductor chip*:

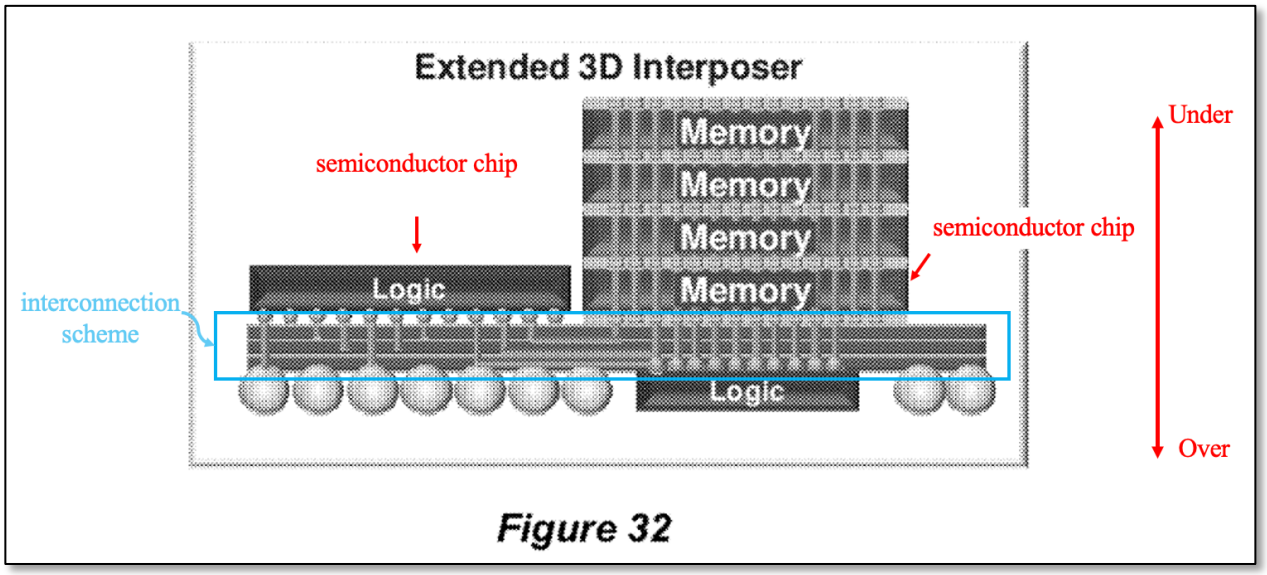


Figure 32

EX1004 at FIG. 32. A POSITA would have been motivated and found it obvious to modifying FIG. 3 per FIG. 32's teahcings of integrating DRAM and logic die into the same package. By integrating DRAM and logic into the same package, the data processing speed can be significantly improved due to the shorter transmission path between the two components, which reduces latency and enhances overall system performance. Further, a POSITA would have had a reasonable expectation of success because a chip would connect to Sundaram's RDL next to FIG. 3's first electronic device 125 in the same way as first electronic device 125 is connected.

O. *Claim 17: "The chip package of claim 1, wherein said compound comprises a SiO_2 compound."*

228. *See* Claim 1(a)(ii), ¶¶ 131-132. Sundaram teaches both a borosilicate glass interposer and a silicon interposer with an **SiO_2** layer. *EX1004* at 9:14-16,

13:58-62, FIG. 34. Borosilicate glass includes silica (SiO_2), thereby satisfying Claim 17. *EX1033* at 3:23-24 ("a borosilicate glass (**SiO_2**-B_2O_3)."); *EX1034* at 2:52-53 ("…the borosilicate glass powder contains **SiO_2**, B_2O_3, and K_2O[.]").

P. ***Claim 18:***

1. 18(Pre): "A chip package comprising"

229. *See* Claim 1(Pre)[4], ¶ 127, incorporated herein.

2. 18(a): "a solid layer having a first surface and a second surface opposite to said first surface,"

230. *See* Claim 1(a), ¶¶ 128-129, incorporated herein.

3. 18(a)(i): "wherein said solid layer comprises a compound of silicon and oxygen,"

231. *See* Claim 1(a)(ii), ¶¶ 131-132, incorporated herein.

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[4] I note that numerous claim limitations of later claims are the same or substantially the same as claim limitations from earlier claims. For example, Claim 18(Pre) is substantially the same as Claim 1(Pre). For each claim limitation that is the same or substantially the same as an earlier claim limitation, I provide a cross-reference citation to my opinions for the earlier claim limitation, which should be understood to incorporate by reference for the later claim limitation.

4. 18(a)(ii): "wherein said solid layer has a thickness between 100 and 300 micrometers;"

232. *See* Claim 1(a)(iii), ¶ 133, incorporated herein.

5. 18(a)(iii): "wherein said solid layer comprises a first region and a second region between said first region and an edge of said solid layer;"

233. *See* Claim 1(a)(iv), ¶ 136, incorporated herein.

6. 18(b): "a plurality of metal conductors in said second region of said solid layer respectively,"

234. *See* Claim 1(b), ¶ 137, incorporated herein. Claim 18(b)'s *metal conductors* correspond to Claim 1(b)'s *copper plugs*.

7. 18(b)(i): "wherein one of said plurality of metal conductors comprises a copper portion and a first metal layer covering a sidewall of said copper portion, wherein said copper portion has a diameter in a direction between 50 and 200 micrometers and greater than a thickness of said first metal layer in said direction,"

a) Sundaram's Teachings

235. Sundaram teaches the metalized through vias 110 (*plurality of metal conductors*) "can be metalized with a highly-conductive metal, for example copper" (*a copper portion*) and "can also be metalized with…a metal seeding liner" (*a first metal layer covering a sidewall of said copper portion*. *EX1004* at 6:25-29. The "metal seeding liner" is *covering a sidewall of said portion* because the seed liner is

deposited before the *copper portion*. Thus, the metal seeding liner covers the *sidewall of said copper portion*.

236. Sundaram teaches interposer 105 is "about 20 to about 200 micrometers in thickness" and the "thickness of the interposer to via diameter aspect ratio is about **1:1** to about 10:1." *EX1004* at 2:22-29. When the interposer to via diameter aspect ratio is 1:1 and the thickness of interposer 105 is 200 micrometers, the through via diameter is thus 200 micrometers based on the thickness of interposer 105. When the interposer to via diameter aspect ratio is 1:4 and the thickness of interposer 105 is 200 micrometers, the through via diameter is thus 50 micrometers based on the thickness of interposer 105. Sundaram, therefore, teaches or renders obvious through vias 110 having *a diameter in a direction between 50 and 200 micrometers*.

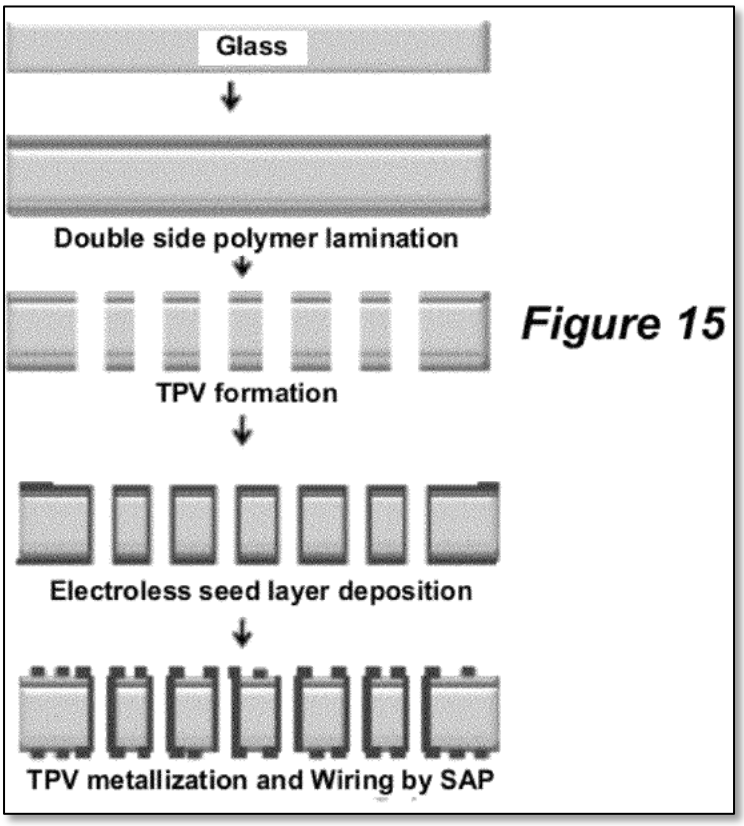
237. I note that the '763 Patent does not indicate any criticality of the claimed copper portion diameter. *EX1001* at 4:24-28. That is, the '763 Patent does not provide the range of 50 and 200 micrometers and then further provide an explanation for why such range is needed, important, or advantageous. Indeed, the '763 Patent describes a variety of ranges, including smaller (10 micrometers) and much larger values (10000 micrometers), indicating to a POSITA that the thickness can vary widely and that the thickness is not otherwise critical. *See EX1001* at 4:46-50.

238. Additionally, Sundaram teaches "TPV metallization consist[ing] of two steps: 1) Cu seed layer formation, and 2) Cu electroplating" where the seed layer is "about **0.5-1 μm thick**" and where the vias are filled with Cu. *EX1004* at 13:30-34. Thus, Sundaram teaches through vias 110 have *a diameter…greater than a thickness of said first metal layer* (0.5-1 μm) *in said direction*. A POSITA would have understood the Cu electroplating step to involve plating on the Cu seed layer, as shown below in FIG. 15, because seed layer formation prior to electroplating was a common technique to form an "electrode for an electroplating process in which a conductive material is deposited." *EX1062* at 1:42-47. Thus, because the seed layer is deposited prior to the *copper portion*, the seed layer (*first metal layer*) *cover[s] a sidewall* of the plated layer (*copper portion*).

b) Motivation to Combine Sundaram's Internal Embodiments

239. To the extent Patent Owner argues Sundaram's teachings of the Cu electroplating to be a separate embodiment, a POSITA would have been motivated and found it obvious to modify Sundaram's glass interposer to have copper filled vias as taught in Sundaram's Polycrystalline Interposer Example #6 described above. *See* ¶ 238; *EX1004* at 13:30-34. Filled plated copper vias had been commonly in use before the '763 Patent using via fill technology that often involved time-dependent plating conditions. *See*, *e.g.*, *EX1011* at FIG. 5G, [0054]-[0055]. A

POSITA would have found it obvious at least because Sundaram also teaches forming TPVs in glass substrate with a seed layer. For example, as shown below, Sundaram teaches "electroless seed layer deposition" is performed prior to "TPV metallization…by SAP." *EX1004* at FIG. 15. As such, a POSITA would have found it obvious to apply Sundaram's method of "TPV metallization consist[ing] of two steps: 1) Cu seed layer formation, and 2) Cu electroplating" where the seed layer is "about **0.5-1 μm thick**" to interposer 105. *EX1004* at 13:30-34.



EX1004 at FIG. 15.

240. A POSITA would have appreciated the benefits of a seed layer for growing the Cu in the through via, such as "void-free electroplating" as taught by Sundaram. *EX1004* at 13:38-40. Indeed, it was known that a "missing seed layer" may "lead to a void in the electroplated metal" resulting in an "increase in their resistance and result in poor reliability." *EX1063* at 3:12-16. Thus, a POSITA would have been motivated to reduce the risk of void formation in Sundaram's electroplated copper, thereby correspondingly reducing the risk of increased resistance and poor reliability. The combination is the application of a known technique (seed layer formation) to a known device (Sundaram's through vias 100) ready for improvement to yield the predictable result of Sundaram's through vias having a *first metal layer covering a sidewall of said copper portion, wherein said copper portion has a diameter in a direction between 50 and 200 micrometers and greater than a thickness of said first metal layer in said direction*. There would have been a reasonable expectation of success at least because Sundaram already teaches a process of forming such a copper seed layer and because seed layers were commonplace in forming vias. *See, e.g., EX1064* at FIGS. 1A-C, [0004] ("…then forming a copper seed layer 16" on the "entire surface of the base 10, including interior surfaces of the via holes 12[.]"), [0005]-[0007].

8. 18(b)(ii): "wherein said first region has a width in said direction greater than a shortest distance between a sidewall of one of said plurality of metal conductors and said edge of said solid layer in said direction and greater than a pitch between two neighboring metal conductors of said plurality of metal conductors;"

241. *See* Claim 1(b)(ii), ¶¶ 140-141, incorporated herein.

9. 18(c): "a first interconnection scheme over said first surface,"

242. *See* Claim 1(c), ¶¶ 142, incorporated herein.

10. 18(c)(i): "wherein said first interconnection scheme comprises a first metal interconnect over said first surface and a first polymer layer over said first metal interconnect,"

243. *See* Claim 1(c)(i), ¶¶ 144, incorporated herein.

11. 18(c)(ii): "wherein said first metal interconnect is connected to a first metal conductor of said plurality of metal conductors,"

244. *See* Claim 1(c)(ii), ¶¶ 147, incorporated herein.

12. 18(c)(iii): "wherein said first metal interconnect comprises a first copper layer;"

245. *See* Claim 1(c)(iii), ¶ 148, incorporated herein. Claim 18(c)(iii)'s *first copper layer* corresponds to Claim 1(c)(iii)'s *second copper layer*.

13. 18(d): "a second interconnection scheme under said second surface,"

246. For the same reasons described above at claim 1(c), the series of traces 145 and vias 140 in the "polymer-metal redistribution layers" *under* the *second surface* of interposer 105 is a *second interconnection scheme under said second surface*. *See* ¶ 142. Indeed, Sundaram teaches that the "polymer-metal redistribution layer[]" is also deposited on "first side 115" of interposer 105 which, as depicted below, is *under said second surface*. *EX1004* at 6:62-67.

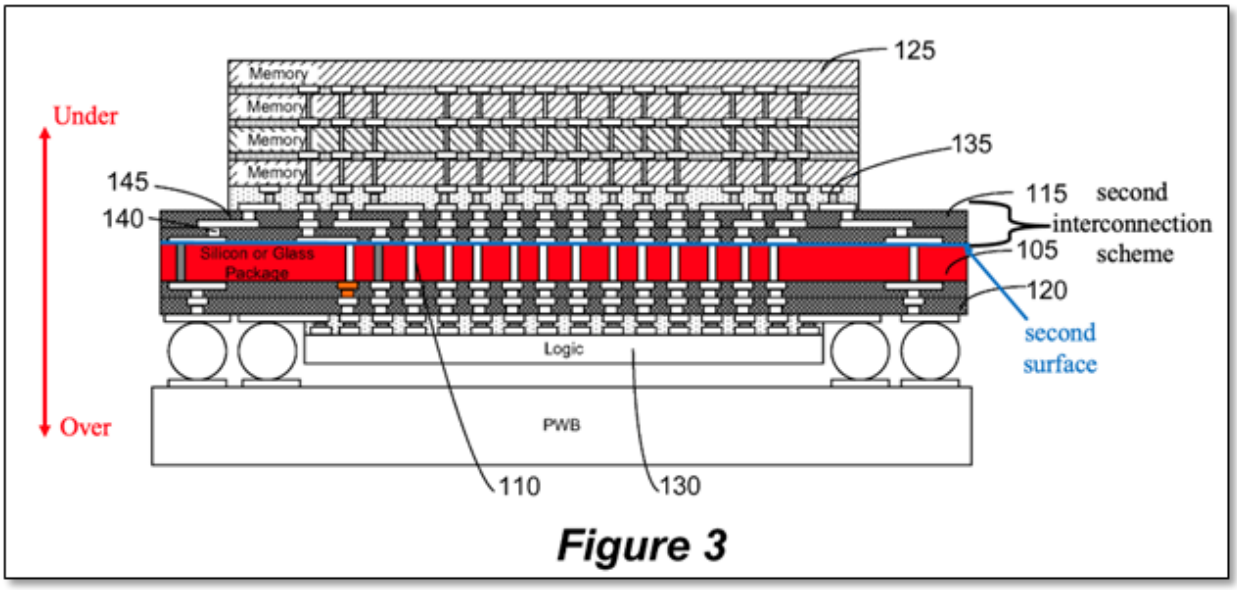


Figure 3

EX1004 at FIG. 3.

14. 18(d)(i): "wherein said second interconnection scheme comprises a second metal interconnect under said second surface and a second polymer layer under said second metal interconnect,"

247. *See* Claims 18(c)(i), 1(c)(i), ¶¶ 243, 144, incorporated herein. Sundaram's RDLs are "polymer-**metal**" and include *interconnects* in the form of

"blind vias 140 and conductor traces 145." *EX1004* at 6:62-67. Additionally, die pads 135 are part of the *second interconnection scheme* for the same reasons described above, i.e., because they electrically connect devices. *See* ¶ 142; *EX1004* at 6:29-31. Sundaram's *second metal interconnect* and *second polymer layer*, which is *under said second metal interconnect* are shown below:

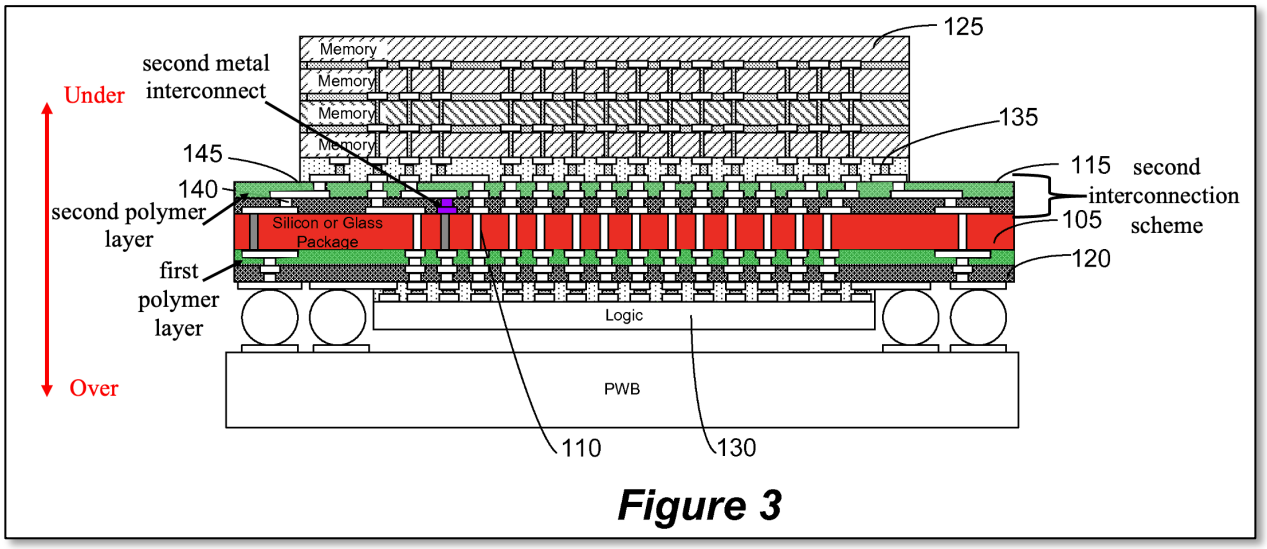
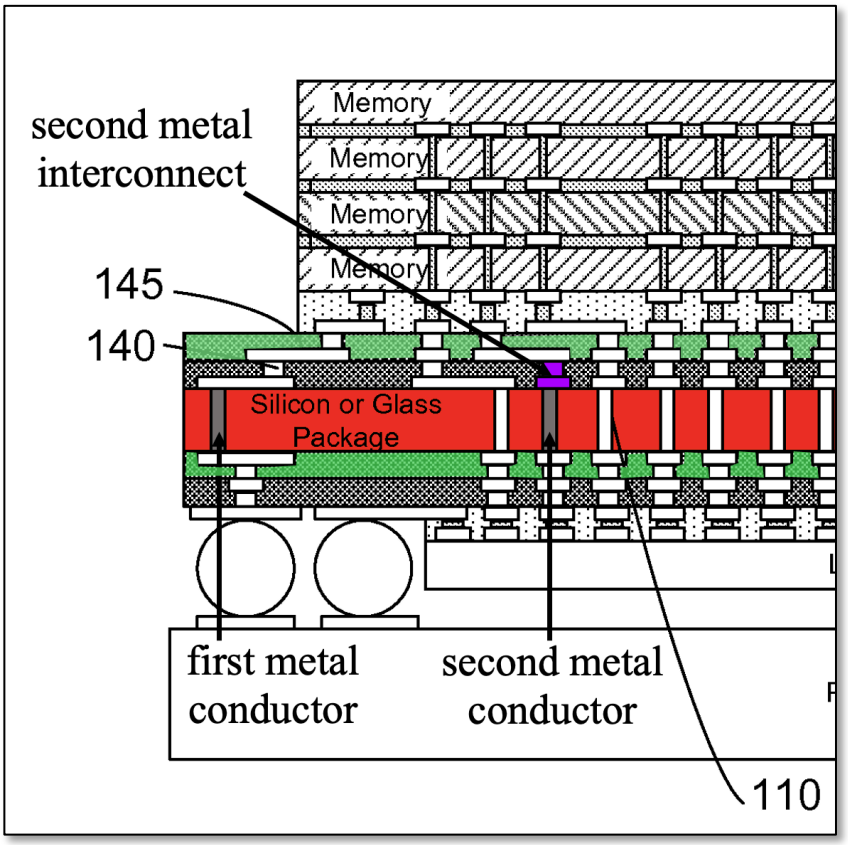


Figure 3

EX1004 at FIG. 3.

15. 18(d)(ii): "wherein said second metal interconnect is connected to a second metal conductor of said plurality of metal conductors,"

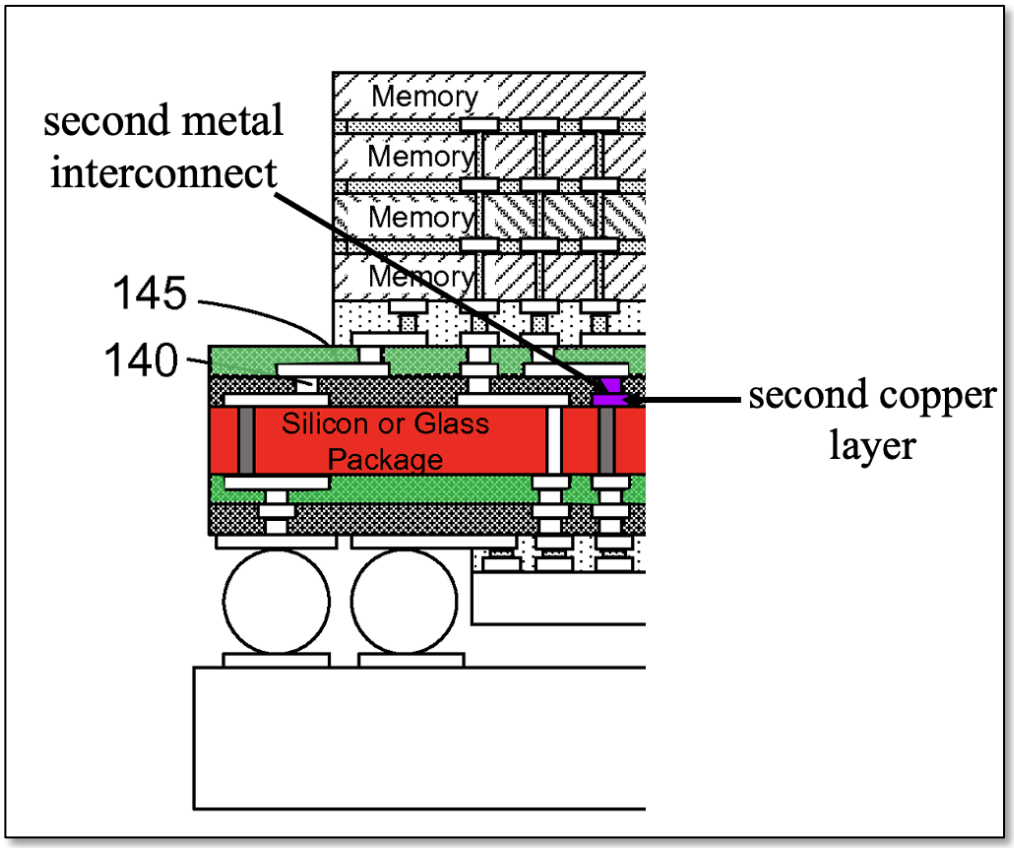
248. For the same reasons described above and as shown below, Sundaram's *second metal interconnect is connected to a second metal conductor of said plurality of metal conductors*. *See* ¶ 147; *EX1004* at 7:4-8.



EX1004 at FIG. 3 (excerpt).

16. 18(d)(iii): "wherein said second metal interconnect comprises a second copper layer; and"

249. *See* Claims 18(c)(iii), 1(c)(iii), ¶¶ 245, 148, incorporated herein. Sundaram's conductor trace 145 comprises *a second copper layer*. *EX1004* at FIG. 15.



EX1004 at FIG. 3 (excerpt).

17. 18(e): "a first semiconductor chip under said first interconnection scheme,"

250. *See* Claim 1(e), ¶ 161, incorporated herein.

18. 18(e)(i): "wherein said first semiconductor chip comprises a first metal bump on a first metal pad of said first semiconductor chip,"

251. *See* Claim 1(e)(i), ¶¶ 162-166, incorporated herein. Claim 18(e)(i)'s *first metal bump* corresponds to Claim 1(e)(i)'s *third metal interconnect*.

19. 18(e)(ii): "wherein said first metal bump comprises a third copper layer with a thickness between 5 and 30 micrometers,"

252. *See* Claim 1(e)(ii), ¶¶ 167-175, incorporated herein.

20. 18(e)(iii): "wherein said first semiconductor chip is connected to a third metal interconnect of said second interconnection scheme through said first metal bump."

253. Sundaram teaches electronic device 125 (*first semiconductor chip*) is "connected with through vias 110, **blind vias 140, and conductor traces 145**." *EX1004* at 7:4-8. As discussed above, blind vias 140, conductor traces 145, and die pads 135 form *metal interconnect[s]* in the *second interconnection scheme*. *See* Claim 18(d)(i); ¶ 247. Additionally, die pads 135 "electrically connect devices using solder, copper bumps with solder caps…" thus forming the *first metal bump.* As shown, first electronic device 125's bump (the *first metal bump*) *is connected to a third metal interconnect* formed by a die pad 135and blind via 140 *of said second interconnection scheme*. *See* ¶ 251.

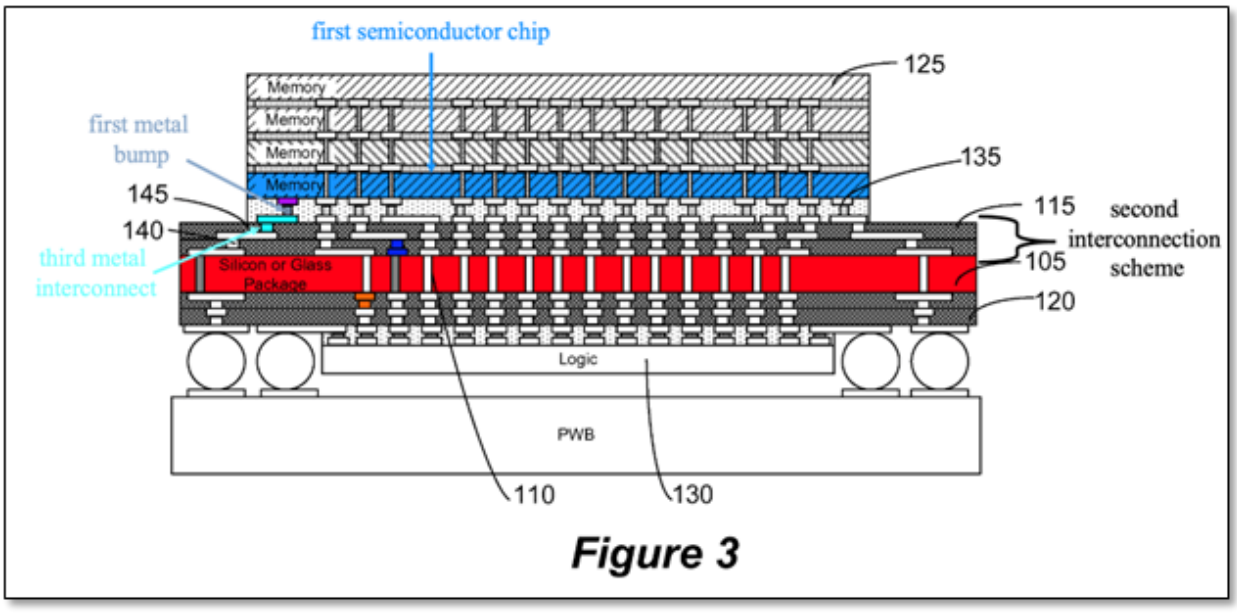


Figure 3

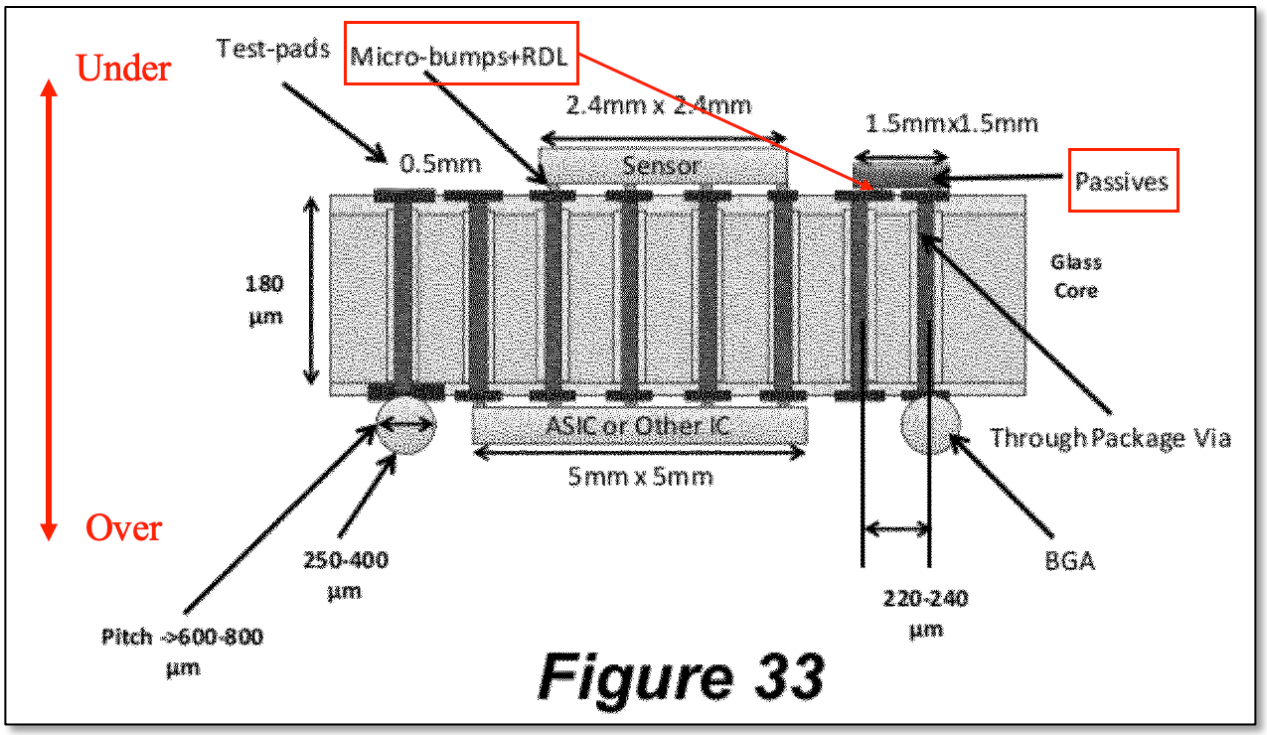
EX1004 at FIG. 3.

Q. ***Claim 19: "The chip package of claim 18, wherein said compound comprises a SiO_2 compound."***

254. *See* Claim 17, ¶ 228, incorporated herein.

R. ***Claim 20: "The chip package of claim 18, further comprising a first passive component under said first interconnection scheme."***

255. *See* Claim 2, ¶¶ 176-183, incorporated herein. As shown, Sundaram teaches the "passives" (*passive component*) *under* an *interconnection scheme*:



EX1004 at FIG. 33.

S. ***Claim 21: "The chip package of claim 18, wherein said first semiconductor chip comprises a central-processing-unit (CPU) circuit block and a graphics-processing-unit (GPU) circuit block."***

256. *See* Claim 5, ¶¶ 189-191, incorporated herein.

T. ***Claim 23: "The chip package of claim 18, wherein said solid layer further comprises a third region opposite to said second region, wherein said third region is between said first region and another edge of said solid layer, wherein said plurality of metal conductors in said third region."***

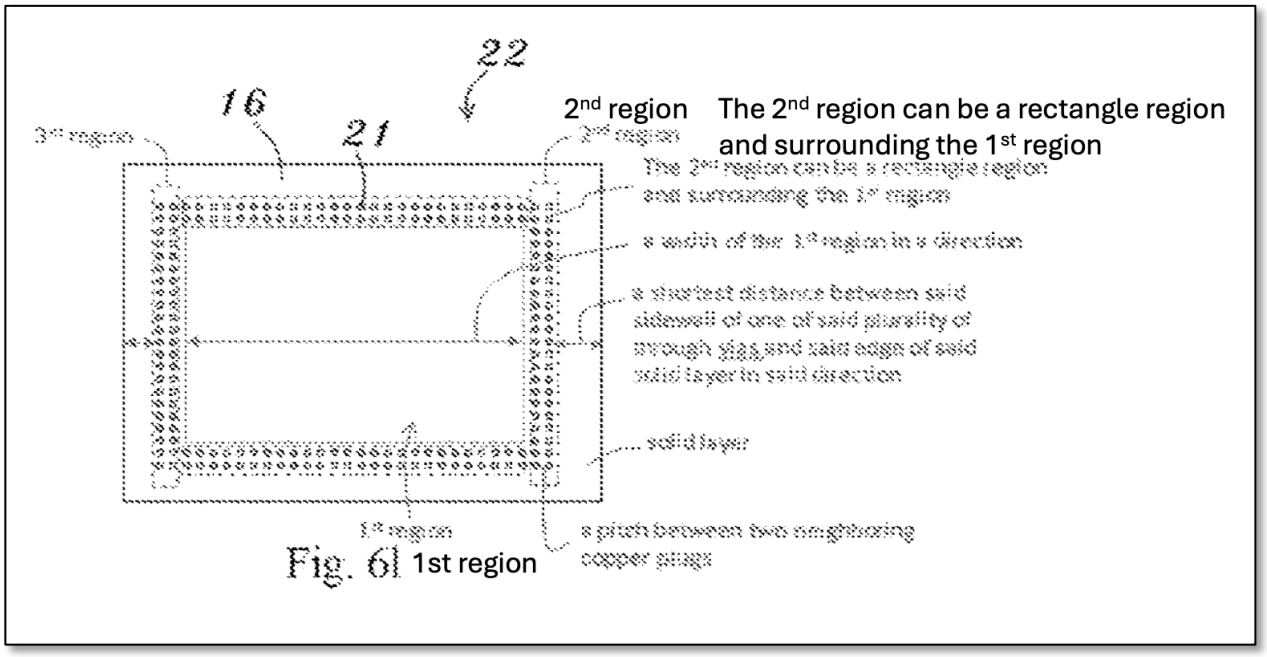
257. *See* Claim 10, ¶ 215, incorporated herein.

IX. OPINIONS REGARDING GROUND 1B: CLAIMS 13 AND 15 ARE OBVIOUS OVER SUNDARAM, LIN-191, AND LIN-863

A. ***Claim 13: "The chip package of claim 1, wherein said second region is a rectangle region and surrounding said first region."***

a) The '763 Patent's "First Region" and "Second Region"

258. I note that during prosecution of the '763 Patent, the Patent Owner provided an annotated version of FIG. 6l arguing specification support for the claimed *rectangle region*, shown below. As I will detail below, the combination of Sundaram-Lin-191-Lin-863 renders obvious a *rectangle region* that is consistent with Patent Owner's alleged support for such claim terms provided during prosecution.



EX1002 at p. 272.

b) Sundaram's Teachings

259. Sundaram teaches "device 125 is of a different pad size and configuration than" device 130 and "connected with through vias 110, blind vias 140, and conductor traces 145." *EX1004* at 7:1-9, FIG. 4. Based on FIGS. 3-4, a POSITA would have understood Sundaram to teach two types of vias 110: (1) through vias for die-to-die connections between first electronic device 125 and second electronic device 130, and (2) through vias for die to PWB connections. Indeed, as shown below, Sundaram's through vias for die to PWB connections connect first electronic device 125 to the PWB because the blue through vias are connected to conductive traces 145 and blind vias 140 in the polymer-metal

redistribution layer that first electronic device 125 connects to. *EX1004* at 6:62-67. Further, per FIGS. 3-4, the die-to-die connections (dashed lines in FIG. 4) are made through pads located at the periphery of the dies, which are connected to the die-to-die vias 110 in interposer 105 (FIG. 3). That is, Sundaram teaches the pads illustrated at the periphery of the dies in FIG. 4 are connected "with through vias" which corresponds to the die-to-die vias 110 shown in FIG. 3. *EX1004* at 7:4-7. Additionally, per FIG. 3, die-to-die vias 110 and the pads of the smaller device 130 are substantially within the same projection region, while the die-to-PWB vias 110 are located outside the peripheral area of the smaller device 130.

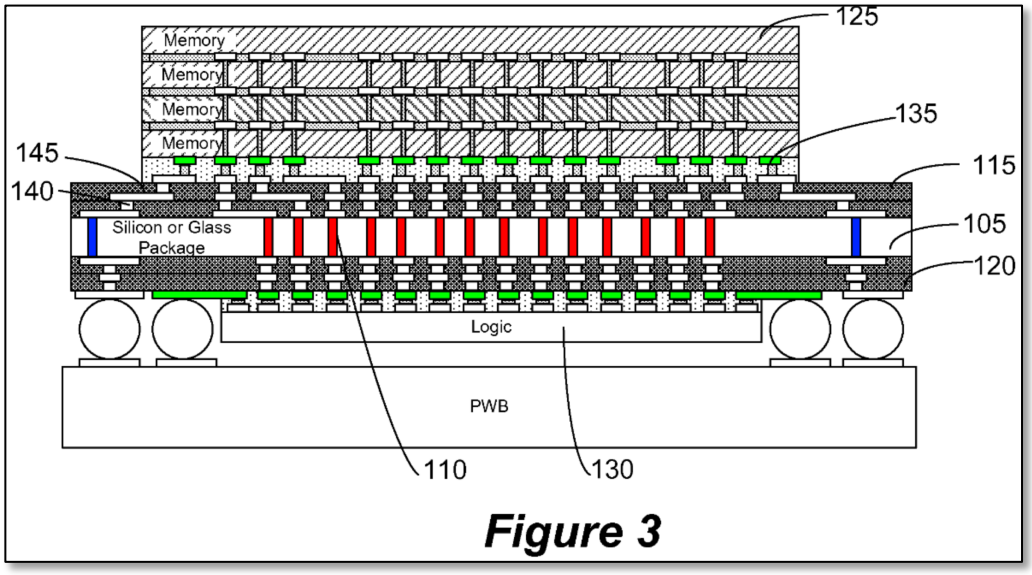


Figure 3

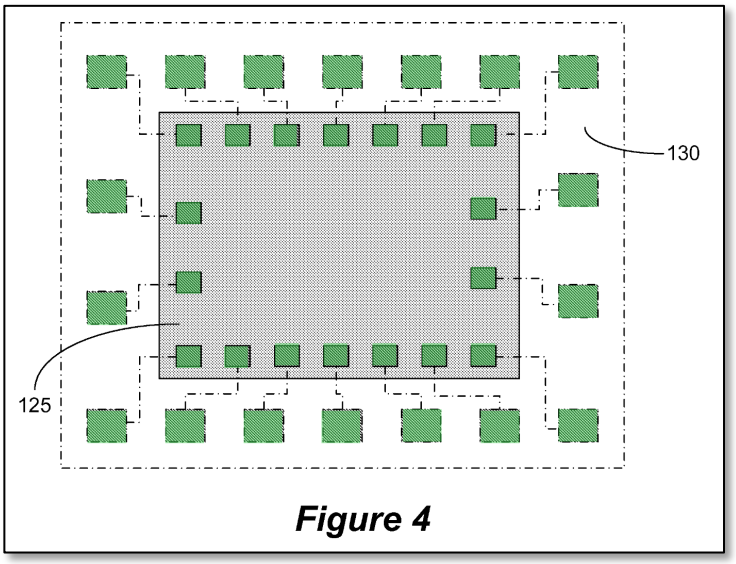


Figure 4

EX1004 at FIGS. 3-4.

260. Thus, because (1) die-to-die vias 110 are located substantially within the same area as second electronic device 130, and (2) the vias for die to PWB connections are located peripherally to second electronic device 130, a POSITA would have understood a plan view of Sundaram's interposer 105 to look as follows:

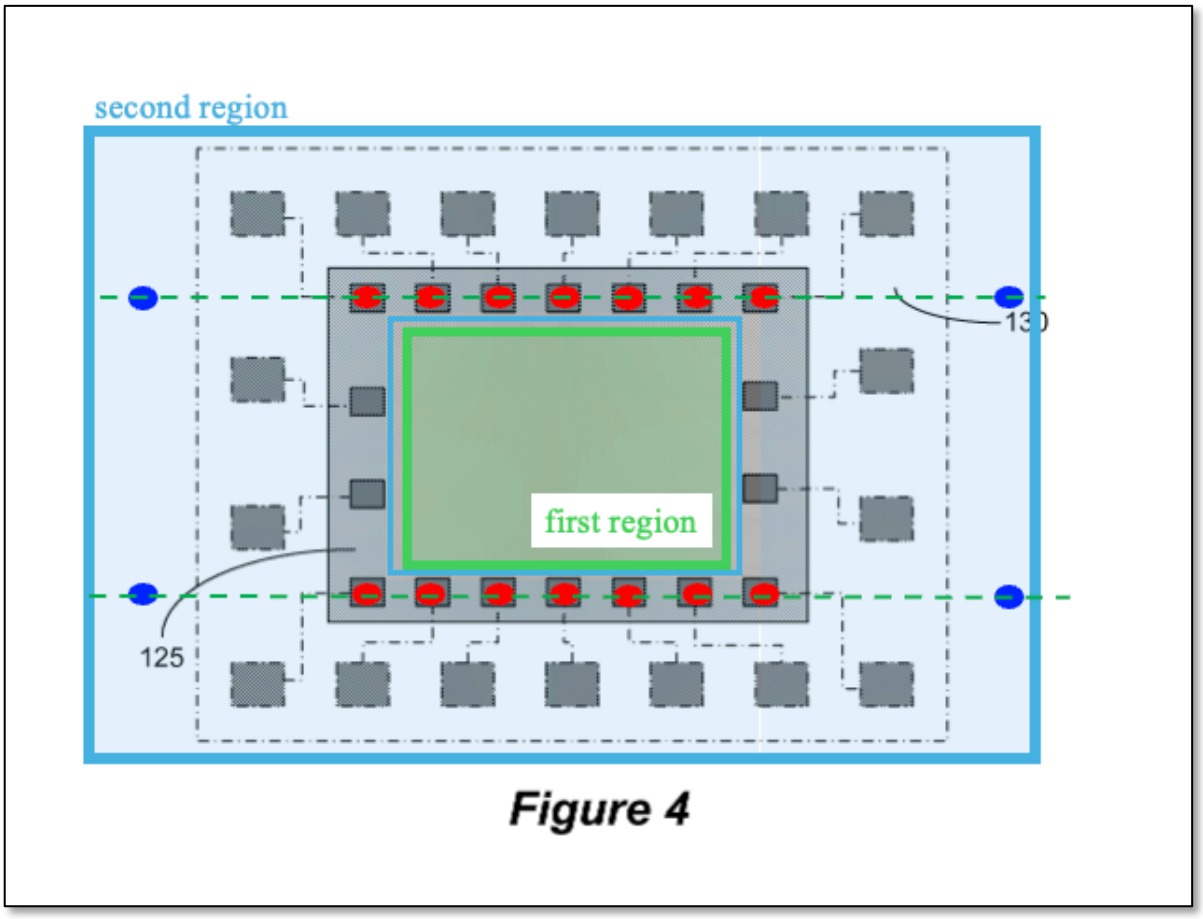


Figure 4

EX1004 at FIG. 4. The dashed lines illustrate exemplary cross-sectional lines corresponding to FIG. 3's cross-section, where both vias for die-to-die connections and vias for die to PWB connections are depicted.

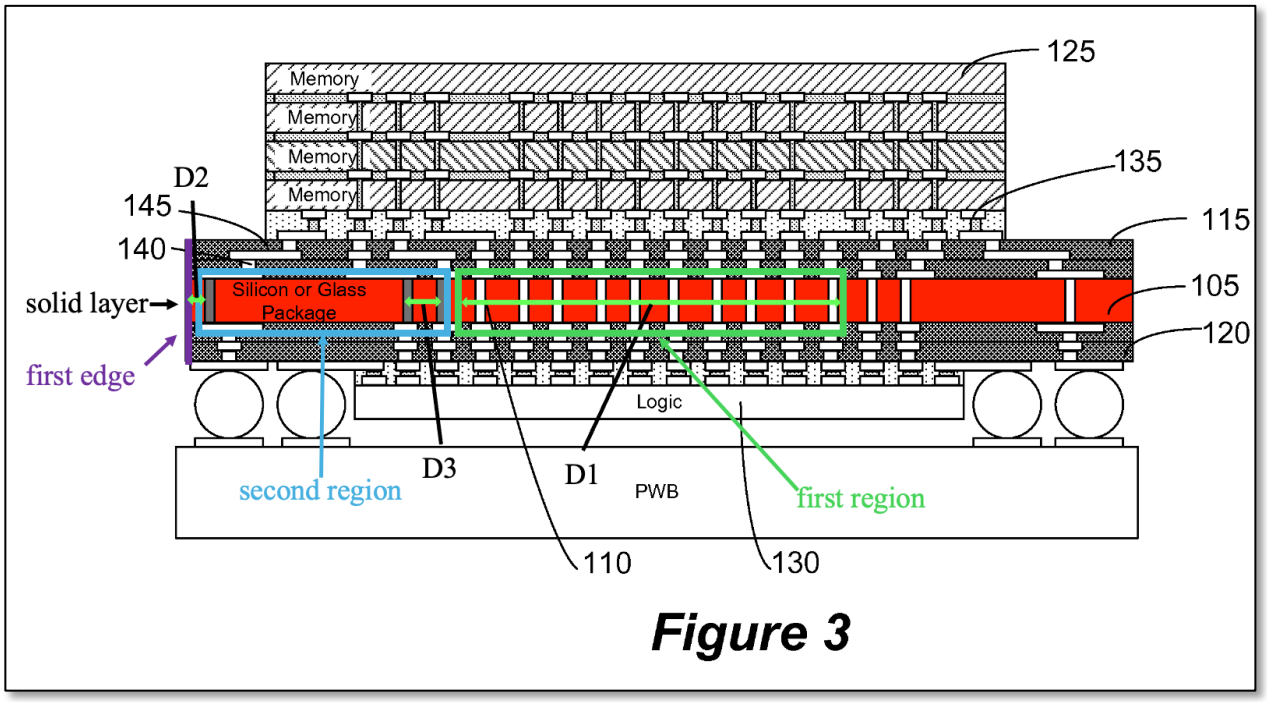


Figure 3

EX1004 at FIG. 3.

261. I note that a POSITA would have understood Sundaram's FIG. 4 to mislabel first electronic device 125 and second electronic device 130 based on their depiction in FIG. 3. Specifically, as shown in FIG. 3, first electronic device 125 is larger than second electronic device 130, whereas in FIG. 4, second electronic device 130 is larger than first electronic device 125. Based on FIG. 3, a POSITA would understand that instead of as labeled, in FIG. 4, the larger outer white box represents first electronic device 125 whereas the smaller inner gray box represents second electronic device 130. Such a configuration is consistent with FIG. 3, where second

electronic device 130 is smaller than first electronic device 125, thereby accommodating space for the solder balls to connect to the PWB.

262. Based on these teachings, a POSITA would have understood Sundaram as teaching the *second region is a rectangle region and surrounding said first region* because the vias for die-to-die connections as depicted are positioned around the periphery of first electronic device 125, such that each through via for die-to-die connections corresponds to a die pad located on the periphery of first electronic device 125. *See* ¶ 260.

263. To the extent PO argues the *rectangle region* is the right-hand side (per *EX1002* at p. 360), Sundaram teaches it:

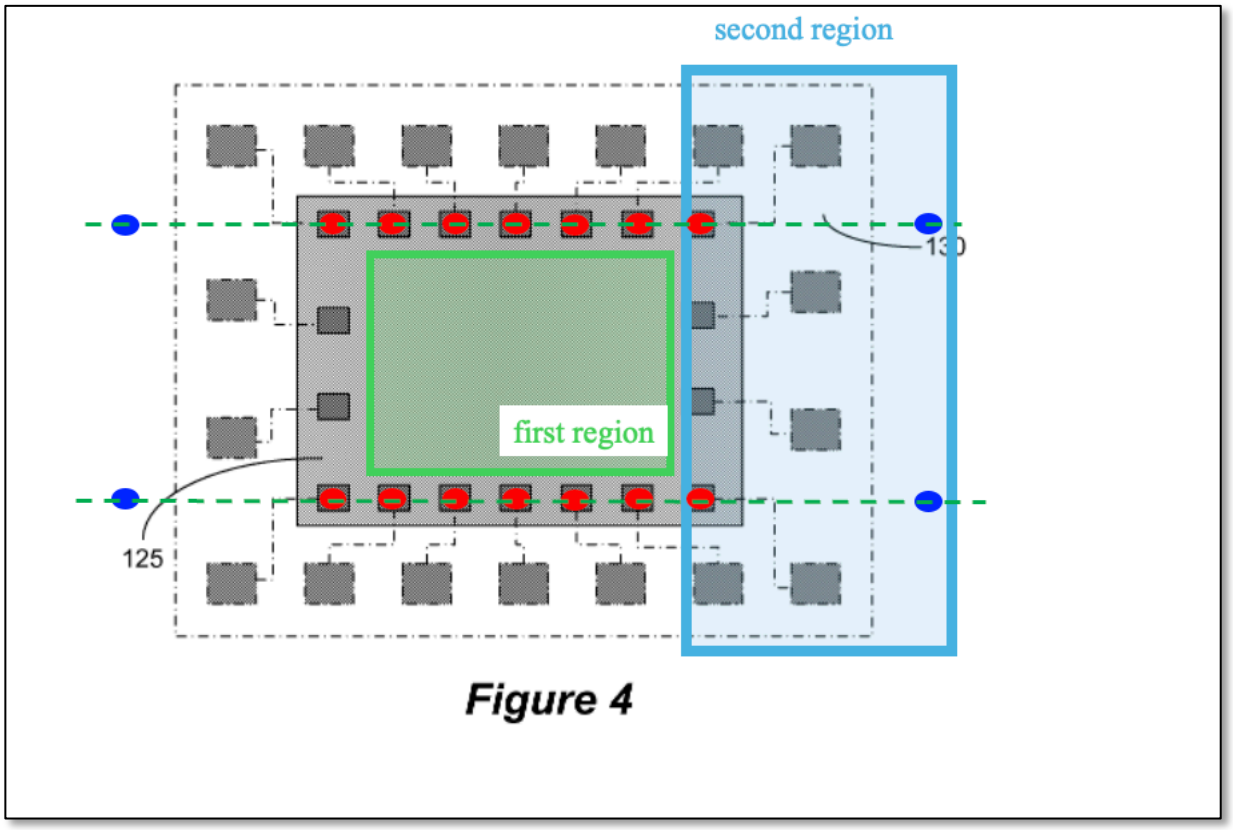


Figure 4

EX1004 at FIG. 4.

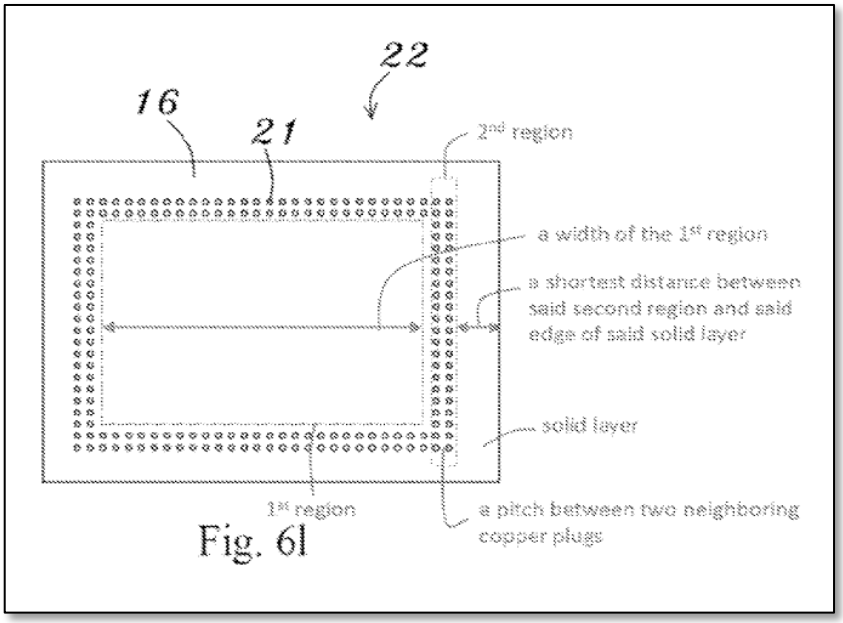


Fig. 6I

EX1002 at p. 360

c) Lin-863's Teachings

264. Additionally or alternatively to Sundaram, Lin-863 teaches a fan-out wafer level chip scale package (Fo-WLCSP) 262 having an encapsulant 226 (i.e., a *solid layer*) through with "conductive TMV[s] [through-mold vias] 225" and "semiconductor die 124" are disposed. *EX1007* at 12:33-42, 14:45-46, FIGS. 9a-9b. Lin-863's TMVs 225 are, like Sundaram's through vias 110, made of copper. *EX1007* at 8:12-20; *EX1004* at 6:25-27. As shown below, Lin-863's package 262 includes a *first region* and *a second region*. *EX1002* at 272. Lin-863's *first region* (green) is surrounded by the *second region* (blue). Lin-863's *second region* is the region on substrate 226 where, as shown below, conductive TMVs 225 are located. As can further be seen in FIG. 9b, because Lin-863's conductive TMVs in the *second region* surround the *first region*, Lin-863's *second region is a rectangle region and surrounding said first region*.

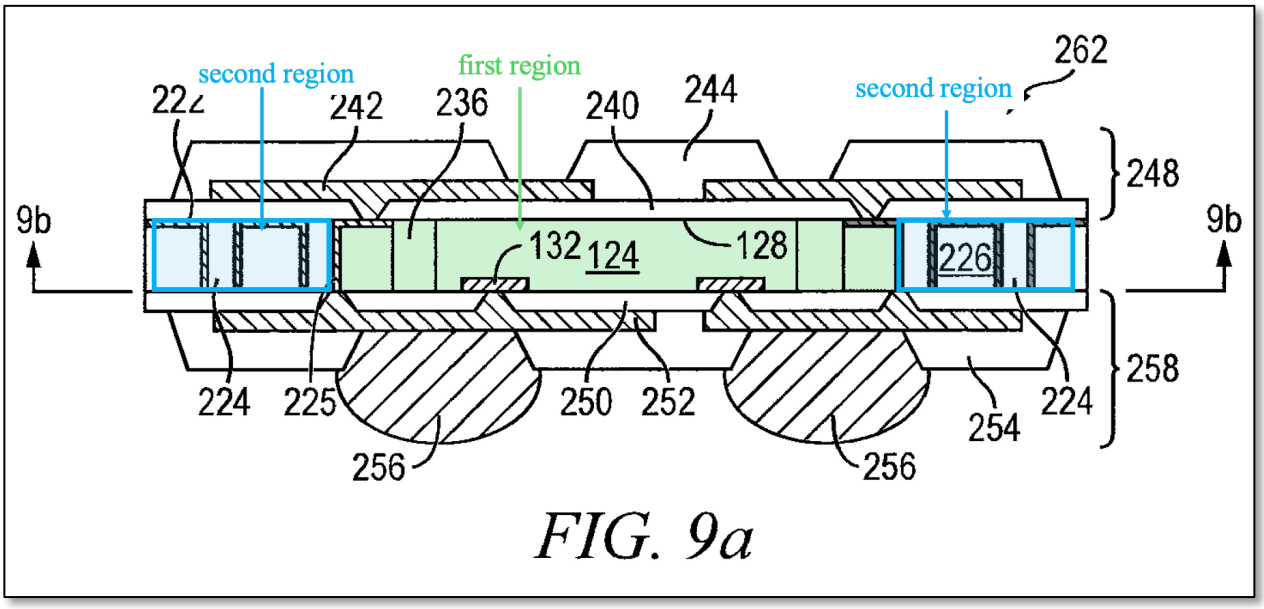

second region
first region
second region
262
222
242
236
240
244
248
9b
9b
132
124
128
226
224
225
250
252
254
224
258
256
256

FIG. 9a

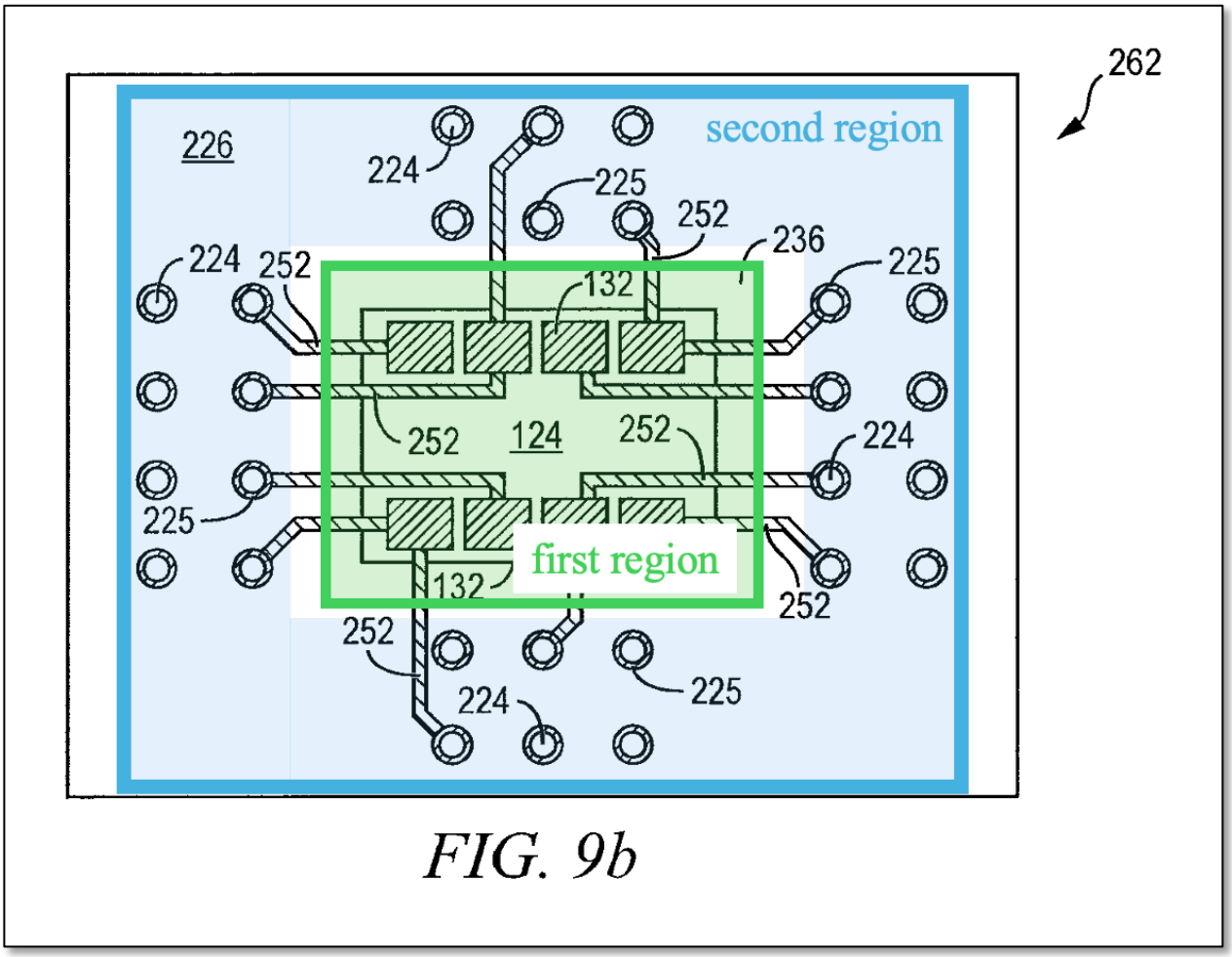

262
226
second region
224
225
252
236
225
224
252
132
252
124
252
224
225
first region
132
252
252
225
224

FIG. 9b

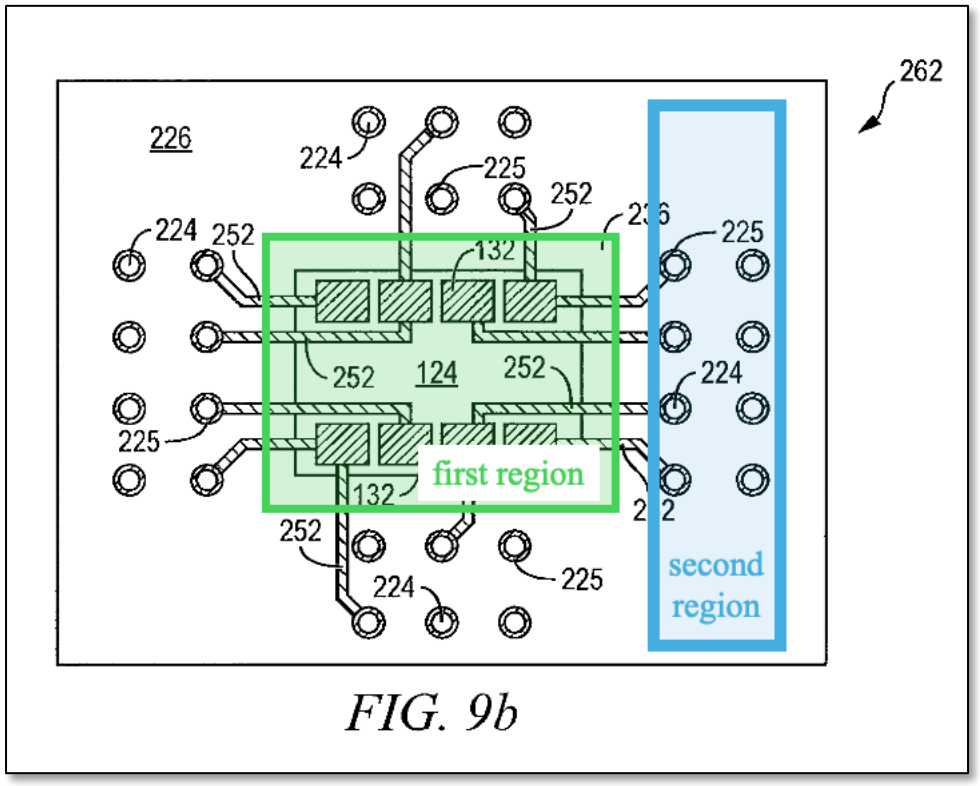


FIG. 9b

EX1007 at FIGS. 9a-b.

d) Motivation to Combine

265. Alternative to the above mapping that Sundaram teaches Claim 13 and if otherwise disputed, a POSITA would have found it obvious and been motivated to configure Sundaram's *second region* having through vias 110 to be *a rectangle region surrounding said first region* based on Lin-863's *rectangle region* having TMVs 225 surrounding Lin-863's *first region*. As shown below and discussed above, Sundaram already at least contemplates such a *rectangle region* in FIG. 4, which "illustrates a top view of the interconnect structure illustrated in FIG. 3" and

depicts chips pads that are connected "with through vias 110[.]" *EX1004* at 3:27-28, 7:1-8; ¶ 260.

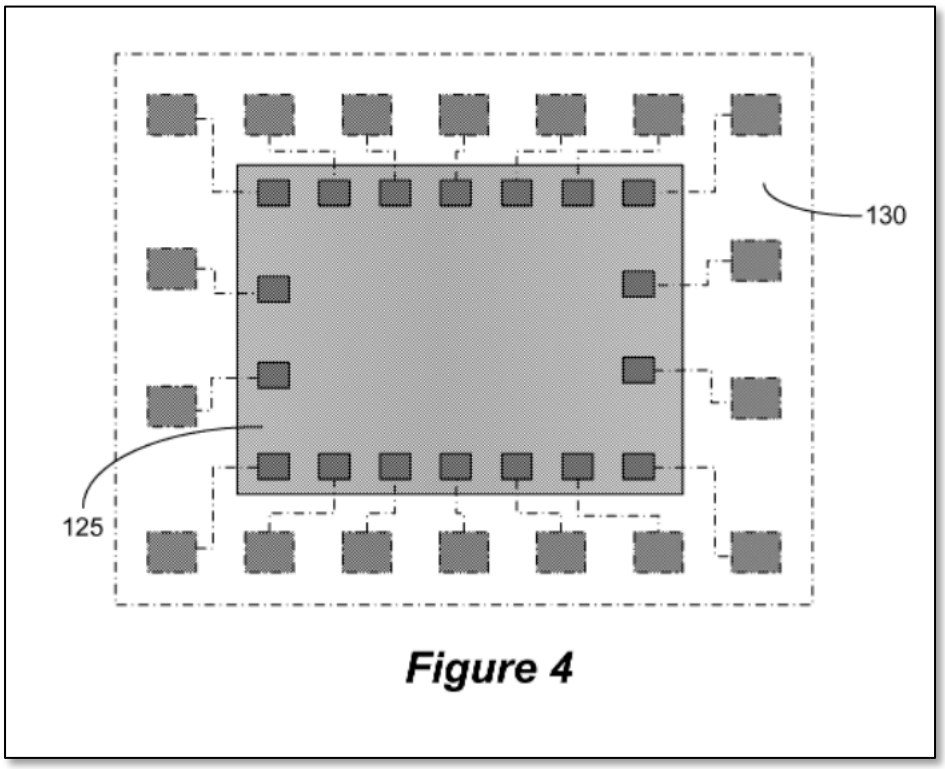


Figure 4

EX1004 at FIG. 4.

266. Based on Sundaram's contemplation of such a *rectangle region*, a POSITA would have found it obvious to structure Sundaram's chip package with through vias 110 in a rectangular second region, per Lin-863, such that the through vias 110 would interconnect the peripheral chip pads of Sundaram's first electronic device 125 and second electronic device 130. Such an arrangement also permits the addition of passive components directly under the chip or, it allows for placement of

heat sink material directly under the chip, improved thermal dissipation, and shorter interconnect paths by embedding the chip within the interposer/package.

267. Further, a POSITA would have been motivated and found it obvious to modify Sundaram's chip package to have through vias 110 in a rectangular second region surrounding a first region to match the standard rectangular geometry of a chip. *EX1069* at 1:65-66 ("Most conventional IC chips have a generally square or rectangular shape when observed in a plan view."). Specifically, chips are cut into a rectangular shape as non-rectangular shapes are difficult to dice using standard dicing machines (e.g., saws) and because non-rectangular shapes do not maximize the use of valuable wafer area where circuitry can be fabricated. *EX1069* at 1:66–2:9 ("This configuration [square or rectangular] is due, at least in part, to the conventional wafer dicing technique[.], "…the dicing machine is typically limited to making long, straight cuts and cannot effectively or efficiently cut more complex IC chip profiles."). Thus, it is practical and common practice to surround a chip with posts arranged in a geometry that mirrors the chip's shape, e.g., to mirror the rectangular shape of device 125. *See, e.g., EX1070* at FIG. 6G; *EX1007* at FIG. 8b; *EX1010* at FIGS. 2, 22; *EX1069* at 2:31-33 ("The generally square or rectangular shape of the conventional IC chip tends to be reflected in the shape of the packages incorporating such IC chips…").

268. The combination is the application of known technique (interconnects in a rectangular arrangement in a chip package) to a known device (Sundaram's chip package) to yield the predictable results of Sundaram's package having through vias 110 in a rectangular region surrounding Sundaram's *first region*. A POSITA would have had a reasonable expectation of success in modifying Sundaram's chip package, per Lin-863, to have a *rectangle region* as the *second region* because Lin-863's fan-out package was well-known and widely used for chip packaging applications. *See, e.g., EX1070* at FIG. 6G; *EX1007* at FIG. 8b; *EX1010* at FIGS. 2, 22.

B. *Claim 15: "The chip package of claim 1, wherein no any copper plug[5] in said first region."*

269. As I discussed above, a POSITA would understand a plan view of Sundaram's interposer 105 to look as follows:

[5] I have been instructed to interpret "no any copper plug" as "no copper plug."

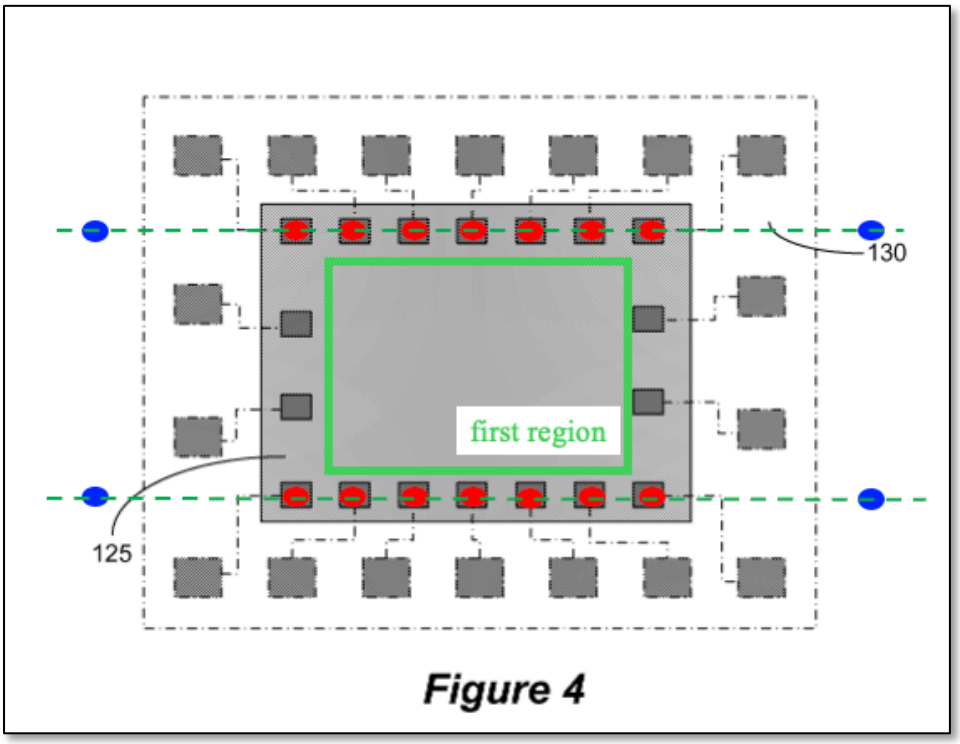


Figure 4

EX1004 at FIG. 4. *See* ¶¶ 259-260.

270. Because Sundaram teaches die-to-die vias connecting pads at the periphery (as opposed to pads in the middle of the dies), a POSITA would have understood Sundaram as teaching the *first region* as having no copper plugs. Indeed, Sundaram's depictions of pads located at the periphery of first electronic device 125 and second electronic device 130 is consistent with traditional metal pad layout architecture, where the "traditional structure is a peripheral array, with contact terminals arranged along or near the periphery of the active circuitry" of a semiconductor device. *EX1103* at 3:67–4:2. A POSITA would understand that where there is no metal pads (i.e., in the middle of Sundaram's dies) there is,

correspondingly, no need for interconnections such as through vias 110. As such, Sundaram's *first region* as depicted above is a region with *no any copper post*.

a) Lin-863's Teachings

271. Additionally or alternatively to Sundaram, Lin-863's *first region* has no *copper…plug[s]* as shown in FIG. 9a, where there are no conductive TMVs 225 present in the *first region*.

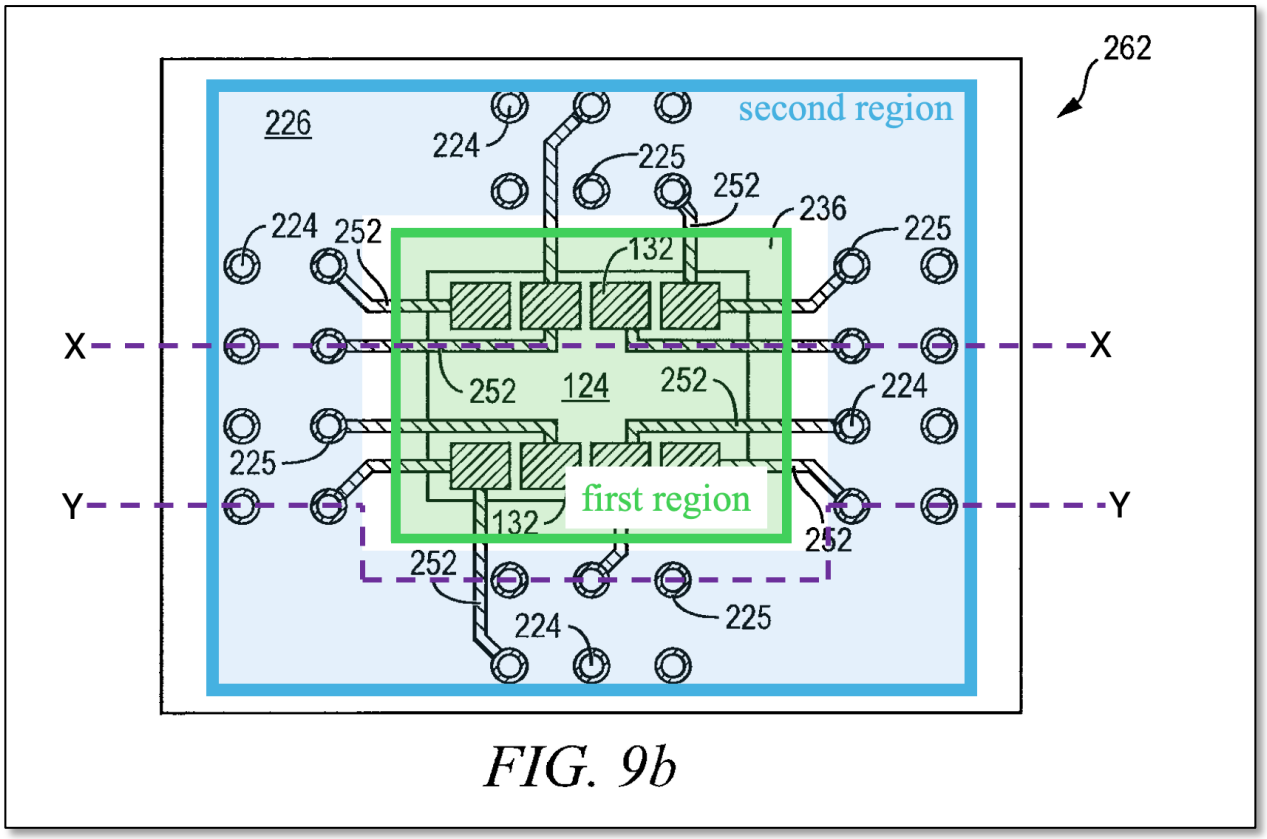


FIG. 9b

EX1007 at FIG. 9b.

272. The lack of *copper plug[s]* in the *first region* is further confirmed in FIG. 9a, which is a "cross-sectional view of Fo-WLCSP 262[,]" where Lin-863's

TMVs 224 are positioned peripherally to Lin-863's *first region*. *EX1007* at 14:45-46.

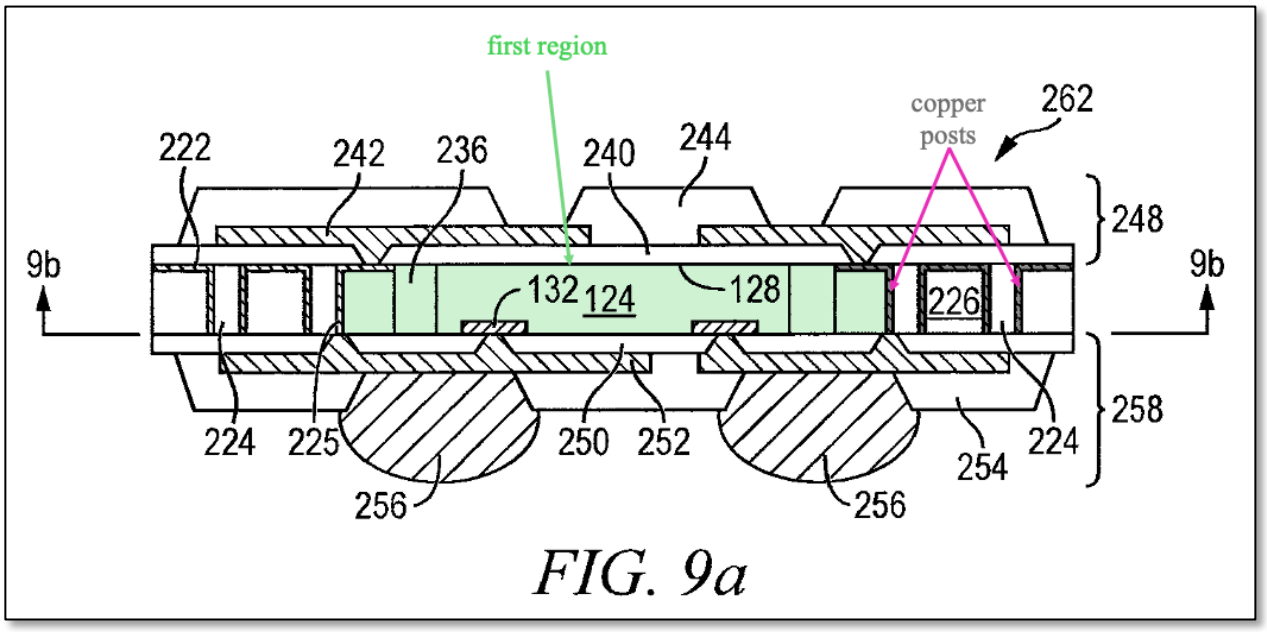
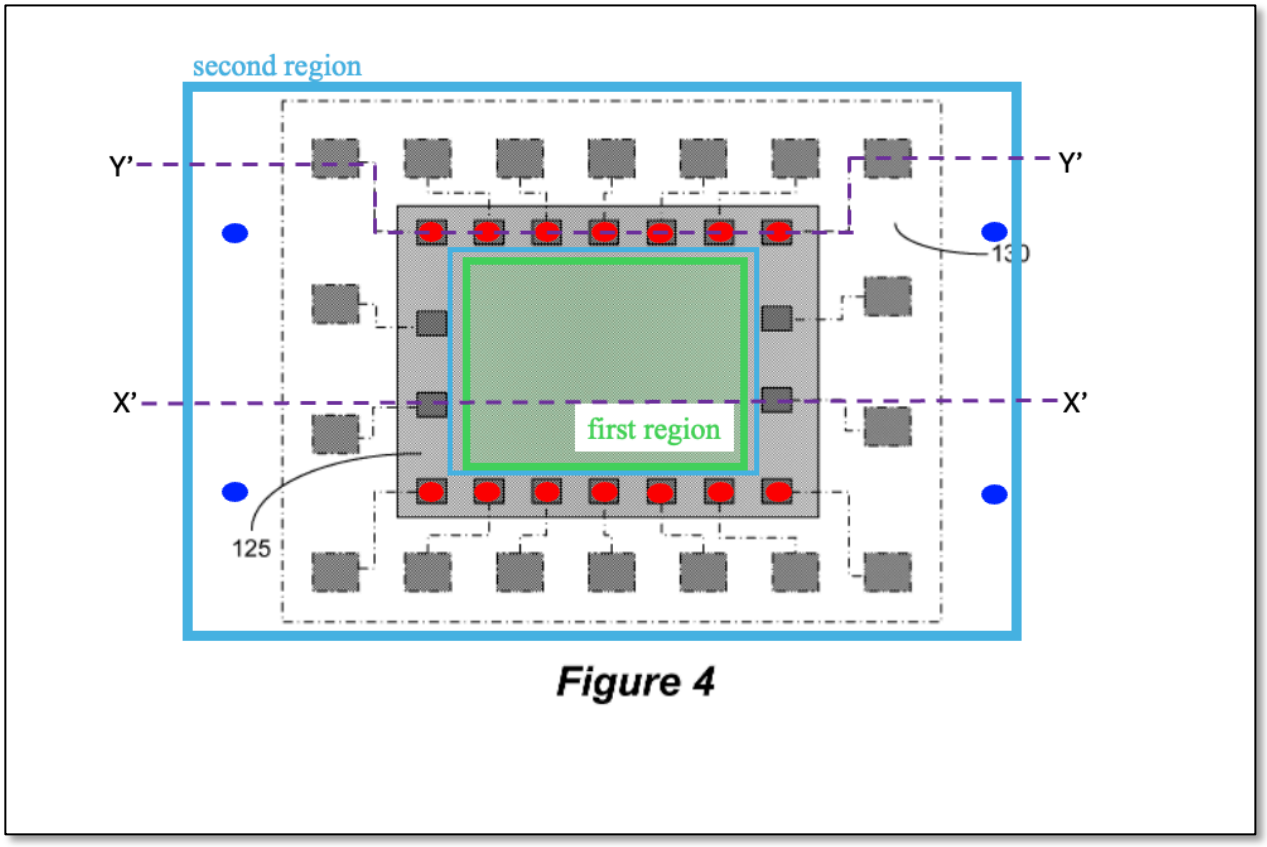


FIG. 9a

EX1007 at FIG. 9a.

273. The 9b-9b cross-section line in FIG. 9a corresponds to the X-X line annotated in FIG. 9b. A POSITA would understand the view shown in Sundaram's FIG. 3 to be taken along a line analogous to Y-Y line in the above-annotated FIG. 9b. *Compare EX1007* at FIG. 9b *with EX1004* at FIG. 4. Specifically, as shown below in FIG. 4 of Sundaram, pads on the first and second electronic device 125, 130 which are "connected with through vias 110," follow the Y'-Y' line, which corresponds to Y-Y in Lin-863 as depicted above. Similarly, when modified per Lin-863, a cross-section of Sundaram's FIG. 4 would reveal the *first region* following

line X'-X', which corresponds to X-X in Lin-863 as depicted above. Thus, Sundaram as modified by Lin-863 teaches *wherein no any copper plug in said first region*.



EX1004 at FIG. 4.

b) Motivation to Combine

274. A POSITA would have found it obvious and been motivated to modify Sundaram's *first region* per Lin-863's *first region* having *no [] copper plugs* to accommodate space for an additional semiconductor chip to be included in Sundaram's package. Specifically, a POSITA would have been motivated to form

an opening in Sundaram's interposer 105 such that an additional chip would be positioned in the chip package, thereby forming a *first region* with *no [] copper plugs* like that in Lin-863's package. A POSITA would have appreciated the additional functionality (i.e., by having more chips) that adding another chip would provide and would have recognized including the additional chip within interposer 105 would have been an efficient use of space, because the overall size of the chip package would not have increased, which would have been desirable to a POSITA, as it was "desirable to minimize thickness of the chip scale package." *EX1068* at [0011]. Additionally, a POSITA would have recognized that by including the additional chip within interposer 105, interconnects between the additional chip and the PWB would be shorter because signals would not have to travel through vias 110 to the other side of interposer 105. A POSITA would have found this advantageous because "shorter interconnects mean it takes less time to process a task, which leads to higher performance" and "reduce[s] power consumption." *EX1072* at 7:61-64.

275. The combination is the application of known technique (no plugs/interconnects in a central region) to a known device (Sundaram's chip package) to yield the predictable results of Sundaram's package having a post-free region where a die is positioned. In the combination, an additional die is positioned in an opening in Sundaram's interposer 105, such that the *first region* has no through

vias 110 (i.e., *no [] copper plugs*). There would have been a reasonable expectation of success for the reasons previously discussed, as well as because methods of controlling plug placement in chip packages were well known and would have merely involved forming through vias 110 only in the *second region*. Further, chip packages having a solid layer with a region with no plugs was well-known, as demonstrated by Lin-863 and others. *See, e.g., EX1073* at FIGS. 6, 8-9, 11:49-51; *EX1127* at FIGS, 1-2, 21M, 22, 7:12-15. Additionally, including a chip in a glass substrate, such as Sundaram's was well-known and methods for producing a chip in a solid substrate, including solid substrates having RDLs, were established, further leading to a reasonable expectation of success. *See, e.g., EX1074* at FIG. 8, [0015], [0023], [0025].

X. OPINIONS REGARDING GROUNDS 1C-D: CLAIM 22 IS OBVIOUS OVER SUNDARAM, LIN-191, AND LIN-691 OR SHENOY

A. *Ground 1C: Lin-691 Teaches Claim 22: "The chip package of claim 18, wherein said first metal layer is a silver-containing layer."*

a) Lin-691's Teachings

276. Shown below, Lin-691 teaches forming a "through-substrate via (TSV)" having a "diffusion barrier layer 54…[that] is blanket formed, covering the sidewalls and bottom of TSV opening 44." *EX1008* at [0019]. "Next, a thin seed layer (not shown) may be blanket formed on diffusion barrier layer 54. *EX1008* at

[0019]. The seed layer may include "metals such as **silver**[.]" *EX1008* at [0019] (emphasis added).

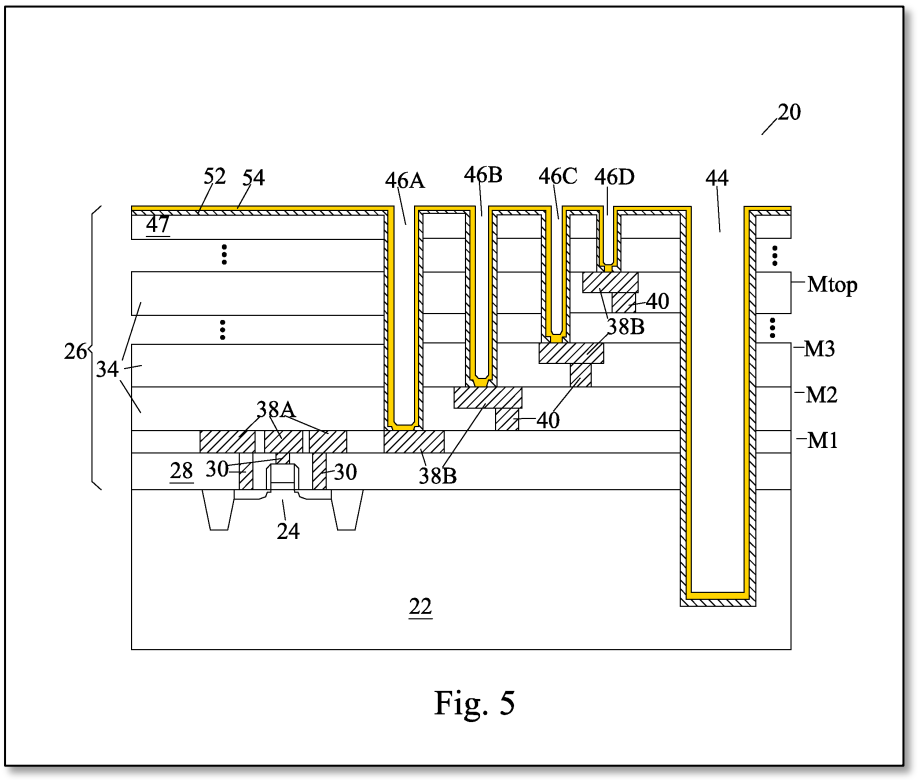


Fig. 5

EX1008 at FIG. 5.

277. "In FIG. 7, a metallic material is filled into openings 44…forming TSV 60[,]" shown below. *EX1008* at [0021]. The "filling material includes copper…" *EX1008* at [0021]. Because the silver seed layer is formed on the diffusion barrier layer 54, then the copper metallic material layer is formed on the thin seed layer, Lin-691's silver seed layer covers the sidewall of the copper portion. That is, Lin-691 teaches forming the diffusion barrier layer 54, then the "not shown" silver seed layer, then the copper portion. *EX1008* at [0019], [0021], FIGS. 5, 7. Because the

copper portion is formed on the silver seed layer, the silver seed layer covers the sidewall of the copper portion, and is, therefore, a *first metal layer [that] is a silver containing layer*. Further, Lin-863's TSV is formed on a "[p]assivation layer 47 [that] may be…un-doped silicate glass," i.e., a similar material to Sundaram's interposer 105 where through via 110 is formed.

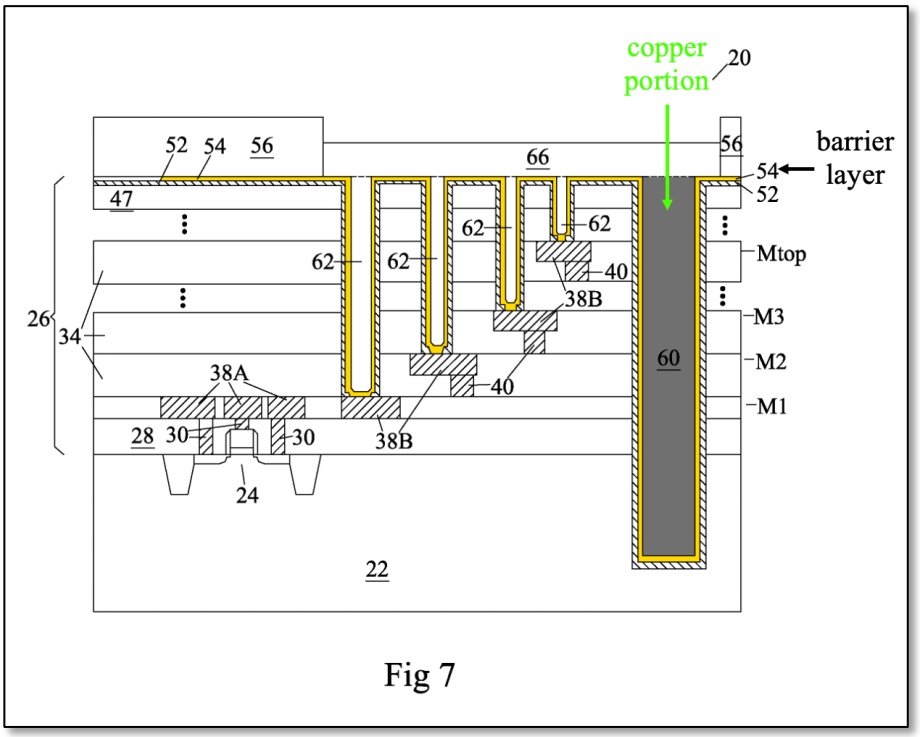


Fig 7

EX1008 at FIG. 7, [0015].

b) Motivation to Combine

278. As discussed in Claim 18(d)(i), Sundaram's through vias 110 comprise a *first metal layer* that is a Cu seed layer. *See* Claim 18(d)(i). A POSITA would have been motivated to and found it obvious to modify the Sundaram's *metal conductor*

such that the Cu *first metal layer* was instead silver (a *silver-containing layer*). Specifically, a POSITA would have appreciated that the improved current distribution provided by silver (as opposed to copper) during subsequent electroplating of the copper through via 110. A silver seed layer would provide a more uniform distribution of plating current than a Cu seeding layer because it has a higher electrical conductivity than Cu, thereby resulting in a more uniform electroplated copper layer. *EX1075* at [0050] ("…the electrical conductivity of silver is highest of all metals."). It was known that "non-uniform nucleation at the seed layer during a plating process" may cause "voids," which as I described above may cause increased resistance and "result in poor reliability." *EX1076* at [0011]; *EX1063* at 3:12-16; ¶ 240. Further, "voids and/or non-uniform deposition" may result in "poor electromigration resistance" and "cause an open circuit." *EX1076* at [0012]. Accordingly, a POSITA would have been motivated to mitigate risks associated with void formation by implementing a silver seed layer (a *silver-containing layer*) such that a more uniform Cu through via 110 would be formed. Additionally, silver adheres more strongly to polymers and glass compared to Cu, resulting in overall better mechanical properties for the plated layer (e.g., reduced risk of delamination).

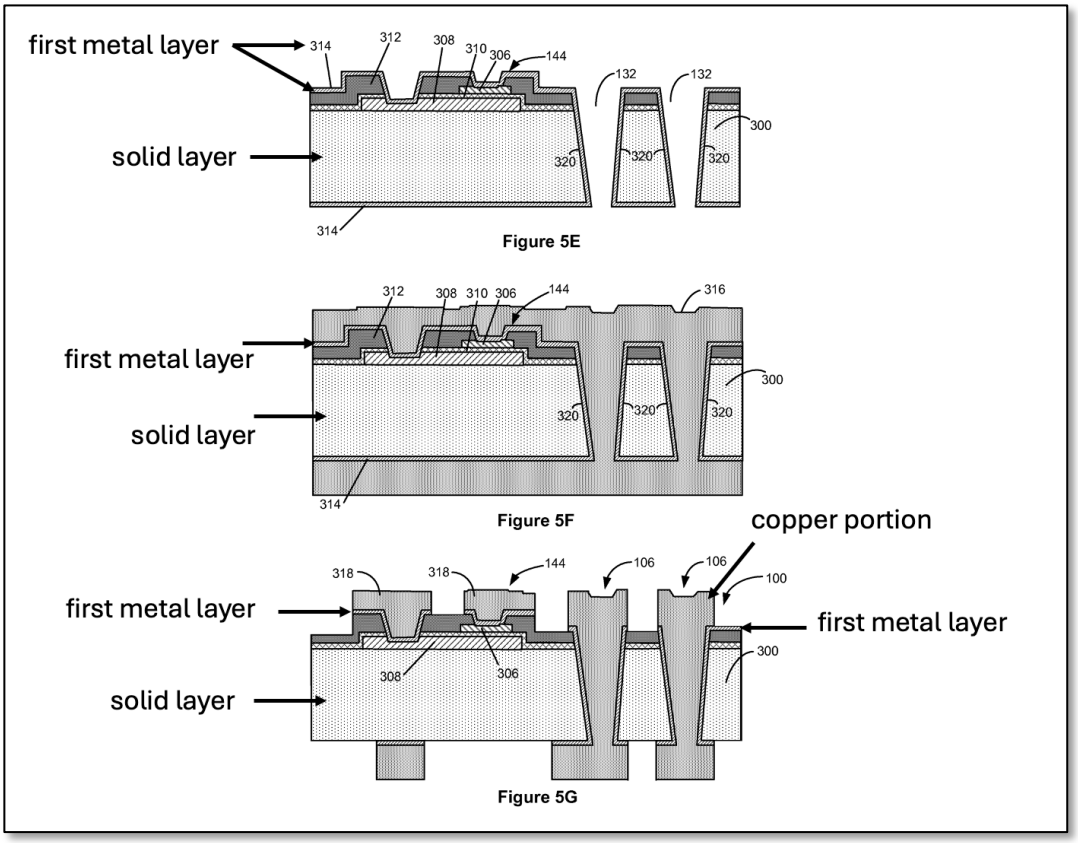
279. The modification is the application of a known technique (Lin-691's silver seed layer) to a known device (the Sundaram's through via 110) ready for

improvements to yield the predictable results of the post being formed with a silver seed layer. Additionally, or alternatively, the modification is the simple substitution of Lin-691's silver seed layer for Sundaram's copper seed layer to obtain the predictable result of Sundaram's *metal conductor* having a silver layer covering the sidewalls of a copper portion. There would have been a reasonable expectation of success because the use of a silver seed layer was well known before the '763 Patent, as demonstrated by Lin-691, and involved routine manufacturing processes, such as "sputtering". *EX1008* at [0019]; *EX1077* at FIG. 2, 3:9-12, 3:47-50; *EX1043* at [0032]. ("The metal-containing wetting film 104 may be deposited by a variety of different deposition methods known by one of ordinary skill in the art, including …sputtering methods.").

B. *Ground 1D: Shenoy Teaches Claim 22: "The chip package of claim 18, wherein said first metal layer is a silver-containing layer."*

280. Shenoy teaches "a glass substrate" with "through-glass via holes," which has "exposed surfaces of the metal layers 306 and 308, and the passivation layer 312 [] conformally coated with a seed layer 314" that includes "Ag." *EX1011* at [0053-0055]. Shenoy thus teaches a *silver-containing layer*. A "plated metal 316 fills the through-glass via holes 132…and covers the conformal seed layer 314" and "can include Cu[.]" *Id.* Additionally, because Shenoy teaches filling "through-glass

via holes" with copper, Shenoy's TGV is analogous to Sundaram's through vias 112 that are similarly "metalized with…copper." *EX1011* at [0053-0055]; *EX1004* at 6:25-27.



EX1011 at FIGS. 5E-5G.

281. A POSITA would have been motivated, found it obvious, and had a reasonable expectation of success for the same reasons discussed above. *See* ¶¶ 278-279, incorporated herein. Additionally, because Shenoy, like Sundaram teaches through glass vias, a POSITA would have had a reasonable expectation of success. Specifically, a POSITA would have recognized that because Shenoy teaches

forming a via in glass substrate and forming a *silver-containing layer* therein, that a *silver-containing layer* would also be successfully formed in Sundaram's through vias 110, which are similarly formed in a glass substrate (i.e., interposer 105). *EX1004* at 2:22-27, 5:54-58.

XI. OPINIONS REGARDING GROUND 2A: CLAIMS 1-5, 7-12, 14-15, 17 ARE OBVIOUS OVER YU AND LIN-191

A. *Claim 1*

1. 1(Pre): "A chip package comprising"

282. Yu teaches a "package 202" that "compris[es] a first die encased in [a] molding compound, a second die on a back side of the **package**, and a third die on a front side of the package…. The package 202 can be the package formed in FIG. 17[.]" *EX1010* at 8:7-13. The semiconductor dies are "a logic circuitry die, a memory die, or any other die" (i.e., are semiconductor *chip[s]*) *EX1010* at 2:50-51. Accordingly, Yu expressly teaches a *chip package*, namely package 202 comprising semiconductor dies:

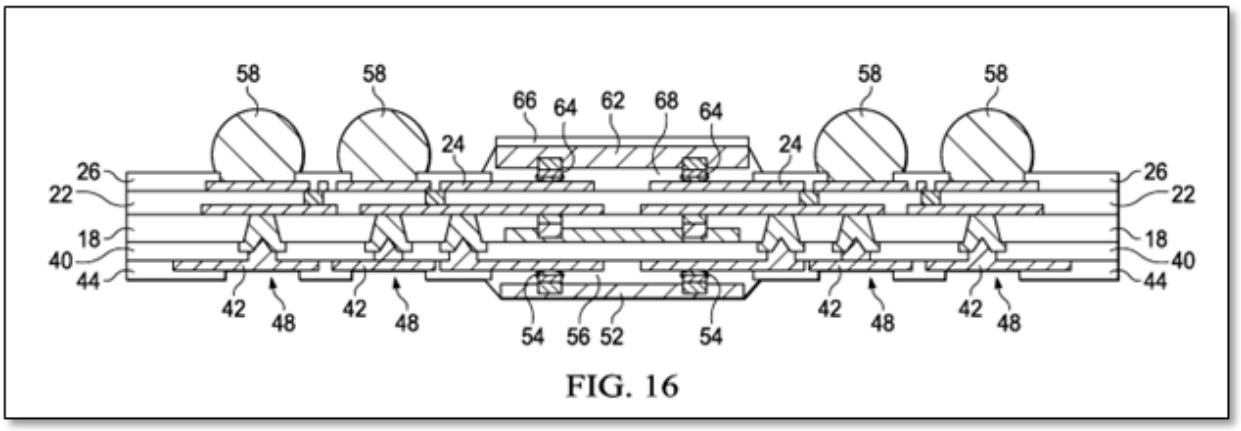


FIG. 16

EX1010 at FIG. 16. I note that FIG. 17 is the same as FIG. 16 except that "connectors 58 are probed using pins" in FIG. 17. *EX1010* at 5:3-5.

2. 1(a): "a solid layer having a first surface and a second surface opposite to said first surface,"

283. As shown below, Yu's package 202 includes "molding compound 18 [that] can be [] epoxy, polyimide, silicone rubber, the like, or a combination thereof," i.e., *a solid layer*. *EX1010 at* 2:61-64. Molding compound 18 has *a first surface opposite* to *a second surface*. Yu identifies molding compound 18 as part of package 202 and depicts the molding compound 18 as a defined, solid region surrounding the internal components of the package. As shown in Yu's FIG. 16, molding compound 18 includes opposing surfaces, *a first surface opposite and a second surface opposite to said first surface*, that bound the *solid layer*.

284. Thus, Yu's molding compound 18 (*solid layer*) comprises *a first surface and a second surface opposite to said first surface*.

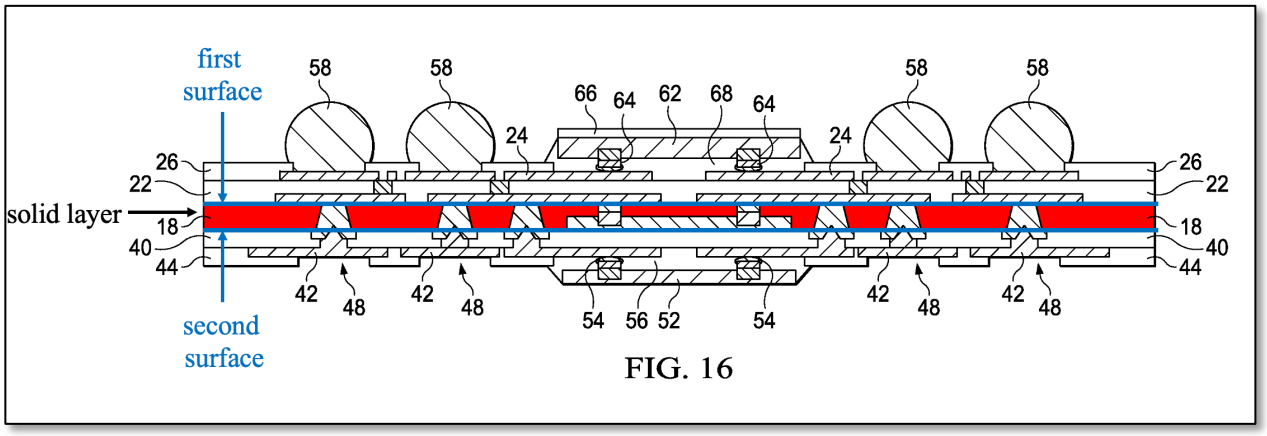


FIG. 16

EX1010 at FIG. 16.

3. 1(a)(i): "wherein said first surface is substantially parallel to said second surface,"

285. As shown, the *first surface is substantially parallel to said second surface*:

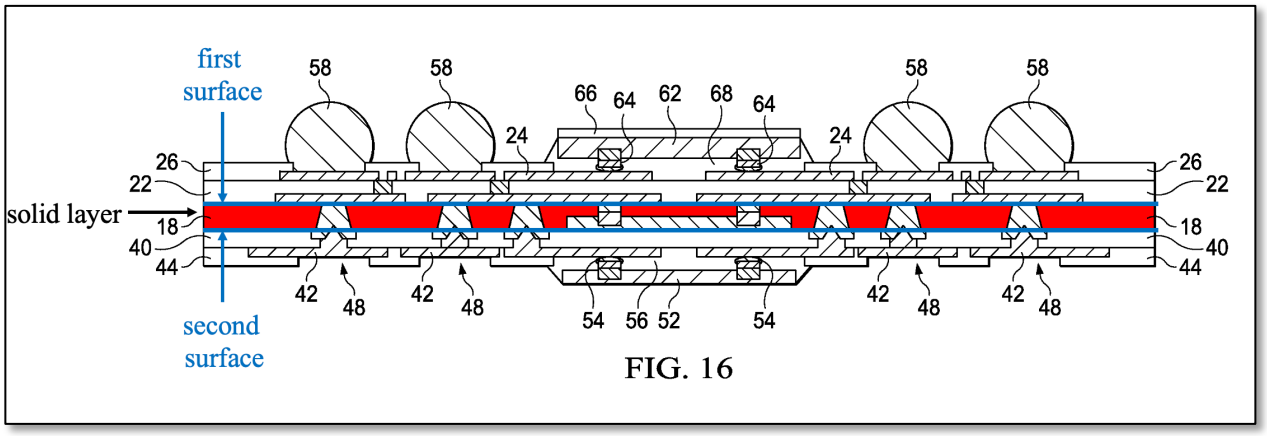


FIG. 16

EX1010 at FIG. 16.

4. 1(a)(ii): "wherein said solid layer comprises a compound of silicon and oxygen,"

286. Molding compound 18 comprises "silicone rubber," which is *a compound of silicon and oxygen. EX1010* at 2:61–65. Silicone rubber is a polymeric material known in the art to be a type of polysiloxane having a "siloxane backbone of repeating Si–O–Si units." *EX1060* at 6:10-17. Accordingly, Yu's molding compound 18, which comprises silicone rubber, is a *solid layer comprising a compound of silicon and oxygen* (i.e., Si-O-Si). Yu further teaches that molding compound 18 comprises "epoxy, polyimide, silicone rubber, the like, or a combination thereof," such that silicone rubber alone or silicone rubber in combination with epoxy and/or polyimide teaches *a compound of silicon and oxygen*. *EX1010* at 2:61-65.

5. 1(a)(iii): "wherein said solid layer has a thickness between 100 and 300 micrometers,"

a) Lin-191's Teachings

287. Lin-191 teaches an "encapsulating layer 85" formed "on top[] of the metal pillars or bumps 14," which correspond structurally to conductive vias or posts such as Yu's TMVs (discussed further at Claim 1(b)). *EX1005* at [0109]. Lin-191 explains that the encapsulating layer 85 covers the bumps and the surrounding regions of the substrate to protect and planarize the device structure. *Id*. Because encapsulating layer 85 includes "a polymer layer," it constitutes a solid layer similar

to Yu's molding compound 18, which likewise encapsulates conductive structures within a solid layer. *Id*.

288. Lin-191's encapsulating layer 85 has a thickness "between about 20 and about 500 micrometers." Similar to my opinions provided for Sundaram for Ground 1A (¶¶ 133-135), Lin-191 teaches or renders obvious the claimed *thickness between 100 and 300 micrometers*. *EX1005* at [0109]-[0111]. Because Lin-191 teaches a range ("between about 20 and about 500 micrometers") that includes the narrower claimed range of *between 100 and 300 micrometers*, Lin-191 teaches or renders obvious Claim 1(a)(iii).

289. Additionally or alternatively, Lin-191's encapsulating layer 85 has a *thickness* equal to the combined thickness of layers 1 and metal pillars or bumps 14. Encapsulating layer 85 is "formed…on the metal layer 13 of the patterned metal layer 1," and "top surfaces 14a" of bumps 14 are "substantially coplanar…with a top surface 85a" of layer 85. *EX1005*, [0109-0110], FIG. 12. Thus, as can be seen in FIG. 21 below, encapsulating layer 85's thickness is equivalent to that of layer 1 plus bump 14. Indeed, Lin-191 teaches layer 85 is "ground or polished" such that "top surfaces 14a of" pillars 14 and "top surfaces 24a" of bumps 24 "are substantially coplanar with…a top surface 85a" of encapsulating layer 85. *EX1005* at [0110]. Pillars 14 have a thickness "between 20 and 110 micrometers[.]" *EX1005* at [0121].

Additionally, pillars 14 are on layer 1, which is formed of adhesion layer 11, seed layer 12, and metal layer 13. *EX1005* at [0075], FIG. 21. Layer 11 has a thickness "less than 1 micrometer, such as between 1 nanometer and 0.5 micrometers," layer 12 has a thickness "less than 1 micrometer, such as between 10 nanometers and 0.8 micrometers," and layer 13 has a thickness "between 3 and 10 micrometers." *EX1005* at [0050], [0060]. Thus, layer 1 plus pillar/bump 14 has a thickness of, at most, 121.3 micrometers (0.5 + 0.8 + 10 + 110) or at least 23.011 micrometers (0.001 + 0.01 +3 + 20). Because layer 85's thickness is the same as the combined thickness of pillars 14 and layer 1, layer 85 thus also has a maximum thickness of 121.3 micrometers, or a minimum thickness of about 23.011 micrometers. *EX1005* at [0050]. Thus, a POSITA would have understood that Lin-191's encapsulating layer 85, like Yu's molding compound 18, is a polymeric solid encapsulant layer of comparable structure and function, disposed over the metal pillars 14 and having a thickness between 23.011 micrometers and 121.3 micrometers, thus teaching or rendering obvious a *thickness between 100 and 300 micrometers*.

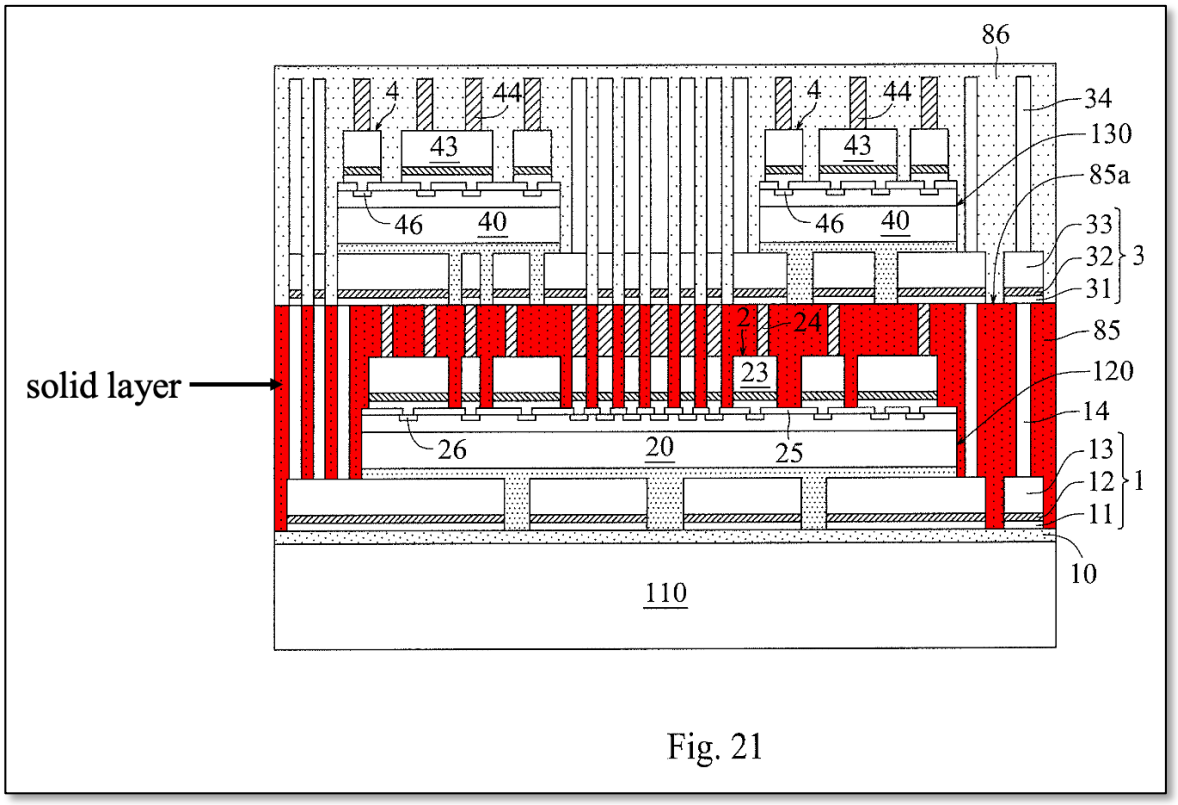


Fig. 21

EX1005 at FIG. 21.

290. Similar to my opinions provided at ¶ 135, I note that the '763 Patent does not indicate any specific criticality for the claimed range. Therefore, for the reasons provided here and in ¶ 135, it is my opinion a POSITA would have found the claimed range taught or obvious.

b) Motivation to Combine

291. A POSITA would have been motivated to apply Lin-191's thickness to Yu's molding compound 18. The modification would have given Yu's molding compound 18 stress buffering capabilities as polymer layers (such as Yu's molding

compound 18) having a thickness "between about 30 μm and about 200 μm" (overlapping with Lin-191's and the claimed range) were known to "act[] as an efficient stress buffer." *EX1080* at [0018]. Stress buffering provided by Yu's molding compound 18 would have been advantageous for a variety of reasons.

292. First, stress buffering provided by Yu's compound 18 and Lin-191's thickness would be beneficial for protecting Yu's die 10 that is in molding compound 18. *EX1010* at 2:61-63, FIG. 2. As demonstrated by Lin-191, the thickness is appropriate for an embedded chip, as encapsulating layer 85 covers chip 120. *EX1005* at FIG. 21. Given that Yu similarly embeds a die 10 in molding compound 18, a POSITA would appreciate that Lin-191's solid layer thickness would apply to Yu's *solid layer*. Given that solid layers with the claimed thickness were known for embedding chips and buffering stress, a POSITA would appreciate the Yu's die 10 would be protected from stress by molding compound 18, thereby reducing the likelihood of stress-induced damage to die 10. *EX1080* at [0018]. Further, molding/encapsulation layers at the claimed thickness were known to environmentally protect embedded die from "external elements and contaminants." *EX1131* at [0046]; ¶ 54.

293. Additionally, Lin-191's thickness would allow for the opportunity to incorporate metal shielding into Yu's molding compound 18 (*solid layer*) which

would reduce electromagnetic interference (in the chip package. EMI negatively impacts signal quality in chip packages such that a POSITA would have found the opportunity to prevent EMI-induced signal degradation. Indeed, ICs were known to "radiate a relatively large amount of electromagnetic energy" that may "interfere with the operation of other devices or circuits in the vicinity of the radiating IC" which prompted the use of "electromagnetic interference (EMI) shielding layer[s]." *EX1136* at 1:28-37, 2:28-30. Such shielding layers were known to be incorporated within and between dielectric layers such that a POSITA would have recognized applying Lin-191's thickness to Yu's molding compound 18 would have advantageously provided the opportunity for such shielding in Yu's package. *See, e.g., EX1137* at 6:1-10, 3:38-41, FIGS. 6-7 (providing a metal power plane 61 (i.e., a shielding layer) that "eliminates crosstalk" within dielectric layers 67, 68).

294. The combination is the application of a known technique (an encapsulant thickness) to a known device (Yu's molding compound 18) ready for improvement to yield predictable results. A POSITA would have had a reasonable expectation of success in applying Lin-191's solid layer thickness to Yu's compound 18 because the range was a common thickness for molding layers in chip packaging before the '763 Patent. *See* ¶¶ 51-54. Additionally, Lin-191's encapsulating layer 85 is, like Yu's molding compound 18 (*solid layer*) formed by a "molding process[.]"

EX1005 at [0109]; *EX1010* at 2:65-66 ("The molding compound 18 can be applied using…compression molding."). Because Lin-191's and Yu's solid layers are formed using the same process, a POSITA would have had a reasonable expectation of success in using Yu's molding process to form molding compound 18 according to Lin-191's layer 85 thickness.

6. 1(a)(iv): "wherein said solid layer comprises a first region and a second region between said first region and an edge of said solid layer;"

295. Shown below, Yu's molding compound 18 (*solid layer*) comprises a *first region* (green) and a *second region* (blue). The *second region* is *between said first region and an edge* (indicted by the purple line) *of said solid layer*:

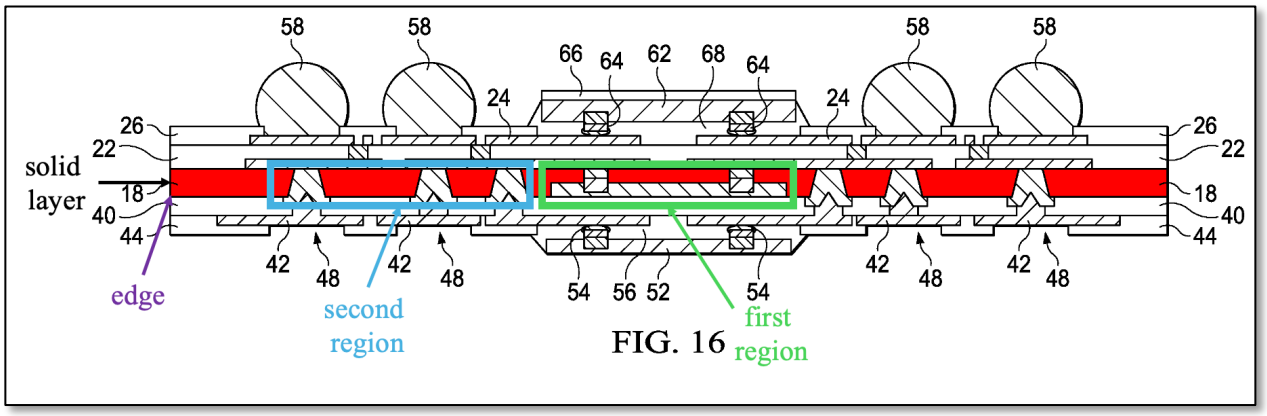


FIG. 16

EX1010 at FIG. 16.

7. 1(b): "a plurality of copper plugs in a plurality of through vias in said second region of said solid layer respectively,"

296. Yu teaches that "TMV [through molding via] openings 36 are formed through the molding compound 18," and that "a seed layer is deposited … into the TMV openings 36," followed by deposition of a "conductive material." *EX1010* at 3:56–4:6. Yu further teaches that both the seed layer and the conductive material are copper, thereby forming copper-filled through vias within the molding compound. *Id.* As a result, the TMVs 38 shown in Yu correspond to a *plurality of copper plugs* extending through the molding compound 18, each positioned within a corresponding TMV opening 36. The copper seed and conductive layers together form solid metallic structures within the through holes, yielding *a plurality of copper plugs in a plurality of through vias*, i.e., the TMV openings 36. These through vias are located in the *second region*, as depicted in Yu's figure below, which illustrates TMVs 38 formed in molding compound 18 in *said second region*.

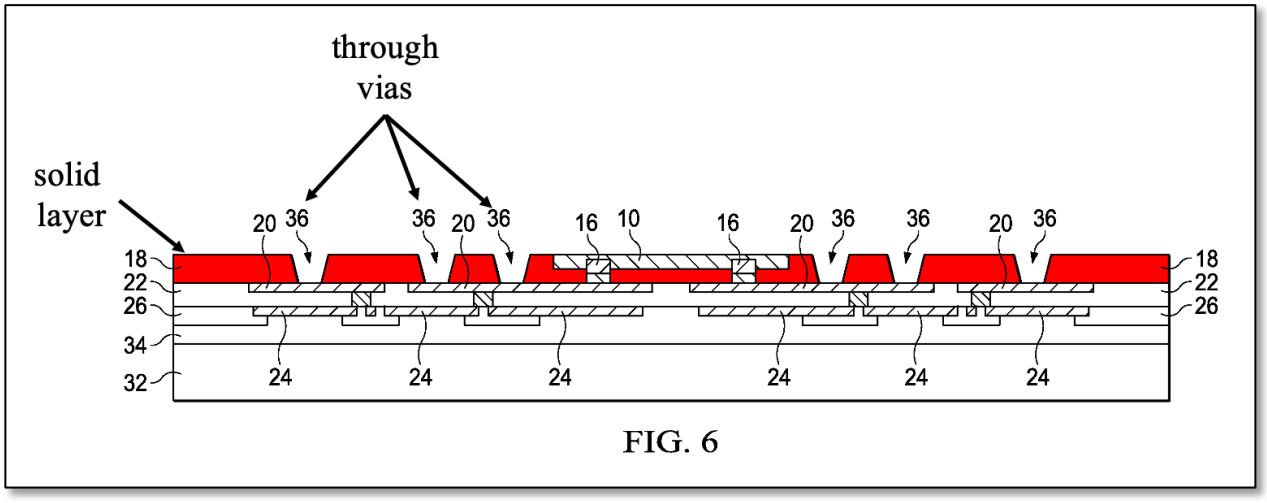


FIG. 6

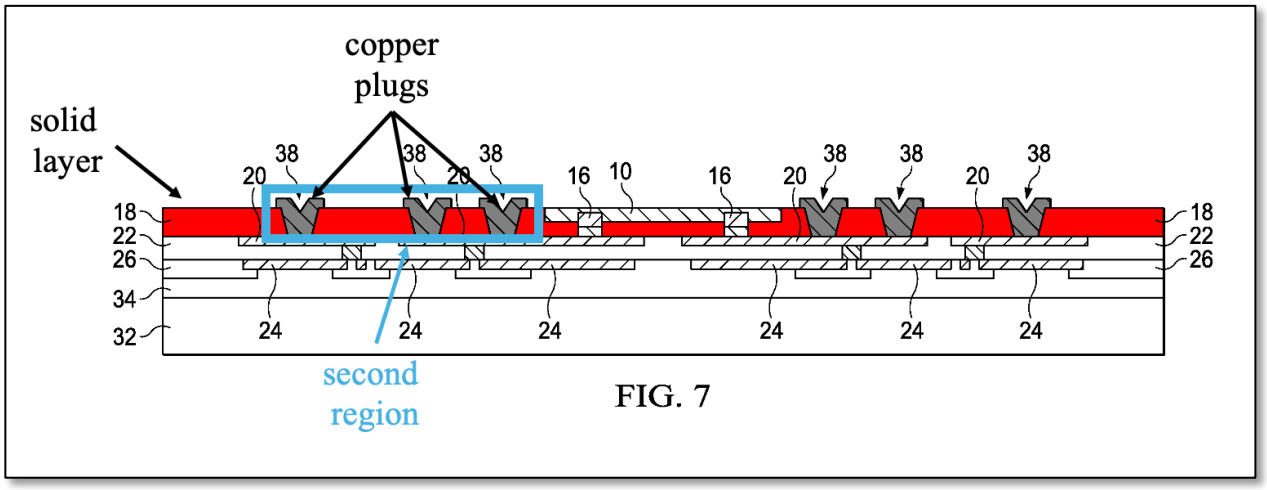


FIG. 7

EX1010 at FIGS. 6-7.

8. 1(b)(i): "wherein one of said plurality of copper plugs comprises a first copper layer contacting a sidewall of one of said plurality of through vias,"

297. Yu teaches that a "seed layer is deposited … into the TMV openings 36," and further identifies the seed layer material as copper. *EX1010* at 3:60–64. In Yu, the TMV openings 36 extend through the molding compound 18 to expose the surfaces of underlying conductive regions, and the deposition of the copper seed layer coats the interior surfaces of those openings. *EX1010* at 2:64-3:19; 10:29-33. Thus, the deposited copper seed layer forms a copper layer that contacts the sidewalls of the TMV openings 36. In this way, a copper seed layer of the *copper plugs* is *a first copper layer contacting a sidewall of one of said plurality of through vias*. The copper seed layer forms the conductive base upon which additional copper material is subsequently plated to fill the TMV openings 36.

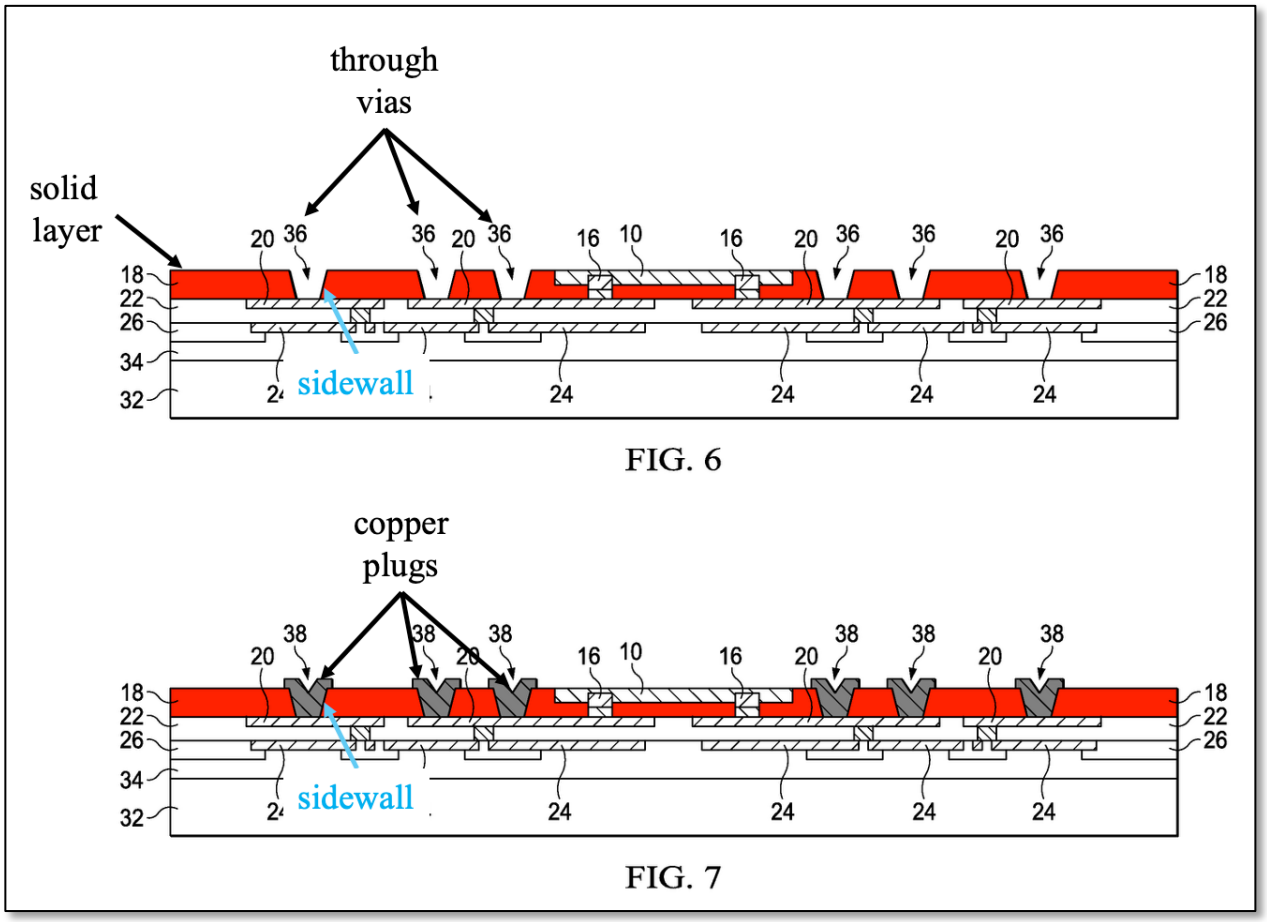


FIG. 6

FIG. 7

EX1010 at FIG. 6.

298. I note that Yu's teachings mirror Patent Owner's statements during original prosecution in the related '768 Patent, where FIG. 17B is annotated to state "A Cu layer of the metal plug contacts with a sidewall of the through via." *EX1032* at p. 537.

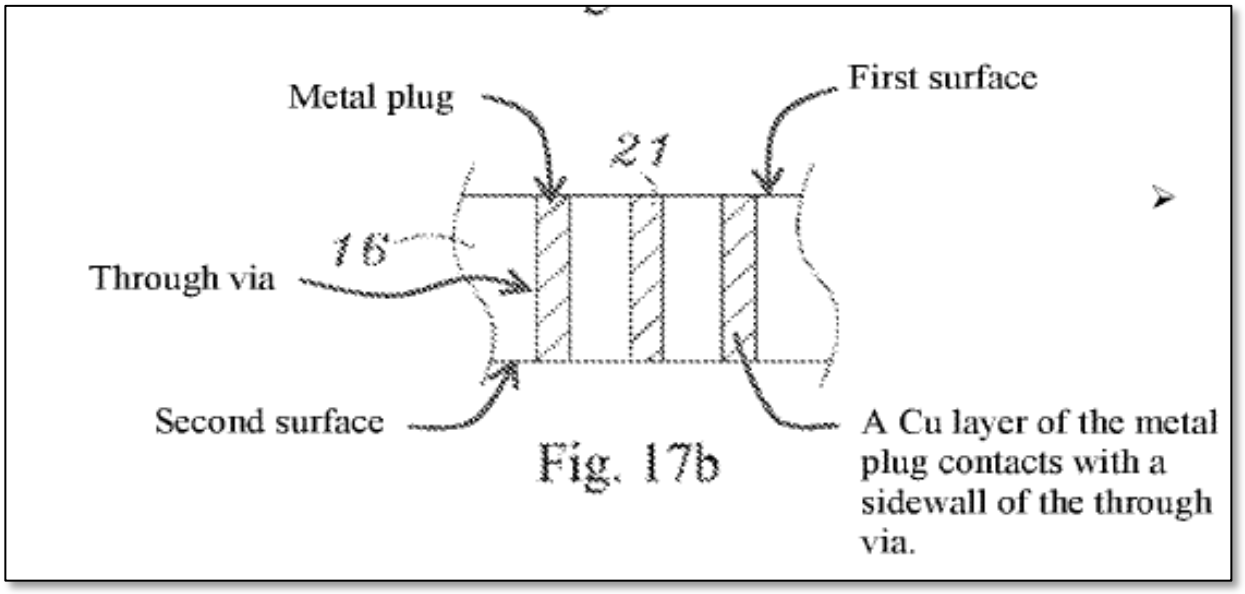


Fig. 17b

EX1032 at p. 537.

9. 1(b)(ii): "wherein said first region has a width in a direction greater than a shortest distance between said sidewall of one of said plurality of through vias and said edge of said solid layer in said direction and greater than a pitch between two neighboring copper plugs of said plurality of copper plugs;"

299. As shown below in FIG. 16, Yu's *first region has a width in a direction* (denoted D1) *greater than a shortest distance between said sidewall of one of said plurality of through vias and said edge of said solid layer in said direction* (denoted D2), and *greater than a pitch between two neighboring copper plugs* (denoted D3) *of said plurality of copper plugs*.

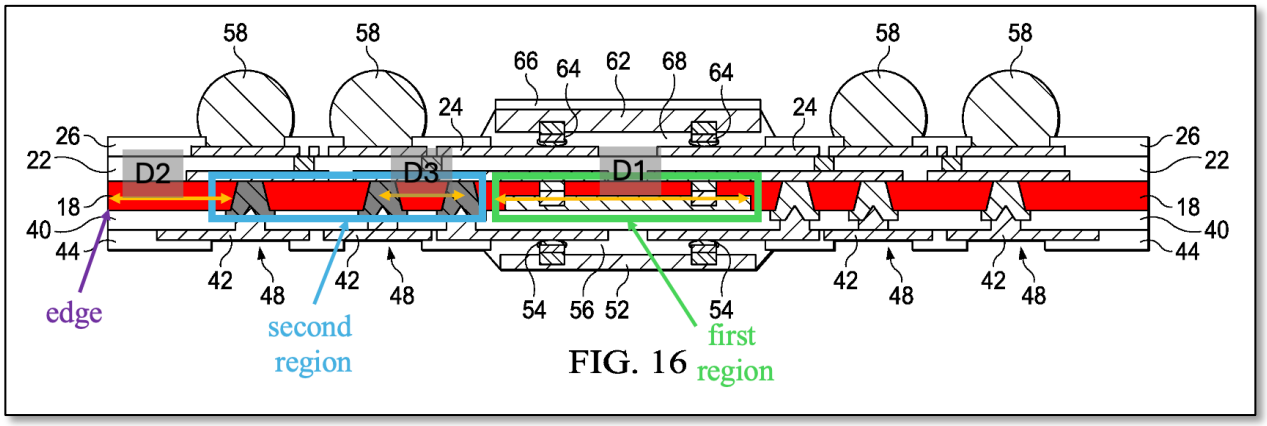


FIG. 16

EX1010 at FIG. 16.

300. I note that annotated FIG. 6l provided by PO during original examination is below, which PO argued illustrates the claimed *width*, *shortest distance*, and *pitch*. As shown above, Yu's *first* and *second* regions mirror this arrangement. The claimed *regions* are not described in the '763 Patent's written description. Applicant relied solely on Applicant-annotated FIG. 6l.

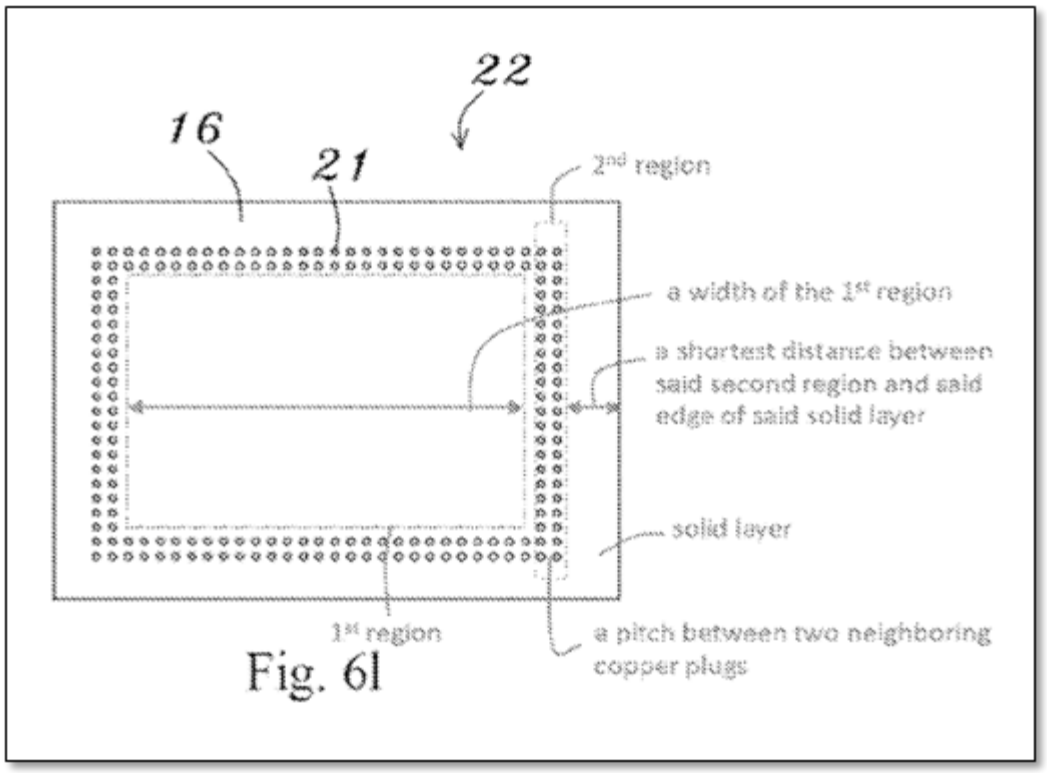


Fig. 6I

EX1002 at p. 272.

10. 1(c): "a first interconnection scheme over said first surface,"

301. Yu teaches a "front side interlayer dielectric (ILD) and redistribution layer (RDL) structure." *EX1010* at 3:4-5. In particular, a seed layer is deposited on the molding compound 18 and patterned to form a "first front-side metallization layer 20." *EX1010* at 3:5-19. A "first ILD layer 22" is then deposited over layer 20 and subsequent metallization and ILD layers are formed, including a second metallization layer 24 and a second ILD layer 26, with openings 28 and 30 formed in the topmost front-side ILD for connectors. *EX1010* at 3:4-19. These layers are all

on the molding compound 18 and constitute a *first interconnection scheme* over the *first surface*. *EX1010* at 3:4-19 (front-side ILD/RDL over molding compound 18; first metallization layer 20), 3:20-27 (first ILD layer 22), 3:28-43 (subsequent metallization/ILD including layers 24 and 26; openings 28, 30).

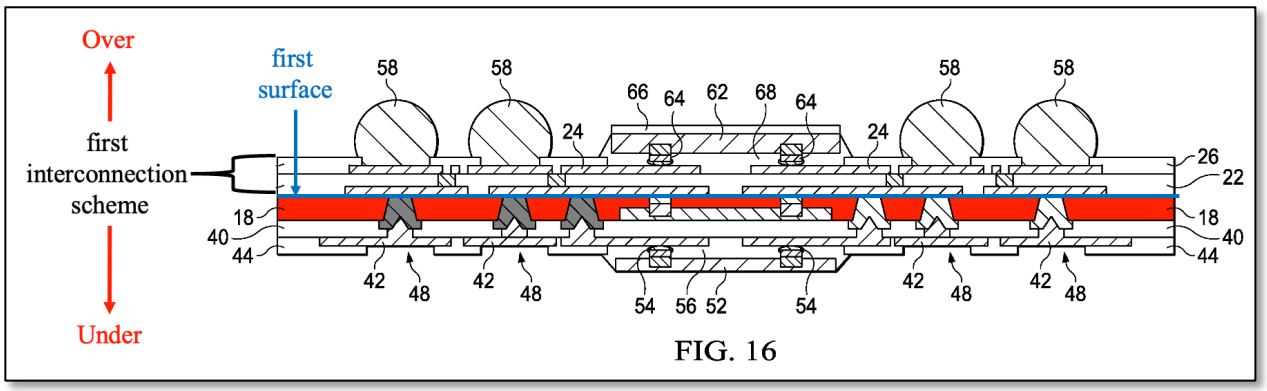


FIG. 16

EX1010 at FIG. 16. I note that metallization layer 20 is assigned a reference numeral in FIGS. 4-7 and 10-11 which depict steps of forming the package 202 of FIG. 16, while the reference numeral for layer 20 in FIG. 16 above is omitted. *See, e.g.,*

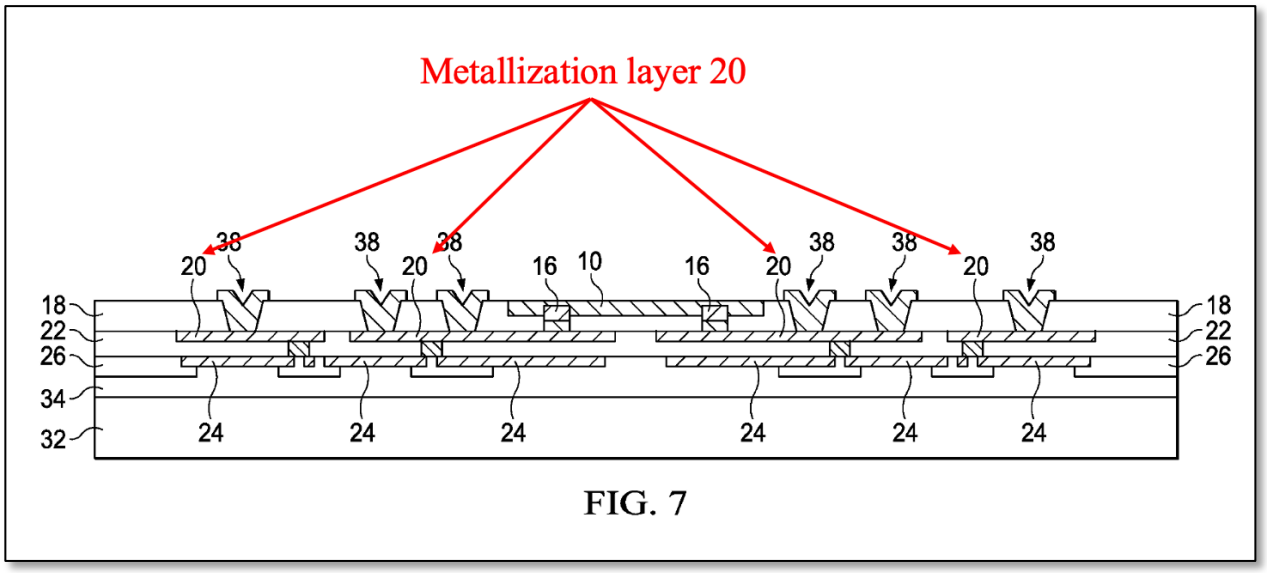


FIG. 7

EX1010 at FIG. 7.

11. 1(c)(i): "wherein said first interconnection scheme comprises a first metal interconnect over said first surface, a second metal interconnect over said first surface and a first polymer layer over said first and second metal interconnects,"

302. Yu teaches that "a seed layer, such as a copper" is "deposited on the molding compound 18" then a "[c]onductive material of the first metallization layer, such as copper… is deposited on the exposed seed layer." *EX1010* at 3:8–18. Yu further explains that "the remaining conductive material forms the first front-side metallization layer 20." *EX1010* at 3:18–20.

303. Because metallization layer 20 comprises copper, a portion of metallization layer 20 is a *first metal interconnect* and is disposed over the *first surface* of the molding compound 18 (*solid layer*), as shown below. Another portion of metallization layer 20 is a *second metal interconnect*.

304. Yu further teaches that "a first ILD layer 22 is deposited on the front side and over the first metallization layer 20. The first ILD layer 22 may be a polyimide, polybenzoxazole (PBO), benzocyclobutene (BCB), the like, or a combination thereof." *EX1010 at* 3:21–27. Thus, ILD layer 22 comprises a polyimide and is a *first polymer layer* formed over metallization layer 20. Accordingly, Yu's *first polymer layer* is *over said first and second metal*

interconnects. The *first polymer layer* at least includes ILD layer 22 but may also include ILD layer 26 (*see* Claim 14, ¶ 353).

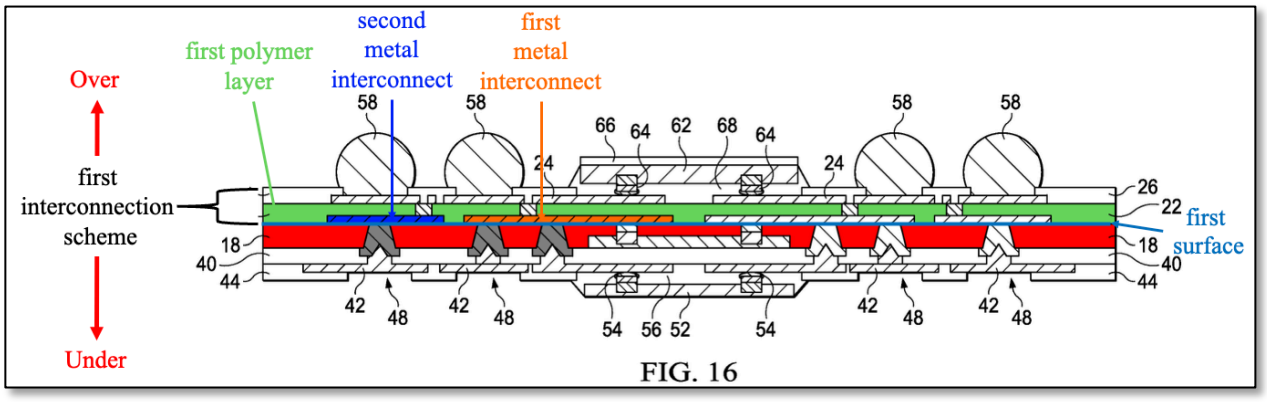


FIG. 16

EX1010 at FIG. 16.

305. Alternatively, ILD layer 26 alone, which also comprises "polyimide," is a *first polymer layer over said first and second metal interconnect*. *EX1010* at 3:20-32.

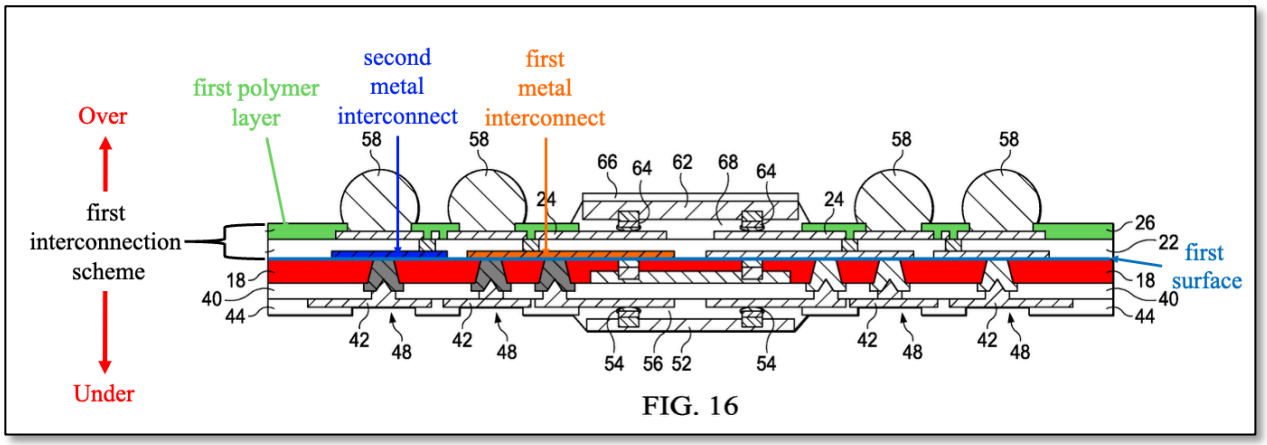


FIG. 16

EX1010 at FIG. 16.

12. 1(c)(ii): "wherein said first metal interconnect is connected to a first copper plug of said plurality of copper plugs, wherein said second metal interconnect is connected to a second copper plug of said plurality of copper plugs,"

306. As shown below, Yu teaches that "TMV [through molding via] openings 36 are formed through the molding compound 18 to the first front side metallization layer 20," followed by deposition of a seed layer and electroplating of a conductive material such as copper to form TMVs 38. *EX1010* at 3:5-19. The TMVs 38 extend through the molding compound 18 and make electrical contact with the first front-side metallization layer 20. Accordingly, metallization layer 20 (*first metal interconnect*) is *connected to a first copper plug of said plurality of copper plugs*. In other words, because Yu teaches that the TMV openings 36 are formed to the first front-side metallization layer 20 and subsequently filled with copper to form TMVs 38 in contact with that layer, the *first copper plug* is *connected to* the *first metal interconnect*. For the same reasons, the *second metal interconnect is connected to a second copper plug of said plurality of copper plugs*.

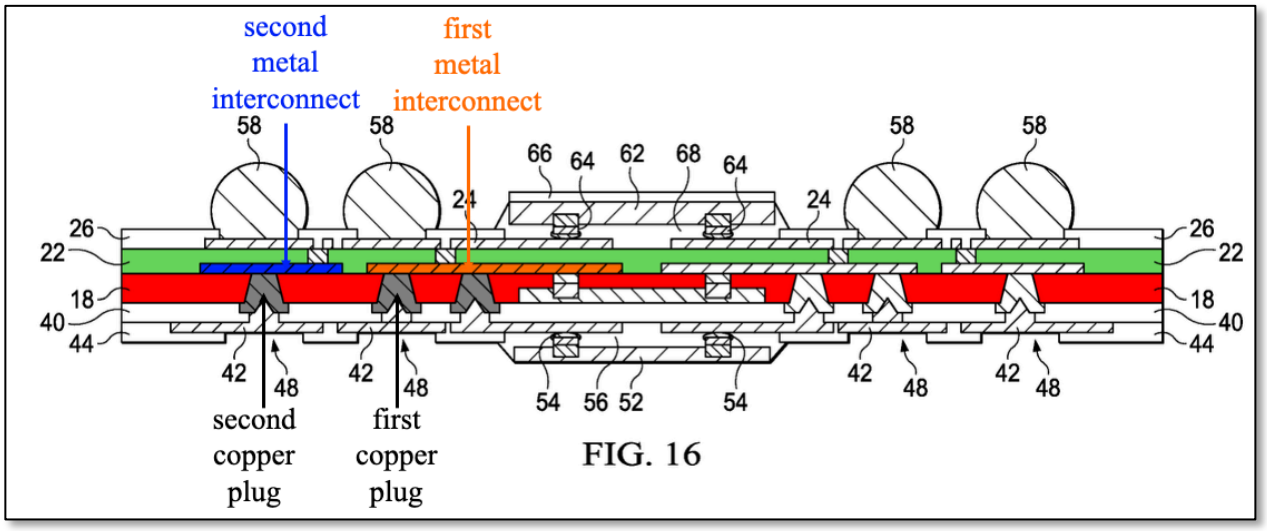


FIG. 16

EX1010 at FIG. 16.

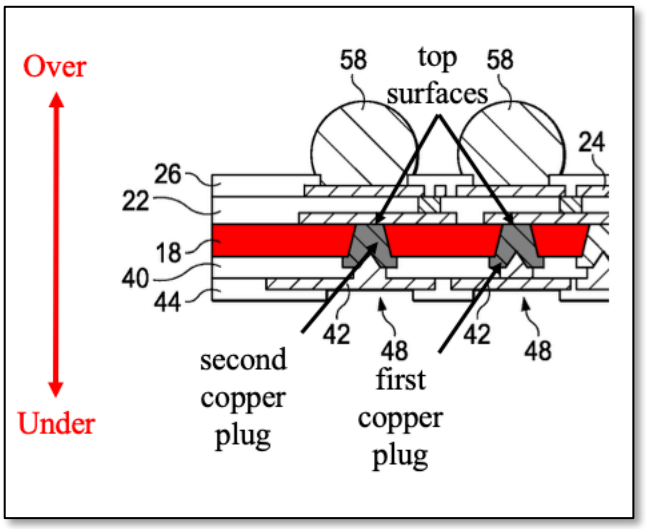
13. 1(c)(iii): "wherein said first metal interconnect comprises a first metal layer and a second copper layer over said first metal layer;"

307. Yu teaches "a front side interlayer dielectric (ILD) and redistribution layer (RDL) structure." 3:4-5. To from the RDL, a "seed layer, such as copper…is deposited on the molding compound 18" then "conductive material of the first metallization layer, such as copper…is deposited on the exposed seed layer, such as by…electroplating" *EX1010* at 3:5–14. Yu further explains that the remaining conductive material forms "the first front side metallization layer 20." *EX1010* at 3:18–20. Thus, metallization layer 20 includes a copper seed layer deposited directly on the molding compound 18 and a copper conductive layer deposited on top of the seed layer. Accordingly, the copper seed layer is *a first metal layer*, and the copper

conductive material plated on the seed layer is *a second copper layer over the first metal layer*.

14. 1(c)(iv): "wherein a top surface of said second copper plug and a top surface of said first copper plug are substantially in the same horizontal plane;"

308. As shown below, the *first* and *second copper plug[s]* comprise *top surface[s]* that *are substantially in the same horizontal plane*. The top surfaces are *in the same horizontal plane* because each top surface is coplanar with the top surface of molding compound 18.



EX1010 at FIG. 16.

15. 1(d): "a first metal bump over said first interconnection scheme"

309. Yu teaches that "conductive connectors 58, such as ball grid array (BGA) balls," are "formed on the front side of the package in the openings 28," and

are "formed on [] bond pads." *EX1010* at 4:45–49. Yu further explains that the openings 28 are formed through the topmost ILD layer 26 to expose portions of the "topmost front-side metallization layer, such as the second metallization layer 24," to which the connectors are electrically coupled. *Id*. at 3:31–36. Yu also teaches that the conductive connectors 58 may be "a lead-free solder" (*metal bump*) and "may be formed on the bond pads." *Id*. at 4:47–50. These connectors 58 are positioned on the front side of the package above the multilayer ILD/RDL stack, including metallization layers 20 and 24 and ILD layers 22 and 26, that together form the *first interconnection scheme*.

310. Accordingly, connector 58 is *a first metal bump over said first interconnection scheme*, because Yu expressly teaches that conductive connectors (BGA balls) 58 are formed on the front side of the package and in electrical contact with the upper metallization layer of the interconnection structure. Alternatively, connector 58 together with its underlying bond pad collectively form *a first metal bump over said first interconnection scheme*.

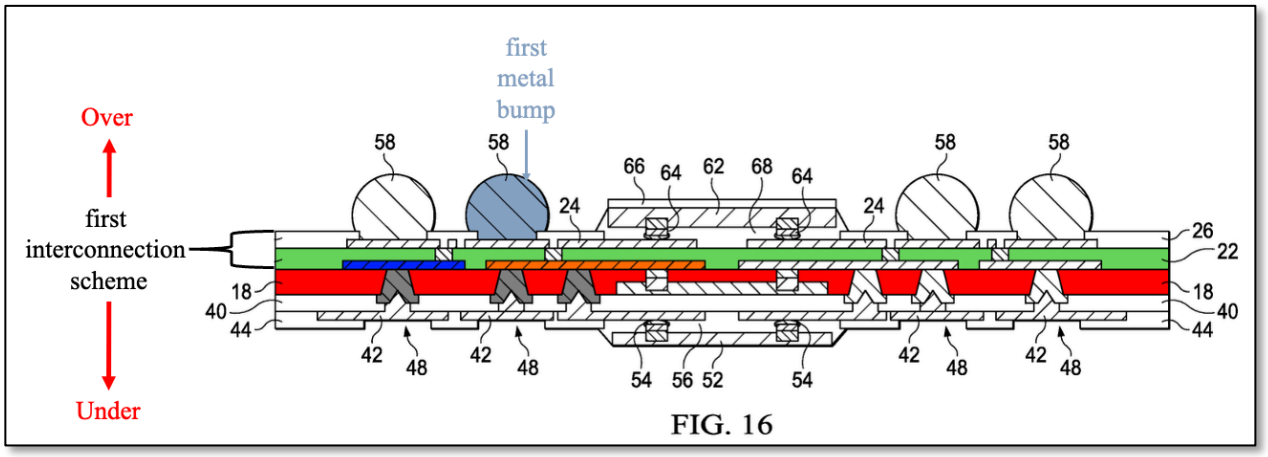


FIG. 16

EX1010 at FIG. 16.

16. 1(d)(i): "wherein said first metal bump comprises a second metal layer and a tin-containing layer over said second metal layer; and"

311. Yu teaches that "connectors 58 may be a lead-free solder." *EX1010* at 4:47–50. Yu further explains that the connectors 58 are "formed on the front side of the package in the openings 28" and "formed on [] bond pads," thereby showing that the solder connectors 58 are disposed over and electrically connected to the upper metallization layer of the front-side interconnection structure. *Id*. at 4:45–49.

312. A POSITA would have understood (A) the bond pad to be metal, as metal bond pads were, and remain, ubiquitous in semiconductor packaging for connecting solder balls to underlying redistribution layers, and (B) the "lead-free solder" to include tin, since tin-based alloys (for example, SnAg or SnAgCu compositions) were the dominant lead-free materials used in commercial packaging

applications. A POSITA would have understood Yu's lead-free solder to be a *tin-containing layer* because Sn-based solders were dominant in commercial packages such as those taught by Yu Thus, the context of the chip packages of Yu means that "solder" necessarily includes Sn-content, thereby teaching the *tin-containing layer*. A POSITA would have understood Yu's disclosure of "lead-free solder" to mean the solder contains tin unless stated otherwise. That is, if someone refers to non-tin-containing solder, it would be specified as such because the "default" solder contains tin.

313. Accordingly, Yu teaches a structure in which the metallization bond pad is a second metal layer and the solder connector 58 is a tin-containing layer over said second metal layer, because the lead-free solder connector is formed on the bond pad. *EX1010* at 4:45–50. Thus, Yu teaches *wherein said first metal bump comprises a second metal layer and a tin-containing layer over said second metal layer*.

a) Lin-191's Teachings and Motivation to Combine

314. Additionally, Lin-191 teaches a metal bump comprising *a second metal layer and a tin-containing layer over said second metal layer*. *See* ¶¶ 153-154, incorporated herein. A POSITA would have been motivated, found it obvious, and had a reasonable expectation of success in modifying Yu per Lin-191 for the same reasons discussed for Sundaram-Lin-191. *See* ¶¶ 155-160, incorporated herein. The

Yu-Lin-191 combination is application of known technique (Lin-191's solder bump structure) to a known device (Yu's connector and pad) ready for improvement to yield predictable results, i.e., Yu's connector 58 comprising a *tin-containing layer over* a *second metal layer* (UBM layer).

17. 1(e): "a first semiconductor chip under said first interconnection scheme,"

315. Yu's package includes "die 52, such as a memory die," (*first semiconductor chip*) which is attached on the back side of the package. *EX1010* at 4:30–36. Yu explains that the back side of the package includes "TMVs 38" extending through the molding compound 18 and that conductive connectors are formed between the die 52 and those vias to establish electrical communication. *Id.* at 4:28–44. As shown in Yu's FIG. 16, die 52 is positioned *under said first interconnection scheme*:

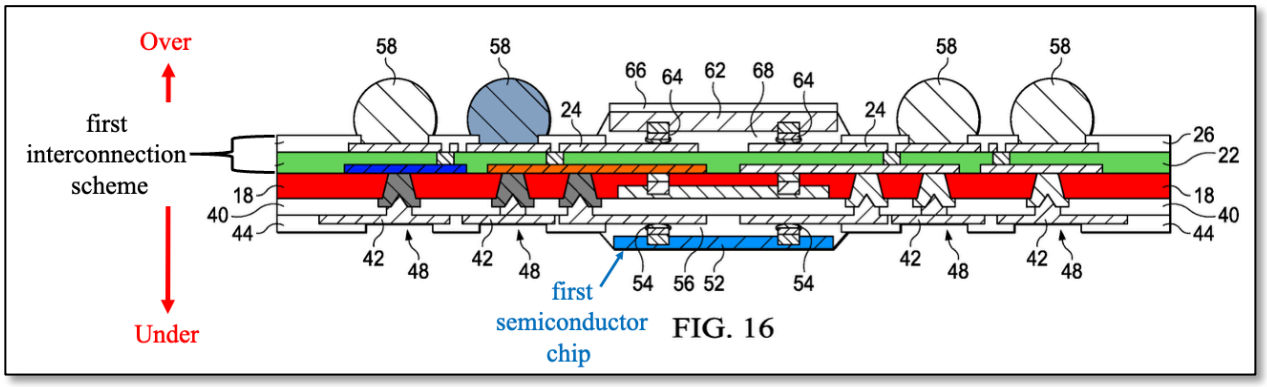


FIG. 16

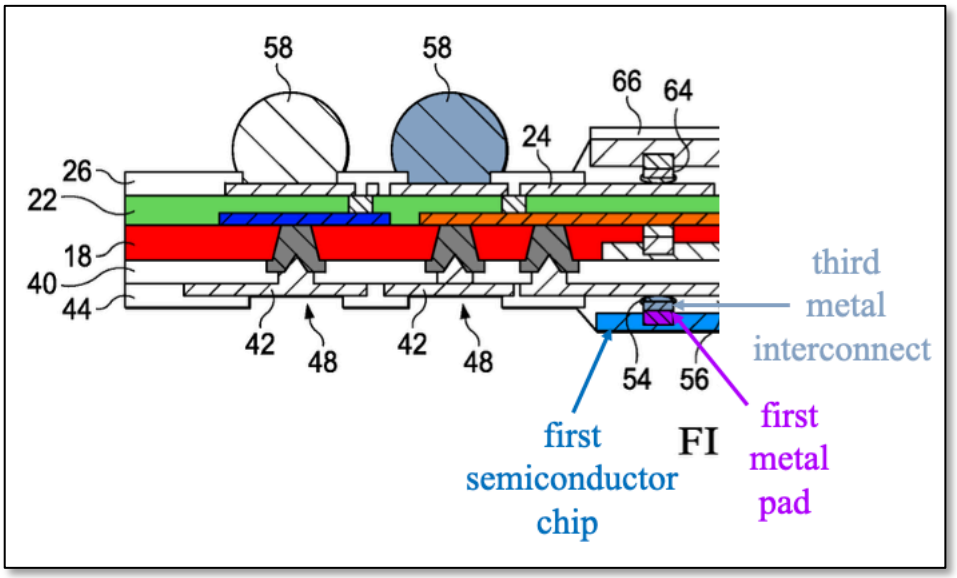
EX1010 at FIG. 16.

18. 1(e)(i): "wherein said first semiconductor chip comprises a third metal interconnect on a first metal pad of said first semiconductor chip,"

316. Yu teaches that die 52 *"*is attached…to conductive features in the second back side metallization layer 42, such as by conductive connectors 54, like controlled collapse chip connection (C4) bumps*." EX1010* at 4:30–34. Connector 54 thus provides the conductive pathway that couples die 52 to metallization layer 42 and functions as *a third metal interconnect on a first metal pad of said first semiconductor chip.*

317. Connector 54 is formed on the underside of die 52, establishing both mechanical and electrical contact to the back-side metallization. Yu's explicit reference to "C4 bumps" reflects the standard flip-chip interconnect process in which solder bumps (metal interconnects) are deposited directly on metal bond pads of the semiconductor die. *See* ¶ 70. Accordingly, a POSITA would have understood that Yu's die 52 includes a metal bond pad underlying each C4 bump, since such pads are required for reliable solder attachment and electrical continuity in C4 packaging.

318. Thus, Yu teaches that die 52 comprises *a first metal pad* and a connector 54 functioning as *a third metal interconnect on* that *first metal pad*. *EX1010* at 4:30–34; FIG. 16.



EX1010 at FIG. 16 (excerpt).

319. A POSITA would have understood the rectangle portion of die 52 to be a *metal pad* of die 52 given that "I/O terminals were traditionally formed by way of metal pads along the periphery of an IC." *EX1095* at 1:24-25. As shown, the C4 bump/connector 54 (*third metal interconnect*) is *on* the *first metal pad*. *EX1010* at 4:30-34.

a) Lin-191's Metal Pad Teaching and Motivation to Combine

320. In addition to Yu, Lin-191 teaches a semiconductor chip 160 with "metal traces or pads 163" that include "aluminum." *EX1005* at [0384]; *see* ¶ 164, incorporated herein. A POSITA would have been motivated and found it obvious to apply Lin-191's teachings of a *metal pad* to Yu's C4 bumps, thereby yielding the

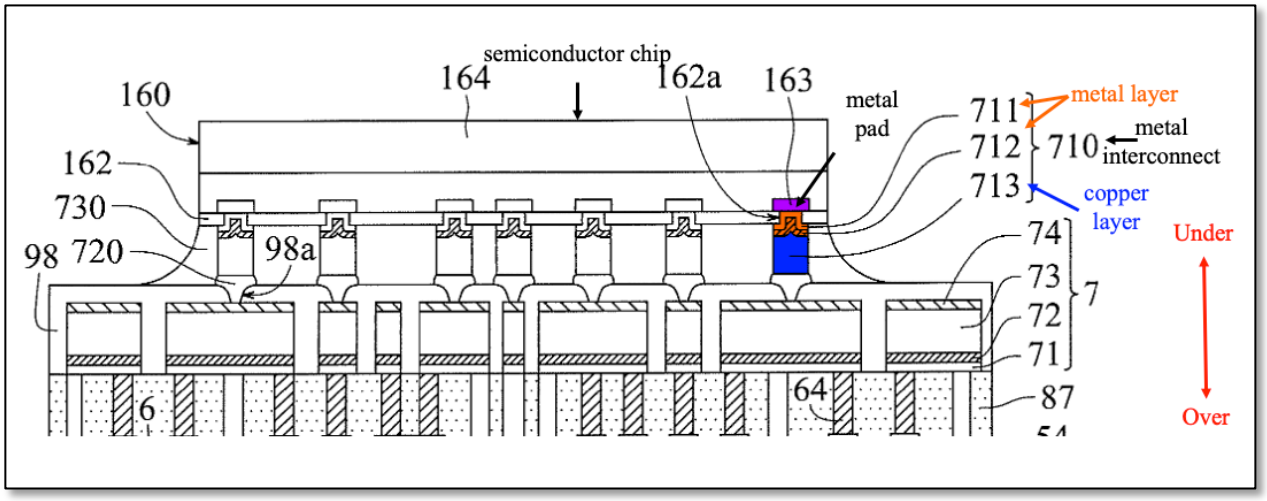
predictable result of Yu's *first semiconductor chip* (die 52) having C4 bumps (*first…pad*) that is *metal*. As I described above, Yu already teaches die 52 comprising connector 54, i.e., the claimed *first pad*, and Lin-191 merely provides additional specificity that the pad is *metal*. *See* ¶¶ 316-318. Modifying Yu's connector 54 to be metal, thereby yielding a *first metal pad*, is merely an implementation detail in Yu's overall system, i.e., Lin-191 provides the specificity of a semiconductor contact pad being *metal*. Thus, for the same motivations described above, a POSITA would have been motivated to modify Yu's connector 54 to be a *first metal pad*. *See* ¶¶ 165-166, incorporated herein.

321. The combination is the combination of prior art elements according to known methods to yield the predictable result of Yu's pad being *metal*. *EX1005* at [0081]. As I described above, metal contact pads were ubiquitous, so a POSITA would have had a reasonable expectation of success in modifying Yu's pad to be *metal*, such as aluminum, per Lin-191. *See* ¶¶ 165-166.

19. 1(e)(ii): "wherein said third metal interconnect comprises a third metal layer on said first metal pad and a third copper layer over said third metal layer, wherein said third copper layer has a thickness between 5 and 30 micrometers."

a) Lin-191's Teachings and Motivation to Combine

322. Lin-191 teaches or renders obvious interconnects/bumps with layers/thickness as recited in Claim 1(e)(ii), and the '763 Patent ascribes no criticality to the claimed *thickness*. *See* ¶¶ 167-168, incorporated herein.



EX1005 at FIG. 72 (excerpt).

323. A POSITA would have found it obvious and been motivated to modify Yu's connector for the reasons discussed with respect to Sundaram, i.e., improved metallurgical bonding and increased resistance to fatigue and stress-induced failure. *See* ¶¶ 169-175, incorporated herein. Yu, like Lin-191's underfill 730, teaches an underfill material 56 such that the thickness of the *fifth copper layer* would advantageously provide ample space for Yu's underfill material 56 to be positioned. *EX1010* at 4:39-40; *see* ¶ 173. Layered bumps, per Lin-191, were routinely manufactured using techniques already contemplated by Yu, leading to a reasonable expectation of success. For example, Lin-191 teaches using a "sputtering process[,]"

"physical-vapor deposition (PVD) process," and electroplating, which are all techniques taught by Yu. *EX1005* at [0400], [0413]; *EX1010* at 3:5-8 ("A seed layer…is deposited…such as by sputtering or another physical vapor deposition process.), 3:11-14 ("Conductive material…is deposited…such as by…electroplating[.]"). Accordingly, the modification would have merely required forming Yu's *third metal interconnect* per Lin-191's structure using techniques already taught by Yu, which would have given a POSITA a reasonable expectation of success.

B. *Claim 2: "The chip package of claim 1, further comprising a passive component over said first interconnection scheme and connected to said first interconnection scheme through a solder layer."*

324. Yu teaches "chip resistors" and "chip capacitors," which are *passive component[s]* as described by the '763 Patent. *EX1010* at 1:41-45; *EX1001* at 13:57-59 ("…a passive device 44…such as an inductor, a capacitor or resistor."

a) Lin-191's Teachings

325. As detailed herein, Lin-191 teaches two embodiments relevant to Claim 2's mapping, namely the FIG. 55 embodiment and the FIG. 84 embodiment. In the FIG. 55 embodiment, Lin-191 teaches chip 140 "can be replaced by a passive component 67," where the passive component is "connected to the metal layer 53 of

the patterned metal layer 5 **through** two solder joints 68."[6] *EX1005* at [0340], FIG. 55. Shown in FIG. 55 below, Lin-191 teaches a "passive component 67, such as a capacitor, inductor, or resistor." *EX1005* at [0341]. Lin-191's patterned metal layers 5 are an *interconnection scheme* because "patterned metal layer 5 may include a metal **interconnect** or trace…." *EX1005* at [0214]. Thus, Lin-191's *passive component* is connected to a metal interconnect in an *interconnection scheme*. Additionally, Lin-191 provides specificity to solder joints 68, teaching that they "may include bismuth, indium, tin-lead alloy, tin-silver alloy, tin-silver-copper alloy, or tin-gold[,]" thereby teaching a *passive component* connected to the *interconnection scheme* (layer 5) through a *solder layer*.

[6] The textual description of FIG. 84 at [0439] does not discuss chip and layers, but Lin-191 states that "[w]hen the same numeral appears in different drawings, it refers to the same or like components or steps." *EX1005* at [0013]. Therefore, Lin-191's discussion of FIG. 55 and chip 140 and layers 5 is applicable to the FIG. 84 embodiment.

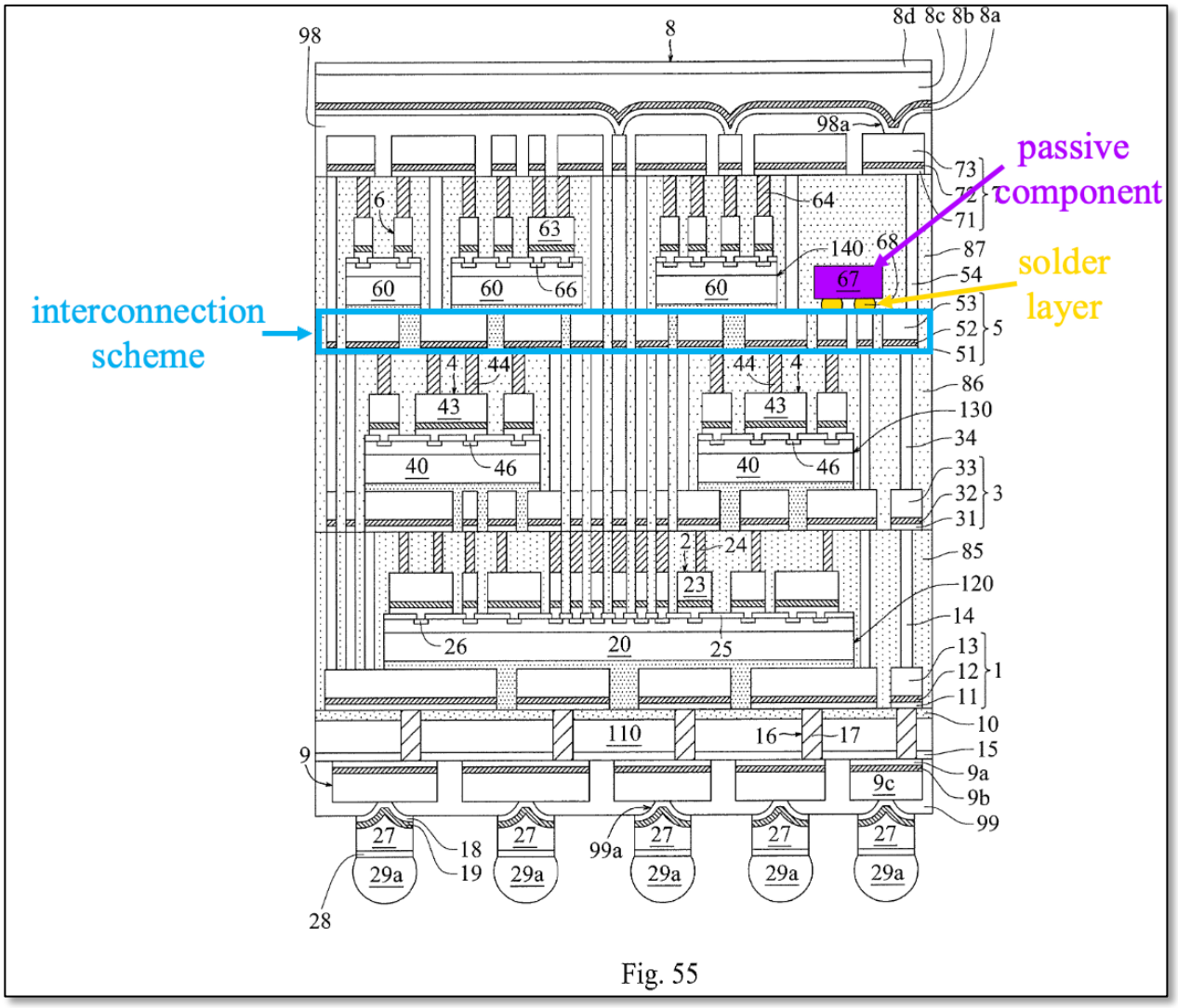


Fig. 55

EX1005 at FIG. 55.

326. In the FIG. 84 embodiment, Lin-191 teaches that chip 140 is *over* and connected to patterned metal layer 5 (*interconnection scheme*). *EX1005* at FIG. 84, [0273], [0340]. That is, chip 140 is *over* patterned metal layer 5 because it is towards the solder balls 29a which connect to a PCB and is therefore in the "over" direction as depicted by the red arrow. *EX1005* at [0439].

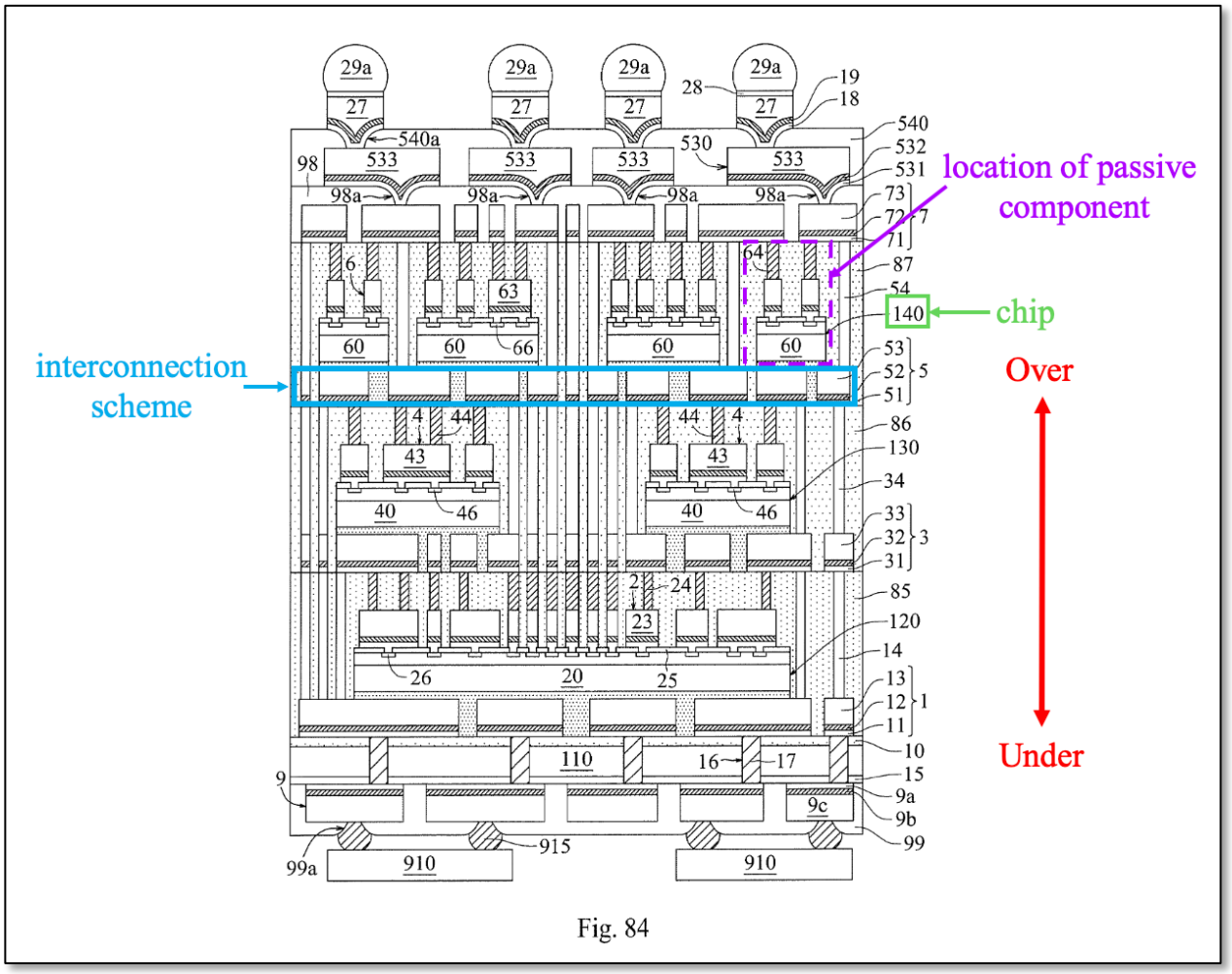


Fig. 84

EX1005 at FIG. 84.

327. Based on Lin-191's express teaching and motivation that "one of the chips 140" can "be replaced by a passive component 67[,]" a POSITA would have found it obvious and been motivated to replace the chip 140 in FIG. 84 with passive component 67, thereby teaching or rendering obvious *passive component* (passive component 67) *over said first interconnection scheme* (layer 5). That is, when chip 140 in FIG. 84 is replaced with passive component 67, the *passive component* is *over*

Lin-191's *interconnection scheme* for the same reasons as discussed above for chip 140. *See* ¶ 326. When chip 140 is replaced with passive component 67, a POSITA would have found it obvious to connect passive component to Lin-191's *interconnection scheme* (patterned metal layer 5) through a *solder layer* (solder joints 68) as taught by Lin-191. *See* FIG. 55, [0340] ("The passive component 67 can be connected to the metal layer 53 of the patterned metal layer 5 through two solder joints 68."). A POSITA would have been motivated to position passive component 67 in place of chip 140 because passive components, such as a capacitor, were known to preserve the integrity of signals from various chips travelling to the PCB. *See, e.g., EX1048* at [0001] ("Chips such as Application Specific Integrated Circuits [] often include power and ground connections to the circuit board. Capacitors, often referred to as 'bypass capacitors' or 'decoupling capacitors,' are usually coupled across the power and ground connections to filter out unwanted electrical noise that may be generated by the power supply. The bypass capacitors may be disposed on the bottom side of circuit board within the footprint of the ASIC."). The modification is the application of a known technique (a passive component connected to an interconnection scheme via a solder joint) to a known device (Lin-191's package) to yield the predictable result of Lin-191's FIG. 84 embodiment having a passive component 67 in place of a chip 140.

328. Further, in the modified FIG. 84 embodiment, multiple passive components, namely passive component 67 and passive component 910 are provided. A POSITA would have found it obvious to include multiple passive components in the chip package at various locations, because such a practice was advantageous for preserving signal integrity throughout the entire chip package. *EX1090* at [0010] ("As the internal circuitry of high performance ICs, such as processors, operates at higher and higher clock frequencies, noise in the power and ground lines increasingly reaches an unacceptable level. This noise can arise due to inductive and capacitive parasitics, for example, as is well known. To reduce such noise, capacitors known as decoupling or by-pass capacitors are often used to provide a stable signal or stable supply of power to the circuitry."). For example, a POSITA would have recognized that positioning passive component 67 in place of chip 140 would preserve the signal integrity of the chip 130 positioned under passive component 67, by filtering out "unwanted electrical noise" from signals traveling from chip 130 toward solder balls 29a, which connect to a printed circuit board. *EX1048* at [0001]; *EX1005* at [0348].

2. Motivation to Combine

329. Yu already teaches passive components such as "chip resistors" and "chip capacitors." *EX1010* at 1:41-42. Lin-191 teaches connecting *passive*

component[s] in a multiple chip package. Thus, based on Lin-191's teachings, a POSITA would have found it obvious and been motivated to modify Yu's chip package to comprise a *passive component* (e.g., passive component 67) *over* the *first interconnection scheme* and connected to a metal interconnect through a *solder layer* (solder joints 68). A POSITA would have appreciated that by connecting a passive component, e.g., a capacitor, over Yu's RDL, Yu's chip package would advantageously preserve the integrity of signals from Yu's dies 52, 62 traveling to a PCB (printed circuit board). As I described above, passive components, such as capacitors, were known to ensure signal quality and integrity because the capacitor maintains transmission line integrity, thereby suppressing distortion in such signals prior to transmission to the PCB. *See* ¶ 328. Indeed, "by use of bypass capacitors on multi-layer printed circuit boards, the total area of the current loop formed by the signal trace and its return current can be minimized. Signal integrity, which is influenced by factors such as impedance, inductive crosstalk to other signals, signal transmission line reflection, and balance, can be improved and noise can be well controlled." *EX1049* at 7:11-19. Additionally, capacitors were known to provide "less noisy power being supplied" to chips in a chip package by "providing a low inductance path between power and ground." *EX1050* at 5:37-41. As such, a POSITA would appreciate both the improvement in signal integrity and reduction in

power noise due to the low-inductance path provided by the *passive component*. Further, including a passive component, such as a capacitor, would reduce the impact of high frequency interference (HFI) on digital signals being transmitted between die 62 a PCB connected to connectors 58, as well as reduce the negative impact of HFI on power supply lines in Yu's chip package, thereby further preserving signal integrity. Specifically, "when events take place that have frequency higher than what can be accommodated by a voltage regulator, noise occurs." *EX1100* at [0004]. A capacitor "works as backup energy storage" that can "quickly provide the shortfall" if the voltage drops due to such high frequency events. *EX1100* at [0004].

330. The modification is the application of a known technique (implementing a passive component) to a known device (Yu's chip package) to yield the predictable result of Yu's chip package having a passive component. Further, a POSITA would have had a reasonable expectation of success in including a *passive component* in Yu's chip package, because soldering passive components into chip packages was a very well-known technique, as demonstrated by Lin-191 and others. *See, e.g., EX1051* at FIG. 14, [0093] ("…chip capacitor 213 are provided with a power electrode 214 to be connected to the power internal electrode layer and the power solder bump 217…and the ground solder bump 220."), Furthermore, the

inclusion of passive components such as Lin-191's was a ubiquitous practice in chip packaging, thus making the modification simple, straightforward, and routine, thereby further evidencing the reasonable expectation of success. *See, e.g., EX1052* at FIG. 2, [0025] ("The flip-chip BGA package 4 further comprises an RC passive component 41 such as a resist or a capacitor…"); *EX1053* at [0030] ("In some embodiments, electronic components such as the component 180 can comprise passive components (e.g., resistors, capacitors, inductors)…").

C. *Claim 3: "The chip package of claim 1, wherein said first interconnection scheme comprise a fourth metal interconnect across over a sidewall of the first semiconductor chip."*

a) "Fourth Metal Interconnect"

331. For the same reasons described above, another portion of metallization layer 20 is *a fourth metal interconnect*. *See* ¶¶ 302-303; *EX1010* at 3:5–20. Further, as shown below, the *fourth metal interconnect* is both *across* and *over* a *sidewall* of die 52 (*first semiconductor chip*). The blue dashed line indicates the *sidewall* of die 52, namely a boundary thereof. Notably, the *fourth metal interconnect* is positioned in the "over" direction relative to the *sidewall*, as indicated by the red arrow depicting the over/under directions. Additionally, the *fourth metal interconnect* extends laterally (i.e., left/right) to the right past the boundary of the *sidewall*. Thus,

the *fourth metal interconnect* is both *across* and *over a sidewall of the first semiconductor chip*.

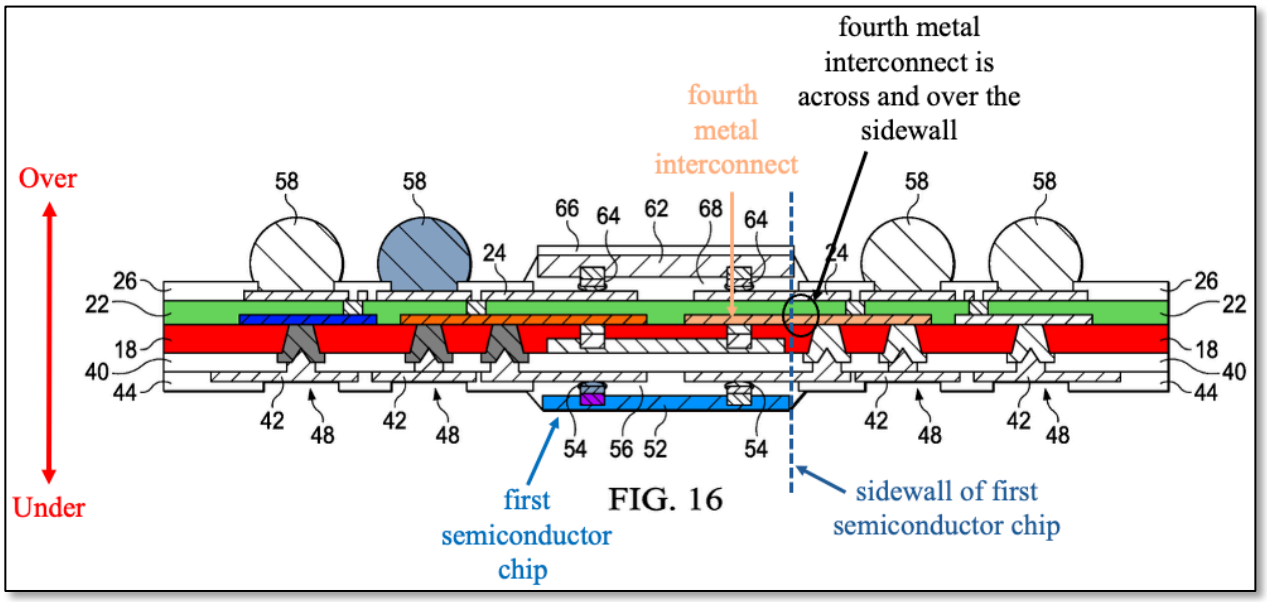
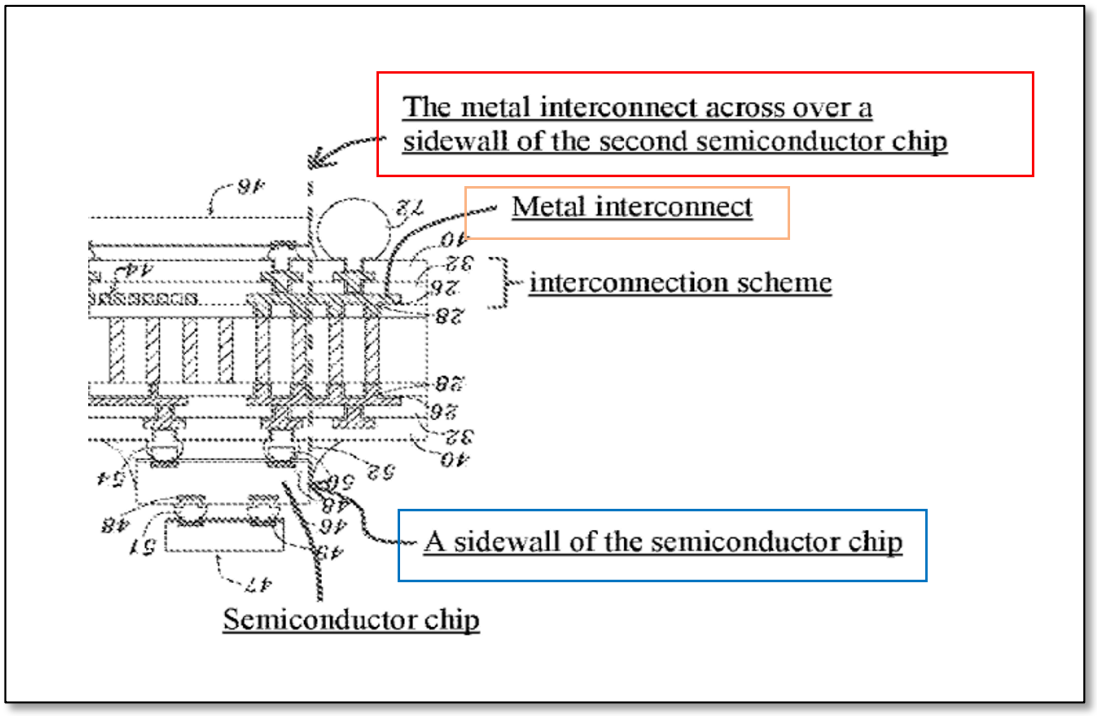


FIG. 16

EX1010 at FIG. 16.

332. I note that Yu's teachings of the *fourth metal interconnect* being *across* and *over* the *sidewall of the first semiconductor chip* are consistent with an annotated figure that Patent Owner provided during prosecution of the related '768 Patent, illustrating support for this specification. In the figure below, I have shown how the Patent Owner's annotations mirror the above mapping of Yu's *fourth metal interconnect*.



EX1032 at p. 537[7].

D. *Claim 4*

1. 4(a): "The chip package of claim 1, further comprising a second semiconductor chip over said first interconnection scheme,"

333. Yu teaches a "die 62, such as a memory die," that is "attached…to conductive features in the second front-side metallization layer 24," such that die 62 is a *second semiconductor chip over said first interconnection scheme*. *EX1010* at 4:53-56. Yu's FIG. 16 shows die 62 positioned over the first die 52, establishing a

[7] Annotated figure Patent Owner argued supports language similar to Claim 3.

stacked configuration characteristic of a package-on-package (PoP) or multi-chip package architecture. In this arrangement, die 52 resides beneath the molding compound 18, while die 62 is mounted above the front-side redistribution structure that includes metallization layers 20 and 24.

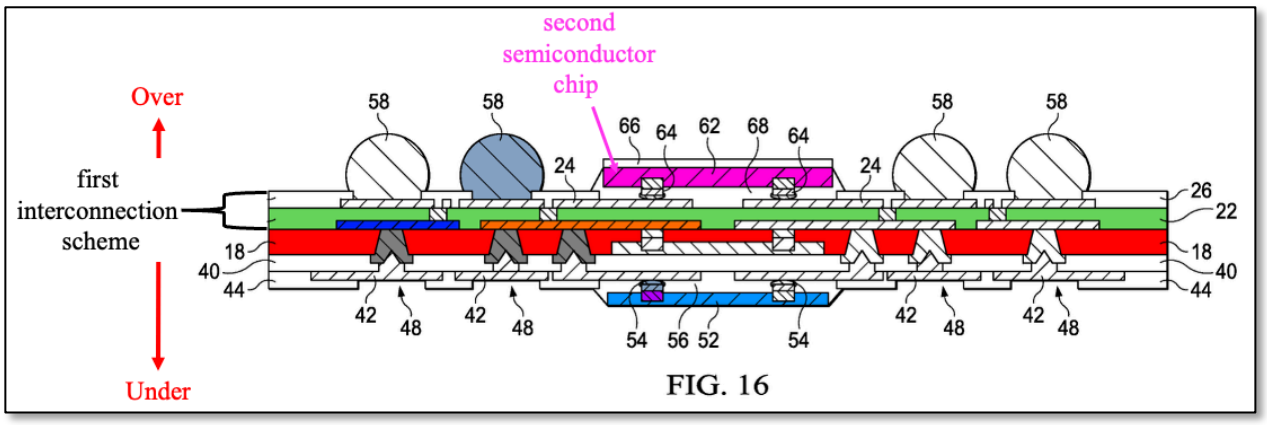


FIG. 16

EX1010 at FIG. 16.

2. 4(b): "wherein said second semiconductor chip comprises a second metal bump between said second semiconductor chip and said first interconnection scheme."

334. Shown below, die 62, like die 52, includes interconnect structures that enable electrical coupling to the underlying metallization features. Yu specifies that die 62 is connected through "connectors 64, such as controlled collapse chip connection (C4) bumps," which "attach to the conductive features in the second front-side metallization layer 24." *EX1010* at 4:56-60. A POSITA would recognize that because "connectors 64" are C4 bumps, that the connector 64 is solder-based interconnect commonly formed from tin-containing alloys (i.e., *metal*). *See* ¶ 70. Yu

thus teaches *wherein said second semiconductor chip comprises a second metal bump between said second semiconductor chip and said first interconnection scheme*:

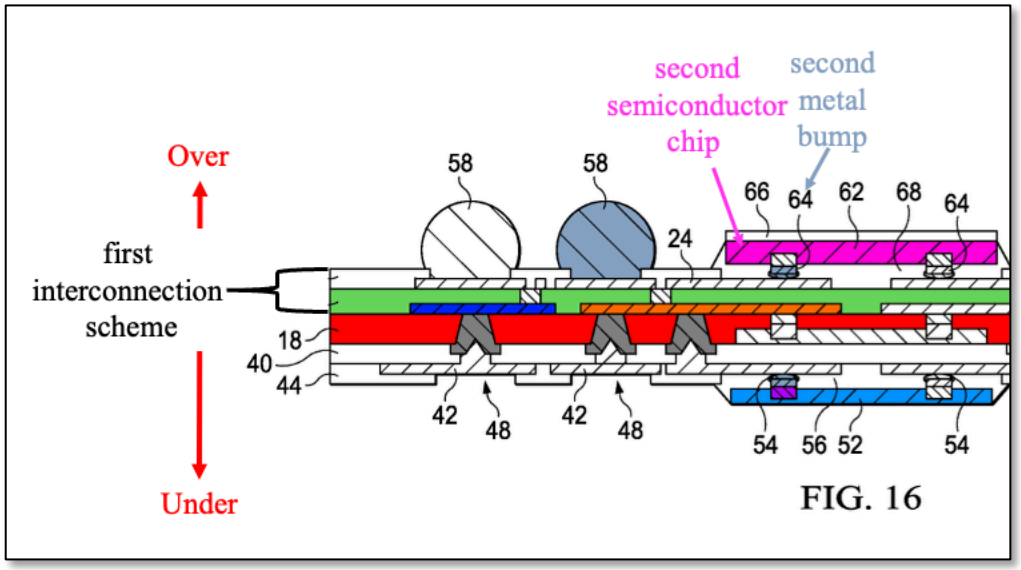


FIG. 16

EX1010 at FIG. 16.

E. *Claim 5: "The chip package of claim 1, wherein said first semiconductor chip comprises a central-processing-unit (CPU) circuit block and a graphics-processing-unit (GPU) circuit block."*

a) Lin-191's Teachings and Motivation to Combine

335. *See* ¶ 189, incorporated herein. The same MTCs and reasonable expectation of success for modifying Sundaram per Lin-191 apply to modifying Yu per Lin-191, e.g., increasing the functionality of Yu's chip package. *See* ¶¶ 190-192, incorporated herein. Further evidencing the motivation and reasonable expectation of success, Yu teaches dies can be "logic circuitry die, a memory die, or any other

die." *EX1010*, 2:50-51. Additionally, Yu, like Sundaram, contemplates "mobile telephone/PDA[s]." *EX1010* at 1:53-55.

F. *Claim 7*

1. 7(a): "The chip package of claim 1, wherein said first interconnection scheme further comprises a fourth metal interconnect over said first metal interconnect and said first polymer layer,"

336. As I described above, Yu teaches a sequence of stacked metallization and dielectric layers forming a multi-level interconnect structure on the front side of the package. *EX1010* at 3:28–32; see ¶ 301. A second metallization layer 24 is "formed using the same process" as metallization layer 20 is formed (i.e., with a seed layer and conductive material such as copper formed over the seed layer) such that a portion of layer 24 is a *fourth metal interconnect*. *EX1010* at 3:5–32; ¶ 302.

337. As shown, Yu's metallization layer 24 (*fourth metal interconnect*) is *over said first metal interconnect and said polymer layer*, as indicated by the red arrow depicting the over/under directions:

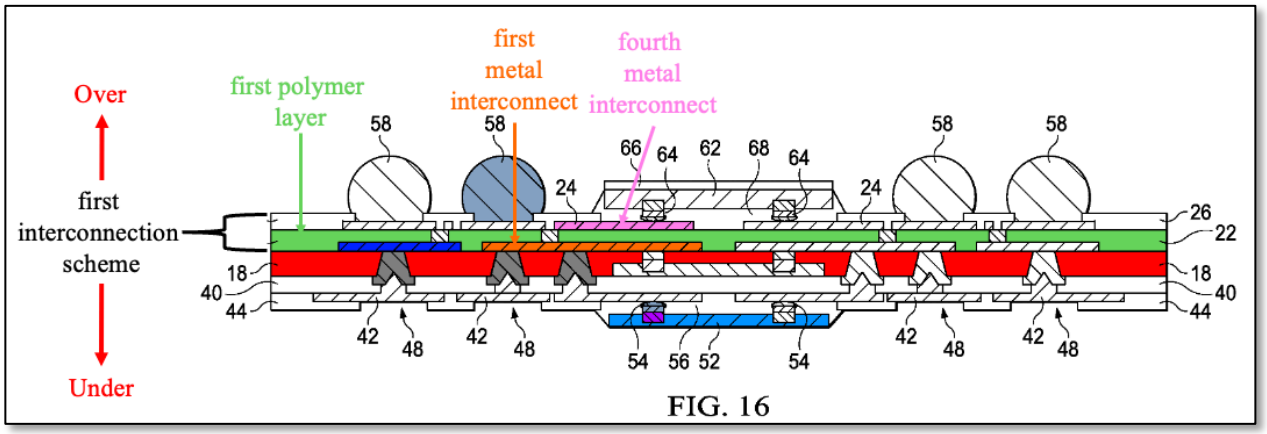


FIG. 16

EX1010 at FIG. 16; ¶ 304.

338. Alternatively, Yu teaches "any number of metallization layers and ILD layers may be formed, and the use of two…is used as an example." *EX1010* at 3:41-43. Because Yu teaches that "any number of metallization layers" may be formed, a third metallization layer (not shown) is *a fourth metal interconnect over said first metal interconnect and said first polymer layer* when the *first polymer layer* is ILD layer 26. *See* ¶ 305. Yu teaches "[c]onductive material deposited during the formation of a subsequent metallization layer may be deposited in openings of the previously formed ILD layer to electrically couple respective metallization layers." *EX1010* at 3:32-35. Thus, when a third metallization layer is formed, a portion of which is the *fourth metal interconnect*, such a layer is formed on layer 26 and below connector 58, resulting in the *fourth metal interconnect over said first metal interconnect and said first polymer layer*:

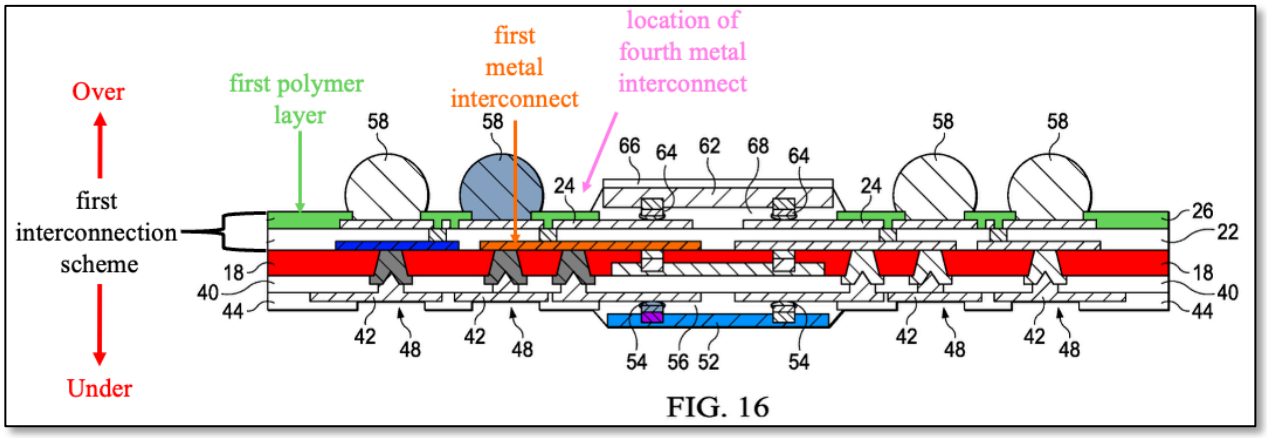


FIG. 16

EX1010 at FIG. 16; ¶ 305.

2. 7(b): "wherein said first polymer[8] is between said first and fourth metal interconnects,"

339. Metallization layer 24 is on ILD layer 22, which is "over the first metallization layer 20" such that ILD layer 22 *is between* layers 20, 24. *EX1010* at 3:20-32. Thus, the *first polymer layer is between said first and fourth metal interconnects*:

[8] I have been instructed to interpret Claim 7(b)'s *first polymer* as referring to the *first polymer layer* introduced in Claim 1(c)(i).

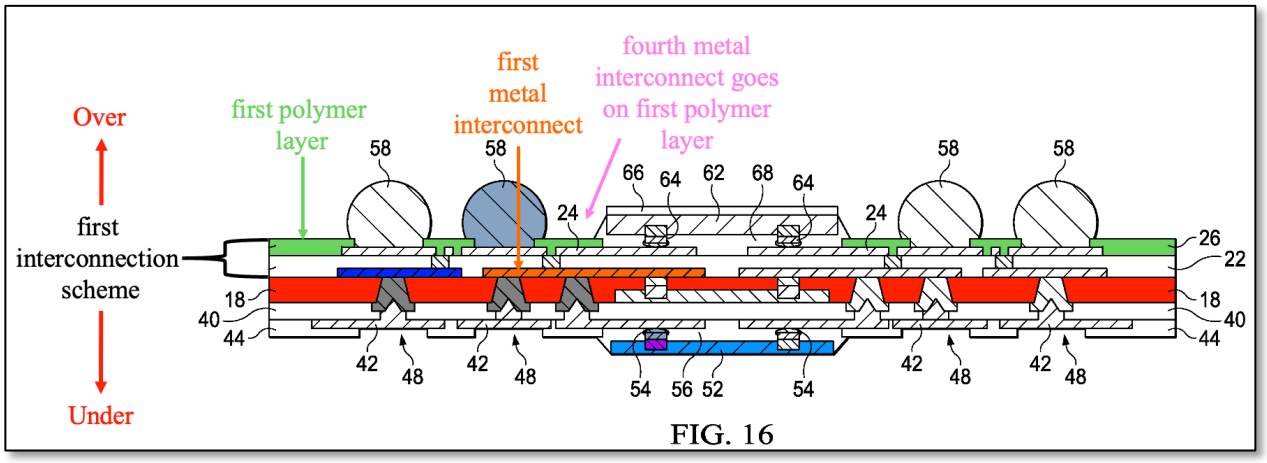


FIG. 16

EX1010 at FIG. 16.

340. Alternatively, because metallization layers are deposited on ILD layers, Yu's third metallization layer (*fourth metal interconnect*) is on ILD layer 26 such that ILD layer 26 (*first polymer*) *is between said first and fourth metal interconnects*. *EX1010* at 3:32-35; ¶ 338.

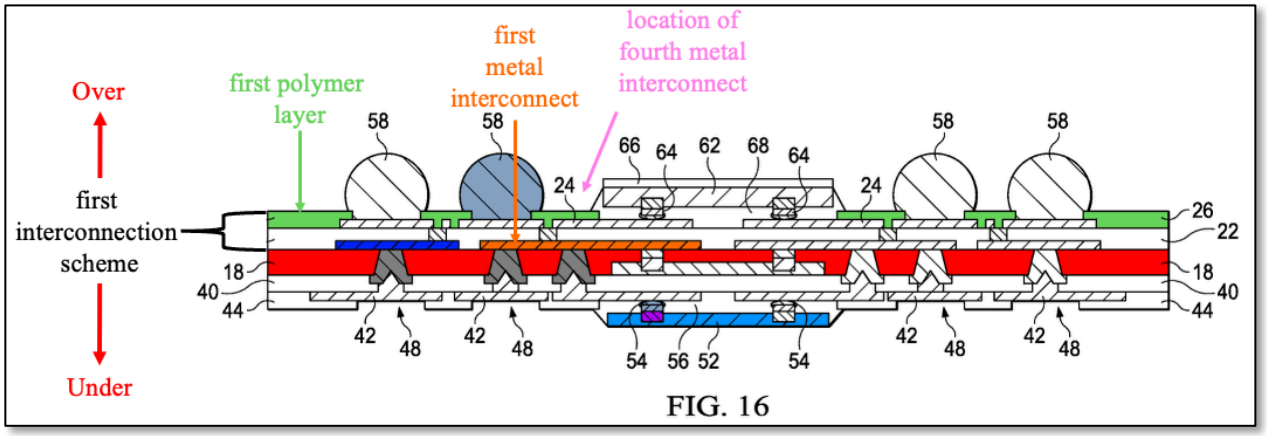


FIG. 16

EX1010 at FIG. 16; ¶ 305.

3. 7(c): "wherein said fourth metal interconnect comprises a fourth metal layer, a fourth copper layer on said fourth metal layer, and a fifth copper layer on said fourth copper layer."

341. As I described above, Yu teaches metallization layers (e.g., metallization layer 24) are formed using a "seed layer, such as copper" and then a "conductive material[,]" also copper, is formed on the copper seed layer. *See* ¶ 302; *EX1010* at 3:8-18. Accordingly, Yu's *fourth metal interconnect* (a portion of metallization layer 24 or portion of a third metallization layer) comprises a *fourth copper layer* (copper seed layer) and a *fifth copper layer* (electroplated copper layer) *on said fourth copper layer*. *See* ¶¶ 336-338.

a) Lin-191's Teachings and Motivation to Combine

342. Lin-191 teaches a metal interconnect having *a fourth metal layer, a fourth copper layer on said fourth metal layer, and a fifth copper layer on said fourth copper layer*. See ¶ 205, incorporated herein. The same MTCs and reasonable expectation of success for modifying Sundaram per Lin-191 apply for the Yu-Lin-191 combination. Like Yu's metallization layers, Lin-191's metal interconnect comprises a copper seed layer 72 and a copper metal layer 73 and additionally comprises metal adhesion layer 71 (*fourth metal layer*) under layers 72, 73. *EX1005* at [0127-0128], [0133]. Thus, a POSITA would have been motivated and found it obvious to apply multi-layered interconnect teachings, including Lin-191's adhesion layer 71 teachings, to Yu's *fourth metal interconnect* thereby yielding *a fourth metal*

layer, a fourth copper layer on said first metal layer, and a fifth copper layer on said fourth copper layer to obtain the benefits of Lin-191's adhesion layer 31.

343. As I discussed above, nickel adhesion layers such as that taught by Lin-191 advantageously mitigate copper diffusion out of the metal interconnect, reducing void formation and the risk of delamination. *See* ¶ 210. Thus, by modifying Yu's metal interconnect to comprise Lin-191's *first metal layer*, diffusion of copper out of Yu's *fourth* and *fifth copper layer[s]* would be reduced, thereby reducing damage to such layers leading to delamination. The modification would thus predictably increase the lifetime of Yu's chip package. The combination is the application of a known technique (Lin-191's three-layer metal interconnect) to a known device (Yu's metal interconnect) ready for improvement to yield predictable results, i.e., Yu's metal interconnects comprising three layers. There would have been a reasonable expectation of success because Lin-191 teaches forming adhesion layer 71 using manufacturing techniques also taught by Yu such that the modification would have been simple and straightforward. Indeed, Lin-191 teaches forming adhesion layer 71 using a "a physical-vapor deposition (PVD) process, such as sputtering process," which is the same technique used to form Yu's copper seed layer. *Compare EX1005* at [0259] *with EX1010 at* 3:5-16 ("A seed layer, such as a copper…is deposited…such as by sputtering or another physical vapor deposition

(PVD) process.") Because Yu's metal interconnect is already formed of a layer deposited by PVD, a POSITA would have had a reasonable expectation of success in forming a *first metal layer* such as Lin-191's layer 71, which is also formed by PVD.

G. *Claim 8: The chip package of claim 1, further comprising a second interconnection scheme under said solid layer and on said second surface."*

344. Yu teaches "a back side ILD and RDL structure" with a "first back side ILD layer 40, a second back side metallization layer 42, [and], a second ILD layer 44[.]" *EX1010* at 4:7-11. The back side ILD and RDL structure is formed "in the same manner as the front side ILD and metallization layers (*first interconnection scheme*). *EX1010* at 4:7-14. Thus, the back side ILD/RDL structure is *a second interconnection scheme under said solid layer and on said second surface*.

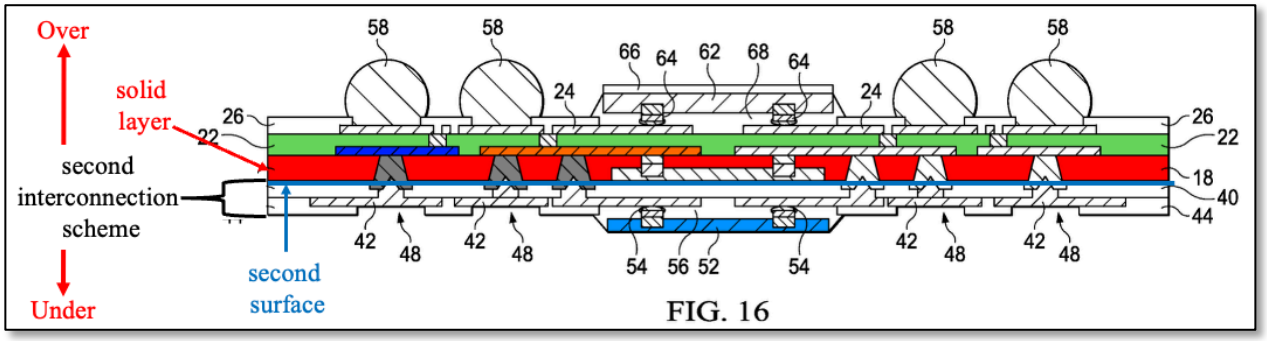


FIG. 16

EX1010 at FIG. 16.

H. *Claim 9: "The chip package of claim 1, wherein said first metal pad is an aluminum pad"*

a) Lin-191's Teachings and MTC

345. *See* ¶ 213, incorporated herein. The same MTCs and reasonable expectation of success for the Sundaram-Lin-191 apply for the Yu-Lin-191 combination. *See* ¶ 214, incorporated herein.

I. *Claim 10: "The chip package of claim 1, wherein said solid layer further comprises a third region opposite to said second region, wherein said third region is between said first region and another edge of said solid layer, wherein said plurality of copper plugs in said plurality of through vias in said third region respectively."*

346. Yu's molding compound 18 (*solid layer*) comprises a *third region*, shown below, which is on the *opposite* side of the *first region* than the *second region* and is, therefore, *opposite to said second* region. The *third region* is *between said first region* (green) *and another second edge of said solid layer*. Additionally, the *third region* comprises a *plurality of copper plugs in said plurality of through vias*, as shown:

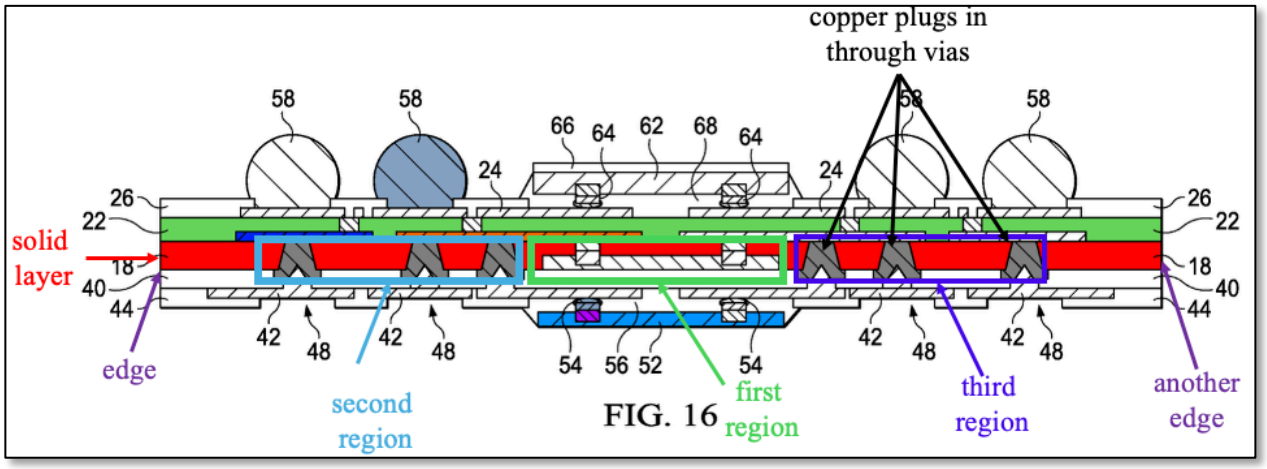


FIG. 16

EX1010 at FIG. 16.

J. *Claim 11: "The chip package of claim 1, wherein said first copper plug has a thickness between 100 and 300 micrometers."*

347. As shown below, Yu's *first copper plug* (TMV 38) extends from either side of the *solid layer*. Because the *solid layer*, per Claim 1(a)(iii), is *between 100 and 300 micrometers* thick, the *first copper plug* of Yu-Lin-191 has a thickness equal to that of the *solid layer,* thus teaching or rendering obvious the claimed *thickness between 100 and 300 micrometers*. *See* ¶¶ 287-294. As discussed, the '763 Patent does not ascribe any criticality to the claimed plug thickness of *between 100 and 300 micrometers*. *See* ¶ 217.

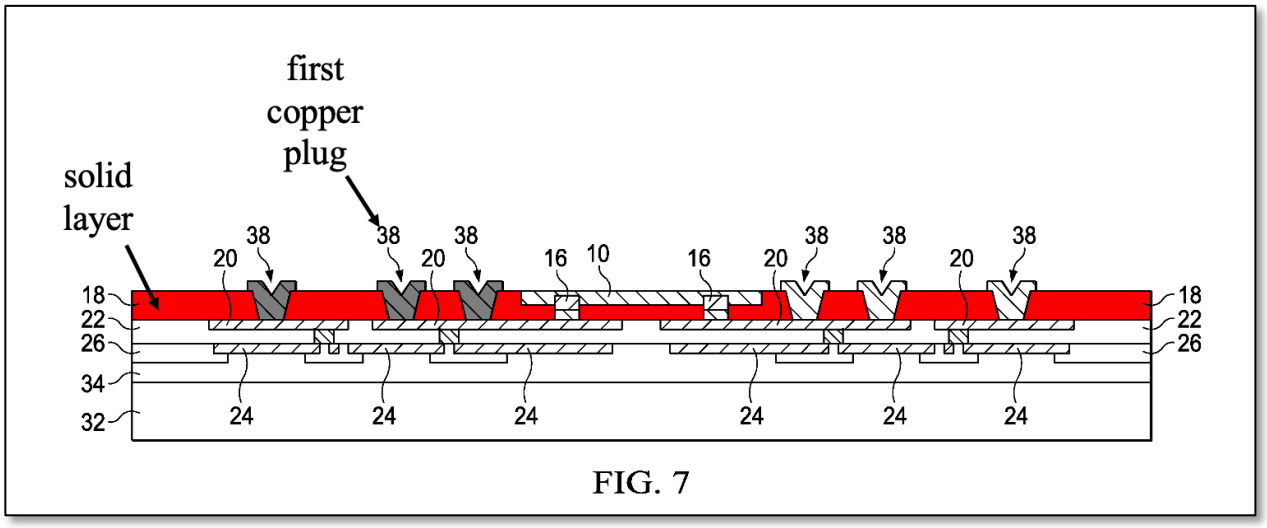


FIG. 7

EX1010 at FIG. 7.

K. ***Claim 12: "The chip package of claim 1, wherein said plurality of copper plugs comprise a third copper plug vertically in one of said plurality of through vias in said solid layer, wherein a pitch between said first and third copper plugs is between 200 and 1000 micrometers."***

348. Yu teaches a *third copper plug vertically in one of said plurality of through vias in said solid layer*, namely a third TMV 38:

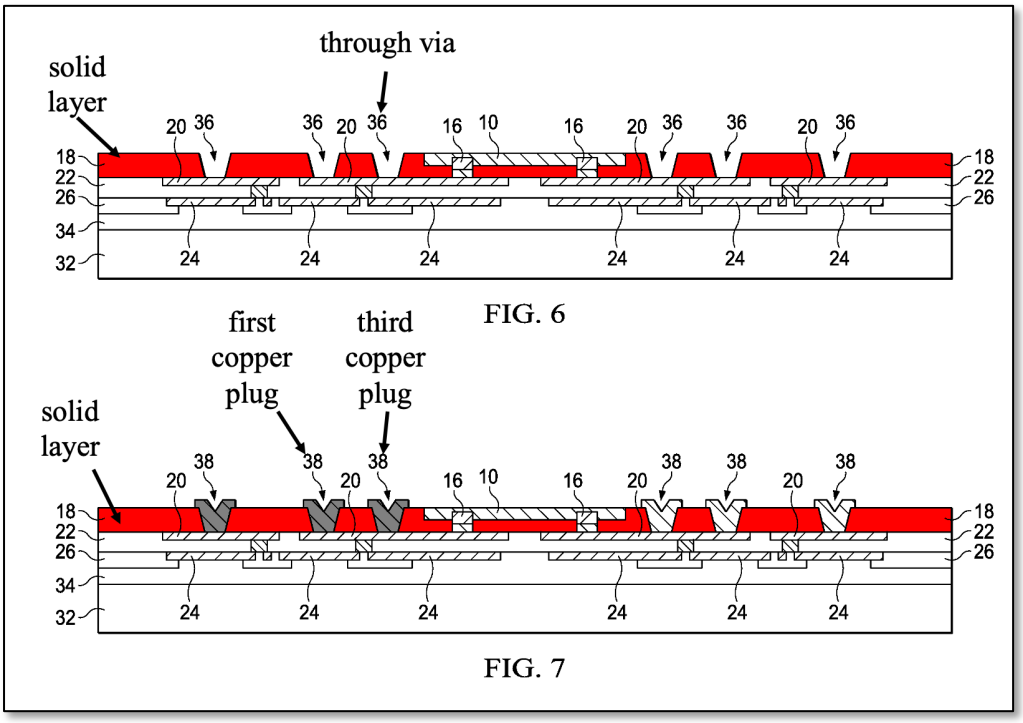


FIG. 6

FIG. 7

EX1010 at FIG. 16; ¶ 296. The *third copper plug* is *vertically in* a *through via* because the TMV 38 is formed vertically in molding compound 18, as illustrated above.

a) Lin-191's Teachings and Motivation to Combine

349. As I discussed above, Lin-191 teaches an "encapsulating 85" that is analogous to Yu's molding compound 18. *See* ¶ 287. Lin-191 further teaches "metal pillars or bumps 14" in encapsulating layer 85 that, like Yu's TMVs 38, are made of "copper" and interconnect components of a chip package. *EX1005* at [0066], [0086]. The "pitch between neighboring or adjacent pairs of metal pillars or bumps 14" can

be "between 100 and 250 micrometers" therefore teaching or rendering obvious *between 200 and 1000 micrometers*. *EX1005* at [0075].

350. I note that the '763 Patent does not indicate any criticality of the claimed pitch. *EX1001* at 6:11-18. That is, the '763 Patent does not provide the range of 200 and 1000 micrometers and then further provide an explanation for why such range is needed, important, or advantageous. Indeed, the '763 Patent describes a variety of ranges, including smaller (5 micrometers) and much larger values (10000 micrometers), indicating to a POSITA that the thickness can vary widely and that the thickness is not otherwise critical. *See EX1001* at 6:11-18.

351. A POSITA would have found it obvious and been motivated to apply Lin-191's pitch to Yu's *first* and *third copper plug[s]*, which are likewise neighboring/adjacent, as shown above. A pitch *between 200 and 1000 micrometers* was known to enable high bandwidth speeds such as "at least about 10 GB/s" in a "digital camera for cell phones[.]" *EX1004* at 6:42-55, FIG. 33 (showing a pitch of neighboring plugs between 220-240 μm). Yu already contemplates chip packages for use "in the mobile telephone/PDA market." *EX1010* at 1:53-55. Accordingly, a POSITA would have been motivated to implement Lin-191's *pitch* of *between 200 and 1000 micrometers* to Yu's *first* and *third copper plug[s]* which was known to provide benefits in cell phones. The combination is the application of a known

technique (Yu's plugs having a pitch between *200 and 1000 micrometers*) to a known device (Yu's chip package) ready for improvement to yield predictable results, i.e., Yu's first and third plugs having a pitch between *200 and 1000 micrometers*. A POSITA would have a reasonable expectation of success at least because the modification would have been simple and straightforward as methods of controlling pitch of metal plugs were well-known. Indeed, the modification would have merely required forming the openings 36 in which TMVs 38 are formed to have such a pitch, and Yu already teaches a "laser technique or a mechanical process like drilling" is used to form openings 36, thereby leading to a reasonable expectation of success. Additionally, Yu explicitly discloses forming TMVs using "laser technique[s] or a mechanical process like drilling," both of which allow precise adjustment of via spacing and diameter. *EX1010* at 3:66–4:1. Lin-191's pitch parameters would therefore be directly implemented using Yu's described manufacturing methods without requiring new materials or processes, further leading to a reasonable expectation of success. A POSITA would have viewed the modification as a routine design optimization, applying a known fine-pitch interconnect spacing from Lin-191 to Yu's analogous TMV structure—to achieve predictable improvements in bandwidth density, form factor reduction, and mechanical reliability.

L. *Claim 14*

1. 14(a): "The chip package of claim 1, further comprising a second semiconductor chip over said first interconnection scheme and connected to said first interconnection scheme through a second metal bump,"

352. *See* ¶¶ 333-334. Yu's die 62 (*second semiconductor chip*) is *over said first interconnection scheme and connected to said first interconnection scheme through a second metal bump* (connector 64). Indeed, Yu expressly teaches that die 62 is connected through "connectors 64, such as controlled collapse chip connection (C4) bumps," which "attach to the conductive features in the second front-side metallization layer 24." *EX1010* at 4:56-60. A POSITA would recognize that these "connectors 64" are solder-based interconnects commonly formed from tin-containing alloys (e.g., Sn-Ag-Cu systems) and that each bump is formed over a bond pad or metal pad on die 62, consistent with standard C4 bumping processes in semiconductor packaging.

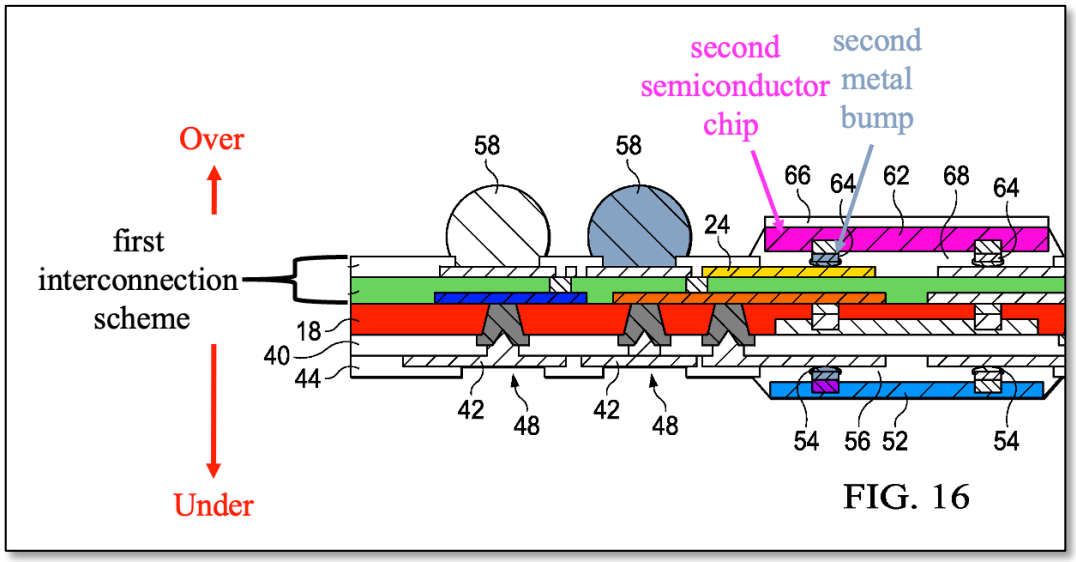


FIG. 16

EX1010 at FIG. 16 (excerpt).

2. 14(b): "wherein said second semiconductor chip has a height is between a backside surface of said second semiconductor chip and a top surface of said first polymer layer is smaller than a thickness of said first metal bump."

353. As I discussed above at Claim 1(c)(i), Yu's *first polymer layer* includes ILD layer 22 but may also include ILD layer 26. *See* ¶ 304. Thus, Yu's die 62 (*second semiconductor chip*) *has a height* that *is between a backside surface* (orange line) *of said second semiconductor chip and a top surface* (indicated by the orange arrow) *of said first polymer layer* that *is smaller than a thickness of said first metal bump*:

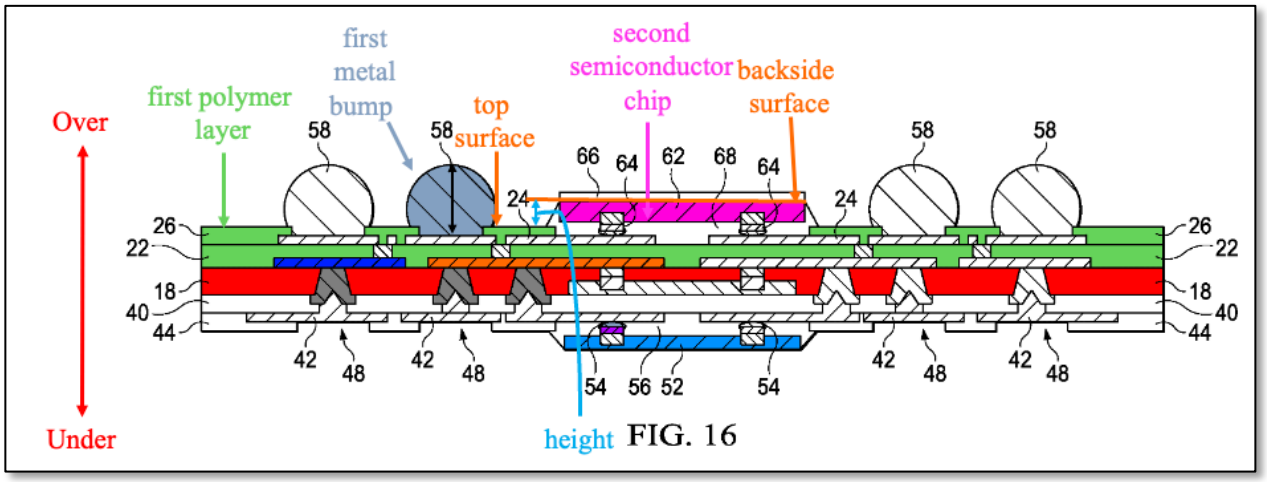


FIG. 16

EX1010 at FIG. 16; ¶ 304.

354. Alternatively, Yu's *first polymer layer* is ILD layer 26, which also results in Yu's die 62 (*second semiconductor chip*) *ha[ving] a height* that *is between a backside surface* (orange line) *of said second semiconductor chip and a top surface* (indicated by the orange arrow) *of said first polymer layer* that *is smaller than a thickness of said first metal bump*:

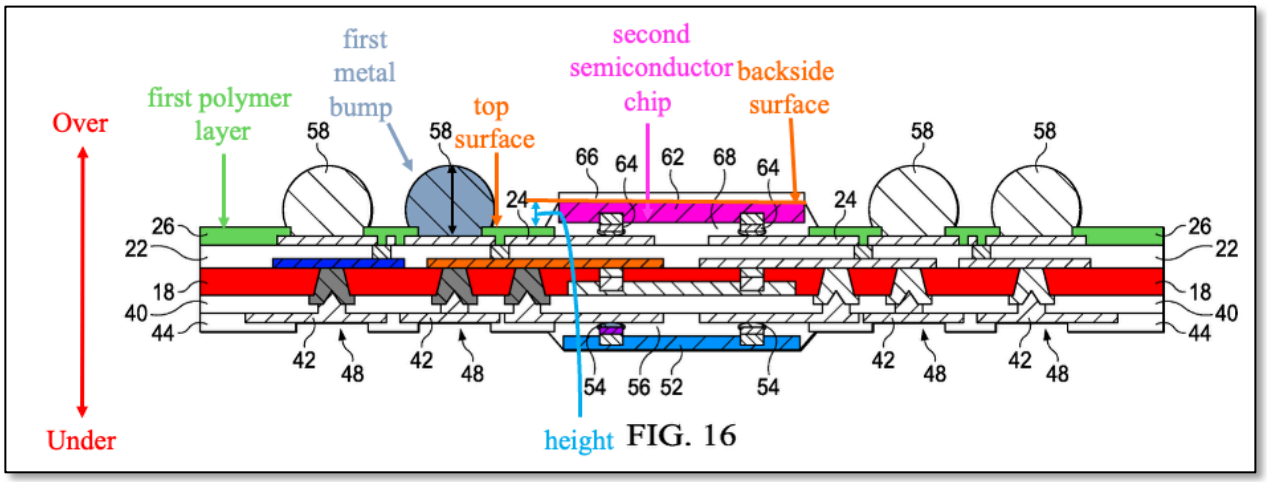


FIG. 16

EX1010 at FIG. 16; ¶ 305.

M. *Claim 15: "The chip package of claim 1, wherein no any copper plug in said first region."*

355. Yu teaches that TMVs 38 (copper plugs) are on either side of the first region, which encapsulates a die 10 such that there are *no any copper posts in said first region.* As shown in FIGS. 1 and 2, Yu describes that package 202 includes "a first die encased in molding compound 18," with through-mold vias (TMVs) 38 extending vertically through the surrounding molding compound. *EX1010* at 2:41-65; 8:7–8. The molding compound 18 defines a distinct encapsulation region surrounding and above die 10, within which the die is embedded.

356. Yu further teaches that the TMVs 38 are "formed through the molding compound 18", showing that the copper-filled posts are positioned in the molding regions adjacent to, rather than within, the die-encapsulating area. *EX1010* at 3:56–4:6. FIGS. 1–2 visually confirm that the TMVs 38 are distributed around the periphery of die 10, connecting the upper and lower metallization structures but avoiding the central die region. The die 10 itself occupies the central *first region* while the TMVs are confined to either side of the *first region*, separated by the molding compound 18 that laterally isolates the die.

357. Accordingly, Yu teaches that TMVs 38 (copper posts) are on either side of the *first region*, which encapsulates a die 10 such that *there are no any copper plugs in said first region*:

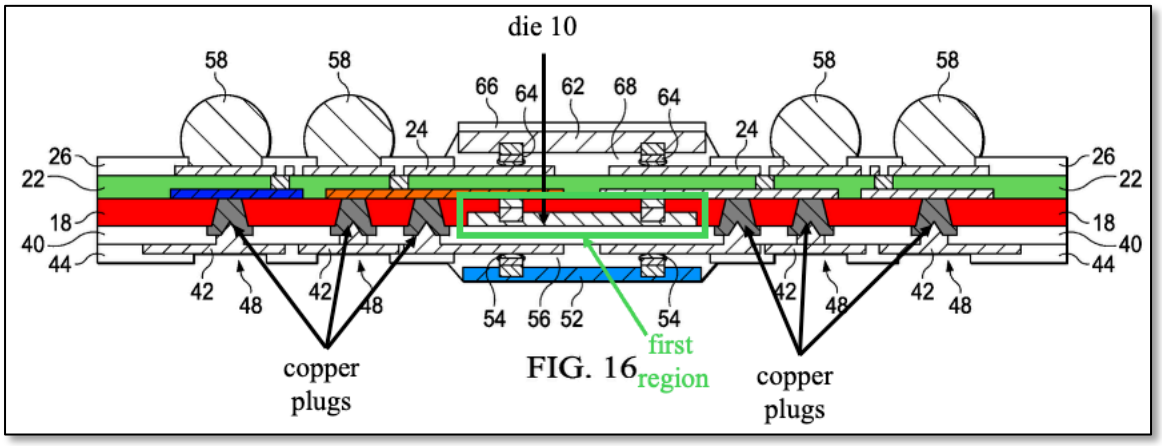


FIG. 16

EX1010 at FIG. 16.

N. *Claim 17: "The chip package of claim 1, wherein said compound comprises a SiO_2 compound."*

a) Lin-191's Teachings and Motivation to Combine

358. *See* ¶¶ 287-289. Lin-191's solid layer includes encapsulating layer 85 (discussed at Claim 1(a)(ii)) and further includes an insulating layer 10, which is made of "silicon dioxide (SiO_2)" and over which layer 85 is "formed." *EX1005* at [0052], [0109].

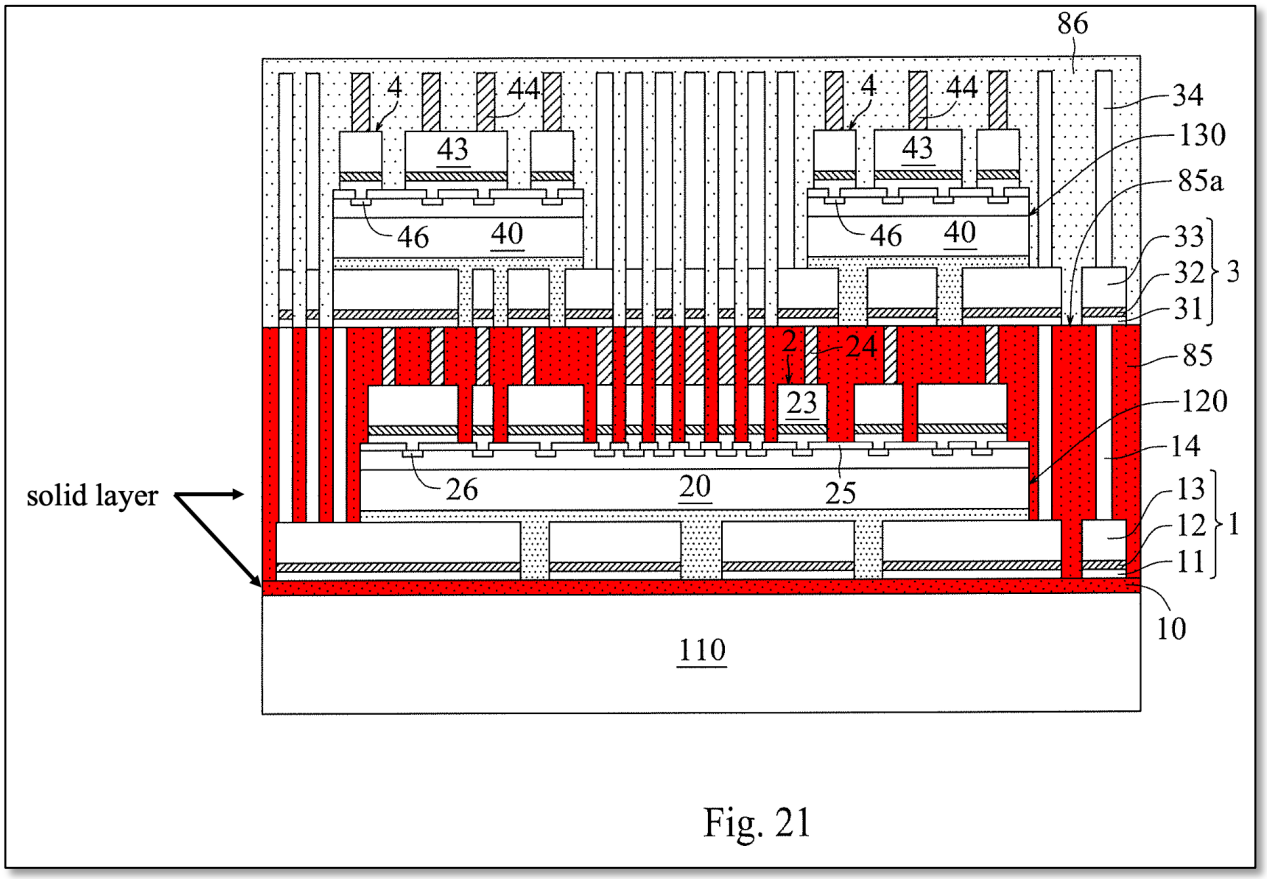


Fig. 21

EX1005 at FIG. 21.

359. Yu teaches molding compound 18 comprises "epoxy, polyimide, silicone rubber, the like, or a combination thereof," i.e., *a compound of silicon and oxygen*. *EX1010*, 2:61-65; *see* ¶ 286. Lin-191 specifically teaches SiO_2. In the combination, Yu is modified per Lin-191 such that *said compound* is the combination of Yu's molding compound 18 and Lin-191's insulating layer 10. Because insulating layer 10 is SiO_2, the Yu-Lin-191 compound *comprises a* SiO_2

compound. *EX1010* at FIGS. 34–35; 8:35–39 (formation of silicon-based interposer structure using oxide isolation layers).

360. A POSITA would have been motivated and found it obvious to modify Yu's molding compound 18 to include an SiO_2 insulating layer as taught by Lin-191 for multiple reasons such that Yu's *solid layer* (molding compound 18) is modified to include an SiO_2 layer similar to Lin-191's teachings of a *solid layer* comprising encapsulating layer 85 and insulating SiO_2 layer 10.

361. First, Yu itself expressly recognizes silicon-oxide-based materials as standard insulating and structural components in its own PoP and interposer packages. Yu discloses that the carrier substrate may comprise "glass, silicon oxide, aluminum oxide, [a] combination thereof, and/or the like" and later describes the interposer's "isolation layer 144 [which] can be, for example, silicon oxide…" *EX1010* at 5:2-5, 6:35-39. Thus, Yu already employs SiO_2 as a dielectric and barrier material within its package architecture. A POSITA would have recognized that forming a thin SiO_2 insulating layer beneath or within Yu's molding compound 18 would be a routine design choice consistent with Yu's own teaching of silicon oxide use throughout the package.

362. Second, a POSITA would have understood that incorporating an SiO_2 layer improves water-vapor and ion barrier performance relative to Yu's polymeric

molding compound. Water vapor permeability is a common problem in die encapsulation as greater water presence leads to increased oxidation, corrosion, and enhanced ion-movement. Yu teaches using silicone rubber and epoxy materials for molding compound 18. *EX1010* at 2:61-65. Combining these with a deposited SiO_2 layer, such as Lin-191's insulating layer 10, would reduce moisture diffusion, minimizing oxidation and corrosion of Yu's copper through-mold vias 38 and metallization layers 20, 24. Thus, the addition of an SiO_2 layer to Yu's package would reduce water vapor penetration, increasing the reliability of Yu's package. Additionally, because Yu's package contains multiple Cu interfaces within the molding compound and interposer, a POSITA would have recognized the benefit of adding a silicon dioxide barrier to increase reliability and prevent ion migration and delamination during thermal cycling. *See EX1010* at 3:5-18; 6:36-41.

363. Third, a POSITA would have appreciated that the SiO_2 layer would enhance electrical and thermal insulation between Yu's conductive structures without departing from Yu's process flow. Yu teaches depositing and curing polyimide and oxide-type dielectrics by CVD, spin-coat, or lamination processes throughout its ILD and RDL formation steps. *EX1010* at 3:21-32; 6:35-39. These are the same fabrication techniques Lin-191 teaches for forming its SiO_2 insulating layer. *EX1005* at [0050]. Accordingly, the addition of a SiO_2 film beneath Yu's

molding compound would have been straightforward and predictable for one of ordinary skill.

364. Thus, the Yu-Lin-191 combination represents the application of a known technique (silicon dioxide barrier layer) to a known device (Yu's chip package) ready for improvement to yield predictable results, i.e., a silicon dioxide layer on Yu's molding compound 10. The combination would result in reduced moisture permeation, improved dielectric strength, and enhanced thermal stability—using materials and processes explicitly taught in Yu. A POSITA would have had a reasonable expectation of success because Yu already uses SiO_2 layers in its carrier substrates and interposer structures, making integration of an SiO_2 compound within the molding system a predictable optimization. *EX1010* at 5:2-5; 6:35-39. Further, Lin-191 teaches layer 10 is formed via "a chemical-vapor deposition (CVD) process, a spin-coating process or a lamination process," which are all techniques also disclosed by Yu, making the modification simple and straightforward. *EX1005*, [0050]; *EX1010*, 7:16-18.

XII. OPINIONS REGARDING GROUND 2B: CLAIMS 6, 16, 18-21, AND 23 ARE OBVIOUS OVER YU, LIN-191, AND SUNDARAM

A. *Claim 6: "The chip package of claim 1, further comprising a second semiconductor chip under said first semiconductor chip, wherein said first semiconductor chip comprises a second metal pad on a top surface of said first semiconductor chip, a third metal pad on a bottom surface of said first semiconductor chip and a through-silicon-via metal layer connects to said second metal pad, wherein said third metal pad is connected to a fourth metal pad of said second semiconductor chip."*

a) Sundaram's Teachings and Motivation to Combine

365. Sundaram teaches Claim 6. *See* ¶¶ 193-199, incorporated herein. A POSITA would have been motivated to apply Sundaram's teachings to Yu such that Yu's die 52 (*first semiconductor chip*) comprises a *through-silicon-via metal layer* connecting *metal pad[s]* and Yu's package includes a *second semiconductor chip under said first semiconductor chip* and connected thereto by the *metal pad[s]*. Yu already teaches multiple chips in a chip package, motivating the combination. *EX1010* at FIG. 52.

366. A POSITA would have recognized that modifying Yu's die 52 to have a TSV connecting metal pads would have allowed for an additional chip (i.e., the *second semiconductor chip*) to be stacked thereon and electrically connected to die 52. Further, a POSITA would have recognized that Sundaram's teachings would enable the additional chip to be added to Yu's package without having to add an entire additional package 202. The ability to add just one additional chip to Yu's

package would have been desirable for applications merely requiring just one more chip and avoided a drastic increase in package size (i.e., because one chip would require less space than another package 202). Indeed, stacking chips in a chip package was known to be advantageous because package functionality would be increased "without increasing the footprint, or the area occupied on a circuit board, of the integrated circuit package." *EX1096* at 1:28-31. Moreover, modifying Yu's package to stack chips would have advantageously increased package density and shortened interconnects between chips in the package. For example, it was known that TSV's "which are vertical connections 'etched through the silicon wafer and filled with metal'" allows for "the addition of many more pathways between 2D layers" in a chip package." *EX1066* at [0017]. Additionally, by "using TSV technology, 3D ICs can pack a great deal of functionality into a small 'footprint.' Thus, critical electrical paths through the device can be drastically shortened, leading to faster operation." *EX1067* at [0005].

367. The modification is the application of a known technique (chip stacking, connecting metal pads with a TSV) to a known device (Yu's chip package) to yield the predictable result of Yu's package 202 having another chip under die 52 connected thereto by metal pads and a TSV. A POSITA would have had a reasonable expectation of success in modifying Yu-Lin-191, per Sundaram because, as I

described above, Sundaram's configuration represents a well-known method for enabling chip stacking and TSVs were common in chips by the time of the '763 Patent. *See* ¶ 196. Additionally, methods of forming both metal pads and TSVs were well known. For example, metal pads may be formed by "patterning with PVD, CVD, sputtering, electrolytic plating, electroless plating." *EX1006* at [0041]; *EX1042* at ("…filled with copper typically by an electroplating process, as known to one of ordinary skill in the art of integrated circuit fabrication."); *EX1043* at [0032] ("…variety of different deposition methods known by one of ordinary skill in the art, including but not limited to, CVD, pulsed CVD, PECVD, ALD, PEALD, or sputtering methods."). Further, "PVD, CVD, electrolytic plating, [or] electroless plating process" may be used to form a TSV *metal layer*. *EX1006* at [0043]. As such, the modification would have been simple and straightforward using techniques familiar to a POSITA, thus leading to a reasonable expectation of success.

B. *Claim 16: "The chip package of claim 1, further comprising a second semiconductor chip under said first interconnection scheme next to said first semiconductor chip."*

a) Sundaram's Teachings and Motivation to Combine

368. *See* ¶ 227, incorporated herein. A POSITA would have found it obvious and been motivated to modify the chip package of Yu-Lin-191 to further comprise a *second semiconductor chip* next to the *first semiconductor chip* based on the

teachings of Sundaram. The modification would have predictably improved Yu's chip package by enabling the addition of another chip without increasing the vertical extent of the package. That is, because a *second semiconductor chip* is positioned next to the *first semiconductor chip*, the overall height of the package is not increased in the way that it is when chips are vertically stacked. The ability to add additional functionality to a chip package without increasing the height of the chip package would have been desirable to a POSITA, as it was "desirable to minimize thickness of the chip scale package." *EX1068* at [0011]. Further, Sundaram expressly motivates the combination teaching that the side-by-side configuration overcomes a problem with adding "multiple dies over 4" in 3D ICs, meaning the ability to add a chips side-by-side overcame issues with stacking more than 4 dies on top of each other. *EX1004* at 7:59-60.

369. The combination is the application of a known technique (Sundaram's side-by-side configuration) to a known device (Yu's chip package) ready for improvement to yield the predictable results described above. Further, there would have been a reasonable expectation of success because the modification would have been simple and straightforward and merely required placing another chip adjacent to Yu's existing die 52 and connecting the chip to Yu's RDL using the same structures/techniques that Yu already teaches for connecting die 52 to the RDL (i.e.,

using connectors 54). Additionally, Yu already teaches connecting die 52 "through the opening 46" in ILD layer 44. *EX1010* at 4:30-34. Additional openings 48 are formed in ILD layer 44 such that a *second semiconductor chip* would be attached to Yu's RDL in the same manner as die 52. *EX1004* at 4:7-10, FIGS. 11-12. Because a *second semiconductor chip* would be attached in the same manner and using the same process, and because openings 48 are available for connecting another chip, there would have been a reasonable expectation of success.

C. *Claim 18*

1. 18(Pre): "A chip package comprising"

370. *See* Claim 1(Pre), ¶ 282 incorporated herein.

2. 18(a): "a solid layer having a first surface and a second surface opposite to said first surface,"

371. *See* Claim 1(a), ¶¶ 283-284, incorporated herein.

3. 18(a)(i): "wherein said solid layer comprises a compound of silicon and oxygen,"

372. *See* Claim 1(a)(ii), ¶ 286, incorporated herein.

4. 18(a)(ii): "wherein said solid layer has a thickness between 100 and 300 micrometers;"

373. *See* Claim 1(a)(iii), ¶¶ 287-294, incorporated herein.

5. 18(a)(iii): "wherein said solid comprises a first region and a second region between said first region and an edge of said solid layer;"

374. *See* Claim 1(a)(iv), ¶ 295, incorporated herein.

6. 18(b): "a plurality of metal conductors in said second region of said solid layer respectively,"

375. *See* Claim 1(b), ¶¶ 296, incorporated herein. Claim 18(b)'s *plurality of metal conductors* corresponds to Claim 1(b)'s *plurality of copper plugs*. Yu's TMVs 38 are *metal conductors* because they are made of copper which is a conductive *metal*.

7. 18(b)(i): "wherein one of said plurality of metal conductors comprises a copper portion and a first metal layer covering a sidewall of said copper portion, wherein said copper portion has a diameter in a direction between 50 and 200 micrometers and greater than a thickness of said first metal layer in said direction,"

376. As discussed, Yu's TMVs 38 (*metal conductors*) are formed by a copper "seed layer" deposited into "TMV openings 36" and a "conductive material, such as copper" deposited onto the copper seed layer. *EX1010* at 3:60–4:6; ¶¶ 296-297. The copper seed layer is a *first metal layer* and the copper deposited on the seed layer is a *copper portion*. Because the *copper portion* is deposited onto the seed layer, the *first metal layer cover[s] a sidewall of said copper portion*.

a) Sundaram's Teachings and MTC

377. Sundaram teaches or renders obvious Claim 18(b)(i), *see* ¶¶ 235-238, incorporated herein. The '763 Patent ascribes no criticality to the claimed *diameter*.

See ¶ 237. A POSITA would have been motivated and found it obvious to apply Sundaram's teachings to Yu's TMVs 38, resulting in *said copper portion having a diameter in a direction between 50 and 200 micrometers and greater than a thickness of said first metal layer in said direction*. Yu already teaches the *first metal layer* (copper seed layer) and *copper portion (*copper deposited onto the copper seed layer) such that the modification is simply the application of Sundaram's dimensions of the seed layer and copper portion to Yu's existing TMVs. Copper TMVs having Sundaram's diameter were common, as demonstrated by Sundaram.

378. It would have been advantageous to apply Sundaram's copper seed layer dimension to Yu's seed layer to reduce void formation in Yu's *copper portion*. Indeed, Sundaram expressly teaches such a seed layer thickness results in a "fast, void-free electroplating" process to "fill the vias with Cu." *EX1004* at 13:38-40. Because Yu's TMVs 38 similarly comprise a copper seed layer and electroplated copper, a POSITA would have appreciated the similarities and recognized that Sundaram's teachings were directly applicable to Yu's *first metal layer* and *copper portion*. The modification is the application of a known technique (Sundaram's *copper portion* dimensions) to a known device (Yu's TMV) ready for improvement to yield predictable results, i.e., Yu's copper portion of TMVs 38 having a diameter in a direction greater than a thickness of Yu's seed layer (*first metal layer*). There

would have been a reasonable expectation of success because Yu already teaches the claimed *first metal layer* and *copper portion* and Sundaram merely provides an express teaching of the commonly-used dimensions for metal conductors.

8. 18(b)(ii): "wherein said first region has a width in said direction greater than a shortest distance between a sidewall of one of said plurality of metal conductors and said edge of said solid layer in said direction and greater than a pitch between two neighboring metal conductors of said plurality of metal conductors;"

379. *See* Claim 1(b)(ii), ¶¶ 299-300, incorporated herein.

9. 18(c): "a first interconnection scheme over said first surface,"

380. *See* Claim 1(c), ¶ 301, incorporated herein.

10. 18(c)(i): "wherein said first interconnection scheme comprises a first metal interconnect over said first surface and a first polymer layer over said first metal interconnect,"

381. *See* Claim 1(c)(i), ¶¶ 302-305, incorporated herein.

11. 18(c)(ii): "wherein said first metal interconnect is connected to a first metal conductor of said plurality of metal conductors,"

382. *See* Claim 1(c)(ii), ¶ 306, incorporated herein. Claim 18(c)(ii)'s *first metal conductor* corresponds to Claim 1(c)(ii)'s *first copper plug*.

12. 18(c)(iii): "wherein said first metal interconnect comprises a first copper layer;"

383. *See* Claim 1(c)(iii), ¶ 307, incorporated herein. Claim 1(c)(iii)'s *second copper layer* corresponds to Claim 18(c)(iii)'s *first copper layer*.

13. 18(d): "a second interconnection scheme under said second surface,"

384. *See* Claim 8, ¶ 344, incorporated herein. Yu's *second interconnection scheme* is *under said second surface*:

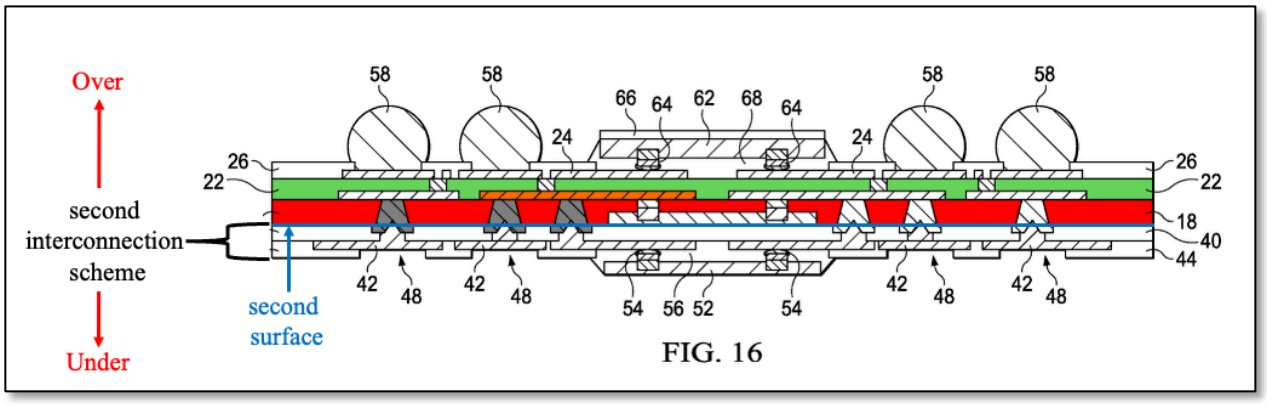


FIG. 16

EX1010 at FIG. 16.

14. 18(d)(i): "wherein said second interconnection scheme comprises a second metal interconnect under said second surface and a second polymer layer under said second metal interconnect,"

385. Yu teaches a "metallization layer 42" that is formed "in the same manner as the…metallization layers on the front side" (i.e., metallization layer 20) such that metallization layer 42, like layer 20, is formed of a copper seed layer and a copper portion (*metal*). *EX1010* at 4:9-14, 3:5-19; *see* ¶¶ 302-303. Thus, a portion of metallization layer 42 is a *second metal interconnect* that is part of the *second interconnection scheme* and *under said second surface*, as shown below.

386. Similarly, Yu teaches an ILD layer 44 that is formed "in the same manner as the ILD layers…on the front side" (i.e., ILD layers 22, 26) such that ILD layer 44, like layers 22, 26 is formed of a "polyimide" (i.e., is a *polymer layer*). *EX1010* at 4:9-14, 3:22-23; *see* ¶¶ 304-305. As shown, the ILD layer 44 is a *second polymer layer under said second metal interconnect*:

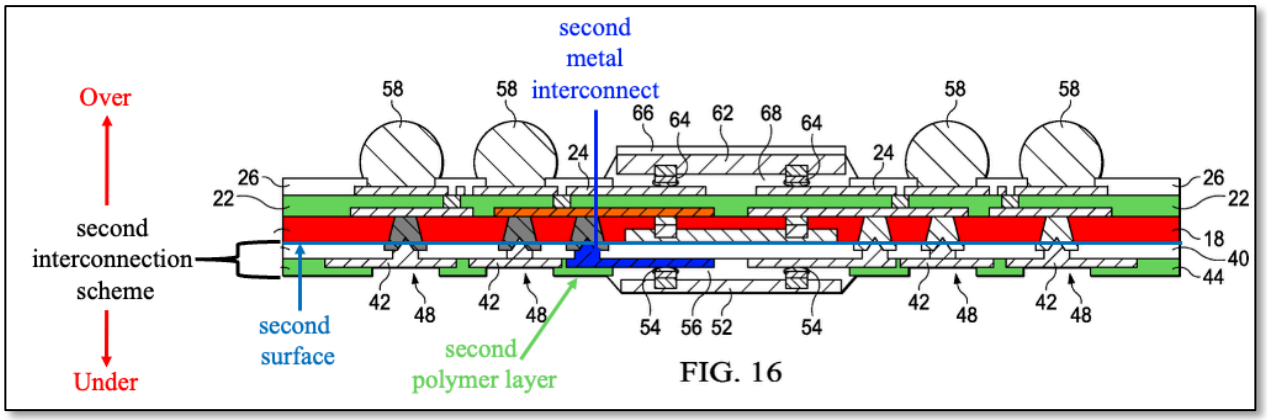


FIG. 16

EX1010 at FIG. 16.

15. 18(d)(ii): "wherein said second metal interconnect is connected to a second metal conductor of said plurality of metal conductors,"

387. As shown below, Yu's *second metal interconnect is connected to a second metal conductor of said plurality of metal conductors*:

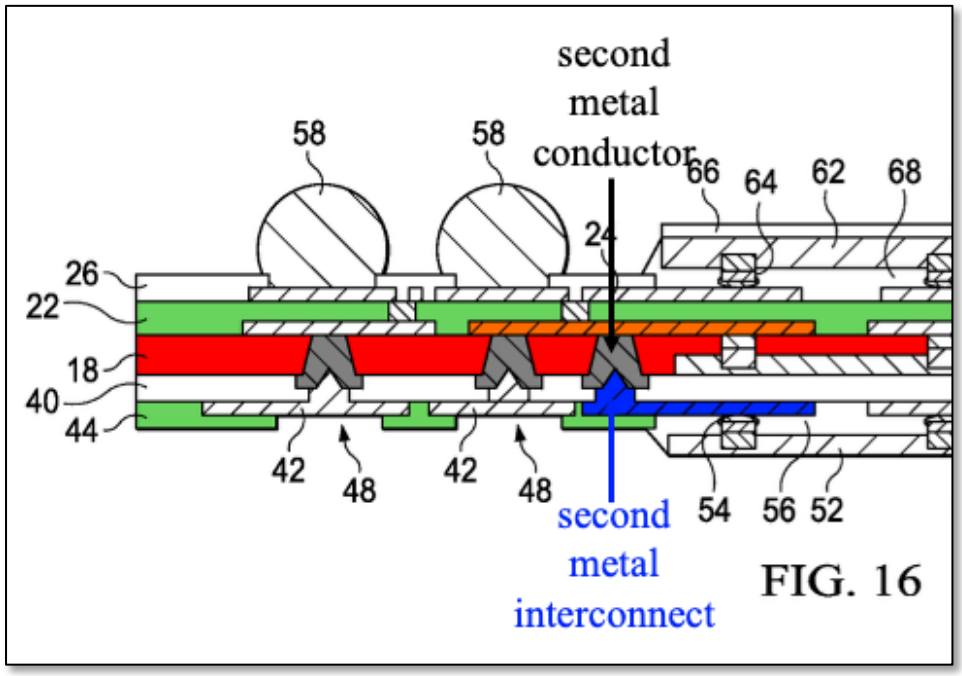


FIG. 16

EX1010 at FIG. 16; *see also* FIGS. 7-8 (depicting layer 42 being formed on TMVs 38), 4:7-17).

16. 18(d)(iii): "wherein said second metal interconnect comprises a second copper layer; and"

388. As I discussed above, Yu's *second metal interconnect* is a portion of metallization layer 42 that is that is formed "in the same manner as the…metallization layers on the front side" (i.e., metallization layer 20) such that metallization layer 42, like layer 20, is formed of a copper seed layer and a copper portion. *EX1010* at 4:9-14, 3:5-19; *see* ¶¶ 302-303, 385. Because Yu's *second metal interconnect* comprises an electroplated copper layer, the *second metal interconnect comprises a second copper layer*.

17. 18(e): "a first semiconductor chip under said first interconnection scheme,"

389. *See* Claim 1(e), ¶ 315, incorporated herein.

18. 18(e)(i): "wherein said first semiconductor chip comprises a first metal bump on a first metal pad of said first semiconductor chip,"

390. *See* Claim 1(e)(i), ¶¶ 316-318, incorporated herein. Claim 1(e)(i)'s *third metal interconnect* corresponds to Claim 18(e)(i)'s *first metal bump*. Petitioners point to another connector 54 as the *first metal bump*:

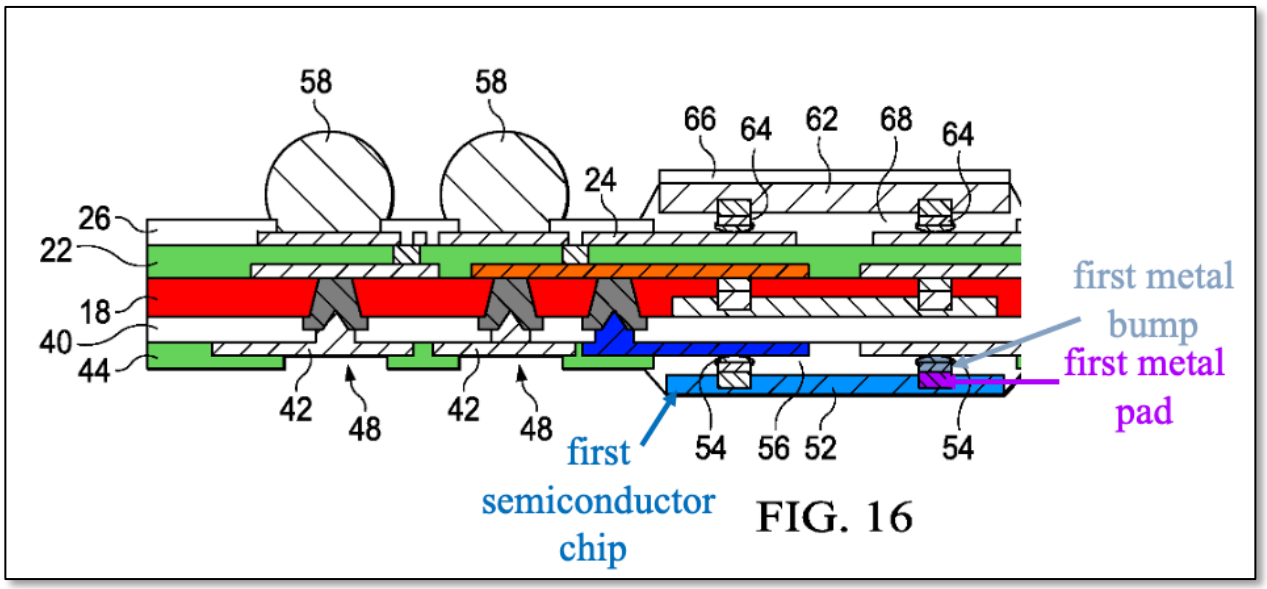


FIG. 16

EX1010 at FIG. 16 (excerpt).

19. 18(e)(ii): "wherein said first metal bump comprises a third copper layer with a thickness between 5 and 30 micrometers,"

391. *See* Claim 1(e)(ii), ¶¶ 322-323, incorporated herein. Claim 18(e)(ii)'s *first metal bump* and *third copper layer* correspond to Claim 1(e)(ii)'s *third metal interconnect* and *third copper layer*, respectively.

20. 18(e)(iii): "wherein said first semiconductor chip is connected to a third metal interconnect of said second interconnection scheme through said first metal bump."

392. Yu's die 52 is *connected to* another portion of layer 42 (*third metal interconnect*) *through said first metal bump* (connector 54), shown below. Indeed, Yu teaches that die 52 "is attached…to conductive features in the second backside metallization layer 42" *(third metal interconnect*) by "connectors 54[.]" *EX1010* at 4:30-33.

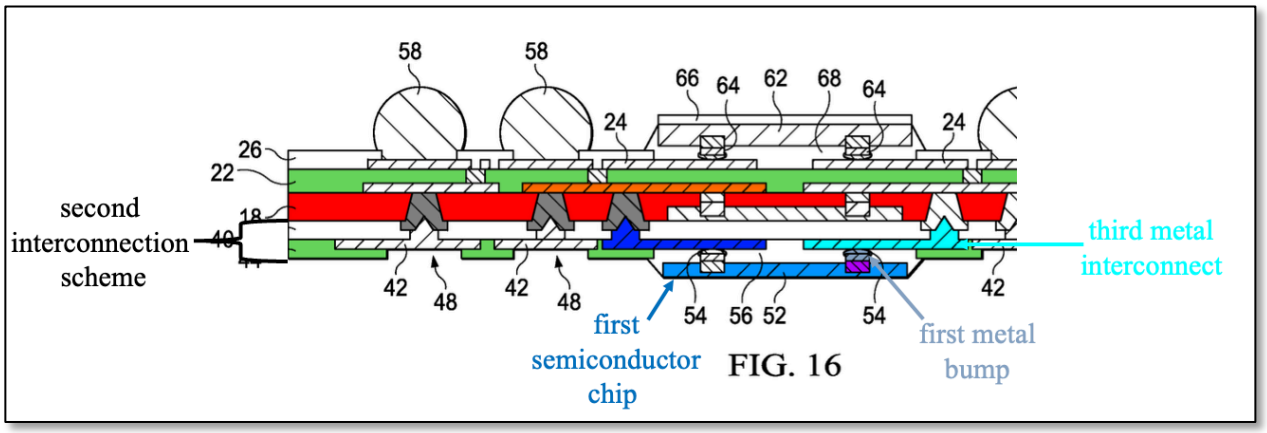


FIG. 16

EX1010 at FIG. 16.

D. *Claim 19: "The chip package of claim 18, wherein said compound comprises a SiO_2 compound."*

393. *See* ¶¶ 358-364, incorporated herein.

E. ***Claim 20: "The chip package of claim 18, further comprising a first passive component under said first interconnection scheme."***

394. *See* ¶¶ 325-328, incorporated herein. The motivation to combine and reasonable expectation of success that I described above at claim 2 are incorporated herein. *See* ¶¶ 329-330, incorporated herein. Additionally, a POSITA would have been motivated to add a passive component *under* Yu's *first interconnection scheme* because the by having the passive component, such as a capacitor, near die 52, the quality of signals output from die 52 would be improved, as the passive component becomes part of the circuit. The *passive component* (e.g., capacitor) *under* would be more effective at filtering out high frequency interference (e.g., HFI generated by die 52 itself) due to the physical proximity between die 52 and the capacitor.

F. ***Claim 21: "The chip package of claim 18, wherein said first semiconductor chip comprises a central-processing-unit (CPU) circuit block and a graphics-processing-unit (GPU) circuit block."***

395. *See* Claim 5, ¶ 335, incorporated herein.

G. ***Claim 23: "The chip package of claim 18, wherein said solid layer further comprises a third region opposite to said second region, wherein said third region is between said first region and another edge of said solid layer, wherein said plurality of metal conductors in said third region."***

396. *See* Claim 10, ¶ 346, incorporated herein.

XIII. OPINIONS REGARDING GROUND 2C: CLAIM 13 IS OBVIOUS OVER YU, LIN-191, AND LIN-863.

A. *Claim 13: "The chip package of claim 1, wherein said second region is a rectangle region and surrounding said first region."*

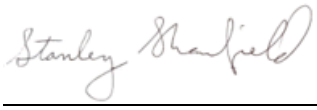
397. Lin-863 teaches Claim 13. *See* ¶ 264. The MTCs and reasonable expectation of success for Sundaram-Lin-863 apply equally to Yu-Lin-863. Further evidencing the reasonable expectation of success, Yu, like Lin-863, teaches both an encapsulated die 10 and a Package-on-Package (PoP) structure. *EX1010* at 2:41–65, 8:6–15. Yu describes that "package 202 comprises a first die encased in molding compound 18" and that "multiple packages 202 can be stacked in the PoP structure," where each stacked package contains redistribution layers and through-mold vias interconnecting multiple metallization levels. *EX1010* at 8:7–13, 8:35–392.

398. A POSITA would have recognized that Yu's encapsulated, multi-layered package corresponds closely to Lin-863's fan-out package structure, which likewise integrates encapsulated dies, redistribution layers, and vertical interconnections. Because Yu already teaches encapsulated dies and stacked PoP assemblies using redistribution and metallization layers, applying Lin-863's fan-out teachings, such as external redistribution and connection routing, would have been a straightforward and predictable modification to Yu's similar chip package. The integration would simply extend Yu's existing fan-out design principles, yielding an

expected enhancement in interconnect density and packaging flexibility. *Compare EX1007* at 11:47–48, FIGS. 6A–7 *with EX1010* at FIG. 52.

XIV. CONCLUSION

399. I declare that all statements made herein of my knowledge are true, and that all statements made on information and belief are believed to be true, and that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Dated: November 21, 2025 By: 

Stanley Shanfield, Ph.D.

Stanley Shanfield



Curriculum Vitae for Stanley Shanfield

Education:

Massachusetts Institute of Technology, Ph.D., Physics, 1981

University of California, Irvine, B.S. Cum Laude, Physics, 1977

Educational Awards:

Outstanding Research Project, U.C. Regents Award, 1977

Phi Beta Kappa, 1977

Four Year Scholarship, Tuition & Research, ERDA/DOE, 1977-1981

Hands-On Professional Expertise:

Semiconductor Physics & Chemistry
Semiconductor Fabrication: Silicon and III-V Materials
Semiconductor Device & Integrated Circuit Engineering
Semiconductor Equipment: Front & Back End
Semiconductor Packaging Design and Manufacturing
Passive Component Design and Manufacturing
RF Design and Fabrication
Digital Design & Fabrication
Semiconductor Manufacturing in Silicon and III-V Materials
MEMS Design and Fabrication: Electrical, Optical, & Sensing Devices
Fiber Optic Device Design and Fabrication
Integrated Optics & Electro-Optical Devices
Plasma Physics

Specialized Training:

Global Positioning Electronics, Systems and Components
Six Sigma Semiconductor Manufacturing
Microwave Engineering
US Patent Law in Technology
Patent Application and Prosecution
Semiconductor Plasma Processing
Thin Film Physics and Technology
MEMS-based Gyroscopes and Accelerometers
Thermoelectric Materials & Technology
Phased Array Radar Engineering
Antennas and Electromagnetic Propagation
Solid State Optical Devices
Fiber Optic Communication System Operation
HALT and HAST Reliability Testing Methods

Professional Experience:

Draper Laboratory Cambridge, MA ***2003 – present***

Division Leader, Advanced Hardware Development
Distinguished Member of Technical Staff
Technical Director

Led division (about 80 staff) in re-invigorating multi-chip integrated circuit module facility, more than doubling associated revenues in two years. By most accounts, made division a viable business & technological entity again. Invented & led implementation of an ultra-miniature electronics fabrication technology which became a top laboratory priority. Led team in realization & fabrication of a newly designed precision MEMS-based gyroscope and associated ASIC. Found funding and led team in developing a miniature power source with energy density at least two orders of magnitude higher than any source previously built. Developed fabrication technology for semiconductor-based low phase noise oscillator design, allowing for receiver operation with extremely low signal strength. Many awards received, most recently, the Draper 2010 Distinguished Performance Award, and 2010 Best Patent Award.

Clarendon Photonics Newton, MA ***2001 – 2003***

Director, Packaging & Integration

30 person photonic chip startup with $18 million 2nd round funding. Invented and productized new, low cost and reliable semiconductor processing, packaging and pig-tailing technology for optical add-drop multiplexer. Established assembly and packaging process, and developed control electronics. Partner with Micron Technologies, using their R&D semiconductor facility.

AXSUN Technologies Bedford/Billerica, MA ***1999 – 2001***

Vice President, Operations
1999 – 2000

Initially three staff members with $6 million funding. Designed, fabricated and productized AXSUN's micro-electromechanical (MEM) Fabry-Perot optical filter. Patents granted on semiconductor processing and control electronics. Completed facility and semiconductor processing design, then completely equipped. Raised 2nd round funding for $36 million. Established process and fabrication facility in Belfast, Northern Ireland for producing thick oxide silicon-on-insulator material.

Director, Manufacturing & Wafer Fab Technology **2000 – 2001**

After 3rd round funding, led device manufacturing, creating wafer fab and assembly infrastructure; hired 70+ people, led production. Delivered first generation product for revenue to multiple customers. Converted pure technology to dominant company revenue with high yield.

Company purchased by Volcano Technologies, San Diego.

Raytheon Corporation Lexington/Andover, MA ***1985 - 1999***

Manager, Semiconductor Operations **1996 – 1999**

Built and led a 300 employee, $60 million revenue 24/7 semiconductor development and manufacturing operation resulting from the consolidation of a number of smaller organizations. Key player in technological development and recipient of Raytheon's 6 Sigma Leadership training. Decision maker in Texas Instrument group acquisition, providing significant expert opinion on semiconductor and design facilities. Obtained state-of-art yields using best available steppers, deep reactive ion etching, plasma assisted CVD, and ion-implantation equipment, and disciplined design-for steppers, deep reactive ion etching, plasma assisted CVD, and ion-implantation equipment, and disciplined design-for-manufacturing
circuit design and layout methodology.

Research Laboratory Manager **1992 – 1996**

Leader of a 90 employee development and contract research organization in high performance semiconductor devices and circuits, measurement, assembly and wafer fab. Led a team which invented and implemented a major revenue generating technology (.$100 million) based on semiconductor device development (pseudomorphic high electron mobility transistor). Increased outside research funding by 50% in 3 years through superior technical performance relative
to competitors.

Section Manager, Semiconductors & ICs **1985 – 1992**

Led a MM-Wave Circuit and Module Development program over 2 years, leading to production win of a satellite terminal electronics generating $320 million in sales. Developed processes for fabricating high power, high frequency multi-function integrated circuits, and combining high performance digital and analog devices in a single integrated circuit.

Spire Corporation Bedford, MA ***1981 – 1984***

Staff Scientist
Senior Staff Scientist

Developed new methods for low temperature deposition of plasma-assisted CVD epitaxial silicon. Wrote joint papers with MIT professor, and had process adopted by equipment manufacturers. Built, operated and characterized ion-assisted deposition system for making coating for semiconductor and machine tool industries. Process eventually purchased by Kennametal, Inc.

Publications

Restricted Publications & Reports

Process Sequence for Formation of Ultra-High Density Multi-Chip Modules:
A high yield, low cost method for creating a system-in-a-package consisting of numerous semiconductor die, passive components, and sensors. Process formed basis for new (2008) facility.

Design and Method of Fabrication of Ultra-High Density Radioisotope Power Source:
In test, a miniature power source that achieves energy density more than 1000X the best chemical battery. Method uses planar semiconductor processing of bulk thermoelectric materials.

Design and Method of Achieving Extremely Low Crystal Oscillator Phase Noise:
Method developed for very low power refrigeration of quartz or sapphire crystal resonators, resulting in extremely low phase noise oscillators. The low phase noise allows extremely high sensitivity in digital receivers, including GPS receivers, leading to use in extremely low signal conditions.

Design, Evaluation & Production of MEMS-based Fabry-Perot Interferometer:
Design and method for ultra-compact spectral analyzer made using semiconductor and optical thin film processing.

Design & Evaluation of Ultra-Fast Control Electronics for Integrated Optical Multiplexer:
Design and performance evaluation of silicon-based integrated optical multiplexer using chip-based local heating

Design and Fabrication of Q-band MILSTAR Communications Terminal Transmitter:
Record power and efficiency 44 GHz transmitter design using new transistor design, and combined waveguide

Key Publications (selected)

Process Characterization of PSG and BPSG Plasma Deposition, J. Electrochem. Soc., Volume 131, Issue 9, pp. 2202-2203

A double-recessed Al0.24GaAs/In0.16GaAs pseudomorphic HEMT for Ka- and Q-band power Applications, Electron Device Letters, IEEE, Volume 14, Issue 9, pp. 456 - 458

Formation of Thick Metal Structures on GaAs MMICs Using Image Reversal Lithography and Evaporated Metal Deposition, J. Electrochem. Soc., Volume 136, Issue 9, pp. 2687-2690

Contact Hole Etching in Load-Locked Hexagonal Reactive Ion Etch System, J. Electrochem. Soc., Vol. 131, No. 8, 1984

An AlGaAs/InGaAs pseudomorphic high electron mobility transistor with Improved Breakdown Voltage for X and Ku-band power applications, Microwave Theory and Techniques, IEEE Transactions on, Volume 41, Issue 5, May 1993, pp. 752 - 759

Hot-electron-induced Degradation of Metal-Semiconductor Field-Effect Transistors, Integrated Circuit Symposium, 1994. Technical Digest 1994., 16th Annual Volume , Issue , 16-19 Oct. 1994, pp. 259

Ion Beam Deposition of Cubic Boron Nitride, J. Vac. Sci. Technol. A Volume 1, Issue 2, pp. 323-325

Patents

US Patent 6504235 - **Passivation layer and process for semiconductor devices**
Method of coating semiconductor devices that prevented parametric shift in electrical performance. Solved key processing problem.

US Patent 4440108 - **Ion Beam Deposition Apparatus**
Design of equipment for deposition of thin films in the presence of ion bombardment. System produced thin films of interest for mechanical, electrical and optical properties and was sold as an equipment product.

US Patent 6525880 - **Integrated Tunable Fabry-Perot filter and Method of Making Same**

Design and method for fabricating very small, very high performance variable optical filter using semiconductor fabrication technology. In current use in fiber optical networks, chemical sensors, and 3-D medical imaging applications.

US Patent 5175020 - **Boron Nitride Films and Process of Making Same**
Ion assisted deposition of ultra-hard cubic boron nitride films for semiconductor and machine tool applications. Significant use in both areas.

US Patent 4526673 - **Coating Method**
Method for deposition of thin films used in semiconductor device fabrication. Method based on direct control of the kinetics of thin film deposition.

US Patent 7727806 - **Systems and Methods for High Density Multi-Component Modules**
Method for fabrication of electronic modules using multiple thinned integrated circuits, patterned multi-level interconnects, passive electronic components, and sensors

US Patent Application 2009/TBD - **Devices, systems, and methods for controlling the temperature of resonant elements**
Devices and systems for achieving low phase noise crystal oscillators using unique low power thermoelectric structures

Expert Witness Experience:

See attachment

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Newton, MA 02465

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Email: shanfield@alum.mit.edu