UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY LTD.,

and

APPLE INC.,
Petitioners

v.

MYW SEMITECH, LLC,
Patent Owner

Inter Partes Review Case No. IPR2026-00066
U.S. Patent No. 11,538,763

PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 11,538,763

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I. INTRODUCTION

IPR is requested of claims 1-23 of USPN 11,538,763. The '763 Patent claims a chip package comprising various well-known components of semiconductor and chip packaging designs. Neither the claimed components nor their claimed configuration is new or non-obvious.

II. LEVEL OF ORDINARY SKILL IN THE ART

A POSITA at the time of the '763 Patent would have had at least a bachelor's degree in electrical engineering, materials science, or physics (or an equivalent degree), and at least two years of experience in semiconductors or semiconductor manufacturing. A master's degree or Ph.D. in a relevant field may substitute for some work experience or vice versa. Additional education or experience might substitute for the above requirements.

III. REQUIREMENTS UNDER 37 C.F.R. § 42.104

A. Grounds for Standing Under 37 C.F.R. § 42.104(a)

Petitioners certify the '763 Patent is eligible for IPR.

B. Identification of Challenge Under 37 C.F.R. § 42.104(b)

Petitioners request the Challenged Claims be found unpatentable on the following grounds.[1]

[1] All references qualify as prior art under at least one of pre-AIA §§102(a)-(b) or (e).

Grounds	Claims Challenged	35 U.S.C. §	References
1A	1-12, 14, 16-21, 23	103	Sundaram (EX1004) and Lin-191 (EX1005)
1B	13, 15	103	Sundaram, Lin-191, and Lin-863 (EX1007)
1C	22	103	Sundaram, Lin-191, and Lin-691 (EX1008)
1D	22	103	Sundaram, Lin-191, and Shenoy (EX1011)
2A	1-5, 7-12, 14-15, 17	103	Yu (EX1010) and Lin-191
2B	6, 16, 18-21, 23	103	Yu, Lin-191, and Sundaram
2C	13	103	Yu, Lin-191, and Lin-863

C. Claim Construction Under 37 C.F.R. § 42.104(b)(3)

For this IPR only, claim construction is unnecessary because, as set forth herein, the prior art falls within the indisputable scope of the Challenged Claims under any reasonable construction (including any proposed in litigation).

IV. ANALOGOUS PRIOR ART

The prior art is analogous to the claimed invention of the '763 Patent. The prior art is from the same field of endeavor of the '763 Patent, namely semiconductor packaging. *EX1001*, 1:27-67, 3:34-37, 14:12-13; *EX1004*, 1:33-42, 5:16-19, 7:61-67; *EX1005*, [0003], [0007]; *EX1007*, 1:7-10, 1:14–2:25; *EX1008*, [0002]-[0004]; *EX1010*, Abstract, 1:10-55, 1:63-67, 4:17-20; *EX1011*, [0001], [0029-0030]; *EX1003*, ¶¶31-33, 93, 102, 112, 117, 124.

The prior art is also reasonably pertinent to at least one purported problem identified in the '763 Patent, namely:

A. Minimizing temperature coefficient of expansion mismatching; *EX1001*, 1:62-63; *EX1004*, 5:62-63; *EX1007*, 2:29-48, 11:20-46, 12:11-32, 14:43-65; *EX1011*, [0042]; *EX1010*, 6:20-26;

B. Creating chip packages with pre-testability capability; *EX1001*, 1:61-62; *EX1004*, 7:41-43, 2:34-35; *EX1005*, [0006], [0105], [0173], [0239], [0401], [0462], [0492-0493]; *EX1010*, 2:17-20; and/or

C. The impact of miniaturization on circuit performance; *EX1001*, 1:34-38; *EX1004*, 1:15-32, 2:21–3:6; *EX1008*, [0001]-[0004]; *EX1003*, ¶¶34-38, 94, 103, 113, 118, 125.

V. GROUND 1A: CLAIMS 1-12, 14, 16-21, AND 23 ARE OBVIOUS OVER SUNDARAM AND LIN-191

A. Claim 1

1. 1(Pre)

Sundaram teaches a *chip package*[2] formed by an "interconnect structure 100 compris[ing] an interposer 105" that interconnects a "first electronic device 125"

[2] Claim language provided in italics. All drawing annotations added. Citations to a claim limitation and/or section number are to the limitations mapping in this Petition and are incorporated by reference, including the motivations to combine (MTC) and

and a "second electronic device 130." *EX1004*, 5:45-58, 6:34-46 (devices 125, 130 are chips), FIG. 33. The interconnect structure 100 "enables the interposer 105 and the **package** can [*sic*] be one and the same." *EX1004*, 7:61-63.

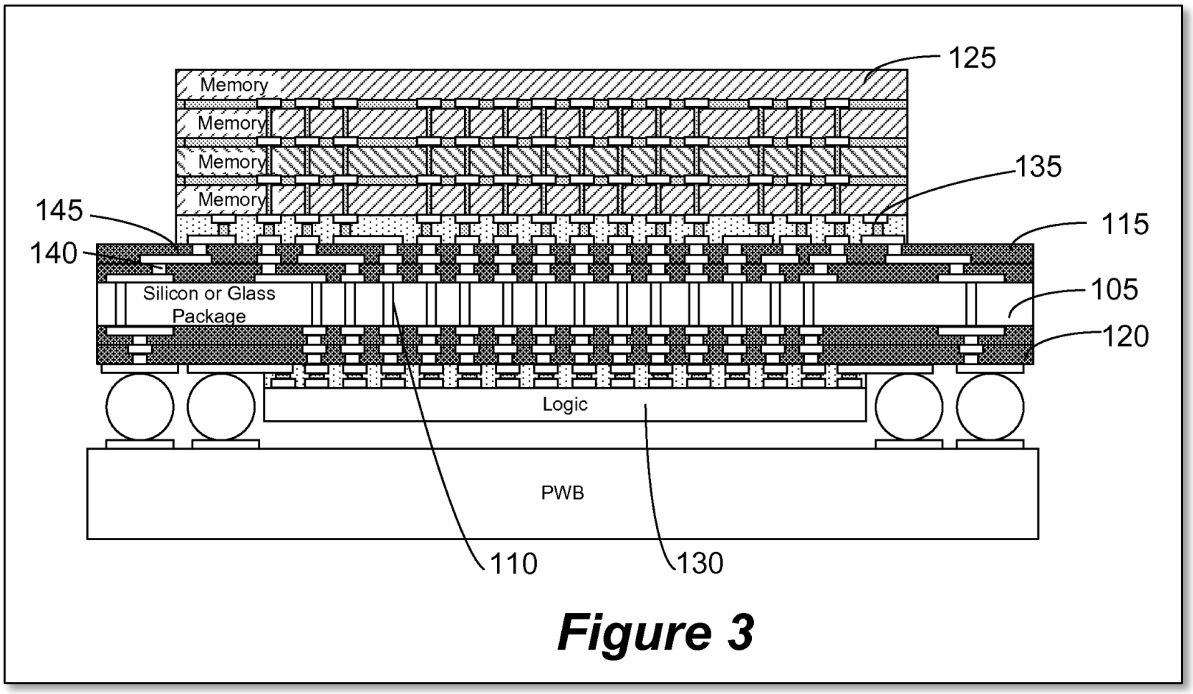


Figure 3

EX1004, FIG. 3; *EX1003*, ¶127.

2. 1(a)

Sundaram's interconnect structure "comprises an interposer [105] having a first side and a second side" (*a first surface and a second surface*) and is "made

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showing of reasonable expectation of success (REOS) provided in the cross-referenced section. All REOS include the benefits described for the respective MTC. All emphases added unless otherwise noted.

of…glass" or "polymer-glass laminates," such that interposer 105 is a *solid layer*. *EX1004*, 2:22-27, 5:54-58. Shown in FIG. 3, below, Sundaram's *second surface* is *opposite to said first surface*.

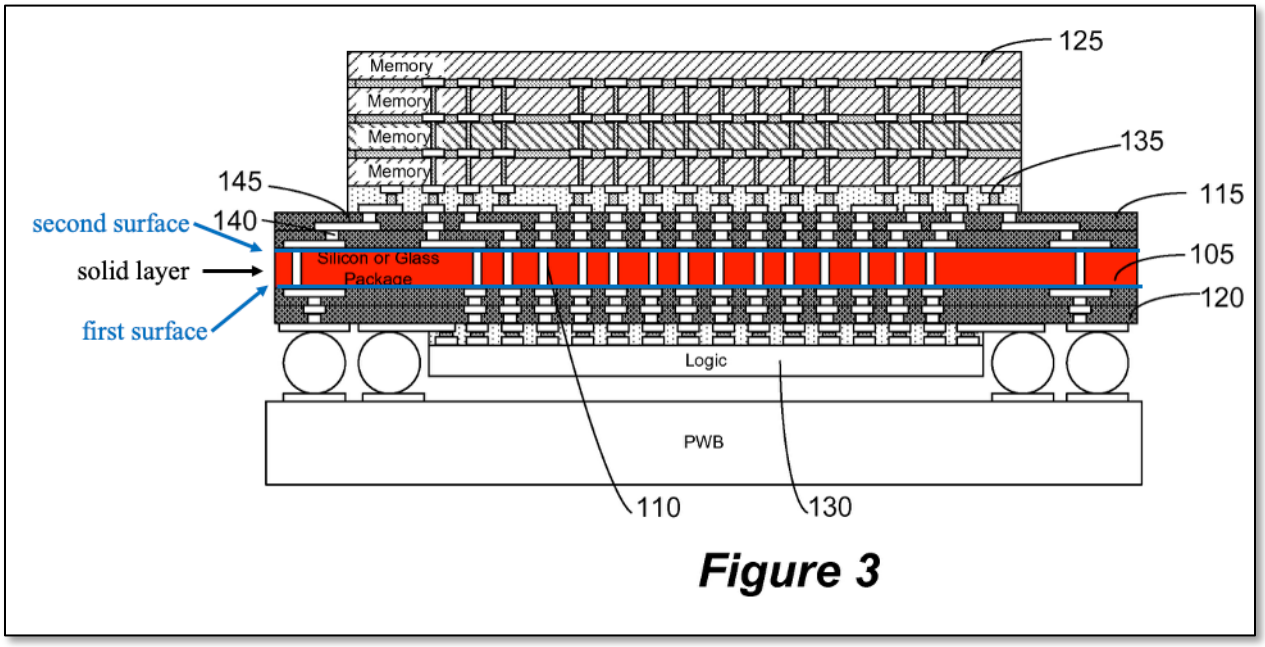


Figure 3

EX1004, FIG. 3; *EX1003*, ¶¶128-129.

3. 1(a)(i)

Sundaram's *first surface is substantially parallel to said second surface*.

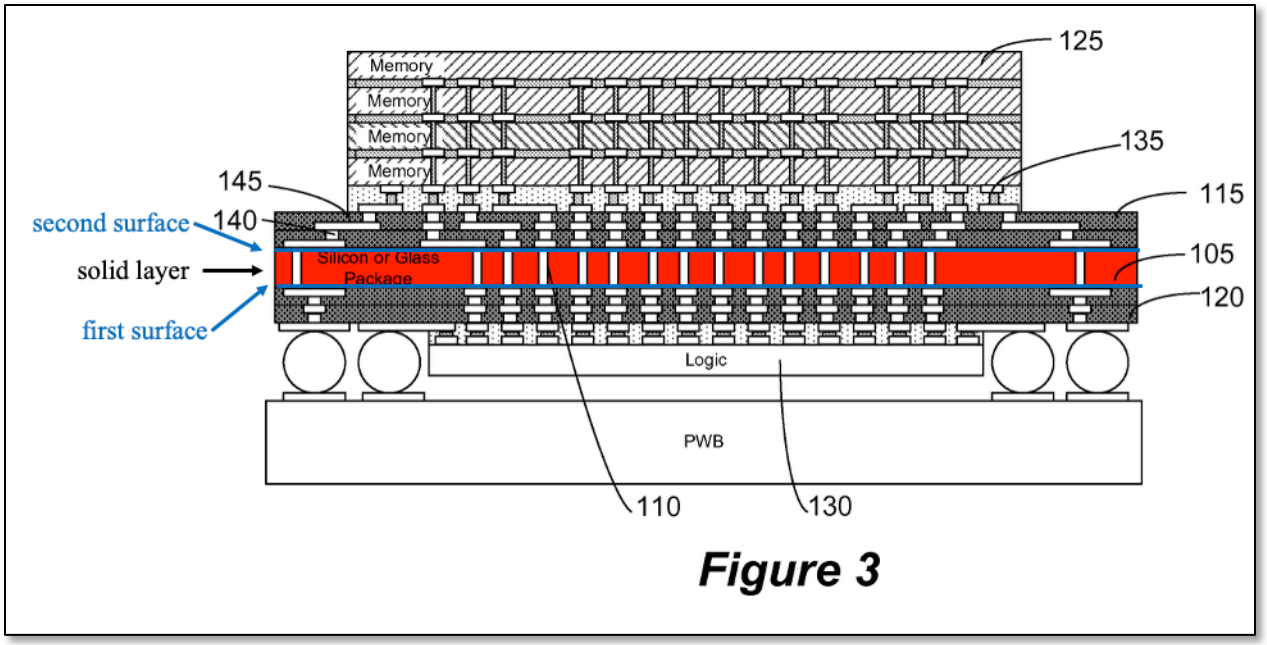


Figure 3

EX1004, FIG. 3; *EX1003*, ¶130.

4. 1(a)(ii)

Interposer 105 comprises "glass," i.e., *a compound of silicon and oxygen*. *EX1004*, 5:54-58, 9:14-16 (borosilicate glass); *EX1003*, ¶131.

Alternatively, Sundaram teaches interposer 105 comprises "silicon" with an SiO_2 layer. *EX1004*, 5:54-58, 14:58-62.

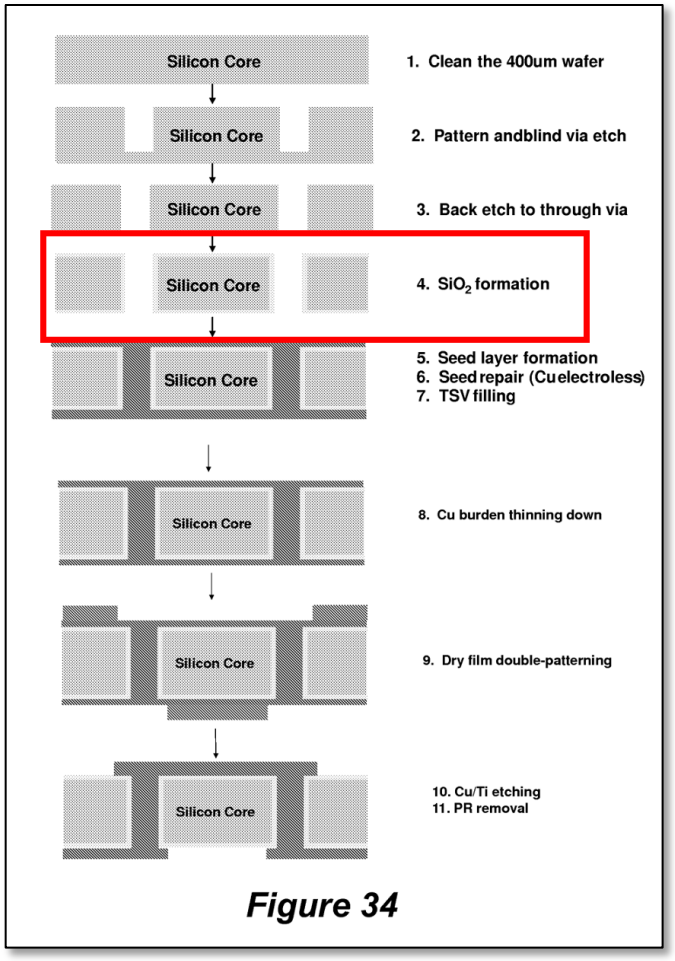


Figure 34

EX1004, FIG. 34; *EX1003*, ¶132.

5. 1(a)(iii)

Sundaram teaches or renders obvious the claimed thickness. Sundaram teaches interposer 105 (*solid layer*) is "about 20 to about 200 micrometers in thickness," which overlaps with the claimed *thickness* range. *EX1004*, 2:22-25, 14:34-36; *EX1003*, ¶133. Additionally, the '763 Patent does not ascribe any criticality to the claimed range of 100 and 300 micrometers. Indeed the '763 Patent describes a variety of ranges, including smaller (20 micrometers) and much larger

values (2000 micrometers), indicating to a POSITA that the thickness can vary widely and that the thickness is not otherwise critical. *EX1001*, 7:54-60; *EX1003*, ¶135; *Clearvalue, Inc. v. Pearl River Polymers, Inc.*, 668 F.3d 1340, 1345 (Fed. Cir. 2012) (finding the prior art reference's teaching of "150 ppm or less" anticipated claimed "less than or equal to 50 ppm" where the challenged patent did not indicate criticality of the claimed range); MPEP 2131.03(II); *UCB Inc., et al. v. Actavis Labs. UT, Inc., et al.*, 65 F.4th 679, 689-90 (Fed. Cir. 2023) ("A presumption of obviousness applies '[w]here a claimed range overlaps with a range disclosed in the prior art.'" (quoting *Ormco Corp. v. Align Tech., Inc*., 463 F.3d 1299, 1311 (Fed. Cir. 2006)); MPEP 2144.05.

Sundaram also teaches an embodiment where a glass interposer has a thickness of 175 micrometers, which is a specific point within the claimed range of *between 100 and 300 micrometers*, further teaching the claimed range. *EX1003*, ¶134; *UCB*, 65 F.4th at 687 ("If the prior art discloses a point within the claimed range, the prior art anticipates the claim"); MPEP 2131.03(I).

6. 1(a)(iv)

Sundaram's interposer 105 includes *a first region* and *a second region between said first region and an edge of said solid layer* as shown:

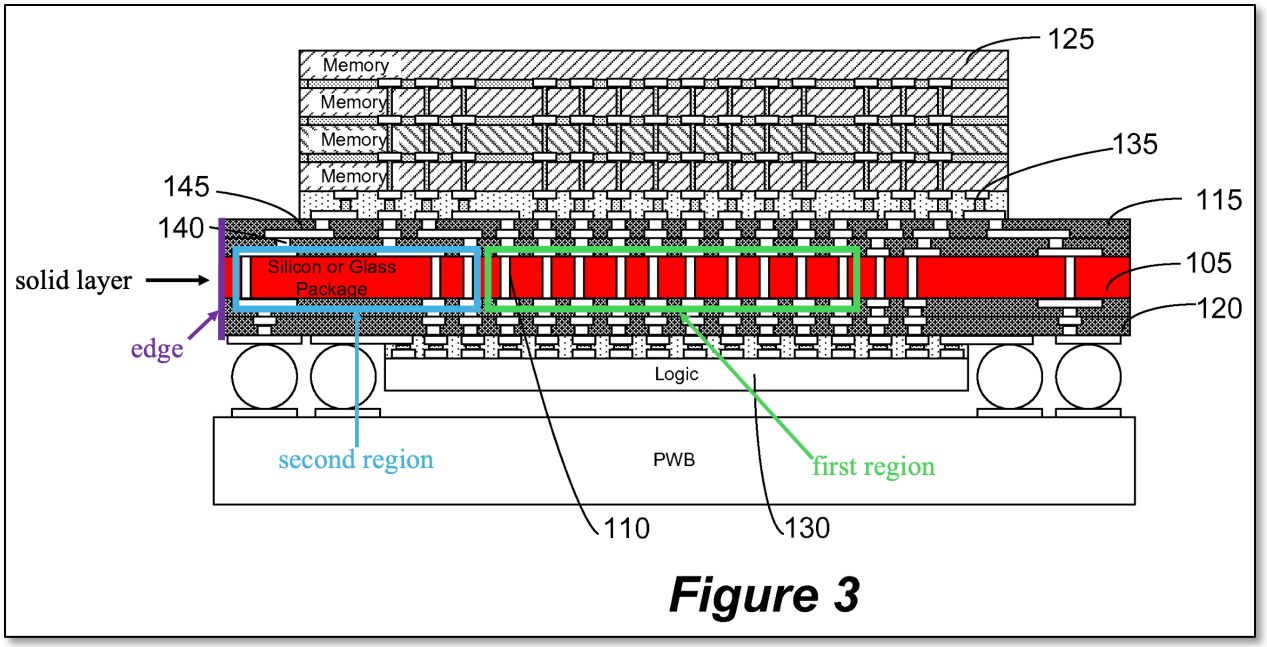


Figure 3

EX1004, FIG. 3; *EX1003*, ¶136.

7. 1(b)

Sundaram teaches a *plurality of copper plugs in a plurality of through vias*, i.e., copper metalized through vias 110 where the copper metallization forms *copper plugs* that are in *through vias*. Specifically, Sundaram teaches "through vias 110 can be defined within the interposer" and "metalized with a highly-conductive metal, for example **copper**." *EX1004*, 6:6-9, 6:25-27, 13:30-34. Through vias 110 are *in said second region*:

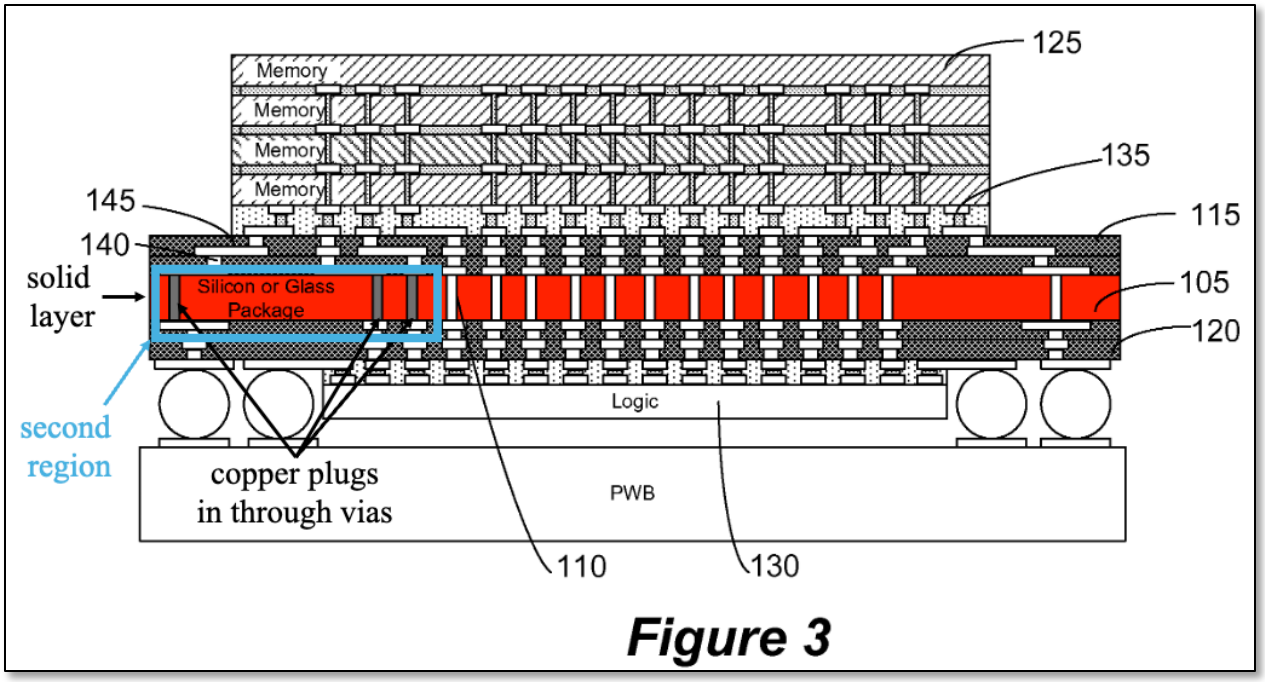


Figure 3

EX1004, FIG. 3; *EX1003*, *EX1003*, ¶137.

8. 1(b)(i)

Sundaram teaches "metaliz[ing]" the through vias 110 with copper such that *one of said plurality of copper plugs comprises a first copper layer contacting a sidewall of* a through via 110. *EX1004*, 6:22-27, 13:30-34; *EX1003*, ¶¶138-139.

9. 1(b)(ii)

See Section V.A.6. The claimed *regions* are not described in the '763 Patent's written description. Applicant relied solely on Applicant-annotated FIG. 6l as support during original examination, illustrating the claimed *width*, *shortest distance*, and *pitch*.

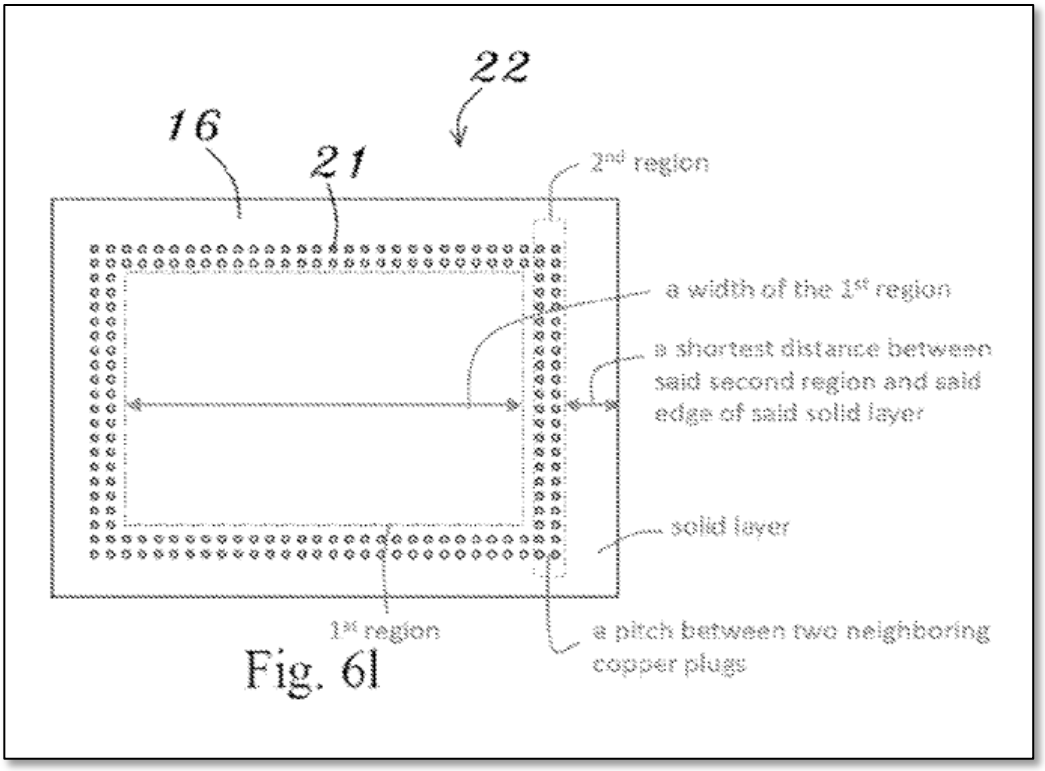


Fig. 6I

EX1002, 272; *EX1003*, ¶141.

Sundaram, including Sundaram's figures, similarly teaches the claimed *regions*. As shown below, Sundaram's *first region has a width in a direction* (denoted D1) that is *greater than a shortest distance between said sidewall of one of said plurality of through vias and said edge…in said direction* (denoted D2), and *a pitch between two neighboring copper plugs* (denoted D3):

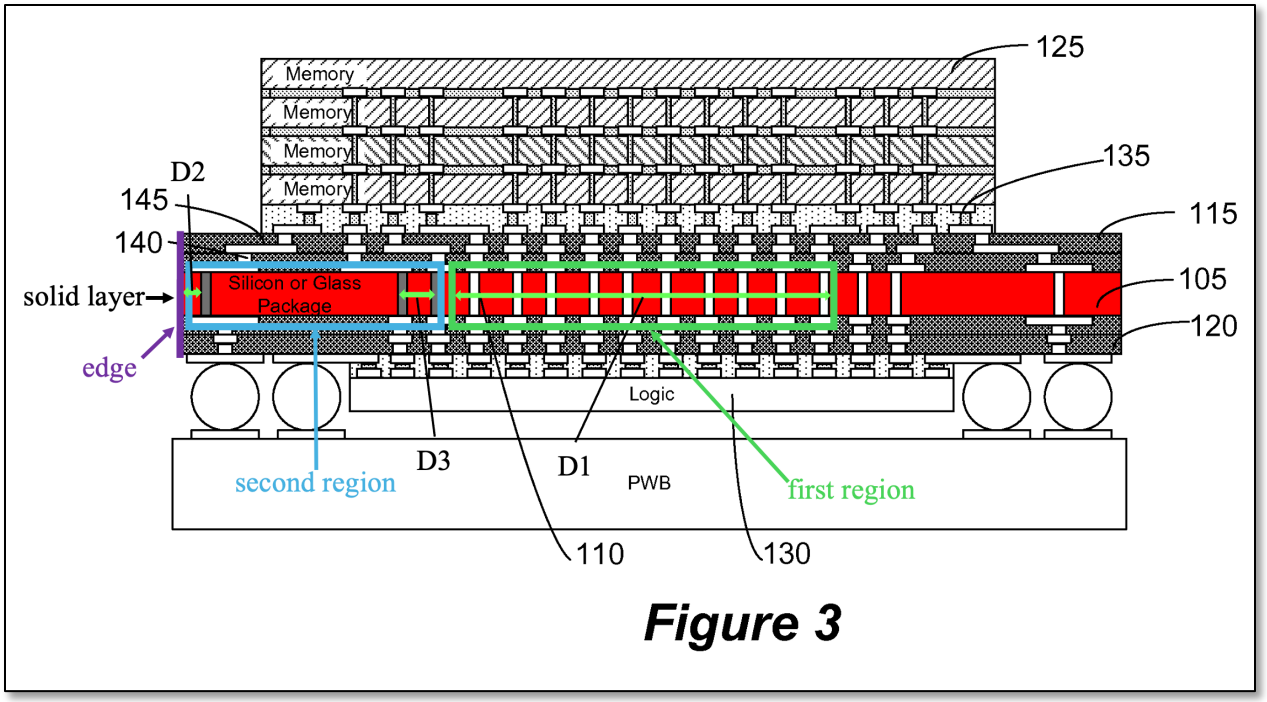


Figure 3

EX1004, FIG. 3; *EX1003*, ¶140; *Regents of Univ. of California v. Satco Prods., Inc.*, No. 2023-1356, 2024 WL 4972639 (Fed. Cir. Dec. 4, 2024) ("[P]atent drawings may be useful in shedding light about the general shapes and relative sizes of elements of the claimed invention, as well as their spatial relations to one another."); *Mahle Behr Charleston Inc. v. Catalano*, IPR2023-00861, Paper 15, at 6-7 (PTAB Apr. 5, 2024) (Director Review).

10. 1(c)

Sundaram teaches "polymer-metal redistribution layers" are "deposited on the first side 115 and second side 120 of the interposer 105" and include "blind vias 140 and conductor traces 145[.]" *EX1004*, 6:62-67. Electronic devices 125, 130 "are connected with through vias 110, blind vias 140, [] conductor traces 145," and "die

pads 135" that are formed *over said first surface*. *EX1004*, 7:4-8, 6:29-33; *EX1003*, ¶142. Thus, blind vias 140, conductor traces 145, pads 135, and the polymer in the polymer-metal redistribution layer (RDL) form *a first interconnection scheme over*[3] *said first surface*:

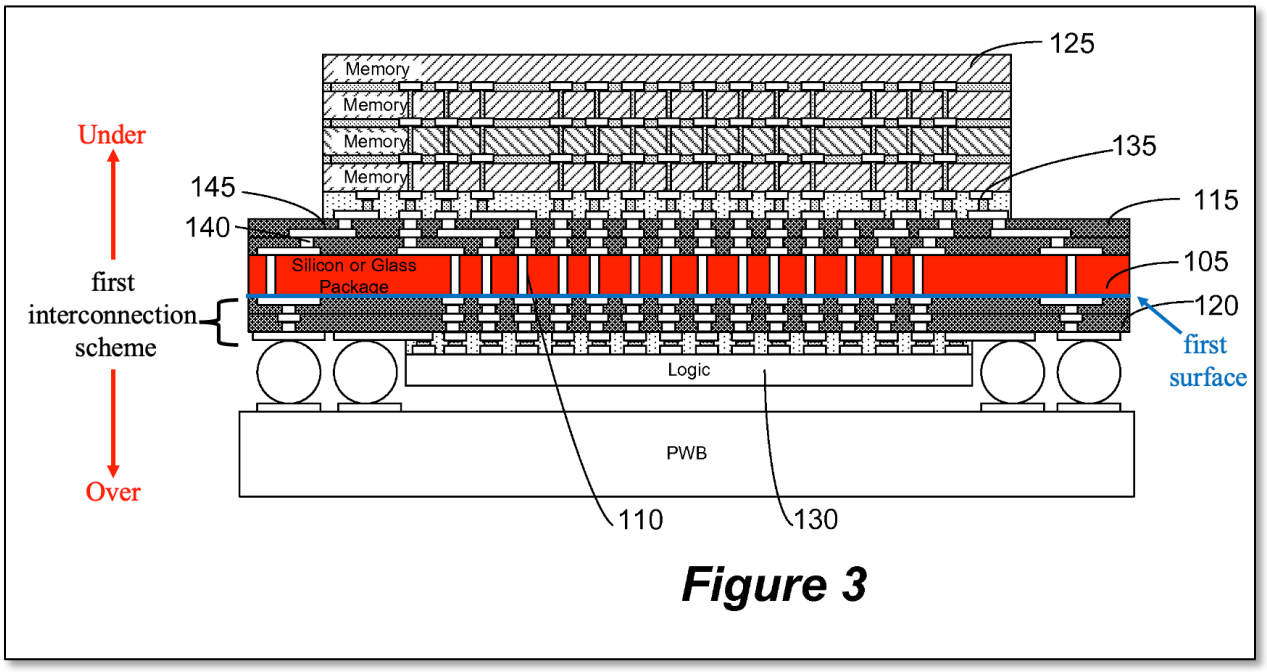


Figure 3

EX1004, FIG. 3.

[3] Petitioners annotate each reference's figures indicating the *over* and *under* direction where appropriate. The *over* direction is towards the PWB. *EX1003*, ¶143. PO similarly used inverted figures during original prosecution of the related USPN 11,107,768 to explain the *over/under* relationship between various claim elements. *Compare EX1001*, FIG. 9t *with EX1032*, 395-400, 537-538; *EX1003*, ¶143.

11. 1(c)(i)

The "blind vias 140" and "conductor traces 145" are the "metal" in the "polymer-metal redistribution layers" such that vias 140 and traces 145 are *metal interconnects* of the *first interconnection scheme*. *EX1004*, 6:62-7:8. Shown below in Sundaram's RDL are a *first metal interconnect* comprising a trace 145 (longer rectangles in FIG. 3) and a via 140 (shorter rectangles) *over said first surface* and a *second metal interconnect* comprising another trace 145 and via 140 *over said first surface*, along with a *first polymer layer over said first and second metal interconnects* (the "polymer" of the "polymer-metal redistribution layers"). *EX1004*, 6:62-67. The *first polymer layer* at least includes the below highlighted layer but may include an additional portion of the RDL (*see* Claim 14).

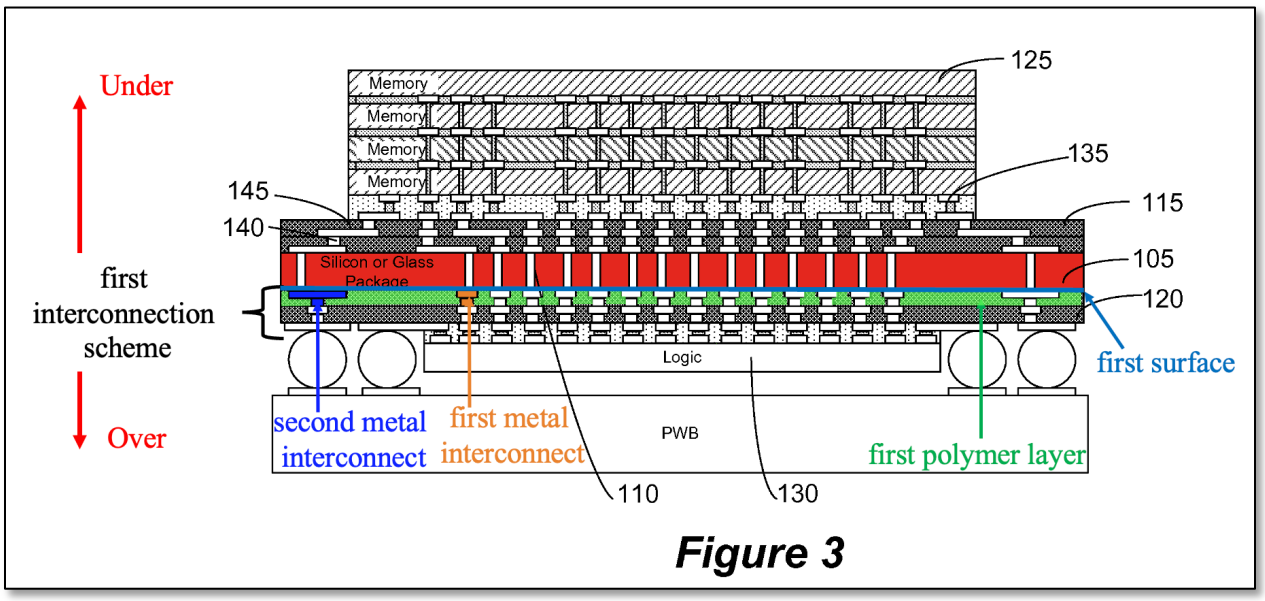


Figure 3

EX1004, FIG. 3; *EX1003*, ¶¶144-145.

Alternatively, Sundaram's outermost layer of the RDL is *a first polymer layer* and is *over* the *first/second metal interconnects*.

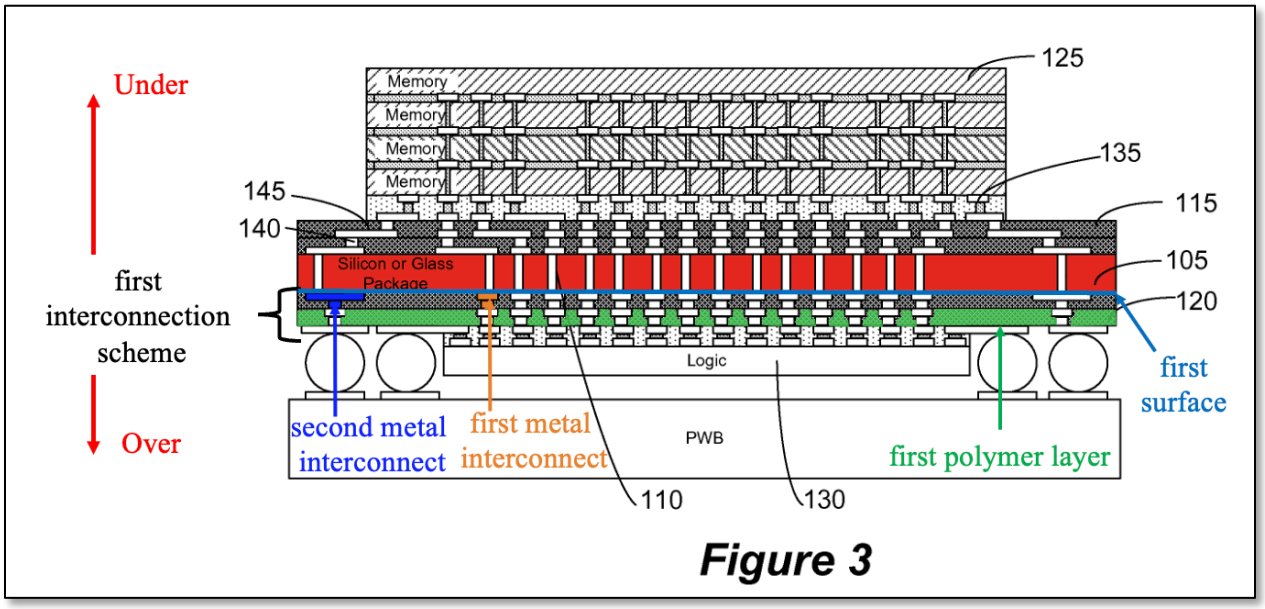


Figure 3

EX1004, FIG. 3; *EX1003*, ¶146.

12. 1(c)(ii)

Shown in FIG. 3, below, Sundaram's *first metal interconnect* and *second metal interconnect* are *connected to a first copper plug* and *a second copper plug*, respectively, such that devices 125, 130 "are connected with through vias, 110, blind vias 140, and conductor traces 145." *EX1004*, 7:4-9.

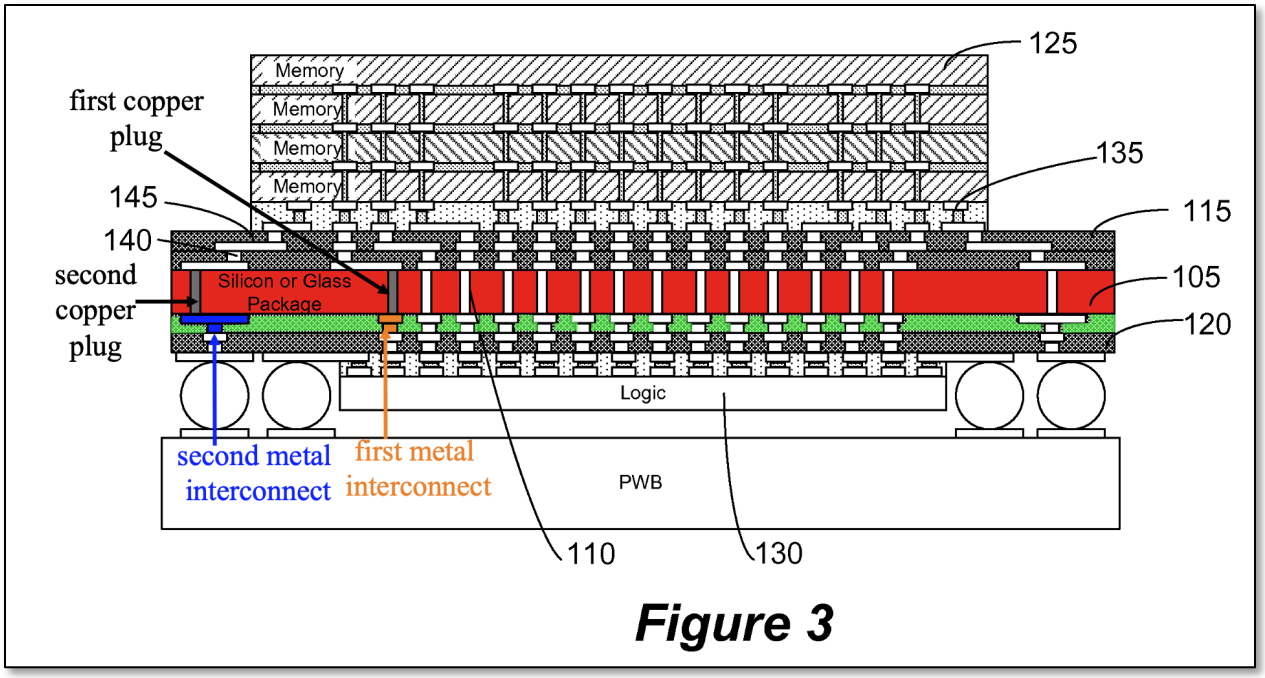
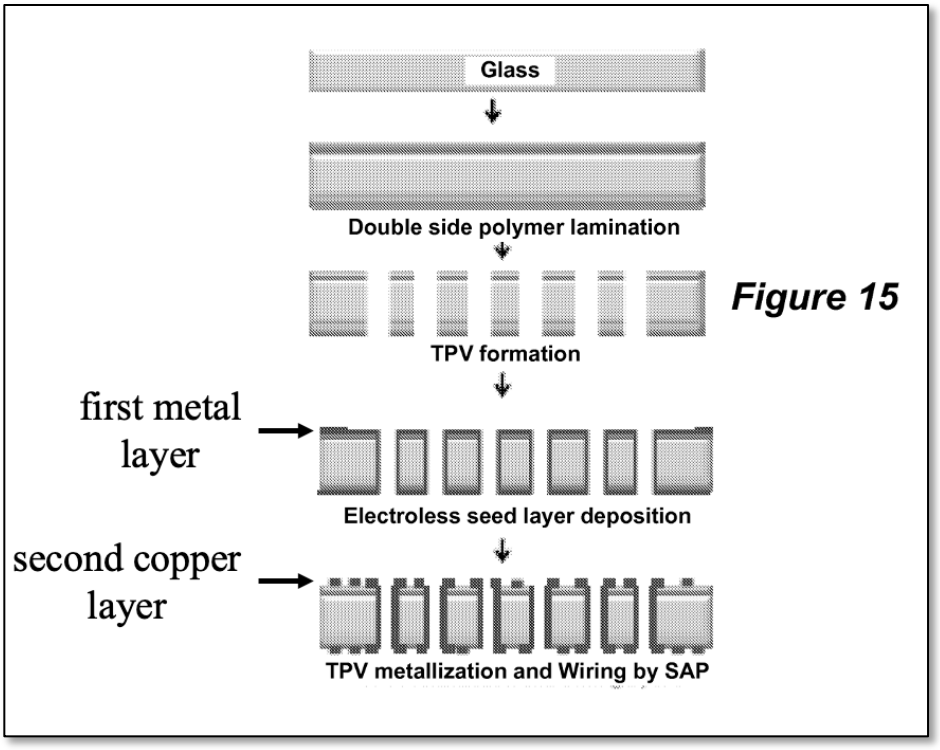


Figure 3

EX1004, FIG. 3; *EX1003*, ¶147.

13. 1(c)(iii)

Sundaram teaches a *first metal layer* formed by "direct metallization using wet electroless copper deposition" and *a second copper layer over said first metal layer* formed by "semi-additive plating" using "copper as metal." *EX1004*, 9:61-65, 10:26-28; *EX1003*, ¶148.

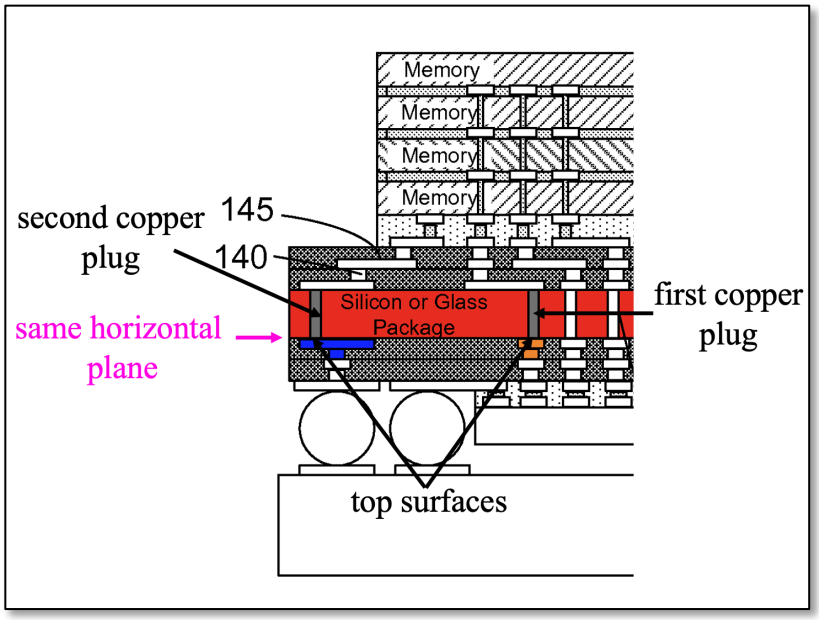


EX1004, FIG. 15.

To the extent PO argues Sundaram's FIGS. 3, 15 embodiments are separate, a POSITA would have been motivated, found obvious, and had a REOS in applying FIG. 15's *layer* teachings to FIG. 3's interconnect structure. *EX1003*, ¶149. A POSITA would have appreciated the advantages of FIG. 15's seed layer (*first metal layer*) for promoting growth of the *second copper layer*, which a POSITA would have understood as necessary in forming a copper via in a glass interposer because glass is insulating. *Id*. There would have been a REOS because FIG. 15 teaches "process flow" for fabricating a "glass test vehicle," i.e., the same material as FIG. 3's glass interposer. *EX1004*, 10:9-15, 8:1, 5:54-59; *see* Section V.A.4; *EX1003*, ¶149.

14. 1(c)(iv)

Shown in FIG. 3, below, the *top surface[s]* of both *copper plug[s] are substantially in the same horizontal plane*. The *top surface* is in the *over* direction.



EX1004, FIG. 3 (excerpt), 2:25-28; *EX1003*, ¶150.

15. 1(d)

Sundaram teaches *a first metal bump over said first interconnection scheme*, namely, a "copper **bump**[] with solder cap[]" that "can electrically connect devices." *EX1004*, 6:29-32.

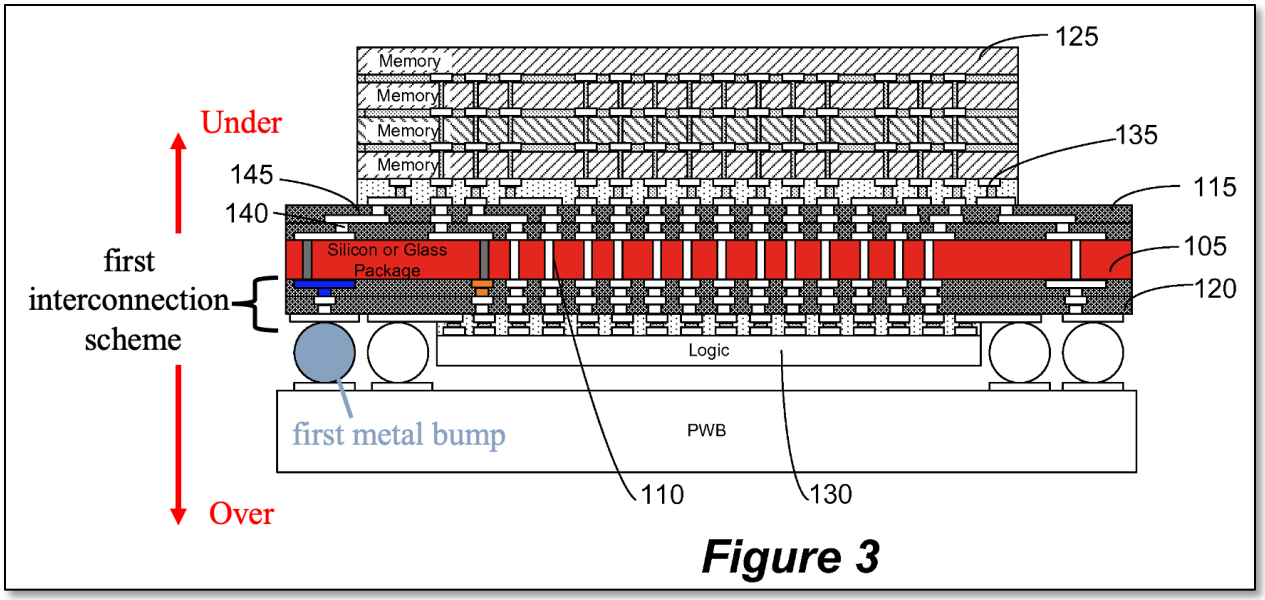


Figure 3

EX1004, FIG. 3; *EX1003*, ¶151.

16. 1(d)(i)

Sundaram's "copper bumps with solder caps" teach *a second metal layer* (the copper bump) *and a tin-containing layer over said second metal layer* (the solder cap) as a POSITA would have understood solder to include tin. *EX1004*, 6:29-32; Sundaram thus teaches this limitation. *EX1003*, ¶152.

a) Lin-191's Teachings

Additionally or alternatively, to Sundaram's teachings, Lin-191 teaches a *bump* with the claimed layers. Specifically, Lin-191 teaches a system-in-package including "solder bumps or balls 29a" formed by reflowing a "solder layer 29," which is "**a tin-containing layer**" formed "on the metal layer 28." *EX1005*, [0320]. Layer 28, along with "adhesion layer 18, the seed layer 19, and **metal** layer[]

27…compose an under bump metallurgic (UBM) layer." *EX1005*, [0323]. Layers 18, 19 are *metal*. *EX1005*, [0308].

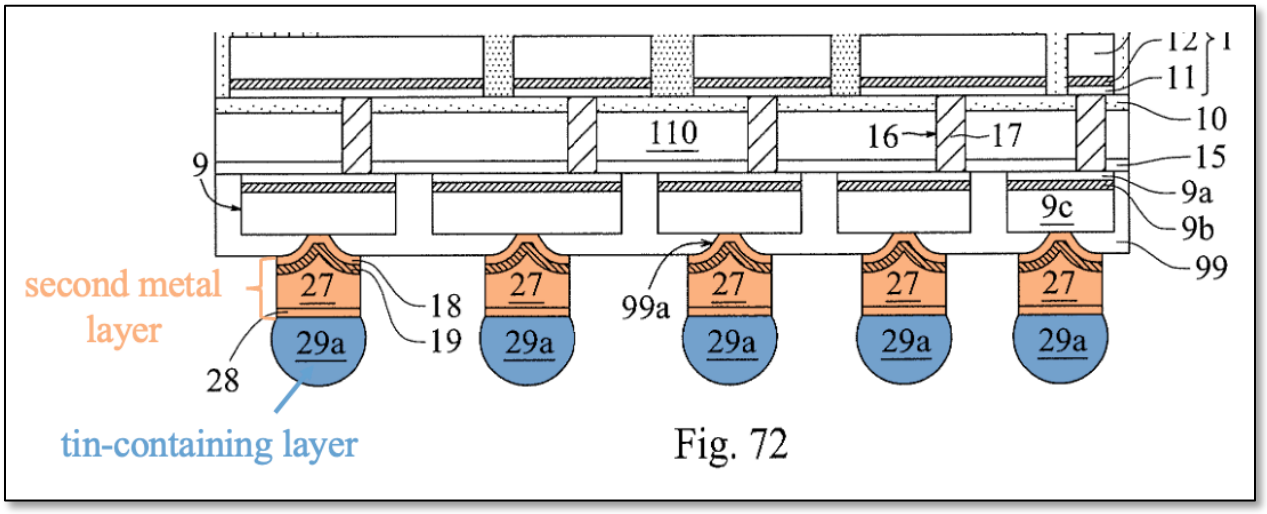


Fig. 72

EX1005, FIG. 72 (excerpt); *EX1003*, ¶¶153-154.

Thus, Lin-191 teaches *a metal bump compris[ing] a second metal layer* (UBM layer) *and a tin-containing layer* (solder layer 29) *over said second metal layer*.

b) MTC

A POSITA would have been motivated and found obvious to apply Lin-191's teachings of a metal bump having *a tin-containing layer over a second metal layer* to Sundaram's copper bump. *EX1003*, ¶155. A POSITA would have appreciated the advantages of applying Lin-191's teachings of a solder ball having a tin-containing layer 29 and the UBM metal layer to improve the strength of Sundaram's copper bump. *EX1005*, [0323], [0437]; *EX1003*, ¶¶156-157. A POSITA would have

appreciated the advantage of a *tin-containing layer*, which was known to "wet and spread on a wide range of substrates…." *EX10XX*, 104; *EX1003*, ¶155.

The Sundaram-Lin-191 combination is the application of a known technique (Lin-191's bump structure) to a known device (Sundaram's bump) ready for improvement to yield predictable result of Sundaram's bump (*first metal bump*) being formed according to Lin-191's teachings. *EX1003*, ¶158. Alternatively, the Sundaram-Lin-191 combination is the simple substitution of Lin-191's solder bump structure for Sundaram's "copper bumps with solder caps." *EX1004*, 6:29-33; *EX1003*, ¶159.

A POSITA would have had a REOS in either applying Lin-191's teachings to Sundaram's bump or substituting Sundaram's bump with Lin-191's bump at least because such a modification/substitution would have involved the application of well-known manufacturing techniques well within the skill of a POSITA. *EX1003*, ¶160. Furthermore, metal bump technology, including UBM layers were commonplace prior to the '763 Patent. *EX1003*, ¶160.

17. 1(e)

Sundaram's first electronic device 125 "can be…stacked memory IC devices" such that a memory chip of the stack is *a first semiconductor chip under said first interconnection scheme*. *EX1004*, 6:34-46.

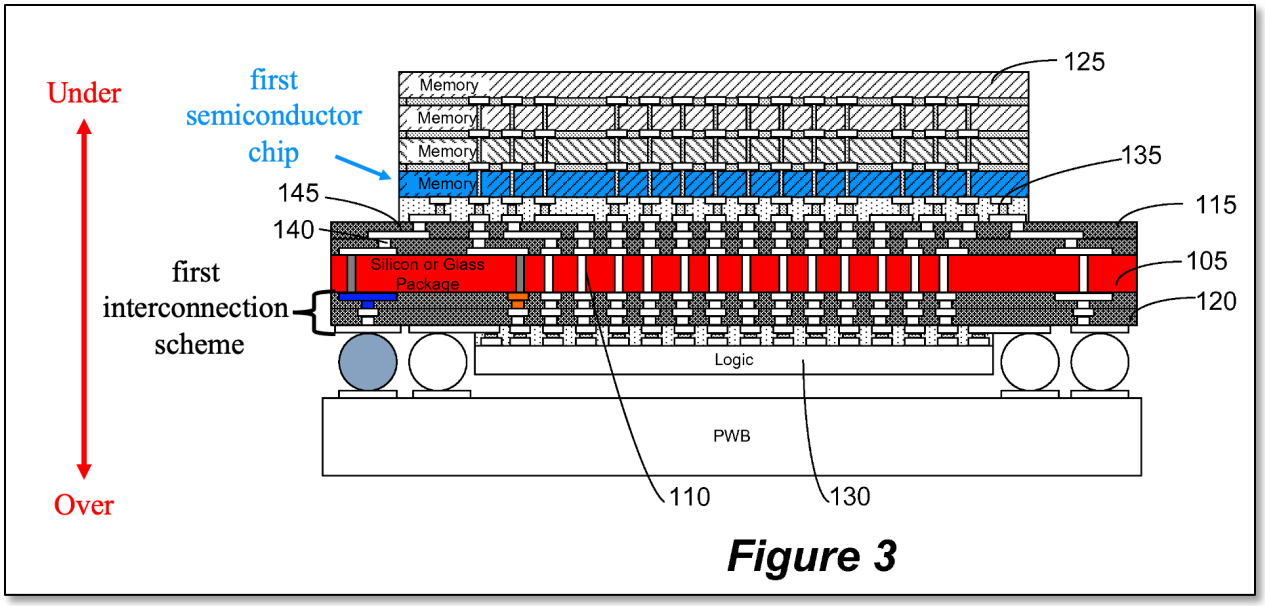


Figure 3

EX1004, FIG. 3; *EX1003*, ¶161.

18. 1(e)(i)

Sundaram's interposer 105 has die pads 135 where "metallization provides die pad surfaces 135[.]". *EX1004*, 6:23-25. A POSITA would understand that device 125 also has die pads (purple) such that an electrical connection is made between interposer 105 and device 125, thus teaching the *first semiconductor chip* having a *first metal pad*. *EX1003*, ¶162. "[D]ie pads 135…can electrically connect devices using solder, copper bumps with solder caps, [and] copper to copper bonding," each of which teaches *a third metal interconnect*. *EX1004*, 6:29-33. In FIG. 3, the *third metal interconnect* is a bump on the metal pad.

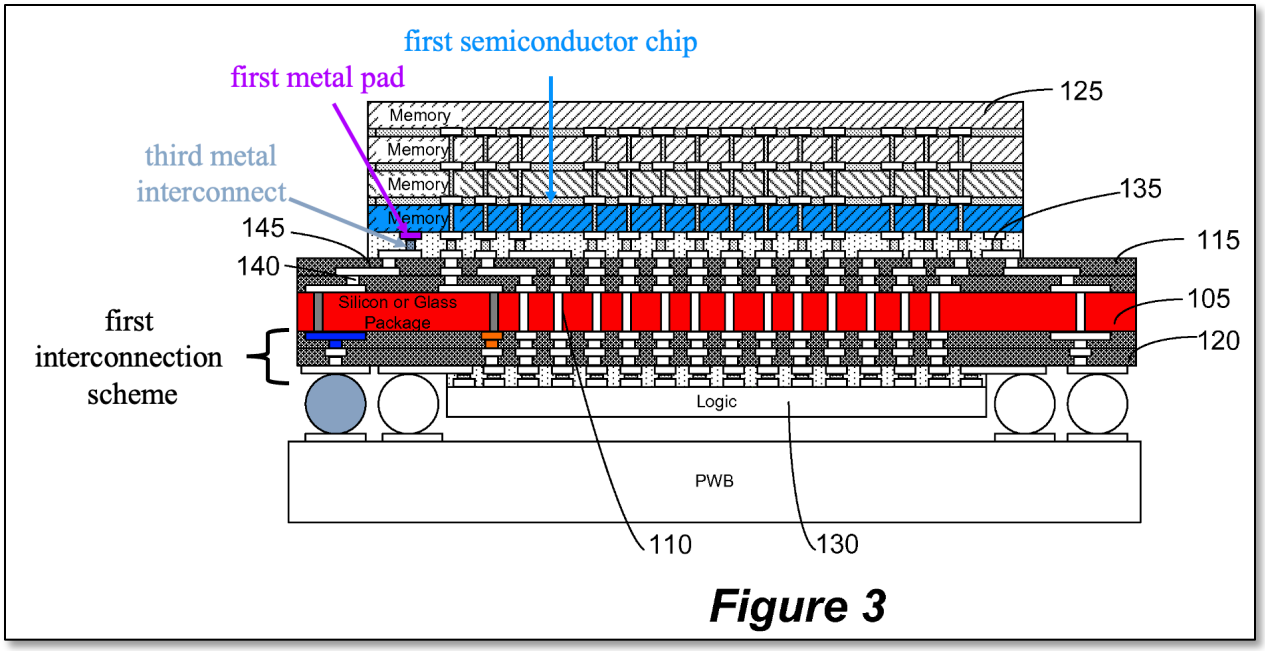


Figure 3

EX1004, FIG. 3.

Additionally, or alternatively, FIG. 32 is a "side-by-side configuration" of the interconnect structure, which includes a memory stack where each chip has a *metal pad*:

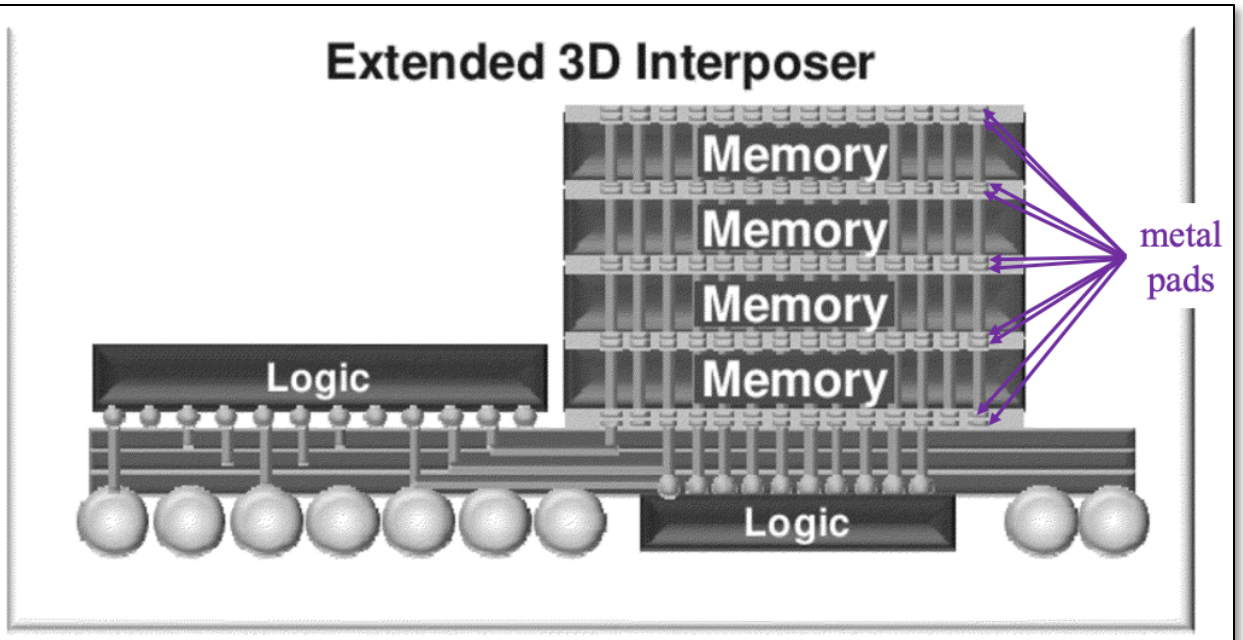
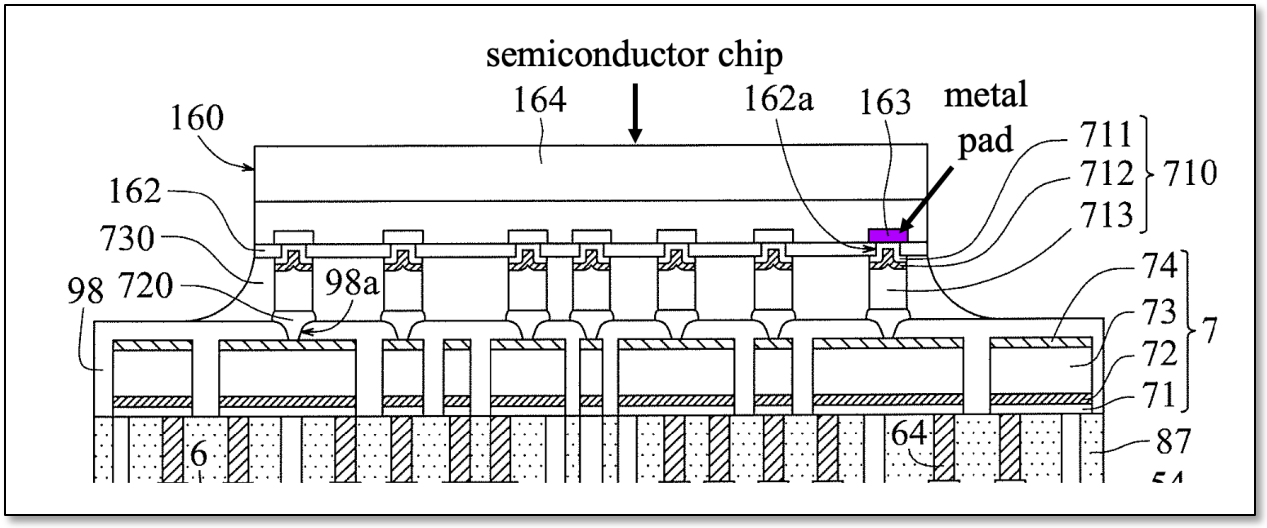


Figure 32

EX1004, FIG. 32, 4:26-27, 7:56-59; *EX1003*, ¶163. MTCs and REOS are below for modifying Sundaram's chip to have a *metal pad* and are incorporated. *See* Section V.A.18.b.

a) Lin-191's "Metal Pad" Teachings

Additionally or alternatively to Sundaram's teachings, Lin-191's system-in package has a semiconductor chip 160 with "**metal** traces or **pads** 163" that include "aluminum." *EX1005*, [0384].



EX1005, FIG. 71 (excerpt); *EX1003*, ¶164.

b) MTC

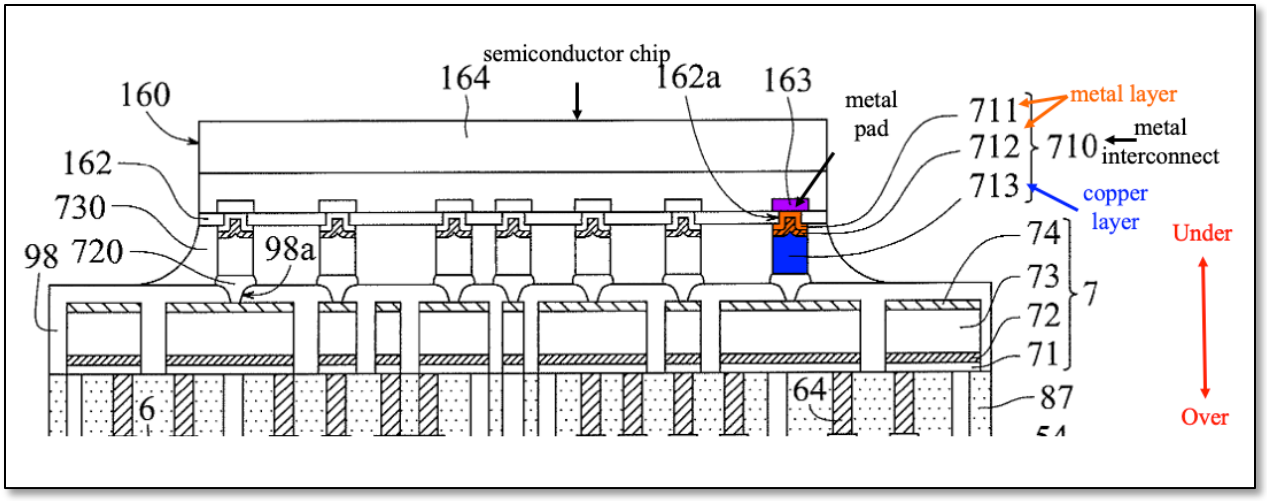
A POSITA would have been motivated and found obvious to modify Sundaram per Lin-191's metal pad teachings. *EX1003*, ¶¶165-166. The modification is merely an implementation detail in Sundaram's chip package, and the combination is the application of a known technique (metal pads) to a known device (Sundaram's semiconductor chip) ready for improvement to yield the predictable result of Sundaram's device 125 having a *first metal pad*. *EX1005,* [0081]; *EX1003*, ¶¶165-166. Because chips having metal pads are ubiquitous and essential for interconnecting the chip to other components, the modification has an REOS. *EX1003*, ¶¶165-166.

19. 1(e)(ii)

a) Lin-191's Teachings

Lin-191's semiconductor chip 160 has "**metal** traces or **pads** 163" that include "aluminum." *EX1005*, [0384]. Metal bumps 710 are *on* "the metal traces or pads 163," and bumps 710 *interconnect* chip 160 to another chip 140 such that bumps 710, like Sundaram's copper bumps, are *metal interconnect[s]*. *EX1005*, [0406].

Bumps 710 include an "adhesion layer 711 under the contact points…of the metal traces or pads 163…a seed layer 712 under the adhesion layer 711, and a metal layer 713 under the seed layer[.]" *EX1005*, [0389]. Adhesion layer 711 includes "nickel" or "titanium." *EX1005*, [0390]. Seed layer 712 "can be a copper layer." *EX1005*, [0392]. Thus, the combination of layers 711 and 712 is a *third metal layer on* metal pad 163. *EX1003*, ¶167. Metal layer 713 is "a single **copper** layer having a thickness…between 2 and 30 micrometers;" thus it is a *copper layer* that teaches or renders obvious *a thickness between 5 and 30 micrometers*. *EX1005*, [0396]; Section V.A.5 (supporting caselaw); *EX1003*, ¶168 (citing *EX1001*, 14:17-29 and opining no criticality of the claimed copper thickness).



EX1005, FIG. 72 (excerpt).

b) MTC

A POSITA would have been motivated and found obvious to modify Sundaram's bump per Lin-191's layered bump teachings (including the thickness of copper layer 713). *EX1003*, ¶¶169-170. This combination would yield Sundaram's bump (*third metal interconnect*) having *a third metal layer over said first metal pad and a third copper layer over said third metal layer*, *wherein said third copper layer has a thickness between 5 and 30 micrometers*. *EX1003,* ¶¶169-170, 173.

A POSITA would have recognized that Lin-191's metal bump provides improved metallurgical bonding and increased resistance to fatigue and stress-induced failure by employing a layered structure. *EX1003*, ¶170. This multi-layer configuration would reduce the risk of intermetallic formation at critical interfaces, mitigate electromigration, and better absorb mechanical strain during thermal cycling. *Id*. Further, the mechanical integrity and reliability of the Sundaram's

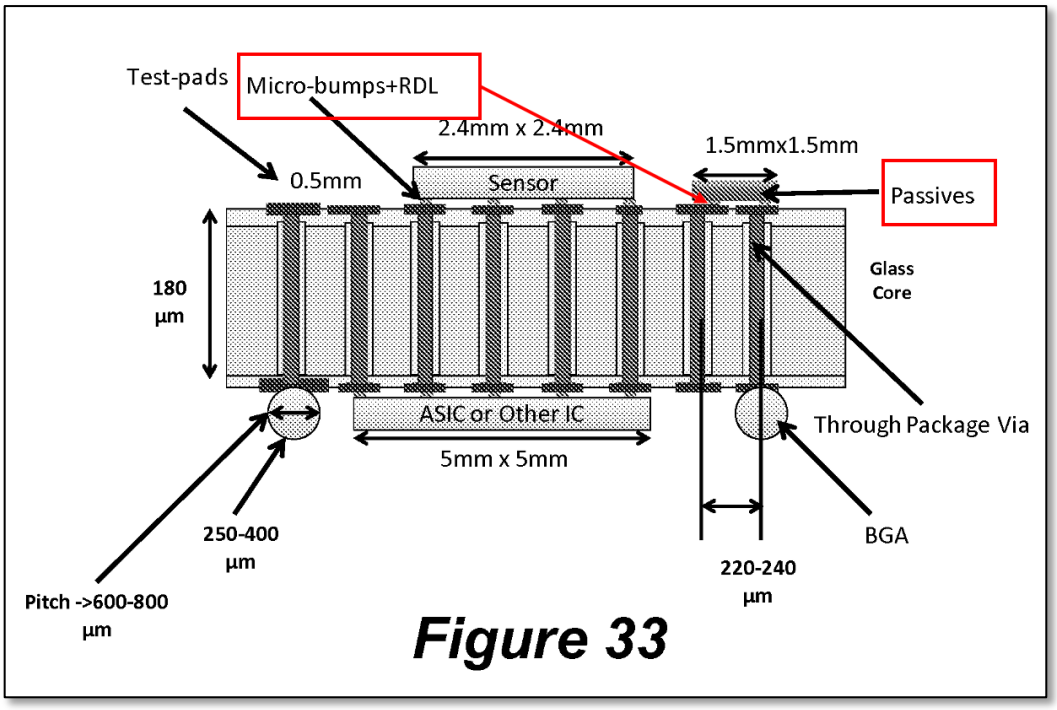
bumps would be improved, particularly in applications subject to repeated temperature fluctuations and mechanical stress, e.g., where the chip package includes "high power logic component[s]." *EX1004*, 6:19-22, FIGS. 30-31; *EX1003*, ¶¶171-172. Accordingly, the Sundaram-Lin-191 combination would have advantageously improved long-term bump performance. *Id.*

The combination is the application of known techniques to improve similar structures in a predictable manner, i.e., improving Sundaram's solder ball in the same way as Lin-191's bump. *EX1003*, ¶174. Alternatively, a POSITA would have been motivated to substitute Lin-191's bump structure for Sundaram's bump to obtain the above-described advantages of Lin-191's teachings. *Id*.

A POSITA would have had a REOS in either applying Lin-191's teachings to Sundaram's bump or substituting Lin-191's bump for Sundaram's similar bump, as both Lin-191 and Sundaram address semiconductor interconnect technology and because bump interconnects were well-known and fabricated using common manufacturing techniques. *EX1003*, ¶175 For example, Lin-191 teaches plating layers to form bump 710, and Sundaram likewise teaches plating techniques, further evidencing the REOS. *Compare EX1005,* [0400] *with EX1004*, 6:22-29, 10:26-29; *EX1003*, ¶175

B. Claim 2

Sundaram teaches a *passive component* ("passives") connected to an interposer by "micro-bumps+RDL" (ReDistribution Layer), thus teaching a *passive component* that is *over* and *connected to* an *interconnection scheme* (RDL) *through a solder layer* (micro-bumps). The micro-bump is a *solder layer* because Sundaram teaches devices are connected using "solder, copper bumps with solder caps…" *EX1004*, 6:29-32.



EX1004, FIG. 33; *EX1003*, ¶¶176-177.

a) MTC Sundaram's Embodiments

Based on Sundaram's FIG. 33 embodiment, a POSITA would have found obvious and been motivated to include a *passive component over* Sundaram *first*

interconnection scheme, e.g., adjacent to FIG. 3's electronic device 130. *EX1003*, ¶178.

A POSITA would have appreciated that by connecting a passive component, e.g., a capacitor, over Sundaram's *first interconnection scheme*, Sundaram's chip package would advantageously mitigate signal desynchronization and preserve signal integrity. *EX1003*, ¶179. The use of passives, such as capacitors, in chip packages was a well-known technique to ensure signal quality and integrity because the capacitor establishes a transmission line signal path, thereby maintaining signal integrity when interconnecting with the PWB (printed wiring board). *EX1003*, ¶¶180-181. Further, including a capacitor would reduce both the impact of high frequency interference (HFI) on digital signals being transmitted between the *first semiconductor chip* and the PWB and the impact of HFI on power supply lines present in the chip package, thereby further preserving signal integrity and reducing signal desynchronization. *EX1003*, ¶182.

The modification is the application of a known technique (a passive component in a chip package) to a known device (Sundaram's chip package) to yield the predictable result of Sundaram's chip package having a passive component over the RDL and connect thereto. *EX1003*, ¶183. A POSITA would have had a REOS in modifying Sundaram's FIG. 3 embodiment because solder bonded passives were

ubiquitous in the industry before the '763 Patent, making the modification simple and straightforward. *Id*.

C. Claim 3

Sundaram's *first interconnection scheme* comprises a *fourth metal interconnect*, namely a die pad. Sundaram teaches "metallization provides die pad surfaces 135" on "the second side 120 of the interposer 105" that "electrically connect devices," and are therefore *metal interconnect[s]*. *EX1003*, ¶184. FIG. 3 illustrates numerous die pad surfaces. An example one of the many die pad surfaces is identified with reference numeral 135 in FIG. 3. *EX1004*, 6:22-33 (referencing die pads (plural)). A POSITA would have understood FIG. 3 expressly teaches a die pad surface such as the orange-highlighted die pad in the below FIG. 3 at least because of the ubiquity of connecting bumps to pads. *EX1003*, ¶184. The orange-highlighted die pad is part of the *first interconnection scheme*. *EX1004*, 6:22-33; *EX1003*, ¶184.

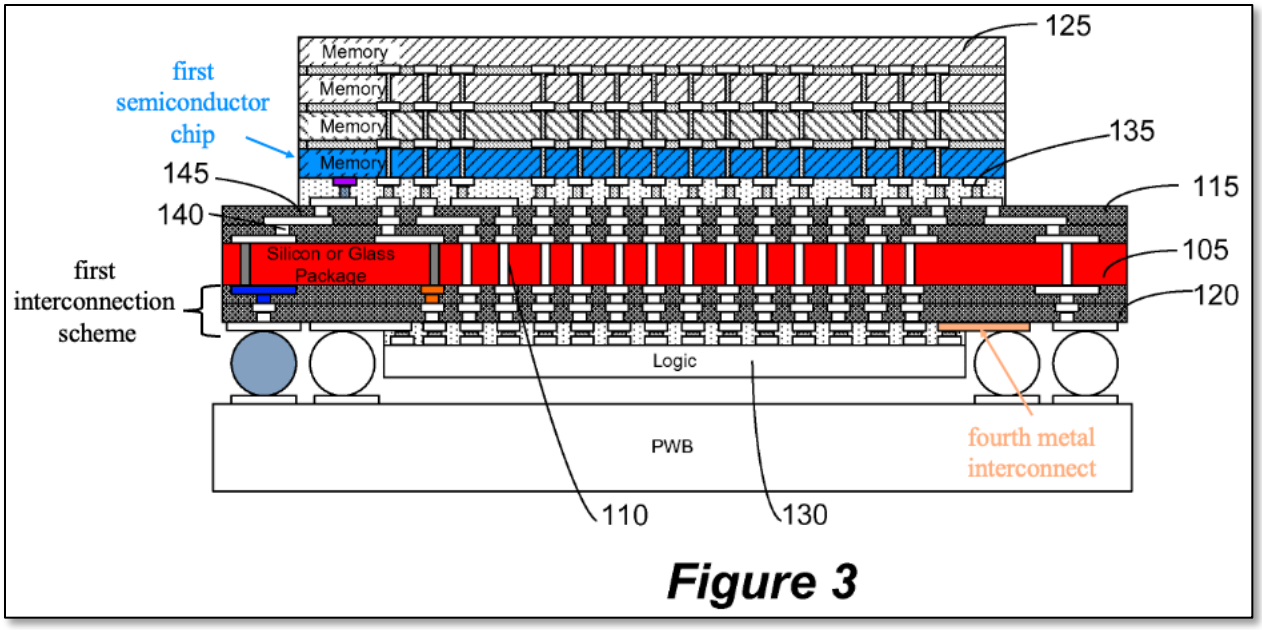
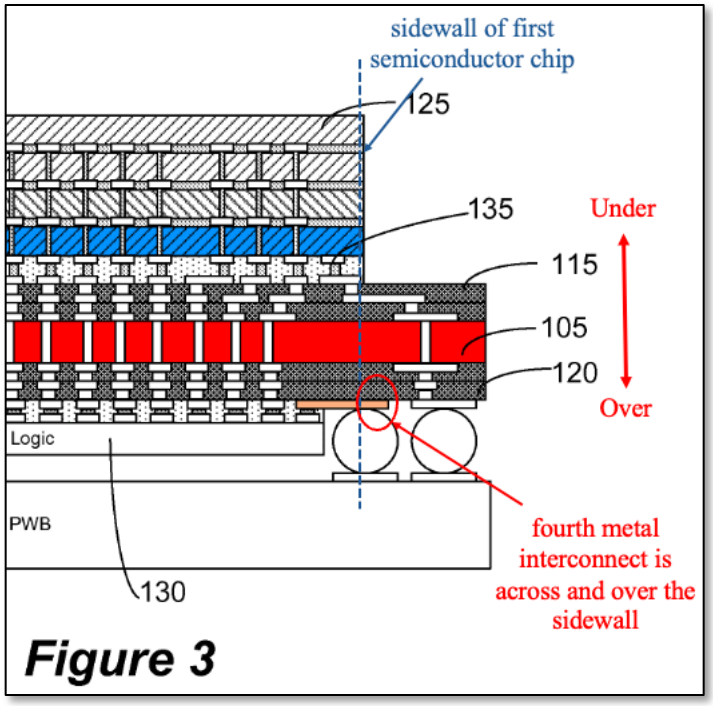


Figure 3

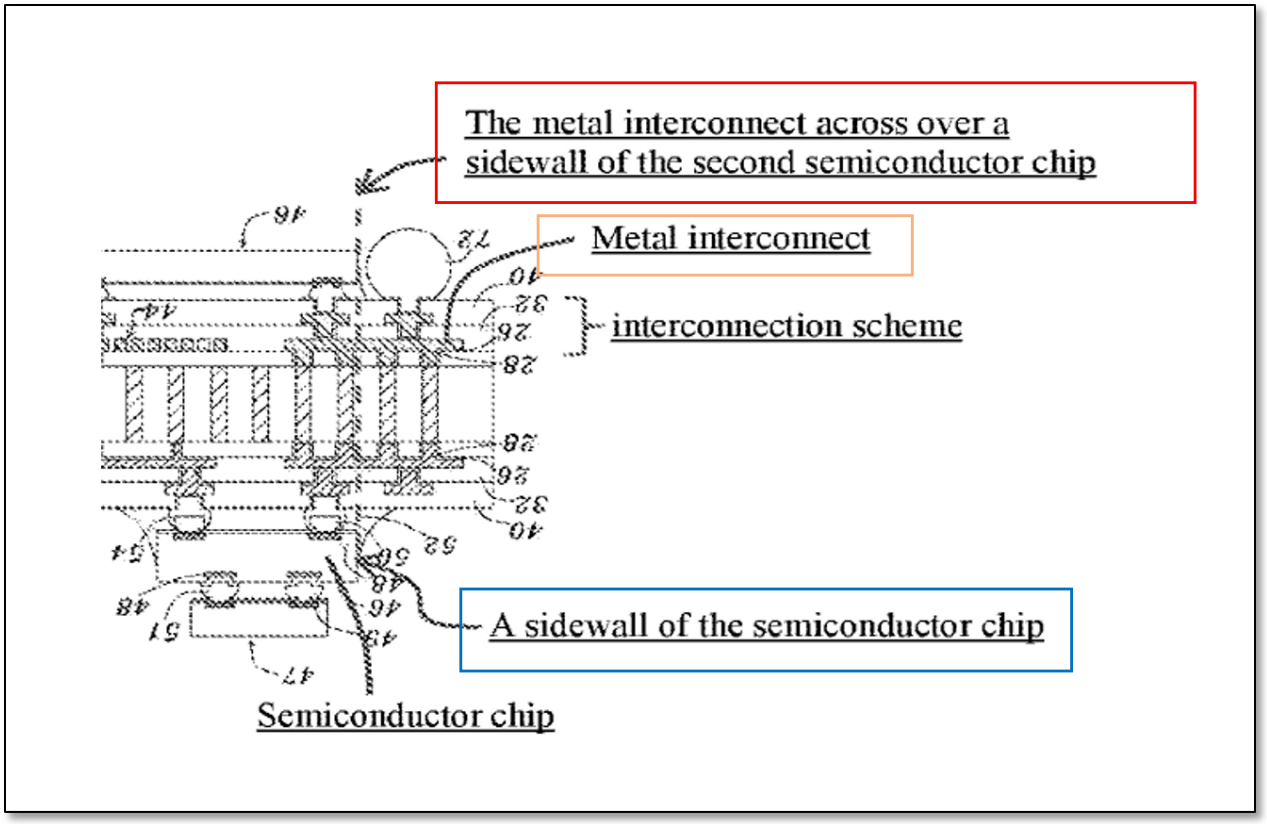
EX1004, FIG. 3.

Sundaram further teaches the orange-highlighted die pad is *across over a sidewall of the first semiconductor chip* (electrical device 125). Sundaram's orange-highlighted pad is *across over* device 125's *sidewall* because the pad is positioned on the opposite side of interposer 105 from device 125's sidewall (*over*) and comprise at least a portion extending laterally beyond device 125's *sidewall* (*across*). *EX1003*, ¶185.



EX1004, FIG. 3 (excerpt).

During prosecution of the related '768 Patent, PO provided an annotated figure illustrating specification support for this limitation, similar to Sundaram's orange-highlighted pad relative to device 125.



EX1032, 537; *EX1003*, ¶186; Section V.A.9 (caselaw regarding drawings); *Omega Eng'g, Inc. v. Raytek Corp.*, 334 F.3d 1314, 1333 (Fed. Cir. 2003) (prosecution disclaimer of parent application attaches to child application); *In re McDonald*, 43 F.4th 1340, 1347 (Fed. Cir. 2022).

D. Claim 4

1. 4(a)

Sundaram teaches a *second semiconductor chip*, namely "a second electronic device 130…attached to the second side 120 of the interposer 105," which is *over said first interconnection scheme*. *EX1004*, 6:34-36.

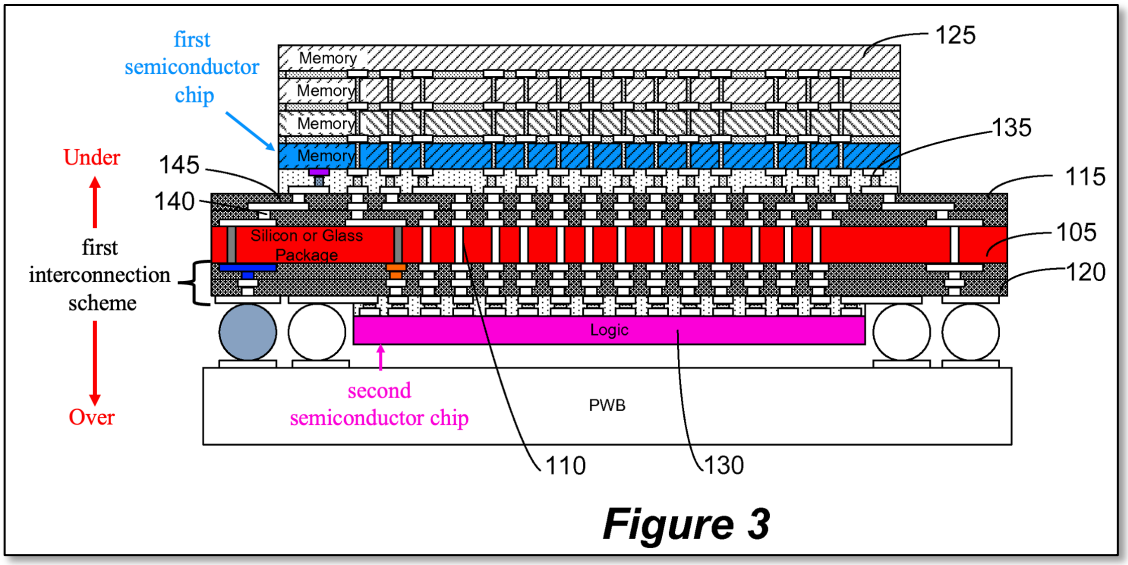
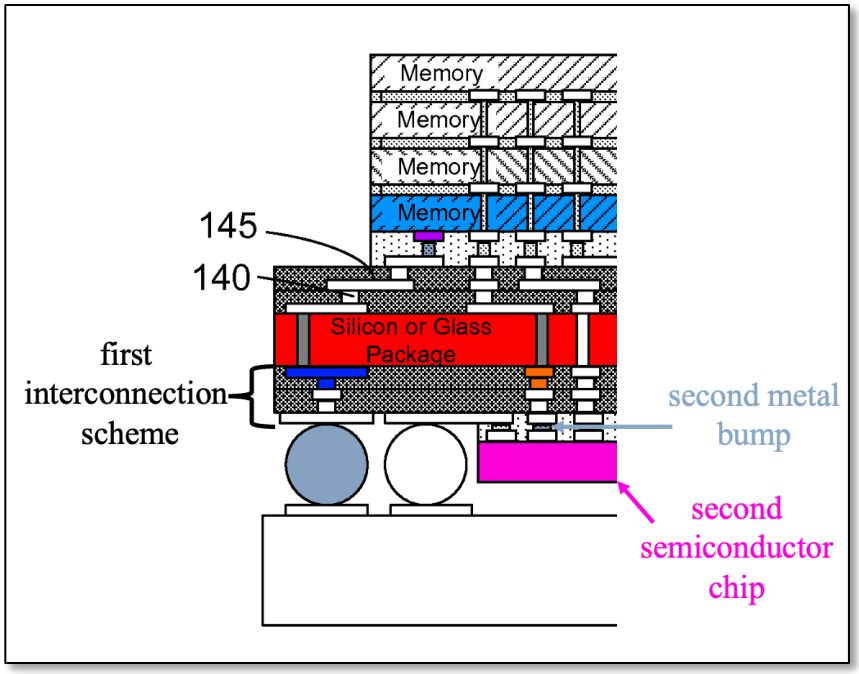


Figure 3

EX1004, FIG. 3; *EX1003*, ¶187.

2. 4(b)

The *second semiconductor chip comprises a second metal bump between* it and *said first interconnection scheme. EX1004*, 6:29-33 ("The die pads 135 that are formed on…the interposer 105 can electrically connect devices using…copper bumps[.]").



EX1004, FIG. 3 (excerpt); *EX1003*, ¶188.

E. Claim 5

a) Lin-191's Teachings

Lin-191 teaches semiconductor chips as "system-on chip[s] (SOC) including **a graphics-processing-unit (GPU) circuit block**, a wireless local area network (WLAN) circuit block **and a central-processing-unit (CPU) circuit block**…" *EX1005*, [0106].

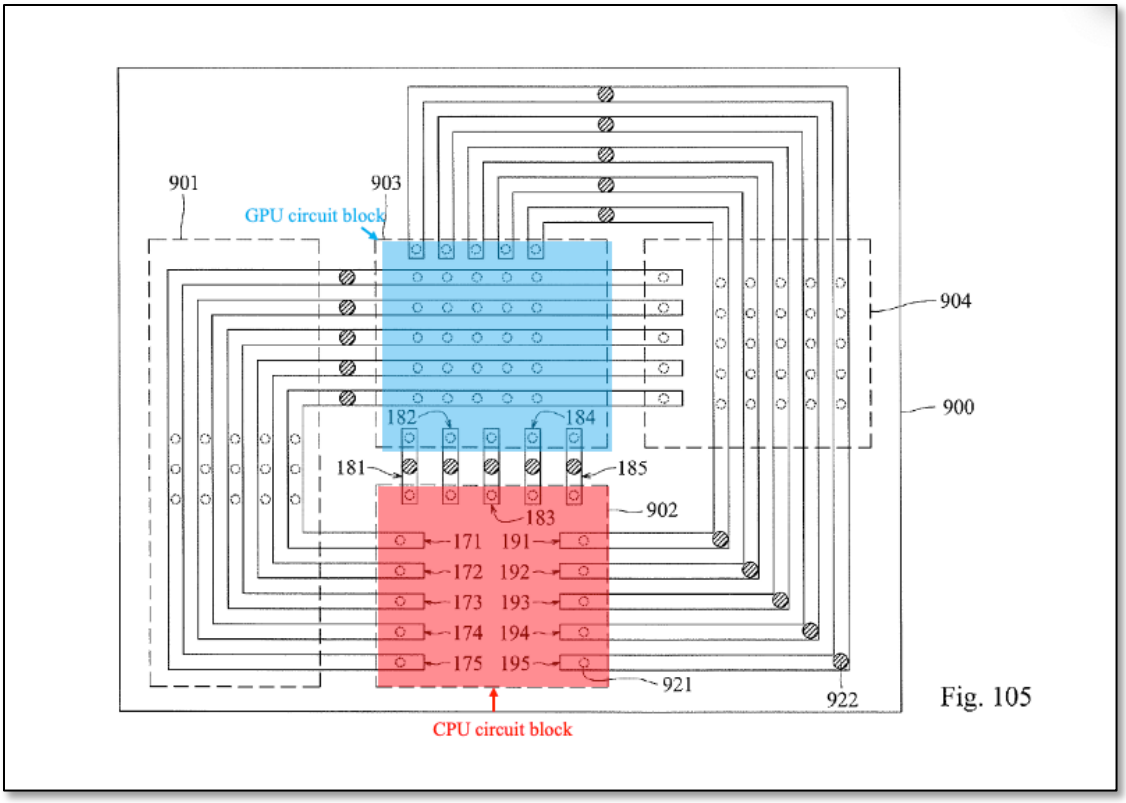


Fig. 105

EX1005, FIG. 105, [0541], [0543]; *EX1003*, ¶189.

b) MTC

A POSITA would have been motivated and found obvious to modify Sundaram's electronic device 125 per Lin-191 to include *a CPU circuit block and a GPU circuit block*. *EX1003*, ¶190. While Sundaram's FIG. 3 depicts device 125 as stacked memory, Sundaram teaches "other electronic devices can also be used as the first electronic device 125." *EX1004*, 6:37-43; *EX1003*, ¶190. Thus, a POSITA would have been motivated and found obvious to apply Lin-191's teachings to Sundaram. *EX1003*, ¶190. Indeed, Sundaram discloses "smart and mobile phone

applications, including video streaming, 3D graphics, camera-functions, and gaming" and contemplates "high power logic component[s]" for device 125:

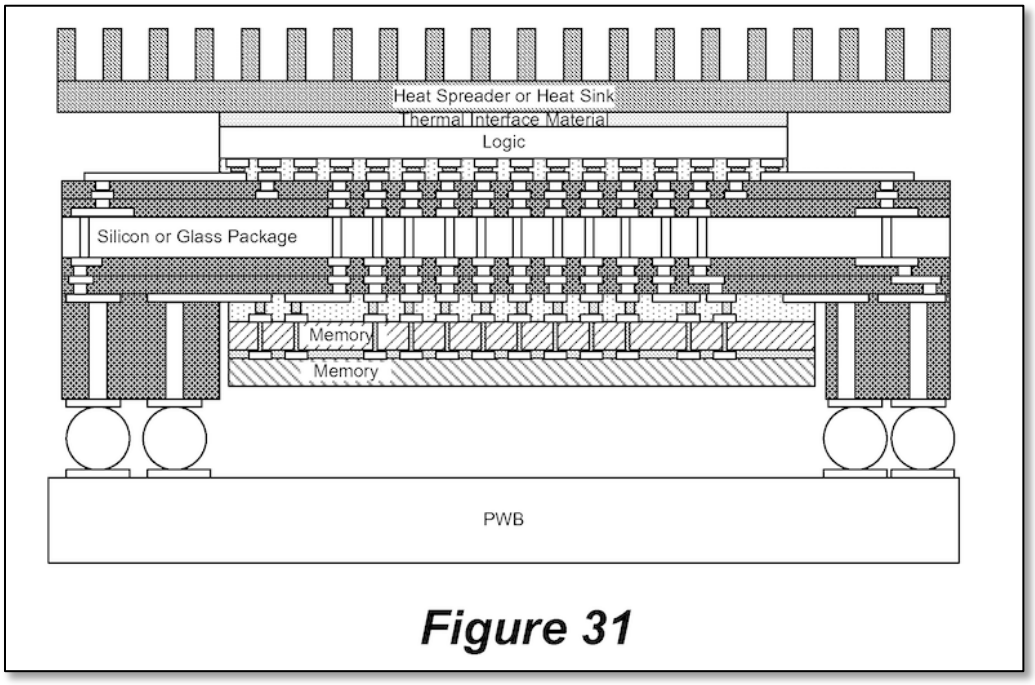


Figure 31

EX1004, 1:20-25, 6:19-22, FIG. 31. Such a combination would have predictably improved Sundaram's chip package by providing it with increased capabilities, i.e., to carry out the functions of both a CPU and a GPU. Further, the modification is an implementation detail a POSITA would have found obvious to implement given Sundaram's teachings of phone applications. *EX1003*, ¶191. Thus, a POSITA would have been motivated and found obvious to apply Lin-191's teachings to Sundaram. *Id.*

The Sundaram-Lin-191 combination is the application of a known technique (a semiconductor chip with GPU and CPU circuit blocks) to a known device

(Sundaram's chip device 125) yielding the predictable results of Sundaram chip device 125 having both CPU and GPU circuit blocks. *EX1003*, ¶191. A POSITA would have been motivated to apply Lin-191's teachings based on the desired functionality of Sundaram's chip package. *Id.*

SoCs that included CPUs and GPUs, such as taught by Lin-191, were well-known before the time of the '763 Patent, leading to a REOS. *EX1003*, ¶192.

F. Claim 6

1. 6(a)

As shown below, Sundaram teaches a *second semiconductor chip* (second memory chip) *under said first semiconductor chip*. Sundaram's "first electronic device 125 can be…stacked memory IC devices[.]" *EX1004*, 6:37-39.

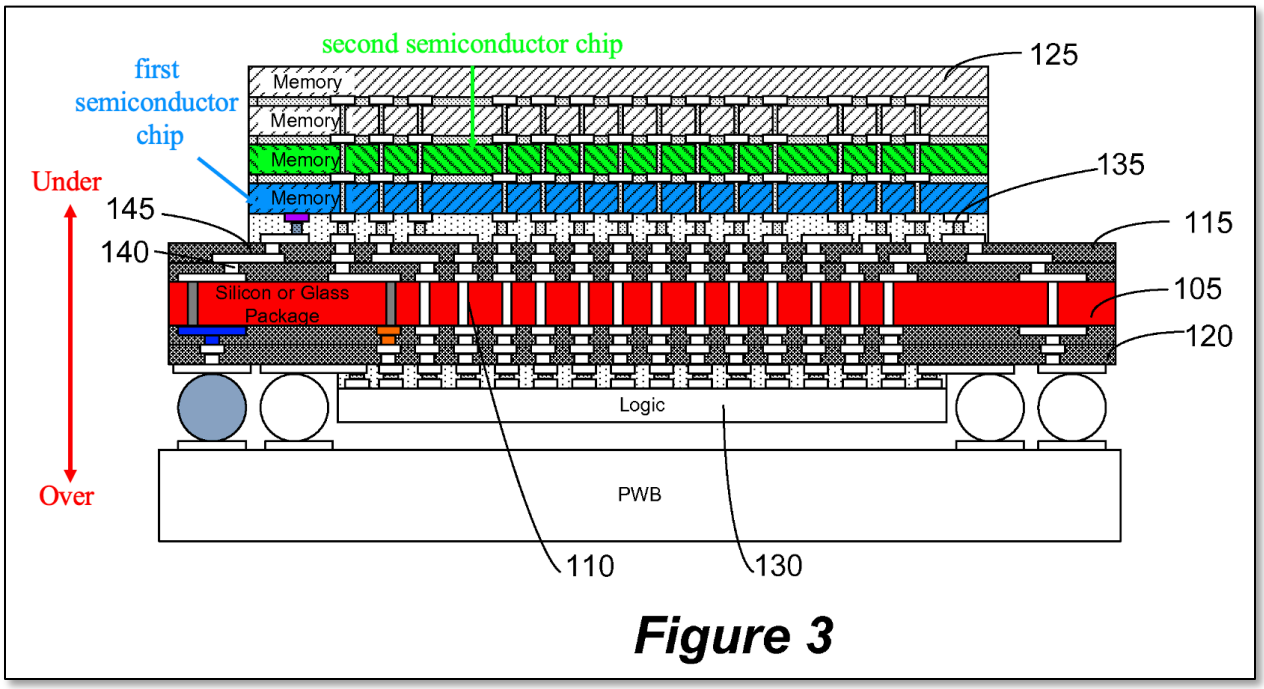
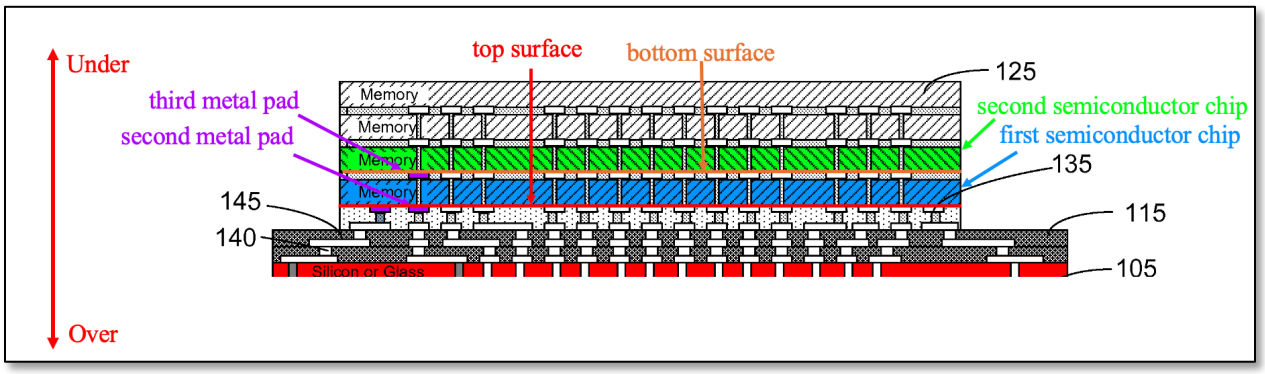


Figure 3

EX1004, FIG 3; *EX1003*, ¶193.

2. 6(b)

FIG. 3 depicts Sundaram's *first* and *second semiconductor chips[]* with *pad[s]* on the top and bottom surfaces, which a POSITA would understand to be *pad[s]* because FIG. 3 expressly illustrates such *pad[s]*. *EX1003*, ¶194. Additionally, a POSITA would have found obvious the *pad* shown in FIG. 3 is a *metal pad* because of the ubiquity of chips having metal pads for forming electrical connections. *Id.*; Section V.A.18. A *metal pad* on the *top surface* is a *second metal pad* and a *metal pad* on the *bottom surface* is a *third metal pad*, respectively. *EX1003*, ¶194.



EX1004, FIG. 3 (excerpt).

FIG. 32 depicts a chip stack similar to FIG. 3's where each chip has a distinct metal pad. A POSITA would have found obvious, been motivated, and had a REOS in modifying FIG. 3's chip stack per FIG. 32's to provide each chip with its own set of pads so that each chip has top and bottom pads connected to one another as each chip must include pads on its surface to provide connection to other electrical

components in the chip package. *EX1003*, ¶195. The modification is a straightforward implementation detail to FIG. 3's chip stack. *Id.*

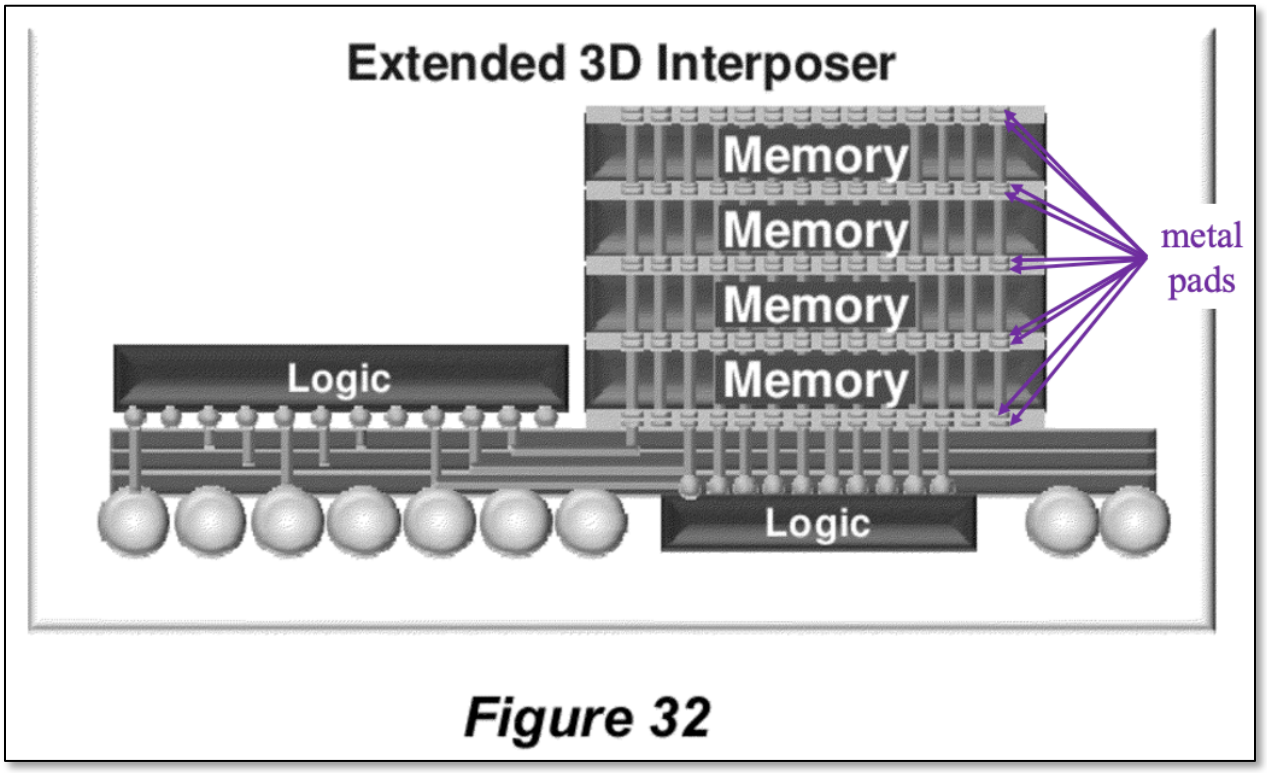


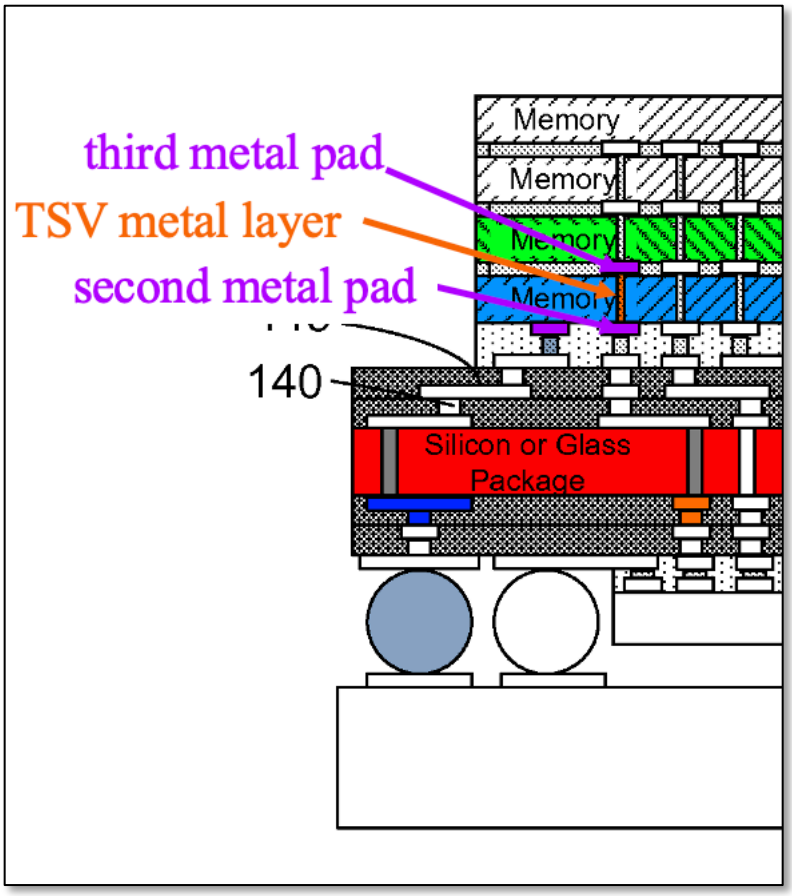
Figure 32

EX1004, FIG. 32.

3. 6(c)

As shown, Sundaram's *first semiconductor chip* comprises an interconnect (orange) connecting pads on the top and bottom surfaces of each memory chip, which a POSITA would have understood as being a *through-silicon-via metal layer* that connects the *third metal pad* to the *second metal pad*. *EX1003*, ¶196. Sundaram teaches TSV metal layers connecting metal pads, referring to the logic chip structure in FIG. 1d as having "TSVs[.]" *EX1004*, 1:39-42, 1:62-67; *EX1004*, 14:13–15:16.

Accordingly, a POSITA would have understood the similar structure shown in device 125 of FIG. 3 to also be a TSV metal layer. *EX1003*, ¶196.



EX1004, FIG. 3 (excerpt).

Sundaram's FIG. 32 also teaches a TSV metal layer connecting second and third metal pads:

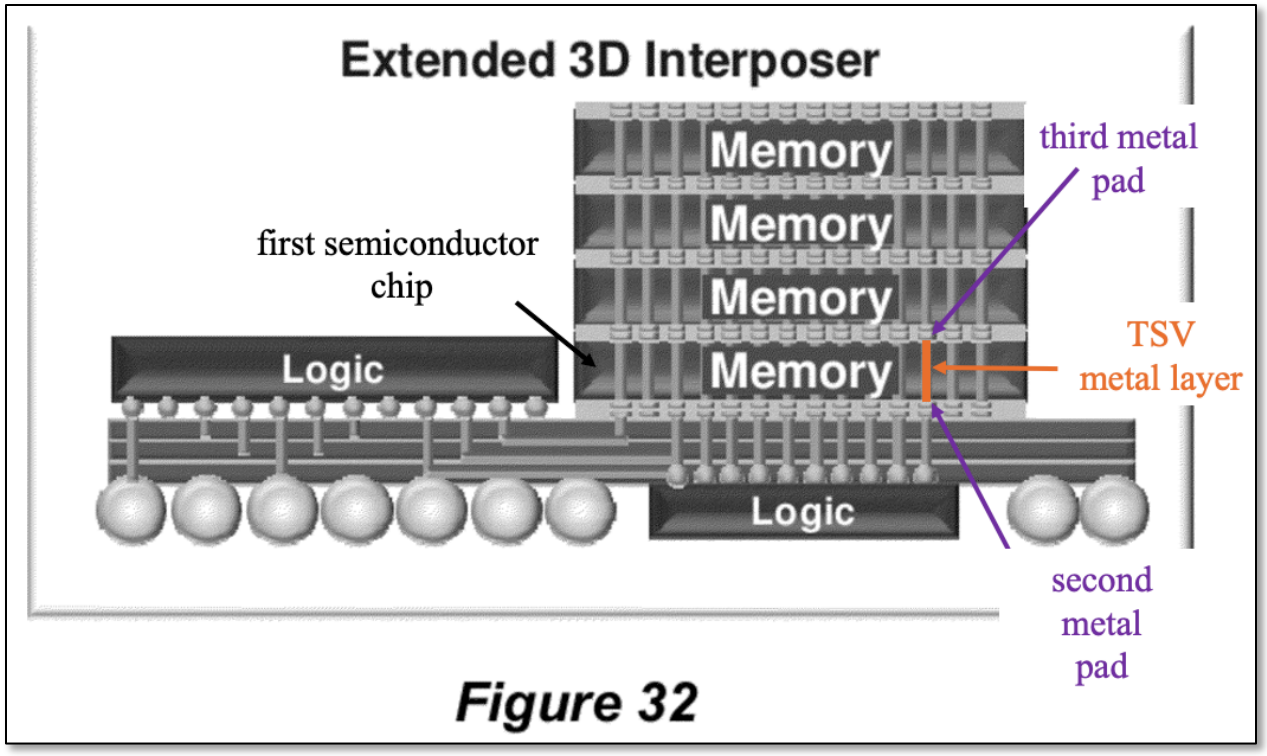
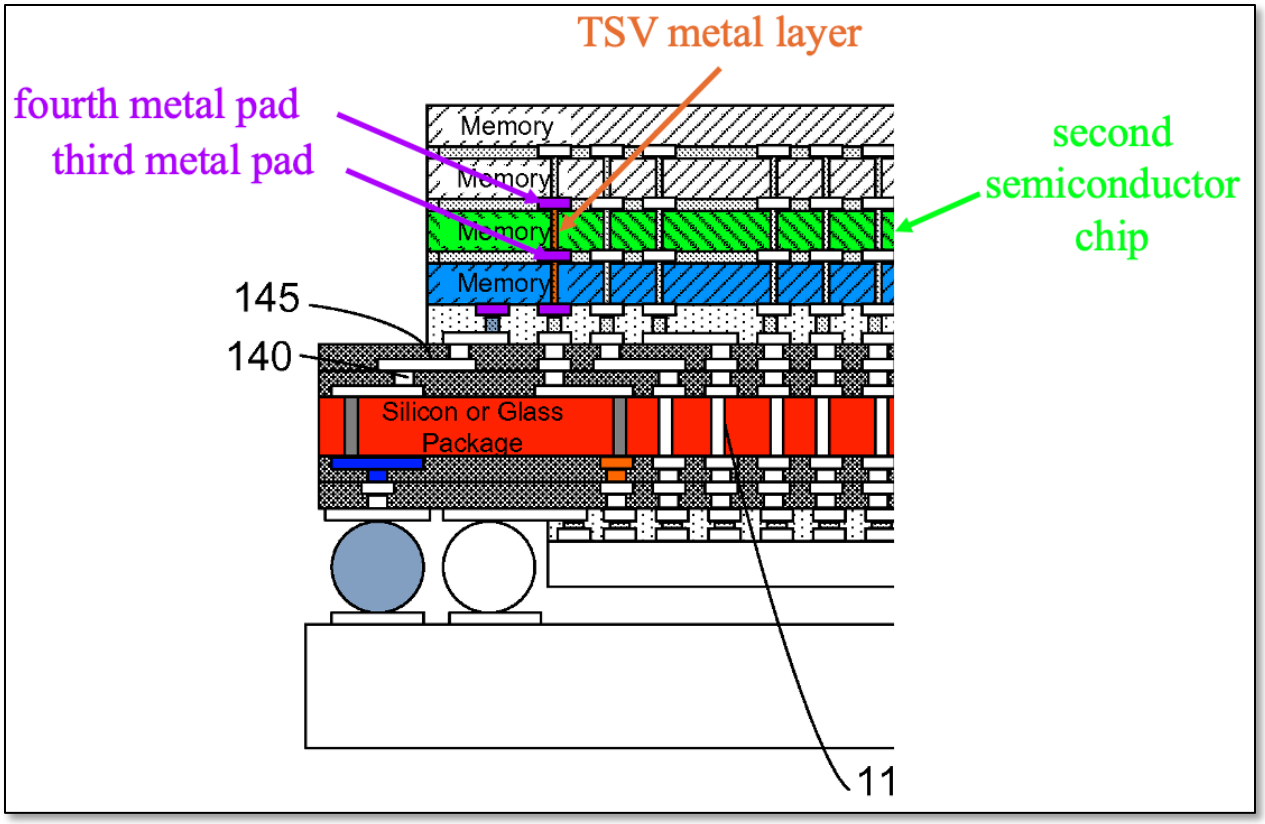


Figure 32

EX1004, FIG. 32; *EX1003*, ¶197.

4. 6(d)

Sundaram teaches the *third metal pad is connected to a fourth metal pad of said second semiconductor chip* through another TSV metal layer.



EX1004, FIG. 3 (excerpt); *EX1003*, ¶198.

FIG. 32 also teaches a *third metal pad* of a first chip *connected to a fourth metal pad of* a *second semiconductor chip*.

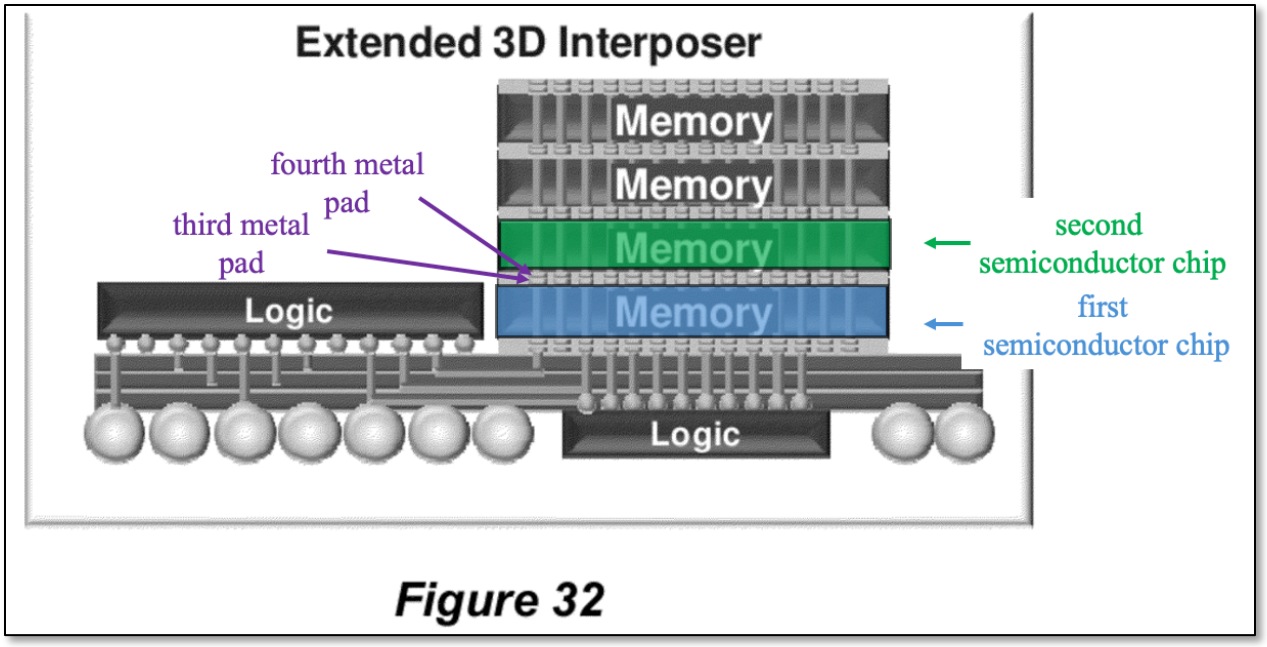


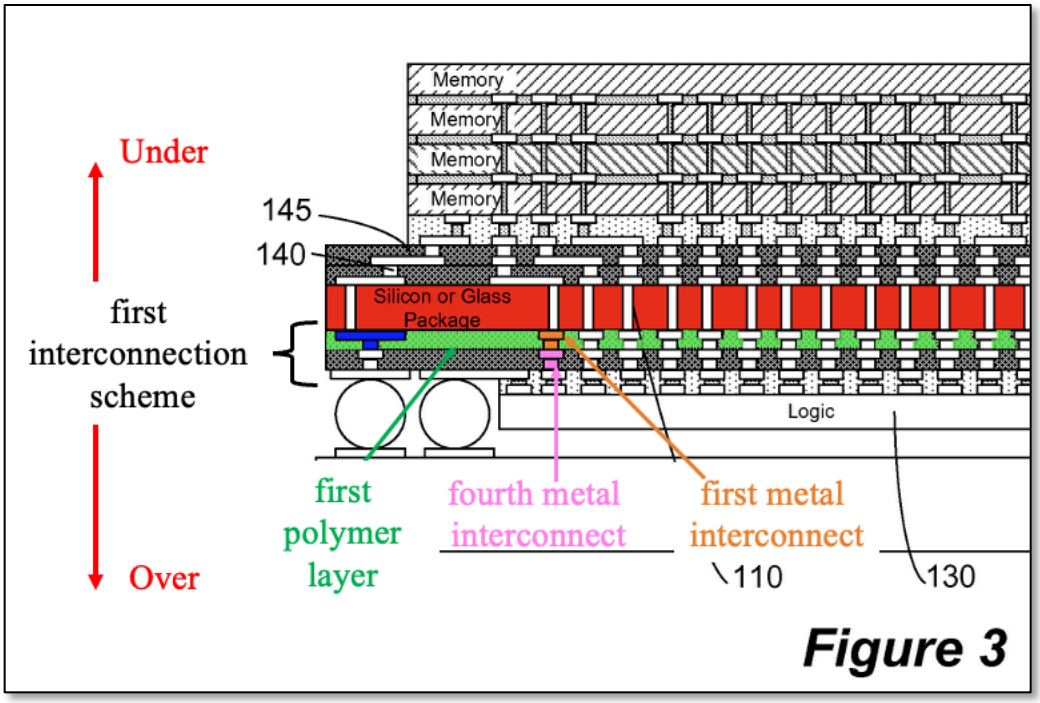
Figure 32

EX1004, FIG. 32; *EX1003*, ¶199.

G. Claim 7

1. 7(a)

Sundaram's *first interconnection scheme* comprises a *fourth metal interconnect*, namely a blind via 140 and conductor trace 145 that are *over* the via 140 of the *first metal interconnect* (*see* Section V.A.11) *and over said first polymer layer*.



EX1004, FIG. 3 (excerpt); *EX1003*, ¶200.

Alternatively, die pad 135 is a *fourth metal interconnect over said first metal interconnect and said first polymer layer*.

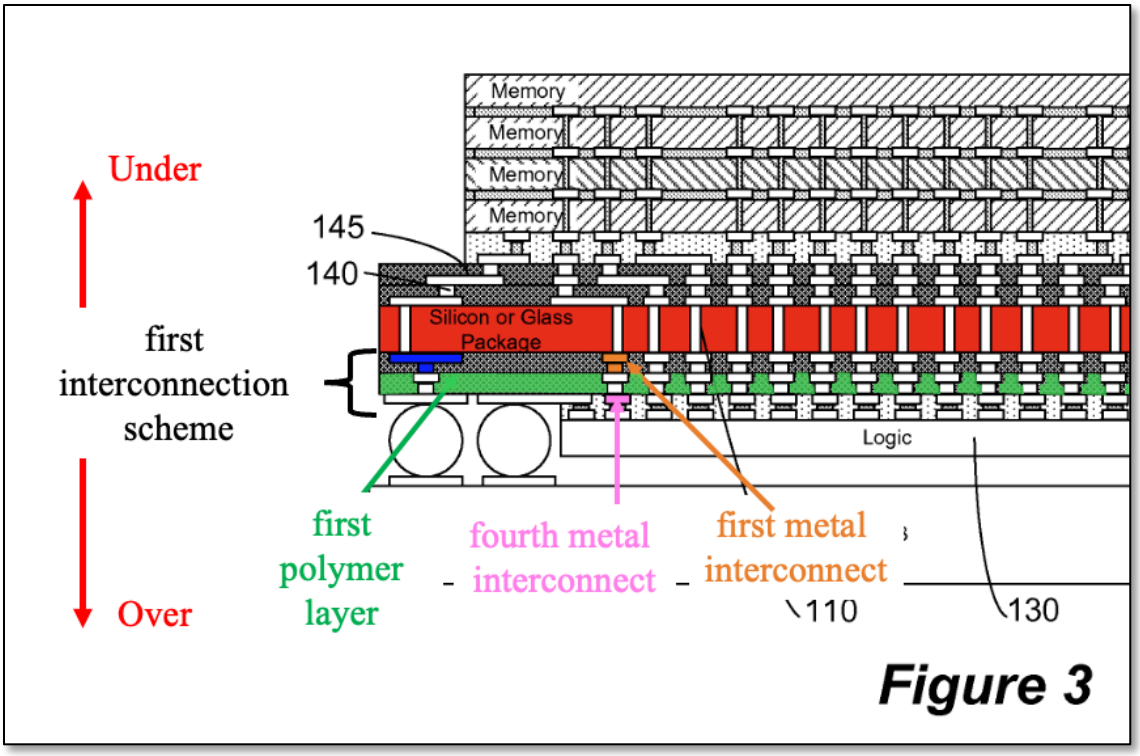


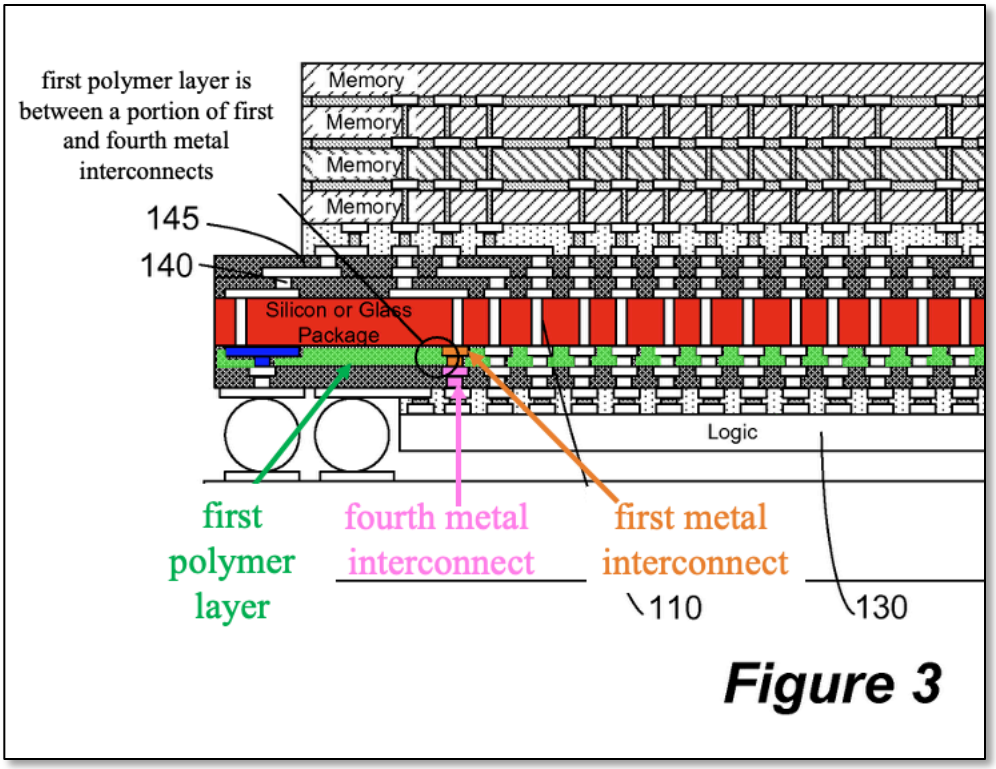
Figure 3

EX1004, FIG. 3; *EX1003*, ¶201.

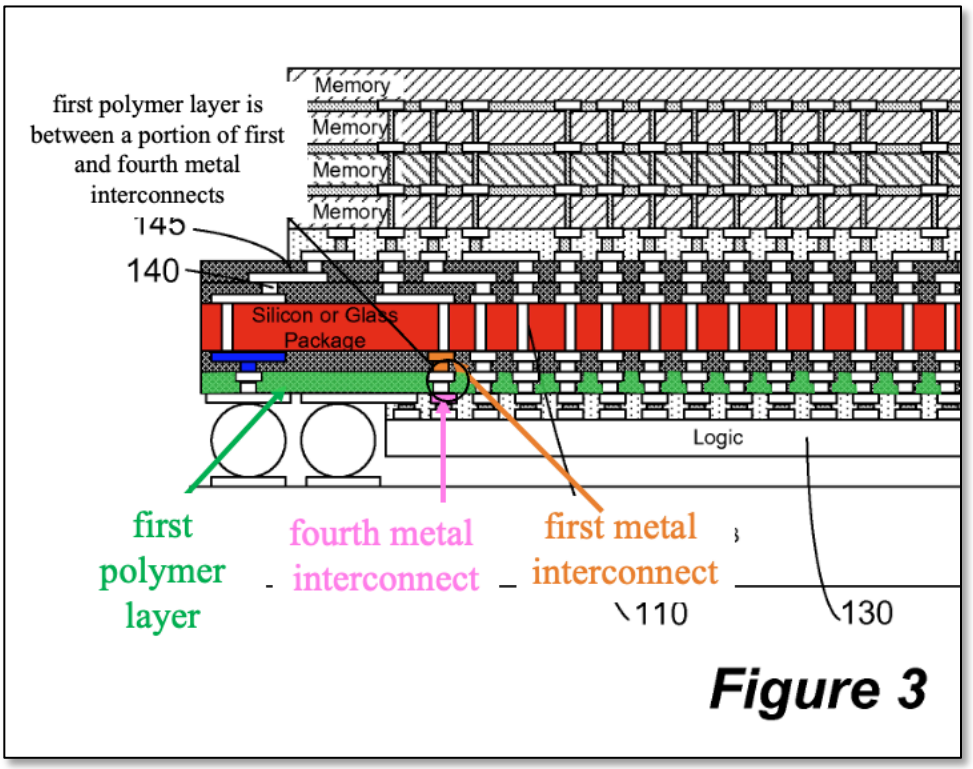
2. 7(b)

Under either mapping of the *fourth metal interconnect* and the *first polymer layer*, Sundaram's *first polymer layer*[4] is *between said first and fourth metal interconnects*, as shown:

[4] Petitioners interpret Claim 7(b)'s *first polymer* as referring to the *first polymer layer* introduced in Claim 1(c)(i).



EX1004, FIG. 3 (excerpt); *EX1003*, ¶202.



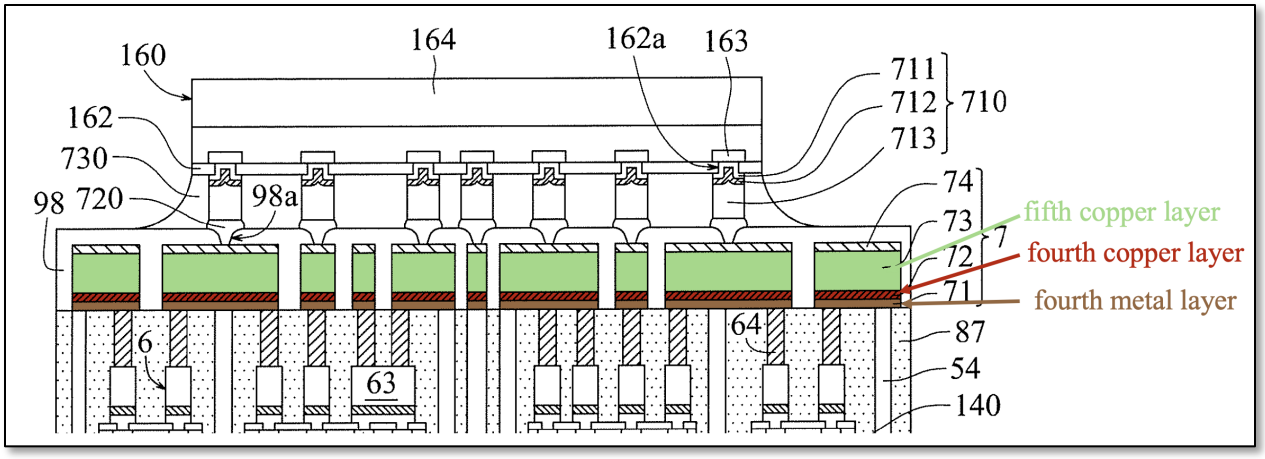
EX1004, FIG. 3 (excerpt); *EX1003*, ¶203.

3. 7(c)

See Section V.A.13 (Sundaram's multilayer interconnect teachings); *EX1003*, ¶204.

a) Lin-191's Teachings

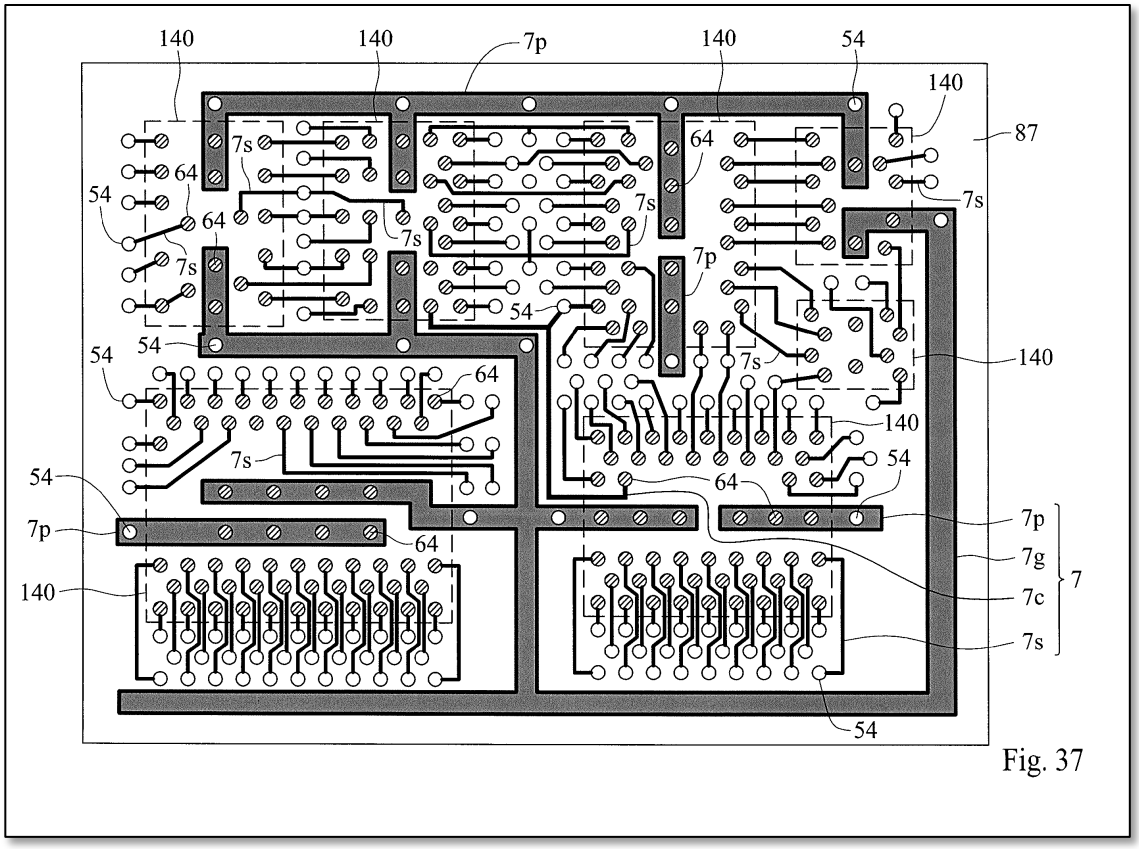
Lin-191 teaches a multilayered metal interconnect with two copper layers and a metal layer, namely, a "patterned metal layer 7" having an "adhesion layer 71, the seed layer 72, the metal layer 73, and the barrier/wetting layer 74" *EX1005,* [0379]. Layer 7 interconnects metal pillars or bumps 64 to various other structures in Lin-191's package and, therefore, is a *metal interconnect*. *EX1005*, [0379]; *EX1003*, ¶205. Adhesion layer 71 is a *metal* (e.g., titanium or nickel) and is thus a *fourth metal layer*. *EX1005,* [0260]-[0264]. Seed layer 72 is "a copper layer" on adhesion layer 71 and is thus a *fourth copper layer on said fourth metal layer*. *EX1005*, [0261]-[0264]. Metal layer 73 "can be…a copper layer…on the seed layer 72" and is thus a *fifth copper layer on said fourth copper layer*. *EX1005*, [0420].



EX1005, FIG. 72 (excerpt); *EX1003*, ¶205.

b) MTC

A POSITA would have been motivated and found obvious to apply Lin-191's teachings of patterned metal layer 7 to Sundaram's via 140 and trace 145 or die pad 135 forming the *fourth metal interconnect*. *EX1003*, ¶206. Lin-191's FIG. 37 illustrates "a schematic top perspective view of the patterned metal layer 7," and, as shown, layer 7 makes lateral electrical connections (e.g., from a bump 54 to a bump 64) such that a POSITA would have understood layer 7 as being an RDL, like Sundaram's RDL.



EX1005, FIG. 37, [0017], [0272-0273]; *EX1003*, ¶207.

The modification would have predictably improved Sundaram's chip package by providing a low resistance current path for signals traveling between the *first metal interconnect* and *fourth metal interconnect*. *EX1003*, ¶208. Copper (i.e., layers 73 and 72) has a low resistivity, high conductivity, and high immunity to electromigration, making copper an attractive option for interconnect applications. *EX1003*, ¶¶208-209.

Additionally, the modification would have predictably improved Sundaram's chip package by reducing the risk of delamination between the copper interconnect

and the metal layers it interconnects and mitigating diffusion of copper into the metal layers it interconnects, both which may negatively impact electrical reliability and ruggedness of the chip package. *EX1003*, ¶210.

The modification is application of a known technique (Lin-191's multi-layer interconnect) to a known component (Sundaram's *fourth metal interconnect*) ready for improvement to yield the predictable result of Sundaram's *fourth metal interconnect* comprising the layers of Lin-191's layer 7. *EX1003*, ¶211. There would have been a REOS at least because methods of forming layered interconnects were well known. *Id.* Further, because Lin-191's layer 7 is an RDL, and Sundaram's RDL is being modified per layer 7's teachings, there would have been a REOS. *Id*.

H. Claim 8

Sundaram teaches "polymer-metal redistribution layers" are "deposited **on the first side 115**…of the interposer 105" and that die pads 135 are formed on first side 115. *EX1004*, 6:62-67; 6:29-33. The RDL and die pads 135 on first side 115 is *a second interconnection scheme under said solid layer and on said second surface* because the RDL "connect[s]" the "electronic devices" 125 and 130. *Id*.

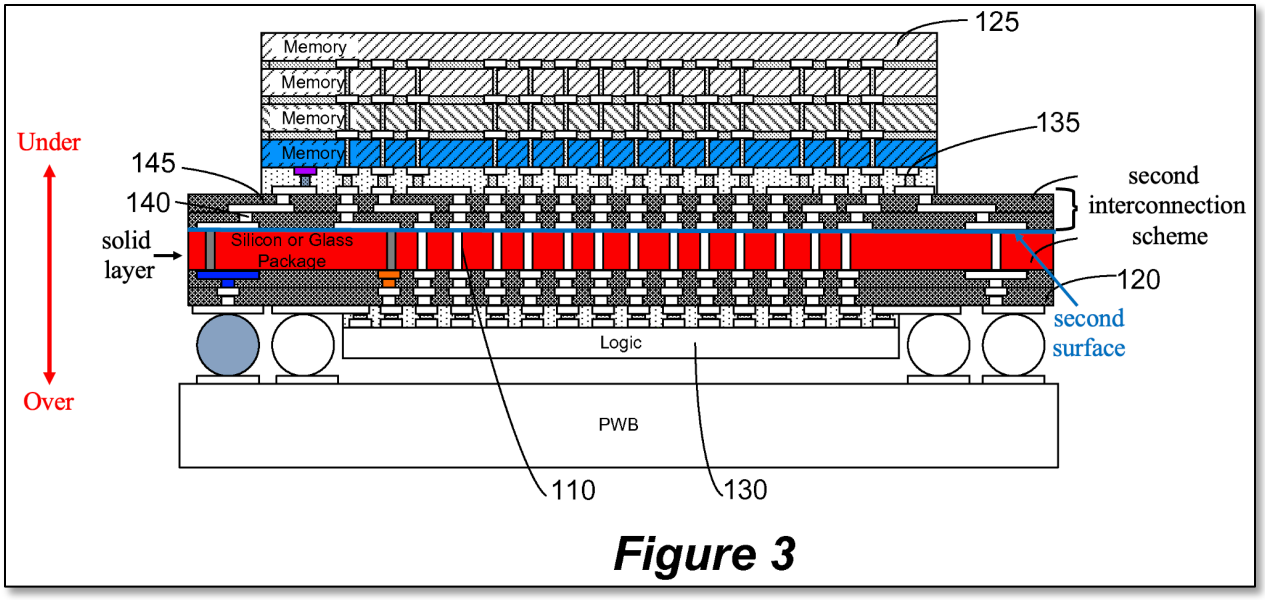


Figure 3

EX1004, FIG. 3; *EX1003*, ¶212.

I. Claim 9

Sundaram alone or Sundaram-Lin-191 teaches a *first metal pad*. *See* Section V.A.18. Lin-191 teaches metal pads 163 that "include **aluminum**." *EX1005*, [0384]. Metal pads are used for interconnecting chips to other components, where metal is used for the connection because it provides low resistance. *EX1003*, ¶¶213-214. Lin-191 teaches specifically a metal pad that is aluminum such that a POSITA would have found obvious and been motivated to apply Lin-191's *aluminum pad* teachings to Sundaram's *first metal pad*. *Id.* Aluminum was a well-known and widely used material for forming contact pads in chips, as it is compatible with established bond wire attachment methods, low cost, and consistent with legacy materials used in semiconductor processing. *Id*. It would have been a cost-effective and commonly-used choice to form Sundaram's pad, which would have had a REOS. *Id*. The

modification is combination of prior art elements according to known methods to yield predictable results. *Id*.

J. Claim 10

Sundaram teaches interposer 105 (*solid layer*) comprises a *third region*[5], which is on the *opposite* side of the *first region* than the *second region* and is, therefore, *opposite to said second* region. The *third region* comprises *copper plugs* in *through vias*.

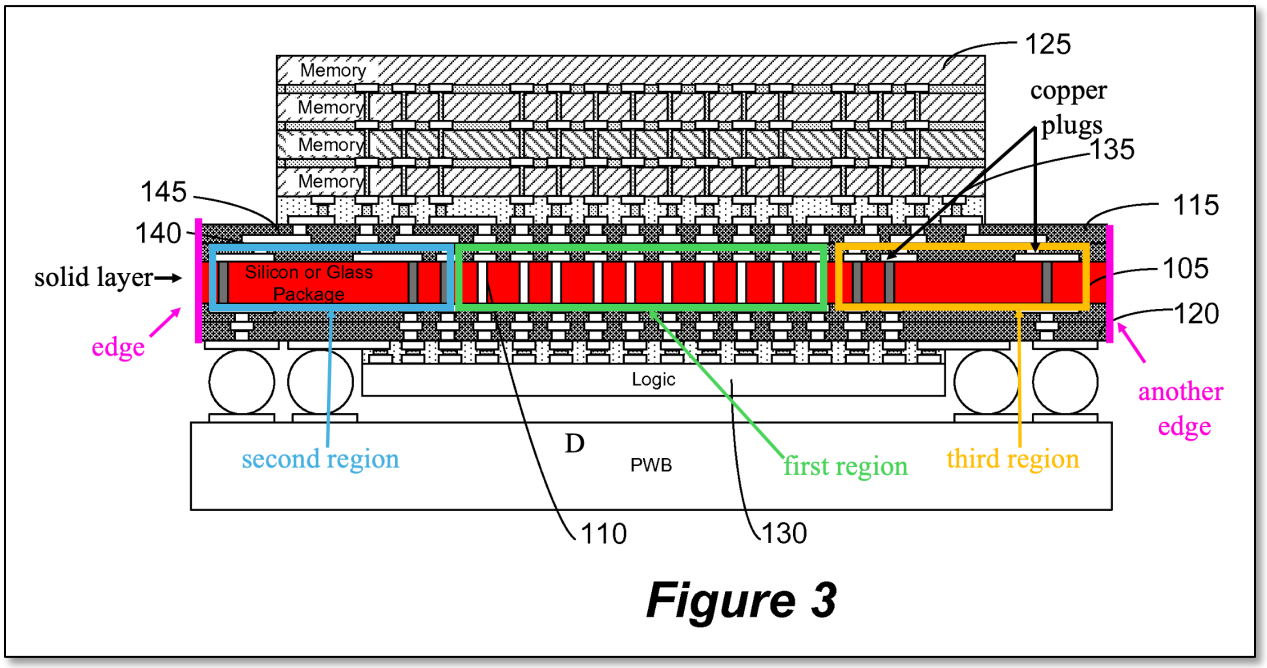


Figure 3

EX1004, FIG. 3, 6:6-9; *EX1003*, ¶215.

[5] The *third region* is not described in the '763 Patent's specification but was introduced by Applicant during original prosecution. *EX1002*, 351-360. Applicant relied solely on FIG. 6l to support the *third region*.

K. Claim 11

Sundaram teaches or renders obvious Claim 11. Sundaram's interposer 105 has a *thickness between 100 and 300 micrometers*. *See* Section V.A.5 (supporting caselaw); *EX1003*, ¶217 (citing *EX1032*, 535-537 and opining no criticality of claimed plug thickness because Applicant argued plug thickness was the same as the substrate's thickness). Through vias 110 "can be defined within the interposer 105 such that each of the through vias 110 extends from the first side 115 to the second side 120[.]" *EX1004*, 6:6-9, 2:22-29 (interposer is 20-200 micrometers thick). Thus, through vias 110 (*first copper plug*) have a thickness equal to that of the *solid layer* i.e., *between 100 and 300 micrometers*. *EX1004*, FIG. 3; *EX1003*, ¶216.

L. Claim 12

Sundaram teaches or renders obvious a third through via 110 (*third copper plug*) that is *vertically in one of said plurality of through vias in said solid layer*.

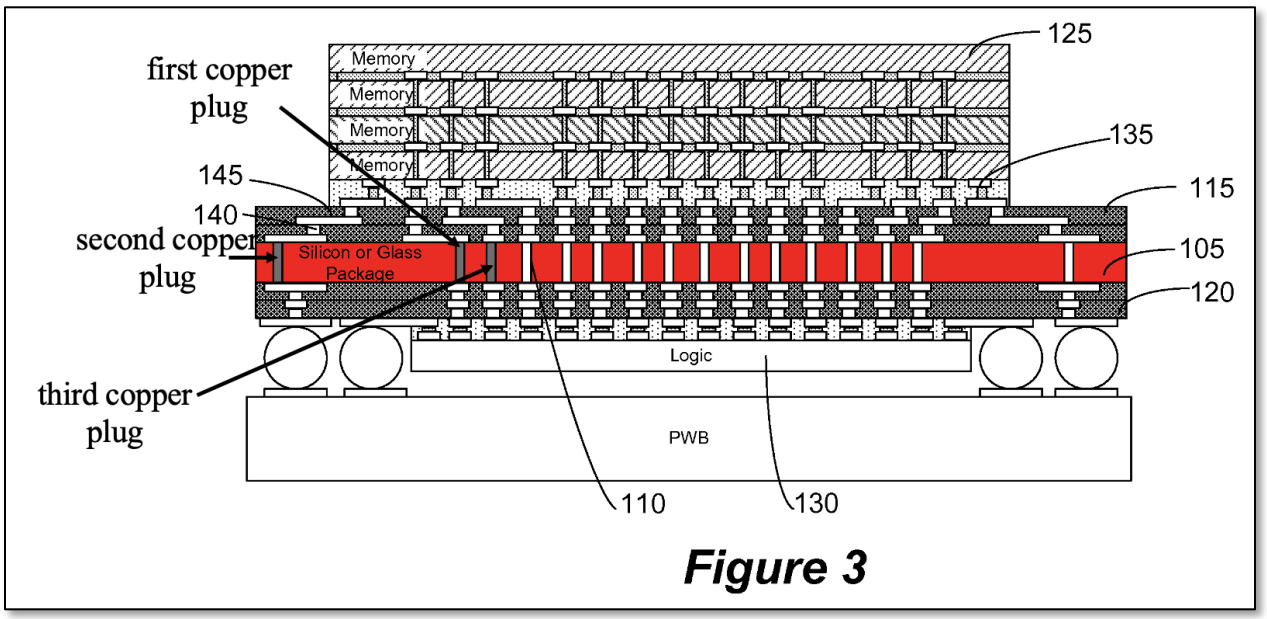
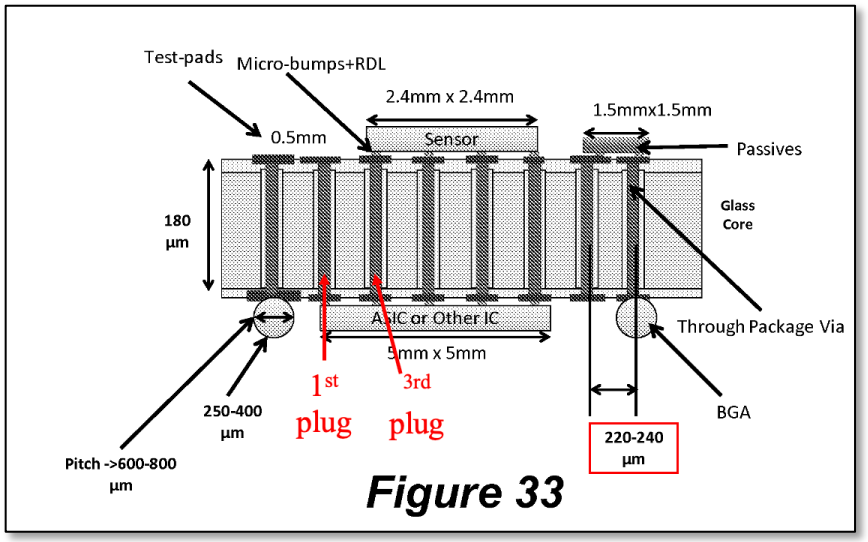


Figure 3

EX1004, FIG. 3; *EX1003*, ¶218.

FIG. 33 teaches through vias having a pitch between "220-240 mm." Annotated below, are *first* and *third plugs* like in FIG. 3. Thus, the *pitch between* the first and third plugs is 220-240 mm, anticipating or rendering obvious the claimed *between 200 and 1000 micrometers*. *EX1004*, FIG. 33. *EX1003*, ¶219. FIG. 33 is a specific example of a chip package for "a digital camera for cell phones" with a "through-via interconnect density" that is "substantially the same" as "the first electronic device 125 or the second electronic device 130 it connects." *EX1004*, 6:42-50.



EX1004, FIG. 33; *EX1003*, ¶220.

The '763 Patent does not ascribe any criticality to the claimed range of between 200 and 1000 micrometers. The '763 Patent describes smaller (5 micrometers) and much larger values (10,000 micrometers), indicating to a POSITA

the thickness varies widely and is not otherwise critical. *EX1001*, 6:11-18; Section V.A.5 (supporting caselaw); *EX1003*, ¶221.

a) MTC Sundaram's Embodiments

To the extent PO argues FIGS. 3 and 33 are separate embodiments, a POSITA would have found obvious and been motivated to modify the pitch of Sundaram's through vias 110 (*plurality of copper plugs*) according to the FIG. 33 embodiment such that a *pitch between said first and third copper plugs is between 200 and 1000 micrometers*. *EX1003*, ¶222. The modification is expressly motivated by Sundaram because FIG. 33 enables high bandwidth speeds such as "at least about 10 GB/s" between "an image sensor chip" and an "Asic chip" in a "digital camera for cell phones." *EX1004*, 6:42-45; *EX1003*, ¶222.

The combination is the application of a known technique (Sundaram's copper plugs having a pitch between *200 and 1000 micrometers*) to a known device (Sundaram's chip package) ready for improvement to yield predictable results. *EX1003*, ¶222. A POSITA would have a REOS at least because the modification would have been simple and straightforward as methods of controlling pitch of copper plugs were well-known. *Id.*

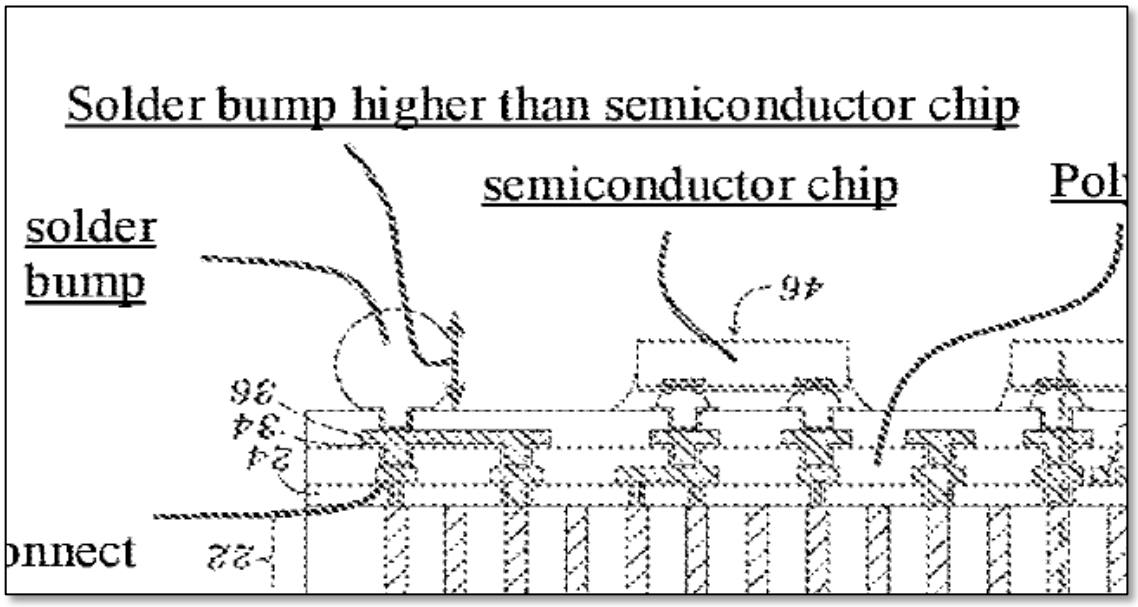
M. Claim 14

1. 14(a)

See Section V.D, reciting corresponding limitations. *EX1003*, ¶223.

2. 14(b)

During original prosecution of the related '768 Patent, PO filed an Amendment with an annotated figure illustrating specification support for Claim 14(b)'s language:



EX1032, 400; *EX1003*, ¶224. Section V.C (caselaw regarding prosecution disclaimer).

Sundaram's *first polymer layer* includes at least the portion described above at Claim 1(c)(i) and further includes the portion highlighted below. *See* Section V.A.11; *EX1003*, ¶225. Shown in FIG. 3, Sundaram's device 130 (*second semiconductor chip*) *has a height [that] is between a backside surface of* device 130 *and a top surface of* Sundaram's *first polymer layer*, which is *smaller than thickness* of Sundaram's solder ball (*first metal bump*). *See* Section V.A.9 (supporting caselaw).

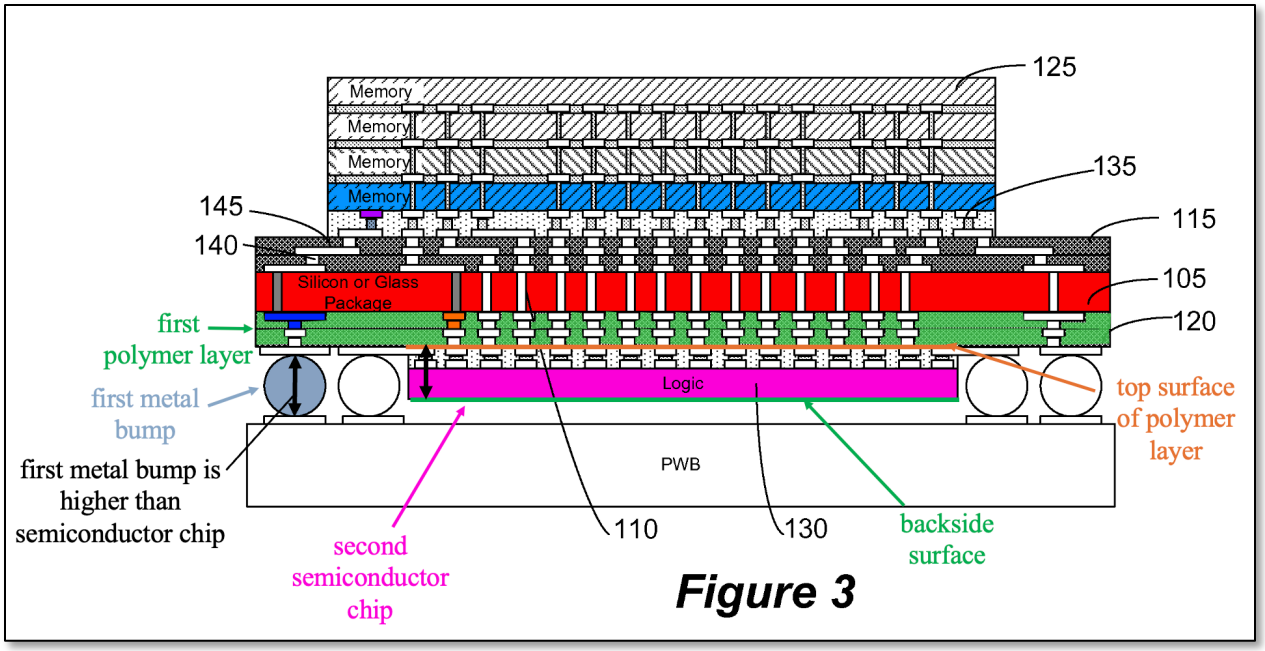


Figure 3

EX1004, FIG. 3; *EX1003*, ¶225.

Alternatively, Sundaram's *first polymer layer* is as annotated below, which also meets the claim limitation.

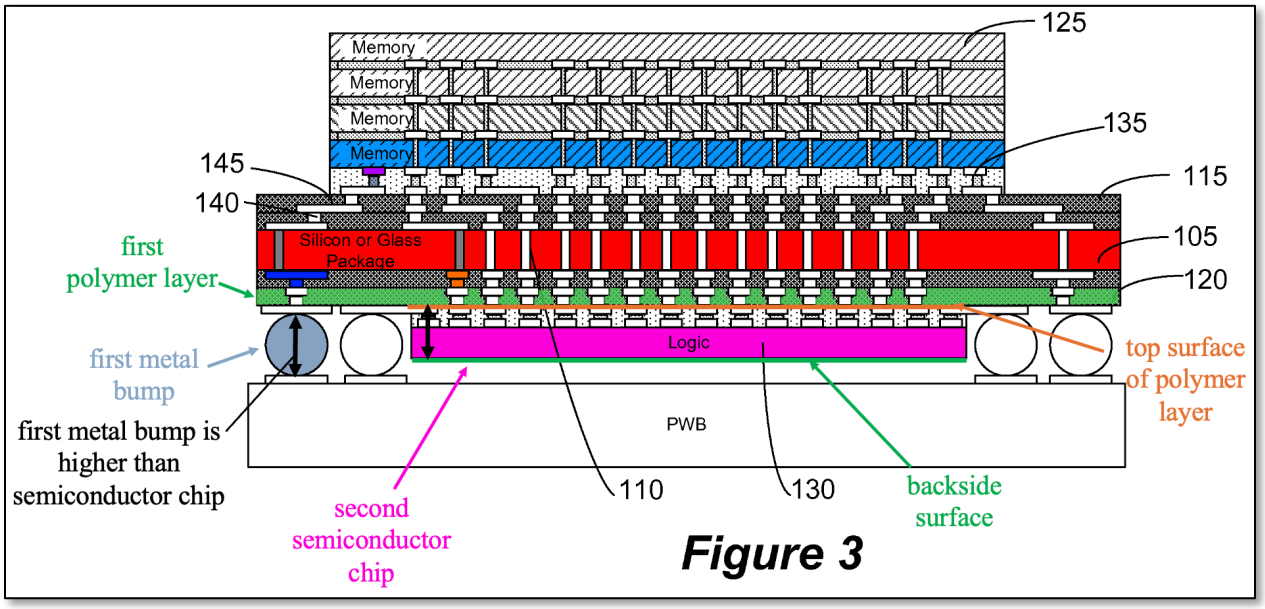


Figure 3

EX1004, FIG. 3; *EX1003*, ¶226; *see* Section V.A.9 (supporting caselaw).

N. Claim 16

Sundaram teaches the "3D interposer…[is] scalable for increased number of dies, not only above and below the interposer but also side by [side.]" *EX1004*, 7:56-59, 4:26-27. Sundaram's side-by-side configuration teaches *a second semiconductor chip under said first interconnection scheme next to said first semiconductor chip*:

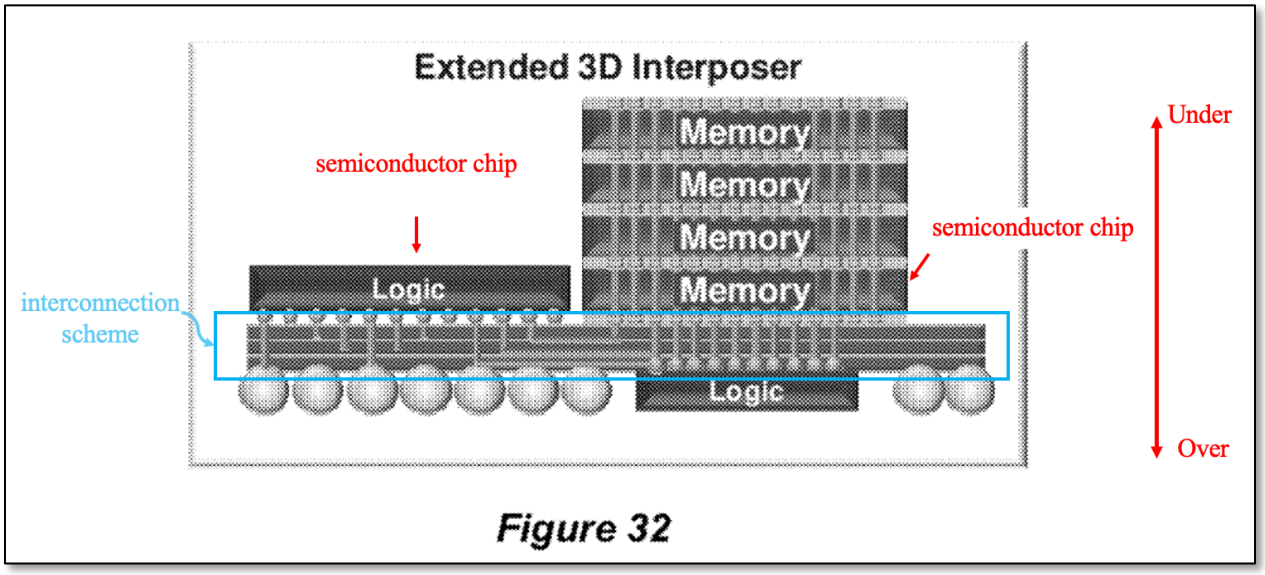


Figure 32

EX1004, FIG. 32. *EX1003*, ¶227. A POSITA would have been motivated and found obvious to modify FIG. 3 with the teachings in FIG. 32 of integrating DRAM and logic die into the same package to advantageously improve the data processing speed can be significantly improved due to the shorter transmission path between the two components, reducing latency and enhancing overall system performance. *EX1003*, ¶227. There would have been a REOS because adding a chip next to FIG. 3's chip 125 would have been simple and straightforward. *Id*.

O. Claim 17

See Section V.A.4. Sundaram teaches both a borosilicate glass interposer and a silicon interposer with an SiO_2 layer. *EX1004*, 9:14-16, 13:58-62, FIG. 34. Borosilicate glass includes silica (SiO_2), teaching Claim 17. *EX1003*, ¶228.

P. Claim 18

1. 18(Pre)

See Section V.A.1.

2. 18(a)

See Section V.A.2.

3. 18(a)(i)

See Section V.A.4.

4. 18(a)(ii)

See Section V.A.5.

5. 18(a)(iii)

See Section V.A.6.

6. 18(b)

See Section V.A.7, reciting corresponding limitations. *EX1003*, ¶234.

7. 18(b)(i)

The metalized through vias 110 (*plurality of metal conductors*) "can be metalized with a highly-conductive metal, for example copper" (*a copper portion*)

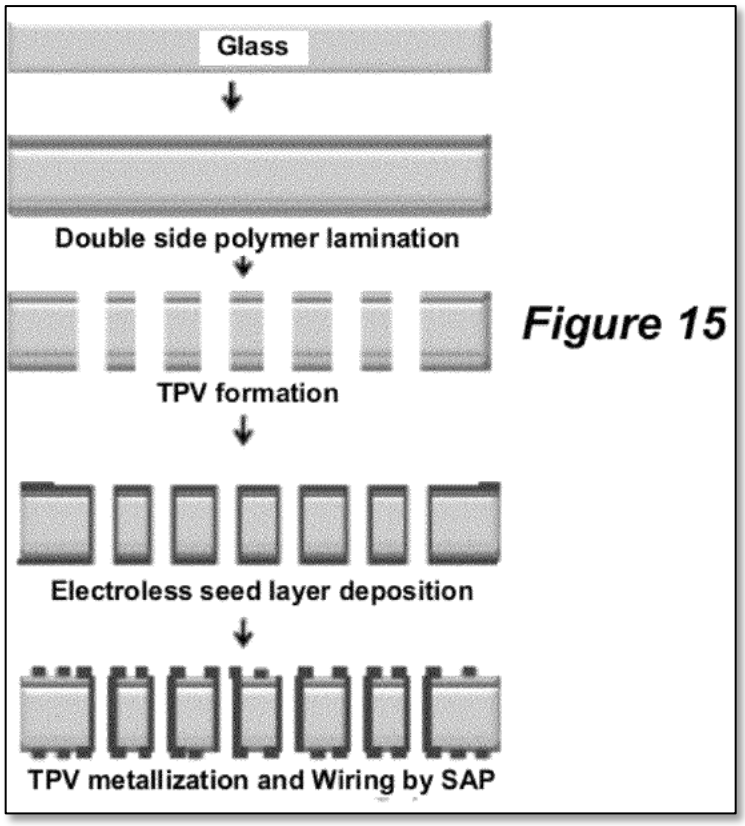
and "can also be metalized with…a metal seeding liner" (*a first metal layer covering a sidewall of said copper portion*. *EX1004*, 6:25-29.

Interposer 105 is "about 20 to about 200 micrometers in thickness" and the "thickness of the interposer to via diameter aspect ratio is about **1:1 to about 10:1**." *EX1004*, 2:22-29. Thus, through vias 110 have *a diameter in a direction between 50 and 200 micrometers*, e.g., of *200 micrometers* when the interposer thickness is 200 micrometers and the interposer to via diameter aspect ratio is 1:1 or of *50 micrometers* when the aspect ratio is 4:1. *EX1003*, ¶¶235-236. Sundaram therefore teaches or renders obvious Claim 18(b)(i). *See* Section V.A.5 (supporting caselaw); *EX1003*, ¶237 (citing *EX1001*, 4:46-50 and opining no criticality of the claimed copper portion diameter).

Additionally, Sundaram teaches "TPV metallization consist[ing] of two steps: 1) Cu seed layer formation, and 2) Cu electroplating" where the seed layer is "about **0.5-1 mm thick**." *EX1004*, 13:30-34. Thus, Sundaram teaches through vias 110 have *a diameter…greater than a thickness of said first metal layer* (0.5-1 mm) *in said direction*. A POSITA would have understood the Cu electroplating step to involve plating on the Cu seed layer such that the seed layer (*first metal layer*) *cover[s] a sidewall* of the plated layer (*copper portion*). *EX1003*, ¶238.

a) MTC

To the extent PO argues Sundaram's teachings of the Cu electroplating to be a separate embodiment, a POSITA would have been motivated and found obvious to modify Sundaram's glass interposer to have copper filled vias as taught in Sundaram's Polycrystalline Interposer Example #6. *EX1003*, ¶239. A POSITA would have found obvious at least because Sundaram also teaches forming TPVs in glass substrate with a seed layer.



EX1004, FIG. 15. A POSITA would have recognized that a seed layer advantageously reduces void formation during copper growing, and using a seed layer was a commonplace method for forming a via. *EX1003*, ¶¶239-240.

8. 18(b)(ii)

See Section V.A.9.

9. 18(c)

See Section V.A.10.

10. 18(c)(i)

See Section V.A.11.

11. 18(c)(ii)

See Section V.A.12.

12. 18(c)(iii)

See Section V.A.13, reciting corresponding limitations. *EX1003*, ¶245.

13. 18(d)

Sundaram teaches *a second interconnection scheme*, i.e., a second "polymer-metal redistribution layer[] deposited on the first side 115…of the interposer," which is *under said second surface*.

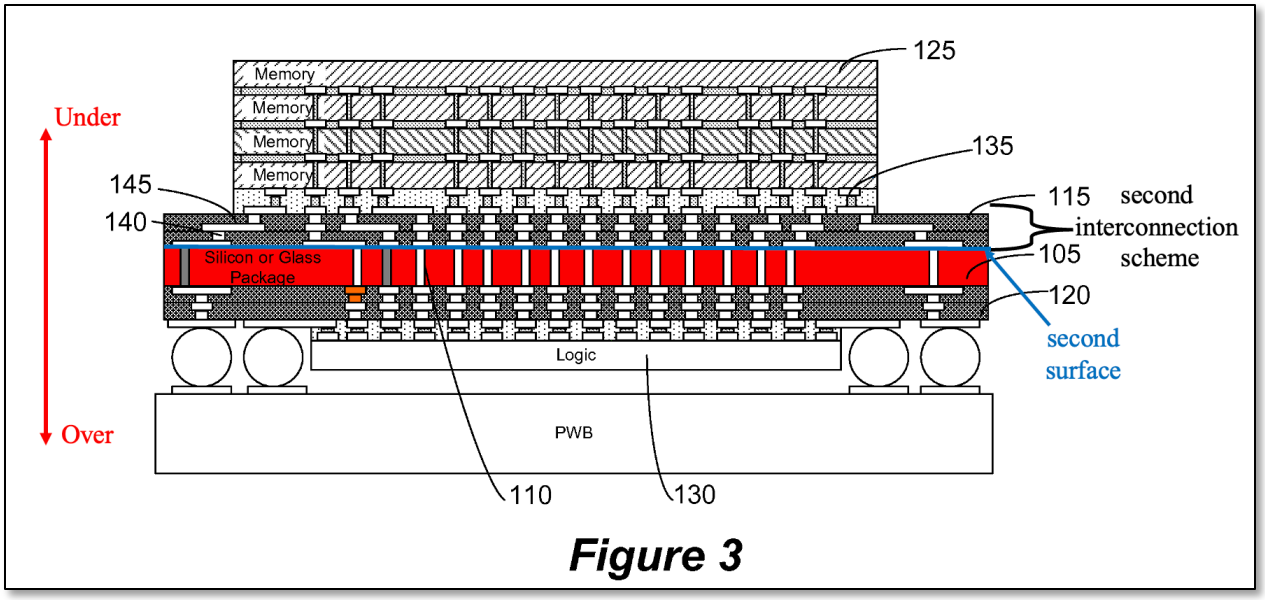


Figure 3

EX1004, FIG. 3, 6:62-67; Section V.H; *EX1003*, ¶246.

14. 18(d)(i)

See Sections V.P.10, V.A.11. Sundaram's RDLs are "polymer-**metal**" and include *interconnects* in the form of "blind vias 140 and conductor traces 145." *EX1004*, 6:62-67. Sundaram's *second metal interconnect* and *second polymer layer*, which is *under said second metal interconnect* are below:

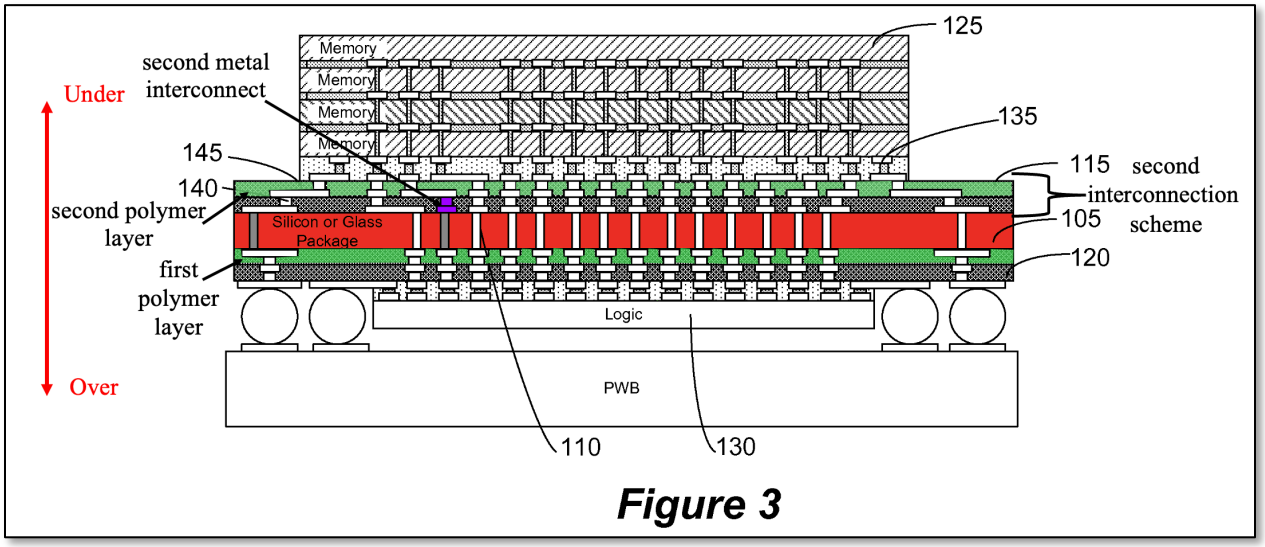
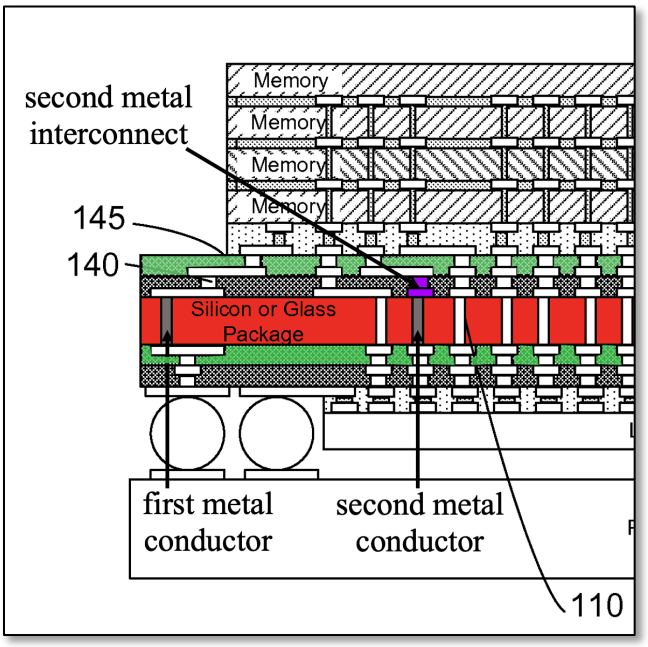


Figure 3

EX1004, FIG. 3; *EX1003*, ¶247.

15. 18(d)(ii)

As seen in FIG. 3, below, Sundaram's *second metal interconnect is connected to a second metal conductor*:



EX1004, FIG. 3 (excerpt); 7:4-9; *see* Section V.A.12; *EX1003*, ¶248.

16. 18(d)(iii)

Sundaram's trace 145 comprises a *second copper layer*. *See* Sections V.P.12, V.A.13; *EX1004*, FIG. 15; *EX1003*, ¶249.

17. 18(e)

See Section V.A.17.

18. 18(e)(i)

See Section V.A.18, reciting corresponding limitations. *EX1003*, ¶251.

19. 18(e)(ii)

See Section V.A.19.

20. 18(e)(iii)

Sundaram teaches electronic device 125 (*first semiconductor chip*) is "connected with through vias 110, **blind vias 140, and conductor traces 145**." *EX1004*, 7:4-8. As discussed, blind vias 140, and conductor traces 145, and die pads 135 form *metal interconnect[s]* in the *second interconnection scheme* such that via 140 and die pad 135, below, are *a third metal interconnect*. *See* Section V.P.14. Shown below, the bump (*first metal bump*) on electronic devices 125 *is connected to a third metal interconnect of said second interconnection scheme*:

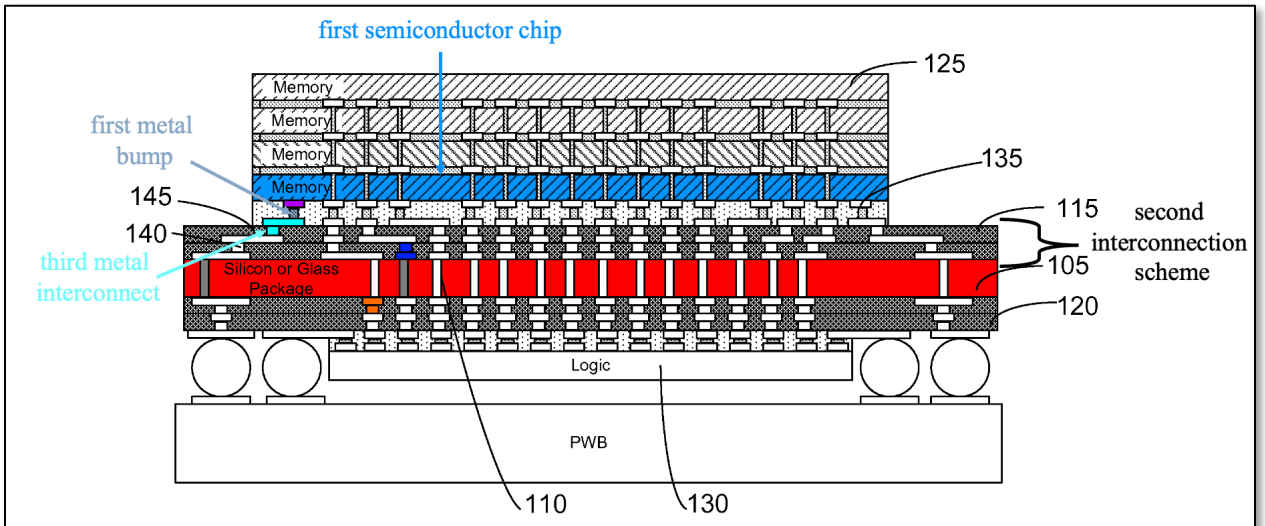


Figure 3

EX1004, FIG. 3, 6:29-32 ("The die pads 135 that are formed on the first 115 and second sides 120…can electrically connect devices using solder, copper bumps with solder caps…."); *EX1003*, ¶253.

Q. Claim 19

See Section V.O.

R. Claim 20

See Section V.B.

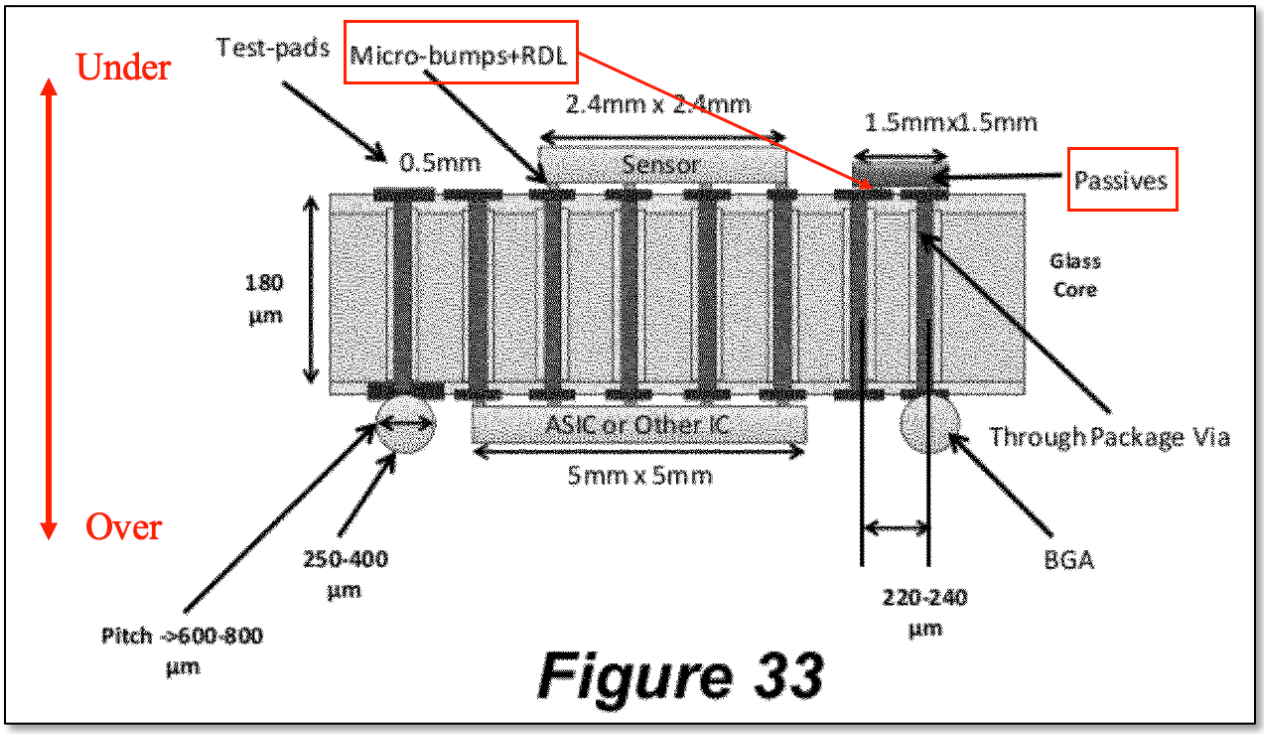


Figure 33

EX1004, FIG. 33; *EX1003*, ¶255.

S. Claim 21

See Section V.E.

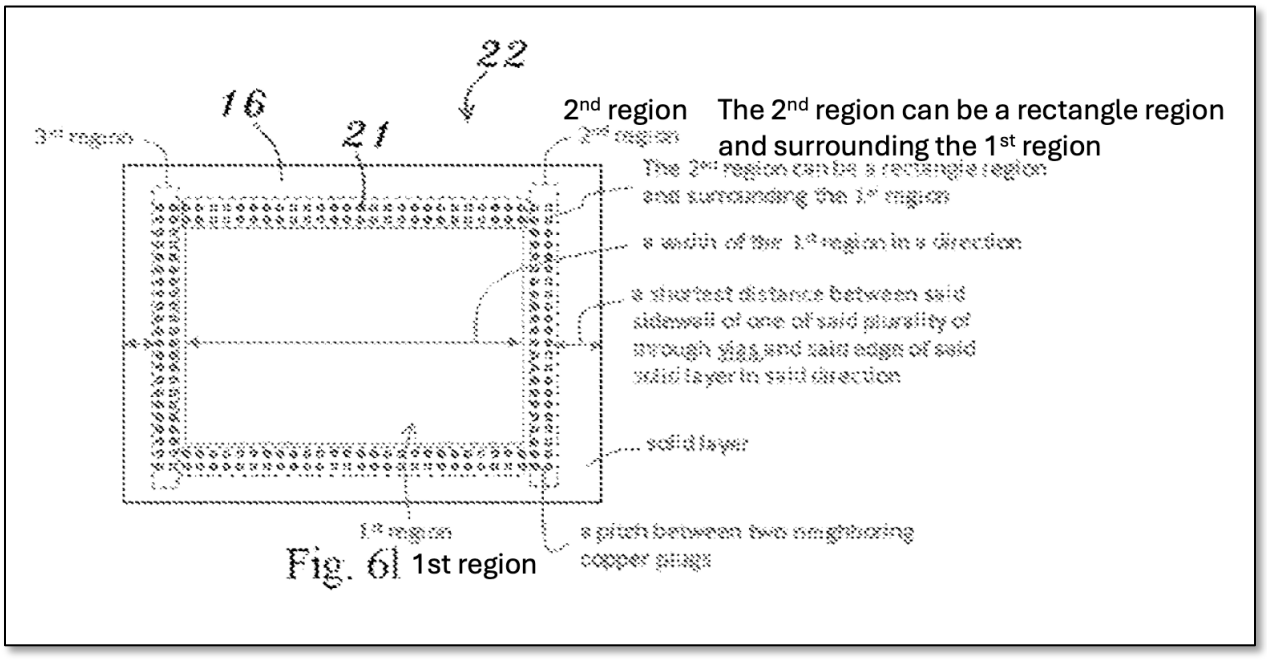
T. Claim 23

See Section V.J.

VI. GROUND 1B: CLAIMS 13 AND 15 ARE OBVIOUS OVER SUNDARAM, LIN-191, AND LIN-863

A. Claim 13

During original examination, PO argued that annotated FIG. 6l shows support for the claimed *rectangle region*.



EX1002, 360; *EX1003*, ¶258.

Sundaram's "FIG. 4 illustrates a top view of the interconnect structure illustrated in FIG. 3," which includes the *first region* and the *second region that is a rectangle region surrounding said first region*. *EX1004*, 3:27-28.

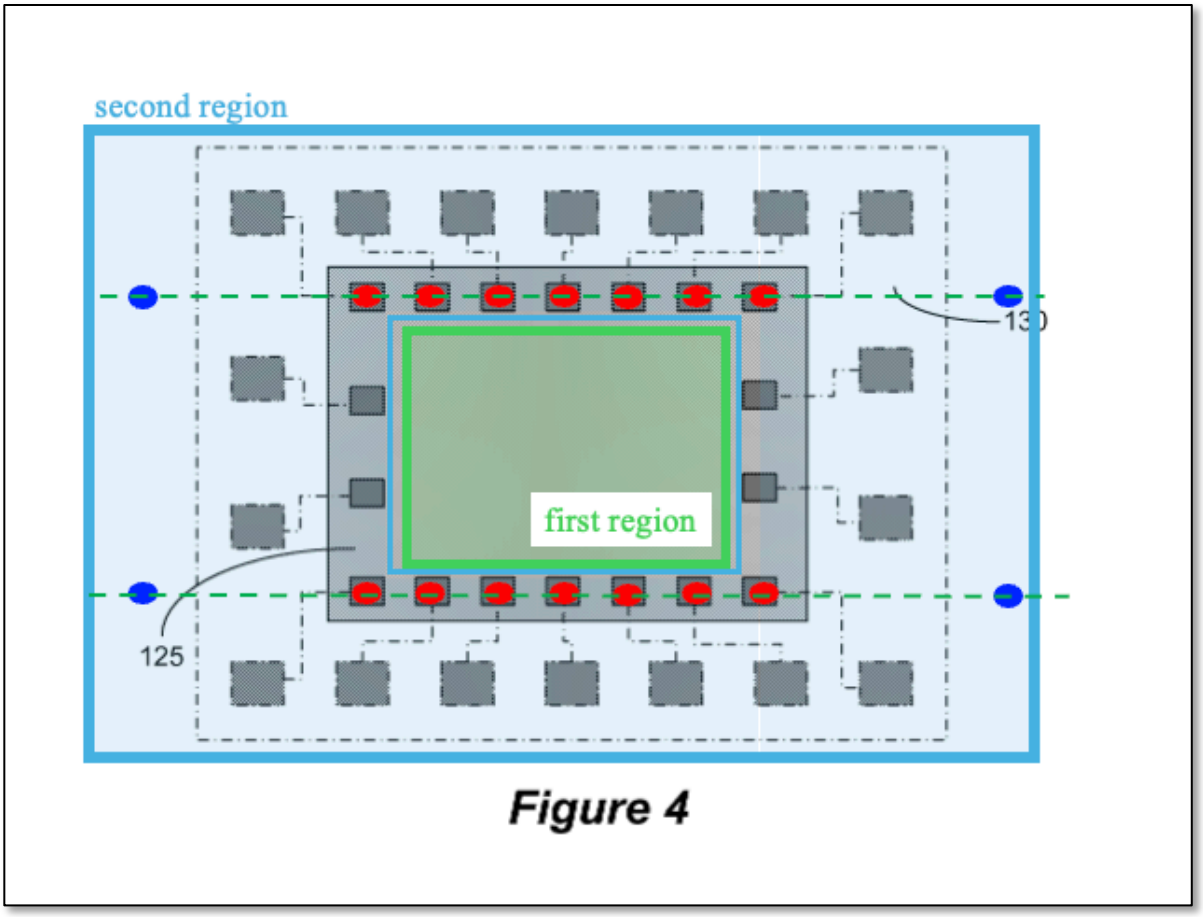


Figure 4

EX1004, FIG. 4.

Sundaram teaches "device 125 is of a different pad size and configuration than" device 130 and "connected with through vias 110, blind vias 140, and conductor traces 145." *EX1004*, 7:1-9, FIG. 4. Based on FIGS. 3-4, a POSITA would have understood Sundaram to teach two types of vias 110: (1) vias for die-to-die connections between devices 125, 130, and (2) vias for die to PWB connections. *EX1003*, ¶259. Further, per FIGS. 3-4, the die-to-die connections (dashed lines in FIG. 4) are made through pads located at the periphery of the dies, which are

connected to the die-to-die vias 110 in interposer 105 (FIG. 3). *Id*. Additionally, per FIG. 3, die-to-die vias 110 and the pads of the smaller device 130 are substantially within the same projection region, while the die-to-PWB vias 110 are located outside the peripheral area of the smaller device 130. *Id.*

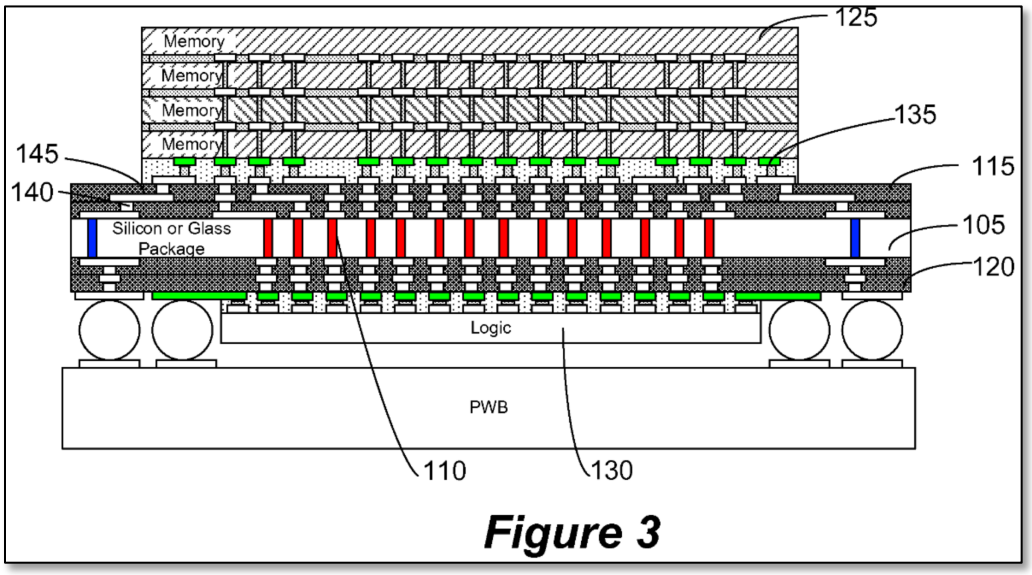


Figure 3

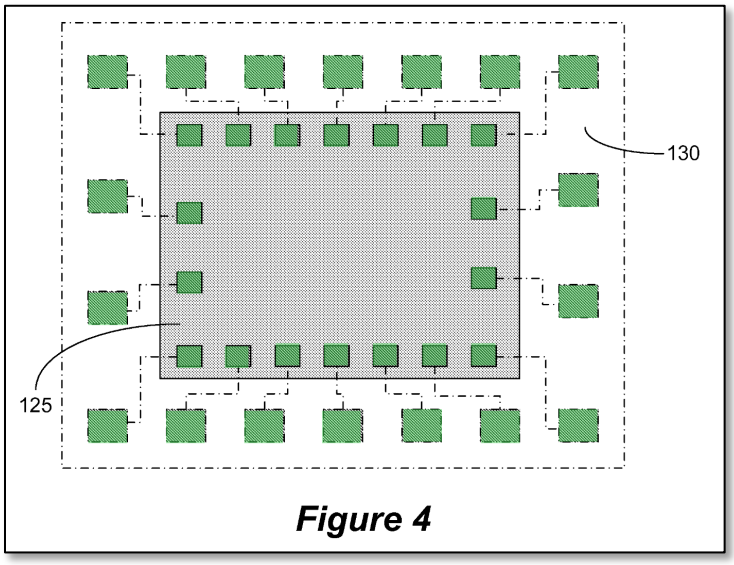


Figure 4

EX1004, FIGS. 3-4[6].

Thus, based on Sundaram's teachings, a POSITA would have understood a plan view of Sundaram's interposer to look as follows, which teaches the claimed *rectangle region*.

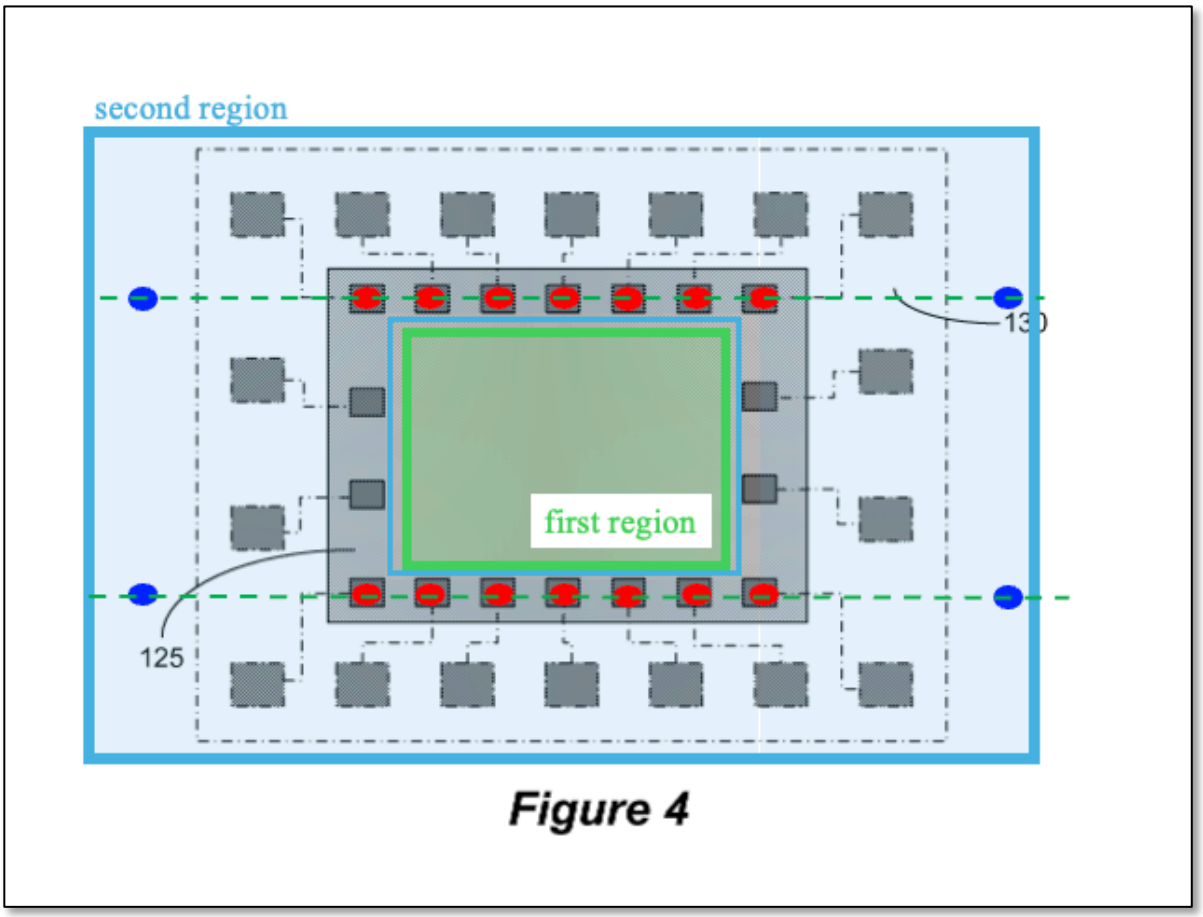


Figure 4

[6] A POSITA would have understood Sundaram's FIG. 4 to mislabel devices 125, 130 based on their depiction in FIG. 3; i.e., per FIG. 3, device 125 is larger than device 130, so the outer box (white) should be device 125, while the inner box (gray) should be device 130. *EX1003*, ¶261.

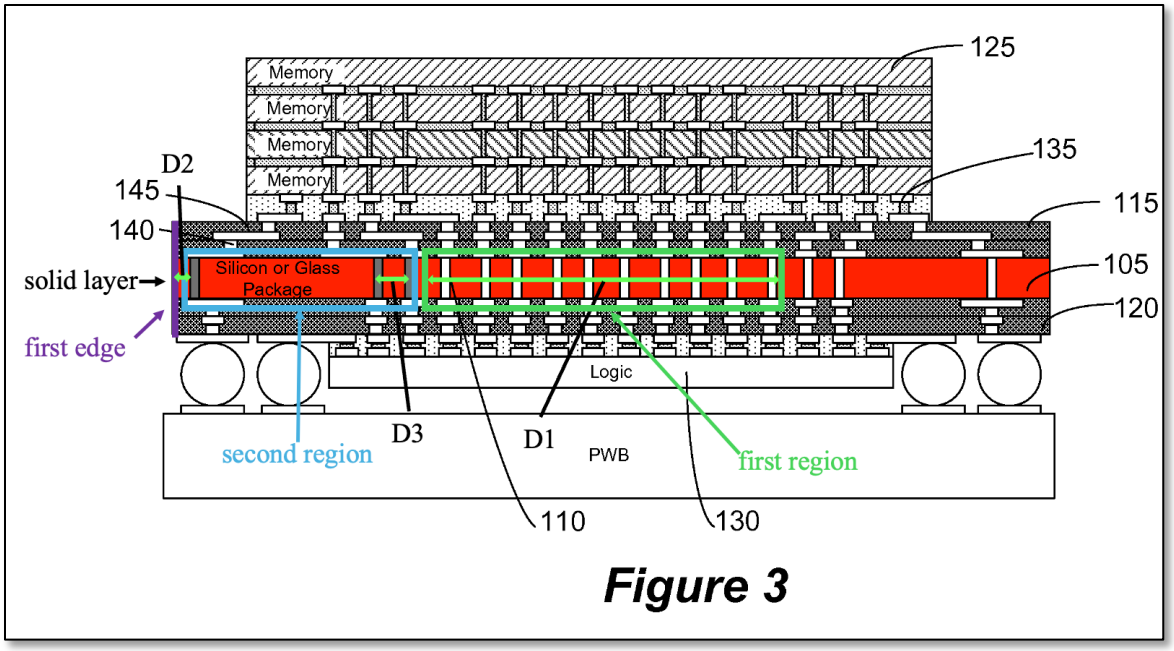


Figure 3

EX1004, FIGS. 3-4; *EX1003*, ¶260. The dashed lines in FIG. 4 illustrate exemplary cross-sectional lines corresponding to FIG. 3's cross-section. *Id*.

To the extent PO argues the *rectangle region* is the right-hand side (per *EX1002*, 360), Sundaram's teaches it:

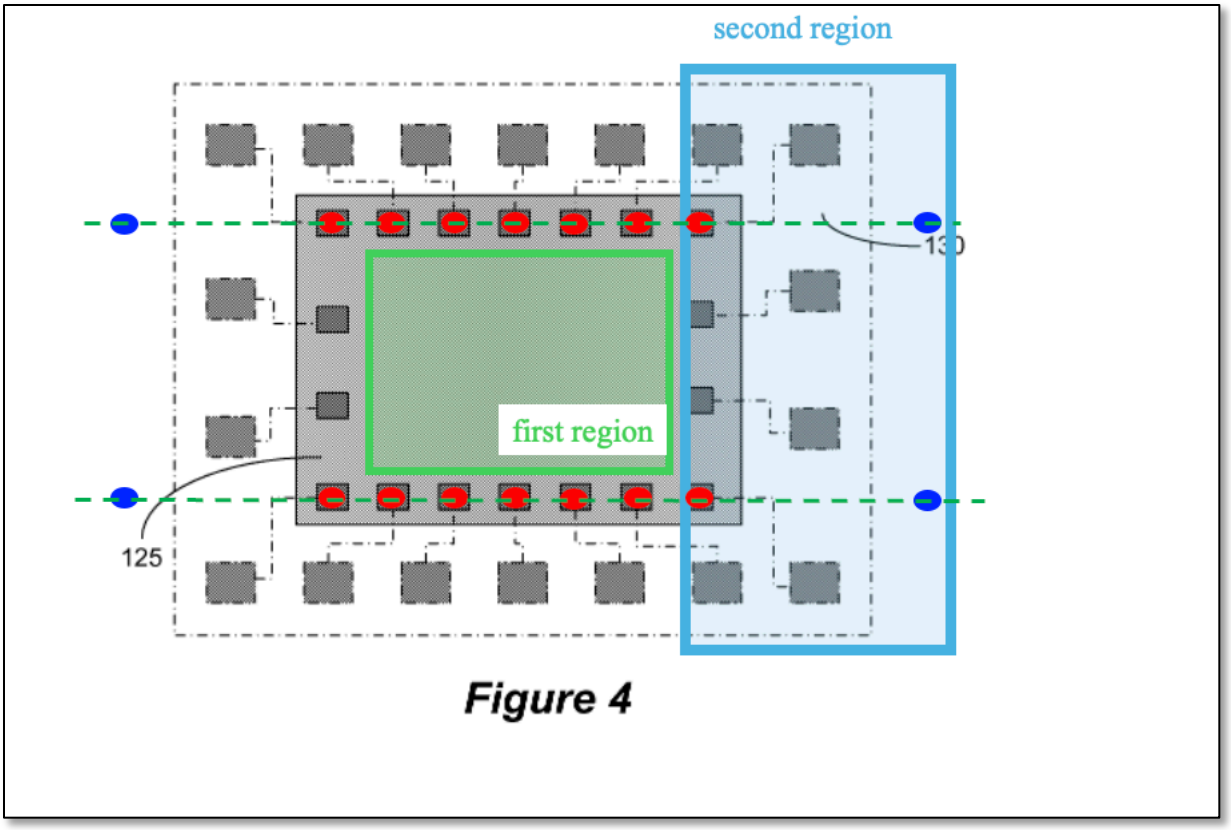


Figure 4

EX1004, FIG. 4; *EX1003*, ¶263.

a) Lin-863's Teachings

Additionally or alternatively to Sundaram, Lin-863 teaches a fan-out wafer level chip scale package 262 having a substrate 226 (*solid layer*) on which "conductive TMV[s] [through-mold vias] 225" and "semiconductor die 124" are disposed. *EX1007*, 12:33-42, 14:45-46, FIGS. 9a-9b. Shown below, package 262 includes a *first region* and *a second region* similar to the '763 Patent's regions identified in FIG. 6l. *EX1002*, 272. Lin-863's *first region* (green) is surrounded by the *second region* (blue), which is the region on substrate 226 where conductive

TMVs 225 are located. *EX1003*, ¶264. Lin-863's *second region is a rectangle region surrounding said first region*:

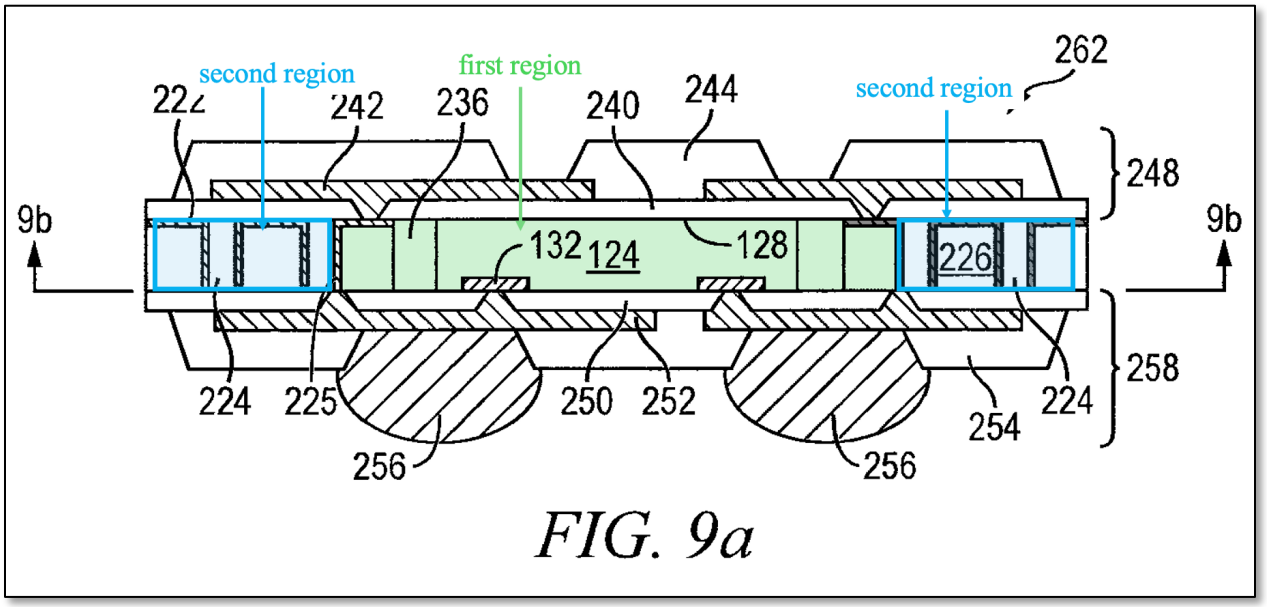


FIG. 9a

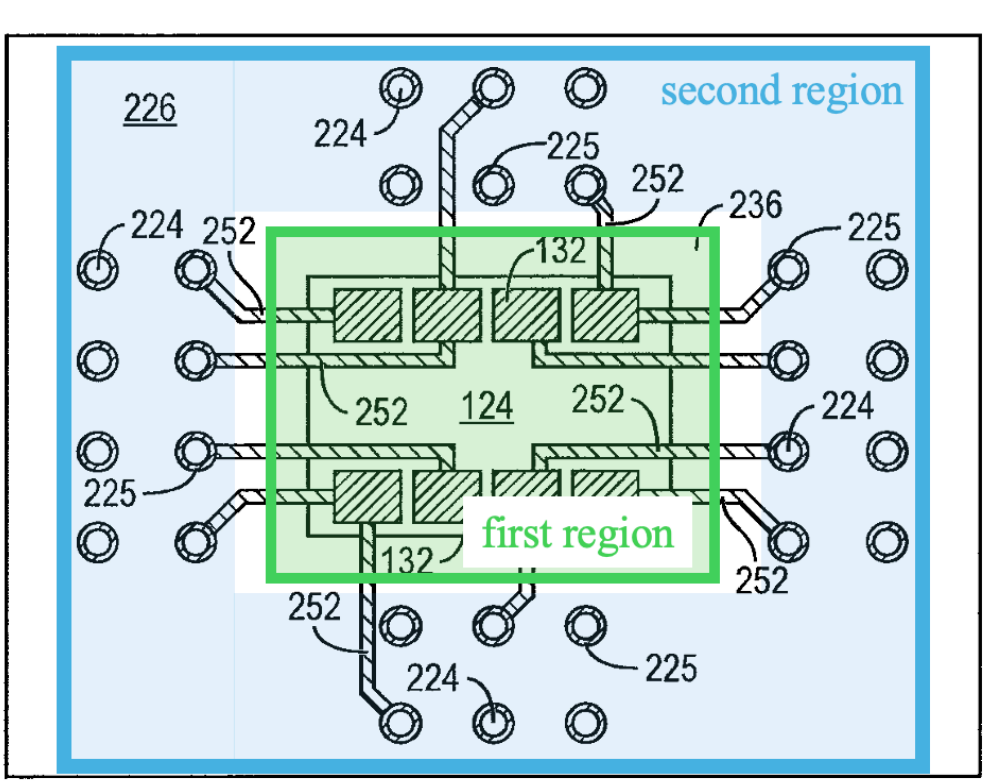

262
226
second region
224
225
252
236
224
252
225
132
252
124
252
224
225
first region
132
252
252
224
225

FIG. 9b

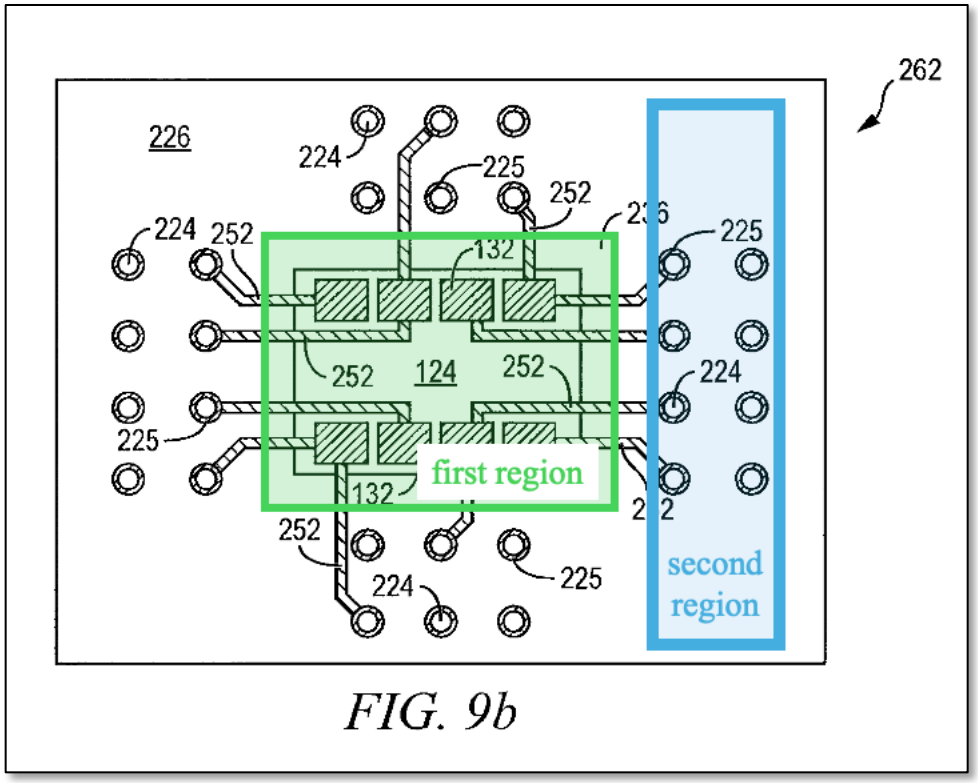


FIG. 9b

EX1007, FIGS. 9a-b; *EX1003*, ¶¶263-264.

b) MTC

Alternative to Petitioner's mapping that Sundaram teaches Claim 13 and if otherwise disputed, a POSITA would have found obvious and been motivated to configure Sundaram's *second region* to be *a rectangle region surrounding said first region* based on Lin-863's teachings. *EX1003*, ¶¶265-267. As discussed, Sundaram teaches or at least contemplates such a *rectangle region* in FIG. 4:

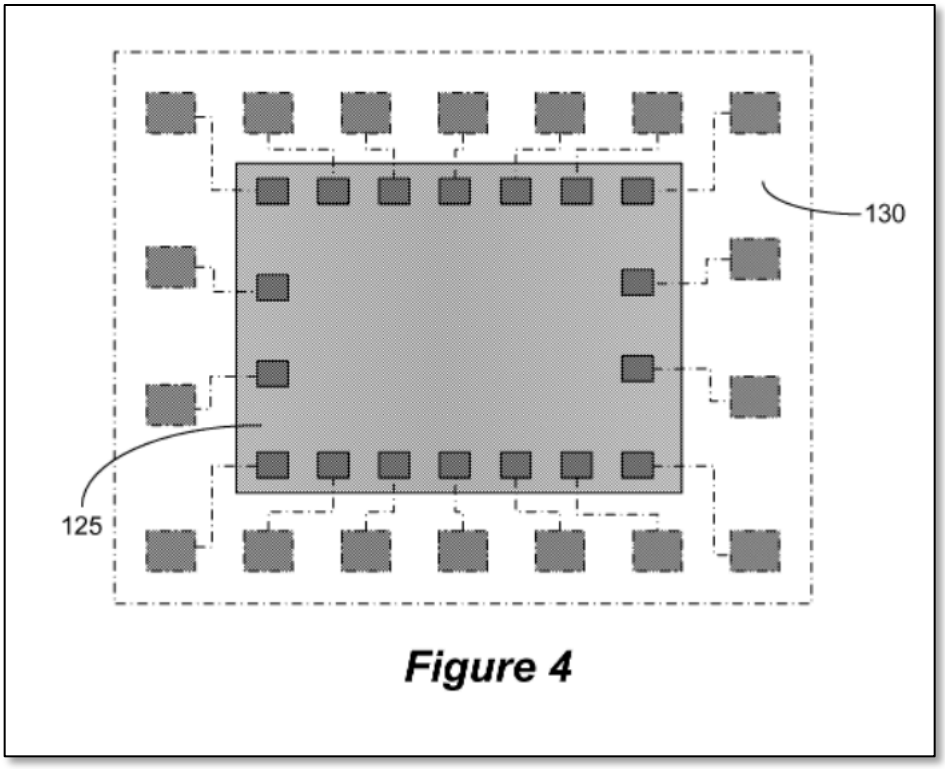


Figure 4

EX1004, FIG. 4; *see* Section VI.A. Thus, it would have been obvious to modify Sundaram per Lin-863 such that Sundaram's interposer 105 (*solid layer*) had a *rectangle region* for enabling the interconnection between the devices 125, 130. *EX1003*, ¶¶265-267. Such an arrangement also permits the addition of passive components directly under the chip or, it allows for placement of heat sink material directly under the chip, improved thermal dissipation, and shorter interconnect paths by embedding the chip within the interposer/package. *Id.*

Further, a POSITA would have been motivated and found obvious to modify Sundaram's chip package to have through vias 110 in a rectangular second region surrounding a first region to match the standard rectangular geometry of a chip.

EX1003, ¶267. Specifically, chips are cut into a rectangular shape as non-rectangular shapes do not maximize the use of valuable wafer area where circuitry can be fabricated. *Id.* Thus, it is practical and common practice to surround a chip with posts/vias arranged in a geometry that mirrors the chip's shape, e.g., to mirror the rectangular shape of device 125. *Id.* This arrangement also permits adding passive components directly under the chip or, it allows for placement of heat sink material directly under the chip, improved thermal dissipation, and shorter interconnect paths by embedding the chip within the interposer/package. *EX1003*, ¶266.

The combination is the application of known technique (interconnects in a rectangular arrangement in a chip package) to a known device (Sundaram's chip package) to yield the predictable results of Sundaram's package having through vias 110 in a rectangular region. *EX1003*, ¶268. There would have been a REOS because Lin-863's fan-out package with a *rectangle region* represents a well-known package geometry. *EX1003*, ¶268.

B. Claim 15

See Section VI.A. Sundaram's FIG. 4 teaches *no any copper plug in said first region*[7]:

[7] Petitioners interpret the claimed *no any copper plug* to be "no copper plug."

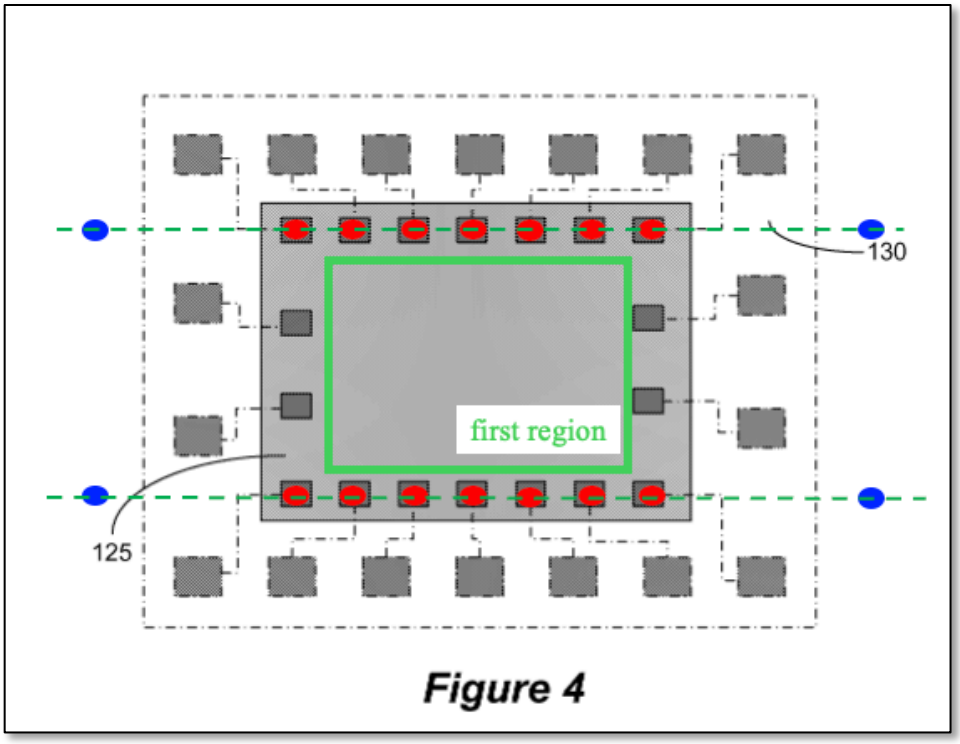


Figure 4

EX1004, FIG. 4; *EX1003*, ¶¶269-270. Because Sundaram teaches that die-to-die vias connecting pads are at the periphery (as opposed to pads in the middle of the dies) and that the die-to-PWB vias are located outside the peripheral area of the smaller device, a POSITA would have understood Sundaram as teaching the *first region* as having no copper plugs. *EX1003*, ¶¶269-270.

a) Lin-863's Teachings

Additionally or alternatively to Sundaram's teachings, Lin-863's *first region* has no *copper…plug[s]* as shown:

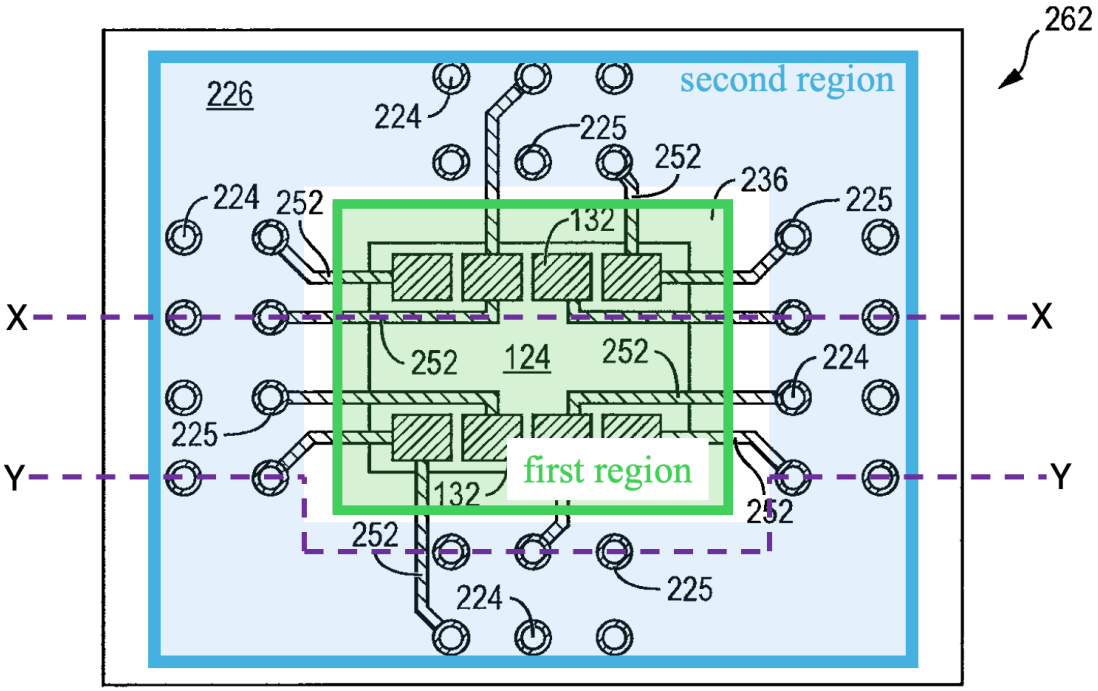


FIG. 9b

EX1007, FIG. 9b; *EX1003*, ¶271.

No copper plug[s] in the *first region* is also depicted in the cross-sectional FIG. 9a, where TMVs 225 are on the sides of the *first region*. *EX1028*, 14:45-46. The 9b-9b cross-section line in FIG. 9a corresponds to the X-X line annotated in 9b, while a POSITA would understand Sundaram's FIG. 3 section to be taken along a line analogous to Y-Y. *Compare EX1007*, FIG. 9b *with EX1004*, FIG. 4; *EX1003*, ¶¶272-273.

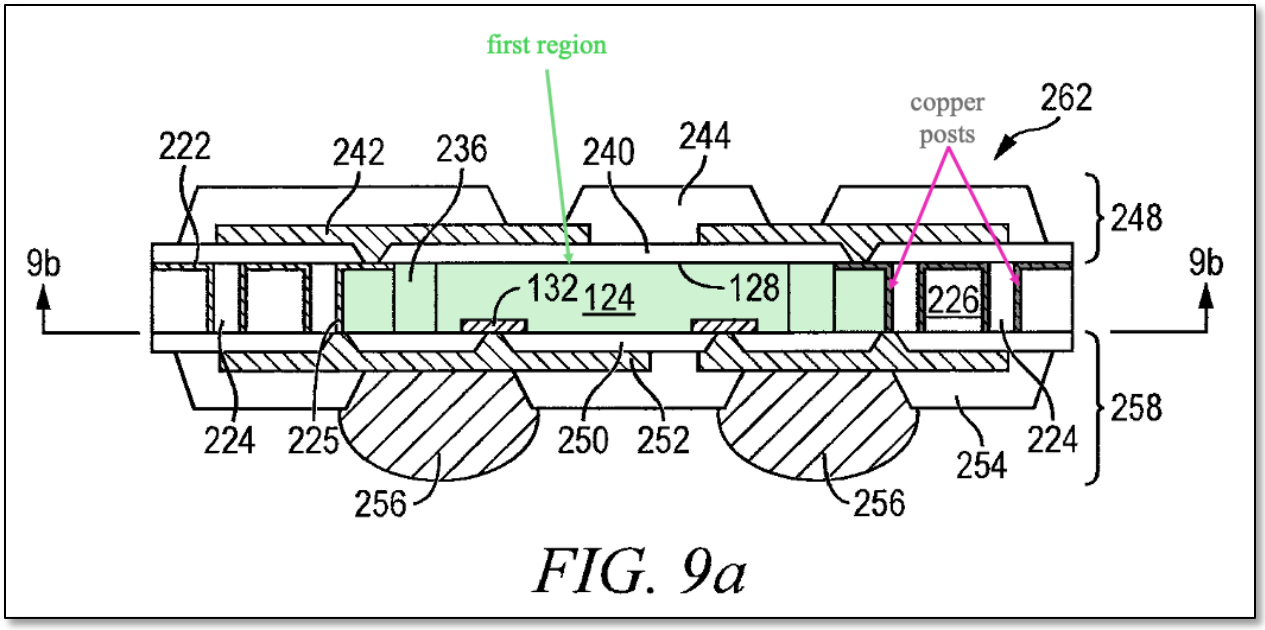


FIG. 9a

EX1007, FIG. 9a.

b) MTC

A POSITA would have found obvious and been motivated to modify Sundaram's *first region* per Lin-863's teachings to accommodate space for an additional semiconductor chip to be included in Sundaram's package. *EX1003*, ¶274. A POSITA would have appreciated the additional functionality that another chip would provide and recognized that including an additional chip in interposer 105 would have been an efficient use of space while providing short interconnect paths for the embedded chip. *Id.*

The combination is the application of known technique (no plugs/interconnects in a central region) to a known device (Sundaram's chip package) to yield the predictable results of Sundaram's package having a post-free

region where a die is positioned. *EX1003*, ¶275. There would have been a REOS for because methods of controlling plug placement in chip packages were well known. *Id*.

VII. GROUNDS 1C-1D: CLAIM 22 IS OBVIOUS OVER SUNDARAM, LIN-191, AND LIN-691 OR SHENOY

A. Ground 1C: Lin-691 Teaches Claim 22

Lin-691 teaches "through-substrate via[s]" (TSVs) formed by forming a "diffusion barrier layer," a "thin seed layer…formed on the diffusion barrier layer," and a "metallic material" on the thin seed layer. *EX1008*, [0005], [0019-0021]. The thin seed layer is "silver," and the "metallic material" is "copper." *EX1008*, [0019], [0021]. Lin-691's TSV 60 is below:

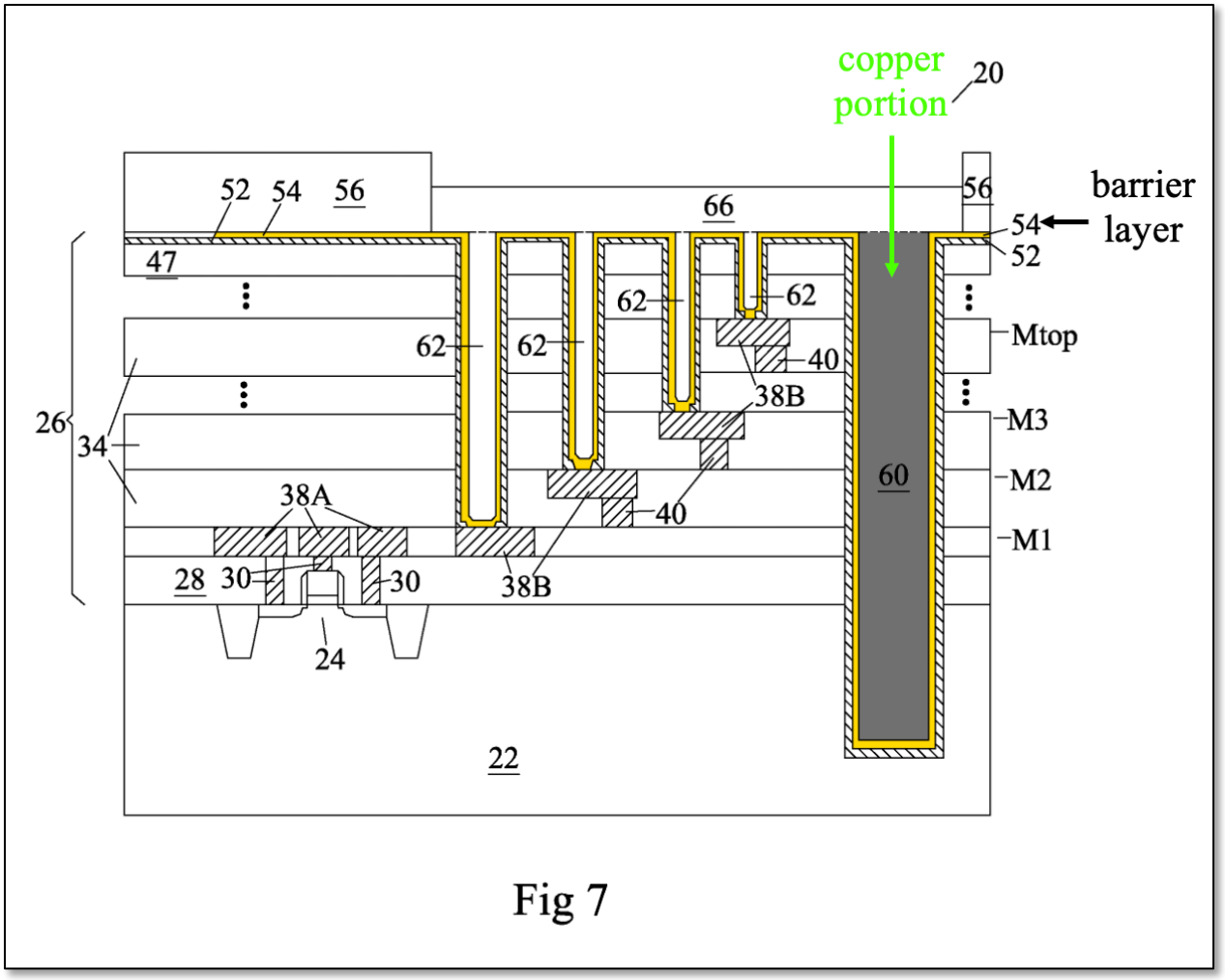


Fig 7

EX1008, FIG. 7. The silver seed layer is "not shown" in FIG. 7; however, because it is "formed on diffusion barrier layer," the layer covers a side wall of the copper portion and is, therefore, a *first metal layer [that] is a silver containing layer*. *EX1003*, ¶¶276-277.

As discussed in Claim 18(b)(i), Sundaram's through vias 110 comprise a *first metal layer* that is a Cu seed layer. *See* Claim 18(b)(i). A POSITA would have found obvious and been motivated to modify Sundaram's *metal conductor* such that the Cu seed layer was instead silver, per Lin-691. *EX1003*, ¶278. A POSITA would have

appreciated the benefits provided by silver's improved current distribution during plating. *Id.* A silver seed layer allows a more uniform distribution of plating current than a Cu seeding layer because it has higher conductivity than Cu, and this results in a more uniform plated layer. *Id*. Silver also adheres more strongly to polymers and glass than Cu, resulting in better overall mechanical properties for the plated layer. *Id*

The modification is the application of a known technique (Lin-691's silver seed layer) to a known device (Sundaram's through via) ready for improvements to yield the predictable results of through via 110 being formed with a silver seed layer. *EX1003*, ¶279. Additionally, or alternatively, the modification is the simple substitution of Lin-691's silver seed layer for Sundaram's copper seed layer to obtain predictable results. *Id*. There would have been a REOS because the use of a silver seed layer, including in conjunction with an inner copper layer was well known before the '763 Patent and involved routine manufacturing processes. *Id*. Further, Lin-691's TSV is formed on a "[p]assivation layer 47 [that] may be…un-doped silicate glass," i.e., a similar material to Sundaram's interposer 105 where through via 110 is formed.

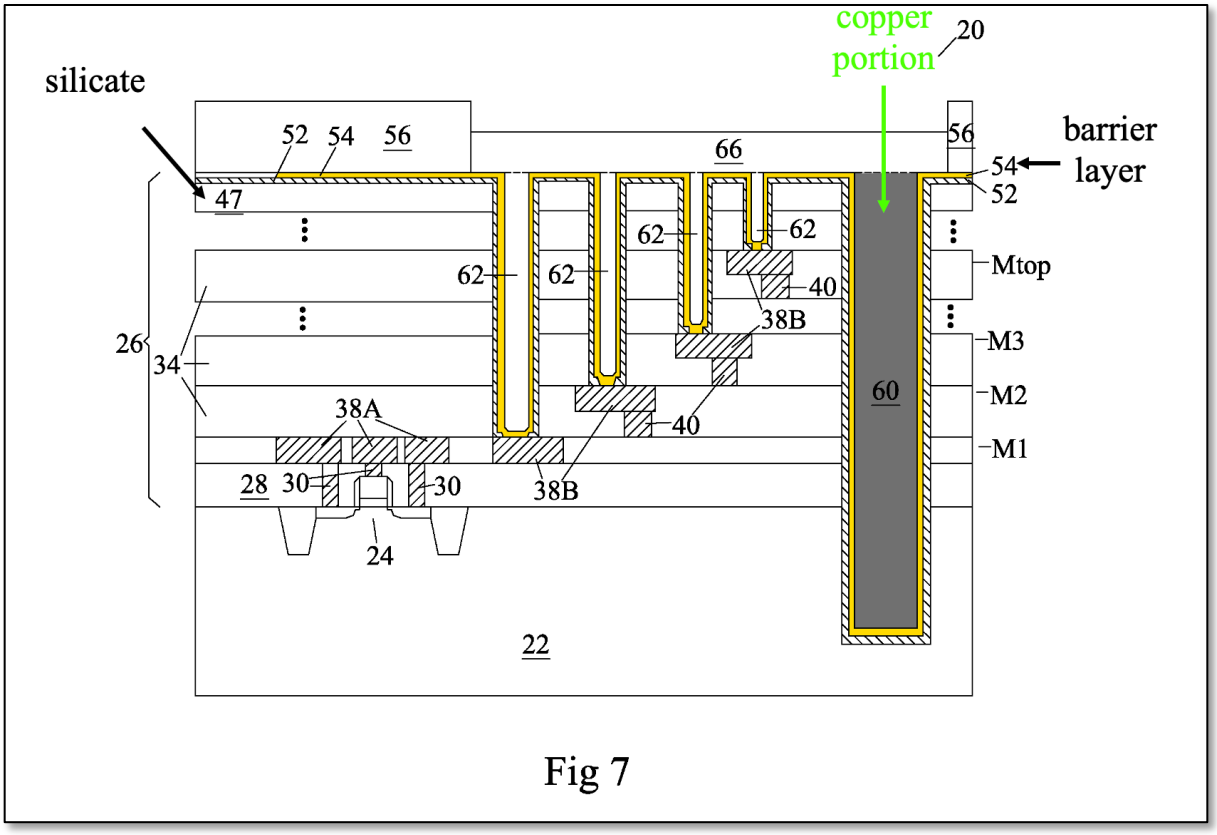
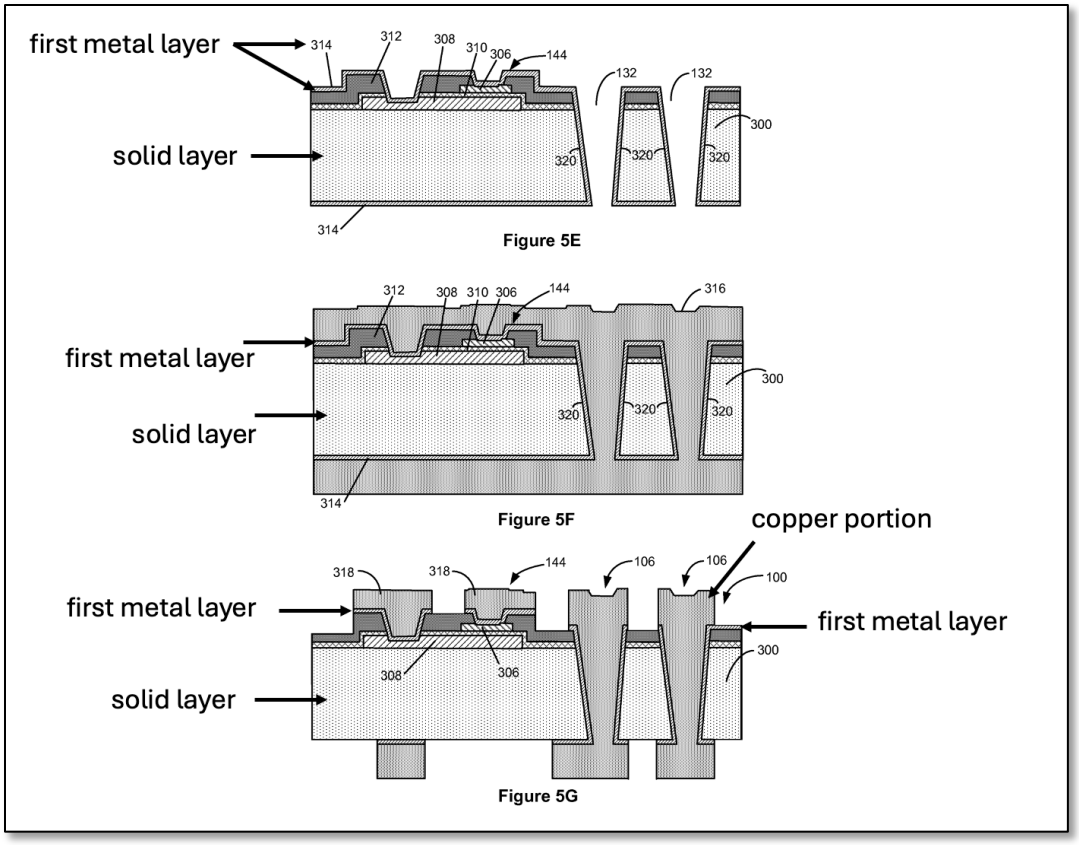


Fig 7

EX1008, FIG. 7, [0015]; EX1003, ¶277.

B. Ground 1D: Shenoy Teaches Claim 22

Shenoy teaches "a glass substrate" with "through-glass via holes," which has "exposed surfaces of the metal layers 306 and 308, and the passivation layer 312 [] conformally coated with a seed layer 314" that includes "Ag." *EX1011*, [0053-0055]. A "plated metal 316 fills the through-glass via holes 132…and covers the conformal seed layer 314" and "can include Cu[.]" *Id.*



EX1011, FIGS. 5E-5G; *EX1003*, ¶280.

A POSITA would have been motivated, found obvious, and had a REOS for the reasons discussed above. *See* Section VII.A; *EX1003*, ¶281. Because Shenoy, like Sundaram teaches through glass vias, there would have been a REOS. *EX1003*, ¶281.

VIII. GROUND 2A: CLAIMS 1-5, 7-12, 14-15, 17 ARE OBVIOUS OVER YU AND LIN-191

A. Claim 1

1. 1(Pre)

Yu teaches a *chip package* 202 that "compris[es] a first die encased in [a] molding compound, a second die on a back side of the package, and a third die on a

front side of the package….The package 202 can be the packaged formed in FIG. 17[.]" *EX1010*, 8:7-13. The semiconductor dies are "a logic circuitry die, a memory die, or any other die." *EX1010*, 2:50-51.

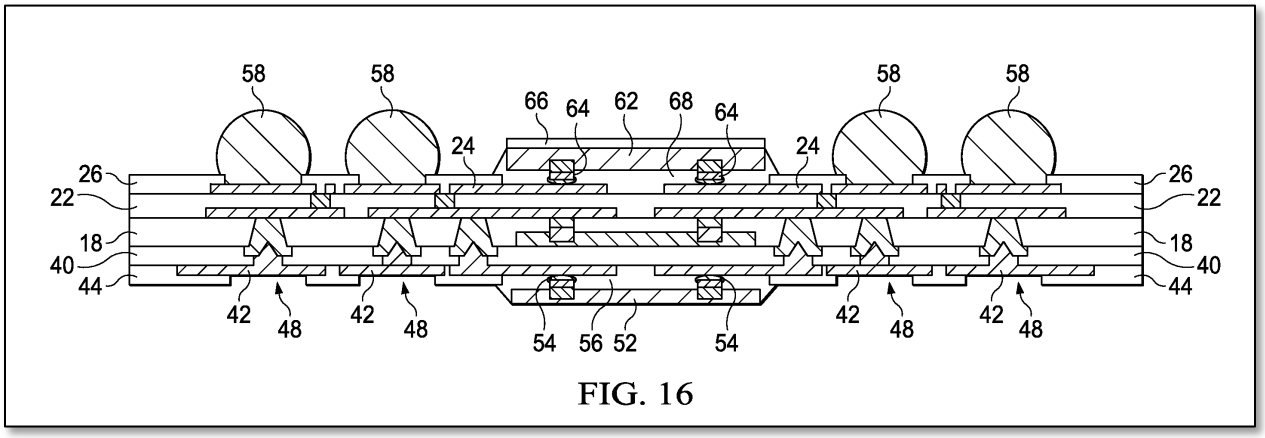


FIG. 16

EX1010, FIG. 16; *EX1003*, ¶282.

2. 1(a)

Package 202 includes "molding compound 18 [that] can be [] epoxy, polyimide, silicone rubber, the like, or a combination thereof," i.e., *a solid layer*. *EX1010,* 2:61-64. Molding compound 18 has *a first surface opposite to a second surface*:

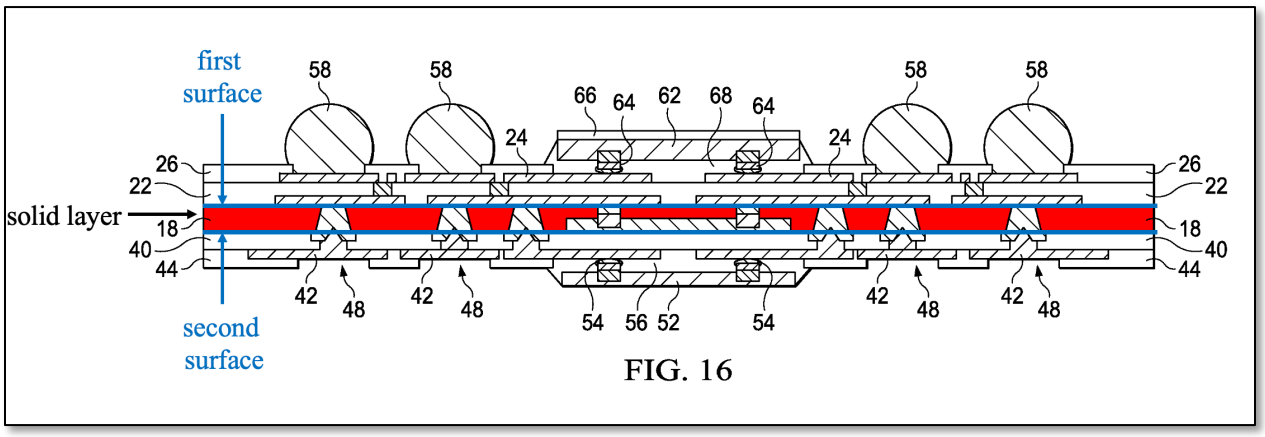


FIG. 16

EX1010, FIG. 16; *EX1003*, ¶¶283-284.

3. 1(a)(i)

Yu's *first surface is substantially parallel to said second surface*:

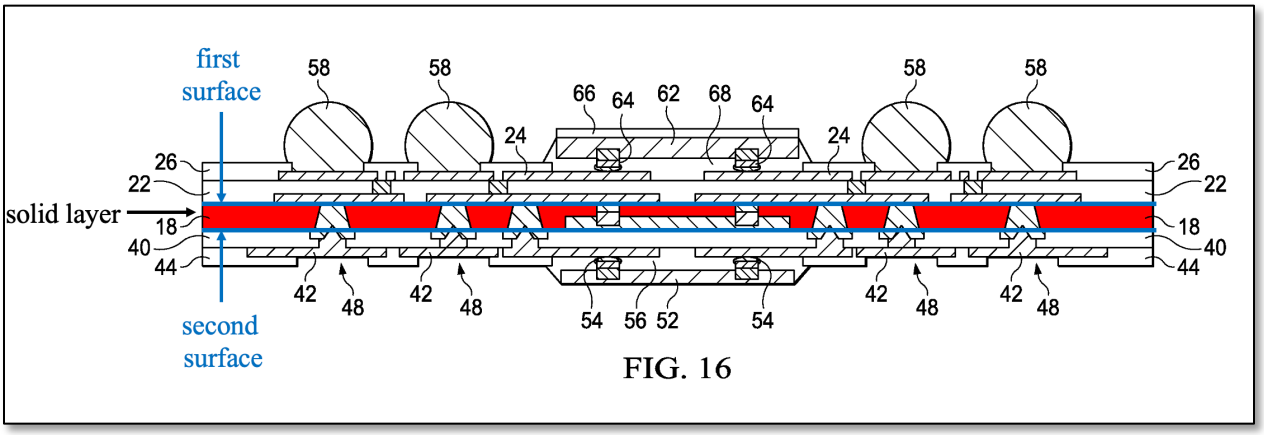


FIG. 16

EX1010, FIG. 16; *EX1003*, ¶285.

4. 1(a)(ii)

Molding compound 18 comprises "epoxy, polyimide, silicone rubber, the like, or a combination thereof," such that silicone rubber alone or silicone rubber in combination with epoxy and/or polyimide teaches *a compound of silicon and oxygen*. *EX1010*, 2:61-65; *EX1003*, ¶286.

5. 1(a)(iii)

a) Lin-191's Teachings

Lin-191 teaches or renders obvious Claim 1(a)(iii).

Lin-191's package includes an "encapsulating layer 85" formed "on…metal pillars or bumps 14" (analogous to Yu's through mold vias (TMVs), discussed further at Claim 1(b)). *EX1005*, [0109]. Layer 85 includes "a polymer layer" such

that layer 85 is a *solid layer*, similar to Yu's molding compound 18. *EX1005*, [0109]. Encapsulating layer 85 has a thickness "between about 20 and about 500 micrometers[.]" *EX1005*, [0109-0111]; *EX1003*, ¶287. Because Lin-191 teaches a range ("between about 20 and about 500 micrometers") that includes the narrower claimed range of *between 100 and 300 micrometers*, Lin-191 teaches or renders obvious Claim 1(a)(iii). *See* Section V.A.5 (supporting caselaw and discussion of '763 Patent not ascribing criticality to Claim 1(a)(iii)'s range); *EX1003*, ¶290.

Additionally or alternatively, layer 85 has a *thickness* equivalent to the combined thickness of layers 1 and bump 14 because layer 85 is "formed…on the metal layer 13 of the patterned metal layer 1," and "top surfaces 14a" of bumps 14 are "substantially coplanar…with a top surface 85a" of layer 85. *EX1005*, [0109-0110], FIG. 12. Lin-191 teaches bumps 14 are "between 20 and 110 micrometers"; layer 11 is "between 1 nanometer and 0.5 micrometers"; layer 12 is "between 10 nanometers and 0.8 micrometers"; and layer 13 is "between 3 and 10 micrometers." *EX1005*, [0121], [0050], [0060]. Thus, Lin-191 teaches layer 85 has a *thickness* between 23.011 micrometers and 121.3 micrometers, overlapping with and teaching or rendering obvious the claimed *thickness*. *EX1003*, ¶289.

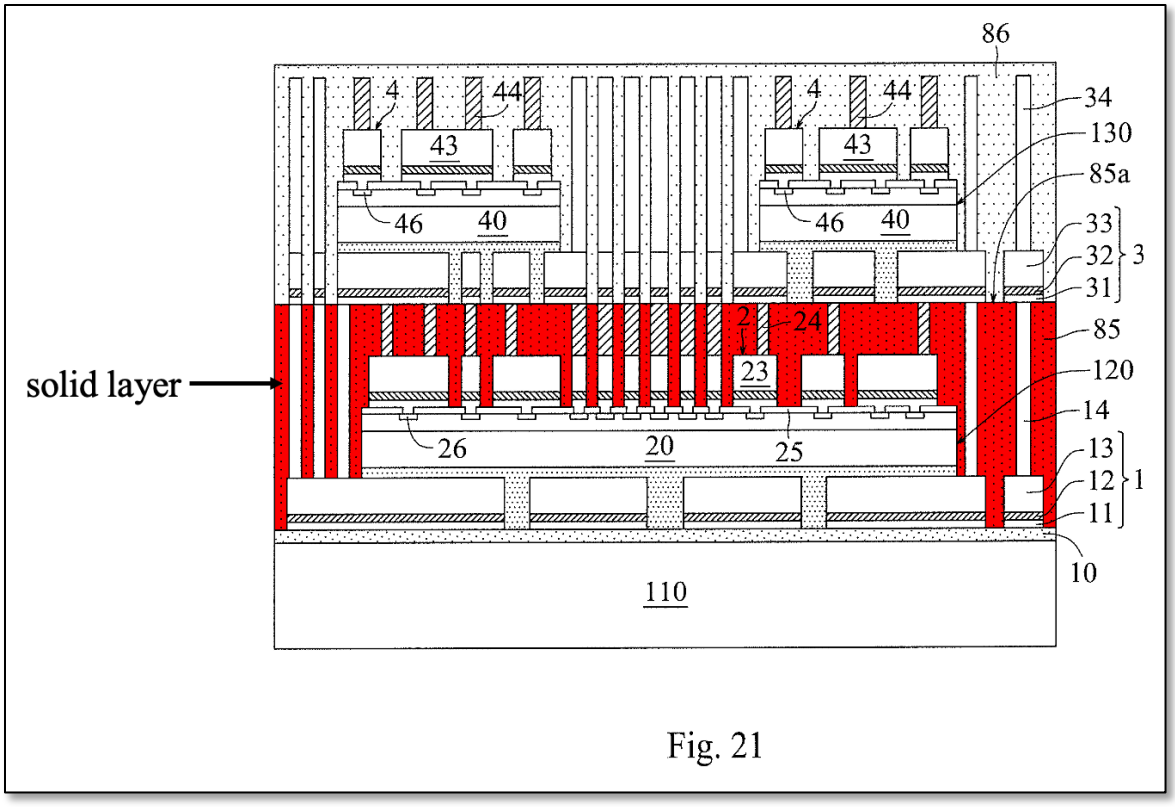


Fig. 21

EX1005, FIG. 21.

b) MTC

A POSITA would have been motivated and found obvious to apply Lin-191's thickness to Yu's molding compound 18. The modification would have provided the advantage of stress buffering, which would have been beneficial in Yu's package for protecting Yu's die 10 embedded in molding compound 18, as Lin-191's thickness was known to be appropriate for embedded chip architecture. *EX1003*, ¶¶291-292. Additionally, Lin-191's thickness would allow for the opportunity to incorporate shielding layers, which a POSITA would have found desirable. *EX1003*, ¶293.

The Yu-Lin-191 combination is the application of a known technique to a known device ready for improvement to yield predictable results. *EX1003*, ¶294. A POSITA would have had a REOS because Lin-191's thickness was a common thickness for molding/encapsulation layers before the '763 Patent. *Id*.

6. 1(a)(iv)

Molding compound 18 includes *a first region* and *a second region between said first region and an edge of said solid layer* as shown:

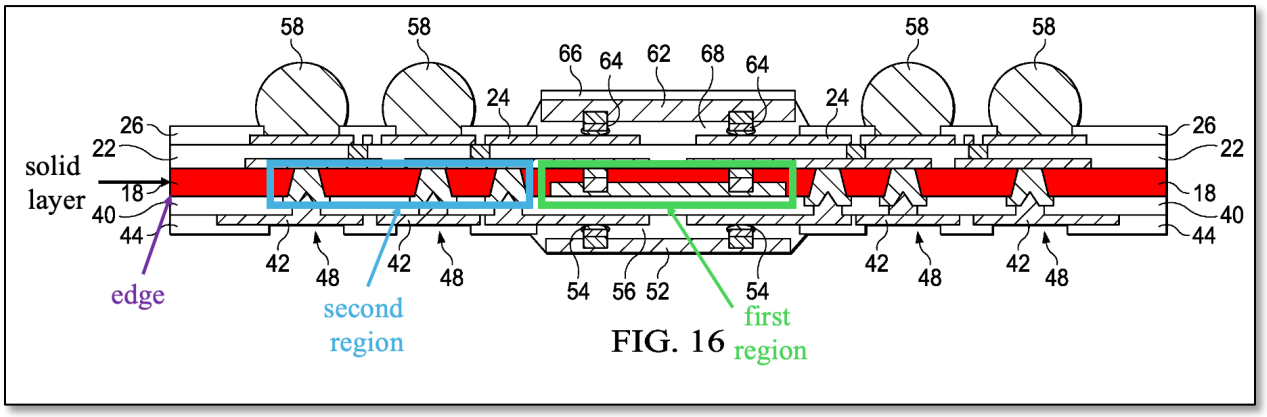


FIG. 16

EX1010, FIG. 16; *EX1003*, ¶295.

7. 1(b)

Yu teaches copper TMVs 38, which are *a plurality of copper plugs in a plurality of through vias*. Specifically, Yu teaches "TMV openings 36 are formed through the molding compound 18," and a "seed layer is deposited…into the TMV openings 36," followed by deposition of a "conductive material." *EX1010*, 3:56-4:6. Both the seed layer and the conductive material are "**copper**." *Id*. TMVs 38 are *in said second region*, as shown:

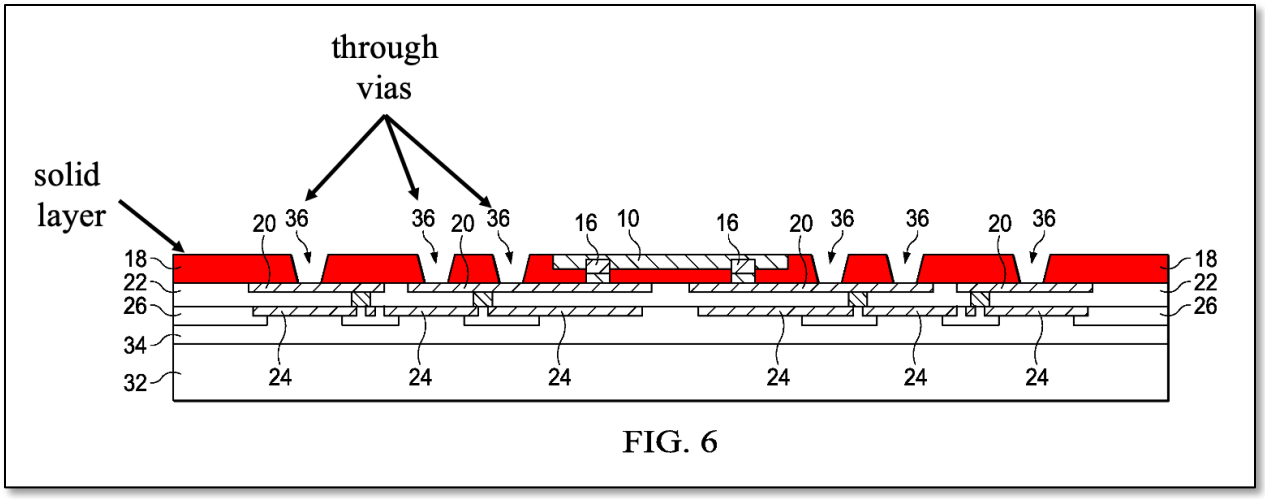


FIG. 6

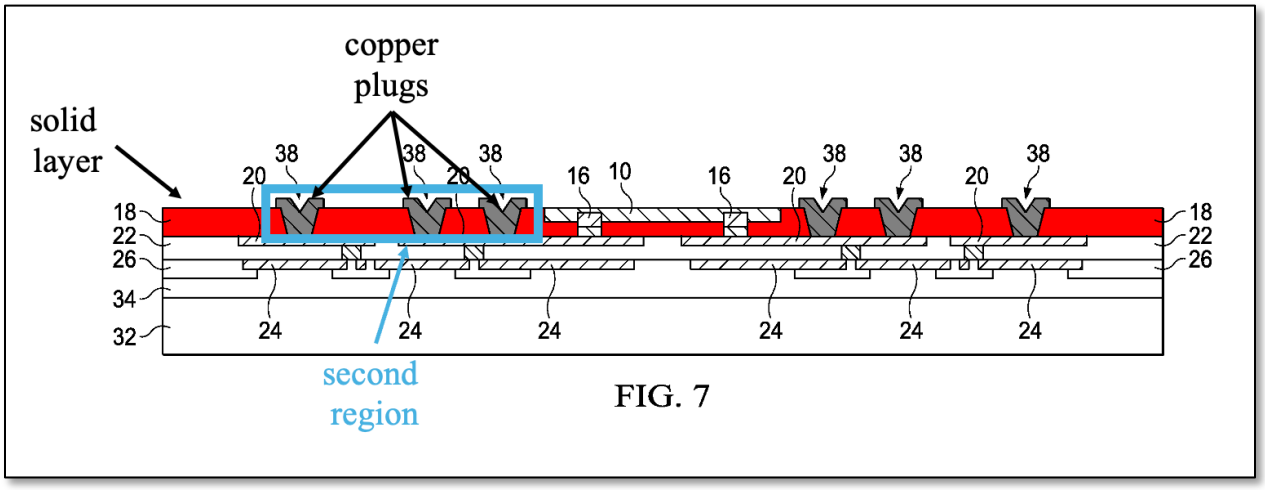
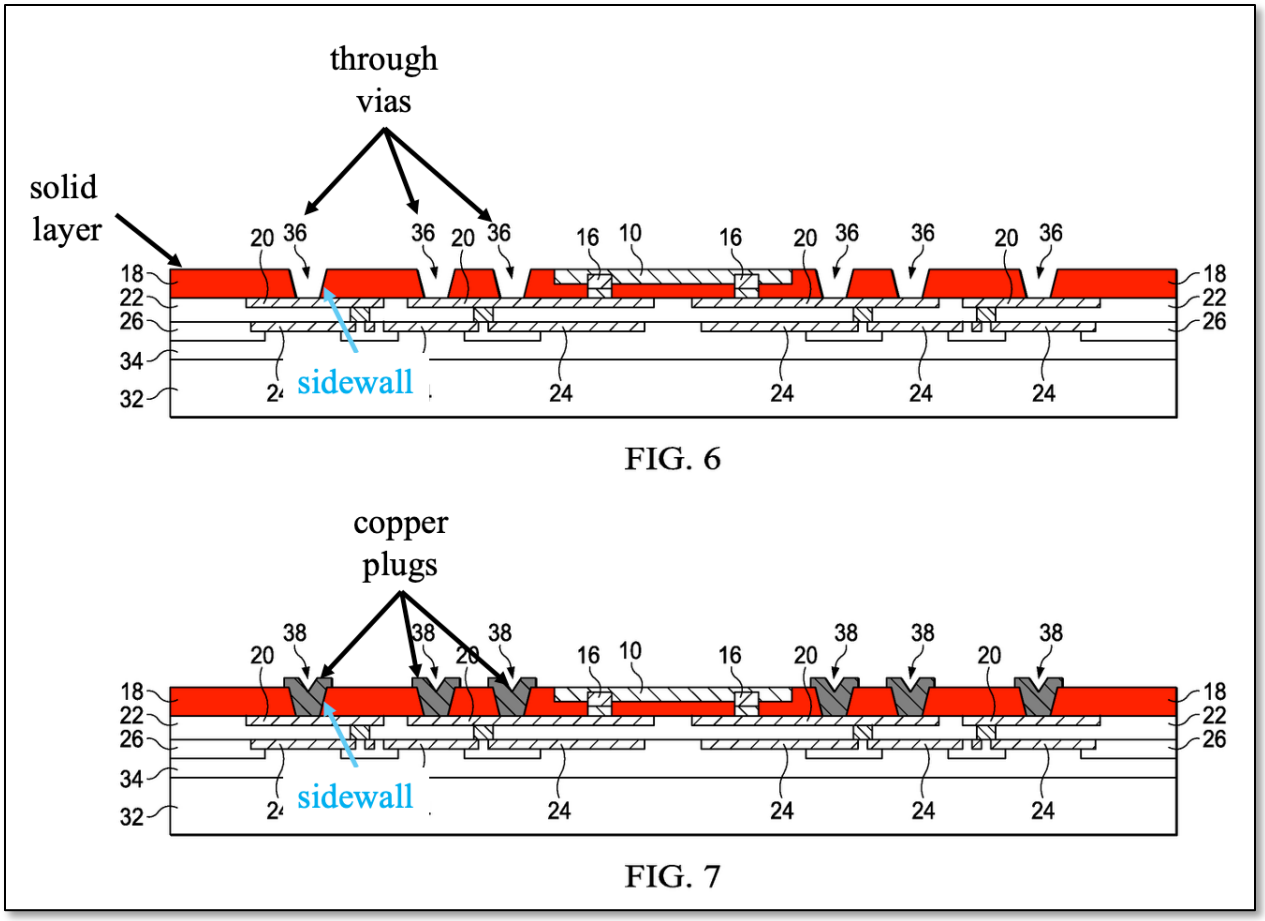


FIG. 7

EX1010, FIGS. 6-7; *EX1003*, ¶296.

8. 1(b)(i)

A copper seed layer of a TMV that is "deposited…into the TMV opening[] 36" is *a first copper layer contacting a sidewall of one of said plurality of through vias*. *EX1010*, 3:60-64.



EX1010, FIG. 6; *EX1003*, ¶¶297-298.

9. 1(b)(ii)

The annotated FIG. 6l submitted by PO during original examination is below, illustrating the claimed *width*, *shortest distance*, and *pitch*. The claimed *regions* are not described in the '763 Patent's written description. Applicant relied solely on FIG. 6l as support.

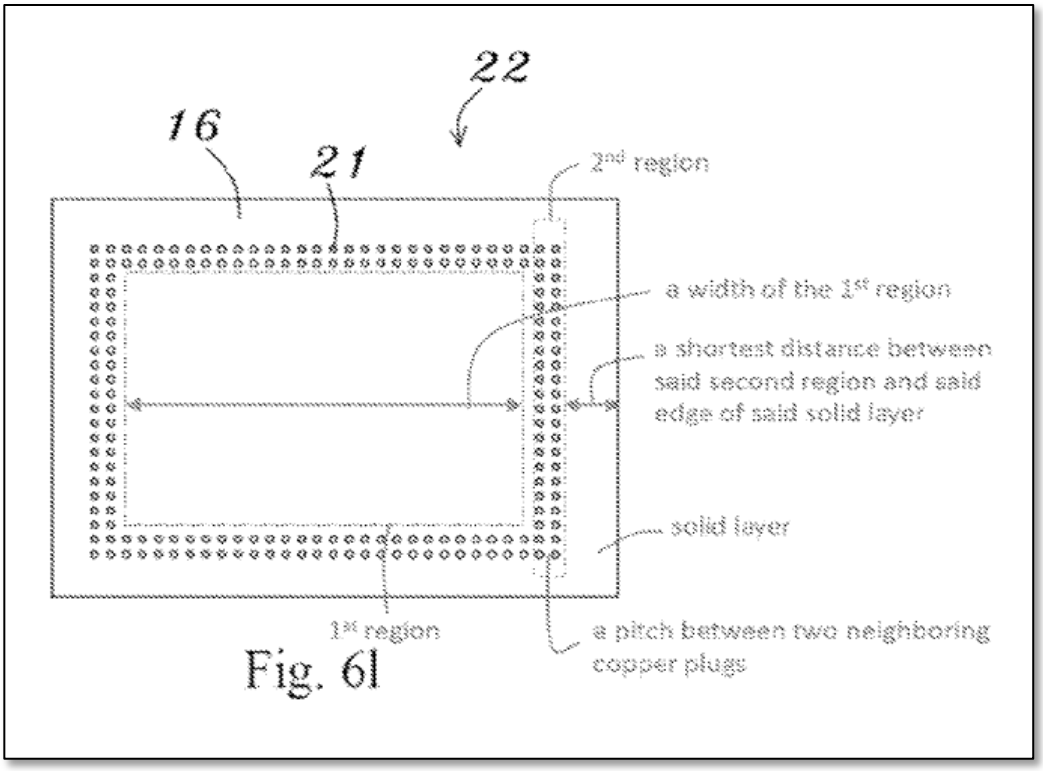


Fig. 6I

EX1002, 272; *EX1003*, ¶300.

Shown in FIG. 16, below, Yu's *first region has a width in a direction* (denoted D1) *greater than a shortest distance between said sidewall of one of said plurality of through vias and said edge…in said direction* (denoted D2), and *greater than a pitch between two neighboring copper plugs* (denoted D3).

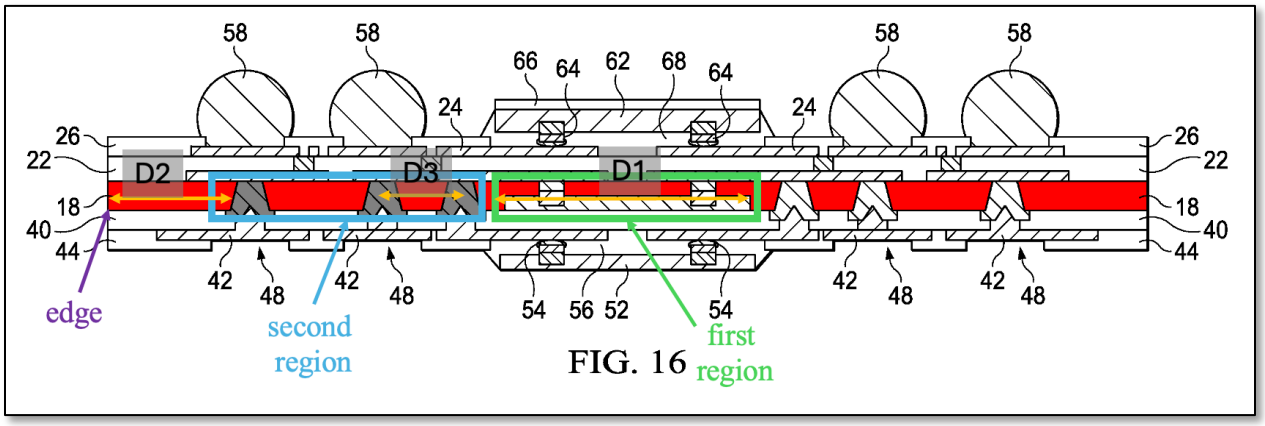


FIG. 16

EX1010, FIG. 16; *EX1003*, ¶299; *see* Section V.A.9 (supporting caselaw).

10. 1(c)

Yu teaches a "front side interlayer dielectric (ILD) and redistribution layer (RDL) structure" that are collectively *a first interconnection scheme over said first surface* because the structure "electrically couple[s]" components in Yu's *package*. *EX1010*, 3:4-15. The ILD/RDL structure includes a "first front side metallization layer 20," a "first ILD layer 22," and "[s]ubsequent metallization layers and ILD layers" including "a second metallization layer 24 and a second ILD layer 26." *EX1010*, 3:16-32, FIGS. 4, 7 (describing and showing the formation of layer 20).

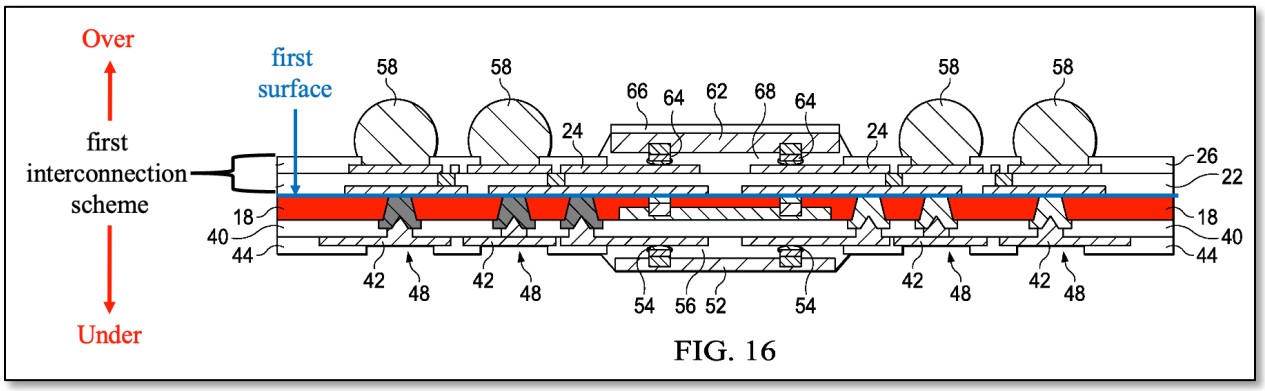


FIG. 16

EX1010, FIG. 16; *EX1003*, ¶301; *see* Section V.A.10, footnote 3.

11. 1(c)(i)

Metallization layer 20 comprises "copper," and a portion of layer 20 is, therefore, *a first metal interconnect*. *EX1010*, 3:11-19. For the same reason, a second portion of layer 20 is a *second metal interconnect*. Both portions of layer 20 are *over said first surface* as shown below. ILD layer 22, which comprises "a polyimide," is

a first polymer layer and is *over* metallization layer 20. *EX1010*, 3:20-23. The *first polymer layer* at least includes ILD layer 22 but may also include ILD layer 26 (*see* Claim 14).

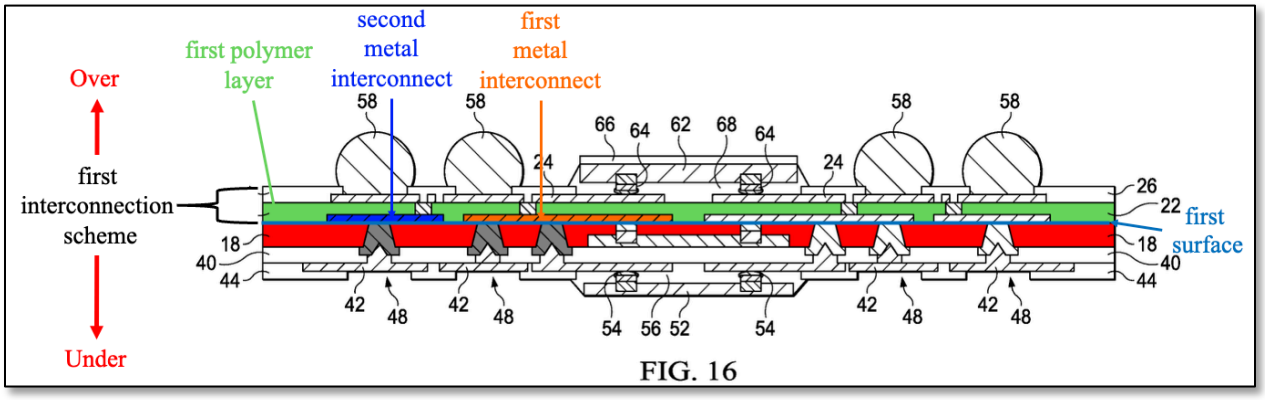


FIG. 16

EX1010, FIG. 16, 3:21-23; *EX1003*, ¶¶302-304.

Alternatively, ILD layer 26, which also comprises "polyimide," is *a first polymer layer over said first and second metal interconnects*. *EX1010*, 3:20-32.

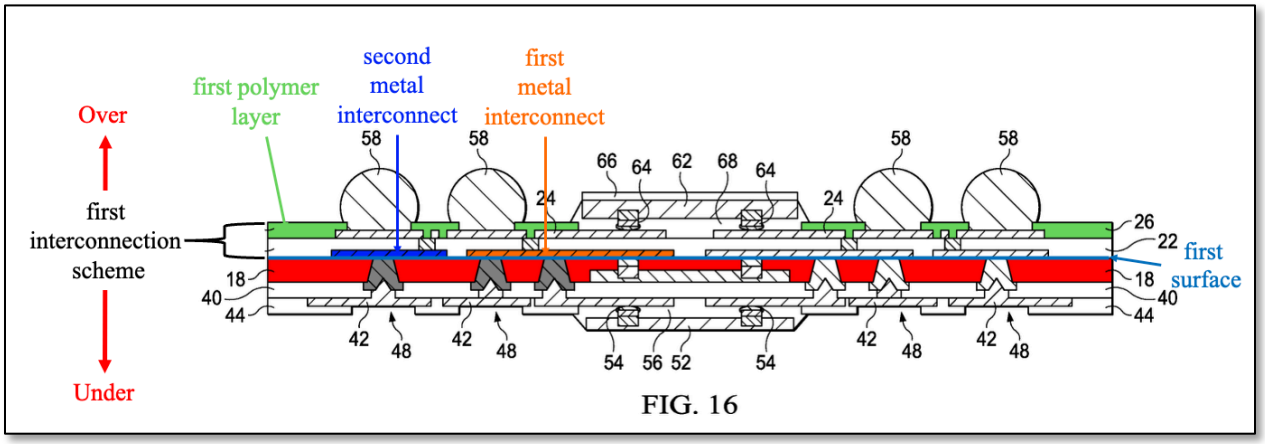


FIG. 16

EX1010, FIG. 16; *EX1003*, ¶305.

12. 1(c)(ii)

Yu's *first metal interconnect is connected to a first copper plug* as "TMV openings 36 are formed through the molding compound 18 to the first front side metallization layer 20," followed by formation of TMVs 38 via electroplating. *EX1010*, 3:56-4:6. For the same reasons, the *second metal interconnect is connected to a second copper plug*.

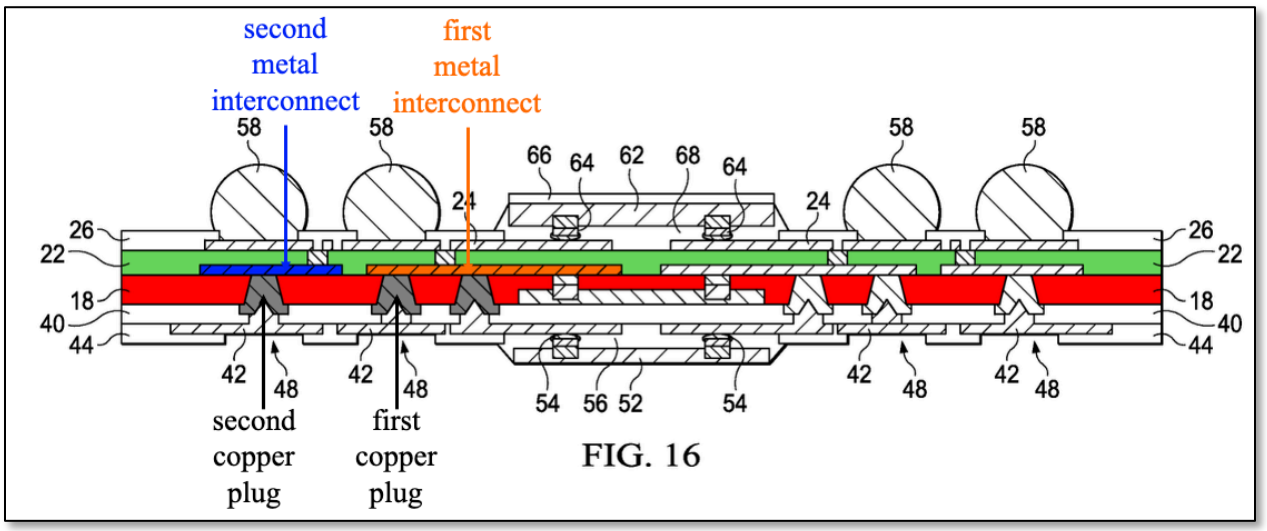


FIG. 16

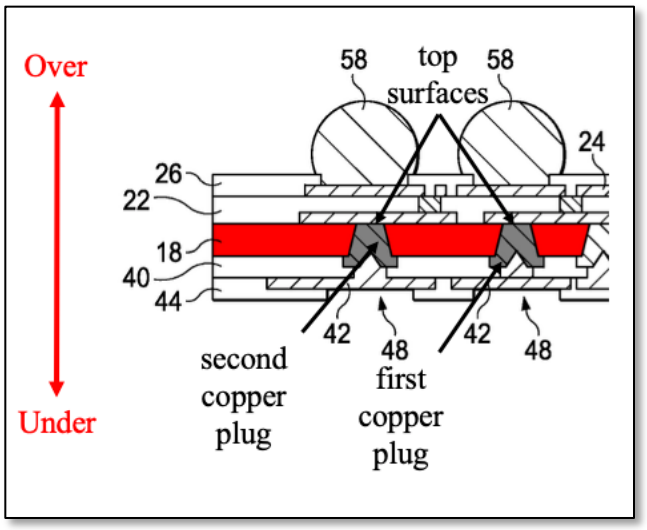
EX1010, FIG. 16; *EX1003*, ¶306.

13. 1(c)(iii)

Yu teaches metallization layer 20 includes a "seed layer, such as **copper**…deposited on the molding compound 18," and a "[c]onductive material…such as **copper**…is deposited on the seed layer." *EX1010*, 3:5-19. Thus, metallization layer 20's copper "seed layer" is *a first metal layer*, and the copper "conductive material" deposited on the seed layer is *a second copper layer over* the copper seed layer. *EX1003*, ¶307.

14. 1(c)(iv)

The *first* and *second copper plug[s]* comprise *top surface[s]* that *are substantially in the same horizontal plane*:



EX1010, FIG. 16; *EX1003*, ¶308.

15. 1(d)

Yu teaches "conductive connectors 58, such as ball grid array (BGA) balls," are formed "on the front side of the package in the openings 28" and "formed on [] bond pads." *EX1010*, 4:45-49. Connector 58 and its bond pad collectively form *a first metal bump*.

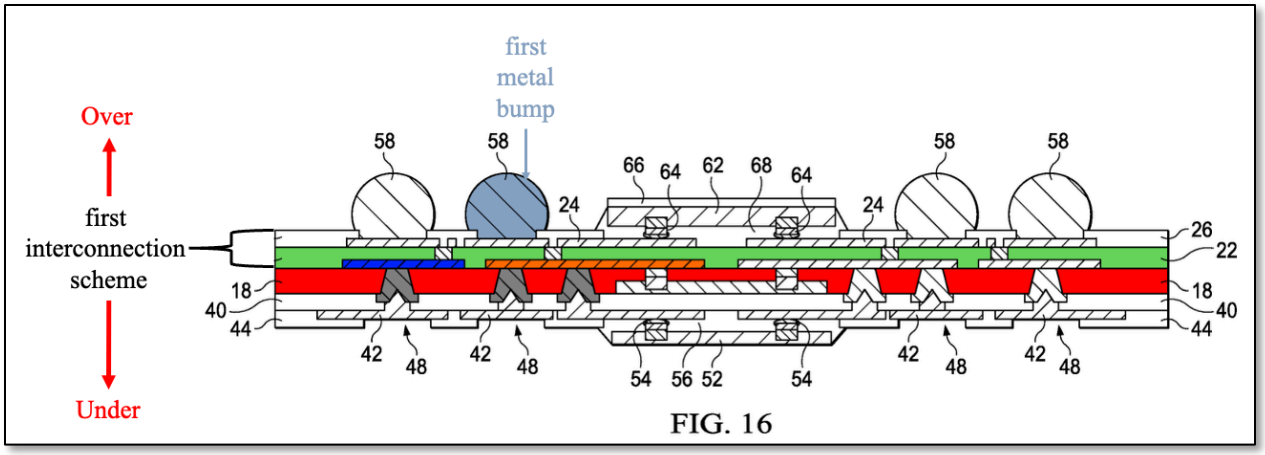


FIG. 16

EX1010, FIG. 16; *EX1003*, ¶¶309-310.

16. 1(d)(i)

Yu teaches "connector[] 58 may be formed on the bond pad[]" and "may be [] lead-free solder." *EX1010*, 4:47-50. A POSITA would have understood (A) the bond pad to be *metal* because bond pads were (and remain) ubiquitously *metal* for interconnecting solder balls in chip packages, and (B) lead-free solder to include *tin*. *EX1003*, ¶¶311-313. Thus, Yu teaches *a second metal layer* (the bond pad) *and a tin-containing layer* (lead-free solder) *over said second metal layer* because the solder connector 58 is on (*over*) the bond pad. *Id.*

a) Lin-191's Teachings and MTC

Additionally, or alternatively, Lin-191 teaches Claim 1(d)(i). *See* Section V.A.16. A POSITA would have been motivated, found obvious, and had a REOS in modifying Yu per Lin-191 for the reasons discussed for Sundaram-Lin-191. *Id.* The Yu-Lin-191 combination is application of known technique (Lin-191's solder bump

structure) to a known device (Yu's connector and pad) ready for improvement to yield predictable results. *EX1003*, ¶314.

17. 1(e)

Yu's package includes "die 52, such as a memory die," which is *a first semiconductor chip under said first interconnection scheme*. *EX1010*, 4:30-36.

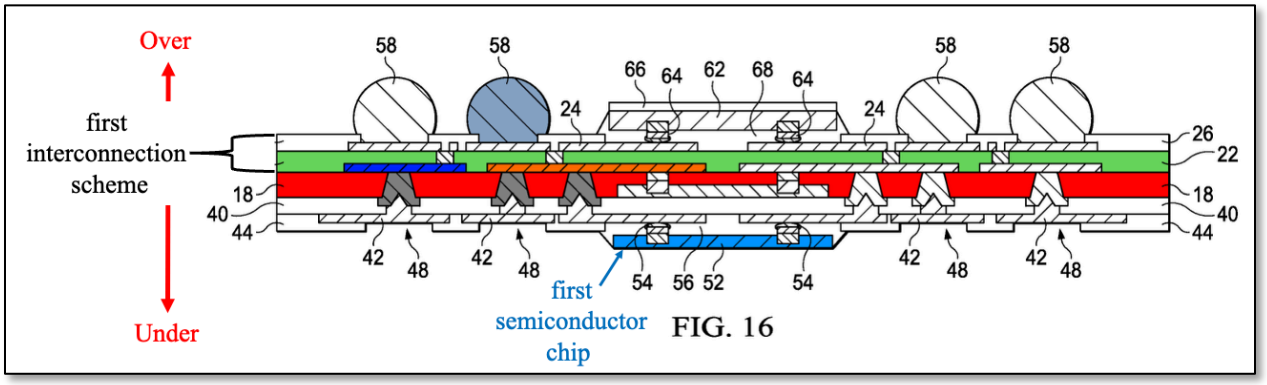
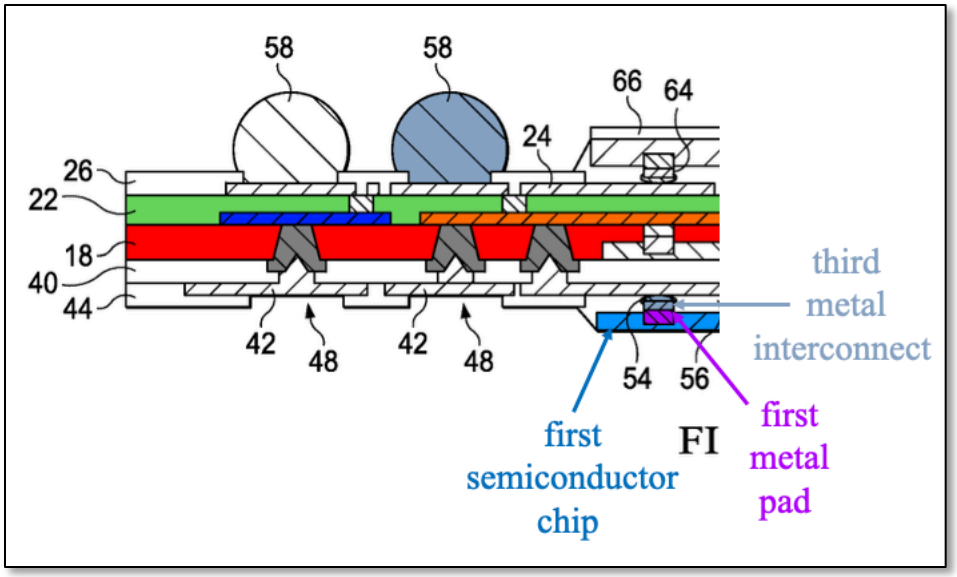


FIG. 16

EX1010, FIG. 16; *EX1003*, ¶315.

18. 1(e)(i)

Die 52 is "attached…to conductive features in the second back side metallization layer 42, such as by conductive connectors 54, like controlled collapse chip connection (C4) bumps." *EX1010*, 4:30-34. A connector 54 is *a third metal interconnect* because it connects die 52 "to conductive features" in layer 42. *Id*. Further, a POSITA would have understood die 52 includes die pads (unlabeled) such that an electrical connection is made between die 52 and other devices (e.g., die 62), thus teaching the *first metal pad of said first semiconductor chip*. *EX1003*, ¶¶316-319; *EX1129*, 1:9-26. As shown below, the connector 54 is *on* the die pad of die 52:



EX1010, FIG. 16 (excerpt).

a) Lin-191's "Metal Pad" Teachings and MTC

Additionally, or alternatively, to Yu, Lin-191 teaches *metal pads*. *See* Sections V.A.18.a-b. Lin-191 teaches an implementation detail of Yu's chip (a metal pad) such that there would have been a motivation and REOS. *EX1003,* ¶320. The combination is the application of known metal pad techniques to Yu's die 52 to yield the predictable result of die 52 having a *metal pad*. *EX1003*, ¶321.

19. 1(e)(ii)

Lin-191 teaches or renders obvious interconnects/bumps with layers/thickness as recited in Claim 1(e)(ii). *See* Section V.A.19 (including no criticality of the claimed *thickness*). A POSITA would have found obvious and been motivated to modify Yu's connector for the reasons discussed with respect to Sundaram, i.e., improved metallurgical bonding and increased resistance to fatigue

and stress-induced failure. *EX1003*, ¶¶322-323. Layered bumps, per Lin-191, were routinely manufactured using techniques contemplated by Yu, leading to a REOS. *Compare EX1005*, [0400] *with EX1010*, 3:11-14; *EX1003*, ¶¶323.

B. Claim 2

Yu teaches "chip resistors" and "chip capacitors," i.e., *passive component[s]*. *EX1010*, 1:41-45; *EX1003*, ¶324.

a) Lin-191's Teachings

Lin-191 discloses two embodiments relevant to Claim 2's mapping. In the FIG. 55 embodiment, Lin-191 teaches chip 140 "can be replaced by a passive component 67," where the passive component is "connected to the metal layer 53 of the patterned metal layer 5 **through** two solder joints 68." *EX1005*, [0340], FIG. 55. Lin-191's FIG. 55 embodiment thus teaches a *passive component*, namely passive component 67. *EX1003*, ¶325. The FIG. 55 embodiment's collective patterned metal layers 5 are *an interconnection scheme* because they include a "metal **interconnect** or trace…" *EX1005*, [0214]. As shown and otherwise expressly taught at [0340], passive component 67 is connected to the *interconnection scheme* (layer 5) *through a solder layer* (solder joint 68).

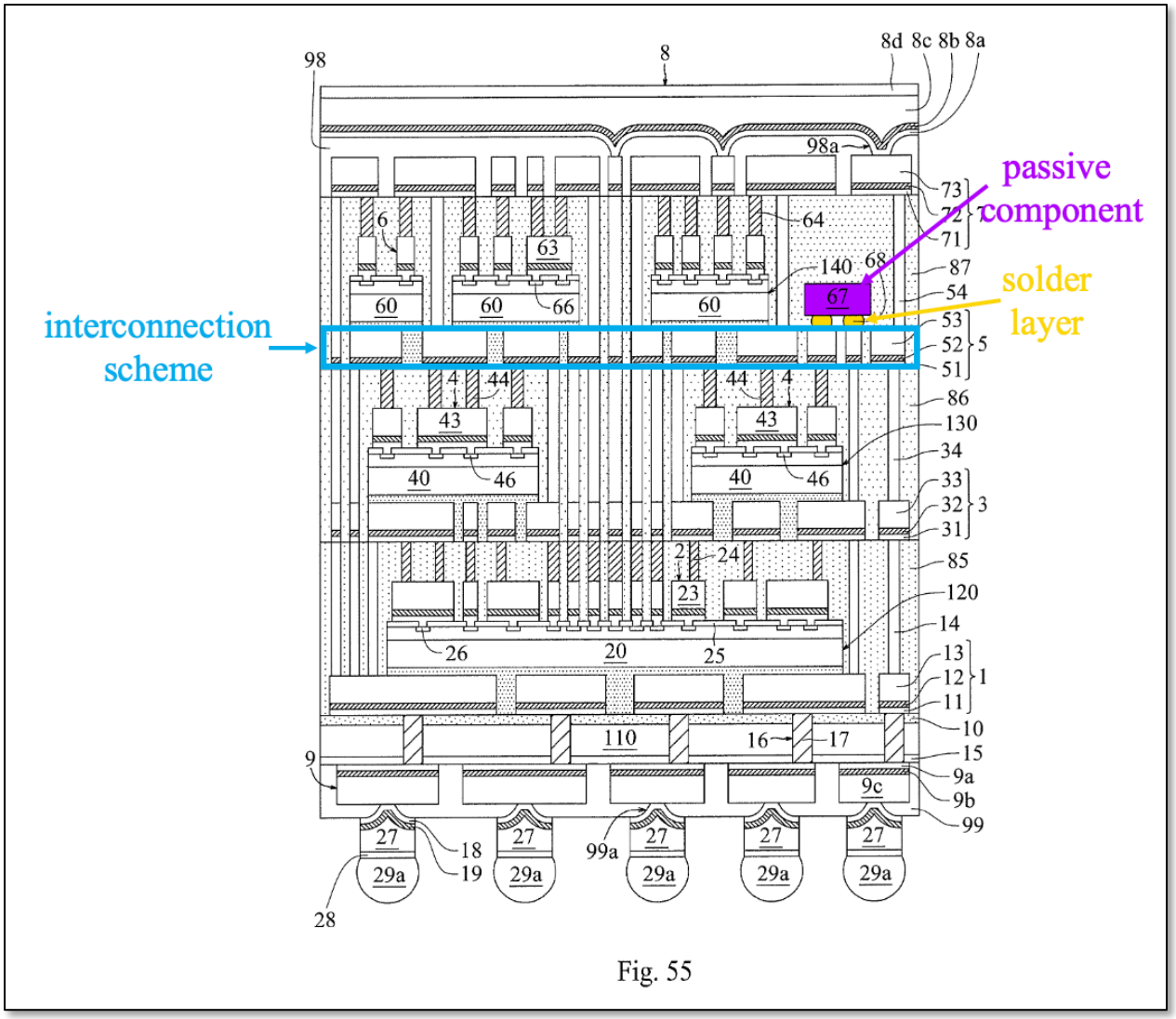


Fig. 55

EX1005, FIG. 55; *EX1003*, ¶325.

In FIG. 84's embodiment, Lin-191 discloses chip 140 is *over* and connected to patterned metal layer 5. *EX1005*, FIG. 84, [0273], [0340].

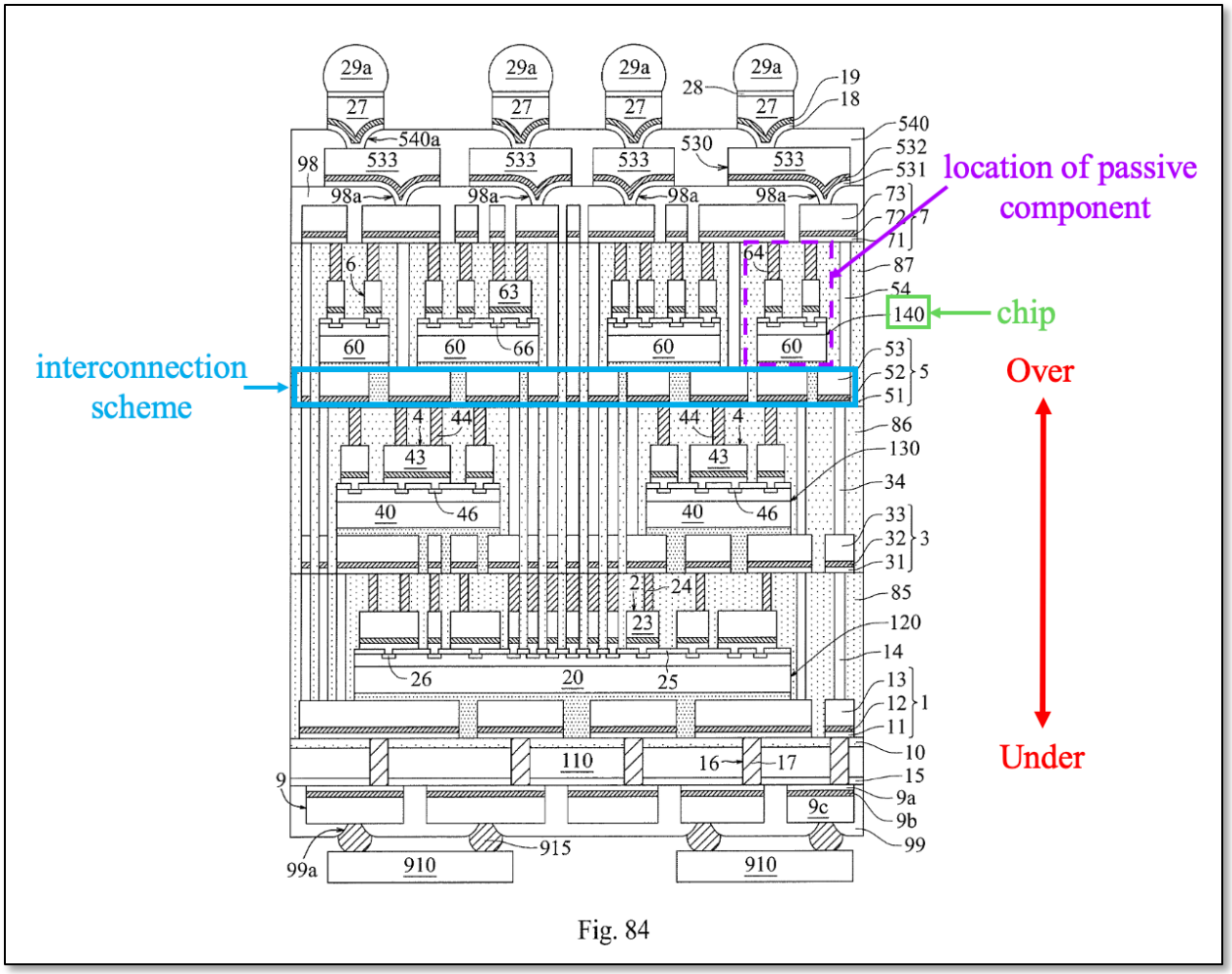


Fig. 84

EX1005, FIG. 84; *EX1003*, ¶326.

Lin-191 expressly discloses replacing chip 140 with passive component 67. *EX1005*, [0340]. Accordingly, Lin-191 teaches or renders obvious *passive component* (passive component 67) *over said first interconnection scheme* (layers 5). Upon chip 140 being replaced with passive component 67, passive component 67 is connected to an *interconnection scheme* (layer 5) through a *solder layer* (solder joints 68), as shown in FIG. 55. *EX1005*, [0340]; *EX1003*, ¶327. To the extent there

is any dispute regarding Lin-191's express disclosure of replacing chip 140 with passive component 67, based on these same disclosures, a POSITA would have found this same structure obvious in view of the same disclosures because the modification is the application of a known technique (a passive component connected to an interconnection scheme via a solder joint) to a known device (Lin-191's package) to yield the predictable result of Lin-191's FIG. 84 embodiment having a passive component 67 in place of a chip 140. *EX1003*, ¶327.

b) MTC

Yu teaches passives including "chip resistors" and "chip capacitors." *EX1010*, 1:41-42. Lin-191 teaches connecting *passive component[s]* in a multiple chip package. Thus, a POSITA would have been motivated and found obvious to modify Yu's *first interconnection scheme* with Lin-191's teachings of a *passive component* connected to a metal interconnect. *EX1003*, ¶329. A POSITA would have appreciated that by connecting a passive component, e.g., a capacitor, over Yu's ILD/RDL structure, Yu's *chip package* would advantageously mitigate signal desynchronization and preserve signal integrity. *Id.* The modification is the application of a known technique (passive component) to a known device (Yu's chip package) to yield predictable results. *EX1003*, ¶330. A POSITA would have had a REOS because soldering passive components into chip packages was a well-

established industry practice before the '763 Patent, and passive components in chip packages was likewise ubiquitous. *Id.*

C. Claim 3

A third metallization layer 20 portion is *a fourth metal interconnect*, which is *over* a sidewall of die 52 because it is positioned on the opposite side of molding compound 18 (*over*) from die 52's *sidewall*. Additionally, metallization layer 20 comprises a portion extending laterally beyond the *sidewall*; thus, metallization layer 20 is *across* the *sidewall*.

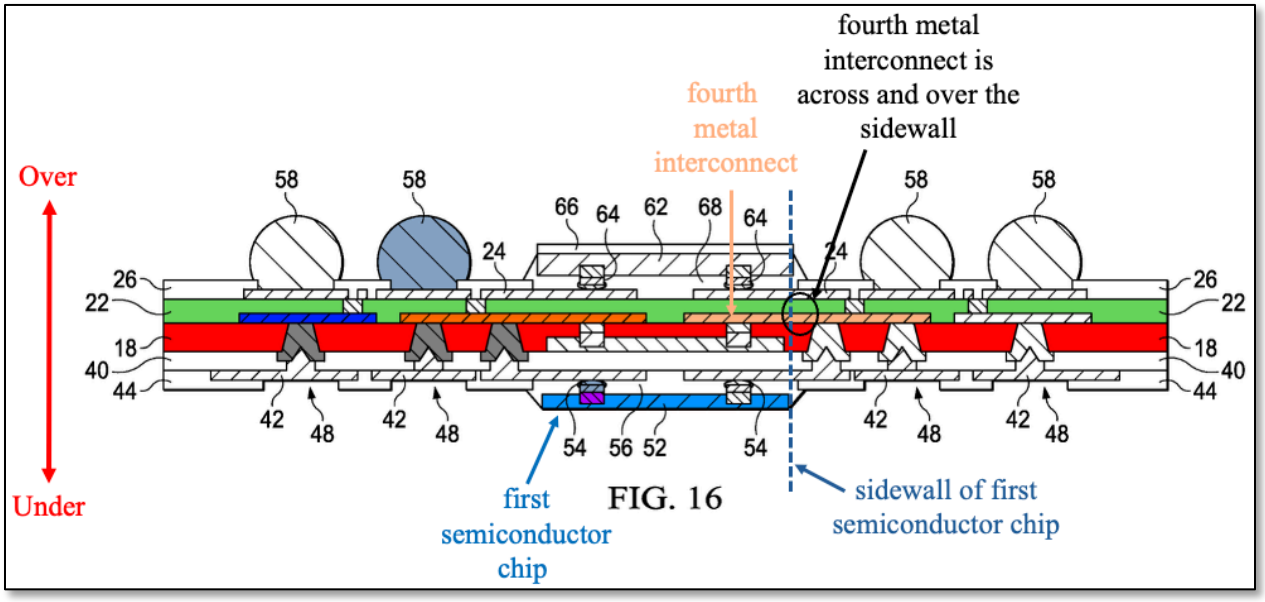
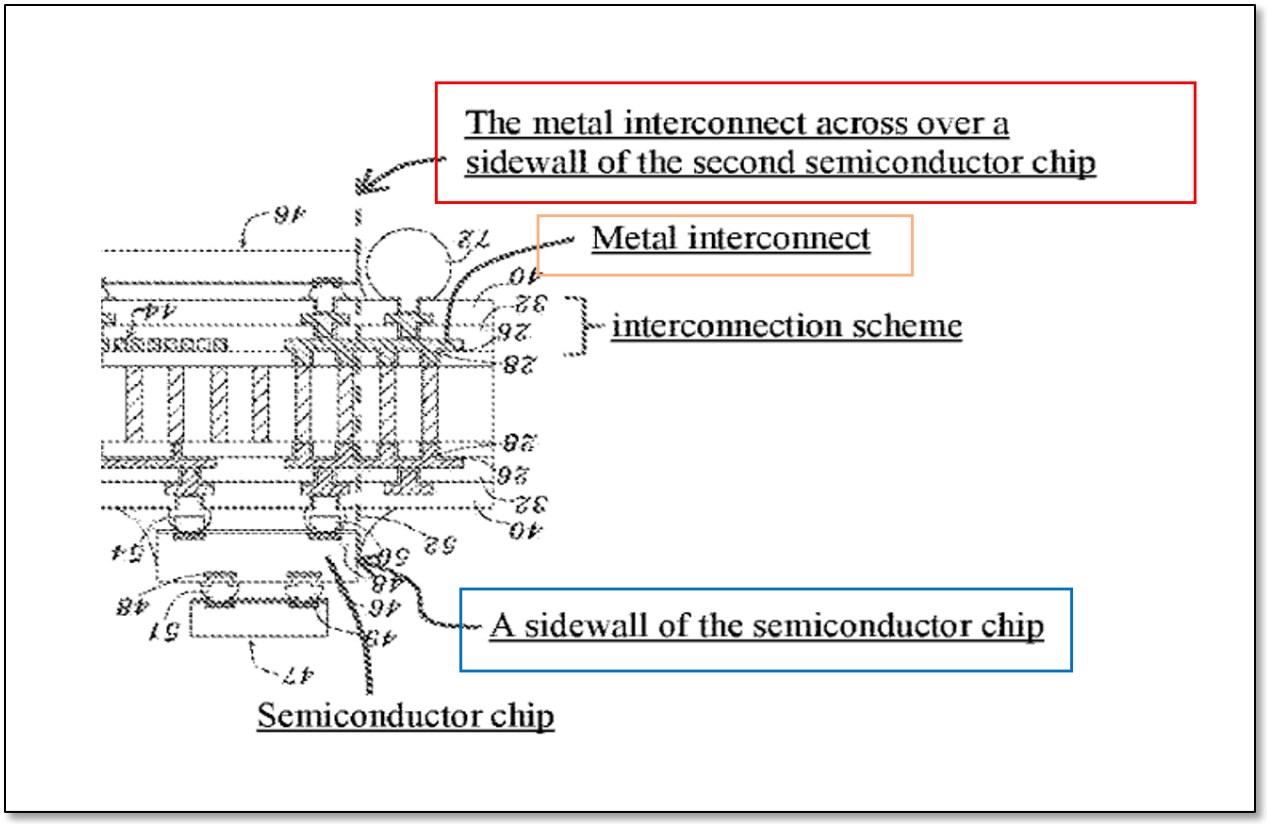


FIG. 16

EX1010, FIG. 16; *EX1003*, ¶¶331-332; *see* Section V.A.9 (supporting caselaw).



EX1032, 537[8].

D. Claim 4

1. 4(a)

Yu's package includes "die 62," i.e., *a second semiconductor chip over said first interconnection scheme*. *EX1010*, 4:53-58.

[8] Annotated figure PO argued supports language similar to Claim 3.

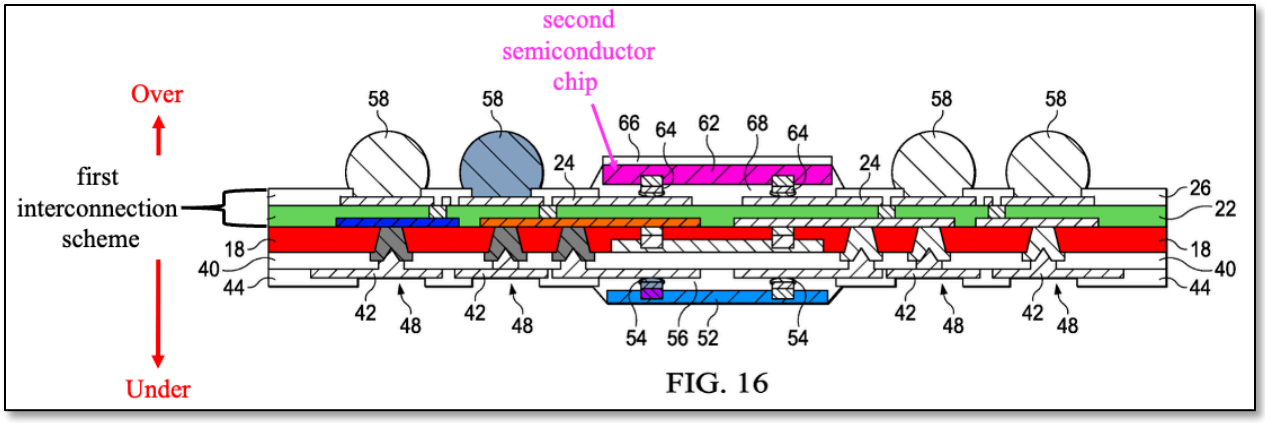


FIG. 16

EX1010, FIG. 16; *EX1003*, ¶333.

2. 4(b)

Die 62 is "attached…to conductive features in the second front side metallization layer 24" by "connectors 64," which are "C4 bumps." *EX1010*, 4:53-58. A connector 64 is a *second metal bump between said second semiconductor chip and first interconnection scheme*:

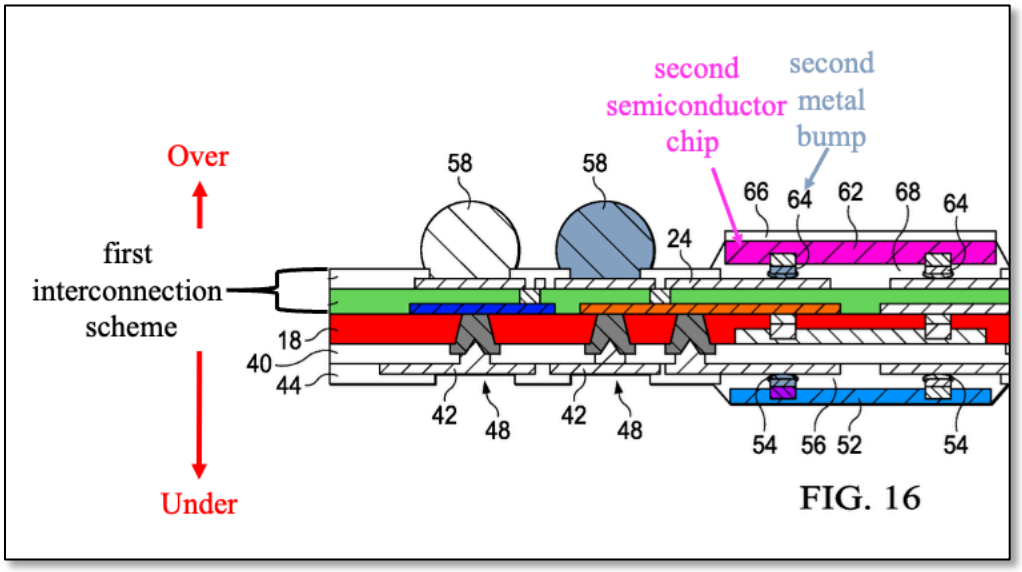


FIG. 16

EX1010, FIG. 16 (excerpt); *EX1003*, ¶334.

E. Claim 5

See Section V.E. The same MTC and REOS for Sundaram-Lin-191 apply to Yu-Lin-191, i.e., the modification would advantageously increase the functionality of Yu's package. *EX1003*, ¶335. Further evidencing the motivation and REOS, Yu teaches dies can be "logic circuitry die, a memory die, or any other die." *EX1010*, 2:50-51.

F. Claim 7

1. 7(a)

A portion of Yu's "second metallization layer 24" is *a fourth metal interconnect over* first metallization layer 20 and ILD layer 22. *EX1010*, 3:28-32; *see* Section VIII.A.11.

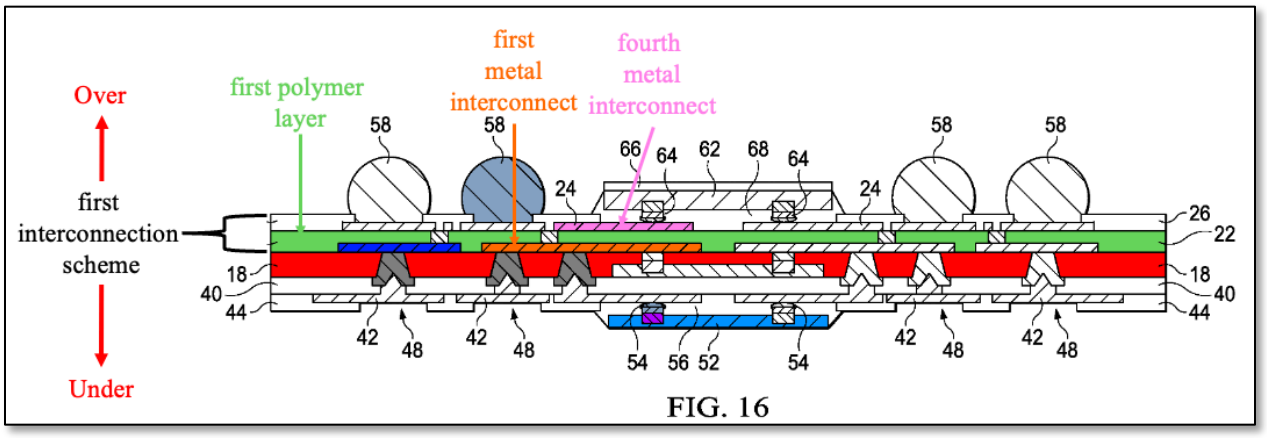


FIG. 16

EX1010, FIG. 16; *EX1003*, ¶¶336-337.

Alternatively, Yu teaches "any number of metallization layers and ILD layers may be formed, and the use of two…is used as an example." *EX1010*, 3:41-43. Thus, a third metallization layer is *a fourth metal interconnect over said first metal*

interconnect and said first polymer layer when the *first polymer layer* is ILD layer 26. Yu teaches "[c]onductive material deposited during the formation of a subsequent metallization layer may be deposited in openings of the previously formed ILD layer to electrically couple respective metallization layers," thus teaching the third metallization layer being on layer 26 and below connector 58. *EX1010*, 3:32-35; *EX1003*, ¶338.

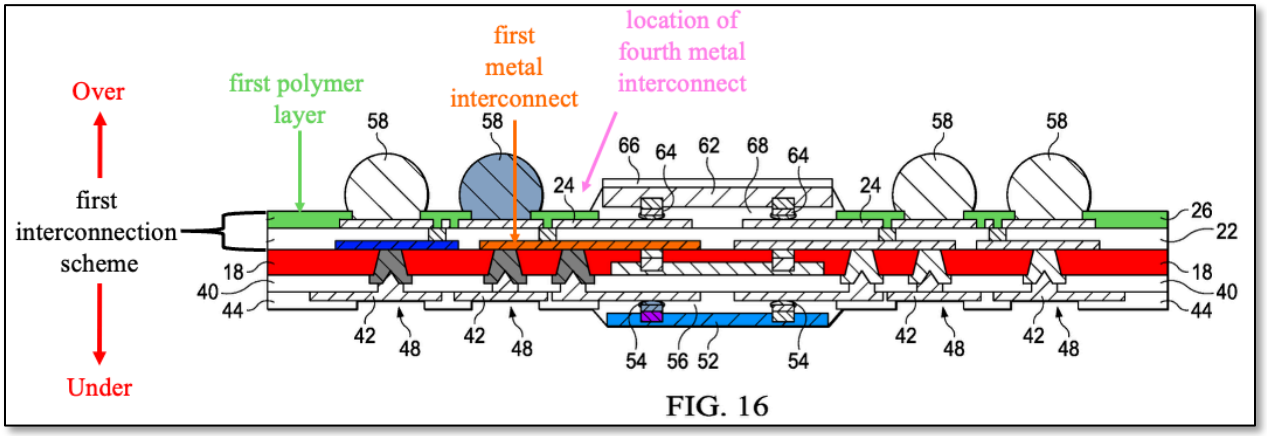


FIG. 16

EX1010, FIG. 16.

2. 7(b)

Metallization layer 24 is on (over) ILD layer 22, which is "over the first metallization layer 20" such that ILD layer 22 *is between* layers 20, 24. *EX1010*, 3:20-35.

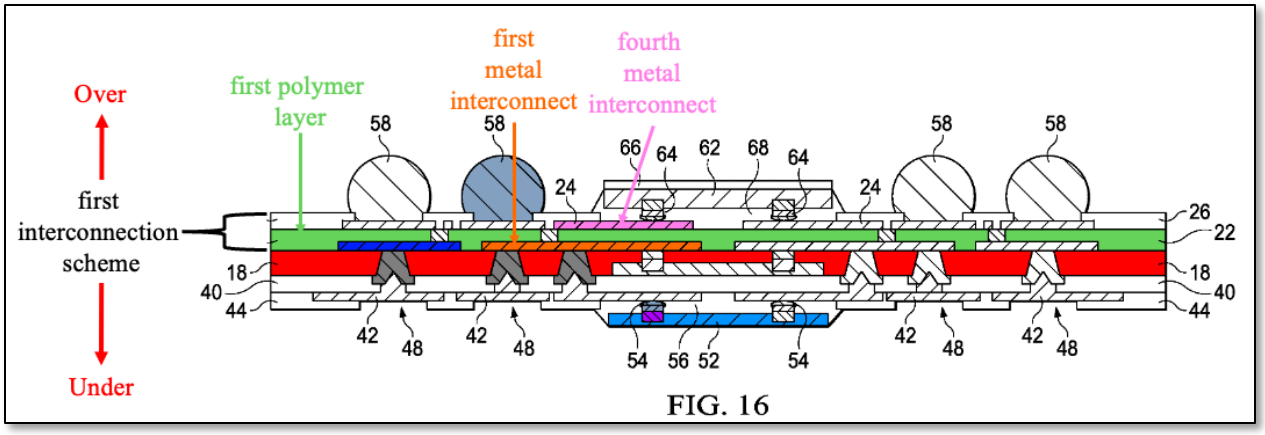


FIG. 16

EX1010, FIG. 16; ¶339.

Alternatively, because metallization layers are deposited on ILD layers, Yu's third metallization layer is on ILD layer 26 such that ILD layer 26 (*first polymer*) *is between said first and fourth metal interconnects*. *EX1010*, 3:32-35; *see* Section V.G.2, footnote 6.

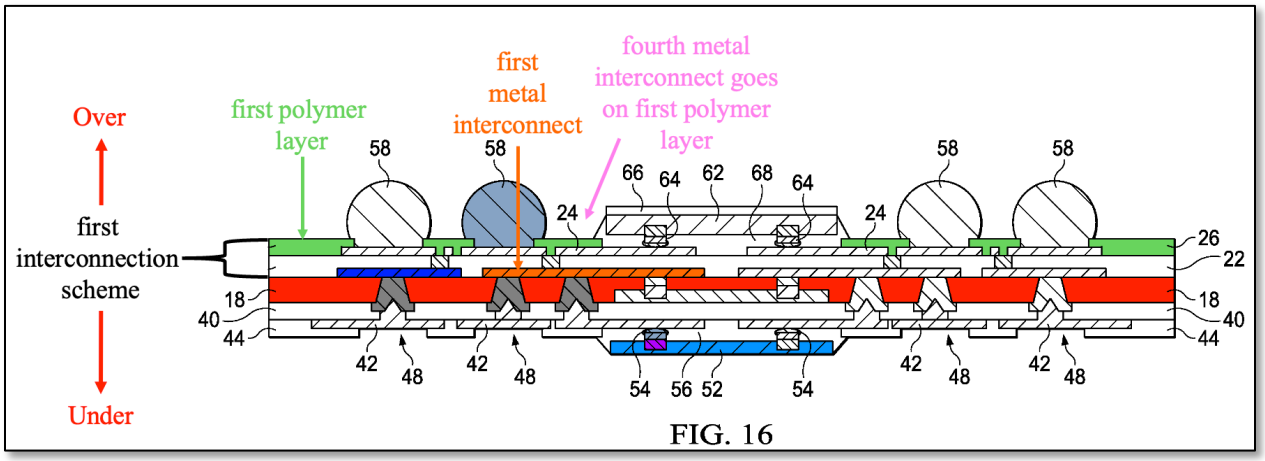


FIG. 16

EX1010, FIG. 16; ¶340.

3. 7(c)

Additional metallization layers are "formed using the same or similar processes as…first metallization layer 20" such that the second metallization layer

24 and the third metallization layer both *comprise[] a fourth copper layer* (copper seed layer) *and a fifth copper layer on said fourth copper layer* (electroplated copper layer). *EX1010*, 3:28-32, 3:5-18; *see* Section VIII.A.13; *EX1003*, ¶341.

a) Lin-191's Teachings and MTC

Lin-191 teaches a *metal interconnect* with the claimed layers. *See* Section V.G.3. The MTCs and REOS for modifying Sundaram per Lin-191 apply for the Yu-Lin-191 combination. Like Yu's metallization layers, Lin-191's metal interconnect comprises a copper seed layer 72 and a copper metal layer 73 and additionally comprises metal adhesion layer 71 (*fourth metal layer*) under layers 72, 73. *EX1005*, [0127-0128], [0133]. Thus, a POSITA would have been motivated and found obvious to apply three-metal layer interconnect teachings, including Lin-191's adhesion layer 71 teachings, to Yu's *fourth metal interconnect* thereby yielding *a fourth metal layer, a fourth copper layer on said first metal layer, and a fifth copper layer on said fourth copper layer* to obtain the benefits of Lin-191's adhesion layer 31. *EX1003*, ¶342.

Advantageously, nickel adhesion layers advantageously mitigate copper diffusion out of the metal interconnect, reducing void formation and the risk of delamination. *EX1003*, ¶343. The combination is the application of a known technique (Lin-191's three-layer metal interconnect) to a known device (Yu's metal interconnect) ready for improvement to yield predictable results. *Id.* There would

have been a REOS because Lin-191 teaches forming adhesion layer 71 using manufacturing techniques also taught by Yu such that the modification would have been simple and straightforward. *Compare EX1005*, [0259] *with EX1010,* 3:5-16; *EX1003*, ¶343.

G. Claim 8

Yu teaches "a back side ILD and RDL structure" with a "first back side ILD layer 40, a second back side metallization layer 42, [and], a second ILD layer 44[.]" *EX1010*, 4:7-11. Thus, the back side ILD/RDL structure is *a second interconnection scheme under said solid layer and on said second surface.*

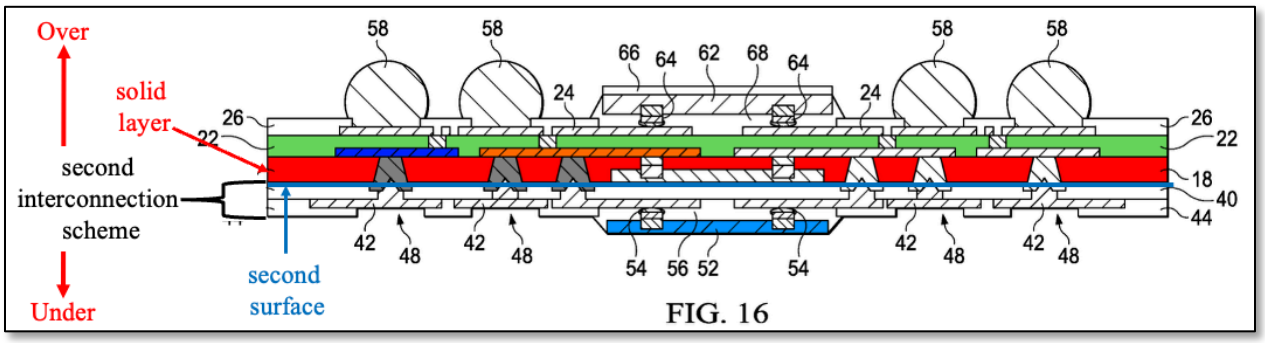


FIG. 16

EX1010, FIG. 16; *EX1003*, ¶344.

H. Claim 9

See Sections VIII.A.18 (mapping the *first metal pad*), V.I (MTCs and REOS incorporated); *EX1003*, ¶345.

I. Claim 10

Molding compound 18 includes *a third region opposite to said second region* and *between said first region and another edge* of compound 18. The *third region* includes a *plurality of copper plugs in said plurality of through vias*:

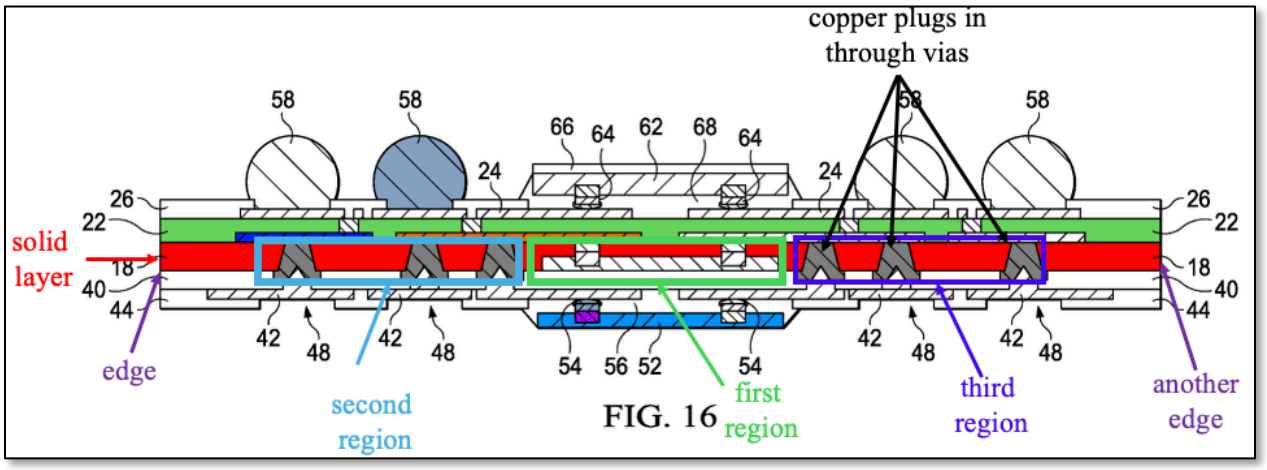


FIG. 16

EX1010, FIG. 16; *EX1003*, ¶346.

J. Claim 11

Yu's TMVs 38 (*first copper plug*) extend from either surface of the *solid layer*. *EX1003*, ¶347. At Claim 1(a)(iii), Yu's *solid layer* is modified per Lin-191 to be *between about 100 and 300 micrometers*. *See* Section VIII.A.5. Because the *first copper plug has a thickness* equal to that of the *solid layer*, Yu-Lin-191 teaches or renders obvious *wherein said first copper plug has a thickness between 100 and 300 micrometers*. *EX1003*, ¶347; Sections V.A.5, V.K (including discussions regarding no criticality of the claimed *thickness*).

K. Claim 12

A third TMV 38 (*third copper plug*) *vertically in* a *though via* is shown below:

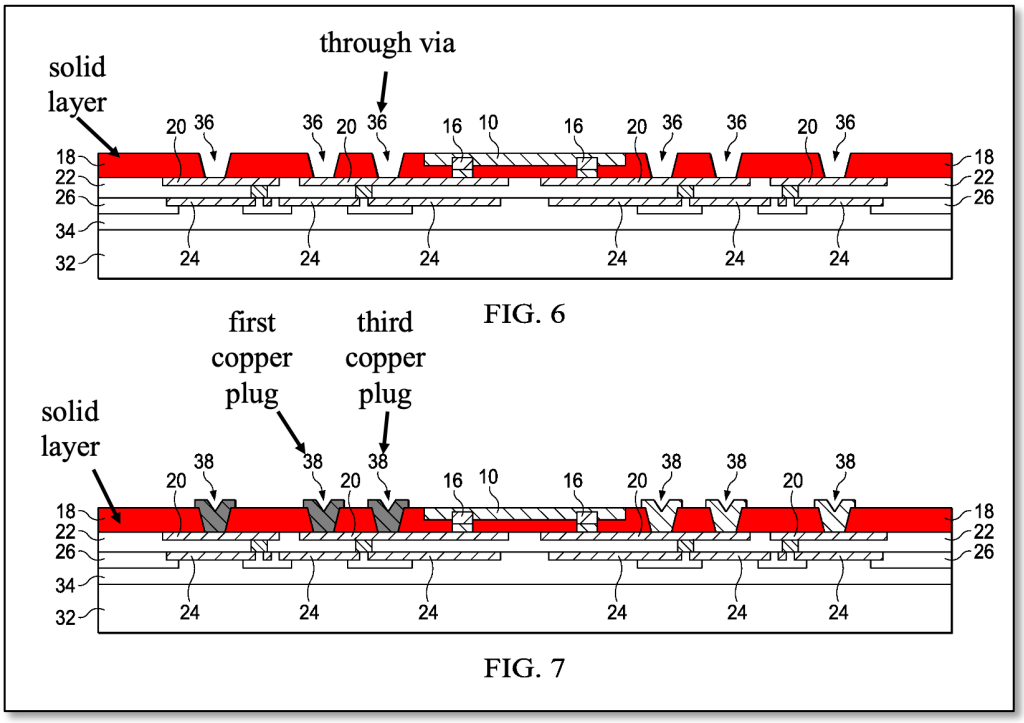


FIG. 6

FIG. 7

EX1010, FIGS. 6-7; *EX1003*, ¶348.

1. Lin-191's Teachings and MTC

Lin-191 teaches encapsulating layer 85 includes "metal pillars or bumps 14" having a "pitch between neighboring or adjacent pairs" of "between 100 and 250 micrometers," falling within the claimed range and thereby teaching or rendering obvious the claimed range. *EX1005*, [0075]; Section V.A.5 (supporting caselaw); *EX1003*, ¶¶349-350 (citing *EX1001*, 6:11-18 and opining no criticality of the claimed pitch).

A POSITA would have found obvious and been motivated to apply Lin-191's pitch to Yu's *first* and *third copper plug[s]*, which are likewise neighboring/adjacent. *EX1003*, ¶351. A pitch *between 200 and 1000 micrometers* was known to enable high bandwidth speeds such as "at least about 10 GB/s" in a "digital camera for cell phones," motivating the combination as Yu expressly contemplates use of the chip package in a cell phone. *EX1004*, 6:42-55; *EX1010*, 1:53-55; *EX1003*, ¶351. The combination is the application of a known technique (Lin-191's plugs having a pitch between *200 and 1000 micrometers*) to a known device (Yu's chip package) ready for improvement to yield predictable results. *EX1003*, ¶351. A POSITA would have a REOS at least because the modification would have been simple and straightforward as methods of controlling pitch of metal plugs were well-known. *Id.*

L. Claim 14

1. 14(a)

See Section VIII.D. Yu's die 62 (*second semiconductor chip*) is *over* and *connected to said first interconnection scheme through a second metal bump* as bump 64 is on metallization layer 24, which is part of Yu's *first interconnection scheme*. *See* Section VIII.A.10.

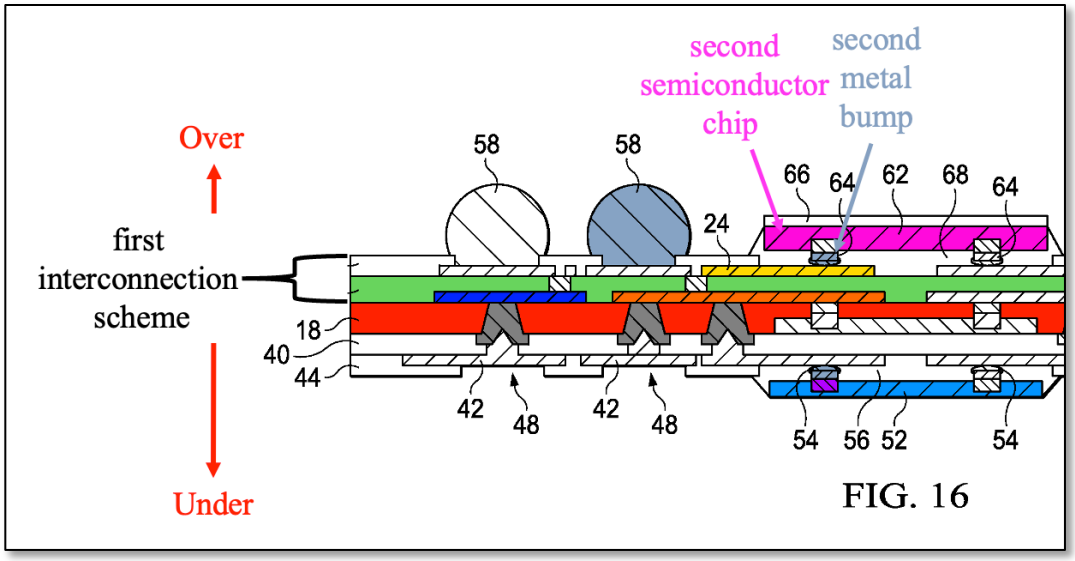


FIG. 16

EX1010, FIG. 16 (excerpt); *EX1003*, ¶352.

2. 14(b)

As discussed at Claim 1(c)(i), Yu's *first polymer layer* may also include layer 26, such that the *first polymer layer* comprises layers 22 and 26. In this mapping, die 62 *has a height between* its *backside surface* and *a top surface of* ILD 26 *smaller than a thickness of said first metal bump*. *See* Section VIII.A.11.

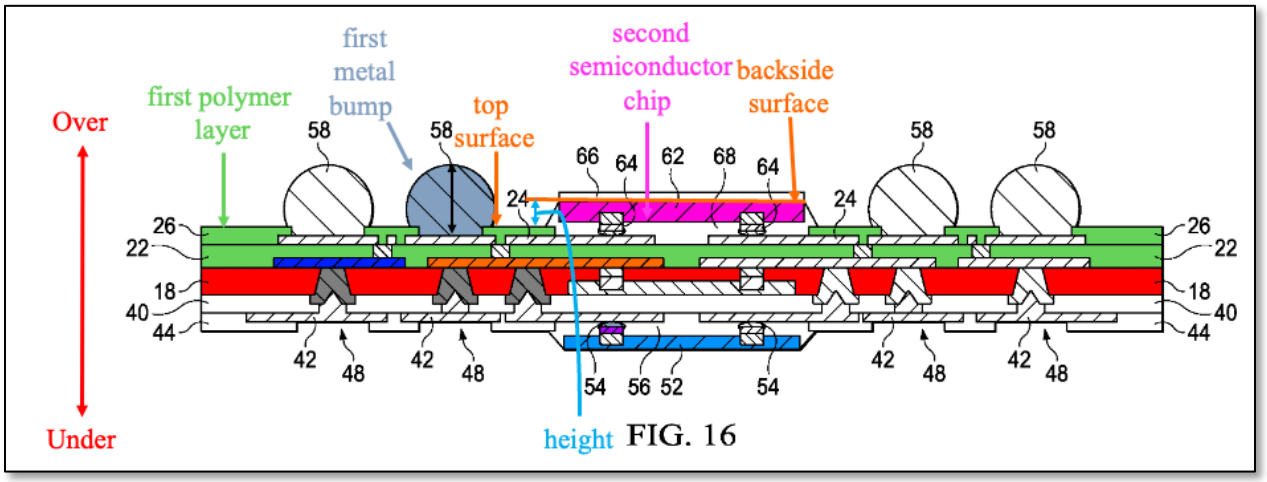


FIG. 16

EX1010, FIG. 16; *EX1003*, ¶353; *see* Section V.A.9 (supporting caselaw).

Alternatively, Yu's *first polymer layer* is layer 26, and die 62's *height* also satisfies Claim 14(b).

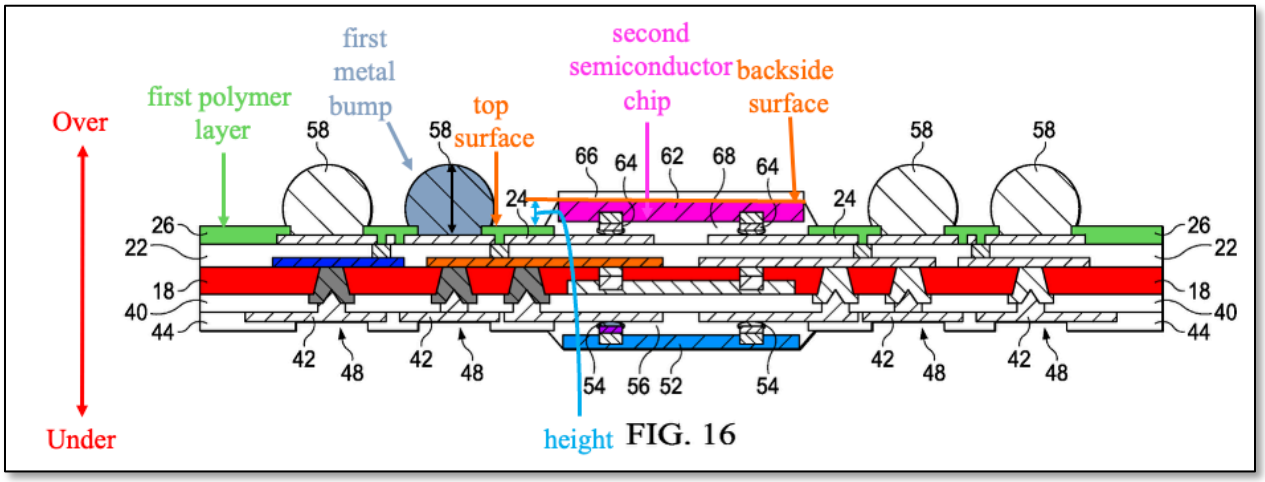


FIG. 16

EX1010, FIG. 16; *EX1003*, ¶354.

M. Claim 15

TMVs 38 (*copper plugs*) are on either side of the *first region*, which encapsulates a die 10 such that there are *no any copper plug[s] in said first region*. *EX1010*, 2:41-65 (describing die 10), FIGS. 1-2, 8:7-8 ("[P]ackage 202 compris[es] a first die encased in molding compound….").

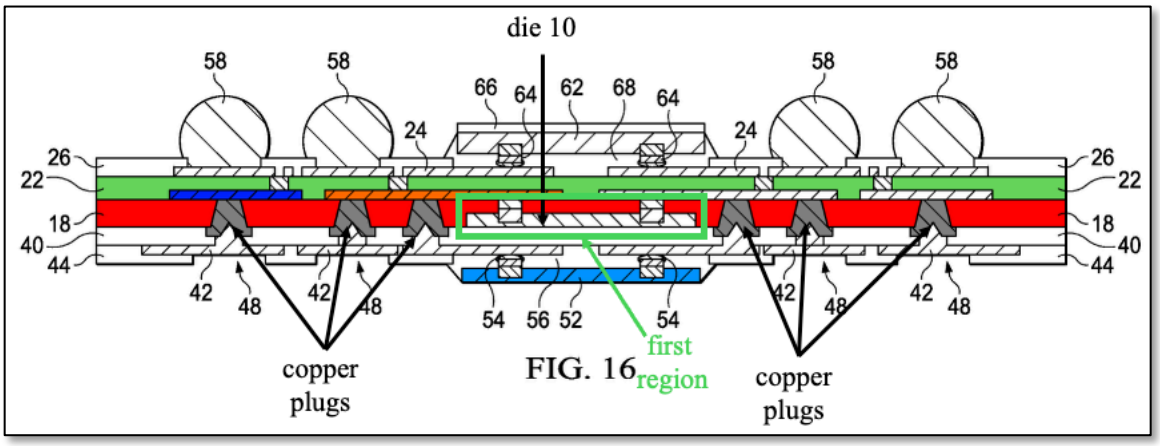


FIG. 16

EX1010, FIG. 16; *EX1003*, ¶¶355-357.

N. Claim 17

a) Lin-191's Teachings

Lin-191's *solid layer* includes encapsulating layer 85 (discussed at Claim 1(a)(ii)) and further includes an insulating layer 10, which is made of "silicon dioxide (SiO_2)" and over which layer 85 is "formed." *EX1005*, [0052], [0109]; *see* Section VIII.A.5.

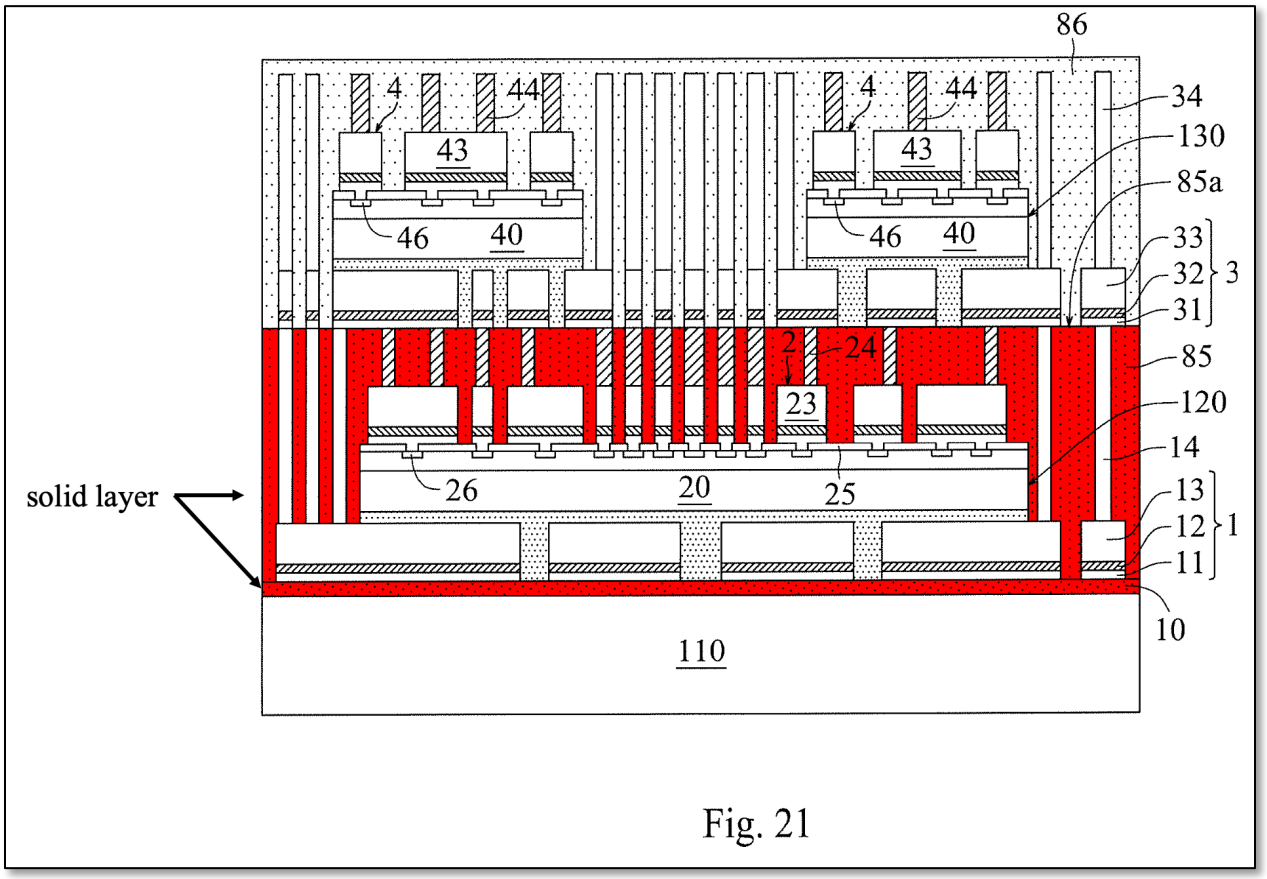


Fig. 21

EX1005, FIG. 21; *EX1003*, ¶358.

Yu teaches molding compound 18 comprises "epoxy, polyimide, silicone rubber, the like, or a combination thereof," i.e., *a compound of silicon and oxygen*.

EX1010, 2:61-65; s*ee* Section VIII.A.4. Lin-191 teaches specifically SiO_2. In the combination, Yu is modified per Lin-191 such that *said compound* is the combination of Yu's molding compound 18 and Lin-191's insulating layer 10.

Because insulating layer 10 is SiO_2, the Yu-Lin-191 *compound comprises a SiO_2 compound*. *EX1003*, ¶¶359-360.

b) MTC

A POSITA would have been motivated and found obvious to modify Yu to have an SiO_2 layer per Lin-191 such that Yu's *solid layer* (molding compound 18) is modified to include an SiO_2 layer similar to Lin-191's teachings of a *solid layer* comprising encapsulating layer 85 and insulating SiO_2 layer 10. *EX1003*, ¶¶360-363. A POSITA would have recognized the SiO_2 layer to advantageously improve Yu's package's water vapor permeability as an SiO_2 layer provides an improved water vapor barrier relative to only having a silicone rubber molding compound. *EX1003*, ¶362. Water vapor permeability is a common problem in die encapsulation as greater water presence leads to increased oxidation, corrosion, and enhanced ion-movement. *Id.* Thus, the addition of an SiO_2 layer to Yu's package would reduce water vapor penetration, increasing the reliability of Yu's package. *Id.* Further advantages result from the insulation provided by the SiO_2 layer. *EX1003*, ¶363. There would have been a REOS because Lin-191 teaches layer 10 is formed via "a chemical-vapor deposition (CVD) process, a spin-coating process or a lamination process," which

are all techniques also disclosed by Yu, making the modification simple and straightforward. *EX1005*, [0050]; *EX1010*, 7:16-18; *EX1003*, ¶364. The combination is the application of Lin-191's known SiO_2 layer technique to Yu's package ready for improvements to yield the predictable results of improved water vapor permeability and insulation. *EX1003*, ¶¶360-364.

IX. GROUND 2B: CLAIMS 6, 16, 18-21, AND 23 ARE OBVIOUS OVER YU, LIN-191, AND SUNDARAM

A. Claim 6

a) Sundaram's Teachings and MTC

Sundaram teaches Claim 6. *See* Sections V.F.1-4. A POSITA would have been motivated to apply Sundaram's teachings to Yu such that Yu's die 52 (*first semiconductor chip*) comprises a *through-silicon-via metal layer* connecting *metal pad[s]* and Yu's package includes a *second semiconductor chip under said first semiconductor chip* and connected thereto by the *metal pad[s]*. *EX1003*, ¶365. Yu teaches multiple chips in a chip package, motivating the combination. *EX1010*, FIG. 52; *EX1003*, ¶365.

A POSITA would have recognized that modifying Yu's die 52 to have a TSV connecting metal pads would have allowed for an additional chip (i.e., the *second semiconductor chip*) to be stacked thereon and electrically connected to die 52. *EX1003*, ¶366. Further, a POSITA would have recognized that Sundaram's teachings would enable the additional chip to be added to Yu's package without

having to add an entire additional package 202. *Id.* The ability to add just one additional chip to Yu's package would have been desirable for applications merely requiring just one more chip and avoided a drastic increase in package size (i.e., because one chip would require less space than another package 202). *Id*. Moreover, modifying Yu's package to stack chips would have advantageously increased package density and shortened interconnects between chips in the package. *Id.*

The modification is the application of a known technique (chip stacking, connecting metal pads with a TSV) to a known device (Yu's chip package) to yield the predictable result of Yu's package 202 having another chip under die 52 connected thereto by metal pads and a TSV. *EX1003*, ¶367. Methods of forming TSVs and metal pads were well established, leading to a REOS. *Id.*

B. Claim 16

a) Sundaram's Teachings and MTC

Sundaram teaches Claim 16. *See* Section V.N. A POSITA would have found obvious and been motivated to modify Yu-Lin-191 further per Sundaram's teachings of adjacent chips under an interconnection scheme. *EX1003*, ¶368. This modification would have predictably improved Yu's chip package by enabling the addition of another chip without increasing the vertical extent of the package. *Id.* Further, Sundaram expressly motivates the combination teaching the side-by-side

configuration overcomes a problem with adding "multiple dies over 4" in 3D ICs. *EX1004*, 7:59-61.

The combination is the application of a known technique (Sundaram's side-by-side configuration) to a known device (Yu's chip package) ready for improvement to yield predictable results. *EX1003*, ¶369. There would have been a REOS because the modification would have been simple and straightforward, i.e., placing another chip adjacent to Yu's existing chip and connecting the chip to metallization layer 24 in the same way as die 52, i.e., via an "opening" in ILD layer 44 and "to conductive features in the second back side metallization layer." *EX1010*, 4:40-43, FIG. 11; *EX1003*, ¶369.

C. Claim 18

1. 18(Pre)

See Section VIII.A.1.

2. 18(a)

See Section VIII.A.2.

3. 18(a)(i)

See Section VIII.A.4.

4. 18(a)(ii)

See Section VIII.A.5.

5. 18(a)(iii)

See Section VIII.A.6.

6. 18(b)

See Section VIII.A.7, reciting corresponding limitations; *EX1003*, ¶375.

7. 18(b)(i)

Yu's TMVs 38 (*metal conductors*) are formed by a copper "seed layer" (*first metal layer*) deposited into "TMV openings 36" and a "conductive material, such as copper" (*copper portion*) deposited onto the copper seed layer. *EX1010*, 3:60–4:6; *EX1003*, ¶376. Because the *copper portion* is deposited onto the seed layer, the *first metal layer cover[s] a sidewall of said copper portion*. *See* Section VIII.A.8.

a) Sundaram's Teachings and MTC

Sundaram teaches or renders obvious Claim 18(b)(i). *See* Section V.P.7. A POSITA would have been motivated and found obvious to apply Sundaram's teachings to Yu's TMVs 38, resulting in *said copper portion having a diameter in a direction between 50 and 200 micrometers and greater than a thickness of said first metal layer in said direction*, teaching or rendering obvious Claim 18(b)(i). Section V.A.5 (supporting caselaw); *EX1003*, ¶377, 237 (citing *EX1001*, 4:46-50 and opining no criticality of the claimed copper thickness).

Yu already teaches the *first metal layer* and *copper portion* such that the modification is simply the application of Sundaram's dimensions to Yu's existing TMVs. *EX1003*, ¶¶377-378. Copper TMVs having Sundaram's diameter were common, and it would have been advantageous to apply Sundaram's copper seed layer dimension to Yu's seed layer to reduce void formation in Yu's *copper portion*.

Id. The modification is the application of a known technique (Sundaram's *copper portion* dimensions) to a known device (Yu's TMV) ready for improvement to yield predictable results. *Id.* There would have been a REOS because Yu already teaches the claimed *first metal layer* and *copper portion* and Sundaram merely provides an express teaching of the commonly-used dimensions for metal conductors. *Id.*

8. 18(b)(ii)

See Section VIII.A.9.

9. 18(c)

See Section VIII.A.10.

10. 18(c)(i)

See Section VIII.A.11.

11. 18(c)(ii)

See Section VIII.A.12, reciting corresponding limitations. *EX1003*, ¶382.

12. 18(c)(iii)

See Section VIII.A.13. Yu's metallization layer 20 *comprises a first copper layer* (copper seed layer). *EX1003*, ¶383.

13. 18(d)

See Section VIII.G. Yu's *second interconnection scheme is under said second surface*:

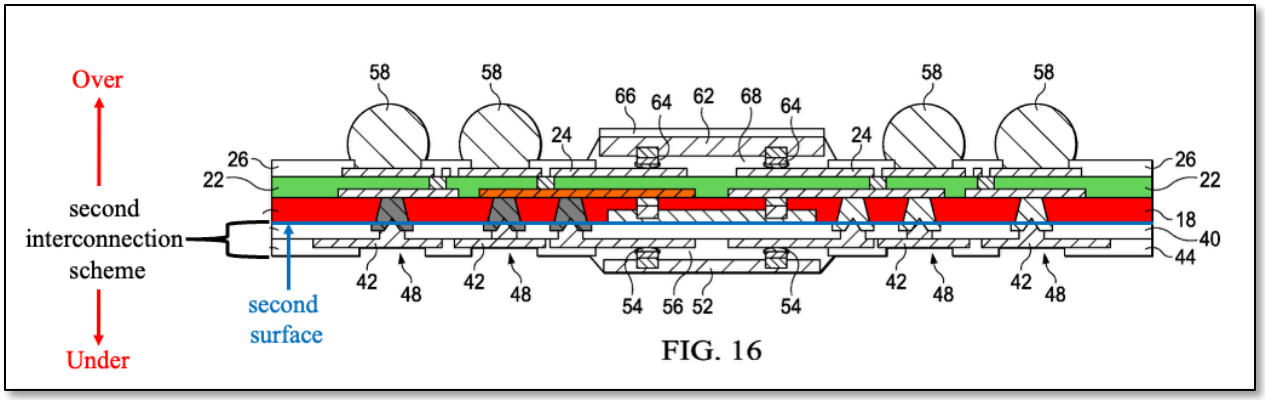


FIG. 16

EX1010, FIG. 16; *EX1003*, ¶384.

14. 18(d)(i)

A portion of metallization layer 42 is *a second metal interconnect under said second surface*, and ILD layer 44 is *a second polymer layer under* layer 42. *EX1010*, 4:7-14. Both layers 42, 44 are "formed the similar to or in the same manner as the ILD layers and metallization layers on the front side" such that Yu teaches layer 42 is *metal* and ILD layer 44 is *polymer*. *EX1010*, 4:7-14; *see* Section VIII.A.11.

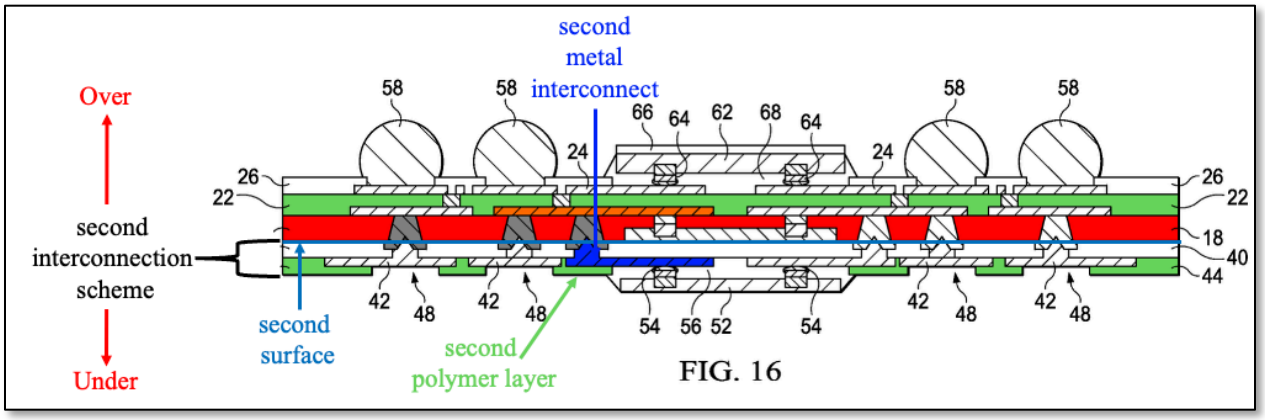
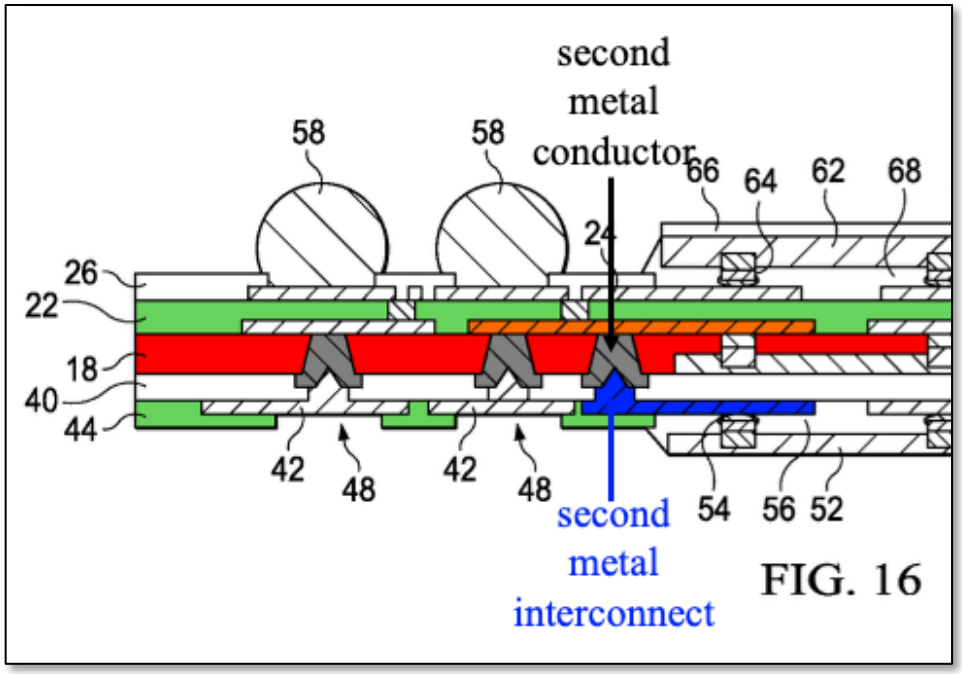


FIG. 16

EX1010, FIG. 16; *EX1003*, ¶¶385-386.

15. 18(d)(ii)

Layer 42 is connected to a TMV 38. *See* Section VIII.A.12.



EX1010, FIG. 16 (excerpt); *EX1003*, ¶387.

16. 18(d)(iii)

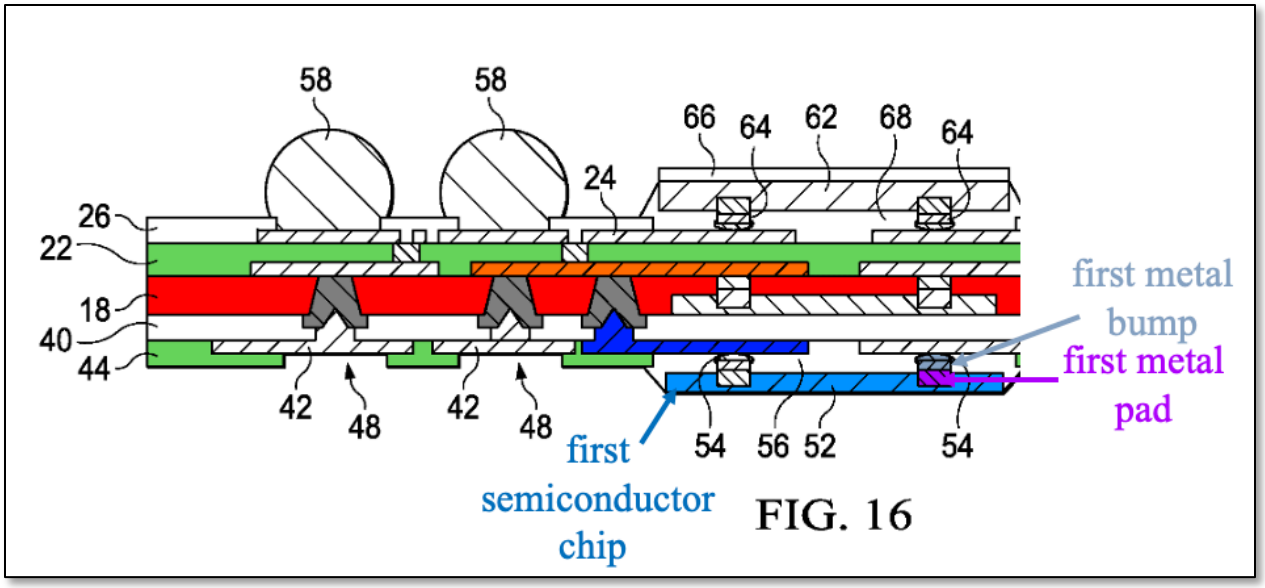
See Sections VIII.A.13, IX.C.12, reciting corresponding limitations. *EX1003*, ¶388.

17. 18(e)

See Section VIII.A.17.

18. 18(e)(i)

See Section VIII.A.18, reciting corresponding limitations. *EX1003*, ¶390.



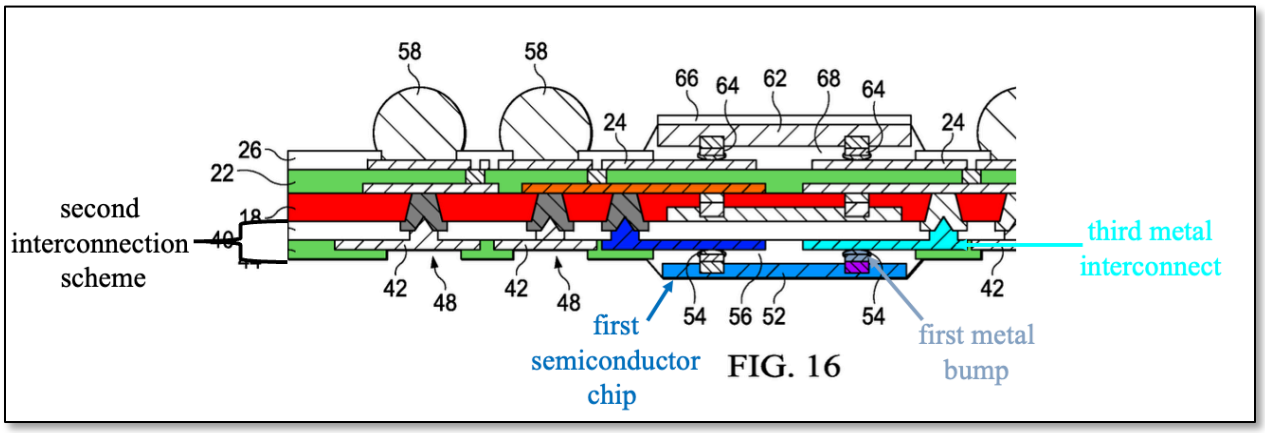
EX1010, FIG. 16 (excerpt)

19. 18(e)(ii)

See Section VIII.A.19, reciting corresponding limitations. *EX1003*, ¶391.

20. 18(e)(iii)

Yu's die 52 is *connected to* another portion of layer 42 (*third metal interconnect*) *through said first metal bump* (connector 54):



EX1010, FIG. 16 (excerpt); *EX1003*, ¶392.

D. Claim 19

See Section VIII.N.

E. Claim 20

See Section VIII.B. A POSITA would have been motivated to modify Yu's chip package to have a passive component *under* the interconnection scheme per Lin-191's FIG. 55 embodiment. *EX1003*, ¶394. Positioning the passive component, e.g., a capacitor, *under* the interconnection scheme would be more effective at filtering out HFI generated by die 52. *Id.*

F. Claim 21

See Section VIII.D.

G. Claim 23

See Section VIII.I.

X. GROUND 2C: CLAIM 13 IS OBVIOUS OVER YU, LIN-191, AND LIN-863

A. Claim 13

a) Lin-863's Teachings and MTC

Lin-863 teaches Claim 13. *See* Section VI.A. The MTCs and REOS for Sundaram-Lin-863 apply for Yu-Lin-863. Further evidencing the REOS, Yu, like Lin-863, already teaches an encapsulated die 10 such that applying Lin-863's fan-out teachings would have been simple and straightforward to Yu's similar *chip package*. *Compare EX1007*, 14:42-46, FIG. 9a *with EX1010*, FIG. 16; *EX1003*, ¶¶397-398.

XI. CONCLUSION

For the foregoing reasons, Petitioners respectfully request *inter partes* review of the Challenged Claims.

Respectfully submitted,

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XII. MANDATORY NOTICES UNDER 37 C.F.R. § 42.8(A)(1)

A. Real Party-In-Interest

Petitioners Taiwan Semiconductor Manufacturing Company Limited and Apple Inc. are the real parties-in-interest. 37 C.F.R. § 42.8(b)(1).

B. Related Matters

The '763 Patent is presently the subject of a patent infringement lawsuit filed against Petitioner, Apple Inc., in the United States District Court for the District of Delaware. *MYW Semitech, LLC v. Apple Inc.*, Case No. 1:25-cv-00504.

C. The Lead and Back-Up Counsel

Petitioners provide the following designation and service information for lead and back-up counsel. 37 C.F.R. §§ 42.8(b)(3) and 42.8(b)(4).

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D. 37 C.F.R. § 42.8(b)(4) – Service Information

Please address all correspondence to the lead and back-up counsel as shown above. Petitioners consent to electronic service by e-mail at the e-mail addresses provided above.

CLAIM LISTING APPENDIX
U.S. Patent No. 11,538,763 for Claims 1-23

Claim Designation	Claim Language
Claim 1(Pre)	A chip package comprising:
Claim 1(a)	a solid layer having a first surface and a second surface opposite to said first surface,
Claim 1(a)(i)	wherein said first surface is substantially parallel to said second surface,
Claim 1(a)(ii)	wherein said solid layer comprises a compound of silicon and oxygen,
Claim 1(a)(iii)	wherein said solid layer has a thickness between 100 and 300 micrometers,
Claim 1(a)(iv)	wherein said solid layer comprises a first region and a second region between said first region and an edge of said solid layer;
Claim 1(b)	a plurality of copper plugs in a plurality of through vias in said second region of said solid layer respectively,
Claim 1(b)(i)	wherein one of said plurality of copper plugs comprises a first copper layer contacting a sidewall of one of said plurality of through vias,
Claim 1(b)(ii)	wherein said first region has a width in a direction greater than a shortest distance between said sidewall of one of said plurality of through vias and said edge of said solid layer in said direction and greater than a pitch between two neighboring copper plugs of said plurality of copper plugs;
Claim 1(c)	a first interconnection scheme over said first surface,
Claim 1(c)(i)	wherein said first interconnection scheme comprises a first metal interconnect over said first surface, a second metal interconnect over said first surface and a first polymer layer over said first and second metal interconnects,
Claim 1(c)(ii)	wherein said first metal interconnect is connected to a first copper plug of said plurality of copper plugs, wherein said second metal interconnect is connected to a second copper plug of said plurality of copper plugs,
Claim 1(c)(iii)	wherein said first metal interconnect comprises a first metal layer and a second copper layer over said first metal layer,

Claim Designation	Claim Language
Claim 1(c)(iv)	wherein a top surface of said second copper plug and a top surface of said first copper plug are substantially in the same horizontal plane;
Claim 1(d)	a first metal bump over said first interconnection scheme,
Claim 1(d)(i)	wherein said first metal bump comprises a second metal layer and a tin-containing layer over said second metal layer; and
Claim 1(e)	a first semiconductor chip under said first interconnection scheme,
Claim 1(e)(i)	wherein said first semiconductor chip comprises a third metal interconnect on a first metal pad of said first semiconductor chip,
Claim 1(e)(ii)	wherein said third metal interconnect comprises a third metal layer on said first metal pad and a third copper layer over said third metal layer, wherein said third copper layer has a thickness between 5 and 30 micrometers.
Claim 2	The chip package of claim 1, further comprising a passive component over said first interconnection scheme and connected to said first interconnection scheme through a solder layer.
Claim 3	The chip package of claim 1, wherein said first interconnection scheme comprise a fourth metal interconnect across over a sidewall of the first semiconductor chip.
Claim 4(a)	The chip package of claim 1, further comprising a second semiconductor chip over said first interconnection scheme,
Claim 4(b)	wherein said second semiconductor chip comprises a second metal bump between said second semiconductor chip and said first interconnection scheme.
Claim 5	The chip package of claim 1, wherein said first semiconductor chip comprises a central-processing-unit (CPU) circuit block and a graphics-processing-unit (GPU) circuit block.
Claim 6(a)	The chip package of claim 1, further comprising a second semiconductor chip under said first semiconductor chip,
Claim 6(b)	wherein said first semiconductor chip comprises a second metal pad on a top surface of said first semiconductor chip, a third metal pad on a bottom surface of said first semiconductor chip
Claim 6(c)	a through-silicon-via metal layer connects to said second metal pad,
Claim 6(d)	wherein said third metal pad is connected to a fourth metal pad of said second semiconductor chip.

Claim Designation	Claim Language
Claim 7(a)	The chip package of claim 1, wherein said first interconnection scheme further comprises a fourth metal interconnect over said first metal interconnect and said first polymer layer,
Claim 7(b)	wherein said first polymer is between said first and fourth metal interconnects,
Claim 7(c)	wherein said fourth metal interconnect comprises a fourth metal layer, a fourth copper layer on said fourth metal layer, and a fifth copper layer on said fourth copper layer.
Claim 8	The chip package of claim 1, further comprising a second interconnection scheme under said solid layer and on said second surface.
Claim 9	The chip package of claim 1, wherein said first metal pad is an aluminum pad.
Claim 10	The chip package of claim 1, wherein said solid layer further comprises a third region opposite to said second region, wherein said third region is between said first region and another edge of said solid layer, wherein said plurality of copper plugs in said plurality of through vias in said third region respectively.
Claim 11	The chip package of claim 1, wherein said first copper plug has a thickness between 100 and 300 micrometers.
Claim 12	The chip package of claim 1, wherein said plurality of copper plugs comprise a third copper plug vertically in one of said plurality of through vias in said solid layer, wherein a pitch between said first and third copper plugs is between 200 and 1000 micrometers.
Claim 13	The chip package of claim 1, wherein said second region is a rectangle region and surrounding said first region.
Claim 14(a)	The chip package of claim 1, further comprising a second semiconductor chip over said first interconnection scheme and connected to said first interconnection scheme through a second metal bump,
Claim 14(b)	wherein said second semiconductor chip has a height is between a backside surface of said second semiconductor chip and a top surface of said first polymer layer is smaller than a thickness of said first metal bump.
Claim 15	The chip package of claim 1, wherein no any copper plug in said first region.

Claim Designation	Claim Language
Claim 16	The chip package of claim 1, further comprising a second semiconductor chip under said first interconnection scheme next to said first semiconductor chip.
Claim 17	The chip package of claim 1, wherein said compound comprises a SiO2 compound.
Claim 18(Pre)	A chip package comprising:
Claim 18(a)	a solid layer having a first surface and a second surface opposite to said first surface,
Claim 18(a)(i)	wherein said solid layer comprises a compound of silicon and oxygen,
Claim 18(a)(ii)	wherein said solid layer has a thickness between 100 and 300 micrometers,
Claim 18(a)(iii)	wherein said solid layer comprises a first region and a second region between said first region and an edge of said solid layer;
Claim 18(b)	a plurality of metal conductors in said second region of said solid layer respectively,
Claim 18(b)(i)	wherein one of said plurality of metal conductors comprises a copper portion and a first metal layer covering a sidewall of said copper portion, wherein said copper portion has a diameter in a direction between 50 and 200 micrometers and greater than a thickness of said first metal layer in said direction,
Claim 18(b)(ii)	wherein said first region has a width in said direction greater than a shortest distance between a sidewall of one of said plurality of metal conductors and said edge of said solid layer in said direction and greater than a pitch between two neighboring metal conductors of said plurality of metal conductors;
Claim 18(c)	a first interconnection scheme over said first surface,
Claim 18(c)(i)	wherein said first interconnection scheme comprises a first metal interconnect over said first surface and a first polymer layer over said first metal interconnect,
Claim 18(c)(ii)	wherein said first metal interconnect is connected to a first metal conductor of said plurality of metal conductors,
Claim 18(c)(iii)	wherein said first metal interconnect comprises a first copper layer;
Claim 18(d)	a second interconnection scheme under said second surface,

Claim Designation	Claim Language
Claim 18(d)(i)	wherein said second interconnection scheme comprises a second metal interconnect under said second surface and a second polymer layer under said second metal interconnect,
Claim 18(d)(ii)	wherein said second metal interconnect is connected to a second metal conductor of said plurality of metal conductors,
Claim 18(d)(iii)	wherein said second metal interconnect comprises a second copper layer; and
Claim 18(e)	a first semiconductor chip under said first interconnection scheme,
Claim 18(e)(i)	wherein said first semiconductor chip comprises a first metal bump on a first metal pad of said first semiconductor chip,
Claim 18(e)(ii)	wherein said first metal bump comprises a third copper layer with a thickness between 5 and 30 micrometers,
Claim 18(e)(iii)	wherein said first semiconductor chip is connected to a third metal interconnect of said second interconnection scheme through said first metal bump.
Claim 19	The chip package of claim 18, wherein said compound comprises a SiO2 compound.
Claim 20	The chip package of claim 18, further comprising a first passive component under said first interconnection scheme.
Claim 21	The chip package of claim 18, wherein said first semiconductor chip comprises a central-processing-unit (CPU) circuit block and a graphics-processing-unit (GPU) circuit block.
Claim 22	The chip package of claim 18, wherein said first metal layer is a silver-containing layer.
Claim 23	The chip package of claim 18, wherein said solid layer further comprises a third region opposite to said second region, wherein said third region is between said first region and another edge of said solid layer, wherein said plurality of metal conductors in said third region.

APPENDIX OF EXHIBITS

Exhibit 1001	U.S. Patent No. 11,538,763
Exhibit 1002	File History of the '763 Patent
Exhibit 1003	Declaration of Stanley Shanfield, Ph.D.
Exhibit 1004	U.S. Patent No. 9,167,694 to Sundaram, et al.
Exhibit 1005	U.S. Patent Publication No. 2010/0290191 to Lin, et al.
Exhibit 1006	U.S. Patent Publication No. 2011/0215458 to Camacho, et al.
Exhibit 1007	U.S. Patent No. 9,679,863 to Lin, et al.
Exhibit 1008	U.S. Patent Publication 2011/0266691 to Lin, et al.
Exhibit 1009	Intentionally left blank
Exhibit 1010	U.S. Patent No. 9,123,763 to Yu, et al.
Exhibit 1011	U.S. Patent Publication 2014/0035935 to Shenoy, et al.
Exhibit 1012	Andrea Chen, et al. *Semiconductor Packaging Materials Interaction and Reliability*, CRC Press, 2012
Exhibit 1013	Philip Garrou, et al., *RDL: an integral part of today's advanced packaging technologies*, Solid State Technology, May 2011
Exhibit 1014	U.S. Patent No. 8,780,576 to Haba, et al.
Exhibit 1015	U.S. Patent No. 7,902,648 to Lee
Exhibit 1016	U.S. Patent No. 7,964,961 to Lee, et al.
Exhibit 1017	U.S. Patent No. 7,241,641 to Savastiouk, et al.
Exhibit 1018	U.S. Patent Publication No. 2005/0110168 to Chuang
Exhibit 1019	U.S. Patent Publication No. 2011/0026232 to Lin, et al.
Exhibit 1020	U.S. Patent No. 5,086,558 to Grube, et al.
Exhibit 1021	U.S. Patent Publication No. 2011/0193219 to Lai, et al.
Exhibit 1022	U.S. Patent No. 6,818,545 to Lee, et al.
Exhibit 1023	U.S. Patent No. 6,974,659 to Su, et al.
Exhibit 1024	U.S. Patent Publication No. 2006/0175686 to Murata, et al.
Exhibit 1025	U.S. Patent Publication No. 2012/0098124 to Wu, et al.
Exhibit 1026	U.S. Patent No. 8,193,604 to Lin et al.
Exhibit 1027	U.S. Patent Publication No. 2004/0203224 to Halahan, et al.
Exhibit 1028	Philip Garrou, *Introduction to 3D Integration,* Handbook of 3D integration: Volumes 1 and 2, Technology and Application of 3D Integrated Circuits, 2012
Exhibit 1029	U.S. Patent Publication No. 2003/0068877 to Kinsman
Exhibit 1030	U.S. Patent Publication No. 2010/0246152 to Lin, et al.
Exhibit 1031	Yi Yang, et al, *CPU-Assisted GPGPU on Fused CPU-GPU Architectures,* IEEE Xplore
Exhibit 1032	File History of U.S. Patent No. 11,107,768

Exhibit 1033	U.S. Patent No. 4,863,773 to Rousseau, et al.
Exhibit 1034	U.S. Patent No. 6,365,265 to Tose, et al.
Exhibit 1035	E.D. Blackshear, et al., *The evolution of build-up package technology and its design challenges*, International Business Machines Corporation, 2005
Exhibit 1036	Intentionally Left Blank
Exhibit 1037	U.S. Patent No. 7,374,969 to Cho, et al.
Exhibit 1038	U.S. Patent No. 7,199,036 to Chan, et al.
Exhibit 1039	U.S. Patent No. 8,158,508 to Lin, et al.
Exhibit 1040	U.S. Patent No. 6,619,538 to Test, et al.
Exhibit 1041	U.S. Patent Publication No. 2011/0101523 to Hwang, et al.
Exhibit 1042	U.S. Patent No. 6,831,003 to Huang, et al.
Exhibit 1043	U.S. Patent Publication No. 2009/0226611 to Suzuki, et al.
Exhibit 1044	U.S. Patent No. 6,077,726 to Mistry, et al.
Exhibit 1045	U.S. Patent Publication No. 2010/0244245 to Pendse, et al.
Exhibit 1046	U.S. Patent Publication No. 2012/0206160 to Wu, et al.
Exhibit 1047	U.S. Patent Publication No. 2009/0174052 to Sogawa, et al.
Exhibit 1048	U.S. Patent Publication No. 2013/0100624 to Carpenter, et al.
Exhibit 1049	U.S. Patent No. 7,047,515 to Vitek, et al.
Exhibit 1050	U.S. Patent No. 8,116,097 to Love, et al.
Exhibit 1051	U.S. Patent Publication No. 2009/0237900 to Origuchi, et al.
Exhibit 1052	U.S. Patent Publication No. 2005/0002167 to Hsuan, et al.
Exhibit 1053	U.S. Patent Publication No. 2008/0067695 to Chow, et al.
Exhibit 1054	U.S. Patent No. 6,489,240 to Iacoponi, et al.
Exhibit 1055	U.S. Patent No. 6,578,178 to Mau
Exhibit 1056	U.S. Patent Publication No. 2012/0001190 to Okabe, et al.
Exhibit 1057	U.S. Patent No. 7,307,348 to Wood, et al.
Exhibit 1058	U.S. Patent No. 8,138,014 to Chi, et al.
Exhibit 1059	U.S. Patent No. 6,506,672 to Dagenais, et al.
Exhibit 1060	U.S. Patent No. 8,518,798 to Graetz
Exhibit 1061	U.S. Patent Publication No. 2009/0261473 to Lee, et al.
Exhibit 1062	U.S. Patent No. 6,440,289 to Woo, et al.
Exhibit 1063	U.S. Patent No. 6,812,143 to Lane, et al.
Exhibit 1064	U.S. Patent Publication No. 2012/0145552 to Nagai, et al.
Exhibit 1065	U.S. Patent Publication No. 2011/0147950 to Tsi, et al.
Exhibit 1066	U.S. Patent Publication No. 2009/0070727 to Solomon
Exhibit 1067	U.S. Patent Publication No. 2012/0098114 to Ishibashi
Exhibit 1068	U.S. Patent Publication No. 2011/0074028 to Pendse
Exhibit 1069	U.S. Patent No. 7,485,955 to Kang, et al.

Exhibit 1070	U.S. Patent Publication No. 2012/0104623 to Pagaila, et al.
Exhibit 1071	Intentionally left blank
Exhibit 1072	U.S. Patent No. 7,772,880 to Solomon
Exhibit 1073	U.S. Patent No. 7,989,270 to Huang, et al.
Exhibit 1074	U.S. Patent Publication No. 2011/0304999 to Yu, et al
Exhibit 1075	U.S. Patent Publication No. 2009/0117327 to Takada
Exhibit 1076	U.S. Patent Publication No. 2005/0081744 to Klocke, et al.,
Exhibit 1077	U.S. Patent No. 6,291,082 to Lopatin
Exhibit 1078	Intentionally left blank
Exhibit 1079	Intentionally left blank
Exhibit 1080	U.S. Patent Publication No. 2012/0319251 to Yu, et al.
Exhibits 1081-1089	Intentionally left blank
Exhibit 1090	U.S. Patent Publication No. 2005/0156280 to Patel, et al.
Exhibits 1091-1092	Intentionally left blank
Exhibit 1093	U.S. Patent No. 6,107,180 to Munroe, et al.
Exhibit 1094	U.S. Patent Publication No. 2011/0210283 to Ramirez, et al.
Exhibit 1095	U.S. Patent No. 6,452,502 to Dishongh, et al.
Exhibit 1096	U.S. Patent No. 6,344,401 to Lam.
Exhibit 1097	Richard K. Ulrich, et al., *Advanced Electronic Packaging,* IEEE Press Series on Microelectrical Systems, 2006
Exhibit 1098	Mulugeta Abtew, et al., *Lead-free Solders in Microelectronics*, Materials Science and Engineering, 2000
Exhibit 1099	Karl J. Puttlitz, et al., *Handbook of Lead-Free Solder Technology for Microelectronic Assemblies*, 2005
Exhibit 1100	U.S. Patent Publication No. 2013/0309832 to Cheng, et al.
Exhibit 1101	U.S. Patent Publication No. 2013/0151869 to Steinman, et al.
Exhibit 1102	Linely Gwennap, *Sandy Bridge Spans Generations: Intel Focuses on Graphics, Multimedia in New Processor Design*, Microprocessor, 2010
Exhibit 1103	U.S. Patent No. 6,330,164 to Khandros, et al.
Exhibit 1104	U.S. Patent No. 6,710,447 to Nogami.
Exhibits 1105-1126	Intentionally left blank
Exhibit 1127	U.S. Patent No. 8,238,113 to Iihola, et al.
Exhibit 1128	Intentionally left blank
Exhibit 1129	U.S. Patent No. 6,468,413 to Fanti, et al.
Exhibit 1130	U.S. Patent No. 8,132,775 to Goldmann.

Exhibit 1131	U.S. Patent Publication No. 2011/0186977 to Chi, et al.
Exhibit 1132	U.S. Patent No. 7,169,627 to Duh, et al.
Exhibit 1133	U.S. Patent No. 6,614,243 to Klehn, et al.
Exhibit 1134	U.S. Patent Publication No. 2009/0162622 to Van Veen, et al.
Exhibit 1135	U.S. Patent No. 6,570,259 to Alcoe, et al.
Exhibit 1136	U.S. Patent No. 7,741,567 to Beddingfield, et al.
Exhibit 1137	U.S. Patent No. 6,407,341 to Anstrom, et al.

CERTIFICATION OF WORD COUNT

The undersigned certifies pursuant to 37 C.F.R. § 42.24 that the foregoing Petition for *Inter Partes* Review, excluding any table of contents, mandatory notices under 37 C.F.R. § 42.8, certificates of service or word count, or appendix of exhibits, contains 13,457 words according to the word-processing program used to prepare this document (Microsoft Word).

Dated: November 21, 2025

Respectfully submitted,

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CERTIFICATE OF SERVICE ON PATENT OWNER
UNDER 37 C.F.R. § 42.105

Pursuant to 37 C.F.R. §§ 42.6(e) and 42.105(b), the undersigned certifies that on November 21, 2025, a complete and entire copy of this Petition for *Inter Partes* Review and Exhibits were provided via Federal Express to the Patent Owner by serving the correspondence address of record for the '763 Patent:

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Further, a courtesy copy of this Petition for *Inter Partes* Review was sent via email to Patent Owner's litigation counsel:

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