

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TAIWAN SEMICONDUCTOR
MANUFACTURING COMPANY LTD. and APPLE INC.
Petitioners

v.

MYW SEMITECH, LLC,
Patent Owner

U.S. Patent No. 11,538,763
Issue Date: December 27, 2022

Title: CHIP PACKAGE

Inter Partes Review No. IPR2026-00066

PATENT OWNER'S RESPONSE

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Other Authorities

37 C.F.R. §42.104(b)(4).....22, 23, 65, 66

PATENT OWNER'S EXHIBIT LIST

Exhibit No.	Description
2001	U.S. Patent No. 9,615,453
2002	Information Disclosure Statement for U.S. Application No. 17/929,180 dated December 21, 2023
2003	[SEALED] Email chain between Richard Juang, counsel for MYW Semitech, and Daniel Richards, counsel for Apple Inc., regarding production of materials
2004	[SEALED] Defendant Apple Inc.'s First Supplemental Responses to Plaintiff MYW Semitech, LLC's First Set of Interrogatories (Nos. 1-12)
2005	[SEALED] Email chain between Richard Juang, counsel for MYW Semitech, and Daniel Richards, counsel for Apple Inc., regarding availability of source code
2006	[SEALED] Email chain between Richard Juang and Peter Yang, counsel for TSMC, regarding inventorship.
2007	Oral Order for Motion to Stay Pending <i>Inter Partes</i> Review, <i>MYW Semitech, LLC v. Apple Inc.</i> , 1-25-cv-00504 (DDE) Dkt. 68 (January 21, 2026)
2008	Stipulation and [Proposed] Order to Amend Scheduling Order, <i>MYW Semitech, LLC v. Apple Inc.</i> , 1-25-cv-00504 (DDE) Dkt. 58 (December 3, 2025)
2009	Apple Inc.'s Infringement Contentions, <i>MYW Semitech, LLC v. Apple Inc.</i> , 1-25-cv-00504 (DDE) (January 9, 2026)
2010	Agreed Stipulation Regarding the Discovery of Electronically Stored Information, <i>MYW Semitech, LLC v. Apple Inc.</i> , 1-25-cv-00504 (DDE) Dkt. 39 (October 14, 2025)
2011	Revision to Rules of Practice Before the Patent Trial and Appeal

	Board, 90 Fed. Reg. 48,335 (proposed Oct. 17, 2025) (to be codified at 37 C.F.R. pt. 42).
2012	Declaration of Richard Juang
2013	Default Protective Order
2014	Apple Inc.’s Proposed Constructions in <i>MYW Semitech, LLC v. Apple Inc.</i> , C.A. No. 25-504-RGA-EGT (Feb. 12, 2026)
2015	Joint Claim Construction Chart in <i>MYW Semitech, LLC v. Apple Inc.</i> , C.A. No. 25-504-RGA-EGT (Feb. 26, 2026)
2016	Defendant Apple Inc.’s Answering Claim Construction Brief
2017	Defendant Apple Inc.’s Initial Invalidity Contentions (Cover Document)
2018	Declaration of Professor David S. Ricketts
2019	CV of Professor David S. Ricketts
2020	Deposition Transcript of Stanley Shanfield, Ph. D., dated July 14, 2026.
2021	<i>Coefficient of Thermal Expansion (CTE)</i> , BYU Integr. Microfabrication Lab, https://cleanroom.byu.edu/cte_materials (last visited Aug. 6, 2026).
2022	Rogers Corp., <i>ULTRALAM® 3000 Liquid Crystalline Polymer Circuit Material</i> , Double-Clad Laminates, Data Sheet No. RF1.3000, Publication No. 92-125 (rev. May 10, 2011).
2023	Yoon, J., Shin, T., Kim, D. et al. Enhancing bonding strength of the electroplated Cu pillars for semiconductor package by controlling grain orientation. <i>Sci Rep</i> 16, 9814 (2026).
2024	<i>Excerpts from CRC Handbook of Chemistry and Physics</i> , 2005, < http://www.hbcnpnetbase.com >, CRC Press, Boca Raton, FL, 2005.

I. INTRODUCTION

The claims of the '763 Patent are directed to specific configurations of semiconductor chip packages. These specific configurations are necessary and beneficial to minimize the size of the semiconductor chip packages while ensuring the highest possible performance. EX1001 ['763 Patent], 1:27-44.

Because the claimed configurations are detailed and specific, none of the asserted references teach or suggest the claimed invention, either alone or in combination. The Petition relies on combinations of six different references. Pet., 2. But even then, the proposed combinations do not map to the claimed configurations. As a result, the Petition's mapping to the claims distorts the references relied upon or maps the references inconsistently within the same challenged claim.

For example, limitation 1(e)(i) requires that the "first semiconductor chip comprises a third metal interconnect." EX1001 ['763 Patent], cl. 1. The Petition alleges Sundaram's figure 3 memory chip is the claimed semiconductor chip and that the memory chip comprises solder bumps that are allegedly the claimed third metal interconnect. But the solder bumps disclosed in Sundaram are external to said memory chip. Thus, Sundaram's memory chip does not "comprise" the solder bumps as required by the claims.

Similarly, limitation 1(e)(ii) requires a “Third Metal Interconnect Comprises a Third Metal Layer on Said First Metal Pad and a Third Copper Layer Over Said Third Metal Layer, Wherein Said Third Copper Layer Has a Thickness Between 5 and 30 Micrometers.” EX1001 [’763 Patent], cl. 1. Because none of the metal layers disclosed in the prior art meet this limitation, the Petition attempts to combine multiple discrete layers from Lin-191 into a single layer. But, as discussed below, the different layers in Lin-191 are separate and would not be combined by a POSITA into a single layer.

Grounds 2A through 2C (based on Yu) have similar deficiencies. For example, limitation 1(e) requires “a first semiconductor chip under said first interconnection scheme, wherein said first semiconductor chip comprises a third metal interconnect on a first metal pad of said first semiconductor chip.” EX1001 [’763 Patent], cl. 1. Yu does not disclose this limitation because the structure the Petition identifies as the alleged “third metal interconnect” is a connector that joins the chip to the package metallization, not a layered interconnect on a metal pad of the chip.

For these and the other reasons described in more detail below, the Petition fails to demonstrate by a preponderance of the evidence that any challenged claim is unpatentable.

II. BACKGROUND

A. Procedural History

Patent Owner (“PO”) is asserting the ’763 Patent (along with U.S. Patent Nos. 11,107,768 (“the ’768 Patent”) and 11,894,306 (“the ’306 Patent”)) against Petitioner Apple in *MYW Semitech, LLC v. Apple Inc.*, Case No. 1:25-cv-00504. (D. Del. 2025). That case was filed on April 24, 2025.

On November 21, 2025, Petitioners filed this IPR, along with IPR2026-00065 and IPR2026-00067 challenging the ’768 and ’306 Patents, respectively. The district court litigation was stayed on June 16, 2026 pending resolution of these IPRs. EX1162.

B. The ’763 Patent

The ’763 Patent was filed as application no. 17/372,459 on July 11, 2021. The ’459 application is a continuation of application No. 16/752,650 on January 26, 2020, which issued as the ’768 Patent. The ’650 application is a continuation of application No. 15/261,956, filed on September 11, 2016, now Patent No. 10,622,310, which is a continuation-in-part of application No. 14/036,256, filed on September 25, 2013, now Patent No. 9,615,453. The ’763 Patent claims priority to provisional application No. 61/705,649, filed on September 26, 2012, and provisional application No. 62/219,249, filed on September 16, 2015.

The '763 Patent discloses a “method and structure to manufacture a glass substrate” and a “chip building a system on the glass substrate.” *See* EX1001, 1:20-23. EX2018 [Ricketts Decl.], ¶74. The glass substrate comprises “multiple metal conductors through in said glass substrate and multiple metal bumps are between said glass substrate and said display panel substrate, wherein said one of said metal conductors is connected to one of said contact pads through one of said metal bumps.” *Id.*, Abstract.

1. Prosecution History

The '459 application that issued as the '763 Patent was filed on July 11, 2021. EX1001 ['763 Patent], (21)-(22). During prosecution, the Applicant filed five preliminary amendments. As discussed below, three of these amendments amended the claims to claim the embodiment disclosed at Fig. 6l and the related disclosure in the specification. '763 Patent Fig. 6l is shown below:

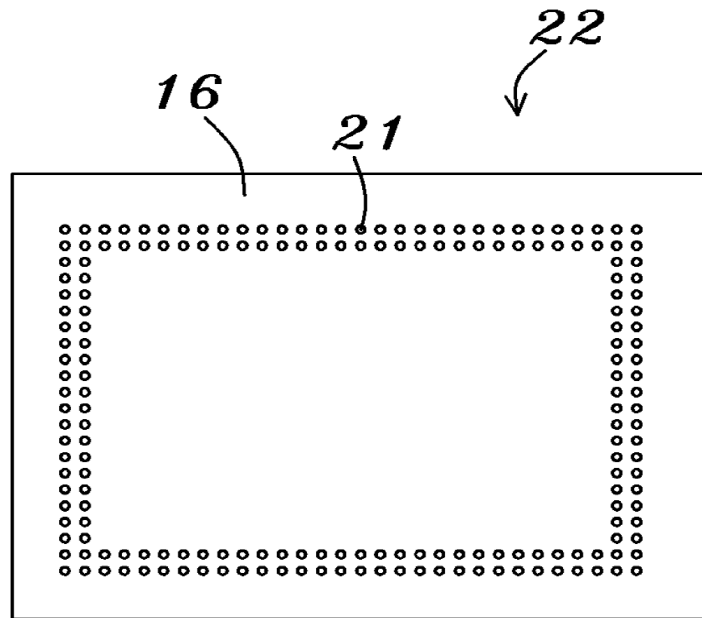


Fig. 6l

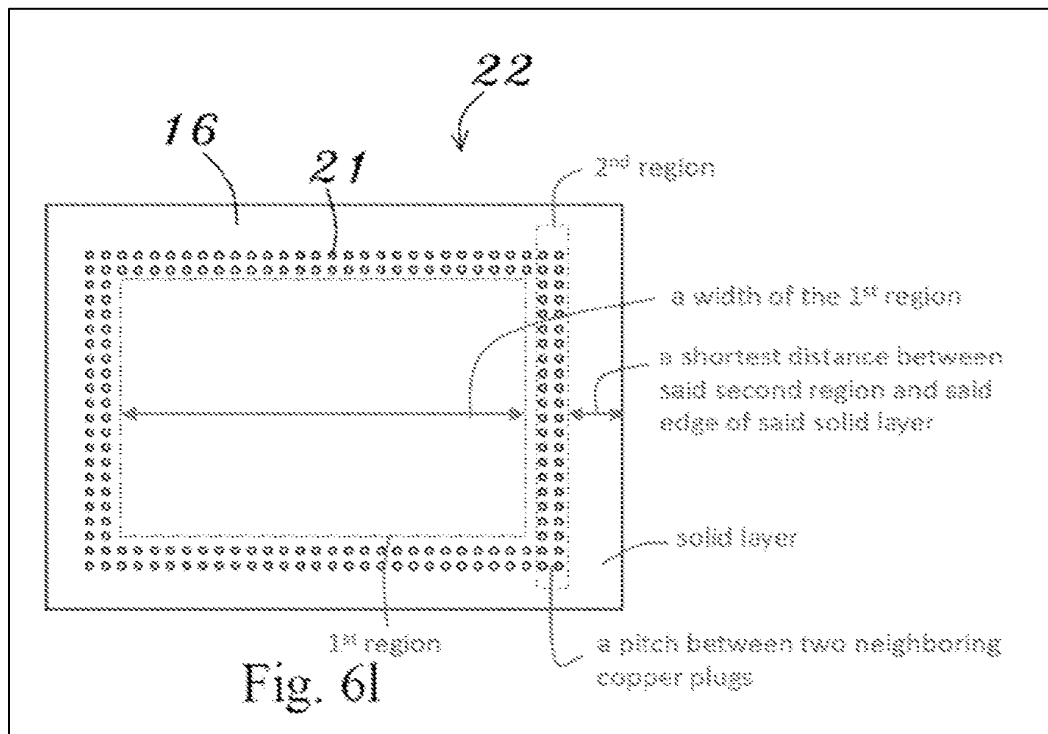
EX1001 ['763 Patent], Fig. 6l. Figure 6l “illustrate[s] a top view of the 1st process of forming the glass substrate [16], in accordance with the present disclosure.” *Id.*, 3:11-13. In Fig. 6l, “the metal plugs 21 are arranged on the side portion of the second substrate 22.” *Id.*, 8:4-7.

On July 12, 2021, the Applicant amended pending claim 1 such that the limitation “two peripheral regions on two sides of said central region” was amended to “two peripheral regions on two sides of said central region respectively” and amended pending claim 16’s limitation “a shortest distance between one of said third copper plugs and an edge of said solid layer” was

amended to “that of one of said peripheral regions in the same direction”. EX1002 [FH], 237. In both cases, the Applicant cited Fig. 6l for support. *Id.*

On July 17, 2021, the Applicant amended further amended pending claim 1 such that the terms “first” and “two peripheral regions on two sides of said central region respectively” were amended to “second” and “a second region, wherein a first region has a width greater than that of said second region in the same direction” *Id.*, 246. Simultaneously, for pending claim 16, the term “central” was amended to “first”, and the limitation “wherein said central region has a largest dimension greater than that of one of said peripheral regions in the same direction” was cancelled. *Id.* In all cases, the Applicant cited Fig. 6l for support. *Id.*

On November 26, 2021, the Applicant amended pending claim 1 such that “the conditions ‘wherein said solid layer comprises a first region and a second region between said first region and an edge of said solid layer’ and ‘wherein said first region has a width greater than a shortest distance between said second region and said edge of said solid layer’ are added”. EX1002 [FH], 272. The Applicant again relied on Fig. 6l for support, and even provided an annotated version of Fig. 6l (below) explaining where the support was to be found:



Id. Notably, the Applicant indicated the 1st region was the region inside the rectangle formed by metal plugs 21.

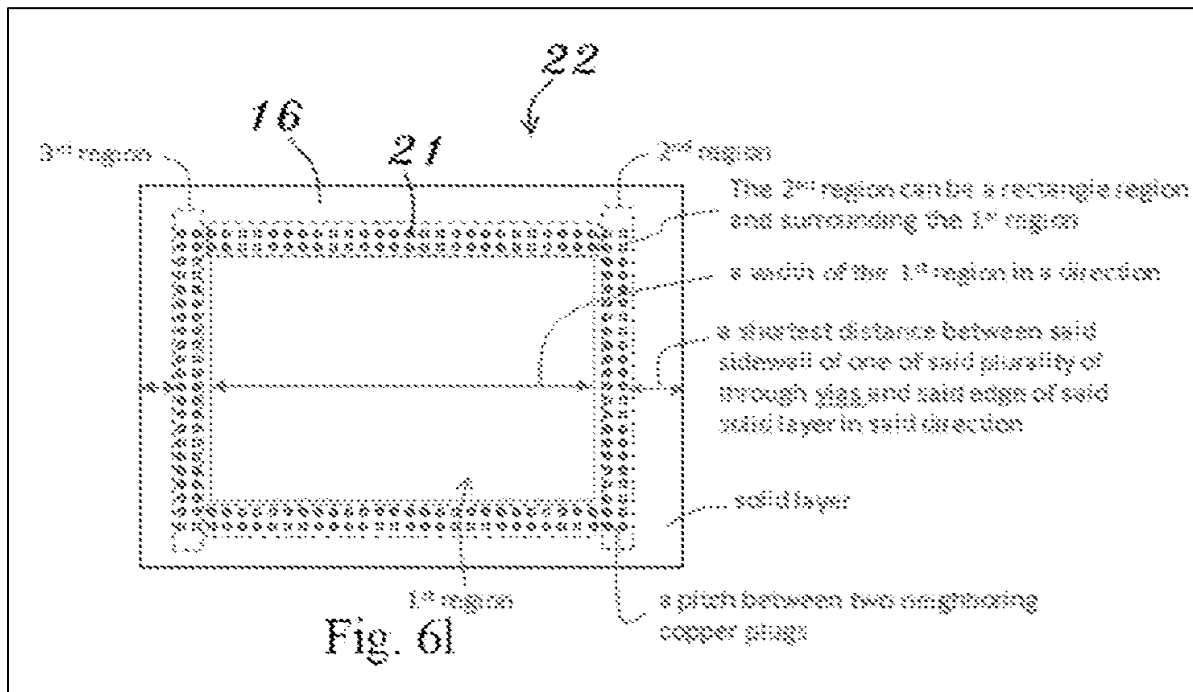
After an additional amendment on April 4, 2022 unrelated to the claimed first and second regions (*id.*, 283), on September 21, 2022, the Examiner allowed the claims. *Id.*, 294-295. The Examiner explained that the pending independent claims “are allowable because the closest prior art does not appear to disclose, alone or in combination, the limitations of material and structure of the chip package in combination with the other required elements.” *Id.*, 294.

On October 14, 2022, the Applicant submitted a request for continued examination and made further amendments to the claims. EX1002 [FH], 351-361.

The Applicant submitted a number of amendments citing support from Fig. 6l. *Id.*, 359. The Applicant explained its amendment to claim 1 as follows:

For the currently-amended claim 1, the conditions “wherein said first region has a width in a direction greater than a shortest distance between said sidewall of one of said plurality of through vias and said edge of said solid layer in said direction and greater than a pitch between two neighboring copper plugs of said plurality of copper plugs” is amended to clarify the conditions in the claim 1, wherein the amendments/conditions are believed to be supported in Fig. 6l in the Specification and Drawings.

Id. The Applicant again provided an annotated version of Fig. 6l (below) further explaining the support:



Id., 360. Again, the Applicant explained that the claimed 1st region is the area inside the rectangle formed by metal plugs 21.

On October 31, 2022, the Examiner allowed the claims, explaining that the independent claims “are allowable because the closest prior art does not appear to disclose, alone or in combination, the limitations of material and structure of the chip package in combination with the other required elements of” the independent claims. *Id.*, 367.

2. Claims of the ’763 Patent

The ’763 Patent has 2 independent claims (1 and 18) and 21 claims that depend from claims 1 and 18. The claims are directed to chip packages using silicon layers with specific layouts of metal plugs and interconnects. EX2018 [Ricketts Decl.], ¶82.

C. Petitioners’ Cited References

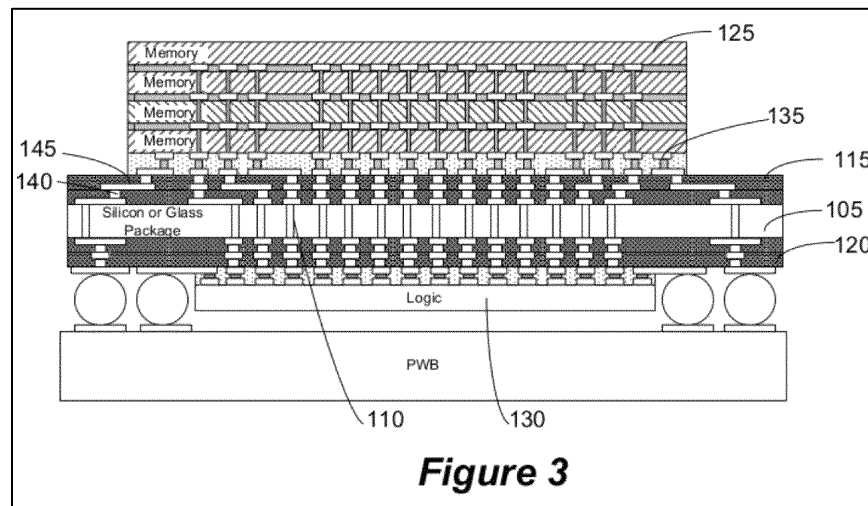
The Petition advances the following seven grounds:

Grounds	Claims Challenged	35 U.S.C. §	References
<u>1A</u>	1-12, 14, 16-21, 23	103	Sundaram (EX1004) and Lin-191 (EX1005)
<u>1B</u>	13, 15	103	Sundaram, Lin-191, and Lin-863 (EX1007)
<u>1C</u>	22	103	Sundaram, Lin-191, and Lin-691 (EX1008)
<u>1D</u>	22	103	Sundaram, Lin-191, and Shenoy (EX1011)
<u>2A</u>	1-5, 7-12, 14-15, 17	103	Yu (EX1010) and Lin-191
<u>2B</u>	6, 16, 18-21, 23	103	Yu, Lin-191, and Sundaram
<u>2C</u>	13	103	Yu, Lin-191, and Lin-863

Pet., 2.

1. Sundaram (EX1004)

Sundaram is directed to a “3D interconnect structure comprising an ultra-thin interposer having a plurality of ultra-high density through-via interconnections defined therein.” EX1004, Abstract. Sundaram figure 3 (relied on in the Petition) shows Sundaram’s interconnect structure comprising an interposer defining a plurality of through vias:



Id., Fig. 3. “[T]he interconnect structure comprises an interposer 105 having a first side 115 and a second side 120.” *Id.*, 5:47-48. “A plurality of ultra-small through vias 110 can be defined within the interposer 105 such that each of the through vias 110 extends from the first side 115 to the second side 120 of the interposer 105.” *Id.*, 6:6-9. These “through vias 110 are ultra-small and can range from about 1-25 micrometers in diameter at about 3-50 micrometers in pitch.” *Id.*, 6:11-13. “A first electronic device 125 can be attached to the first side 115 of the interposer 105 and a second electronic device 130 can be attached to the second side 120 of the interposer 105.” *Id.*, 6:34-36. “[E]lectronic devices having different I/O pad layouts and sizes can also be connected through the use of blind vias 140 and conductor traces 145 defined within polymer-metal redistribution layers deposited on the first side 115 and second side 120 of the interposer 105.” *Id.*, 6:62-67.

2. Lin-191 (EX1005)

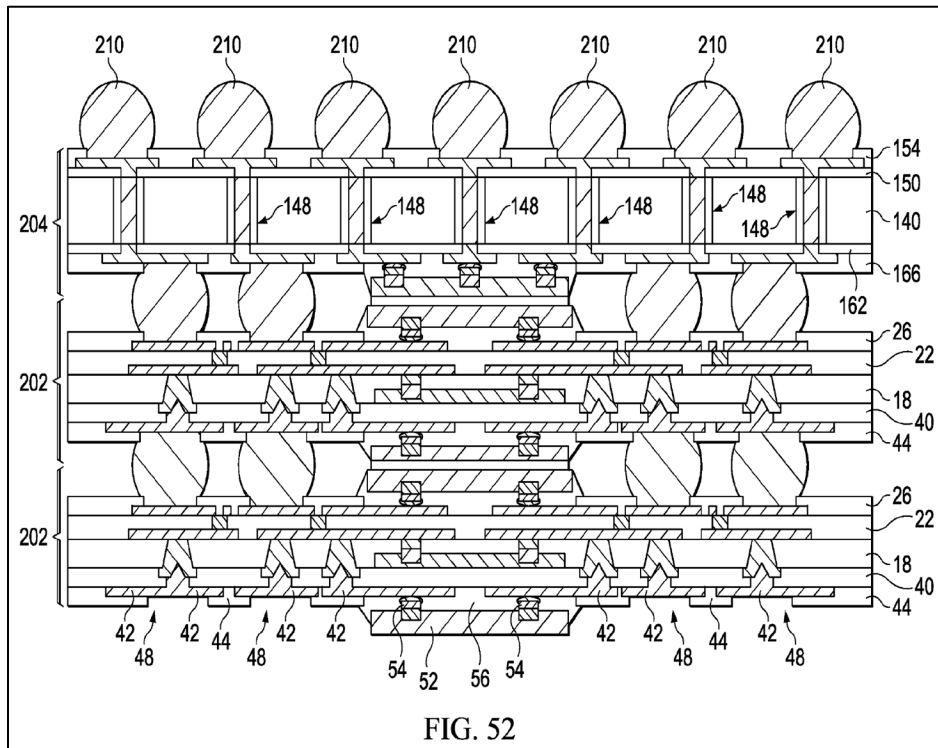
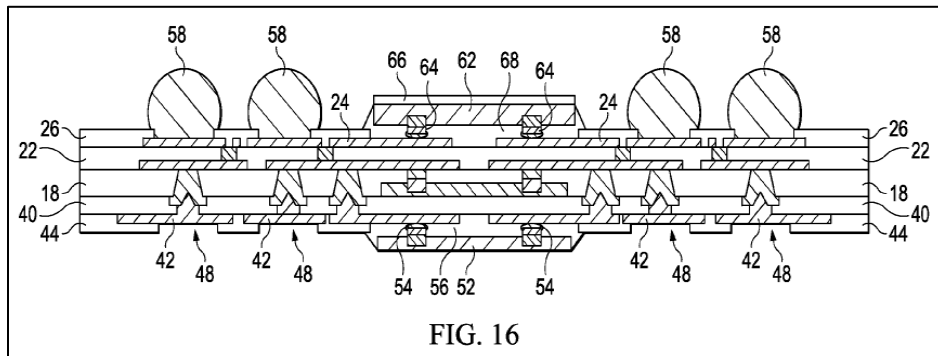
Lin-191 discloses “system-in packages” comprising multi-layer chips in a multi-layer polymer structure. EX1005, Abstract. Lin-191 explains that:

System-in packages, or multichip modules, are described which can include multi-layer chips in a multi-layer polymer structure, on-chip metal bumps on the multi-layer chips, intra-chip metal bumps in the multi-layer polymer structure, and patterned metal layers in the multi-layer polymer structure. The multi-layer chips in the multi-layer polymer structure can be connected to each other or to an external circuit through the on-chip metal bumps, the intra-chip metal bumps and the patterned metal layers. The system-in packages can be connected to external circuits through solder bumps, meal bumps or wirebonded wires.

Id.

3. Yu (EX1010)

Yu discloses a package-on-package (POP) structure having at least one package comprising one die being disposed in a core material between first and second surfaces of the core material. EX1010, Title. The Petition relies primarily on Yu figures 16 and 52:



Id., Figs. 16, 52. Yu provides limited discussion of these figures. Yu figure 16 is an “example of a second portion of a process for forming a package according to an embodiment.” *Id.*, 2:1-3. Yu explains that “In FIG. 16, an underfill material 68, such as liquid epoxy, deformable gel, silicon rubber, the like, or a combination thereof, is dispensed and cured between the third die 62 and the front

side of the package, such as between the third die 62 and the second metallization layer 24.” *Id.*, 4:67-5:4.

Yu figure 52 shows a “step to form electrical connectors on the PoP structure of FIG. 51.” *Id.*, 2:15-16. “In FIG. 52, connectors 210, such as BGA balls, formed coupled to a metallization layer on a front side of the interposer of the interposer package 204, similar to FIG. 50.” *Id.*, 8:36-39.

4. Lin-863 (EX1007)

Lin-863 describes a fan-out wafer-level chip-scale package having a substrate 226 on which “conductive TMV[s] [through-mold vias] 225” and a “semiconductor die 124” are disposed. EX1007 [Lin-863], 12:33-42, 14:45-46, Figs. 9a-9b.

5. Lin-691 (EX1008)

Lin-691 describes through-substrate vias formed by a diffusion-barrier layer, a “thin seed layer . . . formed on the diffusion barrier layer,” and a “metallic material” on the seed layer, where the seed layer is “silver” and the metallic material is “copper.” EX1008 [Lin-691], [0005], [0019]-[0021].

6. Shenoy (EX1011)

Shenoy describes a glass substrate with through-glass via holes conformally coated with a “seed layer 314” that includes Ag, over which a “plated metal 316 . . . can include Cu.” EX1011 [Shenoy], [0053]-[0055].

III. LEVEL OF ORDINARY SKILL

Petitioners allege the following level of ordinary skill:

A POSITA at the time of the '763 Patent would have had at least a bachelor's degree in electrical engineering, materials science, or physics (or an equivalent degree), and at least two years of experience in semiconductors or semiconductor manufacturing. A master's degree or Ph.D. in a relevant field may substitute for some work experience or vice versa. Additional education or experience might substitute for the above requirements.

Pet., 1. For the purposes of this POR, PO does not dispute Petitioners' level of ordinary skill. EX2018 [Ricketts Decl.], ¶¶44-45.

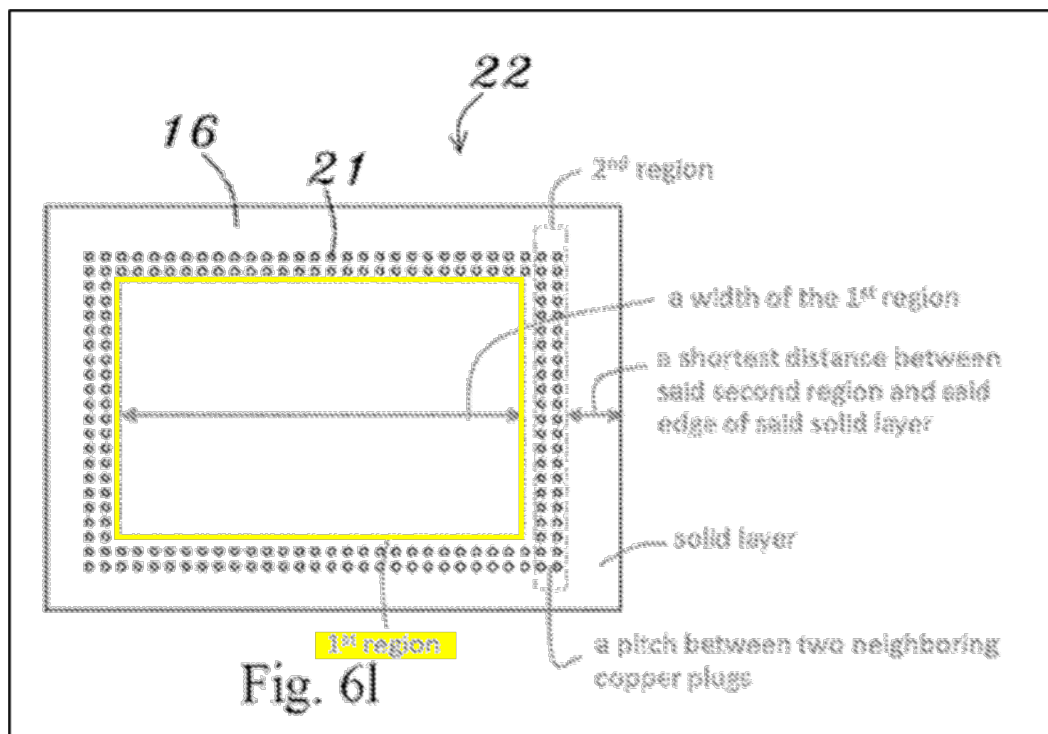
IV. CLAIM CONSTRUCTION

Petitioners allege that claim construction is unnecessary for this IPR. Pet., 2.

PO agrees that no construction is necessary for the claim terms except for the claim term "first region." EX2018 [Ricketts Decl.], ¶47. The prosecution history for the '763 Patent clearly and unmistakably disclaimed any first region that contains metal plugs. *Thorner v. Sony Comput. Entm't Am. LLC*, 669 F.3d 1362, 1366-67 (Fed. Cir. 2012) ("To constitute disclaimer, there must be a clear and unmistakable disclaimer."). During prosecution, the Applicant was clear that the "first region" is a region that does not include metal plugs, and thus disclaimed

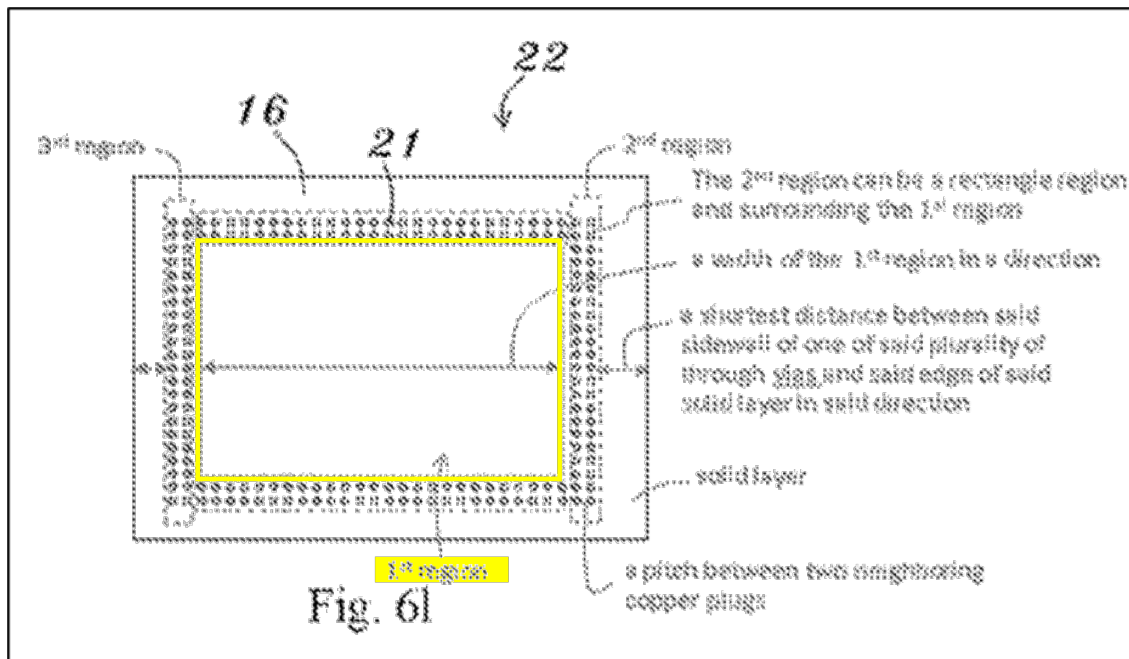
any claim interpretation where the claimed “first region” includes metal plugs. *See* §II.B.1, above.

During prosecution, the Applicant, relying on '763 Patent Fig. 6l for support, identified that the claimed first region is the region inside Fig. 6l's rectangle of metal plugs (shown in yellow below):



EX1002 [FH], 272. The annotation is clear that the 1st region has no metal plugs.

In the amendments in Applicant's request for continued examination, the Applicant made the same point, again identifying the 1st region as the region in Fig. 6l free of metal plugs located inside of the rectangle formed by metal plugs 21 (in yellow):



Id., 360. Applicant cited only Fig. 6l in support of this argument (*Id.*, 272, 360). Thus, the Applicant clearly and unambiguously intended the first region to be a region that does not include metal plugs. EX2018 [Ricketts Decl.], ¶49.

Other portions of the prosecution history support this disclaimer. For example, in a July 16, 2021 preliminary amendment, the Applicant replaced the term “central region” with the term “first region” in pending claims 1 and 16. EX1002 [FH], 241, 246. The Applicant cited only Fig. 6l for support of this amendment. *Id.*, 246. Thus, Applicant clearly intended the first region to be the central region of Fig. 6l that does not include any metal plugs. *Id.*; EX2018 [Ricketts Decl.], ¶50.

Claim 1 further confirms the Applicant’s meaning. While claim 1 claims “a plurality of copper plugs in a plurality of through vias in said *second* region”, it

does not claim any copper (or metal) plugs in the *first* region. EX1001 ['763 Patent], cl. 1. Thus, the Applicant clearly intended the metal plugs to be part of the second region and that the claimed first region be a region that is free from metal (e.g., copper) plugs. EX2018 [Ricketts Decl.], ¶51.

Claim 15 further confirms the disclaimer. Claim 15 requires “the chip package of claim 1, wherein no any copper plug in said first region.” EX1001 ['763 Patent], cl. 15. Thus, claim 15 further confirms that the first region has no metal (e.g., copper) plugs. EX2018 [Ricketts Decl.], ¶52.

Accordingly, the intrinsic record is clear and unmistakable that the Applicant disclaimed a first region with any metal plugs.

V. PETITIONERS FAIL TO DEMONSTRATE BY A PREPONDERANCE OF THE EVIDENCE THAT ANY OF THE CHALLENGED CLAIMS ARE UNPATENTABLE

The claims of the '763 Patent are directed to specific configurations of semiconductor materials useful for semiconductor chip packages. The Petition fails to demonstrate that any of the prior art, either alone or in combination, discloses the specific configurations required by the claims.

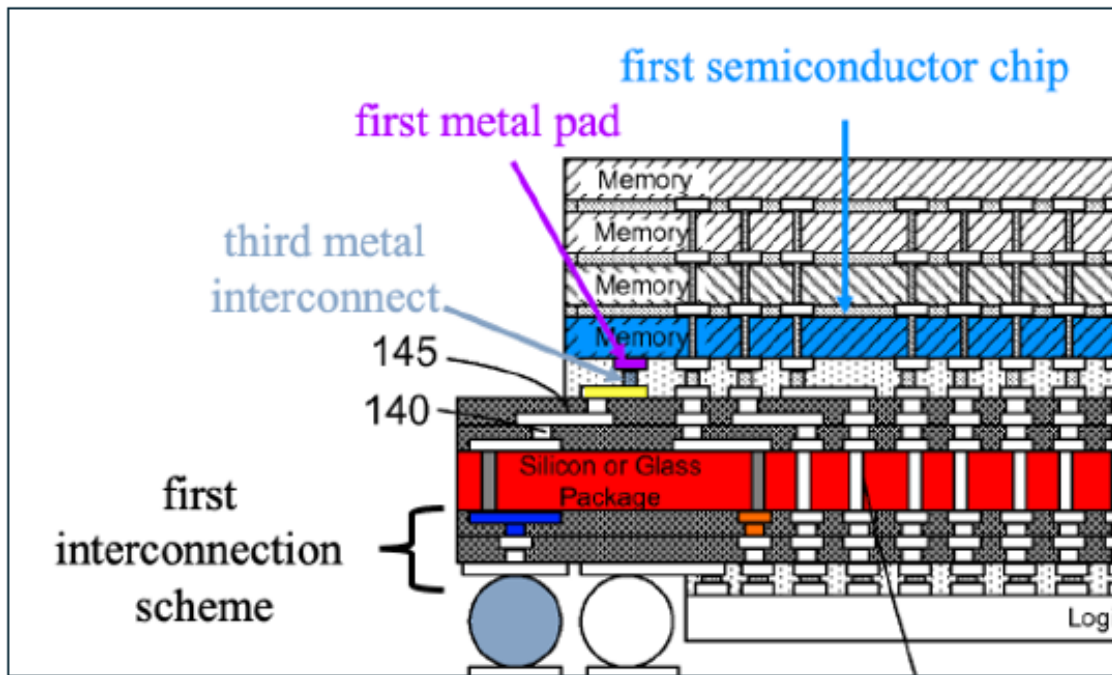
A. Ground 1A (Sundaram and Lin 191)

1. Sundaram and Lin-191 Fail to Teach or Suggest a “First Semiconductor Chip Comprises a Third Metal Interconnect” or “Third Metal Interconnect on a First Metal Pad of Said First Semiconductor Chip.”

a) Sundaram’s memory chip does not comprise a third metal interconnect or third metal interconnect on a first metal pad of said first semiconductor chip.

Limitation 1(e)(i) requires that the “first semiconductor chip comprises a third metal interconnect.” EX1001 [’763 Patent], cl. 1. This limitation is not disclosed by Sundaram because Sundaram’s alleged semiconductor chip does not comprise or include Sundaram’s alleged third metal interconnect. EX2018 [Ricketts Decl.], ¶95.

Petitioners argue that Sundaram Fig. 3’s “die pads 135 [that are formed on the first 115 and second sides 120 of the interposer 105] can electrically connect devices using solder, copper bumps with solder caps, [and] copper to copper bonding,’ each of which teaches a third metal interconnect.” Pet., 22. (citing EX1004, 6:29-33). In particular, the Petition states that “[i]n FIG. 3, the third metal interconnect is a bump on the metal pad.” Pet., 22. That is, as shown below, the Petition alleges that the solder/bumps (gray) (located on top of the die pad 135 (yellow) of interposer 105) is the claimed “third metal interconnect”:



Pet., 23 (excerpting and annotating EX1004 [Sundaram] Fig. 3 (PO added yellow annotation showing die pad 135)).

The structure that the Petition identifies as the claimed “first semiconductor chip” (blue) does not comprise the alleged “third metal interconnect” (bump/solder shown in gray). EX2018 [Ricketts Decl.], ¶97. This is because the bumps/solder are not part of the memory—the alleged “first semiconductor chip” (shown in blue).

Instead, the bumps (or solder) (the alleged “third metal interconnect”) are formed *on the die pad 135 of the interposer 105* to electrically connect devices to the interposer 105. EX1004, 6:29-33. And Sundaram specifically states that the die pads 135 are associated *with the interposer 105*: “[t]he through vias 110 can be

metalized in such a way that the metallization provides die pad surfaces 135 that correspond to each of the vias 110 on both the first side 115 and the second side 120 of the interposer 105.” EX1004 [Sundaram], 6:23-25; *see also* EX1004, 6:29-33. Thus, Sundaram’s bumps/solder are part of or associated with the interposer 105, not the alleged “first semiconductor chip.” EX2018 [Ricketts Decl.], ¶98.

Indeed, Haba (a reference on which Petitioners rely in co-pending IPR2026-00065) demonstrates that solder/bumps (as described in Sundaram) are not considered part of the alleged “first semiconductor chip.” EX2018 [Ricketts Decl.], ¶99. Instead, solder/bumps (as described in Sundaram) are structures that are separate from a semiconductor chip and that are used to connect other components to contacts/pads of the semiconductor chip. EX2018 [Ricketts Decl.], ¶99. EX1161 [Haba], 6:39-47; 7:42-56; 8:27-29; 11:33-35.

Limitation 1(e)(i) requires “wherein said first semiconductor chip comprises a third metal interconnect on a first metal pad of said first semiconductor chip.” EX1001 [’763 Patent], cl. 1. Based on Sundaram’s disclosure, bump/solder (gray) is formed on a die pad 135 of the interposer 105 and, thus, is not on a metal pad of the semiconductor chip. The Petition identifies the “first metal pad” as the component shown in purple above and memory (blue) of electronic device 125 as the claimed “first semiconductor chip.” Pet., 22. Sundaram (and the Petition) therefore places the alleged “third metal interconnect” on the interposer 105 and

the alleged “first metal pad” on the alleged semiconductor chip. EX2018 [Ricketts Decl.], ¶100. Thus, the alleged “third metal interconnect” is not on the alleged “first metal pad.” The alleged “third metal interconnect” is on the die pad 135 (yellow) of the interposer 105. In addition, the “first semiconductor chip” does not comprise a third metal interconnect because the memory (the alleged semiconductor chip) does not comprise the bump/solder (gray) (the alleged third metal interconnect) – the bump/solder (gray) is part of the interposer. EX2018 [Ricketts Decl.], ¶100.

The mismatch described above—the alleged “third metal interconnect” on the interposer 105 and the alleged “first metal pad” on the alleged semiconductor chip—follows at least partially from the fact that Sundaram does not describe the pads or interconnects of electronic device 125. The Petition does not identify any disclosure of those structures and certainly does not explain the component shown above or what it is made of. EX2018 [Ricketts Decl.], ¶101. The Petition states instead that “[a] POSITA would understand that device 125 also has die pads . . . such that an electrical connection is made between interposer 105 and device 125.” Pet., 22; EX1003 [Shanfield Decl.], ¶162. Thus, the Petition is attempting to supply the claimed relationship between the “third metal interconnect” and “first metal pad” through background knowledge of a POSITA. EX2018 [Ricketts Decl.], ¶101. This is impermissible. 37 C.F.R. §42.104(b)(4) “The petition must

specify where each element of the claim is found in the prior art patents or printed publications relied upon”); July 31, 2025 memorandum on Enforcement and Non-Waiver of 37 C.F.R. §42.104(B)(4) (“Background Knowledge Memo”).¹

Dr. Shanfield’s declaration confirms that this mismatch rests on assumption rather than on any disclosure in Sundaram. EX2018 [Ricketts Decl.], ¶102. Dr. Shanfield does not identify any Sundaram teaching of a pad or an interconnect on electronic device 125. He states only that “[a] POSITA would understand that, like interposer 105, first electronic device 125 (first semiconductor chip) also has die pad[s],” and he supports the existence of that pad not with Sundaram but with other references—for example EX1095. EX1003 [Shanfield Decl.], ¶¶162, 165. Reasoning by analogy to the interposer, and by reference to what pads other art shows, is not a teaching that Sundaram’s electronic device 125 comprises the claimed “first metal pad,” or the claimed “third metal interconnect” on it. EX2018 [Ricketts Decl.], ¶102.

¹ *Available at*

https://www.uspto.gov/sites/default/files/documents/aapa_memo_final__signed.pdf?utm_campaign=subscriptioncenter&utm_content=&utm_medium=email&utm_name=&utm_source=govdelivery&utm_term=

The Sundaram passage that the Petition relies on is directed to the interposer. Sundaram states that “[t]he die pads 135 that are formed on the first 115 and second sides 120 of the interposer 105 can electrically connect devices using solder, copper bumps with solder caps, copper to copper bonding, adhesive bonding, metallurgical bonding, non-conductive bonding, or combinations thereof.” EX1004 [Sundaram], 6:29-33. That sentence lists methods for joining a device to the die pads *of the interposer*. EX2018 [Ricketts Decl.], ¶103. It does not describe any structure formed on electronic device 125 or the memory shown in blue above, and it does not describe the layered construction required by limitation 1(e)(ii).

Thus the Petition’s combination of Sundaram and Lin-191 fails because it does not teach or suggest the “first semiconductor chip comprises a third metal interconnect” or a “third metal interconnect on a first metal pad of said first semiconductor chip” as required by limitation 1(e)(i).

b) Lin-191 does not teach or suggest limitation 1(e)(i).

Petitioners do not adequately allege that Lin-191 teaches or suggests the “first semiconductor chip comprises a third metal interconnect.” EX1001 [’763 Patent], cl. 1. Although Petitioners include a section on Lin-191 for Ground 1A limitation 1(e)(i), the statements in that section are directed to the claimed “metal

pad,” not the claimed “third metal interconnect.” Pet., 24-25. The section does not allege Lin-191 teaches or suggests the “first semiconductor chip comprises a third metal interconnect.” EX2018 [Ricketts Decl.], ¶105.

c) The Petition’s motivation to combine Lin-191 and Sundaram is conclusory and wrong.

Petitioners allege there is a motivation to combine Lin-191 and Sundaram because the modification “is the application of a known technique (metal pads) to a known device (Sundaram’s semiconductor chip) ready for improvement to yield the predictable result of Sundaram’s device 125 having a first metal pad.” Pet. 25. This statement offers no substantive explanation as to why the structure (shown in purple above) required the application of the Lin-191’s metal pad teachings. EX2018 [Ricketts Decl.], ¶106. It presupposes that one would modify Sundaram without identifying any issues, shortcomings, or reasons to combine the references. EX2018 [Ricketts Decl.], ¶106.

Sundaram and Lin-191 reflect fundamentally different engineering approaches to building a multi-chip structure, and a POSITA would not have been motivated to merge them. EX2018 [Ricketts Decl.], ¶107. Lin-191 teaches a chip-first, tier-by-tier build in which the substrate is a work-in-progress rather than a finished component: chips carrying on-chip metal bumps are adhered to the substrate, encapsulated, and then polished or ground to expose the bumps before

interconnections are formed, with the sequence repeated for each successive tier. EX1005, ¶[0009]. Consistent with that approach, Lin-191 does not form its through-substrate connections until late in the process—substrate 110 is first thinned to as little as 1 to 10 micrometers by mechanical grinding or chemical-mechanical polishing of its backside, EX1005, ¶[0290], and only then are through holes 16 and through-hole connections 17 formed from that newly exposed surface. EX1005, ¶¶[0292]–[0293]. Sundaram proceeds in the opposite order and for the opposite reason. Sundaram builds and electrically verifies its interposer before any die is attached, and describes this chip-last sequence as the mechanism by which its structure “alleviates the Known Good Die (KGD) concerns in 3DIC integration.” EX1004, 7:51-53, FIG. 6 (steps 605, 610, 615). Sundaram’s claims reinforce that its interposer is meant to be a completed, verifiable article, requiring test pads on both sides to permit testing of devices attached to either side. EX1004, cl. 21–22; EX2018 [Ricketts Decl.], ¶107.

A POSITA seeking the benefits Sundaram describes would have understood that those benefits depend on the interposer being finished and tested before die attachment, and would therefore have seen no advantage in placing that interposer into Lin-191’s process, where the substrate is deliberately left unfinished and is subsequently thinned, ground, and metallized from the backside after the chips are already in place. EX2018 [Ricketts Decl.], ¶107. The features a POSITA would

have been looking to Sundaram for—Sundaram’s through-vias, its redistribution layers, and its test pads—are the same features Lin-191’s later processing steps would have been expected to disturb. EX2018 [Ricketts Decl.], ¶107. A POSITA would not have expected the combined arrangement to retain them or to function as Sundaram describes. EX2018 [Ricketts Decl.], ¶107.

Conversely, a POSITA starting from Lin-191 and reordering its process to preserve Sundaram’s pre-tested interposer would have had to abandon the tiered, chip-first integration that Lin-191 identifies as its contribution, including the high routing density between chips that Lin-191 attributes to its fine-pitched on-chip and intra-chip metal bumps. EX1005, ¶¶[0010]–[0011]; EX2018 [Ricketts Decl.], ¶107. A POSITA would not have had a reason to make either change, or a reasonable expectation that the resulting structure would work as either reference intends. EX2018 [Ricketts Decl.], ¶107. Thus, there is no evidence that a POSITA would have a reason to combine the references.

**2. Sundaram and Lin-191 Do Not Teach or Suggest
“Wherein Said Third Metal Interconnect Comprises a
Third Metal Layer on Said First Metal Pad and a Third
Copper Layer Over Said Third Metal Layer, Wherein Said
Third Copper Layer Has a Thickness Between 5 and 30
Micrometers.”**

The Petition relies solely on Lin-191 for limitation 1(e)(ii). Pet., 26-27. As discussed below, Lin-191 does not teach or suggest this limitation.

a) Lin-191 does not teach or suggest “said third metal interconnect.”

As discussed above, the Petition fails to demonstrate that Sundaram teaches a “first semiconductor chip compris[ing] a third metal interconnect” because Sundaram’s memory chip does not comprise the solder/bumps alleged to be the claimed “said third metal interconnect.” EX2018 [Ricketts Decl.], ¶109.

Although the Petition alleges Lin-191’s bumps 710 are metal interconnects for limitation 1(e)(ii) (Pet., 26-27), the Petition does not rely on Lin- 191 as teaching or suggesting that Sundaram’s first semiconductor chip comprises the claimed third metal interconnect, cl. 1(e)(i). *Id*; EX2018 [Ricketts Decl.], ¶110. The Petition’s treatment of Lin-191 for limitation 1(e)(ii) is directed to the claimed “metal pad,” stating only that “Lin-191’s semiconductor chip 160 has ‘metal traces or pads 163’ that include ‘aluminum.’” Pet., 26. Lin-191 therefore does not remedy the deficiency in Sundaram identified above. *Supra*, §V.A.1.

b) Lin-191 does not teach or suggest “a third metal layer on said first metal pad and a third copper layer over said third metal layer.”

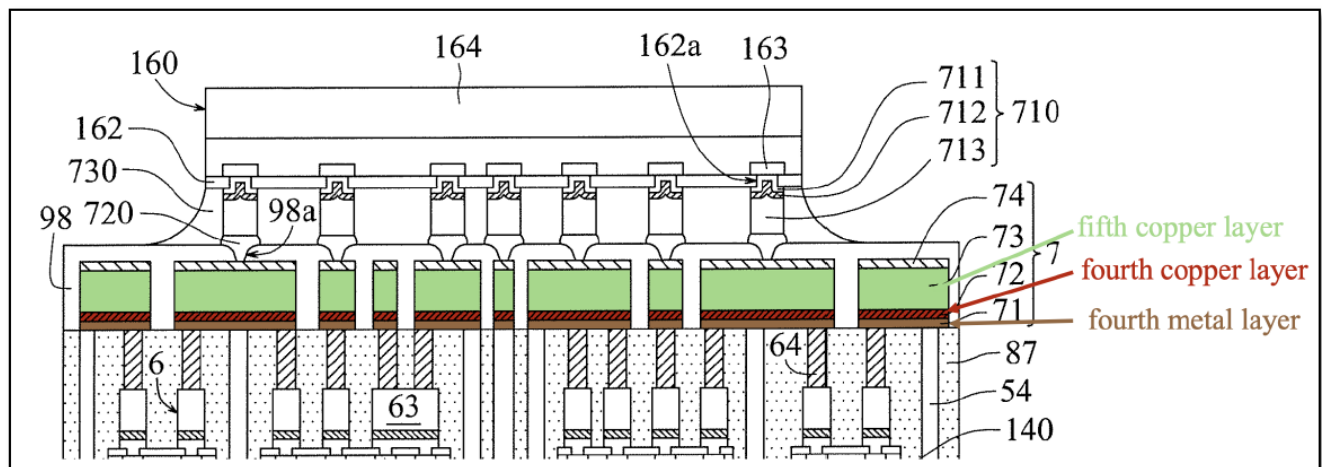
The Petition’s mapping of limitation 1(e)(ii) is inconsistent with the Petition’s own mapping of claim 7. EX2018 [Ricketts Decl.], ¶111. Claim 7 recites a three-layer interconnect and limitation 1(e)(ii) recites a two-layer interconnect. Petitioners assert that adhesion and seed layers are *two separate* layers for claim 7:

¶205. Adhesion layer 71 is a *metal* (e.g., titanium or nickel) and is thus a *fourth metal layer*. EX1005, [0260]-[0264]. Seed layer 72 is “a copper layer” on adhesion layer 71 and is thus a *fourth copper layer on said fourth metal layer*. EX1005, [0261]-[0264]. Metal layer 73 “can be...a copper layer...on the seed layer 72” and is thus a *fifth copper layer on said fourth copper layer*. EX1005, [0420].

Pet., 49 (citing EX1005 [Lin-191], [0260]-[0264], [0420]); EX1003 [Shanfield Decl.], ¶204.

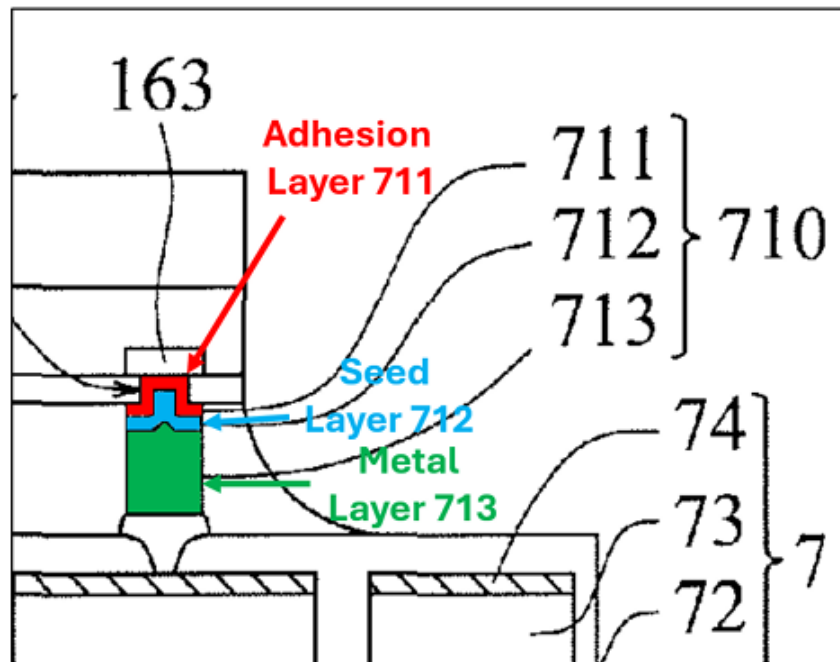
But, when it comes to limitation 1(e)(ii), Petitioners assert that adhesion and seed layers are *one* layer. Those two positions cannot both be correct. EX2018 [Ricketts Decl.], ¶112.

In the Petition's annotation of Lin-191 Fig. 72, adhesion layer 71 and seed layer 72 as well as adhesion layer 711 and seed layer 712 can be seen together:



Pet. 50 (citing EX1005 [Lin-191], FIG. 72 (excerpt); EX1003, ¶205).

The Petition errs in its assertions that “the combination of layers 711 and 712 [in Lin-191 Fig. 72] is a *third metal layer on metal pad 163*.” Pet., 26 (emphasis in original). In other words, in view of Lin-191's configuration, the Petition errs in asserting that two layers 711 and 712 are one layer—“a third metal layer.” EX2018 [Ricketts Decl.], ¶114. Based on Petitioners’ own position regarding claim 7, adhesion layer 711 and seed layer 712 in Lin-191 Fig. 72 are two different layers, not one layer.



EX1005 [Lin-191], Fig. 72 (excerpted and annotated), [0389] (“metal layer 713 under the seed layer 712 and over the solder joints 720.”); (“a seed layer 712 under the adhesion layer 711”).

Notably, Petitioners combine layers 711 and 712 because the claim language requires that a third metal layer is on the first metal pad and that a copper layer is over the third metal layer. EX2018 [Ricketts Decl.], ¶115. The alleged first metal pad is metal pad 163. Adhesion layer 711 is on the metal pad 163 and the alleged copper layer 713 is over seed layer 712, not the adhesion layer 711. Thus, if layers 711 and 712 are not one layer, under Petitioners' apparent view, the claim limitation is not met. EX2018 [Ricketts Decl.], ¶115. But, by Petitioner's own admission, adhesion and seed layers are not the same layer. Pet., 26, 49. Thus, Lin-191 fails to disclose "a third metal layer on said first metal pad and a third copper layer over said third metal layer."

In view of Lin-191's configuration and Petitioner's admission, a POSITA would not consider Lin-191's adhesion layer 711 and seed layer 712 to be a single layer. EX2018 [Ricketts Decl.], ¶116. Lin-191 does not refer to adhesion layer 711 and seed layer 712 as a single layer. EX1005 [Lin-191], [0389]-[0400]. Instead, adhesion layer 711 and seed layer 712 are two different layers made of different materials serving different purposes. EX1005 [Lin-191], [0389] ("a seed layer 712 under the adhesion layer 711"), Fig. 72; EX2018 [Ricketts Decl.], ¶116. A POSITA would understand an adhesion layer as a layer made to allow materials that are not compatible (in adhesion) to adhere to one another. EX2018 [Ricketts Decl.], ¶116.

This is a common occurrence in microfabrication where dissimilar materials are deposited on one another. EX2018 [Ricketts Decl.], ¶116.

The materials that Lin-191 specifies for an adhesion layer 711 are metals and compounds selected for adhesion and diffusion barrier performance rather than for conductivity. EX1005 [Lin-191], [0390]; EX2018 [Ricketts Decl.], ¶117. Lin-191 uses these materials because, for example, copper does not adhere well to, and can diffuse into, the underlying dielectric or pad material. EX2018 [Ricketts Decl.], ¶117.

The separate seed layer in Lin-191 is present for a different reason. EX2018 [Ricketts Decl.], ¶118. Electroplating requires a continuous conductive surface from which the plated metal can nucleate and grow, and the seed layer supplies that surface. EX2018 [Ricketts Decl.], ¶118. This is why Lin-191 specifies seed layer 712 as “copper, silver, gold, nickel or titanium-copper alloy”—metals selected for their compatibility with the metal to be plated. EX1005 [Lin-191], [0390]. EX2018 [Ricketts Decl.], ¶118. The materials Lin-191 specifies for the adhesion layer would not serve as a plating seed, and the copper and noble metals it specifies for the seed layer would not provide the adhesion and barrier function. EX2018 [Ricketts Decl.], ¶118.

Further, the Petition treats Lin-191’s adhesion, seed, and metal layers as three separate claimed layers. EX2018 [Ricketts Decl.], ¶119. For claim 7, the

Petition states that “Lin-191 teaches a multilayered metal interconnect with two copper layers and a metal layer, i.e., a ‘patterned metal layer 7’ having ‘adhesion layer 71, the seed layer 72, metal layer 73....” Pet., 49 (citing EX1005 [Lin-191], [0379], [0260]-[0264], [0420]); EX1003 [Shanfield Decl.], ¶204. The Petition then maps each of those layers to a separate claimed layer: “Adhesion layer 71 is a metal (e.g., titanium or nickel) and is thus a fourth metal layer.... Seed layer 72 is ‘a copper layer’ on adhesion layer 71 and is thus a fourth copper layer on said fourth metal layer.... Metal layer 73 ... is thus a fifth copper layer on said fourth copper layer.” Pet., 49.

The Petition takes the same approach when it maps Lin-191’s under-bump metallurgy for the “first metal bump” of limitation 1(d)(i), describing Lin-191’s “adhesion layer 18, the seed layer 19, and metal layer[] 27” as the separate metal layers that “compose an under bump metallurgic (UBM) layer.” Pet., 19-20 (quoting EX1005 [Lin-191], [0323]); EX1003 [Shanfield Decl.], ¶¶153-154. In those mappings the Petition treats a Lin-191 adhesion and seed layers as two distinct layers. EX2018 [Ricketts Decl.], ¶120. For limitation 1(e)(ii), by contrast, the Petition merges an adhesion layer and a seed layer into a single claimed “third metal layer.”

The Petition elsewhere describes these layers as a “three-metal layer interconnect” and “Lin-191’s three-layer metal interconnect.” Pet., 113. Based on

Petitioners' own statements, a POSITA would understand Lin-191's adhesion layer, seed layer, and metal layer to be three layers, and would not understand an adhesion layer and a seed layer together to be a single layer. EX2018 [Ricketts Decl.], ¶121. Petitioners' position that "the combination of layers 711 and 712 is a third metal layer on metal pad 163" (Pet., 26) merges what Petitioners identify as two distinct layers into one claimed layer, which is inconsistent with Petitioners' own mapping of claim 7 and limitation 1(d)(i). EX2018 [Ricketts Decl.], ¶122.

For these reasons, the structure of the chip package claimed at '763 Patent claim 1 is different than the structure of the semiconductors described in Lin-191. EX2018 [Ricketts Decl.], ¶123. Because neither Sundaram nor Lin-191 teaches or suggests limitation 1(e)(ii), the Petition has not shown that claim 1 (or the claims depending therefrom) are unpatentable.

3. There Is No Motivation to Combine Sundaram and Lin-191.

The Petition advances a separate motivation to combine for limitation 1(e)(ii) that is distinct from the motivation it advances for limitation 1(e)(i). Pet., 27. The Petition asserts that "[a] POSITA would have been motivated and found obvious to modify Sundaram's bump per Lin-191's layered bump teachings," and that the result would be "Sundaram's bump (third metal interconnect) having a third metal layer over said first metal pad and a third copper layer over said third

metal layer, wherein said third copper layer has a thickness between 5 and 30 micrometers.” *Id.* (citing EX1003 [Shanfield Decl.], ¶¶169-170, 173). The Petition states that the rationale is that “Lin-191’s metal bump provides improved metallurgical bonding and increased resistance to fatigue and stress-induced failure by employing a layered structure,” and that the configuration “would reduce the risk of intermetallic formation at critical interfaces, mitigate electromigration, and better absorb mechanical strain during thermal cycling.” *Id.* (citing EX1003 [Shanfield Decl.], ¶170.)

Nothing in Lin-191 indicates that Lin-191’s adhesion layer 711 and seed layer 712 provide increased resistance to fatigue or stress-induced failure, reduced intermetallic formation, mitigation of electromigration, or improved absorption of mechanical strain during thermal cycling. EX2018 [Ricketts Decl.], ¶125. Lin-191 describes those layers structurally and by material and thickness, and does not attribute the asserted advantages to them. EX1005 [Lin-191], [0389]-[0400]; EX2018 [Ricketts Decl.], ¶125.

Dr. Shanfield’s declaration confirms that the asserted advantages are not drawn from Lin-191. EX2018 [Ricketts Decl.], ¶126. To support the propositions that a layered bump prevents diffusion, and increases resistance to fatigue, Dr. Shanfield relies on other references directed to under-bump metallurgy and diffusion barriers generally. EX1003 [Shanfield Decl.], ¶170 (citing EX1022 and

EX1047 for metallurgical bonding and diffusion prevention); ¶171 (citing EX1063 for uniform plating and void prevention). EX2018 [Ricketts Decl.], ¶126.

Moreover, the diffusion Dr. Shanfield identifies is the diffusion of “solder material into the first metal pad,” EX1003 [Shanfield Decl.], ¶170, whereas the Petition describes Sundaram’s own interconnect on die pad 135 as copper. Pet., 26. But the Petition identifies no solder-diffusion, oxide, or adhesion problem in that copper structure that Lin-191’s added layers would remedy. EX2018 [Ricketts Decl.], ¶126. The asserted motivation therefore does not rest on any teaching that Lin-191’s adhesion layer 711 and seed layer 712 supply those advantages in the structure the Petition maps. EX2018 [Ricketts Decl.], ¶126.

Petitioners’ asserted motivation also presupposes a bump structure in Sundaram to be modified. EX2018 [Ricketts Decl.], ¶127. The Petition describes the combination as “modify[ing] Sundaram’s bump per Lin-191’s layered bump teachings.” Pet., 27. As discussed above, Sundaram does not describe the construction of any bump on electronic device 125. A POSITA could not modify a structure that the reference does not describe, and the Petition does not explain what would be modified. EX2018 [Ricketts Decl.], ¶127.

A POSITA would not be motivated to combine Sundaram and Lin-191. EX2018 [Ricketts Decl.], ¶128. The Petition has not shown that a POSITA would have looked to Lin-191’s adhesion-layer/seed-layer/electroplated-layer bump

structure to modify the bump on die pad 135 of Sundaram. EX2018 [Ricketts Decl.], ¶128. A POSITA would have known that an adhesion or diffusion-barrier layer, such as the titanium or nickel adhesion layer 711 that Lin-191 describes, is needed only in particular circumstances, for example: where copper would otherwise diffuse into an adjacent, dissimilar metal; where copper would otherwise diffuse into an oxide or other inorganic dielectric; or where copper does not otherwise bond adequately to the material beneath it. EX2018 [Ricketts Decl.], ¶128. The Petition does not show that any of these circumstances exists in Sundaram.

The Petition's own description of this combination confirms that Sundaram's own bump is copper. EX2018 [Ricketts Decl.], ¶129. The Petition states that Lin-191's bumps 710, "like Sundaram's copper bumps, are metal interconnect[s]." Pet., 26. The Petition's stated motivation for adding Lin-191's layered structure is that it would provide "improved metallurgical bonding and increased resistance to fatigue and stress-induced failure," would "reduce the risk of intermetallic formation at critical interfaces," and would "mitigate electromigration" and "better absorb mechanical strain during thermal cycling." Pet., 27 (citing EX1003 [Shanfield Decl.], ¶¶169-170). This rationale does not identify any specific diffusion, oxide, or adhesion problem with Sundaram's own copper bump on die pad 135 that Lin-191's layers would remedy. EX2018 [Ricketts Decl.], ¶129. Moreover, electronic

device 125 is not described structurally at all, because Sundaram pertains to the interposer not the electronic device 125. EX2018 [Ricketts Decl.], ¶129.

For these reasons, the Petition has not shown that a POSITA would have been motivated to combine Sundaram and Lin-191 in the manner the Petition proposes, and has not shown that the combination teaches or suggests limitation 1(e)(ii).

4. Sundaram Does Not Teach or Suggest the “First Metal Interconnect Comprises a First Metal Layer and a Second Copper Layer Over Said First Metal Layer.”

For other claim limitations discussed above, the Petition relies on Sundaram Figure 3. With regard to limitation 1(c)(iii), however, the Petition relies on Sundaram Figure 15. These two figures, however, relate to *alternative* embodiments that a POSITA would not consider together. EX2018 [Ricketts Decl.], ¶134.

Limitation 1(c)(iii) requires that “said first metal interconnect comprises a first metal layer and a second copper layer over said first metal layer.” EX1001 [’763 Patent], cl. 1. For this two-layer construction, the Petition does not rely on the interconnect structure it identifies in Sundaram’s Figure 3. EX2018 [Ricketts Decl.], ¶135. Instead, the Petition relies on Sundaram’s Figure 15, asserting that Sundaram teaches “a first metal layer formed by ‘direct metallization using wet electroless copper deposition’ and a second copper layer over said first metal layer

formed by ‘semi-additive plating’ using ‘copper as metal.’” Pet., 16 (quoting EX1004 [Sundaram], 9:61-65, 10:26-28) (citing EX1003 [Shanfield Decl.], ¶148).

The Petition states that “a POSITA would have been motivated, found obvious, and had a REOS in applying FIG. 15’s layer teachings to FIG. 3’s interconnect structure.” Pet., 17 (citing EX1003 [Shanfield Decl.], ¶149). This is incorrect. EX2018 [Ricketts Decl.], ¶136.

The Figure 3 interconnect structure is not described as comprising the seed-plus-electroplated two-layer construction of Figure 15. EX2018 [Ricketts Decl.], ¶137. Sundaram describes FIG. 15 not as a package embodiment (like Figure 3) but as the process flow for a research *test vehicle*. Sundaram states that “[a] glass test vehicle was designed and fabricated to characterize the substrate and TPVs in glass,” and that “FIG. 15 shows the process flow used for fabricating the test vehicle.” EX1004 [Sundaram], 10:5-15. Sundaram identifies the purpose of that test vehicle as characterization—it describes “[r]ing resonators ... designed to extract the dielectric constant and loss tangent of the interposer” and additional “structures ... designed and fabricated to characterize the electrical characteristics of the interconnections (lines and TPVs) in glass interposer.” *Id.* A POSITA would understand a “test vehicle” or “demonstrator” of this kind to be an experimental construct built to measure material and electrical properties, not a manufacturing template for the chip package of Figure 3. EX2018 [Ricketts Decl.], ¶137. Notably,

Sundaram shows the “resulting two metal layer structure” of that process in Figure 16a-c—not in Figure 3. *Id.* A POSITA would not have understood Sundaram to teach transplanting the Figure 15 characterization process onto the separate Figure 3 package embodiment. EX2018 [Ricketts Decl.], ¶137.

Sundaram ties the specific Figure 15 process—electroless copper seed formation followed by semi-additive plating—to a particular metallization challenge that Sundaram solves with polymer-laminated glass, and not to the Figure 3 interconnect. EX2018 [Ricketts Decl.], ¶138. Sundaram explains that “direct wet metallization on glass has been a challenge due to surface chemistry of glass and its interaction with metals,” and that “[t]he presence of a surface polymer ... on glass facilitates metallization.” EX1004 [Sundaram], 9:55-62. It is in that context that Sundaram states the glass “TPV side walls were subjected to direct metallization using wet electroless copper deposition” and that “[a] semi-additive plating (SAP) approach was used.” *Id.*, 9:61-64. A POSITA would understand Sundaram's electroless-seed-plus-SAP sequence to have been selected to metallize the polymer-laminated glass of the test vehicle, addressing a known difficulty of metallizing glass, rather than as a general instruction to reconstruct the Figure 3 interconnect. EX2018 [Ricketts Decl.], ¶138.

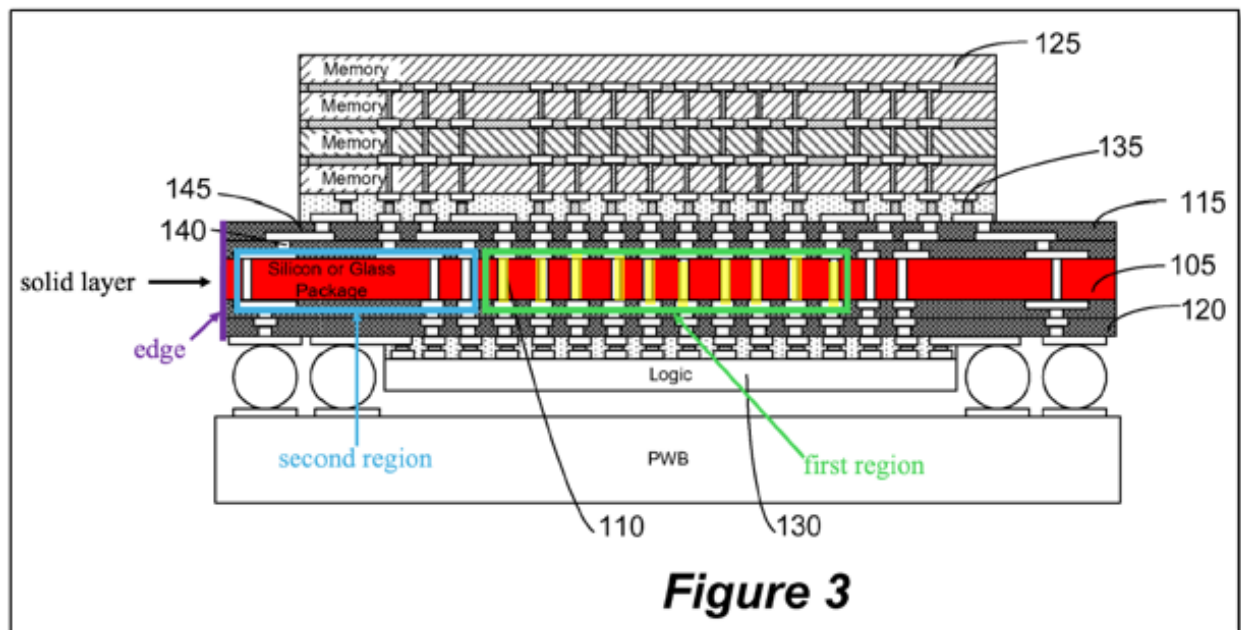
Sundaram describes Figure 3's metallization on its own terms, and the Petition identifies no deficiency in that description that Figure 15's process would

cure. EX2018 [Ricketts Decl.], ¶139. For the Figure 3 embodiment, Sundaram states that its through vias and die pads “can be metalized with a highly-conductive metal, for example copper,” and “can also be metalized with a polymer liner or a metal seeding liner.” EX1004 [Sundaram], 6:22-33. Sundaram does not describe the Figure 3 interconnect as formed by Figure 15’s electroless-seed-plus-SAP two-layer process, and it does not cross-reference Figure 15 as the method for building Figure 3. EX2018 [Ricketts Decl.], ¶139. The Petition identifies no problem, shortcoming, or unmet need in Figure 3’s own metallization that Figure 15’s process would solve. *Id.* Absent any such reason, a POSITA would not have been motivated to displace Figure 3’s described metallization in favor of the Figure 15 test-vehicle process. *Id.*

Thus, Sundaram does not teach or suggest limitation 1(c)(iii).

5. Sundaram Does Not Teach or Suggest a “First Region.”

Various limitations in claims 1 and 18 require “a first region.” *See, e.g.*, EX1001 [’763 Patent], cls. 1(a)(iv); 18(a)(iii). As discussed in Section IV, a “first region” is a region that does not include metal plugs. Petitioner relies on Sundaram



Pet., 9 (citing EX1004, Fig. 3) (annotated by Petitioners; PO has added yellow highlights showing metal plugs).

A POSITA would understand that the cross section of the structure shown in Figure 3 above would be taken vertically through the middle of the structure.

EX2018 [Ricketts Decl.], ¶141. As shown above, Petitioners randomly identify various portions of Sundaram as regions. EX2018 [Ricketts Decl.], ¶141.

Petitioners identifies a “first region” in a green box. This region, however, includes numerous metal plugs (annotated in yellow in the Figure above). Sundaram specifically states that through vias 110 (sixteen of which are shown in Figure 3; ten of which are highlighted in yellow) are “electrically and thermally conducting” and are metalized. EX1004 [Sundaram], 6:16-29. Thus, a POSITA understands that there must be metal plug through the vias 110 to electrically connect devices. *See*

also e.g., id., 6:46-48 (“The interposer 105 and the through vias 110 work to electrically connect the first electronic device 125 and the second electronic device 130.”).

Because the Petition identifies a region having metal plugs, the Petition has not shown the claimed “first region.” EX2018 [Ricketts Decl.], ¶141. And because the Petition has not shown a “first region,” it also has not shown any limitations in claim 1 related to a “first region.” EX2018 [Ricketts Decl.], ¶141. The Petition has not shown the “first region” limitations of claim 10, 13, 15, 18, and 23 have been met. EX2018 [Ricketts Decl.], ¶141.

Figure 4 of Sundaram is “a top view of the interconnect structure illustrated in FIG. 3” (EX1004 [Sundaram], 3:27-28). Thus, Figure 4 does not show any details of the configuration of the interposer 105 which includes metal plugs. And, from Figure 4, one cannot see that there are actually numerous metal plugs in the alleged “first region.” Thus, Sundaram does not disclose the claimed “first region.”

**6. Sundaram Does Not Support the Petition’s
Motivation to Combine for Claim 2’s “Passive Component
... Over Said First Interconnection Scheme.”**

Claim 2 requires “a passive component over said first interconnection scheme and connected to said first interconnection scheme through a solder layer.” EX1001 [’763 Patent], cl. 2. The Petition relies on Sundaram’s Figure 33 for the proposition that a passive component can be connected to an interposer’s

redistribution layer through a solder-based connection. Pet., 29-30. The Petitioner then proposes relocating that passive component into the Figure 3 embodiment relied on for the remaining limitations of claim 1. *Id.* (citing EX1003 [Shanfield Decl.], ¶¶176-182.)

The Petition states that “[b]ased on Sundaram’s FIG. 33 embodiment, a POSITA would have found obvious and been motivated to include a passive component over Sundaram[’s] first interconnection scheme, e.g., adjacent to FIG. 3’s electronic device 130.” Pet., 29-30 (citing EX1003 [Shanfield Decl.], ¶178).

Sundaram’s FIG. 33, however, does not support that placement. EX2018 [Ricketts Decl.], ¶146. FIG. 33 depicts a glass core with an image sensor chip and associated test-pads and micro-bumps-and-RDL structure on one side, and an “ASIC or Other IC” on the opposite side, with BGA solder balls formed beneath the ASIC for connection to the next-level board. EX1004 [Sundaram], Fig. 33; 6:44-46.

The convention the Petition applies is that “over” refers to the direction toward the printed wiring board (“PWB”) and “under” refers to the direction away from the PWB. Pet., 13 n.3; EX1003 [Shanfield Decl.], ¶143. Because the BGA solder balls that connect to the PWB are formed on the ASIC side of FIG. 33, a POSITA would understand the ASIC side of FIG. 33 to be the “over” side and the sensor side to be the “under” side—using Dr. Shanfield’s own mapping elsewhere

of the analogous ASIC-type device (device 130) and sensor-type device (device 125) in the FIG. 3 embodiment. EX2018 [Ricketts Decl.], ¶147; EX1004 [Sundaram], 6:37-45 (device 125 as an image sensor chip, device 130 as the logic/ASIC device).

FIG. 33, however, shows the “Passives” element positioned on the sensor side of the structure—immediately adjacent to the “Sensor” and its micro-bumps-and-RDL connection—not on the ASIC/BGA side. EX1004 [Sundaram], Fig. 33. Sundaram’s own drawing therefore places its passive component on the “under” side of the structure, i.e., the side away from the PWB, and not “over” the interconnection scheme that connects to the PWB. EX2018 [Ricketts Decl.], ¶148.

This is the opposite of where the Petition proposes to place the corresponding element in the FIG. 3 combination. EX2018 [Ricketts Decl.], ¶149. The Petition places its combined passive component “adjacent to FIG. 3’s electronic device 130,” which Dr. Shanfield elsewhere maps to the ASIC-type, PWB-facing side of the FIG. 3 structure. Pet., 29-30. The Petition thus takes the general teaching of FIG. 33—that a passive component can be soldered to an RDL—but relocates that passive component to the side of the structure opposite to where Sundaram actually discloses it. EX2018 [Ricketts Decl.], ¶149. The Petition does so without identifying any disclosure in Sundaram that supports placing a

passive component on the device-130/over side rather than the device-125/under side depicted in FIG. 33. EX2018 [Ricketts Decl.], ¶149.

A POSITA reading FIG. 33 would understand Sundaram’s own teaching to place the passive component on the side of the package furthest from the board-level connection. EX2018 [Ricketts Decl.], ¶150. The Petition provides no reasoning for why a POSITA would instead have placed the passive component on the opposite, PWB-facing side of the package as the Petition proposes. EX2018 [Ricketts Decl.], ¶150. Because the Petition’s sole evidentiary basis for the claimed placement is FIG. 33, and FIG. 33 shows the passive component on the side opposite to where the Petition places it, the Petition has not shown that a POSITA would have been motivated to place a passive component “over said first interconnection scheme” as claim 2 requires, nor has it shown a reasonable expectation of success in doing so. EX2018 [Ricketts Decl.], ¶150.

For these reasons, the Petition fails to prove that claim 2 is unpatentable over Sundaram and Lin-191.

7. The Petition’s Analysis of Lin-191’s for Claim 7 Confirms the Inconsistency Identified for Limitation 1(e)(ii).

Claim 7 recites that “said fourth metal interconnect comprises a fourth metal layer, a fourth copper layer on said fourth metal layer, and a fifth copper layer on said fourth copper layer.” EX1001 [’763 Patent], cl. 7. For this three-layer

construction, the Petition maps Lin-191's patterned metal layer 7 as three separate layers—adhesion layer 71 as the “fourth metal layer,” seed layer 72 as the “fourth copper layer,” and metal layer 73 as the “fifth copper layer.” Pet., 49. As explained above in connection with limitation 1(e)(ii), this mapping—treating a Lin-191 adhesion layer and a Lin-191 seed layer as two distinct layers—is the opposite of the Petition's treatment of the same type of structure (adhesion layer 711 and seed layer 712) for limitation 1(e)(ii). Petitioners' claim 7 mapping confirms that Lin-191's adhesion and seed layers are separate layers. EX2018 [Ricketts Decl.], ¶152.

8. Independent Claim 18 is Patentable For the Same Reasons as Claim 1.

For limitations 18(c)(iii), 18(e), 18(e)(i), and 18(e)(ii), the Petition cross-references claim 1 and relies on the same analysis that it uses for claim 1. Pet., 64, 66-67. Because the Petition relies on the same analysis for claim 18 as it does for claim 1, claim 18 is patentable for the same reasons given for limitations 1(c)(iii), 1(e), 1(e)(i), and 1(e)(ii) above. *Supra*, §V.A.1-5.

B. Ground 1B (Sundaram, Lin-191, and Lin-863)

1. Sundaram and Lin-863 Do Not Teach or Suggest “No [] Copper Plug in Said First Region.”

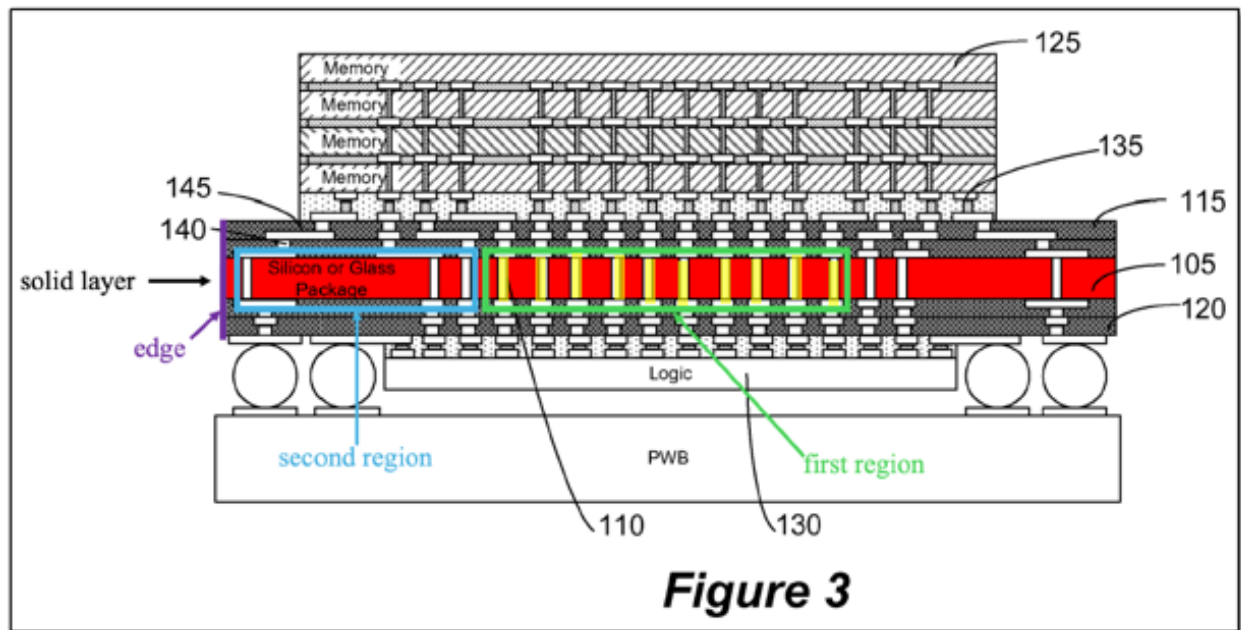
Claim 15 requires “no[] copper plug in said first region.” EX1001 [’763 Patent], cl. 15; *see* Pet., 79. That is, Petitioners “interpret the claimed “no any copper plug” to be ‘no copper plug.’” *Id.*

The Petition asserts two arguments. First, the Petition relies on Sundaram's Figure 4, reasoning that because "die-to-die vias connecting pads are at the periphery" and "die-to-PWB vias are located outside the peripheral area of the smaller device, a POSITA would have understood Sundaram as teaching the first region as having no copper plugs." Pet., 79-80. Second, the Petition relies on Lin-863's Figures 9a-9b as showing a first region with "no copper . . . plug[s]." Pet., 80-82. Thus, Petitioners' analysis fails. EX2018 [Ricketts Decl.], ¶155.

a) Sundaram Does Not Teach or Suggest Claim 15.

Claim 15 is patentable for the reasons discussed in Section V.A.5 with regard to the "first region."

In addition, Figure 3 of Sundaram specifically shows through vias 110 having metal plugs (yellow highlights) in the alleged first region.

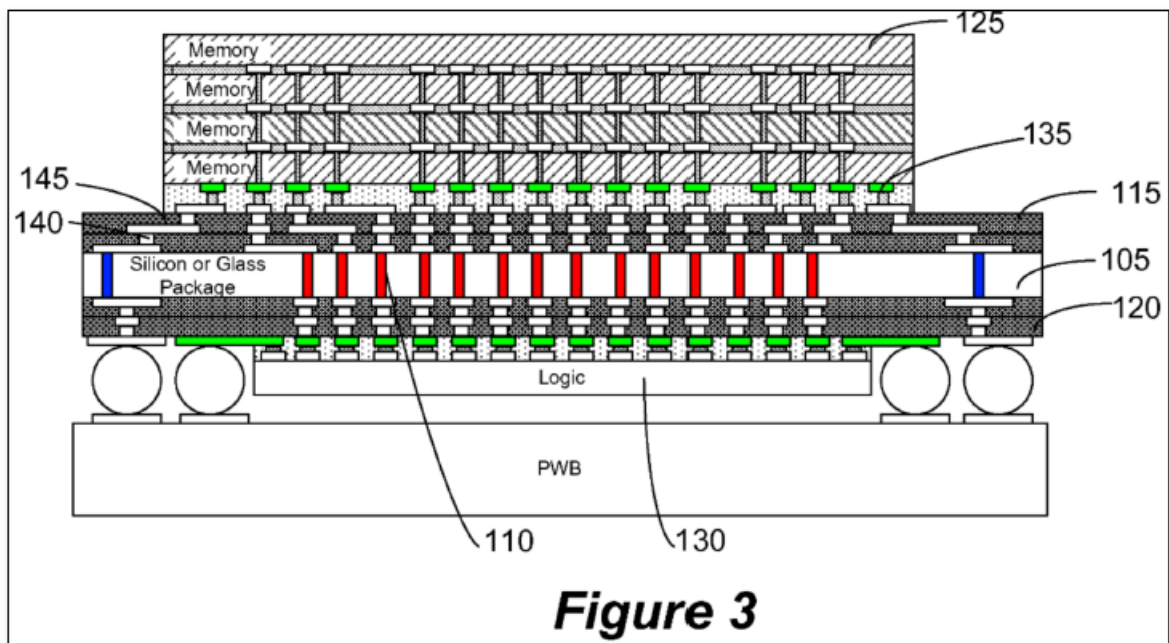


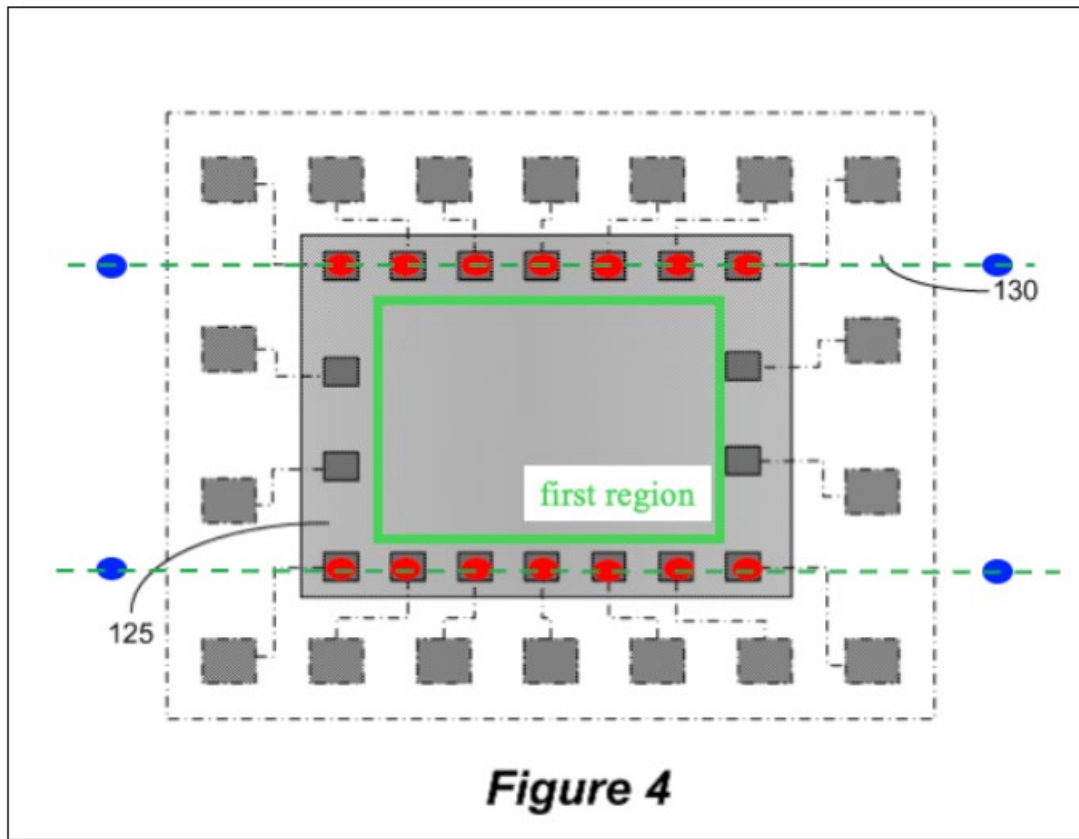
Pet., 9 (citing EX1004 [Sundaram], Fig. 3) (annotated by Petitioners; PO added yellow highlights). Sundaram teaches that these metal plugs can be copper. EX1004 [Sundaram], 6:22-27.

Sundaram's description of its via placement is inconsistent with the Petition's assertion that the alleged "first region" has no metal plugs. Sundaram's disclosure demonstrates that there would be metal (copper) plugs in the alleged "first region." EX2018 [Ricketts Decl.], ¶159. Sundaram states that its interposer "electrically connects the first and second set of devices at the same or similar through-via density as in the first and second electronic devices," and expressly distinguishes this arrangement from prior-art interposers, whose vias "were generally of the same surface-mount pitch as the board, typically from 400-1000 microns." EX1004 [Sundaram], 5:25-35. Sundaram's interposer instead operates "at device pitch of 10-30 microns." *Id.* Sundaram further states that its through vias 110 "are electrically and thermally conducting, and are distributed within the interposer such that they provide localized thermal isolation or thermal conduction between the first and second electronic devices." *Id.*, 6:16-19; see also *id.*, cl. 23 (reciting through-vias "distributed within the [] interposer" to "provide localized thermal isolation or thermal conduction"). A via arrangement designed to match a device's own fine, area-distributed I/O pitch, and to provide "localized" thermal management at points across the device, is inconsistent with an arrangement the

Petition proposes (i.e., no metal plugs in the alleged first region of Sundaram.)

EX2018 [Ricketts Decl.], ¶159. Figure 3's cross-section, reproduced above, is consistent with this description: through vias 110 run continuously across the entire width of the alleged first region.





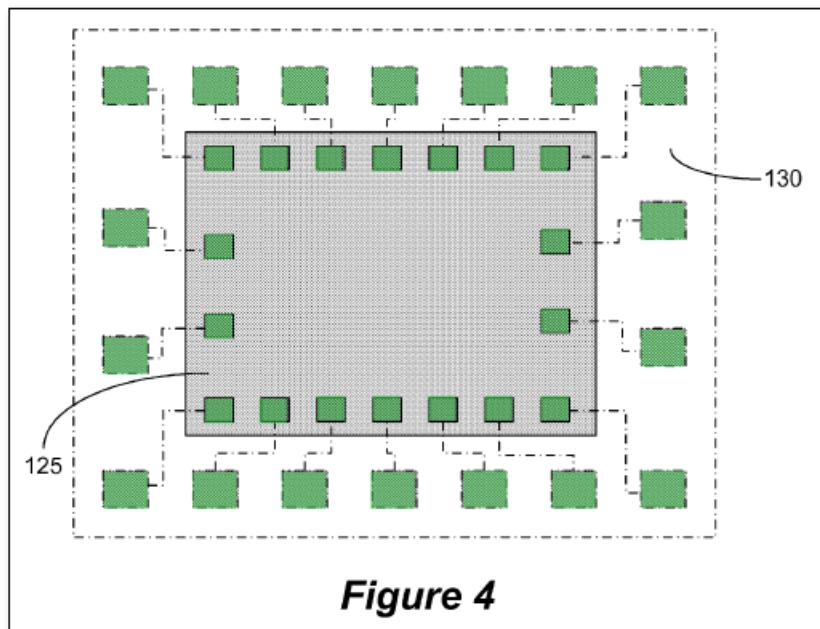
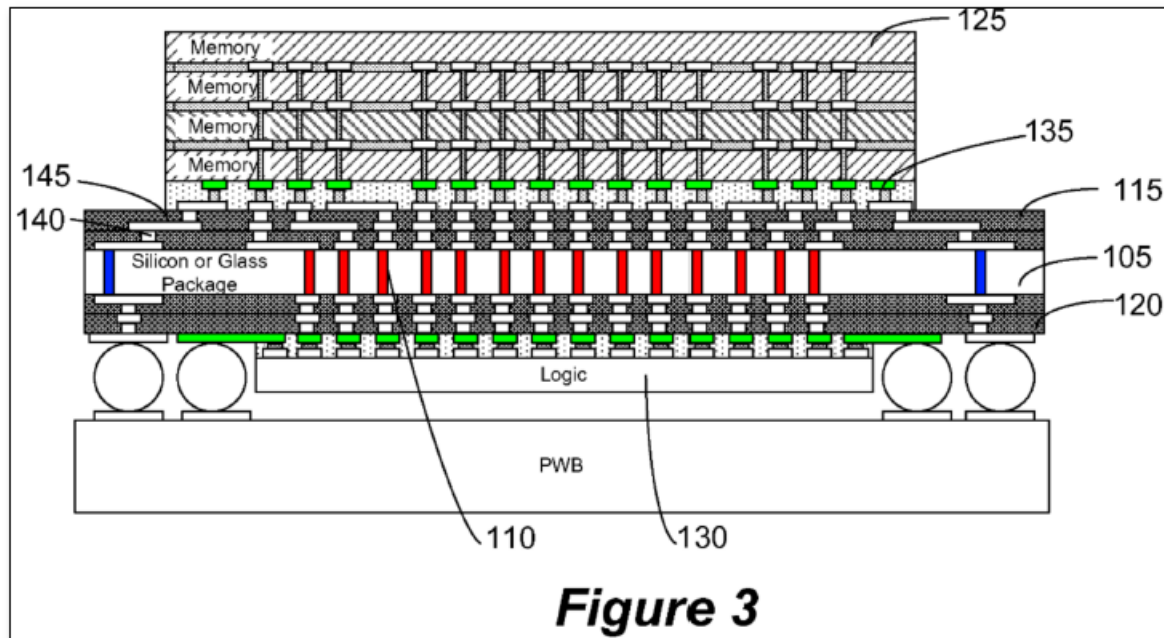
Pet., 71, 80 (EX1004 [Sundaram], Fig. 4) (annotated by Petitioners).

With no support in the specification and without providing any reasoning, as shown above, Petitioners annotate Figure 4 to (1) include blue circles representing metal plugs shown in Figure 3, and (2) add dashed lines which purportedly show the location from where the cross section of Figure 3 is taken. EX2018 [Ricketts Decl.], ¶160. Petitioners' annotations of Figure 4 are wrong. *Id.*

As a threshold matter, without any indication in Sundaram where the cross-section of Figure 3 was taken from in Figure 4, a POSITA would assume Figure 3 would be a cross-section through the middle of Figure 4, not along some random

location (green dashed lines) as Petitioners have done. EX2018 [Ricketts Decl.], ¶161; Pet., 73. The Petition treats the dashed lines in Figure 4 as depicting the specific location of “die-to-die vias 110.” Pet., 79; EX1003 [Shanfield Decl.], ¶¶259-260, 269-270. Sundaram’s specification, however, does not support that reading. Nowhere does Sundaram teach or suggest the location of Petitioners’ annotated green dashed lines. EX2018 [Ricketts Decl.], ¶161.

Figure 4 is simply a top view of Figure 3. EX1004 [Sundaram], 3:27-28. Thus, the features shown on Figure 4 should match exactly with the features of Figure 3. EX2018 [Ricketts Decl.], ¶162. Even using Petitioner’s own view of the cross section location of Figure 3, Petitioners’ annotations of Figures 3 and 4 do not match, demonstrating that Petitioners’ analysis is flawed. For example, annotated Figure 4 shows seven (7) metal plugs in red. But annotated Figure 3 shows fourteen (14) metal plugs in red. Further, the location and spacing of the annotated metal plugs (red) in Figure 4 do not match up with the annotated metal plugs (red) shown in Figure 3. EX2018 [Ricketts Decl.], ¶162. Notably, given that Figure 4 is a top view of Figure 3, the configuration of the interposer 105 (and its metal plugs) in Figure 3 would not even be visible in Figure 4.



Pet., 71 (EX1004 [Sundaram] Fig. 4) (annotated by Petitioners).

As shown above, Petitioners provide additional annotations that further demonstrate that their understanding of Figure 3 and 4 is wrong. EX2018 [Ricketts Decl.], ¶163. Petitioners asserts that the green highlight components are pads. Pet.,

70-71. Once again, the annotation for Figure 3 and 4 do not match. As shown above in annotated Figure 3, there are sixteen (16) pads at the bottom of interposer 105 and sixteen (16) pads underneath the memory of device 125. EX2018 [Ricketts Decl.], ¶163. Petitioners' annotated Figure 4, however, only shows seven pads on the bottom of interposer 105 and seven pads underneath memory of device 125. EX2018 [Ricketts Decl.], ¶163.

Based on Petitioner's annotation, Petitioners' position is that their annotated green boxes in Figure 4 (above) must necessarily line up with through vias 110 (and their metal plug (annotated in red ovals above). EX2018 [Ricketts Decl.], ¶164. This is also wrong. *Id.* Sundaram discloses that devices 125 and 130 can be connected with "through vias 110, blind vias 140, and conductor traces 145." EX1004 [Sundaram], 7:1-9. Sundaram elsewhere explains that this combination of structures exists to let a die's pad layout differ from, and be routed laterally to, the through-via pattern of the interposer: "electronic devices having different I/O pad layouts and sizes can also be connected through the use of blind vias 140 and conductor traces 145 defined within polymer-metal redistribution layers deposited on the first side 115 and second side 120 of the interposer 105." EX1004 [Sundaram], 6:64-69. Because a pad's connection may be completed through a lateral trace rather than a via positioned directly beneath it, the position of a pad in

Figure 4 does not establish where the physical location of associated through vias 110. EX2018 [Ricketts Decl.], ¶164.

Notably, Petitioners assert that Figure 4, as labeled by Sundaram, is inconsistent with Figure 3: in Figure 3, first electronic device 125 is drawn larger than second electronic device 130, while in Figure 4 as labeled, device 130 is the larger of the two. Pet., 72 n.6. The Petition resolves this inconsistency by relabeling Figure 4, concluding that “a POSITA would have understood Sundaram’s FIG. 4 to mislabel devices 125, 130.”² *Id.* The Petitioner’s arguments with regard to claims 13 and 15 depend on accepting this relabeling as correct. But there is no reason a POSITA would relabel Fig. 4 in this manner. EX2018 [Ricketts Decl.], ¶165. Accordingly, Sundaram and Lin-863 do not teach or suggest claim 15.

² Under this position, Figure 4 would also be described incorrectly. EX2018 [Ricketts Decl.], ¶165, n. 1. Figure 4 is supposed to simply be “a top view of the interconnect structure illustrated in FIG. 3.” (EX1004 [Sundaram], 3:27-28; *see also id.*, 7:1-4).

b) Combining Sundaram and Lin-863 Does Not Disclose a First Region with No Copper Plugs and There is No Motivation to Combine.

The Petition seeks to combine Lin-863 (shown below) with Sundaram. But this combination does not result in a structure with no copper plugs in the alleged first region of Sundaram. EX2018 [Ricketts Decl.], ¶166.

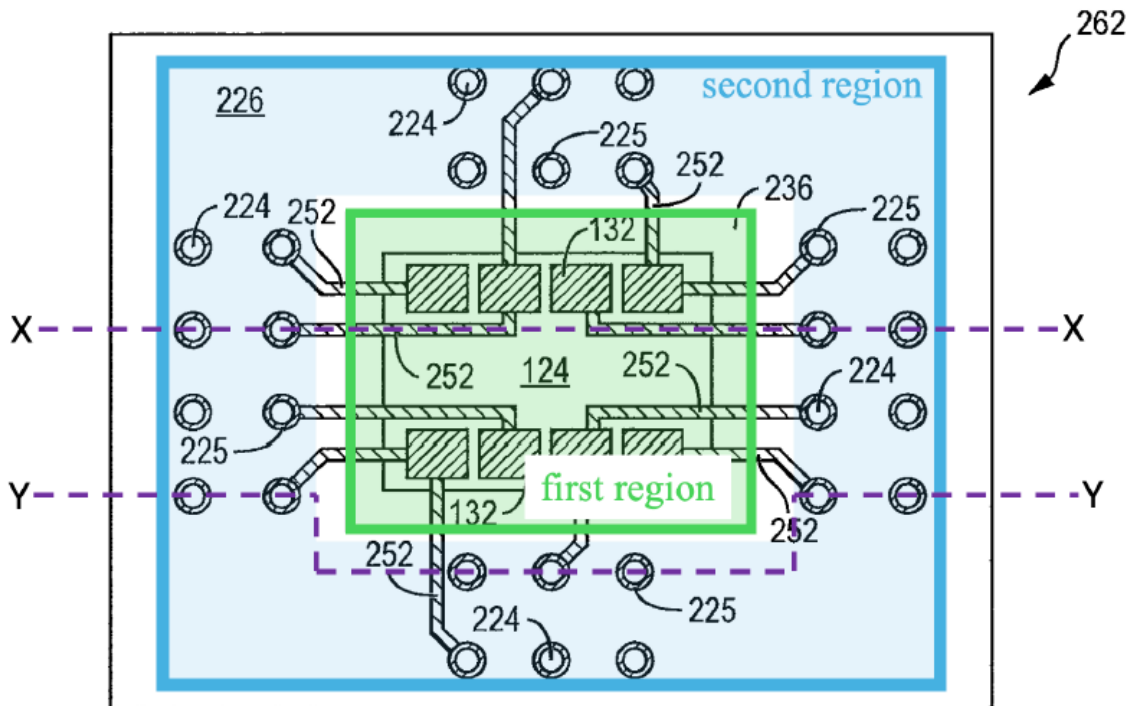


FIG. 9b

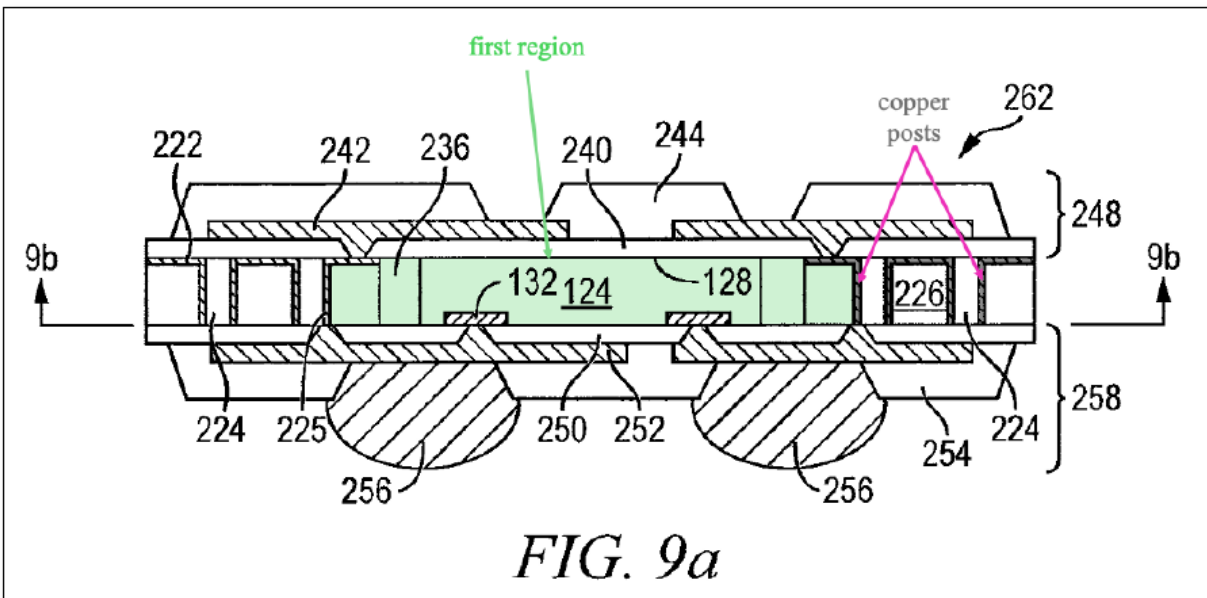


FIG. 9a

Pet., 81-82 (annotating Lin-863 Figs. 9a and 9b).

The Petition asserts that “[a] POSITA would have found obvious and been motivated to modify Sundaram’s first region per Lin-863’s teaching to accommodate space for an additional semiconductor chip to be included in Sundaram’s package.” Pet., 82. Petitioners’ analysis is incorrect. EX2018 [Ricketts Decl.], ¶167.

Sundaram discloses a configuration where two devices 125 and 130 are connected using an interposer 105. EX1004 [Sundaram,], 6:34-36, Fig. 3; EX2018 [Ricketts Decl.], ¶168. The electrical connection between these devices are specifically made using numerous metal plugs in the alleged first region. EX1004 [Sundaram], 6:46-47; EX2018 [Ricketts Decl.], ¶168. A POSITA would not remove the metal plugs in the alleged first region of Sundaram merely because Petitioners can identify some region in Lin-863 between metal plugs (coppers posts) that do not have metal plugs. *Id.*

There is also no motivation to combine Sundaram and Lin-863. EX2018 [Ricketts Decl.], ¶169. Sundaram discloses a thin glass (silicon-oxide) interposer whose fine, device-pitch through vias 110 are designed to match the I/O density of the attached chips. EX1004 [Sundaram], 5:25-29, 6:11-15. Lin-863, on the other hand, discloses a fan-out, chip-scale package in which conductive TMVs are drilled through a thick organic molding compound to route signals to external contacts for package-on-package stacking. EX1007, 8:4-9, 12:51-54. The Petition

identifies no problem in Sundaram that Lin-863's rectangular TMV arrangement would solve, and no teaching in either reference suggesting that Sundaram's copper-plug-in-through-via arrangement should be reorganized to resemble Lin-863's mold-compound via layout. A POSITA presented with Sundaram would have had no reason to look to Lin-863. EX2018 [Ricketts Decl.], ¶169.

There would have been no reasonable expectation of success in combining Sundaram and Lin-863. EX2018 [Ricketts Decl.], ¶170. Lin-863 is a product of Lin-863's *material* and the *process* used to build it, both of which are fundamentally different from Sundaram. *Id.* Thus, a POSITA would not have had a reasonable expectation of successfully when combining Lin-863 and Sundaram.

C. Grounds 1C and 1D (Claim 22's "Silver-Containing Layer")

1. Lin-691 (Ground 1C) Does Not Establish That Claim 22 Would Have Been Obvious.

Claim 22 requires that "said first metal layer is a silver-containing layer." EX1001 ['763 Patent], cl. 22. For Ground 1C, the Petition relies on Lin-691. Pet., 83-84. The Petition proposes to "modify Sundaram's metal conductor such that the Cu seed layer was instead silver, per Lin-691." Pet., 84.

The Petition contends a POSITA would have been motivated to modify Sundaram's copper seed to be silver based on Lin-691. Pet., 84; EX1003 [Shanfield Decl.], ¶¶278-279. This is incorrect. EX2018 [Ricketts Decl.], ¶172. A

POSITA would not be motivated to substitute silver for copper. *Id.* Sundaram teaches that its through-via metallization consist of “1) Cu seed layer formation, and 2) Cu electroplating.” EX1004 [Sundaram], 13:29-33. Copper-on-copper is the conventional process. EX2018 [Ricketts Decl.], ¶172. Introducing a silver seed beneath a copper electroplate creates a dissimilar-metal interface with no corresponding benefit. *Id.* Notably, Lin-691 does not teach that a silver seed is preferable to copper or identify any advantage of silver over copper. *Id.* The Petition’s main rationale to substitute silver is that it “provides improved current distribution ... during subsequent electroplating” because it “has a higher electrical conductivity than Cu.” EX1003 [Shanfield Decl.], ¶278. But silver’s conductivity is only slightly higher than copper—approximately 5-6%. EX2024 [CRC handbook] pp. 2122-23. Such a difference is not at all meaningful with regard to the uniformity of the subsequent copper electroplating. EX2018 [Ricketts Decl.], ¶172. A POSITA would not have expected a marginally more conductive seed (such as silver) to yield a materially more uniform plated via. *Id.*

Dr. Shanfield asserts that “silver adheres more strongly to polymers and glass compared to Cu.” (EX1003 [Shanfield Decl.], ¶278). Lin-691, however, refutes the suggestion that silver would be chosen for adhesion. EX2018 [Ricketts Decl.], ¶172. In Lin-691, it is not the seed (copper or aluminum) that provides adhesion to the underlying dielectric. It is a titanium barrier (located beneath the

seed) that provides the adhesion. EX1008 [Lin-691], [0019]. Dr. Shanfield also asserts that “non-uniform nucleation at the seed layer” may cause voids which may cause poor electromigration resistance, an open circuit, increased resistance, and poor reliability. EX1003 [Shanfield Decl.], ¶278 (citing EX1076 [0011], EX1076 [0012], EX1063[3:12-16]). This supports that Sundaram’s interconnect should have a continuous seed—which it already has in copper. EX2018 [Ricketts Decl.], ¶172. But this has nothing to do with using silver and says nothing about whether using silver is better than copper. *Id.*

Finally, for a reasonable expectation of success, Dr. Shanfield cites various references discussing methods of depositing materials. (EX1008 [0019]; EX1043 [0032] (“sputtering”). But these references do not support selecting silver over copper. EX2018 [Ricketts Decl.], ¶172. They merely establish that seed layers can be deposited by known methods. *Id.*

2. Shenoy (Ground 1D) Does Not Establish That Claim 22 Would Have Been Obvious.

For Ground 1D, the Petition relies, in the alternative, on Shenoy, which describes a glass substrate with through-glass via holes conformally coated with a “seed layer 314” that includes “Ag,” over which a “plated metal 316 . . . can include Cu.” Pet., 86 (citing EX1011 [Shenoy], [0053]-[0055]; EX1003 [Shanfield Decl.], ¶280). The Petition's motivation-to-combine showing for Ground 1D is

derivative of Ground 1C: "A POSITA would have been motivated, found obvious, and had a REOS for the reasons discussed above. See Section VII.A." Pet., 86; EX2018 [Ricketts Decl.], ¶173.

Because Ground 1D relies on the same rationale as Ground 1C, it fails for the same reasons. EX2018 [Ricketts Decl.], ¶174.

D. Ground 2A (Yu and Lin-191)

1. Yu Does Not Teach or Suggest That the "First Semiconductor Chip Comprises a Third Metal Interconnect on a First Metal Pad of Said First Semiconductor Chip."

Limitation 1(e) requires "a first semiconductor chip under said first interconnection scheme, wherein said first semiconductor chip comprises a third metal interconnect on a first metal pad of said first semiconductor chip." EX1001 ['763 Patent], cl. 1. Yu does not disclose this limitation. EX2018 [Ricketts Decl.], ¶175. As with Sundaram in Ground 1A, the structure the Petition identifies as the alleged "third metal interconnect" is a connector that joins the chip to the package metallization, not a layered interconnect on a metal pad of the chip. Pet., 101; EX2018 [Ricketts Decl.], ¶175.

For limitation 1(e)(i), the Petition relies on Yu's "die 52, such as a memory die," as the "first semiconductor chip," and Yu's connector 54 as the "third metal interconnect." Pet., 101 (quoting EX1010 [Yu], 4:30-36). The Petition states that die 52 is "attached . . . to conductive features in the second back side metallization

layer 42, such as by conductive connectors 54, like controlled collapse chip connection (C4) bumps,” and that “[a] connector 54 is a third metal interconnect because it connects die 52 ‘to conductive features’ in layer 42.” Pet., 101 (quoting EX1010 [Yu], 4:30-34).

Whether connector 54 connects die 52 to layer 42 is not the point. EX2018 [Ricketts Decl.], ¶177. The claims require that the semiconductor chip (alleged to be die 52) *comprise* (be part of) the “third metal interconnect” (alleged to be connector 54). Connector 54, however, is not part of die 52. *Id.* Petitioners ignore that connector 54 is described as a material deposited on (bonded to) the layer 42 and then die 52 is attached to the connector.

[A] second die 52, such as a memory die...is attached through the opening 46 to conductive features in the second back side metallization layer 42, such as by conductive connectors 54, like *controlled collapse chip connection (C4) bumps*. The second die 52 may be attached using an acceptable pick-and-place tool and *reflowing connectors 54* between the second die 52 and the conductive features in the second back side metallization layer 42. Accordingly, the connectors 54 may be a *bump on trace (BOT)*.

EX1010 [Yu], 4:30-39. C4 bumps, reflowing connectors, and BOTs are all features that are deposited on layer 42. These type of connectors sit between die 52 (the alleged semiconductor chip) and layer 42 and are used to attach die 52 to layer 42. EX2018 [Ricketts Decl.], ¶177.

By the Petition's own description, Yu's connector 54 is a structure that joins die 52 to the "conductive features in the second back side metallization layer 42" of the package. Pet., 101 (*quoting* EX1010 [Yu], 4:30-34). A POSITA would understand connector 54 to sit between the die and the package metallization, serving to connect the two. EX2018 [Ricketts Decl.], ¶178. It is not a layered metal interconnect formed on a metal pad of die 52. *Id.*

Indeed, Dr. Shanfield admits that connector 54 sits between die 52 and layer 42 and, thus, connector 54 is not part of die 52 (the alleged semiconductor chip).

The "basic idea of C4 is to connect chips (semiconductor devices), chip packages, or such other units by means of *solder bumps between two surfaces* of the units." EX1129 at 1:9-17. The "tiny bumps of electrically conductive solder *bridge the gaps between respective pairs of metal pads on the units being connected*. Each pad has a corresponding pad on the other unit's surface; the pad arrangements are mirror images. *As the units are pressed together and heated the solder bumps on the pads of the first unit are contacted with corresponding conductive pads (having no bumps) on the second unit and reflowed, partially collapsing the solder bumps and making connections between respective pads*" EX1129 at 1:17-26. EX1003 [Shanfield Decl.], ¶70 (emphasis added). Thus, connectors 54 are not part of die 52 and the claim limitation is not met.

As with Sundaram, this follows in part from the fact that Yu does not describe the pads or interconnects of the die it identifies. EX2018 [Ricketts Decl.], ¶181. The Petition does not identify any disclosure in Yu of a metal pad on die 52. EX2018 [Ricketts Decl.], ¶181. Instead, the Petition states that “a POSITA would have understood die 52 includes die pads (unlabeled) such that an electrical connection is made between die 52 and other devices.” Pet., 101; EX1003 [Shanfield Decl.], ¶¶316-319. The Petition supports that proposition with an assumption about what a die would include and with EX1129 rather than with any teaching of Yu. Pet., 101. But relying on background knowledge of a POSITA to supply missing claim limitations in this manner is impermissible. 37 C.F.R. §42.104(b)(4); Background Knowledge Memo.

Dr. Shanfield’s declaration maps Yu’s connector 54 in two inconsistent ways. EX2018 [Ricketts Decl.], ¶182. For limitation 1(e)(i), Dr. Shanfield first identifies connector 54 as the “third metal interconnect,” resting on a separate, undisclosed “metal bond pad underlying each C4 bump.” EX1003 [Shanfield Decl.], ¶¶316-319. Dr. Shanfield asserts that a POSITA would infer the existence of this undisclosed component “since such pads are required for reliable solder attachment.” *Id.*, 317. In the paragraphs that immediately follow, however, Dr. Shanfield identifies connector 54 itself as the claimed pad, stating that “Yu already teaches die 52 comprising connector 54, i.e., the claimed first pad,” and that a

POSITA “would have been motivated to modify Yu’s connector 54 to be a first metal pad.” EX1003 [Shanfield Decl.], ¶¶320-321. The same structure cannot be both the “third metal interconnect” and the “first metal pad” on which limitation 1(e) requires the third metal interconnect to sit. EX2018 [Ricketts Decl.], ¶182. This inconsistency confirms that the Petition has not identified in Yu a “third metal interconnect on a first metal pad of said first semiconductor chip,” and that the alleged metal pad is an assumption drawn from Dr. Shanfield’s assumptions and from EX1095 rather than a disclosure of Yu. *Id.* But again, supplying limitations completely missing from the prior art based on a POSITA’s background knowledge is impermissible. 37 C.F.R. §42.104(b)(4); Background Knowledge Memo.

The Petition’s reliance on Lin-191 for the “metal pad” does not remedy the deficiency regarding a different component—“third metal interconnect,” for the reasons discussed above in connection with limitation 1(e)(i) of Ground 1A. *Supra*, §V.A.1.

2. Yu and Lin-191 Do Not Teach or Suggest the Layered “Third Metal Interconnect” and There Is No Motivation to Combine.

Limitation 1(e)(ii) requires that “said third metal interconnect comprises a third metal layer on said first metal pad and a third copper layer over said third metal layer, wherein said third copper layer has a thickness between 5 and 30 micrometers.” EX1001 [’763 Patent], cl. 1. For the internal layering, the Petition

does not rely on Yu. Instead, it relies on Lin-191 and expressly incorporates its Ground 1A analysis: “Lin-191 teaches or renders obvious interconnects/bumps with layers/thickness as recited in Claim 1(e)(ii). See Section V.A.19.” Pet., 102. For the reasons discussed above in connection with limitation 1(e)(ii) of Ground 1A (*Supra*, §V.A.2), Lin-191 does not supply the claimed “third metal layer.” Its adhesion layer 711 and seed layer 712 are two distinct layers of different materials serving different functions. EX1005 [Lin-191], [0389]-[0392]. EX2018 [Ricketts Decl.], ¶184. The Petition’s merger of these layers and treating them as a single layer is inconsistent with its own mapping of claim 7 and limitation 1(d)(i). Pet., 19, 49; EX2018 [Ricketts Decl.], ¶184.

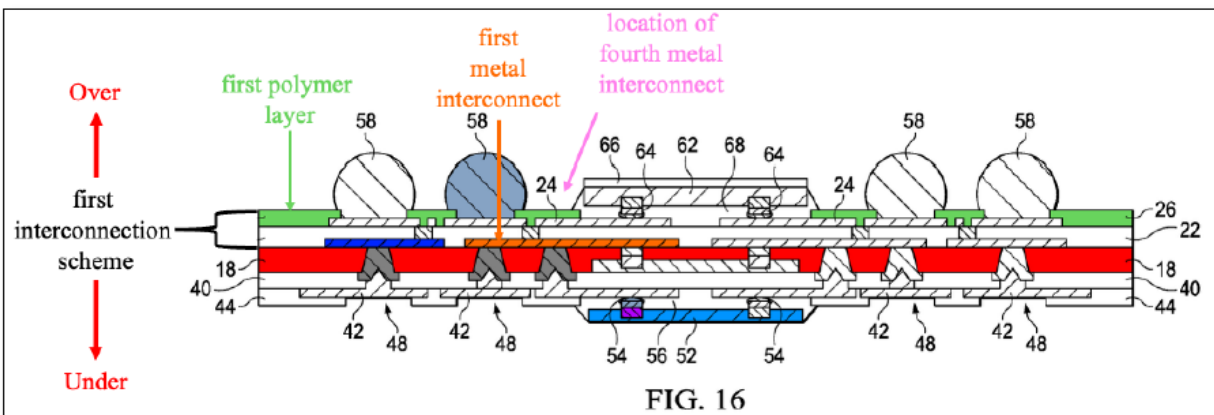
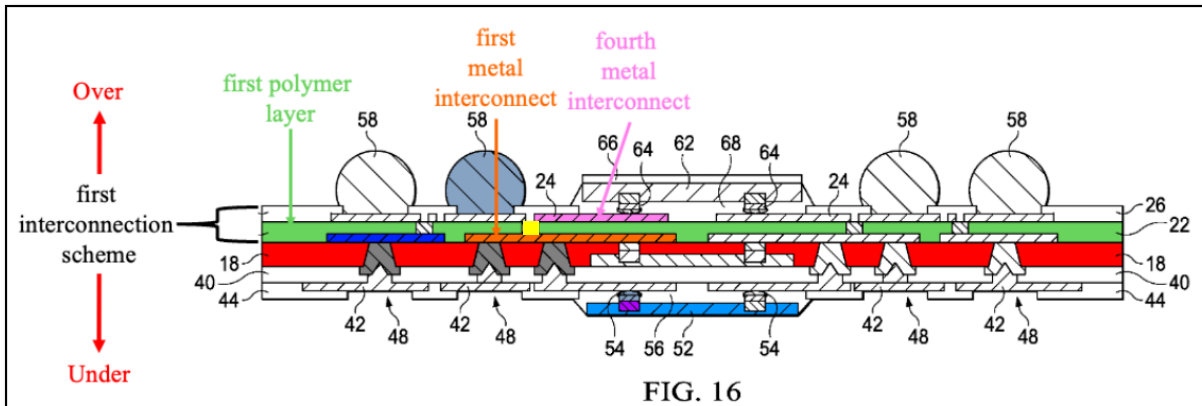
The Petition’s reliance on Yu’s connector 54 introduces a further problem. The Petition identifies connector 54 as a “controlled collapse chip connection (C4) bump[.]” Pet., 101 (quoting EX1010 [Yu], 4:30-34). A POSITA would understand a C4 bump to be composed primarily of solder, in contrast to a layered structure of an adhesion layer, a seed layer, and a thick electroplated copper layer of the kind Lin-191 describes and limitation 1(e)(ii) requires. EX2018 [Ricketts Decl.], ¶185. The Petition does not explain how a C4 solder bump would be reconstructed to comprise “a third metal layer on said first metal pad and a third copper layer . . . between 5 and 30 micrometers,” and Yu does not describe connector 54 as having that construction. EX2018 [Ricketts Decl.], ¶185.

As to motivation, the Petition states that “[a] POSITA would have found obvious and been motivated to modify Yu’s connector for the reasons discussed with respect to Sundaram, i.e., improved metallurgical bonding and increased resistance to fatigue and stress-induced failure.” Pet., 102. Because the rationale is the same as for Sundaram, the deficiencies identified in Ground 1A apply here as well: Lin-191 does not attribute the asserted advantages to its adhesion and seed layers, and the Petition identifies no specific diffusion, oxide, or adhesion problem with Yu’s connector that Lin-191’s added layers would remedy. EX2018 [Ricketts Decl.], ¶186. The Petition’s further assertion that “[l]ayered bumps, per Lin-191, were routinely manufactured using techniques contemplated by Yu” Pet., 103, establishes at most that such bumps were known, not that a POSITA would have reconstructed Yu’s C4-bump connector into the specific layered “third metal interconnect” the claim recites. EX2018 [Ricketts Decl.], ¶186.

3. The Petition Does Not Identify A “First Metal Interconnect” and a “Fourth Metal Interconnect.”

Claim 7 requires a “first metal interconnect” and “a fourth metal interconnect.” As shown below, the Petition identifies the “first metal interconnect” in orange. The Petition identifies the “fourth metal interconnect” as “second metallization layer 24” (pink in the upper figure below) or “a third metallization layer” on layer 26 (abstractly notated by “location of fourth metal interconnect” in

pink in the lower figure below). Pet. 110-111 (citing EX1010, 3:28-35; EX1003, ¶¶336-338).



The claim requires both a first metal interconnect and a fourth metal interconnect—that is, the claim requires two separate interconnects. As discussed below, what the Petition identifies as the first metal interconnect and the fourth metal interconnect are actually different metal layers that are part of one (the same) metal interconnect. Thus, the Petition has not identified two separate interconnects—a first and fourth interconnect. EX2018 [Ricketts Decl.], ¶188.

The '763 Patent distinguishes the metal interconnects of an interconnection scheme by the separate conductive path each provides, and not by vertical position within a single conductive path. EX2018 [Ricketts Decl.], ¶189. Claim 1 illustrates that usage, reciting that “said first metal interconnect is connected to a first copper plug of said plurality of copper plugs” and that “said second metal interconnect is connected to a second copper plug of said plurality of copper plugs.” EX1001 ['763 Patent], cl. 1. A POSITA would understand from that recitation that the metal interconnects of the first interconnection scheme are separate conductive paths, each routing to a different copper plug, rather than two vertically stacked portions of one path. EX2018 [Ricketts Decl.], ¶189.

Claim 7 confirms that the first and fourth metal interconnects are separate. Claim 7 recites “a fourth metal interconnect over said first metal interconnect and said first polymer layer, wherein said first polymer is between said first and fourth metal interconnects.” EX1001 ['763 Patent], cl. 7. The claim thus places the first polymer layer between the first and fourth metal interconnects and recites no electrical connection between them. A POSITA would understand claim 7 to require a fourth metal interconnect that is a separate interconnect from the first metal interconnect, not an upper level of the same conductive path. EX2018 [Ricketts Decl.], ¶190.

The Petition, however, identifies the “first metal interconnect” as a portion of Yu’s first metallization layer 20 and the “fourth metal interconnect” as Yu’s second metallization layer 24 (or a further metallization layer). Yu describes metallization layers 20 and 24 (and a further metallization layer) as successive levels of a single redistribution structure—the metallization layers that the Petition points to are in the same conductive path. EX2018 [Ricketts Decl.], ¶191. Thus, they are part of the same metal interconnect and cannot be two different metal interconnects as required by the claim.

Yu states that “[a] first ILD layer 22 is deposited on the front side and over the first metallization layer 20,” that “[o]penings may be formed through the first ILD layer 22 to the first metallization layer 20,” and that “[c]onductive material deposited during the formation of a subsequent metallization layer may be deposited in openings of the previously formed ILD layer to electrically couple respective metallization layers.” EX1010 [Yu], 3:20-32.

The conductive material occupying the openings in the first ILD layer 22 joins the first metallization layer 20 and the second metallization layer 24 into a single conductive path. Those two portions are not separate conductive paths. They are an upper and a lower portion of the same path, and a signal entering one portion passes directly into the other. A POSITA would not understand vertically stacked, electrically coupled portions of one conductive path to be the separate

“first metal interconnect” and “fourth metal interconnect” that claim 7 requires.

EX2018 [Ricketts Decl.], ¶193.

Indeed, the Petition’s mapping depends on the very connection that claim 7 forecloses. The Petition relies on Yu’s teaching that successive metallization layers are “electrically couple[d]” through the conductive material in the ILD openings. EX1010 [Yu], 3:25-32. But claim 7 requires the first polymer layer to lie between the first and fourth metal interconnects, with no connection between them recited. The structure the Petition identifies—two metallization layers joined through the intervening dielectric—is therefore not the separate first and fourth metal interconnect claim 7 requires. EX2018 [Ricketts Decl.], ¶194. They are different layers of the same interconnect.

For these reasons, the Petition has not shown that Yu teaches or suggests the “fourth metal interconnect” of claim 7. When the Petition identifies the claimed “first metal interconnect” as a portion of metallization layer 20 and the claimed “fourth metal interconnect” as metallization layer 24, it is identifying two layers of the *same* metal interconnect. EX2018 [Ricketts Decl.], ¶195. The Petition has identified only one metal interconnect but the claim requires two metal interconnects.

E. Ground 2B (Yu, Lin-191, and Sundaram)

1. Independent Claim 18 and Its Dependent Claims.

Ground 2B challenges claims 6, 16, and 18-21 and 23 over Yu, Lin-191, and Sundaram. For claim 18, the Petition again relies on the same mapping that it uses for claim 1. Pet., 122-129. For the reasons given above in Ground 2A in connection with limitation 1(e), and in Ground 1A in connection with limitation 1(e)(ii), the Petition has not shown that the limitations of claim 18 have been met. EX2018 [Ricketts Decl.], ¶196.

The Petition adds Sundaram to Yu and Lin-191 for certain limitations of claims 6, 16, and 18-21 and 23. Pet., 122-129. The addition of Sundaram—for a second semiconductor chip, a passive component, or the interposer material—does not cure the deficiency regarding the “first semiconductor chip.” EX2018 [Ricketts Decl.], ¶197. The dependent claims of Ground 2B therefore fail with claim 18, and, to the extent the Petition’s passive-component and interposer-material positions rely on the same Sundaram Figure 33 and Figure 3 mappings addressed above, they fail for the additional reasons given in Ground 1A.

F. Ground 2C (Yu, Lin-191, Lin-863)

Ground 2C alleges claim 13 is obvious over Yu, Lin-191, and Lin-863. Ground 2C fails at least for the reasons discussed above at §V.B for Lin-863 and §V.D for Yu and Lin-191 for underlying claim 1.

G. Claim 22

Grounds 2A-2C do not challenge dependent claim 22. Thus, Grounds 2A-2C cannot demonstrate claim 22 is unpatentable.

VI. CONCLUSION

For at least the foregoing reasons, Petitioners have failed to demonstrate by a preponderance of the evidence that any challenged claim is unpatentable.

Dated: August 21, 2026

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CERTIFICATE OF COMPLIANCE

Pursuant to 37 C.F.R. § 42.24(d), Patent Owner certifies that this Patent Owner Response has 13,291 words as counted by the word-processing system used to prepare this document. This word count complies with the 14,000 word limit under 37 C.F.R. § 42.24(b)(1).

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CERTIFICATE OF SERVICE

The undersigned hereby certifies that the foregoing PATENT OWNER'S RESPONSE was served electronically via email on August 21, 2026, on the following counsel of record for Petitioners:

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