



OPEN Enhancing bonding strength of the electroplated Cu pillars for semiconductor package by controlling grain orientation

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The Cu pillar bump, an electrode formed on a silicon chip, connects the devices inside a high bandwidth memory (HBM) package and is the most important interconnection affecting the electrical, thermal, and mechanical properties of advanced semiconductor package. Recently, the number of input/output (I/O) in HBM packages has been increasing and the fine pitch of Cu pillar is also becoming significantly smaller. Therefore, the bonding strength between electrodes is deteriorating due to the increase in interconnection density and fine pitch, which threatens the reliability of semiconductor packages. Also, the bonding strengths between Cu pillars, electrodes inside HBM package are greatly affected by the plating process, package temperature, interconnection technology, package process, as well as thermal expansion coefficient of materials, crystal structure and orientation of the material, and electrochemical reaction while using electronic packages. After Ti is sputtered as a bonding layer and Cu is sputtered as a seed layer onto the Si chip electrode, and finally, Cu pillar bumps (25 μm in diameter, 55 μm in pitch) are formed through electroplating. When the Cu seed layer is removed by etching, leaving only the electrode portion of chip, the Cu pillar bump is completed, but an undercut occurs at the interface of Cu pillar and Cu seed layer during the etching process of Cu seed layer. Electroplating process of Cu pillar bump was performed at conditions of 3.0, 8.0 and 13.0 A/dm² (ASD). However, the grain size and the orientation of Cu pillar bumps changed significantly depending on the electroplating current density, and the undercut length also varied accordingly. The orientations and the grain sizes of Cu pillar bump was analyzed by EBSD and SEM, respectively. The grain orientation of the Cu filler bump was (111) at a current of 3.0 ASD, and the (100) and (110) orientations of the Cu filler bump were mainly formed at current conditions of 8.0 and 13.0 ASD. Also, the grain size of the Cu filler bump was 2.77 μm when the current density was 3.0 ASD, and 0.93 μm at current density of 13.0 ASD. Length of the undercut etched at the interface of Cu pillars and Cu pad of Si chip increased from 0.43 μm at 3.0 ASD to 1.72 μm at ASD 13.0. Thus, shear strength of Cu pillar bump decreased rapidly from 35.77 gf to 17.65 gf. This study is expected to contribute greatly to improving the reliability of next generation semiconductor packages by clarifying the correlation between electroplating conditions, orientation of grain in Cu pillar, and shear strength of Cu pillar bump.

Keywords Cu pillar bump, Electroplating, Current density, Undercut, Mechanical stress

The growing demand for high-speed data processing in artificial intelligence, high-performance computing, and advanced 2.5D or 3D integration has significantly increased the required chip input and output density. To meet these requirements within limited die footprints, fine-pitch interconnect technologies have become essential. Traditional solder bumps have long been the standard in flip-chip packaging. However, their mechanical

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limitations, especially at pitches below 100 μm , such as reduced stand-off height and limited I/O density, make them unsuitable for next-generation semiconductor packaging. In contrast, Cu pillar bump technology offers a promising alternative that enables finer pitches and provides improved electrical, thermal, and mechanical performance^{1,2}.

Cu pillar bumps consist of a rigid electroplated Cu column with a thin solder layer on top. This structure allows for precise control of bump geometry and stand-off height and also improves signal integrity and current-carrying capability. The microstructural characteristics of the electroplated Cu, particularly its grain size and crystallographic orientation, are key factors in determining the mechanical reliability of the bump and its behavior during subsequent processing steps. Many studies have shown that electroplating current density significantly influences the grain structure of Cu. Higher current densities typically lead to finer grains and changes in crystallographic texture. These microstructural changes affect not only the intrinsic mechanical strength of the Cu pillar but also its behavior in downstream processes such as wet etching³.

In particular the seed-layer etching step is critical for defining the final bump profile and can lead to undesirable undercut formation as isotropic etching progresses laterally beneath the electroplated pillar^{4,5}. This geometric discontinuity reduces the effective contact area at the bump base and serves as a local stress concentrator, increasing the risk of interfacial delamination or crack initiation under thermal and mechanical loads⁶. Furthermore, recent studies have shown that the crystallographic orientation of Cu grains strongly influences their etch resistance. (111)-oriented surfaces exhibit slower etch rates and maintain more stable morphologies than other orientations^{7,8}. These observations indicate that the microstructural evolution during Cu electroplating directly affects undercut formation and, consequently, the mechanical reliability of Cu pillar bumps.

As the dimensions of electronic packaging continue to shrink, modern fine-pitch Cu pillar electroplating demands stringent specifications, including void-free filling, high coplanarity (uniform pillar height), and excellent geometric fidelity. Meeting these complex requirements relies not only on process parameters like current density but also critically on the electrolyte composition. Various additives, such as accelerators, suppressors, and levelers, are employed to modulate nucleation and growth behaviors, thereby controlling grain size and inducing specific crystallographic orientations. Accelerators facilitate charge transfer and lower the overpotential to enhance the plating rate. For instance, Bis-(3-sulfopropyl) disulfide (SPS), a typical accelerator, contributes to reducing surface roughness. Kao et al. demonstrated that tuning the SPS concentration effectively controls the microstructure, resulting in significant changes in grain size and mechanical properties via the Hall–Petch effect⁹. Levelers are essential for ensuring surface flatness and coplanarity. Zhu et al. evaluated the impact of levelers on Cu pillar morphology and highlighted their critical role in preventing void formation and ensuring compatibility with solder caps¹⁰. Furthermore, the synergistic effect of combining these additives is crucial. Wang et al. showed that optimizing the additive combination improves plating efficiency and secures a compact deposition structure with enhanced corrosion resistance¹¹. Beyond chemical additives, process parameters such as pulse plating also play a significant role. Mariani et al. verified that pulsed current and pulsed reverse current significantly enhance the hardness and microstructural homogeneity of Cu deposits¹². Additionally, the behavior of impurities derived from additives is significant. Meiners et al. reported that sulfur impurities specifically segregate at grain boundaries, inhibiting grain growth. However, excessive accumulation can lead to stress concentration and embrittlement¹³. As established above, the final microstructure and texture in Cu electroplating are determined by a complex interplay of the additive package, current mode, and impurity behavior. Therefore, to clarify the fundamental deposition mechanism without these confounding variables, this study utilized a commercial electrolyte with a fixed additive package. By doing so, we deliberately focused on isolating and identifying the specific influence of current density on the grain size and crystallographic orientation of Cu pillars.

Cu pillars with a diameter of 25 μm and a pitch of 55 μm were fabricated under various current density conditions. Electron backscatter diffraction (EBSD) was utilized to characterize the crystallographic orientation and grain structure of the electroplated Cu. Undercut dimensions were quantitatively measured following seed-layer etching. The mechanical integrity of the joints was evaluated through shear testing, while interfacial stress distributions were analyzed using technology computer-aided design (TCAD) simulations. This integrated analysis elucidates the interplay between electroplating conditions, microstructure, and interfacial reliability, providing a foundation for optimizing Cu pillar bump fabrication in advanced semiconductor packaging.

Experimental

Cu pillar bump fabrication

Cu pillar bumps with a diameter of 25 μm and a pitch of 55 μm were fabricated on Ti/Cu seed layers deposited by sputtering, followed by selective photolithography and electroplating¹⁴. A commercial acidic copper electrolyte (Mitsubishi Chemical, Japan) formulated for high throwing power and fine-pitch filling was used. The plating process was conducted at room temperature under acidic conditions (pH 1–2). Accordingly, the cross-sectional texture evolution observed in the Cu pillars should be interpreted as dependent on the specific plating chemistry and operating window, and it may not be directly generalized to other bath formulations. Electroplating was carried out at three current densities (3.0, 8.0, and 13.0 ASD) to grow Cu pillars within the patterned openings. A thin Ni layer was electroplated between two Cu layers to serve as a diffusion barrier and suppress excessive intermetallic compound formation, after which additional Cu was deposited to complete the Cu–Ni–Cu multilayer¹⁵. A Sn–1.8 wt% Ag solder alloy was then plated to form a solder cap, and the photoresist was removed, yielding Cu–Ni–Cu–solder pillar bumps with a height of 38 μm , as shown in Fig. 1; Table 1. After photoresist removal, the exposed Ti/Cu seed layers were etched using a mixture of H_2SO_4 and H_2O_2 solution. During the etching process, isotropic dissolution formed undercuts at the bottom region of the Cu pillar bump.

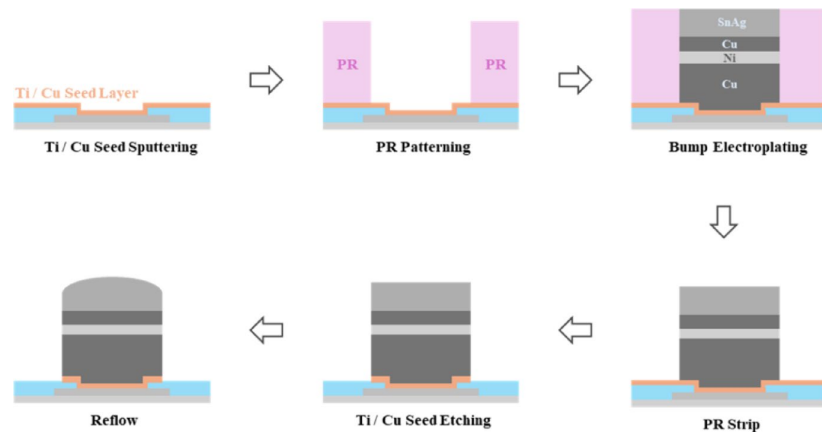


Fig. 1. Schematic of the Cu pillar bump fabrication process.

Parameter	Dimension
Pitch	55 μm
Diameter	25 μm
Solder Cap (Sn-1.8Ag)	12 μm
Height	38 μm
UBM Thickness (Ti/Cu)	0.1 μm /0.3 μm

Table 1. Detailed dimensions of the Cu pillar bump.

The undercut length increased from 0.43 μm to 1.72 μm as the plating current density was raised from 3.0 to 13.0 ASD.

Microstructural characterization

Undercut formation at the base of the Cu pillar bumps was examined using a field-emission scanning electron microscope (FE-SEM, Helios 5 DualBeam, Thermo Fisher, USA). Undercut lengths were measured directly from FE-SEM images to assess variations induced by different electroplating current density conditions. To investigate the internal microstructure of the Cu pillars, cross-sectional specimens were prepared using focused ion beam (FIB) milling. A Ga^+ ion beam was applied perpendicular to the Cu pillar surface with controlled width and depth, enabling precise exposure of the internal structure for further analysis.

EBSD (ZEISS GeminiSEM 460) was employed to analyze the crystallographic orientation and average grain size within the Cu pillar bumps. EBSD analysis of Cu pillar bumps revealed detailed microstructural characteristics, including orientation distribution, texture, and grain size. By comparing the microstructures of Cu pillar bumps fabricated under different electroplating current densities, the effect of current density on the grain growth orientation of Cu pillar bump was investigated. The correlation between current density and orientation of Cu pillar bump was elucidated, and the effect of grain growth orientation on undercut formation was systematically investigated to contribute to improving the reliability of 3D semiconductor packages.

Mechanical characterization

Shear test was conducted to evaluate the adhesion strength of Cu pillar bump with different current densities. Shear tests were conducted using a shear system (DAGE 4000Plus, Nordson, UK) based on JEDEC22-B117 standard with a shear speed of 300 $\mu\text{m/s}$ and a probe height of 12 μm (Fig. 2). To ensure statistical reliability, shear tests were conducted directly on the wafer level with a sample size of 100 bumps for each current density condition. Outliers were rigorously excluded to minimize experimental error. Additionally, for the evaluation of undercut length, 30 randomly selected bumps were analyzed per condition to ensure data representativeness.

The fracture surface of the Cu pillar bump was subsequently analyzed by FE-SEM to determine the failure mode. To investigate the effect of undercut geometry on the stress distribution within the Cu pillar bumps, three-dimensional TCAD simulations were performed. The geometric model was constructed to replicate the dimensions of the fabricated samples, consisting of a cylindrical Cu pillar on a silicon substrate. Crucially, to reflect the experimental etching results, specific undercut geometries were introduced at the Cu/seed-layer interface. Undercut lengths were modeled as 0.43 μm , 1.06 μm , and 1.72 μm , corresponding to the distinct structures observed at current densities of 3.0, 8.0, and 13.0 ASD, respectively. Regarding material properties, this study adopted an isotropic linear elastic model for the Cu pillar. This simplification is justified because the mechanical failure in this system is primarily governed by the geometric stress concentration caused by

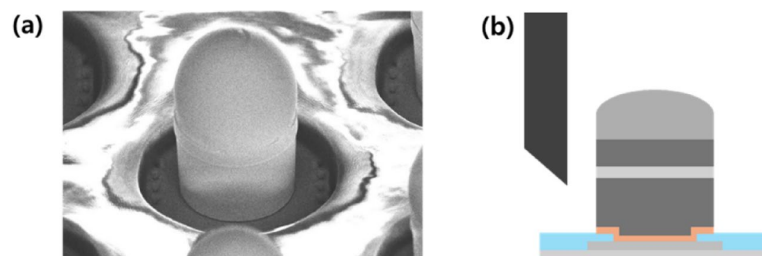


Fig. 2. (a) SEM micrograph of the Cu pillar bump before shear test. (b) Cross-sectional schematic of the boundary conditions of a Cu pillar bump.

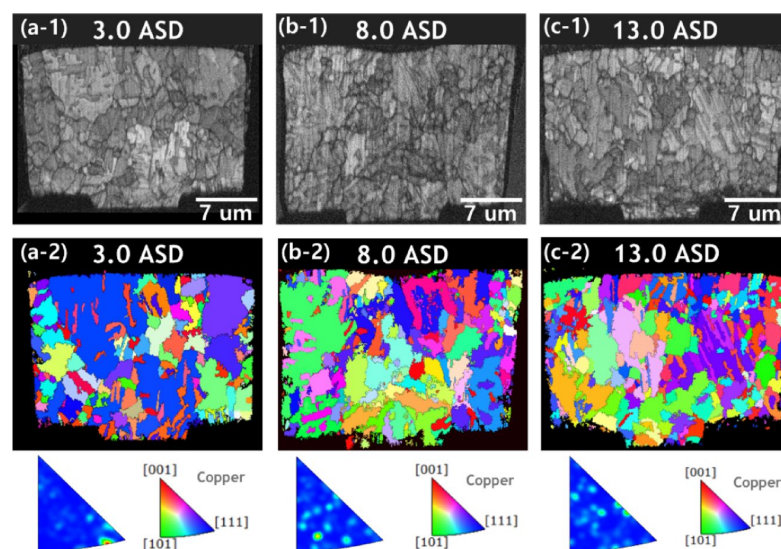


Fig. 3. EBSD Image Quality (IQ) maps of the Cu pillar bump cross-section under various ASD conditions: (a-1) 3.0, (b-1) 8.0, and (c-1) 13.0, EBSD inverse pole figure (IPF) maps of the Cu pillar bump cross-section under various ASD conditions: (a-2) 3.0, (b-2) 8.0, and (c-2) 13.0.

the undercut effect, rather than by crystallographic orientation-dependent stiffness. The Young's modulus and Poisson's ratio for the Cu pillar were assigned as 115 GPa and 0.34, respectively.

Boundary conditions were defined to simulate the destructive shear test conditions. The bottom surface of the substrate was fixed, and a lateral load was applied via a rigid shear tool. The shear tool, characterized by a tip width of 27 μm , was positioned at a shear height of 12 μm from the substrate surface. A total force of 20.1 g was applied to the contact interface, and the resulting equivalent stress distribution was analyzed to identify critical failure initiation sites.

Results and discussions

Microstructural evolution via EBSD analysis

Figure 3a-1 ~ c-1 show Image Quality (IQ) maps of Cu pillar bumps electroplated under various current densities, 3.0, 8.0 and 13 ASD, revealing variations in bump morphology. To quantitatively assess the microstructural differences, EBSD analysis was performed to evaluate grain size, crystallographic orientation, and texture. A high indexing rate of approximately 98.7% was achieved within the region of interest, ensuring the statistical reliability of the EBSD data even for the fine-grained structures. Figure 3a-2 ~ c-2 shows the EBSD inverse pole figure (IPF) maps for Cu pillars plated under varying current densities. The Cu pillar bump with (111) orientation was formed under the electroplating condition of 3.0 ASD, as shown in Fig. 3-a-2. Approximately 88% of the grains in the Cu pillar bumps are oriented along the (111) orientation, indicating a pronounced preferential crystallographic orientation, as shown in Table 2.

Figure 4 shows the average grain sizes for Cu pillar bumps plated at different current densities. At 3.0 ASD (Fig. 4a), the mean grain size is approximately 2.77 μm , whereas at 13.0 ASD (Fig. 4c), it decreases sharply to around 0.93 μm . These results indicate a significant reduction in grain size as current density increases^{16–18}. The observed texture evolution from a strong (111) orientation to a mixed orientation can be elucidated by the competition between the nucleation rate and the crystal growth rate, which is governed by the cathodic

Unit: %	3.0 ASD	8.0 ASD	13.0 ASD
(111)	87.7	39.8	25.6
(110)	5.9	32.6	38.6
(100)	2.8	21.5	22.3
Others	3.6	6.1	13.5

Table 2. Percentage of crystallographic orientations in the Cu pillar cross-sections at different ASD conditions.

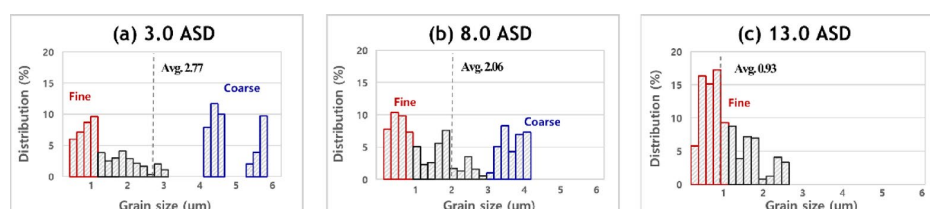


Fig. 4. Grain size distributions of the Cu pillar cross-sections at different ASD conditions: (a) 3.0, (b) 8.0, and (c) 13.0.

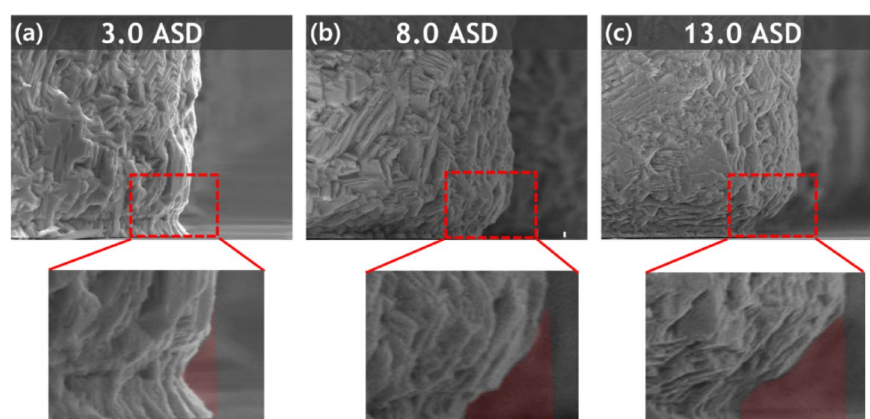


Fig. 5. SEM micrographs of undercut formation in Cu pillars at different ASD conditions: (a) 3.0, (b) 8.0, and (c) 13.0.

overpotential. At a low current density of 3.0 ASD, the relatively low overpotential favors the growth mechanism over nucleation. This condition provides sufficient time for Cu adatoms to diffuse across the surface and arrange themselves into the thermodynamically most stable configuration. Consequently, the grains preferentially grow along the close-packed (111) plane, which possesses the lowest surface energy in the FCC system^{19–22}.

In contrast, the high current density of 13.0 ASD induces a high overpotential, providing a large driving force that exponentially increases the nucleation rate. The rapid deposition creates numerous fine grains and effectively restricts the surface diffusion of adatoms to the lowest-energy sites³. As a result, kinetically trapped orientations with higher surface energies, such as (100) and (110), are formed alongside (111), leading to the random texture observed in the EBSD analysis²¹.

As a result, bumps plated at low current densities exhibit large columnar grains with a strong (111) orientation, while those plated at high current densities develop an isotropic microstructure composed of ultrafine grains. These microstructural differences are expected to significantly influence both the seed-layer etching process and the mechanical performance of the Cu pillar bumps^{23–26}.

Undercut formation after seed-layer etching

During the etching process, undercutting tends to occur at the interface between the Cu pillar bump and the Cu/Ti seed layer due to their difference in current density. In fact, undercutting was primarily observed at the interface between the electroplated Cu columns and the underlying Cu/Ti seed layer. Figure 5 shows the undercut formation at the base of Cu pillar bumps following seed-layer etching, with the extent of undercut varying significantly depending on the plating current density. Specifically, Fig. 5b and c shows that bumps plated at higher current densities increase undercuts with lengths exceeding 1 μm.

Figure 6 compares undercut lengths under different plating conditions. At 3.0 ASD the bump exhibits a minimal undercut length of less than $0.5\ \mu\text{m}$. At 8.0 ASD lateral etching reaches approximately $1.06\ \mu\text{m}$ at the bump perimeter while at 13.0 ASD, the bump displays a pronounced undercut averaging $1.72\ \mu\text{m}$, resulting in a distinct.

The significant disparity in the undercut extent can be rationalized by the microstructural differences induced by the current density, specifically grain size and the resulting grain boundary density. In wet etching processes generally considered isotropic, grain boundaries act as thermodynamically unstable regions characterized by high defect densities and elevated free energies²⁷. Furthermore, these boundaries serve as rapid diffusion channels for the etchant, facilitating deeper penetration into the material. Consequently, a higher density of grain boundaries promotes preferential electrochemical dissolution and accelerates lateral etching. It is well established that grain refinement significantly increases the grain boundary area, which serves as the primary driving force for enhanced etch rates in copper wet etching processes, a mechanism consistent with previous findings²².

While crystallographic orientation can theoretically influence surface reactivity due to differences in planar atomic density, its impact is considered secondary to the dominant effect of grain boundaries in this specific etchant system^{8,28}. In this study, the increase in ASD promoted rapid nucleation, leading to significant grain refinement. As shown in Fig. 4, the 13.0 ASD condition exhibited the finest grain size ($0.93\ \mu\text{m}$) and, consequently, the highest grain boundary density. This microstructural feature correlates directly with the most severe undercut observed in Fig. 6, confirming that the grain boundary-driven mechanism is the dominant contributor to the accelerated etching at high current densities. Ultimately, such excessive undercut reduces the effective bonding area, which may serve as a potential detriment to the mechanical reliability of the interconnects⁵.

Shear test results

A shear test was performed to assess the impact of undercut formation on the mechanical reliability of Cu pillar bump interconnections. As shown in Fig. 7, bumps plated at lower current densities sustained higher shear loads than those plated at higher densities. The bump formed at 3.0 ASD exhibited a shear force of approximately 35.77gf, significantly higher than the bump plated at 13.0 ASD. This suggests that increasing the current density from 3.0 to 13.0 ASD reduces shear force by nearly 50%. A general decline in shear force was observed with increasing current density, likely due to the intensified undercut defects along the bump sidewalls, which reduce the effective bonding area and concentrate local stresses at the bump perimeter, promoting shear failure.

Fracture surface observations after shear testing revealed distinct failure modes depending on the plating current density. Figure 8 shows SEM images of Cu pillar bumps after shear testing. The fracture of the Cu pillar bump electroplated at 3.0 ASD (Fig. 8a) propagates within the Cu pillar bump matrix, exhibiting a ductile failure mode. In contrast, at higher current densities such as 8.0 and 13.0 ASD, the fracture mainly occurs along the undercut, showing an adhesive failure mode. The increased undercuts caused by higher current densities reduce the effective bonding area between the Cu pillar bump and Cu/Ti seed layer, concentrating local stresses and facilitating crack initiation along the undercut below Cu pillar bump^{4,5,29}.

Several studies have shown that grain refinement in electroplated Cu can enhance intrinsic material strength, as described by the Hall–Petch relation. Although the bumps electroplated at 8.0 and 13.0 ASD exhibited refined grains, their shear strength was significantly reduced by geometric undercuts and weakened interfaces⁶. In contrast, the bump plated at 3.0 ASD with larger grains and a (111) texture showed higher ductility and fewer undercuts, resulting in a more uniform stress distribution and a relatively higher fracture load. This indicates that, in this study, the strengthening effect from grain refinement did not dominate the mechanical response of the interconnections, likely due to the presence of defects such as undercuts^{4,30}. In conclusion, while the plating current density can influence the crystallographic properties of Cu pillar bumps, the mechanical reliability of

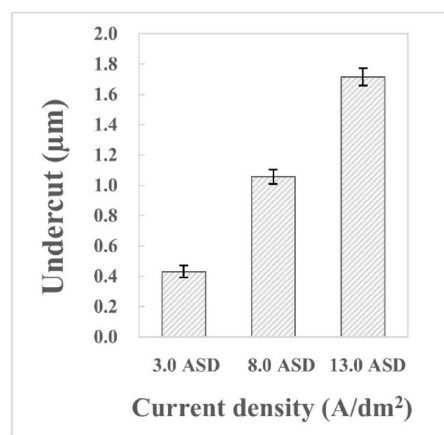


Fig. 6. Undercut length of Cu pillar bumps fabricated at different current densities.

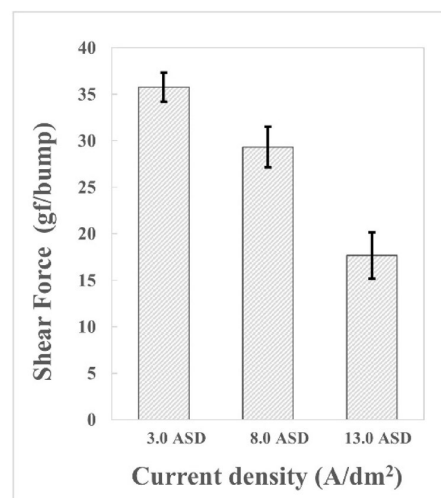


Fig. 7. Shear force of Cu pillar bumps fabricated at different current densities.

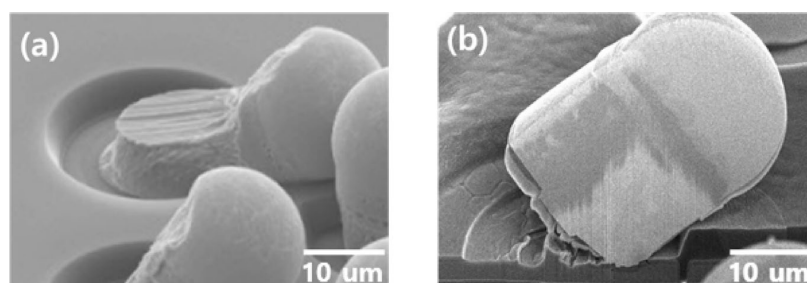


Fig. 8. SEM micrographs of Cu pillar bumps after shear testing: (a) ductile failure mode at ASD 3.0, and (b) adhesive failure mode at ASD 8.0 and 13.0.

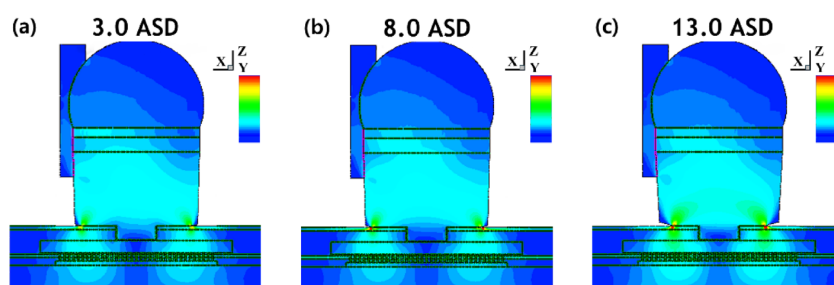


Fig. 9. Finite element simulation results of stress distributions in the Cu pillar bump: (a) ASD 3.0, (b) ASD 8.0, and (c) ASD 13.0.

these structures is primarily determined by geometric defects such as undercuts. These defects outweigh any strengthening effects that may result from microstructural refinement.

TCAD stress analysis results

Although the shear test confirmed that undercut defects reduce the overall joint strength. Therefore, a TCAD-based simulation was employed to more comprehensively examine the stress concentration that occurs in Cu bump interconnections when undercuts are present.

Figure 9 presents the residual stress distribution obtained from the simulation model of the Cu bump and substrate structure, comparing stress profiles with and without undercuts. Notably, in Fig. 9b and c, both

conditions with undercuts exhibit pronounced stress concentrations at the lower edge of the bump. These findings align with the shear test observations, suggesting that undercuts reduce the contact area and concentrate local stresses at the bump perimeter³¹.

Additionally, larger undercuts correspond to increased stress at the lower portion of the bump, which can be attributed to partial loss of contact between the bump base and the substrate. This leads to localized stress concentrations, which qualitatively align with the reduced bond strength observed in shear testing³⁰.

A finite-element study by Long et al. found that a bump with an undercut at its bottom can experience up to an 88% increase in out-of-plane stress⁴. Additionally, as the undercut size grows, higher stress levels are observed due to the reduced contact area between the chip surface and the bump. More importantly, the location of maximum stress coincided with the bump edge, where cracks were observed during shear testing, indicating that undercuts act as microstructural defects that compromise the bump's mechanical integrity.

In conclusion, the presence of an undercut leads to a nonuniform stress distribution at the bump–substrate interface, reducing mechanical reliability. Therefore, minimizing undercut formation and controlling the crystallographic orientation at the bump base are essential for enhancing the overall reliability of Cu bumps³².

Conclusions

This study investigated the influence of plating current density on the microstructure and mechanical reliability of Cu pillar bumps by analyzing their crystallographic orientation undercut morphology and shear strength. Cu pillar bumps were fabricated at three different current densities of 3.0, 8.0 and 13.0 ASD. FIB cross-sectional imaging and EBSD analysis revealed that as the current density increased the grain structure transitioned from large columnar grains with a strong (111) orientation to fine equiaxed grains with mixed orientations.

During seed-layer etching undercut length increased significantly at higher current densities due to the prevalence of grain boundaries and crystal planes more susceptible to chemical etching. The bump electroplated at 3.0 ASD exhibited the highest shear strength whereas the shear strength decreased significantly as the plating current density increased to 13.0 ASD.

Finite element simulations further confirmed that undercuts generate localized stress concentrations at the bump edges which coincide with crack initiation sites observed during shear testing.

In conclusion this study demonstrates that while controlling plating current density can influence grain size and crystallographic orientation the presence of undercut defects serves as a more critical role in determining the mechanical reliability of Cu pillar bumps. It is particularly worth noting that the undercut is an irreversible geometric defect formed during the etching process. Thus, even if grain coarsening occurs during subsequent reflow processes in actual fabrication, the stress concentration induced by the undercut is expected to remain the dominant failure mechanism. Therefore, minimizing undercut formation through optimizing the current density to suppress etch-susceptible crystallographic textures is essential for improving the structural robustness and long-term performance of Cu interconnects in advanced semiconductor packages. This study demonstrated that variations in the applied current density significantly modify the microstructure of Cu pillars, specifically regarding their grain size and preferred crystallographic orientation. These microstructural differences are directly linked to the undercut behavior during seed-layer wet etching and the consequent mechanical reliability. Building upon the results obtained from the fixed current density conditions of 3.0, 8.0, and 13.0 ASD, our future work will extend to a Hybrid-ASD electroplating strategy. For instance, we will explore a multi-step profile that modulates the current density, such as a Low-High-Low sequence, to suppress undercut formation while maintaining a high plating rate. Through this approach, we aim to establish an optimized process window that simultaneously improves process throughput and mechanical reliability, including enhanced shear strength and more stable failure behavior.

Data availability

The datasets used and/or analysed during the current study available from the corresponding author on reasonable request.

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References

1. Fu, L., Bhagavat, M., Selvanayagam, C., Leong, K. & Barber, I. Cu pillar bump development for 7-nm chip package interaction (CPI) technology. *J. Microelectron. Electron. Packag.* **17**, 1–8. <https://doi.org/10.4071/imaps.968260> (2020).
2. Tsao, P. H. et al. in 2016 IEEE 66th Electronic Components and Technology Conference (ECTC) 1148–1153 (2016).
3. Lee, P. T. et al. High-speed electrodeposition for Cu pillar fabrication and Cu pillar adhesion to an Ajinomoto build-up film (ABF). *Mater. Design.* **206** <https://doi.org/10.1016/j.matdes.2021.109830> (2021).
4. Long, X. J., Shang, J. T. & Zhang, L. Design optimization of pillar bump structure for minimizing the stress in brittle low K dielectric material layer. *Acta Metall. Sinica (English Letters)*. **33**, 583–594. <https://doi.org/10.1007/s40195-019-00948-6> (2019).
5. Siow, L. Y. et al. In 2012 IEEE 14th Electronics Packaging Technology Conference (EPTC). 755–758 (IEEE).
6. Fu, L., Bhagavat, M. & Barber, I. in International Symposium on Microelectronics. 000270–000276 (International Microelectronics Assembly and Packaging Society).
7. Steinsland, E., Finstad, T. & Hanneborg, A. Etch rates of (100), (111) and (110) single-crystal silicon in TMAH measured in situ by laser reflectance interferometry. *Sens. Actuators A: Phys.* **86**, 73–80 (2000).
8. Yu, X. et al. Wet anisotropic etching characteristics of Si {111} in KOH-Based solution. *ACS Omega*. **10**, 2940–2948 (2025).
9. Kao, Y. J., Li, Y. J., Shen, Y. A. & Chen, C. M. Significant Hall-Petch effect in micro-nanocrystalline electroplated copper controlled by SPS concentration. *Sci. Rep.* **13**, 428. <https://doi.org/10.1038/s41598-023-27669-2> (2023).
10. Zhu, Q. S., Ding, Z. F., Wei, X. F., Guo, J. & Wang, X. J. Effect of leveler on performance and reliability of copper pillar bumps in wafer electroplating under large current density. *Microelectron. Reliab.* **146** <https://doi.org/10.1016/j.microrel.2023.115030> (2023).

11. Wang, Q., Peng, Y., Mou, Y. & Chen, M. Promotion of High-Speed Copper-Filling performance for interconnections with increasing Aspect-Ratio using compound additives. *Micromachines (Basel)*. 13. <https://doi.org/10.3390/mi13091539> (2022).
12. Mariani, E., Giurlani, W., Bonechi, M., Dell'Aquila, V. & Innocenti, M. A systematic study of pulse and pulse reverse plating on acid copper bath for decorative and functional applications. *Sci. Rep.* **12**, 18175 (2022).
13. Meiners, T., Peng, Z., Gault, B., Liebscher, C. H. & Dehm, G. Sulfur – induced embrittlement in high-purity, polycrystalline copper. *Acta Mater.* **156**, 64–75. <https://doi.org/10.1016/j.actamat.2018.06.013> (2018).
14. Nair, C. et al. In 2015 IEEE 65th electronic components and technology conference (ECTC). 2248–2253 (IEEE).
15. Yu, H. et al. Study on the growth behavior of Ni3Sn4 layer in Cu pillar/Ni/Sn microbump under high-temperature stress. *Mater. Sci. Semiconduct. Process.* **201**, 110058 (2026).
16. Manu, R. & Jayakrishnan, S. Effect of additive and current density on microstructure and texture characteristics of copper electrodeposits. *Int. J. Mater. Res.* **104**, 149–156 (2013).
17. Lai, J. Y. et al. Stress relaxation and grain growth behaviors of (111)-Preferred nanotwinned copper during annealing. *Nanomaterials (Basel)*. <https://doi.org/10.3390/nano13040709> (2023).
18. Fang, C. Y. et al. Effect of electroplating current density on tensile properties of nanotwinned copper foils. *J. Electrochem. Soc.* **169** <https://doi.org/10.1149/1945-7111/ac62be> (2022).
19. Pei, A., Zheng, G., Shi, F., Li, Y. & Cui, Y. Nanoscale nucleation and growth of electrodeposited lithium metal. *Nano Lett.* **17**, 1132–1139 (2017).
20. Yang, Z. H., Wu, P. C. & Chuang, T. H. Effects of substrate bias on the sputtering of high density (111)-nanotwinned Cu films on SiC chips. *Sci. Rep.* **12**, 15408 (2022).
21. Kim, S. J. et al. Flat-surface-assisted and self-regulated oxidation resistance of Cu (111). *Nature* **603**, 434–438 (2022).
22. Zhao, W. et al. Effect of grain boundaries and crystal orientation on etching behavior of 12 µm Thick rolled copper foil. *Mater. Today Commun.* **34**, 105029 (2023).
23. Panigrahi, A. K., Ghosh, T., Vanjari, S. R. K. & Singh, S. G. Demonstration of sub 150°C Cu-Cu thermocompression bonding for 3D IC applications, utilizing an ultra-thin layer of Manganin alloy as an effective surface passivation layer. *Mater. Lett.* **194**, 86–89. <https://doi.org/10.1016/j.matlet.2017.02.041> (2017).
24. Panigrahi, A. K. et al. CMOS In-Line process flow Compatible, sub 100°C Cu–Cu thermocompression bonding using stress engineering. *Electron. Mater. Lett.* **14**, 328–335. <https://doi.org/10.1007/s13391-018-0037-y> (2018).
25. Panigrahi, A. K., Ghosh, T., Vanjari, S. R. K., Singh, S. G. & Oxidation Resistive CMOS compatible Copper-Based alloy ultrathin films as a superior passivation mechanism for achieving 150°C Cu–Cu wafer on wafer thermocompression bonding. *IEEE Trans. Electron. Devices*. **64**, 1239–1245. <https://doi.org/10.1109/ted.2017.2653188> (2017).
26. Panigrahi, A. K., Bonam, S., Ghosh, T., Singh, S. G. & Vanjari, S. R. K. Ultra-thin Ti passivation mediated breakthrough in high quality Cu–Cu bonding at low temperature and pressure. *Mater. Lett.* **169**, 269–272. <https://doi.org/10.1016/j.matlet.2016.01.126> (2016).
27. Lapeire, L., Martinez Lombardia, E., De Graeve, I., Terryn, H. & Verbeken, K. Influence of grain size on the electrochemical behavior of pure copper. *J. Mater. Sci.* **52**, 1501–1510 (2017).
28. Li, Z. et al. Mechanism investigations on water gas shift reaction over Cu (111), Cu (100), and Cu (211) surfaces. *ACS Omega*. **7**, 3514–3521 (2022).
29. Sethu, R. S., Kulkarni, S. H., Ha, H. U. & Soon, K. H. in International Symposium on Microelectronics. 000502–000507 (International Microelectronics Assembly and Packaging Society).
30. Kuechenmeister, F. et al. In International Symposium on Microelectronics. 000173–000179 (International Microelectronics Assembly and Packaging Society).
31. Cerit, M., Kokumer, O. & Genel, K. Stress concentration effects of undercut defect and reinforcement metal in butt welded joint. *Eng. Fail. Anal.* **17**, 571–578 (2010).
32. Zhang, W. et al. in 2012 4th Electronic System-Integration Technology Conference. 1–5 (IEEE).

Author contributions

All authors approved the final manuscript and agree to be accountable for all aspects of the work. J.J.Y. performed methodology and investigation, performed data curation, carried out formal analysis, conducted validation, and wrote the original draft. T.S.S. provided resources and project administration, and contributed to methodology, investigation, data curation, and validation. D.J.K. performed formal analysis and contributed to writing. K.S.P. provided resources and project administration, and contributed to investigation and data curation. D.K.N. provided resources and contributed to methodology and investigation. Y.J.G. provided resources and contributed to methodology, investigation, and data curation. S.B.J. provided supervision and project administration, and contributed to investigation, data curation, and writing.

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Declarations

Competing interests

The authors declare no competing interests.

Ethical approval

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Additional information

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