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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
	Application Number	
	Filing Date	
	First Named Inventor	Ping-Jung Yang
	Art Unit	
	Examiner Name	
	Attorney Docket Number	Mars16-001-US-C01

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Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
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	1	2012/0068271	wo		2012-03-22	Semiconductor Energy Laboratory Co., Ltd.		
	2	2013/138452	wo		2013-09-19	QUALCOMM MEMS TECHNOLOGIES, INC.		

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Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

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See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Ping-Jung Yang/	Date (YYYY-MM-DD)	2020-01-26
Name/Print	Ping-Jung Yang	Registration Number	

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(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
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13 March 2013 (13.03.2013)

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13/418,834 13 March 2012 (13.03.2012) US

(71) Applicant: **QUALCOMM MEMS TECHNOLOGIES, INC.** [US/US]; 5775 Morehouse Drive, San Diego, California 92121-1714 (US).

(72) Inventors: **SHENOY, Ravindra V.**; 5775 Morehouse Drive, San Diego, California 92121 (US). **BURNS, David William**; 5775 Morehouse Drive, San Diego, California 92121 (US). **GOUSEV, Evgeni P.**; 5775 Morehouse Drive, San Diego, California 92121 (US).

(74) Agents: **HO, Michael T.** et al.; WEAVER AUSTIN VILLENEUVE & SAMPSON LLP, P.O. Box 70250, Oakland, California 94612-0250 (US).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

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Declarations under Rule 4.17:

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— *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

Published:

— *with international search report (Art. 21(3))*

— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments (Rule 48.2(h))*

(54) Title: LOW COST INTERPOSER FABRICATED WITH ADDITIVE PROCESSES

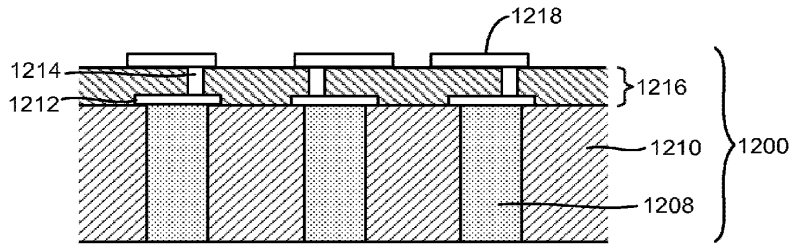


Figure 12A

(57) Abstract: This disclosure provides systems, methods and apparatus for interposers in compact three-dimensional (3-D) device packages. In one aspect, one or more methods of fabricating an interposer using an additive process are provided. The additive process can involve depositing flowable dielectric material around a plurality of metal interconnect posts after forming the plurality of metal interconnect posts on a carrier substrate. In another aspect, an interposer including through-glass vias and one or more passive devices is provided.

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LOW COST INTERPOSER FABRICATED WITH ADDITIVE PROCESSES

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application claims priority to U.S. Patent Application 13/418,834, filed March 13, 2012, titled "LOW COST INTERPOSER FABRICATED WITH ADDITIVE PROCESSES," all of which is incorporated herein by this reference for all purposes.

TECHNICAL FIELD

[0002] This disclosure relates generally to three-dimensional (3-D) device packaging and more particularly to electrically conductive interconnects for 3-D device packages.

DESCRIPTION OF THE RELATED TECHNOLOGY

[0003] Electromechanical systems include devices having electrical and mechanical elements, actuators, transducers, sensors, optical components (e.g., mirrors) and electronics. Electromechanical systems can be manufactured at a variety of scales including, but not limited to, microscales and nanoscales. For example, microelectromechanical systems (MEMS) devices can include structures having sizes ranging from about a micron to hundreds of microns or more. Nanoelectromechanical systems (NEMS) devices can include structures having sizes smaller than a micron including, for example, sizes smaller than several hundred nanometers. Electromechanical elements may be created using deposition, etching, lithography, and/or other micromachining processes that etch away parts of substrates and/or deposited material layers, or that add layers to form electrical and electromechanical devices.

[0004] One type of electromechanical systems device is called an interferometric modulator (IMOD). As used herein, the term interferometric modulator or interferometric light modulator refers to a device that selectively absorbs and/or reflects light using the principles of optical interference. In some implementations, an interferometric modulator may include a pair of conductive plates, one or both of which may be transparent and/or reflective, wholly or in part, and capable of relative motion upon application of an appropriate electrical signal. In an implementation, one plate may include a stationary layer deposited on a substrate and the other plate may include a reflective membrane separated from the stationary layer by an air gap. The position of one plate in relation to another can change the optical interference of light incident on

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the interferometric modulator. Interferometric modulator devices have a wide range of applications, and are anticipated to be used in improving existing products and creating new products, especially those with display capabilities.

[0005] Device packaging in electromechanical systems can protect the functional units of the system from the environment, provide mechanical support for the system components, and provide a high-density interface for stacked electrical interconnections between devices and substrates.

SUMMARY

[0006] The systems, methods and devices of the disclosure each have several innovative aspects, no single one of which is solely responsible for the desirable attributes disclosed herein.

[0007] One innovative aspect of the subject matter described in this disclosure can be implemented in a method of forming an interposer. The method can include forming a sacrificial layer on a carrier substrate and forming a plurality of interconnect posts on the sacrificial layer. The plurality of interconnected posts can be oriented substantially perpendicular to the carrier substrate. One or more flowable dielectric layers can be deposited and solidified to cover the sacrificial layer and the plurality of interconnect posts. The solidified dielectric material can be planarized to expose the plurality of interconnect posts and to form an interposer layer releasably attached to the carrier substrate via the sacrificial layer. In some implementations, the one or more flowable dielectric layers can include one or more spin-on dielectrics or one or more epoxy layers. In some implementations, forming a plurality of interconnect posts can include plating metal posts in a patterned photoresist layer.

[0008] The method can further include forming one or one more passive components on the solidified dielectric material. Examples of passive components include resistors, capacitors, and inductors. In some implementations, one or more passive components can be formed after planarizing the solidified dielectric material. In some implementations, one or more passive components can be formed after forming the sacrificial layer on the carrier substrate and before depositing any flowable dielectric layers. The method can further include plating the plurality of interconnect posts with solderable material. In some implementations, the method can further include forming one or more routing layers on the solidified dielectric material.

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[0009] Another innovative aspect of this disclosure can be implemented in an interposer. The interposer can include an additive glass interposer layer and one or more metal interconnect posts extending through the glass interposer layer. In some implementations, a routing layer including electrically conductive routing lines can be connected to the one or more metal interconnect posts. The density of the routing lines can greater than the density of the interconnect posts. Examples of metals in a metal interconnect post can include nickel, nickel alloy, and copper. In some implementations, the metal interconnect posts can have height to width aspect ratios of greater than about 5:1. Example heights of the metal interconnect posts range from about 10 microns to about 100 microns, and in some cases as much as about 500 microns. Example widths of the metal interconnect posts range from about 5 microns to about 100 microns. Example thicknesses of the glass interposer layer can range from about 10 microns to about 500 microns. In some implementations, the interposer can include one or more passive components on the glass interposer layer. In some implementations, a metal interconnect post can include an interconnect cap that protrudes from the spin-on glass substrate. An interconnect cap can include a solderable material in some implementations.

[0010] Another innovative aspect of this disclosure can be implemented in a method of forming an interposer that includes using an additive process to fabricate an additive glass interposer layer on a carrier substrate and integrating one or more passive components within the interposer layer during the additive process. Examples of passive components include resistors, capacitors and inductors. In some implementations, using the additive process includes depositing flowable dielectric material around a plurality of metal interconnect posts and the carrier substrate after forming the plurality of metal interconnect posts on the carrier substrate.

[0011] Another innovative aspect of this disclosure can be implemented in an apparatus. The apparatus can include a packaging substrate, an interposer layer in electrical communication with the packaging substrate, and one or more dies positioned over the interposer layer. The interposer layer can include a solidified dielectric material, one or more metal interconnect posts extending through the solidified dielectric material, and a routing layer including electrically conductive routing lines connected to the one or more metal interconnect posts. In some implementations, the density of electrical connections from the routing layer to the one or more dies is greater than the density of electrical connections from the interposer layer to the packaging

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substrate. In some implementations, the solidified dielectric material can include spin-on-glass or epoxy. Examples of dies include at least one of memory, logic, radio frequency, application specific integrated circuit, and MEMS chips. In some implementations, the one or more dies can include stacked dies. The apparatus can further include one or more passive components within the interposer layer. Examples of passive components include resistors, capacitors and inductors.

[0012] Another innovative aspect of this disclosure can be implemented in an apparatus including an interposer formed by a process including forming a plurality of interconnect posts on a sacrificial layer, the sacrificial layer formed on a carrier substrate; depositing and solidifying one or more flowable dielectric layers around the interconnect posts; planarizing the solidified dielectric material to expose the interconnect posts; and releasing the interposer from the carrier substrate by sacrificially etching the sacrificial layer.

[0013] The apparatus can further include one or more routing layers on an upper side or a lower side of the interposer. At least one passive component can be formed on an upper side or a lower side of the interposer. In some implementations, at least one interconnect post provides strain relief when the interposer is connected between a packaging substrate and an integrated circuit chip. In some implementations, at least one interconnect post allows heat transfer between an integrated circuit chip and a packaging substrate, the interposer connected between the packaging substrate and the integrated circuit chip. The apparatus can further include one or more of an integrated circuit chip and a packaging substrate attached to the interposer. In some implementations, the interposer provides stress isolation between a packaging substrate and an integrated circuit chip attached to the interposer.

[0014] Details of one or more implementations of the subject matter described in this specification are set forth in the accompanying drawings and the description below. Other features, aspects, and advantages will become apparent from the description, the drawings, and the claims. Note that the relative dimensions of the following figures may not be drawn to scale.

BRIEF DESCRIPTION OF THE DRAWINGS

[0015] Figure 1 shows an example of an isometric view depicting two adjacent pixels in a series of pixels of an interferometric modulator (IMOD) display device.

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[0016] Figure 2 shows an example of a system block diagram illustrating an electronic device incorporating a 3x3 interferometric modulator display.

[0017] Figure 3 shows an example of a diagram illustrating movable reflective layer position versus applied voltage for the interferometric modulator of Figure 1.

[0018] Figure 4 shows an example of a table illustrating various states of an interferometric modulator when various common and segment voltages are applied.

[0019] Figure 5A shows an example of a diagram illustrating a frame of display data in the 3x3 interferometric modulator display of Figure 2.

[0020] Figure 5B shows an example of a timing diagram for common and segment signals that may be used to write the frame of display data illustrated in Figure 5A.

[0021] Figure 6A shows an example of a partial cross-section of the interferometric modulator display of Figure 1.

[0022] Figures 6B–6E show examples of cross-sections of varying implementations of interferometric modulators.

[0023] Figure 7 shows an example of a flow diagram illustrating a manufacturing process for an interferometric modulator.

[0024] Figures 8A–8E show examples of cross-sectional schematic illustrations of various stages in a method of making an interferometric modulator.

[0025] Figure 9 shows an example of a flow diagram illustrating a manufacturing process for forming an interposer.

[0026] Figure 10 shows an example of a flow diagram illustrating a manufacturing process for forming an interposer.

[0027] Figures 11A–11G show examples of cross-sectional schematic illustrations of various stages in a method of manufacturing an interposer layer.

[0028] Figures 12A–12C show examples of cross-sectional schematic illustrations of varying implementations of interposers with one or more routing layers.

[0029] Figure 13 shows an example of a cross-sectional schematic illustration of stacked dies on an interposer.

[0030] Figures 14A–14D show examples of cross-sectional schematic illustrations of various stages in a method of forming an interposer.

[0031] Figures 15A and 15B show examples of cross-sectional schematic illustrations of an interposer positioned between an integrated circuit chip and a packaging substrate.

[0032] Figures 16A and 16B show examples of system block diagrams illustrating a display device that includes a plurality of interferometric modulators.

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[0033] Like reference numbers and designations in the various drawings indicate like elements.

DETAILED DESCRIPTION

[0034] The following detailed description is directed to certain implementations for the purposes of describing the innovative aspects. However, the teachings herein can be applied in a multitude of different ways. The described implementations may be implemented in any device that is configured to display an image, whether in motion (e.g., video) or stationary (e.g., still image), and whether textual, graphical or pictorial. More particularly, it is contemplated that the implementations may be implemented in or associated with a variety of electronic devices such as, but not limited to, mobile telephones, multimedia Internet enabled cellular telephones, mobile television receivers, wireless devices, smartphones, bluetooth devices, personal data assistants (PDAs), wireless electronic mail receivers, hand-held or portable computers, netbooks, notebooks, smartbooks, tablets, printers, copiers, scanners, facsimile devices, GPS receivers/navigators, cameras, MP3 players, camcorders, game consoles, wrist watches, clocks, calculators, television monitors, flat panel displays, electronic reading devices (e.g., e-readers), computer monitors, auto displays (e.g., odometer display, etc.), cockpit controls and/or displays, camera view displays (e.g., display of a rear view camera in a vehicle), electronic photographs, electronic billboards or signs, projectors, architectural structures, microwaves, refrigerators, stereo systems, cassette recorders or players, DVD players, CD players, VCRs, radios, portable memory chips, washers, dryers, washer/dryers, parking meters, packaging (e.g., electromechanical systems (EMS), MEMS and non-MEMS), aesthetic structures (e.g., display of images on a piece of jewelry) and a variety of electromechanical systems devices. The teachings herein also can be used in non-display applications such as, but not limited to, electronic switching devices, radio frequency filters, sensors, accelerometers, gyroscopes, motion-sensing devices, magnetometers, inertial components for consumer electronics, parts of consumer electronics products, varactors, liquid crystal devices, electrophoretic devices, drive schemes, manufacturing processes, electronic test equipment. Thus, the teachings are not intended to be limited to the implementations depicted solely in the Figures, but instead have wide applicability as will be readily apparent to one having ordinary skill in the art.

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[0035] Some implementations described herein relate to 3-D device packaging and interposer technology. An interposer generally serves as an intermediate layer that can be used for direct electrical interconnection between one device or substrate and a second device or substrate with the interposer positioned in between. For example, an interposer may have a pad configuration on one side that can be aligned with corresponding pads on a first device, and a different pad configuration on a second side that corresponds to pads on a second device. The interposer can contain electrical traces that allow interconnecting pads to be aligned and mated to devices on opposite sides. In some implementations, the interposer includes an interposer layer that has electrically conductive interconnects (vias) extending through the layer. For example, in some implementations, the interposer layer can be a through-glass via layer. For example, in some implementations, the interposer layer can be an additive glass interposer layer. In some implementations, the interposers can further include one or more routing or redistribution layers. In some implementations, the interposer may include a ground plane and/or a power plane. In some implementations, one or more passive components can be integrated within the interposer. In some implementations, one or more devices may be attached to each side of the interposer.

[0036] Some implementations described herein relate to additive processes to fabricate interposers. An additive process can involve depositing flowable dielectric material over a plurality of metal interconnect posts and solidifying the flowable dielectric material. In some implementations, the process can further include forming the plurality of metal interconnect posts on a carrier substrate prior to depositing the flowable dielectric material. For example, the flowable dielectric material may be deposited by spinning, dispensing, extruding, injecting, casting or otherwise disposing the dielectric material around, and in some cases, over the interconnect posts. The interconnect posts may be formed, for example, directly on the carrier substrate or on a sacrificial layer disposed on the carrier substrate. Examples of flowable dielectric material include spin-on dielectric and epoxy materials. The process can further include planarizing the solidified dielectric material to form an interposer layer including through-layer interconnects. In some implementations, one or more passive components can be formed prior to or after forming the solidified dielectric material. In some implementations, one or more routing or redistribution layers can be formed prior to or after forming the solidified dielectric material.

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[0037] Some implementations relate to additive glass interposer layers. An additive glass interposer layer is any interposer layer formed by solidifying a flowable dielectric material such as a dispensable glass or epoxy around one or more interconnect posts of the interposer layer.

[0038] Particular implementations of the subject matter described in this disclosure can be implemented to realize one or more of the following potential advantages. Forming an interposer layer using an additive process can reduce the cost of fabrication in comparison to subtractive processes that require multiple patterning and deposition operations. Use of a flowable dielectric material around electroplated posts allows relatively thin interposers to be formed. The posts may be formed with a relatively high density. Patterned photoresist materials may be used to form the electroplated posts, which can then be removed and replaced with a stronger material having a high dielectric strength. One or more routing layers separated by thin dielectric layers may be formed prior to or after formation of the posts. Passive components can also be integrated in a cost-efficient manner within the interposer by using an additive process. Additive processes are also scalable to large panel or continuous roll substrates that can further reduce cost.

[0039] Some implementations described herein relate to 3-D device packaging, including packaging of EMS or MEMS devices. An example of a suitable EMS or MEMS device, to which the described implementations may apply, is a reflective display device. Reflective display devices can incorporate interferometric modulators (IMODs) to selectively absorb and/or reflect light incident thereon using principles of optical interference. IMODs can include an absorber, a reflector that is movable with respect to the absorber, and an optical resonant cavity defined between the absorber and the reflector. The reflector can be moved to two or more different positions, which can change the size of the optical resonant cavity and thereby affect the reflectance of the interferometric modulator. The reflectance spectrums of IMODs can create fairly broad spectral bands which can be shifted across the visible wavelengths to generate different colors. The position of the spectral band can be adjusted by changing the thickness of the optical resonant cavity, i.e., by changing the position of the reflector.

[0040] Figure 1 shows an example of an isometric view depicting two adjacent pixels in a series of pixels of an interferometric modulator (IMOD) display device. The IMOD display device includes one or more interferometric MEMS display elements. In these devices, the pixels of the MEMS display elements can be in either a bright or dark state.

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In the bright ("relaxed," "open" or "on") state, the display element reflects a large portion of incident visible light, e.g., to a user. Conversely, in the dark ("actuated," "closed" or "off") state, the display element reflects little incident visible light. In some implementations, the light reflectance properties of the on and off states may be reversed. MEMS pixels can be configured to reflect predominantly at particular wavelengths allowing for a color display in addition to black and white.

[0041] The IMOD display device can include a row/column array of IMODs. Each IMOD can include a pair of reflective layers, i.e., a movable reflective layer and a fixed partially reflective layer, positioned at a variable and controllable distance from each other to form an air gap (also referred to as an optical gap or cavity). The movable reflective layer may be moved between at least two positions. In a first position, i.e., a relaxed position, the movable reflective layer can be positioned at a relatively large distance from the fixed partially reflective layer. In a second position, i.e., an actuated position, the movable reflective layer can be positioned more closely to the partially reflective layer. Incident light that reflects from the two layers can interfere constructively or destructively depending on the position of the movable reflective layer, producing either an overall reflective or non-reflective state for each pixel. In some implementations, the IMOD may be in a reflective state when unactuated, reflecting light within the visible spectrum, and may be in a dark state when unactuated, reflecting light outside of the visible range (e.g., infrared light). In some other implementations, however, an IMOD may be in a dark state when unactuated, and in a reflective state when actuated. In some implementations, the introduction of an applied voltage can drive the pixels to change states. In some other implementations, an applied charge can drive the pixels to change states.

[0042] The depicted portion of the pixel array in Figure 1 includes two adjacent interferometric modulators 12. In the IMOD 12 on the left (as illustrated), a movable reflective layer 14 is illustrated in a relaxed position at a predetermined distance from an optical stack 16, which includes a partially reflective layer. The voltage V_0 applied across the IMOD 12 on the left is insufficient to cause actuation of the movable reflective layer 14. In the IMOD 12 on the right, the movable reflective layer 14 is illustrated in an actuated position near or adjacent the optical stack 16. The voltage V_{bias} applied across the IMOD 12 on the right is sufficient to maintain the movable reflective layer 14 in the actuated position.

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[0043] In Figure 1, the reflective properties of pixels 12 are generally illustrated with arrows 13 indicating light incident upon the pixels 12, and light 15 reflecting from the IMOD 12 on the left. Although not illustrated in detail, it will be understood by one having ordinary skill in the art that most of the light 13 incident upon the pixels 12 will be transmitted through the transparent substrate 20, toward the optical stack 16. A portion of the light incident upon the optical stack 16 will be transmitted through the partially reflective layer of the optical stack 16, and a portion will be reflected back through the transparent substrate 20. The portion of light 13 that is transmitted through the optical stack 16 will be reflected at the movable reflective layer 14, back toward (and through) the transparent substrate 20. Interference (constructive or destructive) between the light reflected from the partially reflective layer of the optical stack 16 and the light reflected from the movable reflective layer 14 will determine the wavelength(s) of light 15 reflected from the IMOD 12.

[0044] The optical stack 16 can include a single layer or several layers. The layer(s) can include one or more of an electrode layer, a partially reflective and partially transmissive layer, and a transparent dielectric layer. In some implementations, the optical stack 16 is electrically conductive, partially transparent and partially reflective, and may be fabricated, for example, by depositing one or more of the above layers onto a transparent substrate 20. The electrode layer can be formed from a variety of materials, such as various metals, for example indium tin oxide (ITO). The partially reflective layer can be formed from a variety of materials that are partially reflective, such as various metals, e.g., chromium (Cr), semiconductors, and dielectrics. The partially reflective layer can be formed of one or more layers of materials, and each of the layers can be formed of a single material or a combination of materials. In some implementations, the optical stack 16 can include a single semi-transparent thickness of metal or semiconductor which serves as both an optical absorber and conductor, while different, more conductive layers or portions (e.g., of the optical stack 16 or of other structures of the IMOD) can serve to bus signals between IMOD pixels. The optical stack 16 also can include one or more insulating or dielectric layers covering one or more conductive layers or a conductive/absorptive layer.

[0045] In some implementations, the layer(s) of the optical stack 16 can be patterned into parallel strips, and may form row electrodes in a display device as described further below. As will be understood by one having skill in the art, the term "patterned" is used herein to refer to masking as well as etching processes. In some implementations, a

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highly conductive and reflective material, such as aluminum (Al), may be used for the movable reflective layer 14, and these strips may form column electrodes in a display device. The movable reflective layer 14 may be formed as a series of parallel strips of a deposited metal layer or layers (orthogonal to the row electrodes of the optical stack 16) to form columns deposited on top of posts 18 and an intervening sacrificial material deposited between the posts 18. When the sacrificial material is etched away, a defined gap 19, or optical cavity, can be formed between the movable reflective layer 14 and the optical stack 16. In some implementations, the spacing between posts 18 may be approximately 1–1000 um, while the gap 19 may be less than 10,000 Angstroms (Å).

[0046] In some implementations, each pixel of the IMOD, whether in the actuated or relaxed state, is essentially a capacitor formed by the fixed and moving reflective layers. When no voltage is applied, the movable reflective layer 14 remains in a mechanically relaxed state, as illustrated by the IMOD 12 on the left in Figure 1, with the gap 19 between the movable reflective layer 14 and optical stack 16. However, when a potential difference, e.g., voltage, is applied to at least one of a selected row and column, the capacitor formed at the intersection of the row and column electrodes at the corresponding pixel becomes charged, and electrostatic forces pull the electrodes together. If the applied voltage exceeds a threshold, the movable reflective layer 14 can deform and move near or against the optical stack 16. A dielectric layer (not shown) within the optical stack 16 may prevent shorting and control the separation distance between the layers 14 and 16, as illustrated by the actuated IMOD 12 on the right in Figure 1. The behavior is the same regardless of the polarity of the applied potential difference. Though a series of pixels in an array may be referred to in some instances as "rows" or "columns," a person having ordinary skill in the art will readily understand that referring to one direction as a "row" and another as a "column" is arbitrary. Restated, in some orientations, the rows can be considered columns, and the columns considered to be rows. Furthermore, the display elements may be evenly arranged in orthogonal rows and columns (an "array"), or arranged in non-linear configurations, for example, having certain positional offsets with respect to one another (a "mosaic"). The terms "array" and "mosaic" may refer to either configuration. Thus, although the display is referred to as including an "array" or "mosaic," the elements themselves need not be arranged orthogonally to one another, or disposed in an even distribution, in any instance, but may include arrangements having asymmetric shapes and unevenly distributed elements.

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[0047] Figure 2 shows an example of a system block diagram illustrating an electronic device incorporating a 3x3 interferometric modulator display. The electronic device includes a processor 21 that may be configured to execute one or more software modules. In addition to executing an operating system, the processor 21 may be configured to execute one or more software applications, including a web browser, a telephone application, an email program, or other software application.

[0048] The processor 21 can be configured to communicate with an array driver 22. The array driver 22 can include a row driver circuit 24 and a column driver circuit 26 that provide signals to, e.g., a display array or panel 30. The cross section of the IMOD display device illustrated in Figure 1 is shown by the lines 1–1 in Figure 2. Although Figure 2 illustrates a 3x3 array of IMODs for the sake of clarity, the display array 30 may contain a very large number of IMODs, and may have a different number of IMODs in rows than in columns, and vice versa.

[0049] Figure 3 shows an example of a diagram illustrating movable reflective layer position versus applied voltage for the interferometric modulator of Figure 1. For MEMS interferometric modulators, the row/column (i.e., common/segment) write procedure may take advantage of a hysteresis property of these devices as illustrated in Figure 3. An interferometric modulator may require, for example, about a 10-volt potential difference to cause the movable reflective layer, or mirror, to change from the relaxed state to the actuated state. When the voltage is reduced from that value, the movable reflective layer maintains its state as the voltage drops back below, e.g., 10 volts, however, the movable reflective layer does not relax completely until the voltage drops below 2 volts. Thus, a range of voltage, approximately 3 to 7 volts, as shown in Figure 3, exists where there is a window of applied voltage within which the device is stable in either the relaxed or actuated state. This is referred to herein as the "hysteresis window" or "stability window." For a display array 30 having the hysteresis characteristics of Figure 3, the row/column write procedure can be designed to address one or more rows at a time, such that during the addressing of a given row, pixels in the addressed row that are to be actuated are exposed to a voltage difference of about 10 volts, and pixels that are to be relaxed are exposed to a voltage difference of near zero volts. After addressing, the pixels are exposed to a steady state or bias voltage difference of approximately 5-volts such that they remain in the previous strobing state. In this example, after being addressed, each pixel sees a potential difference within the "stability window" of about 3–7 volts. This hysteresis property feature enables the pixel

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design, e.g., illustrated in Figure 1, to remain stable in either an actuated or relaxed pre-existing state under the same applied voltage conditions. Since each IMOD pixel, whether in the actuated or relaxed state, is essentially a capacitor formed by the fixed and moving reflective layers, this stable state can be held at a steady voltage within the hysteresis window without substantially consuming or losing power. Moreover, essentially little or no current flows into the IMOD pixel if the applied voltage potential remains substantially fixed.

[0050] In some implementations, a frame of an image may be created by applying data signals in the form of "segment" voltages along the set of column electrodes, in accordance with the desired change (if any) to the state of the pixels in a given row. Each row of the array can be addressed in turn, such that the frame is written one row at a time. To write the desired data to the pixels in a first row, segment voltages corresponding to the desired state of the pixels in the first row can be applied on the column electrodes, and a first row pulse in the form of a specific "common" voltage or signal can be applied to the first row electrode. The set of segment voltages can then be changed to correspond to the desired change (if any) to the state of the pixels in the second row, and a second common voltage can be applied to the second row electrode. In some implementations, the pixels in the first row are unaffected by the change in the segment voltages applied along the column electrodes, and remain in the state they were set to during the first common voltage row pulse. This process may be repeated for the entire series of rows, or alternatively, columns, in a sequential fashion to produce the image frame. The frames can be refreshed and/or updated with new image data by continually repeating this process at some desired number of frames per second.

[0051] The combination of segment and common signals applied across each pixel (that is, the potential difference across each pixel) determines the resulting state of each pixel. Figure 4 shows an example of a table illustrating various states of an interferometric modulator when various common and segment voltages are applied. As will be readily understood by one having ordinary skill in the art, the "segment" voltages can be applied to either the column electrodes or the row electrodes, and the "common" voltages can be applied to the other of the column electrodes or the row electrodes.

[0052] As illustrated in Figure 4 (as well as in the timing diagram shown in Figure 5B), when a release voltage VC_{REL} is applied along a common line, all interferometric modulator elements along the common line will be placed in a relaxed state,

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alternatively referred to as a released or unactuated state, regardless of the voltage applied along the segment lines, i.e., high segment voltage VS_H and low segment voltage VS_L. In particular, when the release voltage VC_{REL} is applied along a common line, the potential voltage across the modulator (alternatively referred to as a pixel voltage) is within the relaxation window (see Figure 3, also referred to as a release window) both when the high segment voltage VS_H and the low segment voltage VS_L are applied along the corresponding segment line for that pixel.

[0053] When a hold voltage is applied on a common line, such as a high hold voltage VC_{HOLD_H} or a low hold voltage VC_{HOLD_L}, the state of the interferometric modulator will remain constant. For example, a relaxed IMOD will remain in a relaxed position, and an actuated IMOD will remain in an actuated position. The hold voltages can be selected such that the pixel voltage will remain within a stability window both when the high segment voltage VS_H and the low segment voltage VS_L are applied along the corresponding segment line. Thus, the segment voltage swing, i.e., the difference between the high VS_H and low segment voltage VS_L, is less than the width of either the positive or the negative stability window.

[0054] When an addressing, or actuation, voltage is applied on a common line, such as a high addressing voltage VC_{ADD_H} or a low addressing voltage VC_{ADD_L}, data can be selectively written to the modulators along that line by application of segment voltages along the respective segment lines. The segment voltages may be selected such that actuation is dependent upon the segment voltage applied. When an addressing voltage is applied along a common line, application of one segment voltage will result in a pixel voltage within a stability window, causing the pixel to remain unactuated. In contrast, application of the other segment voltage will result in a pixel voltage beyond the stability window, resulting in actuation of the pixel. The particular segment voltage which causes actuation can vary depending upon which addressing voltage is used. In some implementations, when the high addressing voltage VC_{ADD_H} is applied along the common line, application of the high segment voltage VS_H can cause a modulator to remain in its current position, while application of the low segment voltage VS_L can cause actuation of the modulator. As a corollary, the effect of the segment voltages can be the opposite when a low addressing voltage VC_{ADD_L} is applied, with high segment voltage VS_H causing actuation of the modulator, and low segment voltage VS_L having no effect (i.e., remaining stable) on the state of the modulator.

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[0055] In some implementations, hold voltages, address voltages, and segment voltages may be used which always produce the same polarity potential difference across the modulators. In some other implementations, signals can be used which alternate the polarity of the potential difference of the modulators. Alternation of the polarity across the modulators (that is, alternation of the polarity of write procedures) may reduce or inhibit charge accumulation which could occur after repeated write operations of a single polarity.

[0056] Figure 5A shows an example of a diagram illustrating a frame of display data in the 3x3 interferometric modulator display of Figure 2. Figure 5B shows an example of a timing diagram for common and segment signals that may be used to write the frame of display data illustrated in Figure 5A. The signals can be applied to the, e.g., 3x3 array of Figure 2, which will ultimately result in the line time 60e display arrangement illustrated in Figure 5A. The actuated modulators in Figure 5A are in a dark-state, i.e., where a substantial portion of the reflected light is outside of the visible spectrum so as to result in a dark appearance to, e.g., a viewer. Prior to writing the frame illustrated in Figure 5A, the pixels can be in any state, but the write procedure illustrated in the timing diagram of Figure 5B presumes that each modulator has been released and resides in an unactuated state before the first line time 60a.

[0057] During the first line time 60a, a release voltage 70 is applied on common line 1; the voltage applied on common line 2 begins at a high hold voltage 72 and moves to a release voltage 70; and a low hold voltage 76 is applied along common line 3. Thus, the modulators (common 1, segment 1), (1,2) and (1,3) along common line 1 remain in a relaxed, or unactuated, state for the duration of the first line time 60a, the modulators (2,1), (2,2) and (2,3) along common line 2 will move to a relaxed state, and the modulators (3,1), (3,2) and (3,3) along common line 3 will remain in their previous state. With reference to Figure 4, the segment voltages applied along segment lines 1, 2 and 3 will have no effect on the state of the interferometric modulators, as none of common lines 1, 2 or 3 are being exposed to voltage levels causing actuation during line time 60a (i.e., VC_{REL} – relax and VC_{HOLD_L} – stable).

[0058] During the second line time 60b, the voltage on common line 1 moves to a high hold voltage 72, and all modulators along common line 1 remain in a relaxed state regardless of the segment voltage applied because no addressing, or actuation, voltage was applied on the common line 1. The modulators along common line 2 remain in a relaxed state due to the application of the release voltage 70, and the modulators (3,1),

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(3,2) and (3,3) along common line 3 will relax when the voltage along common line 3 moves to a release voltage 70.

[0059] During the third line time 60c, common line 1 is addressed by applying a high address voltage 74 on common line 1. Because a low segment voltage 64 is applied along segment lines 1 and 2 during the application of this address voltage, the pixel voltage across modulators (1,1) and (1,2) is greater than the high end of the positive stability window (i.e., the voltage differential exceeded a predefined threshold) of the modulators, and the modulators (1,1) and (1,2) are actuated. Conversely, because a high segment voltage 62 is applied along segment line 3, the pixel voltage across modulator (1,3) is less than that of modulators (1,1) and (1,2), and remains within the positive stability window of the modulator; modulator (1,3) thus remains relaxed. Also during line time 60c, the voltage along common line 2 decreases to a low hold voltage 76, and the voltage along common line 3 remains at a release voltage 70, leaving the modulators along common lines 2 and 3 in a relaxed position.

[0060] During the fourth line time 60d, the voltage on common line 1 returns to a high hold voltage 72, leaving the modulators along common line 1 in their respective addressed states. The voltage on common line 2 is decreased to a low address voltage 78. Because a high segment voltage 62 is applied along segment line 2, the pixel voltage across modulator (2,2) is below the lower end of the negative stability window of the modulator, causing the modulator (2,2) to actuate. Conversely, because a low segment voltage 64 is applied along segment lines 1 and 3, the modulators (2,1) and (2,3) remain in a relaxed position. The voltage on common line 3 increases to a high hold voltage 72, leaving the modulators along common line 3 in a relaxed state.

[0061] Finally, during the fifth line time 60e, the voltage on common line 1 remains at high hold voltage 72, and the voltage on common line 2 remains at a low hold voltage 76, leaving the modulators along common lines 1 and 2 in their respective addressed states. The voltage on common line 3 increases to a high address voltage 74 to address the modulators along common line 3. As a low segment voltage 64 is applied on segment lines 2 and 3, the modulators (3,2) and (3,3) actuate, while the high segment voltage 62 applied along segment line 1 causes modulator (3,1) to remain in a relaxed position. Thus, at the end of the fifth line time 60e, the 3x3 pixel array is in the state shown in Figure 5A, and will remain in that state as long as the hold voltages are applied along the common lines, regardless of variations in the segment voltage which

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may occur when modulators along other common lines (not shown) are being addressed.

[0062] In the timing diagram of Figure 5B, a given write procedure (i.e., line times 60a–60e) can include the use of either high hold and address voltages, or low hold and address voltages. Once the write procedure has been completed for a given common line (and the common voltage is set to the hold voltage having the same polarity as the actuation voltage), the pixel voltage remains within a given stability window, and does not pass through the relaxation window until a release voltage is applied on that common line. Furthermore, as each modulator is released as part of the write procedure prior to addressing the modulator, the actuation time of a modulator, rather than the release time, may determine the necessary line time. Specifically, in implementations in which the release time of a modulator is greater than the actuation time, the release voltage may be applied for longer than a single line time, as depicted in Figure 5B. In some other implementations, voltages applied along common lines or segment lines may vary to account for variations in the actuation and release voltages of different modulators, such as modulators of different colors.

[0063] The details of the structure of interferometric modulators that operate in accordance with the principles set forth above may vary widely. For example, Figures 6A–6E show examples of cross-sections of varying implementations of interferometric modulators, including the movable reflective layer 14 and its supporting structures. Figure 6A shows an example of a partial cross-section of the interferometric modulator display of Figure 1, where a strip of metal material, i.e., the movable reflective layer 14 is deposited on supports 18 extending orthogonally from the substrate 20. In Figure 6B, the movable reflective layer 14 of each IMOD is generally square or rectangular in shape and attached to supports at or near the corners, on tethers 32. In Figure 6C, the movable reflective layer 14 is generally square or rectangular in shape and suspended from a deformable layer 34, which may include a flexible metal. The deformable layer 34 can connect, directly or indirectly, to the substrate 20 around the perimeter of the movable reflective layer 14. These connections are herein referred to as support posts. The implementation shown in Figure 6C has additional benefits deriving from the decoupling of the optical functions of the movable reflective layer 14 from its mechanical functions, which are carried out by the deformable layer 34. This decoupling allows the structural design and materials used for the reflective layer 14

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and those used for the deformable layer 34 to be optimized independently of one another.

[0064] Figure 6D shows another example of an IMOD, where the movable reflective layer 14 includes a reflective sub-layer 14a. The movable reflective layer 14 rests on a support structure, such as support posts 18. The support posts 18 provide separation of the movable reflective layer 14 from the lower stationary electrode (i.e., part of the optical stack 16 in the illustrated IMOD) so that a gap 19 is formed between the movable reflective layer 14 and the optical stack 16, for example when the movable reflective layer 14 is in a relaxed position. The movable reflective layer 14 also can include a conductive layer 14c, which may be configured to serve as an electrode, and a support layer 14b. In this example, the conductive layer 14c is disposed on one side of the support layer 14b, distal from the substrate 20, and the reflective sub-layer 14a is disposed on the other side of the support layer 14b, proximal to the substrate 20. In some implementations, the reflective sub-layer 14a can be conductive and can be disposed between the support layer 14b and the optical stack 16. The support layer 14b can include one or more layers of a dielectric material, for example, silicon oxynitride (SiON) or silicon dioxide (SiO_2). In some implementations, the support layer 14b can be a stack of layers, such as, for example, a SiO_2/SiON/SiO_2 tri-layer stack. Either or both of the reflective sub-layer 14a and the conductive layer 14c can include, e.g., an aluminum (Al) alloy with about 0.5% copper (Cu), or another reflective metallic material. Employing conductive layers 14a, 14c above and below the dielectric support layer 14b can balance stresses and provide enhanced conduction. In some implementations, the reflective sub-layer 14a and the conductive layer 14c can be formed of different materials for a variety of design purposes, such as achieving specific stress profiles within the movable reflective layer 14.

[0065] As illustrated in Figure 6D, some implementations also can include a black mask structure 23. The black mask structure 23 can be formed in optically inactive regions (e.g., between pixels or under posts 18) to absorb ambient or stray light. The black mask structure 23 also can improve the optical properties of a display device by inhibiting light from being reflected from or transmitted through inactive portions of the display, thereby increasing the contrast ratio. Additionally, the black mask structure 23 can be conductive and be configured to function as an electrical bussing layer. In some implementations, the row electrodes can be connected to the black mask structure 23 to reduce the resistance of the connected row electrode. The black mask structure 23 can

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be formed using a variety of methods, including deposition and patterning techniques. The black mask structure 23 can include one or more layers. For example, in some implementations, the black mask structure 23 includes a molybdenum-chromium (MoCr) layer that serves as an optical absorber, an SiO_2 layer, and an aluminum alloy that serves as a reflector and a bussing layer, with a thickness in the range of about 30–80 Å, 500–1000 Å, and 500–6000 Å, respectively. The one or more layers can be patterned using a variety of techniques, including photolithography and dry etching, including, for example, carbon tetrafluoromethane (CF_4) and/or oxygen (O_2) for the MoCr and SiO_2 layers and chlorine (Cl_2) and/or boron trichloride (BCl_3) for the aluminum alloy layer. In some implementations, the black mask 23 can be an etalon or interferometric stack structure. In such interferometric stack black mask structures 23, the conductive absorbers can be used to transmit or bus signals between lower, stationary electrodes in the optical stack 16 of each row or column. In some implementations, a spacer layer 35 can serve to generally electrically isolate the absorber layer 16a from the conductive layers in the black mask 23.

[0066] Figure 6E shows another example of an IMOD, where the movable reflective layer 14 is self-supporting. In contrast with Figure 6D, the implementation of Figure 6E does not include support posts 18. Instead, the movable reflective layer 14 contacts the underlying optical stack 16 at multiple locations, and the curvature of the movable reflective layer 14 provides sufficient support that the movable reflective layer 14 returns to the unactuated position of Figure 6E when the voltage across the interferometric modulator is insufficient to cause actuation. The optical stack 16, which may contain a plurality of several different layers, is shown here for clarity including an optical absorber 16a, and a dielectric 16b. In some implementations, the optical absorber 16a may serve both as a fixed electrode and as a partially reflective layer.

[0067] In implementations such as those shown in Figures 6A–6E, the IMODs function as direct-view devices, in which images are viewed from the front side of the transparent substrate 20, i.e., the side opposite to that upon which the modulator is arranged. In these implementations, the back portions of the device (that is, any portion of the display device behind the movable reflective layer 14, including, for example, the deformable layer 34 illustrated in Figure 6C) can be configured and operated upon without impacting or negatively affecting the image quality of the display device, because the reflective layer 14 optically shields those portions of the device. For example, in some implementations a bus structure (not illustrated) can be included

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behind the movable reflective layer 14 which provides the ability to separate the optical properties of the modulator from the electromechanical properties of the modulator, such as voltage addressing and the movements that result from such addressing. Additionally, the implementations of Figures 6A–6E can simplify processing, such as, e.g., patterning.

[0068] Figure 7 shows an example of a flow diagram illustrating a manufacturing process 80 for an interferometric modulator, and Figures 8A–8E show examples of cross-sectional schematic illustrations of corresponding stages of such a manufacturing process 80. In some implementations, the manufacturing process 80 can be implemented to manufacture, e.g., interferometric modulators of the general type illustrated in Figures 1 and 6, in addition to other blocks not shown in Figure 7. With reference to Figures 1, 6 and 7, the process 80 begins at block 82 with the formation of the optical stack 16 over the substrate 20. Figure 8A illustrates such an optical stack 16 formed over the substrate 20. The substrate 20 may be a transparent substrate such as glass or plastic, it may be flexible or relatively stiff and unbending, and may have been subjected to prior preparation processes, e.g., cleaning, to facilitate efficient formation of the optical stack 16. As discussed above, the optical stack 16 can be electrically conductive, partially transparent and partially reflective and may be fabricated, for example, by depositing one or more layers having the desired properties onto the transparent substrate 20. In Figure 8A, the optical stack 16 includes a multilayer structure having sub-layers 16a and 16b, although more or fewer sub-layers may be included in some other implementations. In some implementations, one of the sub-layers 16a, 16b can be configured with both optically absorptive and conductive properties, such as the combined conductor/absorber sub-layer 16a. Additionally, one or more of the sub-layers 16a, 16b can be patterned into parallel strips, and may form row electrodes in a display device. Such patterning can be performed by a masking and etching process or another suitable process. In some implementations, one of the sub-layers 16a, 16b can be an insulating or dielectric layer, such as sub-layer 16b that is deposited over one or more metal layers (e.g., one or more reflective and/or conductive layers). In addition, the optical stack 16 can be patterned into individual and parallel strips that form the rows of the display.

[0069] The process 80 continues at block 84 with the formation of a sacrificial layer 25 over the optical stack 16. The sacrificial layer 25 is later removed (e.g., at block 90) to form the cavity 19 and thus the sacrificial layer 25 is not shown in the resulting

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interferometric modulators 12 illustrated in Figure 1. Figure 8B illustrates a partially fabricated device including a sacrificial layer 25 formed over the optical stack 16. The formation of the sacrificial layer 25 over the optical stack 16 may include deposition of a xenon difluoride (XeF_2)-etchable material such as molybdenum (Mo) or amorphous silicon (Si), in a thickness selected to provide, after subsequent removal, a gap or cavity 19 (see also Figures 1 and 8E) having a desired design size. Deposition of the sacrificial material may be carried out using deposition techniques such as physical vapor deposition (PVD, e.g., sputtering), plasma-enhanced chemical vapor deposition (PECVD), thermal chemical vapor deposition (thermal CVD), or spin-coating.

[0070] The process 80 continues at block 86 with the formation of a support structure e.g., a post 18 as illustrated in Figures 1, 6 and 8C. The formation of the post 18 may include patterning the sacrificial layer 25 to form a support structure aperture, then depositing a material (e.g., a polymer or an inorganic material, e.g., silicon oxide) into the aperture to form the post 18, using a deposition method such as PVD, PECVD, thermal CVD, or spin-coating. In some implementations, the support structure aperture formed in the sacrificial layer can extend through both the sacrificial layer 25 and the optical stack 16 to the underlying substrate 20, so that the lower end of the post 18 contacts the substrate 20 as illustrated in Figure 6A. Alternatively, as depicted in Figure 8C, the aperture formed in the sacrificial layer 25 can extend through the sacrificial layer 25, but not through the optical stack 16. For example, Figure 8E illustrates the lower ends of the support posts 18 in contact with an upper surface of the optical stack 16. The post 18, or other support structures, may be formed by depositing a layer of support structure material over the sacrificial layer 25 and patterning to remove portions of the support structure material located away from apertures in the sacrificial layer 25. The support structures may be located within the apertures, as illustrated in Figure 8C, but also can, at least partially, extend over a portion of the sacrificial layer 25. As noted above, the patterning of the sacrificial layer 25 and/or the support posts 18 can be performed by a patterning and etching process, but also may be performed by alternative etching methods.

[0071] The process 80 continues at block 88 with the formation of a movable reflective layer or membrane such as the movable reflective layer 14 illustrated in Figures 1, 6 and 8D. The movable reflective layer 14 may be formed by employing one or more deposition processes, e.g., reflective layer (e.g., aluminum, aluminum alloy) deposition, along with one or more patterning, masking, and/or etching processes. The

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movable reflective layer 14 can be electrically conductive, and referred to as an electrically conductive layer. In some implementations, the movable reflective layer 14 may include a plurality of sub-layers 14a, 14b, 14c as shown in Figure 8D. In some implementations, one or more of the sub-layers, such as sub-layers 14a, 14c, may include highly reflective sub-layers selected for their optical properties, and another sub-layer 14b may include a mechanical sub-layer selected for its mechanical properties. Since the sacrificial layer 25 is still present in the partially fabricated interferometric modulator formed at block 88, the movable reflective layer 14 is typically not movable at this stage. A partially fabricated IMOD that contains a sacrificial layer 25 also may be referred to herein as an "unreleased" IMOD. As described above in connection with Figure 1, the movable reflective layer 14 can be patterned into individual and parallel strips that form the columns of the display.

[0072] The process 80 continues at block 90 with the formation of a cavity, e.g., cavity 19 as illustrated in Figures 1, 6 and 8E. The cavity 19 may be formed by exposing the sacrificial material 25 (deposited at block 84) to an etchant. For example, an etchable sacrificial material such as Mo or amorphous Si may be removed by dry chemical etching, e.g., by exposing the sacrificial layer 25 to a gaseous or vaporous etchant, such as vapors derived from solid XeF_2 for a period of time that is effective to remove the desired amount of material, typically selectively removed relative to the structures surrounding the cavity 19. Other combinations of etchable sacrificial material and etching methods, e.g. wet etching and/or plasma etching, also may be used. Since the sacrificial layer 25 is removed during block 90, the movable reflective layer 14 is typically movable after this stage. After removal of the sacrificial material 25, the resulting fully or partially fabricated IMOD may be referred to herein as a "released" IMOD.

[0073] Implementations described herein relate to interposers and interposers for use in compact three-dimensional (3-D) packages. In some implementations, methods of manufacturing an interposer are described. An interposer is an intermediate layer that can be used for interconnection routing or as a ground or power plane. Interposers can be incorporated within 3-D device packages, such as packages for memory, logic, EMS, MEMS, and other chip devices. In a 3-D structure, electronic components such as semiconductor chips, EMS devices, and the like can be provided in a stacked structure. Interposers can connect components in different layers of a 3-D stacked structure.

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[0074] In some implementations, the interposers described herein include glass or epoxy substrates having through-substrate interconnects (vias). For example, a through-glass via interposer is an interposer including electrically conductive vias that extend through a glass interposer layer and that can provide electrical interconnection between components on both sides of the layer. While portions of the discussion below refer to through-glass via interposers, it is understood that dielectric substrates other than glass may be used, such as epoxy substrates.

[0075] Through-glass via interposers may be used to provide electrical interconnections and mechanical support to electrically connect components in different layers in a stacked structure. In one implementation, two or more dies having integrated circuits may be stacked such that through-glass vias electrically connect the integrated circuits. Through-glass via interposers can provide high wiring density interconnection, reduce coefficient of thermal expansion (CTE) mismatch to the connected dies, and improve electrical performance due to shorter interconnection from the dies to a packaging substrate.

[0076] In some implementations, through-substrate via interposers, including through-glass and through-epoxy via interposers, can be formed using an additive process. An overview of an additive process according to some implementations is given in Figure 9, with examples of specific implementations described further below with reference to Figures 10–11G.

[0077] Figure 9 shows an example of a flow diagram illustrating a manufacturing process for forming an interposer. The process 900 begins at block 902 where a sacrificial layer is formed on a carrier substrate. The carrier substrate may be transparent or non-transparent. Examples of carrier substrate materials can include glass, plastic, and silicon. The sacrificial layer can be any material that can be selectively removed from the interposer layer. Examples include sputtered Cu, sputtered Al, and laser-cleavable polymers. Further examples of carrier substrates and sacrificial materials are described below with reference to Figure 11A.

[0078] The process 900 continues at block 904 where a plurality of interconnect posts are formed that are oriented substantially perpendicularly to the carrier substrate. Forming the plurality of interconnect posts can include plating a plurality of metal posts in a patterned photoresist layer. In some implementations, the metal posts can be electrically conductive vias.

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[0079] The process 900 continues at block 906 where one or more flowable dielectric layers are deposited and cured to cover the sacrificial layer and the plurality of interconnect posts with a solidified dielectric material. In some implementations, the one or more flowable dielectric layers can include one or more spin-on-glass layers. In some implementations, the one or more flowable dielectric layers can include one or more epoxy layers.

[0080] The process 900 continues at block 908 where the solidified dielectric material is planarized to expose the plurality of interconnect posts and to form an interposer layer releasably attached to the carrier substrate via the sacrificial layer. In some implementations, the process 900 can continue with releasing the interposer layer from the carrier substrate (not shown).

[0081] Additional operations may also be present in the process 900. For example, in some implementations, the process 900 can also include plating the plurality of interconnect posts with solderable material. In another example, in some implementations, the process 900 can include forming one or more routing layers on the solidified dielectric material. Interposers including routing layers are described below with reference to Figures 12A–12C. In yet another example, the process 900 can include forming one or more passive components on the solidified dielectric material, as described below with reference to Figure 10.

[0082] Figure 10 shows an example of a flow diagram illustrating a manufacturing process for forming an interposer. The process 1000 begins at block 1002 where an additive process is used to fabricate an interposer layer on a carrier substrate. In some implementations, the additive process includes depositing flowable dielectric material over a plurality of metal interconnect posts after forming the plurality of metal interconnect posts on the carrier substrate.

[0083] The process 1000 continues at block 1004 where one or more passive components are integrated within the interposer layer during the additive process. In some implementations, the one or more passive components include at least one of a resistor, a capacitor or an inductor. In some implementations, block 1004 can include forming one or more passive components on a surface of the interposer layer fabricated in block 1002. For example, a passive component can be vacuum deposited on a dielectric surface or a metal interconnect of the interposer layer. In some implementations, block 1004 can include forming one or more passive components on a sacrificial layer, prior to depositing and curing a flowable dielectric material over the

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passive components. In some implementations, block 1004 can include forming one or more passive components in between deposition of layers of a flowable dielectric material. Passive components can be formed by thin film deposition processes including CVD, atomic layer deposition (ALD), PVD or other vapor deposition technique, electrodeposition, or by ink-jet deposition.

[0084] Figures 11A–11G show examples of cross-sectional schematic illustrations of various stages in a method of manufacturing an interposer layer. Figure 11A is a cross-sectional illustration of a sacrificial layer 1104 covering a carrier substrate 1102. In subsequent operations described below, a through-substrate via interposer layer can be formed on the carrier substrate 1102.

[0085] The carrier substrate 1102 can be glass, plastic, silicon, or other appropriate material. In some implementations, the carrier substrate 1102 can be a large panel or glass plate having an area on the order of about four square meters or more. In some implementations, the carrier substrate 1102 can be provided in a roll, such as a flexible polymer or other flexible material. For example, the carrier substrate 1102 can be provided in a continuous roll of material as part of a roll-to-roll process. Fabrication of the interposer layer on such implementations of the carrier substrate 1102 can facilitate large format batch processing.

[0086] In some implementations, the carrier substrate 1102 can have a thickness of about 50 microns to about 1000 microns. In some implementations, if the carrier substrate 1102 is a large panel, the thickness can be about 300 microns to about 1000 microns. In other implementations, if the carrier substrate 1102 is a roll, the thickness can be about 50 microns to about 300 microns.

[0087] Other substrate materials and thicknesses can be used for the carrier substrate 1102 on which a sacrificial material can be formed. For example, in some implementations, the carrier substrate 1102 can be any material that is inert, has good planarity, is thermally stable at subsequent processing temperatures, and has a similar CTE match with a dielectric material such as spin-on glass. In some implementations, the carrier substrate can be thermally stable at temperatures of at least about 300°, and in some cases, at least about 400°C. The carrier substrate can be substantially planar or can include topographical features. For example, a carrier substrate can include recesses that correspond to the positions of subsequently formed interconnect posts to facilitate the formation of interconnect posts with protrusions.

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[0088] In some implementations, the sacrificial layer 1104 coats the surface of the carrier substrate 1102 on which the through-substrate interposer layer is formed upon, such that removal of the sacrificial layer 1104 releases the carrier substrate 1102 from the interposer layer. The sacrificial layer 1104 can be any material that can be selectively removed without damaging the interposer layer. Examples of sacrificial materials can include metals, semiconductors, and acrylics. For example, the sacrificial material can be a material removable by a wet or dry etching process such as Cu, Mo, MoCr, Al, and amorphous Si. In another example, the sacrificial material can be a material removable by exposure to radiation or thermal treatment such as a UV-removable acrylic. In some implementations, the sacrificial material can be formed from a combination of different sacrificial materials. For example, a first sacrificial material can be used to coat a surface of the carrier substrate 1102 with a second sacrificial material used to form topological features according to the desired implementation. The surface on which the sacrificial layer 1104 is deposited can be planar or include raised or recessed features according to the desired implementation. The sacrificial layer 1104 is generally conformal to the underlying carrier substrate 1102.

[0089] In some implementations, the sacrificial layer 1104 can serve as a seed layer for subsequent interconnect plating. For example, Cu can be both a seed layer and a sacrificial layer. Other examples can include Al, Cr, gold (Au), niobium (Nb), tantalum (Ta), nickel (Ni), tungsten (W), titanium (Ti), and silver (Ag). The sacrificial layer 1104 can be deposited by sputter deposition, though other conformal deposition processes, including ALD, evaporation and other CVD or PVD processes may be used. Example seed layer thicknesses range from about 800 Å to about 10,000 Å, for example from about 1000 Å to about 5000 Å.

[0090] In some other implementations, a seed layer (not shown) can be formed on the sacrificial layer 1104. As examples, a metal seed layer (for example, a Cu seed layer) can be formed on a sacrificial layer of sputtered Al, or a metal seed layer can be formed on a sacrificial layer of a laser-cleavable polymer. Also in some implementations, one or more passive components (not shown) can be fabricated on the sacrificial layer 1104 prior to photoresist deposition.

[0091] Figure 11B shows a cross-sectional illustration of a photoresist layer 1106 formed on the sacrificial layer 1104 and patterned to define interconnect post placement. The photoresist layer 1106 can be patterned by techniques including

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masked exposure to radiation and chemical development. The photoresist layer 1106 can include any suitable photoresist that can be applied and patterned at a desired thickness, can be stripped easily, and can withstand thermal cycles of about 150°C or more. Examples of suitable photoresists can include AZ®4562 and AZ®9260 available from AZ Electronics Materials in Branchburg, New Jersey, Dupont WBR 2000™ Series photoresists, and SU-8 and KMPR photoresists from MicroChem in Newton, Massachusetts.

[0092] The photoresist layer 1106 can have a thickness according to the desired thickness of the interposer layer. The thickness of the photoresist layer 1106 may be about 10% to about 30% greater than the desired interposer layer thickness to accommodate non-uniformity in plating and subsequent planarization. For example, to achieve an interposer thickness of between about 25 microns and about 100 microns, the photoresist thickness can be about 30 microns to about 125 microns.

[0093] Figure 11C shows a cross-sectional illustration of the plated interconnect posts 1108 in the patterned photoresist layer 1106. Any appropriate metal material may be used for the interconnect posts 1108. Examples of interconnect metals may include but are not limited to plated Ni, Ni alloys, Cu, Cu alloys, Au, Au alloys, Al, Al alloys, Ti, Ti alloys, W, W alloys, palladium (Pd), Pd alloys, tin (Sn), Sn alloys, and combinations thereof. In some other implementations, the interconnect posts 1108 can include non-metal conductive materials such as polysilicon in addition to or instead of a metal. In some implementations, the sacrificial layer 1104 has a different metallization than that used for the metal interconnect posts 1108. This is to preserve etch selectivity of the sacrificial layer 1104 with respect to the interconnect posts 1108. For example, a Ni or Ni alloy may be plated on a sputtered Cu layer that functions as sacrificial layer as well as a seed layer. In another example, a Cu or Ni alloy may be plated on a sputtered Cu seed layer, with the Cu seed layer deposited on an Al sacrificial layer. If the sacrificial layer is a laser-cleavable polymer, any appropriate seed layer and interconnect post metallization may be used.

[0094] In some implementations, a solderable material can be plated in the photoresist pattern prior to plating the interconnect posts (not shown). Examples of solderable materials include Cu, Au, Sn, Pd, Ag, and combinations thereof including Au/Sn bilayers, Sn/Ag bilayers, Ni/Pd bilayers, Ni/Au bilayers, and Ni/Pd/Au trilayers.

[0095] Figure 11D shows a cross-sectional illustration of the interconnect posts 1108 on the sacrificial layer 1104 after removal of the photoresist layer 1106. The photoresist

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layer 1106 can be stripped by a technique appropriate for the photoresist, with post-strip cleans of resist-related residue performed in some implementations.

[0096] Figure 11E shows a cross-sectional illustration of a dielectric layer 1110 formed around the interconnect posts 1108. Because the dielectric material of the dielectric layer 1110 is flowable when dispensed or otherwise deposited, it can conformally surround the interconnect posts 1108. The dispensed flowable dielectric material covers and conforms to the topology of the underlying sacrificial layer 1104 and the interconnect posts 1108 without significant voids. For example, the flowable dielectric material may be deposited around the interconnect posts 1108, and in some cases, extend over the tops of the posts. Suitable flowable dielectric materials can include materials with a low dielectric constant, a low loss tangent, and a CTE similar to the CTE of the carrier substrate 1102. Examples of suitable flowable dielectric materials can include epoxies and spin-on dielectrics, such as spin-on glasses.

[0097] A spin-on dielectric refers to any solid dielectric deposited by a spin-on deposition process, which also may be referred to as a spin coating process. In a spin-on deposition process, a liquid solution containing dielectric precursors in a solvent is dispensed on the sacrificial layer 1104. The carrier substrate 1102 may be rotated while or after the solution is dispensed to facilitate uniform distribution of the liquid solution during rotation by centrifugal forces. Rotation speeds of up to about 6000 rpm may be used. Spin-on dielectrics can also include dielectrics formed by dispensing, extruding or casting a liquid solution without subsequent spinning. In some implementations, for example for large panel or continuous roll processes, the spin-on glass can be dispensed with an extrusion mechanism using a blade type nozzle, with no subsequent spinning. The dispensed solution can then be subjected to one or more post-dispensation operations to remove the solvent and form the solid dielectric layer. In some implementations, the dielectric precursor is polymerized during a post-dispensation operation. A spin-on dielectric layer can be an organic or inorganic dielectric layer according to the dielectric precursor used and the desired implementation. In some implementations, multiple layers can be dispensed and cured to build up the spin-on dielectric layer. In implementations where the interposer provides an electrical connection to a glass device substrate, it can be useful to use a dielectric that, once solidified, has a CTE that is matched with the CTE of the glass device substrate. Hence, in some implementations, the dielectric layer 1110 is a spin-on glass layer.

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[0098] In some implementations, the dielectric layer 1110 can include an epoxy, such as a UV curable or thermally curable epoxy, that is flowable when dispensed. The epoxy can be a two-part epoxy with a resin and a hardener. In some implementations, the epoxy can have an epoxide resin and a polyamine hardener. For example, SU-8 from MicroChem in Newton, Massachusetts can be one such suitable epoxy.

[0099] A flowable dielectric material can be cured to solidify it, forming a solid dielectric layer. Figure 11E shows the dielectric layer 1110 after solidification. In some implementations, the dielectric layer 1110 can be cured through a thermal anneal at a temperature of between about 100°C and 450°C. In some implementations, a single dispensation operation can be performed to form the dielectric layer 1110. In some implementations, multiple dispensing/post-dispensing operation cycles can be performed to form the dielectric layer 1110. The dielectric layer 1110 can be dispensed to a thickness greater than the thickness of the interposer layer to accommodate shrinkage during anneal and subsequent planarization. In some implementations, after curing, the surface of a layer of the dielectric material 1110 can include bumps over the interconnect posts 1108, as illustrated in Figure 11E. After curing, the solid dielectric material 1110 can form the substrate material of a through-substrate via interposer layer 1100.

[0100] Figure 11F shows the interposer layer 1100 after planarization of the dielectric layer 1110 and the addition of an optional capping layer. The dielectric layer 1110 can be planarized such that surfaces of the interconnect posts 1108 are exposed and accessible for electrical connection. Planarizing the dielectric layer 1110 can include one or more operations, including lapping, grinding, chemical mechanical planarization (CMP), anisotropic dry etching, or another appropriate method. Furthermore, planarization of the dielectric layer 1110 can remove part of the interconnect posts 1108. In some implementations, planarization can remove between about 5% and about 25% of the interconnect posts 1108.

[0101] Also in some implementations, one or more passive components (not shown), such as capacitors, inductors and resistors, can be fabricated on the dielectric layer 1110 after planarization.

[0102] In some implementations as illustrated in Figure 11F, the interconnect posts 1108 can be capped by plating a solderable material on the exposed surfaces of the interconnect posts 1108. The interconnect caps 1112 can include solderable metallurgies such as Cu, Au, Sn, Pd, Ag, and combinations thereof including Au/Sn

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bilayers, Sn/Ag bilayers, Ni/Pd bilayers, Ni/Au bilayers, and Ni/Pd/Au trilayers. In some implementations, the interconnect caps 1112 have a different metallization than that used for the sacrificial layer 1104. This is to preserve etch selectivity of the sacrificial layer 1104 with respect to the interconnect caps 1112. For example, a Ni/Pd/Au interconnect cap 1112 may be plated on a Ni or Ni alloy interconnect post 1108, with a Cu seed layer serving as the sacrificial layer 1104. In another example, a Cu or Ni/Pd/Au interconnect cap 1112 may be plated on a Cu or Ni alloy interconnect post 1108, with an Al layer serving as the sacrificial the layer 1104.

[0103] In some implementations, the thickness of the plated solderable metal can be between about 0.5 microns and about 2 microns. The interconnect caps 1112 can be used to protect the interconnect posts 1108 from oxidation. In addition, the interconnect caps 1112 can be used to provide an electrical connection between materials that could not otherwise be electrically connected. While the interconnect caps 1112 depicted in Figure 11F cap the interconnect posts 1108 only on the top surface of the interposer layer 1100, in some other implementations, the interconnect posts 1108 can be capped on the bottom surface. For example, as described above with respect to Figure 11C, a solderable material can be plated in the photoresist pattern prior to plating the interconnect posts 1108. The plated solderable material can serve to cap the interconnect posts in some implementations.

[0104] In some implementations, channels 1114 can be formed in the interposer layer 1100 by dicing the dielectric layer 1110. Dicing the dielectric layer 1110 can be achieved by, for example, mechanically sawing or laser cutting the dielectric layer 1110 to form the channels 1114. The channels 1114 can be spaced apart to form the eventual die sizes. In some implementations, the pitch of the channels 1114 can vary between about every 1 mm and about every 15 mm, with the die sizes also between about 1 mm and about 15 mm. In some implementations, the channels 1114 can provide an entry point for a wet etchant that is selective to the sacrificial layer 1104. The channels 1114 may be omitted in some implementations, for example, where the sacrificial layer 1104 is removed via laser ablation.

[0105] Figure 11G shows the diced through-substrate via interposer layer 1100 after being released from the carrier substrate 1102. In some implementations, releasing the interposer layer 1100 from the carrier substrate 1102 can be achieved by etching the exposed sacrificial layer 1104 with an etchant that is selective to the sacrificial layer 1104. Selective etchants can include etchants that have a selectivity of at least about

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100:1 or higher for the sacrificial layer 1104. Specific examples of etchants for selective etching of copper layers include a mixture of acetic acid (CH_3COOH) and hydrogen peroxide (H_2O_2), and ammoniacal-based etchant such as BTP copper etchant from Transene Company, Inc. in Danvers, Massachusetts. Examples of etchants for selective etching of aluminum layers include sodium hydroxide (NaOH), potassium hydroxide (KOH), and alkaline solutions combined with an oxidizer. In some implementations, releasing the interposer layer 1100 from the carrier substrate 1102 can be achieved by laser ablation of the sacrificial layer 1104. The laser beam can ablate the sacrificial layer 1104 through a transparent carrier substrate 1102. The laser beam can have a selected wavelength sufficient to ablate the sacrificial layer 1104, which can be made of a laser-cleavable polymer. In some implementations, the released carrier substrate 1102 can be reused. In some implementations, the carrier substrate may be ground, etched, or otherwise removed.

[0106] In some implementations, the dielectric layer 1110 can be etched back such that interconnect posts 1108 protrude along the bottom surface of the dielectric layer 1110 (not shown). In some implementations, protruding interconnect posts 1108 can be formed without etching back the dielectric layer 1110, for example, by using a carrier substrate having topographical features.

[0107] The resulting interposer layer 1100 can be between about 10 and 100 microns thick according to various implementations. Thicker interposer layers can also be fabricated in some implementations. For example, an interposer layer of about 300 microns to 500 microns can be fabricated using a photoresist of about 400 microns to about 600 microns thick. In some implementations, if for example such thick photoresists are not available, thicker interposer layers can be fabricated using multiple cycles of lithography, plating, flowable dielectric deposition and planarization. These cycles can be performed sequentially to build up an interposer layer of desired thickness on a carrier substrate, or can be performed in parallel with the resulting interposer layers stacked to form an interposer layer of any thickness. Accordingly, single or multiple cycles can be used to fabricate interposer layers of about 10 microns to over 500 microns thick. In some implementations, thinner through-substrate via interposers can correspond to faster performance in integrated circuit systems, and to a thinner stack height when in a stacked configuration.

[0108] The interconnect posts 1108 in the interposer layer 1100 can made of any suitable electrically conductive material. As noted above, examples of interconnect post

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materials can include but are not limited to Ni, Ni alloy, and Cu. In some implementations, the interconnect posts 1108 can be made of Cu, which has a low resistivity.

[0109] Additionally, the interconnect posts 1108 can have any appropriate size and shape. In some implementations, the height to width aspect ratio of the interconnect posts 1108 can be greater than about 5:1. For example, the interconnect posts 1108 can have a diameter between about 5 microns and about 100 microns. The height of the interconnect posts 1108 can be between about 10 microns and 500 microns, for example between about 25 microns and 100 microns. The interconnect posts 1108 can also be configured according to various shapes, such as circular, square, octagonal, hexagonal, and rectangular.

[0110] In some implementations, fabrication of an interposer may be complete at this stage, with the interposer including the interposer layer 1100 having through-substrate interconnects posts 1108 as well as other components, if any, formed on the solidified dielectric layer 1110 and/or on the interconnect posts 1108 such as the interconnect caps 1112 or passive components (not shown). In some other implementations, an interposer may further include one or more additional layers, such as routing or redistribution layers.

[0111] Figures 12A–12C show examples of cross-sectional schematic illustrations of varying implementations of interposers with one or more routing layers. A through-substrate via interposer 1200 can have routing layers 1216 on either or both sides of a through-substrate via interposer layer 1210. The through-substrate via interposer layer 1210 can be manufactured by any of the methods described above. A routing layer 1216, otherwise referred to as a redistribution layer (RDL), can include a plurality of electrically conductive routing lines 1212 and RDL contacts 1214 embedded in a dielectric material for carrying electrical signals. RDL pads 1218 can be disposed on the routing layer 1216 to provide a point of external electrical connection. In some implementations, the routing layer 1216 can serve as an electrical interconnect between the contact points of interconnect posts 1208 in the through-substrate via interposer layer 1210 and various dies (not shown) through routing lines 1212, RDL contacts 1214, and RDL pads 1218. Although Figures 12A–12C show only one routing layer 1216 on the top and/or bottom side of the through-substrate via interposer layer 1210, in some implementations, there can be more than one routing layer 1216 on each side.

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[0112] Each routing layer 1216 can be formed by a series of process steps including deposition of dielectric material and conductive lines, photolithography, etching, and planarization. The dielectric material in a routing layer 1216 can be a solidified flowable dielectric material as described above or can be another dielectric material. Examples of dielectric materials include a polyimide material, a benzocyclobutene material, a polybenzoxazole material, and an ABF film available from Ajinomoto Fine-Techno. In one example, the routing lines 1212 can be about 10 microns thick, and dielectric thickness in the routing layer 1216 can be about 15 microns to 25 microns thick.

[0113] The interconnect posts 1208 and other electrical components such as the routing lines 1212, the RDL contacts 1214, and the RDL pads 1218, can be defined according to density. In some implementations, the density of one or more of the routing lines 1212, the RDL contacts 1214 and the RDL pads 1218 can be greater than the density of the interconnect posts 1208. Alternatively, the interconnect posts 1208, the routing lines 1212, the RDL contacts 1214, and the RDL pads 1218 can be defined according to pitch, where pitch defines the center-to-center spacing between electrically conductive components. In some implementations, the pitch at the top surface of the interposer 1200 can be greater than the pitch at the bottom surface of the interposer 1200. For example, the pitch of the interconnect posts 1208 can be greater than the pitch of the RDL pads 1218. In some implementations, the pitch at the top surface of the interposer 1200 can be between about 20 microns and 125 microns and the pitch at the bottom surface of the interposer 1200 can be between about 100 microns and 500 microns.

[0114] In some implementations, the routing layer 1216 can include passive components (not shown). For example, passive components such as capacitors, resistors, and/or inductors can be coupled with the routing lines 1212 in the routing layer 1216 to provide regulated power between the interconnect posts 1208 and the various dies. Examples of passive components in a routing layer are described below with respect to Figure 13.

[0115] Figure 12A shows a cross-sectional illustration of an interposer 1200 including a routing layer 1216 and a through-substrate via interposer layer 1210, with the routing layer 1216 disposed on the top surface of the through-substrate via interposer layer 1210. In some implementations, the routing layer 1216 may be manufactured after planarization of the dielectric material of the through-substrate via interposer layer

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1210. For example, a routing layer may be formed on the top surface of the interposer layer 1100 shown in Figure 11F or Figure 11G, or after block 908 of Figure 9. The routing layer 1216 may include passive components that electrically connect to the interconnect posts 1208.

[0116] Figure 12B shows a cross-sectional illustration of an interposer 1200 including a routing layer 1216 and a through-substrate via interposer layer 1210, with the routing layer 1216 disposed on the bottom surface of the through-substrate via interposer layer 1210. In some implementations, the routing layer 1216 may be manufactured after forming the sacrificial layer on the carrier substrate but before applying any patterned photoresist layer. For example, a routing layer may be formed on the sacrificial layer 1104 in Figure 11A or after block 902 in Figure 9. In some implementations, the routing layer 1216 may be manufactured after release of a carrier substrate. For example, a routing layer may be formed on the bottom surface of the dielectric layer 1110 in Figure 11G. The routing layer 1216 may include passive components that electrically connect to the interconnect posts 1208.

[0117] Figure 12C shows a cross-sectional illustration of an interposer 1200 with routing layers 1216a and 1216b on both the top and bottom surface of a through-substrate via interposer layer 1200. In some implementations, the routing layer 1216b may be manufactured after forming the sacrificial layer on the carrier substrate but before applying any patterned photoresist. In some implementations, one or both of the routing layers 1216a and 1216b may be manufactured after planarization of the dielectric material. The routing layers 1216a and 1216b can include passive components that electrically connect to the interconnect posts 1208.

[0118] The interposers described herein may be applied with various components in 3-D electronics packaging depending on the application. In some implementations, the interposer may be implemented in one or more application specific integrated circuits (ASICs), digital signal processors (DSPs), digital signal processing devices (DSPDs), programmable logic devices (PLDs), field programmable gate arrays (FPGAs), memory stacks, processors, controllers, microcontrollers, and other electronic devices. One example of an interposer as implemented in a 3-D device package is depicted in Figure 13, described below.

[0119] Figure 13 shows an example of a cross-sectional schematic illustration of stacked dies on an interposer according to one implementation. The packaging system includes a packaging substrate 1322, which can be a material that provides base

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mechanical support to the 3-D device package. In some implementations, the packaging substrate 1322 can be a metal, semiconductor, ceramic, plastic, glass, or a ceramic, organic or fiberglass printed circuit board (PCB) material.

[0120] In Figure 13, the packaging system can include electrical connectors 1320 positioned over a packaging substrate 1322. In some implementations, the electrical connectors 1320 can include under bump metallization (UBM) or solder balls in contact with the packaging substrate 1322. In some implementations, the electrical connectors 1320 may be positioned under the packaging substrate 1322. The electrical connectors 1320 can serve to electrically and physically couple components within the packaging system and can be made of electrically conductive material. As illustrated in Figure 13, the electrical connectors 1320 can connect an interposer 1300 with the packaging substrate 1322 so that the interposer 1300 is in electrical communication with the packaging substrate 1322.

[0121] The interposer 1300, such as one manufactured by any of the methods described earlier herein, can include a solidified dielectric material 1310 and one or more metal interconnect posts 1308 extending through the solidified dielectric material 1310. In some implementations, the solidified dielectric material 1310 includes spin-on glass or epoxy material. The interposer 1300 can further include routing layers 1316a and 1316b with electrically conductive routing lines 1318a and 1318b connected to the one or more metal interconnect posts 1308. In some implementations, the interposer layer 1300 can include one or more passive components such as one or more inductors, capacitors, or resistors. For example, the passive components can include an inductor electrically coupled to the routing lines 1318 to regulate electrical flow. In Figure 13, the routing layer 1316a includes a metal-insulator-metal capacitor formed by insulator layer 1342 and metal layers 1340 and a spiral inductor 1344. The conductive and insulator materials used to form passive components can be the same or different materials used to form the routing lines and main dielectric material of a routing layer.

[0122] The routing layer 1316a is a multi-layer redistribution network including alternating layers of metallization and dielectric material. In some implementations, forming the routing layer 1316a includes forming alternate layers of plated metal, such as plated Cu, and dielectric film. The uppermost layer can include UBM (not shown) for attaching dies.

[0123] The packaging system can further include electrical connectors 1326 to connect the interposer 1300 with dies 1328, 1330, 1332, and 1334 positioned over the interposer

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1300. The electrical connectors 1326 can be any appropriate electrically conductive material such as solder balls. In some implementations, the density of the electrical connectors 1326 from the routing layer 1316 of the interposer 1300 to the dies 1328, 1330, 1332, and 1334 can be greater than the density of the electrical connectors 1320 from the packaging substrate 1322 to the interposer 1300. In some implementations, two or more of the dies 1328, 1330, 1332, and 1334 can be stacked or mounted over one another. In some implementations, the dies 1328, 1330, 1332, and 1334 can include one of a memory, logic, or MEMS chip. It is understood that any number of dies may be mounted in various configurations over the interposer 1300 to achieve a desired implementation. In some implementations, an interposer can have a CTE between the CTE's of the dies, substrates, or layers that it connects. For example, in some implementations, an overlying silicon die may have a CTE of about 3 parts per million (ppm) and an underlying PCB may have a CTE of about 16 ppm; an interposer layer disposed between the silicon die and the PCB may have a CTE between about 3 ppm and 16 ppm, for example, between about 5 and 14 ppm.

[0124] In some implementations, an interposer can be used as part of a 3-D or other package including a display or non-display device fabricated on a glass or epoxy substrate, the combination having well-matched thermal expansion properties. In some implementations, the interposer can be used to communicate data to a processor (such as processor 21 of Figure 16B).

[0125] Figures 14A–14D show examples of cross-sectional schematic illustrations of various stages in a method of forming an interposer. The interposer 1400 is formed in a sequence of stages including forming a plurality of interconnect posts 1408 on a sacrificial layer 1404 that has been deposited on a carrier substrate 1402 such as a glass substrate or panel, as shown in Figure 14A. The sacrificial layer 1404 may also serve as a seed layer for subsequent electro- or electroless plating. An additional seed layer (not shown) may be deposited on the sacrificial layer 1404 prior to plating the interconnect posts. The interconnect posts 1408 may be formed by spinning, dispensing, or otherwise depositing a photoresist layer (not shown) on the sacrificial layer 1404; exposing and developing the photoresist layer to form holes for the interconnect posts 1408; and plating the interconnect posts 1408 through the patterned photoresist. The photoresist layer is subsequently removed. As shown in Figure 14B, one or more flowable dielectric layers 1410 may be spun, dispensed, cast, or otherwise deposited around and possibly over the interconnect posts 1408 on the sacrificial layer 1404. The

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dielectric layer 1410 is solidified and may be planarized to expose the interconnect posts 1408. As shown in Figure 14C, dicing streets 1414 may be cut through the dielectric layer 1410 to expose at least a portion of the sacrificial layer 1404. The cuts may extend into or through the carrier substrate 1402. As shown in Figure 14D, a sacrificial layer etchant may be used to remove the sacrificial layer 1404 and release the interposer 1400, including interconnect posts 1408, from the carrier substrate 1402.

[0126] One or more routing layers (not shown) may be formed on an upper side, lower side, or both sides of the interposer 1400 prior to depositing the flowable dielectric layer 1410 or after the planarization of the dielectric layer 1410, as described above with respect to Figures 12A–12C. One or more passive components (not shown) such as a resistor, a capacitor, an inductor, a coupling transformer, or a power combiner may be formed on an upper side or a lower side of the interposer 1400, as described above with respect to Figure 10 and Figure 13.

[0127] Figures 15A and 15B show examples of cross-sectional schematic illustrations of an interposer positioned between an integrated circuit chip and a packaging substrate. In Figure 15A, an interposer 1500 with a plurality of interconnect posts 1508 is connected between a packaging substrate 1522, such as a PCB, and an integrated circuit chip 1530, also referred to as a die that may be a memory chip, a logic device, a radio frequency (RF) chip, an ASIC, a MEMS chip, or other electronic or mechanical device. Solder bumps or balls 1520 may be used to attach the interposer 1500 to the packaging substrate 1522. Similarly, solder bumps or balls 1526 may be used to attach integrated circuit chip 1530 to corresponding interconnect posts 1508 on interposer 1500. Additional dies (not shown) may be stacked on top of integrated circuit chip 1530, or positioned laterally to integrated circuit chip 1530 and connected to other interconnect posts 1508.

[0128] The interposer 1500 may provide stress isolation and strain relief when the interposer 1500 is connected between the packaging substrate 1522 and the integrated circuit chip 1530. Strain relief may be provided, for example, when the temperature of the integrated circuit chip 1530 rises substantially with respect to the packaging substrate 1522. Alternatively, strain relief may be provided when the overall temperature of integrated circuit chip 1530, interposer 1500, and packaging substrate 1522 rise and stress is generated due to differences in the CTE between the integrated circuit chip 1530 and the packaging substrate 1522. Extra interconnect posts 1508b, as shown in Figure 15B, may be provided to enhance the strain relief due to CTE

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mismatches. The extra interconnect posts 1508b may be attached only to the packaging substrate 1522 as shown, attached only to the integrated circuit die 1530 (not shown), or attached to both the integrated circuit die 1530 and the packaging substrate 1522. Extra bond pads may be provided on the integrated circuit chip 1530 or the packaging substrate 1522 that are dedicated to strain relief.

[0129] Alternatively or in addition to providing electrical connections and possible strain relief between the integrated circuit chip 1530 and the packaging substrate 1522, one or more interconnect posts 1508 may be positioned to provide increased heat transfer between the integrated circuit chip 1530 and the packaging substrate 1522, so that the integrated circuit chip 130 may be kept at a lower temperature closer to that of the packaging substrate 1522 during operation.

[0130] An underfill material (not shown) such as an epoxy may be positioned between the interposer 1500 and the underlying packaging substrate 1522. The underfill material may be injected, for example, between the interposer 1500 and the packaging substrate 1522 and then cured. The underfill material may provide additional stress isolation and protection from excessive shearing forces that may develop during high temperature excursions. The underfill material may also provide additional heat transfer capability between the interposer 1500 and the packaging substrate 1522. Similarly, underfill material may be positioned between the interposer 1500 and an attached integrated circuit chip 1530. Molding compound (not shown) customary in many packaging configurations may be placed over the integrated circuit chip 1530, the interposer 1500, and portions of the packaging substrate 1522.

[0131] Figures 16A and 16B show examples of system block diagrams illustrating a display device 40 that includes a plurality of interferometric modulators. The display device 40 can be, for example, a cellular or mobile telephone. However, the same components of the display device 40 or slight variations thereof are also illustrative of various types of display devices such as televisions, e-readers and portable media players.

[0132] The display device 40 includes a housing 41, a display 30, an antenna 43, a speaker 45, an input device 48, and a microphone 46. The housing 41 can be formed from any of a variety of manufacturing processes, including injection molding, and vacuum forming. In addition, the housing 41 may be made from any of a variety of materials, including, but not limited to: plastic, metal, glass, rubber, and ceramic, or a combination thereof. The housing 41 can include removable portions (not shown) that

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may be interchanged with other removable portions of different color, or containing different logos, pictures, or symbols.

[0133] The display 30 may be any of a variety of displays, including a bi-stable or analog display, as described herein. The display 30 also can be configured to include a flat-panel display, such as plasma, EL, OLED, STN LCD, or TFT LCD, or a non-flat-panel display, such as a CRT or other tube device. In addition, the display 30 can include an interferometric modulator display, as described herein.

[0134] The components of the display device 40 are schematically illustrated in Figure 16B. The display device 40 includes a housing 41 and can include additional components at least partially enclosed therein. For example, the display device 40 includes a network interface 27 that includes an antenna 43 which is coupled to a transceiver 47. The transceiver 47 is connected to a processor 21, which is connected to conditioning hardware 52. The conditioning hardware 52 may be configured to condition a signal (e.g., filter a signal). The conditioning hardware 52 is connected to a speaker 45 and a microphone 46. The processor 21 is also connected to an input device 48 and a driver controller 29. The driver controller 29 is coupled to a frame buffer 28, and to an array driver 22, which in turn is coupled to a display array 30. A power supply 50 can provide power to all components as required by the particular display device 40 design.

[0135] The network interface 27 includes the antenna 43 and the transceiver 47 so that the display device 40 can communicate with one or more devices over a network. The network interface 27 also may have some processing capabilities to relieve, e.g., data processing requirements of the processor 21. The antenna 43 can transmit and receive signals. In some implementations, the antenna 43 transmits and receives RF signals according to the IEEE 16.11 standard, including IEEE 16.11(a), (b), or (g), or the IEEE 802.11 standard, including IEEE 802.11a, b, g or n. In some other implementations, the antenna 43 transmits and receives RF signals according to the BLUETOOTH standard. In the case of a cellular telephone, the antenna 43 is designed to receive code division multiple access (CDMA), frequency division multiple access (FDMA), time division multiple access (TDMA), Global System for Mobile communications (GSM), GSM/General Packet Radio Service (GPRS), Enhanced Data GSM Environment (EDGE), Terrestrial Trunked Radio (TETRA), Wideband-CDMA (W-CDMA), Evolution Data Optimized (EV-DO), 1xEV-DO, EV-DO Rev A, EV-DO Rev B, High Speed Packet Access (HSPA), High Speed Downlink Packet Access (HSDPA), High

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Speed Uplink Packet Access (HSUPA), Evolved High Speed Packet Access (HSPA+), Long Term Evolution (LTE), AMPS, or other known signals that are used to communicate within a wireless network, such as a system utilizing 3G or 4G technology. The transceiver 47 can pre-process the signals received from the antenna 43 so that they may be received by and further manipulated by the processor 21. The transceiver 47 also can process signals received from the processor 21 so that they may be transmitted from the display device 40 via the antenna 43.

[0136] In some implementations, the transceiver 47 can be replaced by a receiver. In addition, the network interface 27 can be replaced by an image source, which can store or generate image data to be sent to the processor 21. The processor 21 can control the overall operation of the display device 40. The processor 21 receives data, such as compressed image data from the network interface 27 or an image source, and processes the data into raw image data or into a format that is readily processed into raw image data. The processor 21 can send the processed data to the driver controller 29 or to the frame buffer 28 for storage. Raw data typically refers to the information that identifies the image characteristics at each location within an image. For example, such image characteristics can include color, saturation, and gray-scale level.

[0137] The processor 21 can include a microcontroller, CPU, or logic unit to control operation of the display device 40. The conditioning hardware 52 may include amplifiers and filters for transmitting signals to the speaker 45, and for receiving signals from the microphone 46. The conditioning hardware 52 may be discrete components within the display device 40, or may be incorporated within the processor 21 or other components.

[0138] The driver controller 29 can take the raw image data generated by the processor 21 either directly from the processor 21 or from the frame buffer 28 and can re-format the raw image data appropriately for high speed transmission to the array driver 22. In some implementations, the driver controller 29 can re-format the raw image data into a data flow having a raster-like format, such that it has a time order suitable for scanning across the display array 30. Then the driver controller 29 sends the formatted information to the array driver 22. Although a driver controller 29, such as an LCD controller, is often associated with the system processor 21 as a stand-alone Integrated Circuit (IC), such controllers may be implemented in many ways. For example, controllers may be embedded in the processor 21 as hardware, embedded in the processor 21 as software, or fully integrated in hardware with the array driver 22.

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[0139] The array driver 22 can receive the formatted information from the driver controller 29 and can re-format the video data into a parallel set of waveforms that are applied many times per second to the hundreds, and sometimes thousands (or more), of leads coming from the display's x-y matrix of pixels.

[0140] In some implementations, the driver controller 29, the array driver 22, and the display array 30 are appropriate for any of the types of displays described herein. For example, the driver controller 29 can be a conventional display controller or a bi-stable display controller (e.g., an IMOD controller). Additionally, the array driver 22 can be a conventional driver or a bi-stable display driver (e.g., an IMOD display driver). Moreover, the display array 30 can be a conventional display array or a bi-stable display array (e.g., a display including an array of IMODs). In some implementations, the driver controller 29 can be integrated with the array driver 22. Such an implementation is common in highly integrated systems such as cellular phones, watches and other small-area displays

[0141] In some implementations, the input device 48 can be configured to allow, e.g., a user to control the operation of the display device 40. The input device 48 can include a keypad, such as a QWERTY keyboard or a telephone keypad, a button, a switch, a rocker, a touch-sensitive screen, or a pressure- or heat-sensitive membrane. The microphone 46 can be configured as an input device for the display device 40. In some implementations, voice commands through the microphone 46 can be used for controlling operations of the display device 40.

[0142] The power supply 50 can include a variety of energy storage devices as are well known in the art. For example, the power supply 50 can be a rechargeable battery, such as a nickel-cadmium battery or a lithium-ion battery. The power supply 50 also can be a renewable energy source, a capacitor, or a solar cell, including a plastic solar cell or solar-cell paint. The power supply 50 also can be configured to receive power from a wall outlet.

[0143] In some implementations, control programmability resides in the driver controller 29 which can be located in several places in the electronic display system. In some other implementations, control programmability resides in the array driver 22. The above-described optimization may be implemented in any number of hardware and/or software components and in various configurations.

[0144] The various illustrative logics, logical blocks, modules, circuits and algorithm steps described in connection with the implementations disclosed herein may be

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implemented as electronic hardware, computer software, or combinations of both. The interchangeability of hardware and software has been described generally, in terms of functionality, and illustrated in the various illustrative components, blocks, modules, circuits and steps described above. Whether such functionality is implemented in hardware or software depends upon the particular application and design constraints imposed on the overall system.

[0145] The hardware and data processing apparatus used to implement the various illustrative logics, logical blocks, modules and circuits described in connection with the aspects disclosed herein may be implemented or performed with a general purpose single- or multi-chip processor, a digital signal processor (DSP), an application specific integrated circuit (ASIC), a field programmable gate array (FPGA) or other programmable logic device, discrete gate or transistor logic, discrete hardware components, or any combination thereof designed to perform the functions described herein. A general purpose processor may be a microprocessor, or, any conventional processor, controller, microcontroller, or state machine. A processor also may be implemented as a combination of computing devices, e.g., a combination of a DSP and a microprocessor, a plurality of microprocessors, one or more microprocessors in conjunction with a DSP core, or any other such configuration. In some implementations, particular steps and methods may be performed by circuitry that is specific to a given function

[0146] In one or more aspects, the functions described may be implemented in hardware, digital electronic circuitry, computer software, firmware, including the structures disclosed in this specification and their structural equivalents thereof, or in any combination thereof. Implementations of the subject matter described in this specification also can be implemented as one or more computer programs, i.e., one or more modules of computer program instructions, encoded on a computer storage media for execution by, or to control the operation of, data processing apparatus.

[0147] Various modifications to the implementations described in this disclosure may be readily apparent to those having ordinary skill in the art, and the generic principles defined herein may be applied to other implementations without departing from the spirit or scope of this disclosure. Thus, the claims are not intended to be limited to the implementations shown herein, but are to be accorded the widest scope consistent with this disclosure, the principles and the novel features disclosed herein. The word "exemplary" is used exclusively herein to mean "serving as an example, instance, or

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illustration." Any implementation described herein as "exemplary" is not necessarily to be construed as preferred or advantageous over other implementations. Additionally, a person having ordinary skill in the art will readily appreciate, the terms "upper" and "lower" are sometimes used for ease of describing the figures, and indicate relative positions corresponding to the orientation of the figure on a properly oriented page, and may not reflect the proper orientation of the IMOD as implemented.

[0148] Certain features that are described in this specification in the context of separate implementations also can be implemented in combination in a single implementation. Conversely, various features that are described in the context of a single implementation also can be implemented in multiple implementations separately or in any suitable subcombination. Moreover, although features may be described above as acting in certain combinations and even initially claimed as such, one or more features from a claimed combination can in some cases be excised from the combination, and the claimed combination may be directed to a subcombination or variation of a subcombination.

[0149] Similarly, while operations are depicted in the drawings in a particular order, this should not be understood as requiring that such operations be performed in the particular order shown or in sequential order, or that all illustrated operations be performed, to achieve desirable results. Further, the drawings may schematically depict one more example processes in the form of a flow diagram. However, other operations that are not depicted can be incorporated in the example processes that are schematically illustrated. For example, one or more additional operations can be performed before, after, simultaneously, or between any of the illustrated operations. In certain circumstances, multitasking and parallel processing may be advantageous. Moreover, the separation of various system components in the implementations described above should not be understood as requiring such separation in all implementations, and it should be understood that the described program components and systems can generally be integrated together in a single software product or packaged into multiple software products. Additionally, other implementations are within the scope of the following claims. In some cases, the actions recited in the claims can be performed in a different order and still achieve desirable results.

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CLAIMS

What is claimed is:

1. A method of forming an interposer comprising:

forming a sacrificial layer on a carrier substrate;

forming a plurality of interconnect posts on the sacrificial layer, the interconnect posts oriented substantially perpendicularly to the carrier substrate;

depositing and solidifying one or more flowable dielectric layers to cover the sacrificial layer and the plurality of interconnect posts with a dielectric material; and

planarizing the solidified dielectric material to expose the plurality of interconnect posts and to form an interposer layer releasably attached to the carrier substrate via the sacrificial layer.

2. The method of claim 1, wherein the one or more flowable dielectric layers include one or more spin-on dielectric layers.

3. The method of claim 1 or 2, wherein the one or more flowable dielectric layers include one or more epoxy layers.

4. The method of any of claims 1-3, wherein forming a plurality of interconnect posts includes plating a plurality of metal posts in a patterned photoresist layer.

5. The method of any of claims 1-4, further comprising forming one or one more passive components on the solidified dielectric material.

6. The method of claim 5, wherein forming the one or more passive components is performed after planarizing the solidified dielectric material.

7. The method of claim 5 or 6, wherein forming the one or more passive components is performed after forming the sacrificial layer on the carrier substrate but before depositing any flowable dielectric layers.

8. The method of any of claims 1-7, further comprising forming one or more routing layers on the solidified dielectric material.

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9. The method of any of claims 1-8, further comprising plating the plurality of interconnect posts with solderable material.

10. An interposer comprising:

an additive glass interposer layer; and

one or more metal interconnect posts extending through the glass interposer layer.

11. The interposer of claim 10, further comprising one or more passive components on the glass interposer layer.

12. The interposer of claim 11, wherein the one or more passive components include at least one of a resistor, a capacitor, and an inductor.

13. The interposer of any of claims 10-12, wherein the one or more metal interconnect posts include at least one of nickel, a nickel alloy, and copper.

14. The interposer of any of claims 10-13, wherein the one or more metal interconnect posts have a height to width aspect ratio of greater than about 5:1.

15. The interposer of any of claims 10-14, wherein the one or more metal interconnect posts have a height of from about 10 microns to about 500 microns and a width of from about 5 microns to about 100 microns.

16. The interposer of any of claims 10-15, wherein the glass interposer layer has a thickness between about 10 and 500 microns.

17. The interposer of any of claims 10-16, wherein the one or more interconnect posts include an interconnect cap that protrudes from the glass interposer layer.

18. The interposer of claim 17, wherein the interconnect cap includes a solderable material.

19. The interposer of any of claims 10-18, further comprising a routing layer including electrically conductive routing lines connected to the one or more metal interconnect posts.

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20. The interposer of claim 19, wherein the density of the routing lines is greater than the density of the metal interconnect posts.

21. A method of forming an interposer, comprising:

using an additive process to fabricate an additive glass interposer layer on a carrier substrate; and

integrating one or more passive components within the interposer layer during the additive process.

22. The method of claim 21, wherein the one or more passive components include at least one of a resistor, a capacitor and an inductor.

23. The method of claim 21 or 22, wherein using the additive process includes depositing flowable dielectric material around a plurality of metal interconnect posts and the carrier substrate after forming the plurality of metal interconnect posts on the carrier substrate.

24. An apparatus, comprising:

a packaging substrate;

an interposer layer in electrical communication with the packaging substrate, wherein the interposer layer includes:

a solidified dielectric material;

one or more metal interconnect posts extending through the solidified dielectric material;

a routing layer including electrically conductive routing lines connected to the one or more metal interconnect posts; and

one or more dies positioned over the interposer layer, wherein the density of electrical connections from the routing layer to the one or more dies is greater than the density of electrical connections from the interposer layer to the packaging substrate.

25. The apparatus of claim 24, wherein the one or more dies include at least one of memory, logic, radio frequency (RF), ASIC or MEMS chips.

26. The apparatus of claim 24 or 25, wherein the one or more dies includes a plurality of stacked dies.

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27. The apparatus of any of claims 24-26, further comprising one or more passive components within the interposer layer.

28. The apparatus of any of claims 24-27, wherein the solidified dielectric material includes spin-on-glass or epoxy.

29. The apparatus of any of claims 24-28, further comprising:
a display;
a processor that is configured to communicate with the display, the processor being configured to process image data; and
a memory device that is configured to communicate with the processor.

30. The apparatus of claim 29, further comprising:
a driver circuit configured to send at least one signal to the display; and
a controller configured to send at least a portion of the image data to the driver circuit.

31. The apparatus of claim 29 or 30, further comprising:
an image source module configured to send the image data to the processor.

32. The apparatus of claim 31, wherein the image source module includes at least one of a receiver, transceiver, and transmitter.

33. The apparatus of any of claims 29-32, further comprising:
an input device configured to receive input data and to communicate the input data to the processor.

34. An apparatus, comprising:
an interposer, wherein the interposer is formed by forming a plurality of interconnect posts on a sacrificial layer, the sacrificial layer formed on a carrier substrate; depositing and solidifying one or more flowable dielectric layers around the interconnect posts; planarizing the solidified dielectric material to expose the interconnect posts; and releasing the interposer from the carrier substrate by sacrificially etching the sacrificial layer.

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35. The apparatus of claim 34, wherein at least one interconnect post provides strain relief when the interposer is connected between a packaging substrate and an integrated circuit chip.

36. The apparatus of claim 34 or 35, wherein at least one interconnect post allows heat transfer between an integrated circuit chip and a packaging substrate, the interposer connected between the packaging substrate and the integrated circuit chip.

37. The apparatus of any of claims 34-36, further comprising one or more routing layers on an upper side or a lower side of the interposer.

38. The apparatus of any of claims 34-37, further comprising at least one passive component formed on an upper side or a lower side of the interposer.

39. The apparatus of any of claims 34-38, further comprising at least one integrated circuit chip attached to the interposer.

40. The apparatus of any of claims 34-39, further comprising a packaging substrate attached to the interposer.

41. The apparatus of any of claims 34-40, wherein the packaging substrate is a printed circuit board.

42. The apparatus of any of claims 34-41, wherein the interposer provides stress isolation between the packaging substrate and an integrated circuit chip attached to the interposer.

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TSMC EX1032 Page 61

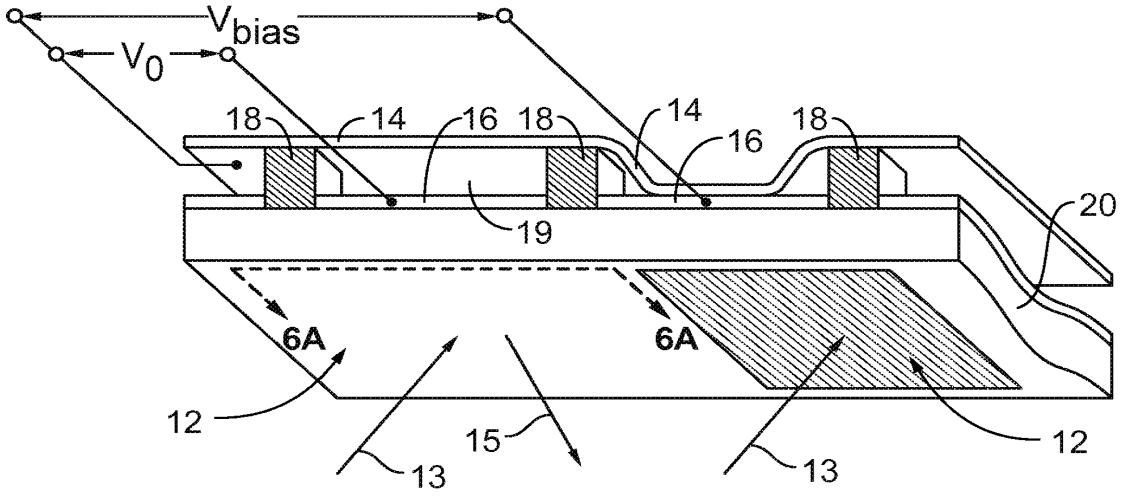


Figure 1

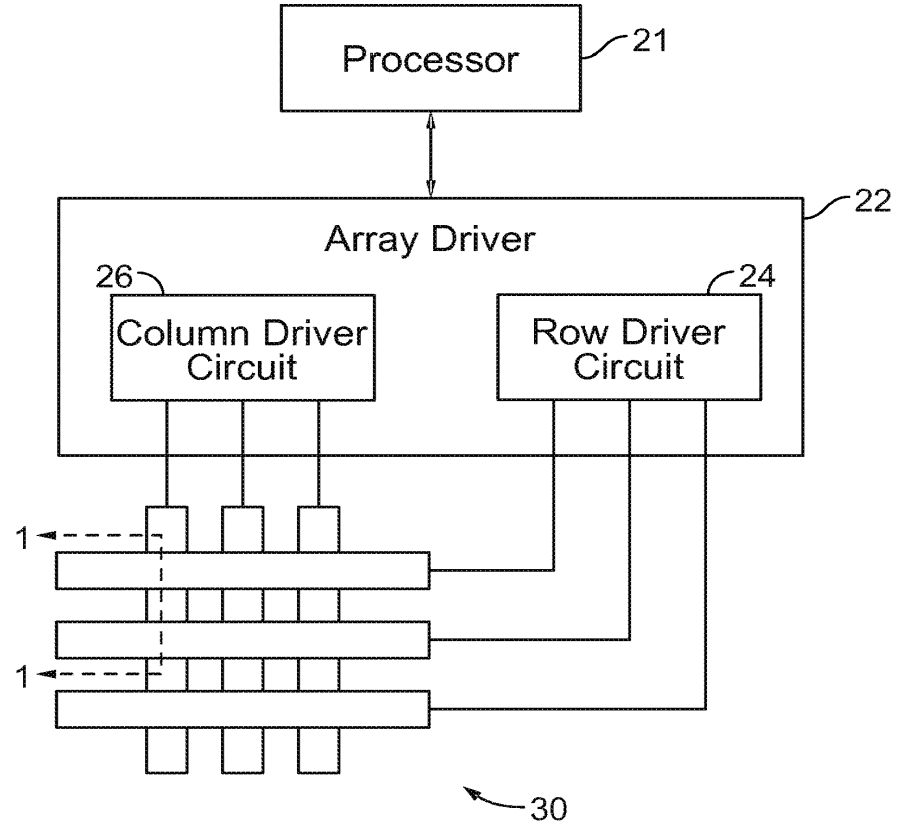


Figure 2

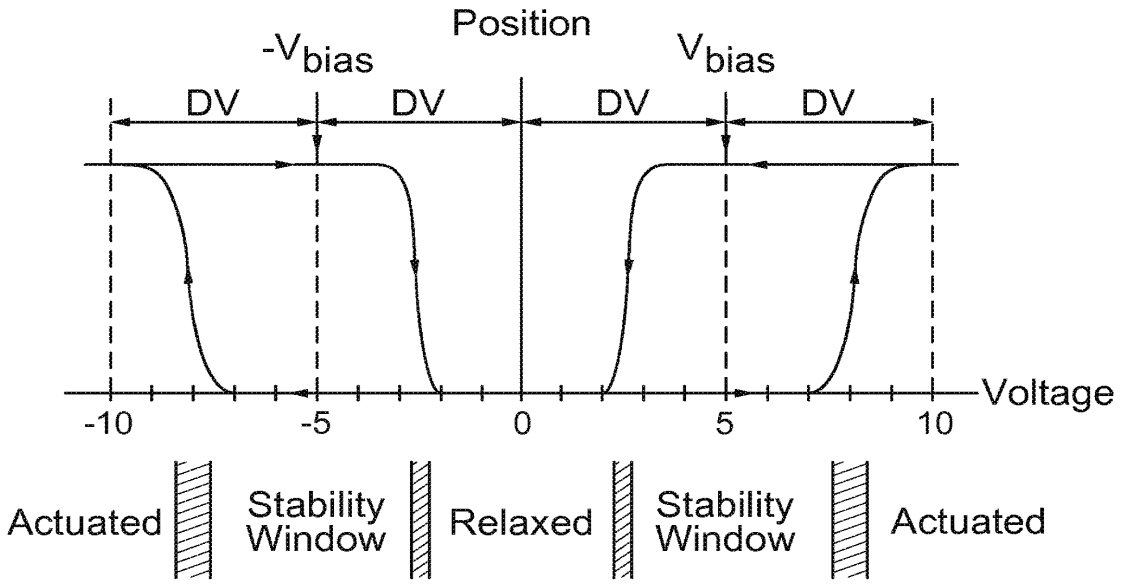


Figure 3

Common Voltages

Segment Voltages	VC_{ADD_H}	VC_{HOLD_H}	VC_{REL}	VC_{HOLD_L}	VC_{ADD_L}
VS_H	Stable	Stable	Relax	Stable	Actuate
VS_L	Actuate	Stable	Relax	Stable	Stable

Figure 4

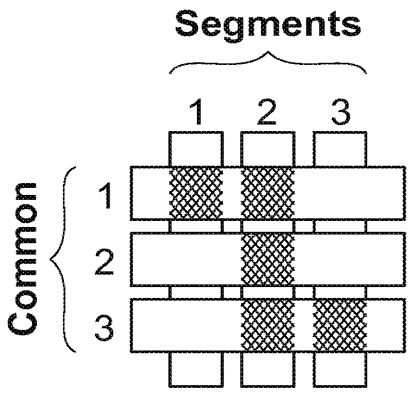


Figure 5A

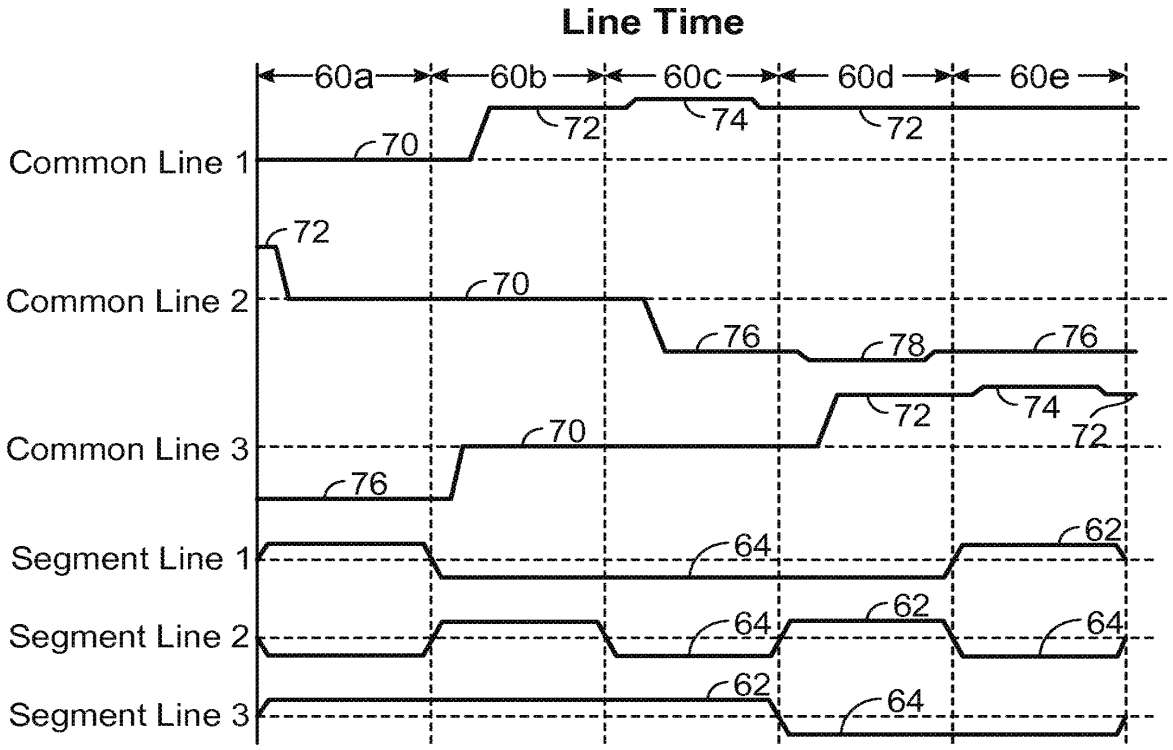


Figure 5B

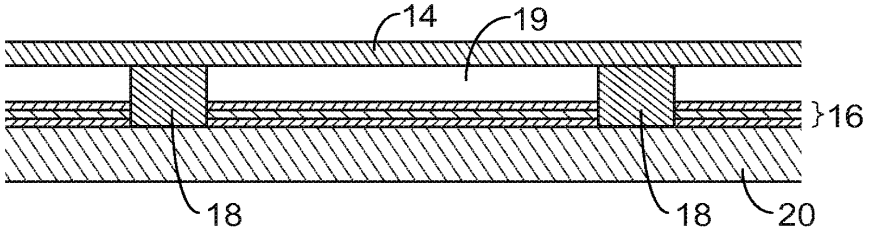


Figure 6A

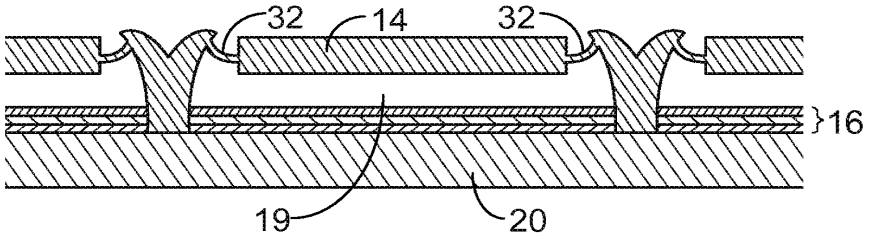


Figure 6B

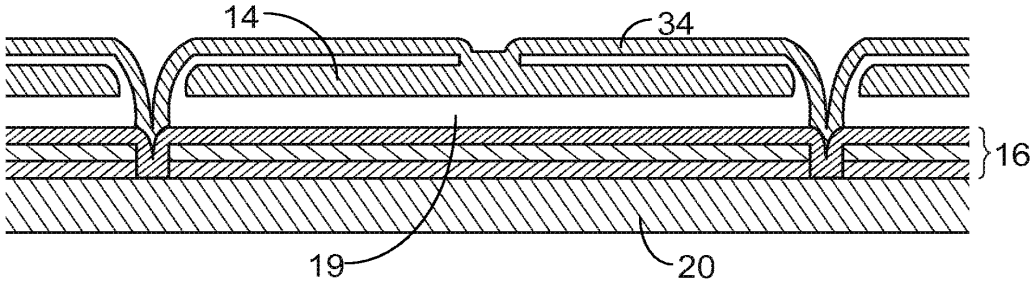


Figure 6C

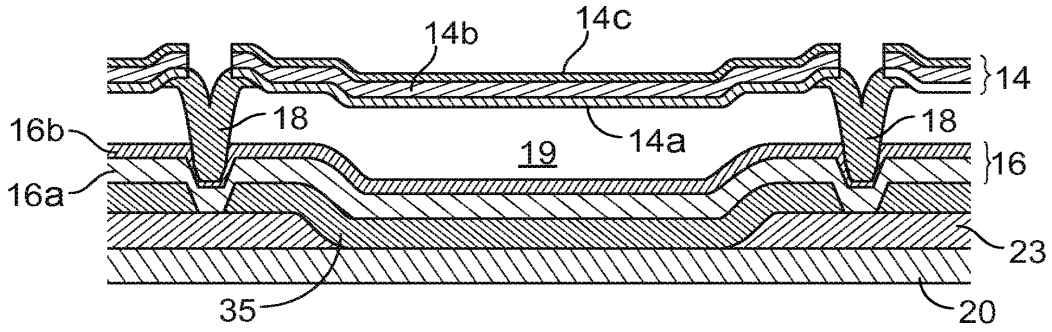


Figure 6D

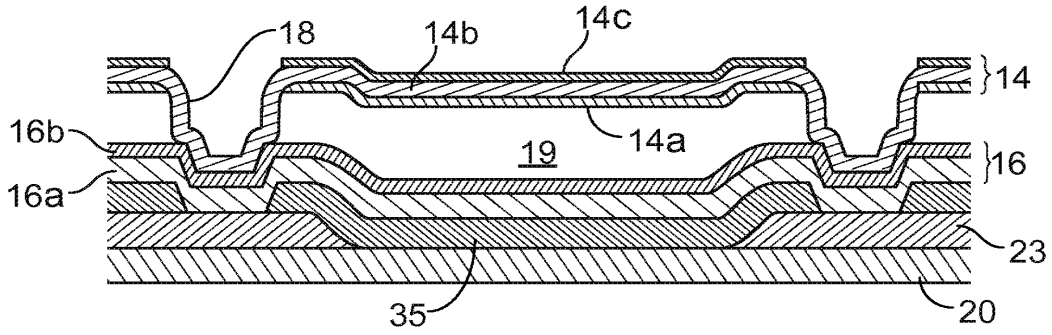


Figure 6E

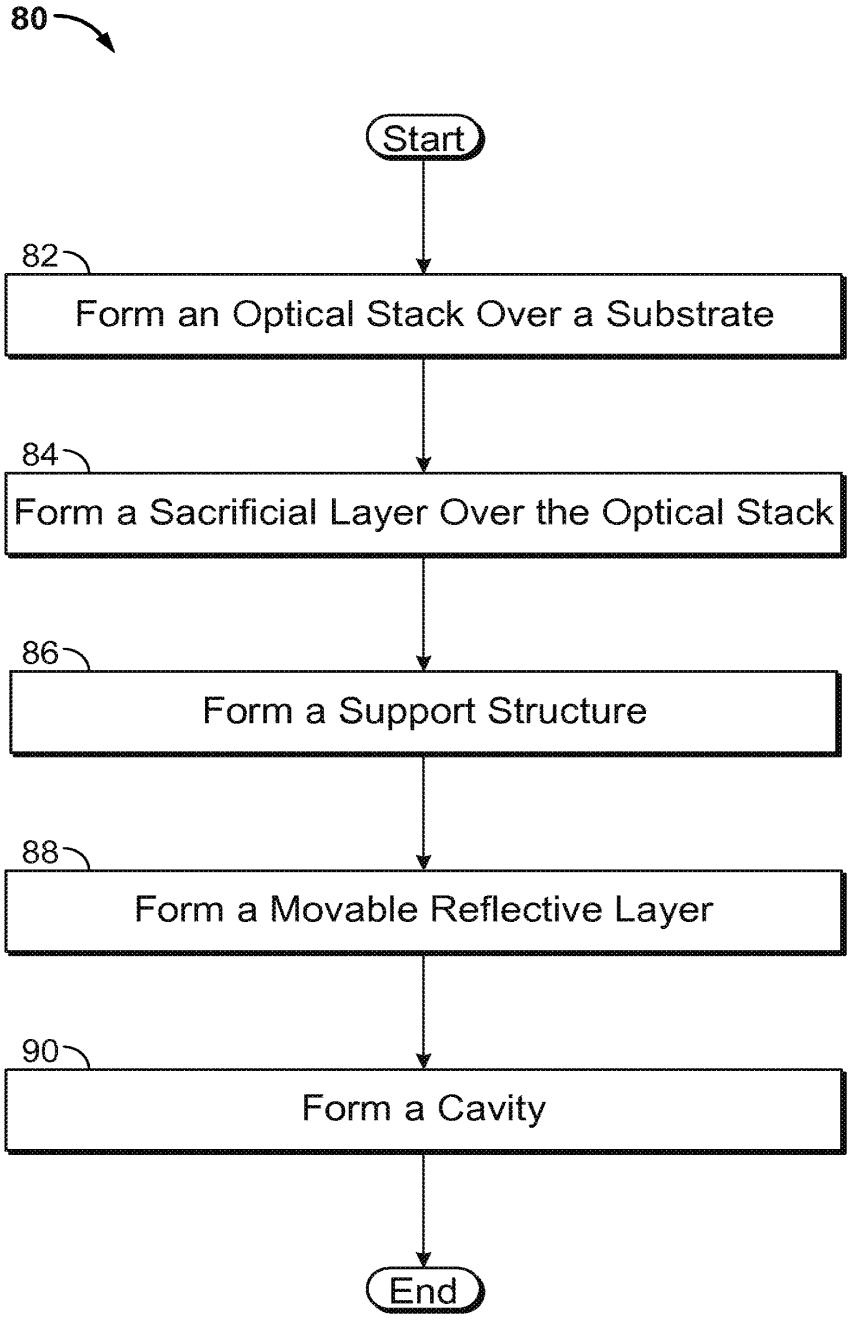

80
Start
82
Form an Optical Stack Over a Substrate
84
Form a Sacrificial Layer Over the Optical Stack
86
Form a Support Structure
88
Form a Movable Reflective Layer
90
Form a Cavity
End

Figure 7

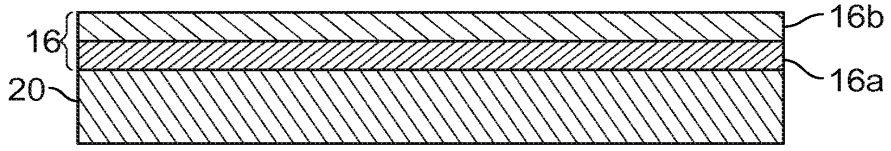


Figure 8A

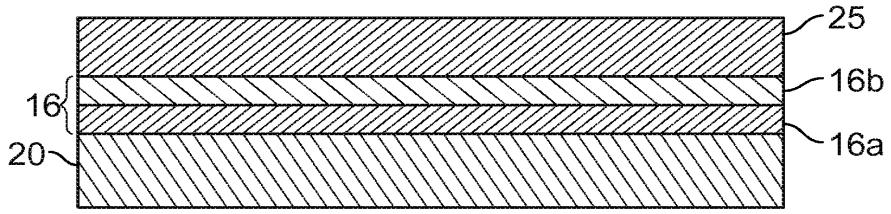


Figure 8B

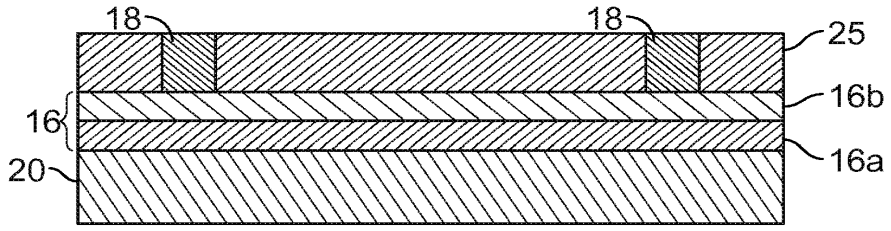


Figure 8C

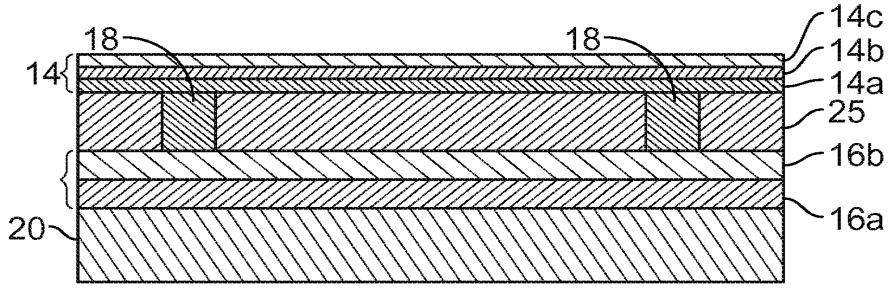


Figure 8D

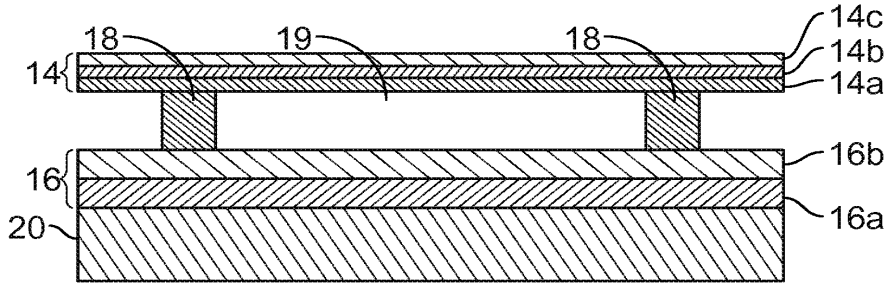


Figure 8E

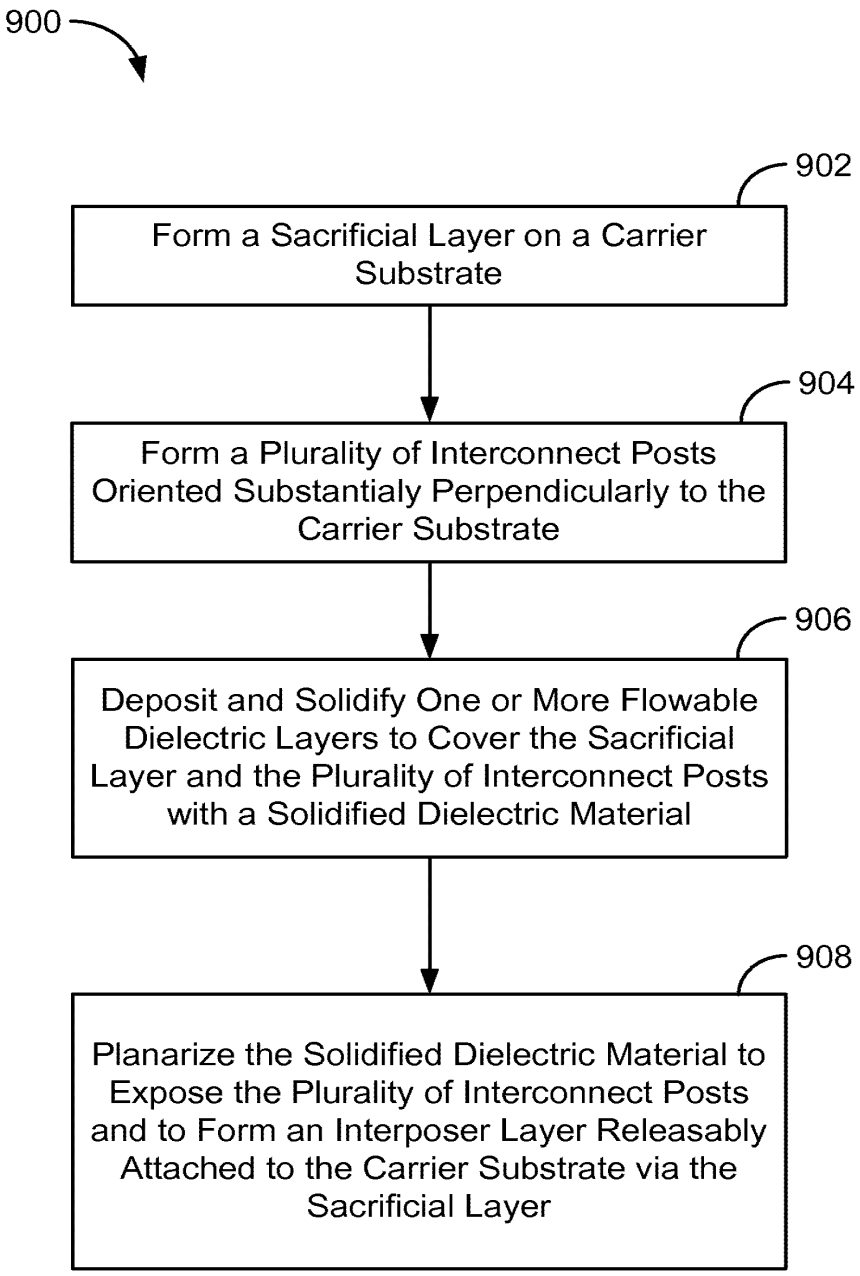

900
902
Form a Sacrificial Layer on a Carrier Substrate
904
Form a Plurality of Interconnect Posts Oriented Substantialy Perpendicularly to the Carrier Substrate
906
Deposit and Solidify One or More Flowable Dielectric Layers to Cover the Sacrificial Layer and the Plurality of Interconnect Posts with a Solidified Dielectric Material
908
Planarize the Solidified Dielectric Material to Expose the Plurality of Interconnect Posts and to Form an Interposer Layer Releasably Attached to the Carrier Substrate via the Sacrificial Layer

Figure 9

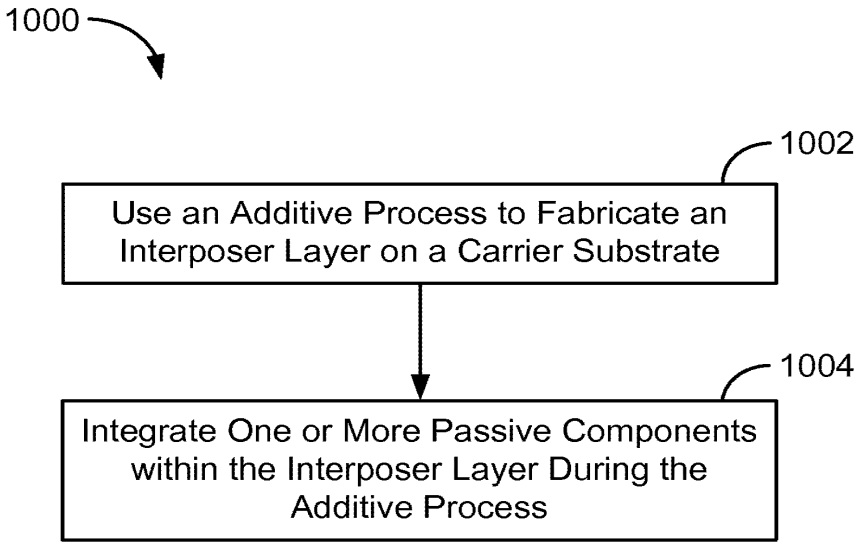

1000
1002
Use an Additive Process to Fabricate an Interposer Layer on a Carrier Substrate
1004
Integrate One or More Passive Components within the Interposer Layer During the Additive Process

Figure 10

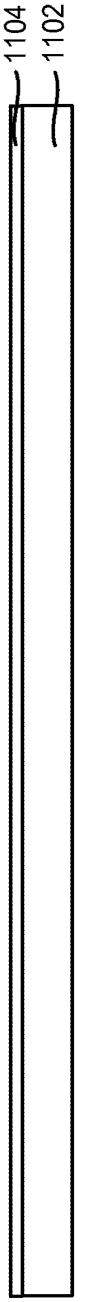


Figure 11A

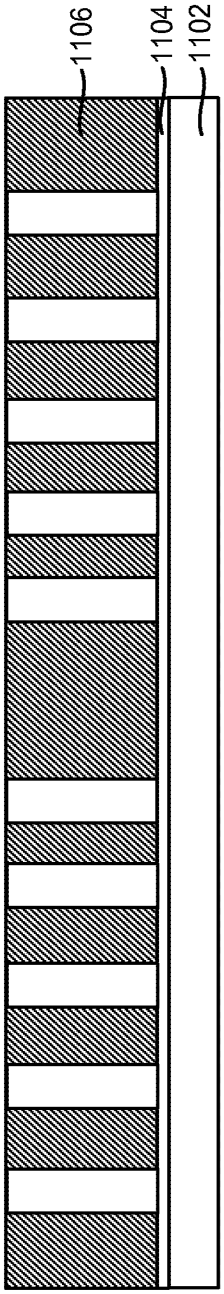


Figure 11B

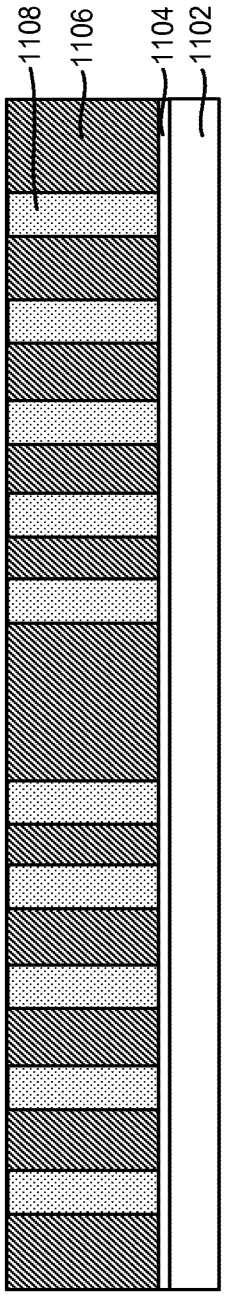


Figure 11C

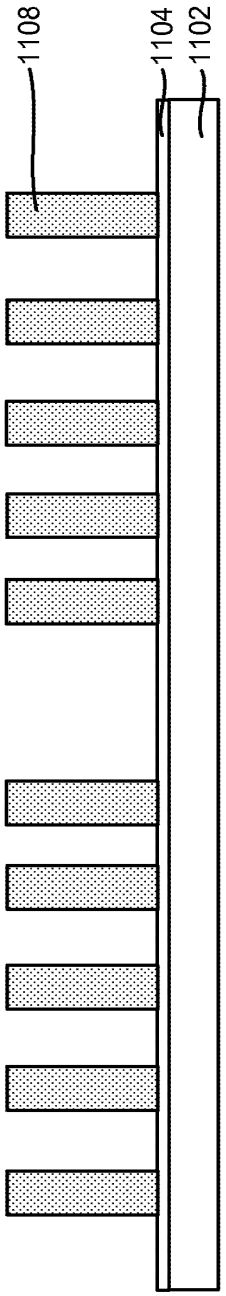


Figure 11D

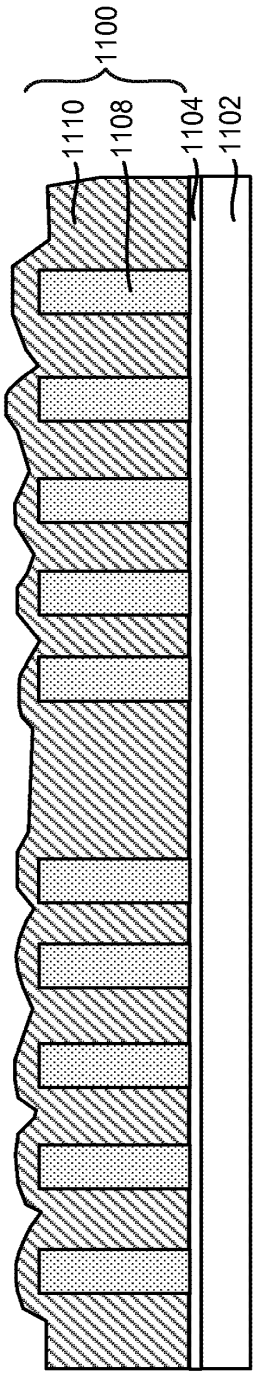


Figure 11E

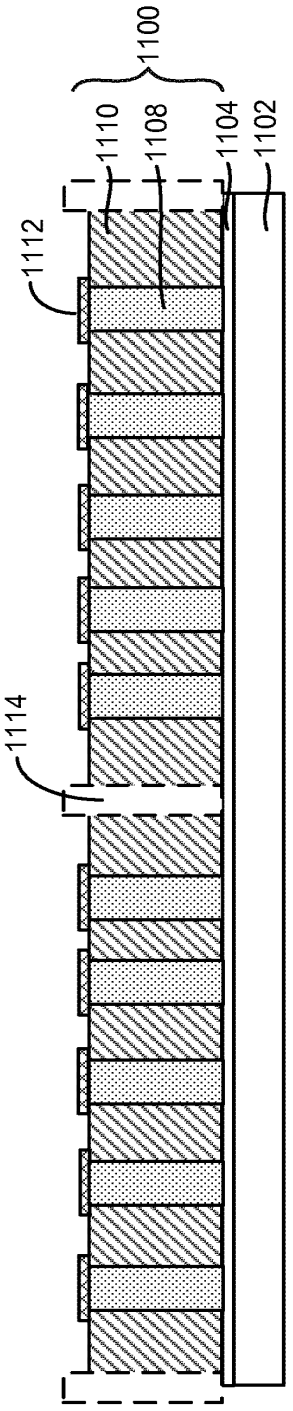


Figure 11F

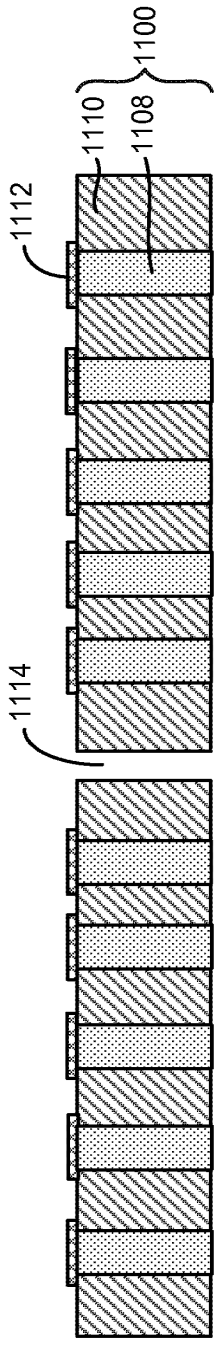


Figure 11G

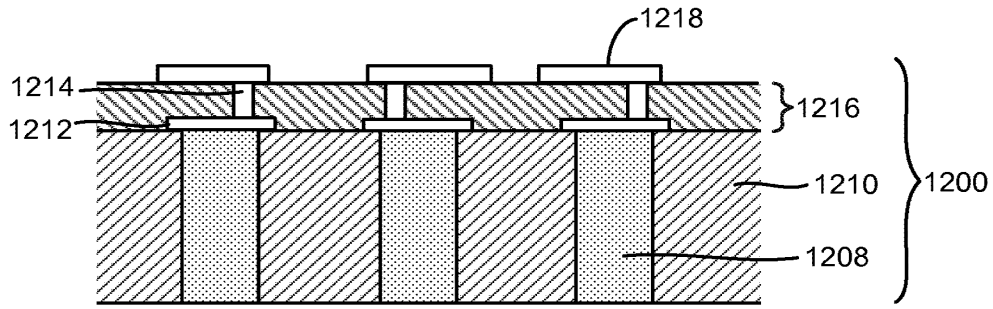


Figure 12A

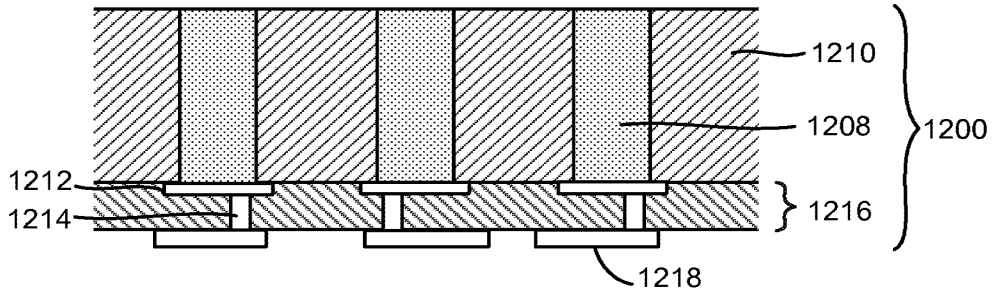


Figure 12B

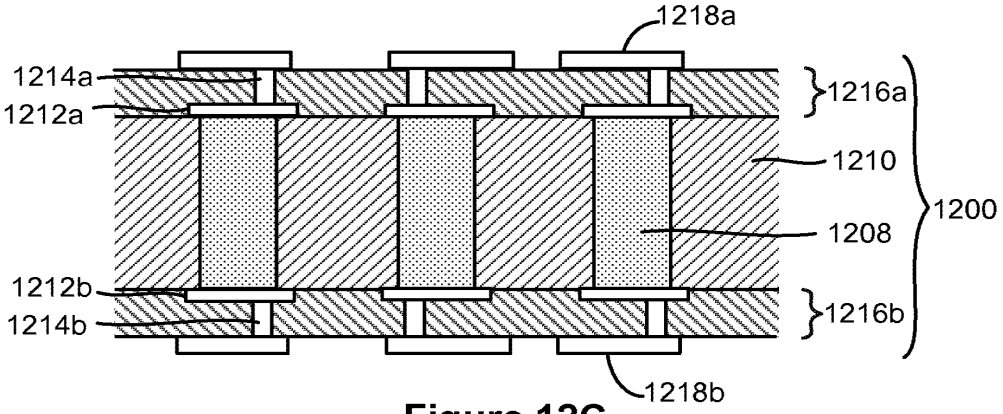


Figure 12C

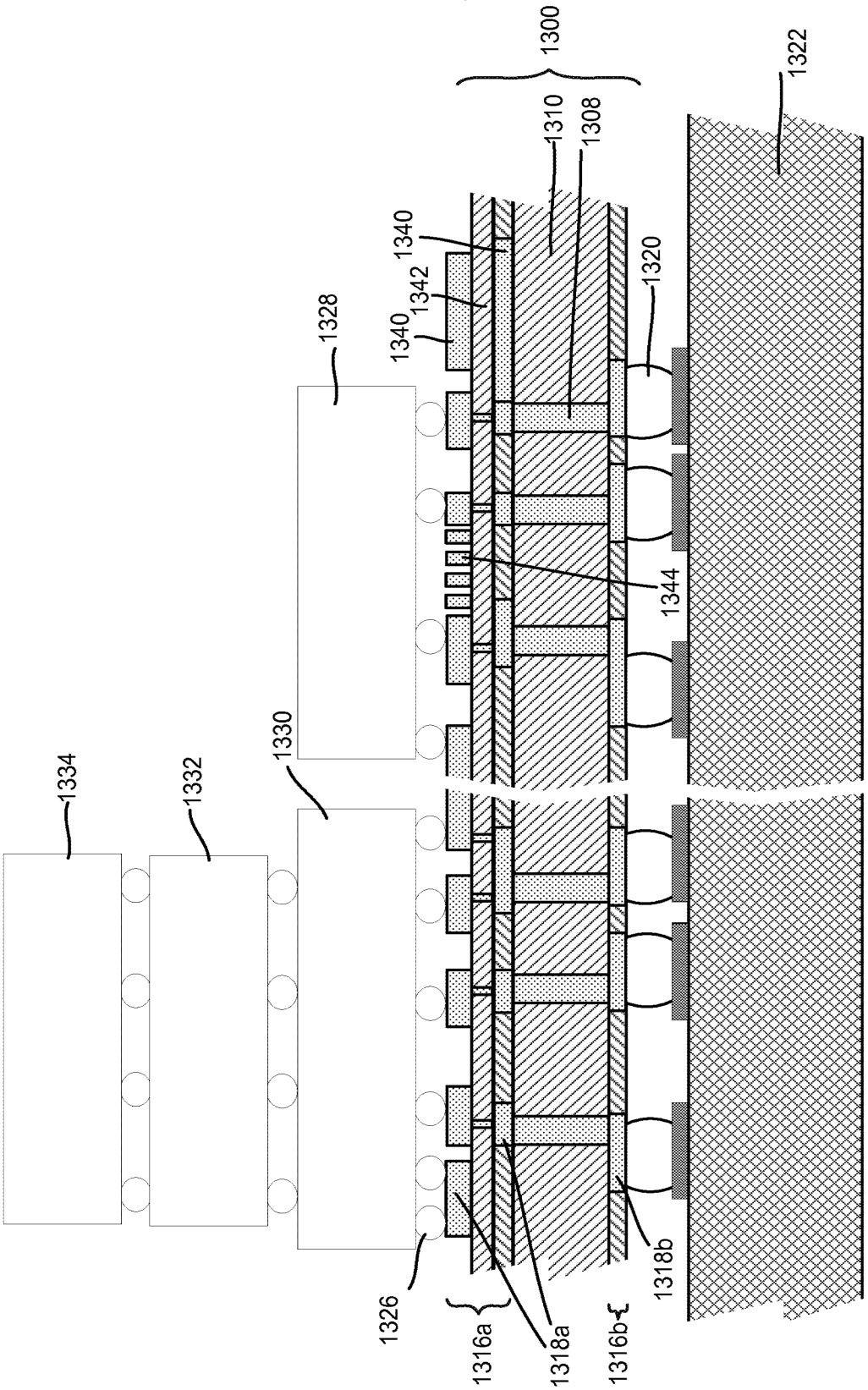

1300
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1316a
1318a
1316b
1318b

Figure 13

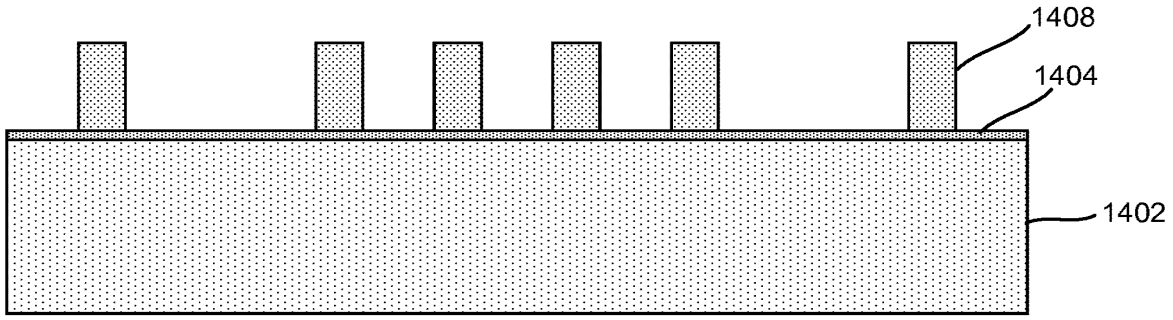


Figure 14A

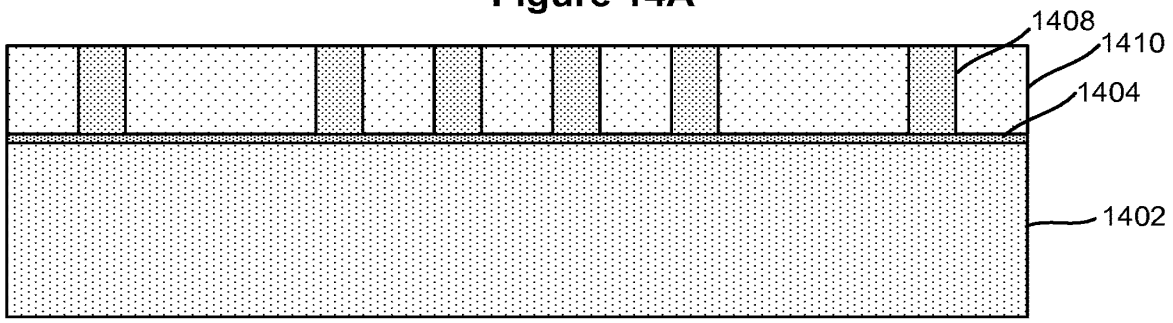


Figure 14B

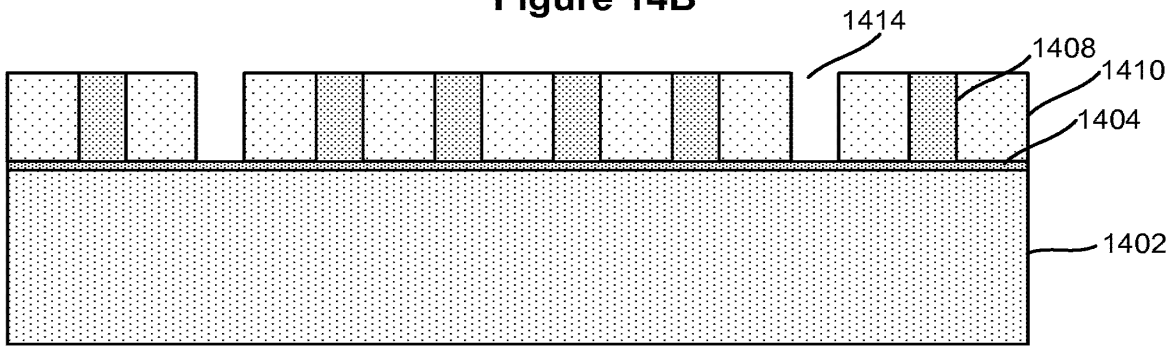


Figure 14C

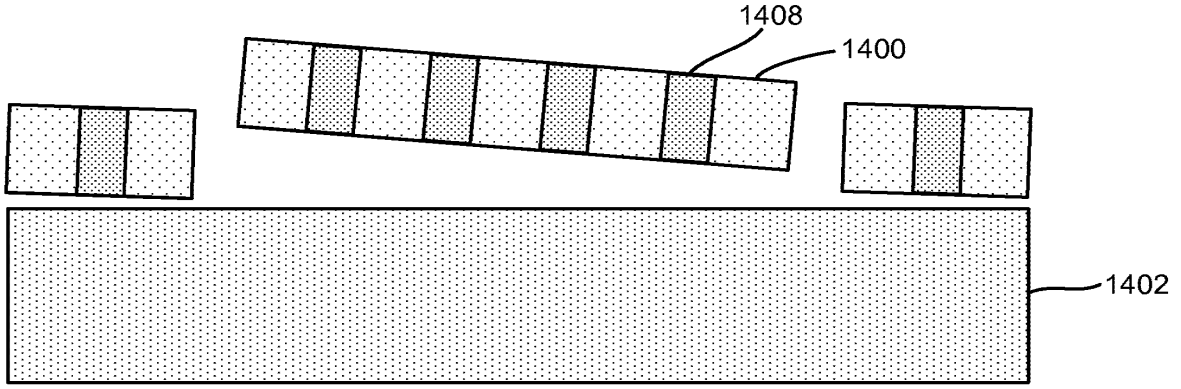


Figure 14D

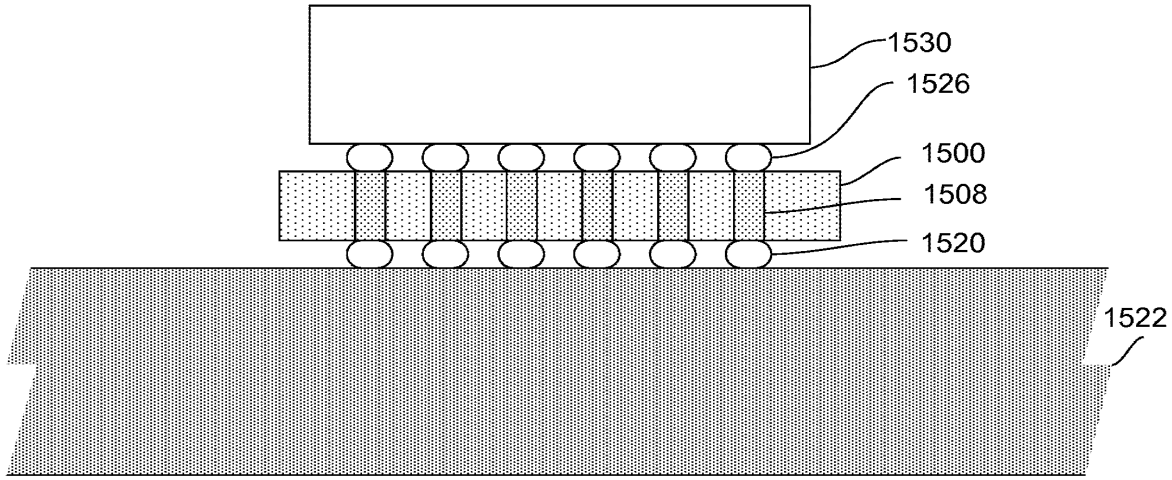


Figure 15A

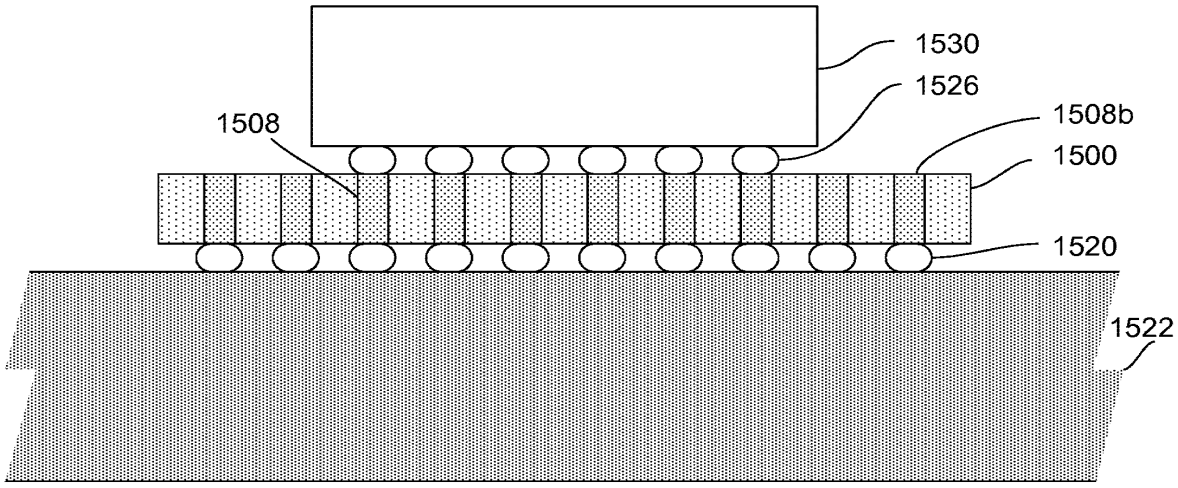


Figure 15B

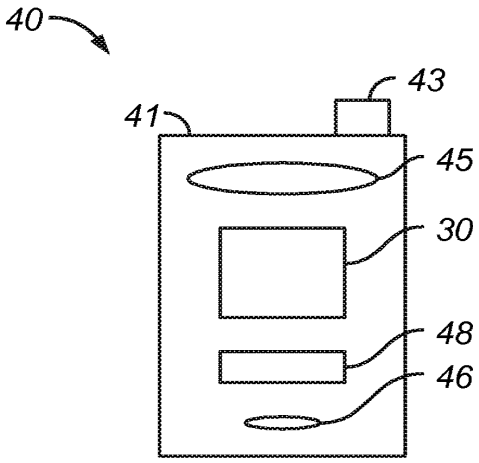


Figure 16A

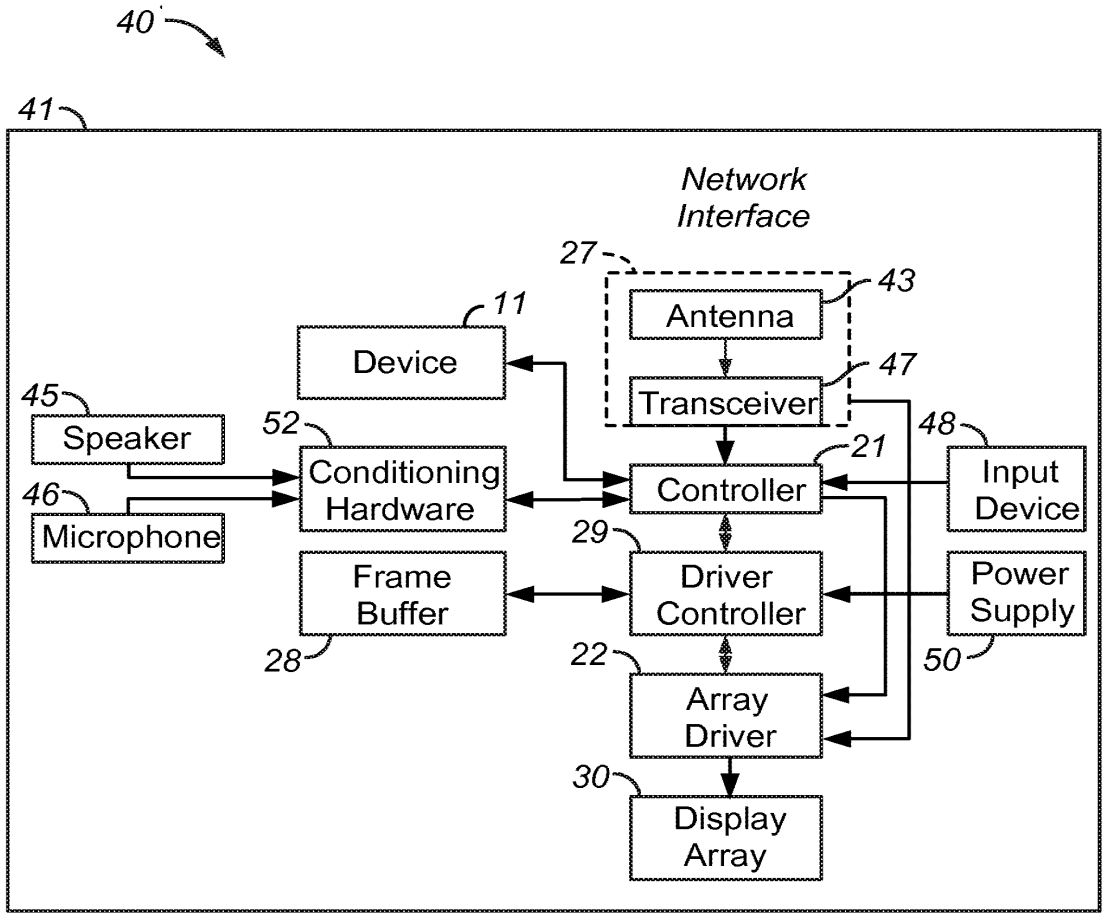


Figure 16B

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2013/030831

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L23/498 H01L21/48
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	JP 2002 368368 A (HITACHI CHEMICAL CO LTD) 20 December 2002 (2002-12-20)	1-9, 11-20, 22,23, 27-33, 35-38
Y	figures 2, 4	4-7,21

Y	EP 1 643 819 A2 (SHINKO ELECTRIC IND CO [JP]) 5 April 2006 (2006-04-05) figures 1E, 1F	4

X	WO 2011/109648 A1 (GEORGIA TECH RES INST [US]; SUNDARAM VENKATESH [US]; LIU FUHAN [US]; T) 9 September 2011 (2011-09-09) figure 18	10,24,34

	-/--	

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
9 August 2013	16/08/2013

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Kästner, Martin

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INTERNATIONAL SEARCH REPORT

International application No
PCT/US2013/030831

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2011/304999 A1 (YU CHEN-HUA [TW] ET AL) 15 December 2011 (2011-12-15)	10
Y	figures 1j, 8	5-7,21

Y	US 5 454 161 A (BEILIN SOLOMON I [US] ET AL) 3 October 1995 (1995-10-03) the whole document	21

A	US 2006/038303 A1 (STERRETT TERRY L [US] ET AL) 23 February 2006 (2006-02-23) the whole document	1-42

2

Form PCT/ISA/210 (continuation of second sheet) (April 2005)

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TSMC EX1032 Page 80

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2013/030831

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
JP 2002368368 A	20-12-2002	JP 5017750 B2	05-09-2012
		JP 2002368368 A	20-12-2002
EP 1643819 A2	05-04-2006	EP 1643819 A2	05-04-2006
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		US 5454161 A	03-10-1995
US 2006038303 A1	23-02-2006	US 2006038303 A1	23-02-2006
		US 2008265391 A1	30-10-2008

Electronic Patent Application Fee Transmittal	
Application Number:	
Filing Date:	
Title of Invention:	METHOD FOR FABRICATING GLASS SUBSTRATE PACKAGE
First Named Inventor/Applicant Name:	Ping-Jung Yang
Filer:	Ping-Jung. Yang
Attorney Docket Number:	Mars16-001-US-C01
Filed as Small Entity	
Filing Fees for Utility under 35 USC 111(a)	

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
UTILITY FILING FEE (ELECTRONIC FILING)	4011	1	75	75
UTILITY SEARCH FEE	2111	1	330	330
UTILITY EXAMINATION FEE	2311	1	380	380
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**785**

Electronic Acknowledgement Receipt	
EFS ID:	38399449
Application Number:	16752650
International Application Number:	
Confirmation Number:	4809
Title of Invention:	METHOD FOR FABRICATING GLASS SUBSTRATE PACKAGE
First Named Inventor/Applicant Name:	Ping-Jung Yang
Customer Number:	102851
Filer:	Ping-Jung. Yang
Filer Authorized By:	
Attorney Docket Number:	Mars16-001-US-C01
Receipt Date:	26-JAN-2020
Filing Date:	
Time Stamp:	02:31:39
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$785
RAM confirmation Number	E20201P337511986
Deposit Account	
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
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6	Foreign Reference	WO2013138452.pdf	3880918 9f62132f9733d2fabeccec10fe48aa8b9e86213f	no	69
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Mars 16-001-US-C01

METHOD FOR FABRICATING GLASS SUBSTRATE PACKAGE

[0001] This patent application is a continuation of application No. 15261956, filed Sept. 11, 2016, now pending, which claims priority benefits from U.S. provisional patent application No. 62/219249, filed Sept. 16, 2015. This patent application of application No. 15261956 is a continuation-in-part of application No. 14/036256, filed Sept. 25, 2013, now patent No. 9615453, which claims the benefit of priority from U.S. provisional patent application No. 61/705,649, filed Sept. 26, 2012, all of which is incorporated herein by reference in their entirety.

BACKGROUND OF THE DISCLOSURE

Field of the Disclosure

[0002]The patent disclosure a method and structure to manufacture a glass substrate, and disclosed embodiments relate to one or more chip building a system on the glass substrate.

Brief Description of the Related Art

[0003] As is well known, microelectronic devices have a tendency to be minimized and thinned with its functional development and a semiconductor package mounted on a mother board is also following the tendency in order to realize a mounting of high integration.

[0004] When the geometric dimensions of the Integrated Circuits are scaled down, the cost per

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die is decreased while some aspects of performance are improved. The metal connections which connect the Integrated Circuit to other circuit or system components become of relative more importance and have, with the further miniaturization of the IC, an increasingly negative impact on the circuit performance. The parasitic capacitance and resistance of the metal interconnections increase, which degrades the chip performance significantly. Of most concern in this respect is the voltage drop along the power and ground buses and the RC delay of the critical signal paths. Attempts to reduce the resistance by using wider metal lines result in higher capacitance of these wires.

[0005] To solve this problem, the approach has been taken to develop low resistance metal (such as copper) for the wires while low dielectric materials are used in between signal lines.

[0006] Increased Input-Output (IO) combined with increased demands for high performance IC's has led to the development of Flip Chip Packages. Flip-chip technology fabricates bumps (typically Pb/Sn solders) on Al pads on chip and interconnect the bumps directly to the package media, which are usually ceramic or plastic based. The flip-chip is bonded face down to the package medium through the shortest path. These technologies can be applied not only to single-chip packaging, but also to higher or integrated levels of packaging in which the packages are larger and to more sophisticated substrates that accommodate several chips to form larger functional units.

[0007] The flip-chip technique, using an area array, has the advantage of achieving the highest density of interconnection to the device and a very low inductance interconnection to the package. However, pre-testability, post-bonding visual inspection, and TCE (Temperature Coefficient of Expansion) matching to avoid solder bump fatigue are still challenges.

[0008] Glass can be used as an interposer to bridge between one or more IC chips and a printed circuit board. In many respects, when used as an interposer / substrate and without the requirement

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for active devices, glass can be a good substitute for a silicon interposer. The advantages of glass in comparison to silicon as an interposer lie in its much lower material cost. Glass also has a CTE closely matched to silicon, so that reliability of interconnects, especially micro-bonds, can be expected to be quite good. Glass has some disadvantages in comparison to silicon – notably its lower thermal conductivity and the difficulty in forming Through Glass Vias (TGV's). Both of these topics are discussed elsewhere in this patent.

SUMMARY OF THE DISCLOSURE

[0009] Embodiments of the present disclosure provide A display device comprises a display panel substrate and a glass substrate over said display panel substrate, wherein said display panel substrate comprises multiple contact pads, a display area, a first boundary, a second boundary, a third boundary and a fourth boundary, wherein said display area comprises a first edge, a second edge, a third edge and a fourth edge, wherein said first boundary is parallel to said third boundary and said first and third edges, wherein said second boundary is parallel to said fourth boundary and said second and fourth edges, wherein a first least distance between said first boundary and said first edge, wherein a second least distance between said second boundary and said second edge, a third least distance between said third boundary and said third edge, a fourth distance between said fourth boundary and said fourth edge, and wherein said first, second, third and fourth least distances are smaller than 100 micrometers, and wherein said glass substrate comprising multiple metal conductors through in said glass substrate and multiple metal bumps are between said glass substrate and said display panel substrate, wherein said one of said metal conductors is connected to one of said contact pads through one of said metal bumps.

[0010] These, as well as other components, steps, features, benefits, and advantages of the present disclosure, will now become clear from a review of the following detailed description of

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illustrative embodiments, the accompanying drawings, and the claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] The drawings disclose illustrative embodiments. They do not set forth all embodiments. Other embodiments may be used in addition or instead. Details that may be apparent or unnecessary may be omitted to save space or for more effective illustration. Conversely, some embodiments may be practiced without all of the details that are disclosed. When the same numeral appears in different drawings, it refers to the same or like components or steps.

[0012] Aspects of the disclosure may be more fully understood from the following description when read together with the accompanying drawings, which are to be regarded as illustrative in nature, and not as limiting. The drawings are not necessarily to scale, emphasis instead being placed on the principles of the disclosure.

[0013] Figs. 1 illustrates a three-dimensional view of a X-axis nets and a Y-axis nets, in accordance with the present disclosure.

[0014] Fig. 2 illustrates a cross-section view of the X-axis nets and the Y-axis nets, in accordance with the present disclosure.

[0015] Fig. 3 illustrates a cross-section view of the Z-axis traces crossed to the X-axis nets and the Y-axis nets, in accordance with the present disclosure.

[0016] Fig. 4 illustrates a three-dimensional view of the Z-axis traces, X-axis nets and the Y-axis nets, in accordance with the present disclosure.

[0017] Fig. 5a-5i illustrate the shape and structure of the Z-axis traces, in accordance with the present disclosure.

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[0018] Figs. 6a-6j are illustrate a 1st process of forming a glass substrate, in accordance with the present disclosure.

[0019] Figs. 6k-6n illustrate a top views of the 1st process of forming the glass substrate, in accordance with the present disclosure.

[0020] Figs. 7a-7o are illustrate a 2nd process of forming the glass substrate, in accordance with the present disclosure.

[0021] Figs. 7p-7r illustrate a top views of the 2nd process of forming the glass substrate, in accordance with the present disclosure.

[0022] Figs. 8a-8d illustrate cross-section views of the glass substrate and the metal plug, in accordance with the present disclosure.

[0023] Figs. 9a-9s illustrate a process to form multiple traces on a top surface and a bottom surface of the glass substrate, in accordance with the present disclosure.

[0024] Figs. 9t-9u illustrate cross-section views of multiple chips formed on the glass substrate, in accordance with the present disclosure.

[0025] Fig. 9v illustrates a cross-section view of the metal bump, in accordance with the present disclosure.

[0026] Fig. 9w illustrates a cross-section view of multiple chips formed on a top surface and bottom surface of the glass substrate, in accordance with the present disclosure.

[0027] Fig. 9x illustrates a cross-section view of multiple chips and a 3D-IC package formed on a top surface and bottom surface of the glass substrate, in accordance with the present disclosure.

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[0028] Fig. 9y illustrates a top views of the multiple chips on the glass substrate, in accordance with the present disclosure.

[0029] Figs. 10a-10j illustrates a damascene process to form the metal layer on the glass substrate, in accordance with the present disclosure.

[0030] Figs. 11a-11i illustrates an embossing process to form the metal layer on the glass substrate, in accordance with the present disclosure.

[0031] Fig. 12 illustrates a cross-section view of the glass substrate of the first application formed on an OLED display substrate, in accordance with the present disclosure.

[0032] Fig. 13 illustrates a cross-section view of the glass substrate of the second application formed on a MEMs display substrate, in accordance with the present disclosure.

[0033] Fig. 14 illustrates a cross-section view of the glass substrate of the third application formed on a LCD display substrate, in accordance with the present disclosure.

[0034] Fig. 15 illustrates a cross-section view of the glass substrate of the fourth application formed on an another LCD display substrate, in accordance with the present disclosure.

[0035] Fig. 16 illustrates a cross-section view of the glass substrate of the fifth application formed on an OLED display substrate, in accordance with the present disclosure.

[0036] Fig. 17a illustrates a cross-section view of the glass substrate of the sixth application formed on an OLED display substrate, in accordance with the present disclosure.

[0037] Fig. 17b illustrates a cross-section view of the structure of the OLED display substrate, in accordance with the present disclosure.

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[0038] Fig. 18 illustrates a three-dimensional view of the display device, in accordance with the present disclosure.

[0039] Fig. 19 illustrates a big display device combined from multiple display device, in accordance with the present disclosure.

[0040] While certain embodiments are depicted in the drawings, one skilled in the art will appreciate that the embodiments depicted are illustrative and that variations of those shown, as well as other embodiments described herein, may be envisioned and practiced within the scope of the present disclosure.

DETAILED DESCRIPTION OF THE DISCLOSURE

[0041] Fig. 1 illustrates a three-dimensional view of a net 2, 4, wherein the net 4 is under the net 2, wherein the net 2 comprises multiple Y-axis traces 2a and multiple X-axis traces 2b under the Y-axis traces 2a, and wherein the net 4 comprises multiple Y-axis traces 4a and multiple X-axis traces 4b under the Y-axis traces 4a. Multiple gaps 3, 5 form in the net 2 and 4. Each of the traces 2a, 2b, 4a and 4b is easily move to change the size of gaps 3 and gaps 5. The diameter (or width) of traces 2a, 2b, 4a and 4b are the same, such as between 10 and 30 micrometers, between 20 and 100 micrometers, between 40 and 150 micrometers, between 50 and 200 micrometers, between 200 and 1000 micrometers or between 500 and 10000 micrometers. The traces 2a, 2b, 4a and 4b may be metal traces or polymer traces, such as copper traces, copper-gold alloy traces, copper-gold-palladium alloy traces, copper-gold-silver alloy traces, copper-platinum alloy traces, copper-iron alloy traces, copper-nickel alloy traces, copper-tungsten traces, tungsten traces, brass wires, zinc plated brass wires, stainless wires, nickel plated stainless wires, phosphor bronze wires, copper plated the aluminum wires, aluminum traces, phenolic resin traces, epoxy resin traces, melamine-

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formaldehyde resin traces or polysiloxanes resin traces. The cross-section shape of traces 2a, 2b, 4a and 4b may be a circular shape, a Square shape, an oblong shape, a rectangle shape or a flat shape.

[0042] Fig. 2 illustrates a cross-section view of the net 2 and the net 4. The gaps 3 and gaps 5 are aligned with each other.

[0043] Next, referring to Fig. 3, multiple metal traces 6 are crossed the net 2 and the net 4 through the gaps 3 and gaps 5. The diameter (or width) of metal traces 6 is between 10 and 30 micrometers, between 20 and 100 micrometers, between 40 and 150 micrometers, between 50 and 200 micrometers, between 200 and 1000 micrometers or between 500 and 10000 micrometers. The traces 6 may be metal traces, such as copper traces, copper-gold alloy traces, copper-gold-palladium alloy traces, copper-gold-silver alloy traces, copper-platinum alloy traces, copper-iron alloy traces, copper-nickel alloy traces, copper-tungsten traces, tungsten traces, brass wires, zinc plated brass wires, stainless wires, nickel plated stainless wires, phosphor bronze wires, copper plated the aluminum wires, aluminum traces, titanium-containing layer plated the copper wires, tantalum-containing layer plated the copper wires. The cross-section shape of traces 6 may be a circular shape, a square shape, an oblong shape, a rectangle shape or a flat shape. The diameter (or width) of traces 6 may be the same with the traces 2a, 2b, 4a and 4b or different with the traces 2a, 2b, 4a and 4b.

[0044] Furthermore, we proposed the material of the traces 6 is copper-tungsten alloy, wherein the copper in the copper-tungsten alloy is 50 percent and the tungsten in the copper-tungsten alloy is 50 percent, the copper in the copper-tungsten alloy is 60 percent and the tungsten in the copper-tungsten alloy is 40 percent, the copper in the copper-tungsten alloy is 70 percent and the tungsten in the copper-tungsten alloy is 30 percent, the copper in the copper-tungsten alloy is 80 percent and the tungsten in the copper-tungsten alloy is 20 percent, the copper in the copper-tungsten alloy is 90 percent and the tungsten in the copper-tungsten alloy is 10 percent, the copper in the copper-

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tungsten alloy is 40 percent and the tungsten in the copper-tungsten alloy is 60 percent, the copper in the copper-tungsten alloy is 30 percent and the tungsten in the copper-tungsten alloy is 70 percent.

[0045] Fig. 4 illustrates a three-dimensional view of a net 2, 4 and traces 6.

[0046] Fig. 5a-5i illustrates the shape and structure of the traces 6. In Fig. 5a, the cross-section shape of traces 6 is a circular shape. In Fig. 5d, the cross-section shape of traces 6 is a square shape. In Fig. 5g, the cross-section shape of traces 6 is a rectangle shape. In Fig. 5b, the cross-section shape of traces 6 is a circular shape and a first covering layer 6a is cover on the traces 6, wherein the first covering layer 6a may be a metal layer, such as a nickel-containing layer, a zinc-containing layer, a titanium-containing layer, a tantalum-containing layer, a silver-containing layer, a chromium-containing layer and wherein the first covering layer 6a may be an anti-oxidation layer, such as an oxide-containing layer. In Fig. 5e, the cross-section shape of traces 6 is a square shape and a first covering layer 6a is cover on the traces 6, wherein the first covering layer 6a may be a metal layer, such as a nickel-containing layer, a zinc-containing layer, a titanium-containing layer, a tantalum-containing layer, a silver-containing layer, a chromium-containing layer and wherein the first covering layer 6a may be an anti-oxidation layer, such as an oxide-containing layer. In Fig. 5h, the cross-section shape of traces 6 is a rectangle shape and a first covering layer 6a is cover on the traces 6, wherein the first covering layer 6a may be a metal layer, such as a nickel-containing layer, a zinc-containing layer, a titanium-containing layer, a tantalum-containing layer, a silver-containing layer, a chromium-containing layer and wherein the first covering layer 6a may be an anti-oxidation layer, such as an oxide-containing layer. In Fig. 5c, the cross-section shape of traces 6 is a circular shape and a second covering layer 6b is cover on the first covering layer 6a, wherein the second covering layer 6b may be an adhesion layer, such as a nickel-containing layer, a zinc-containing layer, a titanium-containing layer, a tantalum-containing layer, a silver-containing layer, a chromium-containing layer and wherein the first covering layer 6a may be an anti-oxidation layer, such as an

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oxide-containing layer. In Fig. 5f, the cross-section shape of traces 6 is a square shape and a second covering layer 6b is cover on the first covering layer 6a, wherein the second covering layer 6b may be an adhesion layer, such as a nickel-containing layer, a zinc-containing layer, a titanium-containing layer, a tantalum-containing layer, a silver-containing layer, a chromium-containing layer and wherein the first covering layer 6a may be an anti-oxidation layer, such as an oxide-containing layer. In Fig. 5i, the cross-section shape of traces 6 is an oblong shape and a second covering layer 6b is cover on the first covering layer 6a, wherein the second covering layer 6b may be an adhesion layer, such as a nickel-containing layer, a zinc-containing layer, a titanium-containing layer, a tantalum-containing layer, a silver-containing layer, a chromium-containing layer and wherein the first covering layer 6a may be an anti-oxidation layer, such as an oxide-containing layer.

[0047] Next, Figs. 6a-6j are illustrated a 1st process of forming a glass substrate of the invention. Please referring to Fig. 6a, the traces 6 are stretched to a suitable length L1, e.g., smaller than 5 meters, such as between 0.5 and 1 meter, or between 1 and 3 meters. In the same time, the net 4 is moved down to a suitable location. The pitch t1 between the traces 2a, 2b, 4a, 4b is greater than the diameter (or width) of traces 6.

[0048] Next, referring to Fig. 6b, the traces 2a, 2b, 4a and 4b are moved to change the pitch t1 to a pitch t2, then the traces 6 are closed up to a pitch t3. The pitch t3 substantially the same with the diameter (or width) of the traces 2a, 2b, 4a and 4b, such as between 5 and 20 micrometers, between 20 and 50 micrometers, between 30 and 80 micrometers, between 20 and 100 micrometers, between 40 and 150 micrometers, between 50 and 200 micrometers, between 200 and 1000 micrometers or between 500 and 10000 micrometers. In the same time, may be apply a force to stretch the traces 6, 2a, 2b, 4a and 4b and make the traces 6 keep strength and keep the pitch t3 fixed.

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[0049] Next, referring to Fig. 6c, a thermal resistance layer 8 is formed on surfaces of the net 4. The thermal resistance layer 8 may be a polymer layer, such as a thermosetting resin, phenolic resin, epoxy resin, melamine-formaldehyde resin, polysiloxanes resin, plaster layer, wherein the thermal resistance layer 8 has a heat deflection temperature between 400 and 900 ℃. When a liquid thermal resistance layer 8 formed on the net 4 and the thermal resistance layer 8 permeated the net 4 through the gaps 5, wherein the thermal resistance layer 8 cover the gaps 5 between traces 4a, traces 4b and traces 6, then curing the thermal resistance layer 8. The thermal resistance layer 8 has a thickness between 0.05 and 1 meter.

[0050] 此Next, referring to Fig. 6d, a mold 10 is provided between the net 2 and the net 4, wherein the mold 10 surrounds the traces 6 and on the thermal resistance layer 8. The mold 10 is hold up by a machine or a device. The mold 10 may be a metal mold, a ceramics mold or a polymer mold, which has a heat deflection temperature between 400 ℃ and 900 ℃ or between 800 ℃ and 1300 ℃.

[0051] Next, referring to Fig. 6e, a fixed layer 12 is formed on the thermal resistance layer 8, wherein the fixed layer 12 may be a glass layer or a polymer layer. When the material of the fixed layer 12 is glass, the fixed layer 12 is a high temperature liquid to form on the thermal resistance layer 8, and then the fixed layer 12 down to a suitable temperature becomes a solid state. The fixed layer 12 has a thickness between 0.01 and 1 meter. The bottom of traces 6 are fixed by the fixed layer 12.

[0052] Next, referring to Fig. 6f, the traces 6 under the net 4 are cut. A tank 14 carries the mold 10, net 4 and the fixed layer 12.

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[0053] Next, referring to Fig. 6g, a glass layer (liquid form) 16 is formed on the fixed layer 12. The glass layer 16 is a high temperature liquid to form on the fixed layer 12 and fill in the mold 10, and then the glass layer 16 down to a suitable temperature becomes a solid state, wherein the glass layer 16 has a glass transition temperature between 300°C and 900°C, between 500°C and 800°C, between 900°C and 1200°C or between 1000°C and 1800°C. The glass layer 16 is a low melting point glass material, wherein the glass layer 16 has a melting point between 300°C and 900°C, 800°C and 1300°C, between 900°C and 1600°C, between 1000°C and 1850°C, or between 1000°C and 2000°C, wherein the melting point may smaller than 1500°C. The glass layer 16 has a thickness greater than 0.5 meters or greater than 0.1 meter. Furthermore, there is a few bubbles or no bubble in glass layer 16, for example, there is zero to 3 bubbles in one cubic meter of the glass layer 16, 1 to 10 bubbles in one cubic meter of the glass layer 16, 5 to 30 bubbles in one cubic meter of the glass layer 16 or 20 to 60 bubbles in one cubic meter of the glass layer 16, wherein the bubble has a diameter between 0.0001 and 0.001 centimeters, between 0.001 and 0.05 centimeters, between 0.05 and 0.1 centimeters or between 0.05 and 0.5 centimeters. The glass layer 16 may be remove bubbles through multiple laminating process, squeezing process and heating process.

[0054] The glass layer 16 refers to an amorphous solid. The material of the glass layer 16 may be included soda-lime glass, boro-silicate glass, alumo-silicate glass, fluoride glasses, phosphate glasses or chalcogen glasses. For example, the composition of the soda-lime glass comprises SiO_2 (74%), Na_2O (13%), CaO (10.5%), Al_2O_3 (1.3%), K_2O (0.3%), SO3 (0.2%), MgO (0.2%), Fe2O3 (0.04%), TiO2 (0.01%), the composition of the boro-silicate glass comprises SiO_2 (81%), B_2O_3 (12%), Na_2O (4.5%), Al_2O_3 (2.0%), the composition of the phosphate glasses comprises a percentage of the P_2O_5 material between 3% and 10% or between 5% and 20%.

[0055] A glass, once formed into a solid body, is capable of being softened and perhaps remitted into a liquid form. The "glass transition temperature" of a glass material is a temperature below

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which the physical properties of the glass are similar to those of a solid and above which the glass material behaves like a liquid.

[0056] If a glass is sufficiently below the glass transition temperature, molecules of the glass may have little relative mobility. As a glass approaches the glass transition temperature, the glass may begin to soften and with increasing temperature the glass will ultimately melt into the liquid state. Thus, a glass body may be softened to an extent sufficient to enable manipulation of the body's shape, allowing for the formation of holes or other features in the glass body. Once the desired form is obtained, glass is usually annealed for the removal of stresses. Surface treatments, coatings or lamination may follow to improve the chemical durability (glass container coatings, glass container internal treatment), strength (toughened glass, bulletproof glass, windshields), or optical properties (insulated glazing, anti-reflective coating).

[0057] Furthermore, the glass layer 16 may be replaced by a polymer layer. When the polymer cured to a solid state. The polymer layer has an expansion coefficient between 3 and 10 ppm/°C.

[0058] Next, referring to Fig. 6h, the mold 10 and the tank 14 are removed and cut the traces 6 from net 2.

[0059] Next, referring to Fig. 6i, the net 4 and the thermal resistance layer 8 are removed, and then a column 25 is produced.

[0060] Next, referring to Fig. 6j, the traces 6 out of the column 25 are removed and cutting the column 25 to produce multiple first substrates 20, wherein the first substrate 20 has a thickness between 20 and 100 micrometers, between 50 and 150 micrometers, between 100 and 300 micrometers or between 150 and 2000 micrometers or greater than 1000 micrometers. The first

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substrates 20 may be make a planarization process using a suitable process, such as a chemical mechanical polishing (CMP) procedure, mechanical grinding, or laser drilling

[0061] Next, referring to Fig. 6k, the first substrate 20 comprises multiple second substrates 22. The second substrates 22 are well-regulated an array in the first substrate 20. Each of the second substrates22 has multiple metal plugs 21, wherein the metal plug 21 is formed from metal traces 6. The metal plug 21 has the same material and structure with metal trace 6.

[0062] Next, referring to Fig. 6l-6n, the metal plugs 21 may be arranged different types, such as Fig. 6l, the metal plugs 21 are arranged on the side portions of the second substrate 22, or such as Fig. 6m, the metal plugs 21 are arranged on the side portions and center portion of the second substrate 22, or such as Fig. 6n, some portions of the second substrate 22 are not arranged the metal plugs 21.

[0063] Fig. 7a-7m are illustrated a 2nd process of forming a glass substrate of the invention. Please referring to Fig. 7a-7b, there is illustrated a first metal plate 7 in Fig. 7a, illustrated a three-dimensional view of the first metal plate 7 in Fig. 7b. The first metal plate 7 has a thickness between 25 micrometers and 1000 micrometers, between 20 micrometers and 500 micrometers, between 30 micrometers and 400 micrometers or between 20 micrometers and 250 micrometers. The first metal plate 7 comprising a first portion 71, a second portion 73 and a third portion 75 between the first portion 71 and second portion 73, wherein the third portion 75 comprises multiple non-circular metal traces 752 are connected to the first portion 71 and the second portion 73, wherein a cross-section view of the non-circular trace 752 comprising a square shape or a rectangle shape. One of the non-circular trace 752 has a width greater than the thickness of one of the non-circular trace 752 , such as between 150 micrometers and 3000 micrometers, between 300 micrometers and 1500 micrometers, between 200 micrometers and 800 micrometers or between 100 micrometers and 500

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micrometers. Multiple gaps 754 are between each two non-circular traces 752, wherein the gap 754 is between 50 micrometers and 3000 micrometers, between 300 micrometers and 1500 micrometers, between 200 micrometers and 800 micrometers or between 150 micrometers and 500 micrometers. The first metal plate 7 comprises a copper metal layer, copper-gold alloy metal layer, copper-gold-palladium alloy metal layer, copper-gold-silver alloy metal layer, copper-platinum alloy metal layer, copper-iron alloy metal layer, copper-nickel alloy metal layer, copper-tungsten metal layer, tungsten metal layer, brass metal layer, zinc plated brass metal layer, stainless metal layer, nickel plated stainless metal layer, phosphor bronze metal layer, copper plated the aluminum metal layer or aluminum metal layer. There are two holes 71a in the first portion 71, wherein the hole 71a has a diameter between 600 micrometers and 2000 micrometers, between 1000 micrometers and 3000 micrometers or between 2000 micrometers and 5000 micrometers. There are two holes 73a corresponding to the hole 71a in the first portion 71, wherein the hole 73a has a diameter between 600 micrometers and 2000 micrometers, between 1000 micrometers and 3000 micrometers or between 2000 micrometers and 5000 micrometers, wherein a first least distance between the two holes 71a is substantially the same to a second least distance between the two holes 73a.

[0064] Next, referring to Fig. 7c-7d, there is illustrated a second metal plate 9 in Fig. 7c, illustrated a three-dimensional view of the second metal plate 9 in Fig. 7d. The second metal plate 9 has a thickness between 25 micrometers and 600 micrometers, between 20 micrometers and 300 micrometers, between 30 micrometers and 250 micrometers or between 25 micrometers and 180 micrometers. There are two holes 90a in the second metal plate 9, wherein the hole 90a has a diameter between 600 micrometers and 2000 micrometers, between 1000 micrometers and 3000 micrometers or between 2000 micrometers and 5000 micrometers, wherein a third least distance between the two holes 90a is substantially the same to a second least distance between the two holes 73a and substantially the same to the first least distance between the two holes 71a. The second

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metal plate 9 comprises a copper metal layer, copper-gold alloy metal layer, copper-gold-palladium alloy metal layer, copper-gold-silver alloy metal layer, copper-platinum alloy metal layer, copper-iron alloy metal layer, copper-nickel alloy metal layer, copper-tungsten metal layer, tungsten metal layer, brass metal layer, zinc plated brass metal layer, stainless metal layer, nickel plated stainless metal layer, phosphor bronze metal layer, copper plated the aluminum metal layer or aluminum metal layer.

[0065] Next, referring to Fig. 7e, there is illustrated a three-dimensional view of a third metal plate 11 in Fig. 7e. The third metal plate 11 has a thickness between 25 micrometers and 600 micrometers, between 20 micrometers and 300 micrometers, between 30 micrometers and 250 micrometers or between 25 micrometers and 180 micrometers. There are four holes 110a, 112a, 114a, 116a in the third metal plate 11, wherein the hole 110a, 112a, 114a, 116a have a diameter between 600 micrometers and 2000 micrometers, between 1000 micrometers and 3000 micrometers or between 2000 micrometers and 5000 micrometers, wherein a fourth least distance between the two hole 110a and hole 112a and a fifth least distance between the two hole 114a and hole 116a are substantially the same to a second least distance between the two holes 73a and substantially the same to the first least distance between the two holes 71a. The third metal plate 11 comprises a copper metal layer, copper-gold alloy metal layer, copper-gold-palladium alloy metal layer, copper-gold-silver alloy metal layer, copper-platinum alloy metal layer, copper-iron alloy metal layer, copper-nickel alloy metal layer, copper-tungsten metal layer, tungsten metal layer, brass metal layer, zinc plated brass metal layer, stainless metal layer, nickel plated stainless metal layer, phosphor bronze metal layer, copper plated the aluminum metal layer or aluminum metal layer.

[0066] Next, referring to Fig. 7f-Fig.7i, providing two bolts 130, 132 pass through two holes 150a of a fixing metal plate 150 and providing two bolts 134, 136 pass through two holes 152a of a fixing metal plate 152 respectively. Next, the bolts 130, 132, 134, 136 are passing through the holes

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110a, 112a, 114a, 116a of the third metal plate 11 respectively and the third metal plate 11 is formed on the fixing metal plate 150 and the fixing metal plate 152. Next, the bolts 130, 132 are passing through the hole 90a of the second metal plate 9 and the bolts 134, 136 are passing through the hole 90a of another the second metal plate 9, then the second metal plates 9 are formed on the third metal plate 11. Next, the bolts 130, 132, 134, 136 are passing through the holes 71a, 73a of the first metal plate 7 respectively and the first metal plate 7 is formed on the second metal plates 9. Next, repeating to site another the second metal plates 9 on another the first metal plate 7 sequentially until to expose a top of the bolts 130, 132, 134, 136. Next, the top of the bolts 130, 132, 134, 136 are passing through the holes 110a, 112a, 114a, 116a of another the third metal plate 11 respectively and the third metal plate 11 is formed on the second metal plates 9. Next, The top of the bolts 130, 132 are passing through two holes 150a of another the fixing metal plate 150 and the top of the bolts 134, 136 are passing through two holes 152a of another the fixing metal plate 152 respectively, then the fixing metal plates 150, 152 are formed on the third metal plate 11. Finally, providing four sleeve nuts 17 lock on the top of the bolts 130, 132, 134, 136. Then, multiple the first metal plates 7, multiple the second metal plates 9, two the third metal plates 11, two fixing metal plates 150 and two fixing metal plates 152 forming a metal trace block 19.

[0067] Next, referring to Fig. 7j the metal trace block 19 is put in a mold 23. The mold 23 may be a metal mold, a ceramics mold or a polymer mold, which has a heat deflection temperature between 400 ℃ and 900 ℃ or between 800 ℃ and 1300 ℃. The mold 23 comprises a gas inlet 23a and a liquid input 23b, wherein the gas inlet 23a is used to input N_2 gas and the liquid input 23b is used to input the liquid form glass layer.

[0068] Next, referring to Fig. 7k, the glass layer (liquid form) 16 fill in the mold 23. The glass layer 16 is a high temperature liquid and fill in the mold 23, and then the glass layer 16 down to a suitable temperature becomes a solid state, wherein the glass layer 16 has a glass transition

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temperature between 300°C and 900°C, between 500°C and 800°C, between 900°C and 1200°C or between 1000°C and 1800°C. The glass layer 16 is a low melting point glass material, wherein the glass layer 16 has a melting point between 300°C and 900°C, 800°C and 1300°C, between 900°C and 1600°C, between 1000°C and 1850°C, or between 1000°C and 2000°C, wherein the melting point may smaller than 1500°C. Furthermore, there is a few bubbles or no bubble in glass layer 16, for example, there is zero to 3 bubbles in one cubic meter of the glass layer 16, 1 to 10 bubbles in one cubic meter of the glass layer 16, 5 to 30 bubbles in one cubic meter of the glass layer 16 or 20 to 60 bubbles in one cubic meter of the glass layer 16, wherein the bubble has a diameter between 0.0001 and 0.001 centimeters, between 0.001 and 0.05 centimeters, between 0.05 and 0.1 centimeters or between 0.05 and 0.5 centimeters. The glass layer 16 may be remove bubbles through multiple laminating process, squeezing process and heating process.

[0069] Next, referring to Fig. 7l, the mold 23is removed and cut the glass layer 16 along a cutting line 16a to remove the fixing metal plate 150, the fixing metal plate 152, the first portion 71 of the first metal plate 7, the second portion 73 of the first metal plate 7 and two the third metal plates 11, and then the column 25 is produced, showed in the Fig. 7m.

[0070] Next, referring to Fig. 7n, cutting the column 25 to produce multiple first substrates 20, wherein the first substrate 20 has a thickness between 20 and 100 micrometers, between 50 and 150 micrometers, between 100 and 300 micrometers or between 150 and 2000 micrometers or greater than 1000 micrometers. The first substrates 20 may be make a planarization process using a suitable process, such as a chemical mechanical polishing (CMP) procedure, mechanical grinding, or laser drilling.

[0071] Next, referring to Fig. 7o, the first substrate 20 comprises multiple second substrates 22. The second substrates 22 are well-regulated an array in the first substrate 20. Each of the second

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substrates has multiple metal plugs 21, wherein the metal plug 21 is formed from the non-circular metal traces 752. The metal plug 21 has the same material, structure and shape with the non-circular metal traces 752. A first pitch 21a and a second pitch 21b is between the metal plugs 21, wherein the first pitch 21a is controlled or the same-2 by a distance of the gap 754 and wherein the second pitch 21b is controlled by a distance of adjacent the non-circular traces 752.

[0072] Next, referring to Fig. 7p-7r, the metal plugs 21 may be arranged different types, such as Fig. 7p, the metal plugs 21 are arranged on the side portions of the second substrate 22, or such as Fig. 7q, the metal plugs 21 are arranged on the side portions and center portion of the second substrate 22, or such as Fig. 7r, some portions of the second substrate 22 are not arranged the metal plugs 21.

[0073] Fig. 8a illustrates a cross-section view of the second substrate 22 illustrates a cross-section view of the metal plug 21. The second substrate 22 comprise an amorphous solid glass layer/body 16 and multiple metal plugs 21, wherein the amorphous solid glass layer/body 16 having a top surface and an opposing bottom surface and the metal plugs 21 extending through the amorphous solid glass layer/body 16 beginning at the top surface and ending at the bottom surface. The top surface of the metal plugs 21 are the same area as the bottom surface of the metal plugs 21.

[0074] Please referring Fig. 8b, the top surface of the metal plugs 21 and the top surface of the amorphous solid glass layer/body 16 are substantially coplanar. The bottom surface of the metal plugs 21 and the bottom surface of the amorphous solid glass layer/body 16 are substantially coplanar.

[0075] Please referring Fig. 8c, the top surface of the metal plugs 21 comprises a top surface of the metal traces 6/ metal traces 752 and a top surface of the first covering layer 6a are substantially coplanar with the top surface of the amorphous solid glass layer/body 16. The bottom surface of the

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metal plugs 21 comprises a bottom surface of the metal traces 6/ metal traces 752 and a bottom surface of the first covering layer 6a are substantially coplanar with the bottom surface of the amorphous solid glass layer/body 16.

[0076] Please referring Fig. 8d, the top surface of the metal plugs 21 comprises a top surface of the metal traces 6/ metal traces 752, a top surface of the first covering layer 6a and a top surface of the second covering layer 6b are substantially coplanar with the top surface of the amorphous solid glass layer/body 16. The bottom surface of the metal plugs 21 comprises a bottom surface of the metal traces 6/ metal traces 752, a bottom surface of the first covering layer 6a and a bottom surface of the second covering layer 6b are substantially coplanar with the bottom surface of the amorphous solid glass layer/body 16.

[0077] Fig. 9a-Fig. 9t illustrates a process to form multiple traces on a top surface and a bottom surface of the first substrate 20.

[0078] Next, referring to Fig. 9a, a first dielectric layer 24 is formed on the top surface of the first substrate 20, wherein the first dielectric layer 24 may include or may be a layer of silicon oxide (such as SiO_2), silicon nitride (such as Si_3N_4), silicon oxynitride (such as SiON), silicon oxycarbide (such as SiOC), phosphosilicate glass (PSG), silicon carbon nitride (such as SiCN), low k dielectric layer (K between 0.5 and 3), or polymer (such as polyimide, benzocyclobutene (BCB), polybenzoxazole (PBO), poly-phenylene oxide (PPO), epoxy, or silosane). The first dielectric layer 24 may be formed or deposited using a suitable process. The first dielectric layer 24 has a thickness between 0.3 and 5 micrometers, between 2 and 10 micrometers, between 1 and 30 micrometers or greater than 30 micrometers.

[0079] Next, referring to Fig. 9b, multiple openings 24a are formed in the first dielectric layer 24 to expose the metal plugs 21. The openings 24a may be formed in the first dielectric layer 24 by a

suitable process, such as etching. The opening 24a has a width between 0.3 and 3 micrometers, between 0.5 and 8 micrometers, between 2 and 20 micrometers or between 2 and 50 micrometers.

[0080] Next, referring to Fig. 9c, a first metal layer 26 is formed on the first dielectric layer 24, on the metal plugs 21 and in the openings 24a. The first metal layer 26 may include an adhesion/barrier layer, such as a layer of titanium, a titanium-tungsten alloy, titanium nitride, chromium, tantalum, tantalum nitride, nickel or nickel vanadium formed using a suitable process, such as vacuum deposition, Physical Vapor Deposition (PVD), Plasma Enhanced Chemical Vapor Deposition (PECVD), sputtering process or an electroplating process, with a thickness, e.g., between 1 nanometer and 2 micrometers, between 0.3 and 3 micrometers or between 0.5 and 10 micrometers.

[0081] Next, referring to Fig. 9d, a second metal layer 28 is formed on the first metal layer 26. The second metal layer 28 may be comprises copper, nickel, gold or aluminum formed using a suitable process, such as vacuum deposition, Physical Vapor Deposition (PVD), Plasma Enhanced Chemical Vapor Deposition (PECVD), sputtering process or an electroplating process, with a thickness, e.g., between 1 nanometer and 5 micrometers, between 1 and 5 micrometers or between 5 and 30 micrometers.

[0082] Next, referring to Fig. 9e, a photoresist layer 30 is formed on the second metal layer 28 by using a suitable process, such as spin coating process or lamination process. Next, a photo exposure process using a 1X stepper and a development process using a chemical solution can be employed to form multiple openings 30a, exposing the second metal layer 28, in the photoresist layer. The photoresist layer 30 may have a thickness, e.g., between 3 and 50 micrometers, wherein the photoresist layer 30 may be a positive-type photo-sensitive resist layer or negative-type photo-sensitive resist layer.

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[0083] Next, referring to Fig. 9f, remove the first metal layer 26 and the second metal layer 28 are under the openings 30a by using a suitable process, such as an etching process.

[0084] Next, referring to Fig. 9g, remove the photoresist layer 30 by using a clean process.

[0085] Next, referring to Fig. 9h, a second dielectric layer 32 is formed on the first dielectric layer 24 and on the second metal layer 28, wherein the second dielectric layer 32 may include or may be a layer of silicon oxide (such as SiO_2), silicon nitride (such as Si_3N_4), silicon oxynitride (such as SiON), silicon oxycarbide (such as SiOC), phosphosilicate glass (PSG), silicon carbon nitride (such as SiCN), low k dielectric layer (K between 0.5 and 3), or polymer (such as polyimide, benzocyclobutene (BCB), polybenzoxazole (PBO), poly-phenylene oxide (PPO), epoxy, or silosane). The second dielectric layer 32 may be formed or deposited using a suitable process. The second dielectric layer 32 has a thickness between 0.3 and 5 micrometers, between 2 and 10 micrometers, between 1 and 30 micrometers or greater than 30 micrometers.

[0086] Next, referring to Fig. 9i, multiple openings 32a are formed in the second dielectric layer 32 to expose the second metal layer 28. The openings 32a may be formed in the second dielectric layer 32 by a suitable process, such as etching. The opening 32a has a width between 0.3 and 3 micrometers, between 0.5 and 8 micrometers, between 2 and 20 micrometers or between 2 and 50 micrometers.

[0087] Next, referring to Fig. 9j, a third metal layer 34 is formed on the second dielectric layer 32, on the second metal layer 28 and in the openings 32a. The third metal layer 34 may include an adhesion/barrier layer, such as a layer of titanium, a titanium-tungsten alloy, titanium nitride, chromium, tantalum, tantalum nitride, nickel or nickel vanadium formed using a suitable process, such as vacuum deposition, Physical Vapor Deposition (PVD), Plasma Enhanced Chemical Vapor

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Deposition (PECVD), sputtering process or an electroplating process, with a thickness, e.g., between 1 nanometer and 2 micrometers, between 0.3 and 3 micrometers or between 0.5 and 10 micrometers.

[0088] Next, referring to Fig. 9k, a fourth metal layer 36 is formed on the third metal layer 34. The fourth metal layer 36 may be comprises copper, nickel, gold or aluminum formed using a suitable process, such as vacuum deposition, Physical Vapor Deposition (PVD), Plasma Enhanced Chemical Vapor Deposition (PECVD), sputtering process or an electroplating process, with a thickness, e.g., between 1 nanometer and 5 micrometers, between 1 and 5 micrometers or between 5 and 30 micrometers.

[0089] Next, referring to Fig. 9l, a photoresist layer 38 is formed on the fourth metal layer 36 by using a suitable process, such as spin coating process or lamination process. Next, a photo exposure process using a 1X stepper and a development process using a chemical solution can be employed to form multiple openings 38a, exposing the fourth metal layer 36, in the photoresist layer. The photoresist layer 38 may have a thickness, e.g., between 3 and 50 micrometers, wherein the photoresist layer 38 may be a positive-type photo-sensitive resist layer or negative-type photo-sensitive resist layer.

[0090] Next, referring to Fig. 9m, remove the third metal layer 34 and the fourth metal layer 36 are under the openings 38a by using a suitable process, such as an etching process.

[0091] Next, referring to Fig. 9n, remove the photoresist layer 38 by using a clean process.

[0092] Next, referring to Fig. 9o, a third dielectric layer 40 is formed on the second second dielectric layer 32 and on the fourth metal layer 36, wherein the third dielectric layer 40 may include or may be a layer of silicon oxide (such as SiO_2), silicon nitride (such as Si_3N_4), silicon oxynitride (such as SiON), silicon oxycarbide (such as SiOC), phosphosilicate glass (PSG), silicon carbon

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nitride (such as SiCN), low k dielectric layer (K between 0.5 and 3), or polymer (such as polyimide, benzocyclobutene (BCB), polybenzoxazole (PBO), poly-phenylene oxide (PPO), epoxy, or silosane). The third dielectric layer 40 may be formed or deposited using a suitable process. The third dielectric layer 40 has a thickness between 0.3 and 5 micrometers, between 2 and 10 micrometers, between 1 and 30 micrometers or greater than 30 micrometers.

[0093] Next, referring to Fig. 9p, multiple openings 40a are formed in the third dielectric layer 40 to expose the fourth metal layer 36. The openings 40a may be formed in the third dielectric layer 40 by a suitable process, such as etching. The opening 40a has a width between 0.3 and 3 micrometers, between 0.5 and 8 micrometers, between 2 and 20 micrometers or between 2 and 50 micrometers.

[0094] Next, referring to Fig. 9q, a protecting layer 42 is formed in the openings 40a, on the third dielectric layer 40 and on the fourth metal layer 36, which can protect the third dielectric layer 40 not to be damaged and the fourth metal layer 36 not be damaged and oxidated.

[0095] Next, referring to Fig. 9r, repeat the processes of Fig.9a-Fig.9p to form the first dielectric layer 24, the first metal layer 26, the second metal layer 28, the second dielectric layer 32, the third metal layer 34, the fourth metal layer 36 and the third dielectric layer 40 on the bottom surface of the first substrate 20.

[0096] Furthermore, referring to Fig. 9s, a passive device 44 may be formed in the first metal layer 28 and the second metal layer 36, such as an inductor, a capacitor or a resistor.

[0097] Next, referring to Fig. 9t, multiple chips 46 and chips 56 set up over the third dielectric layer 40 through a flip chip package process or a wirebonding package process, wherein the chip 46 and 56 comprises may be a memory chip, such as NAND-Flash memory chip, Flash memory chip,

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DRAM chip, SRAM chip or SDRAM chip, a central-processing-unit (CPU) chip, a graphics-processing-unit (GPU) chip, a digital-signal-processing (DSP) chip, a baseband chip, a wireless local area network (WLAN) chip, a logic chip, an analog chip, a global-positioning-system (GPS) chip, a "Bluetooth" chip, or a chip including one or more of a CPU circuit block, a GPU circuit block, a DSP circuit block, a memory circuit block (such as DRAM circuit block, SRAM circuit block, SDRAM circuit block, Flash memory circuit block, or NAND-Flash memory circuit block), a baseband circuit block, a Bluetooth circuit block, a GPS circuit block, a MEMS chip, a COMS image sensor device, a WLAN circuit block, and a modem circuit block, from the semiconductor wafer.

[0098] The chips 46 are set up on the third dielectric layer 40 through a flip chip package process, wherein the chip 46 comprises multiple metal pads 48 and multiple metal bumps 50 formed on the metal pads 48. The metal pad 48 may be an electroplated copper pad, a damascene copper pad or an aluminum pad. The metal bump 50 comprises an adhesion/barrier metal layer formed on the metal pad 48, an electroplated metal layer or an electro-less metal layer formed on the adhesion/barrier metal layer, wherein the adhesion/barrier metal layer comprises a titanium-containing layer, a chromium-containing layer, a tantalum-containing layer or a nickel layer, and the electroplated metal layer comprises a copper layer, a gold layer, a nickel layer, a tin-containing layer, a solder layer, a solder layer over a nickel layer and a copper layer, and the electro-less layer comprises a copper layer, a gold layer or a nickel layer. The electroplated metal layer has a thickness between 2 and 5 micrometers, between 5 and 30 micrometers or between 10 and 50 micrometers. The metal bumps 50 are connected to the fourth metal layer 36 exposed by the openings 40a through a solder layer 54, wherein the solder layer 54 is formed on the fourth metal layer 36 exposed by the openings 40a or is a portion of the metal bump

[0099] 50. An underfill layer 52 is formed between the chips 46 and the third dielectric layer 40.

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[00100] The chips 56 are set up over the third dielectric layer 40 through a polymer adhesion layer 60, wherein the chip 56 comprises multiple metal pads 58. The metal pad 58 may be an electroplated copper pad, a damascene copper pad or an aluminum pad. Multiple metal wires 62 are connected to the metal pads 58 and the fourth metal layer 36 exposed by the openings 40a, wherein the metal wires 62 comprises a gold wire, a copper wire, a metal alloy wire, a silver-containing wire, an aluminum-containing wire or gold-copper alloy wire. An underfill layer 64 is covered the chip56, metal wires 62 and the metal pads 58.

[00101] Multiple discrete passive components 66 set up on the third dielectric layer 40, such as a discrete inductor, a discrete capacitor or a discrete resistor, wherein the discrete passive component 66 comprises a multiple metal pad 68. The discrete passive components 66 mounted on the third dielectric layer 40 through a solder layer 70.

[00102] Next, referring to Fig. 9u, multiple metal bumps 72 are formed on the bottom surface of the substrate 20.

[00103] Fig. 9v is disclosed some structures of metal bump 72.

- Lift side: 1st type of structures of metal bump 72 comprises an adhesion/barrier metal layer 61 formed on the metal pad 48, a metal seed layer 63 formed on the adhesion/barrier metal layer 61, an electroplated metal layer 65 formed on the metal seed layer 63 and a solder layer 67 formed on the electroplated metal layer 65, wherein the adhesion/barrier metal layer 61 comprises a titanium-containing layer, a chromium-containing layer, a tantalum-containing layer or a nickel layer, wherein the first electroplated metal layer 65 comprises a copper layer, a gold layer, a nickel layer, wherein the solder layer 67 can be formed by screen plating, ball mounting, or an electroplating process, such as gold-tin alloy, tin-silver alloy, tin-silver-copper alloy, indium, tin-bismuth alloy, or other lead-free alloy. Lead alloy

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solders can also be used but may be less desirable in some embodiments due to toxicity considerations. The adhesion/barrier metal layer 61 has a thickness between 0.05 and 2 micrometers. The metal seed layer 63 has a thickness between 0.05 and 2 micrometers. The first electroplated metal layer 65 has a thickness between 1 and 5 micrometers, between 2 and 8 micrometers or between 5 and 20 micrometers. The solder layer 67 has a thickness between 30 and 80 micrometers, between 50 and 100 micrometers, between 80 and 150 micrometers or between 120 and 350 micrometers.

- Right side: 2nd type of structure of metal bump 72 comprises an adhesion/barrier metal layer 61 formed on the metal pad 48, a metal seed layer 63 formed on the adhesion/barrier metal layer 61, a first electroplated metal layer 65 formed on the metal seed layer 63 and a second electroplated metal layer 69 formed on the first electroplated metal layer 65, wherein the adhesion/barrier metal layer 61 comprises a titanium-containing layer, a chromium-containing layer, a tantalum-containing layer or a nickel layer, wherein the first electroplated metal layer 65 comprises a copper layer, a gold layer, a nickel layer, wherein the second electroplated metal layer 69 comprises a copper layer, a gold layer, a nickel layer. The adhesion/barrier metal layer 61 has a thickness between 0.05 and 2 micrometers. The metal seed layer 63 has a thickness between 0.05 and 2 micrometers. The first electroplated metal layer 65 has a thickness between 1 and 5 micrometers, between 2 and 4 micrometers, between 5 and 15 micrometers or between 10 and 25 micrometers. The second electroplated metal layer 69 has a thickness between 1 and 5 micrometers, between 2 and 4 micrometers, between 10 and 30 micrometers or between 20 and 60 micrometers.

[00104] Furthermore, referring to Fig. 9w, the chips 46 may be set up on the bottom surface of the first substrate 20.

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[00105] Furthermore, referring to Fig. 9x, the chip 46 may be replaced a 3D IC chip package, wherein the chip 46 comprises a multiple metal pad 48 formed on the top and bottom surface. The metal pads 48 of the top surface of the chip 46 are connected to the metal pads 48 of the bottom surface of the chip 46 through multiple through-silicon-via metal layers. A chip 47 is connected to the 3D IC chip 46 through the flip chip package process, wherein the chip 47 comprises multiple metal pads 49, wherein the metal pad 49 may be an electroplated copper pad, a damascene copper pad or an aluminum pad. The metal pads 49 are connected to the metal pads 48 through a solder layer 51.

[00106] Fig. 9y, illustrates a top view of the first substrate 20. Fig. 9u-Fig. 9w illustrate a cross section view of Line L-L' in Fig. 9y. Multiple the chips 46, the chips 56 and the passive components 66 may also be provided in or on the first substrate 20.

[00107] Next, cutting the first substrate 20 to produce multiple second substrates 22.

[00108] Fig. 10a-Fig. 10j illustrates a damascene process to form the first metal layer 26, the second metal layer 28, the third metal layer 34 and the fourth metal layer 36 on a top surface and a bottom surface of the first substrate 20.

[00109] Referring to Fig. 10a, the dielectric layers 24 in Figs. 9a include two dielectric layers 80 and 82. The dielectric layer 80 is formed on the dielectric layer 82 by a chemical vapor deposition (CVD) process or a spin-on coating process, wherein each of the dielectric layers 80 and 82 may be composed of a low-K oxide layer with a thickness of between 0.3 and 5μm, and preferably of between 0.5 and 3μm, and an oxynitride layer on the low-K oxide layer, of a low-K polymer layer with a thickness of between 0.3 and 5μm, and preferably of between 0.5 and 3μm, and an oxynitride layer on the low-K polymer layer, of a low-K oxide layer with a thickness of between 0.3 and 5μm, and preferably of between 0.5 and 3μm, and a nitride layer on the low-K oxide layer,

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of a low-K polymer layer with a thickness of between 0.3 and 5μm, and preferably of between 0.5 and 3μm, and a nitride layer on the low-K polymer layer, or of a low-K dielectric layer with a thickness of between 0.3 and 5μm, and preferably of between 0.5 and 3μm, and a nitride-containing layer on the low-K dielectric layer. Next, referring to Fig. 10b, a photoresist layer 84 is formed on the dielectric layer 82, an opening 84a in the photoresist layer 84 exposing the dielectric layer 82. Next, referring to Fig. 10c, the dielectric layer 82 under the opening 84a is removed by a dry etching method to form a trench in the dielectric layer 82 exposing the dielectric layer 80. Next, referring to Fig. 10d, after forming the trench in the dielectric layer 82, the photoresist layer 84 is removed. Next, referring to Fig. 10e, a photoresist layer 86 is formed on the dielectric layer 82 and on the dielectric layer 80 exposed by the trench, an opening 86a in the photoresist layer 86 exposing the dielectric layer 80 exposed by the trench. Next, referring to Fig. 19f, the dielectric layer 80 under the opening 86a is removed by a dry etching method to form a via 80a in the dielectric layer 80 exposing the metal plugs 21 in the substrate 20. Next, referring to Fig. 10g, after forming the via 80a in the dielectric layer 80, the photoresist layer 86 is removed. Thereby, an opening 88 including the trench and the via 80a is formed in the dielectric layers 82 and 80. Next, referring to Fig. 10h, an adhesion/barrier layer 90 having a thickness of between 0.1 and 3 micrometers is formed on the metal plugs 21 exposed by the opening 88, on the sidewalls of the opening 88 and on the top surface of the dielectric layer 82. The adhesion/barrier layer 90 can be formed by a sputtering process or a chemical vapor deposition (CVD) process. The material of the adhesion/barrier layer 90 may include titanium, titanium nitride, a titanium-tungsten alloy, tantalum, tantalum nitride, or a composite of the abovementioned materials. For example, the adhesion/barrier layer 90 may be formed by sputtering a tantalum layer on the metallization structure exposed by the opening 88, on the sidewalls of the opening 88 and on the top surface of the dielectric layer 82. Alternatively, the adhesion/barrier layer 90 may be formed by sputtering a tantalum-nitride layer on the metallization structure exposed by the opening 88, on the sidewalls of the opening 88 and on the top surface of the

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dielectric layer 82. Alternatively, the adhesion/barrier layer 90 may be formed by forming a tantalum-nitride layer on the metallization structure exposed by the opening 88, on the sidewalls of the opening 88 and on the top surface of the dielectric layer 82 by a chemical vapor deposition (CVD) process. Next, referring to Fig. 10i, a seed layer 92, made of copper, having a thickness of between 0.1 and 3 micrometers is formed on the adhesion/barrier layer 90 using a sputtering process or a chemical vapor deposition (CVD) process, and then a copper layer 94 having a thickness of between 0.5 and 5μm, and preferably of between 1 and 2μm, is electroplated on the seed layer 92. Next, referring to Fig. 10j, the copper layer 94, the seed layer 92 and the adhesion/barrier layer 90 outside the opening 88 in the dielectric layers 82 and 80 are removed using a chemical mechanical polishing (CMP) process until the top surface of the dielectric layer 82 is exposed to an ambient.

[00110] Fig. 11a-Fig. 11i illustrates an embossing process to form the first metal layer 26, the second metal layer 28, the third metal layer 34 and the fourth metal layer 36 on a top surface and a bottom surface of the first substrate 20.

[00111] Referring to Fig. 11a, the metal plugs 21 are in the glass layer 16 of the first substrate 20, and the opening 96a in the dielectric layer 96 exposes the metal plugs 21.

[00112] Referring to Fig. 11a, a polymer layer 98 can be formed on the dielectric layer 96, and at least one opening 98a is formed in the polymer layer 98 by patterning the polymer layer 98 to expose at least one metal trace 6, as shown in Fig. 11b and Fig. 11c. The metal plugs 21 may include a center portion exposed by an opening 98a and a peripheral portion covered with the polymer layer 98, as shown in Fig. 11b. Alternatively, the opening 98a may expose the entire upper surface of the metal plugs 21 exposed by the opening 96a in the dielectric layer 96 and further may expose the upper surface of the dielectric layer 96 near the metal trace 6, as shown in Fig. 11c.

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[00113] The material of the polymer layer 98 may include benzocyclobutane (BCB), polyimide (PI), polyurethane, epoxy resin, a parylene-based polymer, a solder-mask material, an elastomer, or a porous dielectric material. The polymer layer 98 has a thickness of between 3 and 25μm or between 5 and 50 micrometers.

[00114] The polymer layer 98 can be formed by a spin-on coating process, a lamination process or a screen-printing process. Below, the process of forming a patterned polymer layer 98 is exemplified with the case of spin-on coating a polyimide layer on the dielectric layer 96 and then patterning the polyimide layer.

[00115] Referring to Fig. 11d, an adhesion/barrier layer 100 having a thickness of between 0.1 and 3 micrometers, and preferably between 0.5 and 2 micrometers, is formed on the polymer layer 98 and on the metal plugs 21. The adhesion/barrier layer 100 may be a titanium-tungsten-alloy layer, tantalum-containing layer, a chromium-containing layer or a titanium-nitride layer. The adhesion/barrier layer 100 may be formed by a sputtering method, an evaporation method, or a chemical vapor deposition (CVD) method.

[00116] Referring to Fig. 11e, a photoresist layer 102 can be formed on the adhesion/barrier layer 100 by a spin coating process or a lamination process. Referring to Fig. 11f, the photoresist layer 102 is patterned with the processes of exposure, development, etc., to form a photoresist opening 102a on the above-mentioned adhesion/barrier layer 100 over the metal plugs 21 exposed by the opening 98a.

[00117] Referring to Fig. 11g, an electroplated metal layer 104 is formed on the adhesion/barrier layer 100 in the opening 102a, wherein the electroplated metal layer 104 comprises a copper layer, gold layer, a nickel layer, has a thickness between 2 and 10 micrometers, between 5 and 20 micrometers or between 5 and 35 micrometers.

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[00118] Referring to Fig. 11h, removing the photoresist layer 102.

[00119] Referring to Fig. 11i, the above-mentioned adhesion/barrier layer 100 not under the electroplated metal layer 104 is removed with a dry etching method or a wet etching method. For example, the adhesion/barrier layer 100 made of titanium, titanium-tungsten alloy, titanium nitride, tantalum or tantalum nitride, not under the electroplated metal layer 104 is removed with a reactive ion etching (RIE) process.

[00120] First Application: Please referring to Fig. 12, the second substrates 22 is connected to a OLED display substrate through COG bonding process, wherein the OLED display substrate comprises a first glass substrate 106, a second glass substrate 108, an organic light-emitting diodes layer 110 (or a polymer light-emitting diodes layer, PLED layer) between the first glass substrate 106 and the second glass substrate 108 and multiple transparent electrodes 114. The metal bumps 72 are connected to the transparent electrodes 114 through an anisotropic conductive film (ACF) layer 116, wherein the ACF layer 116 comprises multiple conductive particles 117, such as nickel (Ni) particles, gold (Au) particles, nickel-gold alloy particles, silver-tin alloy particles, silver particles, gold plated particles, silver plated particles or nickel plated particles. The OLED display substrate comprises multiple OLED display panels. The OLED display substrate may comprise touch screen function. A least distance 106a between a centerline of the metal bump 72 and a boundary of the glass substrate 106 is between 3 micrometers and 10 micrometers, 5 micrometers and 15 micrometers, 10 micrometers and 25 micrometers or 20 micrometers and 40 micrometers.

[00121] Next, cutting the second substrates 22 and the OLED display substrate to produce multiple package units.

[00122] Second Application: Furthermore, the OLED display substrate can be replaced to a Micro Electro Mechanical Systems (MEMS) display substrate. Please referring to Fig. 13, the

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second substrates 22 is connected to a MEMS display substrate through COG bonding process, wherein the MEMS display substrate comprises a first glass substrate 106, a MEMS layer 109 and multiple transparent electrodes 114 formed on the first glass substrate 106. The metal bumps 72 are connected to the transparent electrodes 114 through an anisotropic conductive film (ACF) layer 116, wherein the ACF layer 116 comprises multiple conductive particles 117, such as nickel (Ni) particles, gold (Au) particles, nickel-gold alloy particles, silver-tin alloy particles, silver particles, gold plated particles, silver plated particles or nickel plated particles. The MEMS display substrate comprises multiple MEMS display panels. The MEMS display substrate may comprise touch screen function. A least distance 106a between a centerline of the metal bump 72 and a boundary of the glass substrate 106 is between 3 micrometers and 10 micrometers, 5 micrometers and 15 micrometers, 10 micrometers and 25 micrometers or 20 micrometers and 40 micrometers.

[00123] Next, cutting the second substrates 22 and the MEMS display substrate to produce multiple package units.

[00124] Third application: Please referring to Fig. 14, multiple LED devices 122 are packaged on the bottom surface of the second substrates 22. The second substrates 22 is connected to a LCD display substrate through COG bonding process, wherein the LCD display substrate comprises a first glass substrate 106, a second glass substrate 108, and a transistor liquid crystal display layer 111 between the first glass substrate 106 and the second glass substrate 108 and multiple transparent electrodes 114. The metal bumps 72 are connected to the electrodes 114 through an anisotropic conductive film (ACF) layer 116, wherein the ACF layer 116 comprises multiple conductive particles 117, such as nickel (Ni) particles, gold (Au) particles, nickel-gold alloy particles, silver-tin alloy particles, silver particles, gold plated particles, silver plated particles or nickel plated particles. The LCD display substrate comprises multiple LCD display panels. The LCD display substrate may comprise touch screen function, wherein the LCD display substrate

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comprise an in-cell TFT LCD substrate. There are multiple optical layers 128 between the second substrates 22 and LCD display substrate, such as a diffuser sheet layer, a prism sheet layer, a diffuser layer (or diffuser plate) and a reflector layer. A least distance 106a between a centerline of the metal bump 72 and a boundary of the glass substrate 106 is between 3 micrometers and 10 micrometers, 5 micrometers and 15 micrometers, 10 micrometers and 25 micrometers or 20 micrometers and 40 micrometers.

[00125] Next, cutting the second substrates 22 and the LCD display substrate to produce multiple package units.

[00126] Fourth application: Referring to Fig. 15, this structure of the fourth application is similar to the structure of the third application in Fig. 14. The second substrates 22 is connected to a LCD display substrate through flip chip bonding process, wherein the LCD display substrate comprises a first glass substrate 106 and a second glass substrate 108, and a transistor liquid crystal display layer 111 and thin film transistor circuit layers (not shown) between the first glass substrate 106 and the second glass substrate 108, wherein multiple transparent electrodes 114 on bottom surface of the first glass substrate 106 and multiple metal plugs 113 in the first glass substrate 106, wherein the multiple metal plugs 113 are connected to the transparent electrodes 114 respectively. The structure of first glass substrate 106 can refer to the second substrates 22 in the invention. The metal bumps 72 are connected to the transparent electrodes 114 through a solder layer 107, wherein the solder layer 107 comprises gold-tin alloy, tin-silver alloy, tin-silver-copper alloy, indium, tin-bismuth alloy, or other lead-free alloy. The LCD display substrate comprises multiple LCD display panels. The LCD display substrate may comprise touch screen function, wherein the LCD display substrate comprising an in-cell TFT LCD substrate. There are multiple optical layers 128 between the second substrates 22 and LCD display substrate, such as a diffuser sheet layer, a prism sheet layer, a diffuser layer (or diffuser plate) and a reflector layer. A least distance 106a between a

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centerline of the metal bump 72 and a boundary of the glass substrate 106 is between 30 micrometers and 100 micrometers, 50 micrometers and 150 micrometers, 100 micrometers and 250 micrometers or 50 micrometers and 300 micrometers.

[00127] Fifth application: Referring to Fig. 16, this structure of the fifth application is similar to the structure of the fourth application in Fig. 14. The organic light-emitting diodes layer 110 (or a polymer light-emitting diodes layer, PLED layer) is replaced to the liquid crystal display layer 111. The second substrates 22 is connected to a OLED display substrate through flip chip bonding process, wherein the OLED display substrate comprises a first glass substrate 106 and a second glass substrate 108, and an organic light-emitting diodes layer 110 (or a polymer light-emitting diodes layer, PLED layer) and thin film transistor circuit layers (not shown) between the first glass substrate 106 and the second glass substrate 108, wherein multiple transparent electrodes 114 on bottom surface of the first glass substrate 106 and multiple metal plugs 113 in the first glass substrate 106, wherein the multiple metal plugs 113 are connected to the transparent electrodes 114 respectively. The structure of first glass substrate 106 can refer to the second substrates 22 in the invention. The metal bumps 72 are connected to the transparent electrodes 114 through a solder layer 107, wherein the solder layer 107 comprises gold-tin alloy, tin-silver alloy, tin-silver-copper alloy, indium, tin-bismuth alloy, or other lead-free alloy. The OLED display substrate comprises multiple OLED display panels. The OLED display substrate may comprise touch screen function, wherein the OLED display substrate comprising an in-cell TFT OLED substrate. A least distance 106a between a centerline of the metal bump 72 and a boundary of the glass substrate 106 is between 30 micrometers and 100 micrometers, 50 micrometers and 150 micrometers, 100 micrometers and 250 micrometers or 50 micrometers and 300 micrometers.

[00128] Sixth application: Referring to Fig. 17a, the second substrates 22 can be a port of an OLED display substrate. The OLED display substrate comprises the second substrates 22 and

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second glass substrate 108, and an organic light-emitting diodes layer 110 (or a polymer light-emitting diodes layer, PLED layer), thin film transistor circuit layers (not shown) and transparent electrodes 114 between the second substrates 22 and second glass substrate 108, wherein the metal plugs 21 connected to transparent electrodes 114 through the first metal layer 26. The OLED display substrate comprises multiple OLED display panels. The OLED display substrate may comprise touch screen function, wherein the OLED display substrate comprising an in-cell TFT OLED substrate.

[00129] Referring to Fig. 17b, the structure of the OLED display substrate comprises multiple thin film transistors circuits 700 and multiple organic light-emitting components 800 between the second substrates 22 and second glass substrate 108, wherein the thin film transistors circuit 700 comprises a buffer layer 702, a first gate electrode 704a and a first source electrode 704b formed on the buffer layer 702, a first insulating layer 706 formed on the first gate electrode 704a, the first source electrode 704b and the buffer layer 702. An oxide semiconductor layer 710 is formed on the first insulating layer 706 over the first gate electrode 704a and the first source electrode 704b, wherein the oxide semiconductor layer 710 is connected to the first source electrode 704b through the opening in the first insulating layer 706. A second insulating layer 712 is formed on the oxide semiconductor layer 710. A second gate electrode 714a and a second source electrode 714b formed on the second insulating layer 712, wherein the second source electrode 714b connected to the oxide semiconductor layer 710 through an opening in the second insulating layer 712. A protection layer 716 is formed on the second gate electrode 714a, the second source electrode 714b and the second insulating layer 712. The organic light-emitting component 800 formed on the protection layer 716 and connected to the second source electrode 714b through an opening in the protection layer 716.

[00130] The oxide semiconductor layer 710 comprises a ZnO containing layer, wherein the ZnO containing layer can be doped with a group selected from the group constituted of at least one

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ionic: Gallium (Ga), indium (In), tin (Sn), zirconium (Zr), hafnium (Hf), cadmium (Cd), magnesium (Mg), vanadium (V). The first gate electrode 704a, the first source electrode 704b, the second gate electrode 714a and the second source electrode 714b are formed of a metal selected from the following groups: tungsten (W), titanium (Ti), molybdenum (Mo), silver (Ag), tantalum (Ta), aluminum (Al), copper (Cu), gold (Au), chromium (Cr) or niobium (Nb).

[00131] The organic light-emitting component 800 comprises an anode layer 802, a cathode layer 804 and an organic light-emitting layer 806 between the anode layer 802 and the cathode layer 804, wherein the anode layer 802 formed on the protection layer 716 and connected to the second source electrode 714b. A third insulating layer 808 formed on the protection layer 716 and the anode layer 802, then formed a hole/opening in the third insulating layer 808 and on the anode layer 802. Forming the organic light-emitting layer 806 in the opening and on the third insulating layer 808, then formed the cathode layer 804 on the third insulating layer 808 and on the organic light-emitting layer 806. The anode layer 802 is connected to the metal plugs 21 via a conductive layer formed on the opening through the buffer layer 702, a first insulating layer 706 and second insulating layer 712. The cathode layer 804 is connected to the metal plugs 21 via a conductive layer formed on the opening through the buffer layer 702, the first insulating layer 706, second insulating layer 712 and third insulating layer 808. The buffer layer 702、 first insulating layer 706, second insulating layer 712 and third insulating layer 808 comprises a polyimide, polyamide, acryl resin, benzocyclobutene, phenol resin, oxide layer (buffer layer 702), nitride layer (buffer layer 702).

[00132] The anode layer 802 may contain one or more transparent materials such as indium tin oxide (ITO), indium zinc oxide (IZO), zinc oxide (ZnO), indium gallium oxide (IGO), aluminum zinc oxide (AZO) and In2O3, or non-transparent materials such as Ag, Mg, Al, Pt, Pd, Au, Ni, Nd, Ir, Cr, Li, Ca, Mo, Ti, W, MoW, and Al/Cu. The cathode layer 804 may contain one or more

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transparent materials such as indium tin oxide (ITO), indium zinc oxide (IZO), zinc oxide (ZnO), indium gallium oxide (IGO), aluminum zinc oxide (AZO) and In2O3.

[00133] The organic light-emitting layer 806 may include a hole transport layer (HTL) and a hole injection layer (HIL) stacked toward the pixel electrode (anode layer 802 or cathode layer 804), and an electron transport layer (ETL) and an electron injection layer (EIL) stacked toward the pixel electrode (anode layer 802 or cathode layer 804). Furthermore, various other layers may be stacked if required. Further, the light-emitting layer 806 comprises a carbazole biphenyl(CBP), (III)(bis(1-phenylisoquinoline)(acetylacetonate)iridium, PIQIr(acac)),(III)(bis(1-phenylquinoline)(acetylacetonate)iridium, PQIr(acac)), (III)(tris(1-phenylquinoline)iridium (PQIr), octaethylporphyrin platinum,PtOEP 、 (III))(tris(dibenzoylmethane)(o-phenanthroline)europium(III),PED ： Eu(DBM)3(Phen)),perylene, N,N'-Di(naphthalene-1-yl)-N,N'-diphenyl-benzidine, tris-8-hydroxyquinoline aluminum (PEDOT), copper phthalocyanine,CuPc, 4,4',4"-tris(N-(3-methylphenyl)-N-phenylamino)triphenylamine (MTDATA).

[00134] Referring to Fig. 18 and Fig. 19, an outward of display substrate produced from above first application to sixth application is an unframed display 119, wherein the unframed display 119 comprises a display area 119a has four edges 119b, wherein a gap between the each edge 119b and one of four boundaries of the unframed display 119 has a least distance smaller than 15 micrometers, 20 micrometers, 30 micrometers, 50 micrometers, 100 micrometers, 150 micrometers or 200 micrometers. The unframed display 119 is installed in a shell 123 of a display device 125. Some components (not showed in drawings) can install in the display device 125 (or installed on the second substrates 22), for example, a speaker component, a battery component, a microphone component, a signal receiver component, a wireless signal receiver component, a wireless signal transmitter module.

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[00135] Referring to Fig. 19, the display device 125 comprises multiple connecting ports 127 on the shell 123, wherein the connecting ports 127 comprise a signal connecting port, a power connecting port, and/or a ground connecting port. The display device 125 can connect to another one display device 125b to become a bigger display device 129, wherein the connecting ports 127 of the display device 125 are connected to the connecting ports 127 of the display device 125b. Multiple display devices 125 can be combined a big display device, an advertising billboards. The display devices 125 can be used as a tile on the wall of the building. The display devices 125 can be a display unit on a surface of a magic cube.

[00136] The structure of the OLED display substrate disclosed in the Fig. 12 and Fig. 16 can be referred to the paragraph [00125] to the paragraph [00131].

[00137] Those described above are the embodiments to exemplify the present disclosure to enable the person skilled in the art to understand, make and use embodiments of the present disclosure. This description, however, is not intended to limit the scope of the present disclosure. Any equivalent modification and variation according to the spirit of the present disclosure is to be also included within the scope of the claims stated below.

[00138] The components, steps, features, benefits and advantages that have been discussed are merely illustrative. None of them, nor the discussions relating to them, are intended to limit the scope of protection in any way. Numerous other embodiments are also contemplated. These include embodiments that have fewer, additional, and/or different components, steps, features, benefits and advantages. These also include embodiments in which the components and/or steps are arranged and/or ordered differently.

[00139] In reading the present disclosure, one skilled in the art will appreciate that embodiments of the present disclosure can be implemented in hardware, software, firmware, or any

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combinations of such, and over one or more networks. Suitable software can include computer-readable or machine-readable instructions for performing methods and techniques (and portions thereof) of designing and/or controlling the fabrication and design of integrated circuit chips according to the present disclosure. Any suitable software language (machine-dependent or machine-independent) may be utilized. Moreover, embodiments of the present disclosure can be included in or carried by various signals, e.g., as transmitted over a wireless radio frequency (RF) or infrared (IR) communications link or downloaded from the Internet.

[00140] Unless otherwise stated, all measurements, values, ratings, positions, magnitudes, sizes, and other specifications that are set forth in this specification, including in the claims that follow, are approximate, not exact. They are intended to have a reasonable range that is consistent with the functions to which they relate and with what is customary in the art to which they pertain. The scope of protection is limited solely by the claims. That scope is intended and should be interpreted to be as broad as is consistent with the ordinary meaning of the language that is used in the claims when interpreted in light of this specification and the prosecution history that follows and to encompass all structural and functional equivalents.

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CLAIMS

What is claimed is:

1. A chip package comprising:

a first polymer layer has a first surface, a second surface opposed to said first surface, a first sidewall and a second sidewall opposed to said first sidewall, wherein said first surface is parallel to said second surface, multiple first copper plugs extending through a first portion of said first polymer layer from said first surface to said second surface, wherein said multiple first copper plugs are arranged in a first row substantially parallel to said first and second sidewalls, multiple second copper plugs extending through a second portion of said first polymer layer from said first surface to said second surface, wherein said multiple second copper plugs are arranged in a second row substantially parallel to said first and second sidewalls, wherein each of said multiple first and second copper plugs has a top surface coplanar to said first surface and a bottom surface coplanar to said second surface, wherein a first distance between said first row and said second row is greater than a second distance between said first row and said first sidewalls and greater than a third distance between said second row and said second sidewalls, wherein said first polymer layer has a thickness between 100 and 300 micrometers;

a first interconnection scheme over said first surface, wherein said first interconnection scheme comprises a first metal interconnect over said first surface and a second metal interconnect over said first surface, a second polymer layer between said first surface and said first metal interconnect, a third polymer layer between said first and second metal interconnects and a fourth polymer layer on said second metal interconnect, wherein said first metal interconnect comprises a first metal interconnection layer on said first polymer layer, wherein said second metal interconnect comprises a second metal interconnection layer on said second polymer layer, wherein said first

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metal interconnection layer comprises a first metal layer in a first opening in said second polymer layer and a first copper layer on said first metal layer in said first opening, wherein said second metal interconnection layer comprises a second metal layer on said third polymer layer and in a second opening in said third polymer layer and a second copper layer on said second metal layer in said second opening;

a first solder bump on said first interconnection scheme, wherein said first solder bump is connected to one of said multiple first copper plugs through a third opening in said fourth polymer layer, said second metal interconnection layer, said second opening, said first metal interconnection layer and said first opening;

a second solder bump on said first interconnection scheme, wherein said second solder bump is connected to a third metal interconnection layer of said second metal interconnect through a fourth opening in said fourth polymer layer; and

a first chip over said first interconnection scheme and between said first and second solder bumps, wherein said first chip comprises a third solder bump connected to a fourth metal interconnection layer of said second metal interconnect through a fifth opening in said fourth polymer layer.

2. The chip package of claim 1, no any copper plug with thickness between 100 and 300 micrometers is between said first and second rows.

3. The chip package of claim 1, wherein a third portion is between said first and second portions, wherein said third portion is a square and no any copper plug with thickness between 100 and 300 micrometers in said third portion, wherein said third portion has a width greater than said second and third distances, wherein said third portion has a length greater than said second and third distances.

4. The chip package of claim 1, wherein said first polymer layer further comprises multiple third copper plugs extending through a third portion of said first polymer layer from said first

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surface to said second surface, wherein said multiple third copper plugs are arranged in a third row substantially vertical to said first and second sidewalls, multiple fourth copper plugs extending through a fourth portion of said first polymer layer from said first surface to said second surface, wherein said multiple fourth copper plugs are arranged in a fourth row substantially vertical to said first and second sidewalls, wherein each of said multiple third and fourth copper plugs has a top surface coplanar to said first surface and a bottom surface coplanar to said second surface.

5. The chip package of claim 4, no any copper plug with thickness between 100 and 300 micrometers is between said first, second, third and fourth rows.

6. The chip package of claim 1, further comprising a fourth solder bump under said second surface and directly under said one of said multiple first copper plugs, wherein said fourth solder bump connected to said first solder bump through said one of said multiple first copper plugs.

7. The chip package of claim 1, further comprising:

a second interconnection scheme under said second surface, wherein said second interconnection scheme comprises a third metal interconnect under said second surface, a fifth polymer layer between said second surface and said third metal interconnect and a sixth polymer layer under said third metal interconnect, wherein said third metal interconnect comprises a fifth metal interconnection layer under said fifth polymer layer and connected to said one of said multiple first copper plugs, wherein said fifth metal interconnection layer comprises a third metal layer in a sixth opening in said fifth polymer layer and a third copper layer under said third metal layer in said sixth opening; and

a second chip under said second interconnection scheme and connected to said third metal interconnect via a metal wire.

8. The chip package of claim 1, further comprising:

a second interconnection scheme under said second surface, wherein said second interconnection scheme comprises a third metal interconnect under said second surface, a fifth polymer layer

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between said second surface and said third metal interconnect and a sixth polymer layer under said third metal interconnect, wherein said third metal interconnect comprises a fifth metal interconnection layer under said fifth polymer layer and connected to said one of said multiple first copper plugs, wherein said fifth metal interconnection layer comprises a third metal layer in a sixth opening in said fifth polymer layer and a third copper layer under said third metal layer in said sixth opening; and

a second chip under said second interconnection scheme and connected to said third metal interconnect;

a third chip under said second chip; and

multiple metal bumps between said second and third chips.

9. The chip package of claim 1, wherein said first solder bump has a thickness greater than a fourth distance between a top surface of said first chip and a top surface of said fourth polymer layer.

10. The chip package of claim 1, further comprising a second chip over said first interconnection scheme and multiple fourth solder bumps between said second chip and said first interconnection scheme, wherein said second chip connected to a fifth metal interconnection layer of said second metal interconnect through a sixth opening in said fourth polymer layer.

11. A chip package comprising:

a first polymer layer has a first surface, a second surface opposed to said first surface, a first sidewall and a second sidewall opposed to said first sidewall, wherein said first surface is parallel to said second surface, multiple first copper plugs extending through a first portion of said first polymer layer from said first surface to said second surface, wherein said multiple first copper plugs are arranged in a first row substantially parallel to said first and second sidewalls, multiple second copper plugs extending through a second portion of said first polymer layer from said first surface to said second surface, wherein said multiple second copper plugs are arranged in a second row substantially parallel to said first and second sidewalls, wherein each of said multiple first and

second copper plugs has a top surface coplanar to said first surface and a bottom surface coplanar to said second surface, wherein a first distance between said first row and said second row is greater than a second distance between said first row and said first sidewalls and greater than a third distance between said second row and said second sidewalls, wherein said first polymer layer has a thickness between 100 and 300 micrometers;

a first interconnection scheme over said first surface, wherein said first interconnection scheme comprises a first metal interconnect over said first surface, a second polymer layer between said first surface and said first metal interconnect and a third polymer layer on said first metal interconnect, wherein said first metal interconnect comprises a first metal interconnection layer over said second polymer layer, wherein said first metal interconnection layer comprises a first metal layer in a first opening in said second polymer layer and a first copper layer on said first metal layer in said first opening,;

a first solder bump on said first interconnection scheme, wherein said first solder bump is connected to one of said multiple first copper plugs through a second opening in said third polymer layer, said first metal interconnection layer and said first opening;

a second interconnection scheme under said second surface, wherein said second interconnection scheme comprises a second metal interconnect under said second surface, a fourth polymer layer between said second surface and said second metal interconnect and fifth polymer layer under said second metal interconnect, wherein said second metal interconnect comprises a second metal interconnection layer under said fourth polymer layer and connected to said one of said multiple first copper plugs, wherein said second metal interconnection layer comprises a second metal layer in a third opening in said fourth polymer layer and a second copper layer under said second metal layer in said third opening; and

a first chip under said second interconnection scheme and connected to said second metal interconnect via a metal wire through a fourth opening in said fifth polymer layer.

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12. The chip package of claim 11, no any copper plug with thickness between 100 and 300 micrometers is between said first and second rows.

13. The chip package of claim 11, wherein a third portion is between said first and second portions, wherein said third portion is a square and no any copper plug with thickness between 100 and 300 micrometers in said third portion, wherein said third portion has a width greater than said second and third distances, wherein said third portion has a length greater than said second and third distances.

14. The chip package of claim 11, wherein said first polymer layer further comprises multiple third copper plugs extending through a third portion of said first polymer layer from said first surface to said second surface, wherein said multiple third copper plugs are arranged in a third row substantially vertical to said first and second sidewalls, multiple fourth copper plugs extending through a second portion of said first polymer layer from said first surface to said second surface, wherein said multiple fourth copper plugs are arranged in a fourth row substantially vertical to said first and second sidewalls, wherein each of said multiple third and fourth copper plugs has a top surface coplanar to said first surface and a bottom surface coplanar to said second surface.

15. The chip package of claim 14, no any copper plug with thickness between 100 and 300 micrometers is between said first, second, third and fourth rows.

16. The chip package of claim 11, further comprising:

a second chip under said second interconnection scheme and connected to said second metal interconnect;

a third chip under said second chip; and

multiple metal bumps between said second and third chips

17. The chip package of claim 11, further comprising a second solder bump on said first interconnection scheme, a second chip on said first interconnection scheme and multiple third solder bumps between said first interconnection scheme and said second chip, wherein said second chip is

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between said first and second solder bumps and connected to a third metal interconnection layer of said first interconnection scheme through one of said multiple third solder bumps and a fifth opening in said third polymer layer.

18. The chip package of claim 11, further comprising a memory chip under said second interconnection scheme and connected to said second metal interconnect.

19. The chip package of claim 11, further comprising a second solder bump on said first interconnection scheme, a second chip on said first interconnection scheme, a third chip on said first interconnection scheme, multiple third solder bumps between said first interconnection scheme and said second chip and multiple fourth solder bumps between said first interconnection scheme and said third chip, wherein said second and third chips are between said first and second solder bumps, wherein said second chip is connected to a third metal interconnection layer of said first interconnection scheme through one of said multiple third solder bumps and a fifth opening in said third polymer layer, wherein said third chip is connected to a fourth metal interconnection layer of said first interconnection scheme through one of said multiple fourth solder bumps and a sixth opening in said third polymer layer.

20. The chip package of claim 11, further comprising a second solder bump under said second surface and directly under said one of said multiple first copper plugs, wherein said second solder bump connected to said first solder bump through said one of said multiple first copper plugs.

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ABSTRACT

A display device comprises a display panel substrate and a glass substrate over said display panel substrate, wherein said display panel substrate comprises multiple contact pads, a display area, a first boundary, a second boundary, a third boundary and a fourth boundary, wherein said display area comprises a first edge, a second edge, a third edge and a fourth edge, wherein said first boundary is parallel to said third boundary and said first and third edges, wherein said second boundary is parallel to said fourth boundary and said second and fourth edges, wherein a first least distance between said first boundary and said first edge, wherein a second least distance between said second boundary and said second edge, a third least distance between said third boundary and said third edge, a fourth distance between said fourth boundary and said fourth edge, and wherein said first, second, third and fourth least distances are smaller than 100 micrometers, and wherein said glass substrate comprising multiple metal conductors through in said glass substrate and multiple metal bumps are between said glass substrate and said display panel substrate, wherein said one of said metal conductors is connected to one of said contact pads through one of said metal bumps.

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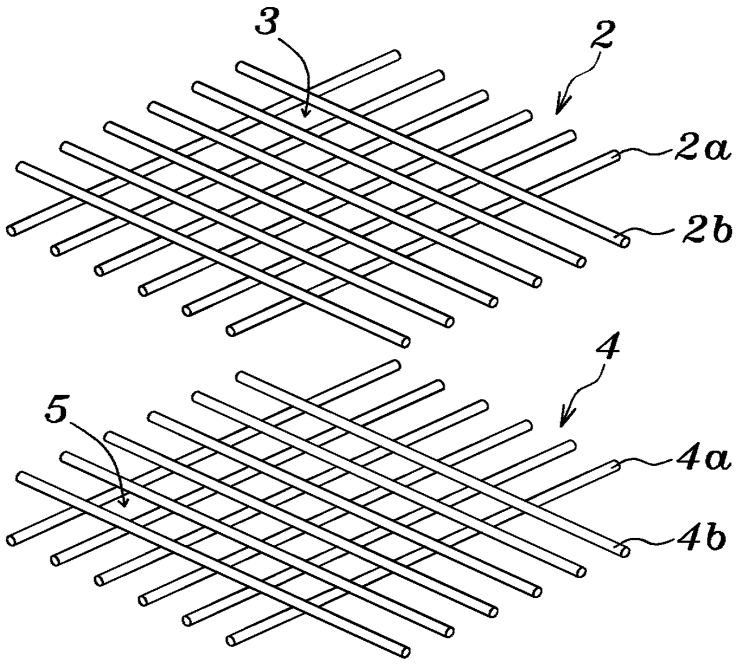


Fig. 1

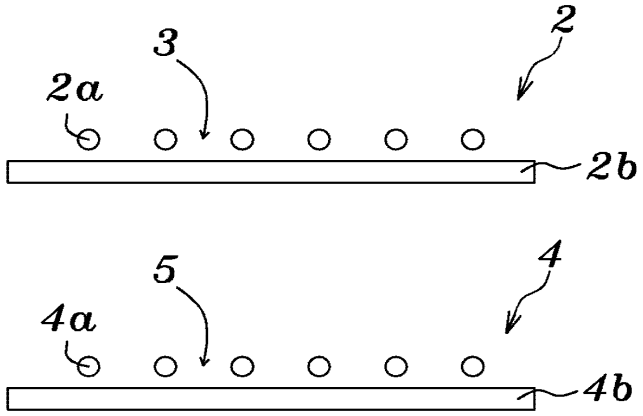


Fig. 2

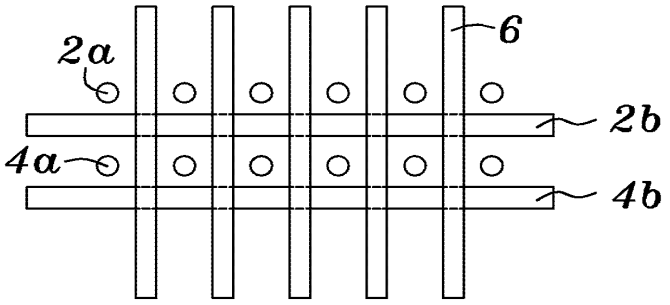


Fig. 3

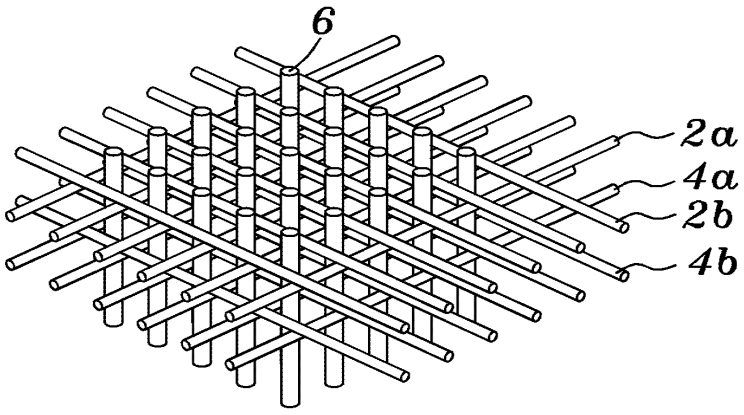


Fig. 4

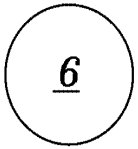


Fig. 5a

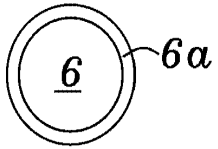


Fig. 5b

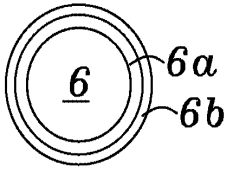


Fig. 5c

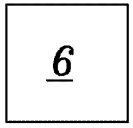


Fig. 5d

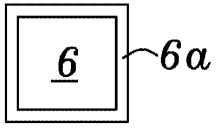


Fig. 5e

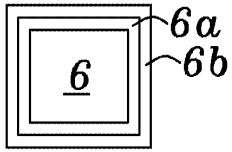


Fig. 5f

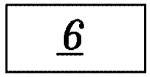


Fig. 5g

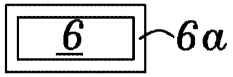


Fig. 5h

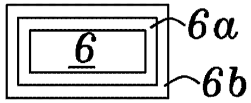


Fig. 5i

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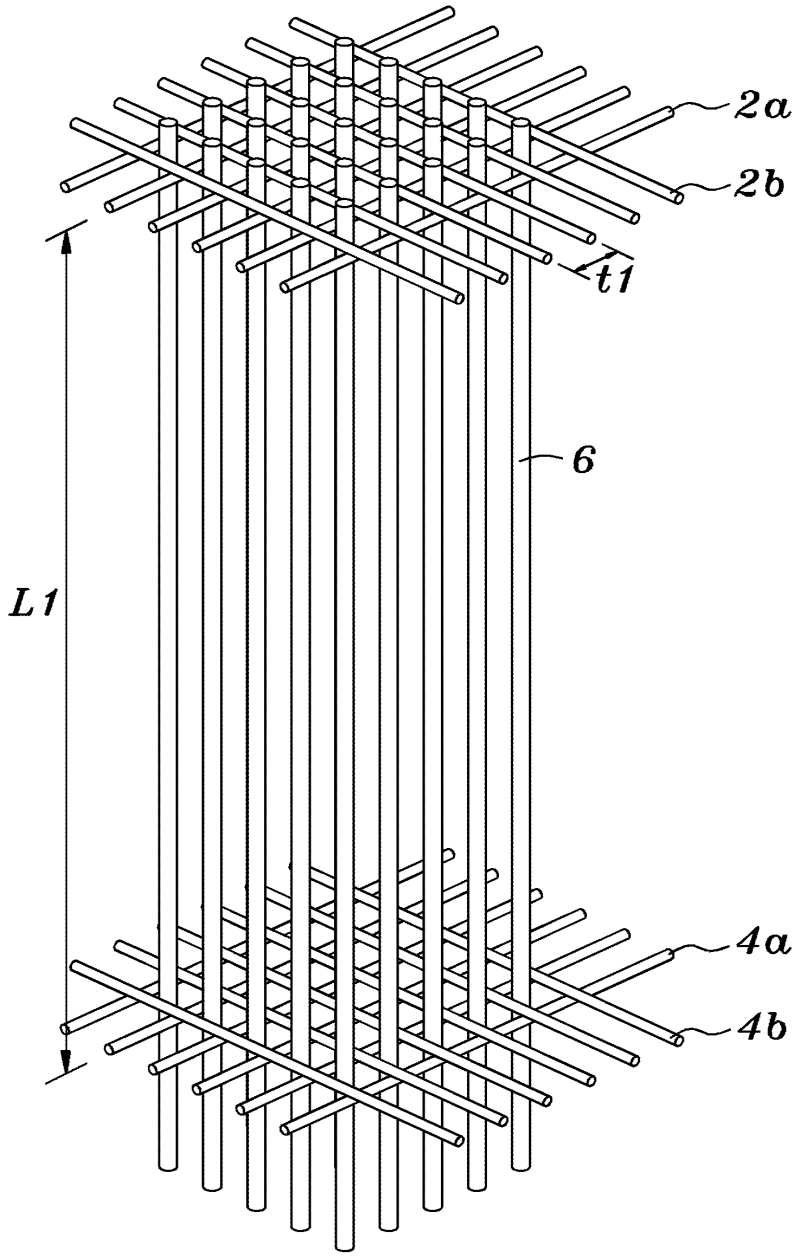


Fig. 6a

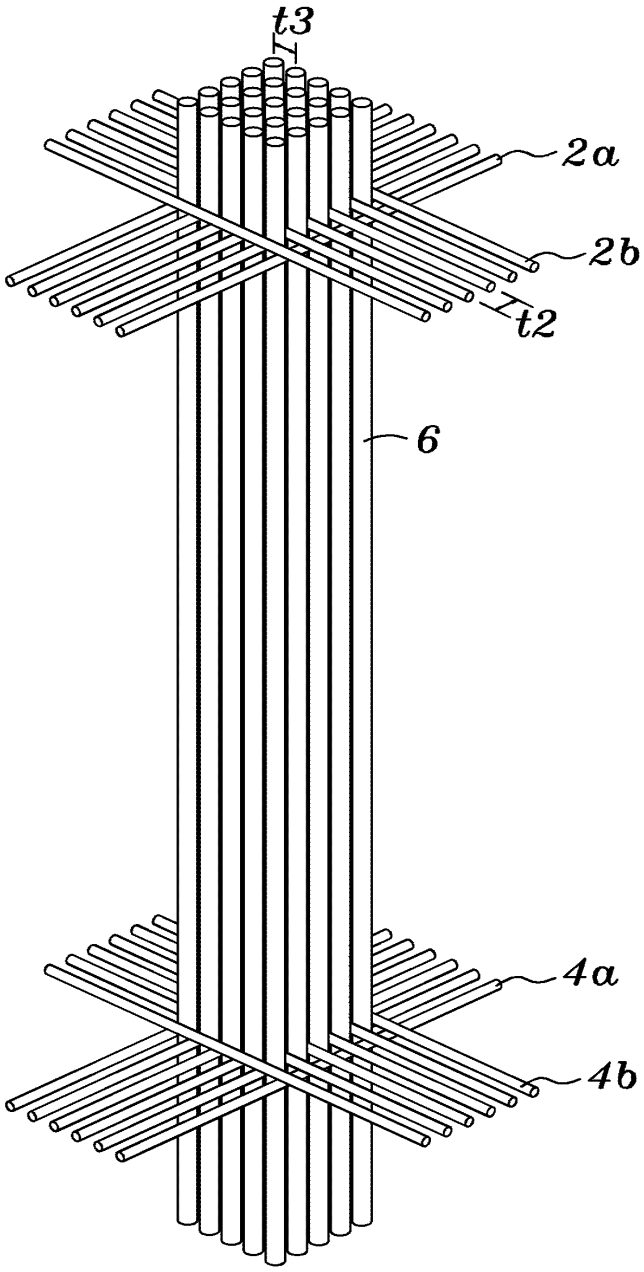


Fig. 6b

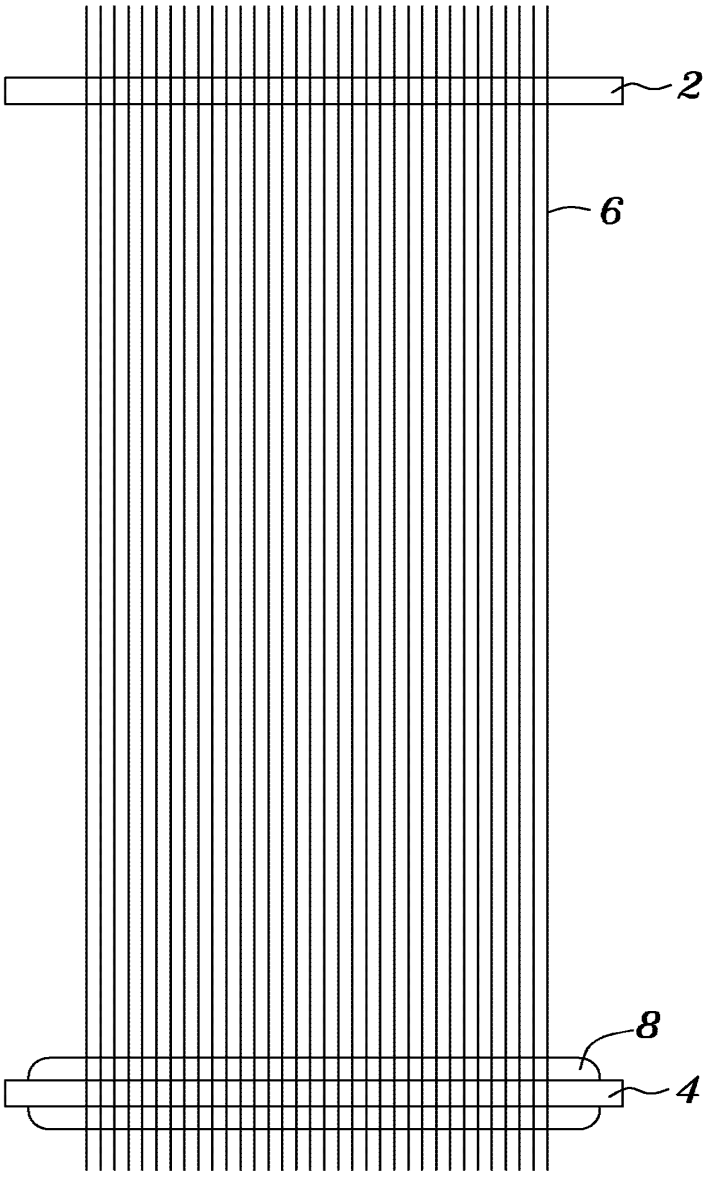


Fig. 6c

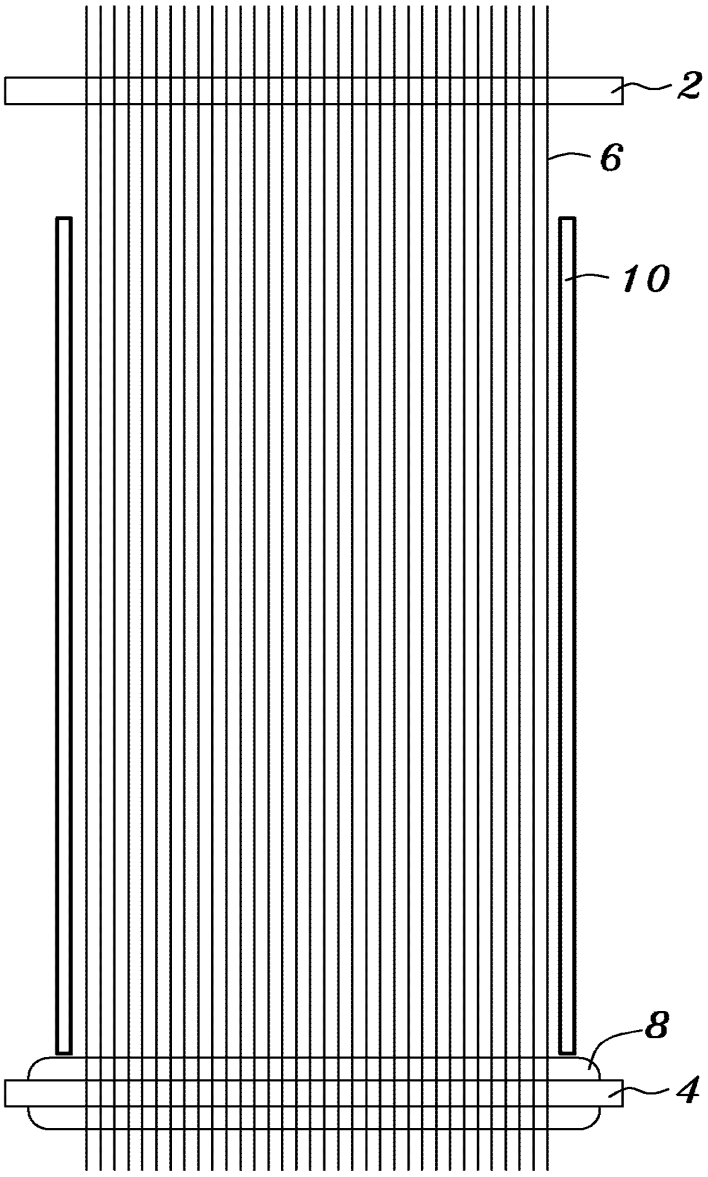


Fig. 6d

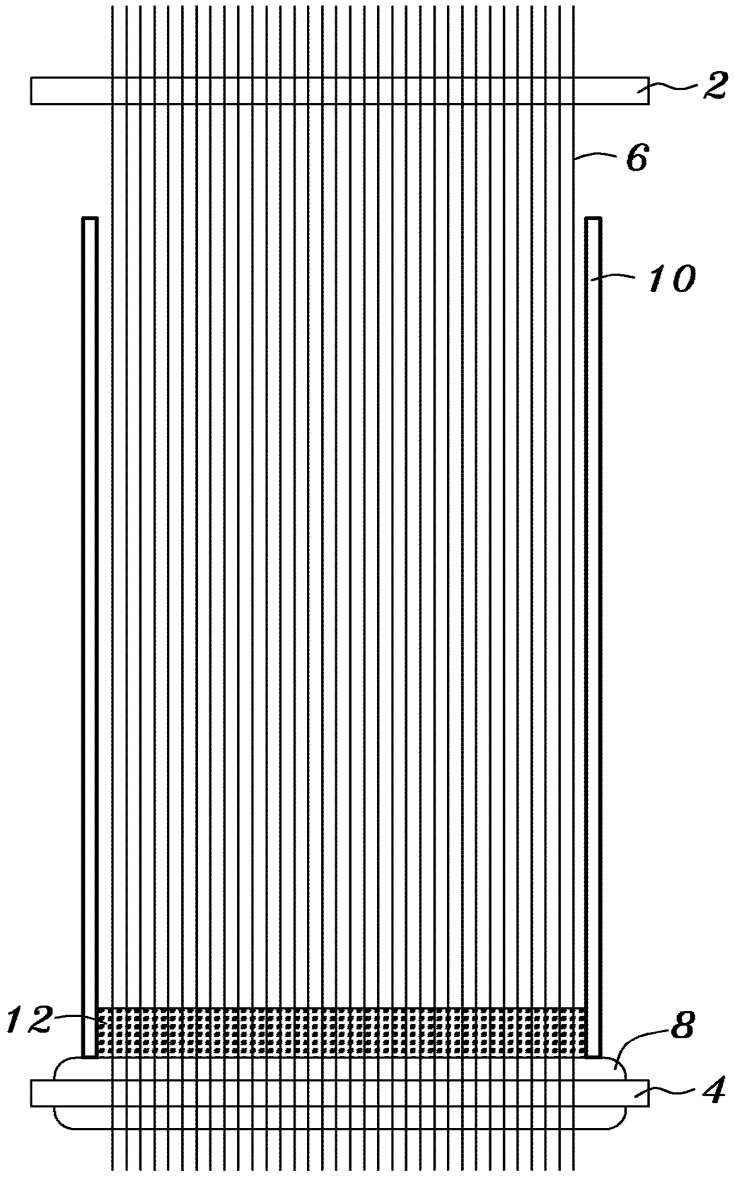


Fig. 6e

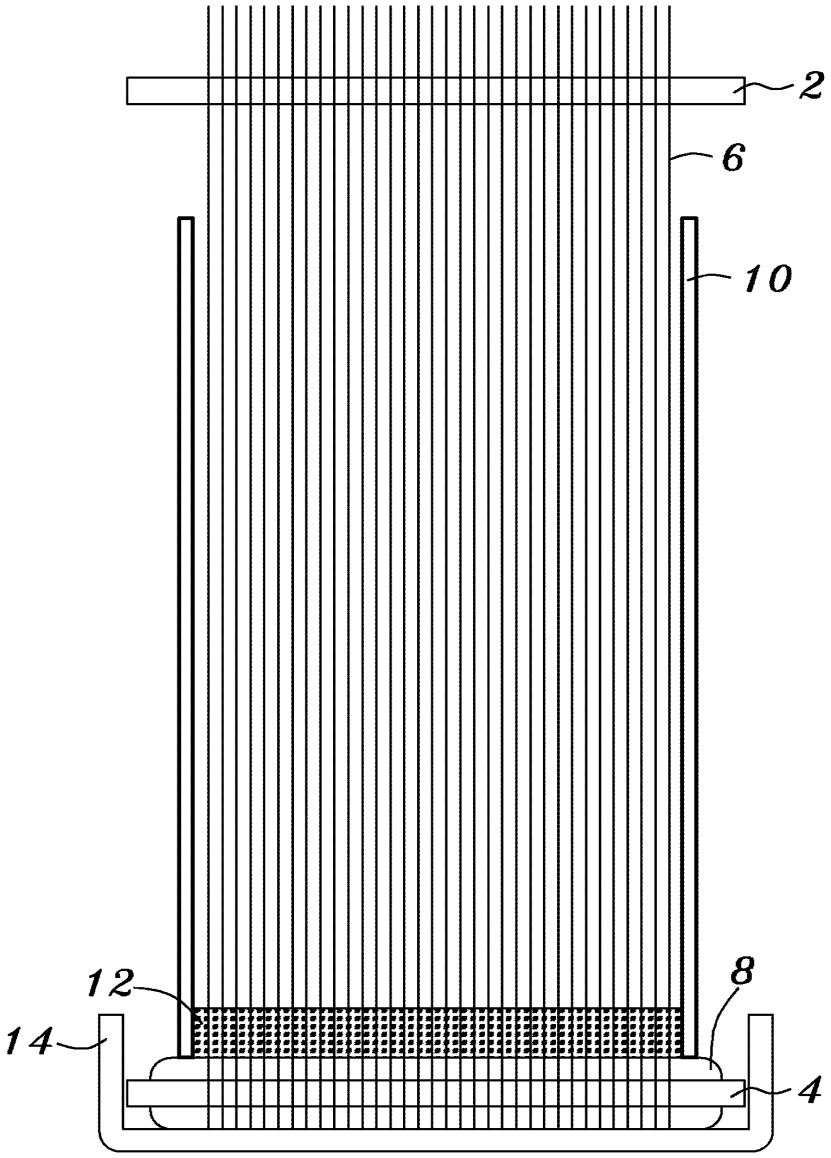


Fig. 6f

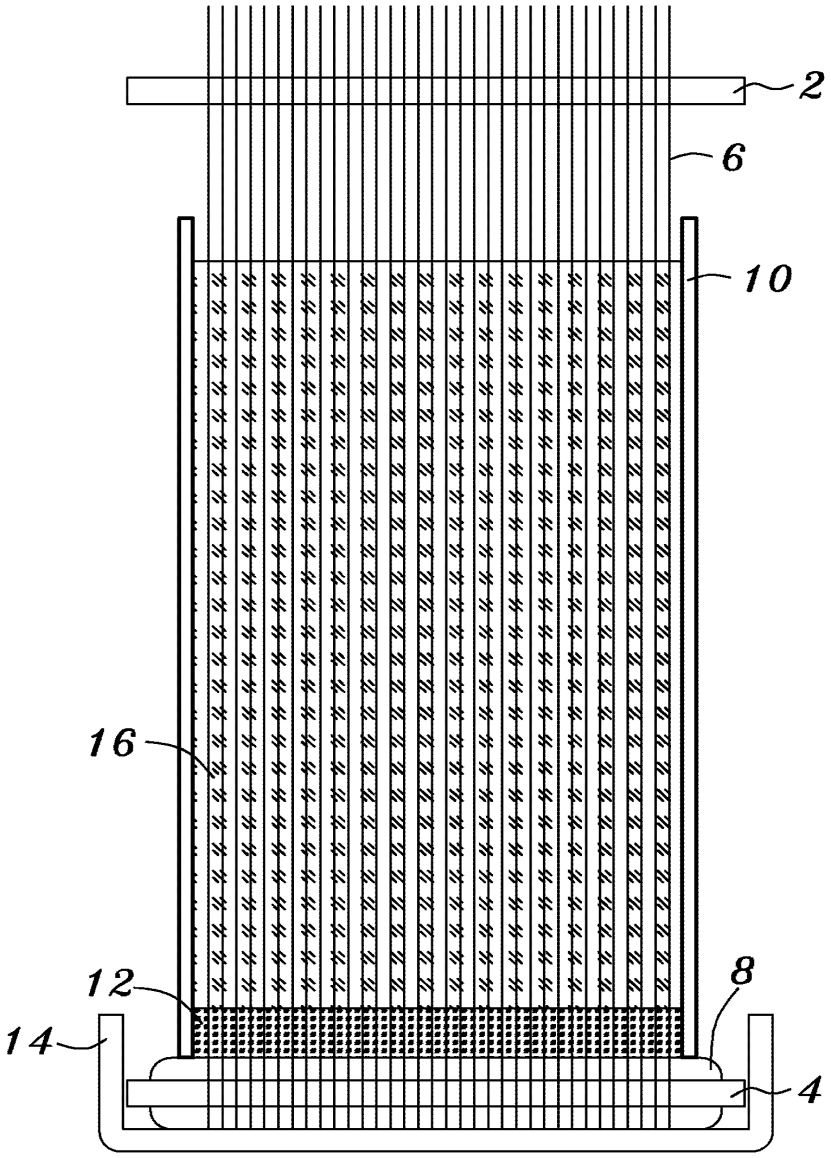


Fig. 6g

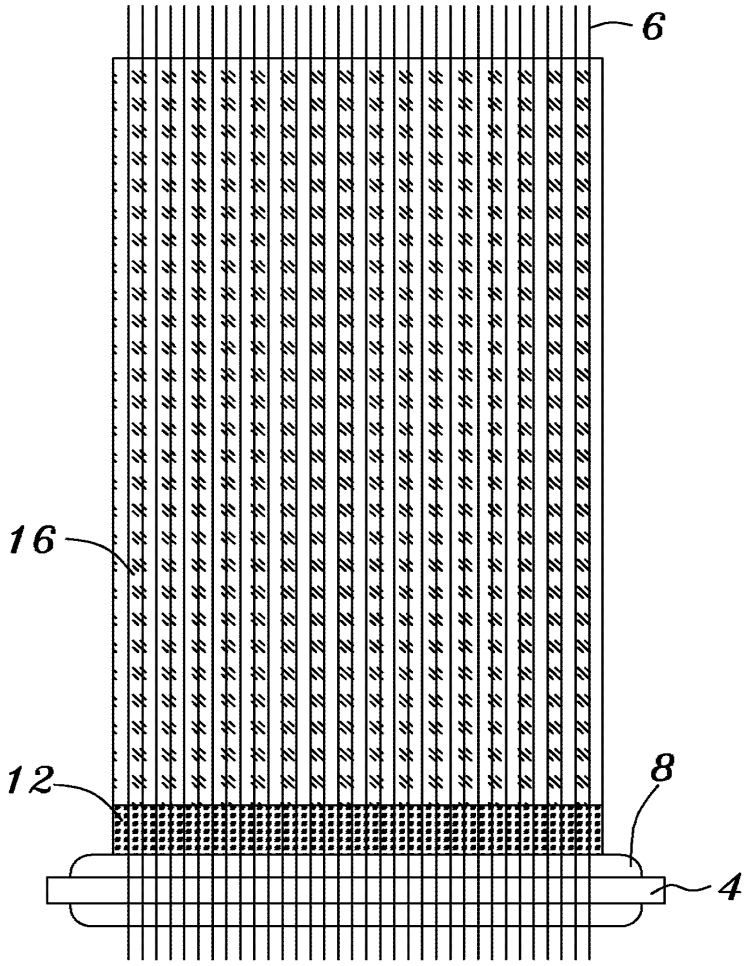


Fig. 6h

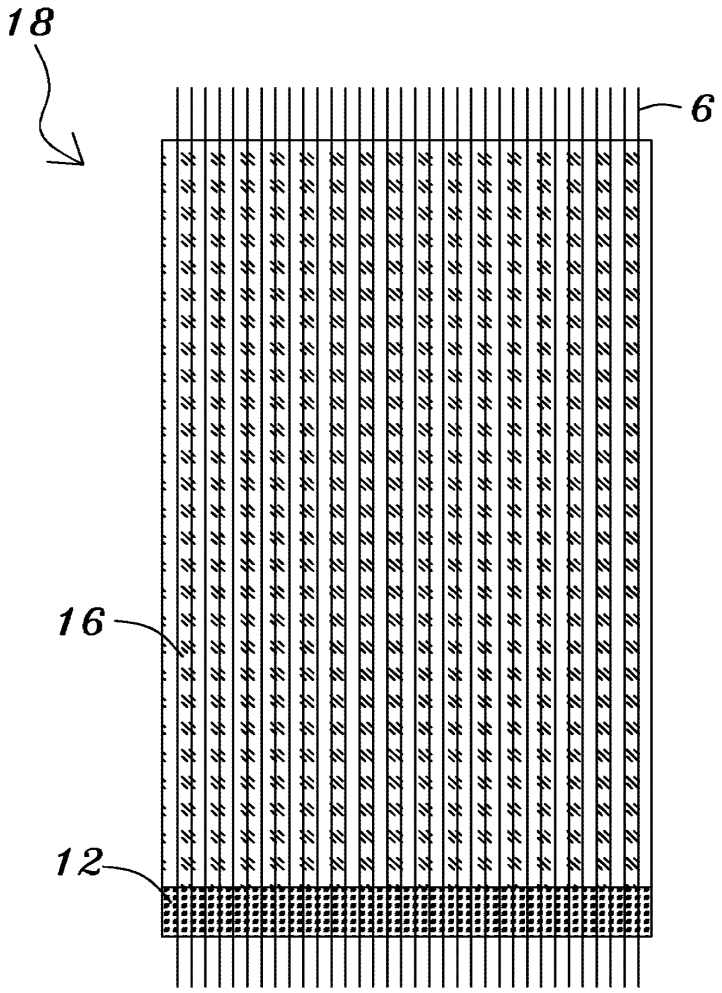


Fig. 6i

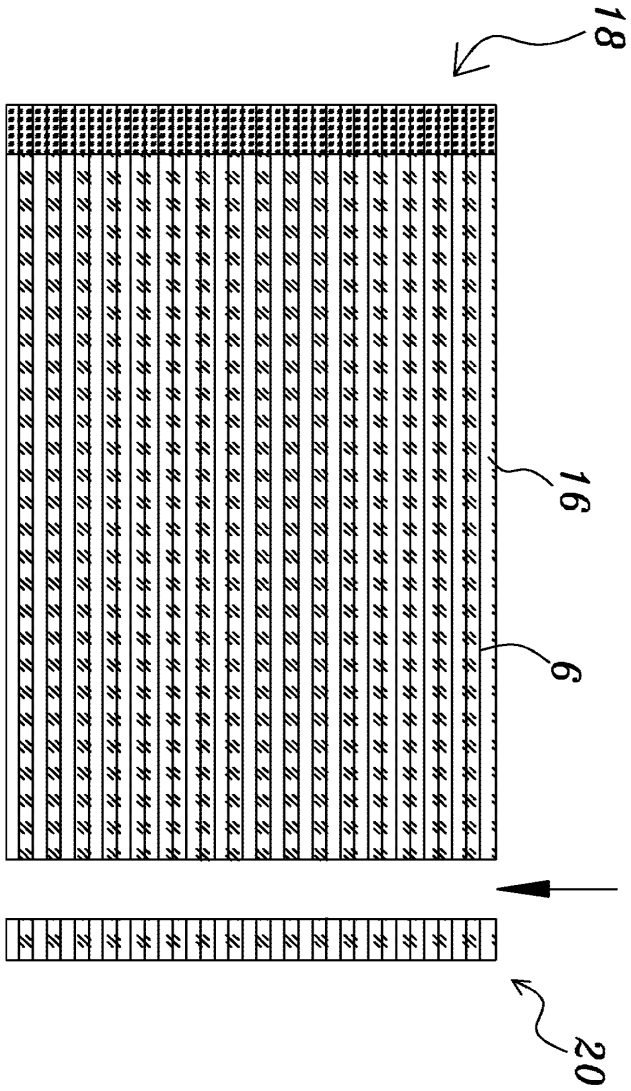


Fig. 6j

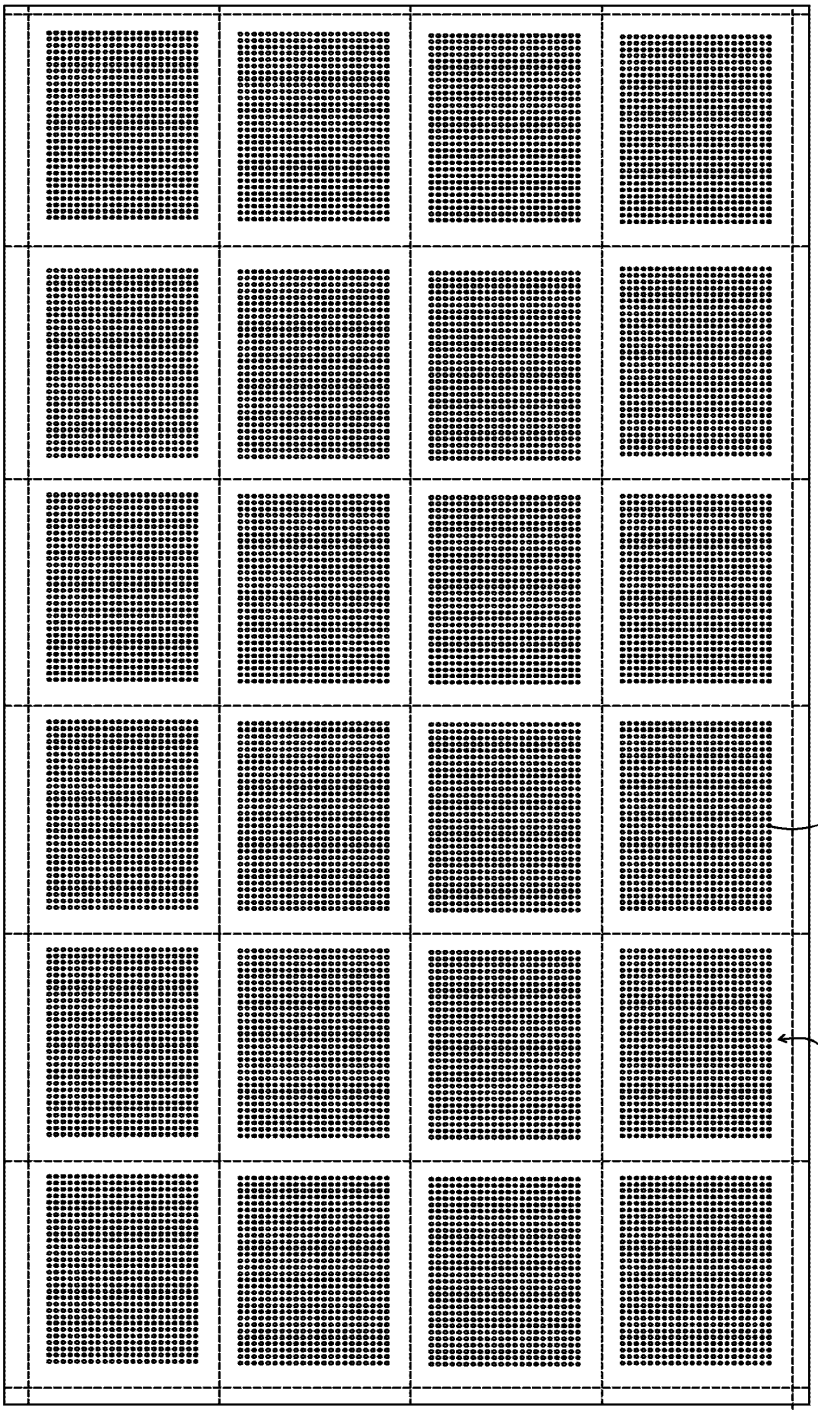


Fig. 6k

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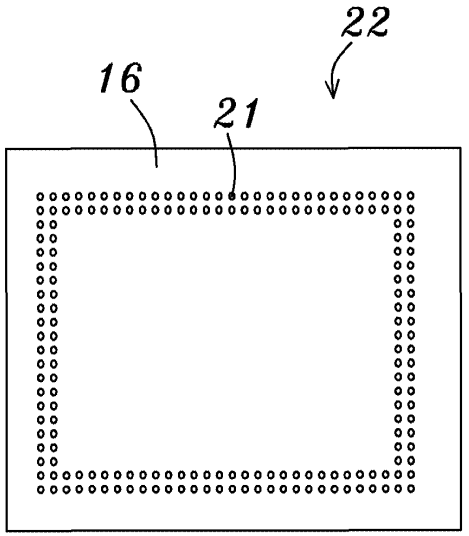


Fig. 6l

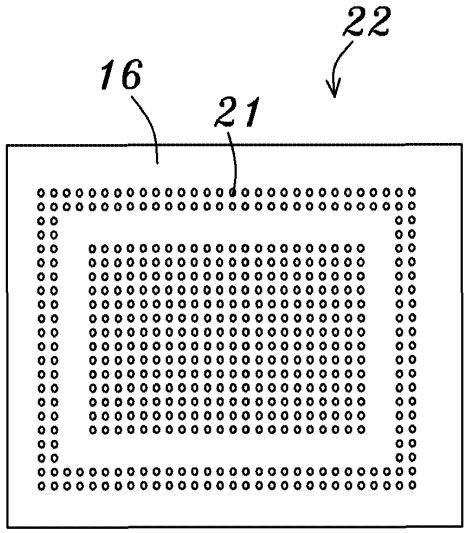


Fig. 6m

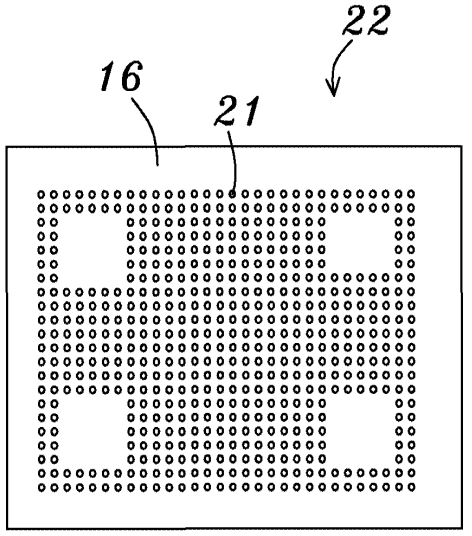


Fig. 6n

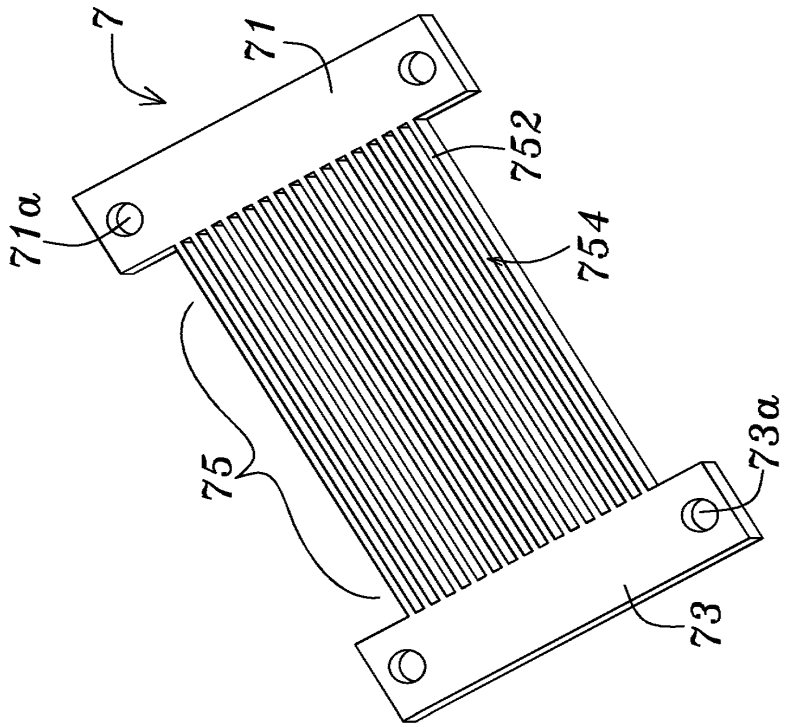


Fig. 7b

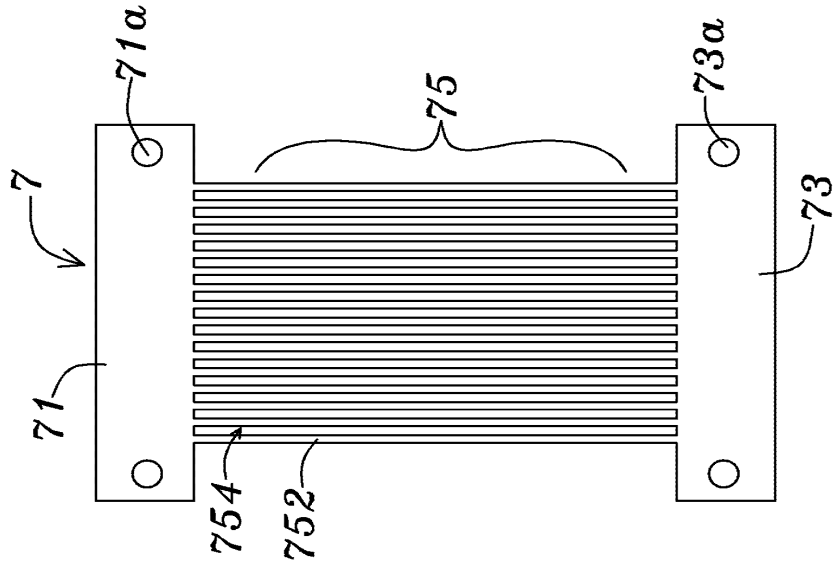


Fig. 7a

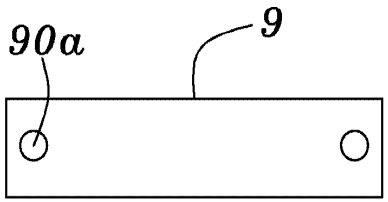


Fig. 7c

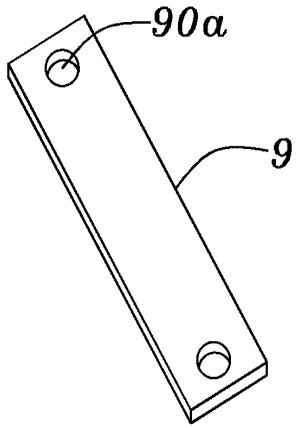


Fig. 7d

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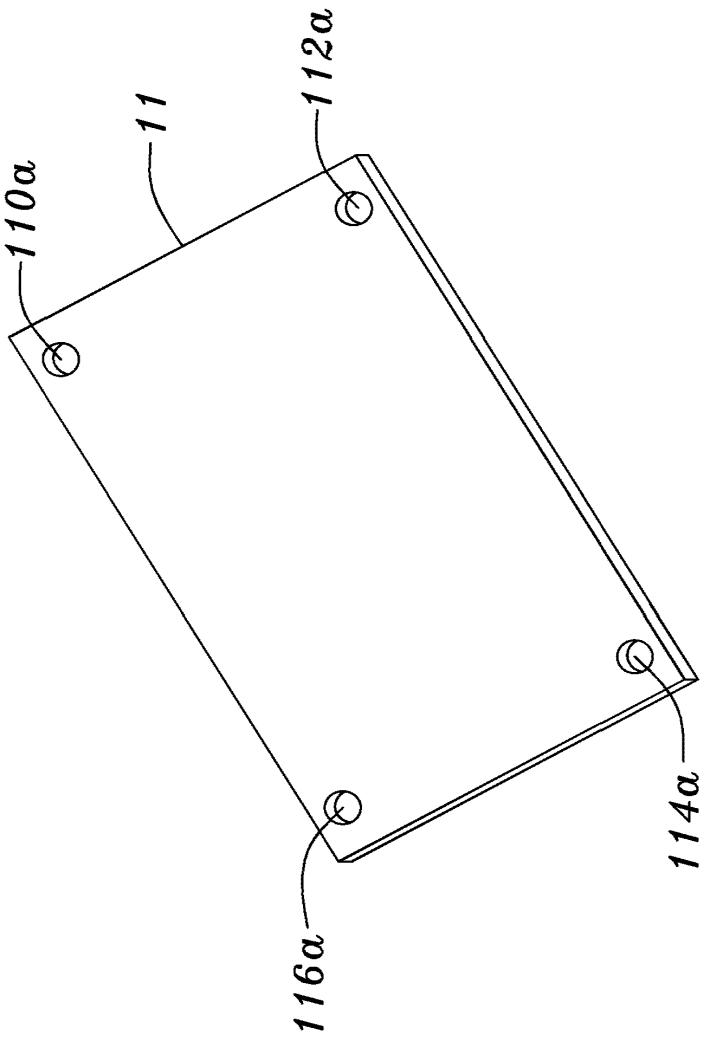


Fig. 7e

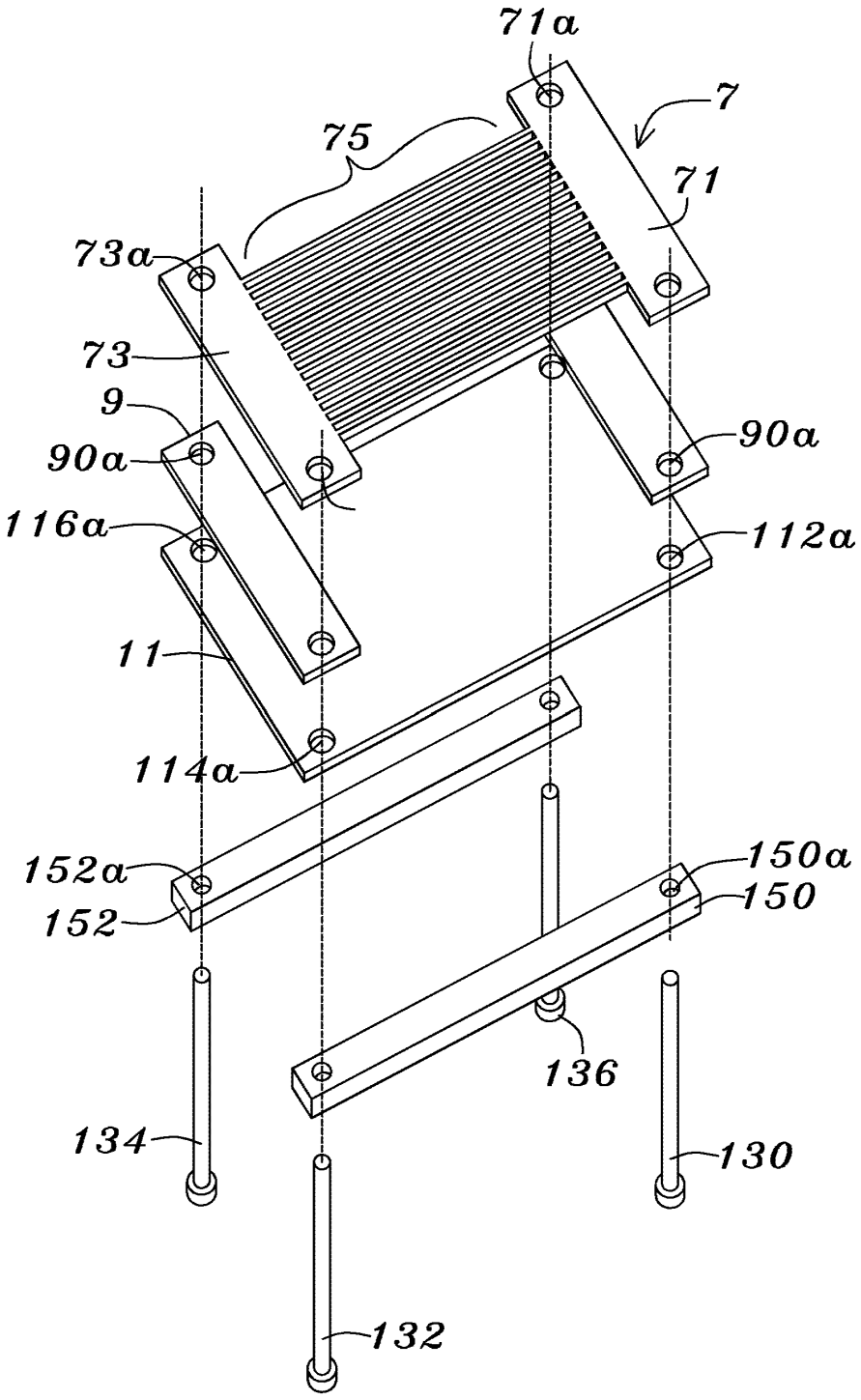

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Fig. 7f

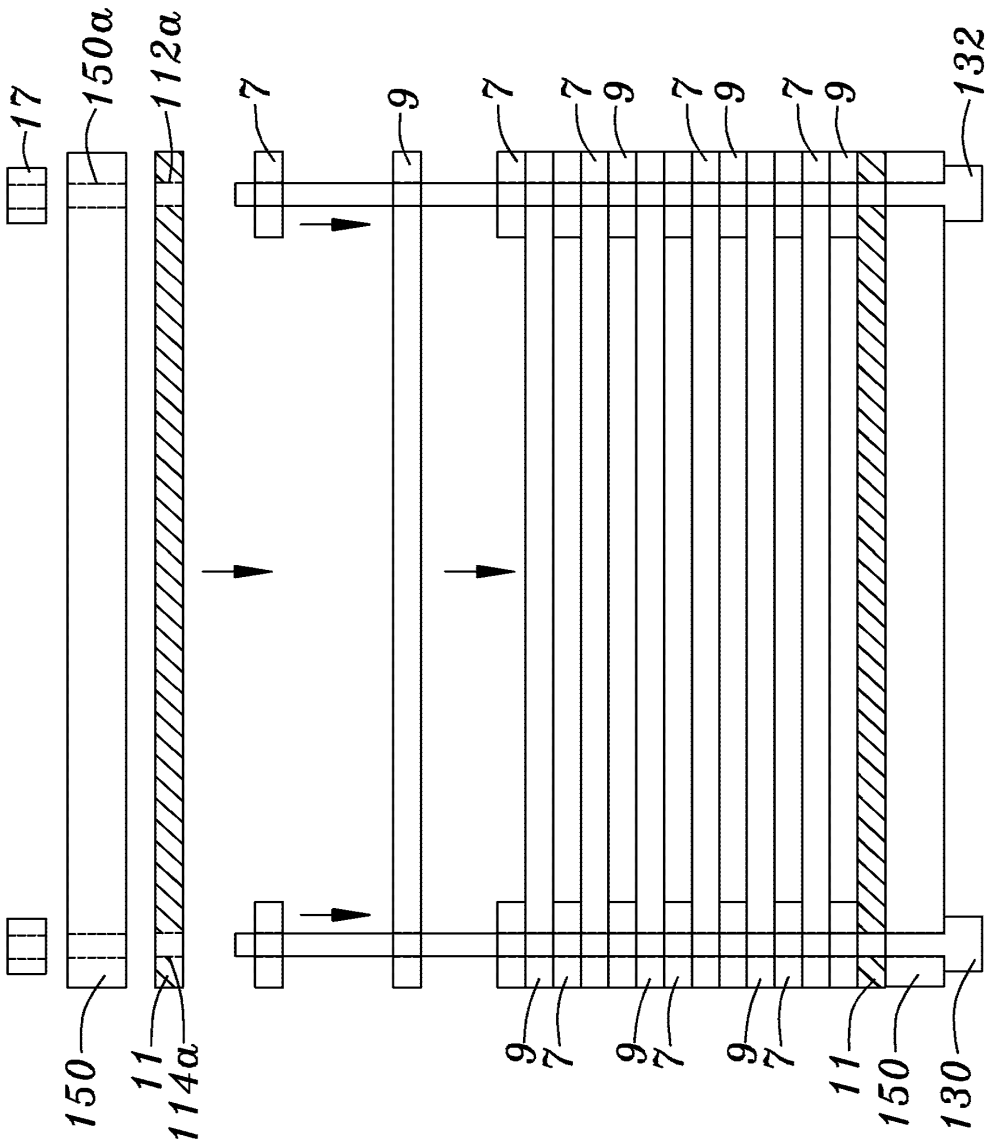


Fig. 7g

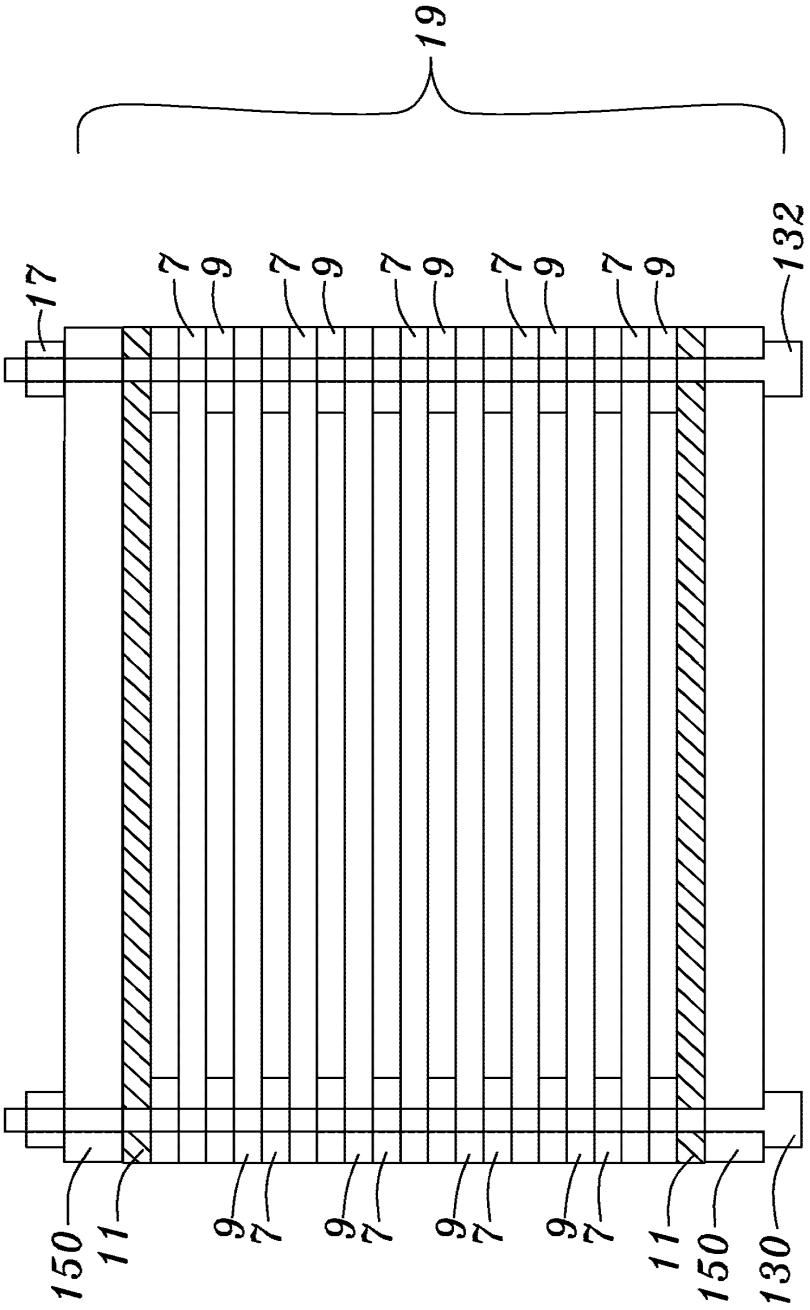


Fig. 7h

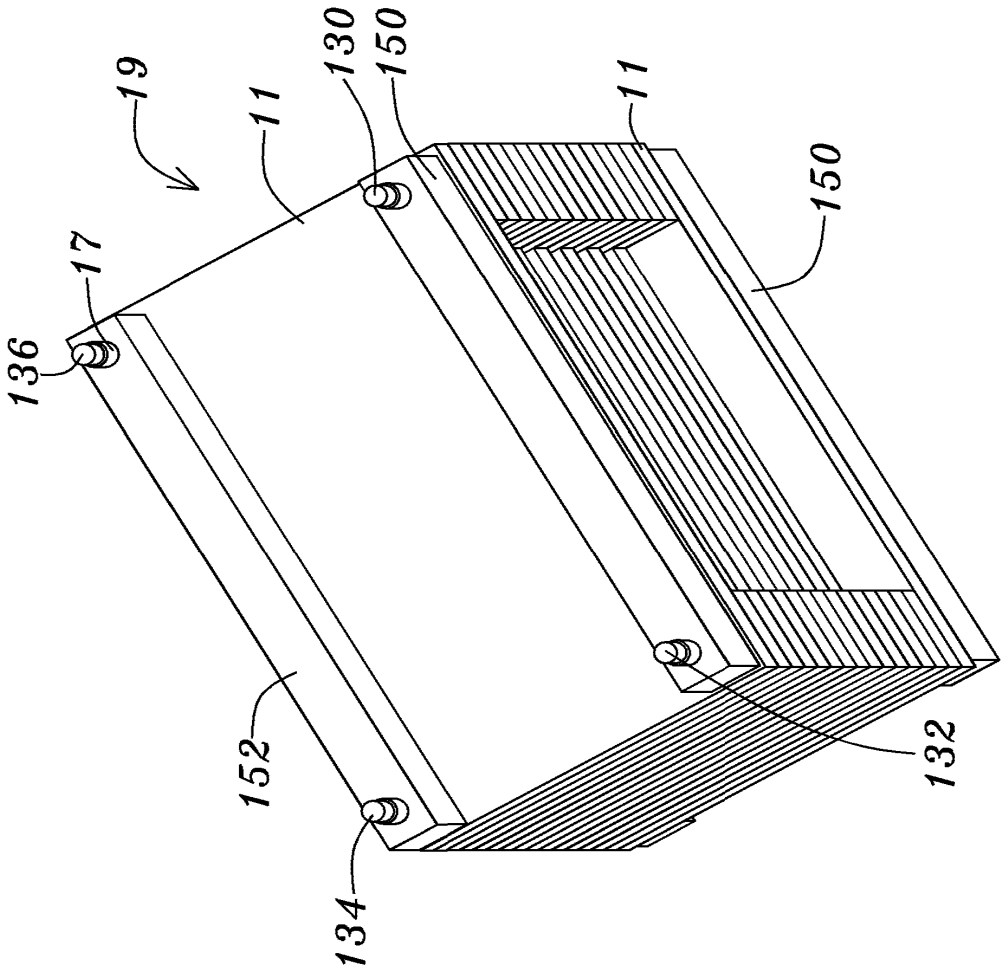


Fig. 7i

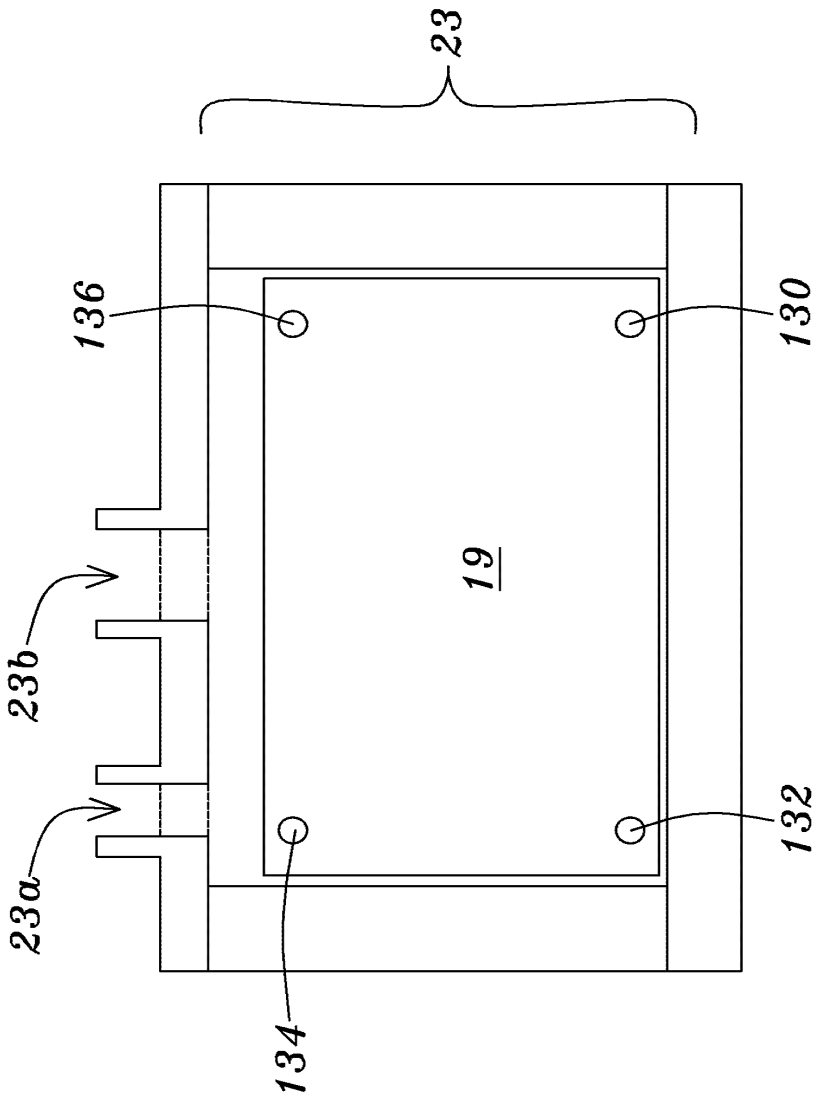


Fig. 7j

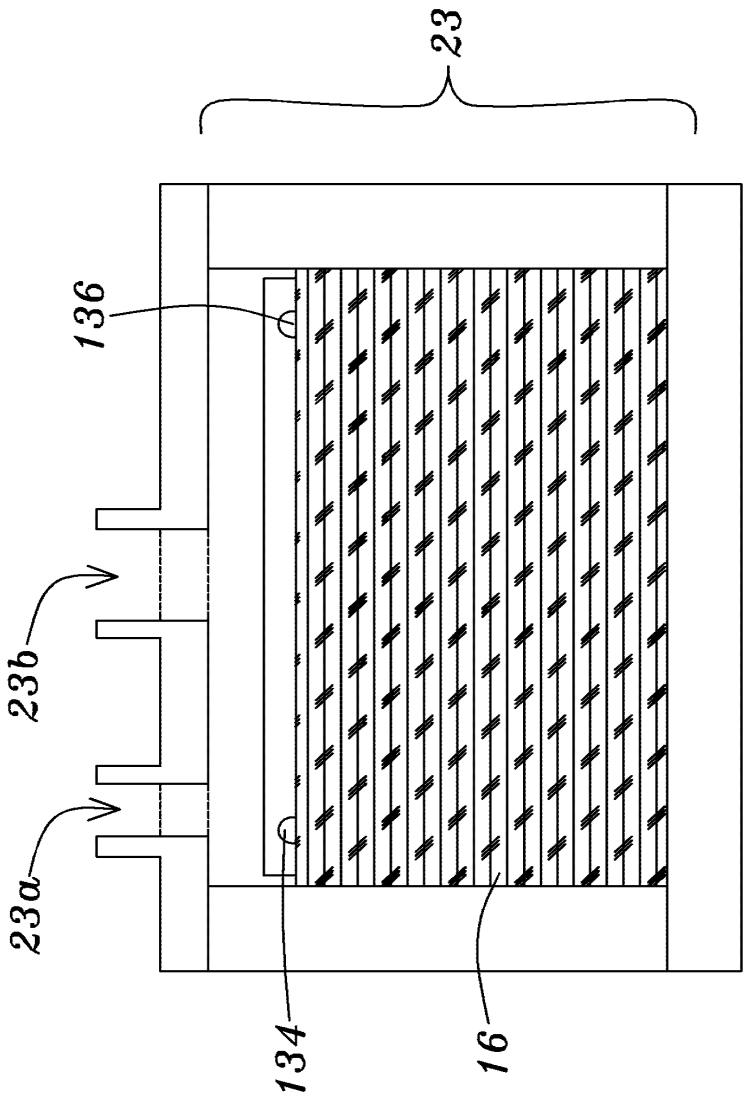


Fig. 7k

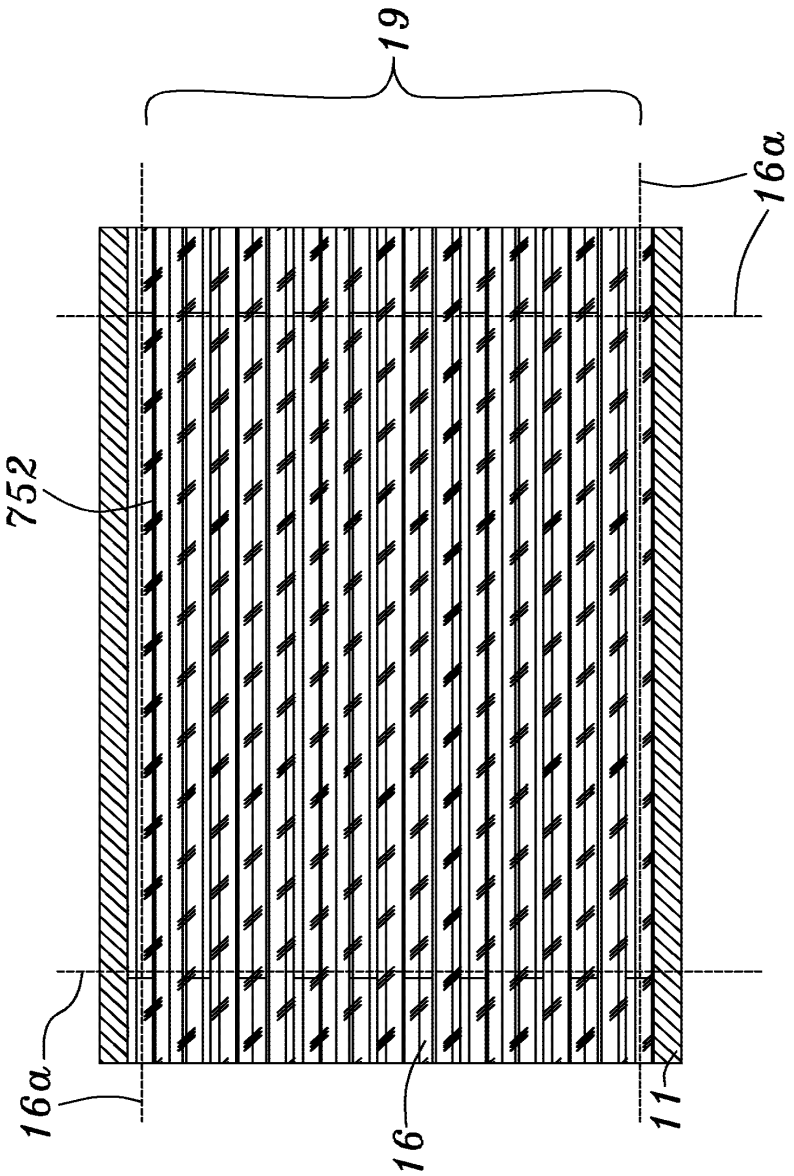


Fig. 71

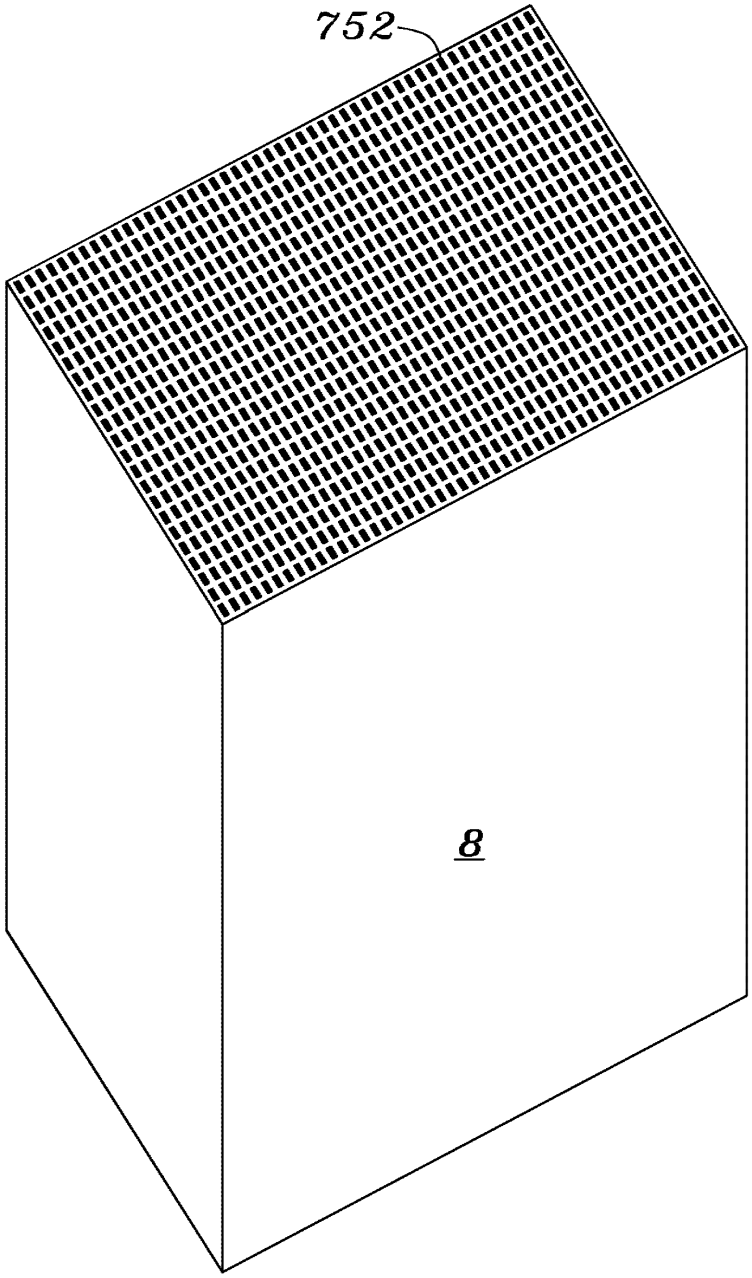


Fig. 7m

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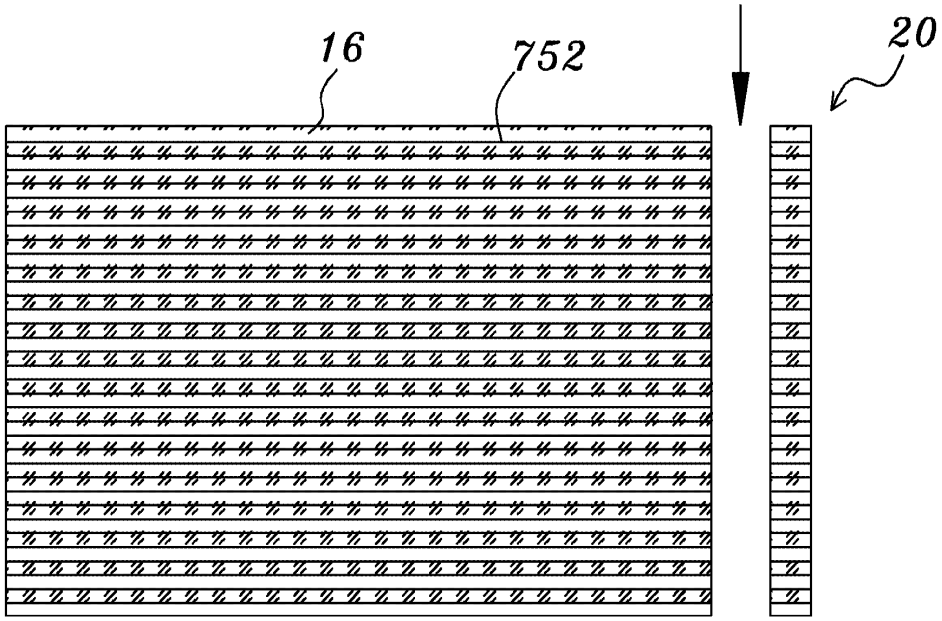


Fig. 7n

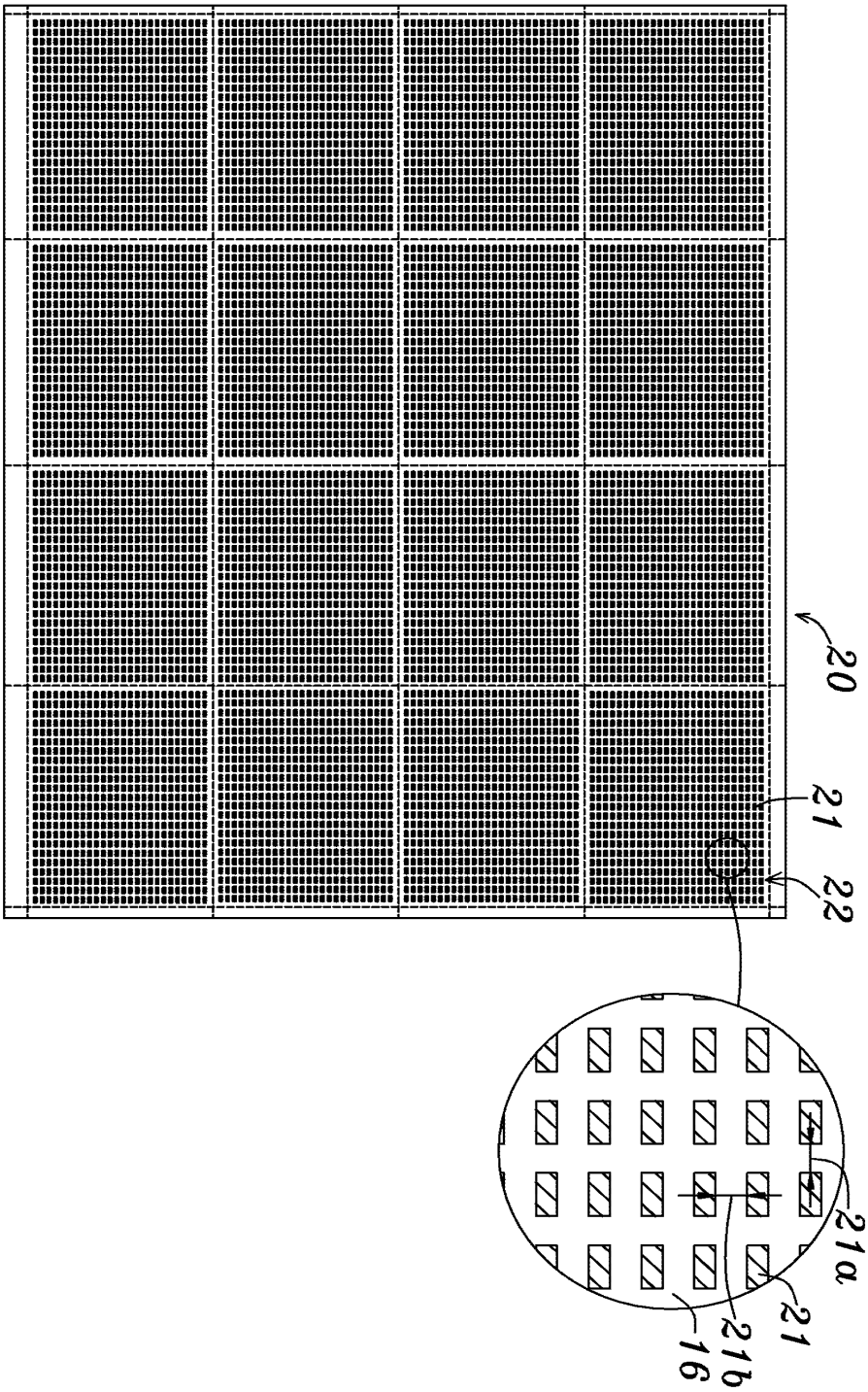


Fig. 7o

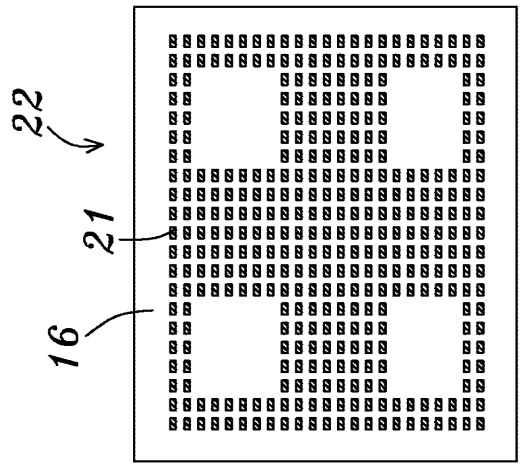


Fig. 7r

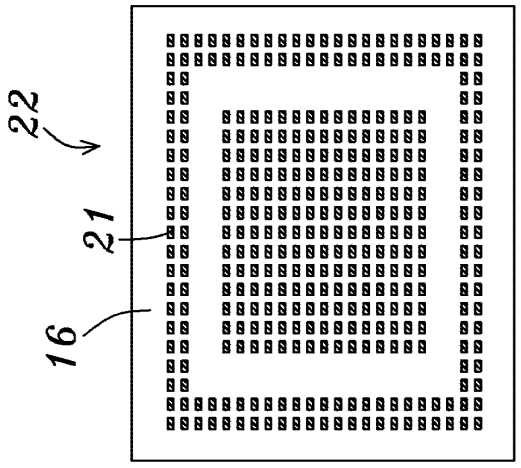


Fig. 7q

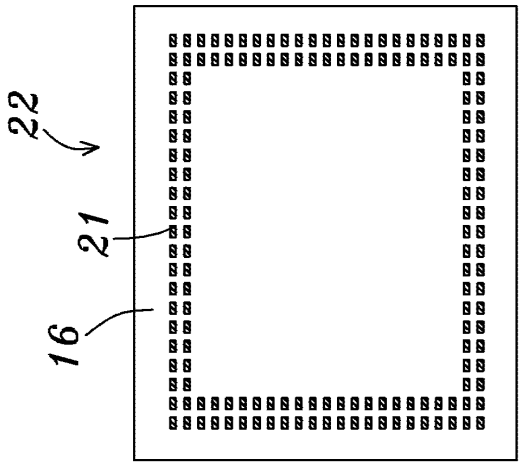


Fig. 7p

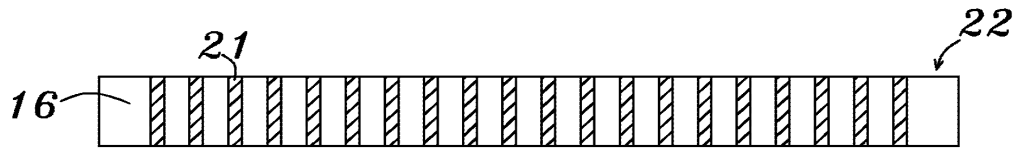


Fig. 8a

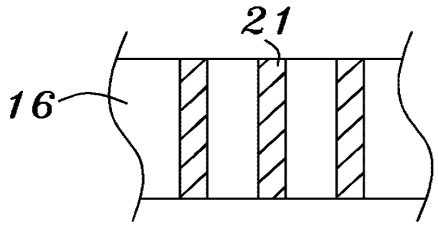


Fig. 8b

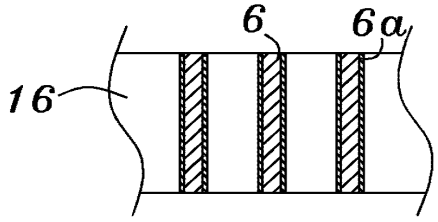


Fig. 8c

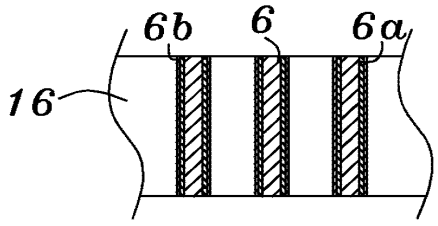


Fig. 8d

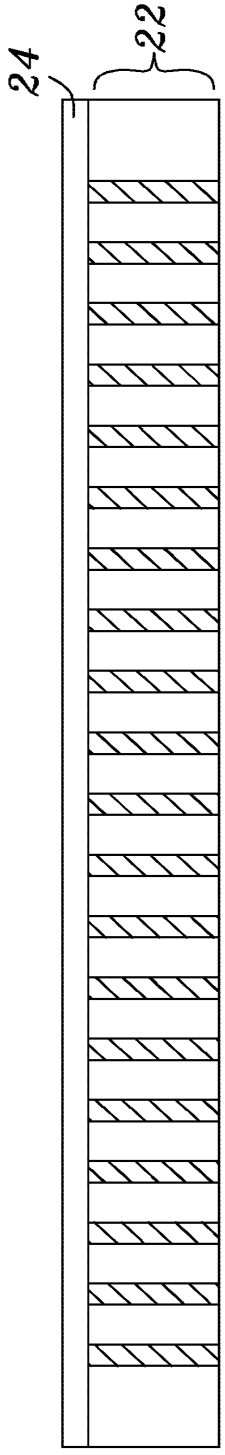


Fig. 9a

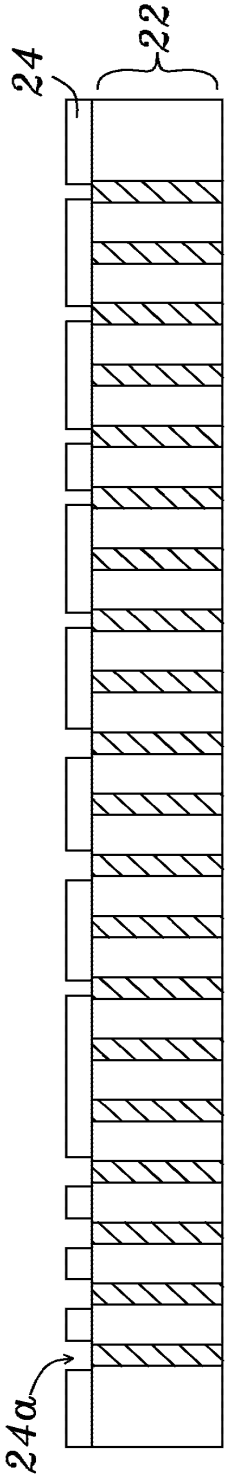


Fig. 9b

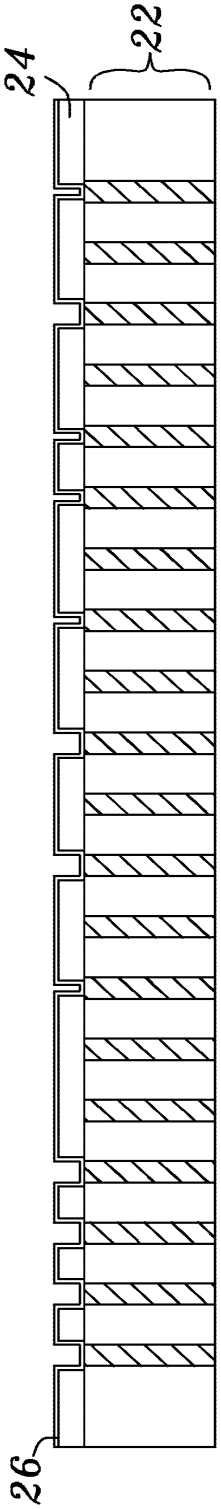


Fig. 9c

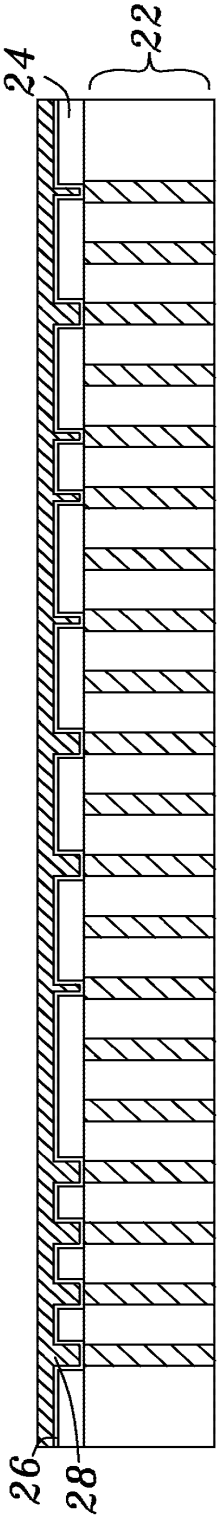


Fig. 9d

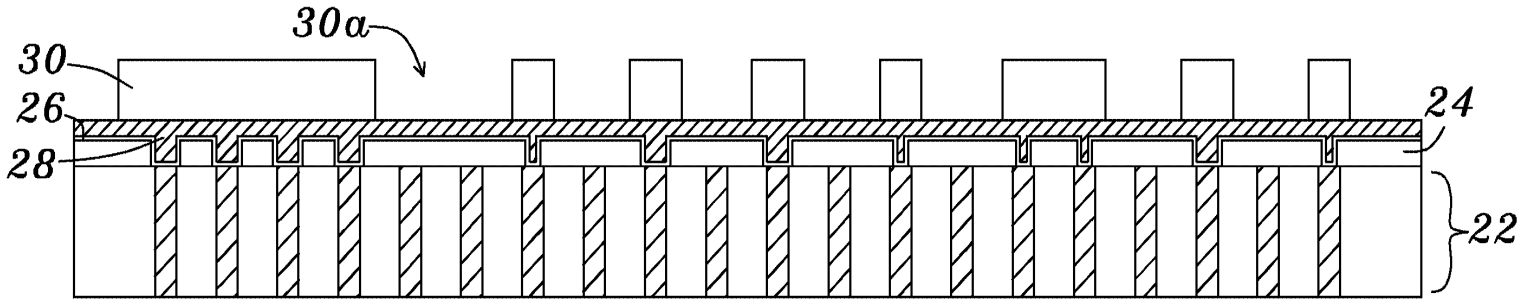


Fig. 9e

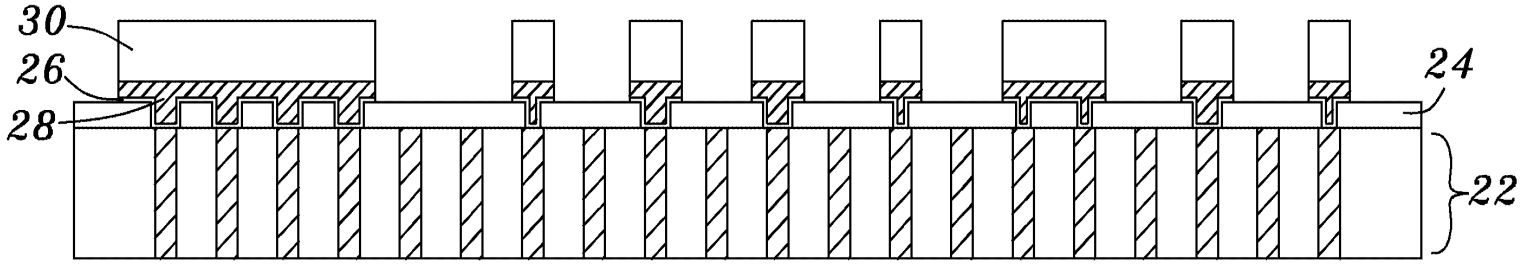


Fig. 9f

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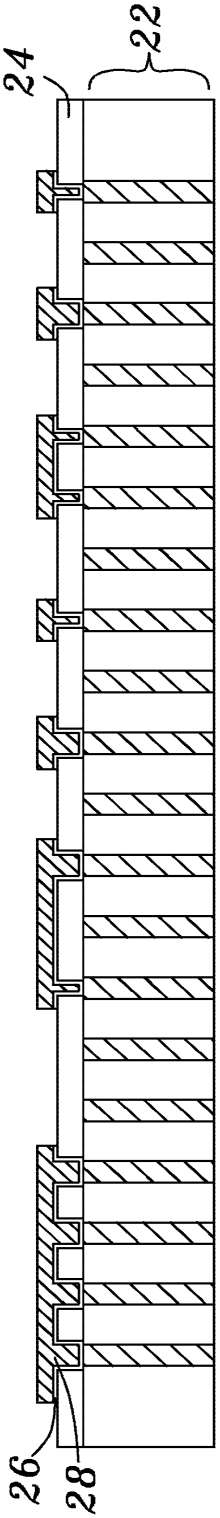


Fig. 9g

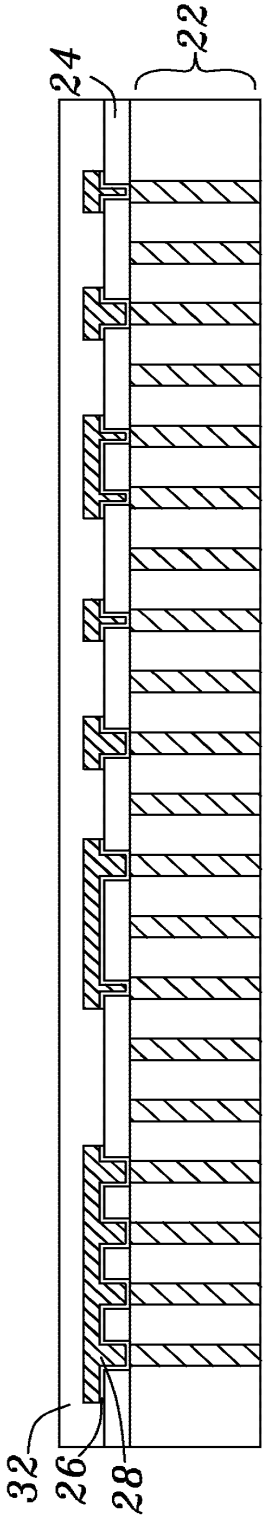


Fig. 9h

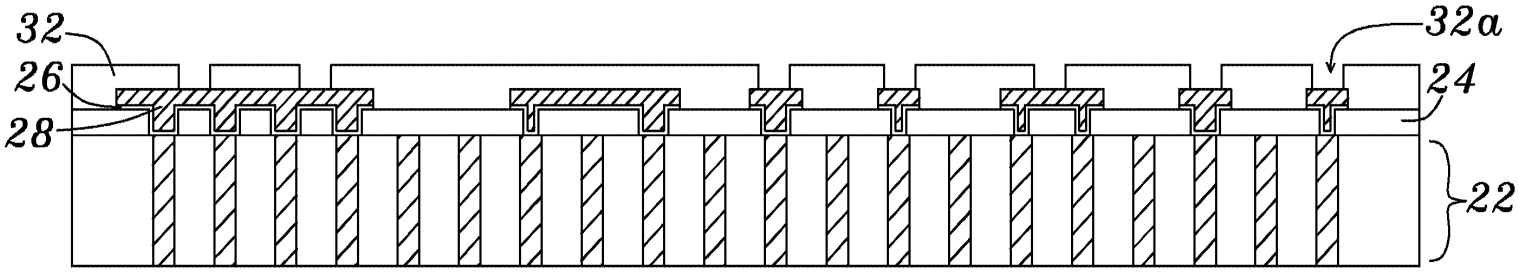


Fig. 9i

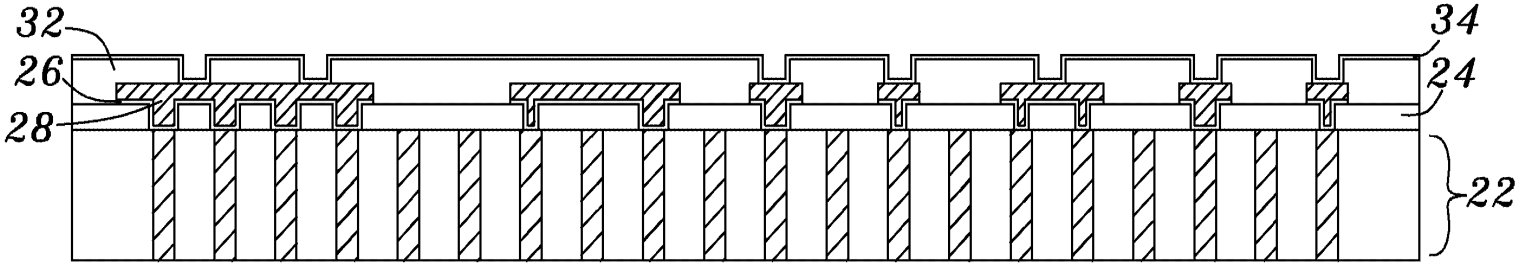


Fig. 9j

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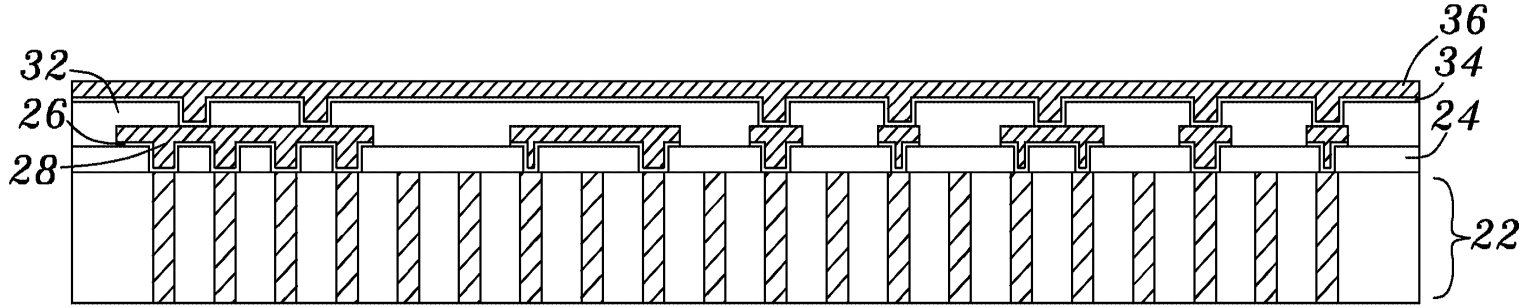


Fig. 9k

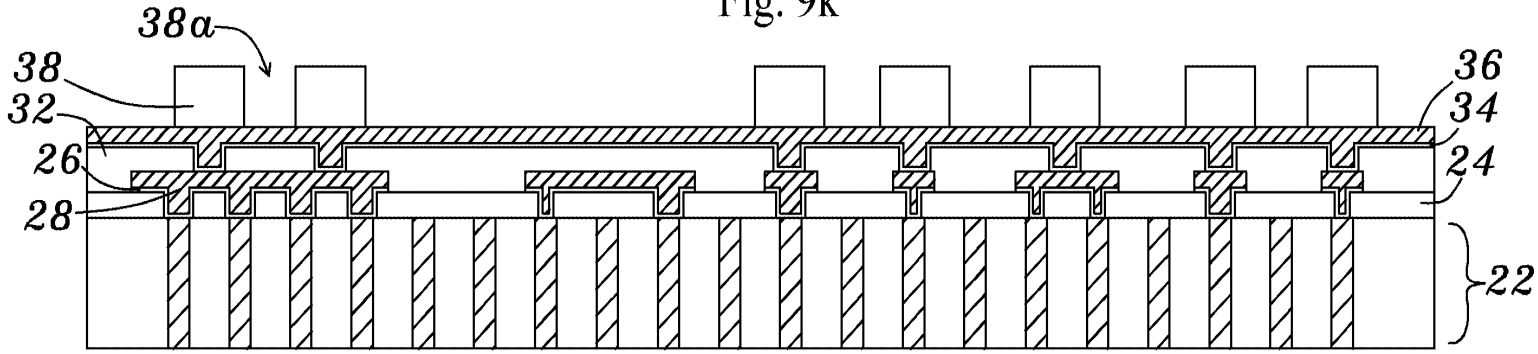


Fig. 9l

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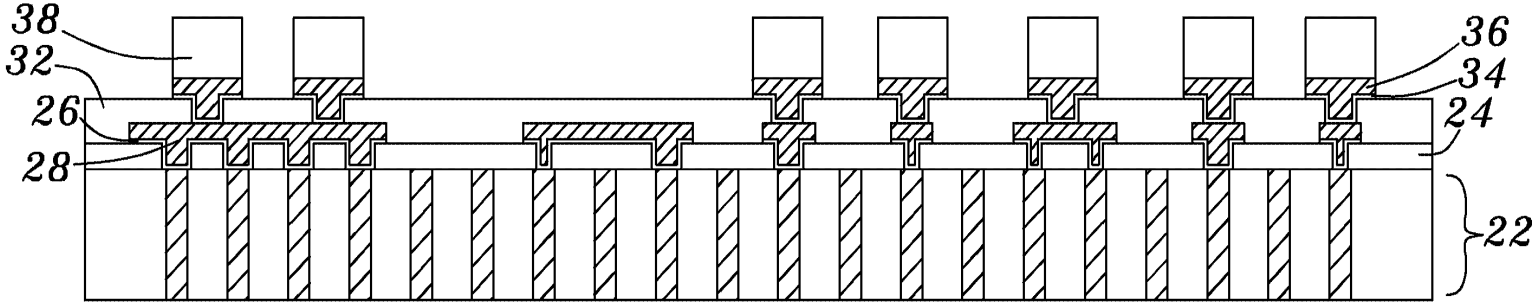


Fig. 9m

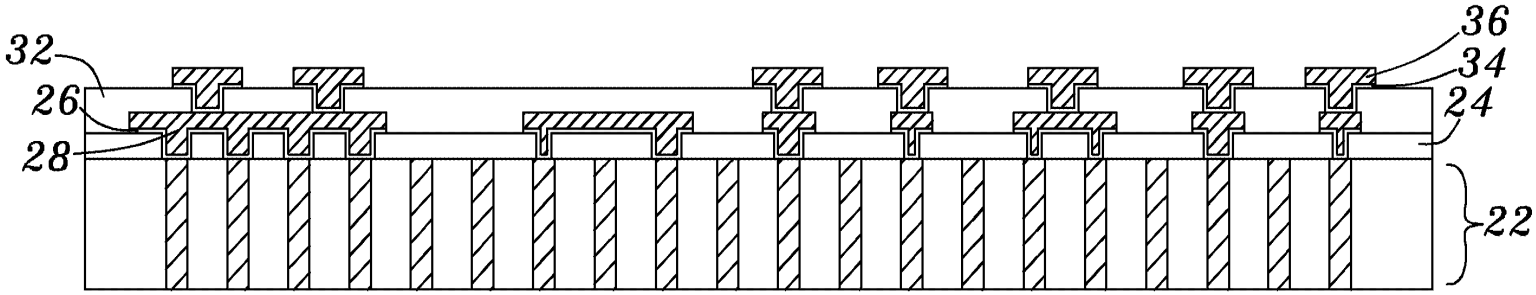


Fig. 9n

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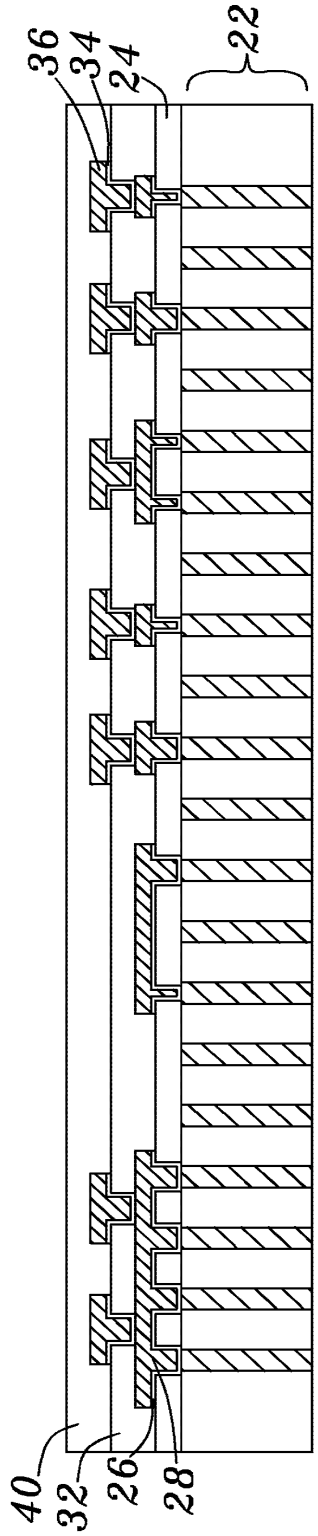


Fig. 9o

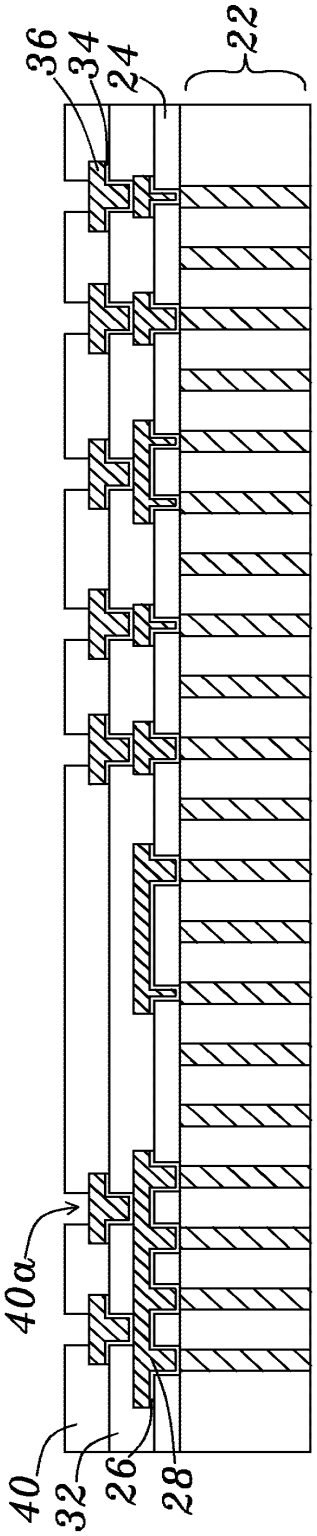


Fig. 9p

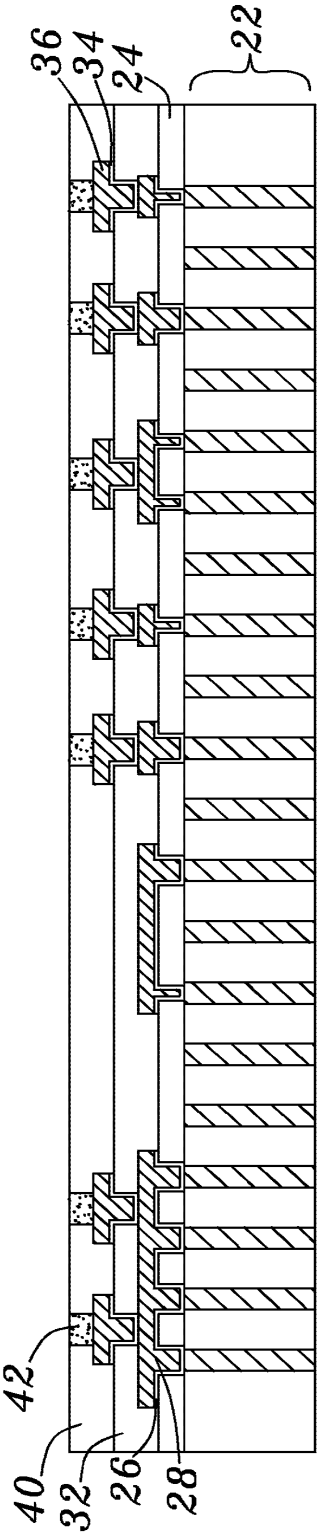

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Fig. 9q

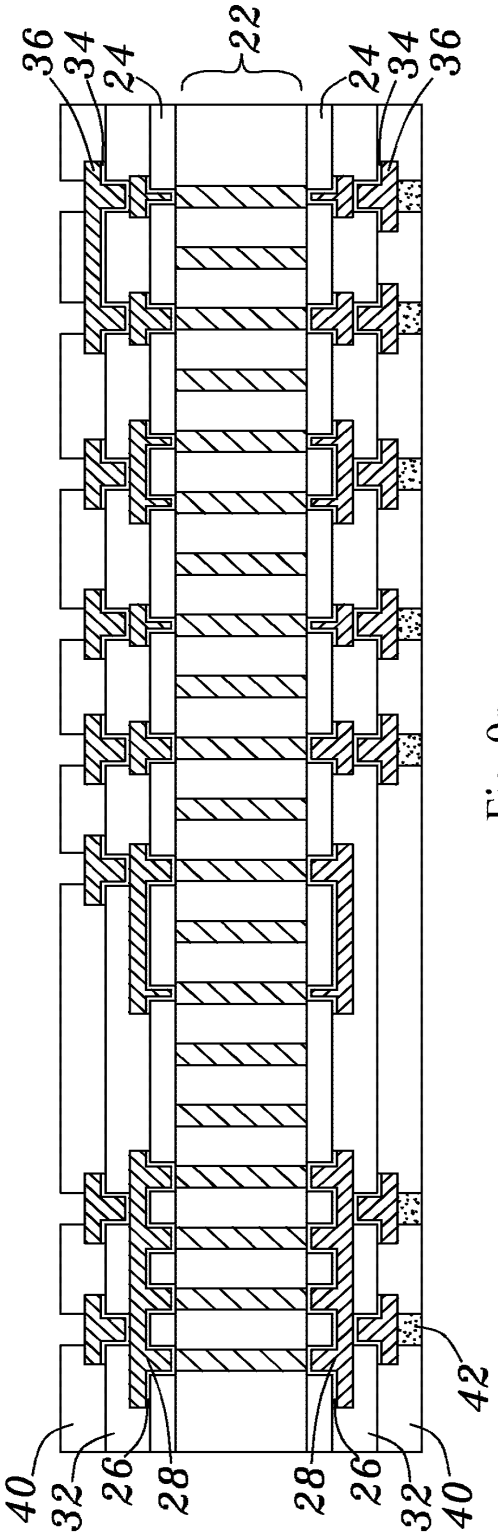

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Fig. 9r

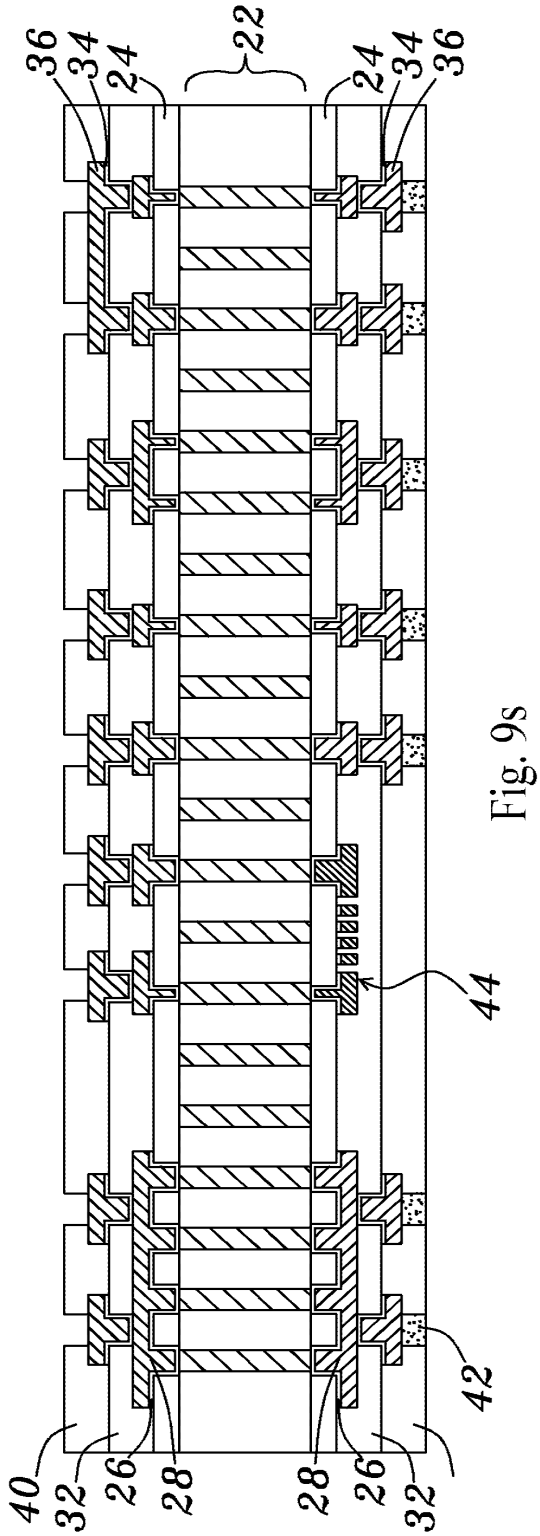


Fig. 9s

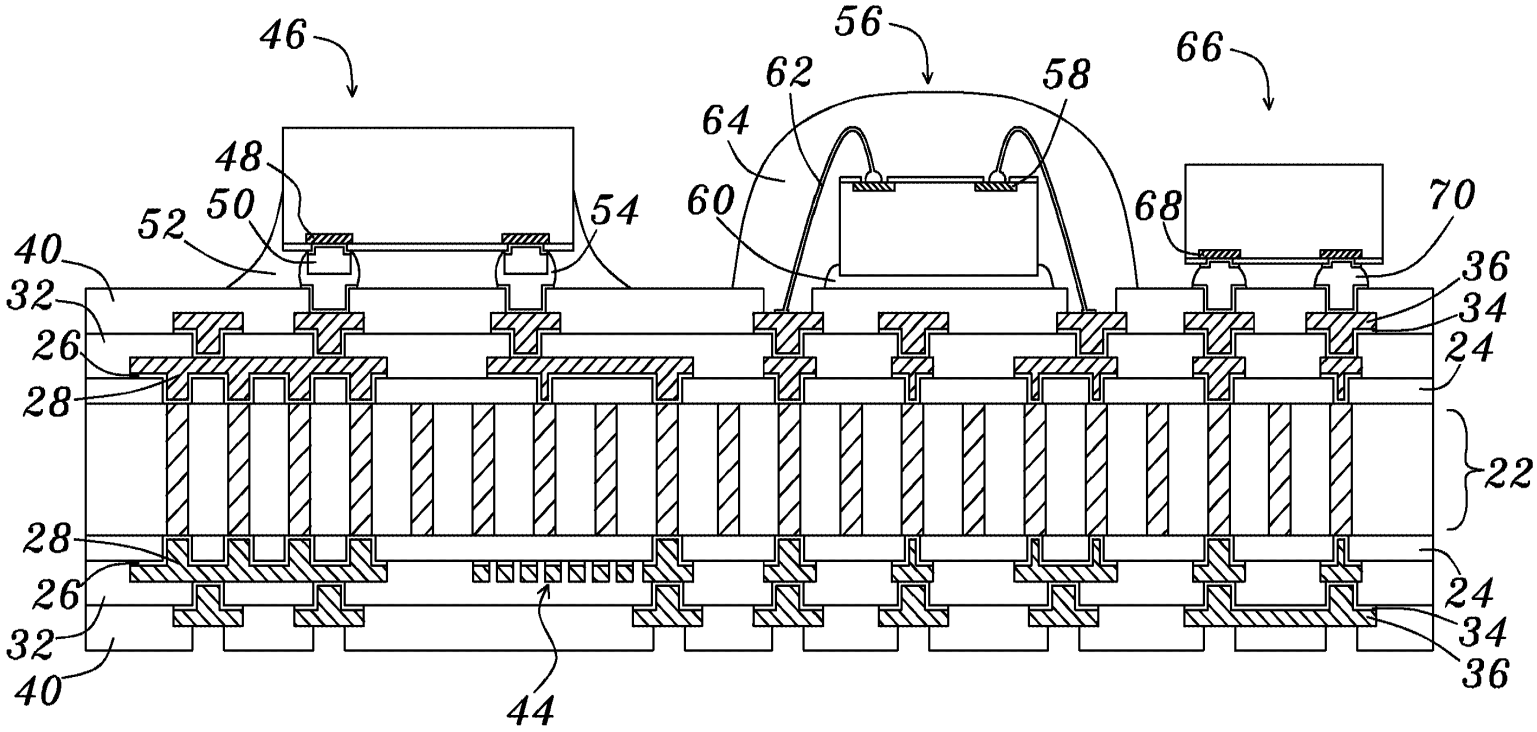


Fig. 9t

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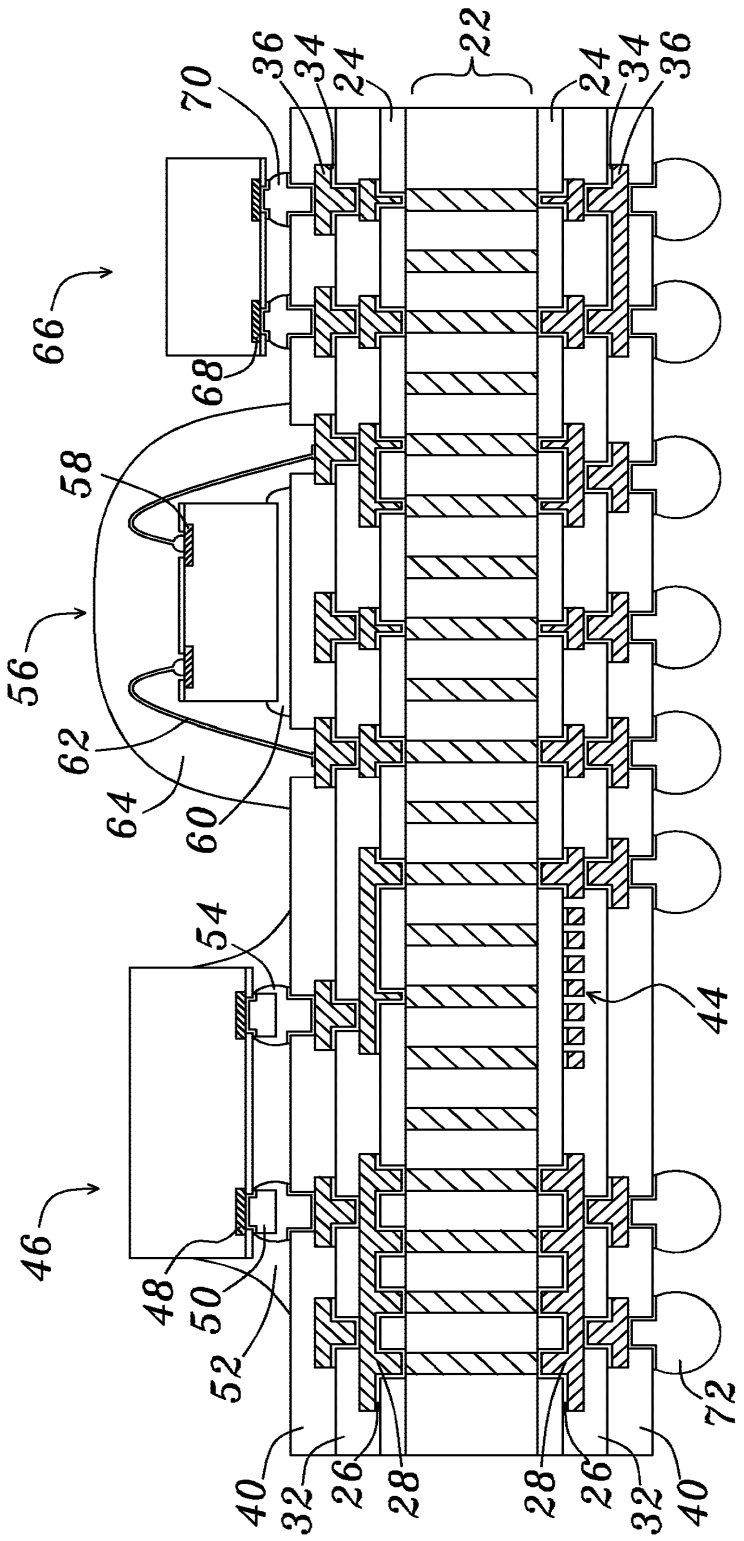

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Fig. 9u

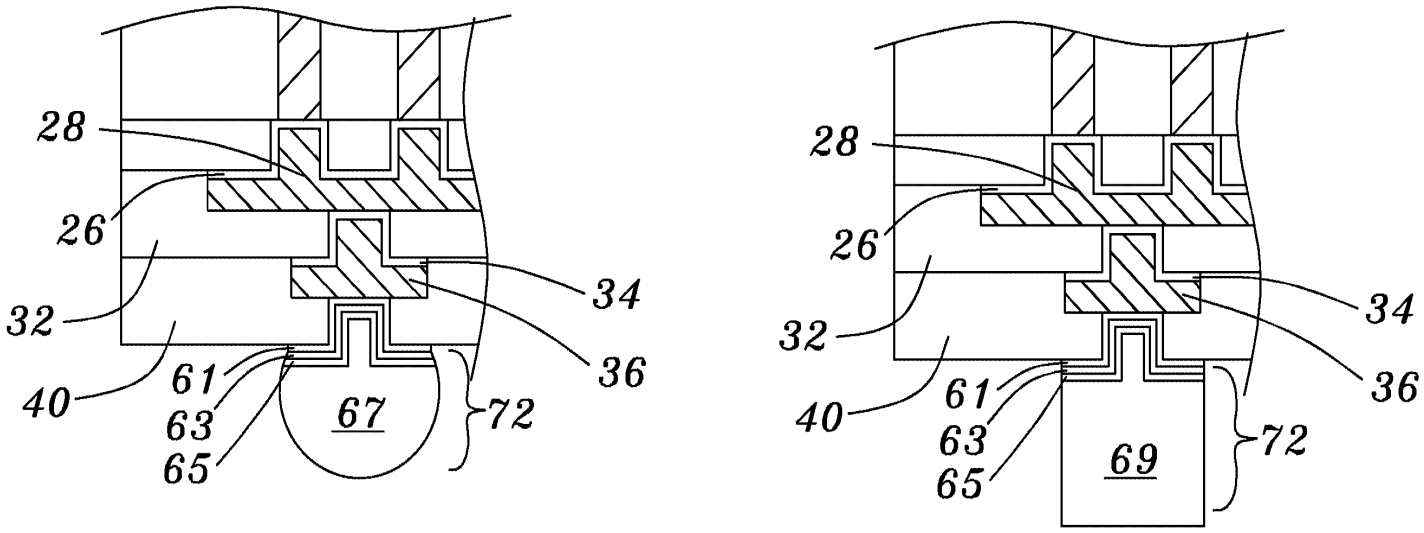


Fig. 9v

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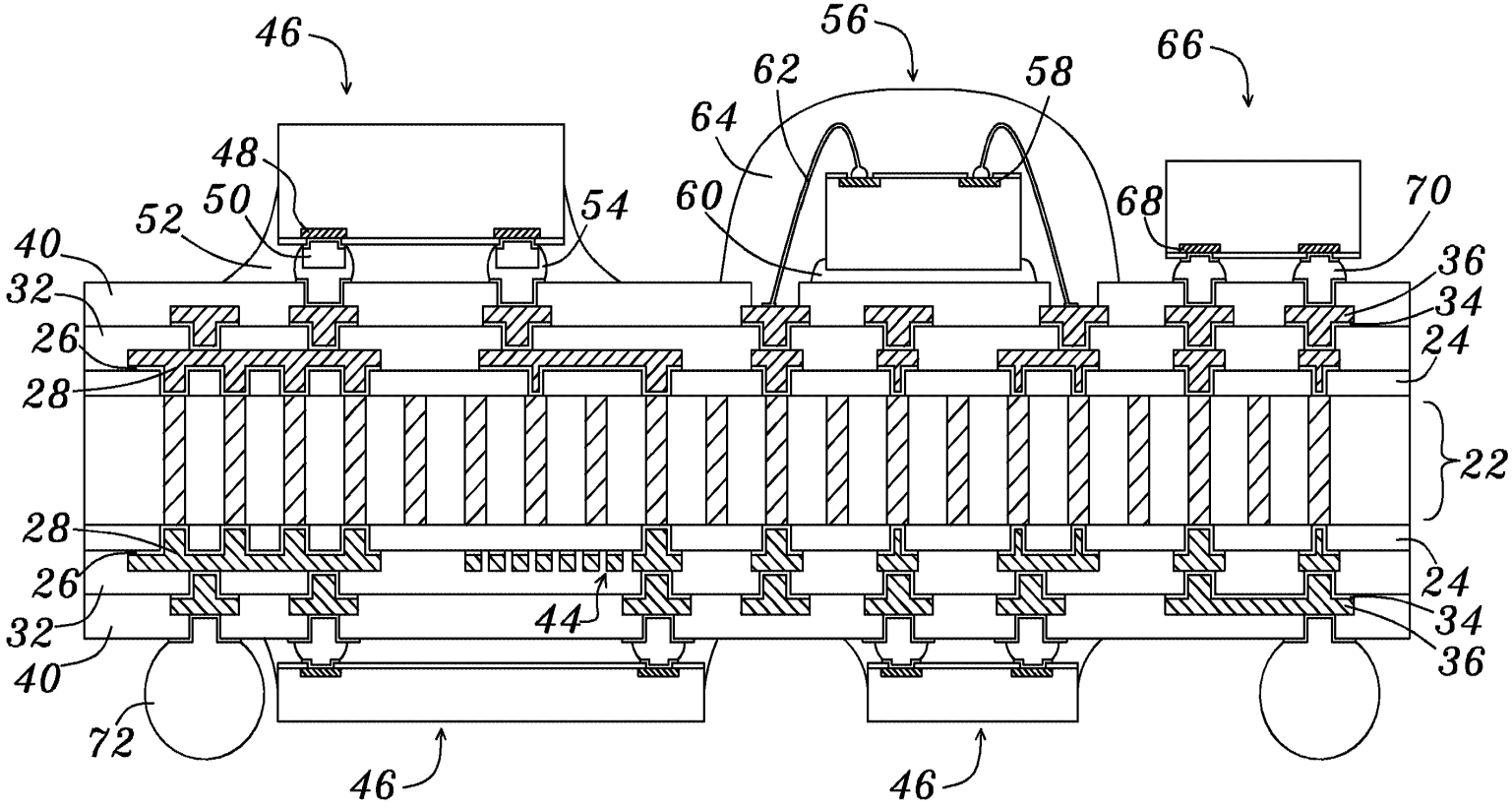


Fig. 9w

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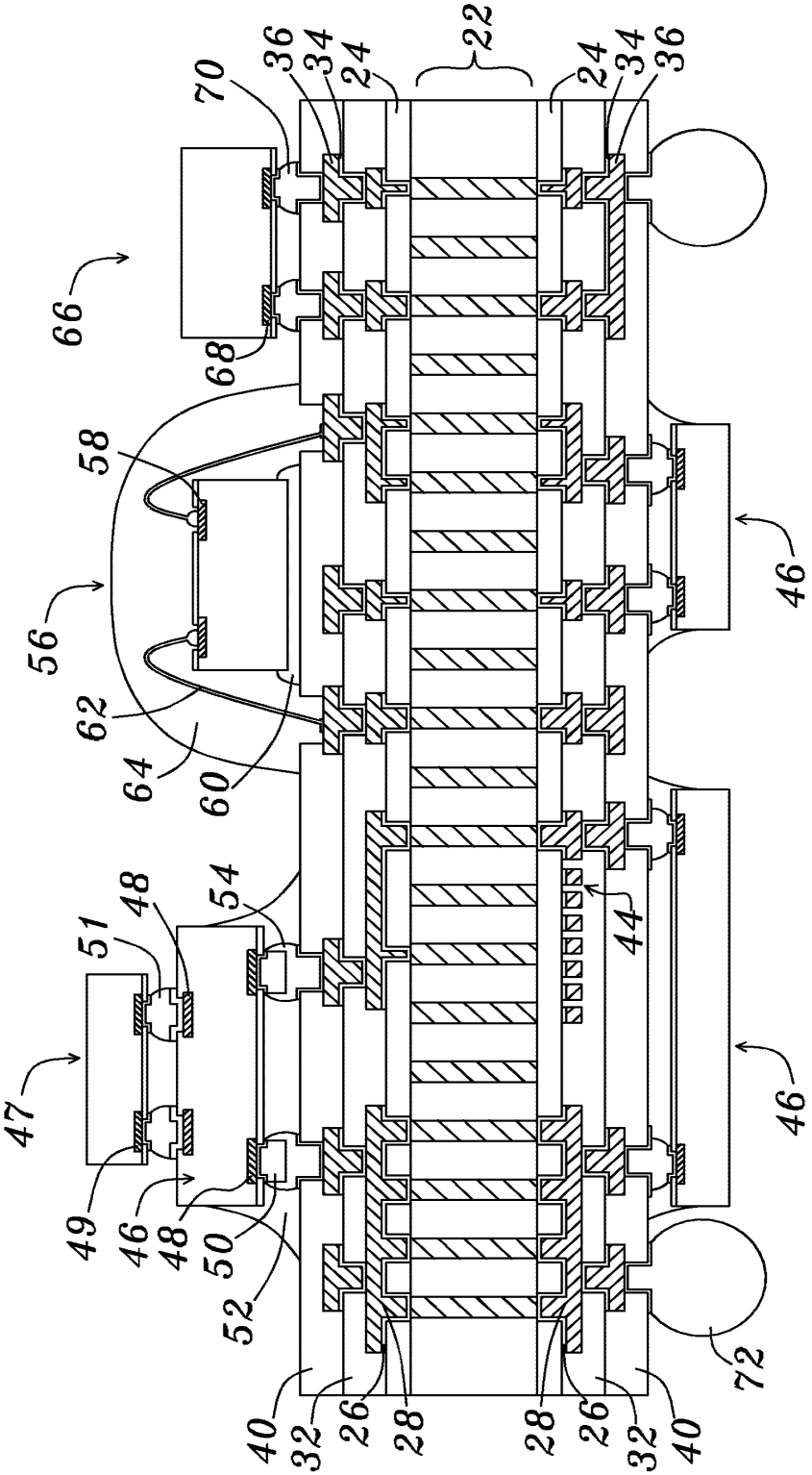

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Fig. 9x

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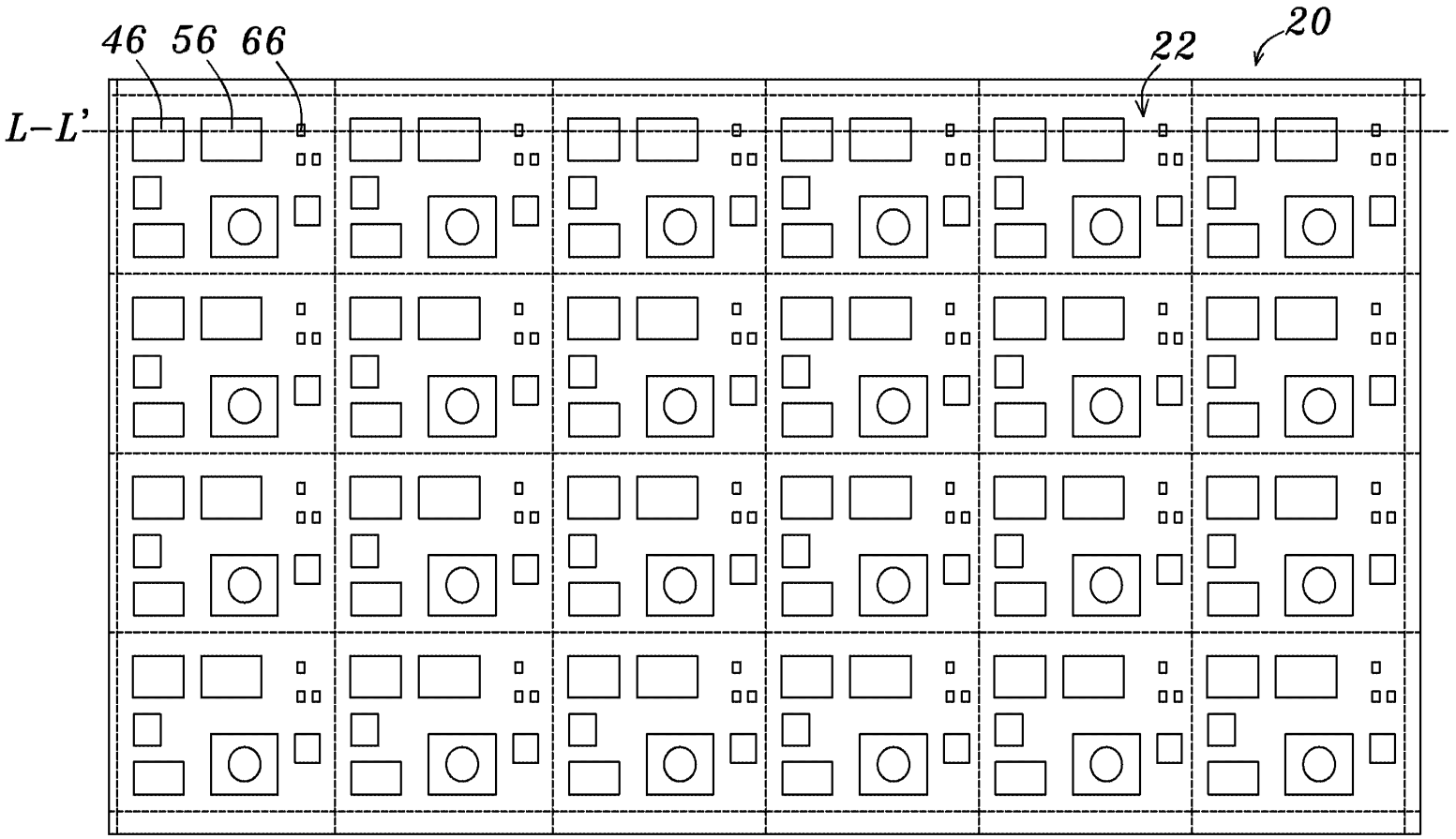


Fig. 9y

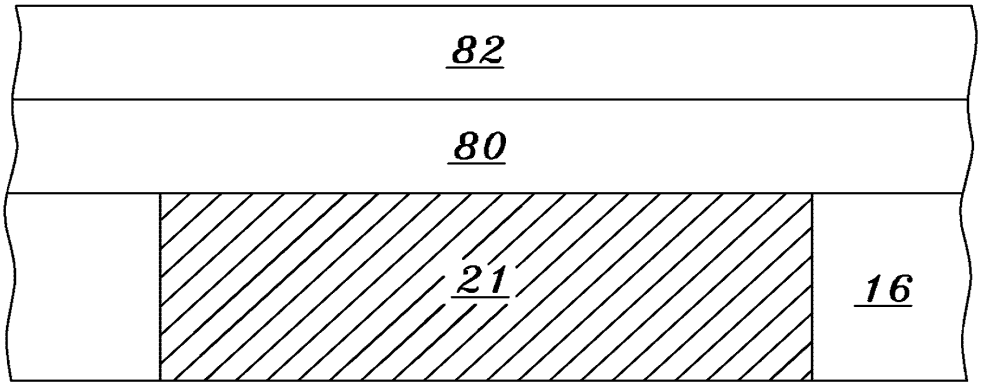


Fig. 10a

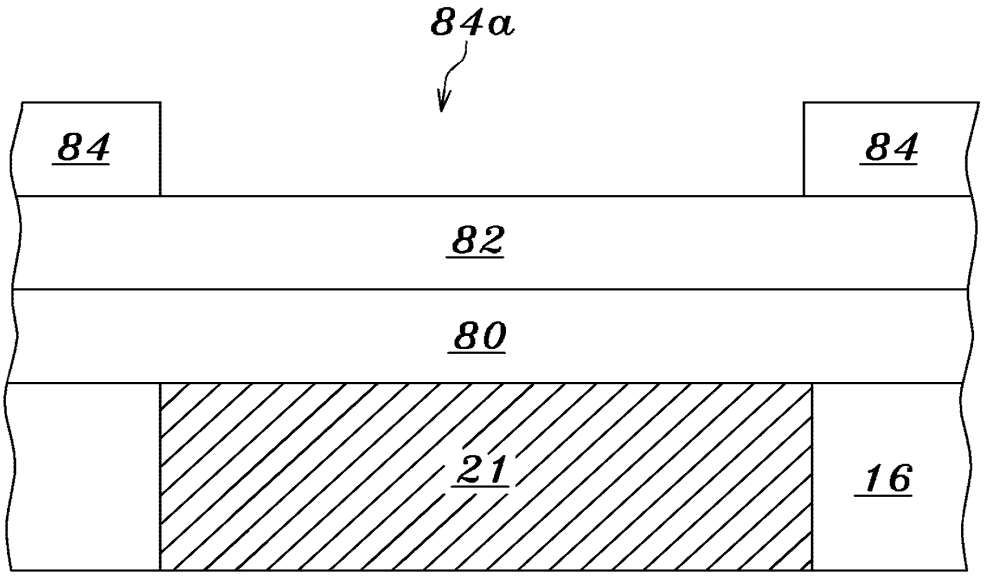


Fig. 10b

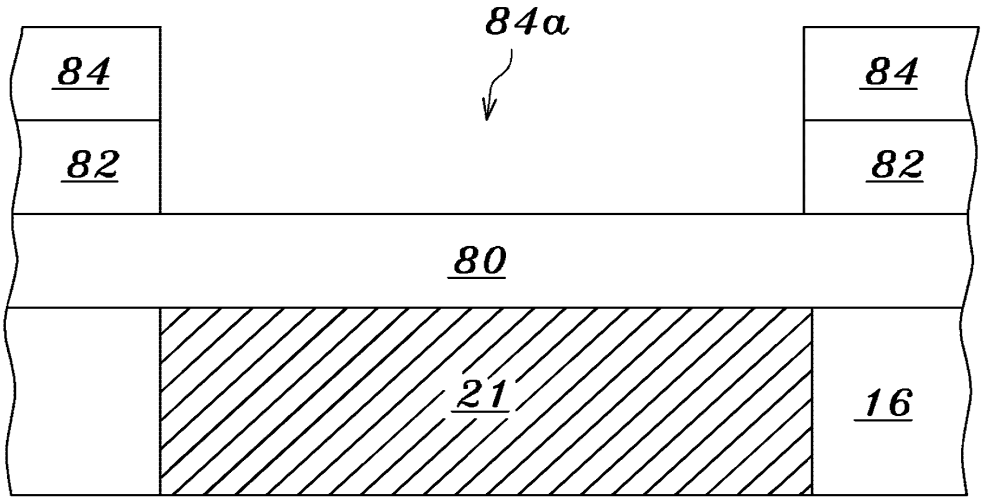


Fig. 10c

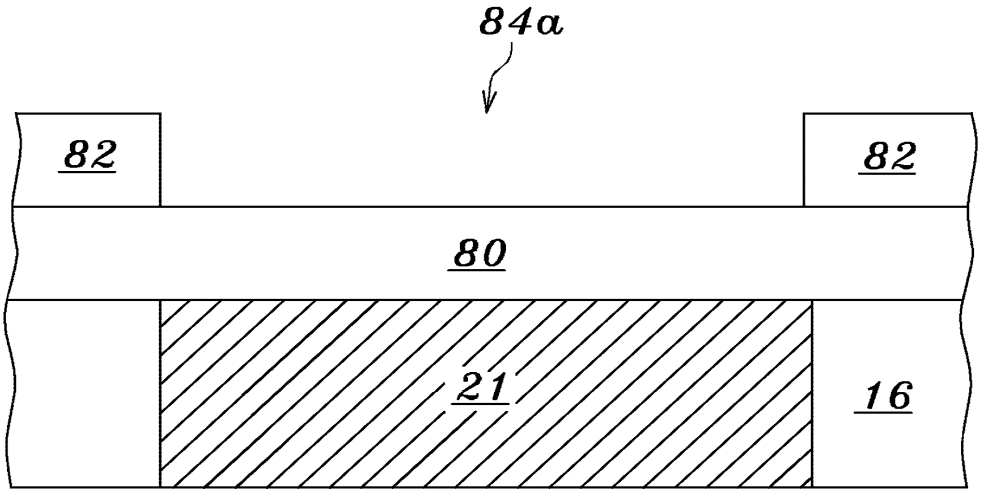


Fig. 10d

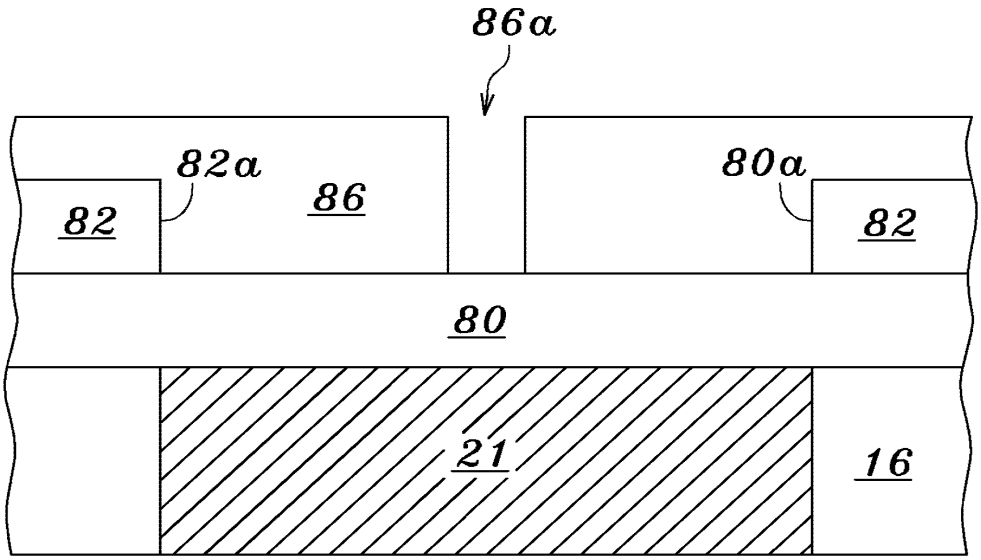


Fig. 10e

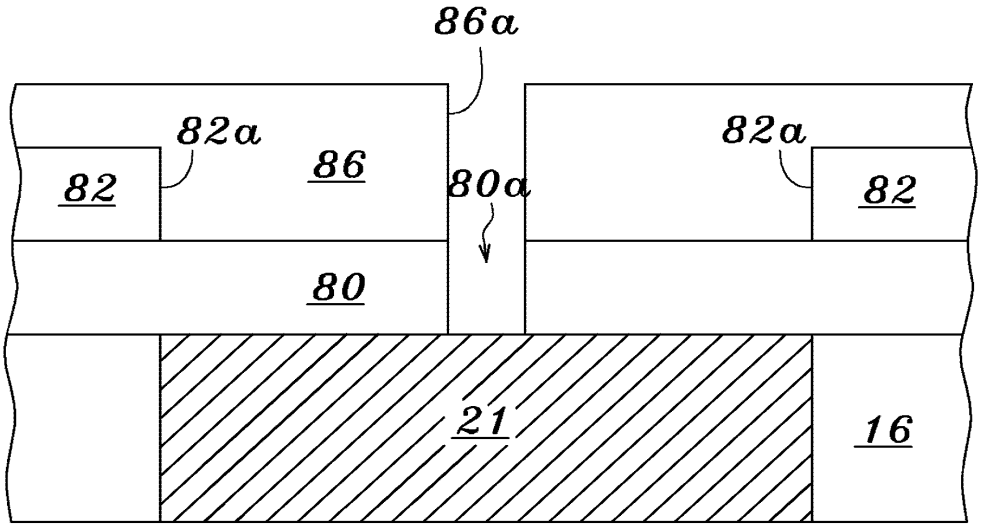


Fig. 10f

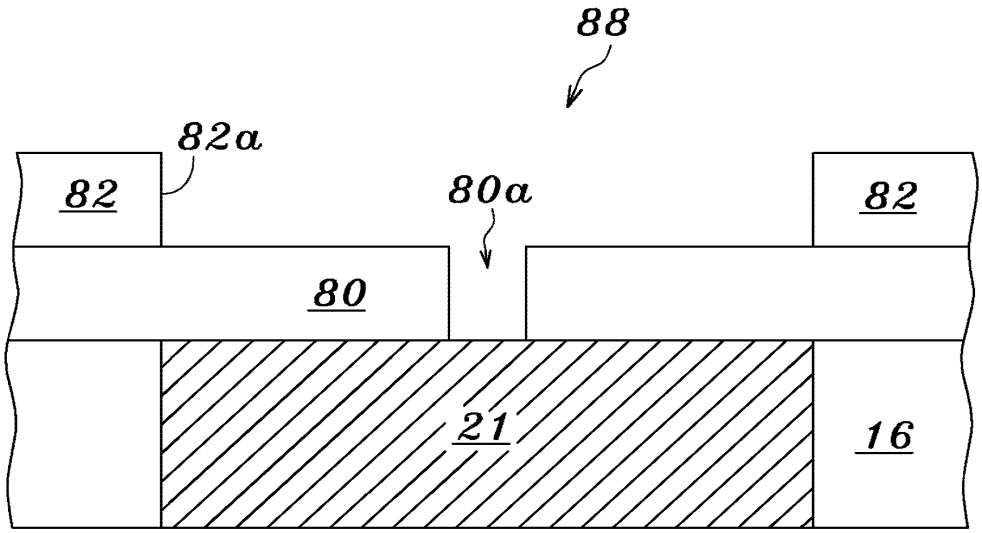


Fig. 10g

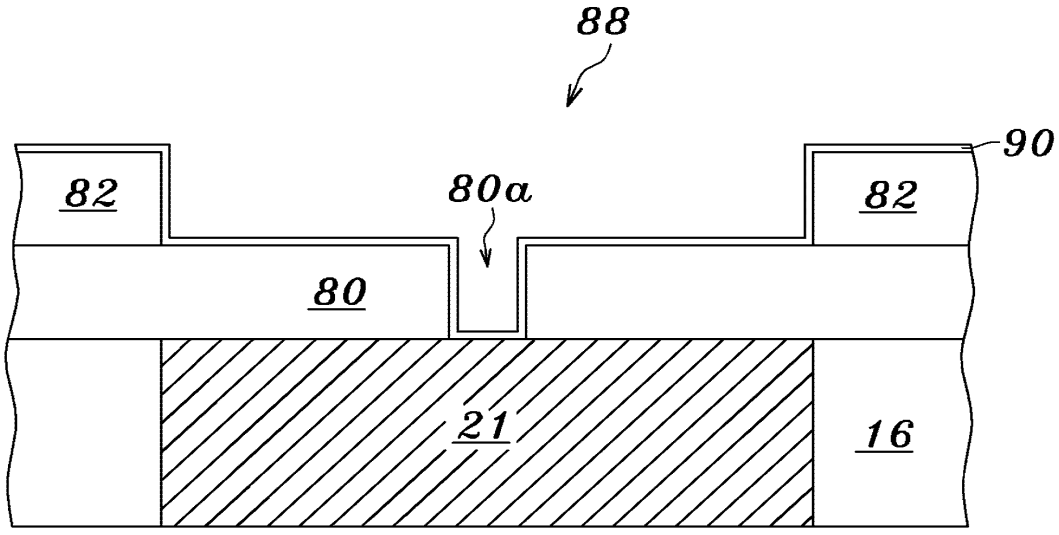


Fig. 10h

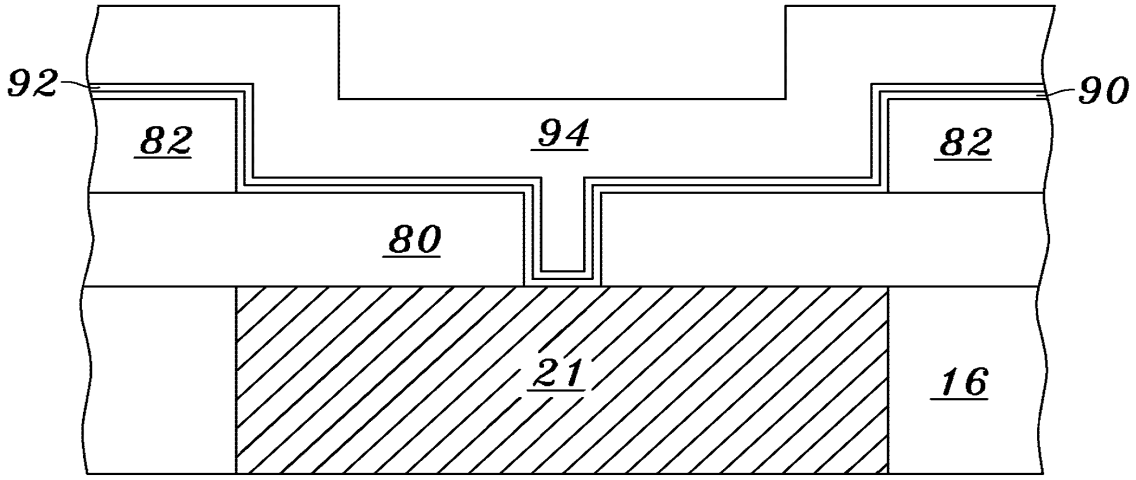


Fig. 10i

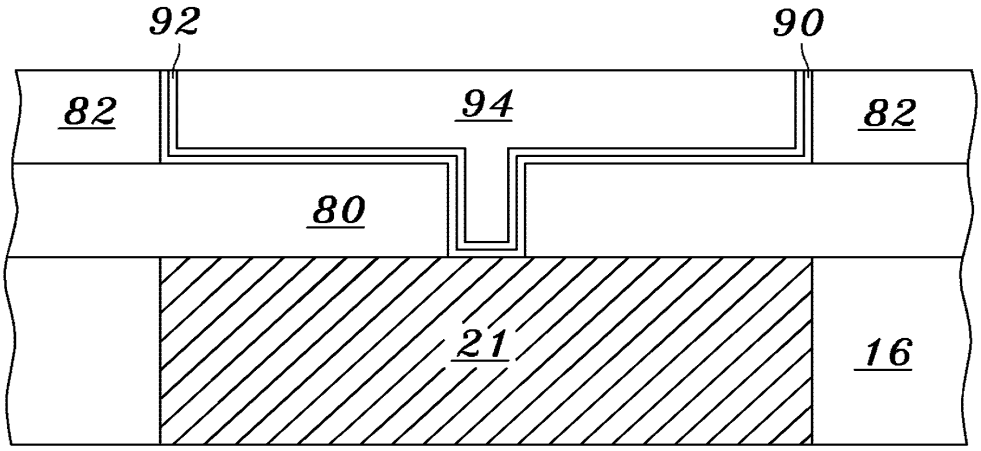


Fig. 10j

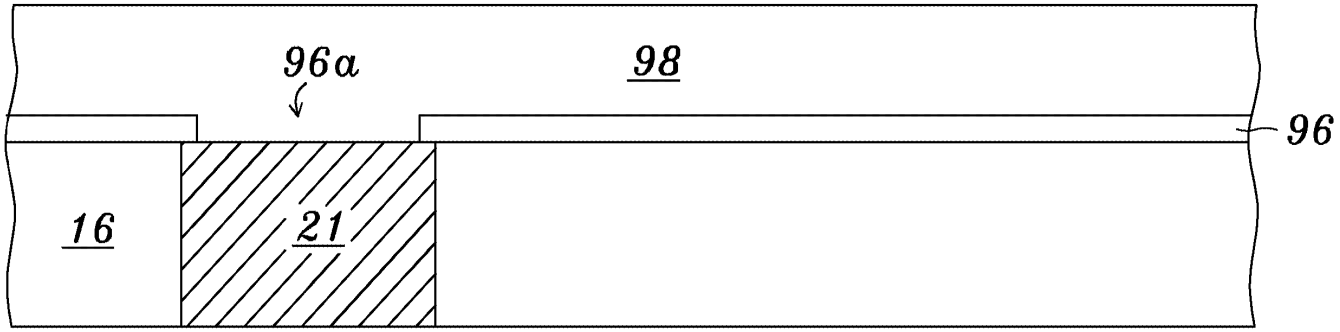


Fig. 11a

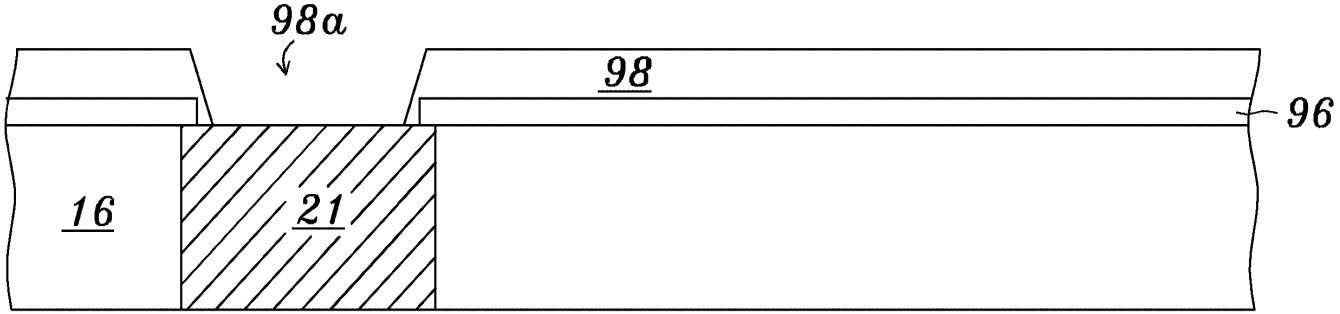


Fig. 11b

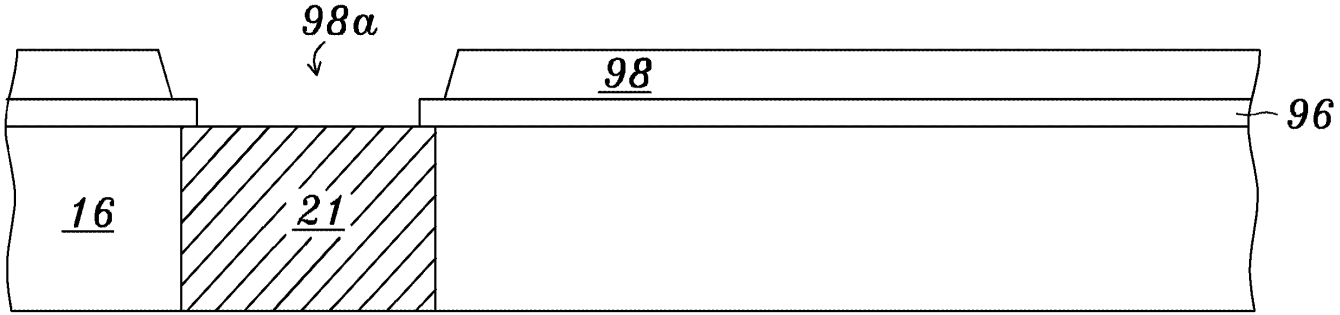


Fig. 11c

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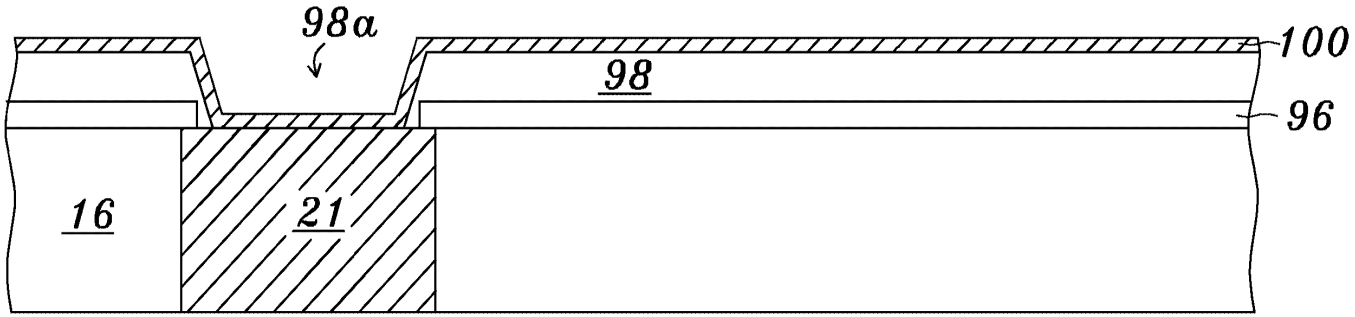


Fig. 11d

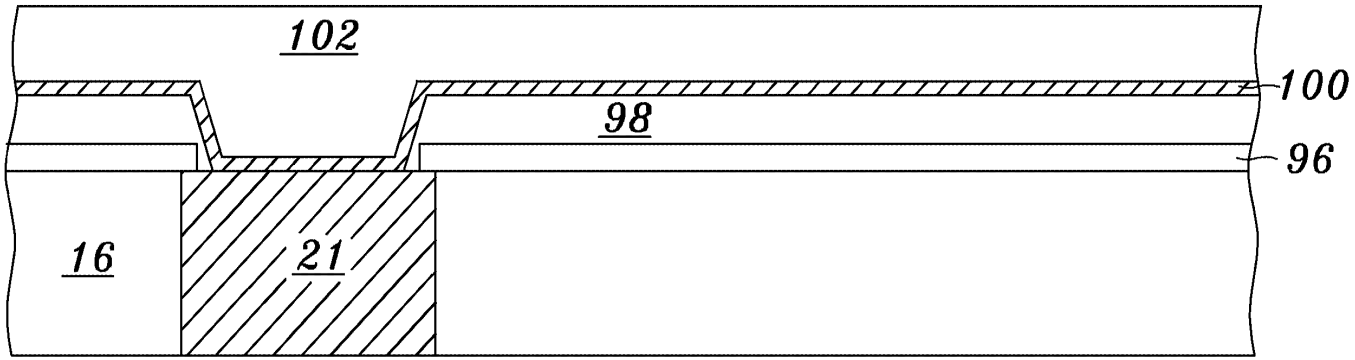


Fig. 11e

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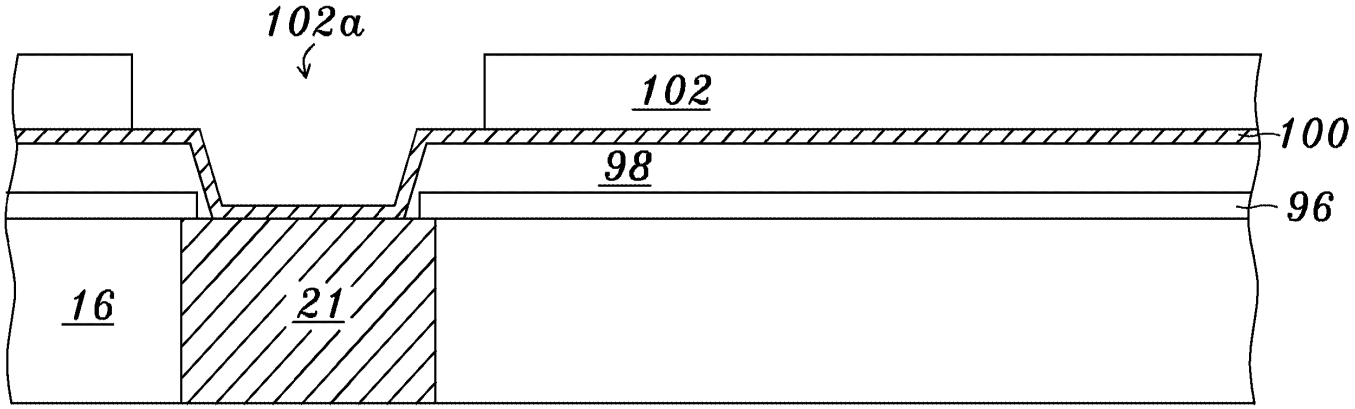


Fig. 11f

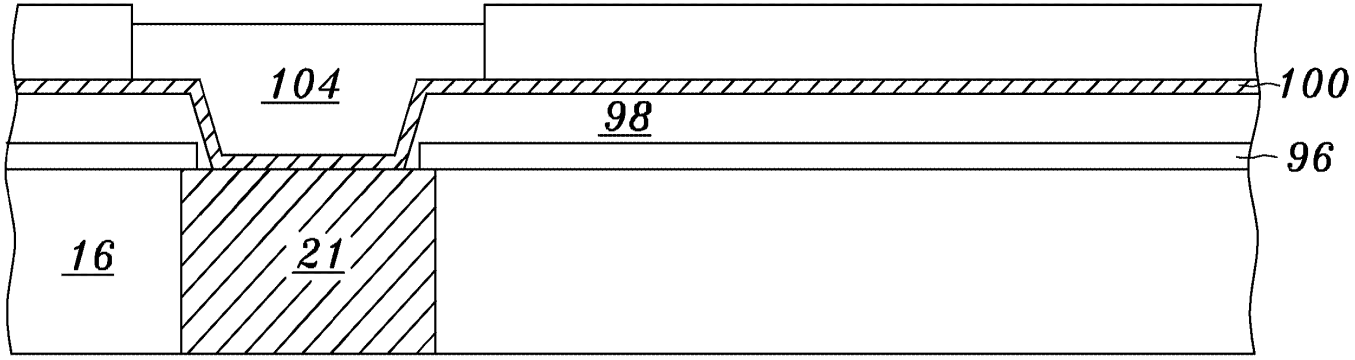


Fig. 11g

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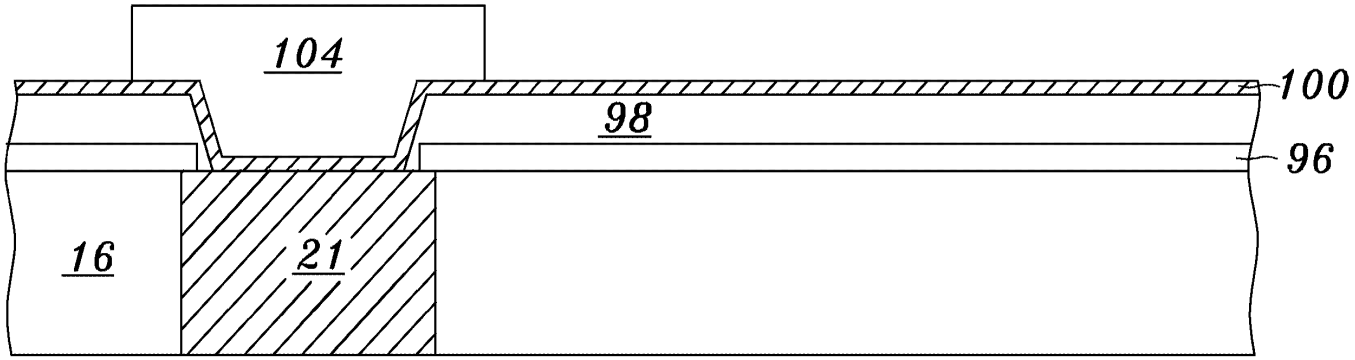


Fig. 11h

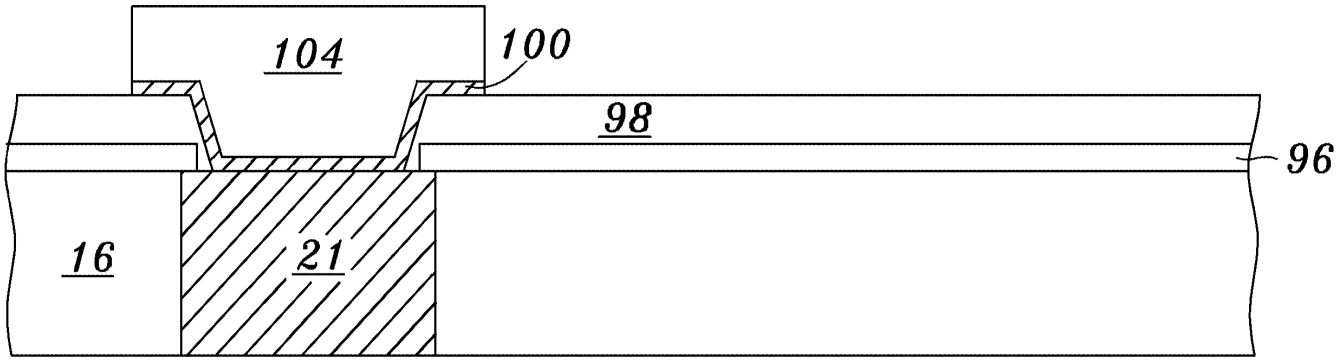


Fig. 11i

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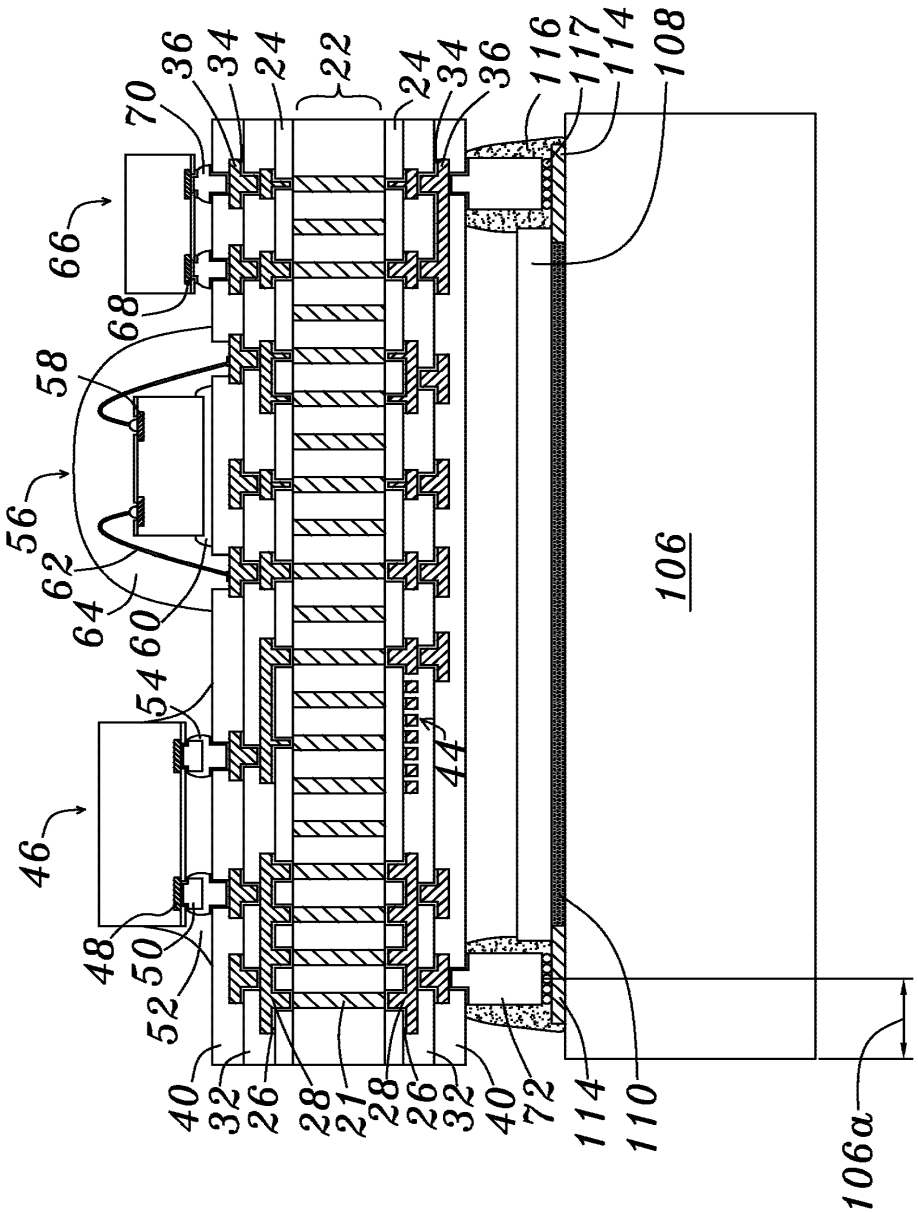

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Fig. 12

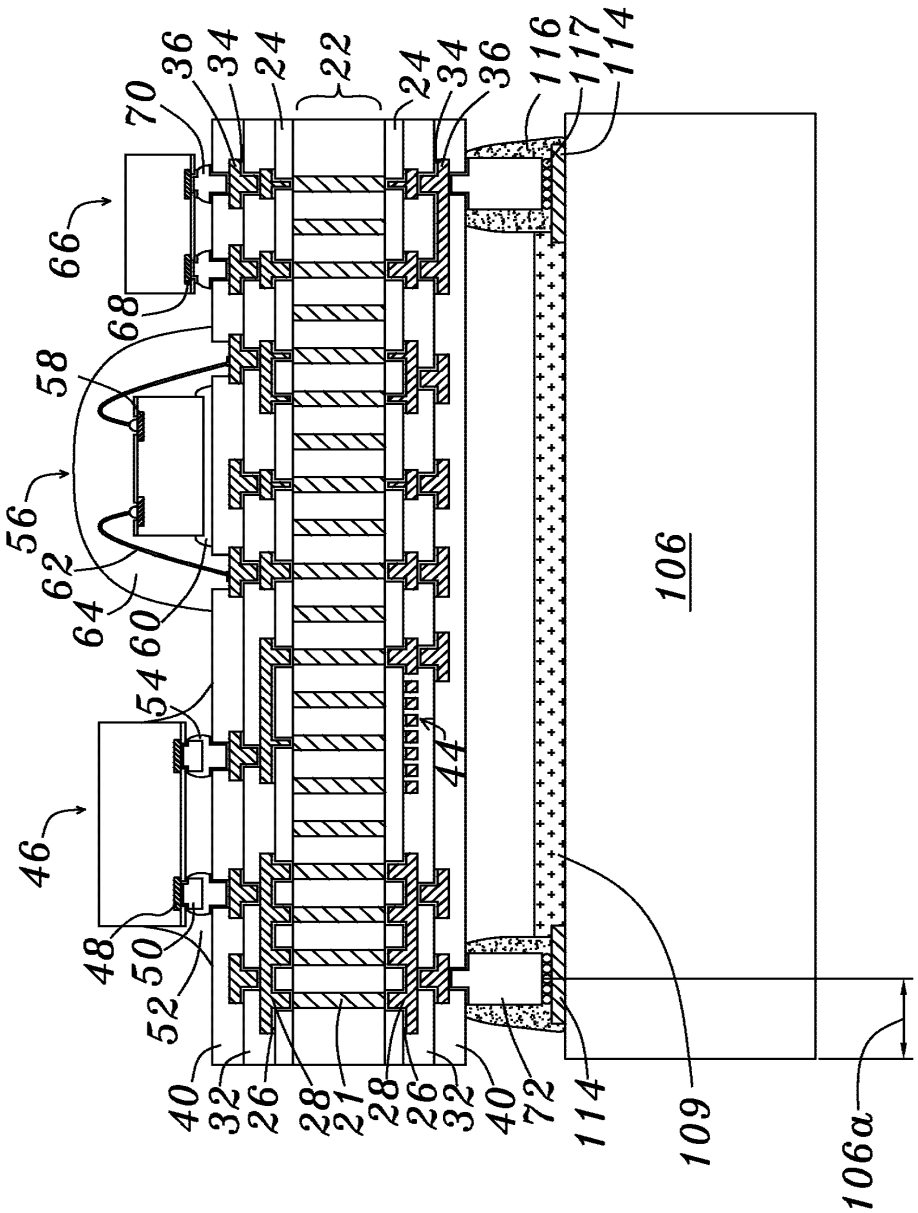

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Fig. 13

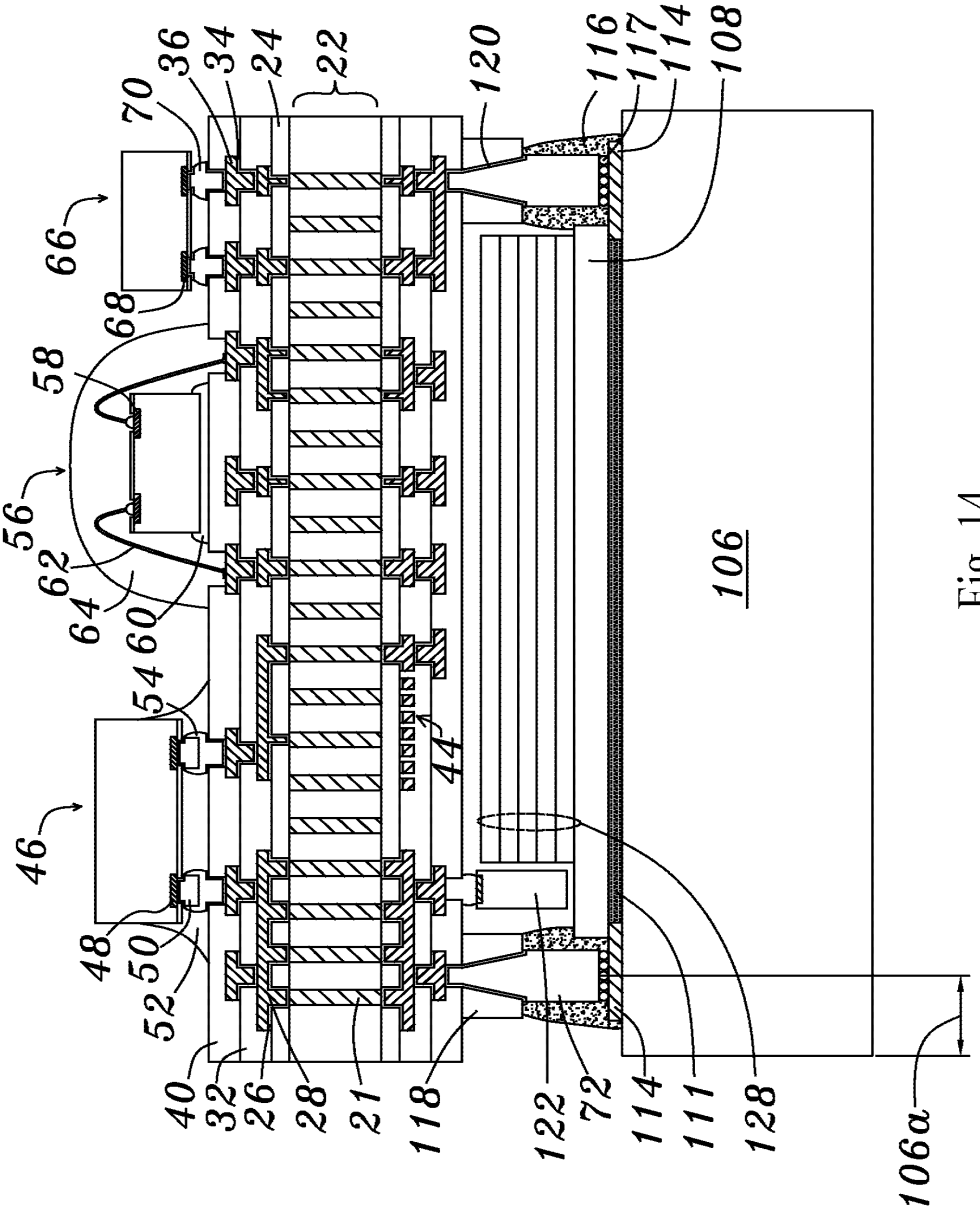

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Fig. 14

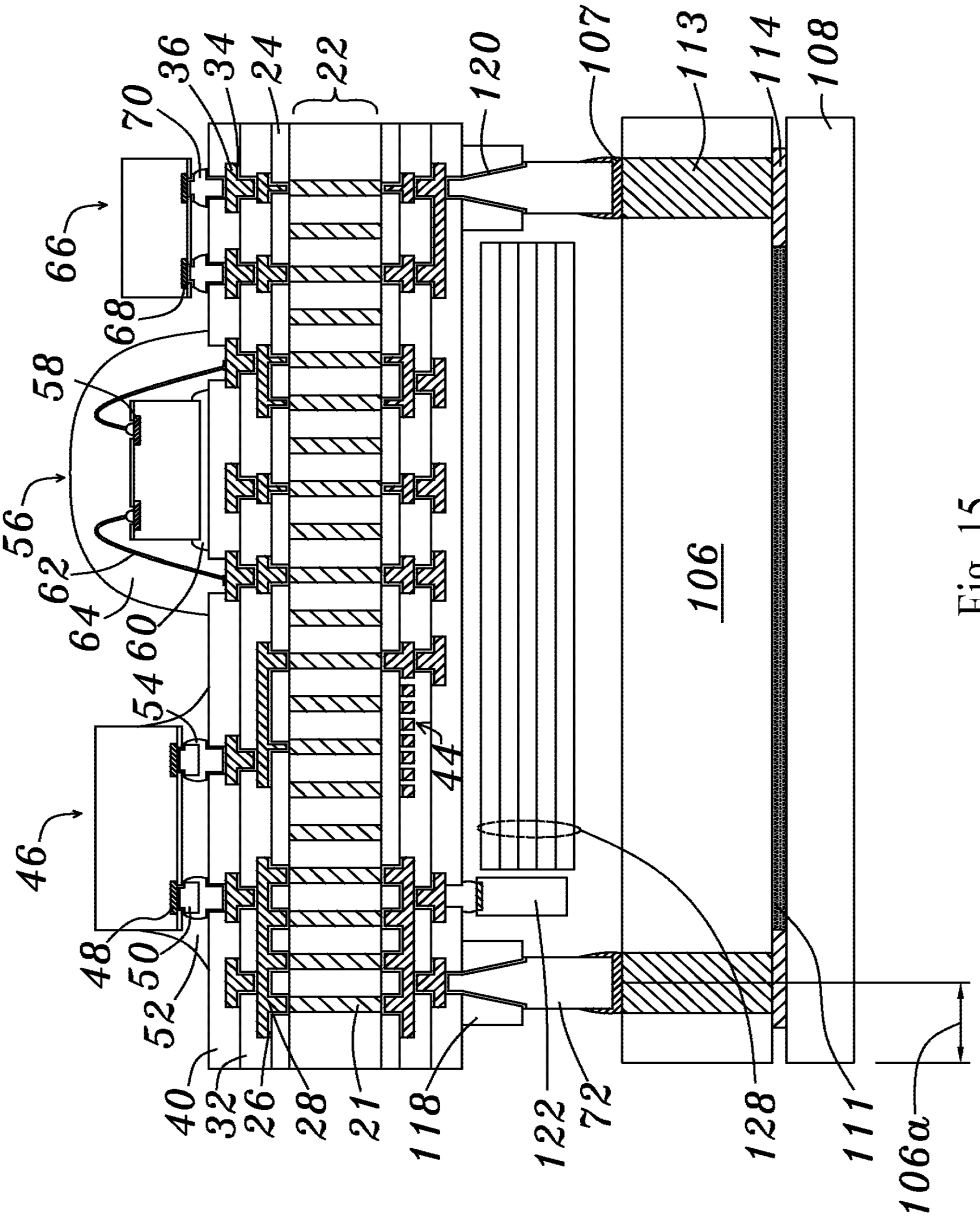

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Fig. 15

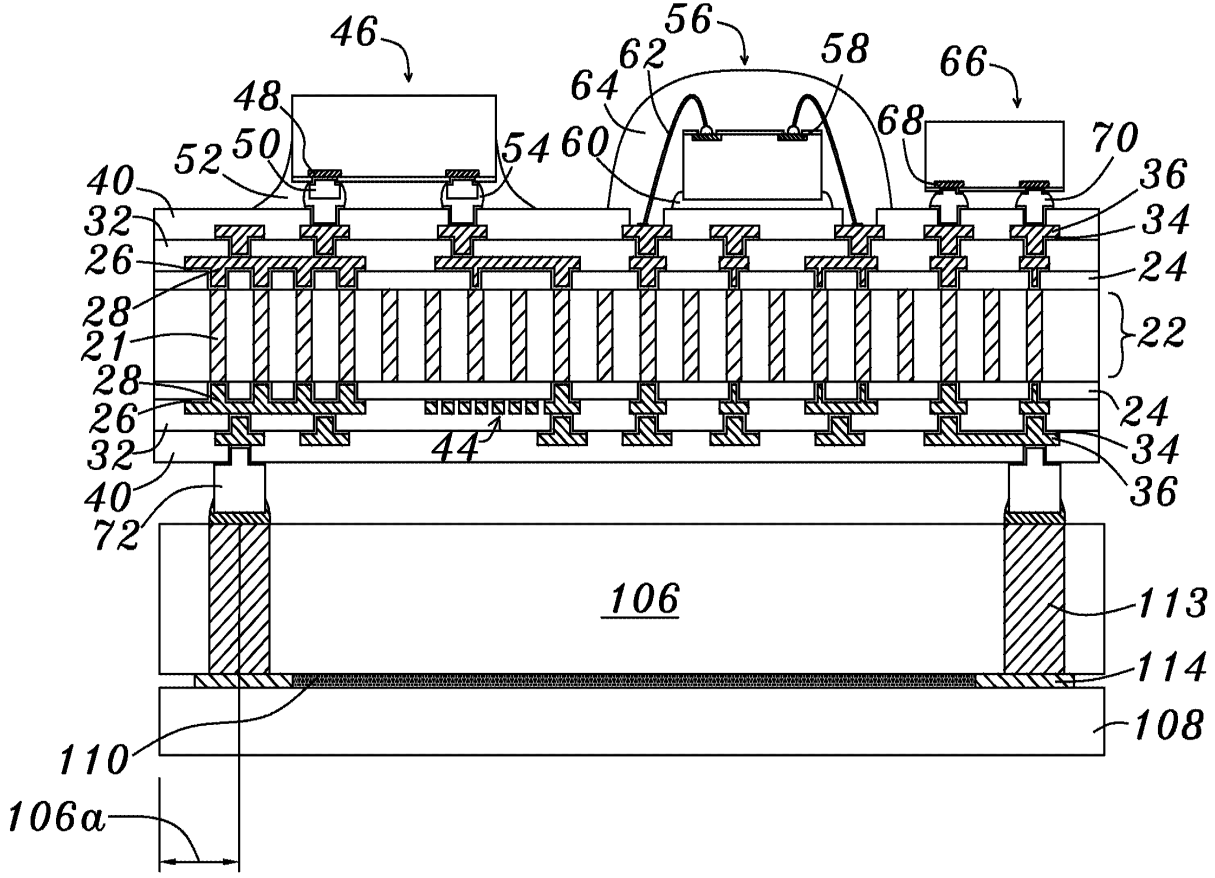


Fig. 16

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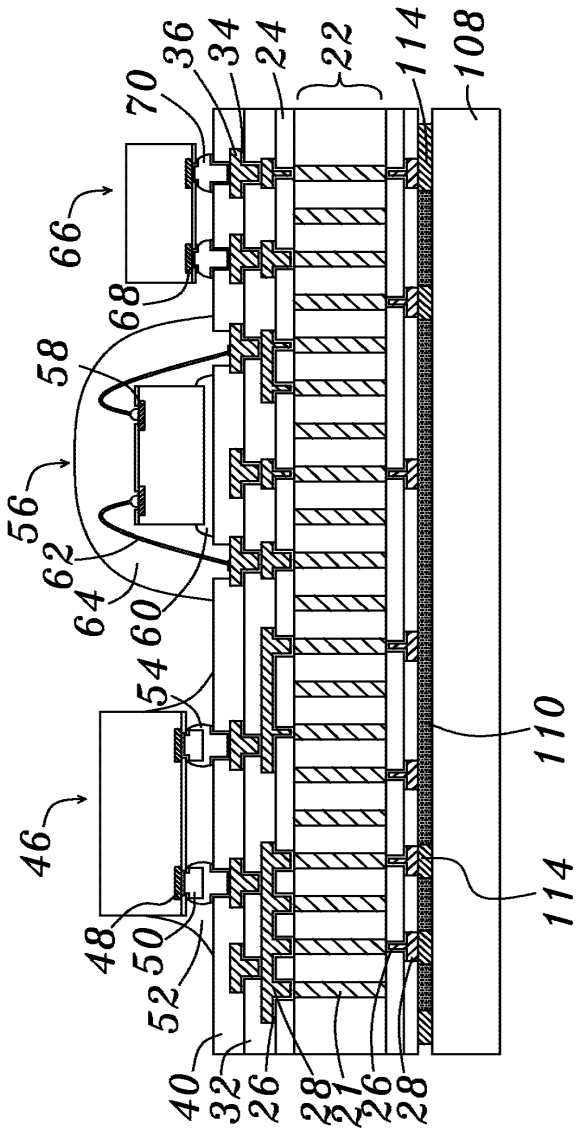

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Fig. 17a

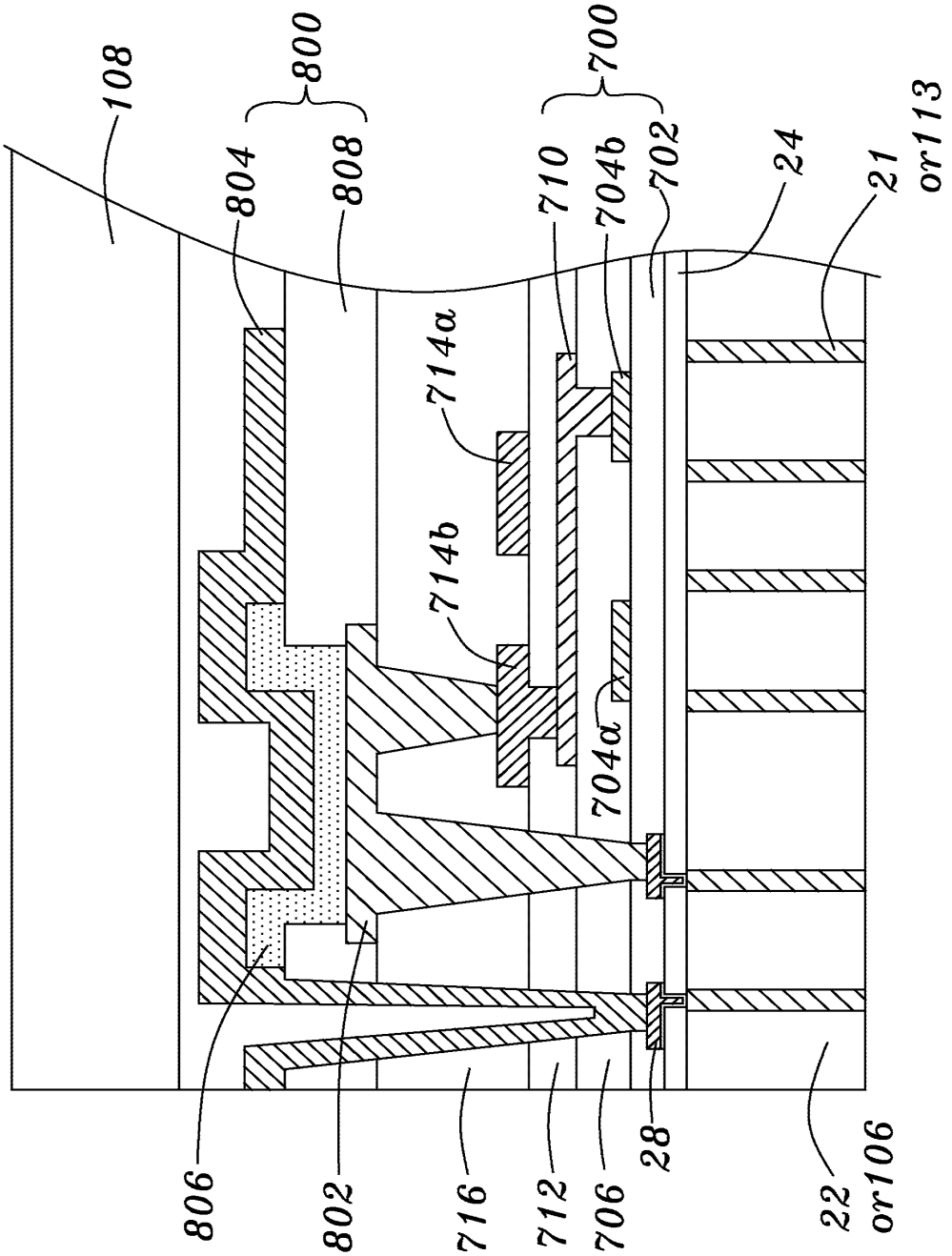

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Fig. 17b

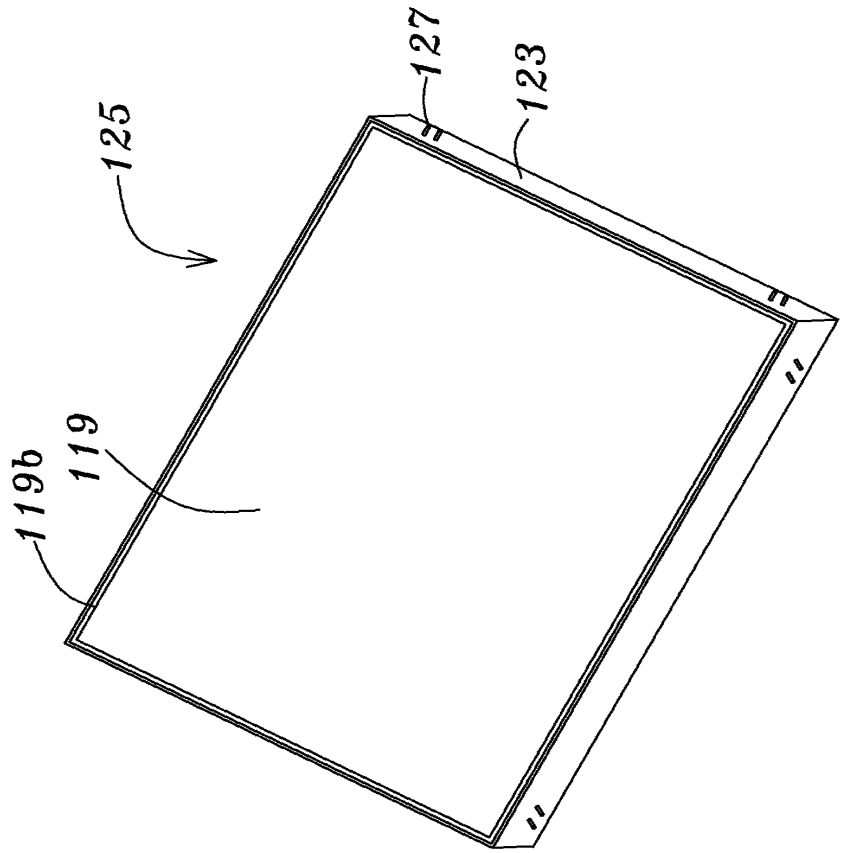


Fig. 18

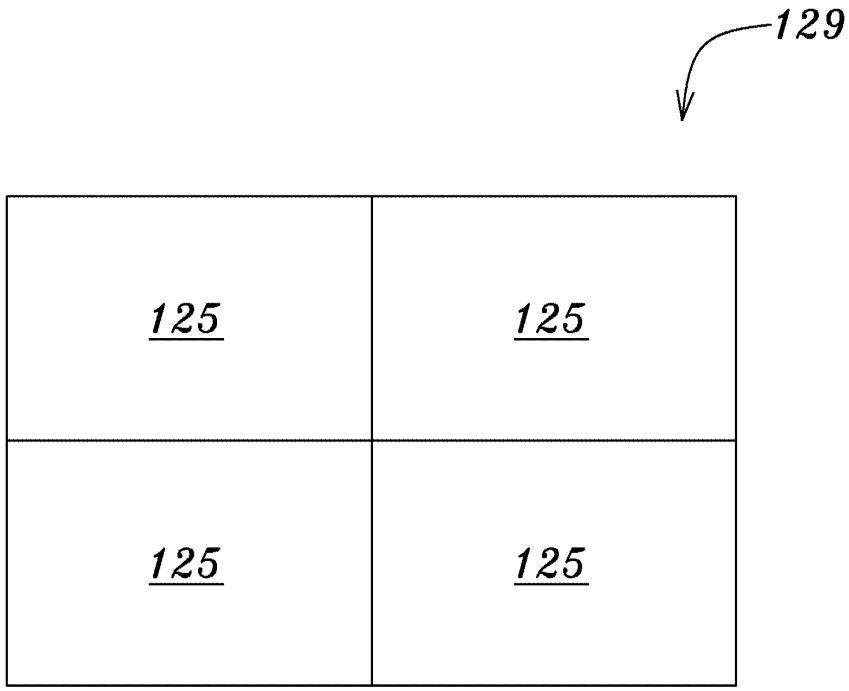


Fig. 19

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DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of Invention	METHOD FOR FABRICATING GLASS SUBSTRATE PACKAGE

As the below named inventor, I hereby declare that:

This declaration is directed to:

- [■] The attached application, or
- [ ] United States application or PCT international application number _____

filed on _____.

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

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LEGAL NAME OF INVENTOR

Inventor: Ping-Jung Yang Date (Optional): 2016-09-11

Signature: /Ping-Jung Yang/

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form or must have been previously filed. Use an additional PTO/AIA/01 form for each additional inventor.

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2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	Mars16-001-US-C01
	Application Number	
Title of Invention	METHOD FOR FABRICATING GLASS SUBSTRATE PACKAGE	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor 1 — Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
Mr.	Ping-Jung		Yang	

Residence Information (Select One) US Residency ● Non US Residency Active US Military Service

City	Hsinchu City	Country of Residence [i]	TW

Mailing Address of Inventor:

Address 1	No. 52, Ln. 97, Shengjun Rd., North Dist.		
Address 2			
City	Hsinchu city	**State/Province**	
Postal Code	300	**Country** [i]	TW

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

☐ **An Address is being provided for the correspondence Information of this application.**

Customer Number	102851		
Email Address	semars3898@gmail.com	Add Email	Remove Email

Application Information:

Title of the Invention	METHOD FOR FABRICATING GLASS SUBSTRATE PACKAGE		
Attorney Docket Number	Mars16-001-US-C01	**Small Entity Status Claimed**	☒
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)		**Suggested Figure for Publication (if any)**	

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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	Mars16-001-US-C01
	Application Number	
Title of Invention	METHOD FOR FABRICATING GLASS SUBSTRATE PACKAGE	

Filing By Reference :

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32).
Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:	● Customer Number	US Patent Practitioner	○ Limited Recognition (37 CFR 11.9)
Customer Number	102851		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, or 365(c) or indicate National Stage entry from a PCT application. Providing this information in the application data sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.
When referring to the current application, please leave the application number blank.

Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
	Continuation of	15261956	2016-09-11
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
15261956	Claims benefit of provisional	62/219249	2015-09-16

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	Mars16-001-US-C01
	Application Number	
Title of Invention	METHOD FOR FABRICATING GLASS SUBSTRATE PACKAGE	

Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
15261956	Continuation in part of	14/036256	2013-09-25	9615453	2017-04-04
Prior Application Status	Expired				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)		
14/036256	Claims benefit of provisional	61705649	2012-09-26		

Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button. Add

Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55(d). When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX)[i] the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(h)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

Remove

Application Number	Country[i]	Filing Date (YYYY-MM-DD)	Access Code[i] (if applicable)

Additional Foreign Priority Data may be generated within this form by selecting the **Add** button. Add

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.
NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

Authorization to Permit Access:

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	Mars16-001-US-C01
	Application Number	
Title of Invention	METHOD FOR FABRICATING GLASS SUBSTRATE PACKAGE	

☐ Authorization to Permit Access to the Instant Application by the Participating Offices

If checked, the undersigned hereby grants the USPTO authority to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the World Intellectual Property Office (WIPO), and any other intellectual property offices in which a foreign application claiming priority to the instant patent application is filed access to the instant patent application. See 37 CFR 1.14(c) and (h). This box should not be checked if the applicant does not wish the EPO, JPO, KIPO, WIPO, or other intellectual property office in which a foreign application claiming priority to the instant patent application is filed to have access to the instant patent application.

In accordance with 37 CFR 1.14(h)(3), access will be provided to a copy of the instant patent application with respect to: 1) the instant patent application-as-filed; 2) any foreign application to which the instant patent application claims priority under 35 U.S.C. 119(a)-(d) if a copy of the foreign application that satisfies the certified copy requirement of 37 CFR 1.55 has been filed in the instant patent application; and 3) any U.S. application-as-filed from which benefit is sought in the instant patent application.

In accordance with 37 CFR 1.14(c), access may be provided to information concerning the date o f filing this Authorization.

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Applicant 1 Remove

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.

Clear

Assignee	Legal Representative under 35 U.S.C. 117	● Joint Inventor
Person to whom the inventor is obligated to assign.	Person who shows sufficient proprietary interest	

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor :

If the Applicant is an Organization check here. ☐

Prefix	Given Name	Middle Name	Family Name	Suffix
	Ping-Jung		Yang	

PTO/AIA/14 (12-13)
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	Mars16-001-US-C01
	Application Number	
Title of Invention	METHOD FOR FABRICATING GLASS SUBSTRATE PACKAGE	

Mailing Address Information For Applicant:			
Address 1	No. 52, Ln. 97, Shengjun Rd., North Dist.		
Address 2			
City	Hsin-Chu City	**State/Province**	
Country i	TW	Postal Code	
Phone Number	886-913635863	Fax Number	
Email Address	semars3898@gmail.com		

Additional Applicant Data may be generated within this form by selecting the Add button. Add

Assignee Information including Non-Applicant Assignee Information:

Providing assignment information in this section does not subsitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Assignee 1

Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication . An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.

Remove

If the Assignee or Non-Applicant Assignee is an Organization check here. ☐

Prefix	**Given Name**	Middle Name	**Family Name**	Suffix

Mailing Address Information For Assignee including Non-Applicant Assignee:			
Address 1			
Address 2			
City		**State/Province**	
Country i		Postal Code	
Phone Number		Fax Number	
Email Address			

Additional Assignee or Non-Applicant Assignee Data may be generated within this form by selecting the Add button. Add

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TSMC EX1032 Page 205

PTO/AIA/14 (12-13)
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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	Mars16-001-US-C01
	Application Number	
Title of Invention	METHOD FOR FABRICATING GLASS SUBSTRATE PACKAGE	

Signature:

Remove

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Signature	/Ping-Jung Yang/			Date (YYYY-MM-DD)	2020-01-26
First Name	Ping-Jung	Last Name	Yang	Registration Number	

Additional Signature may be generated within this form by selecting the Add button. Add

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent C o o p eration Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

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UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
16/752,650	01/26/2020	2185	785	Mars16-001-US-C01	20	2

CONFIRMATION NO. 4809

FILING RECEIPT

102851
PING-JUNG YANG
NO 2, NIOUPU SOUTH RD., SIANGSHAN DISTRICT
HSINCHU CITY, 30091
TAIWAN

OC000000114689550

Date Mailed: 02/12/2020

Receipt is acknowledged of this non-provisional utility patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF FIRST INVENTOR, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection.

Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please submit a written request for a corrected Filing Receipt, including a properly marked-up ADS showing the changes with strike-through for deletions and underlining for additions. If you received a "Notice to File Missing Parts" or other Notice requiring a response for this application, please submit any request for correction to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections provided that the request is grantable.

Inventor(s)

Ping-Jung Yang, Hsinchu City, TAIWAN;

Applicant(s)

Ping-Jung Yang, Hsin-Chu City, TAIWAN

Power of Attorney: None

Domestic Priority data as claimed by applicant

This application is a CON of 15/261,956 09/11/2016
which claims benefit of 62/219,249 09/16/2015
and is a CIP of 14/036,256 09/25/2013 PAT 9615453
which claims benefit of 61/705,649 09/26/2012

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.
Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access Application via Priority Document Exchange: No

Permission to Access Search Results: No

IPR2026-00067
TSMC EX1032 Page 208

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

If Required, Foreign Filing License Granted: 02/12/2020

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 16/752,650**

Projected Publication Date: 05/21/2020

Non-Publication Request: No

Early Publication Request: No
**** SMALL ENTITY ****
Title

METHOD FOR FABRICATING GLASS SUBSTRATE PACKAGE

Preliminary Class

710

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific

countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

SelectUSA

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The U.S. offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to promote and facilitate business investment. SelectUSA provides information assistance to the international investor community; serves as an ombudsman for existing and potential investors; advocates on behalf of U.S. cities, states, and regions competing for global investment; and counsels U.S. economic development organizations on investment attraction best practices. To learn more about why the United States is the best country in the world to develop

technology, manufacture products, deliver services, and grow your business, visit http://www.SelectUSA.gov or call +1-202-482-6800.

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TSMC EX1032 Page 211

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 16/752,650

APPLICATION AS FILED - PART I

	(Column 1)	(Column 2)	SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE($)	FEE($)		RATE($)	FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	75		N/A	
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	330		N/A	
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	380		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	20 minus 20 =	*	x 50 =	0.00	OR		
INDEPENDENT CLAIMS (37 CFR 1.16(h))	2 minus 3 =	*	x 230 =	0.00			
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			0.00			
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				0.00			
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	785		TOTAL	

APPLICATION AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE($)	ADDITIONAL FEE($)		RATE($)	ADDITIONAL FEE($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

Docket No.: Mars-16-001-US-C01 **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	Customer Number: 102851
Ping-Jung Yang	:	Confirmation Number: 4809
Application No.: 16752650	:	Group Art Unit: Not yet
Filed: Jan. 26, 2020	:	Examiner: Not Yet Assigned

For: METHOD FOR FABRICATING GLASS SUBSTRATE PACKAGE

AMENDMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Please amend the above-identified application and consider the remarks as follows:

Amendments to the Specification begin on page 2 of this paper.

Amendments to the Claims are reflected in the listing of claims which begins on page 3 of this paper.

Remarks/Arguments begin on page 11 of this paper.

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Amendments to the Specification:

Please amend the title of the patent application from "METHOD FOR FABRICATING GLASS SUBSTRATE PACKAGE" to "CHIP PACKAGE"

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TSMC EX1032 Page 214

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

What is claimed is:

Claims 1-20 Cancelled

21. (Newly added) A chip package comprising:

a first polymer layer has a first surface, a second surface opposed to said first surface, a first sidewall and a second sidewall opposed to said first sidewall, wherein said first surface is parallel to said second surface, multiple first copper plugs extending through a first portion of said first polymer layer from said first surface to said second surface, wherein said multiple first copper plugs are arranged in a first row substantially parallel to said first and second sidewalls, multiple second copper plugs extending through a second portion of said first polymer layer from said first surface to said second surface, wherein said multiple second copper plugs are arranged in a second row substantially parallel to said first and second sidewalls, wherein each of said multiple first and second copper plugs has a top surface coplanar to said first surface and a bottom surface coplanar to said second surface, wherein a first distance between said first row and said second row is greater than a second distance between said first row and said first sidewalls and greater than a third distance between said second row and said second sidewalls, wherein said first polymer layer has a thickness between 100 and 300 micrometers;

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a first interconnection scheme over said first surface, wherein said first interconnection scheme comprises a first metal interconnect over said first surface, a second polymer layer between said first surface and said first metal interconnect and a third polymer layer on said first metal interconnect, wherein said first metal interconnect comprises a first metal interconnection layer over said second polymer layer, wherein said first metal interconnection layer comprises a first metal layer in a first opening in said second polymer layer and a first copper layer on said first metal layer in said first opening,;

a first solder bump on said first interconnection scheme, wherein said first solder bump is connected to one of said multiple first copper plugs through a second opening in said third polymer layer, said first metal interconnection layer and said first opening;

a second interconnection scheme under said second surface, wherein said second interconnection scheme comprises a second metal interconnect under said second surface, a fourth polymer layer between said second surface and said second metal interconnect and fifth polymer layer under said second metal interconnect, wherein said second metal interconnect comprises a second metal interconnection layer under said fourth polymer layer and connected to said one of said multiple first copper plugs, wherein said second metal interconnection layer comprises a second metal layer in a third opening in said fourth polymer layer and a second copper layer under said second metal layer in said third opening;

a first chip under said second interconnection scheme and connected to said second metal interconnect via a metal wire through a fourth opening in said fifth polymer layer;

a second chip under said second interconnection scheme and connected to said second metal interconnect;

a third chip under said second chip; and

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multiple first metal bumps between said second and third chips.

22. (Newly added) The chip package of claim 21, no any copper plug with thickness between 100 and 300 micrometers is between said first and second rows.

23. (Newly added) The chip package of claim 21, wherein a third portion is between said first and second portions, wherein said third portion is a square and no any copper plug with thickness between 100 and 300 micrometers in said third portion, wherein said third portion has a width greater than said second and third distances, wherein said third portion has a length greater than said second and third distances.

24. (Newly added) The chip package of claim 21, wherein said first polymer layer further comprises multiple third copper plugs extending through a third portion of said first polymer layer from said first surface to said second surface, wherein said multiple third copper plugs are arranged in a first column substantially vertical to said first and second sidewalls, multiple fourth copper plugs extending through a second portion of said first polymer layer from said first surface to said second surface, wherein said multiple fourth copper plugs are arranged in a second column substantially vertical to said first and second sidewalls, wherein each of said multiple third and fourth copper plugs has a top surface coplanar to said first surface and a bottom surface coplanar to said second surface.

25. (Newly added) The chip package of claim 24, no any copper plug with thickness between 100 and 300 micrometers is between said first and second rows and first and second columns.

26. (Newly added) The chip package of claim 21, wherein said third chip is a DRAM chip.

27. (Newly added) The chip package of claim 21, further comprising a second solder bump on said first interconnection scheme, a fourth chip on said first interconnection scheme and multiple second metal bumps between said first interconnection scheme and said fourth chip, wherein said

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fourth chip is between said first and second solder bumps and connected to a third metal interconnection layer of said first interconnection scheme through one of said multiple second metal bumps and a fifth opening in said third polymer layer.

28. (Newly added) The chip package of claim 21, wherein said first chip is a memory chip.

29. (Newly added) The chip package of claim 21, further comprising a second solder bump on said first interconnection scheme, a fourth chip on said first interconnection scheme, a fifth chip on said first interconnection scheme, multiple second metal bumps between said first interconnection scheme and said fourth chip and multiple third metal bumps between said first interconnection scheme and said fifth chip, wherein said fourth chip is between said first and second solder bumps, wherein said fourth chip is connected to a third metal interconnection layer of said first interconnection scheme through one of said multiple second metal bumps and a fifth opening in said third polymer layer, wherein said fifth chip is connected to a fourth metal interconnection layer of said first interconnection scheme through one of said multiple third metal bumps and a sixth opening in said third polymer layer.

30. (Newly added) The chip package of claim 21, further comprising a second solder bump under said second surface and directly under said one of said multiple first copper plugs, wherein said second solder bump connected to said first solder bump through said one of said multiple first copper plugs.

31. (Newly added) A chip package comprising:

a first polymer layer has a first surface, a second surface opposed to said first surface, a first sidewall and a second sidewall opposed to said first sidewall, wherein said first surface is parallel to said second surface, multiple first copper plugs extending through a first portion of said first polymer layer from said first surface to said second surface, wherein said multiple first

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copper plugs are arranged in a first row substantially parallel to said first and second sidewalls, multiple second copper plugs extending through a second portion of said first polymer layer from said first surface to said second surface, wherein said multiple second copper plugs are arranged in a second row substantially parallel to said first and second sidewalls, wherein each of said multiple first and second copper plugs has a top surface coplanar to said first surface and a bottom surface coplanar to said second surface, wherein a first distance between said first row and said second row is greater than a second distance between said first row and said first sidewalls and greater than a third distance between said second row and said second sidewalls, wherein said first polymer layer has a thickness between 100 and 300 micrometers;

a first interconnection scheme over said first surface, wherein said first interconnection scheme comprises a first metal interconnect over said first surface and a second metal interconnect over said first surface, a second polymer layer between said first surface and said first metal interconnect, a third polymer layer between said first and second metal interconnects and a fourth polymer layer on said second metal interconnect, wherein said first metal interconnect comprises a first metal interconnection layer on said first polymer layer, wherein said second metal interconnect comprises a second metal interconnection layer on said second polymer layer, wherein said first metal interconnection layer comprises a first metal layer in a first opening in said second polymer layer and a first copper layer on said first metal layer in said first opening, wherein said second metal interconnection layer comprises a second metal layer on said third polymer layer and in a second opening in said third polymer layer and a second copper layer on said second metal layer in said second opening;

a first solder bump on said first interconnection scheme, wherein said first solder bump is connected to one of said multiple first copper plugs through a third opening in said fourth

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polymer layer, said second metal interconnection layer, said second opening, said first metal interconnection layer and said first opening;

a second solder bump on said first interconnection scheme, wherein said second solder bump is connected to a third metal interconnection layer of said second metal interconnect through a fourth opening in said fourth polymer layer;

a first chip over said first interconnection scheme and between said first and second solder bumps, wherein said first chip comprises a first metal bump connected to a fourth metal interconnection layer of said second metal interconnect through a fifth opening in said fourth polymer layer, wherein said first chip and said first and second solder bumps are in the same horizontal plane, wherein a fourth distance is between a backside surface of said first chip and a top surface of said fourth polymer layer is smaller than a thickness of said first solder bump; and

a second chip over said first interconnection scheme, wherein said second chip comprises a second metal bump connected to a fifth metal interconnection layer of said second metal interconnect through a sixth opening in said fourth polymer layer.

32. (Newly added) The chip package of claim 31, no any copper plug with thickness between 100 and 300 micrometers is between said first and second rows.

33. (Newly added) The chip package of claim 31, wherein a third portion is between said first and second portions, wherein said third portion is a square and no any copper plug with thickness between 100 and 300 micrometers in said third portion, wherein said third portion has a width greater than said second and third distances, wherein said third portion has a length greater than said second and third distances.

34. (Newly added) The chip package of claim 31, wherein said first polymer layer further comprises multiple third copper plugs extending through a third portion of said first polymer

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layer from said first surface to said second surface, wherein said multiple third copper plugs are arranged in a first column substantially vertical to said first and second sidewalls, multiple fourth copper plugs extending through a fourth portion of said first polymer layer from said first surface to said second surface, wherein said multiple fourth copper plugs are arranged in a second column substantially vertical to said first and second sidewalls, wherein each of said multiple third and fourth copper plugs has a top surface coplanar to said first surface and a bottom surface coplanar to said second surface.

35. (Newly added) The chip package of claim 34, no any copper plug with thickness between 100 and 300 micrometers is between said first and second rows and first and second columns.

36. (Newly added) The chip package of claim 31, further comprising a third solder bump under said second surface and directly under said one of said multiple first copper plugs, wherein said third solder bump connected to said first solder bump through said one of said multiple first copper plugs.

37. (Newly added) The chip package of claim 31, further comprising:

a second interconnection scheme under said second surface, wherein said second interconnection scheme comprises a third metal interconnect under said second surface, a fifth polymer layer between said second surface and said third metal interconnect and a sixth polymer layer under said third metal interconnect, wherein said third metal interconnect comprises a fifth metal interconnection layer under said fifth polymer layer and connected to said one of said multiple first copper plugs, wherein said fifth metal interconnection layer comprises a third metal layer in a sixth opening in said fifth polymer layer and a third copper layer under said third metal layer in said sixth opening; and

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a third chip under said second interconnection scheme and connected to said third metal interconnect via a metal wire.

38. (Newly added) The chip package of claim 31, further comprising:

a second interconnection scheme under said second surface, wherein said second interconnection scheme comprises a third metal interconnect under said second surface, a fifth polymer layer between said second surface and said third metal interconnect and a sixth polymer layer under said third metal interconnect, wherein said third metal interconnect comprises a fifth metal interconnection layer under said fifth polymer layer and connected to said one of said multiple first copper plugs, wherein said fifth metal interconnection layer comprises a third metal layer in a sixth opening in said fifth polymer layer and a third copper layer under said third metal layer in said sixth opening; and

a third chip under said second interconnection scheme and connected to said third metal interconnect;

a fourth chip under said third chip; and

multiple third metal bumps between said third and fourth chips.

39. The chip package of claim 31, wherein said second chip is between said first and second solder bumps.

40. (Newly added) The chip package of claim 31, wherein said second metal layer comprises titanium.

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REMARKS/ARGUMENTS

Claims 1-20 are cancelled and claims 21-40 is newly added herein. Claims 21-40 are pending in the application, of which claims 21 and 31 are the pending independent claims. No new matter is believed to be added into the application by this paper.

In order to make the content of claims consistent with the title of the invention, the title of the invention is amended from "METHOD FOR FABRICATING GLASS SUBSTRATE PACKAGE" to "CHIP PACKAGE".

The above amendment is not believed to add any new matter.

In view of the Amendments, Applicants submit that the claims are in condition for allowance and respectfully request a notice to this effect.

Respectfully submitted,



Date: __2020-03-08_____ Ping-Jung Yang

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PTO/SB/08a (01-10)
Approved for use through 07/31/2012. OMB 0651-0031
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT
(Not for submission under 37 CFR 1.99)

Application Number	16752650
Filing Date	2020-01-26
First Named Inventor	Ping-Jung Yang
Art Unit	1782
Examiner Name	
Attorney Docket Number	Mars16-001-US-C01

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	9362187		2016-06-07	Ossimitz; Peter	
	2	9593009		2017-03-14	Fuergut; Edward et al.	
	3	9704843		2017-07-11	Kilger; Thomas et al.	
	4	10043768		2018-08-07	Meyer; Thorsten et al.	
	5	8952489		2015-02-10	Elian; Klaus et al.	
	6	8952521		2015-02-10	Wojnowski; Maciej et al.	
	7	9331060		2016-05-03	Otremba; Ralf et al.	
	8	9735113		2017-08-15	Chi; HeeJo et al.	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
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	First Named Inventor	Ping-Jung Yang
	Art Unit	1782
	Examiner Name	
	Attorney Docket Number	Mars16-001-US-C01

	9	9679863		2017-06-13	Lin; Yaojian et al.	
	10	9524955		2016-12-20	Huang; Rui et al.	
	11	9508626		2016-11-29	Pagaila; Reza A. et al.	
	12	9406658		2016-08-02	Lee; Chun-Che et al.	
	13	9406619		2016-08-02	Pagaila; Reza A. et al.	
	14	9397050		2016-07-19	Shin; HanGil et al.	
	15	9385009		2016-07-05	Lin; Yaojian et al.	
	16	9385006		2016-07-05	Lin; Yaojian	
	17	9343442		2016-05-17	Chen; Chih-Hua et al.	
	18	9324672		2016-04-26	Pagaila; Reza A. et al.	
	19	9281292		2016-03-08	Hu; Chuan et al.	

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	Application Number	16752650
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	First Named Inventor	Ping-Jung Yang
	Art Unit	1782
	Examiner Name	
	Attorney Docket Number	Mars16-001-US-C01

	20	9224647		2015-12-29	Koo; Jun Mo et al.	
	21	9082806		2015-07-14	Lin; Yaojian et al.	
	22	8993377		2015-03-31	Koo; Jun Mo et al.	
	23	8916421		2014-12-23	Gong; Zhiwei et al.	
	24	8895440		2014-11-25	Choi; DaeSik et al.	
	25	8883561		2014-11-11	Park; DongSam et al.	
	26	8796137		2014-08-05	Pagaila; Reza A. et al.	
	27	8786060		2014-07-22	Yen; Han-Chee et al.	
	28	8742579		2014-06-03	Pagaila; Reza A. et al.	

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	Application Number	16752650
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	First Named Inventor	Ping-Jung Yang
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
	Application Number	16752650
	Filing Date	2020-01-26
	First Named Inventor	Ping-Jung Yang
	Art Unit	1782
	Examiner Name	
	Attorney Docket Number	Mars16-001-US-C01

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Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Ping-Jung Yang/	Date (YYYY-MM-DD)	2020-03-08
Name/Print	Ping-Jung Yang	Registration Number	

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

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Application Number:	16752650
International Application Number:	
Confirmation Number:	4809
Title of Invention:	METHOD FOR FABRICATING GLASS SUBSTRATE PACKAGE
First Named Inventor/Applicant Name:	Ping-Jung Yang
Customer Number:	102851
Filer:	Ping-Jung. Yang
Filer Authorized By:	
Attorney Docket Number:	Mars16-001-US-C01
Receipt Date:	08-MAR-2020
Filing Date:	26-JAN-2020
Time Stamp:	00:39:02
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

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Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		Mars16-001-US-C01-PA-03072020.pdf	158471 03ae5b7e182ce9ac89a2969125f008ebcd01a147	yes	11

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	Document Description	**Start**	**End**
	Preliminary Amendment	1	1
	Specification	2	2
	Claims	3	10
	Applicant Arguments/Remarks Made in an Amendment	11	11

Warnings:					
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2	Information Disclosure Statement (IDS) Form (SB08)	Mars16-001-IDS-03082020.pdf	613091 f8252c7a85780275891feb63d0e90deac0cca1dd	no	6
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PTO/SB/06 (09-11)
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 16/752,650	Filing Date 01/26/2020	☐ To be Mailed

ENTITY: ☐ LARGE ☑ SMALL ☐ MICRO

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A		N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A		N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*		x $50 =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*		x $230 =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).				
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))					
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL	

APPLICATION AS AMENDED - PART II

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT	03/08/2020	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 20	Minus	** 20	= 0		x $50 =	0
	Independent (37 CFR 1.16(h))	* 2	Minus	*** 3	= 0		x $230 =	0
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	0

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=		x $0 =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=		x $0 =	
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.	SLIE
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".	/SHARON M WEST/
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".	
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.	

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
16/752,650	01/26/2020	Ping-Jung Yang	Mars16-001-US-C01

CONFIRMATION NO. 4809

102851
PING-JUNG YANG
NO 2, NIOUPU SOUTH RD., SIANGSHAN DISTRICT
HSINCHU CITY, 30091
TAIWAN

PUBLICATION NOTICE

OC000000117168364

Title:METHOD FOR FABRICATING GLASS SUBSTRATE PACKAGE

Publication No.US-2020-0161245-A1
Publication Date:05/21/2020

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently http://www.uspto.gov/patft/.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Public Records Division. The Public Records Division can be reached by telephone at (571) 272-3150 or (800) 972-6382, by facsimile at (571) 273-3250, by mail addressed to the United States Patent and Trademark Office, Public Records Division, Alexandria, VA 22313-1450 or via the Internet.

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Docket No.: Mars-16-001-US-C01 **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	Customer Number: 102851
Ping-Jung Yang	:	Confirmation Number: 4809
Application No.: 16752650	:	Group Art Unit: 2812
Filed: Jan. 26, 2020	:	Examiner: LIU, XIAOMING

For: Chip Package

AMENDMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Please amend the above-identified application and consider the remarks as follows:

Amendments to the Specification begin on page 2 of this paper.

Amendments to the Claims are reflected in the listing of claims which begins on page 3 of this paper.

Remarks/Arguments begin on page 12 of this paper.

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Amendments to the Specification:

Please amend the paragraph [0057] from line 5-7 of page 13 in the specification filed on Sept. 25, 2013 for disclosure accuracy, as below:

[0057] Furthermore, the glass layer 16 may be replaced by a polymer layer. When the polymer layer cured to a solid state. ~~The,~~ then the polymer layer has an ~~expansion coefficient~~ coefficient of expansion between 3 and 10 ppm/°C.

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Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

What is claimed is:

Claims 1-20 Cancelled

21. (Currently amended) A chip package comprising:

a first polymer layer has a first surface~~;~~ and a second surface opposed to said first surface, ~~a first sidewall and a second sidewall opposed to said first sidewall,~~ wherein said first surface is parallel to said second surface, ~~multiple~~ a first copper ~~plugs~~ plug extending through ~~a first portion of~~ said first polymer layer from said first surface to said second surface, ~~wherein said multiple first copper plugs are arranged in a first row substantially parallel to said first and second sidewalls, multiple~~ and a second copper ~~plugs~~ plug extending through ~~a second portion of~~ said first polymer layer from said first surface to said second surface, ~~wherein said multiple second copper plugs are arranged in a second row substantially parallel to said first and second sidewalls,~~ wherein ~~each of said multiple~~ said first and second copper plugs has a top surface coplanar ~~to~~ with said first surface~~, and a bottom surface coplanar to said second surface, wherein a first distance between said first row and said second row is greater than a second distance between said first row and said first sidewalls and greater than a third distance between said second row and said second sidewalls,~~ wherein said first polymer layer has a thickness between 100 and 300 micrometers and has a coefficient of expansion between 3 and 10 ppm/°C;

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a first interconnection scheme over said first surface, wherein said first interconnection scheme comprises a first metal interconnect over said first surface, a second metal interconnect over said first surface; and a second polymer layer over ~~between said first surface and~~ said first and second metal ~~interconnect~~ interconnects, wherein said first metal interconnect is connected to said first and second copper plugs, ~~and a third polymer layer on said first metal interconnect, wherein said first metal interconnect comprises a first metal interconnection layer over said second polymer layer,~~ wherein said first metal ~~interconnection layer~~ interconnect comprises a first metal layer ~~in a first opening in said second polymer layer~~ and a first copper layer on said first metal layer ~~in said first opening~~;

a first solder bump ~~on~~ over said first interconnection scheme and connected to said second metal interconnect, ~~wherein said first solder bump is connected to one of said multiple first copper plugs through a second opening in said third polymer layer, said first metal interconnection layer and said first opening; and~~

~~a second interconnection scheme under said second surface, wherein said second interconnection scheme comprises a second metal interconnect under said second surface, a fourth polymer layer between said second surface and said second metal interconnect and fifth polymer layer under said second metal interconnect, wherein said second metal interconnect comprises a second metal interconnection layer under said fourth polymer layer and connected to said one of said multiple first copper plugs, wherein said second metal interconnection layer comprises a second metal layer in a third opening in said fourth polymer layer and a second copper layer under said second metal layer in said third opening;~~

a first chip under said ~~second~~ first interconnection scheme, ~~and connected to said second metal interconnect via a metal wire through a fourth opening in said fifth polymer layer;~~

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~~a second chip under said second interconnection scheme and connected to said second metal interconnect;~~

~~a third chip under said second chip; and~~

~~multiple first metal bumps between said second and third chips.~~

22. (Currently amended) The chip package of claim 21, ~~no any copper plug with thickness between 100 and 300 micrometers is between said first and second rows~~ further comprising a passive component over said first surface.

23. (Currently amended) The chip package of claim 21, ~~wherein a third portion is between said first and second portions, wherein said third portion is a square and no any copper plug with thickness between 100 and 300 micrometers in said third portion, wherein said third portion has a width greater than said second and third distances, wherein said third portion has a length greater than said second and third distances~~ further comprising a second chip over said first surface and a third chip over said second chip.

24. (Currently amended) The chip package of claim 21, further comprising a second chip over said first interconnection scheme, wherein said second chip comprises a metal bump between said second chip and said first interconnection scheme ~~wherein said first polymer layer further comprises multiple third copper plugs extending through a third portion of said first polymer layer from said first surface to said second surface, wherein said multiple third copper plugs are arranged in a first column substantially vertical to said first and second sidewalls, multiple fourth copper plugs extending through a second portion of said first polymer layer from said first surface to said second surface, wherein said multiple fourth copper plugs are arranged in a second column substantially vertical to said first and second sidewalls, wherein each of said~~

~~multiple third and fourth copper plugs has a top surface coplanar to said first surface and a bottom surface coplanar to said second surface~~.

25. (Currently amended) The chip package of claim ~~24~~21, ~~no any copper plug with thickness between 100 and 300 micrometers is between said first and second rows and first and second columns~~ wherein said first chip comprises a central-processing-unit (CPU) circuit block and a graphics-processing-unit (GPU) circuit block.

26. (Currently amended) The chip package of claim 21, wherein said ~~third~~ first chip comprises a central-processing-unit (CPU) circuit block and a DRAM circuit block ~~is a DRAM chip~~.

27. (Currently amended) The chip package of claim 21, ~~further comprising a second solder bump on said first interconnection scheme, a fourth chip on said first interconnection scheme and multiple second metal bumps between said first interconnection scheme and said fourth chip, wherein said fourth chip is between said first and second solder bumps and connected to a third metal interconnection layer of said first interconnection scheme through one of said multiple second metal bumps and a fifth opening in said third polymer layer~~ wherein said first interconnection scheme further comprises a third metal interconnect over said first metal interconnect, wherein said third metal interconnect comprises a second metal layer and a second copper layer on said second metal layer.

28. (Currently amended) The chip package of claim 21, wherein said ~~first chip is a memory chip~~ first copper plugs has a top surface coplanar with said first surface.

29. (Currently amended) The chip package of claim 21, wherein said first copper plugs has a top surface coplanar with said first surface and a bottom surface coplanar with said second surface ~~further comprising a second solder bump on said first interconnection scheme, a fourth chip on said first interconnection scheme, a fifth chip on said first interconnection scheme, multiple~~

~~second metal bumps between said first interconnection scheme and said fourth chip and multiple third metal bumps between said first interconnection scheme and said fifth chip, wherein said fourth chip is between said first and second solder bumps, wherein said fourth chip is connected to a third metal interconnection layer of said first interconnection scheme through one of said multiple second metal bumps and a fifth opening in said third polymer layer, wherein said fifth chip is connected to a fourth metal interconnection layer of said first interconnection scheme through one of said multiple third metal bumps and a sixth opening in said third polymer layer.~~

30. (Currently amended) The chip package of claim 21, further comprising a second solder bump under said second surface and directly under said ~~one of said multiple~~ first copper plugs~~, wherein said second solder bump connected to said first solder bump through said one of said multiple first copper plugs~~.

31. (Previously presented) A chip package comprising:

a first polymer layer has a first surface, a second surface opposed to said first surface, a first sidewall and a second sidewall opposed to said first sidewall, wherein said first surface is parallel to said second surface, multiple first copper plugs extending through a first portion of said first polymer layer from said first surface to said second surface, wherein said multiple first copper plugs are arranged in a first row substantially parallel to said first and second sidewalls, multiple second copper plugs extending through a second portion of said first polymer layer from said first surface to said second surface, wherein said multiple second copper plugs are arranged in a second row substantially parallel to said first and second sidewalls, wherein each of said multiple first and second copper plugs has a top surface coplanar to said first surface and a bottom surface coplanar to said second surface, wherein a first distance between said first row and said second row is greater than a second distance between said first row and said first

sidewalls and greater than a third distance between said second row and said second sidewalls, wherein said first polymer layer has a thickness between 100 and 300 micrometers;

a first interconnection scheme over said first surface, wherein said first interconnection scheme comprises a first metal interconnect over said first surface and a second metal interconnect over said first surface, a second polymer layer between said first surface and said first metal interconnect, a third polymer layer between said first and second metal interconnects and a fourth polymer layer on said second metal interconnect, wherein said first metal interconnect comprises a first metal interconnection layer on said first polymer layer, wherein said second metal interconnect comprises a second metal interconnection layer on said second polymer layer, wherein said first metal interconnection layer comprises a first metal layer in a first opening in said second polymer layer and a first copper layer on said first metal layer in said first opening, wherein said second metal interconnection layer comprises a second metal layer on said third polymer layer and in a second opening in said third polymer layer and a second copper layer on said second metal layer in said second opening;

a first solder bump on said first interconnection scheme, wherein said first solder bump is connected to one of said multiple first copper plugs through a third opening in said fourth polymer layer, said second metal interconnection layer, said second opening, said first metal interconnection layer and said first opening;

a second solder bump on said first interconnection scheme, wherein said second solder bump is connected to a third metal interconnection layer of said second metal interconnect through a fourth opening in said fourth polymer layer;

a first chip over said first interconnection scheme and between said first and second solder bumps, wherein said first chip comprises a first metal bump connected to a fourth metal

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interconnection layer of said second metal interconnect through a fifth opening in said fourth polymer layer, wherein said first chip and said first and second solder bumps are in the same horizontal plane, wherein a fourth distance is between a backside surface of said first chip and a top surface of said fourth polymer layer is smaller than a thickness of said first solder bump; and

a second chip over said first interconnection scheme, wherein said second chip comprises a second metal bump connected to a fifth metal interconnection layer of said second metal interconnect through a sixth opening in said fourth polymer layer.

32. (Previously presented) The chip package of claim 31, no any copper plug with thickness between 100 and 300 micrometers is between said first and second rows.

33. (Previously presented) The chip package of claim 31, wherein a third portion is between said first and second portions, wherein said third portion is a square and no any copper plug with thickness between 100 and 300 micrometers in said third portion, wherein said third portion has a width greater than said second and third distances, wherein said third portion has a length greater than said second and third distances.

34. (Previously presented) The chip package of claim 31, wherein said first polymer layer further comprises multiple third copper plugs extending through a third portion of said first polymer layer from said first surface to said second surface, wherein said multiple third copper plugs are arranged in a first column substantially vertical to said first and second sidewalls, multiple fourth copper plugs extending through a fourth portion of said first polymer layer from said first surface to said second surface, wherein said multiple fourth copper plugs are arranged in a second column substantially vertical to said first and second sidewalls, wherein each of said multiple third and fourth copper plugs has a top surface coplanar to said first surface and a bottom surface coplanar to said second surface.

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35. (Currently amended) The chip package of claim ~~34~~ 31, wherein said first polymer layer has a coefficient of expansion between 3 and 10 ppm/°C ~~no any copper plug with thickness between 100 and 300 micrometers is between said first and second rows and first and second columns~~.

36. (Previously presented) The chip package of claim 31, further comprising a third solder bump under said second surface and directly under said one of said multiple first copper plugs, wherein said third solder bump connected to said first solder bump through said one of said multiple first copper plugs.

37. (Previously presented) The chip package of claim 31, further comprising:

a second interconnection scheme under said second surface, wherein said second interconnection scheme comprises a third metal interconnect under said second surface, a fifth polymer layer between said second surface and said third metal interconnect and a sixth polymer layer under said third metal interconnect, wherein said third metal interconnect comprises a fifth metal interconnection layer under said fifth polymer layer and connected to said one of said multiple first copper plugs, wherein said fifth metal interconnection layer comprises a third metal layer in a sixth opening in said fifth polymer layer and a third copper layer under said third metal layer in said sixth opening; and

a third chip under said second interconnection scheme and connected to said third metal interconnect via a metal wire.

38. (Previously presented) The chip package of claim 31, further comprising:

a second interconnection scheme under said second surface, wherein said second interconnection scheme comprises a third metal interconnect under said second surface, a fifth polymer layer between said second surface and said third metal interconnect and a sixth polymer layer under said third metal interconnect, wherein said third metal interconnect comprises a fifth

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metal interconnection layer under said fifth polymer layer and connected to said one of said multiple first copper plugs, wherein said fifth metal interconnection layer comprises a third metal layer in a sixth opening in said fifth polymer layer and a third copper layer under said third metal layer in said sixth opening; and

a third chip under said second interconnection scheme and connected to said third metal interconnect;

a fourth chip under said third chip; and

multiple third metal bumps between said third and fourth chips.

39. (Previously presented) The chip package of claim 31, wherein said second chip is between said first and second solder bumps.

40. (Currently amended) The chip package of claim 31, further comprising a third chip under said first interconnection scheme, wherein said third chip comprises a central-processing-unit (CPU) circuit block and a graphics-processing-unit (GPU) circuit block. ~~wherein said second metal layer comprises titanium.~~

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REMARKS/ARGUMENTS

Claims 1-20 are cancelled. Claims 21-40 are pending in the application, of which claims 21 and 31 are the pending independent claims. Claims 21-30, 35 and 40 are currently amended herein. No new matter is believed to be added into the application by this paper.

Amendments to Specification

In this paper, in para. [0057], page 13, "When the polymer cured to a solid state. The polymer layer…" is amended to be "When the polymer layer cured to a solid state~~. The~~, then the polymer layer…" and "expansion coefficient" is amended to be "coefficient of expansion", as supported in the paragraph for disclosure accuracy.

Applicants submit that the substitute specification contains no new matter in compliance with 37 CFR §1.125(b), and respectfully request that it be made a part of the record of the present application. No additional pages were added due to the amendments.

In view of the Amendments, Applicants submit that the claims are in condition for allowance and respectfully request a notice to this effect.

Respectfully submitted,

Mars Yang

Date: __2020-08-13_____ Ping-Jung Yang

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TSMC EX1032 Page 245

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Application Number	16752650
Filing Date	2020-01-26
First Named Inventor	Ping-Jung Yang
Art Unit	1782
Examiner Name	LIU, XIAOMING
Attorney Docket Number	Mars16-001-US-C01

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Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	10192796		2019-01-29	Lin; Yaojian et al.	
	2	9837303		2017-12-05	Lin; Yaojian et al.	
	3	9704780		2017-07-11	Marimuthu; Pandi C. et al.	
	4	9431331		2016-08-30	Do; Byung Tai et al.	
	5	9048211		2015-06-02	Pagaila; Reza A. et al.	
	6	8987918		2015-03-24	Razdan; Sandeep et al.	
	7	8980691		2015-03-17	Lin; Yaojian	
	8	8846454		2014-09-30	Shim; Il Kwon et al.	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	16752650
	Filing Date	2020-01-26
	First Named Inventor	Ping-Jung Yang
	Art Unit	1782
	Examiner Name	LIU, XIAOMING
	Attorney Docket Number	Mars16-001-US-C01

	9	8648470		2014-02-11	Lin; Yaojian et al.	

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	16752650
	Filing Date	2020-01-26
	First Named Inventor	Ping-Jung Yang
	Art Unit	1782
	Examiner Name	LIU, XIAOMING
	Attorney Docket Number	Mars16-001-US-C01

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
	Application Number	16752650
	Filing Date	2020-01-26
	First Named Inventor	Ping-Jung Yang
	Art Unit	1782
	Examiner Name	LIU, XIAOMING
	Attorney Docket Number	Mars16-001-US-C01

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Ping-Jung Yang/	Date (YYYY-MM-DD)	2020-08-13
Name/Print	Ping-Jung Yang	Registration Number	

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt	
EFS ID:	40270765
Application Number:	16752650
International Application Number:	
Confirmation Number:	4809
Title of Invention:	METHOD FOR FABRICATING GLASS SUBSTRATE PACKAGE
First Named Inventor/Applicant Name:	Ping-Jung Yang
Customer Number:	102851
Filer:	Ping-Jung. Yang
Filer Authorized By:	
Attorney Docket Number:	Mars16-001-US-C01
Receipt Date:	13-AUG-2020
Filing Date:	26-JAN-2020
Time Stamp:	08:42:32
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		Mars16-001-US-C01-PA-08132020.pdf	135376 fb9ece827a0f4a5a85285c79d0f911985f75710e	yes	12

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Preliminary Amendment	1	1
	Specification	2	2
	Claims	3	11
	Applicant Arguments/Remarks Made in an Amendment	12	12

Warnings:					
Information:					
2	Information Disclosure Statement (IDS) Form (SB08)	Mars16-001-IDS-08132020.pdf	612435 aae02b467b292f889d6adae050c9a16b2675b563	no	5
Warnings:					
Information:					
		Total Files Size (in bytes):	747811		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 16/752,650	Filing Date 01/26/2020	☐ To be Mailed

ENTITY: ☐ LARGE ☑ SMALL ☐ MICRO

APPLICATION AS FILED - PART I

	(Column 1)	(Column 2)			
FOR	NUMBER FILED	NUMBER EXTRA		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A		N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A		N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*		x $50 =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*		x $230 =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).				
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))					
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL	

APPLICATION AS AMENDED - PART II

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT	08/13/2020	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 20	Minus	** 20	= 0		x $50 =	0
	Independent (37 CFR 1.16(h))	* 2	Minus	*** 3	= 0		x $230 =	0
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	0

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=		x $0 =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=		x $0 =	
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.	SLIE
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".	/SHARON M WEST/
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".	
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.	

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/752,650	01/26/2020	Ping-Jung Yang	Mars16-001-US-C01	4809

102851 7590 09/21/2020

PING-JUNG YANG
NO 2, NIOUPU SOUTH RD., SIANGSHAN DISTRICT
HSINCHU CITY, 30091
TAIWAN

EXAMINER	
LIU, XIAOMING	

ART UNIT	PAPER NUMBER
2812	

MAIL DATE	DELIVERY MODE
09/21/2020	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	**Application No.** 16/752,650	**Applicant(s)** Yang, Ping-Jung	
	Examiner XIAOMING LIU	**Art Unit** 2812	**AIA (FITF) Status** No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☑ Responsive to communication(s) filed on 8/13/2020.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL.** 2b) ☑ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5) ☑ Claim(s) 21-40 is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6) ☐ Claim(s) _____ is/are allowed.

7) ☑ Claim(s) 21-40 is/are rejected.

8) ☐ Claim(s) _____ is/are objected to.

9) ☐ Claim(s) _____ are subject to restriction and/or election requirement

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to **PPHfeedback@uspto.gov.**

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☑ The drawing(s) filed on 1/26/2020 is/are: a)☑ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☑ Notice of References Cited (PTO-892)

2) ☑ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date 1/26/2020, 3/8/2020, and 8/13/2020.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date _____.

4) ☐ Other: _____.

DETAILED ACTION

Notice of Pre-AIA or AIA Status

The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

Information Disclosure Statement

The information disclosure statement (IDS) submitted on 1/26/2020, 3/8/2020, and 8/13/2020. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

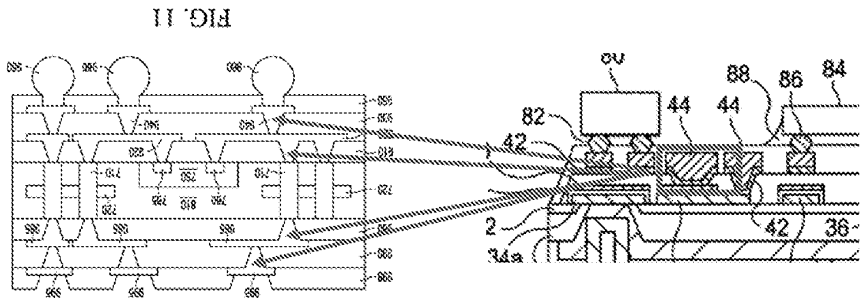
Claim Rejections - 35 USC § 103

In the event the determination of the status of the application as subject to AIA 35 U.S.C. 102 and 103 (or as subject to pre-AIA 35 U.S.C. 102 and 103) is incorrect, any correction of the statutory basis for the rejection will not be considered a new ground of rejection if the prior art relied upon, and the rationale supporting the rejection, would be the same under either status.

The following is a quotation of 35 U.S.C. 103 which forms the basis for all obviousness rejections set forth in this Office action:

> A patent for a claimed invention may not be obtained, notwithstanding that the claimed invention is not identically disclosed as set forth in section 102, if the differences between the claimed invention and the prior art are such that the claimed invention as a whole would have been obvious before the effective filing date of the claimed invention to a person having ordinary skill in the art to which the claimed invention pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 21, 22, 24, and 27-29 are rejected under 35 U.S.C. 103 as being unpatentable over Gong et al. US 2013/0049217 in view of Lin et al. US 2009/0155959.



Re claim 21, Gong teaches a chip package (fig11) comprising:

a first polymer layer (810, fig11, [35]) has a first surface (surface of 810 with 750, fig11); and a second surface (surface of 810 facing 980, fig11) opposed to said first surface, wherein said first surface is parallel to said second surface (fig11),

a first copper plug (left 710 located left of 750, fig11, [25, 34]) extending through said first polymer layer from said first surface to said second surface (fig11), and a second copper plug (right 710 located left of 750, fig11, [25, 34]) extending through said first polymer layer from said first surface to said second surface, wherein said first and second copper plugs has a top surface (surface of 710 on side of 750, fig11) coplanar with said first surface (surface of 810 with 750, fig11),

wherein said first polymer layer has a coefficient of expansion between 3 and 10ppm/C (polyimide as 810 with a CTE of in the range of 1-10 ppm/C see teaching reference Tiedtke US 2011/0257716 [43]);

a first interconnection scheme (920, 940, fig11, [41]) over said first surface, wherein said first interconnection scheme comprises a first metal interconnect (left 920, fig11, [40]) over said first surface, a second metal interconnect (right 920, fig11, [40]) over said first surface; and

a second polymer layer (930, fig11, [39, 41]) over said first and second metal interconnects, wherein said first metal interconnect is connected to said first and second copper plugs (fig11),

a first solder bump (960, fig11, [41]) over said first interconnection scheme and connected to said second metal interconnect (right 920, fig11, [40]); and

a first chip (750, fig11, [35]) under said first interconnection scheme.

The embodiment in fig11 does not explicitly show wherein said first polymer layer has a thickness between 100 and 300 micrometers.

Gong teaches the length of each signal conduit can typically be in a range of 100µm to 2mm.

It would have been obvious to one having ordinary skill in the art before the effective filing date of the claimed invention to adjust the thickness of the interposer to a desired thickness to encapsulate the package (Gong, [25]).

See In re Aller, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955). It is not inventive to discover optimum or workable ranges by routine experimentation. Note that the specification contains no disclosure of either the critical nature of the claimed ranges or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 f.2d 1575, 16 USPQ2d 1934 (Fed. Cir. 1990).

Gong does not explicitly show wherein said first metal interconnect comprises a first metal layer and a first copper layer on said first metal layer;

Lin teaches a first metal interconnect (42 and 44, fig2b, [26]) comprises a first metal layer (42, fig2B, [26]) and a first copper layer (44, fig2B, [26]) on said first metal layer. Lin also teaches the inserted conductive layer 42 acts as an adhesion to facilitate deposition of conductive layer 44 ([25]).

It would have been obvious to one having ordinary skill in the art before the effective filing date of the claimed invention to combine the teaching of Gong with the teaching of Lin to add a metal adhesion layer to facilitate deposition of conductive layer 920 (Lin, [25]).

Re claim 22, Gong modified above teaches the chip package of claim 21, further comprising a passive component over said first surface (Lin 80 in fig2f bonded to Gong 960).

Re claim 24, Gong modified above teaches the chip package of claim 21, further comprising a second chip (Lin 80 in fig2f bonded to Gong 960) over said first interconnection scheme, wherein said second chip comprises a metal bump (Lin, 82, fig2f, [46]) between said second chip (Lin, 80, fig2f, [46]) and said first interconnection scheme (Lin, 44 and 42, fig2f, [25]; Gong, 920, fig11, [40]).

Re claim 27, Gong modified above teaches the chip package of claim 21, wherein said first interconnection scheme further comprises a third metal interconnect (Gong, 940 with adhesion metal layer of Lin, fig11, [41]) over said first metal interconnect, wherein said third metal interconnect comprises a second metal layer (Lin 42 formed on Gong 940) and a second copper layer (Gong, 940, fig11, [41]) on said second metal layer.

Re claim 28, Gong modified above teaches the chip package of claim 21, wherein said first copper plugs has a top surface (Gong, surface of 710 in contact with 920, fig11) coplanar with said first surface (Gong, surface of 810 with 750, fig11).

Re claim 29, Gong modified above teaches the chip package of claim 21, wherein said first copper plugs has a top surface (Gong, surface of 710 in contact with 920, fig11) coplanar with said first surface (Gong, surface of 810 with 750, fig11) and a bottom surface (Gong, surface of 710 facing 980, fig11) coplanar with said second surface (Gong, surface of 810 facing 980, fig11).

Claim 23 is rejected under 35 U.S.C. 103 as being unpatentable over Gong et al. US 2013/0049217 in view of Lin et al. US 2009/0155959 and Bathan et al. US 2009/0230517.

Re claim 23, Gong in view of Lin teaches the chip package of claim 21, further comprising a second chip (Lin 80 in fig2f bonded to Gong 960) over said first surface

Gong does not explicitly show a third chip over said second chip.

Bathan teaches a third chip (606, fig6, [54]) over said second chip (602, fig6, [54]) over a carrier (402, fig6, [53). Bathan also teaches module packages and package stacks minimize occurrence of gross component failure in a more integrated circuit (Bathan, [2, 5]).

It would have been obvious to one having ordinary skill in the art before the effective filing date of the claimed invention to combine the teaching of Gong modified above with the teaching of Bathan to use the interposer of Gong in the chip setup of Bathan. The motivation to do so is to achieve high integration with minimum occurrence of gross component failure in a more integrated circuit (Bathan, [2, 5]).

Claims 25, 26, 30-33, 35, 36, and 39 are rejected under 35 U.S.C. 103 as being unpatentable over Gong et al. US 2013/0049217 in view of Lin et al. US 2009/0155959 and Chen et al. US 2013/0277801.

Re claim 25, Gong does not explicitly show the chip package of claim 21, wherein said first chip comprises a central-processing-unit (CPU) circuit block and a graphics-processing-unit (GPU) circuit block.

Chen teaches a chip comprises a central-processing-unit (CPU) circuit block (204, fig1, [26]) and a graphics-processing-unit (GPU) circuit block (204, fig1, [26]) over a carrier (102, fig1, [24]).

It would have been obvious to one having ordinary skill in the art before the effective filing date of the claimed invention to combine the teaching of Gong modified above with the teaching of Chen to mount the package of Chen. The motivation to do so is to reduce size and increase integration (Chen, [5]).

Re claim 26, Gong does not explicitly show the chip package of claim 21, wherein said first chip comprises a central-processing-unit (CPU) circuit block and a DRAM circuit block.

Chen teaches a chip comprises a central-processing-unit (CPU) circuit block (204/104, fig1, [26]) and a DRAM circuit block (204/104, fig1, [26]) over a carrier (102, fig1, [24]).

It would have been obvious to one having ordinary skill in the art before the effective filing date of the claimed invention to combine the teaching of Gong modified above with the teaching of Chen to mount the package of Chen. The motivation to do so is to reduce size and increase integration (Chen, [5]).

Re claim 30, Gong does not explicitly show the chip package of claim 21, further comprising a second solder bump under said second surface and directly under said first copper plugs.

Chen teaches a second solder bump (114, fig4, [24]) under a second surface and directly under a carrier (102, fig4, [24]).

It would have been obvious to one having ordinary skill in the art before the effective filing date of the claimed invention to combine the teaching of Gong modified above with the teaching of Chen to form solder bumps on each side of the interposer as in Chen. The motivation to do so is to reduce size and increase integration (Chen, [5]).

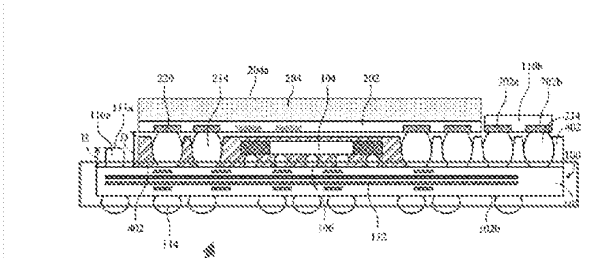


FIG. 7A

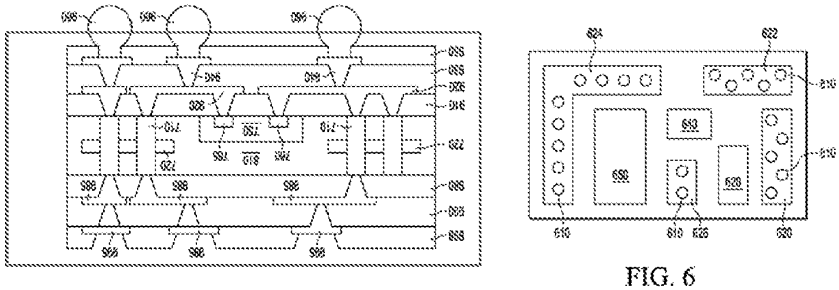


FIG. 6

Re claim 31, Gong teaches a chip package (fig11) comprising:

a first polymer layer (810, fig11, [35]) has a first surface (surface of 810 with 750, fig11), a second surface (surface of 810 facing 980, fig11) opposed to said first surface, a first sidewall (left side wall of 810, fig11) and a second sidewall (right side wall of 810, fig11) opposed to said first sidewall,

wherein said first surface is parallel to said second surface (fig11), multiple first copper plugs (left 710, fig11, [25, 34]) extending through a first portion (left side of 810, fig11) of said first polymer layer from said first surface to said second surface,

wherein said multiple first copper plugs are arranged in a first row substantially parallel to said first and second sidewalls (fig5 or 6), multiple second copper plugs (right 710, fig11, [25, 34]) extending through a second portion (right side of 810, fig11) of said first polymer layer from said first surface to said second surface,

wherein said multiple second copper plugs are arranged in a second row substantially parallel to said first and second sidewalls (fig5 or 6),

wherein each of said multiple first and second copper plugs has a top surface (surface of 710 on side of 750, fig11) coplanar to said first surface (surface of 810 with 750, fig11) and a bottom surface (surface of 710 facing 980, fig11) coplanar to said second surface (surface of 810 facing 980, fig11),

wherein a first distance (center gap of 710 with 750 in between, fig11) between said first row and said second row is greater than a second distance (distance between left sidewall of 810 and left 710, fig11) between said first row and said first sidewalls and greater than a third distance (distance between right sidewall of 810 and right 710, fig11) between said second row and said second sidewalls,

a first interconnection scheme (920 and 940, fig11, [41]) over said first surface, wherein said first interconnection scheme comprises a first metal interconnect (920, fig11, [40]) over said first surface and a second metal interconnect (940, fig11, [40]) over said first surface,

a second polymer layer (910, fig11, [39]) between said first surface and said first metal interconnect,

a third polymer layer (930, fig11, [39, 41]) between said first and second metal interconnects and

a fourth polymer layer (950, fig11, [39, 41]) on said second metal interconnect (940, fig11, [40]),

wherein said first metal interconnect comprises a first metal interconnection layer (920, fig11, [40]) on said first polymer layer (810, fig11, [35]),

wherein said second metal interconnect comprises a second metal interconnection layer (940, fig11, [40]) on said second polymer layer (910, fig11, [39]),

wherein said first metal interconnection layer comprises a first metal layer in a first opening in said second polymer layer (space in 910 holding 920, fig11),

wherein said second metal interconnection layer comprises a second metal layer on said third polymer layer and in a second opening in said third polymer layer (space in 930 holding 940, fig11);

a first solder bump (left 960, fig11, [41]) on said first interconnection scheme (920 and 940, fig11, [41]), wherein said first solder bump is connected to one of said multiple first copper plugs through a third opening in said fourth polymer layer (space in 950 holding 960, fig11, [39, 41]), said second metal interconnection layer (940, fig11, [40]), said second opening (space in 930 holding 940, fig11), said first metal interconnection layer (920, fig11, [40]) and said first opening (space in 910 holding 920, fig11);

a second solder bump (right 960, fig11, [41]) on said first interconnection scheme (920 and 940, fig11, [41]), wherein said second solder bump is connected to a third metal interconnection layer (right 940 in contact with right 960, fig11, [40]) of said second metal interconnect (940, fig11, [40]) through a fourth opening in said fourth polymer layer (space in 950 holding left 960, fig11, [39, 41]);

The embodiment in fig11 does not explicitly show wherein said first polymer layer has a thickness between 100 and 300 micrometers;

Gong teaches the length of each signal conduit can typically be in a range of 100μm to 2mm.

It would have been obvious to one having ordinary skill in the art before the effective filing date of the claimed invention to adjust the thickness of the interposer to a desired thickness to encapsulate the package (Gong, [25]).

See In re Aller, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955). It is not inventive to discover optimum or workable ranges by routine experimentation. Note that the specification contains no disclosure of either the critical nature of the claimed ranges or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 f.2d 1575, 16 USPQ2d 1934 (Fed. Cir. 1990).

Gong does not explicitly show first and second metal interconnect comprises a first metal layer and a first copper layer on said first metal layer; a first chip over said first interconnection scheme and between said first and second solder bumps, wherein said first chip comprises a first metal bump connected to a fourth metal interconnection layer of said second metal interconnect through a fifth opening in said fourth polymer layer, wherein said first chip and said first and second solder bumps are in the same horizontal plane, wherein a fourth distance is between a backside surface of said first chip and a top surface of said fourth polymer layer is smaller than a thickness of said first solder bump; and a second chip over said first interconnection scheme, wherein said second chip comprises a second metal bump connected to a fifth metal interconnection layer of said second metal interconnect through a sixth opening in said fourth polymer layer.

Lin teaches a metal interconnect (42 and 44, fig2B, [26]) comprises a first metal layer (42, fig2B, [26]) and a first copper layer (44, fig2B, [26]) on said first metal layer. Lin also teaches the inserted conductive layer 42 acts as an adhesion to facilitate deposition of conductive layer 44 ([25]).

It would have been obvious to one having ordinary skill in the art before the effective filing date of the claimed invention to combine the teaching of Gong with the teaching of Lin to add a metal adhesion layer to facilitate deposition of conductive layer 920 (Lin, [25]).

Cheng teaches a first chip (104, fig7A) over said first interconnection scheme and between a first and second solder bumps (214, fig7A), wherein said first chip comprises a first metal bump connected to a fourth metal interconnection layer (106 and interconnect in 102, fig4), wherein said first chip and said first and second solder bumps are in the same horizontal plane (top surface of 102, fig7A), wherein a fourth distance (height of 106, fig7A) is between a backside surface of said first chip and a top surface of said fourth polymer layer is smaller than a thickness of said first solder bump (height of 214, fig4); and a second chip (110b, fig7A) over said first interconnection scheme, wherein said second chip comprises a second metal bump (214 under 110b, fig7A) connected to a fifth metal interconnection layer of said

second metal interconnect (interconnect in contact with 214 in 102, fig7A) through a sixth opening in said fourth layer (space in 402 holding 214, fig7A).

It would have been obvious to one having ordinary skill in the art before the effective filing date of the claimed invention to combine the teaching of Gong modified above with the teaching of Chen to mount package with a top view of Gong fig6 and side view of Chen7A. The motivation to do so is to reduce size and increase integration (Chen, [5]).

Re claim 32, Gong modified above teaches the chip package of claim 31, no any copper plug with thickness between 100 and 300 micrometers is between said first and second rows (Gong, fig11).

Re claim 33, Gong modified above teaches the chip package of claim 31, wherein a third portion (Gong, center part with 750, fig11 and 5) is between said first (Gong, left side of 810 with 710, fig11) and second portions (Gong, right side of 810 with 710, fig11), wherein said third portion is a square and no any copper plug with thickness between 100 and 300 micrometers in said third portion (Gong, fig5), wherein said third portion has a width greater than said second and third distances (Gong, fig5), wherein said third portion has a length greater than said second and third distances (Gong, fig5).

Re claim 35, Gong modified above teaches the chip package of claim 31, wherein said first polymer layer has a coefficient of expansion between 3 and 10 ppm/C (polyimide as Gong 810 with a CTE of in the range of 1-10 ppm/C see teaching reference Tiedtke US 2011/0257716 [43]).

Re claim 36, Gong modified above teaches the chip package of claim 31, further comprising a third solder bump under said second surface (Chen, bump on both side of interposer, fig7A) and directly under said one of said multiple first copper plugs, wherein said third solder bump connected to said first solder bump through said one of said multiple first copper plugs (Gong, fig11 with bumps formed on 995).

Re claim 39, Gong modified above teaches the chip package of claim 31, wherein said second chip is between said first and second solder bumps (Gong, 620-650 between 620 and 624, fig6).

Claims 37, 38, and 40 are rejected under 35 U.S.C. 103 as being unpatentable over Gong et al. US 2013/0049217 in view of Lin et al. US 2009/0155959, Chen et al. US 2013/0277801, and Bathan et al. US 2009/0230517

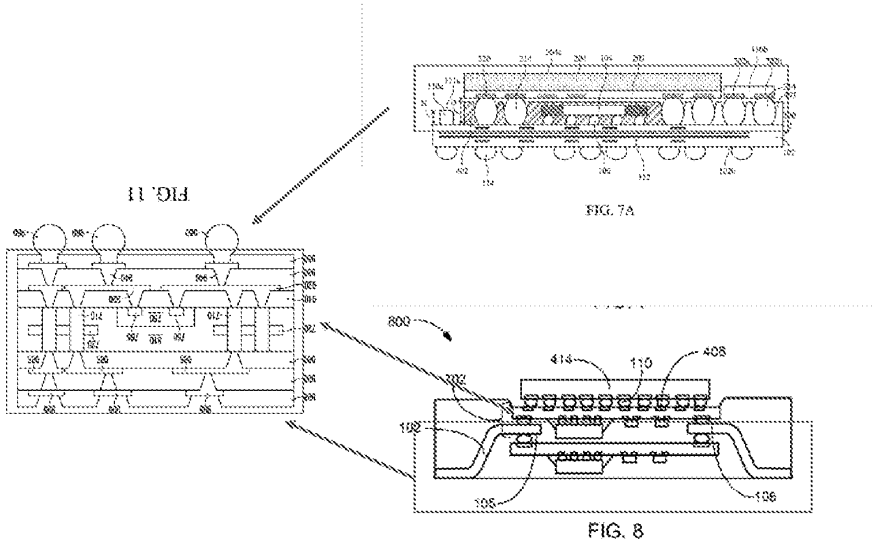


FIG. 8

Re claim 37, Gong modified above teaches the chip package of claim 31, further comprising: a second interconnection scheme (Gong, 985 and 995, fig11) under said second surface, wherein said second interconnection scheme comprises a third metal interconnect (Gong, 985, fig11) under said second surface, a fifth polymer layer (Gong, 980, fig11) between said second surface and said third metal interconnect and a sixth polymer layer (Gong, 960, fig11) under said third metal interconnect (Gong, 985, fig11), wherein said third metal interconnect comprises a fifth metal interconnection layer (Gong, part of 985 in 990, fig11) under said fifth polymer layer and connected to said one of said multiple first copper plugs, wherein said fifth metal interconnection layer (Gong, part of 985 with metal adhesion layer of Lin in 990, fig11) comprises a third metal layer (adhesion layer of Lin added under Gong 985) in a sixth opening (Gong, space in 980, fig 11) in said fifth polymer layer and a third copper layer (Gong, 985 on adhesion layer, fig11) under said third metal layer in said sixth opening;

Gong does not explicitly show a third chip under said second interconnection scheme and connected to said third metal interconnect via a metal wire.

Bathan teaches a chips mounted on both side of a carrier (fig8). Bathan also teaches module packages and package stacks minimize occurrence of gross component failure in a more integrated circuit (Bathan, [2, 5]).

It would have been obvious to one having ordinary skill in the art before the effective filing date of the claimed invention to combine the teaching of Gong modified above with the teaching of Bathan to use the interposer of Gong in the chip setup of Bathan. The motivation to do so is to achieve high integration with minimum occurrence of gross component failure in a more integrated circuit (Bathan, [2, 5]).

Re claim 38, Gong modified above teaches the chip package of claim 31, further comprising: a second interconnection scheme (Gong, 985 and 995, fig11) under said second surface, wherein said second interconnection scheme comprises a third metal interconnect (Gong, 985, fig11) under said second surface, a fifth polymer layer (Gong, 980, fig11) between said second surface and said third metal interconnect and a sixth polymer layer (Gong, 960, fig11) under said third metal interconnect, wherein said third metal interconnect comprises a fifth metal interconnection layer (Gong, part of 985 in 990, fig11) under said fifth polymer layer and connected to said one of said multiple first copper plugs, wherein said fifth metal interconnection layer comprises a third metal layer (adhesion layer of Lin added under Gong 985) in a sixth opening (Gong, space in 980, fig 11) in said fifth polymer layer and a third copper layer (Gong, 985 on adhesion layer, fig11) under said third metal layer in said sixth opening;

Gong does not explicitly show a third chip under said second interconnection scheme and connected to said third metal interconnect; a fourth chip under said third chip; and multiple third metal bumps between said third and fourth chips.

Bathan teaches a chip s mounted on both side of a carrier (fig8) wherein a third chip (112, fig7 and 8) under said second interconnection scheme and connected to said third metal interconnect (connects in interposer 402, fig7 and 8); a fourth chip (chip under 102, fig8) under said third chip (112, fig7 and 8); and multiple third metal bumps (bumps under chips under 102, fig8) between said third and fourth chips. Bathan also teaches module packages and package stacks minimize occurrence of gross component failure in a more integrated circuit (Bathan, [2, 5]).

It would have been obvious to one having ordinary skill in the art before the effective filing date of the claimed invention to combine the teaching of Gong modified above with the teaching of Bathan to use the interposer of Gong in the chip setup of Bathan. The motivation to do so is to achieve high integration with minimum occurrence of gross component failure in a more integrated circuit (Bathan, [2, 5]).

Re claim 40, Gong modified above teaches the chip package of claim 31, further comprising a third chip (Chen, 204, fig1, [26]), wherein said third chip comprises a central-processing-unit (CPU) circuit block and a graphics-processing-unit (GPU) circuit block (Chen, [26]).

Gong does not explicitly show a third chip under said first interconnection scheme.

Bathan teaches a chips mounted on both side of a carrier (fig8). Bathan also teaches module packages and package stacks minimize occurrence of gross component failure in a more integrated circuit (Bathan, [2, 5]).

It would have been obvious to one having ordinary skill in the art before the effective filing date of the claimed invention to combine the teaching of Gong modified above with the teaching of Bathan to use the interposer of Gong in the chip setup of Bathan. The motivation to do so is to achieve high integration with minimum occurrence of gross component failure in a more integrated circuit (Bathan, [2, 5]).

Claims 34 are rejected under 35 U.S.C. 103 as being unpatentable over Gong et al. US 2013/0049217 in view of Lin et al. US 2009/0155959, Chen et al. US 2013/0277801 and Law et al. US 2010/0252934.

Re claim 34, Gong modified above teaches the chip package of claim 31, wherein said first polymer layer further comprises multiple third copper plugs (Gong, 610, fig6, [32]) extending through a third portion of said first polymer layer from said first surface to said second surface, wherein each of said multiple third and fourth copper plugs has a top surface coplanar to said first surface and a bottom surface coplanar to said second surface (Gong, fig11).

Gong does not explicitly show wherein said multiple third copper plugs are arranged in a first column substantially vertical to said first and second sidewalls, multiple fourth copper plugs extending through a fourth portion of said first polymer layer from said first surface to said second surface, wherein said multiple fourth copper plugs are arranged in a second column substantially vertical to said first and second sidewalls.

Law teaches a layout wherein said multiple third plugs are arranged in a first column substantially vertical to said first and second sidewalls (301 and 303 top, fig5b), multiple fourth plugs extending through a fourth portion (301 and 303 bottom, fig5b) of said first layer from said first surface to said second surface, wherein said multiple fourth plugs are arranged in a second column substantially vertical to said first and second sidewalls.

It would have been obvious to one having ordinary skill in the art before the effective filing date of the claimed invention to combine the teaching of Gong with the teaching of Law to adjust via layout and achieve smaller chip package sizes (Law, [42]).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to XIAOMING LIU whose telephone number is (571)270-0384. The examiner can normally be reached on Monday-Friday, 9am-8pm, EST.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Charles Garber can be reached on (571)272-2194. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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/XIAOMING LIU/
Examiner, Art Unit 2812

Notice of References Cited	Application/Control No. 16/752,650	Applicant(s)/Patent Under Reexamination Yang, Ping-Jung	
	Examiner XIAOMING LIU	Art Unit 2812	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-20130277801-A1	10-2013	CHEN; Nan-Cheng	H01L23/49816	257/532
*	B	US-20130049217-A1	02-2013	Gong; Zhiwei	H01L24/19	257/774
*	C	US-20110257716-A1	10-2011	Tiedtke; Hans-Jurgen	A61N1/0543	607/116
*	D	US-20100252934-A1	10-2010	Law; Oscar M.K.	H01L21/76877	257/774
*	E	US-20090230517-A1	09-2009	Bathan; Henry Descalzo	H01L25/03	257/666
*	F	US-20090155959-A1	06-2009	Lin; Yaojian	H01L25/16	438/124
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Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/752,650	Yang, Ping-Jung
	Examiner	Art Unit
	XIAOMING LIU	2812

CPC - Searched*		
Symbol	**Date**	**Examiner**
H01L23/49827 | H01L23/5384 | H01L2224/08165 | H01L2224/16165 | H01L2224/16235 | H01L2224/32165 | H01L2224/32235 | H01L2224/40165 | H01L2224/40235 | H01L2224/48165 | H01L2224/48235 with date and text	09/17/2020	XL

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Inventor search Conducted, limited with text	09/17/2020	XL
Assignee search Conducted, limited with text	09/17/2020	XL
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Non-Patent Literature searched: science direct, TC2800	09/17/2020	XL

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Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
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	Examiner	Art Unit
	XIAOMING LIU	2812

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner

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Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/752,650	Yang, Ping-Jung
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	XIAOMING LIU	2812

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

CLAIMS

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	09/17/2020								
	1	-								
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Doc description: Information Disclosure Statement (IDS) Filed

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(Not for submission under 37 CFR 1.99)

Application Number	16752650
Filing Date	2020-01-26
First Named Inventor	Ping-Jung Yang
Art Unit	1782
Examiner Name	LIU, XIAOMING
Attorney Docket Number	Mars16-001-US-C01

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	1	10192796		2019-01-29	Lin; Yaojian et al.	
	2	9837303		2017-12-05	Lin; Yaojian et al.	
	3	9704780		2017-07-11	Marimuthu; Pandi C. et al.	
	4	9431331		2016-08-30	Do; Byung Tai et al.	
	5	9048211		2015-06-02	Pagaila; Reza A. et al.	
	6	8987918		2015-03-24	Razdan; Sandeep et al.	
	7	8980691		2015-03-17	Lin; Yaojian	
	8	8846454		2014-09-30	Shim; Il Kwon et al.	

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	Application Number	16752650
	Filing Date	2020-01-26
	First Named Inventor	Ping-Jung Yang
	Art Unit	1782
	Examiner Name	LIU, XIAOMING
	Attorney Docket Number	Mars16-001-US-C01

	9	8648470		2014-02-11	Lin; Yaojian et al.	

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	Application Number	16752650
	Filing Date	2020-01-26
	First Named Inventor	Ping-Jung Yang
	Art Unit	1782
	Examiner Name	LIU, XIAOMING
	Attorney Docket Number	Mars16-001-US-C01

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	16752650
	Filing Date	2020-01-26
	First Named Inventor	Ping-Jung Yang
	Art Unit	1782
	Examiner Name	LIU, XIAOMING
	Attorney Docket Number	Mars16-001-US-C01

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

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See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Ping-Jung Yang/	Date (YYYY-MM-DD)	2020-08-13
Name/Print	Ping-Jung Yang	Registration Number	

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7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

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Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (01-10)
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
	Application Number	
	Filing Date	
	First Named Inventor	Ping-Jung Yang
	Art Unit	
	Examiner Name	
	Attorney Docket Number	Mars16-001-US-C01

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	4221047		1980-09-09	Narken et al.	
	2	4639543		1987-01-27	Fang	
	3	4975103		1990-12-04	Ackermann et al.	
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	Examiner Name	
	Attorney Docket Number	Mars16-001-US-C01

	9	6309901		2001-10-30	Tahon et al.	
	10	6339197		2002-01-15	Fushie et al.	
	11	6539750		2003-04-01	Takagi et al.	
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	20	7071521		2006-07-04	Leib et al.	
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	Examiner Name	
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	32	7808799		2007-11-15	Tadahiko Kawabe	
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	Attorney Docket Number	Mars16-001-US-C01

	42	9147638		2015-09-29	Liu; Yueli et al.	
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Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
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	6	20080283277		2008-11-20	Muramatsu et al.	
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	17	20110026232		2011-02-03	Lin et al.	
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	28	20130307140		2013-11-21	HUANG; Hui-Min et al.	
	29	20140103488		2014-04-17	Chen; Hsu-Hsien et al.	
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	35	20170345761		2017-11-30	Yu; Chen-Hua et al.	
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	38	20110147055		2011-06-23	Qing Ma. et al.	

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	39	20110242050		2011-10-06	San-ho BYUN et al.	
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	41	20070268581		2007-11-22	Palmateer; Lauren	

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	1	2012/0068271	wo		2012-03-22	Semiconductor Energy Laboratory Co., Ltd.		
	2	2013/138452	wo		2013-09-19	QUALCOMM MEMS TECHNOLOGIES, INC.		

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Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

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	Examiner Name	
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CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Ping-Jung Yang/	Date (YYYY-MM-DD)	2020-01-26
Name/Print	Ping-Jung Yang	Registration Number	

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

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3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

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EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	2	("20200161245").PN.	US-PGPUB; USPAT; USOCR; DERWENT	OR	OFF	2020/09/10 12:31
S2	2	S1 and polymer and copper	US-PGPUB; USPAT; USOCR; DERWENT	OR	OFF	2020/09/10 13:04
S3	277	(US-20120282739-$ or US-20120319254-$ or US-20120089180-$ or US-20100244059-$ or US-20090179317-$ or US-20090127638-$ or US-20070135550-$ or US-20110127314-$ or US-20090160053-$ or US-20110204513-$ or US-20100260224-$ or US-20060081877-$ or US-20120174855-$ or US-20100200898-$ or US-20110233754-$ or US-20130280826-$ or US-20130292808-$ or US-20120062439-$ or US-20080308917-$ or US-20040238857-$ or US-20130241077-$ or US-20100059855-$ or US-20110188193-$ or US-20110165734-$ or US-20090230531-$ or US-20090152714-$).did. or (US-20090152692-$ or US-20080211084-$ or US-20070132093-$ or US-20050224937-$ or US-20130105967-$ or US-20070158818-$ or US-20130161784-$ or US-20120199843-$ or US-20120193802-$ or US-20120161163-$ or US-20120132817-$ or US-20120049366-$ or US-20060270079-$ or US-20130193465-$ or US-20130234318-$ or US-20130113091-$ or US-20110260308-$ or US-20040238956-$ or US-20080182398-$ or US-20150214206-$ or US-20150221624-$ or US-20140035134-$ or US-20100078781-$ or US-20140312497-$ or US-20140160699-$ or US-20110215444-$ or US-20150262931-$).did. or (US-20150108661-$ or US-20100184256-$	US-PGPUB; USPAT; USOCR; DERWENT	OR	OFF	2020/09/10 13:39

		or US-20090256670-$ or US-20080150119-$ or US-20050253231-$ or US-20030096089-$ or US-20150342060-$ or US-20120094442-$ or US-20110115083-$ or US-20140217436-$ or US-20140048949-$ or US-20130214386-$ or US-20120086117-$ or US-20120049363-$ or US-20120032282-$ or US-20140264810-$ or US-20120160647-$ or US-20100000775-$ or US-20070243704-$ or US-20050090035-$ or US-20050151272-$ or US-20100019373-$ or US-20140118978-$ or US-20120293977-$ or US-20110227223-$ or US-20090236730-$ or US-20080049392-$).did. or (US-20090096070-$ or US-20130168857-$ or US-20110309526-$ or US-20080211111-$ or US-20080277802-$ or US-20070080469-$ or US-20140246223-$ or US-20150162194-$ or US-20160343592-$ or US-20140054796-$ or US-20130343067-$ or US-20130017652-$ or US-20120306104-$ or US-20120019123-$ or US-20110291541-$ or US-20110222280-$ or US-20100171139-$ or US-20120305977-$ or US-20150021754-$ or US-20110121449-$ or US-20150221614-$ or US-20130200531-$ or US-20130062761-$ or US-20120028411-$ or US-20130295725-$ or US-20060194370-$ or US-20080212288-$).did. or (US-7589405-$ or US-8906794-$ or US-6614122-$ or US-8558399-$ or US-8432022-$ or US-8228682-$ or US-8982577-$ or US-4706167-$ or US-5531020-$ or US-8252615-$ or US-6331451-$ or US-8946886-$ or US-8415785-$ or US-5804881-$ or US-9786623-$ or US-9040352-$ or US-7855391-$ or US-8507927-$ or US-7619901-$ or US-9768038-$ or US-9627261-$ or US-5250843-$ or US-9735113-$ or US-9431316-$ or US-8617935-$ or US-8518749-$).did. or (US-8482134-$ or US-8258012-$ or US-8105872-$ or US-7955942-$ or US-7846777-$ or US-7727806-$).did.				

S4	121	("10192796" | "8648470" | "8846454" | "8980691" | "8987918" | "9048211" | "9431331" | "9704780" | "9837303" | "10043768" | "8742579" | "8786060" | "8796137" | "8883561" | "8895440" | "8916421" | "8952489" | "8952521" | "8993377" | "9082806" | "9224647" | "9281292" | "9324672" | "9331060" | "9343442" | "9362187" | "9385006" | "9385009" | "9397050" | "9406619" | "9406658" | "9508626" | "9524955" | "9593009" | "9679863" | "9704843" | "9735113" | "20020038725" | "20020145197" | "20020159243" | "20050012217" | "20060006539" | "20060020371" | "20070045841" | "20070268581" | "20080054457" | "20080080111" | "20080113505" | "20080129439" | "20080149384" | "20080150623" | "20080283277" | "20080284014" | "20080318361" | "20090109655" | "20090174065" | "20090273073" | "20100164030" | "20100200898" | "20100246152" | "20100290191" | "20110026232" | "20110065250" | "20110089574" | "20110147055" | "20110242050" | "20130292846" | "20130307140" | "20140103488" | "20140210101" | "20140252646" | "20140264839" | "20140367160" | "20150166329" | "20170345761" | "20170345764" | "20170373004" | "4221047" | "4639543" | "4975103" | "5294238" | "5705855" | "6156413" | "6177707" | "6194762" | "6265771" | "6309901" | "6339197" | "6434016" | "6539750" | "6673698" | "6691409" | "6772514" | "6799438" | "6839946" | "6894358" | "6989604" | "7038309" | "7071521" | "7072018" | "7091589" | "7151009" | "7259080" | "7279771" | "7285834" | "7337540" | "7362403" | "7476623" | "7557440" | "7749900" | "7808799" | "7993510" | "8207453" | "8338238" | "8354297" | "8822281" | "8878360" | "9048233" | "9147638" | "9385105" | "9627365").PN.	US-PGPUB; USPAT	OR	OFF	2020/09/10 13:40
S5	19	((("YANG") near3 ("Ping-Jung"))).INV.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2020/09/10 13:40

S6	3,569	(H01L2224/45147).CPC.	US-PGPUB	OR	OFF	2020/09/10 13:42
S7	2	("20200161245").PN.	US-PGPUB; USPAT; USOCR; DERWENT	OR	OFF	2020/09/10 13:42
S8	799	S6 and polymer and chip	US-PGPUB	OR	OFF	2020/09/10 13:43
S9	2	("2009/0315171").URPN.	USPAT	OR	OFF	2020/09/10 13:48
S10	5	("20080277783" | "20090315171" | "20110110061" | "8318537" | "9064757").PN. OR ("9437534").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2020/09/10 13:49
S11	9	("2011/0110061").URPN.	USPAT	OR	OFF	2020/09/10 13:50
S12	1,645	((("YUAN") near3 ("Zhongfa")) OR (("LIU") near3 ("Yong")) OR (("LIU") near3 ("Yumin")) OR (("QIAN") near3 ("Qiuxiao"))).INV.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2020/09/10 13:54
S13	28	S12 and copper and polymer	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2020/09/10 13:55
S14	18	("2009/0184403").URPN.	USPAT	OR	OFF	2020/09/10 13:58
S15	4	("20090184403").PN. OR ("8614120").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2020/09/10 13:58
S16	20,179	(H01L23/49827 | H01L23/5384 | H01L2224/08165 | H01L2224/16165 | H01L2224/16235 | H01L2224/32165 | H01L2224/32235 | H01L2224/40165 | H01L2224/40235 | H01L2224/48165 | H01L2224/48235).CPC.	US-PGPUB; USPAT; USOCR	OR	OFF	2020/09/10 14:05
S17	6,787	S16 and copper and polymer	US-PGPUB; USPAT; USOCR	OR	OFF	2020/09/10 14:05
S18	2,733	S16 and copper same polymer	US-PGPUB; USPAT; USOCR	OR	OFF	2020/09/10 14:05
S19	970	S16 and cpu same gpu	US-PGPUB; USPAT; USOCR	OR	OFF	2020/09/10 14:11

S20	82	S16 and cpu same gpu same passive	US-PGPUB; USPAT; USOCR	OR	OFF	2020/09/10 14:15
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S24	2	"20130242493"	US-PGPUB; USPAT;	OR	OFF	2020/09/10 18:34

			USOCR; DERWENT			
S25	32	("2013/0242493").URPN.	USPAT	OR	OFF	2020/09/10 18:36
S27	21	"ppm/.degree.C"	USPAT	OR	OFF	2020/09/10 18:42
S28	1,788	polymer same expansion adj coefficient	USPAT	OR	OFF	2020/09/10 18:45
S29	446	polymer near10 expansion adj coefficient	USPAT	OR	OFF	2020/09/10 18:45
S34	3	"20110257716"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2020/09/10 18:55
S35	46	(US-20110304008-$ or US-20120313207-$ or US-20120241938-$ or US-20120193785-$ or US-20120052631-$ or US-20110297434-$ or US-20110026232-$ or US-20100290191-$ or US-20100207154-$ or US-20100200898-$ or US-20100102457-$ or US-20100044850-$ or US-20090315171-$ or US-20110110061-$ or US-20100123257-$ or US-20100052119-$ or US-20090184403-$ or US-20120326170-$ or US-20130050228-$ or US-20130049217-$ or US-20120313209-$ or US-20120306096-$ or US-20120228749-$ or US-20140124777-$ or US-20140042637-$ or US-20130328211-$).did. or (US-20130292844-$ or US-20130119562-$ or US-20100258944-$ or US-20100258946-$ or US-20100252937-$ or US-20080149384-$ or US-20130277855-$ or US-20170373004-$ or US-20170345761-$ or US-20130242493-$).did. or (US-9437534-$ or US-8247269-$ or US-8614120-$ or US-7968978-$ or US-9627365-$ or US-9817312-$ or US-9615453-$ or US-9363890-$ or US-9161443-$ or US-9030751-$).did.	US-PGPUB; USPAT	OR	OFF	2020/09/10 18:58
S37	30	S35 and polyimide	US-PGPUB; USPAT	OR	ON	2020/09/10 19:00

S38	65	(US-20160181184-$ or US-20170062361-$ or US-20160163666-$ or US-20150206934-$ or US-20140021618-$ or US-20120208129-$ or US-20180062386-$ or US-20160173039-$ or US-20160087588-$ or US-20110241793-$ or US-20110057742-$ or US-20100032818-$ or US-20100001363-$ or US-20130147540-$ or US-20190259758-$ or US-20190252306-$ or US-20150179591-$ or US-20140346663-$ or US-20140312362-$ or US-20140077362-$ or US-20130200528-$ or US-20130026658-$ or US-20100165585-$ or US-20160071820-$).did. or (US-6659663-$ or US-10153553-$ or US-6829152-$ or US-10580726-$ or US-10090266-$ or US-9972555-$ or US-8168470-$ or US-9954028-$ or US-10177115-$).did.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2020/09/10 22:50
S39	1,659	((("STATS") near3 ("CHIPPAC") near3 ("LTD"))).AS,AANM.	USPAT	OR	OFF	2020/09/10 22:51
S40	3	"20090230517"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2020/09/10 22:57
S41	3	"20090155959"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2020/09/10 23:20
S42	3	"20130049217"	US-PGPUB; USPAT; USOCR; DERWENT	OR	OFF	2020/09/11 10:28
S44	3	"20090155959"	US-PGPUB; USPAT; USOCR; DERWENT	OR	OFF	2020/09/11 10:34
S45	2	"20090155959" and passive	US-PGPUB; USPAT; USOCR; DERWENT	OR	OFF	2020/09/11 10:35

S46	3	"20090230517"	US-PGPUB; USPAT; USOCR; DERWENT	OR	OFF	2020/09/11 10:57
S47	20,179	(H01L23/49827 | H01L23/5384 | H01L2224/08165 | H01L2224/16165 | H01L2224/16235 | H01L2224/32165 | H01L2224/32235 | H01L2224/40165 | H01L2224/40235 | H01L2224/48165 | H01L2224/48235).CPC.	US-PGPUB; USPAT; USOCR	OR	OFF	2020/09/11 11:06
S48	537	S47 and cpu same gpu same DRAM	US-PGPUB; USPAT; USOCR	OR	OFF	2020/09/11 11:06
S49	127	S47 and cpu same gpu same DRAM and integration	US-PGPUB; USPAT; USOCR	OR	OFF	2020/09/11 11:06
S50	20,179	(H01L23/49827 | H01L23/5384 | H01L2224/08165 | H01L2224/16165 | H01L2224/16235 | H01L2224/32165 | H01L2224/32235 | H01L2224/40165 | H01L2224/40235 | H01L2224/48165 | H01L2224/48235).CPC.	US-PGPUB; USPAT; USOCR	OR	OFF	2020/09/11 13:47
S51	146	S50 and tsv same layout	US-PGPUB; USPAT; USOCR	OR	OFF	2020/09/11 13:47
S52	6	"20130049217" "20090155959" "20090230517" "20130277801" "20110257716" "20100252934"	US-PGPUB	OR	OFF	2020/09/17 16:44

EAST Search History (Interference)

<This search history is empty>

9/17/2020 4:58:50 PM
C:\Users\xliu3\Documents\EAST\Workspaces\202001\16752650_1.wsp

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (01-10)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT
(Not for submission under 37 CFR 1.99)

Application Number	16752650
Filing Date	2020-01-26
First Named Inventor	Ping-Jung Yang
Art Unit	1782
Examiner Name	
Attorney Docket Number	Mars16-001-US-C01

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	9362187		2016-06-07	Ossimitz; Peter	
	2	9593009		2017-03-14	Fuergut; Edward et al.	
	3	9704843		2017-07-11	Kilger; Thomas et al.	
	4	10043768		2018-08-07	Meyer; Thorsten et al.	
	5	8952489		2015-02-10	Elian; Klaus et al.	
	6	8952521		2015-02-10	Wojnowski; Maciej et al.	
	7	9331060		2016-05-03	Otremba; Ralf et al.	
	8	9735113		2017-08-15	Chi; HeeJo et al.	

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /X.L/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	16752650
	Filing Date	2020-01-26
	First Named Inventor	Ping-Jung Yang
	Art Unit	1782
	Examiner Name	
	Attorney Docket Number	Mars16-001-US-C01

	9	9679863		2017-06-13	Lin; Yaojian et al.	
	10	9524955		2016-12-20	Huang; Rui et al.	
	11	9508626		2016-11-29	Pagaila; Reza A. et al.	
	12	9406658		2016-08-02	Lee; Chun-Che et al.	
	13	9406619		2016-08-02	Pagaila; Reza A. et al.	
	14	9397050		2016-07-19	Shin; HanGil et al.	
	15	9385009		2016-07-05	Lin; Yaojian et al.	
	16	9385006		2016-07-05	Lin; Yaojian	
	17	9343442		2016-05-17	Chen; Chih-Hua et al.	
	18	9324672		2016-04-26	Pagaila; Reza A. et al.	
	19	9281292		2016-03-08	Hu; Chuan et al.	

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /X.L/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	16752650
	Filing Date	2020-01-26
	First Named Inventor	Ping-Jung Yang
	Art Unit	1782
	Examiner Name	
	Attorney Docket Number	Mars16-001-US-C01

	20	9224647		2015-12-29	Koo; Jun Mo et al.	
	21	9082806		2015-07-14	Lin; Yaojian et al.	
	22	8993377		2015-03-31	Koo; Jun Mo et al.	
	23	8916421		2014-12-23	Gong; Zhiwei et al.	
	24	8895440		2014-11-25	Choi; DaeSik et al.	
	25	8883561		2014-11-11	Park; DongSam et al.	
	26	8796137		2014-08-05	Pagaila; Reza A. et al.	
	27	8786060		2014-07-22	Yen; Han-Chee et al.	
	28	8742579		2014-06-03	Pagaila; Reza A. et al.	

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U.S.PATENT APPLICATION PUBLICATIONS Remove

Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	16752650
	Filing Date	2020-01-26
	First Named Inventor	Ping-Jung Yang
	Art Unit	1782
	Examiner Name	
	Attorney Docket Number	Mars16-001-US-C01

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Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2]	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1							

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Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1		

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EXAMINER SIGNATURE

Examiner Signature	/XIAOMING LIU/	Date Considered	09/17/2020

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /X.L/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	16752650
	Filing Date	2020-01-26
	First Named Inventor	Ping-Jung Yang
	Art Unit	1782
	Examiner Name	
	Attorney Docket Number	Mars16-001-US-C01

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Ping-Jung Yang/	Date (YYYY-MM-DD)	2020-03-08
Name/Print	Ping-Jung Yang	Registration Number	

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /X.L/

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /X.L/

Bibliographic Data

Application No: 16/752,650

Foreign Priority claimed: ○ Yes ◉ No

35 USC 119 (a-d) conditions met: ☐ Yes ☑ No ☐ Met After Allowance

Verified and Acknowledged: /XIAOMING LIU/ (Examiner's Signature) | (Initials)

Title: METHOD FOR FABRICATING GLASS SUBSTRATE PACKAGE

FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
01/26/2020	257	2812	Mars16-001-US-C01
RULE			

APPLICANTS

Ping-Jung Yang, Hsin-Chu City, TAIWAN

INVENTORS

Ping-Jung Yang, Hsinchu City, TAIWAN

CONTINUING DATA

This application is a CON of 15261956 09/11/2016 PAT 10622310

15261956 has PRO of 62219249 09/16/2015

15261956 is a CIP of 14036256 09/25/2013 PAT 9615453

14036256 has PRO of 61705649 09/26/2012

FOREIGN APPLICATIONS

IF REQUIRED, FOREIGN LICENSE GRANTED**

02/12/2020

**** SMALL ENTITY ****

STATE OR COUNTRY

TAIWAN

ADDRESS

PING-JUNG YANG
NO 2, NIOUPU SOUTH RD., SIANGSHAN DISTRICT
HSINCHU CITY, 30091
TAIWAN

FILING FEE RECEIVED

$785

Docket No.: Mars-16-001-US-C01 **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	Customer Number: 102851
Ping-Jung Yang	:	Confirmation Number: 4809
Application No.: 16752650	:	Group Art Unit: 2812
Filed: Jan. 26, 2020	:	Examiner: LIU, XIAOMING

For: CHIP PACKAGE

RESPONSE TO OFFICE ACTION

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In response to the non-final Office action dated Sept. 21, 2020, please amend the above-identified application as follows:

Amendments to Specification are reflected in the substitute specification with markings (marked up version) and substitute specification without markings (clean version), both submitted herewith, as required and in compliance with 37 CFR §§ 1.52, 1.121, 1.125, which hereby corrects and replaces the substitute specification of the above-captioned application filed on Jan. 26, 2020.

Amendments to the Claims are reflected in the listing of claims which begins on page 12 of this paper.

Remarks/Arguments begin on page 22 of this paper.

IPR2026-00067
TSMC EX1032 Page 308

~~METHOD FOR FABRICATING GLASS SUBSTRATE~~ CHIP PACKAGE

[0001] This patent application is a continuation of application No. 15261956, filed Sept. 11, 2016, now pending, which claims priority benefits from U.S. provisional patent application No. 62/219249, filed Sept. 16, 2015. This patent application of application No. 15261956 is a continuation-in-part of application No. 14/036256, filed Sept. 25, 2013, now patent No. 9615453, which claims the benefit of priority from U.S. provisional patent application No. 61/705,649, filed Sept. 26, 2012, all of which is incorporated herein by reference in their entirety.

BACKGROUND OF THE DISCLOSURE

Field of the Disclosure

[0002]The patent disclosure a method and structure to manufacture a glass substrate, and disclosed embodiments relate to one or more chip building a system on the glass substrate.

Brief Description of the Related Art

[0003] As is well known, microelectronic devices have a tendency to be minimized and thinned with its functional development and a semiconductor package mounted on a mother board is also following the tendency in order to realize a mounting of high integration.

IPR2026-00067
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[0004] When the geometric dimensions of the Integrated Circuits are scaled down, the cost per die is decreased while some aspects of performance are improved. The metal connections which connect the Integrated Circuit to other circuit or system components become of relative more importance and have, with the further miniaturization of the IC, an increasingly negative impact on the circuit performance. The parasitic capacitance and resistance of the metal interconnections increase, which degrades the chip performance significantly. Of most concern in this respect is the voltage drop along the power and ground buses and the RC delay of the critical signal paths. Attempts to reduce the resistance by using wider metal lines result in higher capacitance of these wires.

[0005] To solve this problem, the approach has been taken to develop low resistance metal (such as copper) for the wires while low dielectric materials are used in between signal lines.

[0006] Increased Input-Output (IO) combined with increased demands for high performance, and then IC's has led to the development of ~~Flip-Chip~~ flip-chip Packages. Flip-chip technology fabricates bumps (typically Pb/Sn solders) on Al pads of ~~on~~ chip and ~~interconnect~~ interconnects the bumps directly to the package media, which are usually ceramic or plastic based. The flip-chip is bonded face down to the package medium through the shortest path. These technologies can be applied not only to single-chip packaging, but also to higher or integrated levels of packaging in which the packages are larger and to more sophisticated substrates that accommodate several chips to form larger functional units.

[0007] The flip-chip technique, using an area array, has the advantage of achieving the highest density of interconnection to the device and a very low inductance interconnection to the package. However, pre-testability, post-bonding visual inspection, and TCE (Temperature Coefficient of Expansion) matching to avoid solder bump fatigue are still challenges.

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[0008] Glass can be used as an interposer to bridge between one or more IC chips and a printed circuit board. In many respects, when used as an interposer / substrate and without the requirement for active devices, glass can be a good substitute for a silicon interposer. The advantages of glass in comparison to silicon as an interposer lie in its much lower material cost. Glass also has a CTE closely matched to silicon, so that reliability of interconnects, especially micro-bonds, can be expected to be quite good. Glass has some disadvantages in comparison to silicon – notably its lower thermal conductivity and the difficulty in forming Through Glass Vias (TGV's). Both of these topics are discussed elsewhere in this patent.

SUMMARY OF THE DISCLOSURE

[0009] Embodiments of the present disclosure provide A display device comprises a display panel substrate and a glass substrate over said display panel substrate, wherein said display panel substrate comprises multiple contact pads, a display area, a first boundary, a second boundary, a third boundary and a fourth boundary, wherein said display area comprises a first edge, a second edge, a third edge and a fourth edge, wherein said first boundary is parallel to said third boundary and said first and third edges, wherein said second boundary is parallel to said fourth boundary and said second and fourth edges, wherein a first least distance between said first boundary and said first edge, wherein a second least distance between said second boundary and said second edge, a third least distance between said third boundary and said third edge, a fourth distance between said fourth boundary and said fourth edge, and wherein said first, second, third and fourth least distances are smaller than 100 micrometers, and wherein said glass substrate comprising multiple metal conductors through in said glass substrate and multiple metal bumps are between said glass substrate and said display panel substrate, wherein said one of said metal conductors is connected to one of said contact pads through one of said metal bumps.

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[0010] These, as well as other components, steps, features, benefits, and advantages of the present disclosure, will now become clear from a review of the following detailed description of illustrative embodiments, the accompanying drawings, and the claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] The drawings disclose illustrative embodiments. They do not set forth all embodiments. Other embodiments may be used in addition or instead. Details that may be apparent or unnecessary may be omitted to save space or for more effective illustration. Conversely, some embodiments may be practiced without all of the details that are disclosed. When the same numeral appears in different drawings, it refers to the same or like components or steps.

[0012] Aspects of the disclosure may be more fully understood from the following description when read together with the accompanying drawings, which are to be regarded as illustrative in nature, and not as limiting. The drawings are not necessarily to scale, emphasis instead being placed on the principles of the disclosure.

[0013] Figs. 1 illustrates a three-dimensional view of a X-axis nets and a Y-axis nets, in accordance with the present disclosure.

[0014] Fig. 2 illustrates a cross-section view of the X-axis nets and the Y-axis nets, in accordance with the present disclosure.

[0015] Fig. 3 illustrates a cross-section view of the Z-axis traces crossed to the X-axis nets and the Y-axis nets, in accordance with the present disclosure.

[0016] Fig. 4 illustrates a three-dimensional view of the Z-axis traces, X-axis nets and the Y-axis nets, in accordance with the present disclosure.

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[0017] ~~Fig. 5a-5i~~ Figs. 5a-5i illustrate the shape and structure of the Z-axis traces, in accordance with the present disclosure.

[0018] Figs. 6a-6j ~~are~~ illustrate a 1st process of forming a glass substrate, in accordance with the present disclosure.

[0019] Figs. 6k-6n illustrate a top views of the 1st process of forming the glass substrate, in accordance with the present disclosure.

[0020] Figs. 7a-7o ~~are~~ illustrate a 2nd process of forming the glass substrate, in accordance with the present disclosure.

[0021] Figs. 7p-7r illustrate a top views of the 2nd process of forming the glass substrate, in accordance with the present disclosure.

[0022] Figs. 8a-8d illustrate cross-section views of the glass substrate and the metal plug, in accordance with the present disclosure.

[0023] Figs. 9a-9s illustrate a process to form multiple traces on a top surface and a bottom surface of the glass substrate, in accordance with the present disclosure.

[0024] Figs. 9t-9u illustrate cross-section views of multiple chips formed on the glass substrate, in accordance with the present disclosure.

[0025] Fig. 9v illustrates a cross-section view of the metal bump, in accordance with the present disclosure.

[0026] Fig. 9w illustrates a cross-section view of multiple chips formed on a top surface and bottom surface of the glass substrate, in accordance with the present disclosure.

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[0027] Fig. 9x illustrates a cross-section view of multiple chips and a 3D-IC package formed on a top surface and bottom surface of the glass substrate, in accordance with the present disclosure.

[0028] Fig. 9y illustrates a top views of the multiple chips on the glass substrate, in accordance with the present disclosure.

[0029] Figs. 10a-10j ~~illustrates~~ illustrate a damascene process to form the metal layer on the glass substrate, in accordance with the present disclosure.

[0030] Figs. 11a-11i ~~illustrates~~ illustrate an embossing process to form the metal layer on the glass substrate, in accordance with the present disclosure.

[0031] Fig. 12 illustrates a cross-section view of the glass substrate of the first application formed on an OLED display substrate, in accordance with the present disclosure.

[0032] Fig. 13 illustrates a cross-section view of the glass substrate of the second application formed on a MEMs display substrate, in accordance with the present disclosure.

[0033] Fig. 14 illustrates a cross-section view of the glass substrate of the third application formed on a LCD display substrate, in accordance with the present disclosure.

[0034] Fig. 15 illustrates a cross-section view of the glass substrate of the fourth application formed on an another LCD display substrate, in accordance with the present disclosure.

[0035] Fig. 16 illustrates a cross-section view of the glass substrate of the fifth application formed on an OLED display substrate, in accordance with the present disclosure.

[0036] Fig. 17a illustrates a cross-section view of the glass substrate of the sixth application formed on an OLED display substrate, in accordance with the present disclosure.

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[0037] Fig. 17b illustrates a cross-section view of the structure of the OLED display substrate, in accordance with the present disclosure.

[0038] Fig. 18 illustrates a three-dimensional view of the display device, in accordance with the present disclosure.

[0039] Fig. 19 illustrates a big display device combined from multiple display device, in accordance with the present disclosure.

[0040] While certain embodiments are depicted in the drawings, one skilled in the art will appreciate that the embodiments depicted are illustrative and that variations of those shown, as well as other embodiments described herein, may be envisioned and practiced within the scope of the present disclosure.

DETAILED DESCRIPTION OF THE DISCLOSURE

[0041] Fig. 1 illustrates a three-dimensional view of a net 2, 4, wherein the net 4 is under the net 2, wherein the net 2 comprises multiple Y-axis traces 2a and multiple X-axis traces 2b under the Y-axis traces 2a, and wherein the net 4 comprises multiple Y-axis traces 4a and multiple X-axis traces 4b under the Y-axis traces 4a. Multiple gaps 3~~,~~ and 5 ~~form~~ are formed in the net 2 and 4. Each of the traces 2a, 2b, 4a and 4b is easily ~~move~~ moved to change the size of gaps 3 and gaps 5. The diameter (or width) of traces 2a, 2b, 4a and 4b are the same, such as between 10 and 30 micrometers, between 20 and 100 micrometers, between 40 and 150 micrometers, between 50 and 200 micrometers, between 200 and 1000 micrometers or between 500 and 10000 micrometers. The traces 2a, 2b, 4a and 4b may be metal traces or polymer traces, such as copper traces, copper-gold alloy traces, copper-gold-palladium alloy traces, copper-gold-silver alloy traces, copper-platinum alloy traces, copper-iron alloy traces, copper-nickel alloy traces, copper-tungsten traces, tungsten traces, brass

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wires, zinc plated brass wires, stainless wires, nickel plated stainless wires, phosphor bronze wires, copper plated the aluminum wires, aluminum traces, phenolic resin traces, epoxy resin traces, melamine-formaldehyde resin traces or polysiloxanes resin traces. The cross-section shape of traces 2a, 2b, 4a and 4b may be a circular shape, a Square shape, an oblong shape, a rectangle shape or a flat shape.

[0042] Fig. 2 illustrates a cross-section view of the net 2 and the net 4. The gaps 3 and gaps 5 are aligned with each other.

[0043] Next, referring to Fig. 3, multiple metal traces 6 are crossed the net 2 and the net 4 through the gaps 3 and gaps 5. The diameter (or width) of metal traces 6 is between 10 and 30 micrometers, between 20 and 100 micrometers, between 40 and 150 micrometers, between 50 and 200 micrometers, between 200 and 1000 micrometers or between 500 and 10000 micrometers. The traces 6 may be metal traces, such as copper traces, copper-gold alloy traces, copper-gold-palladium alloy traces, copper-gold-silver alloy traces, copper-platinum alloy traces, copper-iron alloy traces, copper-nickel alloy traces, copper-tungsten traces, tungsten traces, brass wires, zinc plated brass wires, stainless wires, nickel plated stainless wires, phosphor bronze wires, copper plated the aluminum wires, aluminum traces, titanium-containing layer plated the copper wires, tantalum-containing layer plated the copper wires. The cross-section shape of traces 6 may be a circular shape, a square shape, an oblong shape, a rectangle shape or a flat shape. The diameter (or width) of traces 6 may be the same with the traces 2a, 2b, 4a and 4b or different with the traces 2a, 2b, 4a and 4b.

[0044] Furthermore, we proposed the material of the traces 6 is copper-tungsten alloy, wherein the copper in the copper-tungsten alloy is 50 percent and the tungsten in the copper-tungsten alloy is 50 percent, the copper in the copper-tungsten alloy is 60 percent and the tungsten in the copper-tungsten alloy is 40 percent, the copper in the copper-tungsten alloy is 70 percent and the tungsten in

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the copper-tungsten alloy is 30 percent, the copper in the copper-tungsten alloy is 80 percent and the tungsten in the copper-tungsten alloy is 20 percent, the copper in the copper-tungsten alloy is 90 percent and the tungsten in the copper-tungsten alloy is 10 percent, the copper in the copper-tungsten alloy is 40 percent and the tungsten in the copper-tungsten alloy is 60 percent, the copper in the copper-tungsten alloy is 30 percent and the tungsten in the copper-tungsten alloy is 70 percent.

[0045] Fig. 4 illustrates a three-dimensional view of a net 2, 4 and traces 6.

[0046] Fig. 5a-5i ~~illustrates~~ illustrate the shape and structure of the traces 6. In Fig. 5a, the cross-section shape of traces 6 is a circular shape. In Fig. 5d, the cross-section shape of traces 6 is a square shape. In Fig. 5g, the cross-section shape of traces 6 is a rectangle shape. In Fig. 5b, the cross-section shape of traces 6 is a circular shape and a first covering layer 6a is cover on the traces 6, wherein the first covering layer 6a may be a metal layer, such as a nickel-containing layer, a zinc-containing layer, a titanium-containing layer, a tantalum-containing layer, a silver-containing layer, a chromium-containing layer and wherein the first covering layer 6a may be an anti-oxidation layer, such as an oxide-containing layer. In Fig. 5e, the cross-section shape of traces 6 is a square shape and a first covering layer 6a is cover on the traces 6, wherein the first covering layer 6a may be a metal layer, such as a nickel-containing layer, a zinc-containing layer, a titanium-containing layer, a tantalum-containing layer, a silver-containing layer, a chromium-containing layer and wherein the first covering layer 6a may be an anti-oxidation layer, such as an oxide-containing layer. In Fig. 5h, the cross-section shape of traces 6 is a rectangle shape and a first covering layer 6a is cover on the traces 6, wherein the first covering layer 6a may be a metal layer, such as a nickel-containing layer, a zinc-containing layer, a titanium-containing layer, a tantalum-containing layer, a silver-containing layer, a chromium-containing layer and wherein the first covering layer 6a may be an anti-oxidation layer, such as an oxide-containing layer. In Fig. 5c, the cross-section shape of traces 6 is a circular shape and a second covering layer 6b is cover on the first covering layer 6a, wherein the second

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covering layer 6b may be an adhesion layer, such as a nickel-containing layer, a zinc-containing layer, a titanium-containing layer, a tantalum-containing layer, a silver-containing layer, a chromium-containing layer and wherein the first covering layer 6a may be an anti-oxidation layer, such as an oxide-containing layer. In Fig. 5f, the cross-section shape of traces 6 is a square shape and a second covering layer 6b is cover on the first covering layer 6a, wherein the second covering layer 6b may be an adhesion layer, such as a nickel-containing layer, a zinc-containing layer, a titanium-containing layer, a tantalum-containing layer, a silver-containing layer, a chromium-containing layer and wherein the first covering layer 6a may be an anti-oxidation layer, such as an oxide-containing layer. In Fig. 5i, the cross-section shape of traces 6 is an oblong shape and a second covering layer 6b is cover on the first covering layer 6a, wherein the second covering layer 6b may be an adhesion layer, such as a nickel-containing layer, a zinc-containing layer, a titanium-containing layer, a tantalum-containing layer, a silver-containing layer, a chromium-containing layer and wherein the first covering layer 6a may be an anti-oxidation layer, such as an oxide-containing layer.

[0047] Next, Figs. 6a-6j are illustrated a 1st process of forming a glass substrate of the invention. Please referring to Fig. 6a, the traces 6 are stretched to a suitable length L1, e.g., smaller than 5 meters, such as between 0.5 and 1 meter, or between 1 and 3 meters. ~~In~~ At the same time, the net 4 is moved down to a suitable location. The pitch t1 between the traces 2a, 2b, 4a, 4b is greater than the diameter (or width) of traces 6.

[0048] Next, referring to Fig. 6b, the traces 2a, 2b, 4a and 4b are moved to change the pitch t1 to a pitch t2, then the traces 6 are closed up to a pitch t3. The pitch t3 substantially the same with the diameter (or width) of the traces 2a, 2b, 4a and 4b, such as between 5 and 20 micrometers, between 20 and 50 micrometers, between 30 and 80 micrometers, between 20 and 100 micrometers, between 40 and 150 micrometers, between 50 and 200 micrometers, between 200 and 1000 micrometers or

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between 500 and 10000 micrometers. ~~In~~ At the same time, ~~may be apply~~ maybe applied a force to stretch the traces 6, 2a, 2b, 4a and 4b and make the traces 6 keep strength and keep the pitch t3 fixed.

[0049] Next, referring to Fig. 6c, a thermal resistance layer 8 is formed on surfaces of the net 4. The thermal resistance layer 8 may be a polymer layer, such as a thermosetting resin, phenolic resin, epoxy resin, melamine-formaldehyde resin, polysiloxanes resin, plaster layer, wherein the thermal resistance layer 8 has a heat deflection temperature between 400 and 900 ℃. When a liquid thermal resistance layer 8 formed on the net 4 and the thermal resistance layer 8 permeated the net 4 through the gaps 5, wherein the thermal resistance layer 8 ~~cover~~ covers the gaps 5 between traces 4a, traces 4b and traces 6, then curing the thermal resistance layer 8. The thermal resistance layer 8 has a thickness between 0.05 and 1 meter.

[0050] 此Next, referring to Fig. 6d, a mold 10 is provided between the net 2 and the net 4, wherein the mold 10 surrounds the traces 6 and on the thermal resistance layer 8. The mold 10 is ~~hold~~ held up by a machine or a device. The mold 10 may be a metal mold, a ceramics mold or a polymer mold, which has a heat deflection temperature between 400 ℃ and 900 ℃ or between 800 ℃ and 1300 ℃.

[0051] Next, referring to Fig. 6e, a fixed layer 12 is formed on the thermal resistance layer 8, wherein the fixed layer 12 may be a glass layer or a polymer layer. When the material of the fixed layer 12 is glass, the fixed layer 12 is a high temperature liquid to form on the thermal resistance layer 8, and then the fixed layer 12 down to a suitable temperature becomes a solid state. The fixed layer 12 has a thickness between 0.01 and 1 meter. The bottom of traces 6 ~~are~~ is fixed by the fixed layer 12.

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[0052] Next, referring to Fig. 6f, the traces 6 under the net 4 are cut. A tank 14 carries the mold 10, net 4 and the fixed layer 12.

[0053] Next, referring to Fig. 6g, a glass layer (liquid form) 16 is formed on the fixed layer 12. The glass layer 16 is a high temperature liquid to form on the fixed layer 12 and fill in the mold 10, and then the glass layer 16 down to a suitable temperature becomes a solid state, wherein the glass layer 16 has a glass transition temperature between 300°C and 900°C, between 500°C and 800°C, between 900°C and 1200°C or between 1000°C and 1800°C. The glass layer 16 is a low melting point glass material, wherein the glass layer 16 has a melting point between 300°C and 900°C, 800°C and 1300°C, between 900°C and 1600°C, between 1000°C and 1850°C, or between 1000°C and 2000°C, wherein the melting point may smaller than 1500°C. The glass layer 16 has a thickness greater than 0.5 meters or greater than 0.1 meter. Furthermore, there is a few bubbles or no bubble in glass layer 16, for example, there is zero to 3 bubbles in one cubic ~~cubic~~ meter of the glass layer 16, 1 to 10 bubbles in one cubic meter of the glass layer 16, 5 to 30 bubbles in one cubic meter of the glass layer 16 or 20 to 60 bubbles in one cubic meter of the glass layer 16, wherein the bubble has a diameter between 0.0001 and 0.001 centimeters, between 0.001 and 0.05 centimeters, between 0.05 and 0.1 centimeters or between 0.05 and 0.5 centimeters. The glass layer 16 may be ~~remove~~ removed bubbles through multiple processes of a laminating process, a squeezing process and a heating process.

[0054] The glass layer 16 refers to an amorphous solid. The material of the glass layer 16 may be included soda-lime glass, boro-silicate glass, alumo-silicate glass, fluoride glasses, phosphate glasses or chalcogen glasses. For example, the composition of the soda-lime glass comprises SiO_2 (74%), Na_2O (13%), CaO (10.5%), Al_2O_3 (1.3%), K_2O (0.3%), SO3 (0.2%), MgO (0.2%), Fe2O3 (0.04%), TiO2 (0.01%), the composition of the boro-silicate glass comprises SiO_2 (81%), B_2O_3

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(12%), Na_2O (4.5%), Al_2O_3 (2.0%), the composition of the phosphate glasses comprises a percentage of the P_2O_5 material between 3% and 10% or between 5% and 20%.

[0055] A glass, once formed into a solid body, is capable of being softened and perhaps remitted into a liquid form. The "glass transition temperature" of a glass material is a temperature below which the physical properties of the glass are similar to those of a solid and above which the glass material behaves like a liquid.

[0056] If a glass is sufficiently below the glass transition temperature, molecules of the glass may have little relative mobility. As a glass approaches the glass transition temperature, the glass may begin to soften and with increasing ~~temperature~~ temperature, the glass will ultimately melt into the liquid state. Thus, a glass body may be softened to an extent sufficient to enable manipulation of the body's shape, allowing for the formation of holes or other features in the glass body. Once the desired form is obtained, glass is usually annealed for the removal of stresses. Surface treatments, coatings or lamination may follow to improve the chemical durability (glass container coatings, glass container internal treatment), strength (toughened glass, bulletproof glass, windshields), or optical properties (insulated glazing, anti-reflective coating).

[0057] Furthermore, the glass layer 16 may be replaced by a polymer layer. When the polymer layer cured to a solid state~~. The~~, then the polymer layer has ~~an expansion coefficient~~ a coefficient of expansion between 3 and 10 ppm/°C.

[0058] Next, referring to Fig. 6h, the mold 10 and the tank 14 are removed and cut the traces 6 from net 2.

[0059] Next, referring to Fig. 6i, the net 4 and the thermal resistance layer 8 are removed, and then a column 25 is produced.

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[0060] Next, referring to Fig. 6j, the traces 6 out of the column 25 are removed and cutting the column 25 to produce multiple first substrates 20, wherein the first substrate 20 has a thickness between 20 and 100 micrometers, between 50 and 150 micrometers, between 100 and 300 micrometers or between 150 and 2000 micrometers or greater than 1000 micrometers. The first substrates 20 may be ~~make~~ made a planarization process using a suitable process, such as a chemical mechanical polishing (CMP) procedure, mechanical grinding, or laser drilling

[0061] Next, referring to Fig. 6k, the first substrate 20 comprises multiple second substrates 22. The second substrates 22 are well-regulated an array in the first substrate 20. Each of the second substrates22 has multiple metal plugs 21, wherein the metal plug 21 is formed from metal traces 6. The metal plug 21 has the same material and structure with metal trace 6.

[0062] Next, referring to ~~Fig.~~ Figs. 6l-6n, the metal plugs 21 may be arranged in different types, such as Fig. 6l, the metal plugs 21 are arranged on the side portions of the second substrate 22, or such as Fig. 6m, the metal plugs 21 are arranged on the side portions and center portion of the second substrate 22, or such as Fig. 6n, some portions of the second substrate 22 are not arranged the metal plugs 21.

[0063] ~~Fig.~~ Figs. 7a-7m are illustrated a 2nd process of forming a glass substrate of the invention. Please referring to Fig. 7a-7b, there is illustrated a first metal plate 7 in Fig. 7a, illustrated a three-dimensional view of the first metal plate 7 in Fig. 7b. The first metal plate 7 has a thickness between 25 micrometers and 1000 micrometers, between 20 micrometers and 500 micrometers, between 30 micrometers and 400 micrometers or between 20 micrometers and 250 micrometers. The first metal plate 7 comprising a first portion 71, a second portion 73 and a third portion 75 between the first portion 71 and second portion 73, wherein the third portion 75 comprises multiple non-circular metal traces 752 are connected to the first portion 71 and the second portion 73, wherein a cross-

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section view of the non-circular trace 752 comprising a square shape or a rectangle shape. One of the non-circular ~~trace~~ traces 752 has a width greater than the thickness of one of the non-circular ~~trace~~ traces 752, such as between 150 micrometers and 3000 micrometers, between 300 micrometers and 1500 micrometers, between 200 micrometers and 800 micrometers or between 100 micrometers and 500 micrometers. Multiple gaps 754 are between each two neighboring non-circular traces 752, wherein the gap 754 is between 50 micrometers and 3000 micrometers, between 300 micrometers and 1500 micrometers, between 200 micrometers and 800 micrometers or between 150 micrometers and 500 micrometers. The first metal plate 7 comprises a copper metal layer, copper-gold alloy metal layer, copper-gold-palladium alloy metal layer, copper-gold-silver alloy metal layer, copper-platinum alloy metal layer, copper-iron alloy metal layer, copper-nickel alloy metal layer, copper-tungsten metal layer, tungsten metal layer, brass metal layer, zinc plated brass metal layer, stainless metal layer, nickel plated stainless metal layer, phosphor bronze metal layer, copper plated the aluminum metal layer or aluminum metal layer. There are two holes 71a in the first portion 71, wherein the hole 71a has a diameter between 600 micrometers and 2000 micrometers, between 1000 micrometers and 3000 micrometers or between 2000 micrometers and 5000 micrometers. There are two holes 73a corresponding to the hole 71a in the first portion 71, wherein the hole 73a has a diameter between 600 micrometers and 2000 micrometers, between 1000 micrometers and 3000 micrometers or between 2000 micrometers and 5000 micrometers, wherein a first least distance between the two holes 71a is substantially the same to a second least distance between the two holes 73a.

[0064] Next, referring to ~~Fig.~~ Figs. 7c-7d, there is illustrated a second metal plate 9 in Fig. 7c, illustrated a three-dimensional view of the second metal plate 9 in Fig. 7d. The second metal plate 9 has a thickness between 25 micrometers and 600 micrometers, between 20 micrometers and 300 micrometers, between 30 micrometers and 250 micrometers or between 25 micrometers and 180

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micrometers. There are two holes 90a in the second metal plate 9, wherein the hole 90a has a diameter between 600 micrometers and 2000 micrometers, between 1000 micrometers and 3000 micrometers or between 2000 micrometers and 5000 micrometers, wherein a third least distance between the two holes 90a is substantially the same to a second least distance between the two holes 73a and substantially the same to the first least distance between the two holes 71a. The second metal plate 9 comprises a copper metal layer, copper-gold alloy metal layer, copper-gold-palladium alloy metal layer, copper-gold-silver alloy metal layer, copper-platinum alloy metal layer, copper-iron alloy metal layer, copper-nickel alloy metal layer, copper-tungsten metal layer, tungsten metal layer, brass metal layer, zinc plated brass metal layer, stainless metal layer, nickel plated stainless metal layer, phosphor bronze metal layer, copper plated the aluminum metal layer or aluminum metal layer.

[0065] Next, referring to Fig. 7e, there is illustrated a three-dimensional view of a third metal plate 11 in Fig. 7e. The third metal plate 11 has a thickness between 25 micrometers and 600 micrometers, between 20 micrometers and 300 micrometers, between 30 micrometers and 250 micrometers or between 25 micrometers and 180 micrometers. There are four holes 110a, 112a, 114a, 116a in the third metal plate 11, wherein the hole 110a, 112a, 114a, 116a have a diameter between 600 micrometers and 2000 micrometers, between 1000 micrometers and 3000 micrometers or between 2000 micrometers and 5000 micrometers, wherein a fourth least distance between the ~~two~~ hole 110a and hole 112a and a fifth least distance between the ~~two~~ hole 114a and hole 116a are substantially the same to a second least distance between the two holes 73a and substantially the same to the first least distance between the two holes 71a. The third metal plate 11 comprises a copper metal layer, copper-gold alloy metal layer, copper-gold-palladium alloy metal layer, copper-gold-silver alloy metal layer, copper-platinum alloy metal layer, copper-iron alloy metal layer, copper-nickel alloy metal layer, copper-tungsten metal layer, tungsten metal layer, brass metal layer,

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zinc plated brass metal layer, stainless metal layer, nickel plated stainless metal layer, phosphor bronze metal layer, copper plated the aluminum metal layer or aluminum metal layer.

[0066] Next, referring to Fig. 7f-Fig.7i, providing two bolts 130, 132 pass through two holes 150a of a fixing metal plate 150 and providing two bolts 134, 136 pass through two holes 152a of a fixing metal plate 152 respectively. Next, the bolts 130, 132, 134, 136 are passing through the holes 110a, 112a, 114a, 116a of the third metal plate 11 respectively and the third metal plate 11 is formed on the fixing metal plate 150 and the fixing metal plate 152. Next, the bolts 130, 132 are passing through the hole 90a of the second metal plate 9 and the bolts 134, 136 are passing through the hole 90a of another the second metal plate 9, then the second metal plates 9 are formed on the third metal plate 11. Next, the bolts 130, 132, 134, 136 are passing through the holes 71a, 73a of the first metal plate 7 respectively and the first metal plate 7 is formed on the second metal plates 9. Next, repeating to site another the second metal plates 9 on another the first metal plate 7 sequentially until to expose a top of the bolts 130, 132, 134, 136. Next, the top of the bolts 130, 132, 134, 136 are passing through the holes 110a, 112a, 114a~~, 116a~~ and 116a of another the third metal plate 11 respectively and the third metal plate 11 is formed on the second metal plates 9. Next, ~~The~~ the top of the bolts 130, 132 are passing through two holes 150a of another the fixing metal plate 150 and the top of the bolts 134, 136 are passing through two holes 152a of another the fixing metal plate 152 respectively, then the fixing metal plates 150, 152 are formed on the third metal plate 11. Finally, providing four sleeve nuts 17 lock on the top of the bolts 130, 132, 134, 136. Then, multiple the first metal plates 7, multiple the second metal plates 9, two the third metal plates 11, two fixing metal plates 150 and two fixing metal plates 152 forming a metal trace block 19.

[0067] Next, referring to Fig. 7j the metal trace block 19 is put in a mold 23. The mold 23 may be a metal mold, a ceramics mold or a polymer mold, which has a heat deflection temperature between 400 ℃ and 900 ℃ or between 800 ℃ and 1300 ℃. The mold 23 comprises a gas inlet 23a

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and a liquid input 23b, wherein the gas inlet 23a is used to input N_2 gas and the liquid input 23b is used to input the liquid form glass layer.

[0068] Next, referring to Fig. 7k, the glass layer (liquid form) 16 fill in the mold 23. The glass layer 16 is a high temperature liquid and fill in the mold 23, and then the glass layer 16 down to a suitable temperature becomes a solid state, wherein the glass layer 16 has a glass transition temperature between 300°C and 900°C, between 500°C and 800°C, between 900°C and 1200°C or between 1000°C and 1800°C. The glass layer 16 is a low melting point glass material, wherein the glass layer 16 has a melting point between 300°C and 900°C, 800°C and 1300°C, between 900°C and 1600°C, between 1000°C and 1850°C, or between 1000°C and 2000°C, wherein the melting point may smaller than 1500°C. Furthermore, there is a few bubbles or no bubble in glass layer 16, for example, there is zero to 3 bubbles in one cubic meter of the glass layer 16, 1 to 10 bubbles in one cubic meter of the glass layer 16, 5 to 30 bubbles in one cubic meter of the glass layer 16 or 20 to 60 bubbles in one cubic meter of the glass layer 16, wherein the bubble has a diameter between 0.0001 and 0.001 centimeters, between 0.001 and 0.05 centimeters, between 0.05 and 0.1 centimeters or between 0.05 and 0.5 centimeters. The glass layer 16 may be ~~remove~~ removed bubbles through multiple processes of a laminating process, a squeezing process and a heating process.

[0069] Next, referring to Fig. 7l, the mold 23is removed and cut the glass layer 16 along a cutting line 16a to remove the fixing metal plate 150, the fixing metal plate 152, the first portion 71 of the first metal plate 7, the second portion 73 of the first metal plate 7 and two the third metal plates 11, and then the column 25 is produced, showed in the Fig. 7m.

[0070] Next, referring to Fig. 7n, cutting the column 25 to produce multiple first substrates 20, wherein the first substrate 20 has a thickness between 20 and 100 micrometers, between 50 and 150

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micrometers, between 100 and 300 micrometers or between 150 and 2000 micrometers or greater than 1000 micrometers. The first substrates 20 may be ~~make~~ made a planarization process using a suitable process, such as a chemical mechanical polishing (CMP) procedure, mechanical grinding, or laser drilling.

[0071] Next, referring to Fig. 7o, the first substrate 20 comprises multiple second substrates 22. The second substrates 22 are well-regulated an array in the first substrate 20. Each of the second substrates has multiple metal plugs 21, wherein the metal plug 21 is formed from the non-circular metal traces 752. The metal plug 21 has the same material, structure and shape with the non-circular metal traces 752. A first pitch 21a and a second pitch 21b ~~is~~ are between the metal plugs 21, wherein the first pitch 21a is controlled or the same-2 by a distance of the gap 754 and wherein the second pitch 21b is controlled by a distance of adjacent the non-circular traces 752.

[0072] Next, referring to ~~Fig.~~ Figs. 7p-7r, the metal plugs 21 may be arranged in different types, such as Fig. 7p, the metal plugs 21 are arranged on the side portions of the second substrate 22, or such as Fig. 7q, the metal plugs 21 are arranged on the side portions and center portion of the second substrate 22, or such as Fig. 7r, some portions of the second substrate 22 are not arranged the metal plugs 21.

[0073] Fig. 8a illustrates a cross-section view of the second substrate 22 illustrates a cross-section view of the metal plug 21. The second substrate 22 ~~comprise~~ comprises an amorphous solid glass layer/body 16 and multiple metal plugs 21, wherein the amorphous solid glass layer/body 16 having a top surface and an opposing bottom surface and the metal plugs 21 extending through the amorphous solid glass layer/body 16 beginning at the top surface and ending at the bottom surface. The top surface of the metal plugs 21 are the same area as the bottom surface of the metal plugs 21.

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[0074] Please referring Fig. 8b, the top surface of the metal plugs 21 and the top surface of the amorphous solid glass layer/body 16 are substantially coplanar. The bottom surface of the metal plugs 21 and the bottom surface of the amorphous solid glass layer/body 16 are substantially coplanar.

[0075] Please referring Fig. 8c, the top surface of the metal plugs 21 comprises a top surface of the metal traces 6/ metal traces 752 and a top surface of the first covering layer 6a are substantially coplanar with the top surface of the amorphous solid glass layer/body 16. The bottom surface of the metal plugs 21 comprises a bottom surface of the metal traces 6/ metal traces 752 and a bottom surface of the first covering layer 6a are substantially coplanar with the bottom surface of the amorphous solid glass layer/body 16.

[0076] Please referring Fig. 8d, the top surface of the metal plugs 21 comprises a top surface of the metal traces 6/ metal traces 752, a top surface of the first covering layer 6a and a top surface of the second covering layer 6b are substantially coplanar with the top surface of the amorphous solid glass layer/body 16. The bottom surface of the metal plugs 21 comprises a bottom surface of the metal traces 6/ metal traces 752, a bottom surface of the first covering layer 6a and a bottom surface of the second covering layer 6b are substantially coplanar with the bottom surface of the amorphous solid glass layer/body 16.

[0077] Fig. 9a-Fig. 9t ~~illustrates~~ illustrate a process to form multiple traces on a top surface and a bottom surface of the first substrate 20.

[0078] Next, referring to Fig. 9a, a first dielectric layer 24 is formed on the top surface of the first substrate 20, wherein the first dielectric layer 24 may include or ~~may be~~ maybe a layer of silicon oxide (such as SiO_2), silicon nitride (such as Si_3N_4), silicon oxynitride (such as SiON), silicon oxycarbide (such as SiOC), phosphosilicate glass (PSG), silicon carbon nitride (such as

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SiCN), low k dielectric layer (K between 0.5 and 3), or polymer (such as polyimide, benzocyclobutene (BCB), polybenzoxazole (PBO), poly-phenylene oxide (PPO), epoxy, or silosane). The first dielectric layer 24 may be formed or deposited using a suitable process. The first dielectric layer 24 has a thickness between 0.3 and 5 micrometers, between 2 and 10 micrometers, between 1 and 30 micrometers or greater than 30 micrometers.

[0079] Next, referring to Fig. 9b, multiple openings 24a are formed in the first dielectric layer 24 to expose the metal plugs 21. The openings 24a may be formed in the first dielectric layer 24 by a suitable process, such as etching. The opening 24a has a width between 0.3 and 3 micrometers, between 0.5 and 8 micrometers, between 2 and 20 micrometers or between 2 and 50 micrometers.

[0080] Next, referring to Fig. 9c, a first metal layer 26 is formed on the first dielectric layer 24, on the metal plugs 21 and in the openings 24a. The first metal layer 26 may include an adhesion/barrier layer, such as a layer of titanium, a titanium-tungsten alloy, titanium nitride, chromium, tantalum, tantalum nitride, nickel or nickel vanadium formed using a suitable process, such as a vacuum deposition, a Physical Vapor Deposition (PVD), a Plasma Enhanced Chemical Vapor Deposition (PECVD), a sputtering process or an electroplating process, with a thickness, e.g., between 1 nanometer and 2 micrometers, between 0.3 and 3 micrometers or between 0.5 and 10 micrometers.

[0081] Next, referring to Fig. 9d, a second metal layer 28 is formed on the first metal layer 26. The second metal layer 28 ~~may be~~ maybe comprises copper, nickel, gold or aluminum formed using a suitable process, such as a vacuum deposition, a Physical Vapor Deposition (PVD), a Plasma Enhanced Chemical Vapor Deposition (PECVD), a sputtering process or an electroplating process, with a thickness, e.g., between 1 nanometer and 5 micrometers, between 1 and 5 micrometers or between 5 and 30 micrometers.

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[0082] Next, referring to Fig. 9e, a photoresist layer 30 is formed on the second metal layer 28 by using a suitable process, such as a spin coating process or a lamination process. Next, a photo exposure process using a 1X stepper and a development process using a chemical solution can be employed to form multiple openings 30a, exposing the second metal layer 28, in the photoresist layer. The photoresist layer 30 may have a thickness, e.g., between 3 and 50 micrometers, wherein the photoresist layer 30 may be a positive-type photo-sensitive resist layer or negative-type photo-sensitive resist layer.

[0083] Next, referring to Fig. 9f, remove the first metal layer 26 and the second metal layer 28 are under the openings 30a by using a suitable process, such as an etching process.

[0084] Next, referring to Fig. 9g, remove the photoresist layer 30 by using a clean process.

[0085] Next, referring to Fig. 9h, a second dielectric layer 32 is formed on the first dielectric layer 24 and on the second metal layer 28, wherein the second dielectric layer 32 may include or may be a layer of silicon oxide (such as SiO_2), silicon nitride (such as Si_3N_4), silicon oxynitride (such as SiON), silicon oxycarbide (such as SiOC), phosphosilicate glass (PSG), silicon carbon nitride (such as SiCN), low k dielectric layer (K between 0.5 and 3), or polymer (such as polyimide, benzocyclobutene (BCB), polybenzoxazole (PBO), poly-phenylene oxide (PPO), epoxy, or silosane). The second dielectric layer 32 may be formed or deposited using a suitable process. The second dielectric layer 32 has a thickness between 0.3 and 5 micrometers, between 2 and 10 micrometers, between 1 and 30 micrometers or greater than 30 micrometers.

[0086] Next, referring to Fig. 9i, multiple openings 32a are formed in the second dielectric layer 32 to expose the second metal layer 28. The openings 32a may be formed in the second dielectric layer 32 by a suitable process, such as etching. The opening 32a has a width between 0.3 and 3

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micrometers, between 0.5 and 8 micrometers, between 2 and 20 micrometers or between 2 and 50 micrometers.

[0087] Next, referring to Fig. 9j, a third metal layer 34 is formed on the second dielectric layer 32, on the second metal layer 28 and in the openings 32a. The third metal layer 34 may include an adhesion/barrier layer, such as a layer of titanium, a titanium-tungsten alloy, titanium nitride, chromium, tantalum, tantalum nitride, nickel or nickel vanadium formed using a suitable process, such as a vacuum deposition, a Physical Vapor Deposition (PVD), a Plasma Enhanced Chemical Vapor Deposition (PECVD), a sputtering process or an electroplating process, with a thickness, e.g., between 1 nanometer and 2 micrometers, between 0.3 and 3 micrometers or between 0.5 and 10 micrometers.

[0088] Next, referring to Fig. 9k, a fourth metal layer 36 is formed on the third metal layer 34. The fourth metal layer 36 ~~may be~~ maybe comprises copper, nickel, gold or aluminum formed using a suitable process, such as a vacuum deposition, a Physical Vapor Deposition (PVD), a Plasma Enhanced Chemical Vapor Deposition (PECVD), a sputtering process or an electroplating process, with a thickness, e.g., between 1 nanometer and 5 micrometers, between 1 and 5 micrometers or between 5 and 30 micrometers.

[0089] Next, referring to Fig. 9l, a photoresist layer 38 is formed on the fourth metal layer 36 by using a suitable process, such as a spin coating process or a lamination process. Next, a photo exposure process using a 1X stepper and a development process using a chemical solution can be employed to form multiple openings 38a, exposing the fourth metal layer 36, in the photoresist layer. The photoresist layer 38 may have a thickness, e.g., between 3 and 50 micrometers, wherein the photoresist layer 38 may be a positive-type photo-sensitive resist layer or negative-type photo-sensitive resist layer.

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[0090] Next, referring to Fig. 9m, remove the third metal layer 34 and the fourth metal layer 36 are under the openings 38a by using a suitable process, such as an etching process.

[0091] Next, referring to Fig. 9n, remove the photoresist layer 38 by using a clean process.

[0092] Next, referring to Fig. 9o, a third dielectric layer 40 is formed on the second ~~second~~ dielectric layer 32 and on the fourth metal layer 36, wherein the third dielectric layer 40 may include or ~~may be~~ maybe a layer of silicon oxide (such as SiO_2), silicon nitride (such as Si_3N_4), silicon oxynitride (such as SiON), silicon oxycarbide (such as SiOC), phosphosilicate glass (PSG), silicon carbon nitride (such as SiCN), low k dielectric layer (K between 0.5 and 3), or polymer (such as polyimide, benzocyclobutene (BCB), polybenzoxazole (PBO), poly-phenylene oxide (PPO), epoxy, or silosane). The third dielectric layer 40 may be formed or deposited using a suitable process. The third dielectric layer 40 has a thickness between 0.3 and 5 micrometers, between 2 and 10 micrometers, between 1 and 30 micrometers or greater than 30 micrometers.

[0093] Next, referring to Fig. 9p, multiple openings 40a are formed in the third dielectric layer 40 to expose the fourth metal layer 36. The openings 40a may be formed in the third dielectric layer 40 by a suitable process, such as etching. The opening 40a has a width between 0.3 and 3 micrometers, between 0.5 and 8 micrometers, between 2 and 20 micrometers or between 2 and 50 micrometers.

[0094] Next, referring to Fig. 9q, a protecting layer 42 is formed in the openings 40a, on the third dielectric layer 40 and on the fourth metal layer 36, which can protect the third dielectric layer 40 not to be damaged and the fourth metal layer 36 not be damaged and ~~oxidated~~ oxidized.

[0095] Next, referring to Fig. 9r, repeat the processes of Fig.9a-Fig.9p to form the first dielectric layer 24, the first metal layer 26, the second metal layer 28, the second dielectric layer 32, the third

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metal layer 34, the fourth metal layer 36 and the third dielectric layer 40 on the bottom surface of the first substrate 20.

[0096] Furthermore, referring to Fig. 9s, a passive device 44 may be formed in the first metal layer 28 and the second metal layer 36, such as an inductor, a capacitor or a resistor.

[0097] Next, referring to Fig. 9t, multiple chips 46 and chips 56 set up over the third dielectric layer 40 through a ~~flip-chip~~ flip-chip package process or a ~~wirebonding~~ wire-bonding package process, wherein the chip 46 ~~and~~ or 56 comprises may be a memory chip, such as NAND-Flash memory chip, Flash memory chip, DRAM chip, SRAM chip or SDRAM chip, a central-processing-unit (CPU) chip, a graphics-processing-unit (GPU) chip, a digital-signal-processing (DSP) chip, a baseband chip, a wireless local area network (WLAN) chip, a logic chip, an analog chip, a global-positioning-system (GPS) chip, a "Bluetooth" chip, or a chip including one or more of a CPU circuit block, a GPU circuit block, a DSP circuit block, a memory circuit block (such as DRAM circuit block, SRAM circuit block, SDRAM circuit block, Flash memory circuit block, or NAND-Flash memory circuit block), a baseband circuit block, a Bluetooth circuit block, a GPS circuit block, a MEMS chip, a COMS image sensor device, a WLAN circuit block, and a modem circuit block, from the semiconductor wafer.

[0098] The chips 46 are set up on the third dielectric layer 40 through a ~~flip-chip~~ flip-chip package process, wherein the chip 46 comprises multiple metal pads 48 and multiple metal bumps 50 formed on the metal pads 48. The metal pad 48 may be an electroplated copper pad, a damascene copper pad or an aluminum pad. The metal bump 50 comprises an adhesion/barrier metal layer formed on the metal pad 48, an electroplated metal layer or an electro-less metal layer formed on the adhesion/barrier metal layer, wherein the adhesion/barrier metal layer comprises a titanium-containing layer, a chromium-containing layer, a tantalum-containing layer or a nickel layer, and the

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electroplated metal layer comprises a copper layer, a gold layer, a nickel layer, a tin-containing layer, a solder layer, a solder layer over a nickel layer and a copper layer, and the electro-less layer comprises a copper layer, a gold layer or a nickel layer. The electroplated metal layer has a thickness between 2 and 5 micrometers, between 5 and 30 micrometers or between 10 and 50 micrometers. The metal bumps 50 are connected to the fourth metal layer 36 exposed by the openings 40a through a solder layer 54, wherein the solder layer 54 is formed on the fourth metal layer 36 exposed by the openings 40a or is a portion of the metal bump

[0099] 50. An underfill layer 52 is formed between the chips 46 and the third dielectric layer 40.

[00100] The chips 56 are set up over the third dielectric layer 40 through a polymer adhesion layer 60, wherein the chip 56 comprises multiple metal pads 58. The metal pad 58 may be an electroplated copper pad, a damascene copper pad or an aluminum pad. Multiple metal wires 62 are connected to the metal pads 58 and the fourth metal layer 36 exposed by the openings 40a, wherein the metal wires 62 comprises a gold wire, a copper wire, a metal alloy wire, a silver-containing wire, an aluminum-containing wire or gold-copper alloy wire. An underfill layer 64 is covered the chip56, the metal wires 62 and the metal pads 58.

[00101] Multiple discrete passive components 66 set up on the third dielectric layer 40, such as a discrete inductor, a discrete capacitor or a discrete resistor, wherein the discrete passive component 66 comprises a multiple metal pad 68. The discrete passive components 66 mounted on the third dielectric layer 40 through a solder layer 70.

[00102] Next, referring to Fig. 9u, multiple metal bumps 72 are formed on the bottom surface of the substrate 20.

[00103] Fig. 9v is disclosed some structures of metal bump 72.

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- Lift side: 1st type of structures of metal bump 72 comprises an adhesion/barrier metal layer 61 formed on the metal pad 48, a metal seed layer 63 formed on the adhesion/barrier metal layer 61, an electroplated metal layer 65 formed on the metal seed layer 63 and a solder layer 67 formed on the electroplated metal layer 65, wherein the adhesion/barrier metal layer 61 comprises a titanium-containing layer, a chromium-containing layer, a tantalum-containing layer or a nickel layer, wherein the first electroplated metal layer 65 comprises a copper layer, a gold layer, a nickel layer, wherein the solder layer 67 can be formed by screen plating, ball mounting, or an electroplating process, such as gold-tin alloy, tin-silver alloy, tin-silver-copper alloy, indium, tin-bismuth alloy, or other lead-free alloy. Lead alloy solders can also be used but may be less desirable in some embodiments due to toxicity considerations. The adhesion/barrier metal layer 61 has a thickness between 0.05 and 2 micrometers. The metal seed layer 63 has a thickness between 0.05 and 2 micrometers. The first electroplated metal layer 65 has a thickness between 1 and 5 micrometers, between 2 and 8 micrometers or between 5 and 20 micrometers. The solder layer 67 has a thickness between 30 and 80 micrometers, between 50 and 100 micrometers, between 80 and 150 micrometers or between 120 and 350 micrometers.

- Right side: 2nd type of structure of metal bump 72 comprises an adhesion/barrier metal layer 61 formed on the metal pad 48, a metal seed layer 63 formed on the adhesion/barrier metal layer 61, a first electroplated metal layer 65 formed on the metal seed layer 63 and a second electroplated metal layer 69 formed on the first electroplated metal layer 65, wherein the adhesion/barrier metal layer 61 comprises a titanium-containing layer, a chromium-containing layer, a tantalum-containing layer or a nickel layer, wherein the first electroplated metal layer 65 comprises a copper layer, a gold layer, a nickel layer, wherein the second electroplated metal layer 69 comprises a copper layer, a gold layer, a nickel

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layer. The adhesion/barrier metal layer 61 has a thickness between 0.05 and 2 micrometers. The metal seed layer 63 has a thickness between 0.05 and 2 micrometers. The first electroplated metal layer 65 has a thickness between 1 and 5 micrometers, between 2 and 4 micrometers, between 5 and 15 micrometers or between 10 and 25 micrometers. The second electroplated metal layer 69 has a thickness between 1 and 5 micrometers, between 2 and 4 micrometers, between 10 and 30 micrometers or between 20 and 60 micrometers.

[00104] Furthermore, referring to Fig. 9w, the chips 46 may be set up on the bottom surface of the first substrate 20.

[00105] Furthermore, referring to Fig. 9x, the chip 46 may be replaced a 3D IC chip package, wherein the chip 46 comprises a multiple metal pad 48 formed on the top and bottom surface. The metal pads 48 of the top surface of the chip 46 are connected to the metal pads 48 of the bottom surface of the chip 46 through multiple through-silicon-via metal layers. A chip 47 is connected to the 3D IC chip 46 through the ~~flip-chip~~ flip-chip package process, wherein the chip 47 comprises multiple metal pads 49, wherein the metal pad 49 may be an electroplated copper pad, a damascene copper pad or an aluminum pad. The metal pads 49 are connected to the metal pads 48 through a solder layer 51.

[00106] Fig. 9y, illustrates a top view of the first substrate 20. Fig. 9u-Fig. 9w illustrate a ~~cross-section~~ cross-section view of Line L-L' in Fig. 9y. Multiple the chips 46, the chips 56 and the passive components 66 may also be provided in or on the first substrate 20.

[00107] Next, cutting the first substrate 20 to produce multiple second substrates 22.

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[00108] Fig. 10a-Fig. 10j ~~illustrates~~ illustrate a damascene process to form the first metal layer 26, the second metal layer 28, the third metal layer 34 and the fourth metal layer 36 on a top surface and a bottom surface of ~~the~~ the first substrate 20.

[00109] Referring to Fig. 10a, the dielectric layers 24 in ~~Figs.~~ Fig. 9a include two dielectric layers 80 and 82. The dielectric layer 80 is formed on the dielectric layer 82 by a chemical vapor deposition (CVD) process or a spin-on coating process, wherein each of the dielectric layers 80 and 82 may be composed of a low-K oxide layer with a thickness of between 0.3 and 5μm, and preferably of between 0.5 and 3μm, and an oxynitride layer on the low-K oxide layer, of a low-K polymer layer with a thickness of between 0.3 and 5μm, and preferably of between 0.5 and 3μm, and an oxynitride layer on the low-K polymer layer, of a low-K oxide layer with a thickness of between 0.3 and 5μm, and preferably of between 0.5 and 3μm, and a nitride layer on the low-K oxide layer, of a low-K polymer layer with a thickness of between 0.3 and 5μm, and preferably of between 0.5 and 3μm, and a nitride layer on the low-K polymer layer, or of a low-K dielectric layer with a thickness of between 0.3 and 5μm, and preferably of between 0.5 and 3μm, and a nitride-containing layer on the low-K dielectric layer. Next, referring to Fig. 10b, a photoresist layer 84 is formed on the dielectric layer 82, an opening 84a in the photoresist layer 84 exposing the dielectric layer 82. Next, referring to Fig. 10c, the dielectric layer 82 under the opening 84a is removed by a dry etching method to form a trench in the dielectric layer 82 exposing the dielectric layer 80. Next, referring to Fig. 10d, after forming the trench in the dielectric layer 82, the photoresist layer 84 is removed. Next, referring to Fig. 10e, a photoresist layer 86 is formed on the dielectric layer 82 and on the dielectric layer 80 exposed by the trench, an opening 86a in the photoresist layer 86 exposing the dielectric layer 80 exposed by the trench. Next, referring to Fig. 19f, the dielectric layer 80 under the opening 86a is removed by a dry etching method to form a via 80a in the dielectric layer 80 exposing the metal plugs 21 in the substrate 20. Next, referring to Fig. 10g, after forming the via 80a in the

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dielectric layer 80, the photoresist layer 86 is removed. Thereby, an opening 88 including the trench and the via 80a is formed in the dielectric layers 82 and 80. Next, referring to Fig. 10h, an adhesion/barrier layer 90 having a thickness of between 0.1 and 3 micrometers is formed on the metal plugs 21 exposed by the opening 88, on the sidewalls of the opening 88 and on the top surface of the dielectric layer 82. The adhesion/barrier layer 90 can be formed by a sputtering process or a chemical vapor deposition (CVD) process. The material of the adhesion/barrier layer 90 may include titanium, titanium nitride, a titanium-tungsten alloy, tantalum, tantalum nitride, or a composite of the abovementioned materials. For example, the adhesion/barrier layer 90 may be formed by sputtering a tantalum layer on the metallization structure exposed by the opening 88, on the sidewalls of the opening 88 and on the top surface of the dielectric layer 82. Alternatively, the adhesion/barrier layer 90 may be formed by sputtering a tantalum-nitride layer on the metallization structure exposed by the opening 88, on the sidewalls of the opening 88 and on the top surface of the dielectric layer 82. Alternatively, the adhesion/barrier layer 90 may be formed by forming a tantalum-nitride layer on the metallization structure exposed by the opening 88, on the sidewalls of the opening 88 and on the top surface of the dielectric layer 82 by a chemical vapor deposition (CVD) process. Next, referring to Fig. 10i, a seed layer 92, made of copper, having a thickness of between 0.1 and 3 micrometers is formed on the adhesion/barrier layer 90 using a sputtering process or a chemical vapor deposition (CVD) process, and then a copper layer 94 having a thickness of between 0.5 and 5μm, and preferably of between 1 and 2μm, is electroplated on the seed layer 92. Next, referring to Fig. 10j, the copper layer 94, the seed layer 92 and the adhesion/barrier layer 90 outside the opening 88 in the dielectric layers 82 and 80 are removed using a chemical mechanical polishing (CMP) process until the top surface of the dielectric layer 82 is exposed to an ambient.

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[00110] Fig. 11a-Fig. 11i ~~illustrates~~ illustrate an embossing process to form the first metal layer 26, the second metal layer 28, the third metal layer 34 and the fourth metal layer 36 on a top surface and a bottom surface of the first substrate 20.

[00111] Referring to Fig. 11a, the metal plugs 21 are in the glass layer 16 of the first substrate 20, and the opening 96a in the dielectric layer 96 exposes the metal plugs 21.

[00112] Referring to Fig. 11a, a polymer layer 98 can be formed on the dielectric layer 96, and at least one opening 98a is formed in the polymer layer 98 by patterning the polymer layer 98 to expose at least one metal trace 6, as shown in Fig. 11b and Fig. 11c. The metal plugs 21 may include a center portion exposed by an opening 98a and a peripheral portion covered with the polymer layer 98, as shown in Fig. 11b. Alternatively, the opening 98a may expose the entire upper surface of the metal plugs 21 exposed by the opening 96a in the dielectric layer 96 and further may expose the upper surface of the dielectric layer 96 near the metal trace 6, as shown in Fig. 11c.

[00113] The material of the polymer layer 98 may include benzocyclobutane (BCB), polyimide (PI), polyurethane, epoxy resin, a parylene-based polymer, a solder-mask material, an elastomer, or a porous dielectric material. The polymer layer 98 has a thickness of between 3 and 25μm or between 5 and 50 micrometers.

[00114] The polymer layer 98 can be formed by a spin-on coating process, a lamination process or a screen-printing process. Below, the process of forming a patterned polymer layer 98 is exemplified with the case of spin-on coating a polyimide layer on the dielectric layer 96 and then patterning the polyimide layer.

[00115] Referring to Fig. 11d, an adhesion/barrier layer 100 having a thickness of between 0.1 and 3 micrometers, and preferably between 0.5 and 2 micrometers, is formed on the polymer

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layer 98 and on the metal plugs 21. The adhesion/barrier layer 100 may be a titanium-tungsten-alloy layer, tantalum-containing layer, a chromium-containing layer or a titanium-nitride layer. The adhesion/barrier layer 100 may be formed by a sputtering method, an evaporation method, or a chemical vapor deposition (CVD) method.

[00116] Referring to Fig. 11e, a photoresist layer 102 can be formed on the adhesion/barrier layer 100 by a spin coating process or a lamination process. Referring to Fig. 11f, the photoresist layer 102 is patterned with the processes of exposure, development, etc., to form a photoresist opening 102a on the above-mentioned adhesion/barrier layer 100 over the metal plugs 21 exposed by the opening 98a.

[00117] Referring to Fig. 11g, an electroplated metal layer 104 is formed on the adhesion/barrier layer 100 in the opening 102a, wherein the electroplated metal layer 104 comprises a copper layer, gold layer, a nickel layer, has a thickness between 2 and 10 micrometers, between 5 and 20 micrometers or between 5 and 35 micrometers.

[00118] Referring to Fig. 11h, removing the photoresist layer 102.

[00119] Referring to Fig. 11i, the above-mentioned adhesion/barrier layer 100 not under the electroplated metal layer 104 is removed with a dry etching method or a wet etching method. For example, the adhesion/barrier layer 100 made of titanium, titanium-tungsten alloy, titanium nitride, tantalum or tantalum nitride, not under the electroplated metal layer 104 is removed with a reactive ion etching (RIE) process.

[00120] First Application: Please referring to Fig. 12, the second substrates 22 is connected to a OLED display substrate through COG bonding process, wherein the OLED display substrate comprises a first glass substrate 106, a second glass substrate 108, an organic light-emitting diodes

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layer 110 (or a polymer light-emitting diodes layer, PLED layer) between the first glass substrate 106 and the second glass substrate 108 and multiple transparent electrodes 114. The metal bumps 72 are connected to the transparent electrodes 114 through an anisotropic conductive film (ACF) layer 116, wherein the ACF layer 116 comprises multiple conductive particles 117, such as nickel (Ni) particles, gold (Au) particles, nickel-gold alloy particles, silver-tin alloy particles, silver particles, gold plated particles, silver plated particles or nickel plated particles. The OLED display substrate comprises multiple OLED display panels. The OLED display substrate may comprise a touch screen function. A least distance 106a between a centerline of the metal bump 72 and a boundary of the glass substrate 106 is between 3 micrometers and 10 micrometers, 5 micrometers and 15 micrometers, 10 micrometers and 25 micrometers or 20 micrometers and 40 micrometers.

[00121] Next, cutting the second substrates 22 and the OLED display substrate to produce multiple package units.

[00122] Second Application: Furthermore, the OLED display substrate can be replaced ~~to~~ with a Micro Electro Mechanical Systems (MEMS) display substrate. Please referring to Fig. 13, the second substrates 22 is connected to a MEMS display substrate through COG bonding process, wherein the MEMS display substrate comprises a first glass substrate 106, a MEMS layer 109 and multiple transparent electrodes 114 formed on the first glass substrate 106. The metal bumps 72 are connected to the transparent electrodes 114 through an anisotropic conductive film (ACF) layer 116, wherein the ACF layer 116 comprises multiple conductive particles 117, such as nickel (Ni) particles, gold (Au) particles, nickel-gold alloy particles, silver-tin alloy particles, silver particles, gold plated particles, silver plated particles or nickel plated particles. The MEMS display substrate comprises multiple MEMS display panels. The MEMS display substrate may comprise touch screen function. A least distance 106a between a centerline of the metal bump 72 and a boundary of the

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glass substrate 106 is between 3 micrometers and 10 micrometers, 5 micrometers and 15 micrometers, 10 micrometers and 25 micrometers or 20 micrometers and 40 micrometers.

[00123] Next, cutting the second substrates 22 and the MEMS display substrate to produce multiple package units.

[00124] Third application: Please ~~referring~~ refer to Fig. 14, multiple LED devices 122 are packaged on the bottom surface of the second substrates 22. The second substrates 22 is connected to a LCD display substrate through COG bonding process, wherein the LCD display substrate comprises a first glass substrate 106, a second glass substrate 108, and a transistor liquid crystal display layer 111 between the first glass substrate 106 and the second glass substrate 108 and multiple transparent electrodes 114. The metal bumps 72 are connected to the electrodes 114 through an anisotropic conductive film (ACF) layer 116, wherein the ACF layer 116 comprises multiple conductive particles 117, such as nickel (Ni) particles, gold (Au) particles, nickel-gold alloy particles, silver-tin alloy particles, silver particles, gold plated particles, silver plated particles or nickel plated particles. The LCD display substrate comprises multiple LCD display panels. The LCD display substrate may ~~comprise~~ comprises a touch screen function, wherein the LCD display substrate ~~comprise~~ comprises an in-cell TFT LCD substrate. There are multiple optical layers 128 between the second substrates 22 and LCD display substrate, such as a diffuser sheet layer, a prism sheet layer, a diffuser layer (or diffuser plate) and a reflector layer. A least distance 106a between a centerline of the metal bump 72 and a boundary of the glass substrate 106 is between 3 micrometers and 10 micrometers, 5 micrometers and 15 micrometers, 10 micrometers and 25 micrometers or 20 micrometers and 40 micrometers.

[00125] Next, cutting the second substrates 22 and the LCD display substrate to produce multiple package units.

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[00126] Fourth application: Referring to Fig. 15, this structure of the fourth application is similar to the structure of the third application in Fig. 14. The second substrates 22 is connected to a LCD display substrate through ~~flip-chip~~ flip-chip bonding process, wherein the LCD display substrate comprises a first glass substrate 106 and a second glass substrate 108, and a transistor liquid crystal display layer 111 and thin film transistor circuit layers (not shown) between the first glass substrate 106 and the second glass substrate 108, wherein multiple transparent electrodes 114 on the bottom surface of the first glass substrate 106 and multiple metal plugs 113 in the first glass substrate 106, wherein the multiple metal plugs 113 are connected to the transparent electrodes 114 respectively. The structure of the first glass substrate 106 can refer to the second substrates 22 in the invention. The metal bumps 72 are connected to the transparent electrodes 114 through a solder layer 107, wherein the solder layer 107 comprises gold-tin alloy, tin-silver alloy, tin-silver-copper alloy, indium, tin-bismuth alloy, or other lead-free alloy. The LCD display substrate comprises multiple LCD display panels. The LCD display substrate may comprise touch screen function, wherein the LCD display substrate comprising an in-cell TFT LCD substrate. There are multiple optical layers 128 between the second substrates 22 and LCD display substrate, such as a diffuser sheet layer, a prism sheet layer, a diffuser layer (or diffuser plate) and a reflector layer. A least distance 106a between a centerline of the metal bump 72 and a boundary of the glass substrate 106 is between 30 micrometers and 100 micrometers, 50 micrometers and 150 micrometers, 100 micrometers and 250 micrometers or 50 micrometers and 300 micrometers.

[00127] Fifth application: Referring to Fig. 16, this structure of the fifth application is similar to the structure of the fourth application in Fig. 14. The organic light-emitting diodes layer 110 (or a polymer light-emitting diodes layer, PLED layer) is replaced ~~to~~ with the liquid crystal display layer 111. The second substrates 22 is connected to a OLED display substrate through ~~flip-chip~~ flip-chip bonding process, wherein the OLED display substrate comprises a first glass substrate 106 and a

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second glass substrate 108, and an organic light-emitting diodes layer 110 (or a polymer light-emitting diodes layer, PLED layer) and thin film transistor circuit layers (not shown) between the first glass substrate 106 and the second glass substrate 108, wherein multiple transparent electrodes 114 on the bottom surface of the first glass substrate 106 and multiple metal plugs 113 in the first glass substrate 106, wherein the multiple metal plugs 113 are connected to the transparent electrodes 114 respectively. The structure of the first glass substrate 106 can refer to the second substrates 22 in the invention. The metal bumps 72 are connected to the transparent electrodes 114 through a solder layer 107, wherein the solder layer 107 comprises gold-tin alloy, tin-silver alloy, tin-silver-copper alloy, indium, tin-bismuth alloy, or other lead-free alloy. The OLED display substrate comprises multiple OLED display panels. The OLED display substrate may comprise touch screen function, wherein the OLED display substrate comprising an in-cell TFT OLED substrate. A least distance 106a between a centerline of the metal bump 72 and a boundary of the glass substrate 106 is between 30 micrometers and 100 micrometers, 50 micrometers and 150 micrometers, 100 micrometers and 250 micrometers or 50 micrometers and 300 micrometers.

[00128] Sixth application: Referring to Fig. 17a, the second substrates 22 can be a port of an OLED display substrate. The OLED display substrate comprises the second substrates 22 and the second glass substrate 108, and an organic light-emitting diodes layer 110 (or a polymer light-emitting diodes layer, PLED layer), thin film transistor circuit layers (not shown) and transparent electrodes 114 between the second substrates 22 and the second glass substrate 108, wherein the metal plugs 21 connected to transparent electrodes 114 through the first metal layer 26. The OLED display substrate comprises multiple OLED display panels. The OLED display substrate may comprise touch screen function, wherein the OLED display substrate comprising an in-cell TFT OLED substrate.

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[00129] Referring to Fig. 17b, the structure of the OLED display substrate comprises multiple thin film transistors circuits 700 and multiple organic light-emitting components 800 between the second substrates 22 and the second glass substrate 108, wherein the thin film transistors circuit 700 comprises a buffer layer 702, a first gate electrode 704a and a first source electrode 704b formed on the buffer layer 702, a first insulating layer 706 formed on the first gate electrode 704a, the first source electrode 704b and the buffer layer 702. An oxide semiconductor layer 710 is formed on the first insulating layer 706 over the first gate electrode 704a and the first source electrode 704b, wherein the oxide semiconductor layer 710 is connected to the first source electrode 704b through the opening in the first insulating layer 706. A second insulating layer 712 is formed on the oxide semiconductor layer 710. A second gate electrode 714a and a second source electrode 714b formed on the second insulating layer 712, wherein the second source electrode 714b connected to the oxide semiconductor layer 710 through an opening in the second insulating layer 712. A protection layer 716 is formed on the second gate electrode 714a, the second source electrode 714b and the second insulating layer 712. The organic light-emitting component 800 formed on the protection layer 716 and connected to the second source electrode 714b through an opening in the protection layer 716.

[00130] The oxide semiconductor layer 710 comprises a ZnO containing layer, wherein the ZnO containing layer can be doped with a group selected from the group constituted of at least one ionic: Gallium (Ga), indium (In), tin (Sn), zirconium (Zr), hafnium (Hf), cadmium (Cd), magnesium (Mg), vanadium (V). The first gate electrode 704a, the first source electrode 704b, the second gate electrode 714a and the second source electrode 714b are formed of a metal selected from the following groups: tungsten (W), titanium (Ti), molybdenum (Mo), silver (Ag), tantalum (Ta), aluminum (Al), copper (Cu), gold (Au), chromium (Cr) or niobium (Nb).

[00131] The organic light-emitting component 800 comprises an anode layer 802, a cathode layer 804 and an organic light-emitting layer 806 between the anode layer 802 and the cathode layer

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804, wherein the anode layer 802 formed on the protection layer 716 and connected to the second source electrode 714b. A third insulating layer 808 formed on the protection layer 716 and the anode layer 802, then formed a hole/opening in the third insulating layer 808 and on the anode layer 802. Forming the organic light-emitting layer 806 in the opening and on the third insulating layer 808, then formed the cathode layer 804 on the third insulating layer 808 and on the organic light-emitting layer 806. The anode layer 802 is connected to the metal plugs 21 via a conductive layer formed on the opening through the buffer layer 702, a first insulating layer 706 and second insulating layer 712. The cathode layer 804 is connected to the metal plugs 21 via a conductive layer formed on the opening through the buffer layer 702, the first insulating layer 706, the second insulating layer 712 and the third insulating layer 808. The buffer layer 702、the first insulating layer 706, the second insulating layer 712 and the third insulating layer 808 ~~comprises~~ comprise a polyimide, polyamide, acryl resin, benzocyclobutene, phenol resin, oxide layer (buffer layer 702), nitride layer (buffer layer 702).

[00132] The anode layer 802 may contain one or more transparent materials such as indium tin oxide (ITO), indium zinc oxide (IZO), zinc oxide (ZnO), indium gallium oxide (IGO), aluminum zinc oxide (AZO) and In2O3, or non-transparent materials such as Ag, Mg, Al, Pt, Pd, Au, Ni, Nd, Ir, Cr, Li, Ca, Mo, Ti, W, MoW, and Al/Cu. The cathode layer 804 may contain one or more transparent materials such as indium tin oxide (ITO), indium zinc oxide (IZO), zinc oxide (ZnO), indium gallium oxide (IGO), aluminum zinc oxide (AZO) and ~~In2O3~~ In_2O_3.

[00133] The organic light-emitting layer 806 may include a hole transport layer (HTL) and a hole injection layer (HIL) stacked toward the pixel electrode (anode layer 802 or cathode layer 804), and an electron transport layer (ETL) and an electron injection layer (EIL) stacked toward the pixel electrode (anode layer 802 or cathode layer 804). Furthermore, various other layers may be stacked if required. Further, the light-emitting layer 806 comprises a carbazole biphenyl(CBP), (III)(bis(1-

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phenylisoquinoline)(acetylacetonate)iridium, PIQIr(acac)),(III)(bis(1-phenylquinoline)(acetylacetonate)iridium, PQIr(acac)), (III)(tris(1-phenylquinoline)iridium (PQIr), octaethylporphyrin platinum,PtOEP 、 (III))(tris(dibenzoylmethane)(o-phenanthroline)europium(III),PED ： Eu(DBM)3(Phen)),perylene, N,N'-Di(naphthalene-1-yl)-N,N'-diphenyl-benzidine, tris-8-hydroxyquinoline aluminum (PEDOT), copper phthalocyanine,CuPc, 4,4',4"-tris(N-(3-methylphenyl)-N-phenylamino)triphenylamine (MTDATA).

[00134] Referring to Fig. 18 and Fig. 19, an outward of display substrate produced from above first application to sixth application is an unframed display 119, wherein the unframed display 119 comprises a display area 119a has four edges 119b, wherein a gap between ~~the~~ each edge 119b and one of four boundaries of the unframed display 119 has a least distance smaller than 15 micrometers, 20 micrometers, 30 micrometers, 50 micrometers, 100 micrometers, 150 micrometers or 200 micrometers. The unframed display 119 is installed in a shell 123 of a display device 125. Some components (not showed in drawings) can install in the display device 125 (or installed on the second substrates 22), for example, a speaker component, a battery component, a microphone component, a signal receiver component, a wireless signal receiver component, a wireless signal transmitter module.

[00135] Referring to Fig. 19, the display device 125 comprises multiple connecting ports 127 on the shell 123, wherein the connecting ports 127 comprise a signal connecting port, a power connecting port, and/or a ground connecting port. The display device 125 can connect to another one display device 125b to become a bigger display device 129, wherein the connecting ports 127 of the display device 125 are connected to the connecting ports 127 of the display device 125b. Multiple display devices 125 can be combined with a big display device, an advertising ~~billboards~~ billboard.

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The display devices 125 can be used as a tile on the wall of the building. The display devices 125 can be a display unit on a surface of a magic cube.

[00136] The structure of the OLED display substrate disclosed in the Fig. 12 and Fig. 16 can be referred to the paragraph [00125] to the paragraph [00131].

[00137] Those described above are the embodiments to exemplify the present disclosure to enable the person skilled in the art to understand, make and use embodiments of the present disclosure. This description, however, is not intended to limit the scope of the present disclosure. Any equivalent modification and variation according to the spirit of the present disclosure is to be also included within the scope of the claims stated below.

[00138] The components, steps, features, benefits and advantages that have been discussed are merely illustrative. None of them, nor the discussions relating to them, are intended to limit the scope of protection in any way. Numerous other embodiments are also contemplated. These include embodiments that have fewer, additional, and/or different components, steps, features, benefits and advantages. These also include embodiments in which the components and/or steps are arranged and/or ordered differently.

[00139] In reading the present disclosure, one skilled in the art will appreciate that embodiments of the present disclosure can be implemented in hardware, software, firmware, or any combinations of such, and over one or more networks. Suitable software can include computer-readable or machine-readable instructions for performing methods and techniques (and portions thereof) of designing and/or controlling the fabrication and design of integrated circuit chips according to the present disclosure. Any suitable software language (machine-dependent or machine-independent) may be utilized. Moreover, embodiments of the present disclosure can be included in or carried by various signals, e.g., as transmitted over a wireless radio frequency (RF) or

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infrared (IR) communications link or downloaded from the Internet.

[00140] Unless otherwise stated, all measurements, values, ratings, positions, magnitudes, sizes, and other specifications that are set forth in this specification, including in the claims that follow, are approximate, not exact. They are intended to have a reasonable range that is consistent with the functions to which they relate and with what is customary in the art to which they pertain. The scope of protection is limited solely by the claims. That scope is intended and should be interpreted to be as broad as is consistent with the ordinary meaning of the language that is used in the claims when interpreted in light of this specification and the prosecution history that follows and to encompass all structural and functional equivalents.

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CHIP PACKAGE

[0001] This patent application is a continuation of application No. 15261956, filed Sept. 11, 2016, now pending, which claims priority benefits from U.S. provisional patent application No. 62/219249, filed Sept. 16, 2015. This patent application of application No. 15261956 is a continuation-in-part of application No. 14/036256, filed Sept. 25, 2013, now patent No. 9615453, which claims the benefit of priority from U.S. provisional patent application No. 61/705,649, filed Sept. 26, 2012, all of which is incorporated herein by reference in their entirety.

BACKGROUND OF THE DISCLOSURE

Field of the Disclosure

[0002]The patent disclosure a method and structure to manufacture a glass substrate, and disclosed embodiments relate to one or more chip building a system on the glass substrate.

Brief Description of the Related Art

[0003] As is well known, microelectronic devices have a tendency to be minimized and thinned with its functional development and a semiconductor package mounted on a mother board is also following the tendency in order to realize a mounting of high integration.

[0004] When the geometric dimensions of the Integrated Circuits are scaled down, the cost per

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die is decreased while some aspects of performance are improved. The metal connections which connect the Integrated Circuit to other circuit or system components become of relative more importance and have, with the further miniaturization of the IC, an increasingly negative impact on the circuit performance. The parasitic capacitance and resistance of the metal interconnections increase, which degrades the chip performance significantly. Of most concern in this respect is the voltage drop along the power and ground buses and the RC delay of the critical signal paths. Attempts to reduce the resistance by using wider metal lines result in higher capacitance of these wires.

[0005] To solve this problem, the approach has been taken to develop low resistance metal (such as copper) for the wires while low dielectric materials are used in between signal lines.

[0006] Increased Input-Output (IO) combined with increased demands for high performance, and then IC's has led to the development of flip-chip Packages. Flip-chip technology fabricates bumps (typically Pb/Sn solders) on Al pads of chip and interconnects the bumps directly to the package media, which are usually ceramic or plastic based. The flip-chip is bonded face down to the package medium through the shortest path. These technologies can be applied not only to single-chip packaging, but also to higher or integrated levels of packaging in which the packages are larger and to more sophisticated substrates that accommodate several chips to form larger functional units.

[0007] The flip-chip technique, using an area array, has the advantage of achieving the highest density of interconnection to the device and a very low inductance interconnection to the package. However, pre-testability, post-bonding visual inspection, and TCE (Temperature Coefficient of Expansion) matching to avoid solder bump fatigue are still challenges.

[0008] Glass can be used as an interposer to bridge between one or more IC chips and a printed circuit board. In many respects, when used as an interposer / substrate and without the requirement

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for active devices, glass can be a good substitute for a silicon interposer. The advantages of glass in comparison to silicon as an interposer lie in its much lower material cost. Glass also has a CTE closely matched to silicon, so that reliability of interconnects, especially micro-bonds, can be expected to be quite good. Glass has some disadvantages in comparison to silicon – notably its lower thermal conductivity and the difficulty in forming Through Glass Vias (TGV's). Both of these topics are discussed elsewhere in this patent.

SUMMARY OF THE DISCLOSURE

[0009] Embodiments of the present disclosure provide A display device comprises a display panel substrate and a glass substrate over said display panel substrate, wherein said display panel substrate comprises multiple contact pads, a display area, a first boundary, a second boundary, a third boundary and a fourth boundary, wherein said display area comprises a first edge, a second edge, a third edge and a fourth edge, wherein said first boundary is parallel to said third boundary and said first and third edges, wherein said second boundary is parallel to said fourth boundary and said second and fourth edges, wherein a first least distance between said first boundary and said first edge, wherein a second least distance between said second boundary and said second edge, a third least distance between said third boundary and said third edge, a fourth distance between said fourth boundary and said fourth edge, and wherein said first, second, third and fourth least distances are smaller than 100 micrometers, and wherein said glass substrate comprising multiple metal conductors through in said glass substrate and multiple metal bumps are between said glass substrate and said display panel substrate, wherein said one of said metal conductors is connected to one of said contact pads through one of said metal bumps.

[0010] These, as well as other components, steps, features, benefits, and advantages of the present disclosure, will now become clear from a review of the following detailed description of

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illustrative embodiments, the accompanying drawings, and the claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] The drawings disclose illustrative embodiments. They do not set forth all embodiments. Other embodiments may be used in addition or instead. Details that may be apparent or unnecessary may be omitted to save space or for more effective illustration. Conversely, some embodiments may be practiced without all of the details that are disclosed. When the same numeral appears in different drawings, it refers to the same or like components or steps.

[0012] Aspects of the disclosure may be more fully understood from the following description when read together with the accompanying drawings, which are to be regarded as illustrative in nature, and not as limiting. The drawings are not necessarily to scale, emphasis instead being placed on the principles of the disclosure.

[0013] Figs. 1 illustrates a three-dimensional view of a X-axis nets and a Y-axis nets, in accordance with the present disclosure.

[0014] Fig. 2 illustrates a cross-section view of the X-axis nets and the Y-axis nets, in accordance with the present disclosure.

[0015] Fig. 3 illustrates a cross-section view of the Z-axis traces crossed to the X-axis nets and the Y-axis nets, in accordance with the present disclosure.

[0016] Fig. 4 illustrates a three-dimensional view of the Z-axis traces, X-axis nets and the Y-axis nets, in accordance with the present disclosure.

[0017] Figs. 5a-5i illustrate the shape and structure of the Z-axis traces, in accordance with the present disclosure.

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[0018] Figs. 6a-6j illustrate a 1st process of forming a glass substrate, in accordance with the present disclosure.

[0019] Figs. 6k-6n illustrate a top views of the 1st process of forming the glass substrate, in accordance with the present disclosure.

[0020] Figs. 7a-7o illustrate a 2nd process of forming the glass substrate, in accordance with the present disclosure.

[0021] Figs. 7p-7r illustrate a top views of the 2nd process of forming the glass substrate, in accordance with the present disclosure.

[0022] Figs. 8a-8d illustrate cross-section views of the glass substrate and the metal plug, in accordance with the present disclosure.

[0023] Figs. 9a-9s illustrate a process to form multiple traces on a top surface and a bottom surface of the glass substrate, in accordance with the present disclosure.

[0024] Figs. 9t-9u illustrate cross-section views of multiple chips formed on the glass substrate, in accordance with the present disclosure.

[0025] Fig. 9v illustrates a cross-section view of the metal bump, in accordance with the present disclosure.

[0026] Fig. 9w illustrates a cross-section view of multiple chips formed on a top surface and bottom surface of the glass substrate, in accordance with the present disclosure.

[0027] Fig. 9x illustrates a cross-section view of multiple chips and a 3D-IC package formed on a top surface and bottom surface of the glass substrate, in accordance with the present disclosure.

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[0028] Fig. 9y illustrates a top views of the multiple chips on the glass substrate, in accordance with the present disclosure.

[0029] Figs. 10a-10j illustrate a damascene process to form the metal layer on the glass substrate, in accordance with the present disclosure.

[0030] Figs. 11a-11i illustrate an embossing process to form the metal layer on the glass substrate, in accordance with the present disclosure.

[0031] Fig. 12 illustrates a cross-section view of the glass substrate of the first application formed on an OLED display substrate, in accordance with the present disclosure.

[0032] Fig. 13 illustrates a cross-section view of the glass substrate of the second application formed on a MEMs display substrate, in accordance with the present disclosure.

[0033] Fig. 14 illustrates a cross-section view of the glass substrate of the third application formed on a LCD display substrate, in accordance with the present disclosure.

[0034] Fig. 15 illustrates a cross-section view of the glass substrate of the fourth application formed on an another LCD display substrate, in accordance with the present disclosure.

[0035] Fig. 16 illustrates a cross-section view of the glass substrate of the fifth application formed on an OLED display substrate, in accordance with the present disclosure.

[0036] Fig. 17a illustrates a cross-section view of the glass substrate of the sixth application formed on an OLED display substrate, in accordance with the present disclosure.

[0037] Fig. 17b illustrates a cross-section view of the structure of the OLED display substrate, in accordance with the present disclosure.

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[0038] Fig. 18 illustrates a three-dimensional view of the display device, in accordance with the present disclosure.

[0039] Fig. 19 illustrates a big display device combined from multiple display device, in accordance with the present disclosure.

[0040] While certain embodiments are depicted in the drawings, one skilled in the art will appreciate that the embodiments depicted are illustrative and that variations of those shown, as well as other embodiments described herein, may be envisioned and practiced within the scope of the present disclosure.

DETAILED DESCRIPTION OF THE DISCLOSURE

[0041] Fig. 1 illustrates a three-dimensional view of a net 2, 4, wherein the net 4 is under the net 2, wherein the net 2 comprises multiple Y-axis traces 2a and multiple X-axis traces 2b under the Y-axis traces 2a, and wherein the net 4 comprises multiple Y-axis traces 4a and multiple X-axis traces 4b under the Y-axis traces 4a. Multiple gaps 3and 5 are formed in the net 2 and 4. Each of the traces 2a, 2b, 4a and 4b is easily moved to change the size of gaps 3 and gaps 5. The diameter (or width) of traces 2a, 2b, 4a and 4b are the same, such as between 10 and 30 micrometers, between 20 and 100 micrometers, between 40 and 150 micrometers, between 50 and 200 micrometers, between 200 and 1000 micrometers or between 500 and 10000 micrometers. The traces 2a, 2b, 4a and 4b may be metal traces or polymer traces, such as copper traces, copper-gold alloy traces, copper-gold-palladium alloy traces, copper-gold-silver alloy traces, copper-platinum alloy traces, copper-iron alloy traces, copper-nickel alloy traces, copper-tungsten traces, tungsten traces, brass wires, zinc plated brass wires, stainless wires, nickel plated stainless wires, phosphor bronze wires, copper plated the aluminum wires, aluminum traces, phenolic resin traces, epoxy resin traces, melamine-

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formaldehyde resin traces or polysiloxanes resin traces. The cross-section shape of traces 2a, 2b, 4a and 4b may be a circular shape, a Square shape, an oblong shape, a rectangle shape or a flat shape.

[0042] Fig. 2 illustrates a cross-section view of the net 2 and the net 4. The gaps 3 and gaps 5 are aligned with each other.

[0043] Next, referring to Fig. 3, multiple metal traces 6 are crossed the net 2 and the net 4 through the gaps 3 and gaps 5. The diameter (or width) of metal traces 6 is between 10 and 30 micrometers, between 20 and 100 micrometers, between 40 and 150 micrometers, between 50 and 200 micrometers, between 200 and 1000 micrometers or between 500 and 10000 micrometers. The traces 6 may be metal traces, such as copper traces, copper-gold alloy traces, copper-gold-palladium alloy traces, copper-gold-silver alloy traces, copper-platinum alloy traces, copper-iron alloy traces, copper-nickel alloy traces, copper-tungsten traces, tungsten traces, brass wires, zinc plated brass wires, stainless wires, nickel plated stainless wires, phosphor bronze wires, copper plated the aluminum wires, aluminum traces, titanium-containing layer plated the copper wires, tantalum-containing layer plated the copper wires. The cross-section shape of traces 6 may be a circular shape, a square shape, an oblong shape, a rectangle shape or a flat shape. The diameter (or width) of traces 6 may be the same with the traces 2a, 2b, 4a and 4b or different with the traces 2a, 2b, 4a and 4b.

[0044] Furthermore, we proposed the material of the traces 6 is copper-tungsten alloy, wherein the copper in the copper-tungsten alloy is 50 percent and the tungsten in the copper-tungsten alloy is 50 percent, the copper in the copper-tungsten alloy is 60 percent and the tungsten in the copper-tungsten alloy is 40 percent, the copper in the copper-tungsten alloy is 70 percent and the tungsten in the copper-tungsten alloy is 30 percent, the copper in the copper-tungsten alloy is 80 percent and the tungsten in the copper-tungsten alloy is 20 percent, the copper in the copper-tungsten alloy is 90 percent and the tungsten in the copper-tungsten alloy is 10 percent, the copper in the copper-

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tungsten alloy is 40 percent and the tungsten in the copper-tungsten alloy is 60 percent, the copper in the copper-tungsten alloy is 30 percent and the tungsten in the copper-tungsten alloy is 70 percent.

[0045] Fig. 4 illustrates a three-dimensional view of a net 2, 4 and traces 6.

[0046] Fig. 5a-5i illustrate the shape and structure of the traces 6. In Fig. 5a, the cross-section shape of traces 6 is a circular shape. In Fig. 5d, the cross-section shape of traces 6 is a square shape. In Fig. 5g, the cross-section shape of traces 6 is a rectangle shape. In Fig. 5b, the cross-section shape of traces 6 is a circular shape and a first covering layer 6a is cover on the traces 6, wherein the first covering layer 6a may be a metal layer, such as a nickel-containing layer, a zinc-containing layer, a titanium-containing layer, a tantalum-containing layer, a silver-containing layer, a chromium-containing layer and wherein the first covering layer 6a may be an anti-oxidation layer, such as an oxide-containing layer. In Fig. 5e, the cross-section shape of traces 6 is a square shape and a first covering layer 6a is cover on the traces 6, wherein the first covering layer 6a may be a metal layer, such as a nickel-containing layer, a zinc-containing layer, a titanium-containing layer, a tantalum-containing layer, a silver-containing layer, a chromium-containing layer and wherein the first covering layer 6a may be an anti-oxidation layer, such as an oxide-containing layer. In Fig. 5h, the cross-section shape of traces 6 is a rectangle shape and a first covering layer 6a is cover on the traces 6, wherein the first covering layer 6a may be a metal layer, such as a nickel-containing layer, a zinc-containing layer, a titanium-containing layer, a tantalum-containing layer, a silver-containing layer, a chromium-containing layer and wherein the first covering layer 6a may be an anti-oxidation layer, such as an oxide-containing layer. In Fig. 5c, the cross-section shape of traces 6 is a circular shape and a second covering layer 6b is cover on the first covering layer 6a, wherein the second covering layer 6b may be an adhesion layer, such as a nickel-containing layer, a zinc-containing layer, a titanium-containing layer, a tantalum-containing layer, a silver-containing layer, a chromium-containing layer and wherein the first covering layer 6a may be an anti-oxidation layer, such as an

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oxide-containing layer. In Fig. 5f, the cross-section shape of traces 6 is a square shape and a second covering layer 6b is cover on the first covering layer 6a, wherein the second covering layer 6b may be an adhesion layer, such as a nickel-containing layer, a zinc-containing layer, a titanium-containing layer, a tantalum-containing layer, a silver-containing layer, a chromium-containing layer and wherein the first covering layer 6a may be an anti-oxidation layer, such as an oxide-containing layer. In Fig. 5i, the cross-section shape of traces 6 is an oblong shape and a second covering layer 6b is cover on the first covering layer 6a, wherein the second covering layer 6b may be an adhesion layer, such as a nickel-containing layer, a zinc-containing layer, a titanium-containing layer, a tantalum-containing layer, a silver-containing layer, a chromium-containing layer and wherein the first covering layer 6a may be an anti-oxidation layer, such as an oxide-containing layer.

[0047] Next, Figs. 6a-6j are illustrated a 1st process of forming a glass substrate of the invention. Please referring to Fig. 6a, the traces 6 are stretched to a suitable length L1, e.g., smaller than 5 meters, such as between 0.5 and 1 meter, or between 1 and 3 meters. At the same time, the net 4 is moved down to a suitable location. The pitch t1 between the traces 2a, 2b, 4a, 4b is greater than the diameter (or width) of traces 6.

[0048] Next, referring to Fig. 6b, the traces 2a, 2b, 4a and 4b are moved to change the pitch t1 to a pitch t2, then the traces 6 are closed up to a pitch t3. The pitch t3 substantially the same with the diameter (or width) of the traces 2a, 2b, 4a and 4b, such as between 5 and 20 micrometers, between 20 and 50 micrometers, between 30 and 80 micrometers, between 20 and 100 micrometers, between 40 and 150 micrometers, between 50 and 200 micrometers, between 200 and 1000 micrometers or between 500 and 10000 micrometers. At the same time, maybe applied a force to stretch the traces 6, 2a, 2b, 4a and 4b and make the traces 6 keep strength and keep the pitch t3 fixed.

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[0049] Next, referring to Fig. 6c, a thermal resistance layer 8 is formed on surfaces of the net 4. The thermal resistance layer 8 may be a polymer layer, such as a thermosetting resin, phenolic resin, epoxy resin, melamine-formaldehyde resin, polysiloxanes resin, plaster layer, wherein the thermal resistance layer 8 has a heat deflection temperature between 400 and 900 ℃. When a liquid thermal resistance layer 8 formed on the net 4 and the thermal resistance layer 8 permeated the net 4 through the gaps 5, wherein the thermal resistance layer 8 covers the gaps 5 between traces 4a, traces 4b and traces 6, then curing the thermal resistance layer 8. The thermal resistance layer 8 has a thickness between 0.05 and 1 meter.

[0050] Next, referring to Fig. 6d, a mold 10 is provided between the net 2 and the net 4, wherein the mold 10 surrounds the traces 6 and on the thermal resistance layer 8. The mold 10 is held up by a machine or a device. The mold 10 may be a metal mold, a ceramics mold or a polymer mold, which has a heat deflection temperature between 400 ℃ and 900 ℃ or between 800 ℃ and 1300 ℃.

[0051] Next, referring to Fig. 6e, a fixed layer 12 is formed on the thermal resistance layer 8, wherein the fixed layer 12 may be a glass layer or a polymer layer. When the material of the fixed layer 12 is glass, the fixed layer 12 is a high temperature liquid to form on the thermal resistance layer 8, and then the fixed layer 12 down to a suitable temperature becomes a solid state. The fixed layer 12 has a thickness between 0.01 and 1 meter. The bottom of traces 6 is fixed by the fixed layer 12.

[0052] Next, referring to Fig. 6f, the traces 6 under the net 4 are cut. A tank 14 carries the mold 10, net 4 and the fixed layer 12.

[0053] Next, referring to Fig. 6g, a glass layer (liquid form) 16 is formed on the fixed layer 12. The glass layer 16 is a high temperature liquid to form on the fixed layer 12 and fill in the mold 10, and then the glass layer 16 down to a suitable temperature becomes a solid state, wherein the glass

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layer 16 has a glass transition temperature between 300°C and 900°C, between 500°C and 800°C, between 900°C and 1200°C or between 1000°C and 1800°C. The glass layer 16 is a low melting point glass material, wherein the glass layer 16 has a melting point between 300°C and 900°C, 800°C and 1300°C, between 900°C and 1600°C, between 1000°C and 1850°C, or between 1000°C and 2000°C, wherein the melting point may smaller than 1500°C. The glass layer 16 has a thickness greater than 0.5 meters or greater than 0.1 meter. Furthermore, there is a few bubbles or no bubble in glass layer 16, for example, there is zero to 3 bubbles in one cubic meter of the glass layer 16, 1 to 10 bubbles in one cubic meter of the glass layer 16, 5 to 30 bubbles in one cubic meter of the glass layer 16 or 20 to 60 bubbles in one cubic meter of the glass layer 16, wherein the bubble has a diameter between 0.0001 and 0.001 centimeters, between 0.001 and 0.05 centimeters, between 0.05 and 0.1 centimeters or between 0.05 and 0.5 centimeters. The glass layer 16 may be removed bubbles through multiple processes of a laminating process, a squeezing process and a heating process.

[0054] The glass layer 16 refers to an amorphous solid. The material of the glass layer 16 may be included soda-lime glass, boro-silicate glass, alumo-silicate glass, fluoride glasses, phosphate glasses or chalcogen glasses. For example, the composition of the soda-lime glass comprises SiO_2 (74%), Na_2O (13%), CaO (10.5%), Al_2O_3 (1.3%), K_2O (0.3%), SO3 (0.2%), MgO (0.2%), Fe2O3 (0.04%), TiO2 (0.01%), the composition of the boro-silicate glass comprises SiO_2 (81%), B_2O_3 (12%), Na_2O (4.5%), Al_2O_3 (2.0%), the composition of the phosphate glasses comprises a percentage of the P_2O_5 material between 3% and 10% or between 5% and 20%.

[0055] A glass, once formed into a solid body, is capable of being softened and perhaps remitted into a liquid form. The "glass transition temperature" of a glass material is a temperature below which the physical properties of the glass are similar to those of a solid and above which the glass material behaves like a liquid.

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[0056] If a glass is sufficiently below the glass transition temperature, molecules of the glass may have little relative mobility. As a glass approaches the glass transition temperature, the glass may begin to soften and with increasing temperature, the glass will ultimately melt into the liquid state. Thus, a glass body may be softened to an extent sufficient to enable manipulation of the body's shape, allowing for the formation of holes or other features in the glass body. Once the desired form is obtained, glass is usually annealed for the removal of stresses. Surface treatments, coatings or lamination may follow to improve the chemical durability (glass container coatings, glass container internal treatment), strength (toughened glass, bulletproof glass, windshields), or optical properties (insulated glazing, anti-reflective coating).

[0057] Furthermore, the glass layer 16 may be replaced by a polymer layer. When the polymer layer cured to a solid state, then the polymer layer has a coefficient of expansion between 3 and 10 ppm/°C.

[0058] Next, referring to Fig. 6h, the mold 10 and the tank 14 are removed and cut the traces 6 from net 2.

[0059] Next, referring to Fig. 6i, the net 4 and the thermal resistance layer 8 are removed, and then a column 25 is produced.

[0060] Next, referring to Fig. 6j, the traces 6 out of the column 25 are removed and cutting the column 25 to produce multiple first substrates 20, wherein the first substrate 20 has a thickness between 20 and 100 micrometers, between 50 and 150 micrometers, between 100 and 300 micrometers or between 150 and 2000 micrometers or greater than 1000 micrometers. The first substrates 20 may be made a planarization process using a suitable process, such as a chemical mechanical polishing (CMP) procedure, mechanical grinding, or laser drilling

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[0061] Next, referring to Fig. 6k, the first substrate 20 comprises multiple second substrates 22. The second substrates 22 are well-regulated an array in the first substrate 20. Each of the second substrates22 has multiple metal plugs 21, wherein the metal plug 21 is formed from metal traces 6. The metal plug 21 has the same material and structure with metal trace 6.

[0062] Next, referring to Figs. 6l-6n, the metal plugs 21 may be arranged in different types, such as Fig. 6l, the metal plugs 21 are arranged on the side portions of the second substrate 22, or such as Fig. 6m, the metal plugs 21 are arranged on the side portions and center portion of the second substrate 22, or such as Fig. 6n, some portions of the second substrate 22 are not arranged the metal plugs 21.

[0063] Figs. 7a-7m are illustrated a 2nd process of forming a glass substrate of the invention. Please referring to Fig. 7a-7b, there is illustrated a first metal plate 7 in Fig. 7a, illustrated a three-dimensional view of the first metal plate 7 in Fig. 7b. The first metal plate 7 has a thickness between 25 micrometers and 1000 micrometers, between 20 micrometers and 500 micrometers, between 30 micrometers and 400 micrometers or between 20 micrometers and 250 micrometers. The first metal plate 7 comprising a first portion 71, a second portion 73 and a third portion 75 between the first portion 71 and second portion 73, wherein the third portion 75 comprises multiple non-circular metal traces 752 are connected to the first portion 71 and the second portion 73, wherein a cross-section view of the non-circular trace 752 comprising a square shape or a rectangle shape. One of the non-circular traces 752 has a width greater than the thickness of one of the non-circular traces 752, such as between 150 micrometers and 3000 micrometers, between 300 micrometers and 1500 micrometers, between 200 micrometers and 800 micrometers or between 100 micrometers and 500 micrometers. Multiple gaps 754 are between each two neighboring non-circular traces 752, wherein the gap 754 is between 50 micrometers and 3000 micrometers, between 300 micrometers and 1500 micrometers, between 200 micrometers and 800 micrometers or between 150 micrometers and 500

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micrometers. The first metal plate 7 comprises a copper metal layer, copper-gold alloy metal layer, copper-gold-palladium alloy metal layer, copper-gold-silver alloy metal layer, copper-platinum alloy metal layer, copper-iron alloy metal layer, copper-nickel alloy metal layer, copper-tungsten metal layer, tungsten metal layer, brass metal layer, zinc plated brass metal layer, stainless metal layer, nickel plated stainless metal layer, phosphor bronze metal layer, copper plated the aluminum metal layer or aluminum metal layer. There are two holes 71a in the first portion 71, wherein the hole 71a has a diameter between 600 micrometers and 2000 micrometers, between 1000 micrometers and 3000 micrometers or between 2000 micrometers and 5000 micrometers. There are two holes 73a corresponding to the hole 71a in the first portion 71, wherein the hole 73a has a diameter between 600 micrometers and 2000 micrometers, between 1000 micrometers and 3000 micrometers or between 2000 micrometers and 5000 micrometers, wherein a first least distance between the two holes 71a is substantially the same to a second least distance between the two holes 73a.

[0064] Next, referring to Figs. 7c-7d, there is illustrated a second metal plate 9 in Fig. 7c, illustrated a three-dimensional view of the second metal plate 9 in Fig. 7d. The second metal plate 9 has a thickness between 25 micrometers and 600 micrometers, between 20 micrometers and 300 micrometers, between 30 micrometers and 250 micrometers or between 25 micrometers and 180 micrometers. There are two holes 90a in the second metal plate 9, wherein the hole 90a has a diameter between 600 micrometers and 2000 micrometers, between 1000 micrometers and 3000 micrometers or between 2000 micrometers and 5000 micrometers, wherein a third least distance between the two holes 90a is substantially the same to a second least distance between the two holes 73a and substantially the same to the first least distance between the two holes 71a. The second metal plate 9 comprises a copper metal layer, copper-gold alloy metal layer, copper-gold-palladium alloy metal layer, copper-gold-silver alloy metal layer, copper-platinum alloy metal layer, copper-iron alloy metal layer, copper-nickel alloy metal layer, copper-tungsten metal layer, tungsten metal

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layer, brass metal layer, zinc plated brass metal layer, stainless metal layer, nickel plated stainless metal layer, phosphor bronze metal layer, copper plated the aluminum metal layer or aluminum metal layer.

[0065] Next, referring to Fig. 7e, there is illustrated a three-dimensional view of a third metal plate 11 in Fig. 7e. The third metal plate 11 has a thickness between 25 micrometers and 600 micrometers, between 20 micrometers and 300 micrometers, between 30 micrometers and 250 micrometers or between 25 micrometers and 180 micrometers. There are four holes 110a, 112a, 114a, 116a in the third metal plate 11, wherein the hole 110a, 112a, 114a, 116a have a diameter between 600 micrometers and 2000 micrometers, between 1000 micrometers and 3000 micrometers or between 2000 micrometers and 5000 micrometers, wherein a fourth least distance between the hole 110a and hole 112a and a fifth least distance between the hole 114a and hole 116a are substantially the same to a second least distance between the two holes 73a and substantially the same to the first least distance between the two holes 71a. The third metal plate 11 comprises a copper metal layer, copper-gold alloy metal layer, copper-gold-palladium alloy metal layer, copper-gold-silver alloy metal layer, copper-platinum alloy metal layer, copper-iron alloy metal layer, copper-nickel alloy metal layer, copper-tungsten metal layer, tungsten metal layer, brass metal layer, zinc plated brass metal layer, stainless metal layer, nickel plated stainless metal layer, phosphor bronze metal layer, copper plated the aluminum metal layer or aluminum metal layer.

[0066] Next, referring to Fig. 7f-Fig.7i, providing two bolts 130, 132 pass through two holes 150a of a fixing metal plate 150 and providing two bolts 134, 136 pass through two holes 152a of a fixing metal plate 152 respectively. Next, the bolts 130, 132, 134, 136 are passing through the holes 110a, 112a, 114a, 116a of the third metal plate 11 respectively and the third metal plate 11 is formed on the fixing metal plate 150 and the fixing metal plate 152. Next, the bolts 130, 132 are passing through the hole 90a of the second metal plate 9 and the bolts 134, 136 are passing through the hole

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90a of another the second metal plate 9, then the second metal plates 9 are formed on the third metal plate 11. Next, the bolts 130, 132, 134, 136 are passing through the holes 71a, 73a of the first metal plate 7 respectively and the first metal plate 7 is formed on the second metal plates 9. Next, repeating to site another the second metal plates 9 on another the first metal plate 7 sequentially until to expose a top of the bolts 130, 132, 134, 136. Next, the top of the bolts 130, 132, 134, 136 are passing through the holes 110a, 112a, 114a and 116a of another the third metal plate 11 respectively and the third metal plate 11 is formed on the second metal plates 9. Next, the top of the bolts 130, 132 are passing through two holes 150a of another the fixing metal plate 150 and the top of the bolts 134, 136 are passing through two holes 152a of another the fixing metal plate 152 respectively, then the fixing metal plates 150, 152 are formed on the third metal plate 11. Finally, providing four sleeve nuts 17 lock on the top of the bolts 130, 132, 134, 136. Then, multiple the first metal plates 7, multiple the second metal plates 9, two the third metal plates 11, two fixing metal plates 150 and two fixing metal plates 152 forming a metal trace block 19.

[0067] Next, referring to Fig. 7j the metal trace block 19 is put in a mold 23. The mold 23 may be a metal mold, a ceramics mold or a polymer mold, which has a heat deflection temperature between 400 ℃ and 900 ℃ or between 800 ℃ and 1300 ℃. The mold 23 comprises a gas inlet 23a and a liquid input 23b, wherein the gas inlet 23a is used to input N_2 gas and the liquid input 23b is used to input the liquid form glass layer.

[0068] Next, referring to Fig. 7k, the glass layer (liquid form) 16 fill in the mold 23. The glass layer 16 is a high temperature liquid and fill in the mold 23, and then the glass layer 16 down to a suitable temperature becomes a solid state, wherein the glass layer 16 has a glass transition temperature between 300°C and 900°C, between 500°C and 800°C, between 900°C and 1200°C or between 1000°C and 1800°C. The glass layer 16 is a low melting point glass material, wherein the glass layer 16 has a melting point between 300°C and 900°C, 800°C and 1300°C, between 900°C

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and 1600°C, between 1000°C and 1850°C, or between 1000°C and 2000°C, wherein the melting point may smaller than 1500°C. Furthermore, there is a few bubbles or no bubble in glass layer 16, for example, there is zero to 3 bubbles in one cubic meter of the glass layer 16, 1 to 10 bubbles in one cubic meter of the glass layer 16, 5 to 30 bubbles in one cubic meter of the glass layer 16 or 20 to 60 bubbles in one cubic meter of the glass layer 16, wherein the bubble has a diameter between 0.0001 and 0.001 centimeters, between 0.001 and 0.05 centimeters, between 0.05 and 0.1 centimeters or between 0.05 and 0.5 centimeters. The glass layer 16 may be removed bubbles through multiple processes of a laminating process, a squeezing process and a heating process.

[0069] Next, referring to Fig. 7l, the mold 23is removed and cut the glass layer 16 along a cutting line 16a to remove the fixing metal plate 150, the fixing metal plate 152, the first portion 71 of the first metal plate 7, the second portion 73 of the first metal plate 7 and two the third metal plates 11, and then the column 25 is produced, showed in the Fig. 7m.

[0070] Next, referring to Fig. 7n, cutting the column 25 to produce multiple first substrates 20, wherein the first substrate 20 has a thickness between 20 and 100 micrometers, between 50 and 150 micrometers, between 100 and 300 micrometers or between 150 and 2000 micrometers or greater than 1000 micrometers. The first substrates 20 may be made a planarization process using a suitable process, such as a chemical mechanical polishing (CMP) procedure, mechanical grinding, or laser drilling.

[0071] Next, referring to Fig. 7o, the first substrate 20 comprises multiple second substrates 22. The second substrates 22 are well-regulated an array in the first substrate 20. Each of the second substrates has multiple metal plugs 21, wherein the metal plug 21 is formed from the non-circular metal traces 752. The metal plug 21 has the same material, structure and shape with the non-circular metal traces 752. A first pitch 21a and a second pitch 21b are between the metal plugs 21, wherein

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the first pitch 21a is controlled or the same-2 by a distance of the gap 754 and wherein the second pitch 21b is controlled by a distance of adjacent the non-circular traces 752.

[0072] Next, referring to Figs. 7p-7r, the metal plugs 21 may be arranged in different types, such as Fig. 7p, the metal plugs 21 are arranged on the side portions of the second substrate 22, or such as Fig. 7q, the metal plugs 21 are arranged on the side portions and center portion of the second substrate 22, or such as Fig. 7r, some portions of the second substrate 22 are not arranged the metal plugs 21.

[0073] Fig. 8a illustrates a cross-section view of the second substrate 22 illustrates a cross-section view of the metal plug 21. The second substrate 22 comprises an amorphous solid glass layer/body 16 and multiple metal plugs 21, wherein the amorphous solid glass layer/body 16 having a top surface and an opposing bottom surface and the metal plugs 21 extending through the amorphous solid glass layer/body 16 beginning at the top surface and ending at the bottom surface. The top surface of the metal plugs 21 are the same area as the bottom surface of the metal plugs 21.

[0074] Please referring Fig. 8b, the top surface of the metal plugs 21 and the top surface of the amorphous solid glass layer/body 16 are substantially coplanar. The bottom surface of the metal plugs 21 and the bottom surface of the amorphous solid glass layer/body 16 are substantially coplanar.

[0075] Please referring Fig. 8c, the top surface of the metal plugs 21 comprises a top surface of the metal traces 6/ metal traces 752 and a top surface of the first covering layer 6a are substantially coplanar with the top surface of the amorphous solid glass layer/body 16. The bottom surface of the metal plugs 21 comprises a bottom surface of the metal traces 6/ metal traces 752 and a bottom surface of the first covering layer 6a are substantially coplanar with the bottom surface of the amorphous solid glass layer/body 16.

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[0076] Please referring Fig. 8d, the top surface of the metal plugs 21 comprises a top surface of the metal traces 6/ metal traces 752, a top surface of the first covering layer 6a and a top surface of the second covering layer 6b are substantially coplanar with the top surface of the amorphous solid glass layer/body 16. The bottom surface of the metal plugs 21 comprises a bottom surface of the metal traces 6/ metal traces 752, a bottom surface of the first covering layer 6a and a bottom surface of the second covering layer 6b are substantially coplanar with the bottom surface of the amorphous solid glass layer/body 16.

[0077] Fig. 9a-Fig. 9t illustrate a process to form multiple traces on a top surface and a bottom surface of the first substrate 20.

[0078] Next, referring to Fig. 9a, a first dielectric layer 24 is formed on the top surface of the first substrate 20, wherein the first dielectric layer 24 may include or maybe a layer of silicon oxide (such as SiO_2), silicon nitride (such as Si_3N_4), silicon oxynitride (such as SiON), silicon oxycarbide (such as SiOC), phosphosilicate glass (PSG), silicon carbon nitride (such as SiCN), low k dielectric layer (K between 0.5 and 3), or polymer (such as polyimide, benzocyclobutene (BCB), polybenzoxazole (PBO), poly-phenylene oxide (PPO), epoxy, or silosane). The first dielectric layer 24 may be formed or deposited using a suitable process. The first dielectric layer 24 has a thickness between 0.3 and 5 micrometers, between 2 and 10 micrometers, between 1 and 30 micrometers or greater than 30 micrometers.

[0079] Next, referring to Fig. 9b, multiple openings 24a are formed in the first dielectric layer 24 to expose the metal plugs 21. The openings 24a may be formed in the first dielectric layer 24 by a suitable process, such as etching. The opening 24a has a width between 0.3 and 3 micrometers, between 0.5 and 8 micrometers, between 2 and 20 micrometers or between 2 and 50 micrometers.

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[0080] Next, referring to Fig. 9c, a first metal layer 26 is formed on the first dielectric layer 24, on the metal plugs 21 and in the openings 24a. The first metal layer 26 may include an adhesion/barrier layer, such as a layer of titanium, a titanium-tungsten alloy, titanium nitride, chromium, tantalum, tantalum nitride, nickel or nickel vanadium formed using a suitable process, such as a vacuum deposition, a Physical Vapor Deposition (PVD), a Plasma Enhanced Chemical Vapor Deposition (PECVD), a sputtering process or an electroplating process, with a thickness, e.g., between 1 nanometer and 2 micrometers, between 0.3 and 3 micrometers or between 0.5 and 10 micrometers.

[0081] Next, referring to Fig. 9d, a second metal layer 28 is formed on the first metal layer 26. The second metal layer 28 maybe comprises copper, nickel, gold or aluminum formed using a suitable process, such as a vacuum deposition, a Physical Vapor Deposition (PVD), a Plasma Enhanced Chemical Vapor Deposition (PECVD), a sputtering process or an electroplating process, with a thickness, e.g., between 1 nanometer and 5 micrometers, between 1 and 5 micrometers or between 5 and 30 micrometers.

[0082] Next, referring to Fig. 9e, a photoresist layer 30 is formed on the second metal layer 28 by using a suitable process, such as a spin coating process or a lamination process. Next, a photo exposure process using a 1X stepper and a development process using a chemical solution can be employed to form multiple openings 30a, exposing the second metal layer 28, in the photoresist layer. The photoresist layer 30 may have a thickness, e.g., between 3 and 50 micrometers, wherein the photoresist layer 30 may be a positive-type photo-sensitive resist layer or negative-type photo-sensitive resist layer.

[0083] Next, referring to Fig. 9f, remove the first metal layer 26 and the second metal layer 28 are under the openings 30a by using a suitable process, such as an etching process.

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[0084] Next, referring to Fig. 9g, remove the photoresist layer 30 by using a clean process.

[0085] Next, referring to Fig. 9h, a second dielectric layer 32 is formed on the first dielectric layer 24 and on the second metal layer 28, wherein the second dielectric layer 32 may include or may be a layer of silicon oxide (such as SiO_2), silicon nitride (such as Si_3N_4), silicon oxynitride (such as SiON), silicon oxycarbide (such as SiOC), phosphosilicate glass (PSG), silicon carbon nitride (such as SiCN), low k dielectric layer (K between 0.5 and 3), or polymer (such as polyimide, benzocyclobutene (BCB), polybenzoxazole (PBO), poly-phenylene oxide (PPO), epoxy, or silosane). The second dielectric layer 32 may be formed or deposited using a suitable process. The second dielectric layer 32 has a thickness between 0.3 and 5 micrometers, between 2 and 10 micrometers, between 1 and 30 micrometers or greater than 30 micrometers.

[0086] Next, referring to Fig. 9i, multiple openings 32a are formed in the second dielectric layer 32 to expose the second metal layer 28. The openings 32a may be formed in the second dielectric layer 32 by a suitable process, such as etching. The opening 32a has a width between 0.3 and 3 micrometers, between 0.5 and 8 micrometers, between 2 and 20 micrometers or between 2 and 50 micrometers.

[0087] Next, referring to Fig. 9j, a third metal layer 34 is formed on the second dielectric layer 32, on the second metal layer 28 and in the openings 32a. The third metal layer 34 may include an adhesion/barrier layer, such as a layer of titanium, a titanium-tungsten alloy, titanium nitride, chromium, tantalum, tantalum nitride, nickel or nickel vanadium formed using a suitable process, such as a vacuum deposition, a Physical Vapor Deposition (PVD), a Plasma Enhanced Chemical Vapor Deposition (PECVD), a sputtering process or an electroplating process, with a thickness, e.g., between 1 nanometer and 2 micrometers, between 0.3 and 3 micrometers or between 0.5 and 10 micrometers.

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[0088] Next, referring to Fig. 9k, a fourth metal layer 36 is formed on the third metal layer 34. The fourth metal layer 36 maybe comprises copper, nickel, gold or aluminum formed using a suitable process, such as a vacuum deposition, a Physical Vapor Deposition (PVD), a Plasma Enhanced Chemical Vapor Deposition (PECVD), a sputtering process or an electroplating process, with a thickness, e.g., between 1 nanometer and 5 micrometers, between 1 and 5 micrometers or between 5 and 30 micrometers.

[0089] Next, referring to Fig. 9l, a photoresist layer 38 is formed on the fourth metal layer 36 by using a suitable process, such as a spin coating process or a lamination process. Next, a photo exposure process using a 1X stepper and a development process using a chemical solution can be employed to form multiple openings 38a, exposing the fourth metal layer 36, in the photoresist layer. The photoresist layer 38 may have a thickness, e.g., between 3 and 50 micrometers, wherein the photoresist layer 38 may be a positive-type photo-sensitive resist layer or negative-type photo-sensitive resist layer.

[0090] Next, referring to Fig. 9m, remove the third metal layer 34 and the fourth metal layer 36 are under the openings 38a by using a suitable process, such as an etching process.

[0091] Next, referring to Fig. 9n, remove the photoresist layer 38 by using a clean process.

[0092] Next, referring to Fig. 9o, a third dielectric layer 40 is formed on the second dielectric layer 32 and on the fourth metal layer 36, wherein the third dielectric layer 40 may include or maybe a layer of silicon oxide (such as SiO_2), silicon nitride (such as Si_3N_4), silicon oxynitride (such as SiON), silicon oxycarbide (such as SiOC), phosphosilicate glass (PSG), silicon carbon nitride (such as SiCN), low k dielectric layer (K between 0.5 and 3), or polymer (such as polyimide, benzocyclobutene (BCB), polybenzoxazole (PBO), poly-phenylene oxide (PPO), epoxy, or silosane). The third dielectric layer 40 may be formed or deposited using a suitable process. The third

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dielectric layer 40 has a thickness between 0.3 and 5 micrometers, between 2 and 10 micrometers, between 1 and 30 micrometers or greater than 30 micrometers.

[0093] Next, referring to Fig. 9p, multiple openings 40a are formed in the third dielectric layer 40 to expose the fourth metal layer 36. The openings 40a may be formed in the third dielectric layer 40 by a suitable process, such as etching. The opening 40a has a width between 0.3 and 3 micrometers, between 0.5 and 8 micrometers, between 2 and 20 micrometers or between 2 and 50 micrometers.

[0094] Next, referring to Fig. 9q, a protecting layer 42 is formed in the openings 40a, on the third dielectric layer 40 and on the fourth metal layer 36, which can protect the third dielectric layer 40 not to be damaged and the fourth metal layer 36 not be damaged and oxidized.

[0095] Next, referring to Fig. 9r, repeat the processes of Fig.9a-Fig.9p to form the first dielectric layer 24, the first metal layer 26, the second metal layer 28, the second dielectric layer 32, the third metal layer 34, the fourth metal layer 36 and the third dielectric layer 40 on the bottom surface of the first substrate 20.

[0096] Furthermore, referring to Fig. 9s, a passive device 44 may be formed in the first metal layer 28 and the second metal layer 36, such as an inductor, a capacitor or a resistor.

[0097] Next, referring to Fig. 9t, multiple chips 46 and chips 56 set up over the third dielectric layer 40 through a flip-chip package process or a wire-bonding package process, wherein the chip 46 or 56 comprises may be a memory chip, such as NAND-Flash memory chip, Flash memory chip, DRAM chip, SRAM chip or SDRAM chip, a central-processing-unit (CPU) chip, a graphics-processing-unit (GPU) chip, a digital-signal-processing (DSP) chip, a baseband chip, a wireless local area network (WLAN) chip, a logic chip, an analog chip, a global-positioning-system (GPS)

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chip, a "Bluetooth" chip, or a chip including one or more of a CPU circuit block, a GPU circuit block, a DSP circuit block, a memory circuit block (such as DRAM circuit block, SRAM circuit block, SDRAM circuit block, Flash memory circuit block, or NAND-Flash memory circuit block), a baseband circuit block, a Bluetooth circuit block, a GPS circuit block, a MEMS chip, a COMS image sensor device, a WLAN circuit block, and a modem circuit block, from the semiconductor wafer.

[0098] The chips 46 are set up on the third dielectric layer 40 through a flip-chip package process, wherein the chip 46 comprises multiple metal pads 48 and multiple metal bumps 50 formed on the metal pads 48. The metal pad 48 may be an electroplated copper pad, a damascene copper pad or an aluminum pad. The metal bump 50 comprises an adhesion/barrier metal layer formed on the metal pad 48, an electroplated metal layer or an electro-less metal layer formed on the adhesion/barrier metal layer, wherein the adhesion/barrier metal layer comprises a titanium-containing layer, a chromium-containing layer, a tantalum-containing layer or a nickel layer, and the electroplated metal layer comprises a copper layer, a gold layer, a nickel layer, a tin-containing layer, a solder layer, a solder layer over a nickel layer and a copper layer, and the electro-less layer comprises a copper layer, a gold layer or a nickel layer. The electroplated metal layer has a thickness between 2 and 5 micrometers, between 5 and 30 micrometers or between 10 and 50 micrometers. The metal bumps 50 are connected to the fourth metal layer 36 exposed by the openings 40a through a solder layer 54, wherein the solder layer 54 is formed on the fourth metal layer 36 exposed by the openings 40a or is a portion of the metal bump

[0099] 50. An underfill layer 52 is formed between the chips 46 and the third dielectric layer 40.

[00100] The chips 56 are set up over the third dielectric layer 40 through a polymer adhesion layer 60, wherein the chip 56 comprises multiple metal pads 58. The metal pad 58 may be an

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electroplated copper pad, a damascene copper pad or an aluminum pad. Multiple metal wires 62 are connected to the metal pads 58 and the fourth metal layer 36 exposed by the openings 40a, wherein the metal wires 62 comprises a gold wire, a copper wire, a metal alloy wire, a silver-containing wire, an aluminum-containing wire or gold-copper alloy wire. An underfill layer 64 is covered the chip56, the metal wires 62 and the metal pads 58.

[00101] Multiple discrete passive components 66 set up on the third dielectric layer 40, such as a discrete inductor, a discrete capacitor or a discrete resistor, wherein the discrete passive component 66 comprises a multiple metal pad 68. The discrete passive components 66 mounted on the third dielectric layer 40 through a solder layer 70.

[00102] Next, referring to Fig. 9u, multiple metal bumps 72 are formed on the bottom surface of the substrate 20.

[00103] Fig. 9v is disclosed some structures of metal bump 72.

- Lift side: 1st type of structures of metal bump 72 comprises an adhesion/barrier metal layer 61 formed on the metal pad 48, a metal seed layer 63 formed on the adhesion/barrier metal layer 61, an electroplated metal layer 65 formed on the metal seed layer 63 and a solder layer 67 formed on the electroplated metal layer 65, wherein the adhesion/barrier metal layer 61 comprises a titanium-containing layer, a chromium-containing layer, a tantalum-containing layer or a nickel layer, wherein the first electroplated metal layer 65 comprises a copper layer, a gold layer, a nickel layer, wherein the solder layer 67 can be formed by screen plating, ball mounting, or an electroplating process, such as gold-tin alloy, tin-silver alloy, tin-silver-copper alloy, indium, tin-bismuth alloy, or other lead-free alloy. Lead alloy solders can also be used but may be less desirable in some embodiments due to toxicity considerations. The adhesion/barrier metal layer 61 has a thickness between 0.05 and 2

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micrometers. The metal seed layer 63 has a thickness between 0.05 and 2 micrometers. The first electroplated metal layer 65 has a thickness between 1 and 5 micrometers, between 2 and 8 micrometers or between 5 and 20 micrometers. The solder layer 67 has a thickness between 30 and 80 micrometers, between 50 and 100 micrometers, between 80 and 150 micrometers or between 120 and 350 micrometers.

- Right side: 2nd type of structure of metal bump 72 comprises an adhesion/barrier metal layer 61 formed on the metal pad 48, a metal seed layer 63 formed on the adhesion/barrier metal layer 61, a first electroplated metal layer 65 formed on the metal seed layer 63 and a second electroplated metal layer 69 formed on the first electroplated metal layer 65, wherein the adhesion/barrier metal layer 61 comprises a titanium-containing layer, a chromium-containing layer, a tantalum-containing layer or a nickel layer, wherein the first electroplated metal layer 65 comprises a copper layer, a gold layer, a nickel layer, wherein the second electroplated metal layer 69 comprises a copper layer, a gold layer, a nickel layer. The adhesion/barrier metal layer 61 has a thickness between 0.05 and 2 micrometers. The metal seed layer 63 has a thickness between 0.05 and 2 micrometers. The first electroplated metal layer 65 has a thickness between 1 and 5 micrometers, between 2 and 4 micrometers, between 5 and 15 micrometers or between 10 and 25 micrometers. The second electroplated metal layer 69 has a thickness between 1 and 5 micrometers, between 2 and 4 micrometers, between 10 and 30 micrometers or between 20 and 60 micrometers.

[00104] Furthermore, referring to Fig. 9w, the chips 46 may be set up on the bottom surface of the first substrate 20.

[00105] Furthermore, referring to Fig. 9x, the chip 46 may be replaced a 3D IC chip package, wherein the chip 46 comprises a multiple metal pad 48 formed on the top and bottom surface. The

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metal pads 48 of the top surface of the chip 46 are connected to the metal pads 48 of the bottom surface of the chip 46 through multiple through-silicon-via metal layers. A chip 47 is connected to the 3D IC chip 46 through the flip-chip package process, wherein the chip 47 comprises multiple metal pads 49, wherein the metal pad 49 may be an electroplated copper pad, a damascene copper pad or an aluminum pad. The metal pads 49 are connected to the metal pads 48 through a solder layer 51.

[00106] Fig. 9y, illustrates a top view of the first substrate 20. Fig. 9u-Fig. 9w illustrate a cross-section view of Line L-L' in Fig. 9y. Multiple the chips 46, the chips 56 and the passive components 66 may also be provided in or on the first substrate 20.

[00107] Next, cutting the first substrate 20 to produce multiple second substrates 22.

[00108] Fig. 10a-Fig. 10j illustrate a damascene process to form the first metal layer 26, the second metal layer 28, the third metal layer 34 and the fourth metal layer 36 on a top surface and a bottom surface of the first substrate 20.

[00109] Referring to Fig. 10a, the dielectric layers 24 in Fig. 9a include two dielectric layers 80 and 82. The dielectric layer 80 is formed on the dielectric layer 82 by a chemical vapor deposition (CVD) process or a spin-on coating process, wherein each of the dielectric layers 80 and 82 may be composed of a low-K oxide layer with a thickness of between 0.3 and 5μm, and preferably of between 0.5 and 3μm, and an oxynitride layer on the low-K oxide layer, of a low-K polymer layer with a thickness of between 0.3 and 5μm, and preferably of between 0.5 and 3μm, and an oxynitride layer on the low-K polymer layer, of a low-K oxide layer with a thickness of between 0.3 and 5μm, and preferably of between 0.5 and 3μm, and a nitride layer on the low-K oxide layer, of a low-K polymer layer with a thickness of between 0.3 and 5μm, and preferably of between 0.5 and 3μm, and a nitride layer on the low-K polymer layer, or of a low-K dielectric layer with a

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thickness of between 0.3 and 5μm, and preferably of between 0.5 and 3μm, and a nitride-containing layer on the low-K dielectric layer. Next, referring to Fig. 10b, a photoresist layer 84 is formed on the dielectric layer 82, an opening 84a in the photoresist layer 84 exposing the dielectric layer 82. Next, referring to Fig. 10c, the dielectric layer 82 under the opening 84a is removed by a dry etching method to form a trench in the dielectric layer 82 exposing the dielectric layer 80. Next, referring to Fig. 10d, after forming the trench in the dielectric layer 82, the photoresist layer 84 is removed. Next, referring to Fig. 10e, a photoresist layer 86 is formed on the dielectric layer 82 and on the dielectric layer 80 exposed by the trench, an opening 86a in the photoresist layer 86 exposing the dielectric layer 80 exposed by the trench. Next, referring to Fig. 19f, the dielectric layer 80 under the opening 86a is removed by a dry etching method to form a via 80a in the dielectric layer 80 exposing the metal plugs 21 in the substrate 20. Next, referring to Fig. 10g, after forming the via 80a in the dielectric layer 80, the photoresist layer 86 is removed. Thereby, an opening 88 including the trench and the via 80a is formed in the dielectric layers 82 and 80. Next, referring to Fig. 10h, an adhesion/barrier layer 90 having a thickness of between 0.1 and 3 micrometers is formed on the metal plugs 21 exposed by the opening 88, on the sidewalls of the opening 88 and on the top surface of the dielectric layer 82. The adhesion/barrier layer 90 can be formed by a sputtering process or a chemical vapor deposition (CVD) process. The material of the adhesion/barrier layer 90 may include titanium, titanium nitride, a titanium-tungsten alloy, tantalum, tantalum nitride, or a composite of the abovementioned materials. For example, the adhesion/barrier layer 90 may be formed by sputtering a tantalum layer on the metallization structure exposed by the opening 88, on the sidewalls of the opening 88 and on the top surface of the dielectric layer 82. Alternatively, the adhesion/barrier layer 90 may be formed by sputtering a tantalum-nitride layer on the metallization structure exposed by the opening 88, on the sidewalls of the opening 88 and on the top surface of the dielectric layer 82. Alternatively, the adhesion/barrier layer 90 may be formed by forming a tantalum-nitride layer on the metallization structure exposed by the opening 88, on the sidewalls of

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the opening 88 and on the top surface of the dielectric layer 82 by a chemical vapor deposition (CVD) process. Next, referring to Fig. 10i, a seed layer 92, made of copper, having a thickness of between 0.1 and 3 micrometers is formed on the adhesion/barrier layer 90 using a sputtering process or a chemical vapor deposition (CVD) process, and then a copper layer 94 having a thickness of between 0.5 and 5μm, and preferably of between 1 and 2μm, is electroplated on the seed layer 92. Next, referring to Fig. 10j, the copper layer 94, the seed layer 92 and the adhesion/barrier layer 90 outside the opening 88 in the dielectric layers 82 and 80 are removed using a chemical mechanical polishing (CMP) process until the top surface of the dielectric layer 82 is exposed to an ambient.

[00110] Fig. 11a-Fig. 11i illustrate an embossing process to form the first metal layer 26, the second metal layer 28, the third metal layer 34 and the fourth metal layer 36 on a top surface and a bottom surface of the first substrate 20.

[00111] Referring to Fig. 11a, the metal plugs 21 are in the glass layer 16 of the first substrate 20, and the opening 96a in the dielectric layer 96 exposes the metal plugs 21.

[00112] Referring to Fig. 11a, a polymer layer 98 can be formed on the dielectric layer 96, and at least one opening 98a is formed in the polymer layer 98 by patterning the polymer layer 98 to expose at least one metal trace 6, as shown in Fig. 11b and Fig. 11c. The metal plugs 21 may include a center portion exposed by an opening 98a and a peripheral portion covered with the polymer layer 98, as shown in Fig. 11b. Alternatively, the opening 98a may expose the entire upper surface of the metal plugs 21 exposed by the opening 96a in the dielectric layer 96 and further may expose the upper surface of the dielectric layer 96 near the metal trace 6, as shown in Fig. 11c.

[00113] The material of the polymer layer 98 may include benzocyclobutane (BCB), polyimide (PI), polyurethane, epoxy resin, a parylene-based polymer, a solder-mask material, an

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elastomer, or a porous dielectric material. The polymer layer 98 has a thickness of between 3 and 25μm or between 5 and 50 micrometers.

[00114] The polymer layer 98 can be formed by a spin-on coating process, a lamination process or a screen-printing process. Below, the process of forming a patterned polymer layer 98 is exemplified with the case of spin-on coating a polyimide layer on the dielectric layer 96 and then patterning the polyimide layer.

[00115] Referring to Fig. 11d, an adhesion/barrier layer 100 having a thickness of between 0.1 and 3 micrometers, and preferably between 0.5 and 2 micrometers, is formed on the polymer layer 98 and on the metal plugs 21. The adhesion/barrier layer 100 may be a titanium-tungsten-alloy layer, tantalum-containing layer, a chromium-containing layer or a titanium-nitride layer. The adhesion/barrier layer 100 may be formed by a sputtering method, an evaporation method, or a chemical vapor deposition (CVD) method.

[00116] Referring to Fig. 11e, a photoresist layer 102 can be formed on the adhesion/barrier layer 100 by a spin coating process or a lamination process. Referring to Fig. 11f, the photoresist layer 102 is patterned with the processes of exposure, development, etc., to form a photoresist opening 102a on the above-mentioned adhesion/barrier layer 100 over the metal plugs 21 exposed by the opening 98a.

[00117] Referring to Fig. 11g, an electroplated metal layer 104 is formed on the adhesion/barrier layer 100 in the opening 102a, wherein the electroplated metal layer 104 comprises a copper layer, gold layer, a nickel layer, has a thickness between 2 and 10 micrometers, between 5 and 20 micrometers or between 5 and 35 micrometers.

[00118] Referring to Fig. 11h, removing the photoresist layer 102.

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[00119] Referring to Fig. 11i, the above-mentioned adhesion/barrier layer 100 not under the electroplated metal layer 104 is removed with a dry etching method or a wet etching method. For example, the adhesion/barrier layer 100 made of titanium, titanium-tungsten alloy, titanium nitride, tantalum or tantalum nitride, not under the electroplated metal layer 104 is removed with a reactive ion etching (RIE) process.

[00120] First Application: Please referring to Fig. 12, the second substrates 22 is connected to a OLED display substrate through COG bonding process, wherein the OLED display substrate comprises a first glass substrate 106, a second glass substrate 108, an organic light-emitting diodes layer 110 (or a polymer light-emitting diodes layer, PLED layer) between the first glass substrate 106 and the second glass substrate 108 and multiple transparent electrodes 114. The metal bumps 72 are connected to the transparent electrodes 114 through an anisotropic conductive film (ACF) layer 116, wherein the ACF layer 116 comprises multiple conductive particles 117, such as nickel (Ni) particles, gold (Au) particles, nickel-gold alloy particles, silver-tin alloy particles, silver particles, gold plated particles, silver plated particles or nickel plated particles. The OLED display substrate comprises multiple OLED display panels. The OLED display substrate may comprise a touch screen function. A least distance 106a between a centerline of the metal bump 72 and a boundary of the glass substrate 106 is between 3 micrometers and 10 micrometers, 5 micrometers and 15 micrometers, 10 micrometers and 25 micrometers or 20 micrometers and 40 micrometers.

[00121] Next, cutting the second substrates 22 and the OLED display substrate to produce multiple package units.

[00122] Second Application: Furthermore, the OLED display substrate can be replaced with a Micro Electro Mechanical Systems (MEMS) display substrate. Please referring to Fig. 13, the second substrates 22 is connected to a MEMS display substrate through COG bonding process,

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wherein the MEMS display substrate comprises a first glass substrate 106, a MEMS layer 109 and multiple transparent electrodes 114 formed on the first glass substrate 106. The metal bumps 72 are connected to the transparent electrodes 114 through an anisotropic conductive film (ACF) layer 116, wherein the ACF layer 116 comprises multiple conductive particles 117, such as nickel (Ni) particles, gold (Au) particles, nickel-gold alloy particles, silver-tin alloy particles, silver particles, gold plated particles, silver plated particles or nickel plated particles. The MEMS display substrate comprises multiple MEMS display panels. The MEMS display substrate may comprise touch screen function. A least distance 106a between a centerline of the metal bump 72 and a boundary of the glass substrate 106 is between 3 micrometers and 10 micrometers, 5 micrometers and 15 micrometers, 10 micrometers and 25 micrometers or 20 micrometers and 40 micrometers.

[00123] Next, cutting the second substrates 22 and the MEMS display substrate to produce multiple package units.

[00124] Third application: Please refer to Fig. 14, multiple LED devices 122 are packaged on the bottom surface of the second substrates 22. The second substrates 22 is connected to a LCD display substrate through COG bonding process, wherein the LCD display substrate comprises a first glass substrate 106, a second glass substrate 108, and a transistor liquid crystal display layer 111 between the first glass substrate 106 and the second glass substrate 108 and multiple transparent electrodes 114. The metal bumps 72 are connected to the electrodes 114 through an anisotropic conductive film (ACF) layer 116, wherein the ACF layer 116 comprises multiple conductive particles 117, such as nickel (Ni) particles, gold (Au) particles, nickel-gold alloy particles, silver-tin alloy particles, silver particles, gold plated particles, silver plated particles or nickel plated particles. The LCD display substrate comprises multiple LCD display panels. The LCD display substrate may comprises a touch screen function, wherein the LCD display substrate comprises an in-cell TFT LCD substrate. There are multiple optical layers 128 between the second substrates 22 and LCD

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display substrate, such as a diffuser sheet layer, a prism sheet layer, a diffuser layer (or diffuser plate) and a reflector layer. A least distance 106a between a centerline of the metal bump 72 and a boundary of the glass substrate 106 is between 3 micrometers and 10 micrometers, 5 micrometers and 15 micrometers, 10 micrometers and 25 micrometers or 20 micrometers and 40 micrometers.

[00125] Next, cutting the second substrates 22 and the LCD display substrate to produce multiple package units.

[00126] Fourth application: Referring to Fig. 15, this structure of the fourth application is similar to the structure of the third application in Fig. 14. The second substrates 22 is connected to a LCD display substrate through flip-chip bonding process, wherein the LCD display substrate comprises a first glass substrate 106 and a second glass substrate 108, and a transistor liquid crystal display layer 111 and thin film transistor circuit layers (not shown) between the first glass substrate 106 and the second glass substrate 108, wherein multiple transparent electrodes 114 on the bottom surface of the first glass substrate 106 and multiple metal plugs 113 in the first glass substrate 106, wherein the multiple metal plugs 113 are connected to the transparent electrodes 114 respectively. The structure of the first glass substrate 106 can refer to the second substrates 22 in the invention. The metal bumps 72 are connected to the transparent electrodes 114 through a solder layer 107, wherein the solder layer 107 comprises gold-tin alloy, tin-silver alloy, tin-silver-copper alloy, indium, tin-bismuth alloy, or other lead-free alloy. The LCD display substrate comprises multiple LCD display panels. The LCD display substrate may comprise touch screen function, wherein the LCD display substrate comprising an in-cell TFT LCD substrate. There are multiple optical layers 128 between the second substrates 22 and LCD display substrate, such as a diffuser sheet layer, a prism sheet layer, a diffuser layer (or diffuser plate) and a reflector layer. A least distance 106a between a centerline of the metal bump 72 and a boundary of the glass substrate 106 is between 30

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micrometers and 100 micrometers, 50 micrometers and 150 micrometers, 100 micrometers and 250 micrometers or 50 micrometers and 300 micrometers.

[00127] Fifth application: Referring to Fig. 16, this structure of the fifth application is similar to the structure of the fourth application in Fig. 14. The organic light-emitting diodes layer 110 (or a polymer light-emitting diodes layer, PLED layer) is replaced with the liquid crystal display layer 111. The second substrates 22 is connected to a OLED display substrate through flip-chip bonding process, wherein the OLED display substrate comprises a first glass substrate 106 and a second glass substrate 108, and an organic light-emitting diodes layer 110 (or a polymer light-emitting diodes layer, PLED layer) and thin film transistor circuit layers (not shown) between the first glass substrate 106 and the second glass substrate 108, wherein multiple transparent electrodes 114 on the bottom surface of the first glass substrate 106 and multiple metal plugs 113 in the first glass substrate 106, wherein the multiple metal plugs 113 are connected to the transparent electrodes 114 respectively. The structure of the first glass substrate 106 can refer to the second substrates 22 in the invention. The metal bumps 72 are connected to the transparent electrodes 114 through a solder layer 107, wherein the solder layer 107 comprises gold-tin alloy, tin-silver alloy, tin-silver-copper alloy, indium, tin-bismuth alloy, or other lead-free alloy. The OLED display substrate comprises multiple OLED display panels. The OLED display substrate may comprise touch screen function, wherein the OLED display substrate comprising an in-cell TFT OLED substrate. A least distance 106a between a centerline of the metal bump 72 and a boundary of the glass substrate 106 is between 30 micrometers and 100 micrometers, 50 micrometers and 150 micrometers, 100 micrometers and 250 micrometers or 50 micrometers and 300 micrometers.

[00128] Sixth application: Referring to Fig. 17a, the second substrates 22 can be a port of an OLED display substrate. The OLED display substrate comprises the second substrates 22 and the second glass substrate 108, and an organic light-emitting diodes layer 110 (or a polymer light-

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emitting diodes layer, PLED layer), thin film transistor circuit layers (not shown) and transparent electrodes 114 between the second substrates 22 and the second glass substrate 108, wherein the metal plugs 21 connected to transparent electrodes 114 through the first metal layer 26. The OLED display substrate comprises multiple OLED display panels. The OLED display substrate may comprise touch screen function, wherein the OLED display substrate comprising an in-cell TFT OLED substrate.

[00129] Referring to Fig. 17b, the structure of the OLED display substrate comprises multiple thin film transistors circuits 700 and multiple organic light-emitting components 800 between the second substrates 22 and the second glass substrate 108, wherein the thin film transistors circuit 700 comprises a buffer layer 702, a first gate electrode 704a and a first source electrode 704b formed on the buffer layer 702, a first insulating layer 706 formed on the first gate electrode 704a, the first source electrode 704b and the buffer layer 702. An oxide semiconductor layer 710 is formed on the first insulating layer 706 over the first gate electrode 704a and the first source electrode 704b, wherein the oxide semiconductor layer 710 is connected to the first source electrode 704b through the opening in the first insulating layer 706. A second insulating layer 712 is formed on the oxide semiconductor layer 710. A second gate electrode 714a and a second source electrode 714b formed on the second insulating layer 712, wherein the second source electrode 714b connected to the oxide semiconductor layer 710 through an opening in the second insulating layer 712. A protection layer 716 is formed on the second gate electrode 714a, the second source electrode 714b and the second insulating layer 712. The organic light-emitting component 800 formed on the protection layer 716 and connected to the second source electrode 714b through an opening in the protection layer 716.

[00130] The oxide semiconductor layer 710 comprises a ZnO containing layer, wherein the ZnO containing layer can be doped with a group selected from the group constituted of at least one ionic: Gallium (Ga), indium (In), tin (Sn), zirconium (Zr), hafnium (Hf), cadmium (Cd), magnesium

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(Mg), vanadium (V). The first gate electrode 704a, the first source electrode 704b, the second gate electrode 714a and the second source electrode 714b are formed of a metal selected from the following groups: tungsten (W), titanium (Ti), molybdenum (Mo), silver (Ag), tantalum (Ta), aluminum (Al), copper (Cu), gold (Au), chromium (Cr) or niobium (Nb).

[00131] The organic light-emitting component 800 comprises an anode layer 802, a cathode layer 804 and an organic light-emitting layer 806 between the anode layer 802 and the cathode layer 804, wherein the anode layer 802 formed on the protection layer 716 and connected to the second source electrode 714b. A third insulating layer 808 formed on the protection layer 716 and the anode layer 802, then formed a hole/opening in the third insulating layer 808 and on the anode layer 802. Forming the organic light-emitting layer 806 in the opening and on the third insulating layer 808, then formed the cathode layer 804 on the third insulating layer 808 and on the organic light-emitting layer 806. The anode layer 802 is connected to the metal plugs 21 via a conductive layer formed on the opening through the buffer layer 702, a first insulating layer 706 and second insulating layer 712. The cathode layer 804 is connected to the metal plugs 21 via a conductive layer formed on the opening through the buffer layer 702, the first insulating layer 706, the second insulating layer 712 and the third insulating layer 808. The buffer layer 702、the first insulating layer 706, the second insulating layer 712 and the third insulating layer 808 comprise a polyimide, polyamide, acryl resin, benzocyclobutene, phenol resin, oxide layer (buffer layer 702), nitride layer (buffer layer 702).

[00132] The anode layer 802 may contain one or more transparent materials such as indium tin oxide (ITO), indium zinc oxide (IZO), zinc oxide (ZnO), indium gallium oxide (IGO), aluminum zinc oxide (AZO) and In2O3, or non-transparent materials such as Ag, Mg, Al, Pt, Pd, Au, Ni, Nd, Ir, Cr, Li, Ca, Mo, Ti, W, MoW, and Al/Cu. The cathode layer 804 may contain one or more transparent materials such as indium tin oxide (ITO), indium zinc oxide (IZO), zinc oxide (ZnO), indium gallium oxide (IGO), aluminum zinc oxide (AZO) and In_2O_3.

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[00133] The organic light-emitting layer 806 may include a hole transport layer (HTL) and a hole injection layer (HIL) stacked toward the pixel electrode (anode layer 802 or cathode layer 804), and an electron transport layer (ETL) and an electron injection layer (EIL) stacked toward the pixel electrode (anode layer 802 or cathode layer 804). Furthermore, various other layers may be stacked if required. Further, the light-emitting layer 806 comprises a carbazole biphenyl(CBP), (III)(bis(1-phenylisoquinoline)(acetylacetonate)iridium, PIQIr(acac)),(III)(bis(1-phenylquinoline)(acetylacetonate)iridium, PQIr(acac)), (III)(tris(1-phenylquinoline)iridium (PQIr), octaethylporphyrin platinum,PtOEP 、 (III))(tris(dibenzoylmethane)(o-phenanthroline)europium(III),PED ： Eu(DBM)3(Phen)),perylene, N,N'-Di(naphthalene-1-yl)-N,N'-diphenyl-benzidine, tris-8-hydroxyquinoline aluminum (PEDOT), copper phthalocyanine,CuPc, 4,4',4"-tris(N-(3-methylphenyl)-N-phenylamino)triphenylamine (MTDATA).

[00134] Referring to Fig. 18 and Fig. 19, an outward of display substrate produced from above first application to sixth application is an unframed display 119, wherein the unframed display 119 comprises a display area 119a has four edges 119b, wherein a gap between each edge 119b and one of four boundaries of the unframed display 119 has a least distance smaller than 15 micrometers, 20 micrometers, 30 micrometers, 50 micrometers, 100 micrometers, 150 micrometers or 200 micrometers. The unframed display 119 is installed in a shell 123 of a display device 125. Some components (not showed in drawings) can install in the display device 125 (or installed on the second substrates 22), for example, a speaker component, a battery component, a microphone component, a signal receiver component, a wireless signal receiver component, a wireless signal transmitter module.

[00135] Referring to Fig. 19, the display device 125 comprises multiple connecting ports 127 on the shell 123, wherein the connecting ports 127 comprise a signal connecting port, a power

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connecting port, and/or a ground connecting port. The display device 125 can connect to another one display device 125b to become a bigger display device 129, wherein the connecting ports 127 of the display device 125 are connected to the connecting ports 127 of the display device 125b. Multiple display devices 125 can be combined with a big display device, an advertising billboard. The display devices 125 can be used as a tile on the wall of the building. The display devices 125 can be a display unit on a surface of a magic cube.

[00136] The structure of the OLED display substrate disclosed in the Fig. 12 and Fig. 16 can be referred to the paragraph [00125] to the paragraph [00131].

[00137] Those described above are the embodiments to exemplify the present disclosure to enable the person skilled in the art to understand, make and use embodiments of the present disclosure. This description, however, is not intended to limit the scope of the present disclosure. Any equivalent modification and variation according to the spirit of the present disclosure is to be also included within the scope of the claims stated below.

[00138] The components, steps, features, benefits and advantages that have been discussed are merely illustrative. None of them, nor the discussions relating to them, are intended to limit the scope of protection in any way. Numerous other embodiments are also contemplated. These include embodiments that have fewer, additional, and/or different components, steps, features, benefits and advantages. These also include embodiments in which the components and/or steps are arranged and/or ordered differently.

[00139] In reading the present disclosure, one skilled in the art will appreciate that embodiments of the present disclosure can be implemented in hardware, software, firmware, or any combinations of such, and over one or more networks. Suitable software can include computer-readable or machine-readable instructions for performing methods and techniques (and portions

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thereof) of designing and/or controlling the fabrication and design of integrated circuit chips according to the present disclosure. Any suitable software language (machine-dependent or machine-independent) may be utilized. Moreover, embodiments of the present disclosure can be included in or carried by various signals, e.g., as transmitted over a wireless radio frequency (RF) or infrared (IR) communications link or downloaded from the Internet.

[00140] Unless otherwise stated, all measurements, values, ratings, positions, magnitudes, sizes, and other specifications that are set forth in this specification, including in the claims that follow, are approximate, not exact. They are intended to have a reasonable range that is consistent with the functions to which they relate and with what is customary in the art to which they pertain. The scope of protection is limited solely by the claims. That scope is intended and should be interpreted to be as broad as is consistent with the ordinary meaning of the language that is used in the claims when interpreted in light of this specification and the prosecution history that follows and to encompass all structural and functional equivalents.

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Electronic Patent Application Fee Transmittal	
Application Number:	16752650
Filing Date:	26-Jan-2020
Title of Invention:	METHOD FOR FABRICATING GLASS SUBSTRATE PACKAGE
First Named Inventor/Applicant Name:	Ping-Jung Yang
Filer:	Ping-Jung. Yang
Attorney Docket Number:	Mars16-001-US-C01
Filed as Small Entity	
Filing Fees for Utility under 35 USC 111(a)	

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
CLAIMS IN EXCESS OF 20	2202	6	50	300
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**300**

Electronic Acknowledgement Receipt	
EFS ID:	41040452
Application Number:	16752650
International Application Number:	
Confirmation Number:	4809
Title of Invention:	METHOD FOR FABRICATING GLASS SUBSTRATE PACKAGE
First Named Inventor/Applicant Name:	Ping-Jung Yang
Customer Number:	102851
Filer:	Ping-Jung. Yang
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Attorney Docket Number:	Mars16-001-US-C01
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		Mars16-001-US-C01-RP-11052020.pdf	2073892 05a936296786ee2f18718c6ffc9562c4c7ee00e3	yes	37
	Multipart Description/PDF files in .zip description				
	Document Description		**Start**	**End**	
	Applicant Arguments/Remarks Made in an Amendment		22	37	
	Claims		12	21	
	Specification		2	11	
	Amendment/Req. Reconsideration-After Non-Final Reject		1	1	
Warnings:					
Information:					
2	Specification	Mars16-001-US-C01-SPEC-Markedversion-11012020.pdf	297856 b72989b60c7471b2b48fb7744fcbb9cc8b4a1cff	no	41
Warnings:					
Information:					
3	Specification	Mars16-001-US-C01-SPEC-cleanversion-11012020.pdf	292027 e9ac24754eda1c49c9597a868605bc1501e6daa7	no	40
Warnings:					
Information:					
4	Fee Worksheet (SB06)	fee-info.pdf	30009 2656a82771953905002e490db4e6c4fa838e2630	no	2
Warnings:					
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		Total Files Size (in bytes):	2693784		

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If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

REMARKS/ARGUMENTS

The Examiner is thanked for the thorough examination of the present application and non-final Office action issued on September 21, 2020. Claims 1-20 are cancelled. Claims 21-46 are pending in the application, of which claims 21 and 31 are the pending independent claims and claims 41-46 are newly added. No new matter is believed to be added into the application by this paper. Applicants respectfully request reconsideration of the present application and claims for at least the following reasons.

Claim Amendments

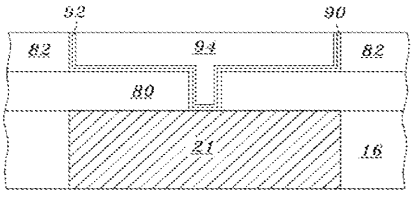
Patent Priority:

This patent application is a continuation of application No. 15261956, filed Sept. 11, 2016, now pending, which claims priority benefits from U.S. provisional patent application No. 62/219249, filed Sept. 16, 2015. This patent application of application No. 15261956 is a continuation-in-part of application No. 14/036256, filed Sept. 25, 2013, now patent No. 9615453, **which claims the benefit of priority from U.S. provisional patent application No. 61/705,649**, filed Sept. 26, 2012, all of which is incorporated herein by reference in their entirety

All elements/conditions of the Claims 21-47 are from U.S. provisional patent application No. 61/705,649, filed Sept. 26, 2012 and disclosed in the Non-Provisional patent application of application No. 14/036256, filed Sept. 25, 2013.

1. For claims 21 and 31 the subject matter that "first metal interconnect comprises a first metal layer, a first copper layer on said first metal layer, and a second copper layer on said first copper layer", is disclosed and supported in Figs. 19h-19j and paragraphs [0049]-[0050] in the specification of the provisional App. No. 61/705,649 filed on Sept. 26, 2012, (and disclosed and supported in Figs. 10h-10j and paragraphs [0108]-[0109] in the specification of the provisional App. No. 14/036256, filed on Sept. 25, 2013)as below:

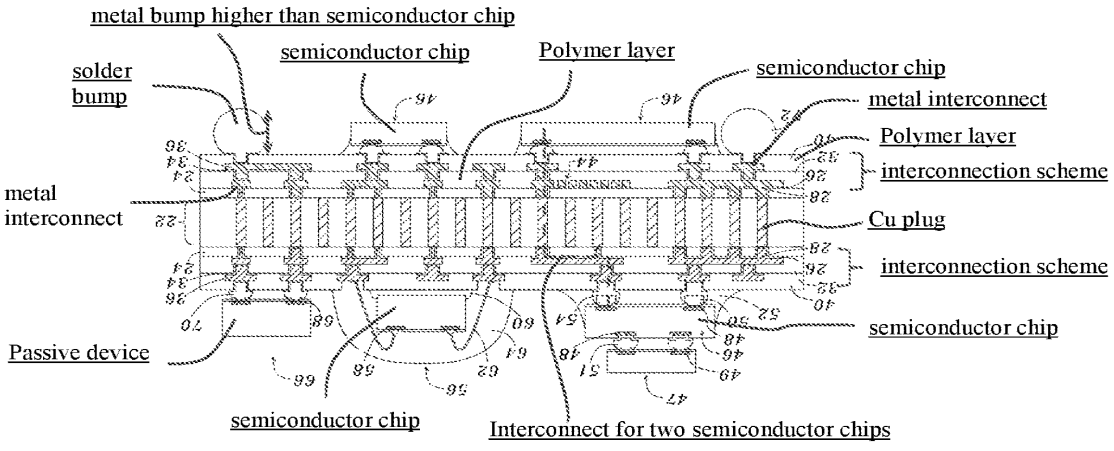
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[0049] Fig. 19a-Fig. 19j illustrates a damascene process to form the first metal layer 26, the second metal layer 28…
[0050]…Fig. 19h, an **adhesion/barrier layer 90** having a thickness of between 0.1 and 3 micrometers is formed on the metal trace 6 exposed by the opening 88…
…Next, referring to Fig. 10i, Fig. 19i, a **seed layer 92, made of copper**, having a thickness of between 0.1 and 3 micrometers is formed on the adhesion/barrier layer 90…
…a **copper layer 94** having a thickness of between 0.5 and 5μm, and preferably of between 1 and 2μm, is electroplated on the seed layer 92. …

2. For claims 21 and 31 the subject matter that "first metal bump over said first interconnection scheme and connected to said second copper plug through said second metal interconnect, wherein said first metal bump comprises a tin-containing layer", is disclosed and supported in Fig.18v-Fig.18x and paragraph [0044] in the specification of the provisional App. No. 61/705,649 filed on Sept. 26, 2012, (and disclosed and supported in Fig.9v-Fig.9x and paragraph [0103] in the specification of the provisional App. No. 14/036256, filed on Sept. 25, 2013) as below:

[0044] …. referring to Fig. 18v, …The **bumps 72** comprises an adhesion/barrier metal layer formed on the metal pad 48, an electroplated metal layer or an electro-less metal layer formed on the adhesion/barrier metal layer,….. the electroplated metal layer comprises a copper layer, a gold layer, a nickel layer, a **tin-containing layer**



3. For claims 21, 23, 24, 25, 26, 31 and 43-44 the subject matter that "a first semiconductor chip", "second semiconductor chip" and "third semiconductor chip" and "semiconductor chip comprises a central-processing-unit (CPU) circuit block and a graphics-processing-unit (GPU) circuit block", is disclosed and supported in Fig.18v-Fig.18x and paragraph [0040] in the specification of the provisional App. No. 61/705,649 filed on Sept. 26, 2012, (and disclosed and supported in Fig.9v-Fig.9x and paragraph [0097] in the specification of the provisional App. No. 14/036256, filed on Sept. 25, 2013) as below:

[0040] .... wherein the chip 46 and 56 comprises may be a memory chip....or **a chip including one or more of a CPU circuit block, a GPU circuit block**...and a modem circuit block, **from the semiconductor wafer**.

4. For claims 27 and 31 the subject matter that "third metal interconnect over said first metal interconnect and said second polymer layer, wherein said second polymer is between said first and third metal interconnects" (**claim 27**), "and **a second polymer layer over said first and second metal interconnects**, wherein said first metal interconnect is connected to said first copper plug, wherein said first metal interconnect comprises a first metal layer, a first copper layer on said first metal layer, and a second copper layer on said first copper layer;" (claim 31) are disclosed and supported in Figs. 18h-18n and paragraphs [0028] in the specification of the provisional App. No. 61/705,649 filed on Sept. 26, 2012, as below:

[0028] .... referring to Fig. 18h, a dielectric layer 32 is formed on the first dielectric layer 24 and on the second metal layer 28, wherein the dielectric layer 32 may include or may be a layer of silicon oxide (such as SiO_2),...or **polymer** (such as polyimide, benzocyclobutene (BCB), polybenzoxazole (PBO), poly-phenylene oxide (PPO), epoxy, or silosane)...

5. For claim 28 the subject matter that "further comprising a second interconnection scheme under said first polymer layer and on said second surface.", is disclosed and supported in Fig. 18s and paragraph [0038] in the specification of the provisional App. No. 61/705,649 filed on Sept. 26, 2012, as below:

[0038] .... referring to Fig. 18s, repeat the processes of Fig.18a-Fig.18p to form the dielectric layer 24, the first metal layer 26, the second metal layer 28, the dielectric layer 32, the

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third metal layer 34, the fourth metal layer 36 and the dielectric layer 40 on the bottom surface of the first substrate 20.

6. For claims 21and 31 the subject matter that "a third copper plug extending through said first polymer layer from said first surface to said second surface, wherein said first, second and third copper plugs each has a top surface coplanar with said first surface, wherein a pitch between said first and third plugs is between 50 and 200 micrometers," **(claim 21)** and "wherein said first surface is parallel to said second surface, a first copper plug extending through said first polymer layer from said first surface to said second surface, and a second copper plug extending through said first polymer layer from said first surface to said second surface, and a third copper plug extending through said first polymer layer from said first surface to said second surface, wherein said first, and second and third copper plugs each has a top surface coplanar with said first surface, wherein a pitch between said first and third plugs is between 50 and 200 micrometers,"**(claim 31)**, is disclosed and supported in Fig. 17a and Fig. 7 and paragraphs [007], [0013] and [0017]in the specification of the provisional App. No. 61/705,649 filed on Sept. 26, 2012, as below:

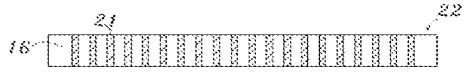


Fig. 17a

[0007] …the **traces 6 are closed up to a pitch t3.** The pitch t3 substantially the same with the diameter (or width) of the traces 2a, 2b, 4a and 4b, such as between 10 and 30 micrometers…**between 50 and 200 micrometers**,
[0013] …**glass layer 16 may be replaced by a polymer layer**. When the polymer cured to a solid state. **The polymer layer has an expansion coefficient between 3 and 6 ppm/°C.**
[0017] …The second substrates 22 are well-regulated an array in the first substrate 20. Each of the second substrates has multiple metal plugs 21, wherein the **metal plug 21 is formed from metal traces 6**. …

7. For claims 23, 31, 32, 34, 36-38 41 and 45-46 the subject matter that:

"a second semiconductor chip over said first interconnection scheme and a third semiconductor chip over said second semiconductor chip" **(claim 23)**,

"a second semiconductor chip under said first interconnection scheme and said first semiconductor chip, wherein said first interconnection scheme is between said first and second semiconductor chips"**(claim 31)**,

"a third semiconductor chip over said first interconnection scheme and next to said first semiconductor chip" (**claim 32**),

"third semiconductor chip over said first interconnection scheme and next to said first semiconductor chip, wherein said third semiconductor chip is connected to said first metal bump through said first metal interconnect."(**claim 34**),

"third semiconductor chip under said second semiconductor chip and multiple fourth metal bumps between said second and third semiconductor chips, wherein said second semiconductor chip comprises a first metal pad on a top surface and a second metal pad on a bottom surface, wherein said first metal pad is connected to said second metal pad through a through-silicon-via metal layer." (**claim 36**),

"passive component connect to said second metal bump through said first interconnection scheme" (**claim 37**)

"second semiconductor chip comprises a fourth metal bump at a third surface of said second semiconductor chip and connect to said first semiconductor chip through said second metal interconnect, wherein said third metal bump is at a fourth surface of said first semiconductor chip, wherein said third surface is faced to said fourth surface."(**claim 38**)

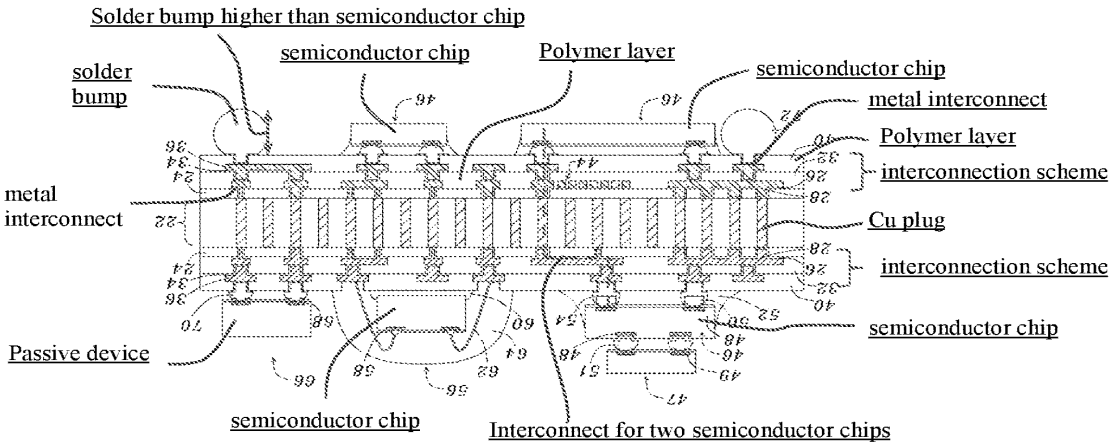
"a second semiconductor chip over said first interconnection scheme and connected to said first metal interconnect through a third metal bump, wherein said second semiconductor chip has a height is between a backside surface of said second semiconductor chip and a top surface of said second polymer layer is smaller than a thickness of said first metal bump" (**claim 41**)

"a height is between a backside surface of said first semiconductor chip and a top surface of said second polymer layer is smaller than a thickness of said first metal bump" (**claim 45**)

"said second semiconductor chip is coupled to said first semiconductor chip through said second metal interconnect" (**claim 46**)

are disclosed and supported in Fig.18v-Fig.18x and paragraph [0040]-[0046] in the specification of the provisional App. No. 61/705,649 filed on Sept. 26, 2012, (and disclosed and

supported in Fig.9v-Fig.9x and paragraphs [0103]-[0105] in the specification of the provisional App. No. 14/036256, filed on Sept. 25, 2013) as below:



8. For claims 33, 26 and 42 the subject matter that "second semiconductor chip comprises a first metal pad on a top surface and a second metal pad on a bottom surface, wherein said first metal pad is connected to said second metal pad through a through-silicon-via metal layer"**(claim 33)** and "first semiconductor chip comprises a first metal pad on a top surface and a second metal pad on a bottom surface, wherein said first metal pad is connected to said second metal pad through a through-silicon-via metal layer"**(claim 26)**, "a second semiconductor chip under said first semiconductor chip, wherein first semiconductor chip comprise a first metal pad connected to a second metal pad of said second semiconductor chip through a solder layer, wherein said solder layer between said first and second semiconductor chips"**(claim 42)** are disclosed and supported in Fig. 18x and paragraph [0046] in the specification of the provisional App. No. 61/705,649 filed on Sept. 26, 2012, as below:

[0046] .... the chip 46 may be a 3D IC chip, wherein the chip 46 comprises a multiple metal pad 48 formed on the top and bottom surface. The metal pads 48 of the top surface of the chip 46 are connected to the metal pads 48 of the bottom surface of the chip 46 through multiple **through-silicon-via metal layers**. **A chip 47 is connected to the 3D IC chip 46 through the flip chip package process,** wherein the chip 47 comprises multiple metal pads 49, wherein the

metal pad 49 may be an electroplated copper pad, a damascene copper pad or an aluminum pad. **The metal pads 49 are connected to the metal pads 48 through a solder layer 51**.

9. For claims 39 the subject matter that "further comprising a third semiconductor chip under said first interconnection scheme and next to said second semiconductor chip, wherein said third **semiconductor chip is a memory chip**", is disclosed and supported in Fig. 18x and paragraph [0040] in the specification of the provisional App. No. 61/705,649 filed on Sept. 26, 2012, as below:

[0040] .... wherein **the chip 46 or 56 comprises may be a memory chip**

10. For claims 21, 30 and 40 the subject matter that "first semiconductor chip comprises a second metal bump, wherein said second metal bump comprises a second metal layer with a thickness between 5 and 30 micrometers"(**claim 21**), "second metal layer comprises a copper layer" (**claim 30**) and "first semiconductor chip comprises a metal bump, wherein said metal bump comprises a second metal layer with a thickness between 5 and 30 micrometers, wherein said second metal layer comprises a copper layer" (**claim 40**), are disclosed and supported in Fig. 18x and paragraph [0041] in the specification of the provisional App. No. 61/705,649 filed on Sept. 26, 2012, (and disclosed and supported in Fig. 9x and paragraph [0098] in the specification of the provisional App. No. 14/036256, filed on Sept. 25, 2013), as below:

[0041] .... **The metal bump 50 comprises** an adhesion/barrier metal layer formed on the metal pad 48, an **electroplated metal layer** or an electro-less metal layer formed on the adhesion/barrier metal layer.... the **electroplated metal layer comprises a copper layer**, a gold layer... The **electroplated metal layer has a thickness** between 2 and 5 micrometers, **between 5 and 30 micrometers** or between...

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Claim Rejections - 35 USC §103

Claims 21, 22, 24, and 27-29 are rejected under 35 U.S.C. 103 as being unpatentable over Gong et al. US 2013/0049217 in view of Lin et al. US 2009/0155959. Claims 25, 26, 30-33, 35, 36, and 39 are rejected under 35 U.S.C. 103 as being unpatentable over Gong et al. US 2013/0049217 in view of Lin et al. US 2009/0155959 and Chen et al. US 2013/0277801. Applicants respectfully traverse these rejections and reconsideration and withdrawal of these rejections are respectfully requested. Please review the comments/arguments below:

I. Claim 21

Amended independent claim 21, recites the following:

21. A chip package comprising:

a first polymer layer has a first surface and a second surface opposed to said first surface, wherein said first surface is parallel to said second surface, a first copper plug extending through said first polymer layer from said first surface to said second surface, and a second copper plug extending through said first polymer layer from said first surface to said second surface, and a third copper plug extending through said first polymer layer from said first surface to said second surface, wherein said first, and second and third copper plugs each has a top surface coplanar with said first surface**, wherein a pitch between said first and third plugs is between 50 and 200 micrometers**, wherein said first polymer layer has a thickness between 100 and 300 micrometers and **has a coefficient of expansion between 3 and 10 ppm/°C**;

a first interconnection scheme over said first surface, wherein said first interconnection scheme comprises a first metal interconnect over said first surface, a second metal interconnect over said first surface and a second polymer layer over said first and second metal interconnects, wherein said first metal interconnect is connected to said first and second copper plugs plug, **wherein said first metal interconnect comprises a first metal layer, and a first copper layer on said first metal layer, and a second copper layer on said first copper layer**;

a first solder metal bump over said first interconnection scheme and connected to said second copper plug through said second metal interconnect, wherein said first metal bump comprises a tin-containing layer; and

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a first semiconductor chip under said first interconnection scheme, wherein said first semiconductor chip comprises a second metal bump, wherein said second metal bump comprises a second metal layer with a thickness between 5 and 30 micrometers.

1. The applied references (Gong et al. US 2013/0049217; Lin et al. US 2009/0155959), either alone or in combination, are not seen to disclose or suggest the foregoing features of each of amended independent Claims 21.

Applicants respectfully submit that Gong and Lin do not disclose or suggest the feature of amended Claim 21 that " **a pitch between said first and third plugs is between 50 and 200 micrometers**", "first metal interconnect comprises a first metal layer, and **a first copper layer on said first metal layer, and a second copper layer on said first copper layer** " and "**first semiconductor chip comprises a second metal bump, wherein said second metal bump comprises a second metal layer with a thickness between 5 and 30 micrometers**". The comments/arguments below:

i. Gong discloses or suggests the feature of "The "active surface" of die 750 is a surface of the die having **bond pads 760 and 765**." (See paragraph [0034], Fig. 11, Gong). However, Gong do not disclose or suggest the feature of "first semiconductor chip comprises a second metal bump, wherein said second metal bump comprises a second metal layer with a thickness between 5 and 30 micrometers"

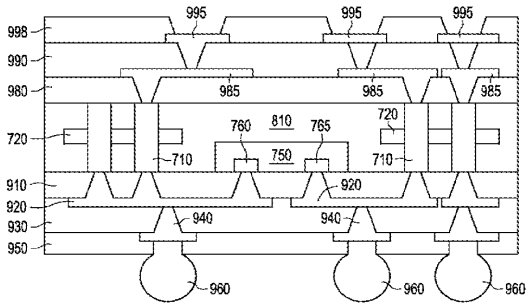


FIG. 11

iii. Lin discloses or suggests the feature of "**Conductive layer 44 is patterned and formed over conductive layer 42**. .... In one embodiment, for example, **conductive layer 42**

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includes titanium (Ti) and conductive layer 44 includes Cu." (See paragraph [0026], Fig. 11, Lin) Therefore, Lin only discloses or suggests "one Cu layer (44) on the metal layer (42)".. However, Lin do not disclose or suggest the feature of "first metal interconnect comprises a first metal layer, and a first copper layer on said first metal layer, and a second copper layer on said first copper layer".

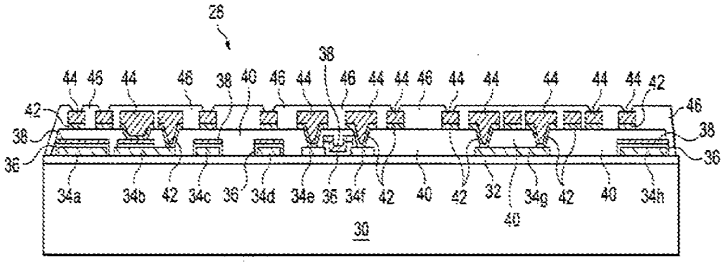


FIG. 2a

2. Furthermore, the Non-Final Office Action asserts that "said first polymer layer has a coefficient of expansion between 3 and 10 ppm/°C (polyimide as 810 with a CTE of in the range of 1-10 ppm/C see teaching reference Tiedtke US 2011/0257716 [43])", however, Tiedtke discloses:

   A. the invention relates to a stimulation electrode array for stimulating nerve cells in a human or animal body and a method of manufacturing same. The electrode array of the present invention is particularly designed for use **in a medical implant device** and, more particularly, in a retinal implant. (See paragraph [0002], Tiedtke)

   B. **(I).** "The electrode array 1 comprises a substrate 2 for supporting a plurality of electrodes 3 and **includes two layers of polymer material, namely a first layer 4,** which is applied to a base or support structure B, and **a second layer 5, which is applied directly to the first layer 4**." (See paragraph [0002], Tiedtke)

   (II). "...Further polyimide materials that have **a CTE within the range of about 20 to 40 ppm/°C for use in the first layer 4** will be known to the skilled person. The

polyimide material of the second layer 5, on the other hand, may consist of PI-2611 which has a CTE of about 3 ppm/°C. (i.e. $3x10^{-6}$/°C). Further polyimide materials that have **a CTE within the range of 1 to 10 ppm/°C for use in the second layer 5**...." (See paragraph [0043], Tiedtke)

(III). "a **contact end 6 of each of the electrodes 3** extends to and/or projects from the outer surface 7 of the second layer 5 in the substrate 2 **for contact with the tissue to be stimulated in the human or animal body**.." (See paragraph [0045], Tiedtke)

(IV). "As with the embodiments **in** FIGS. 1 to 3, the higher CTE of the regions of material 41 of the first layer 4 compared to the CTE of the second layer 5 induces a deformation of the substrate 2 **to produce a curved surface profile in the electrode array 1 for optimising stimulation of the retina tissue by the implant device 10**" (See paragraph [0048], Tiedtke)

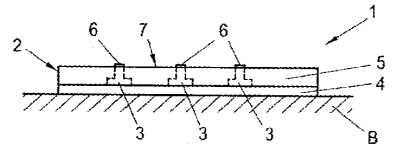


Figure 1

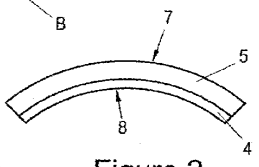


Figure 2

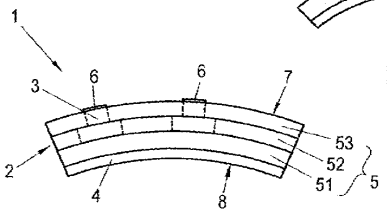


Figure 3

According to the Tiedtke disclosed **(I)-(IV)** points, we can summary below:

a. Tiedtke's invention is in a "**medical**" field, not in "chip package" field, however, no any disclosure, suggest or intention about "chip", "semiconductor", "chip package" in Tiedtke's invention.

b. The application/goal of Tiedtke's invention is "**produce a curved surface profile in the electrode array 1** for optimizing stimulation of the retina tissue by the implant device 10", that means, "**curved surface profile in the electrode array 1"** is final structure, thus Tiedtke do not disclose or suggest the feature of "first, and second and third copper plugs each has a top surface **coplanar with** said first surface (of the polymer layer)".

c. Tiedtke disclose or suggest feature of "**contact end 6** of each of the electrodes 3 extends to and/or projects from the outer surface 7 of the second layer 5 in the substrate 2 **for contact with the tissue to be stimulated in the human or animal body**", that means, the metal interconnect can not be formed on the outer surface 7 of the second layer 5.

Therefore, according to above a, b and c comments for Tiedtke's disclosure. Applicant respectfully submits that, in formulating the rejections of claim 21, the Examiner can not combine Gong, Lin and Tiedtke of references to reject the claim 21, the arguments are list below:

- **The technical field of Tiedtke is different with that of Gong and Lin, and different with that of the invention (claim 21), too**. Tiedtke's invention is in a "medical" field, not in "chip package" field, however, no any disclosure, suggest or intention about "chip", "semiconductor", "chip package" in Tiedtke's invention.

- Accordingly, a combination of Tiedtke and Gong would not result in the feature that " first surface is parallel to said second surface" and "first, and second and third copper plugs each has a top surface coplanar with said first surface", because Tiedtke's goal is that of "**produce a curved surface profile in the electrode array 1** for optimizing stimulation of the retina tissue by the implant device 10" . Furthermore, the "semiconductor chip" bonded on the "**curved surface**" through flip-chip bonding process/metal bump is very difficult or not allowed.

Furthermore, the "Low CTE (between 3 and 10 ppm/°C) polymer layer" used in semiconductor chip package is an innovative application/invention in 2012-2014. Therefore, the applicant cannot understand or accept why the combination of two different technical fields (medical and chip packaging) can be used to reject claim 21.

In view of the above, amended independent Claim 21 is believed to be allowable over the applied references. Reconsideration and withdrawal of the rejections of Claim 21 is therefore respectfully requested.

II. Claims 22-30 and claims 41-44

The claims 22-30 and 41-44 currently under consideration in the application are dependent from their respective independent claim 21 discussed above and therefore are believed to be allowable over the applied references for at least similar reasons. Because each dependent claim is deemed to define an additional aspect of the invention, the individual consideration of each on its own merits is respectfully requested.

III. Claims 31

Amended independent claim 31, recites the following:

31. A chip package comprising:

a first polymer layer has a first surface, a second surface opposed to said first surface, wherein said first surface is parallel to said second surface, a first copper plug extending through said first polymer layer from said first surface to said second surface, a second copper plug extending through said first polymer layer from said first surface to said second surface, and a third copper plug extending through said first polymer layer from said first surface to said second surface, wherein said first, second and third copper plugs each has a top surface coplanar with said first surface, **wherein a pitch between said first and third plugs is between 50 and 200 micrometers**, wherein said first polymer layer has a thickness between 100 and 300 micrometers;

a first interconnection scheme over said first surface, wherein said first interconnection scheme comprises a first metal interconnect over said first surface, a second metal interconnect over said first surface and a second polymer layer over said first and second metal interconnects, wherein said first metal interconnect is connected to said first copper plug, wherein said first metal interconnect comprises a first metal layer, a first copper layer on said first metal layer, and a second copper layer on said first copper layer;

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a first metal bump over said first interconnection scheme, wherein said first metal bump is connected to said first copper plug through a first opening in said second polymer layer and said first metal interconnect, wherein said first metal bump comprises a tin-containing layer;

a second metal bump said first interconnection scheme, wherein said second metal bump is connected to said first interconnection scheme through a second opening in said second polymer layer;

a first semiconductor chip over said first interconnection scheme and between said first and second metal bumps, wherein said first semiconductor chip comprises a third metal bump connected to a second metal interconnect through a third opening in said second polymer layer; and

a second semiconductor chip under said first interconnection scheme and said first semiconductor chip, wherein said first interconnection scheme is between said first and second semiconductor chips, wherein said **second semiconductor chip comprises a central-processing-unit (CPU) circuit block and a graphics-processing-unit (GPU) circuit block**.

1. The applied references (Gong et al. US 2013/0049217; Lin et al. US 2009/0155959 and Chen et al. US 2013/0277801), either alone or in combination, are not seen to disclose or suggest the foregoing features of each of amended independent Claims 31.

Applicants respectfully submit that Gong and Lin do not disclose or suggest the feature of amended Claim 31 that " **a pitch between said first and third plugs is between 50 and 200 micrometers**", "first metal interconnect comprises a first metal layer, and **a first copper layer on said first metal layer, and a second copper layer on said first copper layer** " and " **second semiconductor chip comprises a central-processing-unit (CPU) circuit block and a graphics-processing-unit (GPU) circuit block** ". The comments/arguments below:

i. Lin discloses or suggests the feature of "**Conductive layer 44 is patterned and formed over conductive layer 42**. .... In one embodiment, for example, **conductive layer 42 includes titanium (Ti) and conductive layer 44 includes Cu**.". (See paragraph [0026], Fig. 11, Lin) Therefore, Lin only discloses or suggests "one Cu layer (44) on the metal layer (42)". However, Lin do not disclose or suggest the feature of "first metal interconnect comprises a first metal layer, a first copper layer on said first metal layer, and a second copper layer on said first copper layer".

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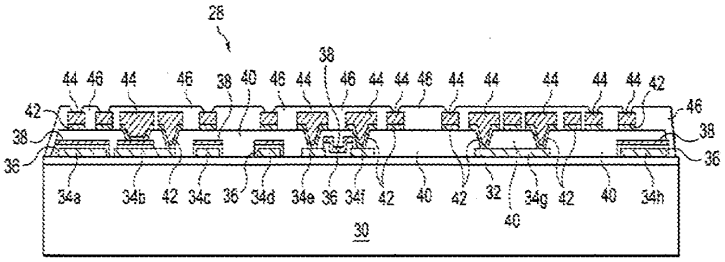


FIG. 2a

ii. The filing date of Chen et al. US 2013/0277801 is March 8, 2013, which claims provisional application No. 61635493, filed on Apr. 19, 2012. However, all elements/conditions of the Claims 31 are from U.S. provisional patent application No. 61/705,649 filed on Sept. 26, 2012. **The effective date of the claim 31 of the patent application is earlier than the filing date of Chen et al. US 2013/0277801.**

iii. Chen discloses or suggests the feature of "the power line (112a) may be electrically connected to a central processing unit **(CPU) or** a graphic processing unit **(GPU)** which may be disposed on or in the lower **chip package 100** and/or the upper **chip package 200**." (See paragraph [0026], Fig. 1, Chen). Therefore, Chen only discloses or suggests "**a CPU or a GPU disposed on or in a chip package**", not "**a CPU circuit block and a GPU circuit block are in one chip**". However, Chen does not disclose or suggest the feature of "second semiconductor chip comprises a central-processing-unit (CPU) circuit block **and** a graphics-processing-unit (GPU) circuit block". The feature of claim 31 is the feature of "**one chip comprises a CPU circuit block and a GPU circuit block**" or "**a CPU circuit block and a GPU circuit block are in one chip**".

Furthermore, the applicant had reviewed the specification of provisional application No. 61635493 (claimed the priority by Chen), Chen does not disclose or suggest the feature of "second semiconductor chip comprises a central-processing-unit (CPU) circuit block **and** a graphics-processing-unit (GPU) circuit block" in the specification of the provisional application No. 61635493, too.

Therefore, according to the comments of **ii** and **iii**, **the reference of "Chen et al. US 2013/0277801" can not be a "Prior reference" to reject the claim 31.**

In view of the above, amended independent Claim 31 is believed to be allowable over the applied references (Gong et al. US 2013/0049217 in view of Lin et al. US 2009/0155959), without reference of Chen et al. US 2013/0277801. Reconsideration and withdrawal of the rejections of Claim 31 is therefore respectfully requested.

IV. Claims 32-40 and claims 45-46

The claims 32-40 and 45-46 currently under consideration in the application are dependent from their respective independent claim 31 discussed above and therefore are believed to be allowable over the applied references for at least similar reasons. Because each dependent claim is deemed to define an additional aspect of the invention, the individual consideration of each on its own merits is respectfully requested.

CONCLUSION

In view of the Amendments and Remarks herein, Applicants submit that the application is in condition for allowance and respectfully request a notice to this effect. Should the Examiner have any questions, please email the question listed below.

Respectfully submitted,

Mars Yang

Date: __2020-11-05_____ Ping-Jung Yang

Email: semars3898@gmail.com

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Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

What is claimed is:

Claims 1-20 Cancelled

21. (Currently amended) A chip package comprising:

a first polymer layer has a first surface and a second surface opposed to said first surface, wherein said first surface is parallel to said second surface, a first copper plug extending through said first polymer layer from said first surface to said second surface, ~~and~~ a second copper plug extending through said first polymer layer from said first surface to said second surface, and a third copper plug extending through said first polymer layer from said first surface to said second surface, wherein said first, ~~and~~ second and third copper plugs ~~has~~ each has a top surface coplanar with said first surface, wherein a pitch between said first and third plugs is between 50 and 200 micrometers, wherein said first polymer layer has a thickness between 100 and 300 micrometers and has a coefficient of expansion between 3 and 10 ppm/°C;

a first interconnection scheme over said first surface, wherein said first interconnection scheme comprises a first metal interconnect over said first surface, a second metal interconnect over said first surface and a second polymer layer over said first and second metal interconnects, wherein said first metal interconnect is connected to said first ~~and second~~ copper ~~plugs~~ plug,

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wherein said first metal interconnect comprises a first metal layer, ~~and~~ a first copper layer on said first metal layer, and a second copper layer on said first copper layer;

a first ~~solder~~ metal bump over said first interconnection scheme and connected to said second copper plug through said second metal interconnect, wherein said first metal bump comprises a tin-containing layer; and

a first semiconductor chip under said first interconnection scheme, wherein said first semiconductor chip comprises a second metal bump, wherein said second metal bump comprises a second metal layer with a thickness between 5 and 30 micrometers.

22. (Currently amended) The chip package of claim 21, further comprising a passive component over said ~~first surface~~interconnection scheme and connected to said first metal interconnect through a solder layer.

23. (Currently amended) The chip package of claim 21, further comprising a second semiconductor chip over said first ~~surface~~ interconnection scheme and a third semiconductor chip over said second semiconductor chip.

24. (Currently amended) The chip package of claim 21, further comprising a second semiconductor chip over said first interconnection scheme, wherein said second semiconductor chip comprises a third metal bump between said second semiconductor chip and said first interconnection scheme.

25. (Currently amended) The chip package of claim 21, wherein said first semiconductor chip comprises a central-processing-unit (CPU) circuit block and a graphics-processing-unit (GPU) circuit block.

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26. (Currently amended) The chip package of claim 21, wherein said first semiconductor chip comprises a first metal pad on a top surface and a second metal pad on a bottom surface, wherein said first metal pad is connected to said second metal pad through a through-silicon-via metal layer. ~~a central processing unit (CPU) circuit block and a DRAM circuit block.~~

27. (Currently amended) The chip package of claim 21, wherein said first interconnection scheme further comprises a third metal interconnect over said first metal interconnect and said second polymer layer, wherein said second polymer is between said first and third metal interconnects, wherein said third metal interconnect comprises a ~~second~~ third metal layer, ~~and~~ a ~~second~~ third copper layer on said ~~second~~ third metal layer, and a fourth copper layer on said third copper layer.

28. (Currently amended) The chip package of claim 21, further comprising a second interconnection scheme under said first polymer layer and on said second surface. ~~wherein said first copper plugs has a top surface coplanar with said first surface.~~

29. (Currently amended) The chip package of claim 21, wherein said first copper plugs has a top surface coplanar with said first surface and a bottom surface coplanar with said second surface.

30. (Currently amended) The chip package of claim 21, wherein said second metal layer comprises a copper layer. ~~further comprising a second solder bump under said second surface and directly under said first copper plugs.~~

31. (Currently amended) A chip package comprising:

~~a first sidewall and a second sidewall opposed to said first sidewall, wherein said first surface is parallel to said second surface, multiple first copper plugs extending through a first portion of said first polymer layer from said first surface to said second surface, wherein said multiple first copper plugs are arranged in a first row substantially parallel to said first and~~

~~second sidewalls, multiple second copper plugs extending through a second portion of said first polymer layer from said first surface to said second surface, wherein said multiple second copper plugs are arranged in a second row substantially parallel to said first and second sidewalls, wherein each of said multiple first and second copper plugs has a top surface coplanar to said first surface and a bottom surface coplanar to said second surface, wherein a first distance between said first row and said second row is greater than a second distance between said first row and said first sidewalls and greater than a third distance between said second row and said second sidewalls,~~ a first polymer layer has a first surface, a second surface opposed to said first surface, wherein said first surface is parallel to said second surface, a first copper plug extending through said first polymer layer from said first surface to said second surface, a second copper plug extending through said first polymer layer from said first surface to said second surface, and a third copper plug extending through said first polymer layer from said first surface to said second surface, wherein said first, second and third copper plugs each has a top surface coplanar with said first surface, wherein a pitch between said first and third plugs is between 50 and 200 micrometers, wherein said first polymer layer has a thickness between 100 and 300 micrometers;

a first interconnection scheme over said first surface, wherein said first interconnection scheme comprises a first metal interconnect over said first surface, ~~and~~ a second metal interconnect over said first surface and a second polymer layer over said first and second metal interconnects, wherein said first metal interconnect is connected to said first copper plug, wherein said first metal interconnect comprises a first metal layer, a first copper layer on said first metal layer, and a second copper layer on said first copper layer; ~~, a second polymer layer between said first surface and said first metal interconnect, a third polymer layer between said first and second metal interconnects and a fourth polymer layer on said second metal~~

~~interconnect, wherein said first metal interconnect comprises a first metal interconnection layer on said first polymer layer, wherein said second metal interconnect comprises a second metal interconnection layer on said second polymer layer, wherein said first metal interconnection layer comprises a first metal layer in a first opening in said second polymer layer and a first copper layer on said first metal layer in said first opening, wherein said second metal interconnection layer comprises a second metal layer on said third polymer layer and in a second opening in said third polymer layer and a second copper layer on said second metal layer in said second opening;~~

a first ~~solder~~ metal bump ~~on~~ over said first interconnection scheme, wherein said first ~~solder~~ metal bump is connected to ~~one of~~ said ~~multiple~~ first copper ~~plugs~~ plug through a ~~third~~ first opening in said ~~fourth~~ second polymer layer and said first metal interconnect, wherein said first metal bump comprises a tin-containing layer; ~~, said second metal interconnection layer, said second opening, said first metal interconnection layer and said first opening;~~

a second ~~solder~~ metal bump ~~on~~ over said first interconnection scheme, wherein said second ~~solder~~ metal bump is connected to ~~a third metal interconnection layer of said second metal interconnect~~ said first interconnection scheme through a ~~fourth~~ second opening in said ~~fourth~~ second polymer layer;

a first semiconductor chip over said first interconnection scheme and between said first and second ~~solder~~ metal bumps, wherein said first semiconductor chip comprises a ~~first~~ third metal bump connected to a ~~fourth metal interconnection layer of said second metal interconnect~~ second metal interconnect through a ~~fifth~~ third opening in said ~~fourth~~ second polymer layer~~, wherein said first chip and said first and second solder bumps are in the same horizontal plane,~~

~~wherein a fourth distance is between a backside surface of said first chip and a top surface of said fourth polymer layer is smaller than a thickness of said first solder bump~~; and

a second semiconductor chip ~~over~~ under said first interconnection scheme and said first semiconductor chip, wherein said first interconnection scheme is between said first and second semiconductor chips, wherein said second semiconductor chip comprises a central-processing-unit (CPU) circuit block and a graphics-processing-unit (GPU) circuit block. ~~second metal bump connected to a fifth metal interconnection layer of said second metal interconnect through a sixth opening in said fourth polymer layer.~~

32. (Currently amended) The chip package of claim 31, further comprising a third semiconductor chip over said first interconnection scheme and next to said first semiconductor chip.~~no any copper plug with thickness between 100 and 300 micrometers is between said first and second rows.~~

33. (Currently amended) The chip package of claim 31, wherein said second semiconductor chip comprises a first metal pad on a top surface and a second metal pad on a bottom surface, wherein said first metal pad is connected to said second metal pad through a through-silicon-via metal layer.~~a third portion is between said first and second portions, wherein said third portion is a square and no any copper plug with thickness between 100 and 300 micrometers in said third portion, wherein said third portion has a width greater than said second and third distances, wherein said third portion has a length greater than said second and third distances.~~

34. (Currently amended) The chip package of claim 31, further comprising a third semiconductor chip over said first interconnection scheme and next to said first semiconductor chip, wherein said third semiconductor chip is connected to said first metal bump through said first metal interconnect.~~wherein said first polymer layer further comprises multiple third copper plugs~~

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~~extending through a third portion of said first polymer layer from said first surface to said second surface, wherein said multiple third copper plugs are arranged in a first column substantially vertical to said first and second sidewalls, multiple fourth copper plugs extending through a fourth portion of said first polymer layer from said first surface to said second surface, wherein said multiple fourth copper plugs are arranged in a second column substantially vertical to said first and second sidewalls, wherein each of said multiple third and fourth copper plugs has a top surface coplanar to said first surface and a bottom surface coplanar to said second surface.~~

35. (Previously presented) The chip package of claim 31, wherein said first polymer layer has a coefficient of expansion between 3 and 10 ppm/°C .

36. (Currently amended) The chip package of claim 31, further comprising <u>further comprising a third semiconductor chip under said second semiconductor chip and multiple fourth metal bumps between said second and third semiconductor chips, wherein said second semiconductor chip comprises a first metal pad on a top surface and a second metal pad on a bottom surface, wherein said first metal pad is connected to said second metal pad through a through-silicon-via metal layer.</u> ~~a third solder bump under said second surface and directly under said one of said multiple first copper plugs, wherein said third solder bump connected to said first solder bump through said one of said multiple first copper plugs.~~

37. (Currently amended) The chip package of claim 31, further comprising <u>a passive component connect to said second metal bump through said first interconnection scheme.</u> ~~:~~

~~a second interconnection scheme under said second surface, wherein said second interconnection scheme comprises a third metal interconnect under said second surface, a fifth polymer layer between said second surface and said third metal interconnect and a sixth polymer layer under said third metal interconnect, wherein said third metal interconnect comprises a fifth metal~~

~~interconnection layer under said fifth polymer layer and connected to said one of said multiple first copper plugs, wherein said fifth metal interconnection layer comprises a third metal layer in a sixth opening in said fifth polymer layer and a third copper layer under said third metal layer in said sixth opening; and~~

~~a third chip under said second interconnection scheme and connected to said third metal interconnect via a metal wire.~~

38. (Currently amended) The chip package of claim 31, wherein said second semiconductor chip comprises a fourth metal bump at a third surface of said second semiconductor chip and connect to said first semiconductor chip through said second metal interconnect, wherein said third metal bump is at a fourth surface of said first semiconductor chip, wherein said third surface is faced to said fourth surface. ~~further comprising:~~

~~a second interconnection scheme under said second surface, wherein said second interconnection scheme comprises a third metal interconnect under said second surface, a fifth polymer layer between said second surface and said third metal interconnect and a sixth polymer layer under said third metal interconnect, wherein said third metal interconnect comprises a fifth metal interconnection layer under said fifth polymer layer and connected to said one of said multiple first copper plugs, wherein said fifth metal interconnection layer comprises a third metal layer in a sixth opening in said fifth polymer layer and a third copper layer under said third metal layer in said sixth opening; and~~

~~a third chip under said second interconnection scheme and connected to said third metal interconnect;~~

~~a fourth chip under said third chip; and~~

~~multiple third metal bumps between said third and fourth chips.~~

39. (Currently amended) The chip package of claim 31, ~~wherein said second chip is between said first and second solder bumps.~~ further comprising a third semiconductor chip under said first interconnection scheme and next to said second semiconductor chip, wherein said third semiconductor chip is a memory chip.

40. (Currently amended) The chip package of claim 31, wherein said second semiconductor chip comprises a fourth metal bump, wherein said fourth metal bump comprises a second metal layer with a thickness between 5 and 30 micrometers, wherein said second metal layer comprises a third copper layer. ~~further comprising a third chip under said first interconnection scheme, wherein said third chip comprises a central-processing-unit (CPU) circuit block and a graphics-processing-unit (GPU) circuit block. .~~

41. (Newly added) The chip package of claim 21, further comprising a second semiconductor chip over said first interconnection scheme and connected to said first metal interconnect through a third metal bump, wherein said second semiconductor chip has a height is between a backside surface of said second semiconductor chip and a top surface of said second polymer layer is smaller than a thickness of said first metal bump.

42. (Newly added) The chip package of claim 21, further comprising a second semiconductor chip under said first semiconductor chip, wherein first semiconductor chip comprise a first metal pad connected to a second metal pad of said second semiconductor chip through a solder layer, wherein said solder layer between said first and second semiconductor chips.

43. (Newly added) The chip package of claim 21, further comprising a second semiconductor chip over said first interconnection scheme, wherein said first semiconductor chip comprises a central-processing-unit (CPU) circuit block and a graphics-processing-unit (GPU) circuit block.

44. (Newly added) The chip package of claim 21, further comprising a second semiconductor chip under said first interconnection scheme and next to said first semiconductor chip, wherein said first semiconductor chip comprises a central-processing-unit (CPU) circuit block and a graphics-processing-unit (GPU) circuit block.

45. (Newly added) The chip package of claim 31, wherein a height is between a backside surface of said first semiconductor chip and a top surface of said second polymer layer is smaller than a thickness of said first metal bump.

46. (Newly added) The chip package of claim 31, wherein said second semiconductor chip is coupled to said first semiconductor chip through said second metal interconnect.

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Amendments to the Specification:

In this paper, the specification is amended to correct informalities and for disclosure consistency, complying with the provisions of 37 CFR §1.121(e), to correct inaccuracies of description and definition, and to secure substantial correspondence between the claims, the remainder of the specification, and the drawings, as requested by the Examiner.

1. Please amend the title of the patent application from "METHOD FOR FABRICATING GLASS SUBSTRATE PACKAGE" to "CHIP PACKAGE". In order to make the content of claims consistent with the title of the invention.
(Remark: The applicant submitted the amendment for the title of the patent application on Aug. 13, 2020, but there is no any action/response for the amendment from the examiner in the non-final Office action issued on Sept. 21, 2020)

2. Please amend the paragraph [0006] from lines 11-13 of page 2 in the specification filed on Sept. 25, 2013 for disclosure accuracy, as below:

[0006] Increased Input-Output (IO) combined with increased demands for high performance, and then IC's has led to the development of ~~Flip-Chip~~ flip-chip Packages. Flip-chip technology fabricates bumps (typically Pb/Sn solders) on Al pads of ~~on~~ chip and ~~interconnect~~ interconnects the bumps …

3. Please amend the paragraph [0017] from line 21 of page 4 in the specification filed on Sept. 25, 2013 for disclosure accuracy, as below:

[0017] ~~Fig. 5a-5i~~ Figs. 5a-5i illustrate the shape and structure of the Z-axis traces, in accordance with the present disclosure.

4. Please amend the paragraphs [0018] and [0020] from lines 1 and 5 of page 5 in the specification filed on Sept. 25, 2013 for disclosure accuracy, as below:

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[0018] Figs. 6a-6j ~~are~~ illustrate a 1st process of forming a glass substrate, in accordance with the present disclosure.

[0020] Figs. 7a-7o ~~are~~ illustrate a 2nd process of forming the glass substrate, in accordance with the present disclosure.

5. Please amend the paragraphs [0029] to [0030] from lines 4 and 6 of page 6 in the specification filed on Sept. 25, 2013 for disclosure accuracy, as below:

[0029] Figs. 10a-10j ~~illustrates~~ illustrate a damascene process to form the metal layer on the glass substrate, in accordance with the present disclosure.

[0030] Figs. 11a-11i ~~illustrates~~ illustrate an embossing process to form the metal layer on the glass substrate, in accordance with the present disclosure.

6. Please amend the paragraph [0041] from lines 13 and 14 of page 7 in the specification filed on Sept. 25, 2013 for disclosure accuracy, as below:

[0041] …Multiple gaps 3~~,~~ and 5 ~~form~~ are formed in the net 2 and 4. Each of the traces 2a, 2b, 4a and 4b is easily ~~move~~ moved to change the size of gaps 3 and gaps 5. …

7. Please amend the paragraph [0046] from line 6 of page 9 in the specification filed on Sept. 25, 2013 for disclosure accuracy, as below:

[0046] Fig. 5a-5i ~~illustrates~~ illustrate the shape and structure of the traces 6.

8. Please amend the paragraphs [0047] and [0048] from lines 16 and 24 of page 10 in the specification filed on Sept. 25, 2013 for disclosure accuracy, as below:

[0047] …~~In~~ At the same time, the net 4 is moved down to …

[0048] …~~In~~ At the same time, ~~may be apply~~ maybe applied a force to …

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9. Please amend the paragraphs [0049]-[0051] from lines 8-9, 11, 13 and 20 of page 11 in the specification filed on Sept. 25, 2013 for disclosure accuracy, as below:

[0049] …wherein the thermal resistance layer 8 ~~cover~~ covers the gaps 5 between traces 4a, traces 4b and traces 6, then curing the thermal resistance layer 8.

[0050] 井Next, referring to Fig. 6d, a mold 10 is provided between the net 2 and the net 4, wherein the mold 10 surrounds the traces 6 and on the thermal resistance layer 8. The mold 10 is ~~hold~~ held up by a machine or a device.

[0051]…The bottom of traces 6 ~~are~~ is fixed by the fixed layer 12.

10. Please amend the paragraph [0053] from lines 12, 16 and 17 of page 12 in the specification filed on Sept. 25, 2013 for disclosure accuracy, as below:

[0053] …for example, there is zero to 3 bubbles in one cubic ~~cubic~~ meter of the glass layer 16, …

[0053] …The glass layer 16 may be ~~remove~~ removed bubbles through multiple processes of a laminating process, a squeezing process and a heating process.

11. Please amend the paragraphs [0056] and [0057] from lines 9, 17 and 18 of page 13 in the specification filed on Sept. 25, 2013 for disclosure accuracy, as below:

[0056] …the glass may begin to soften and with increasing ~~temperature~~ temperature, the glass will ultimately melt into the liquid state. …

[0057] …When the polymer layer cured to a solid state~~. The~~, then the polymer layer has ~~an expansion coefficient~~ a coefficient of expansion between 3 and 10 ppm/°C.

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(Remark: The applicant submitted the amendment for paragraph [0057] of the patent application on Mar. 8, 2020, but there is no any action/response for the amendment from the examiner in the non-final Office action issued on Sept. 21, 2020)

12. Please amend the paragraphs [0060] and [0062]-[0063] from lines 5, 11 and 63 of page 14 in the specification filed on Sept. 25, 2013 for disclosure accuracy, as below:

[0060] ...The first substrates 20 may be ~~make~~ made a planarization process using a suitable process. ...

[0062] Next, referring to ~~Fig.~~ Figs. 6l-6n, the metal plugs 21 may be arranged in different types, ...

[0063] ~~Fig.~~Figs. 7a-7m are illustrated a 2nd process of forming a glass substrate of the invention. ...

13. Please amend the paragraphs [0063] and [0064] from lines 2, 3, 5 and 21 of page 15 in the specification filed on Sept. 25, 2013 for disclosure accuracy, as below:

[0063]...One of the non-circular ~~trace~~ traces 752 has a width greater than the thickness of one of the non-circular ~~trace~~ traces 752, ...

[0064] Next, referring to ~~Fig.~~ Figs. 7c-7d,

14. Please amend the paragraph [0065] from line 19 of page 16 in the specification filed on Sept. 25, 2013 for disclosure accuracy, as below:

[0065]...wherein a fourth least distance between the ~~two~~ hole 110a and hole 112a and a fifth least distance between the ~~two~~ hole 114a...

15. Please amend the paragraph [0066] from lines 14-15 of page 17 in the specification filed on

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Sept. 25, 2013 for disclosure accuracy, as below:

[0065]…Next, the top of the bolts 130, 132, 134, 136 are passing through the holes 110a, 112a, 114a~~, 116a~~ and 116a of another the third metal plate 11 respectively and the third metal plate 11 is formed on the second metal plates 9. Next, ~~The~~ the top of the bolts 130, 132…

16. Please amend the paragraph [0068] from lines 15-16 of page 18 in the specification filed on Sept. 25, 2013 for disclosure accuracy, as below:

[0068]…The glass layer 16 may be ~~remove~~ removed bubbles through multiple processes of a laminating process, a squeezing process and a heating process.

17. Please amend the paragraphs [0070]-[0073] from lines 2, 9, 12 and 18 of page 19 in the specification filed on Sept. 25, 2013 for disclosure accuracy, as below:

[0070]…The first substrates 20 may be ~~make~~ made a planarization process using a suitable process…

[0071]…A first pitch 21a and a second pitch 21b ~~is~~ are between the metal plugs 21, …

[0072] Next, referring to ~~Fig.~~ Figs. 7p-7r, the metal plugs 21 may be arranged in different types, …

[0073] …The second substrate 22 ~~comprise~~ comprises an amorphous solid glass layer/body 16 …

18. Please amend the paragraphs [0077] and [0078] from lines 18 and 21 of page 20 in the specification filed on Sept. 25, 2013 for disclosure accuracy, as below:

[0077] Fig. 9a-Fig. 9t ~~illustrates~~ illustrate a process to form multiple traces on a top

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surface and a bottom surface of the first substrate 20.

[0078]…wherein the first dielectric layer 24 may include or ~~may be~~ maybe a layer of silicon oxide (such as SiO_2), …

19. Please amend the paragraphs [0080] and [0081] from lines 14, 15 and 19-21 of page 21 in the specification filed on Sept. 25, 2013 for disclosure accuracy, as below:

[0080] …such as a vacuum deposition, a Physical Vapor Deposition (PVD), a Plasma Enhanced Chemical Vapor Deposition (PECVD), a sputtering process or an electroplating process, …

[0081] …The second metal layer 28 ~~may be~~ maybe comprises copper, nickel, gold or aluminum formed using a suitable process, such as a vacuum deposition, a Physical Vapor Deposition (PVD), a Plasma Enhanced Chemical Vapor Deposition (PECVD), a sputtering process …

20. Please amend the paragraph [0082] from line 2 of page 22 in the specification filed on Sept. 25, 2013 for disclosure accuracy, as below:

[0082] …such as a spin coating process or a lamination process. Next, a photo…

21. Please amend the paragraphs [0087]-[0089] from lines 7, 8, 12-14 and 18 of page 23 in the specification filed on Sept. 25, 2013 for disclosure accuracy, as below:

[0087] …such as a vacuum deposition, a Physical Vapor Deposition (PVD), a Plasma Enhanced Chemical Vapor Deposition (PECVD), a sputtering process or …

[0088] …The fourth metal layer 36 ~~may be~~ maybe comprises copper, nickel, gold or aluminum formed using a suitable process, such as a vacuum deposition, a Physical Vapor

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Deposition (PVD), a Plasma Enhanced Chemical Vapor Deposition (PECVD), a sputtering process or …

[0089] …such as a spin coating process or a lamination process. Next, a photo …

22. Please amend the paragraphs [0092] and [0094] from lines 4, 6 and 20 of page 24 in the specification filed on Sept. 25, 2013 for disclosure accuracy, as below:

[0087] …a third dielectric layer 40 is formed on the second ~~second~~ dielectric layer 32 and on the fourth metal layer 36, wherein the third dielectric layer 40 may include or ~~may be~~ maybe a layer of silicon oxide (such as SiO_2), …

[0094] …the fourth metal layer 36 not be damaged and ~~oxidated~~ oxidized.

23. Please amend the paragraphs [0097] and [0098] from lines 5-6 and 17 of page 25 in the specification filed on Sept. 25, 2013 for disclosure accuracy, as below:

[0097] …third dielectric layer 40 through a ~~flip chip~~ flip-chip package process or a ~~wirebonding~~ wire-bonding package process, wherein the chip 46 ~~and~~ or 56 comprises may be a memory chip...

[0098] The chips 46 are set up on the third dielectric layer 40 through a ~~flip chip~~ flip-chip package process, …

24. Please amend the paragraph [0100] from line 15 of page 26 in the specification filed on Sept. 25, 2013 for disclosure accuracy, as below:

[0100] …An underfill layer 64 is covered the chip56, the metal wires 62 and the metal pads 58.

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25. Please amend the paragraphs [0105] and [0106] from lines 13, 17 and 18 of page 28 in the specification filed on Sept. 25, 2013 for disclosure accuracy, as below:

[0105] …the 3D IC chip 46 through the ~~flip chip~~ flip-chip package process, …

[0106] Fig. 9y, illustrates a top view of the first substrate 20. Fig. 9u-Fig. 9w illustrate a ~~cross section~~ cross-section view of Line L-L' in Fig. 9y.

26. Please amend the paragraphs [0108] and [0109] from lines 1, 3 and 4 of page 29 in the specification filed on Sept. 25, 2013 for disclosure accuracy, as below:

[0108] Fig. 10a-Fig. 10j ~~illustrates~~ illustrate a damascene process to form the first metal layer 26, the second metal layer 28, the third metal layer 34 and the fourth metal layer 36 on a top surface and a bottom surface of ~~the~~ the first substrate 20.

[0109] …the dielectric layers 24 in ~~Figs.~~ Fig. 9a include two dielectric layers 80 and 82. …

27. Please amend the paragraph [0110] from line 1 of page 31 in the specification filed on Sept. 25, 2013 for disclosure accuracy, as below:

[0110] Fig. 11a-Fig. 11i ~~illustrates~~ illustrate an embossing process to form the first metal layer 26, …

28. Please amend the paragraphs [0120] and [0122] from lines 1, 3 and 4 of page 33 in the specification filed on Sept. 25, 2013 for disclosure accuracy, as below:

[0120] …The OLED display substrate may comprise a touch screen function. …

[0122] …the OLED display substrate can be replaced ~~to~~ with a Micro Electro Mechanical Systems (MEMS)…

29. Please amend the paragraph [0124] from lines 5, 15 and 16 of page 34 in the specification filed on Sept. 25, 2013 for disclosure accuracy, as below:

[0124] …Third application: Please ~~referring~~ refer to Fig. 14, …

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[0124] ...The LCD display substrate may ~~comprise~~ comprises a touch screen function, wherein the LCD display substrate ~~comprise~~ comprises an in-cell TFT LCD substrate. ...

30. Please amend the paragraphs [0126] and [0127] from lines 3, 7, 9 and 22-23 of page 35 in the specification filed on Sept. 25, 2013 for disclosure accuracy, as below:

[0126] ...LCD display substrate through ~~flip chip~~ flip-chip bonding process, ...

[0126] ...electrodes 114 on the bottom surface of the first glass substrate 106...

[0126] ...The structure of the first glass substrate 106 can refer to the second substrates 22...

[0127] ...The organic light-emitting diodes layer 110 (or a polymer light-emitting diodes layer, PLED layer) is replaced ~~to~~ with the liquid crystal display layer 111. The second substrates 22 is connected to a OLED display substrate through ~~flip chip~~ flip-chip bonding process ...

31. Please amend the paragraphs [0127] and [0128] from lines 4, 6, 16 and 19 of page 36 in the specification filed on Sept. 25, 2013 for disclosure accuracy, as below:

[0127] ...transparent electrodes 114 on the bottom surface of the first glass substrate 106...

[0127] ...The structure of the first glass substrate 106 can refer ...

[0128] ...the second substrates 22 and the second glass substrate 108, ...

[0128] ...electrodes 114 between the second substrates 22 and the second glass substrate 108, ...

32. Please amend the paragraph [0129] from line 3 of page 37 in the specification filed on Sept. 25, 2013 for disclosure accuracy, as below:

[0129] ...second substrates 22 and the second glass substrate 108, ...

33. Please amend the paragraphs [0131] and [0132] from lines 9-11 and 19 of page 38 in the specification filed on Sept. 25, 2013 for disclosure accuracy, as below:

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[0131] ...the first insulating layer 706, the second insulating layer 712 and the third insulating layer 808. The buffer layer 702、the first insulating layer 706, the second insulating layer 712 and the third insulating layer 808 ~~comprises~~ comprise a polyimide, ...

[0132] ...indium gallium oxide (IGO), aluminum zinc oxide (AZO) and ~~In2O3~~ In_2O_3.

34. Please amend the paragraphs [0134] and [0135] from lines 9 and 22 of page 38 in the specification filed on Sept. 25, 2013 for disclosure accuracy, as below:

[0134] ...wherein a gap between ~~the~~ each edge 119b...

[0135] ...display devices 125 can be combined with a big display device, an advertising ~~billboards~~ billboard. ...

Applicants submit that the substitute specification contains no new matter in compliance with 37 CFR §1.125(b), and respectfully request that it be made a part of the record of the present application. No additional pages were added due to the amendments.

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Docket No.: Mars-16-001-US-C01 **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	Customer Number: 102851
Ping-Jung Yang	:	Confirmation Number: 4809
Application No.: 16752650	:	Group Art Unit: 2812
Filed: Jan. 26, 2020	:	Examiner: LIU, XIAOMING

For: CHIP PACKAGE

Supplemental Amendment

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Please amend the above-identified application and consider the remarks as follows:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks/Arguments begin on page 9 of this paper.

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Electronic Acknowledgement Receipt	
EFS ID:	41052729
Application Number:	16752650
International Application Number:	
Confirmation Number:	4809
Title of Invention:	METHOD FOR FABRICATING GLASS SUBSTRATE PACKAGE
First Named Inventor/Applicant Name:	Ping-Jung Yang
Customer Number:	102851
Filer:	Ping-Jung. Yang
Filer Authorized By:	
Attorney Docket Number:	Mars16-001-US-C01
Receipt Date:	06-NOV-2020
Filing Date:	26-JAN-2020
Time Stamp:	08:42:14
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		Mars16-001-US-C01-SA-11062020-1.pdf	582255 3b64926995634db729128bfffe114b0089d06a04	yes	10

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Applicant Arguments/Remarks Made in an Amendment	9	10
	Claims	2	8
	Supplemental Response or Supplemental Amendment	1	1
Warnings:			
Information:			
	Total Files Size (in bytes):	582255	

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New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

REMARKS/ARGUMENTS

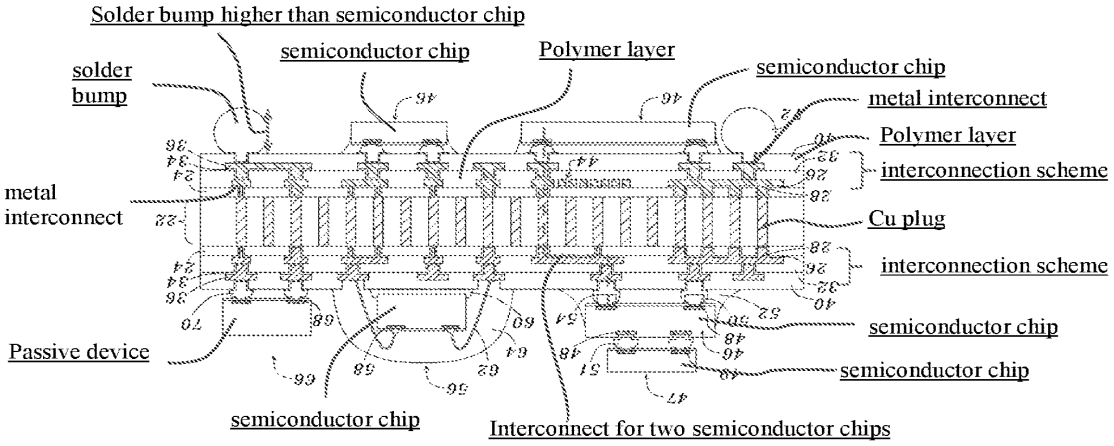
Claims 1-20 are cancelled. Claims 21-46 are pending in the application, of which claims 21 and 31 are the pending independent claims. No new matter is believed to be added into the application by this paper.

Claim Amendments

1. For claims 21, 30 and 40 the subject matter that "first semiconductor chip comprises a fourth metal interconnect on a metal pad of said first semiconductor chip, wherein said fourth metal interconnect comprises a second metal layer on said metal pad and a third metal layer over said second metal layer, wherein said third metal layer comprises a third copper layer and ~~with~~ has a thickness between 5 and 30 micrometers, wherein said fourth metal interconnect is coupled to said third metal interconnect" (Claim 21), "metal pad is an aluminum pad." (Claim 30) and "second semiconductor chip comprises a third metal interconnect on a metal pad of said second semiconductor chip, wherein said third metal interconnect comprises a second metal layer on said metal pad and a third metal layer over said second metal layer, wherein said third metal layer comprises a third copper layer and has a thickness between 5 and 30 micrometers, wherein said third metal interconnect is coupled to said a fourth metal interconnect of said first interconnection scheme" (Claim 40), are disclosed and supported in Fig. 18x and paragraph [0041] in the specification of the provisional App. No. 61/705,649 filed on Sept. 26, 2012, (and disclosed and supported in Fig. 9x and paragraph [0098] in the specification of the provisional App. No. 14/036256, filed on Sept. 25, 2013), as below:

[0041] .... the chip 46 comprises multiple metal pads 48 and **multiple metal bumps 50 formed on the metal pads 48**. The metal pad 48 may be an electroplated copper pad, a damascene copper pad or an aluminum pad. **The metal bump 50 comprises an adhesion/barrier metal layer formed on the metal pad 48, an electroplated metal layer** or an electro-less metal layer formed **on the adhesion/barrier metal layer**.... the **electroplated metal layer comprises a copper layer**, a gold layer... The **electroplated metal layer has a thickness** between 2 and 5 micrometers, **between 5 and 30 micrometers** or between...

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The above amendment is not believed to add any new matter.

In view of the Amendments, Applicants submit that the claims are in condition for allowance and respectfully request a notice to this effect.

Respectfully submitted,

Mars Yang

Date: __2020-11-06_____ Ping-Jung Yang

Email: semars3898@gmail.com

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Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

What is claimed is:

Claims 1-20 Cancelled

21. (Currently amended) A chip package comprising:

a first polymer layer has a first surface and a second surface opposed to said first surface, wherein said first surface is parallel to said second surface, a first copper plug extending through said first polymer layer from said first surface to said second surface, a second copper plug extending through said first polymer layer from said first surface to said second surface, and a third copper plug extending through said first polymer layer from said first surface to said second surface, wherein said first, second and third copper plugs each has a top surface coplanar with said first surface, wherein a pitch between said first and third plugs is between 50 and 200 micrometers, wherein said first polymer layer has a thickness between 100 and 300 micrometers and has a coefficient of expansion between 3 and 10 ppm/°C;

a first interconnection scheme over said first surface, wherein said first interconnection scheme comprises a first metal interconnect over said first surface, a second metal interconnect over said first surface, a third metal interconnect over said first surface and a second polymer layer over said first, second and ~~second~~ third metal interconnects, wherein said first metal interconnect is connected to said first copper plug, wherein said first metal interconnect

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comprises a first metal layer, a first copper layer on said first metal layer, and a second copper layer on said first copper layer;

a first metal bump over said first interconnection scheme and connected to said second copper plug through said second metal interconnect, wherein said first metal bump comprises a tin-containing layer; and

a first semiconductor chip under said first interconnection scheme, wherein said first semiconductor chip comprises a ~~second metal bump~~ fourth metal interconnect on a metal pad of said first semiconductor chip, wherein said ~~second metal bump~~ fourth metal interconnect comprises a second metal layer on said metal pad and a third metal layer over said second metal layer, wherein said third metal layer comprises a third copper layer and ~~with~~ has a thickness between 5 and 30 micrometers, wherein said fourth metal interconnect is coupled to said third metal interconnect.

22. (Previously presented) The chip package of claim 21, further comprising a passive component over said interconnection scheme and connected to said first metal interconnect through a solder layer.

23. (Previously presented) The chip package of claim 21, further comprising a second semiconductor chip over said first interconnection scheme and a third semiconductor chip over said second semiconductor chip.

24. (Previously presented) The chip package of claim 21, further comprising a second semiconductor chip over said first interconnection scheme, wherein said second semiconductor chip comprises a third metal bump between said second semiconductor chip and said first interconnection scheme.

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25. (Previously presented) The chip package of claim 21, wherein said first semiconductor chip comprises a central-processing-unit (CPU) circuit block and a graphics-processing-unit (GPU) circuit block.

26. (Previously presented) The chip package of claim 21, wherein said first semiconductor chip comprises a first metal pad on a top surface and a second metal pad on a bottom surface, wherein said first metal pad is connected to said second metal pad through a through-silicon-via metal layer.

27. (Currently amended) The chip package of claim 21, wherein said first interconnection scheme further comprises a ~~third~~ fifth metal interconnect over said first metal interconnect and said second polymer layer, wherein said second polymer is between said first and ~~third~~ fifth metal interconnects, wherein said ~~third~~ fifth metal interconnect comprises a ~~third~~ fourth metal layer, a ~~third~~ fourth copper layer on said ~~third~~ fourth metal layer, and a ~~fourth~~ fifth copper layer on said ~~third~~ fourth copper layer.

28. (Previously presented) The chip package of claim 21, further comprising a second interconnection scheme under said first polymer layer and on said second surface.

29. (Previously presented) The chip package of claim 21, wherein said first copper plugs has a top surface coplanar with said first surface and a bottom surface coplanar with said second surface.

30. (Currently amended) The chip package of claim 21, wherein said metal pad is an aluminum pad. ~~second metal layer comprises a copper layer.~~

31. (Previously presented) A chip package comprising:

a first polymer layer has a first surface, a second surface opposed to said first surface, wherein said first surface is parallel to said second surface, a first copper plug extending through

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said first polymer layer from said first surface to said second surface, a second copper plug extending through said first polymer layer from said first surface to said second surface, and a third copper plug extending through said first polymer layer from said first surface to said second surface, wherein said first, second and third copper plugs each has a top surface coplanar with said first surface, wherein a pitch between said first and third plugs is between 50 and 200 micrometers, wherein said first polymer layer has a thickness between 100 and 300 micrometers;

a first interconnection scheme over said first surface, wherein said first interconnection scheme comprises a first metal interconnect over said first surface, a second metal interconnect over said first surface and a second polymer layer over said first and second metal interconnects, wherein said first metal interconnect is connected to said first copper plug, wherein said first metal interconnect comprises a first metal layer, a first copper layer on said first metal layer, and a second copper layer on said first copper layer;

a first metal bump over said first interconnection scheme, wherein said first metal bump is connected to said first copper plug through a first opening in said second polymer layer and said first metal interconnect, wherein said first metal bump comprises a tin-containing layer;

a second metal bump over said first interconnection scheme, wherein said second metal bump is connected to said first interconnection scheme through a second opening in said second polymer layer;

a first semiconductor chip over said first interconnection scheme and between said first and second metal bumps, wherein said first semiconductor chip comprises a third metal bump connected to a second metal interconnect through a third opening in said second polymer layer; and

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a second semiconductor chip under said first interconnection scheme and said first semiconductor chip, wherein said first interconnection scheme is between said first and second semiconductor chips, wherein said second semiconductor chip comprises a central-processing-unit (CPU) circuit block and a graphics-processing-unit (GPU) circuit block.

32. (Previously presented) The chip package of claim 31, further comprising a third semiconductor chip over said first interconnection scheme and next to said first semiconductor chip.

33. (Previously presented) The chip package of claim 31, wherein said second semiconductor chip comprises a first metal pad on a top surface and a second metal pad on a bottom surface, wherein said first metal pad is connected to said second metal pad through a through-silicon-via metal layer.

34. (Previously presented) The chip package of claim 31, further comprising a third semiconductor chip over said first interconnection scheme and next to said first semiconductor chip, wherein said third semiconductor chip is connected to said first metal bump through said first metal interconnect.

35. (Previously presented) The chip package of claim 31, wherein said first polymer layer has a coefficient of expansion between 3 and 10 ppm/°C .

36. (Previously presented) The chip package of claim 31, further comprising further comprising a third semiconductor chip under said second semiconductor chip and multiple fourth metal bumps between said second and third semiconductor chips, wherein said second semiconductor chip comprises a first metal pad on a top surface and a second metal pad on a bottom surface, wherein said first metal pad is connected to said second metal pad through a through-silicon-via metal layer.

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37. (Previously presented) The chip package of claim 31, further comprising a passive component connect to said second metal bump through said first interconnection scheme.

38. (Previously presented) The chip package of claim 31, wherein said second semiconductor chip comprises a fourth metal bump at a third surface of said second semiconductor chip and connect to said first semiconductor chip through said second metal interconnect, wherein said third metal bump is at a fourth surface of said first semiconductor chip, wherein said third surface is faced to said fourth surface.

39. (Previously presented) The chip package of claim 31, further comprising a third semiconductor chip under said first interconnection scheme and next to said second semiconductor chip, wherein said third semiconductor chip is a memory chip.

40. (Currently amended) The chip package of claim 31, wherein said second semiconductor chip comprises a third metal interconnect on a metal pad of said second semiconductor chip, wherein said third metal interconnect comprises a second metal layer on said metal pad and a third metal layer over said second metal layer, wherein said third metal layer comprises a third copper layer and has a thickness between 5 and 30 micrometers, wherein said third metal interconnect is coupled to said a fourth metal interconnect of said first interconnection scheme. ~~fourth metal bump, wherein said fourth metal bump comprises a second metal layer with a thickness between 5 and 30 micrometers, wherein said second metal layer comprises a third copper layer.~~

41. (Previously presented) The chip package of claim 21, further comprising a second semiconductor chip over said first interconnection scheme and connected to said first metal interconnect through a third metal bump, wherein said second semiconductor chip has a height is between a backside surface of said second semiconductor chip and a top surface of said second polymer layer is smaller than a thickness of said first metal bump.

42. (Previously presented) The chip package of claim 21, further comprising a second semiconductor chip under said first semiconductor chip, wherein first semiconductor chip

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comprise a first metal pad connected to a second metal pad of said second semiconductor chip through a solder layer, wherein said solder layer between said first and second semiconductor chips.

43. (Previously presented) The chip package of claim 21, further comprising a second semiconductor chip over said first interconnection scheme, wherein said first semiconductor chip comprises a central-processing-unit (CPU) circuit block and a graphics-processing-unit (GPU) circuit block.

44. (Previously presented) The chip package of claim 21, further comprising a second semiconductor chip under said first interconnection scheme and next to said first semiconductor chip, wherein said first semiconductor chip comprises a central-processing-unit (CPU) circuit block and a graphics-processing-unit (GPU) circuit block.

45. (Previously presented) The chip package of claim 31, wherein a height is between a backside surface of said first semiconductor chip and a top surface of said second polymer layer is smaller than a thickness of said first metal bump.

46. (Previously presented) The chip package of claim 31, wherein said second semiconductor chip is coupled to said first semiconductor chip through said second metal interconnect.

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PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 16/752,650	Filing Date 01/26/2020	☐ To be Mailed

ENTITY: ☑ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A		N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A		N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*		x $100 =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*		x $460 =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).				
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))					
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL	

APPLICATION AS AMENDED - PART II

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT	11/05/2020	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 24	Minus	** 20	= 4		x $100 =	400
	Independent (37 CFR 1.16(h))	* 3	Minus	*** 3	= 0		x $480 =	0
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	400

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT	11/06/2020	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 26	Minus	** 24	= 2		x $100 =	200
	Independent (37 CFR 1.16(h))	* 2	Minus	*** 3	= 0		x $480 =	0
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	200

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.	LIE
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".	/ANGELA S WHITE/
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".	
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.	

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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NOTICE OF ALLOWANCE AND FEE(S) DUE

102851 7590 04/26/2021

PING-JUNG YANG
NO 2, NIOUPU SOUTH RD., SIANGSHAN DISTRICT
HSINCHU CITY, 30091
TAIWAN

EXAMINER	
LIU, XIAOMING	
ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 04/26/2021

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/752,650	01/26/2020	Ping-Jung Yang	Mars16-001-US-C01	4809

TITLE OF INVENTION: CHIP PACKAGE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	$600	$0.00	$0.00	$600	07/26/2021

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Maintenance fees are due in utility patents issuing on applications filed on or after Dec. 12, 1980. It is patentee's responsibility to ensure timely payment of maintenance fees when due. More information is available at www.uspto.gov/PatentMaintenanceFees.

PTOL-85 (Rev. 02/11)

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PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via EFS-Web.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

102851 7590 04/26/2021

PING-JUNG YANG
NO 2, NIOUPU SOUTH RD., SIANGSHAN DISTRICT
HSINCHU CITY, 30091
TAIWAN

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via EFS-Web or by facsimile to (571) 273-2885, on the date below.

(Typed or printed name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/752,650	01/26/2020	Ping-Jung Yang	Mars16-001-US-C01	4809

TITLE OF INVENTION: CHIP PACKAGE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	$600	$0.00	$0.00	$600	07/26/2021

EXAMINER	ART UNIT	CLASS-SUBCLASS
LIU, XIAOMING	2812	257-091000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-09 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. Fees submitted: ❑Issue Fee ❑Publication Fee (if required) ❑Advance Order - # of Copies _____

4b. Method of Payment: *(Please first reapply any previously paid fee shown above)*

❑ Electronic Payment via EFS-Web ❑ Enclosed check ❑ Non-electronic payment by credit card (Attach form PTO-2038)

❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. _____

5. **Change in Entity Status** (from status indicated above)

❑ Applicant certifying micro entity status. See 37 CFR 1.29

❑ Applicant asserting small entity status. See 37 CFR 1.27

❑ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/752,650	01/26/2020	Ping-Jung Yang	Mars16-001-US-C01	4809

102851 7590 04/26/2021

PING-JUNG YANG
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HSINCHU CITY, 30091
TAIWAN

EXAMINER	
LIU, XIAOMING	
ART UNIT	**PAPER NUMBER**
2812	

DATE MAILED: 04/26/2021

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

PTOL-85 (Rev. 02/11)

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OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 16/752,650	Applicant(s) Yang, Ping-Jung	
	Examiner XIAOMING LIU	Art Unit 2812	AIA (FITF) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☑ This communication is responsive to 11/6/2020.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☑ The allowed claim(s) is/are 21-46 . As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see **http://www.uspto.gov/patents/init_events/pph/index.jsp** or send an inquiry to **PPHfeedback@uspto.gov.**

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some *c) ☐ None of the:

   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____ .

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____ .

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____.
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material _____.
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date. _____.
5. ☐ Examiner's Amendment/Comment
6. ☑ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/XIAOMING LIU/
Examiner, Art Unit 2812

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DETAILED ACTION

The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

Allowable Subject Matter

Claims 21-46 are allowed.

The following is an examiner's statement of reasons for allowance: currently independent claims 21 and 31 are allowable because the closest prior art does not appear to disclose, alone or in combination, the limitations of "wherein a pitch between said first and third plugs is between 50 and 200 micrometers, wherein said first polymer layer has a thickness between 100 and 300 micrometers and has a coefficient of expansion between 3 and 10 ppm/C; … wherein said first semiconductor chip comprises fourth metal interconnect on a metal pad of said first semiconductor chip, wherein said fourth metal interconnect comprises a second metal layer on said metal pad and a third metal laver over said second metal laver, wherein said third metal laver comprises a third copper laver and has a thickness between 5 and 30 micrometers, wherein said fourth metal interconnect is coupled to said third metal interconnect." in combination with the other required elements of claim 1 and "wherein said first, second and third copper plugs each has a top surface coplanar with said first surface, wherein a pitch between said first and third plugs is between 50 and 200 micrometers, wherein said first polymer layer has a thickness between 100 and 300 micrometers;… a first metal bump over said first interconnection scheme, wherein said first metal bump is connected to said first copper plug through a first opening in said second polymer layer and said first metal interconnect, wherein said first metal bump comprises a tin-containing layer; a second metal bump over said first interconnection scheme, wherein said second metal bump is connected to said first interconnection scheme through a second opening in said second polymer layer; a first semiconductor chip over said first interconnection scheme and between said first and second metal bumps, wherein said first semiconductor chip comprises a third

metal bump connected to a second metal interconnect through a third opening in said second polymer layer; and a second semiconductor chip under said first interconnection scheme and said first semiconductor chip, wherein said first interconnection scheme is between said first and second semiconductor chips" in combination with the other required elements of claim 31.

Specifically, the limitations are material to the inventive concept of the application in hand to forming a polymer interconnect with sufficient coefficient of expansion to enable holes and other features formed inside with improved chemical durability, strength and optical properties.

Dependent claims 22-30 and 32-46 are respectively dependent on currently amended allowable independent claims 21 or 31. Therefore, claims 22-30 and 32-46 incorporate the allowable limitations of claims 21 or 31. Consequently, claims 22-30 and 32-46 are allowable.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to XIAOMING LIU whose telephone number is (571)270-0384. The examiner can normally be reached on Monday-Friday, 9am-8pm, EST.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Charles Garber can be reached on (571)272-2194. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see https://ppair-my.uspto.gov/pair/PrivatePair. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/XIAOMING LIU/
Examiner, Art Unit 2812

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/752,650	Yang, Ping-Jung
	Examiner	Art Unit
	XIAOMING LIU	2812

CPC - Searched*		
Symbol	Date	Examiner
H01L23/49827 | H01L23/5384 | H01L2224/08165 | H01L2224/16165 | H01L2224/16235 | H01L2224/32165 | H01L2224/32235 | H01L2224/40165 | H01L2224/40235 | H01L2224/48165 | H01L2224/48235 with date and text	09/17/2020	XL

CPC Combination Sets - Searched*		
Symbol	Date	Examiner

US Classification - Searched*			
Class	Subclass	Date	Examiner

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	Date	Examiner
Searched East: (USPAT, USPGPUB, USOCR, FPRS, EPO, JPO, DERWENT, IBMTDB)	09/17/2020	XL
Inventor search Conducted, limited with text	09/17/2020	XL
Assignee search Conducted, limited with text	09/17/2020	XL
Google text search conducted	09/17/2020	XL
Non-Patent Literature searched: science direct, TC2800	09/17/2020	XL
updated search	04/22/2021	XL

/XIAOMING LIU/ Examiner, Art Unit 2812	

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Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/752,650	Yang, Ping-Jung
	Examiner	Art Unit
	XIAOMING LIU	2812

Interference Search			
US Class/CPC Symbol	**US Subclass/CPC Group**	**Date**	**Examiner**
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H01L2224	08165 16165 16235 32165 40165 40235 48165 48235 with text	04/22/2021	XL
	all CPC group with text	04/22/2021	XL

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Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/752,650	Yang, Ping-Jung
	Examiner	**Art Unit**
	XIAOMING LIU	2812

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Symbol					**Type**	**Version**
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H01L	/	23	/	49833	I	2013-01-01
H01L	/	51	/	0096	I	2013-01-01
H01L	/	2224	/	1308	A	2013-01-01
H01L	/	2224	/	13076	A	2013-01-01
H01L	/	2924	/	181	A	2013-01-01
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H01L	/	2224	/	73204	A	2013-01-01

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	26	
/XIAOMING LIU/ Examiner, Art Unit 2812	22 April 2021	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	21	fig17b

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Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/752,650	Yang, Ping-Jung
	Examiner	**Art Unit**
	XIAOMING LIU	2812

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NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	26	
/XIAOMING LIU/ Examiner, Art Unit 2812	22 April 2021	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	21	fig17b

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Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/752,650	Yang, Ping-Jung
	Examiner	Art Unit
	XIAOMING LIU	2812

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NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	26	
/XIAOMING LIU/ Examiner, Art Unit 2812	22 April 2021	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	21	fig17b

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Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/752,650	Yang, Ping-Jung
	Examiner	Art Unit
	XIAOMING LIU	2812

CPC Combination Sets								
Symbol					Type	Set	Ranking	Version
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NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	26	
/XIAOMING LIU/ Examiner, Art Unit 2812	22 April 2021	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	21	fig17b

U.S. Patent and Trademark Office — Part of Paper No.: 20210422

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Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/752,650	Yang, Ping-Jung
	Examiner	Art Unit
	XIAOMING LIU	2812

CPC Combination Sets								
Symbol					Type	Set	Ranking	Version
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H01L	/	2924	/	00012	A	35	2	2013-01-01
H01L	/	2224	/	13111	A	36	1	2013-01-01
H01L	/	2924	/	01047	A	36	2	2013-01-01
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NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	26	
/XIAOMING LIU/ Examiner, Art Unit 2812	22 April 2021	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	21	fig17b

U.S. Patent and Trademark Office — Part of Paper No.: 20210422

IPR2026-00067
TSMC EX1032 Page 458

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/752,650	Yang, Ping-Jung
	Examiner	Art Unit
	XIAOMING LIU	2812

CPC Combination Sets								
Symbol					Type	Set	Ranking	Version
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(Primary Examiner)	(Date)	21	fig17b

U.S. Patent and Trademark Office — Part of Paper No.: 20210422

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TSMC EX1032 Page 459

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/752,650	Yang, Ping-Jung
	Examiner	**Art Unit**
	XIAOMING LIU	2812

INTERNATIONAL CLASSIFICATION				
CLAIMED				
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H01L23/15	/	23	/	15
H01L23/498	/	23	/	498

NON-CLAIMED				
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US ORIGINAL CLASSIFICATION	
CLASS	**SUBCLASS**

CROSS REFERENCES(S)						
CLASS	**SUBCLASS (ONE SUBCLASS PER BLOCK)**					

NONE		Total Claims Allowed:	
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U.S. Patent and Trademark Office — Part of Paper No.: 20210422

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TSMC EX1032 Page 460

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/752,650	Yang, Ping-Jung
	Examiner	Art Unit
	XIAOMING LIU	2812

☑ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIMS

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
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	4		13	2	22	11	31	20	40						
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NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	26	
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(Primary Examiner)	(Date)	21	fig17b

U.S. Patent and Trademark Office — Part of Paper No.: 20210422

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EAST Search History

EAST Search History (Prior Art)

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S51	146	S50 and tsv same layout	US-PGPUB; USPAT; USOCR	OR	OFF	2020/09/11 13:47
S52	6	"20130049217" "20090155959" "20090230517" "20130277801" "20110257716" "20100252934"	US-PGPUB	OR	OFF	2020/09/17 16:44
S53	71	(US-20110304008-$ or US-20120313207-$ or US-20120241938-$ or US-20120193785-$ or US-20120052631-$ or US-20110297434-$ or US-20110026232-$ or US-20100290191-$ or US-20100207154-$ or US-20100200898-$ or US-20100102457-$ or US-20100044850-$ or US-20090315171-$ or US-20110110061-$ or US-20100123257-$ or US-20100052119-$ or US-20090184403-$ or US-20120326170-$ or US-20130050228-$ or US-20130049217-$ or US-20120313209-$ or US-20120306096-$ or US-20120228749-$ or US-20140124777-$ or US-20140042637-$ or US-20130328211-$).did. or (US-20130292844-$ or US-20130119562-$ or US-20100258944-$ or US-20100258946-$ or US-20100252937-$ or US-20080149384-$ or US-	US-PGPUB; USPAT	OR	ON	2021/04/22 11:47

		20130277855-$ or US-20170373004-$ or US-20170345761-$ or US-20130242493-$ or US-20100252934-$).did. or (US-9437534-$ or US-8247269-$ or US-8614120-$ or US-7968978-$ or US-9627365-$ or US-9817312-$ or US-9615453-$ or US-9363890-$ or US-9161443-$ or US-9030751-$ or US-8354304-$ or US-8273602-$ or US-8270176-$ or US-8263434-$ or US-8217514-$ or US-8193036-$ or US-8133762-$ or US-8110440-$ or US-8110908-$ or US-8105915-$ or US-8080445-$ or US-8067308-$ or US-8067828-$ or US-8067275-$ or US-8063477-$ or US-8034661-$).did. or (US-8008121-$ or US-7977802-$ or US-7935570-$ or US-7880293-$ or US-7858441-$ or US-7842542-$ or US-7838337-$ or US-7790503-$).did.				
S54	21,477	(H01L23/49827 | H01L23/5384 | H01L2224/08165 | H01L2224/16165 | H01L2224/16235 | H01L2224/32165 | H01L2224/32235 | H01L2224/40165 | H01L2224/40235 | H01L2224/48165 | H01L2224/48235).CPC.	US-PGPUB; USPAT; USOCR	OR	OFF	2021/04/22 11:47
S55	166	S54 and tsv same layout	US-PGPUB; USPAT; USOCR	OR	OFF	2021/04/22 11:47
S56	2	("20200161245").PN.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2021/04/22 11:48
S57	2	("20140085842").PN.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2021/04/22 12:22
S58	3	"20110147055"	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2021/04/22 12:24

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S59	10,057	(H01L23/49827 | H01L23/5384 | H01L2224/08165 | H01L2224/16165 |	USPAT	OR	OFF	2021/04/22 11:37

		H01L2224/16235 | H01L2224/32165 | H01L2224/32235 | H01L2224/40165 | H01L2224/40235 | H01L2224/48165 | H01L2224/48235).CPC.				
S60	8	S59 and (copper and pitch and (coeffcient or expansion) and thickness).clm.	USPAT	OR	OFF	2021/04/22 11:44
S61	22	S59 and (pitch and (coeffcient or expansion) and thickness).clm.	USPAT	OR	OFF	2021/04/22 11:45
S62	242	(pitch and (coeffcient or expansion) and thickness).clm.	USPAT	OR	OFF	2021/04/22 11:45

4/22/2021 12:26:06 PM
C:\Users\xliu3\Documents\EAST\Workspaces\202001\16752650_1.wsp

Bibliographic Data

Application No: 16/752,650

Foreign Priority claimed: ○ Yes ◉ No

35 USC 119 (a-d) conditions met: ☐ Yes ☑ No ☐ Met After Allowance

Verified and Acknowledged: /XIAOMING LIU/ (Examiner's Signature) | (Initials)

Title: CHIP PACKAGE

FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
01/26/2020	257	2812	Mars16-001-US-C01
RULE			

APPLICANTS

Ping-Jung Yang, Hsin-Chu City, TAIWAN

INVENTORS

Ping-Jung Yang, Hsinchu City, TAIWAN

CONTINUING DATA

This application is a CON of 15261956 09/11/2016 PAT 10622310

15261956 has PRO of 62219249 09/16/2015

15261956 is a CIP of 14036256 09/25/2013 PAT 9615453

14036256 has PRO of 61705649 09/26/2012

FOREIGN APPLICATIONS

IF REQUIRED, FOREIGN LICENSE GRANTED**

02/12/2020

**** SMALL ENTITY ****

STATE OR COUNTRY

TAIWAN

ADDRESS

PING-JUNG YANG
NO 2, NIOUPU SOUTH RD., SIANGSHAN DISTRICT
HSINCHU CITY, 30091
TAIWAN

FILING FEE RECEIVED

$785

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/752,650	01/26/2020	Ping-Jung Yang	Mars16-001-US-C01	4809

102851 7590 05/10/2021

PING-JUNG YANG
NO 2, NIOUPU SOUTH RD., SIANGSHAN DISTRICT
HSINCHU CITY, 30091
TAIWAN

EXAMINER	
LIU, XIAOMING	

ART UNIT	PAPER NUMBER
2812	

MAIL DATE	DELIVERY MODE
05/10/2021	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov

Application No. : 16752650
Applicant : Vang
Filing Date : 01/26/2020
Date Mailed : 05/10/2021

NOTICE TO FILE CORRECTED APPLICATION PAPERS

Notice of Allowance Mailed

This application has been accorded an Allowance Date and is being prepared for issuance. The application, however, is incomplete for the reasons below.

Applicant is given two (2) months from the mail date of this Notice within which to respond. This time period for reply is extendable under 37 CFR 1.136(a) for only TWO additional MONTHS.

The informalities requiring correction are indicated in the attachment(s). If the informality pertains to the abstract, specification (including claims) or drawings, the informality must be corrected with an amendment in compliance with 37 CFR 1.121 (or, if the application is a reissue application, 37 CFR 1.173). Such an amendment may be filed after payment of the issue fee if limited to correction of informalities noted herein. See Waiver of 37 CFR 1.312 for Documents Required by the Office of Patent Publication, 1280 Off. Gaz. Patent Office 918 (March 23, 2004). In addition, if the informality is not corrected until after payment of the issue fee, for purposes of 35 U.S.C. 154(b)(1)(iv), "all outstanding requirements" will be considered to have been satisfied when the informality has been corrected. A failure to respond within the above-identified time period will result in the application being ABANDONED.

See attachment(s).

A copy of this notice MUST be returned with the reply. Please address response to "Mail Stop Issue Fee, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450".

/Shirley Winslow/
Publication Branch
Office of Data Management
(571) 272-4200

Application No. 16752650

SPECIFICATION REFERS TO ITS OWN PAGE/PARAGRAPH NUMBER(S) AND/OR SPECIFICATION REFERS TO NONEXISTENT CLAIM(S)

[X] The patent will be printed in numbered columns with intercolumnar line numbers and without paragraph numbers. Any reference(s) within the applicant-filed specification to its own page number(s) or paragraph number(s) will have no meaning in the printed patent.

In response to this notice, the applicant either should file an amendment to the specification that removes the reference(s) to the page number(s) or paragraph number(s) or should submit a letter stating that the patent specification should be printed with the reference(s) to the page number(s) or paragraph number(s).

See Page(s)/Paragraph(s) p. 39 (paragraph 00136).

[ ] The specification refers by number to one or more claims that are not present in the allowed application – that is, the claim number(s) mentioned in the specification are higher than the total number of allowed claims.

In response to this notice, the applicant either should file an amendment to the specification that removes the reference(s) to the nonexistent claim(s) or should submit a letter stating that the patent specification should be printed with the reference(s) to the nonexistent claim(s).

See Page(s)/Paragraph(s) .

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 16/752,650	Filing Date 01/26/2020	☐ To be Mailed

ENTITY: ☐ LARGE ☑ SMALL ☐ MICRO

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A		N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A		N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*		x $50 =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*		x $230 =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).				
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))					
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL	

APPLICATION AS AMENDED - PART II

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT	05/25/2021	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 28	Minus	** 24	= 4		x $50 =	200
	Independent (37 CFR 1.16(h))	* 3	Minus	*** 3	= 0		x $240 =	0
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	200

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=		x $0 =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=		x $0 =	
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.	LIE
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".	/MARCUS A PRIDGEN/
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".	
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.	

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Doc code: RCEX
Doc description: Request for Continued Examination (RCE)

PTO/SB/30EFS (02-18)
Approved for use through 11/30/2020. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

REQUEST FOR CONTINUED EXAMINATION(RCE)TRANSMITTAL
(Submitted Only via EFS-Web)

Application Number	16752650	Filing Date	2020-01-26	Docket Number (if applicable)	Mars-16-001-US-C01	Art Unit	2812
First Named Inventor	Ping-Jung Yang			Examiner Name	LIU, XIAOMING		

This is a Request for Continued Examination (RCE) under 37 CFR 1.114 of the above-identified application.
Request for Continued Examination (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, or to any design application. The Instruction Sheet for this form is located at WWW.USPTO.GOV

SUBMISSION REQUIRED UNDER 37 CFR 1.114

Note: If the RCE is proper, any previously filed unentered amendments and amendments enclosed with the RCE will be entered in the order in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).

☐ Previously submitted. If a final Office action is outstanding, any amendments filed after the final Office action may be considered as a submission even if this box is not checked.

- ☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____
- ☐ Other _____

☒ Enclosed

- ☒ Amendment/Reply
- ☒ Information Disclosure Statement (IDS)
- ☐ Affidavit(s)/ Declaration(s)
- ☐ Other _____

MISCELLANEOUS

☐ Suspension of action on the above-identified application is requested under 37 CFR 1.103(c) for a period of months _____
(Period of suspension shall not exceed 3 months; Fee under 37 CFR 1.17(i) required)

☐ Other _____

FEES

☐ **The RCE fee under 37 CFR 1.17(e) is required by 37 CFR 1.114 when the RCE is filed.**
The Director is hereby authorized to charge any underpayment of fees, or credit any overpayments, to Deposit Account No _____

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

Patent Practitioner Signature

X Applicant Signature

PTO/SB/30EFS (02-18)
Approved for use through 11/30/2020. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Applicant Signature			
Applicant 1		Remove	
Signature	/Ping-Jung Yang/	Date (YYYY-MM-DD)	2021-05-25
Name	Ping-Jung Yang		
Click ADD for additional Applicant Signature		Add	

This collection of information is required by 37 CFR 1.114. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

IPR2026-00067
TSMC EX1032 Page 479

Electronic Patent Application Fee Transmittal

Application Number:	16752650
Filing Date:	26-Jan-2020
Title of Invention:	CHIP PACKAGE
First Named Inventor/Applicant Name:	Ping-Jung Yang
Filer:	Ping-Jung. Yang
Attorney Docket Number:	Mars16-001-US-C01

Filed as Small Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
CLAIMS IN EXCESS OF 20	2202	2	50	100
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
RCE- 1ST REQUEST	2801	1	680	680
		Total in USD ($)		**780**

Electronic Acknowledgement Receipt	
EFS ID:	42811503
Application Number:	16752650
International Application Number:	
Confirmation Number:	4809
Title of Invention:	CHIP PACKAGE
First Named Inventor/Applicant Name:	Ping-Jung Yang
Customer Number:	102851
Filer:	Ping-Jung. Yang
Filer Authorized By:	
Attorney Docket Number:	Mars16-001-US-C01
Receipt Date:	25-MAY-2021
Filing Date:	26-JAN-2020
Time Stamp:	11:44:22
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$780
RAM confirmation Number	E20215OB46513423
Deposit Account	
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		Mars16-001-US-C01-RP-05252021.pdf	850624 b856804848b4524bfff360b6ab107410125c57fe	yes	16
	Multipart Description/PDF files in .zip description				
	Document Description		**Start**	**End**	
	Amendment Submitted/Entered with Filing of CPA/RCE		1	1	
	Specification		2	2	
	Claims		3	10	
	Applicant Arguments/Remarks Made in an Amendment		11	16	
Warnings:					
Information:					
2	Specification	Mars16-001-US-C01-SPEC-cleanversion-05252021.pdf	299703 535837ce575d139063e3a874017c31609b433623	no	40
Warnings:					
Information:					
3	Information Disclosure Statement (IDS) Form (SB08)	Mars16-001-IDS-05252021.pdf	612827 ee16b8a4527fbf740c4dcbfb1d6ba89879a1fbb8	no	5
Warnings:					
Information:					
4	Request for Continued Examination (RCE)	Mars16-001-US-C01-RCE-05252021.pdf	1349994 c8c8d16bc3b437dbc359bd6797cb6b3e3f960bb8	no	3
Warnings:					
Information:					

5	Fee Worksheet (SB06)	fee-info.pdf	31683 2919f4a5a1bb6f1cb62be4810207d8068a7220df	no	2
Warnings:					
Information:					
			Total Files Size (in bytes):	3144831	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Docket No.: Mars-16-001-US-C01 **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	Customer Number: 102851
Ping-Jung Yang	:	Confirmation Number: 4809
Application No.: 16752650	:	Group Art Unit: 2812
Filed: Jan. 26, 2020	:	Examiner: LIU, XIAOMING

For: CHIP PACKAGE

AMENDMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Please amend the above-identified application and consider the remarks as follows:

Amendments to Specification begin on page 2 of this paper. The substitute specification without markings (clean version) is submitted herewith, which hereby corrects and replaces the substitute specification of the above-captioned application submitted on Nov. 5, 2020.

Amendments to the Claims are reflected in the listing of claims which begins on page 3 of this paper.

Remarks/Arguments begin on page 11 of this paper.

Copy of the Notice mailed on May 10, 2021 begins after **Remarks/Arguments**.

IPR2026-00067
TSMC EX1032 Page 485

Amendments to the Specification:

Please amend the paragraph [00136] of page 39 in the specification submitted on Nov. 5, 2020 for disclosure accuracy and correctness, as below:

[00136] The structure of the OLED display substrate disclosed in ~~the~~ Fig. 12 and Fig. 16 can be referred to related specifications as above. ~~the paragraph [00125] to the paragraph [00131].~~

IPR2026-00067
TSMC EX1032 Page 486

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

What is claimed is:

Claims 1-20 Cancelled

21. (Currently amended) A chip package comprising:

a first polymer layer ~~has~~ having a first surface and a second surface ~~opposed~~ opposite to said first surface, wherein said first surface is substantially parallel to said second surface, wherein said first polymer layer has a thickness between 100 and 300 micrometers and has a coefficient of expansion between 3 and 10 ppm/°C;

a first ~~copper~~ metal plug ~~extending through~~ vertically in a first through via in said first polymer layer, wherein said first metal plug comprises a first copper layer, wherein the first copper layer contacts with a sidewall of said first through via; ~~from said first surface to said second surface, a second copper plug extending through said first polymer layer from said first surface to said second surface, and a third copper plug extending through said first polymer layer from said first surface to said second surface, wherein said first, second and third copper plugs each has a top surface coplanar with said first surface, wherein a pitch between said first and third plugs is between 50 and 200 micrometers, wherein said first polymer layer has a thickness between 100 and 300 micrometers and has a coefficient of expansion between 3 and 10 ppm/°C;~~

a second metal plug vertically in a second through via in said first polymer layer, wherein said second metal plug comprises a second copper layer, wherein a top surface of said second metal plug and a top surface of said first metal plug are in the same horizontal plane;

a first interconnection scheme over said first surface, wherein said first interconnection scheme comprises a first metal interconnect over said first surface, a second metal interconnect over said first surface, a third metal interconnect over said first surface and a second polymer layer over said first, second and third metal interconnects, wherein said first metal interconnect is connected to said first ~~copper~~ metal plug, wherein said second metal interconnect is connected to said second metal plug, wherein said first metal interconnect comprises a first metal layer, a ~~first~~ third copper layer on said first metal layer, and a ~~second~~ fourth copper layer on said ~~first~~ third copper layer;

a first metal bump over said first interconnection scheme and ~~connected to~~ said second ~~copper~~ metal plug ~~through said second metal interconnect~~, wherein said first metal bump comprises a tin-containing layer; and

a first semiconductor chip under said first interconnection scheme, wherein said first semiconductor chip comprises a fourth metal interconnect on a first metal pad of said first semiconductor chip, wherein said fourth metal interconnect comprises a second metal layer on said first metal pad and a ~~third metal~~ fifth copper layer over said second metal layer, wherein said ~~third metal layer comprises a third~~ fifth copper layer ~~and~~ has a thickness between 5 and 30 micrometers, wherein said fourth metal interconnect is ~~coupled~~ connected to said third metal interconnect.

22. (Currently amended) The chip package of claim 21, further comprising a passive component over said first interconnection scheme and connected to said first ~~metal interconnect~~ interconnection scheme through a solder layer.

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23. (Currently amended) The chip package of claim 21, wherein said first interconnection scheme comprise a fifth metal interconnect across over a sidewall of the first semiconductor chip. ~~further comprising a second semiconductor chip over said first interconnection scheme and a third semiconductor chip over said second semiconductor chip.~~

24. (Currently amended) The chip package of claim 21, further comprising a second semiconductor chip over said first interconnection scheme, wherein said second semiconductor chip comprises a ~~third~~ second metal bump between said second semiconductor chip and said first interconnection scheme.

25. (Previously presented) The chip package of claim 21, wherein said first semiconductor chip comprises a central-processing-unit (CPU) circuit block and a graphics-processing-unit (GPU) circuit block.

26. (Currently amended) The chip package of claim 21, wherein said first semiconductor chip comprises a ~~first~~ second metal pad on a top surface of said first semiconductor chip and a ~~second~~ third metal pad on a bottom surface of said first semiconductor chip, wherein said ~~first~~ second metal pad is connected to said ~~second~~ third metal pad through a through-silicon-via metal layer.

27. (Currently amended) The chip package of claim 21, wherein said first interconnection scheme further comprises a fifth metal interconnect over said first metal interconnect and said second polymer layer, wherein said second polymer is between said first and fifth metal interconnects, wherein said fifth metal interconnect comprises a ~~fourth~~ third metal layer, a ~~fourth~~ sixth copper layer on said ~~fourth~~ third metal layer, and a ~~fifth~~ seventh copper layer on said ~~fourth~~ sixth copper layer.

28. (Previously presented) The chip package of claim 21, further comprising a second interconnection scheme under said first polymer layer and on said second surface.

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29. (Currently amended) The chip package of claim 21, wherein said first ~~copper~~ metal plugs has a top surface substantially coplanar with said first surface ~~and a bottom surface coplanar with said second surface~~.

30. (Currently amended) The chip package of claim 21, wherein said first metal pad is an aluminum pad.

31. (Currently amended) A chip package comprising:

a first polymer layer ~~has~~ having a first surface, a second surface ~~opposed~~ opposite to said first surface, wherein said first surface is substantially parallel to said second surface, wherein said first polymer layer has a thickness between 100 and 300 micrometers;

a first ~~copper~~ metal plug ~~extending~~ vertically in a first through via in ~~through~~ said first polymer layer, wherein said first metal plug comprises a first copper layer, wherein the first copper layer contacts with a sidewall of said first through via; ~~from said first surface to said second surface, a second copper plug extending through said first polymer layer from said first surface to said second surface, and a third copper plug extending through said first polymer layer from said first surface to said second surface, wherein said first, second and third copper plugs each has a top surface coplanar with said first surface, wherein a pitch between said first and third plugs is between 50 and 200 micrometers, wherein said first polymer layer has a thickness between 100 and 300 micrometers;~~

a second metal plug vertically in a second through via in said first polymer layer, wherein said second metal plug comprises a second copper layer, wherein a top surface of said second metal plug and a top surface of said first metal plug are in the same horizontal plane;

a first interconnection scheme over said first surface, wherein said first interconnection scheme comprises a first metal interconnect over said first surface, a second metal interconnect over said first surface and a second polymer layer over said first and second metal interconnects, wherein said first metal interconnect is connected to said first ~~copper~~ metal plug, wherein said first metal

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interconnect comprises a first metal layer, a ~~first~~ third copper layer on said first metal layer, and a ~~second~~ fourth copper layer on said ~~first~~ third copper layer;

a first metal bump over said first interconnection scheme, wherein said first metal bump is connected to said first interconnection scheme ~~copper plug~~ through a first opening in said second polymer layer, ~~and said first metal interconnect,~~ wherein said first metal bump comprises a tin-containing layer;

a second metal bump over said first interconnection scheme, wherein said second metal bump is connected to said first interconnection scheme through a second opening in said second polymer layer;

a first semiconductor chip over said first interconnection scheme and between said first and second metal bumps;

a third metal bump between said first semiconductor chip and said first interconnection scheme, wherein said ~~first semiconductor chip comprises a~~ third metal bump connected to ~~a~~ said second metal interconnect through a third opening in said second polymer layer; and

a second semiconductor chip under said first interconnection scheme and said first semiconductor chip, wherein said first interconnection scheme is between said first and second semiconductor chips, wherein said second semiconductor chip comprises a central-processing-unit (CPU) circuit block and a graphics-processing-unit (GPU) circuit block.

32. (Currently amended) The chip package of claim 31, further comprising a third semiconductor chip over said first interconnection scheme ~~and next to said first semiconductor chip~~.

33. (Currently amended) The chip package of claim 31, wherein said second semiconductor chip comprises a first metal pad on a top surface of said second semiconductor chip and a second metal pad on a bottom surface of said second semiconductor chip, wherein said first metal pad is connected to said second metal pad through a through-silicon-via metal layer.

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34. (Currently amended) The chip package of claim 31, further comprising a third metal plug vertically in a third through via in said first polymer layer, wherein a pitch between said first and third metal plugs is between 200 and 1000 micrometers. ~~semiconductor chip over said first interconnection scheme and next to said first semiconductor chip, wherein said third semiconductor chip is connected to said first metal bump through said first metal interconnect.~~

35. (Previously presented) The chip package of claim 31, wherein said first polymer layer has a coefficient of expansion between 3 and 10 ppm/°C .

36. (Currently amended) The chip package of claim 31, further comprising ~~further comprising~~ a third semiconductor chip under said second semiconductor chip and multiple fourth metal bumps between said second and third semiconductor chips, wherein said second semiconductor chip comprises a first metal pad on a top surface of said second semiconductor chip and a second metal pad on a bottom surface of said second semiconductor chip, wherein said first metal pad is connected to said second metal pad through a through-silicon-via metal layer.

37. (Currently amended) The chip package of claim 31, further comprising a passive component over said first interconnection scheme. ~~connect to said second metal bump through said first interconnection scheme.~~

38. (Currently amended) The chip package of claim 31, wherein said first interconnection scheme comprise a third metal interconnect across over a sidewall of the second semiconductor chip. ~~second semiconductor chip comprises a fourth metal bump at a third surface of said second semiconductor chip and connect to said first semiconductor chip through said second metal interconnect, wherein said third metal bump is at a fourth surface of said first semiconductor chip, wherein said third surface is faced to said fourth surface.~~

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39. (Currently amended) The chip package of claim 31, further comprising a third semiconductor chip under said first interconnection scheme ~~and next to said second semiconductor chip~~, wherein said third semiconductor chip is a memory chip.

40. (Currently amended) The chip package of claim 31, wherein said second semiconductor chip comprises a third metal interconnect on a metal pad of said second semiconductor chip, wherein said third metal interconnect comprises a second metal layer on said metal pad and a ~~third metal~~ fifth copper layer over said second metal layer, wherein said ~~third metal layer comprises a third~~fifth copper layer ~~and~~ has a thickness between 5 and 30 micrometers, wherein said third metal interconnect is ~~coupled~~ connected to said a fourth metal interconnect of said first interconnection scheme.

41. (Currently amended) The chip package of claim 21, further comprising a second semiconductor chip over said first interconnection scheme and connected to said first ~~metal interconnect~~ interconnection scheme through a ~~third~~ second metal bump, wherein said second semiconductor chip has a height is between a backside surface of said second semiconductor chip and a top surface of said second polymer layer is smaller than a thickness of said first metal bump.

42. (Currently amended) The chip package of claim 21, further comprising a second semiconductor chip under said first semiconductor chip, wherein said first semiconductor chip comprise a ~~first~~ second metal pad connected to a ~~second~~ third metal pad of said second semiconductor chip through a solder layer, wherein said solder layer between said first and second semiconductor chips.

43. (Previously presented) The chip package of claim 21, further comprising a second semiconductor chip over said first interconnection scheme, wherein said first semiconductor chip comprises a central-processing-unit (CPU) circuit block and a graphics-processing-unit (GPU) circuit block.

44. (Currently amended) The chip package of claim 21, further comprising a third metal plug vertically in a third through via in said first polymer layer, wherein a pitch between said first and third metal plugs is between 200 and 1000 micrometers. ~~further comprising a second semiconductor chip under said first interconnection scheme and next to said first semiconductor chip, wherein said~~

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~~first semiconductor chip comprises a central processing unit (CPU) circuit block and a graphics processing unit (GPU) circuit block.~~

45. (Previously presented) The chip package of claim 31, wherein a height is between a backside surface of said first semiconductor chip and a top surface of said second polymer layer is smaller than a thickness of said first metal bump.

46. (Currently amended) The chip package of claim 31, wherein said second semiconductor chip is coupled to said first semiconductor chip through said ~~second metal interconnect~~ first interconnection scheme.

47. (Newly added) The chip package of claim 21, wherein said first metal plug has a thickness between 100 and 300 micrometers.

48. (Newly added) The chip package of claim 31, wherein said first metal plug has a thickness between 100 and 300 micrometers.

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CHIP PACKAGE

[0001] This patent application is a continuation of application No. 15261956, filed Sept. 11, 2016, now pending, which claims priority benefits from U.S. provisional patent application No. 62/219249, filed Sept. 16, 2015. This patent application of application No. 15261956 is a continuation-in-part of application No. 14/036256, filed Sept. 25, 2013, now patent No. 9615453, which claims the benefit of priority from U.S. provisional patent application No. 61/705,649, filed Sept. 26, 2012, all of which is incorporated herein by reference in their entirety.

BACKGROUND OF THE DISCLOSURE

Field of the Disclosure

[0002]The patent disclosure a method and structure to manufacture a glass substrate, and disclosed embodiments relate to one or more chip building a system on the glass substrate.

Brief Description of the Related Art

[0003] As is well known, microelectronic devices have a tendency to be minimized and thinned with its functional development and a semiconductor package mounted on a mother board is also following the tendency in order to realize a mounting of high integration.

[0004] When the geometric dimensions of the Integrated Circuits are scaled down, the cost per

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die is decreased while some aspects of performance are improved. The metal connections which connect the Integrated Circuit to other circuit or system components become of relative more importance and have, with the further miniaturization of the IC, an increasingly negative impact on the circuit performance. The parasitic capacitance and resistance of the metal interconnections increase, which degrades the chip performance significantly. Of most concern in this respect is the voltage drop along the power and ground buses and the RC delay of the critical signal paths. Attempts to reduce the resistance by using wider metal lines result in higher capacitance of these wires.

[0005] To solve this problem, the approach has been taken to develop low resistance metal (such as copper) for the wires while low dielectric materials are used in between signal lines.

[0006] Increased Input-Output (IO) combined with increased demands for high performance, and then IC's has led to the development of flip-chip Packages. Flip-chip technology fabricates bumps (typically Pb/Sn solders) on Al pads of chip and interconnects the bumps directly to the package media, which are usually ceramic or plastic based. The flip-chip is bonded face down to the package medium through the shortest path. These technologies can be applied not only to single-chip packaging, but also to higher or integrated levels of packaging in which the packages are larger and to more sophisticated substrates that accommodate several chips to form larger functional units.

[0007] The flip-chip technique, using an area array, has the advantage of achieving the highest density of interconnection to the device and a very low inductance interconnection to the package. However, pre-testability, post-bonding visual inspection, and TCE (Temperature Coefficient of Expansion) matching to avoid solder bump fatigue are still challenges.

[0008] Glass can be used as an interposer to bridge between one or more IC chips and a printed circuit board. In many respects, when used as an interposer / substrate and without the requirement

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for active devices, glass can be a good substitute for a silicon interposer. The advantages of glass in comparison to silicon as an interposer lie in its much lower material cost. Glass also has a CTE closely matched to silicon, so that reliability of interconnects, especially micro-bonds, can be expected to be quite good. Glass has some disadvantages in comparison to silicon – notably its lower thermal conductivity and the difficulty in forming Through Glass Vias (TGV's). Both of these topics are discussed elsewhere in this patent.

SUMMARY OF THE DISCLOSURE

[0009] Embodiments of the present disclosure provide A display device comprises a display panel substrate and a glass substrate over said display panel substrate, wherein said display panel substrate comprises multiple contact pads, a display area, a first boundary, a second boundary, a third boundary and a fourth boundary, wherein said display area comprises a first edge, a second edge, a third edge and a fourth edge, wherein said first boundary is parallel to said third boundary and said first and third edges, wherein said second boundary is parallel to said fourth boundary and said second and fourth edges, wherein a first least distance between said first boundary and said first edge, wherein a second least distance between said second boundary and said second edge, a third least distance between said third boundary and said third edge, a fourth distance between said fourth boundary and said fourth edge, and wherein said first, second, third and fourth least distances are smaller than 100 micrometers, and wherein said glass substrate comprising multiple metal conductors through in said glass substrate and multiple metal bumps are between said glass substrate and said display panel substrate, wherein said one of said metal conductors is connected to one of said contact pads through one of said metal bumps.

[0010] These, as well as other components, steps, features, benefits, and advantages of the present disclosure, will now become clear from a review of the following detailed description of

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illustrative embodiments, the accompanying drawings, and the claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] The drawings disclose illustrative embodiments. They do not set forth all embodiments. Other embodiments may be used in addition or instead. Details that may be apparent or unnecessary may be omitted to save space or for more effective illustration. Conversely, some embodiments may be practiced without all of the details that are disclosed. When the same numeral appears in different drawings, it refers to the same or like components or steps.

[0012] Aspects of the disclosure may be more fully understood from the following description when read together with the accompanying drawings, which are to be regarded as illustrative in nature, and not as limiting. The drawings are not necessarily to scale, emphasis instead being placed on the principles of the disclosure.

[0013] Figs. 1 illustrates a three-dimensional view of a X-axis nets and a Y-axis nets, in accordance with the present disclosure.

[0014] Fig. 2 illustrates a cross-section view of the X-axis nets and the Y-axis nets, in accordance with the present disclosure.

[0015] Fig. 3 illustrates a cross-section view of the Z-axis traces crossed to the X-axis nets and the Y-axis nets, in accordance with the present disclosure.

[0016] Fig. 4 illustrates a three-dimensional view of the Z-axis traces, X-axis nets and the Y-axis nets, in accordance with the present disclosure.

[0017] Figs. 5a-5i illustrate the shape and structure of the Z-axis traces, in accordance with the present disclosure.

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[0018] Figs. 6a-6j illustrate a 1st process of forming a glass substrate, in accordance with the present disclosure.

[0019] Figs. 6k-6n illustrate a top views of the 1st process of forming the glass substrate, in accordance with the present disclosure.

[0020] Figs. 7a-7o illustrate a 2nd process of forming the glass substrate, in accordance with the present disclosure.

[0021] Figs. 7p-7r illustrate a top views of the 2nd process of forming the glass substrate, in accordance with the present disclosure.

[0022] Figs. 8a-8d illustrate cross-section views of the glass substrate and the metal plug, in accordance with the present disclosure.

[0023] Figs. 9a-9s illustrate a process to form multiple traces on a top surface and a bottom surface of the glass substrate, in accordance with the present disclosure.

[0024] Figs. 9t-9u illustrate cross-section views of multiple chips formed on the glass substrate, in accordance with the present disclosure.

[0025] Fig. 9v illustrates a cross-section view of the metal bump, in accordance with the present disclosure.

[0026] Fig. 9w illustrates a cross-section view of multiple chips formed on a top surface and bottom surface of the glass substrate, in accordance with the present disclosure.

[0027] Fig. 9x illustrates a cross-section view of multiple chips and a 3D-IC package formed on a top surface and bottom surface of the glass substrate, in accordance with the present disclosure.

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[0028] Fig. 9y illustrates a top views of the multiple chips on the glass substrate, in accordance with the present disclosure.

[0029] Figs. 10a-10j illustrate a damascene process to form the metal layer on the glass substrate, in accordance with the present disclosure.

[0030] Figs. 11a-11i illustrate an embossing process to form the metal layer on the glass substrate, in accordance with the present disclosure.

[0031] Fig. 12 illustrates a cross-section view of the glass substrate of the first application formed on an OLED display substrate, in accordance with the present disclosure.

[0032] Fig. 13 illustrates a cross-section view of the glass substrate of the second application formed on a MEMs display substrate, in accordance with the present disclosure.

[0033] Fig. 14 illustrates a cross-section view of the glass substrate of the third application formed on a LCD display substrate, in accordance with the present disclosure.

[0034] Fig. 15 illustrates a cross-section view of the glass substrate of the fourth application formed on an another LCD display substrate, in accordance with the present disclosure.

[0035] Fig. 16 illustrates a cross-section view of the glass substrate of the fifth application formed on an OLED display substrate, in accordance with the present disclosure.

[0036] Fig. 17a illustrates a cross-section view of the glass substrate of the sixth application formed on an OLED display substrate, in accordance with the present disclosure.

[0037] Fig. 17b illustrates a cross-section view of the structure of the OLED display substrate, in accordance with the present disclosure.

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[0038] Fig. 18 illustrates a three-dimensional view of the display device, in accordance with the present disclosure.

[0039] Fig. 19 illustrates a big display device combined from multiple display device, in accordance with the present disclosure.

[0040] While certain embodiments are depicted in the drawings, one skilled in the art will appreciate that the embodiments depicted are illustrative and that variations of those shown, as well as other embodiments described herein, may be envisioned and practiced within the scope of the present disclosure.

DETAILED DESCRIPTION OF THE DISCLOSURE

[0041] Fig. 1 illustrates a three-dimensional view of a net 2, 4, wherein the net 4 is under the net 2, wherein the net 2 comprises multiple Y-axis traces 2a and multiple X-axis traces 2b under the Y-axis traces 2a, and wherein the net 4 comprises multiple Y-axis traces 4a and multiple X-axis traces 4b under the Y-axis traces 4a. Multiple gaps 3and 5 are formed in the net 2 and 4. Each of the traces 2a, 2b, 4a and 4b is easily moved to change the size of gaps 3 and gaps 5. The diameter (or width) of traces 2a, 2b, 4a and 4b are the same, such as between 10 and 30 micrometers, between 20 and 100 micrometers, between 40 and 150 micrometers, between 50 and 200 micrometers, between 200 and 1000 micrometers or between 500 and 10000 micrometers. The traces 2a, 2b, 4a and 4b may be metal traces or polymer traces, such as copper traces, copper-gold alloy traces, copper-gold-palladium alloy traces, copper-gold-silver alloy traces, copper-platinum alloy traces, copper-iron alloy traces, copper-nickel alloy traces, copper-tungsten traces, tungsten traces, brass wires, zinc plated brass wires, stainless wires, nickel plated stainless wires, phosphor bronze wires, copper plated the aluminum wires, aluminum traces, phenolic resin traces, epoxy resin traces, melamine-

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formaldehyde resin traces or polysiloxanes resin traces. The cross-section shape of traces 2a, 2b, 4a and 4b may be a circular shape, a Square shape, an oblong shape, a rectangle shape or a flat shape.

[0042] Fig. 2 illustrates a cross-section view of the net 2 and the net 4. The gaps 3 and gaps 5 are aligned with each other.

[0043] Next, referring to Fig. 3, multiple metal traces 6 are crossed the net 2 and the net 4 through the gaps 3 and gaps 5. The diameter (or width) of metal traces 6 is between 10 and 30 micrometers, between 20 and 100 micrometers, between 40 and 150 micrometers, between 50 and 200 micrometers, between 200 and 1000 micrometers or between 500 and 10000 micrometers. The traces 6 may be metal traces, such as copper traces, copper-gold alloy traces, copper-gold-palladium alloy traces, copper-gold-silver alloy traces, copper-platinum alloy traces, copper-iron alloy traces, copper-nickel alloy traces, copper-tungsten traces, tungsten traces, brass wires, zinc plated brass wires, stainless wires, nickel plated stainless wires, phosphor bronze wires, copper plated the aluminum wires, aluminum traces, titanium-containing layer plated the copper wires, tantalum-containing layer plated the copper wires. The cross-section shape of traces 6 may be a circular shape, a square shape, an oblong shape, a rectangle shape or a flat shape. The diameter (or width) of traces 6 may be the same with the traces 2a, 2b, 4a and 4b or different with the traces 2a, 2b, 4a and 4b.

[0044] Furthermore, we proposed the material of the traces 6 is copper-tungsten alloy, wherein the copper in the copper-tungsten alloy is 50 percent and the tungsten in the copper-tungsten alloy is 50 percent, the copper in the copper-tungsten alloy is 60 percent and the tungsten in the copper-tungsten alloy is 40 percent, the copper in the copper-tungsten alloy is 70 percent and the tungsten in the copper-tungsten alloy is 30 percent, the copper in the copper-tungsten alloy is 80 percent and the tungsten in the copper-tungsten alloy is 20 percent, the copper in the copper-tungsten alloy is 90 percent and the tungsten in the copper-tungsten alloy is 10 percent, the copper in the copper-

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tungsten alloy is 40 percent and the tungsten in the copper-tungsten alloy is 60 percent, the copper in the copper-tungsten alloy is 30 percent and the tungsten in the copper-tungsten alloy is 70 percent.

[0045] Fig. 4 illustrates a three-dimensional view of a net 2, 4 and traces 6.

[0046] Fig. 5a-5i illustrate the shape and structure of the traces 6. In Fig. 5a, the cross-section shape of traces 6 is a circular shape. In Fig. 5d, the cross-section shape of traces 6 is a square shape. In Fig. 5g, the cross-section shape of traces 6 is a rectangle shape. In Fig. 5b, the cross-section shape of traces 6 is a circular shape and a first covering layer 6a is cover on the traces 6, wherein the first covering layer 6a may be a metal layer, such as a nickel-containing layer, a zinc-containing layer, a titanium-containing layer, a tantalum-containing layer, a silver-containing layer, a chromium-containing layer and wherein the first covering layer 6a may be an anti-oxidation layer, such as an oxide-containing layer. In Fig. 5e, the cross-section shape of traces 6 is a square shape and a first covering layer 6a is cover on the traces 6, wherein the first covering layer 6a may be a metal layer, such as a nickel-containing layer, a zinc-containing layer, a titanium-containing layer, a tantalum-containing layer, a silver-containing layer, a chromium-containing layer and wherein the first covering layer 6a may be an anti-oxidation layer, such as an oxide-containing layer. In Fig. 5h, the cross-section shape of traces 6 is a rectangle shape and a first covering layer 6a is cover on the traces 6, wherein the first covering layer 6a may be a metal layer, such as a nickel-containing layer, a zinc-containing layer, a titanium-containing layer, a tantalum-containing layer, a silver-containing layer, a chromium-containing layer and wherein the first covering layer 6a may be an anti-oxidation layer, such as an oxide-containing layer. In Fig. 5c, the cross-section shape of traces 6 is a circular shape and a second covering layer 6b is cover on the first covering layer 6a, wherein the second covering layer 6b may be an adhesion layer, such as a nickel-containing layer, a zinc-containing layer, a titanium-containing layer, a tantalum-containing layer, a silver-containing layer, a chromium-containing layer and wherein the first covering layer 6a may be an anti-oxidation layer, such as an

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oxide-containing layer. In Fig. 5f, the cross-section shape of traces 6 is a square shape and a second covering layer 6b is cover on the first covering layer 6a, wherein the second covering layer 6b may be an adhesion layer, such as a nickel-containing layer, a zinc-containing layer, a titanium-containing layer, a tantalum-containing layer, a silver-containing layer, a chromium-containing layer and wherein the first covering layer 6a may be an anti-oxidation layer, such as an oxide-containing layer. In Fig. 5i, the cross-section shape of traces 6 is an oblong shape and a second covering layer 6b is cover on the first covering layer 6a, wherein the second covering layer 6b may be an adhesion layer, such as a nickel-containing layer, a zinc-containing layer, a titanium-containing layer, a tantalum-containing layer, a silver-containing layer, a chromium-containing layer and wherein the first covering layer 6a may be an anti-oxidation layer, such as an oxide-containing layer.

[0047] Next, Figs. 6a-6j are illustrated a 1st process of forming a glass substrate of the invention. Please referring to Fig. 6a, the traces 6 are stretched to a suitable length L1, e.g., smaller than 5 meters, such as between 0.5 and 1 meter, or between 1 and 3 meters. At the same time, the net 4 is moved down to a suitable location. The pitch t1 between the traces 2a, 2b, 4a, 4b is greater than the diameter (or width) of traces 6.

[0048] Next, referring to Fig. 6b, the traces 2a, 2b, 4a and 4b are moved to change the pitch t1 to a pitch t2, then the traces 6 are closed up to a pitch t3. The pitch t3 substantially the same with the diameter (or width) of the traces 2a, 2b, 4a and 4b, such as between 5 and 20 micrometers, between 20 and 50 micrometers, between 30 and 80 micrometers, between 20 and 100 micrometers, between 40 and 150 micrometers, between 50 and 200 micrometers, between 200 and 1000 micrometers or between 500 and 10000 micrometers. At the same time, maybe applied a force to stretch the traces 6, 2a, 2b, 4a and 4b and make the traces 6 keep strength and keep the pitch t3 fixed.

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[0049] Next, referring to Fig. 6c, a thermal resistance layer 8 is formed on surfaces of the net 4. The thermal resistance layer 8 may be a polymer layer, such as a thermosetting resin, phenolic resin, epoxy resin, melamine-formaldehyde resin, polysiloxanes resin, plaster layer, wherein the thermal resistance layer 8 has a heat deflection temperature between 400 and 900 ℃. When a liquid thermal resistance layer 8 formed on the net 4 and the thermal resistance layer 8 permeated the net 4 through the gaps 5, wherein the thermal resistance layer 8 covers the gaps 5 between traces 4a, traces 4b and traces 6, then curing the thermal resistance layer 8. The thermal resistance layer 8 has a thickness between 0.05 and 1 meter.

[0050] Next, referring to Fig. 6d, a mold 10 is provided between the net 2 and the net 4, wherein the mold 10 surrounds the traces 6 and on the thermal resistance layer 8. The mold 10 is held up by a machine or a device. The mold 10 may be a metal mold, a ceramics mold or a polymer mold, which has a heat deflection temperature between 400 ℃ and 900 ℃ or between 800 ℃ and 1300 ℃.

[0051] Next, referring to Fig. 6e, a fixed layer 12 is formed on the thermal resistance layer 8, wherein the fixed layer 12 may be a glass layer or a polymer layer. When the material of the fixed layer 12 is glass, the fixed layer 12 is a high temperature liquid to form on the thermal resistance layer 8, and then the fixed layer 12 down to a suitable temperature becomes a solid state. The fixed layer 12 has a thickness between 0.01 and 1 meter. The bottom of traces 6 is fixed by the fixed layer 12.

[0052] Next, referring to Fig. 6f, the traces 6 under the net 4 are cut. A tank 14 carries the mold 10, net 4 and the fixed layer 12.

[0053] Next, referring to Fig. 6g, a glass layer (liquid form) 16 is formed on the fixed layer 12. The glass layer 16 is a high temperature liquid to form on the fixed layer 12 and fill in the mold 10, and then the glass layer 16 down to a suitable temperature becomes a solid state, wherein the glass

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layer 16 has a glass transition temperature between 300°C and 900°C, between 500°C and 800°C, between 900°C and 1200°C or between 1000°C and 1800°C. The glass layer 16 is a low melting point glass material, wherein the glass layer 16 has a melting point between 300°C and 900°C, 800°C and 1300°C, between 900°C and 1600°C, between 1000°C and 1850°C, or between 1000°C and 2000°C, wherein the melting point may smaller than 1500°C. The glass layer 16 has a thickness greater than 0.5 meters or greater than 0.1 meter. Furthermore, there is a few bubbles or no bubble in glass layer 16, for example, there is zero to 3 bubbles in one cubic meter of the glass layer 16, 1 to 10 bubbles in one cubic meter of the glass layer 16, 5 to 30 bubbles in one cubic meter of the glass layer 16 or 20 to 60 bubbles in one cubic meter of the glass layer 16, wherein the bubble has a diameter between 0.0001 and 0.001 centimeters, between 0.001 and 0.05 centimeters, between 0.05 and 0.1 centimeters or between 0.05 and 0.5 centimeters. The glass layer 16 may be removed bubbles through multiple processes of a laminating process, a squeezing process and a heating process.

[0054] The glass layer 16 refers to an amorphous solid. The material of the glass layer 16 may be included soda-lime glass, boro-silicate glass, alumo-silicate glass, fluoride glasses, phosphate glasses or chalcogen glasses. For example, the composition of the soda-lime glass comprises SiO_2 (74%), Na_2O (13%), CaO (10.5%), Al_2O_3 (1.3%), K_2O (0.3%), SO3 (0.2%), MgO (0.2%), Fe2O3 (0.04%), TiO2 (0.01%), the composition of the boro-silicate glass comprises SiO_2 (81%), B_2O_3 (12%), Na_2O (4.5%), Al_2O_3 (2.0%), the composition of the phosphate glasses comprises a percentage of the P_2O_5 material between 3% and 10% or between 5% and 20%.

[0055] A glass, once formed into a solid body, is capable of being softened and perhaps remitted into a liquid form. The "glass transition temperature" of a glass material is a temperature below which the physical properties of the glass are similar to those of a solid and above which the glass material behaves like a liquid.

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[0056] If a glass is sufficiently below the glass transition temperature, molecules of the glass may have little relative mobility. As a glass approaches the glass transition temperature, the glass may begin to soften and with increasing temperature, the glass will ultimately melt into the liquid state. Thus, a glass body may be softened to an extent sufficient to enable manipulation of the body's shape, allowing for the formation of holes or other features in the glass body. Once the desired form is obtained, glass is usually annealed for the removal of stresses. Surface treatments, coatings or lamination may follow to improve the chemical durability (glass container coatings, glass container internal treatment), strength (toughened glass, bulletproof glass, windshields), or optical properties (insulated glazing, anti-reflective coating).

[0057] Furthermore, the glass layer 16 may be replaced by a polymer layer. When the polymer layer cured to a solid state, then the polymer layer has a coefficient of expansion between 3 and 10 ppm/°C.

[0058] Next, referring to Fig. 6h, the mold 10 and the tank 14 are removed and cut the traces 6 from net 2.

[0059] Next, referring to Fig. 6i, the net 4 and the thermal resistance layer 8 are removed, and then a column 25 is produced.

[0060] Next, referring to Fig. 6j, the traces 6 out of the column 25 are removed and cutting the column 25 to produce multiple first substrates 20, wherein the first substrate 20 has a thickness between 20 and 100 micrometers, between 50 and 150 micrometers, between 100 and 300 micrometers or between 150 and 2000 micrometers or greater than 1000 micrometers. The first substrates 20 may be made a planarization process using a suitable process, such as a chemical mechanical polishing (CMP) procedure, mechanical grinding, or laser drilling

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[0061] Next, referring to Fig. 6k, the first substrate 20 comprises multiple second substrates 22. The second substrates 22 are well-regulated an array in the first substrate 20. Each of the second substrates22 has multiple metal plugs 21, wherein the metal plug 21 is formed from metal traces 6. The metal plug 21 has the same material and structure with metal trace 6.

[0062] Next, referring to Figs. 6l-6n, the metal plugs 21 may be arranged in different types, such as Fig. 6l, the metal plugs 21 are arranged on the side portions of the second substrate 22, or such as Fig. 6m, the metal plugs 21 are arranged on the side portions and center portion of the second substrate 22, or such as Fig. 6n, some portions of the second substrate 22 are not arranged the metal plugs 21.

[0063] Figs. 7a-7m are illustrated a 2nd process of forming a glass substrate of the invention. Please referring to Fig. 7a-7b, there is illustrated a first metal plate 7 in Fig. 7a, illustrated a three-dimensional view of the first metal plate 7 in Fig. 7b. The first metal plate 7 has a thickness between 25 micrometers and 1000 micrometers, between 20 micrometers and 500 micrometers, between 30 micrometers and 400 micrometers or between 20 micrometers and 250 micrometers. The first metal plate 7 comprising a first portion 71, a second portion 73 and a third portion 75 between the first portion 71 and second portion 73, wherein the third portion 75 comprises multiple non-circular metal traces 752 are connected to the first portion 71 and the second portion 73, wherein a cross-section view of the non-circular trace 752 comprising a square shape or a rectangle shape. One of the non-circular traces 752 has a width greater than the thickness of one of the non-circular traces 752, such as between 150 micrometers and 3000 micrometers, between 300 micrometers and 1500 micrometers, between 200 micrometers and 800 micrometers or between 100 micrometers and 500 micrometers. Multiple gaps 754 are between each two neighboring non-circular traces 752, wherein the gap 754 is between 50 micrometers and 3000 micrometers, between 300 micrometers and 1500 micrometers, between 200 micrometers and 800 micrometers or between 150 micrometers and 500

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micrometers. The first metal plate 7 comprises a copper metal layer, copper-gold alloy metal layer, copper-gold-palladium alloy metal layer, copper-gold-silver alloy metal layer, copper-platinum alloy metal layer, copper-iron alloy metal layer, copper-nickel alloy metal layer, copper-tungsten metal layer, tungsten metal layer, brass metal layer, zinc plated brass metal layer, stainless metal layer, nickel plated stainless metal layer, phosphor bronze metal layer, copper plated the aluminum metal layer or aluminum metal layer. There are two holes 71a in the first portion 71, wherein the hole 71a has a diameter between 600 micrometers and 2000 micrometers, between 1000 micrometers and 3000 micrometers or between 2000 micrometers and 5000 micrometers. There are two holes 73a corresponding to the hole 71a in the first portion 71, wherein the hole 73a has a diameter between 600 micrometers and 2000 micrometers, between 1000 micrometers and 3000 micrometers or between 2000 micrometers and 5000 micrometers, wherein a first least distance between the two holes 71a is substantially the same to a second least distance between the two holes 73a.

[0064] Next, referring to Figs. 7c-7d, there is illustrated a second metal plate 9 in Fig. 7c, illustrated a three-dimensional view of the second metal plate 9 in Fig. 7d. The second metal plate 9 has a thickness between 25 micrometers and 600 micrometers, between 20 micrometers and 300 micrometers, between 30 micrometers and 250 micrometers or between 25 micrometers and 180 micrometers. There are two holes 90a in the second metal plate 9, wherein the hole 90a has a diameter between 600 micrometers and 2000 micrometers, between 1000 micrometers and 3000 micrometers or between 2000 micrometers and 5000 micrometers, wherein a third least distance between the two holes 90a is substantially the same to a second least distance between the two holes 73a and substantially the same to the first least distance between the two holes 71a. The second metal plate 9 comprises a copper metal layer, copper-gold alloy metal layer, copper-gold-palladium alloy metal layer, copper-gold-silver alloy metal layer, copper-platinum alloy metal layer, copper-iron alloy metal layer, copper-nickel alloy metal layer, copper-tungsten metal layer, tungsten metal

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layer, brass metal layer, zinc plated brass metal layer, stainless metal layer, nickel plated stainless metal layer, phosphor bronze metal layer, copper plated the aluminum metal layer or aluminum metal layer.

[0065] Next, referring to Fig. 7e, there is illustrated a three-dimensional view of a third metal plate 11 in Fig. 7e. The third metal plate 11 has a thickness between 25 micrometers and 600 micrometers, between 20 micrometers and 300 micrometers, between 30 micrometers and 250 micrometers or between 25 micrometers and 180 micrometers. There are four holes 110a, 112a, 114a, 116a in the third metal plate 11, wherein the hole 110a, 112a, 114a, 116a have a diameter between 600 micrometers and 2000 micrometers, between 1000 micrometers and 3000 micrometers or between 2000 micrometers and 5000 micrometers, wherein a fourth least distance between the hole 110a and hole 112a and a fifth least distance between the hole 114a and hole 116a are substantially the same to a second least distance between the two holes 73a and substantially the same to the first least distance between the two holes 71a. The third metal plate 11 comprises a copper metal layer, copper-gold alloy metal layer, copper-gold-palladium alloy metal layer, copper-gold-silver alloy metal layer, copper-platinum alloy metal layer, copper-iron alloy metal layer, copper-nickel alloy metal layer, copper-tungsten metal layer, tungsten metal layer, brass metal layer, zinc plated brass metal layer, stainless metal layer, nickel plated stainless metal layer, phosphor bronze metal layer, copper plated the aluminum metal layer or aluminum metal layer.

[0066] Next, referring to Fig. 7f-Fig.7i, providing two bolts 130, 132 pass through two holes 150a of a fixing metal plate 150 and providing two bolts 134, 136 pass through two holes 152a of a fixing metal plate 152 respectively. Next, the bolts 130, 132, 134, 136 are passing through the holes 110a, 112a, 114a, 116a of the third metal plate 11 respectively and the third metal plate 11 is formed on the fixing metal plate 150 and the fixing metal plate 152. Next, the bolts 130, 132 are passing through the hole 90a of the second metal plate 9 and the bolts 134, 136 are passing through the hole

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90a of another the second metal plate 9, then the second metal plates 9 are formed on the third metal plate 11. Next, the bolts 130, 132, 134, 136 are passing through the holes 71a, 73a of the first metal plate 7 respectively and the first metal plate 7 is formed on the second metal plates 9. Next, repeating to site another the second metal plates 9 on another the first metal plate 7 sequentially until to expose a top of the bolts 130, 132, 134, 136. Next, the top of the bolts 130, 132, 134, 136 are passing through the holes 110a, 112a, 114a and 116a of another the third metal plate 11 respectively and the third metal plate 11 is formed on the second metal plates 9. Next, the top of the bolts 130, 132 are passing through two holes 150a of another the fixing metal plate 150 and the top of the bolts 134, 136 are passing through two holes 152a of another the fixing metal plate 152 respectively, then the fixing metal plates 150, 152 are formed on the third metal plate 11. Finally, providing four sleeve nuts 17 lock on the top of the bolts 130, 132, 134, 136. Then, multiple the first metal plates 7, multiple the second metal plates 9, two the third metal plates 11, two fixing metal plates 150 and two fixing metal plates 152 forming a metal trace block 19.

[0067] Next, referring to Fig. 7j the metal trace block 19 is put in a mold 23. The mold 23 may be a metal mold, a ceramics mold or a polymer mold, which has a heat deflection temperature between 400 ℃ and 900 ℃ or between 800 ℃ and 1300 ℃. The mold 23 comprises a gas inlet 23a and a liquid input 23b, wherein the gas inlet 23a is used to input N_2 gas and the liquid input 23b is used to input the liquid form glass layer.

[0068] Next, referring to Fig. 7k, the glass layer (liquid form) 16 fill in the mold 23. The glass layer 16 is a high temperature liquid and fill in the mold 23, and then the glass layer 16 down to a suitable temperature becomes a solid state, wherein the glass layer 16 has a glass transition temperature between 300°C and 900°C, between 500°C and 800°C, between 900°C and 1200°C or between 1000°C and 1800°C. The glass layer 16 is a low melting point glass material, wherein the glass layer 16 has a melting point between 300°C and 900°C, 800°C and 1300°C, between 900°C

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and 1600°C, between 1000°C and 1850°C, or between 1000°C and 2000°C, wherein the melting point may smaller than 1500°C. Furthermore, there is a few bubbles or no bubble in glass layer 16, for example, there is zero to 3 bubbles in one cubic meter of the glass layer 16, 1 to 10 bubbles in one cubic meter of the glass layer 16, 5 to 30 bubbles in one cubic meter of the glass layer 16 or 20 to 60 bubbles in one cubic meter of the glass layer 16, wherein the bubble has a diameter between 0.0001 and 0.001 centimeters, between 0.001 and 0.05 centimeters, between 0.05 and 0.1 centimeters or between 0.05 and 0.5 centimeters. The glass layer 16 may be removed bubbles through multiple processes of a laminating process, a squeezing process and a heating process.

[0069] Next, referring to Fig. 7l, the mold 23is removed and cut the glass layer 16 along a cutting line 16a to remove the fixing metal plate 150, the fixing metal plate 152, the first portion 71 of the first metal plate 7, the second portion 73 of the first metal plate 7 and two the third metal plates 11, and then the column 25 is produced, showed in the Fig. 7m.

[0070] Next, referring to Fig. 7n, cutting the column 25 to produce multiple first substrates 20, wherein the first substrate 20 has a thickness between 20 and 100 micrometers, between 50 and 150 micrometers, between 100 and 300 micrometers or between 150 and 2000 micrometers or greater than 1000 micrometers. The first substrates 20 may be made a planarization process using a suitable process, such as a chemical mechanical polishing (CMP) procedure, mechanical grinding, or laser drilling.

[0071] Next, referring to Fig. 7o, the first substrate 20 comprises multiple second substrates 22. The second substrates 22 are well-regulated an array in the first substrate 20. Each of the second substrates has multiple metal plugs 21, wherein the metal plug 21 is formed from the non-circular metal traces 752. The metal plug 21 has the same material, structure and shape with the non-circular metal traces 752. A first pitch 21a and a second pitch 21b are between the metal plugs 21, wherein

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the first pitch 21a is controlled or the same-2 by a distance of the gap 754 and wherein the second pitch 21b is controlled by a distance of adjacent the non-circular traces 752.

[0072] Next, referring to Figs. 7p-7r, the metal plugs 21 may be arranged in different types, such as Fig. 7p, the metal plugs 21 are arranged on the side portions of the second substrate 22, or such as Fig. 7q, the metal plugs 21 are arranged on the side portions and center portion of the second substrate 22, or such as Fig. 7r, some portions of the second substrate 22 are not arranged the metal plugs 21.

[0073] Fig. 8a illustrates a cross-section view of the second substrate 22 illustrates a cross-section view of the metal plug 21. The second substrate 22 comprises an amorphous solid glass layer/body 16 and multiple metal plugs 21, wherein the amorphous solid glass layer/body 16 having a top surface and an opposing bottom surface and the metal plugs 21 extending through the amorphous solid glass layer/body 16 beginning at the top surface and ending at the bottom surface. The top surface of the metal plugs 21 are the same area as the bottom surface of the metal plugs 21.

[0074] Please referring Fig. 8b, the top surface of the metal plugs 21 and the top surface of the amorphous solid glass layer/body 16 are substantially coplanar. The bottom surface of the metal plugs 21 and the bottom surface of the amorphous solid glass layer/body 16 are substantially coplanar.

[0075] Please referring Fig. 8c, the top surface of the metal plugs 21 comprises a top surface of the metal traces 6/ metal traces 752 and a top surface of the first covering layer 6a are substantially coplanar with the top surface of the amorphous solid glass layer/body 16. The bottom surface of the metal plugs 21 comprises a bottom surface of the metal traces 6/ metal traces 752 and a bottom surface of the first covering layer 6a are substantially coplanar with the bottom surface of the amorphous solid glass layer/body 16.

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[0076] Please referring Fig. 8d, the top surface of the metal plugs 21 comprises a top surface of the metal traces 6/ metal traces 752, a top surface of the first covering layer 6a and a top surface of the second covering layer 6b are substantially coplanar with the top surface of the amorphous solid glass layer/body 16. The bottom surface of the metal plugs 21 comprises a bottom surface of the metal traces 6/ metal traces 752, a bottom surface of the first covering layer 6a and a bottom surface of the second covering layer 6b are substantially coplanar with the bottom surface of the amorphous solid glass layer/body 16.

[0077] Fig. 9a-Fig. 9t illustrate a process to form multiple traces on a top surface and a bottom surface of the first substrate 20.

[0078] Next, referring to Fig. 9a, a first dielectric layer 24 is formed on the top surface of the first substrate 20, wherein the first dielectric layer 24 may include or maybe a layer of silicon oxide (such as SiO_2), silicon nitride (such as Si_3N_4), silicon oxynitride (such as SiON), silicon oxycarbide (such as SiOC), phosphosilicate glass (PSG), silicon carbon nitride (such as SiCN), low k dielectric layer (K between 0.5 and 3), or polymer (such as polyimide, benzocyclobutene (BCB), polybenzoxazole (PBO), poly-phenylene oxide (PPO), epoxy, or silosane). The first dielectric layer 24 may be formed or deposited using a suitable process. The first dielectric layer 24 has a thickness between 0.3 and 5 micrometers, between 2 and 10 micrometers, between 1 and 30 micrometers or greater than 30 micrometers.

[0079] Next, referring to Fig. 9b, multiple openings 24a are formed in the first dielectric layer 24 to expose the metal plugs 21. The openings 24a may be formed in the first dielectric layer 24 by a suitable process, such as etching. The opening 24a has a width between 0.3 and 3 micrometers, between 0.5 and 8 micrometers, between 2 and 20 micrometers or between 2 and 50 micrometers.

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[0080] Next, referring to Fig. 9c, a first metal layer 26 is formed on the first dielectric layer 24, on the metal plugs 21 and in the openings 24a. The first metal layer 26 may include an adhesion/barrier layer, such as a layer of titanium, a titanium-tungsten alloy, titanium nitride, chromium, tantalum, tantalum nitride, nickel or nickel vanadium formed using a suitable process, such as a vacuum deposition, a Physical Vapor Deposition (PVD), a Plasma Enhanced Chemical Vapor Deposition (PECVD), a sputtering process or an electroplating process, with a thickness, e.g., between 1 nanometer and 2 micrometers, between 0.3 and 3 micrometers or between 0.5 and 10 micrometers.

[0081] Next, referring to Fig. 9d, a second metal layer 28 is formed on the first metal layer 26. The second metal layer 28 maybe comprises copper, nickel, gold or aluminum formed using a suitable process, such as a vacuum deposition, a Physical Vapor Deposition (PVD), a Plasma Enhanced Chemical Vapor Deposition (PECVD), a sputtering process or an electroplating process, with a thickness, e.g., between 1 nanometer and 5 micrometers, between 1 and 5 micrometers or between 5 and 30 micrometers.

[0082] Next, referring to Fig. 9e, a photoresist layer 30 is formed on the second metal layer 28 by using a suitable process, such as a spin coating process or a lamination process. Next, a photo exposure process using a 1X stepper and a development process using a chemical solution can be employed to form multiple openings 30a, exposing the second metal layer 28, in the photoresist layer. The photoresist layer 30 may have a thickness, e.g., between 3 and 50 micrometers, wherein the photoresist layer 30 may be a positive-type photo-sensitive resist layer or negative-type photo-sensitive resist layer.

[0083] Next, referring to Fig. 9f, remove the first metal layer 26 and the second metal layer 28 are under the openings 30a by using a suitable process, such as an etching process.

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[0084] Next, referring to Fig. 9g, remove the photoresist layer 30 by using a clean process.

[0085] Next, referring to Fig. 9h, a second dielectric layer 32 is formed on the first dielectric layer 24 and on the second metal layer 28, wherein the second dielectric layer 32 may include or may be a layer of silicon oxide (such as SiO_2), silicon nitride (such as Si_3N_4), silicon oxynitride (such as SiON), silicon oxycarbide (such as SiOC), phosphosilicate glass (PSG), silicon carbon nitride (such as SiCN), low k dielectric layer (K between 0.5 and 3), or polymer (such as polyimide, benzocyclobutene (BCB), polybenzoxazole (PBO), poly-phenylene oxide (PPO), epoxy, or silosane). The second dielectric layer 32 may be formed or deposited using a suitable process. The second dielectric layer 32 has a thickness between 0.3 and 5 micrometers, between 2 and 10 micrometers, between 1 and 30 micrometers or greater than 30 micrometers.

[0086] Next, referring to Fig. 9i, multiple openings 32a are formed in the second dielectric layer 32 to expose the second metal layer 28. The openings 32a may be formed in the second dielectric layer 32 by a suitable process, such as etching. The opening 32a has a width between 0.3 and 3 micrometers, between 0.5 and 8 micrometers, between 2 and 20 micrometers or between 2 and 50 micrometers.

[0087] Next, referring to Fig. 9j, a third metal layer 34 is formed on the second dielectric layer 32, on the second metal layer 28 and in the openings 32a. The third metal layer 34 may include an adhesion/barrier layer, such as a layer of titanium, a titanium-tungsten alloy, titanium nitride, chromium, tantalum, tantalum nitride, nickel or nickel vanadium formed using a suitable process, such as a vacuum deposition, a Physical Vapor Deposition (PVD), a Plasma Enhanced Chemical Vapor Deposition (PECVD), a sputtering process or an electroplating process, with a thickness, e.g., between 1 nanometer and 2 micrometers, between 0.3 and 3 micrometers or between 0.5 and 10 micrometers.

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[0088] Next, referring to Fig. 9k, a fourth metal layer 36 is formed on the third metal layer 34. The fourth metal layer 36 maybe comprises copper, nickel, gold or aluminum formed using a suitable process, such as a vacuum deposition, a Physical Vapor Deposition (PVD), a Plasma Enhanced Chemical Vapor Deposition (PECVD), a sputtering process or an electroplating process, with a thickness, e.g., between 1 nanometer and 5 micrometers, between 1 and 5 micrometers or between 5 and 30 micrometers.

[0089] Next, referring to Fig. 9l, a photoresist layer 38 is formed on the fourth metal layer 36 by using a suitable process, such as a spin coating process or a lamination process. Next, a photo exposure process using a 1X stepper and a development process using a chemical solution can be employed to form multiple openings 38a, exposing the fourth metal layer 36, in the photoresist layer. The photoresist layer 38 may have a thickness, e.g., between 3 and 50 micrometers, wherein the photoresist layer 38 may be a positive-type photo-sensitive resist layer or negative-type photo-sensitive resist layer.

[0090] Next, referring to Fig. 9m, remove the third metal layer 34 and the fourth metal layer 36 are under the openings 38a by using a suitable process, such as an etching process.

[0091] Next, referring to Fig. 9n, remove the photoresist layer 38 by using a clean process.

[0092] Next, referring to Fig. 9o, a third dielectric layer 40 is formed on the second dielectric layer 32 and on the fourth metal layer 36, wherein the third dielectric layer 40 may include or maybe a layer of silicon oxide (such as SiO_2), silicon nitride (such as Si_3N_4), silicon oxynitride (such as SiON), silicon oxycarbide (such as SiOC), phosphosilicate glass (PSG), silicon carbon nitride (such as SiCN), low k dielectric layer (K between 0.5 and 3), or polymer (such as polyimide, benzocyclobutene (BCB), polybenzoxazole (PBO), poly-phenylene oxide (PPO), epoxy, or silosane). The third dielectric layer 40 may be formed or deposited using a suitable process. The third

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dielectric layer 40 has a thickness between 0.3 and 5 micrometers, between 2 and 10 micrometers, between 1 and 30 micrometers or greater than 30 micrometers.

[0093] Next, referring to Fig. 9p, multiple openings 40a are formed in the third dielectric layer 40 to expose the fourth metal layer 36. The openings 40a may be formed in the third dielectric layer 40 by a suitable process, such as etching. The opening 40a has a width between 0.3 and 3 micrometers, between 0.5 and 8 micrometers, between 2 and 20 micrometers or between 2 and 50 micrometers.

[0094] Next, referring to Fig. 9q, a protecting layer 42 is formed in the openings 40a, on the third dielectric layer 40 and on the fourth metal layer 36, which can protect the third dielectric layer 40 not to be damaged and the fourth metal layer 36 not be damaged and oxidized.

[0095] Next, referring to Fig. 9r, repeat the processes of Fig.9a-Fig.9p to form the first dielectric layer 24, the first metal layer 26, the second metal layer 28, the second dielectric layer 32, the third metal layer 34, the fourth metal layer 36 and the third dielectric layer 40 on the bottom surface of the first substrate 20.

[0096] Furthermore, referring to Fig. 9s, a passive device 44 may be formed in the first metal layer 28 and the second metal layer 36, such as an inductor, a capacitor or a resistor.

[0097] Next, referring to Fig. 9t, multiple chips 46 and chips 56 set up over the third dielectric layer 40 through a flip-chip package process or a wire-bonding package process, wherein the chip 46 or 56 comprises may be a memory chip, such as NAND-Flash memory chip, Flash memory chip, DRAM chip, SRAM chip or SDRAM chip, a central-processing-unit (CPU) chip, a graphics-processing-unit (GPU) chip, a digital-signal-processing (DSP) chip, a baseband chip, a wireless local area network (WLAN) chip, a logic chip, an analog chip, a global-positioning-system (GPS)

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chip, a "Bluetooth" chip, or a chip including one or more of a CPU circuit block, a GPU circuit block, a DSP circuit block, a memory circuit block (such as DRAM circuit block, SRAM circuit block, SDRAM circuit block, Flash memory circuit block, or NAND-Flash memory circuit block), a baseband circuit block, a Bluetooth circuit block, a GPS circuit block, a MEMS chip, a COMS image sensor device, a WLAN circuit block, and a modem circuit block, from the semiconductor wafer.

[0098] The chips 46 are set up on the third dielectric layer 40 through a flip-chip package process, wherein the chip 46 comprises multiple metal pads 48 and multiple metal bumps 50 formed on the metal pads 48. The metal pad 48 may be an electroplated copper pad, a damascene copper pad or an aluminum pad. The metal bump 50 comprises an adhesion/barrier metal layer formed on the metal pad 48, an electroplated metal layer or an electro-less metal layer formed on the adhesion/barrier metal layer, wherein the adhesion/barrier metal layer comprises a titanium-containing layer, a chromium-containing layer, a tantalum-containing layer or a nickel layer, and the electroplated metal layer comprises a copper layer, a gold layer, a nickel layer, a tin-containing layer, a solder layer, a solder layer over a nickel layer and a copper layer, and the electro-less layer comprises a copper layer, a gold layer or a nickel layer. The electroplated metal layer has a thickness between 2 and 5 micrometers, between 5 and 30 micrometers or between 10 and 50 micrometers. The metal bumps 50 are connected to the fourth metal layer 36 exposed by the openings 40a through a solder layer 54, wherein the solder layer 54 is formed on the fourth metal layer 36 exposed by the openings 40a or is a portion of the metal bump

[0099] 50. An underfill layer 52 is formed between the chips 46 and the third dielectric layer 40.

[00100] The chips 56 are set up over the third dielectric layer 40 through a polymer adhesion layer 60, wherein the chip 56 comprises multiple metal pads 58. The metal pad 58 may be an

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electroplated copper pad, a damascene copper pad or an aluminum pad. Multiple metal wires 62 are connected to the metal pads 58 and the fourth metal layer 36 exposed by the openings 40a, wherein the metal wires 62 comprises a gold wire, a copper wire, a metal alloy wire, a silver-containing wire, an aluminum-containing wire or gold-copper alloy wire. An underfill layer 64 is covered the chip56, the metal wires 62 and the metal pads 58.

[00101] Multiple discrete passive components 66 set up on the third dielectric layer 40, such as a discrete inductor, a discrete capacitor or a discrete resistor, wherein the discrete passive component 66 comprises a multiple metal pad 68. The discrete passive components 66 mounted on the third dielectric layer 40 through a solder layer 70.

[00102] Next, referring to Fig. 9u, multiple metal bumps 72 are formed on the bottom surface of the substrate 20.

[00103] Fig. 9v is disclosed some structures of metal bump 72.

- Lift side: 1st type of structures of metal bump 72 comprises an adhesion/barrier metal layer 61 formed on the metal pad 48, a metal seed layer 63 formed on the adhesion/barrier metal layer 61, an electroplated metal layer 65 formed on the metal seed layer 63 and a solder layer 67 formed on the electroplated metal layer 65, wherein the adhesion/barrier metal layer 61 comprises a titanium-containing layer, a chromium-containing layer, a tantalum-containing layer or a nickel layer, wherein the first electroplated metal layer 65 comprises a copper layer, a gold layer, a nickel layer, wherein the solder layer 67 can be formed by screen plating, ball mounting, or an electroplating process, such as gold-tin alloy, tin-silver alloy, tin-silver-copper alloy, indium, tin-bismuth alloy, or other lead-free alloy. Lead alloy solders can also be used but may be less desirable in some embodiments due to toxicity considerations. The adhesion/barrier metal layer 61 has a thickness between 0.05 and 2

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micrometers. The metal seed layer 63 has a thickness between 0.05 and 2 micrometers. The first electroplated metal layer 65 has a thickness between 1 and 5 micrometers, between 2 and 8 micrometers or between 5 and 20 micrometers. The solder layer 67 has a thickness between 30 and 80 micrometers, between 50 and 100 micrometers, between 80 and 150 micrometers or between 120 and 350 micrometers.

- Right side: 2nd type of structure of metal bump 72 comprises an adhesion/barrier metal layer 61 formed on the metal pad 48, a metal seed layer 63 formed on the adhesion/barrier metal layer 61, a first electroplated metal layer 65 formed on the metal seed layer 63 and a second electroplated metal layer 69 formed on the first electroplated metal layer 65, wherein the adhesion/barrier metal layer 61 comprises a titanium-containing layer, a chromium-containing layer, a tantalum-containing layer or a nickel layer, wherein the first electroplated metal layer 65 comprises a copper layer, a gold layer, a nickel layer, wherein the second electroplated metal layer 69 comprises a copper layer, a gold layer, a nickel layer. The adhesion/barrier metal layer 61 has a thickness between 0.05 and 2 micrometers. The metal seed layer 63 has a thickness between 0.05 and 2 micrometers. The first electroplated metal layer 65 has a thickness between 1 and 5 micrometers, between 2 and 4 micrometers, between 5 and 15 micrometers or between 10 and 25 micrometers. The second electroplated metal layer 69 has a thickness between 1 and 5 micrometers, between 2 and 4 micrometers, between 10 and 30 micrometers or between 20 and 60 micrometers.

[00104] Furthermore, referring to Fig. 9w, the chips 46 may be set up on the bottom surface of the first substrate 20.

[00105] Furthermore, referring to Fig. 9x, the chip 46 may be replaced a 3D IC chip package, wherein the chip 46 comprises a multiple metal pad 48 formed on the top and bottom surface. The

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metal pads 48 of the top surface of the chip 46 are connected to the metal pads 48 of the bottom surface of the chip 46 through multiple through-silicon-via metal layers. A chip 47 is connected to the 3D IC chip 46 through the flip-chip package process, wherein the chip 47 comprises multiple metal pads 49, wherein the metal pad 49 may be an electroplated copper pad, a damascene copper pad or an aluminum pad. The metal pads 49 are connected to the metal pads 48 through a solder layer 51.

[00106] Fig. 9y, illustrates a top view of the first substrate 20. Fig. 9u-Fig. 9w illustrate a cross-section view of Line L-L' in Fig. 9y. Multiple the chips 46, the chips 56 and the passive components 66 may also be provided in or on the first substrate 20.

[00107] Next, cutting the first substrate 20 to produce multiple second substrates 22.

[00108] Fig. 10a-Fig. 10j illustrate a damascene process to form the first metal layer 26, the second metal layer 28, the third metal layer 34 and the fourth metal layer 36 on a top surface and a bottom surface of the first substrate 20.

[00109] Referring to Fig. 10a, the dielectric layers 24 in Fig. 9a include two dielectric layers 80 and 82. The dielectric layer 80 is formed on the dielectric layer 82 by a chemical vapor deposition (CVD) process or a spin-on coating process, wherein each of the dielectric layers 80 and 82 may be composed of a low-K oxide layer with a thickness of between 0.3 and 5μm, and preferably of between 0.5 and 3μm, and an oxynitride layer on the low-K oxide layer, of a low-K polymer layer with a thickness of between 0.3 and 5μm, and preferably of between 0.5 and 3μm, and an oxynitride layer on the low-K polymer layer, of a low-K oxide layer with a thickness of between 0.3 and 5μm, and preferably of between 0.5 and 3μm, and a nitride layer on the low-K oxide layer, of a low-K polymer layer with a thickness of between 0.3 and 5μm, and preferably of between 0.5 and 3μm, and a nitride layer on the low-K polymer layer, or of a low-K dielectric layer with a

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thickness of between 0.3 and 5μm, and preferably of between 0.5 and 3μm, and a nitride-containing layer on the low-K dielectric layer. Next, referring to Fig. 10b, a photoresist layer 84 is formed on the dielectric layer 82, an opening 84a in the photoresist layer 84 exposing the dielectric layer 82. Next, referring to Fig. 10c, the dielectric layer 82 under the opening 84a is removed by a dry etching method to form a trench in the dielectric layer 82 exposing the dielectric layer 80. Next, referring to Fig. 10d, after forming the trench in the dielectric layer 82, the photoresist layer 84 is removed. Next, referring to Fig. 10e, a photoresist layer 86 is formed on the dielectric layer 82 and on the dielectric layer 80 exposed by the trench, an opening 86a in the photoresist layer 86 exposing the dielectric layer 80 exposed by the trench. Next, referring to Fig. 19f, the dielectric layer 80 under the opening 86a is removed by a dry etching method to form a via 80a in the dielectric layer 80 exposing the metal plugs 21 in the substrate 20. Next, referring to Fig. 10g, after forming the via 80a in the dielectric layer 80, the photoresist layer 86 is removed. Thereby, an opening 88 including the trench and the via 80a is formed in the dielectric layers 82 and 80. Next, referring to Fig. 10h, an adhesion/barrier layer 90 having a thickness of between 0.1 and 3 micrometers is formed on the metal plugs 21 exposed by the opening 88, on the sidewalls of the opening 88 and on the top surface of the dielectric layer 82. The adhesion/barrier layer 90 can be formed by a sputtering process or a chemical vapor deposition (CVD) process. The material of the adhesion/barrier layer 90 may include titanium, titanium nitride, a titanium-tungsten alloy, tantalum, tantalum nitride, or a composite of the abovementioned materials. For example, the adhesion/barrier layer 90 may be formed by sputtering a tantalum layer on the metallization structure exposed by the opening 88, on the sidewalls of the opening 88 and on the top surface of the dielectric layer 82. Alternatively, the adhesion/barrier layer 90 may be formed by sputtering a tantalum-nitride layer on the metallization structure exposed by the opening 88, on the sidewalls of the opening 88 and on the top surface of the dielectric layer 82. Alternatively, the adhesion/barrier layer 90 may be formed by forming a tantalum-nitride layer on the metallization structure exposed by the opening 88, on the sidewalls of

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the opening 88 and on the top surface of the dielectric layer 82 by a chemical vapor deposition (CVD) process. Next, referring to Fig. 10i, a seed layer 92, made of copper, having a thickness of between 0.1 and 3 micrometers is formed on the adhesion/barrier layer 90 using a sputtering process or a chemical vapor deposition (CVD) process, and then a copper layer 94 having a thickness of between 0.5 and 5μm, and preferably of between 1 and 2μm, is electroplated on the seed layer 92. Next, referring to Fig. 10j, the copper layer 94, the seed layer 92 and the adhesion/barrier layer 90 outside the opening 88 in the dielectric layers 82 and 80 are removed using a chemical mechanical polishing (CMP) process until the top surface of the dielectric layer 82 is exposed to an ambient.

[00110] Fig. 11a-Fig. 11i illustrate an embossing process to form the first metal layer 26, the second metal layer 28, the third metal layer 34 and the fourth metal layer 36 on a top surface and a bottom surface of the first substrate 20.

[00111] Referring to Fig. 11a, the metal plugs 21 are in the glass layer 16 of the first substrate 20, and the opening 96a in the dielectric layer 96 exposes the metal plugs 21.

[00112] Referring to Fig. 11a, a polymer layer 98 can be formed on the dielectric layer 96, and at least one opening 98a is formed in the polymer layer 98 by patterning the polymer layer 98 to expose at least one metal trace 6, as shown in Fig. 11b and Fig. 11c. The metal plugs 21 may include a center portion exposed by an opening 98a and a peripheral portion covered with the polymer layer 98, as shown in Fig. 11b. Alternatively, the opening 98a may expose the entire upper surface of the metal plugs 21 exposed by the opening 96a in the dielectric layer 96 and further may expose the upper surface of the dielectric layer 96 near the metal trace 6, as shown in Fig. 11c.

[00113] The material of the polymer layer 98 may include benzocyclobutane (BCB), polyimide (PI), polyurethane, epoxy resin, a parylene-based polymer, a solder-mask material, an

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elastomer, or a porous dielectric material. The polymer layer 98 has a thickness of between 3 and 25μm or between 5 and 50 micrometers.

[00114] The polymer layer 98 can be formed by a spin-on coating process, a lamination process or a screen-printing process. Below, the process of forming a patterned polymer layer 98 is exemplified with the case of spin-on coating a polyimide layer on the dielectric layer 96 and then patterning the polyimide layer.

[00115] Referring to Fig. 11d, an adhesion/barrier layer 100 having a thickness of between 0.1 and 3 micrometers, and preferably between 0.5 and 2 micrometers, is formed on the polymer layer 98 and on the metal plugs 21. The adhesion/barrier layer 100 may be a titanium-tungsten-alloy layer, tantalum-containing layer, a chromium-containing layer or a titanium-nitride layer. The adhesion/barrier layer 100 may be formed by a sputtering method, an evaporation method, or a chemical vapor deposition (CVD) method.

[00116] Referring to Fig. 11e, a photoresist layer 102 can be formed on the adhesion/barrier layer 100 by a spin coating process or a lamination process. Referring to Fig. 11f, the photoresist layer 102 is patterned with the processes of exposure, development, etc., to form a photoresist opening 102a on the above-mentioned adhesion/barrier layer 100 over the metal plugs 21 exposed by the opening 98a.

[00117] Referring to Fig. 11g, an electroplated metal layer 104 is formed on the adhesion/barrier layer 100 in the opening 102a, wherein the electroplated metal layer 104 comprises a copper layer, gold layer, a nickel layer, has a thickness between 2 and 10 micrometers, between 5 and 20 micrometers or between 5 and 35 micrometers.

[00118] Referring to Fig. 11h, removing the photoresist layer 102.

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[00119] Referring to Fig. 11i, the above-mentioned adhesion/barrier layer 100 not under the electroplated metal layer 104 is removed with a dry etching method or a wet etching method. For example, the adhesion/barrier layer 100 made of titanium, titanium-tungsten alloy, titanium nitride, tantalum or tantalum nitride, not under the electroplated metal layer 104 is removed with a reactive ion etching (RIE) process.

[00120] First Application: Please referring to Fig. 12, the second substrates 22 is connected to a OLED display substrate through COG bonding process, wherein the OLED display substrate comprises a first glass substrate 106, a second glass substrate 108, an organic light-emitting diodes layer 110 (or a polymer light-emitting diodes layer, PLED layer) between the first glass substrate 106 and the second glass substrate 108 and multiple transparent electrodes 114. The metal bumps 72 are connected to the transparent electrodes 114 through an anisotropic conductive film (ACF) layer 116, wherein the ACF layer 116 comprises multiple conductive particles 117, such as nickel (Ni) particles, gold (Au) particles, nickel-gold alloy particles, silver-tin alloy particles, silver particles, gold plated particles, silver plated particles or nickel plated particles. The OLED display substrate comprises multiple OLED display panels. The OLED display substrate may comprise a touch screen function. A least distance 106a between a centerline of the metal bump 72 and a boundary of the glass substrate 106 is between 3 micrometers and 10 micrometers, 5 micrometers and 15 micrometers, 10 micrometers and 25 micrometers or 20 micrometers and 40 micrometers.

[00121] Next, cutting the second substrates 22 and the OLED display substrate to produce multiple package units.

[00122] Second Application: Furthermore, the OLED display substrate can be replaced with a Micro Electro Mechanical Systems (MEMS) display substrate. Please referring to Fig. 13, the second substrates 22 is connected to a MEMS display substrate through COG bonding process,

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wherein the MEMS display substrate comprises a first glass substrate 106, a MEMS layer 109 and multiple transparent electrodes 114 formed on the first glass substrate 106. The metal bumps 72 are connected to the transparent electrodes 114 through an anisotropic conductive film (ACF) layer 116, wherein the ACF layer 116 comprises multiple conductive particles 117, such as nickel (Ni) particles, gold (Au) particles, nickel-gold alloy particles, silver-tin alloy particles, silver particles, gold plated particles, silver plated particles or nickel plated particles. The MEMS display substrate comprises multiple MEMS display panels. The MEMS display substrate may comprise touch screen function. A least distance 106a between a centerline of the metal bump 72 and a boundary of the glass substrate 106 is between 3 micrometers and 10 micrometers, 5 micrometers and 15 micrometers, 10 micrometers and 25 micrometers or 20 micrometers and 40 micrometers.

[00123] Next, cutting the second substrates 22 and the MEMS display substrate to produce multiple package units.

[00124] Third application: Please refer to Fig. 14, multiple LED devices 122 are packaged on the bottom surface of the second substrates 22. The second substrates 22 is connected to a LCD display substrate through COG bonding process, wherein the LCD display substrate comprises a first glass substrate 106, a second glass substrate 108, and a transistor liquid crystal display layer 111 between the first glass substrate 106 and the second glass substrate 108 and multiple transparent electrodes 114. The metal bumps 72 are connected to the electrodes 114 through an anisotropic conductive film (ACF) layer 116, wherein the ACF layer 116 comprises multiple conductive particles 117, such as nickel (Ni) particles, gold (Au) particles, nickel-gold alloy particles, silver-tin alloy particles, silver particles, gold plated particles, silver plated particles or nickel plated particles. The LCD display substrate comprises multiple LCD display panels. The LCD display substrate may comprises a touch screen function, wherein the LCD display substrate comprises an in-cell TFT LCD substrate. There are multiple optical layers 128 between the second substrates 22 and LCD

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display substrate, such as a diffuser sheet layer, a prism sheet layer, a diffuser layer (or diffuser plate) and a reflector layer. A least distance 106a between a centerline of the metal bump 72 and a boundary of the glass substrate 106 is between 3 micrometers and 10 micrometers, 5 micrometers and 15 micrometers, 10 micrometers and 25 micrometers or 20 micrometers and 40 micrometers.

[00125] Next, cutting the second substrates 22 and the LCD display substrate to produce multiple package units.

[00126] Fourth application: Referring to Fig. 15, this structure of the fourth application is similar to the structure of the third application in Fig. 14. The second substrates 22 is connected to a LCD display substrate through flip-chip bonding process, wherein the LCD display substrate comprises a first glass substrate 106 and a second glass substrate 108, and a transistor liquid crystal display layer 111 and thin film transistor circuit layers (not shown) between the first glass substrate 106 and the second glass substrate 108, wherein multiple transparent electrodes 114 on the bottom surface of the first glass substrate 106 and multiple metal plugs 113 in the first glass substrate 106, wherein the multiple metal plugs 113 are connected to the transparent electrodes 114 respectively. The structure of the first glass substrate 106 can refer to the second substrates 22 in the invention. The metal bumps 72 are connected to the transparent electrodes 114 through a solder layer 107, wherein the solder layer 107 comprises gold-tin alloy, tin-silver alloy, tin-silver-copper alloy, indium, tin-bismuth alloy, or other lead-free alloy. The LCD display substrate comprises multiple LCD display panels. The LCD display substrate may comprise touch screen function, wherein the LCD display substrate comprising an in-cell TFT LCD substrate. There are multiple optical layers 128 between the second substrates 22 and LCD display substrate, such as a diffuser sheet layer, a prism sheet layer, a diffuser layer (or diffuser plate) and a reflector layer. A least distance 106a between a centerline of the metal bump 72 and a boundary of the glass substrate 106 is between 30

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micrometers and 100 micrometers, 50 micrometers and 150 micrometers, 100 micrometers and 250 micrometers or 50 micrometers and 300 micrometers.

[00127] Fifth application: Referring to Fig. 16, this structure of the fifth application is similar to the structure of the fourth application in Fig. 14. The organic light-emitting diodes layer 110 (or a polymer light-emitting diodes layer, PLED layer) is replaced with the liquid crystal display layer 111. The second substrates 22 is connected to a OLED display substrate through flip-chip bonding process, wherein the OLED display substrate comprises a first glass substrate 106 and a second glass substrate 108, and an organic light-emitting diodes layer 110 (or a polymer light-emitting diodes layer, PLED layer) and thin film transistor circuit layers (not shown) between the first glass substrate 106 and the second glass substrate 108, wherein multiple transparent electrodes 114 on the bottom surface of the first glass substrate 106 and multiple metal plugs 113 in the first glass substrate 106, wherein the multiple metal plugs 113 are connected to the transparent electrodes 114 respectively. The structure of the first glass substrate 106 can refer to the second substrates 22 in the invention. The metal bumps 72 are connected to the transparent electrodes 114 through a solder layer 107, wherein the solder layer 107 comprises gold-tin alloy, tin-silver alloy, tin-silver-copper alloy, indium, tin-bismuth alloy, or other lead-free alloy. The OLED display substrate comprises multiple OLED display panels. The OLED display substrate may comprise touch screen function, wherein the OLED display substrate comprising an in-cell TFT OLED substrate. A least distance 106a between a centerline of the metal bump 72 and a boundary of the glass substrate 106 is between 30 micrometers and 100 micrometers, 50 micrometers and 150 micrometers, 100 micrometers and 250 micrometers or 50 micrometers and 300 micrometers.

[00128] Sixth application: Referring to Fig. 17a, the second substrates 22 can be a port of an OLED display substrate. The OLED display substrate comprises the second substrates 22 and the second glass substrate 108, and an organic light-emitting diodes layer 110 (or a polymer light-

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emitting diodes layer, PLED layer), thin film transistor circuit layers (not shown) and transparent electrodes 114 between the second substrates 22 and the second glass substrate 108, wherein the metal plugs 21 connected to transparent electrodes 114 through the first metal layer 26. The OLED display substrate comprises multiple OLED display panels. The OLED display substrate may comprise touch screen function, wherein the OLED display substrate comprising an in-cell TFT OLED substrate.

[00129] Referring to Fig. 17b, the structure of the OLED display substrate comprises multiple thin film transistors circuits 700 and multiple organic light-emitting components 800 between the second substrates 22 and the second glass substrate 108, wherein the thin film transistors circuit 700 comprises a buffer layer 702, a first gate electrode 704a and a first source electrode 704b formed on the buffer layer 702, a first insulating layer 706 formed on the first gate electrode 704a, the first source electrode 704b and the buffer layer 702. An oxide semiconductor layer 710 is formed on the first insulating layer 706 over the first gate electrode 704a and the first source electrode 704b, wherein the oxide semiconductor layer 710 is connected to the first source electrode 704b through the opening in the first insulating layer 706. A second insulating layer 712 is formed on the oxide semiconductor layer 710. A second gate electrode 714a and a second source electrode 714b formed on the second insulating layer 712, wherein the second source electrode 714b connected to the oxide semiconductor layer 710 through an opening in the second insulating layer 712. A protection layer 716 is formed on the second gate electrode 714a, the second source electrode 714b and the second insulating layer 712. The organic light-emitting component 800 formed on the protection layer 716 and connected to the second source electrode 714b through an opening in the protection layer 716.

[00130] The oxide semiconductor layer 710 comprises a ZnO containing layer, wherein the ZnO containing layer can be doped with a group selected from the group constituted of at least one ionic: Gallium (Ga), indium (In), tin (Sn), zirconium (Zr), hafnium (Hf), cadmium (Cd), magnesium

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(Mg), vanadium (V). The first gate electrode 704a, the first source electrode 704b, the second gate electrode 714a and the second source electrode 714b are formed of a metal selected from the following groups: tungsten (W), titanium (Ti), molybdenum (Mo), silver (Ag), tantalum (Ta), aluminum (Al), copper (Cu), gold (Au), chromium (Cr) or niobium (Nb).

[00131] The organic light-emitting component 800 comprises an anode layer 802, a cathode layer 804 and an organic light-emitting layer 806 between the anode layer 802 and the cathode layer 804, wherein the anode layer 802 formed on the protection layer 716 and connected to the second source electrode 714b. A third insulating layer 808 formed on the protection layer 716 and the anode layer 802, then formed a hole/opening in the third insulating layer 808 and on the anode layer 802. Forming the organic light-emitting layer 806 in the opening and on the third insulating layer 808, then formed the cathode layer 804 on the third insulating layer 808 and on the organic light-emitting layer 806. The anode layer 802 is connected to the metal plugs 21 via a conductive layer formed on the opening through the buffer layer 702, a first insulating layer 706 and second insulating layer 712. The cathode layer 804 is connected to the metal plugs 21 via a conductive layer formed on the opening through the buffer layer 702, the first insulating layer 706, the second insulating layer 712 and the third insulating layer 808. The buffer layer 702、the first insulating layer 706, the second insulating layer 712 and the third insulating layer 808 comprise a polyimide, polyamide, acryl resin, benzocyclobutene, phenol resin, oxide layer (buffer layer 702), nitride layer (buffer layer 702).

[00132] The anode layer 802 may contain one or more transparent materials such as indium tin oxide (ITO), indium zinc oxide (IZO), zinc oxide (ZnO), indium gallium oxide (IGO), aluminum zinc oxide (AZO) and In2O3, or non-transparent materials such as Ag, Mg, Al, Pt, Pd, Au, Ni, Nd, Ir, Cr, Li, Ca, Mo, Ti, W, MoW, and Al/Cu. The cathode layer 804 may contain one or more transparent materials such as indium tin oxide (ITO), indium zinc oxide (IZO), zinc oxide (ZnO), indium gallium oxide (IGO), aluminum zinc oxide (AZO) and In_2O_3.

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[00133] The organic light-emitting layer 806 may include a hole transport layer (HTL) and a hole injection layer (HIL) stacked toward the pixel electrode (anode layer 802 or cathode layer 804), and an electron transport layer (ETL) and an electron injection layer (EIL) stacked toward the pixel electrode (anode layer 802 or cathode layer 804). Furthermore, various other layers may be stacked if required. Further, the light-emitting layer 806 comprises a carbazole biphenyl(CBP), (III)(bis(1-phenylisoquinoline)(acetylacetonate)iridium, PIQIr(acac)),(III)(bis(1-phenylquinoline)(acetylacetonate)iridium, PQIr(acac)), (III)(tris(1-phenylquinoline)iridium (PQIr), octaethylporphyrin platinum,PtOEP 、 (III))(tris(dibenzoylmethane)(o-phenanthroline)europium(III),PED ： Eu(DBM)3(Phen)),perylene, N,N'-Di(naphthalene-1-yl)-N,N'-diphenyl-benzidine, tris-8-hydroxyquinoline aluminum (PEDOT), copper phthalocyanine,CuPc, 4,4',4"-tris(N-(3-methylphenyl)-N-phenylamino)triphenylamine (MTDATA).

[00134] Referring to Fig. 18 and Fig. 19, an outward of display substrate produced from above first application to sixth application is an unframed display 119, wherein the unframed display 119 comprises a display area 119a has four edges 119b, wherein a gap between each edge 119b and one of four boundaries of the unframed display 119 has a least distance smaller than 15 micrometers, 20 micrometers, 30 micrometers, 50 micrometers, 100 micrometers, 150 micrometers or 200 micrometers. The unframed display 119 is installed in a shell 123 of a display device 125. Some components (not showed in drawings) can install in the display device 125 (or installed on the second substrates 22), for example, a speaker component, a battery component, a microphone component, a signal receiver component, a wireless signal receiver component, a wireless signal transmitter module.

[00135] Referring to Fig. 19, the display device 125 comprises multiple connecting ports 127 on the shell 123, wherein the connecting ports 127 comprise a signal connecting port, a power

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connecting port, and/or a ground connecting port. The display device 125 can connect to another one display device 125b to become a bigger display device 129, wherein the connecting ports 127 of the display device 125 are connected to the connecting ports 127 of the display device 125b. Multiple display devices 125 can be combined with a big display device, an advertising billboard. The display devices 125 can be used as a tile on the wall of the building. The display devices 125 can be a display unit on a surface of a magic cube.

[00136] The structure of the OLED display substrate disclosed in Fig. 12 and Fig. 16 can be referred to related specifications as above.

[00137] Those described above are the embodiments to exemplify the present disclosure to enable the person skilled in the art to understand, make and use embodiments of the present disclosure. This description, however, is not intended to limit the scope of the present disclosure. Any equivalent modification and variation according to the spirit of the present disclosure is to be also included within the scope of the claims stated below.

[00138] The components, steps, features, benefits and advantages that have been discussed are merely illustrative. None of them, nor the discussions relating to them, are intended to limit the scope of protection in any way. Numerous other embodiments are also contemplated. These include embodiments that have fewer, additional, and/or different components, steps, features, benefits and advantages. These also include embodiments in which the components and/or steps are arranged and/or ordered differently.

[00139] In reading the present disclosure, one skilled in the art will appreciate that embodiments of the present disclosure can be implemented in hardware, software, firmware, or any combinations of such, and over one or more networks. Suitable software can include computer-readable or machine-readable instructions for performing methods and techniques (and portions

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thereof) of designing and/or controlling the fabrication and design of integrated circuit chips according to the present disclosure. Any suitable software language (machine-dependent or machine-independent) may be utilized. Moreover, embodiments of the present disclosure can be included in or carried by various signals, e.g., as transmitted over a wireless radio frequency (RF) or infrared (IR) communications link or downloaded from the Internet.

[00140] Unless otherwise stated, all measurements, values, ratings, positions, magnitudes, sizes, and other specifications that are set forth in this specification, including in the claims that follow, are approximate, not exact. They are intended to have a reasonable range that is consistent with the functions to which they relate and with what is customary in the art to which they pertain. The scope of protection is limited solely by the claims. That scope is intended and should be interpreted to be as broad as is consistent with the ordinary meaning of the language that is used in the claims when interpreted in light of this specification and the prosecution history that follows and to encompass all structural and functional equivalents.

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REMARKS/ARGUMENTS

Claims 1-20 are cancelled. Claims 21-48 are pending in the application, of which claims 21 and 31 are the pending independent claims. Claims 47-48 are newly added. No new matter is believed to be added into the application by this paper.

Claim Amendments

Patent Priority:

This patent application is a continuation of application No. 15261956, filed Sept. 11, 2016, now pending, which claims priority benefits from U.S. provisional patent application No. 62/219249, filed Sept. 16, 2015. This patent application of application No. 15261956 is a continuation-in-part of application No. 14/036256, filed Sept. 25, 2013, now patent No. 9615453, **which claims the benefit of priority from U.S. provisional patent application No. 61/705,649**, filed Sept. 26, 2012, all of which is incorporated herein by reference in their entirety

All elements/conditions of the Claims 21-48 are from U.S. provisional patent application No. 61/705,649, filed Sept. 26, 2012 and disclosed in the Non-Provisional patent application of application No. 15261956, filed Sept. 11, 2016.

1. For claims 21, 31, 47 and 48 the subject matter that "a first metal plug vertically in a first through via in said first polymer layer, wherein said first metal plug comprises a first copper layer, wherein the first copper layer contacts with a sidewall of said first through via" (claims 21 and 31), "a second metal plug vertically in a second through via in said first polymer layer, wherein said second metal plug comprises a second copper layer, wherein a top surface of said second metal plug and a top surface of said first metal plug are in the same horizontal plane" (claims 21 and 31) and "first metal plug has a thickness between 100 and 300 micrometers" (claims 47 and 48) are disclosed and supported in Figs. 15, 17a and 17b, and paragraphs [0003], [0016] and [0017] in the specification of the provisional App. No. 61/705,649 filed on Sept. 26, 2012, (and disclosed and supported in Figs. 6j, 8a and 8b, and paragraph [0038], [0057] and [0058] in the specification of the non-provisional App. No. 15/261956, filed on Sept. 11, 2016), as below:

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[0003] …The traces 6 may be metal traces, such as **copper traces**. ….

[0016] Next, referring to Fig. 15, the traces 6 out of the column 8 are removed and cutting the column 8 to produce multiple first substrates 20, wherein the **first substrate 20 has a thickness** between 20 and 100 micrometers, between 50 and 150 micrometers, **between 100 and 300 micrometers** or between 150 and 2000 micrometers or greater than 1000 micrometers. The **first substrates 20 may be make a planarization process** using a suitable process, such as a chemical mechanical polishing (CMP) procedure, mechanical grinding, or laser drilling

[0017] Next, referring to Fig. 16a, the **first substrate 20 comprises multiple second substrates 22**. The second substrates 22 are well-regulated an array in the first substrate 20. **Each of the second substrates has multiple metal plugs 21, wherein the metal plug 21 is formed from metal traces 6. The metal plug 21 has the same material and structure with metal trace 6**.

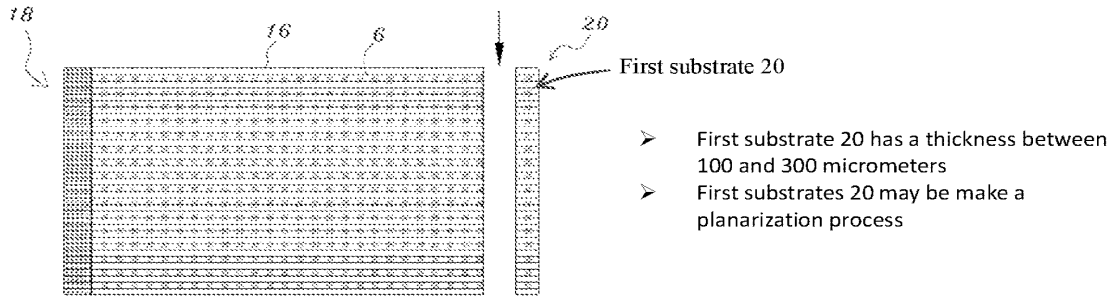


Fig. 15

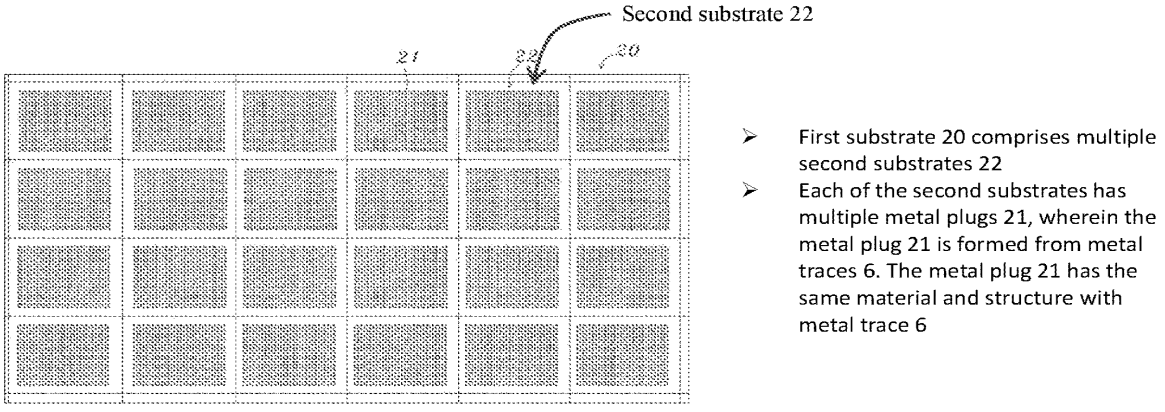


Fig. 16a

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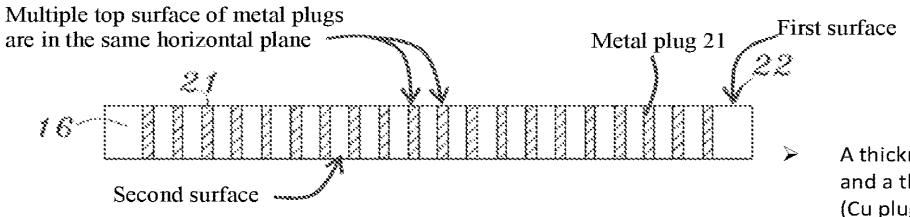


Fig. 17a

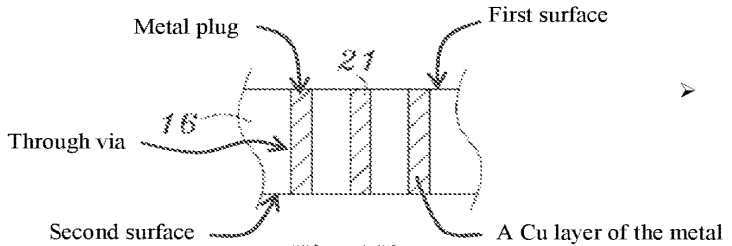
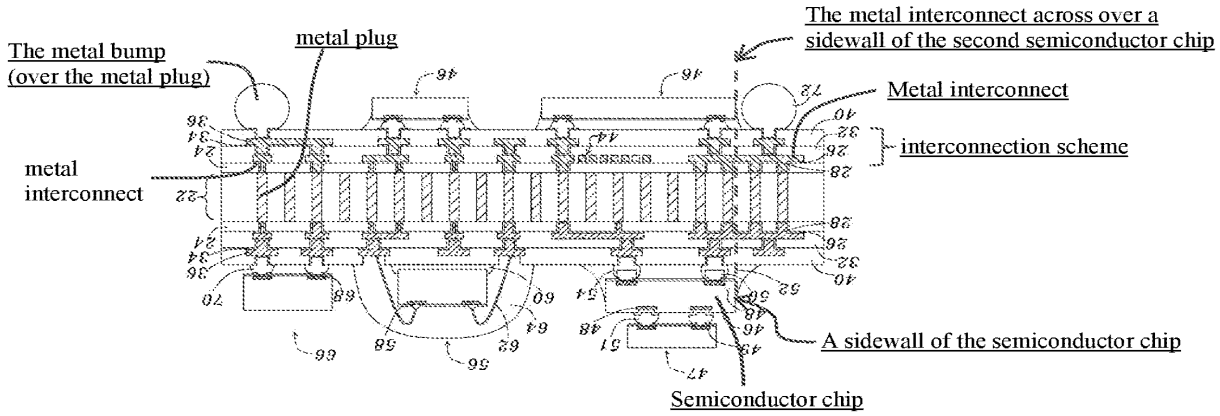


Fig. 17b

- A thickness of the second substrate 22 and a thickness of the metal plug 21 (Cu plug) are substantially the same with the thickness of the first substrate 20, therefore, the condition of "the thickness of the metal plug 21 is between 100 and 300 micrometers" in claims 47 and 48 can be supported.
- The condition of "a bottom surface of the metal plug is substantially coplanar with said second surface" in claims 21 and 31 can be supported from Figs. 17a and 17b.

2. For claims 21, 23, 38 the subject matter that "a first metal bump over said first interconnection scheme and said second metal plug" (claim 21) and "metal interconnect across over a sidewall of the second semiconductor chip" (claims 23 and 38) are disclosed and supported in Fig. 18x of the provisional App. No. 61/705,649 filed on Sept. 26, 2012, (and disclosed and supported in Fig. 9x of the non-provisional App. No. 15/261956, filed on Sept. 11, 2016), as below:



3. For claims 34 and 44 the subject matter that "third metal plug vertically in a third through via in said first polymer layer, wherein a pitch between said first and third metal plugs is between 200 and 1000 micrometers" are disclosed and supported in Fig. 7 and paragraph [0007] in the

specification of the provisional App. No. 61/705,649 filed on Sept. 26, 2012, (and disclosed and supported in Fig. 6b and paragraph [0045] of the non-provisional App. No. 15/261956, filed on Sept. 11, 2016), as below:

[0007] Next, referring to Fig. 7, the traces 2a, 2b, 4a and 4b are moved to change the pitch t1 to a pitch t2, then the traces 6 are closed up to a pitch t3. **The pitch t3 substantially the same with the diameter (or width) of the traces 2a, 2b, 4a and 4b, such as** between 10 and 30 micrometers, between 20 and 100 micrometers, between 40 and 150 micrometers, between 50 and 200 micrometers, **between 200 and 1000 micrometers** or between 500 and 10000 micrometers. In the same time, may be apply a force to stretch the traces 6, 2a, 2b, 4a and 4b and make the traces 6 keep strength and keep the pitch t3 fixed.

In view of the Amendments, Applicants submit that the claims are in condition for allowance and respectfully request a notice to this effect.

Others amendments

In the response submitted on Nov. 5, 2020, the data of "provisional application No. 14/036256, filed Sept. 25, 2013" in the REMARKS/ARGUMENTS (pages 22-28) for claims amendment supporting, amends to "Non-provisional patent App. No. 15/261956, filed on Sept. 11, 2016".

All elements/conditions of the Claims 21-48 are from U.S. provisional patent application No. 61/705,649, filed Sept. 26, 2012. Therefore, the applicant believes this amendment does not affect the support of the claims.

Respectfully submitted,

Mars Yang

Date: __2021-05-25_____ Ping-Jung Yang
Email: semars3898@gmail.com

IPR2026-00067
TSMC EX1032 Page 538

UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov

Application No. : 16752650
Applicant : Vang
Filing Date : 01/26/2020
Date Mailed : 05/10/2021

NOTICE TO FILE CORRECTED APPLICATION PAPERS

Notice of Allowance Mailed

This application has been accorded an Allowance Date and is being prepared for issuance. The application, however, is incomplete for the reasons below.

Applicant is given two (2) months from the mail date of this Notice within which to respond. This time period for reply is extendable under 37 CFR 1.136(a) for only TWO additional MONTHS.

The informalities requiring correction are indicated in the attachment(s). If the informality pertains to the abstract, specification (including claims) or drawings, the informality must be corrected with an amendment in compliance with 37 CFR 1.121 (or, if the application is a reissue application, 37 CFR 1.173). Such an amendment may be filed after payment of the issue fee if limited to correction of informalities noted herein. See Waiver of 37 CFR 1.312 for Documents Required by the Office of Patent Publication, 1280 Off. Gaz. Patent Office 918 (March 23, 2004). In addition, if the informality is not corrected until after payment of the issue fee, for purposes of 35 U.S.C. 154(b)(1)(iv), "all outstanding requirements" will be considered to have been satisfied when the informality has been corrected. A failure to respond within the above-identified time period will result in the application being ABANDONED.

See attachment(s).

*A copy of this notice **MUST** be returned with the reply. Please address response to "Mail Stop Issue Fee, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450".*

/Shirley Winslow/
Publication Branch
Office of Data Management
(571) 272-4200

Application No. 16752650

SPECIFICATION REFERS TO ITS OWN PAGE/PARAGRAPH NUMBER(S) AND/OR SPECIFICATION REFERS TO NONEXISTENT CLAIM(S)

[X] The patent will be printed in numbered columns with intercolumnar line numbers and without paragraph numbers. Any reference(s) within the applicant-filed specification to its own page number(s) or paragraph number(s) will have no meaning in the printed patent.

In response to this notice, the applicant either should file an amendment to the specification that removes the reference(s) to the page number(s) or paragraph number(s) or should submit a letter stating that the patent specification should be printed with the reference(s) to the page number(s) or paragraph number(s).

See Page(s)/Paragraph(s) p. 39 (paragraph 00136).

[ ] The specification refers by number to one or more claims that are not present in the allowed application – that is, the claim number(s) mentioned in the specification are higher than the total number of allowed claims.

In response to this notice, the applicant either should file an amendment to the specification that removes the reference(s) to the nonexistent claim(s) or should submit a letter stating that the patent specification should be printed with the reference(s) to the nonexistent claim(s).

See Page(s)/Paragraph(s) .

PTO/SB/08a (01-10)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT
(Not for submission under 37 CFR 1.99)

Application Number	16752650
Filing Date	2020-01-26
First Named Inventor	Ping-Jung Yang
Art Unit	1782
Examiner Name	LIU, XIAOMING
Attorney Docket Number	Mars16-001-US-C01

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	6423570		2002-07-23	Ma, et al.	
	2	7569422		2009-08-04	Lin	
	3	7019406		2006-03-28	Huang, et al.	
	4	6002592		1999-12-14	Nakamura, et al.	
	5	8431977		2013-04-30	Yang	
	6	8193555		2012-06-05	Lin, et al.	
	7	10490521		2019-11-26	Hu, et al.	
	8	8445323		2013-03-21	Lin, et al.	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	16752650
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	First Named Inventor	Ping-Jung Yang
	Art Unit	1782
	Examiner Name	LIU, XIAOMING
	Attorney Docket Number	Mars16-001-US-C01

	9	8456856		2010-03-11	Lin et al.	
	10	8837872		2014-09-16	Yang et al.	

If you wish to add additional U.S. Patent citation information please click the Add button. Add

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Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20050098891		2005-05-12	Wakabayashi, Takeshi, et al.	
	2	20040238945		2004-12-02	Huang, Chien-Ping et al.	
	3	20060292851		2006-12-28	Lin; Mou-Shiung et al.	
	4	20110278736		2011-11-17	Lin; Yaojian et al.	
	5	20110285005		2011-11-24	LIN; Yung-Chi et al.	
	6	20120193785		2012-08-02	Mou-Shiung Lin et al.	

If you wish to add additional U.S. Published Application citation information please click the Add button. Add

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
	Application Number	16752650
	Filing Date	2020-01-26
	First Named Inventor	Ping-Jung Yang
	Art Unit	1782
	Examiner Name	LIU, XIAOMING
	Attorney Docket Number	Mars16-001-US-C01

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1							

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NON-PATENT LITERATURE DOCUMENTS Remove

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1		

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EXAMINER SIGNATURE

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
	Application Number	16752650
	Filing Date	2020-01-26
	First Named Inventor	Ping-Jung Yang
	Art Unit	1782
	Examiner Name	LIU, XIAOMING
	Attorney Docket Number	Mars16-001-US-C01

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Ping-Jung Yang/	Date (YYYY-MM-DD)	2021-05-25
Name/Print	Ping-Jung Yang	Registration Number	

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

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TSMC EX1032 Page 545

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

102851 7590 06/22/2021

PING-JUNG YANG
NO 2, NIOUPU SOUTH RD., SIANGSHAN DISTRICT
HSINCHU CITY, 30091
TAIWAN

EXAMINER	
LIU, XIAOMING	
ART UNIT	**PAPER NUMBER**
2812	

DATE MAILED: 06/22/2021

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/752,650	01/26/2020	Ping-Jung Yang	Mars16-001-US-C01	4809

TITLE OF INVENTION: CHIP PACKAGE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	$600	$0.00	$0.00	$600	09/22/2021

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Maintenance fees are due in utility patents issuing on applications filed on or after Dec. 12, 1980. It is patentee's responsibility to ensure timely payment of maintenance fees when due. More information is available at www.uspto.gov/PatentMaintenanceFees.

PTOL-85 (Rev. 02/11)

IPR2026-00067
TSMC EX1032 Page 546

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via EFS-Web.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

102851 7590 06/22/2021

PING-JUNG YANG
NO 2, NIOUPU SOUTH RD., SIANGSHAN DISTRICT
HSINCHU CITY, 30091
TAIWAN

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via EFS-Web or by facsimile to (571) 273-2885, on the date below.

(Typed or printed name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/752,650	01/26/2020	Ping-Jung Yang	Mars16-001-US-C01	4809

TITLE OF INVENTION: CHIP PACKAGE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	$600	$0.00	$0.00	$600	09/22/2021

EXAMINER	ART UNIT	CLASS-SUBCLASS
LIU, XIAOMING	2812	257-091000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-09 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. Fees submitted: ❑Issue Fee ❑Publication Fee (if required) ❑Advance Order - # of Copies _____

4b. Method of Payment: *(Please first reapply any previously paid fee shown above)*

❑ Electronic Payment via EFS-Web ❑ Enclosed check ❑ Non-electronic payment by credit card (Attach form PTO-2038)

❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. _____

5. **Change in Entity Status** (from status indicated above)

❑ Applicant certifying micro entity status. See 37 CFR 1.29

❑ Applicant asserting small entity status. See 37 CFR 1.27

❑ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

IPR2026-00067
TSMC EX1032 Page 547

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/752,650	01/26/2020	Ping-Jung Yang	Mars16-001-US-C01	4809

102851 7590 06/22/2021

PING-JUNG YANG
NO 2, NIOUPU SOUTH RD., SIANGSHAN DISTRICT
HSINCHU CITY, 30091
TAIWAN

EXAMINER	
LIU, XIAOMING	
ART UNIT	**PAPER NUMBER**
2812	

DATE MAILED: 06/22/2021

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

IPR2026-00067
TSMC EX1032 Page 548

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 16/752,650	Applicant(s) Yang, Ping-Jung	
	Examiner XIAOMING LIU	Art Unit 2812	AIA (FITF) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☑ This communication is responsive to 5/25/2021.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☑ The allowed claim(s) is/are 21-48 . As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see **http://www.uspto.gov/patents/init_events/pph/index.jsp** or send an inquiry to **PPHfeedback@uspto.gov.**

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some *c) ☐ None of the:

   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____ .

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____ .

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☑ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 5/25/2021.
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material _____.
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date. _____.
5. ☐ Examiner's Amendment/Comment
6. ☑ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/XIAOMING LIU/
Examiner, Art Unit 2812

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DETAILED ACTION

The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 5/25/2021 has been entered.

Information Disclosure Statement

The information disclosure statement (IDS) submitted on 5/25/2021. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Allowable Subject Matter

Claims 21-48 are allowed.

The following is an examiner's statement of reasons for allowance: currently independent claims 21 and 31 are allowable because the closest prior art does not appear to disclose, alone or in combination, the limitations of material and structure of the chip package in combination with the other required elements of claim 21 or 31.

Specifically, the limitations are material to the inventive concept of the application in hand to forming a polymer interconnect with sufficient coefficient of expansion to enable holes and other features formed inside with improved chemical durability, strength and optical properties.

Dependent claims 22-30 and 32-48 are respectively dependent on currently amended allowable independent claims 21 or 31. Therefore, claims 22-30 and 32-48 incorporate the allowable limitations of claims 21 or 31. Consequently, claims 22-30 and 32-48 are allowable.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to XIAOMING LIU whose telephone number is (571)270-0384. The examiner can normally be reached on Monday-Friday, 9am-8pm, EST.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Charles Garber can be reached on (571)272-2194. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see https://ppair-

my.uspto.gov/pair/PrivatePair. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/XIAOMING LIU/
Examiner, Art Unit 2812

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/752,650	Yang, Ping-Jung
	Examiner	**Art Unit**
	XIAOMING LIU	2812

CPC							
Symbol						**Type**	**Version**
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H01L	/	2224	/	48465		A	2013-01-01
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NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	28	
/XIAOMING LIU/ Examiner, Art Unit 2812	17 June 2021	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	21	fig17b

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Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/752,650	Yang, Ping-Jung
	Examiner	**Art Unit**
	XIAOMING LIU	2812

CPC						
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NONE		**Total Claims Allowed:**	
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/XIAOMING LIU/ Examiner, Art Unit 2812	17 June 2021	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	21	fig17b

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Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/752,650	Yang, Ping-Jung
	Examiner	**Art Unit**
	XIAOMING LIU	2812

CPC Combination Sets

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NONE		Total Claims Allowed:	
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(Primary Examiner)	(Date)	21	fig17b

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Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/752,650	Yang, Ping-Jung
	Examiner	Art Unit
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NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	28	
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(Primary Examiner)	(Date)	21	fig17b

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Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/752,650	Yang, Ping-Jung
	Examiner	Art Unit
	XIAOMING LIU	2812

CPC Combination Sets								
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NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	28	
/XIAOMING LIU/ Examiner, Art Unit 2812	17 June 2021	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	21	fig17b

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Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/752,650	Yang, Ping-Jung
	Examiner	**Art Unit**
	XIAOMING LIU	2812

CPC Combination Sets								
Symbol					**Type**	**Set**	**Ranking**	**Version**
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H01L	/	2224	/	32225	A	38	3	2013-01-01
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H01L	/	2924	/	00	A	40	5	2013-01-01
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NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	28	
/XIAOMING LIU/ Examiner, Art Unit 2812	17 June 2021	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	21	fig17b

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Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/752,650	Yang, Ping-Jung
	Examiner	**Art Unit**
	XIAOMING LIU	2812

INTERNATIONAL CLASSIFICATION					
CLAIMED					
H01L23/538	/	23	/	538	
H01L23/15	/	23	/	15	
H01L23/498	/	23	/	498	

NON-CLAIMED				
	/		/	

US ORIGINAL CLASSIFICATION	
CLASS	**SUBCLASS**

CROSS REFERENCES(S)						
CLASS	**SUBCLASS (ONE SUBCLASS PER BLOCK)**					

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	28	
/XIAOMING LIU/ Examiner, Art Unit 2812	17 June 2021	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	21	fig17b

U.S. Patent and Trademark Office — Part of Paper No.: 20210604

IPR2026-00067
TSMC EX1032 Page 560

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/752,650	Yang, Ping-Jung
	Examiner	**Art Unit**
	XIAOMING LIU	2812

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIMS

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
	1		10		19	8	28	18	37	27	46				
	2		11		20	9	29	19	38	11	47				
	3		12	1	21	10	30	20	39	28	48				
	4		13	2	22	12	31	21	40						
	5		14	3	23	13	32	22	41						
	6		15	4	24	14	33	23	42						
	7		16	5	25	15	34	24	43						
	8		17	6	26	16	35	25	44						
	9		18	7	27	17	36	26	45						

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	28	
/XIAOMING LIU/ Examiner, Art Unit 2812	17 June 2021	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	21	fig17b

U.S. Patent and Trademark Office — Part of Paper No.: 20210604

IPR2026-00067
TSMC EX1032 Page 561

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/752,650	Yang, Ping-Jung
	Examiner	Art Unit
	XIAOMING LIU	2812

CPC - Searched*		
Symbol	**Date**	**Examiner**
H01L23/49827 | H01L23/5384 | H01L2224/08165 | H01L2224/16165 | H01L2224/16235 | H01L2224/32165 | H01L2224/32235 | H01L2224/40165 | H01L2224/40235 | H01L2224/48165 | H01L2224/48235 with date and text	09/17/2020	XL

CPC Combination Sets - Searched*		
Symbol	**Date**	**Examiner**

US Classification - Searched*			
Class	**Subclass**	**Date**	**Examiner**

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	**Date**	**Examiner**
Searched East: (USPAT, USPGPUB, USOCR, FPRS, EPO, JPO, DERWENT, IBMTDB)	09/17/2020	XL
Inventor search Conducted, limited with text	09/17/2020	XL
Assignee search Conducted, limited with text	09/17/2020	XL
Google text search conducted	09/17/2020	XL
Non-Patent Literature searched: science direct, TC2800	09/17/2020	XL
updated search	04/22/2021	XL
updated search	06/05/2021	XL

/XIAOMING LIU/ Examiner, Art Unit 2812	

IPR2026-00067
TSMC EX1032 Page 562

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/752,650	Yang, Ping-Jung
	Examiner	Art Unit
	XIAOMING LIU	2812

Interference Search			
US Class/CPC Symbol	**US Subclass/CPC Group**	**Date**	**Examiner**
H01L23	49827 53840 with text	06/17/2021	XL
H01L2224	08165 16165 16235 32165 40165 40235 48165 48235 with text	06/17/2021	XL
	all CPC group with text	06/17/2021	XL

/XIAOMING LIU/ Examiner, Art Unit 2812	

IPR2026-00067
TSMC EX1032 Page 563

Bibliographic Data

Application No: 16/752,650

Foreign Priority claimed: ○ Yes ◉ No

35 USC 119 (a-d) conditions met: ☐ Yes ☑ No ☐ Met After Allowance

Verified and Acknowledged: /XIAOMING LIU/ (Examiner's Signature) | (Initials)

Title: CHIP PACKAGE

FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
01/26/2020	257	2812	Mars16-001-US-C01
RULE			

APPLICANTS

Ping-Jung Yang, Hsin-Chu City, TAIWAN

INVENTORS

Ping-Jung Yang, Hsinchu City, TAIWAN

CONTINUING DATA

This application is a CON of 15261956 09/11/2016 PAT 10622310

15261956 has PRO of 62219249 09/16/2015

15261956 is a CIP of 14036256 09/25/2013 PAT 9615453

14036256 has PRO of 61705649 09/26/2012

FOREIGN APPLICATIONS

IF REQUIRED, FOREIGN LICENSE GRANTED**

02/12/2020

**** SMALL ENTITY ****

STATE OR COUNTRY

TAIWAN

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PING-JUNG YANG
NO 2, NIOUPU SOUTH RD., SIANGSHAN DISTRICT
HSINCHU CITY, 30091
TAIWAN

FILING FEE RECEIVED

$785

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (01-10)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT
(Not for submission under 37 CFR 1.99)

Application Number	16752650
Filing Date	2020-01-26
First Named Inventor	Ping-Jung Yang
Art Unit	1782
Examiner Name	LIU, XIAOMING
Attorney Docket Number	Mars16-001-US-C01

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	6423570		2002-07-23	Ma, et al.	
	2	7569422		2009-08-04	Lin	
	3	7019406		2006-03-28	Huang, et al.	
	4	6002592		1999-12-14	Nakamura, et al.	
	5	8431977		2013-04-30	Yang	
	6	8193555		2012-06-05	Lin, et al.	
	7	10490521		2019-11-26	Hu, et al.	
	8	8445323		2013-03-21	Lin, et al.	

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /X.L/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	16752650
	Filing Date	2020-01-26
	First Named Inventor	Ping-Jung Yang
	Art Unit	1782
	Examiner Name	LIU, XIAOMING
	Attorney Docket Number	Mars16-001-US-C01

	9	8456856		2010-03-11	Lin et al.	
	10	8837872		2014-09-16	Yang et al.	

If you wish to add additional U.S. Patent citation information please click the Add button. Add

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Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20050098891		2005-05-12	Wakabayashi, Takeshi, et al.	
	2	20040238945		2004-12-02	Huang, Chien-Ping et al.	
	3	20060292851		2006-12-28	Lin; Mou-Shiung et al.	
	4	20110278736		2011-11-17	Lin; Yaojian et al.	
	5	20110285005		2011-11-24	LIN; Yung-Chi et al.	
	6	20120193785		2012-08-02	Mou-Shiung Lin et al.	

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	Application Number	16752650
	Filing Date	2020-01-26
	First Named Inventor	Ping-Jung Yang
	Art Unit	1782
	Examiner Name	LIU, XIAOMING
	Attorney Docket Number	Mars16-001-US-C01

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2]	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1							

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Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1		

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EXAMINER SIGNATURE

Examiner Signature	/XIAOMING LIU/	Date Considered	06/17/2021

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /X.L/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	16752650
	Filing Date	2020-01-26
	First Named Inventor	Ping-Jung Yang
	Art Unit	1782
	Examiner Name	LIU, XIAOMING
	Attorney Docket Number	Mars16-001-US-C01

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Ping-Jung Yang/	Date (YYYY-MM-DD)	2021-05-25
Name/Print	Ping-Jung Yang	Registration Number	

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

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6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

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9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

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EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	2	("20200161245").PN.	US-PGPUB; USPAT; USOCR; DERWENT	OR	OFF	2020/09/10 12:31
S2	2	S1 and polymer and copper	US-PGPUB; USPAT; USOCR; DERWENT	OR	OFF	2020/09/10 13:04
S3	277	(US-20120282739-$ or US-20120319254-$ or US-20120089180-$ or US-20100244059-$ or US-20090179317-$ or US-20090127638-$ or US-20070135550-$ or US-20110127314-$ or US-20090160053-$ or US-20110204513-$ or US-20100260224-$ or US-20060081877-$ or US-20120174855-$ or US-20100200898-$ or US-20110233754-$ or US-20130280826-$ or US-20130292808-$ or US-20120062439-$ or US-20080308917-$ or US-20040238857-$ or US-20130241077-$ or US-20100059855-$ or US-20110188193-$ or US-20110165734-$ or US-20090230531-$ or US-20090152714-$).did. or (US-20090152692-$ or US-20080211084-$ or US-20070132093-$ or US-20050224937-$ or US-20130105967-$ or US-20070158818-$ or US-20130161784-$ or US-20120199843-$ or US-20120193802-$ or US-20120161163-$ or US-20120132817-$ or US-20120049366-$ or US-20060270079-$ or US-20130193465-$ or US-20130234318-$ or US-20130113091-$ or US-20110260308-$ or US-20040238956-$ or US-20080182398-$ or US-20150214206-$ or US-20150221624-$ or US-20140035134-$ or US-20100078781-$ or US-20140312497-$ or US-20140160699-$ or US-20110215444-$ or US-20150262931-$).did. or (US-20150108661-$ or US-20100184256-$	US-PGPUB; USPAT; USOCR; DERWENT	OR	OFF	2020/09/10 13:39

		or US-20090256670-$ or US-20080150119-$ or US-20050253231-$ or US-20030096089-$ or US-20150342060-$ or US-20120094442-$ or US-20110115083-$ or US-20140217436-$ or US-20140048949-$ or US-20130214386-$ or US-20120086117-$ or US-20120049363-$ or US-20120032282-$ or US-20140264810-$ or US-20120160647-$ or US-20100000775-$ or US-20070243704-$ or US-20050090035-$ or US-20050151272-$ or US-20100019373-$ or US-20140118978-$ or US-20120293977-$ or US-20110227223-$ or US-20090236730-$ or US-20080049392-$).did. or (US-20090096070-$ or US-20130168857-$ or US-20110309526-$ or US-20080211111-$ or US-20080277802-$ or US-20070080469-$ or US-20140246223-$ or US-20150162194-$ or US-20160343592-$ or US-20140054796-$ or US-20130343067-$ or US-20130017652-$ or US-20120306104-$ or US-20120019123-$ or US-20110291541-$ or US-20110222280-$ or US-20100171139-$ or US-20120305977-$ or US-20150021754-$ or US-20110121449-$ or US-20150221614-$ or US-20130200531-$ or US-20130062761-$ or US-20120028411-$ or US-20130295725-$ or US-20060194370-$ or US-20080212288-$).did. or (US-7589405-$ or US-8906794-$ or US-6614122-$ or US-8558399-$ or US-8432022-$ or US-8228682-$ or US-8982577-$ or US-4706167-$ or US-5531020-$ or US-8252615-$ or US-6331451-$ or US-8946886-$ or US-8415785-$ or US-5804881-$ or US-9786623-$ or US-9040352-$ or US-7855391-$ or US-8507927-$ or US-7619901-$ or US-9768038-$ or US-9627261-$ or US-5250843-$ or US-9735113-$ or US-9431316-$ or US-8617935-$ or US-8518749-$).did. or (US-8482134-$ or US-8258012-$ or US-8105872-$ or US-7955942-$ or US-7846777-$ or US-7727806-$).did.				

S4	121	("10192796" | "8648470" | "8846454" | "8980691" | "8987918" | "9048211" | "9431331" | "9704780" | "9837303" | "10043768" | "8742579" | "8786060" | "8796137" | "8883561" | "8895440" | "8916421" | "8952489" | "8952521" | "8993377" | "9082806" | "9224647" | "9281292" | "9324672" | "9331060" | "9343442" | "9362187" | "9385006" | "9385009" | "9397050" | "9406619" | "9406658" | "9508626" | "9524955" | "9593009" | "9679863" | "9704843" | "9735113" | "20020038725" | "20020145197" | "20020159243" | "20050012217" | "20060006539" | "20060020371" | "20070045841" | "20070268581" | "20080054457" | "20080080111" | "20080113505" | "20080129439" | "20080149384" | "20080150623" | "20080283277" | "20080284014" | "20080318361" | "20090109655" | "20090174065" | "20090273073" | "20100164030" | "20100200898" | "20100246152" | "20100290191" | "20110026232" | "20110065250" | "20110089574" | "20110147055" | "20110242050" | "20130292846" | "20130307140" | "20140103488" | "20140210101" | "20140252646" | "20140264839" | "20140367160" | "20150166329" | "20170345761" | "20170345764" | "20170373004" | "4221047" | "4639543" | "4975103" | "5294238" | "5705855" | "6156413" | "6177707" | "6194762" | "6265771" | "6309901" | "6339197" | "6434016" | "6539750" | "6673698" | "6691409" | "6772514" | "6799438" | "6839946" | "6894358" | "6989604" | "7038309" | "7071521" | "7072018" | "7091589" | "7151009" | "7259080" | "7279771" | "7285834" | "7337540" | "7362403" | "7476623" | "7557440" | "7749900" | "7808799" | "7993510" | "8207453" | "8338238" | "8354297" | "8822281" | "8878360" | "9048233" | "9147638" | "9385105" | "9627365").PN.	US-PGPUB; USPAT	OR	OFF	2020/09/10 13:40
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S6	3,569	(H01L2224/45147).CPC.	US-PGPUB	OR	OFF	2020/09/10 13:42
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S10	5	("20080277783" | "20090315171" | "20110110061" | "8318537" | "9064757").PN. OR ("9437534").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2020/09/10 13:49
S11	9	("2011/0110061").URPN.	USPAT	OR	OFF	2020/09/10 13:50
S12	1,645	((("YUAN") near3 ("Zhongfa")) OR (("LIU") near3 ("Yong")) OR (("LIU") near3 ("Yumin")) OR (("QIAN") near3 ("Qiuxiao"))).INV.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2020/09/10 13:54
S13	28	S12 and copper and polymer	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2020/09/10 13:55
S14	18	("2009/0184403").URPN.	USPAT	OR	OFF	2020/09/10 13:58
S15	4	("20090184403").PN. OR ("8614120").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2020/09/10 13:58
S16	20,179	(H01L23/49827 | H01L23/5384 | H01L2224/08165 | H01L2224/16165 | H01L2224/16235 | H01L2224/32165 | H01L2224/32235 | H01L2224/40165 | H01L2224/40235 | H01L2224/48165 | H01L2224/48235).CPC.	US-PGPUB; USPAT; USOCR	OR	OFF	2020/09/10 14:05
S17	6,787	S16 and copper and polymer	US-PGPUB; USPAT; USOCR	OR	OFF	2020/09/10 14:05
S18	2,733	S16 and copper same polymer	US-PGPUB; USPAT; USOCR	OR	OFF	2020/09/10 14:05
S19	970	S16 and cpu same gpu	US-PGPUB; USPAT; USOCR	OR	OFF	2020/09/10 14:11

S20	82	S16 and cpu same gpu same passive	US-PGPUB; USPAT; USOCR	OR	OFF	2020/09/10 14:15
S21	121	("10192796" | "8648470" | "8846454" | "8980691" | "8987918" | "9048211" | "9431331" | "9704780" | "9837303" | "10043768" | "8742579" | "8786060" | "8796137" | "8883561" | "8895440" | "8916421" | "8952489" | "8952521" | "8993377" | "9082806" | "9224647" | "9281292" | "9324672" | "9331060" | "9343442" | "9362187" | "9385006" | "9385009" | "9397050" | "9406619" | "9406658" | "9508626" | "9524955" | "9593009" | "9679863" | "9704843" | "9735113" | "20020038725" | "20020145197" | "20020159243" | "20050012217" | "20060006539" | "20060020371" | "20070045841" | "20070268581" | "20080054457" | "20080080111" | "20080113505" | "20080129439" | "20080149384" | "20080150623" | "20080283277" | "20080284014" | "20080318361" | "20090109655" | "20090174065" | "20090273073" | "20100164030" | "20100200898" | "20100246152" | "20100290191" | "20110026232" | "20110065250" | "20110089574" | "20110147055" | "20110242050" | "20130292846" | "20130307140" | "20140103488" | "20140210101" | "20140252646" | "20140264839" | "20140367160" | "20150166329" | "20170345761" | "20170345764" | "20170373004" | "4221047" | "4639543" | "4975103" | "5294238" | "5705855" | "6156413" | "6177707" | "6194762" | "6265771" | "6309901" | "6339197" | "6434016" | "6539750" | "6673698" | "6691409" | "6772514" | "6799438" | "6839946" | "6894358" | "6989604" | "7038309" | "7071521" | "7072018" | "7091589" | "7151009" | "7259080" | "7279771" | "7285834" | "7337540" | "7362403" | "7476623" | "7557440" | "7749900" | "7808799" | "7993510" | "8207453" | "8338238" | "8354297" | "8822281" | "8878360" | "9048233" | "9147638" | "9385105" | "9627365").PN.	US-PGPUB; USPAT	OR	OFF	2020/09/10 18:30
S24	2	"20130242493"	US-PGPUB; USPAT;	OR	OFF	2020/09/10 18:34

			USOCR; DERWENT			
S25	32	("2013/0242493").URPN.	USPAT	OR	OFF	2020/09/10 18:36
S27	21	"ppm/.degree.C"	USPAT	OR	OFF	2020/09/10 18:42
S28	1,788	polymer same expansion adj coefficient	USPAT	OR	OFF	2020/09/10 18:45
S29	446	polymer near10 expansion adj coefficient	USPAT	OR	OFF	2020/09/10 18:45
S34	3	"20110257716"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2020/09/10 18:55
S35	46	(US-20110304008-$ or US-20120313207-$ or US-20120241938-$ or US-20120193785-$ or US-20120052631-$ or US-20110297434-$ or US-20110026232-$ or US-20100290191-$ or US-20100207154-$ or US-20100200898-$ or US-20100102457-$ or US-20100044850-$ or US-20090315171-$ or US-20110110061-$ or US-20100123257-$ or US-20100052119-$ or US-20090184403-$ or US-20120326170-$ or US-20130050228-$ or US-20130049217-$ or US-20120313209-$ or US-20120306096-$ or US-20120228749-$ or US-20140124777-$ or US-20140042637-$ or US-20130328211-$).did. or (US-20130292844-$ or US-20130119562-$ or US-20100258944-$ or US-20100258946-$ or US-20100252937-$ or US-20080149384-$ or US-20130277855-$ or US-20170373004-$ or US-20170345761-$ or US-20130242493-$).did. or (US-9437534-$ or US-8247269-$ or US-8614120-$ or US-7968978-$ or US-9627365-$ or US-9817312-$ or US-9615453-$ or US-9363890-$ or US-9161443-$ or US-9030751-$).did.	US-PGPUB; USPAT	OR	OFF	2020/09/10 18:58
S37	30	S35 and polyimide	US-PGPUB; USPAT	OR	ON	2020/09/10 19:00

S38	65	(US-20160181184-$ or US-20170062361-$ or US-20160163666-$ or US-20150206934-$ or US-20140021618-$ or US-20120208129-$ or US-20180062386-$ or US-20160173039-$ or US-20160087588-$ or US-20110241793-$ or US-20110057742-$ or US-20100032818-$ or US-20100001363-$ or US-20130147540-$ or US-20190259758-$ or US-20190252306-$ or US-20150179591-$ or US-20140346663-$ or US-20140312362-$ or US-20140077362-$ or US-20130200528-$ or US-20130026658-$ or US-20100165585-$ or US-20160071820-$).did. or (US-6659663-$ or US-10153553-$ or US-6829152-$ or US-10580726-$ or US-10090266-$ or US-9972555-$ or US-8168470-$ or US-9954028-$ or US-10177115-$).did.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2020/09/10 22:50
S39	1,659	((("STATS") near3 ("CHIPPAC") near3 ("LTD"))).AS,AANM.	USPAT	OR	OFF	2020/09/10 22:51
S40	3	"20090230517"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2020/09/10 22:57
S41	3	"20090155959"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2020/09/10 23:20
S42	3	"20130049217"	US-PGPUB; USPAT; USOCR; DERWENT	OR	OFF	2020/09/11 10:28
S44	3	"20090155959"	US-PGPUB; USPAT; USOCR; DERWENT	OR	OFF	2020/09/11 10:34
S45	2	"20090155959" and passive	US-PGPUB; USPAT; USOCR; DERWENT	OR	OFF	2020/09/11 10:35

S46	3	"20090230517"	US-PGPUB; USPAT; USOCR; DERWENT	OR	OFF	2020/09/11 10:57
S47	20,179	(H01L23/49827 | H01L23/5384 | H01L2224/08165 | H01L2224/16165 | H01L2224/16235 | H01L2224/32165 | H01L2224/32235 | H01L2224/40165 | H01L2224/40235 | H01L2224/48165 | H01L2224/48235).CPC.	US-PGPUB; USPAT; USOCR	OR	OFF	2020/09/11 11:06
S48	537	S47 and cpu same gpu same DRAM	US-PGPUB; USPAT; USOCR	OR	OFF	2020/09/11 11:06
S49	127	S47 and cpu same gpu same DRAM and integration	US-PGPUB; USPAT; USOCR	OR	OFF	2020/09/11 11:06
S50	20,179	(H01L23/49827 | H01L23/5384 | H01L2224/08165 | H01L2224/16165 | H01L2224/16235 | H01L2224/32165 | H01L2224/32235 | H01L2224/40165 | H01L2224/40235 | H01L2224/48165 | H01L2224/48235).CPC.	US-PGPUB; USPAT; USOCR	OR	OFF	2020/09/11 13:47
S51	146	S50 and tsv same layout	US-PGPUB; USPAT; USOCR	OR	OFF	2020/09/11 13:47
S52	6	"20130049217" "20090155959" "20090230517" "20130277801" "20110257716" "20100252934"	US-PGPUB	OR	OFF	2020/09/17 16:44
S53	71	(US-20110304008-$ or US-20120313207-$ or US-20120241938-$ or US-20120193785-$ or US-20120052631-$ or US-20110297434-$ or US-20110026232-$ or US-20100290191-$ or US-20100207154-$ or US-20100200898-$ or US-20100102457-$ or US-20100044850-$ or US-20090315171-$ or US-20110110061-$ or US-20100123257-$ or US-20100052119-$ or US-20090184403-$ or US-20120326170-$ or US-20130050228-$ or US-20130049217-$ or US-20120313209-$ or US-20120306096-$ or US-20120228749-$ or US-20140124777-$ or US-20140042637-$ or US-20130328211-$).did. or (US-20130292844-$ or US-20130119562-$ or US-20100258944-$ or US-20100258946-$ or US-20100252937-$ or US-20080149384-$ or US-	US-PGPUB; USPAT	OR	ON	2021/04/22 11:47

		20130277855-$ or US-20170373004-$ or US-20170345761-$ or US-20130242493-$ or US-20100252934-$).did. or (US-9437534-$ or US-8247269-$ or US-8614120-$ or US-7968978-$ or US-9627365-$ or US-9817312-$ or US-9615453-$ or US-9363890-$ or US-9161443-$ or US-9030751-$ or US-8354304-$ or US-8273602-$ or US-8270176-$ or US-8263434-$ or US-8217514-$ or US-8193036-$ or US-8133762-$ or US-8110440-$ or US-8110908-$ or US-8105915-$ or US-8080445-$ or US-8067308-$ or US-8067828-$ or US-8067275-$ or US-8063477-$ or US-8034661-$).did. or (US-8008121-$ or US-7977802-$ or US-7935570-$ or US-7880293-$ or US-7858441-$ or US-7842542-$ or US-7838337-$ or US-7790503-$).did.				
S54	21,477	(H01L23/49827 | H01L23/5384 | H01L2224/08165 | H01L2224/16165 | H01L2224/16235 | H01L2224/32165 | H01L2224/32235 | H01L2224/40165 | H01L2224/40235 | H01L2224/48165 | H01L2224/48235).CPC.	US-PGPUB; USPAT; USOCR	OR	OFF	2021/04/22 11:47
S55	166	S54 and tsv same layout	US-PGPUB; USPAT; USOCR	OR	OFF	2021/04/22 11:47
S56	2	("20200161245").PN.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2021/04/22 11:48
S57	2	("20140085842").PN.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2021/04/22 12:22
S58	3	"20110147055"	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2021/04/22 12:24
S63	31	(US-20040238945-$ | US-20050098891-$ | US-20060292851-$ | US-20110278736-$ | US-20110285005-$ | US-20120193785-$ | US-10490521-$ | US-6002592-$ | US-6423570-$ | US-7019406-$ | US-7569422-$ | US-8193555-$ | US-8431977-$ | US-	US-PGPUB; USPAT; USOCR; DERWENT	OR	OFF	2021/06/03 01:46

		8445323-$ | US-8456856-$ | US-8837872-$).DID.				
S64	2	("20200161245").PN.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2021/06/03 01:52
S67	7	S63 and cpu same gpu	US-PGPUB; USPAT; USOCR; DERWENT	OR	OFF	2021/06/03 02:18
S68	10	("20060193691" | "20090014826" | "20090042338" | "20090057868" | "6777767" | "7582556" | "8193555").PN. OR ("8431977").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2021/06/03 02:48
S69	3	"20110304008"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/06/04 14:18
S70	13	("2011/0304008").URPN.	USPAT	OR	ON	2021/06/04 14:21
S71	130	("2012/0193785").URPN.	USPAT	OR	ON	2021/06/04 17:27
S73	3	"20120170887"	US-PGPUB; USPAT; USOCR; DERWENT	OR	OFF	2021/06/05 17:28
S75	3	"20110304008"	US-PGPUB; USPAT; USOCR; DERWENT	OR	OFF	2021/06/05 17:58
S76	33	("20040238941" | "20040262735" | "20050130368" | "20070096292" | "20080001285" | "20080099911" | "20080136004" | "20090170242" | "20090294899" | "20090302435" | "20100006994" | "20100059876" | "5250843" | "5353498" | "5841193" | "6495912" | "6828670" | "6905912" | "7214565" | "7619901" | "7772081" | "7790503" | "7858441" | "8193604").PN. OR ("8445323").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2021/06/05 19:41
S77	5	"20100140779"	US-PGPUB; USPAT; USOCR; FPRS; EPO;	OR	ON	2021/06/05 19:45

			JPO; DERWENT; IBM_TDB			
S78	3	"20110304008" "20100140779" "20120170887"	US-PGPUB	OR	OFF	2021/06/05 23:31
S79	1	"10622310".pn.	US-PGPUB; USPAT	OR	OFF	2021/06/05 23:41

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S59	10,057	(H01L23/49827 | H01L23/5384 | H01L2224/08165 | H01L2224/16165 | H01L2224/16235 | H01L2224/32165 | H01L2224/32235 | H01L2224/40165 | H01L2224/40235 | H01L2224/48165 | H01L2224/48235).CPC.	USPAT	OR	OFF	2021/04/22 11:37
S60	8	S59 and (copper and pitch and (coeffcient or expansion) and thickness).clm.	USPAT	OR	OFF	2021/04/22 11:44
S61	22	S59 and (pitch and (coeffcient or expansion) and thickness).clm.	USPAT	OR	OFF	2021/04/22 11:45
S62	242	(pitch and (coeffcient or expansion) and thickness).clm.	USPAT	OR	OFF	2021/04/22 11:45
S80	244	(pitch and (coeffcient or expansion) and thickness).clm.	USPAT	OR	OFF	2021/06/17 11:20
S81	10,183	(H01L23/49827 | H01L23/5384 | H01L2224/08165 | H01L2224/16165 | H01L2224/16235 | H01L2224/32165 | H01L2224/32235 | H01L2224/40165 | H01L2224/40235 | H01L2224/48165 | H01L2224/48235).CPC.	USPAT	OR	OFF	2021/06/17 11:20
S82	22	S81 and (pitch and (coeffcient or expansion) and thickness).clm.	USPAT	OR	OFF	2021/06/17 11:20

6/17/2021 11:21:06 AM
C:\Users\xliu3\Documents\EAST\Workspaces\202001\16752650_1.wsp

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 16/752,650	Filing Date 01/26/2020	☐ To be Mailed

ENTITY: ☐ LARGE ☑ SMALL ☐ MICRO

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A		N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A		N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*		x $50 =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*		x $230 =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).				
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))					
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL	

APPLICATION AS AMENDED - PART II

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT	06/24/2021	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 28	Minus	** 28	= 0		x $50 =	0
	Independent (37 CFR 1.16(h))	* 2	Minus	*** 3	= 0		x $240 =	0
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	0

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=		x $0 =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=		x $0 =	
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.	LIE
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".	/JACKIE A WHITE/
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".	
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.	

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Doc code: RCEX
Doc description: Request for Continued Examination (RCE)

PTO/SB/30EFS (02-18)
Approved for use through 11/30/2020. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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REQUEST FOR CONTINUED EXAMINATION(RCE)TRANSMITTAL
(Submitted Only via EFS-Web)

Application Number	16752650	Filing Date	2020-01-26	Docket Number (if applicable)	Mars-16-001-US-C01	Art Unit	2812
First Named Inventor	Ping-Jung Yang			Examiner Name	LIU, XIAOMING		

This is a Request for Continued Examination (RCE) under 37 CFR 1.114 of the above-identified application.
Request for Continued Examination (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, or to any design application. The Instruction Sheet for this form is located at WWW.USPTO.GOV

SUBMISSION REQUIRED UNDER 37 CFR 1.114

Note: If the RCE is proper, any previously filed unentered amendments and amendments enclosed with the RCE will be entered in the order in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).

☐ Previously submitted. If a final Office action is outstanding, any amendments filed after the final Office action may be considered as a submission even if this box is not checked.

- ☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____
- ☐ Other _____

☒ Enclosed

- ☒ Amendment/Reply
- ☐ Information Disclosure Statement (IDS)
- ☐ Affidavit(s)/ Declaration(s)
- ☐ Other _____

MISCELLANEOUS

☐ Suspension of action on the above-identified application is requested under 37 CFR 1.103(c) for a period of months _____
(Period of suspension shall not exceed 3 months; Fee under 37 CFR 1.17(i) required)

☐ Other _____

FEES

☐ **The RCE fee under 37 CFR 1.17(e) is required by 37 CFR 1.114 when the RCE is filed.**
The Director is hereby authorized to charge any underpayment of fees, or credit any overpayments, to Deposit Account No _____

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

Patent Practitioner Signature

X Applicant Signature

PTO/SB/30EFS (02-18)
Approved for use through 11/30/2020. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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Applicant Signature			
Applicant 1		Remove	
Signature	/Ping-Jung Yang/	Date (YYYY-MM-DD)	2021-06-24
Name	Ping-Jung Yang		
Click ADD for additional Applicant Signature		Add	

This collection of information is required by 37 CFR 1.114. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal	
Application Number:	16752650
Filing Date:	26-Jan-2020
Title of Invention:	CHIP PACKAGE
First Named Inventor/Applicant Name:	Ping-Jung Yang
Filer:	Ping-Jung. Yang
Attorney Docket Number:	Mars16-001-US-C01
Filed as Small Entity	
Filing Fees for Utility under 35 USC 111(a)	

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
RCE- 2ND AND SUBSEQUENT REQUEST	2820	1	1000	1000
		Total in USD ($)		**1000**

Electronic Acknowledgement Receipt	
EFS ID:	43076934
Application Number:	16752650
International Application Number:	
Confirmation Number:	4809
Title of Invention:	CHIP PACKAGE
First Named Inventor/Applicant Name:	Ping-Jung Yang
Customer Number:	102851
Filer:	Ping-Jung. Yang
Filer Authorized By:	
Attorney Docket Number:	Mars16-001-US-C01
Receipt Date:	24-JUN-2021
Filing Date:	26-JAN-2020
Time Stamp:	11:40:18
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		Mars16-001-US-C01-RCE-06232021-v2.pdf	489415 62b7f3e51626cf9449c989b76db718f07b42146f	yes	11

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Amendment Submitted/Entered with Filing of CPA/RCE	1	1
	Claims	2	9
	Applicant Arguments/Remarks Made in an Amendment	10	11

Warnings:					
Information:					
2	Request for Continued Examination (RCE)	Mars16-001-US-C01-RCE-06242021.pdf	1349960 6b5b853349ae2a524ffbe4ad10731006901a8e90	no	3
Warnings:					
Information:					
3	Fee Worksheet (SB06)	fee-info.pdf	29929 604cc7ef3a5f85e1e4dbd819f4e195d01b730273	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	1869304		

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Docket No.: Mars-16-001-US-C01 **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	Customer Number: 102851
Ping-Jung Yang	:	Confirmation Number: 4809
Application No.: 16752650	:	Group Art Unit: 2812
Filed: Jan. 26, 2020	:	Examiner: LIU, XIAOMING

For: CHIP PACKAGE

AMENDMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Please amend the above-identified application and consider the remarks as follows:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks/Arguments begin on page 10 of this paper.

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Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

What is claimed is:

Claims 1-20 Cancelled

21. (Previously presented) A chip package comprising:

a first polymer layer having a first surface and a second surface opposite to said first surface, wherein said first surface is substantially parallel to said second surface, wherein said first polymer layer has a thickness between 100 and 300 micrometers and has a coefficient of expansion between 3 and 10 ppm/°C;

a first metal plug vertically in a first through via in said first polymer layer, wherein said first metal plug comprises a first copper layer, wherein the first copper layer contacts with a sidewall of said first through via;

a second metal plug vertically in a second through via in said first polymer layer, wherein said second metal plug comprises a second copper layer, wherein a top surface of said second metal plug and a top surface of said first metal plug are in the same horizontal plane;

a first interconnection scheme over said first surface, wherein said first interconnection scheme comprises a first metal interconnect over said first surface, a second metal interconnect over said first surface, a third metal interconnect over said first surface and a second polymer layer over said first, second and third metal interconnects, wherein said first metal interconnect is connected to

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TSMC EX1032 Page 590

said first metal plug, wherein said second metal interconnect is connected to said second metal plug, wherein said first metal interconnect comprises a first metal layer, a third copper layer on said first metal layer, and a fourth copper layer on said third copper layer;

a first metal bump over said first interconnection scheme and said second metal plug, wherein said first metal bump comprises a tin-containing layer; and

a first semiconductor chip under said first interconnection scheme, wherein said first semiconductor chip comprises a fourth metal interconnect on a first metal pad of said first semiconductor chip, wherein said fourth metal interconnect comprises a second metal layer on said first metal pad and a fifth copper layer over said second metal layer, wherein said fifth copper layer has a thickness between 5 and 30 micrometers, wherein said fourth metal interconnect is connected to said third metal interconnect.

22. (Previously presented) The chip package of claim 21, further comprising a passive component over said first interconnection scheme and connected to said first interconnection scheme through a solder layer.

23. (Previously presented) The chip package of claim 21, wherein said first interconnection scheme comprise a fifth metal interconnect across over a sidewall of the first semiconductor chip.

24. (Previously presented) The chip package of claim 21, further comprising a second semiconductor chip over said first interconnection scheme, wherein said second semiconductor chip comprises a second metal bump between said second semiconductor chip and said first interconnection scheme.

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25. (Previously presented) The chip package of claim 21, wherein said first semiconductor chip comprises a central-processing-unit (CPU) circuit block and a graphics-processing-unit (GPU) circuit block.

26. (Previously presented) The chip package of claim 21, wherein said first semiconductor chip comprises a second metal pad on a top surface of said first semiconductor chip and a third metal pad on a bottom surface of said first semiconductor chip, wherein said second metal pad is connected to said third metal pad through a through-silicon-via metal layer.

27. (Previously presented) The chip package of claim 21, wherein said first interconnection scheme further comprises a fifth metal interconnect over said first metal interconnect and said second polymer layer, wherein said second polymer is between said first and fifth metal interconnects, wherein said fifth metal interconnect comprises a third metal layer, a sixth copper layer on said third metal layer, and a seventh copper layer on said sixth copper layer.

28. (Previously presented) The chip package of claim 21, further comprising a second interconnection scheme under said first polymer layer and on said second surface.

29. (Previously presented) The chip package of claim 21, wherein said first metal plugs has a top surface substantially coplanar with said first surface.

30. (Previously presented) The chip package of claim 21, wherein said first metal pad is an aluminum pad.

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31. (Previously presented) A chip package comprising:

a first polymer layer having a first surface, a second surface opposite to said first surface, wherein said first surface is substantially parallel to said second surface, wherein said first polymer layer has a thickness between 100 and 300 micrometers;

a first metal plug vertically in a first through via in said first polymer layer, wherein said first metal plug comprises a first copper layer, wherein the first copper layer contacts with a sidewall of said first through via;

a second metal plug vertically in a second through via in said first polymer layer, wherein said second metal plug comprises a second copper layer, wherein a top surface of said second metal plug and a top surface of said first metal plug are in the same horizontal plane;

a first interconnection scheme over said first surface, wherein said first interconnection scheme comprises a first metal interconnect over said first surface, a second metal interconnect over said first surface and a second polymer layer over said first and second metal interconnects, wherein said first metal interconnect is connected to said first metal plug, wherein said first metal interconnect comprises a first metal layer, a third copper layer on said first metal layer, and a fourth copper layer on said third copper layer;

a first metal bump over said first interconnection scheme, wherein said first metal bump is connected to said first interconnection scheme through a first opening in said second polymer layer, wherein said first metal bump comprises a tin-containing layer;

a second metal bump over said first interconnection scheme, wherein said second metal bump is connected to said first interconnection scheme through a second opening in said second polymer layer;

a first semiconductor chip over said first interconnection scheme and between said first and second metal bumps;

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a third metal bump between said first semiconductor chip and said first interconnection scheme, wherein said third metal bump connected to said second metal interconnect through a third opening in said second polymer layer; and

a second semiconductor chip under said first interconnection scheme and said first semiconductor chip, wherein said first interconnection scheme is between said first and second semiconductor chips, wherein said second semiconductor chip comprises a central-processing-unit (CPU) circuit block and a graphics-processing-unit (GPU) circuit block.

32. (Previously presented) The chip package of claim 31, further comprising a third semiconductor chip over said first interconnection scheme.

33. (Previously presented) The chip package of claim 31, wherein said second semiconductor chip comprises a first metal pad on a top surface of said second semiconductor chip and a second metal pad on a bottom surface of said second semiconductor chip, wherein said first metal pad is connected to said second metal pad through a through-silicon-via metal layer.

34. (Previously presented) The chip package of claim 31, further comprising a third metal plug vertically in a third through via in said first polymer layer, wherein a pitch between said first and third metal plugs is between 200 and 1000 micrometers.

35. (Previously presented) The chip package of claim 31, wherein said first polymer layer has a coefficient of expansion between 3 and 10 ppm/°C .

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36. (Previously presented) The chip package of claim 31, further comprising a third semiconductor chip under said second semiconductor chip and multiple fourth metal bumps between said second and third semiconductor chips, wherein said second semiconductor chip comprises a first metal pad on a top surface of said second semiconductor chip and a second metal pad on a bottom surface of said second semiconductor chip, wherein said first metal pad is connected to said second metal pad through a through-silicon-via metal layer.

37. (Currently amended) The chip package of claim 31, further comprising a passive component over said first ~~interconnection scheme~~ surface.

38. (Previously presented) The chip package of claim 31, wherein said first interconnection scheme comprise a third metal interconnect across over a sidewall of the second semiconductor chip.

39. (Previously presented) The chip package of claim 31, further comprising a third semiconductor chip under said first interconnection scheme, wherein said third semiconductor chip is a memory chip.

40. (Previously presented) The chip package of claim 31, wherein said second semiconductor chip comprises a third metal interconnect on a metal pad of said second semiconductor chip, wherein said third metal interconnect comprises a second metal layer on said metal pad and a fifth copper layer over said second metal layer, wherein said fifth copper layer has a thickness between 5 and 30 micrometers, wherein said third metal interconnect is connected to said a fourth metal interconnect of said first interconnection scheme.

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41. (Previously presented) The chip package of claim 21, further comprising a second semiconductor chip over said first interconnection scheme and connected to said first interconnection scheme through a second metal bump, wherein said second semiconductor chip has a height is between a backside surface of said second semiconductor chip and a top surface of said second polymer layer is smaller than a thickness of said first metal bump.

42. (Previously presented) The chip package of claim 21, further comprising a second semiconductor chip under said first semiconductor chip, wherein said first semiconductor chip comprise a second metal pad connected to a third metal pad of said second semiconductor chip through a solder layer, wherein said solder layer between said first and second semiconductor chips.

43. (Currently amended) The chip package of claim 21, further comprising a second semiconductor chip ~~over~~ under said first ~~interconnection scheme~~semiconductor chip, wherein said first semiconductor chip comprises a ~~central processing unit (CPU) circuit block and a graphics processing unit (GPU) circuit block~~ second metal pad on a top surface of said first semiconductor chip, a third metal pad on a bottom surface of said first semiconductor chip and a through-silicon-via metal layer connects to said second metal pad, wherein said third metal pad is connected to a fourth metal pad of said second semiconductor chip.

44. (Previously presented) The chip package of claim 21, further comprising a third metal plug vertically in a third through via in said first polymer layer, wherein a pitch between said first and third metal plugs is between 200 and 1000 micrometers.

45. (Previously presented) The chip package of claim 31, wherein a height is between a backside surface of said first semiconductor chip and a top surface of said second polymer layer is smaller than a thickness of said first metal bump.

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TSMC EX1032 Page 596

46. (Previously presented) The chip package of claim 31, wherein said second semiconductor chip is coupled to said first semiconductor chip through said first interconnection scheme.

47. (Previously presented) The chip package of claim 21, wherein said first metal plug has a thickness between 100 and 300 micrometers.

48. (Previously presented) The chip package of claim 31, wherein said first metal plug has a thickness between 100 and 300 micrometers.

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TSMC EX1032 Page 597

REMARKS/ARGUMENTS

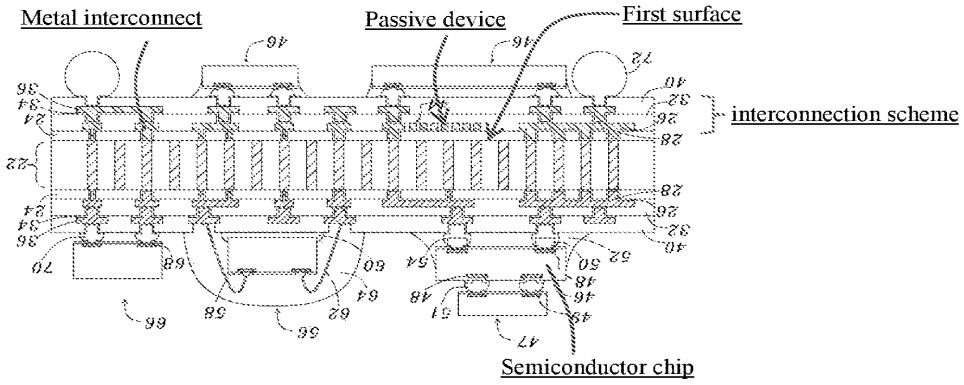
Claims 1-20 are cancelled. Claims 21-48 are pending in the application, of which claims 21 and 31 are the pending independent claims. No new matter is believed to be added into the application by this paper.

Other Amendments

The condition/item of the "coefficient of expansion between 3 and 10 ppm/°C" in claims 21 and 35 is disclosed in the Non-Provisional patent application of application No. 14/036256, filed Sept. 25, 2013, not disclosed in the provisional patent application No. 61/705,649, filed Sept. 26, 2012. The applicant apologizes for this error. Please review and examine the claim 21 according to the revised condition/item. However, the applicant still believes the claim 21 can overcome previous references or prior arts.

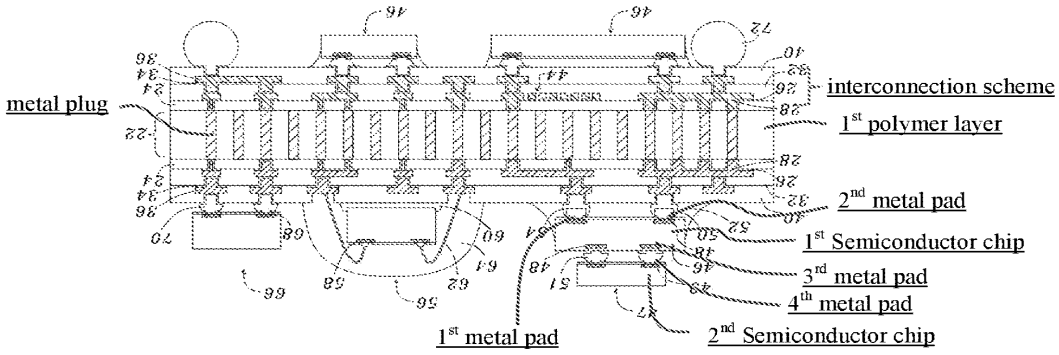
Claim Amendments

For claim 37 the subject matter that "a passive component over said first surface" (claim 37) is disclosed and supported in Fig. 18y of the non-provisional App. No. 14/036256, filed Sept. 25, 2013, (and disclosed and supported in Fig. 9x of the non-provisional App. No. 15/261956, filed on Sept. 11, 2016), as below:



For claim 43 the subject matter that "a second semiconductor chip under said first semiconductor chip, wherein said first semiconductor chip comprises a second metal pad on a top surface of said first semiconductor chip, a third metal pad on a bottom surface of said first semiconductor chip and a through-silicon-via metal layer connects to said second metal pad, wherein said third metal pad is connected to a fourth metal pad of said second semiconductor chip" (claim 43) is disclosed and supported in Fig. 18y and paragraph [0087] of the non-provisional App. No. 14/036256, filed Sept. 25, 2013, (and disclosed and supported in Fig. 9x and paragraph [0105] of the non-provisional App. No. 15/261956, filed on Sept. 11, 2016), as below:

[0087] .... The metal pads 48 of the top surface of the chip 46 are connected to the metal pads 48 of the bottom surface of the chip 46 through multiple through-silicon-via metal layers,....



Respectfully submitted,

Mars Yang

Date: __2021-06-24_____
Email: semars3898@gmail.com

Ping-Jung Yang

Electronic Patent Application Fee Transmittal	
Application Number:	16752650
Filing Date:	26-Jan-2020
Title of Invention:	CHIP PACKAGE
First Named Inventor/Applicant Name:	Ping-Jung Yang
Filer:	Ping-Jung. Yang
Attorney Docket Number:	Mars16-001-US-C01
Filed as Small Entity	
Filing Fees for Utility under 35 USC 111(a)	

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
RCE- 2ND AND SUBSEQUENT REQUEST	2820	1	1000	1000
		Total in USD ($)		**1000**

Electronic Acknowledgement Receipt	
EFS ID:	43078676
Application Number:	16752650
International Application Number:	
Confirmation Number:	4809
Title of Invention:	CHIP PACKAGE
First Named Inventor/Applicant Name:	Ping-Jung Yang
Customer Number:	102851
Filer:	Ping-Jung. Yang
Filer Authorized By:	
Attorney Docket Number:	Mars16-001-US-C01
Receipt Date:	24-JUN-2021
Filing Date:	26-JAN-2020
Time Stamp:	13:11:46
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$1000
RAM confirmation Number	E20216ND13401640
Deposit Account	
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Fee Worksheet (SB06)	fee-info.pdf	29929 5b9a88b49a7853a22078c35c63db213d0ef10130	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	29929		

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New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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NOTICE OF ALLOWANCE AND FEE(S) DUE

102851 7590 07/09/2021

PING-JUNG YANG
NO 2, NIOUPU SOUTH RD., SIANGSHAN DISTRICT
HSINCHU CITY, 30091
TAIWAN

EXAMINER	
LIU, XIAOMING	
ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 07/09/2021

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/752,650	01/26/2020	Ping-Jung Yang	Mars16-001-US-C01	4809

TITLE OF INVENTION: CHIP PACKAGE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	$600	$0.00	$0.00	$600	10/12/2021

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Maintenance fees are due in utility patents issuing on applications filed on or after Dec. 12, 1980. It is patentee's responsibility to ensure timely payment of maintenance fees when due. More information is available at www.uspto.gov/PatentMaintenanceFees.

PTOL-85 (Rev. 02/11)

IPR2026-00067
TSMC EX1032 Page 604

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via EFS-Web.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

102851 7590 07/09/2021

PING-JUNG YANG
NO 2, NIOUPU SOUTH RD., SIANGSHAN DISTRICT
HSINCHU CITY, 30091
TAIWAN

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via EFS-Web or by facsimile to (571) 273-2885, on the date below.

(Typed or printed name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/752,650	01/26/2020	Ping-Jung Yang	Mars16-001-US-C01	4809

TITLE OF INVENTION: CHIP PACKAGE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	$600	$0.00	$0.00	$600	10/12/2021

EXAMINER	ART UNIT	CLASS-SUBCLASS
LIU, XIAOMING	2812	257-091000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-09 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. Fees submitted: ❑Issue Fee ❑Publication Fee (if required) ❑Advance Order - # of Copies _____

4b. Method of Payment: *(Please first reapply any previously paid fee shown above)*

❑ Electronic Payment via EFS-Web ❑ Enclosed check ❑ Non-electronic payment by credit card (Attach form PTO-2038)

❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. _____

5. **Change in Entity Status** (from status indicated above)

❑ Applicant certifying micro entity status. See 37 CFR 1.29

❑ Applicant asserting small entity status. See 37 CFR 1.27

❑ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

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UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/752,650	01/26/2020	Ping-Jung Yang	Mars16-001-US-C01	4809

102851 7590 07/09/2021

PING-JUNG YANG
NO 2, NIOUPU SOUTH RD., SIANGSHAN DISTRICT
HSINCHU CITY, 30091
TAIWAN

EXAMINER	
LIU, XIAOMING	
ART UNIT	**PAPER NUMBER**
2812	

DATE MAILED: 07/09/2021

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

PTOL-85 (Rev. 02/11)

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OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 16/752,650	Applicant(s) Yang, Ping-Jung	
	Examiner XIAOMING LIU	Art Unit 2812	AIA (FITF) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☑ This communication is responsive to 6/24/2021.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☑ The allowed claim(s) is/are 21-48 . As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see **http://www.uspto.gov/patents/init_events/pph/index.jsp** or send an inquiry to **PPHfeedback@uspto.gov.**

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some *c) ☐ None of the:

   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____ .

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____ .

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____.
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material _____.
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date. _____.
5. ☐ Examiner's Amendment/Comment
6. ☑ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/XIAOMING LIU/
Examiner, Art Unit 2812

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DETAILED ACTION

The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 6/24/2021 has been entered.

Allowable Subject Matter

Claims 21-48 are allowed.

The following is an examiner's statement of reasons for allowance: currently independent claims 21 and 31 are allowable because the closest prior art does not appear to disclose, alone or in combination, the limitations of material and structure of the chip package in combination with the other required elements of claim 21 or 31.

Specifically, the limitations are material to the inventive concept of the application in hand to forming a polymer interconnect with sufficient coefficient of expansion to enable holes and other features formed inside with improved chemical durability, strength and optical properties.

Dependent claims 22-30 and 32-48 are respectively dependent on currently amended allowable independent claims 21 or 31. Therefore, claims 22-30 and 32-48 incorporate the allowable limitations of claims 21 or 31. Consequently, claims 22-30 and 32-48 are allowable.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to XIAOMING LIU whose telephone number is (571)270-0384. The examiner can normally be reached on Monday-Friday, 9am-8pm, EST.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Charles Garber can be reached on (571)272-2194. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see https://ppair-my.uspto.gov/pair/PrivatePair. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/XIAOMING LIU/
Examiner, Art Unit 2812

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/752,650	Yang, Ping-Jung
	Examiner	Art Unit
	XIAOMING LIU	2812

CPC - Searched*		
Symbol	**Date**	**Examiner**
H01L23/49827 | H01L23/5384 | H01L2224/08165 | H01L2224/16165 | H01L2224/16235 | H01L2224/32165 | H01L2224/32235 | H01L2224/40165 | H01L2224/40235 | H01L2224/48165 | H01L2224/48235 with date and text	09/17/2020	XL

CPC Combination Sets - Searched*		
Symbol	**Date**	**Examiner**

US Classification - Searched*			
Class	**Subclass**	**Date**	**Examiner**

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	**Date**	**Examiner**
Searched East: (USPAT, USPGPUB, USOCR, FPRS, EPO, JPO, DERWENT, IBMTDB)	09/17/2020	XL
Inventor search Conducted, limited with text	09/17/2020	XL
Assignee search Conducted, limited with text	09/17/2020	XL
Google text search conducted	09/17/2020	XL
Non-Patent Literature searched: science direct, TC2800	09/17/2020	XL
updated search	04/22/2021	XL
updated search	06/05/2021	XL
updated search	07/02/2021	XL

/XIAOMING LIU/ Examiner, Art Unit 2812	

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Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/752,650	Yang, Ping-Jung
	Examiner	Art Unit
	XIAOMING LIU	2812

Interference Search			
US Class/CPC Symbol	**US Subclass/CPC Group**	**Date**	**Examiner**
H01L23	49827 53840 with text	06/17/2021	XL
H01L2224	08165 16165 16235 32165 40165 40235 48165 48235 with text	06/17/2021	XL
	all CPC group with text	06/17/2021	XL

/XIAOMING LIU/ Examiner, Art Unit 2812	

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Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/752,650	Yang, Ping-Jung
	Examiner	**Art Unit**
	XIAOMING LIU	2812

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H01L	/	23	/	49833	I	2013-01-01
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NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	28	
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(Primary Examiner)	(Date)	21	fig17b

U.S. Patent and Trademark Office — Part of Paper No.: 20210702

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Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/752,650	Yang, Ping-Jung
	Examiner	**Art Unit**
	XIAOMING LIU	2812

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C09K	/	2323	/	03	A	2020-08-01

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	28	
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(Primary Examiner)	(Date)	21	fig17b

U.S. Patent and Trademark Office — Part of Paper No.: 20210702

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Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/752,650	Yang, Ping-Jung
	Examiner	Art Unit
	XIAOMING LIU	2812

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NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	28	
/XIAOMING LIU/ Examiner, Art Unit 2812	02 July 2021	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	21	fig17b

U.S. Patent and Trademark Office — Part of Paper No.: 20210702

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Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/752,650	Yang, Ping-Jung
	Examiner	**Art Unit**
	XIAOMING LIU	2812

CPC Combination Sets								
Symbol					**Type**	**Set**	**Ranking**	**Version**
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H01L	/	2924	/	01047	A	22	2	2013-01-01
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NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	28	
/XIAOMING LIU/ Examiner, Art Unit 2812	02 July 2021	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	21	fig17b

U.S. Patent and Trademark Office — Part of Paper No.: 20210702

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TSMC EX1032 Page 616

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/752,650	Yang, Ping-Jung
	Examiner	Art Unit
	XIAOMING LIU	2812

CPC Combination Sets								
Symbol					Type	Set	Ranking	Version
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H01L	/	2224	/	13005	A	25	1	2013-01-01
H01L	/	2924	/	206	A	25	2	2013-01-01
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H01L	/	2924	/	207	A	26	2	2013-01-01
H01L	/	2224	/	03462	A	27	1	2013-01-01
H01L	/	2924	/	00014	A	27	2	2013-01-01
H01L	/	2224	/	1146	A	28	1	2013-01-01
H01L	/	2924	/	00014	A	28	2	2013-01-01
H01L	/	2224	/	11334	A	29	1	2013-01-01
H01L	/	2924	/	00014	A	29	2	2013-01-01
H01L	/	2224	/	11462	A	30	1	2013-01-01
H01L	/	2924	/	00014	A	30	2	2013-01-01
H01L	/	2224	/	05624	A	31	1	2013-01-01
H01L	/	2924	/	00014	A	31	2	2013-01-01
H01L	/	2224	/	45144	A	32	1	2013-01-01
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H01L	/	2924	/	00	A	34	2	2013-01-01
H01L	/	2924	/	181	A	35	1	2013-01-01
H01L	/	2924	/	00012	A	35	2	2013-01-01
H01L	/	2224	/	13111	A	36	1	2013-01-01
H01L	/	2924	/	01047	A	36	2	2013-01-01
H01L	/	2924	/	01029	A	36	3	2013-01-01
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H01L	/	2224	/	48465	A	37	1	2013-01-01

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	28	
/XIAOMING LIU/ Examiner, Art Unit 2812	02 July 2021	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	21	fig17b

U.S. Patent and Trademark Office — Part of Paper No.: 20210702

IPR2026-00067
TSMC EX1032 Page 617

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/752,650	Yang, Ping-Jung
	Examiner	**Art Unit**
	XIAOMING LIU	2812

CPC Combination Sets								
Symbol					**Type**	**Set**	**Ranking**	**Version**
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H01L	/	2224	/	13144	A	41	1	2013-01-01
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NONE		**Total Claims Allowed:**	
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(Primary Examiner)	(Date)	21	fig17b

U.S. Patent and Trademark Office — Part of Paper No.: 20210702

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Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/752,650	Yang, Ping-Jung
	Examiner	**Art Unit**
	XIAOMING LIU	2812

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CLAIMED					
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H01L23/15	/	23	/	15	
H01L23/498	/	23	/	498	

NON-CLAIMED				
	/		/	

US ORIGINAL CLASSIFICATION	
CLASS	**SUBCLASS**

CROSS REFERENCES(S)						
CLASS	**SUBCLASS (ONE SUBCLASS PER BLOCK)**					

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	28	
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(Primary Examiner)	(Date)	21	fig17b

U.S. Patent and Trademark Office — Part of Paper No.: 20210702

IPR2026-00067
TSMC EX1032 Page 619

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/752,650	Yang, Ping-Jung
	Examiner	**Art Unit**
	XIAOMING LIU	2812

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIMS

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
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	2		11		20	9	29	23	38	15	47				
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	4		13	2	22	16	31	25	40						
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NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	28	
/XIAOMING LIU/ Examiner, Art Unit 2812	02 July 2021	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	21	fig17b

U.S. Patent and Trademark Office Part of Paper No.: 20210702

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TSMC EX1032 Page 620

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
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		or US-20090256670-$ or US-20080150119-$ or US-20050253231-$ or US-20030096089-$ or US-20150342060-$ or US-20120094442-$ or US-20110115083-$ or US-20140217436-$ or US-20140048949-$ or US-20130214386-$ or US-20120086117-$ or US-20120049363-$ or US-20120032282-$ or US-20140264810-$ or US-20120160647-$ or US-20100000775-$ or US-20070243704-$ or US-20050090035-$ or US-20050151272-$ or US-20100019373-$ or US-20140118978-$ or US-20120293977-$ or US-20110227223-$ or US-20090236730-$ or US-20080049392-$).did. or (US-20090096070-$ or US-20130168857-$ or US-20110309526-$ or US-20080211111-$ or US-20080277802-$ or US-20070080469-$ or US-20140246223-$ or US-20150162194-$ or US-20160343592-$ or US-20140054796-$ or US-20130343067-$ or US-20130017652-$ or US-20120306104-$ or US-20120019123-$ or US-20110291541-$ or US-20110222280-$ or US-20100171139-$ or US-20120305977-$ or US-20150021754-$ or US-20110121449-$ or US-20150221614-$ or US-20130200531-$ or US-20130062761-$ or US-20120028411-$ or US-20130295725-$ or US-20060194370-$ or US-20080212288-$).did. or (US-7589405-$ or US-8906794-$ or US-6614122-$ or US-8558399-$ or US-8432022-$ or US-8228682-$ or US-8982577-$ or US-4706167-$ or US-5531020-$ or US-8252615-$ or US-6331451-$ or US-8946886-$ or US-8415785-$ or US-5804881-$ or US-9786623-$ or US-9040352-$ or US-7855391-$ or US-8507927-$ or US-7619901-$ or US-9768038-$ or US-9627261-$ or US-5250843-$ or US-9735113-$ or US-9431316-$ or US-8617935-$ or US-8518749-$).did. or (US-8482134-$ or US-8258012-$ or US-8105872-$ or US-7955942-$ or US-7846777-$ or US-7727806-$).did.				

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S48	537	S47 and cpu same gpu same DRAM	US-PGPUB; USPAT; USOCR	OR	OFF	2020/09/11 11:06
S49	127	S47 and cpu same gpu same DRAM and integration	US-PGPUB; USPAT; USOCR	OR	OFF	2020/09/11 11:06
S50	20,179	(H01L23/49827 | H01L23/5384 | H01L2224/08165 | H01L2224/16165 | H01L2224/16235 | H01L2224/32165 | H01L2224/32235 | H01L2224/40165 | H01L2224/40235 | H01L2224/48165 | H01L2224/48235).CPC.	US-PGPUB; USPAT; USOCR	OR	OFF	2020/09/11 13:47
S51	146	S50 and tsv same layout	US-PGPUB; USPAT; USOCR	OR	OFF	2020/09/11 13:47
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S53	71	(US-20110304008-$ or US-20120313207-$ or US-20120241938-$ or US-20120193785-$ or US-20120052631-$ or US-20110297434-$ or US-20110026232-$ or US-20100290191-$ or US-20100207154-$ or US-20100200898-$ or US-20100102457-$ or US-20100044850-$ or US-20090315171-$ or US-20110110061-$ or US-20100123257-$ or US-20100052119-$ or US-20090184403-$ or US-20120326170-$ or US-20130050228-$ or US-20130049217-$ or US-20120313209-$ or US-20120306096-$ or US-20120228749-$ or US-20140124777-$ or US-20140042637-$ or US-20130328211-$).did. or (US-20130292844-$ or US-20130119562-$ or US-20100258944-$ or US-20100258946-$ or US-20100252937-$ or US-20080149384-$ or US-	US-PGPUB; USPAT	OR	ON	2021/04/22 11:47

		20130277855-$ or US-20170373004-$ or US-20170345761-$ or US-20130242493-$ or US-20100252934-$).did. or (US-9437534-$ or US-8247269-$ or US-8614120-$ or US-7968978-$ or US-9627365-$ or US-9817312-$ or US-9615453-$ or US-9363890-$ or US-9161443-$ or US-9030751-$ or US-8354304-$ or US-8273602-$ or US-8270176-$ or US-8263434-$ or US-8217514-$ or US-8193036-$ or US-8133762-$ or US-8110440-$ or US-8110908-$ or US-8105915-$ or US-8080445-$ or US-8067308-$ or US-8067828-$ or US-8067275-$ or US-8063477-$ or US-8034661-$).did. or (US-8008121-$ or US-7977802-$ or US-7935570-$ or US-7880293-$ or US-7858441-$ or US-7842542-$ or US-7838337-$ or US-7790503-$).did.				
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S56	2	("20200161245").PN.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2021/04/22 11:48
S57	2	("20140085842").PN.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2021/04/22 12:22
S58	3	"20110147055"	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2021/04/22 12:24
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S70	13	("2011/0304008").URPN.	USPAT	OR	ON	2021/06/04 14:21
S71	130	("2012/0193785").URPN.	USPAT	OR	ON	2021/06/04 17:27
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S77	5	"20100140779"	US-PGPUB; USPAT; USOCR; FPRS; EPO;	OR	ON	2021/06/05 19:45

			JPO; DERWENT; IBM_TDB			
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S79	1	"10622310".pn.	US-PGPUB; USPAT	OR	OFF	2021/06/05 23:41

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S59	10,057	(H01L23/49827 | H01L23/5384 | H01L2224/08165 | H01L2224/16165 | H01L2224/16235 | H01L2224/32165 | H01L2224/32235 | H01L2224/40165 | H01L2224/40235 | H01L2224/48165 | H01L2224/48235).CPC.	USPAT	OR	OFF	2021/04/22 11:37
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7/2/2021 4:26:11 PM
C:\Users\xliu3\Documents\EAST\Workspaces\202001\16752650_1.wsp

Bibliographic Data

Application No: 16/752,650

Foreign Priority claimed: ○ Yes ◉ No

35 USC 119 (a-d) conditions met: ☐ Yes ☑ No ☐ Met After Allowance

Verified and Acknowledged: /XIAOMING LIU/ (Examiner's Signature) | (Initials)

Title: CHIP PACKAGE

FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
01/26/2020	257	2812	Mars16-001-US-C01
RULE			

APPLICANTS

Ping-Jung Yang, Hsin-Chu City, TAIWAN

INVENTORS

Ping-Jung Yang, Hsinchu City, TAIWAN

CONTINUING DATA

This application is a CON of 15261956 09/11/2016 PAT 10622310

15261956 has PRO of 62219249 09/16/2015

15261956 is a CIP of 14036256 09/25/2013 PAT 9615453

14036256 has PRO of 61705649 09/26/2012

FOREIGN APPLICATIONS

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TAIWAN

FILING FEE RECEIVED

$785

Docket No.: Mars-16-001-US-C01 **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	Customer Number: 102851
Ping-Jung Yang	:	Confirmation Number: 4809
Application No.: 16752650	:	Group Art Unit: 2812
Filed: Jan. 26, 2020	:	Examiner: LIU, XIAOMING

For: CHIP PACKAGE

AMENDMENT AFTER ALLOWANCE UNDER 37 CFR §1.312

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Commissioner:

Pursuant to amendments after allowance under 37 CFR §1.312, Applicants hereby respectfully submit this paper and request to amend claim 1 of the above-identified application in the manner presented hereafter. The amendments embody merely the correction of formal matters in the claims without changing the scopes thereof.

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks/Arguments are beginning on page 10 of this paper.

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Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

What is claimed is:

Claims 1-20 Cancelled

21. (Previously presented) A chip package comprising:

a first polymer layer having a first surface and a second surface opposite to said first surface, wherein said first surface is substantially parallel to said second surface, wherein said first polymer layer has a thickness between 100 and 300 micrometers and has a coefficient of expansion between 3 and 10 ppm/°C;

a first metal plug vertically in a first through via in said first polymer layer, wherein said first metal plug comprises a first copper layer, wherein the first copper layer contacts with a sidewall of said first through via;

a second metal plug vertically in a second through via in said first polymer layer, wherein said second metal plug comprises a second copper layer, wherein a top surface of said second metal plug and a top surface of said first metal plug are in the same horizontal plane;

a first interconnection scheme over said first surface, wherein said first interconnection scheme comprises a first metal interconnect over said first surface, a second metal interconnect over said first surface, a third metal interconnect over said first surface and a second polymer layer over said first, second and third metal interconnects, wherein said first metal interconnect is connected to

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said first metal plug, wherein said second metal interconnect is connected to said second metal plug, wherein said first metal interconnect comprises a first metal layer, a third copper layer on said first metal layer, and a fourth copper layer on said third copper layer;

a first metal bump over said first interconnection scheme and said second metal plug, wherein said first metal bump comprises a tin-containing layer; and

a first semiconductor chip under said first interconnection scheme, wherein said first semiconductor chip comprises a fourth metal interconnect on a first metal pad of said first semiconductor chip, wherein said fourth metal interconnect comprises a second metal layer on said first metal pad and a fifth copper layer over said second metal layer, wherein said fifth copper layer has a thickness between 5 and 30 micrometers, wherein said fourth metal interconnect is connected to said third metal interconnect.

22. (Previously presented) The chip package of claim 21, further comprising a passive component over said first interconnection scheme and connected to said first interconnection scheme through a solder layer.

23. (Previously presented) The chip package of claim 21, wherein said first interconnection scheme comprise a fifth metal interconnect across over a sidewall of the first semiconductor chip.

24. (Previously presented) The chip package of claim 21, further comprising a second semiconductor chip over said first interconnection scheme, wherein said second semiconductor chip comprises a second metal bump between said second semiconductor chip and said first interconnection scheme.

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25. (Previously presented) The chip package of claim 21, wherein said first semiconductor chip comprises a central-processing-unit (CPU) circuit block and a graphics-processing-unit (GPU) circuit block.

26. (Previously presented) The chip package of claim 21, wherein said first semiconductor chip comprises a second metal pad on a top surface of said first semiconductor chip and a third metal pad on a bottom surface of said first semiconductor chip, wherein said second metal pad is connected to said third metal pad through a through-silicon-via metal layer.

27. (Previously presented) The chip package of claim 21, wherein said first interconnection scheme further comprises a fifth metal interconnect over said first metal interconnect and said second polymer layer, wherein said second polymer is between said first and fifth metal interconnects, wherein said fifth metal interconnect comprises a third metal layer, a sixth copper layer on said third metal layer, and a seventh copper layer on said sixth copper layer.

28. (Previously presented) The chip package of claim 21, further comprising a second interconnection scheme under said first polymer layer and on said second surface.

29. (Previously presented) The chip package of claim 21, wherein said first metal plugs has a top surface substantially coplanar with said first surface.

30. (Previously presented) The chip package of claim 21, wherein said first metal pad is an aluminum pad.

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31. (Currently amended) A chip package comprising:

a first polymer layer having a first surface[[,]] and a second surface opposite to said first surface, wherein said first surface is substantially parallel to said second surface, wherein said first polymer layer has a thickness between 100 and 300 micrometers;

a first metal plug vertically in a first through via in said first polymer layer, wherein said first metal plug comprises a first copper layer, wherein the first copper layer contacts with a sidewall of said first through via;

a second metal plug vertically in a second through via in said first polymer layer, wherein said second metal plug comprises a second copper layer, wherein a top surface of said second metal plug and a top surface of said first metal plug are in the same horizontal plane;

a first interconnection scheme over said first surface, wherein said first interconnection scheme comprises a first metal interconnect over said first surface, a second metal interconnect over said first surface and a second polymer layer over said first and second metal interconnects, wherein said first metal interconnect is connected to said first metal plug, wherein said first metal interconnect comprises a first metal layer, a third copper layer on said first metal layer, and a fourth copper layer on said third copper layer;

a first metal bump over said first interconnection scheme, wherein said first metal bump is connected to said first interconnection scheme through a first opening in said second polymer layer, wherein said first metal bump comprises a tin-containing layer;

a second metal bump over said first interconnection scheme, wherein said second metal bump is connected to said first interconnection scheme through a second opening in said second polymer layer;

a first semiconductor chip over said first interconnection scheme and between said first and second metal bumps;

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a third metal bump between said first semiconductor chip and said first interconnection scheme, wherein said third metal bump connected to said second metal interconnect through a third opening in said second polymer layer; and

a second semiconductor chip under said first interconnection scheme and said first semiconductor chip, wherein said first interconnection scheme is between said first and second semiconductor chips, wherein said second semiconductor chip comprises a central-processing-unit (CPU) circuit block and a graphics-processing-unit (GPU) circuit block.

32. (Previously presented) The chip package of claim 31, further comprising a third semiconductor chip over said first interconnection scheme.

33. (Previously presented) The chip package of claim 31, wherein said second semiconductor chip comprises a first metal pad on a top surface of said second semiconductor chip and a second metal pad on a bottom surface of said second semiconductor chip, wherein said first metal pad is connected to said second metal pad through a through-silicon-via metal layer.

34. (Previously presented) The chip package of claim 31, further comprising a third metal plug vertically in a third through via in said first polymer layer, wherein a pitch between said first and third metal plugs is between 200 and 1000 micrometers.

35. (Previously presented) The chip package of claim 31, wherein said first polymer layer has a coefficient of expansion between 3 and 10 ppm/°C .

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36. (Previously presented) The chip package of claim 31, further comprising a third semiconductor chip under said second semiconductor chip and multiple fourth metal bumps between said second and third semiconductor chips, wherein said second semiconductor chip comprises a first metal pad on a top surface of said second semiconductor chip and a second metal pad on a bottom surface of said second semiconductor chip, wherein said first metal pad is connected to said second metal pad through a through-silicon-via metal layer.

37. (Previously presented) The chip package of claim 31, further comprising a passive component over said first surface.

38. (Previously presented) The chip package of claim 31, wherein said first interconnection scheme comprise a third metal interconnect across over a sidewall of the second semiconductor chip.

39. (Previously presented) The chip package of claim 31, further comprising a third semiconductor chip under said first interconnection scheme, wherein said third semiconductor chip is a memory chip.

40. (Previously presented) The chip package of claim 31, wherein said second semiconductor chip comprises a third metal interconnect on a metal pad of said second semiconductor chip, wherein said third metal interconnect comprises a second metal layer on said metal pad and a fifth copper layer over said second metal layer, wherein said fifth copper layer has a thickness between 5 and 30 micrometers, wherein said third metal interconnect is connected to said a fourth metal interconnect of said first interconnection scheme.

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41. (Previously presented) The chip package of claim 21, further comprising a second semiconductor chip over said first interconnection scheme and connected to said first interconnection scheme through a second metal bump, wherein said second semiconductor chip has a height is between a backside surface of said second semiconductor chip and a top surface of said second polymer layer is smaller than a thickness of said first metal bump.

42. (Previously presented) The chip package of claim 21, further comprising a second semiconductor chip under said first semiconductor chip, wherein said first semiconductor chip comprise a second metal pad connected to a third metal pad of said second semiconductor chip through a solder layer, wherein said solder layer between said first and second semiconductor chips.

43. (Previously presented) The chip package of claim 21, further comprising a second semiconductor chip under said first semiconductor chip, wherein said first semiconductor chip comprises a second metal pad on a top surface of said first semiconductor chip, a third metal pad on a bottom surface of said first semiconductor chip and a through-silicon-via metal layer connects to said second metal pad, wherein said third metal pad is connected to a fourth metal pad of said second semiconductor chip.

44. (Previously presented) The chip package of claim 21, further comprising a third metal plug vertically in a third through via in said first polymer layer, wherein a pitch between said first and third metal plugs is between 200 and 1000 micrometers.

45. (Previously presented) The chip package of claim 31, wherein a height is between a backside surface of said first semiconductor chip and a top surface of said second polymer layer is smaller than a thickness of said first metal bump.

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46. (Previously presented) The chip package of claim 31, wherein said second semiconductor chip is coupled to said first semiconductor chip through said first interconnection scheme.

47. (Previously presented) The chip package of claim 21, wherein said first metal plug has a thickness between 100 and 300 micrometers.

48. (Previously presented) The chip package of claim 31, wherein said first metal plug has a thickness between 100 and 300 micrometers.

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REMARKS/ARGUMENTS

REMARKS

The Examiner is thanked for the thorough examination of the present application and Notice of Allowance issued on July. 9, 2021. Upon entry of this amendment, no claim has been canceled, no new claim has been added, and claim 1 has been amended under 37 CFR §1.312, complying with the provisions of 37 CFR §1.121, embodying merely the correction of formal matters in the claims without changing the scope thereof. Claims 1-20 are now allowed in the present application. Applicants respectfully request entrance of the amendments under 37 CFR §1.312 for at least the following reasons. No new matter has been introduced into the disclosure by the amendments.

Amendments to the Claims

In this paper, claim 31 has been amended to correct informalities and for disclosure consistency, complying with the provisions of 37 CFR §1.121(e), to correct inaccuracies of description and definition, and to secure substantial correspondence between the claims, the remainder of the specification, and the drawings.

In claim 31, "," was deleted and replaced with " and ". A) The amendment is needed to correct informalities in grammar. As the amendment corrects informalities, B) the amended claims require no additional search or examination and C) the amendment does not change the patentability of claim 31. D) The amendment was not presented earlier as it was only found following review after receiving the Notice of Allowance.

In light of the above, Applicants respectfully request entrance of the amendments under 37 CFR §1.312 to claim 31.

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In this paper, claim 31 is amended to correct informalities and for disclosure consistency, complying with the provisions of 37 CFR §1.121(e), to correct inaccuracies of description and definition, and to secure substantial correspondence between the claims, the remainder of the specification, and the drawings.

Thus, upon entry of these amendments, no claim has been canceled, no new claim has been added, and claim 31 has been amended under 37 CFR §1.312, complying with the provisions of 37 CFR §1.121, embodying merely the correction of formal matters in the claims without changing the scope thereof.

With respect to the claim amendments, Applicants would like to note that they have not dedicated to the public or abandoned any unclaimed subject matter and have not acquiesced to any rejections or objections by the Patent office. Applicants also expressly reserve the right to pursue prosecution on any presently excluded subject matter in one or more future continuation and/or divisional application(s).

Internet Communications

Pursuant to MPEP 502.03: "Recognizing that Internet communications are not secure, I hereby authorize the USPTO to communicate with me concerning any subject matter of this application by electronic mail. I understand that a copy of these communications will be made of record in the application file."

CONCLUSION

In view of the amendments herein, Applicants submit that the claims remain in condition for allowance and respectfully request amendment of the application in the manner identified above.

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Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact the undersigned by phone (886-913-635-863) or email (semars3898@gmail.com).

Respectfully submitted,



Date: __2021-07-11_____ Ping-Jung Yang
Email: semars3898@gmail.com

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TSMC EX1032 Page 645

Electronic Acknowledgement Receipt	
EFS ID:	43216834
Application Number:	16752650
International Application Number:	
Confirmation Number:	4809
Title of Invention:	CHIP PACKAGE
First Named Inventor/Applicant Name:	Ping-Jung Yang
Customer Number:	102851
Filer:	Ping-Jung. Yang
Filer Authorized By:	
Attorney Docket Number:	Mars16-001-US-C01
Receipt Date:	11-JUL-2021
Filing Date:	26-JAN-2020
Time Stamp:	08:16:20
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		Mars16-001-US-C01-AANOA-07112021.pdf	123168 d0833f86193f163bb3e092f3d1c405cba1d4f6dd	yes	12

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Amendment after Notice of Allowance (Rule 312)	1	1
	Claims	2	9
	Applicant Arguments/Remarks Made in an Amendment	10	12
Warnings:			
Information:			
	Total Files Size (in bytes):	123168	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

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If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PART B - FEE(S) TRANSMITTAL

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P.O. Box 1450
Alexandria, Virginia 22313-1450

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Ping-Jung Yang	(Typed or printed name)
Ping-Jung Yang	(Signature)
2021-07-11	(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/752,650	01/26/2020	Ping-Jung Yang	Mars16-001-US-C01	4809

TITLE OF INVENTION: CHIP PACKAGE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	$600	$0.00	$0.00	$600	10/12/2021

EXAMINER	ART UNIT	CLASS-SUBCLASS
LIU, XIAOMING	2812	257-091000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-09 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: Ping-Jung Yang

(B) RESIDENCE: (CITY and STATE OR COUNTRY): HsinChu City, Taiwan

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☒ Individual ☐ Corporation or other private group entity ☐ Government

4a. Fees submitted: ☒ Issue Fee ☐ Publication Fee (if required) ☐ Advance Order - # of Copies _____

4b. Method of Payment: *(Please first reapply any previously paid fee shown above)*

☐ Electronic Payment via EFS-Web ☐ Enclosed check ☐ Non-electronic payment by credit card (Attach form PTO-2038)

☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. _____

5. **Change in Entity Status** (from status indicated above)

☐ Applicant certifying micro entity status. See 37 CFR 1.29

☐ Applicant asserting small entity status. See 37 CFR 1.27

☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature Ping-Jung Yang Date 2021-07-11

Typed or printed name Ping-Jung Yang Registration No. _____

PTOL-85 Part B (08-18) Approved for use through 01/31/2020 OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

IPR2026-00067
TSMC EX1032 Page 648

Electronic Patent Application Fee Transmittal

Application Number:	16752650
Filing Date:	26-Jan-2020
Title of Invention:	CHIP PACKAGE
First Named Inventor/Applicant Name:	Ping-Jung Yang
Filer:	Ping-Jung. Yang
Attorney Docket Number:	Mars16-001-US-C01

Filed as Small Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
UTILITY APPL ISSUE FEE	2501	1	600	600

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**600**

Electronic Acknowledgement Receipt	
EFS ID:	43216837
Application Number:	16752650
International Application Number:	
Confirmation Number:	4809
Title of Invention:	CHIP PACKAGE
First Named Inventor/Applicant Name:	Ping-Jung Yang
Customer Number:	102851
Filer:	Ping-Jung. Yang
Filer Authorized By:	
Attorney Docket Number:	Mars16-001-US-C01
Receipt Date:	11-JUL-2021
Filing Date:	26-JAN-2020
Time Stamp:	08:25:55
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$600
RAM confirmation Number	E20217A927344608
Deposit Account	
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	16752650-issuefee.pdf	107778 a3a42eba26887c5fb0c1e89f7181205073af7952	no	1
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	29449 889fa00b94560ea5de81b01e18257836fe2a0ebc	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	137227		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/752,650	01/26/2020	Ping-Jung Yang	Mars16-001-US-C01	4809

102851 7590 07/15/2021

PING-JUNG YANG
NO 2, NIOUPU SOUTH RD., SIANGSHAN DISTRICT
HSINCHU CITY, 30091
TAIWAN

EXAMINER	
LIU, XIAOMING	

ART UNIT	PAPER NUMBER
2812	

MAIL DATE	DELIVERY MODE
07/15/2021	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Response to Rule 312 Communication	Application No.	Applicant(s)	
	16/752,650	Yang, Ping-Jung	
	Examiner	Art Unit	AIA (FITF) Status
	XIAOMING LIU	2812	No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

1. ☑ The amendment filed on 11 July 2021 under 37 CFR 1.312 has been considered, and has been:
   a) ☑ entered.
   b) ☐ entered as directed to matters of form not affecting the scope of the invention.
   c) ☐ disapproved because the amendment was filed after the payment of the issue fee.
      Any amendment filed after the date the issue fee is paid must be accompanied by a petition under 37 CFR 1.313(c)(1) and the required fee to withdraw the application from issue.
   d) ☐ disapproved. See explanation below.
   e) ☐ entered in part. See explanation below.

/XIAOMING LIU/
Examiner, Art Unit 2812

OK TO ENTER: /X.L/

Docket No.: Mars-16-001-US-C01 **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	Customer Number: 102851
Ping-Jung Yang	:	Confirmation Number: 4809
Application No.: 16752650	:	Group Art Unit: 2812
Filed: Jan. 26, 2020	:	Examiner: LIU, XIAOMING

For: CHIP PACKAGE

AMENDMENT AFTER ALLOWANCE UNDER 37 CFR §1.312

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Commissioner:

Pursuant to amendments after allowance under 37 CFR §1.312, Applicants hereby respectfully submit this paper and request to amend claim 1 of the above-identified application in the manner presented hereafter. The amendments embody merely the correction of formal matters in the claims without changing the scopes thereof.

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks/Arguments are beginning on page 10 of this paper.

IPR2026-00067
TSMC EX1032 Page 655

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	
	Filing Date	
	First Named Inventor	Ping-Jung Yang
	Art Unit	
	Examiner Name	
	Attorney Docket Number	Mars16-001-US-C01

	17	20110026232		2011-02-03	Lin et al.	
	18	20110089574		2011-04-21	Kazuo ITOH	
	19	20080129439		2008-06-05	Tomonaga Nishikawa	
	20	20080113505		2008-05-15	Terry G. Sparks	
	21	20060020371		2006-01-26	Donhee Ham	
	22	20060006539		2006-01-12	Satoshi Matsui, et al.	
	23	20110147055		2011-06-23	Qing Ma et al.	
	24	20080318361		2008-12-25	Kwon Whan HAN	
Change(s) applied to document, /C.S./ 6/3/2021	25	20070045841		2007-03-01	Cho; Won Gu ; et al.	
	26	20110065250		2011-03-17	~~Semiconductor Energy Laboratory Co., Ltd.~~ Tokunaga	
	27	20130292846		2013-11-07	Lee; Seok-hyun et al.	

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /X.L/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	
	Filing Date	
	First Named Inventor	Ping-Jung Yang
	Art Unit	
	Examiner Name	
	Attorney Docket Number	Mars16-001-US-C01

	42	9147638		2015-09-29	Liu; Yueli et al.	
	43	9385105		2016-07-05	Meyer; Thorsten et al.	
	44	9627365		2017-04-18	Yu; Chen-Hua et al.	
Change(s) applied to document, /C.S./ 6/3/2020	45	8338238		12/2012 ~~11212-12-26~~	Hajime TOKUNAGA , Atsugi et al.	

If you wish to add additional U.S. Patent citation information please click the Add button. Add

U.S.PATENT APPLICATION PUBLICATIONS Remove

Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20020038725		2002-04-04	Suzuki et al.	
	2	20020145197		2002-10-10	Ohta et al.	
	3	20020159243		2002-10-31	Ogawa et al.	
	4	20050012217		2005-01-20	Mori et al.	
	5	20080149384		2008-06-26	Kawabe	

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /X.L/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	
	Filing Date	
	First Named Inventor	Ping-Jung Yang
	Art Unit	
	Examiner Name	
	Attorney Docket Number	Mars16-001-US-C01

	31	8207453		2012-06-26	Ma; Qing et al.	
Change(s) applied to document, /C.S./ 6/3/2021	32	7808799		10/2010 ~~2007-11-15~~	Tadahiko Kawabe	
	33	6265771		2001-07-24	Ference; Thomas G. et al.	
	34	6434016		2002-08-13	Zeng; Ming et al.	
	35	7151009		2006-12-19	Kim; Soon-Bum et al.	
	36	7557440		2009-07-07	Yamamoto; Hiroshi et al.	
	37	8354297		2013-01-15	Pagaila; Reza A. et al.	
	38	8822281		2014-09-02	Pagaila; Reza A. et al.	
	39	8878360		2014-11-04	Meyer; Thorsten et al.	
	40	8987918		2015-03-24	Razdan; Sandeep et al.	
	41	9048233		2015-06-02	Wu; Wei-Cheng et al.	

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /X.L/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	16752650
	Filing Date	2020-01-26
	First Named Inventor	Ping-Jung Yang
	Art Unit	1782
	Examiner Name	LIU, XIAOMING
	Attorney Docket Number	Mars16-001-US-C01

Change(s) applied to document, /T.W./ 7/28/2021

	9	8456856		~~2013-06-11~~ 06/2013	Lin et al.	
	10	8837872		2014-09-16	Yang et al.	

If you wish to add additional U.S. Patent citation information please click the Add button. Add

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Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20050098891		2005-05-12	Wakabayashi, Takeshi, et al.	
	2	20040238945		2004-12-02	Huang, Chien-Ping et al.	
	3	20060292851		2006-12-28	Lin; Mou-Shiung et al.	
	4	20110278736		2011-11-17	Lin; Yaojian et al.	
	5	20110285005		2011-11-24	LIN; Yung-Chi et al.	
	6	20120193785		2012-08-02	Mou-Shiung Lin et al.	

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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/752,650	08/31/2021	11107768	Mars16-001-US-C01	4809

102851 7590 08/11/2021

PING-JUNG YANG
NO 2, NIOUPU SOUTH RD., SIANGSHAN DISTRICT
HSINCHU CITY, 30091
TAIWAN

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 15 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Ping-Jung Yang, Hsinchu City, TAIWAN;
Ping-Jung Yang, Hsin-Chu City, TAIWAN

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508940057 12/27/2024

PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1
Stylesheet Version v1.2

Assignment ID: PATI718284

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT
SEQUENCE:	1

CONVEYING PARTY DATA

Name	Execution Date
Mr. Ping-Jung Yang	12/26/2024

RECEIVING PARTY DATA

Company Name:	MYW SEMITECH, LLC
Street Address:	8 The Green, #21147
City:	Dover
State/Country:	DELAWARE
Postal Code:	19901

PROPERTY NUMBERS Total: 12

Property Type	Number
Application Number:	61705649
Application Number:	62219249
Application Number:	14036256
Application Number:	15261956
Application Number:	15476999
Application Number:	16139040
Application Number:	16752650
Application Number:	17372459
Application Number:	17985827
Application Number:	18524118
Application Number:	18778983
Application Number:	19001689

CORRESPONDENCE DATA

Fax Number:

Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.

Phone: 0913635863
Email: semars3898@gmail.com
Correspondent Name: Mr. Ping-Jung Yang
Address Line 1: No.52, Ln. 97, Shengjun Rd.

Address Line 4:	Hsinchu City, TAIWAN 300
ATTORNEY DOCKET NUMBER:	Mars Patents assignment
NAME OF SUBMITTER:	Ping-Jung Yang
SIGNATURE:	Ping-Jung Yang
DATE SIGNED:	12/27/2024
	This document serves as an Oath/Declaration (37 CFR 1.63).

Total Attachments: 4
source=Assignment-MYW SEMITECH LLC-signed-12262024#page1.tiff
source=Assignment-MYW SEMITECH LLC-signed-12262024#page2.tiff
source=Assignment-MYW SEMITECH LLC-signed-12262024#page3.tiff
source=Assignment-MYW SEMITECH LLC-signed-12262024#page4.tiff

ASSIGNMENT OF PATENT RIGHTS

For good and valuable consideration, the receipt of which is hereby acknowledged, **PING-JUNG YANG**, a citizen of Taiwan, residing in No. 52, Ln. 97, Shengjun Rd., North Dist., Hsinchu City, Taiwan (***"Assignor"***), does hereby assign, transfer, and convey unto **MYW SEMITECH, LLC.**, a Delaware corporation with an address at 8 The Green, #21147, Dover, DE 19901 USA (***"Assignee"***), or its designees all right, title, and interest that exist today and may exist in the future in and to all of the following (collectively, the ***"Patent Rights"***):

(a) the provisional patent applications, patent applications and patents listed in the table below (the "***Patents***");

(b) all patents and patent applications (i) to which any of the Patents directly or indirectly claims priority, (ii) for which any of the Patents directly or indirectly forms a basis for priority, and/or (iii) that were co-owned applications that directly or indirectly incorporate by reference the Patents;

(c) all reissues, reexaminations, extensions, continuations, continuations in part, continuing prosecution applications, requests for continuing examinations, divisions, registrations of any item in any of the foregoing categories (a) and (b);

(d) all foreign patents, patent applications, and counterparts relating to any item in any of the foregoing categories (a) through (c), including, without limitation, certificates of invention, utility models, industrial design protection, design patent protection, and other governmental grants or issuances;

(e) all items in any of the foregoing in categories (b) through (d), whether or not expressly listed as Patents below and whether or not claims in any of the foregoing have been rejected, withdrawn, cancelled, or the like;

(f) all inventions, invention disclosures, and discoveries described in any item in any of the foregoing categories (a) through (e) that (i) are included in any claim in the Patents and/or any item in the foregoing categories (b) through (e), (ii) are subject matter capable of being reduced to a patent claim in a reissue or reexamination proceedings brought on any of the Patents and/or any item in the foregoing categories (b) through (e), and/or (iii) could have been included as a claim in any of the Patents and/or any item in the foregoing categories (b) through (e);

(g) all rights to apply in any or all countries of the world for patents, certificates of invention, utility models, industrial design protections, design patent protections, or other governmental grants or issuances of any type related to any item in any of the foregoing categories (a) through (f), including, without limitation, under the Paris Convention for the

Protection of Industrial Property, the International Patent Cooperation Treaty, or any other convention, treaty, agreement, or understanding;

(h) all causes of action (whether known or unknown or whether currently pending, filed, or otherwise) and other enforcement rights under, or on account of, any of the Patents and/or any item in any of the foregoing categories (b) through (g), including, without limitation, all causes of action and other enforcement rights for

(i) damages,
(ii) injunctive relief, and
(iii) any other remedies of any kind

for past, current, and future infringement; and

(i) all rights to collect royalties and other payments under or on account of any of the Patents and/or any item in any of the foregoing categories (b) through (h).

No.	Appl. No.	Filing Date	No.	Appl. No.	Filing Date
1	61/705649	09-26-2012	7	16/752650	01-26-2020
2	62/219249	09-16-2015	8	17/372459	07-11-2021
3	14/036256	09-25-2013	9	17/985827	11-12-2022
4	15/261956	09-11-2016	10	18/524118	11-30-2023
5	15/476999	04-01-2017	11	18/778983	07-21-2024
6	16/139040	09-23-2018	12	19/001689	12-26-2024

Assignor represents, warrants and covenants that:

(1) Assignor has the full power and authority, and has obtained all third party consents, approvals and/or other authorizations required to enter into this Agreement and to carry out its obligations hereunder, including the assignment of the Patent Rights to Assignee; and

(2) Assignor owns, and by this document assigns to Assignee, all right, title, and interest to the Patent Rights, including, without limitation, all right, title, and interest to sue for infringement of the Patent Rights. Assignor has obtained and properly recorded previously executed assignments for the Patent Rights as necessary to fully perfect its rights and title

therein in accordance with governing law and regulations in each respective jurisdiction. The Patent Rights are free and clear of all liens, claims, mortgages, security interests or other encumbrances, and restrictions. There are no actions, suits, investigations, claims or proceedings threatened, pending or in progress relating in any way to the Patent Rights. There are no existing contracts, agreements, options, commitments, proposals, bids, offers, or rights with, to, or in any person to acquire any of the Patent Rights.

Assignor hereby authorizes the respective patent office or governmental agency in each jurisdiction to issue any and all patents, certificates of invention, utility models or other governmental grants or issuances that may be granted upon any of the Patent Rights in the name of Assignee, as the assignee to the entire interest therein.

Assignor will do all things necessary, proper, or advisable, including without limitation, the execution, acknowledgment, and recordation of specific assignments, oaths, declarations, and other documents on a country-by-country basis, to assist Assignee in obtaining, perfecting, sustaining, and/or enforcing the Patent Rights. Such assistance will include providing, and obtaining from the respective inventors, prompt production of pertinent facts and documents, giving of testimony, execution of petitions, oaths, powers of attorney, specifications, declarations or other papers, and other assistance reasonably necessary for filing patent applications, complying with any duty of disclosure, and conducting prosecution, reexamination, reissue, interference or other priority proceedings, opposition proceedings, cancellation proceedings, public use proceedings, infringement or other court actions and the like with respect to the Patent Rights.

The terms and conditions of this Assignment of Patent Rights will inure to the benefit of Assignee, its successors, assigns, and other legal representatives and will be binding upon Assignor, its successors, assigns, and other legal representatives.

[REMAINDER OF THIS PAGE INTENTIONALLY LEFT BLANK]

IN WITNESS WHEREOF this Assignment of Patent Rights is executed at _____ on _____.

ASSIGNOR

By: Ping-Jung Yang Dec. 26. 2024

Name: PING-JUNG YANG

Title: Inventor