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(54) TESTING OF SEMICONDUCTOR CHIPS WITH MICROBUMPS

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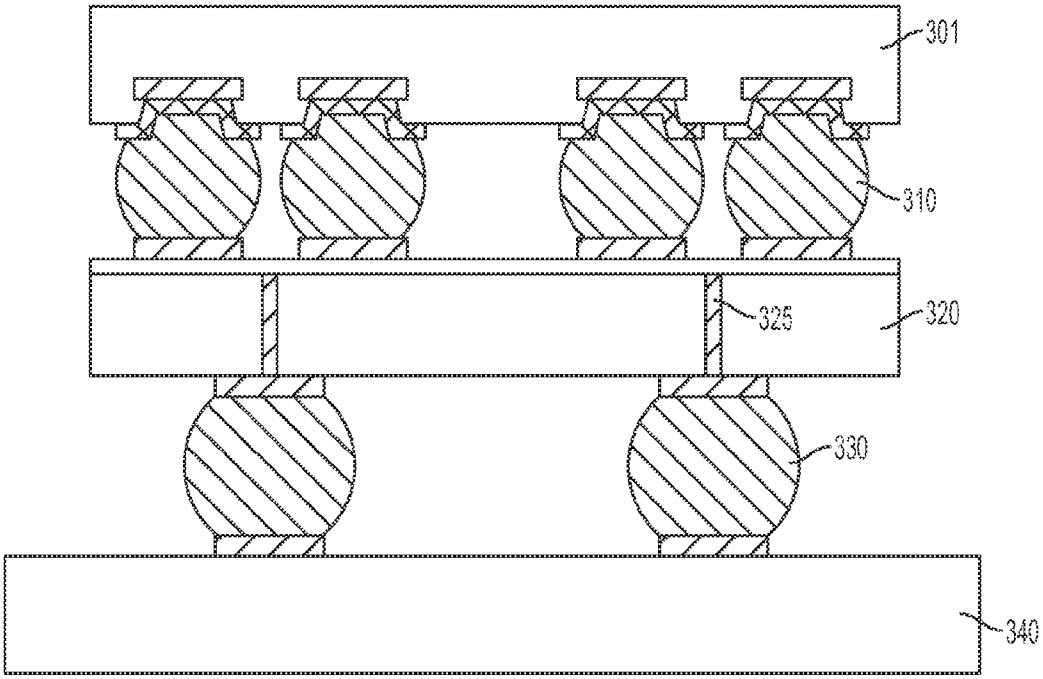
(57) **ABSTRACT**

Test structures for performing electrical tests of devices under one or more microbumps are provided. Each test structure includes at least one microbump pad and a test pad. The microbump pad is a part of a metal pad connected to an interconnect for a device. A width of the microbump pad is equal to or less than about 50 μm. The test pad is connected to the at least one microbump pad. The test pad has a size large enough to allow circuit probing of the device. The test pad is another part of the metal pad. A width of the test pad is greater than the at least one microbump pad.



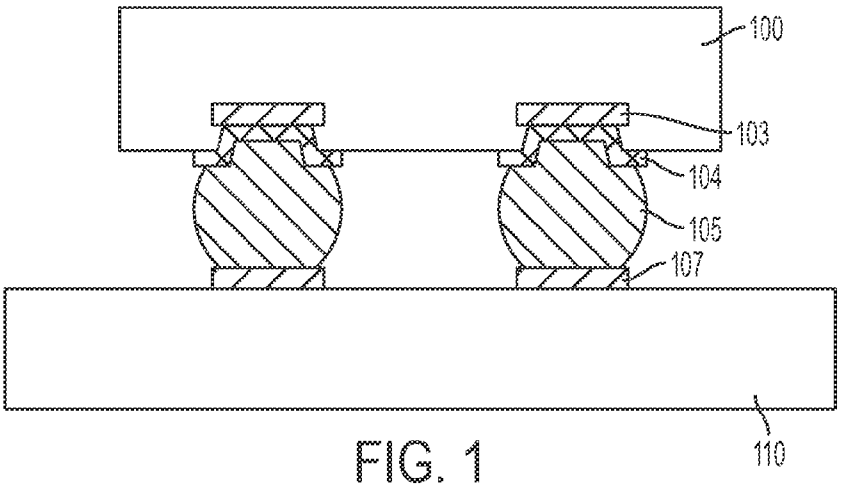


FIG. 1

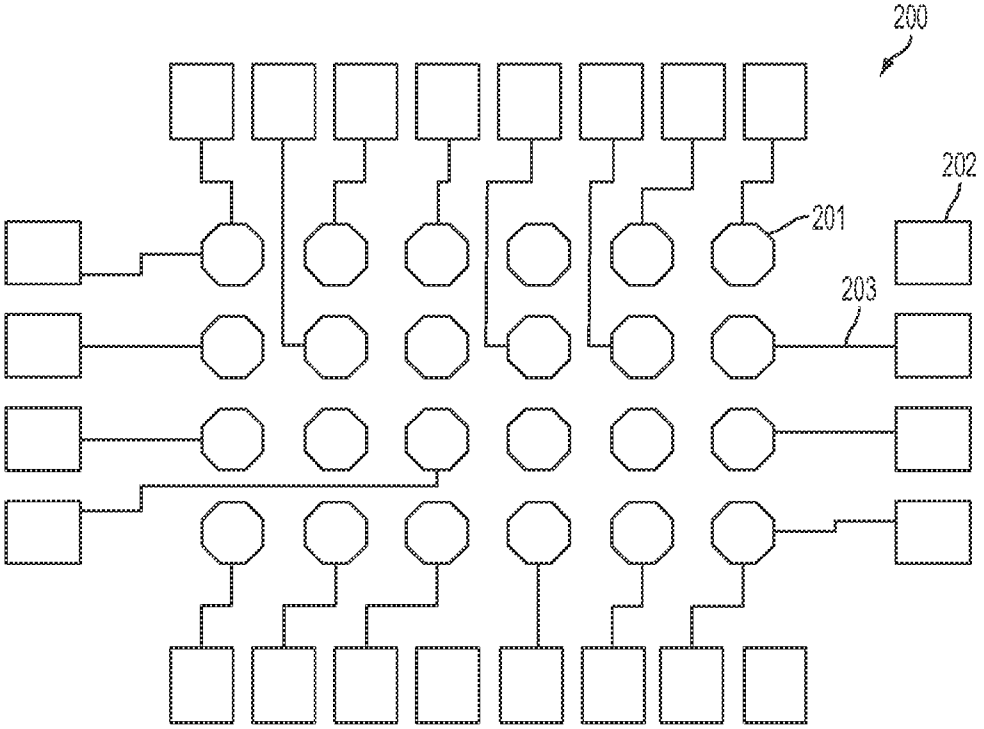


FIG. 2

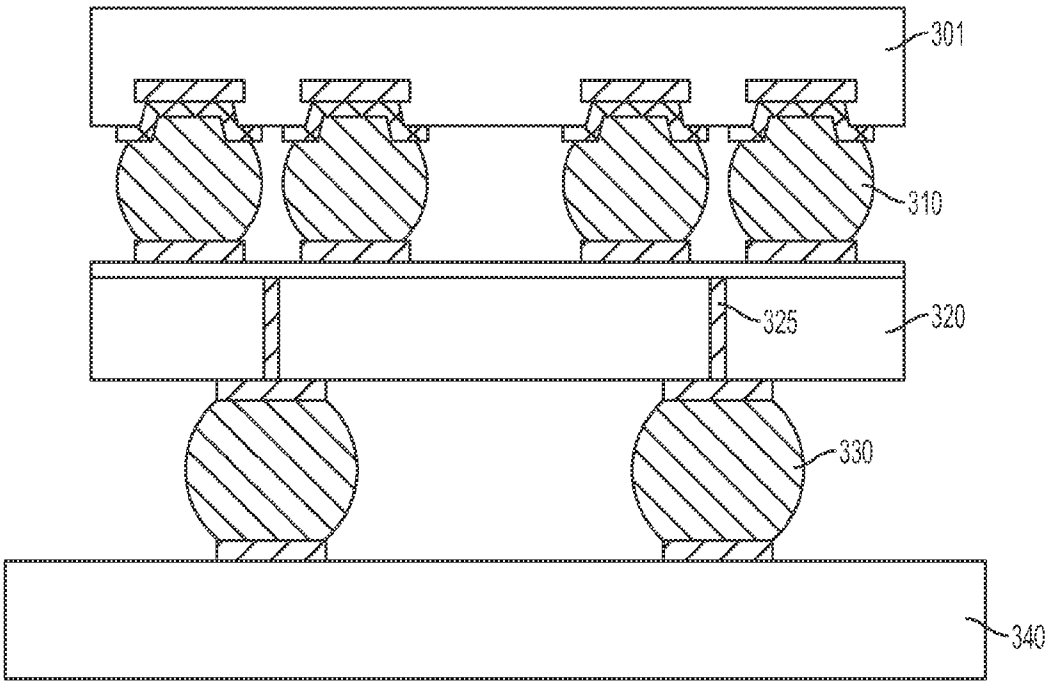


FIG. 3

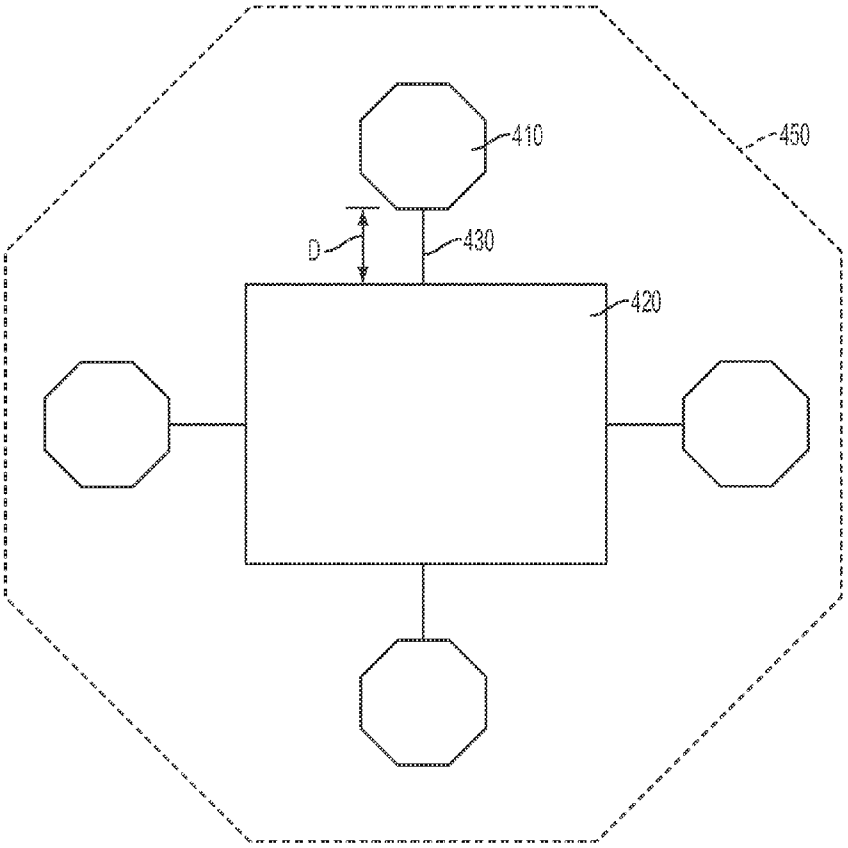


FIG. 4A

FIG. 4B

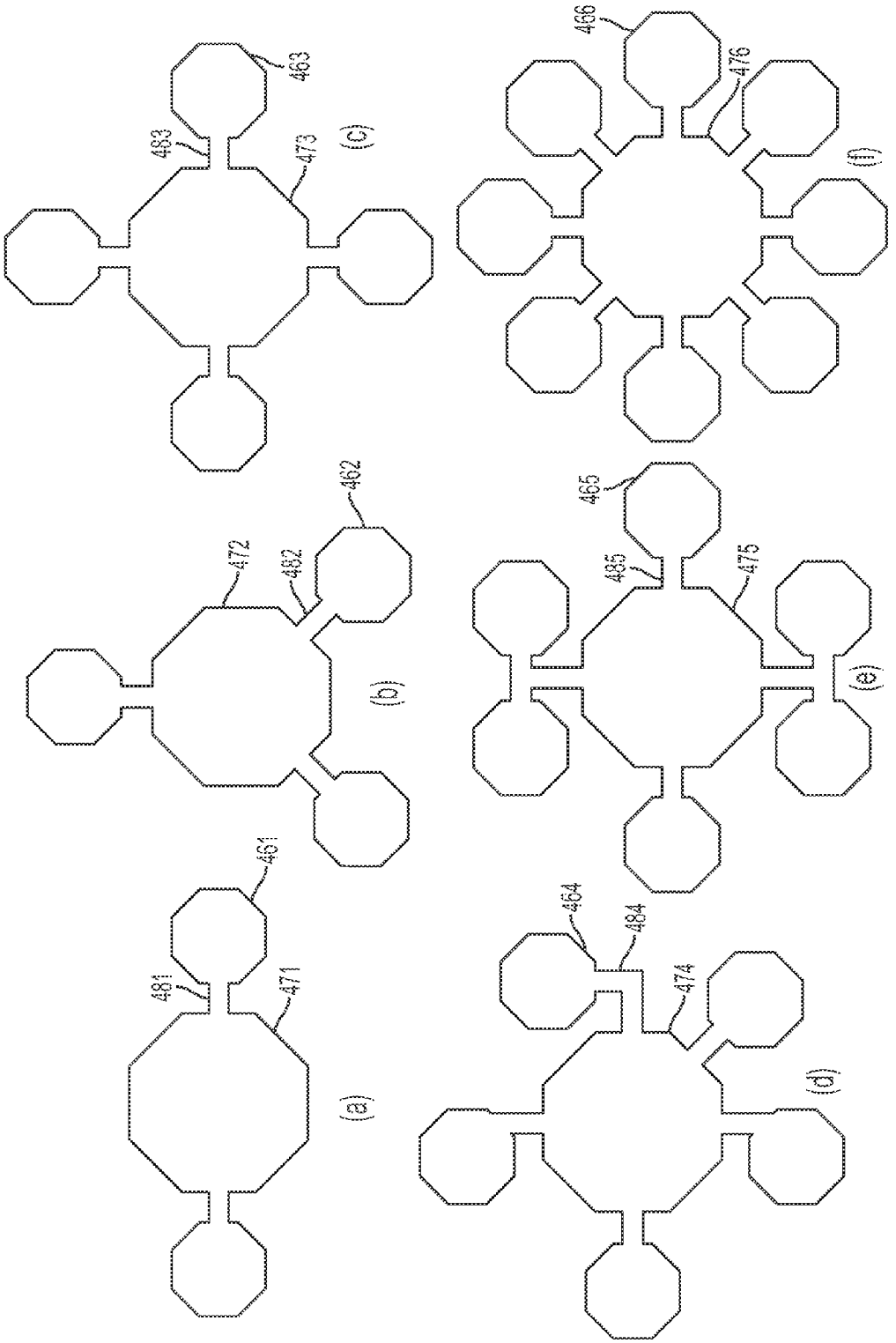

(a)
481
471
461
(b)
472
482
462
(c)
483
473
463
(d)
484
474
464
(e)
485
475
465
(f)
476
466

FIG. 4C

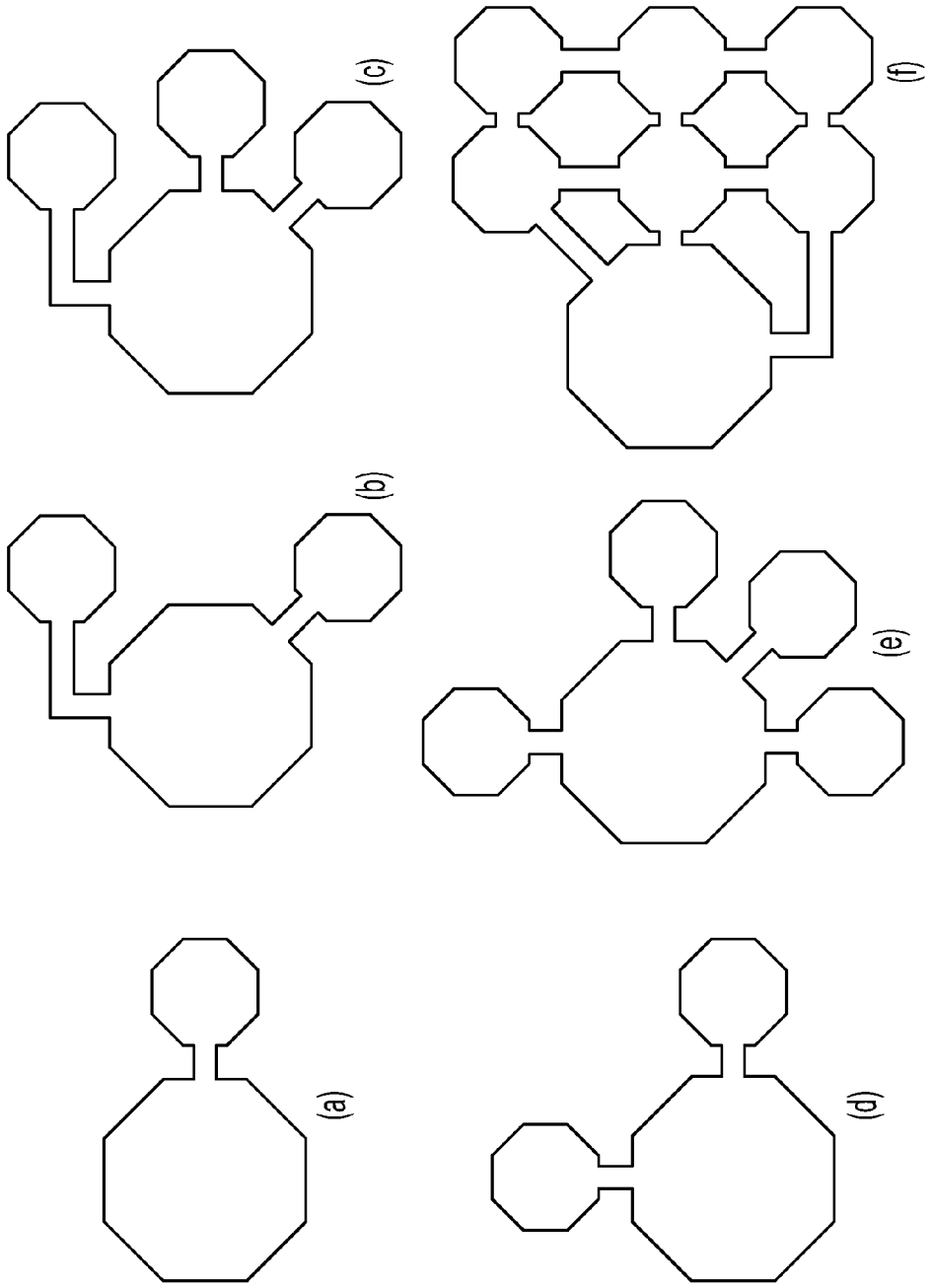


FIG. 4D

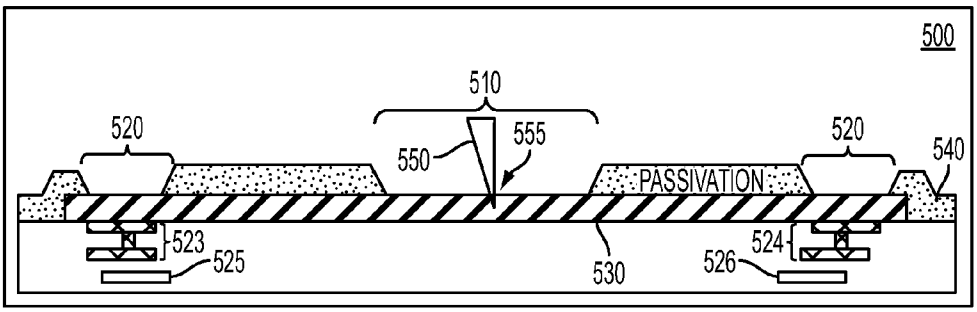


FIG. 5A

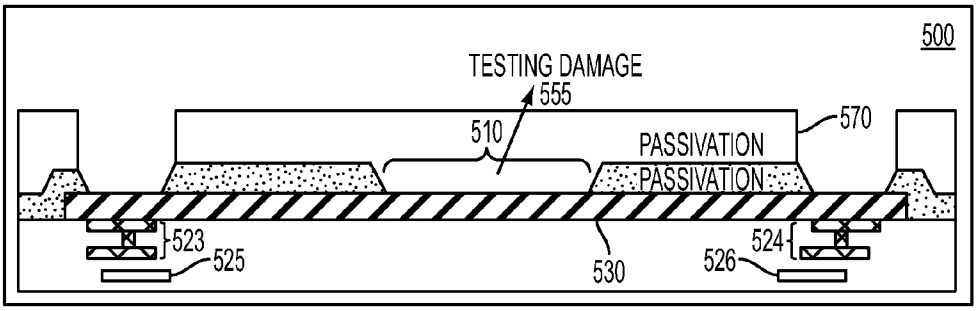


FIG. 5B

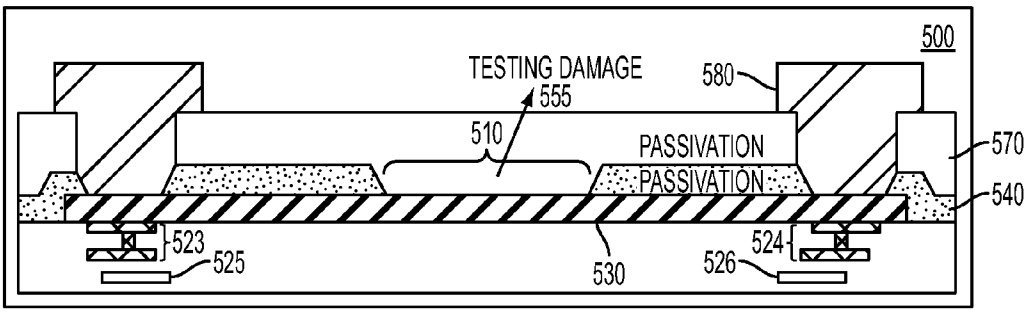


FIG. 5C

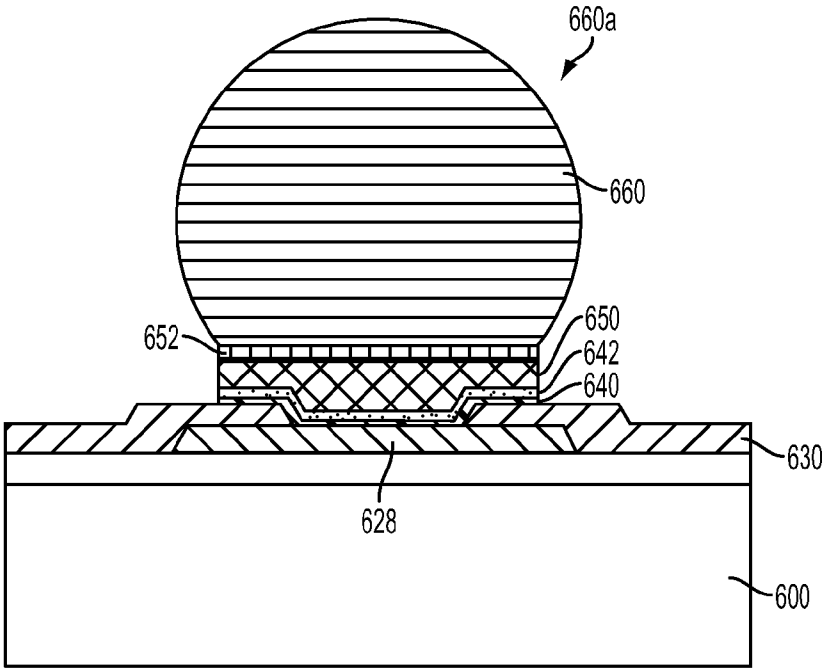

660a
660
650
652
642
640
630
628
600

FIG. 6A

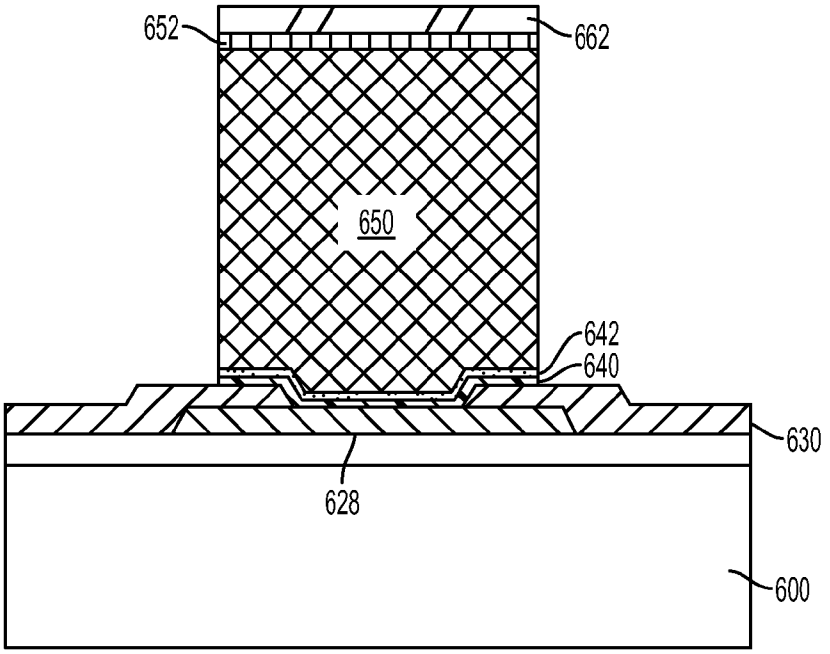

652
662
650
642
640
630
628
600

FIG. 6B

TESTING OF SEMICONDUCTOR CHIPS WITH MICROBUMPS

FIELD

[0001] This disclosure relates generally to integrated circuits, and more particularly to testing of semiconductor chips with microbumps.

BACKGROUND

[0002] Integrated circuits have experienced continuous rapid growth due to constant improvements in the integration density of various electronic components (i.e., transistors, diodes, resistors, capacitors, etc.). For the most part, this improvement in integration density has come from repeated reductions in minimum feature size, allowing more components to be integrated into a given chip area.

[0003] The volume occupied by the integrated components is near the surface of the semiconductor wafer. Although dramatic improvements in lithography have resulted in considerable improvements in two-dimensional (2D) integrated circuit formation, there are physical limitations to the density that can be achieved in two dimensions. One of these limitations is the minimum size needed to make these components. Further, when more devices are put into one chip, more complex designs are required. An additional limitation comes from the significant gains in the number and length of interconnections between devices as the number of devices increases. When the number and length of interconnections increase, both circuit resistive-capacitive (RC) delay and power consumption increase.

[0004] Three-dimensional integrated circuits (3DIC) were thus formed to address issues raised by increase in circuit densities. The dies are stacked, with wire-bonding, flip-chip bonding, and/or through-silicon vias (TSV) being used to stack the dies together and to connect the dies to package substrates. Circuit probe (CP) testing of advanced semiconductor chips and 3DIC with high device density becomes challenging.

BRIEF DESCRIPTION OF THE DRAWINGS

[0005] The present disclosure will be readily understood by the following detailed description in conjunction with the accompanying drawings, and like reference numerals designate like structural elements.

[0006] FIG. **1** shows a schematic diagram of an integrated circuit (IC) chip on a package substrate, in accordance with some embodiments.

[0007] FIG. **2** shows a top schematic view of a portion of a semiconductor chip with bumps, in accordance with some embodiments.

[0008] FIG. **3** shows a schematic diagram of a packaged semiconductor chip involving microbumps, in accordance with some embodiments.

[0009] FIG. **4**A shows a top view of a number of microbumps surrounding a test pad, in accordance with some embodiments.

[0010] FIG. **4**B shows examples of shapes of the testing pads described above, in accordance with some embodiments.

[0011] FIGS. **4**C(a)-(f) show a top view of a number of configurations of microbumps with test pads, in accordance with some embodiments.

[0012] FIGS. **4**D(a)-((f) show a top view of a number of configurations of microbumps with test pads, in accordance with some other embodiments.

[0013] FIGS. **5**A-**5**C are cross-sectional views of a region of a testing pad in a process of probing and formation of microbumps, in accordance with some embodiments.

[0014] FIG. **6**A shows a bump structure on a substrate, in accordance with some embodiments.

[0015] FIG. **6**B shows a copper post on a substrate, in accordance with some embodiments.

DETAILED DESCRIPTION

[0016] It is to be understood that the following disclosure provides many different embodiments, or examples, for implementing different features. Specific examples of components and arrangements are described below to simplify the present disclosure. These are, of course, merely examples and are not intended to be limiting. In addition, the present disclosure may repeat reference numerals and/or letters in the various examples. This repetition is for the purpose of simplicity and clarity and does not in itself dictate a relationship between the various embodiments and/or configurations discussed.

[0017] Modern integrated circuits are made of millions of active devices, such as transistors and capacitors. These devices are initially isolated from each other, but are later interconnected together to form functional circuits. Typical interconnect structures include lateral interconnections, such as metal lines (wirings), and vertical interconnections, such as vias and contacts. Interconnections are increasingly determining the limits of performance and the density of modern integrated circuits. On top of the interconnect structures, bond pads are formed and exposed on the surface of the respective chip. Electrical connections are made through these bond pads to connect the chip to a package substrate or another die. Bond pads can be used for wire bonding or flip-chip bonding. Flip-chip packaging utilizes bumps to establish electrical contact between a chip's I/O pads and the substrate or lead frame of the package.

[0018] FIG. **1** shows a schematic diagram of an integrated circuit (IC) chip **100** on a package substrate **110**, in accordance with some embodiments. IC chip **100** is packaged with flip-chip packaging by forming bumps **105** on the front-side of the IC chip **100**. Bumps **105** electrically and possibly physically contact the I/O pads (metal pads) **103** of the IC chip **100**. In some embodiments, there is an under bump metallurgy (UBM) layer **104** between the bumps **105** and the metal pads **103**. The IC chip **100** with the bumps **105** is flipped over to be placed on a package substrate **110**. The surface of substrate **110** may have metal pads **107** to receive bumps **105**. In some embodiments, the space between and around the IC chip **100**, the bumps **105** and the substrate **100** could be filled with an under-fill material (not shown). The embodiment shown in FIG. **1**A is merely an example. Other embodiments are also possible. IC chip **100** with bumps **105** could be applied on other types of substrates, such as an application board, and a substrate with embedded passive and/or active devices.

[0019] Conventionally, the sizes of the flip chip bumps are equal to or greater than about 75 μm. The sizes of the conventional flip chip bumps allow the semiconductor chips connected to the bumps to be electrically tested to determine whether the circuits under (or connected) to the bumps pass

functional tests. Sometimes such as tests may also called circuit probe (CP), or electronic die sort (EDS).

[0020] Conventional bumps, such as bumps **105**, can be probed for such tests. Alternatively, test pads can be added to allow functional tests. FIG. **2** shows a top schematic view of a portion **200** of a semiconductor chip with bumps, in accordance with some embodiments. The metal pads (or bump pads) **201** under bumps are represented by octagons in FIG. **2**. As shown in FIG. **1**, bumps (not shown) may be placed directly above these metal pads. There are a number of test pads **202** surrounding the metal pads **201** (and bumps above them). The test pads are connected to the metal pads via conductive lines **203**. The conductive lines may be redistribution lines (RDLs), which are formed above the metal pads under the bumps, metal lines, or post-passivation interconnects (PPI). The test pads **202** may be at the same or at different level as the conductive lines **203**. The test pads **202** are connected to different bumps **201** to perform functional tests. However, placing the test pads **202** around the bumps **201** takes away the real-estate on the surface of the semiconductor chip.

[0021] As feature size scales down, the number of transistors and interconnects on a chip has increased continuously. As a result, the number of chip to package input/output (I/O) interconnects have also increased significantly. With the increased chip to package I/O interconnects, the sizes of bumps could be reduced to equal to or less than about 50 μm. Such reduced-size bumps are called "microbumps."

[0022] FIG. **3** shows a schematic diagram of a packaged semiconductor chip involving microbumps, in accordance with some embodiments. A semiconductor chip **300** (a flipped chip) is disposed on a silicon substrate **320**, which has through silicon vias **325** for assisting heat dissipation. The silicon substrate **320** may or may not have active devices on the substrate. The semiconductor chip **300** is connected to silicon substrate **320** via microbumps **310**. The silicon substrate **320** is placed on another package substrate **340**, with bumps **330**, which are regular bumps and are larger than microbumps **310**.

[0023] After semiconductor chip **300** is prepared, and before it is placed on substrate **320**, it is desirable to perform electrical tests on chip **300** to determine if the circuits on chip **300** meet the specification of functional tests. If the test results show problems with chip **300**, chip **300** could be discarded and another good chip could be used instead. Such screening can prevent the entire package shown in FIG. **3** from being discarded and can increase package yield, which would result in cost-saving.

[0024] As mentioned above, conventional flip chip bumps, with sizes equal to or greater than about 75 μm, allow circuit probing (or electrical tests). However, the current circuit probes are too large for microbumps (or μbumps). For example, the sizes (or widths) of the tips of probes may be in a range from about 2.5 mil to about 5 mil, which are too large for microbumps. An alternative for testing semiconductor chips with microbumps would be to use test pads, such as those described in FIG. **2**. However, test pads occupy the precious real-estate on the surface of the semiconductor chip, as mentioned above.

[0025] As mentioned above, regular bumps are much larger than microbumps. For example, regular bumps have diameters in a range from about 75 μm to about 150 μm. In contrast, the diameters of microbumps are in a range from about 20 μm to about 50 μm, in accordance with some embodiments. As a result, extra space on the surface of semiconductor may become available due to the usage of microbumps.

[0026] FIG. **4**A shows a top view **400** of a number of bump pads **410** surrounding a test pad **420**, in accordance with some embodiments. FIG. **4**A shows **4** bump pads **410** surrounding the test pad **420**. The bump pads **410** are connected to test pad **420** via metal lines **430**. Due to the smaller size of the microbumps, the bump pads **410** are also smaller, with widths only slightly larger than the 20 μm to about 50 μm. The exemplary bump pads **410** are shown to be in octagonal shape in FIG. **4**A. Other shapes are also possible. The testing pad **420** is shown in FIG. **4**A to be a square. The test pad **420** may also be in other shapes, such as a circle, a hexagon, an octagon, a rectangle, or other polygons. FIG. **4**B shows examples of shapes of the testing pads **420** described above, in accordance with some embodiments. The smallest width of the test pads **420** is greater than about 60 which allows probing tests, in accordance with some embodiments. The distance D between the bump pads **410** and the test pad **420** is in a range from about 20 μm to about 80 μm.

[0027] Since the microbumps are smaller than regular bumps. The surface space saved from using microbumps, instead of using regular bumps, could be used for the testing pads. Using the surface saved by using microbumps for test pad(s) can minimize the impact of the test pads occupying the real-estate of the surface of a semiconductor chip. FIG. **4**A shows a pad area **450** for a regular bump, in accordance of some embodiments. The microbumps **410** and the testing pad **420** are within the pad area **450** of a regular bump. The microbumps **410** and the testing pad **420** could also occupy an area slightly larger than the pad area **450** of a regular bump. However, the usage of microbumps saves surface real-estate and can minimize the impact of having a test pad(s).

[0028] FIGS. **4**C(a)-(f) show a top view of a number of configurations of microbumps with test pads, in accordance with some embodiments. In FIGS. **4**C(a)-(f), the bump pads **461**, **462**, **463**, **464**, **465**, and **466** surround the test pads **471**, **472**, **473**, **474**, **475**, and **476** and are distributed symmetrically around the test pads. The probing areas are within the test pads due to coverage of edge areas by a passivation layer. Similarly, the microbumps are placed within the bump pads. The bump pads and testing pads are connected to one another via conductive lines **491**, **492**, **493**, **494**, **495**, and **496**, which are on the same level or different level of the metal pads, **461**-**466** and **471**-**476**. The testing pads are illustrated to be in octagonal shapes. However, they could be in other shapes, as described in FIG. **4**B. The bump pads under the microbumps are shown in octagonal shapes, which are also merely exemplary.

[0029] The number of bump pads (or microbumps) could be in a range from 2 to 8, in accordance with some embodiments. For smaller microbumps, the number of bumps can be even higher. Different numbers of microbumps could be connected to the test pads to allow performing functional tests of different devices connected to the same I/O connections and/or under the same input signals. For example, some functions of the semiconductor chip could involve applying or pulling signals (or current) from devices connected to a number of bumps. The different connections show in FIGS. **4**C(a)-(f) allow such testing. The symmetrical configuration of bump pads for microbumps could make stress distribution due to the formation of microbumps more even, which could reduce the chance of interface delamination for the microbumps.

[0030] Alternatively, the microbumps do not need to be distributed asymmetrically around the testing pads. FIGS. **4**D(a)-(f) show a top view of a number of configurations of microbumps with test pads, in accordance with some other embodiments. FIG. **4**D(a)-(f) show different numbers of microbumps are connected to the testing pads and are arranged asymmetrically.

[0031] In some embodiments, there are a number of test pads with microbumps in some of the arrangements described above on a semiconductor chip. Different combinations could be needed on different chips to complete functional testing of various devices on the chips. For example, different inputs/outputs (I/Os), such as I/Os for signals, power, and ground (or grounding), need different numbers of microbumps due to different current requirement and also the I_{max} (maximum current) limits of microbumps. Therefore, different combinations of numbers of microbumps are needed to allow testing.

[0032] Circuit probing can damage the metal pads, which leads to the copper seed layer coverage and poor bump plating (or formation). Poor bump formation could lead to particle and corrosion issues. However, if the testing pads are covered by a passivation layer after the testing is completed, the risks of such issues are completed resolved or greatly reduced.

[0033] FIGS. **5**A-**5**C are cross-sectional views of a region **500** of a testing pad in a process of probing and formation of microbumps, in accordance with some embodiments. FIG. **5**A shows that a test pad region **510** and two opening regions (or bump pads) **520** for forming microbumps. Under the two opening regions (or bump pads) **520** for forming microbumps, there are interconnects **523**, **524** connecting the to-be-formed microbumps with devices **525** and **526**. The interconnect **523**, **524** and devices **525**, **526** (on substrate **505**) shown in FIG. **5**A are merely exemplary. Other configurations and additional interconnects/devices could be involved. The test pad region **510** is formed on a metal pad **530**, which could be a top metal layer, a redistribution layer (RDL), or a post passivation interconnect (PPI) layer, in accordance with some embodiments. Regions **520** and test pad region **510** are electrically and physically connected. FIG. **5**A shows that the test pad region **510** and the regions **520** are defined by a first passivation layer **540** through lithographical patterning. The first passivation layer **540** is deposited over the metal pad **530**. The test pad region **510** is separated from the regions **520** so that the microbumps formed in regions **520** would be physically separated from the test pad **510**. The outline(s) of the conductive line(s) between test pad and microbump pad(s) are also defined by the first passivation layer, which is not shown in FIG. **5**A.

[0034] FIG. **5**A shows a probe **550** touching the test pad region **510**. The probing causes damage (see region **555**) on the surface of the test pad region **510**. The probing in test pad region **510** allowed electrical data related to devices connected to regions **520** to be tested. As mentioned above, the regions for forming microbumps that are connected to the test pad could be in a range from 1 to many. After the probing is completed, microbumps will be formed on regions **520**. In some other embodiments, an UBM layer (not shown) is formed after the probing is performed. The UBM layer is under the microbumps to provide a diffusion barrier and to enhance adhesion. In some embodiments, the UBM layer (not shown) is formed to cover the openings **520** before probing is performed. The structure of microbumps with details of the UBM layer will be described later. The formation of the UBM layer involves deposition, patterning and etching the UBM layer. After the UBM layer is formed, the substrate a second passivation layer **570** is deposited and patterned to expose regions **520**. The second passivation layer **570** may be made of an organic polymer, such as polyimide. In some embodiments, the second passivation layer **570** is made of a photosensitive polyimide. In some other embodiments, the second passivation layer **570** may be a dielectric material, which may be deposited by chemical vapor deposition or by spin-on. For example, the dielectric material may be SiO_2, SiN, or other suitable passivation material. The test pad region **520** is covered by the second passivation layer **570**; therefore, the issues such as particles and corrosion due to test pad damage are resolved. The damaged area is covered and protected. In some embodiments, the thickness of the second passivation layer **570** is in a range from about 1 μm to about 10 μm. In some other embodiments, the thickness of the second passivation layer **570** is in a range from about 2 μm to about 5 μm.

[0035] FIG. **5**C shows the microbumps **580** formed on the substrate of FIG. **5**B after the second passivation layer **570** is formed, in accordance with some embodiments. The microbumps **580** may be formed by plating, in accordance with some embodiments. Prior to plating the substrate, a photoresist, which could be wet or dry (not shown in FIG. **5**C), is patterned over the second passivation layer **570** to define of the microbumps **580** above regions **520**. The microbumps can be made of various materials, such as solder or copper. After the microbumps are deposited, substrate **505** may undergo a reflow process.

[0036] The structures of microbumps and the processes of forming the microbumps could be similar to regular bumps. FIGS. **6**A and **6**B show two exemplary structures of microbumps on substrates, in accordance with some embodiments. FIG. **6**A shows a bump structure on a substrate **600**, in accordance with some embodiments. Metal pad **628**, which is used as bump pad, is formed over one or more interconnect structures (not shown). Metal pad **628** may comprise aluminum, and hence may also be referred to as aluminum pad **628**, although it may also be formed of, or include, other materials, such as copper, silver, gold, nickel, tungsten, alloys thereof, and/or multi-layers thereof. In some embodiments, a passivation layer **630** is formed to cover edge portions of metal pad **628**. The passivation layer **630** may be formed of polyimide or other known dielectric materials. Additional pas sivation layers may be formed over the interconnect structures (not shown) and at the same level, or over, metal pad **628**.

[0037] An opening is formed in passivation layer **630**, with metal pad **628** exposed. A diffusion barrier layer **640** and a thin seed layer **642** are formed to cover the opening with the diffusion barrier layer **640** in contact with the metal pad **628**, in accordance with some embodiments. Diffusion barrier layer **640** may be a titanium layer, a titanium nitride layer, a tantalum layer, or a tantalum nitride layer. The materials of seed layer **642** may include copper or copper alloys, and hence is referred to as copper seed layer **642** hereinafter. However, other metals, such as silver, gold, aluminum, and combinations thereof, may also be included. In some embodiments, diffusion barrier layer **640** and copper seed layer **642** are formed using sputtering.

[0038] A copper layer **650** may be deposited or plated on the exposed surface of copper seed layer **642**, in accordance with some embodiments. A metal layer **652** may be optionally formed on the copper layer **650**. In some embodiments, metal layer **652** is a nickel-containing layer comprising, for example, a nickel layer or a nickel alloy layer by plating. A

solder layer **660** is formed on nickel layer **652**, for example, by plating. Solder layer **660** may be a lead-free pre-solder layer formed of, for example, SnAg, or a solder material, including alloys of tin, lead, silver, copper, nickel, bismuth, or combinations thereof. A solder reflowing process is performed to form solder bump **660**a, as shown in FIG. **6**A.

[0039] In alternative embodiments, as shown in FIG. **6**B, the thickness of copper layer **650** is increased so that copper layer **650** becomes a copper post (or pillar). In some embodiments, after the optional formation of metal layer **652** on copper post **650**, a solder layer **662**, which may be a thin solder layer, may be plated on metal layer **652**. The embodiments shown in FIGS. **6**A and **6**B are only two examples; other embodiments of bumps are also possible. Further details of bump formation process may be found in U.S. patent application Ser. No. 12/842,617, filed on Jul. 23, 2010 and entitled "Preventing UBM Oxidation in Bump Formation Processes," and U.S. patent spplication Ser. No. 12/846,353, filed on Jul. 29, 2010 and entitled "Mechanisms for Forming Copper Pillar Bumps," both of which are incorporated herein in their entireties.

[0040] The embodiments described above provide mechanisms for performing functional tests on devices connected to microbump pads under microbumps. Test pads that are larger than microbumps are formed to allow such testing. Due to the surface areas saved by using microbumps, the effect of test pads on surface real-estate of semiconductor chips could be reduced to minimum or none. The test pad can be connected to one or more microbump pads during testing. These one or more microbumps may be distributed symmetrically or asymmetrically around the test pads. The test pads could be damaged due to circuit probing and could be covered by a passivation layer after probing to protect the damaged surface.

[0041] In one embodiment, a test structure for performing electrical tests of devices under one or more microbumps is provided. The test structure includes at least one device, and a metal pad connected to an interconnect for the at least one device. The metal pad includes a first portion forming at least one microbump pad, and a width of the at least one microbump pad is equal to or less than about 50 μm. The metal pad also includes a second portion forming a test pad connected to the at least one microbump pad, and the test pad has a size large enough to allow circuit probing of the at least first device. A width of the test pad is greater than the at least one microbump pad.

[0042] In another embodiment, a test structure for performing electrical tests of devices under one or more microbumps is provided. The test structure includes at least one microbump pad, and the at least one microbump pad is a part of a metal pad connected to an interconnect for at least a first device. A width of the at least one microbump pad is equal to or less than about 50 μm. The test structure also includes a test pad connected to the at least one microbump pad, and the test pad has a size large enough to allow circuit probing involving at least the first device. The test pad is another part of the metal pad, and a width of the test pad is greater than the at least one microbump pad. The test pad is covered after circuit probe by a passivation material to prevent particle and corrosion issues.

[0043] In yet another embodiment, a method of forming and testing a test structure for electrical tests of devices under one or more microbumps is provided. The method includes depositing a first passivation layer over a metal pad on a semiconductor substrate and defining at least one microbump pad connected to a test pad by patterning the first passivation layer. The at least one microbump pad is connected to an interconnect of a first device. The method also includes performing circuit probing on the test pad to electrically testing devices connected to the at least one microbump pad, and forming a second passivation layer to cover the test pad and to expose the at least one microbump pad. The method further includes forming a microbump in each of the at least one microbump pad.

[0044] Various modifications, changes, and variations apparent to those of skill in the art may be made in the arrangement, operation, and details of the methods and systems disclosed. Although the foregoing embodiments have been described in some detail for purposes of clarity of understanding, it will be apparent that certain changes and modifications may be practiced within the scope of the appended claims. Accordingly, the present embodiments are to be considered as illustrative and not restrictive, and the disclosure is not to be limited to the details given herein, but may be modified within the scope and equivalents of the appended claims.

What is claimed is:

1. A test structure for performing electrical tests of devices under one or more microbumps, comprising:

at least one device; and

a metal pad connected to an interconnect for the at least one device, the metal pad comprising:

a first portion forming at least one microbump pad, wherein a width of the at least one microbump pad is equal to or less than about 50 μm, and

a second portion forming a test pad connected to the at least one microbump pad, wherein the test pad has a size large enough to allow circuit probing of the at least first device, and wherein a width of the test pad is greater than the at least one microbump pad.

2. The test structure of claim **1**, wherein the least one microbump pad is for depositing a microbump in each of the at least one microbump pad, and wherein the microbump has a width in a range from about 20 μm to about 50 μm.

3. The test structure of claim **2**, wherein a space between the at least one microbump pad and the test pad is between about 20 μm to about 80 μm.

4. The test structure of claim **1**, wherein the test pad has a width greater than about 60 μm to allow circuit probe.

5. The test structure of claim **1**, the metal pad is at a level of at least one of a top metal, a pad metal above the top metal, a redistribution layer, or a post passivation interconnect.

6. The test structure of claim **1**, wherein the test pad is adapted to be covered after circuit probing by a passivation material to prevent particle and corrosion issues.

7. The test structure of claim **6**, wherein the passivation material is at least one of a polyimide, a silicon oxide, or a silicon nitride.

8. The test structure of claim **1**, wherein the at least one microbump pad includes 2 to 8 microbump pads, and wherein the 2 to 8 microbump pads are connected to the test pad, and wherein the 2 to 8 microbump pads are symmetrically distributed around the test pad to balance a stress induced by a formation of microbumps on the 2 to 8 microbump pads and to reduce interface delamination of microbumps formed on the 2 to 8 microbump pads.

9. The test structure of claim **1**, wherein the at least one microbump pad includes 2 to 8 microbump pads, and wherein

the 2 to 8 microbump pads are connected to the test pad, and wherein the 2 to 8 microbump pads are asymmetrically distributed around the test pad.

10. The test structure of claim **1**, further comprising additional test pads, and wherein each test pad is connected to one or more microbumps for testing devices connected to the one or more microbumps, and wherein the test pad and the additional test pads are used to test inputs/outputs (I/Os) with different currents.

11. The test structure of claim **1**, wherein the at least one microbump pad is covered by an under bump metallurgy (UBM) layer.

12. The test structure of claim **1**, wherein outlines of the test pad and the at least one microbump pad are defined by a passivation layer.

13. The test structure of claim **1**, wherein more than one device is connected to the at least one microbump pad.

14. A test structure for performing electrical tests of devices under one or more microbumps, comprising:

at least one microbump pad, wherein the at least one microbump pad is a part of a metal pad connected to an interconnect for at least a first device, and wherein a width of the at least one microbump pad is equal to or less than about 50 μm; and

a test pad connected to the at least one microbump pad, wherein the test pad has a size large enough to allow circuit probe involving at least the first device, and wherein the test pad is another part of the metal pad, and wherein a width of the test pad is greater than the at least one microbump pad; wherein the test pad is covered after circuit probe by a passivation material to prevent particle and corrosion issues.

15. A method of forming and testing a test structure for electrical tests of devices under one or more microbumps, comprising:

depositing a first passivation layer over a metal pad on a semiconductor substrate;

defining at least one microbump pad connected to a test pad by patterning the first passivation layer, wherein the at least one microbump pad is connected to interconnect of a first device;

performing circuit probing on the test pad to electrically test devices connected to the at least one microbump pad;

forming a second passivation layer to cover the test pad and to expose the at least one microbump pad; and

forming a microbump on each of the at least one microbump pad.

16. The method of claim **15**, wherein the at least one microbump pad is a part of the metal pad connected to interconnect for at least a first device, and wherein a width of the at least one microbump pad is equal to or less than about 50 μm, wherein the test pad connected to the at least one microbump pad, wherein in the test pad has a size large enough to allow circuit probe involving the at least first device, and wherein the test pad is another part of the metal pad, and wherein a width of the test pad is greater than the at least one microbump pad.

17. The method of claim **15**, wherein an under bump metallurgy (UBM) layer is formed between the microbump and each of the at least one microbump pad underneath the microbump.

18. The method of claim **15**, wherein the second passivation layer is deposited over the test pad to protect damaged surface due to circuit probe from causing particles and corrosion, and wherein the second passivation layer is at least one of a polyimide, an silicon oxide, or a silicon nitride layer.

19. The method of claim **15**, wherein the microbump has a width in a range from about 20 μm to about 50 μm, and wherein a space between the at least microbump and the test pad is between about 20 μm to about 80 μm, and wherein the test pad has a width greater than about 60 μm to allow circuit probing.

20. The method of claim **15**, wherein the at least one microbump pad includes 2 to 8 microbump pads, and wherein the 2 to 8 microbump pads are connected to the test pad, and wherein the 2 to 8 microbump pads are symmetrically distributed around the test pad to balance a stress induced by a formation of microbumps on the 2 to 8 microbump pads and to reduce interface delamination of microbumps formed on the 2 to 8 microbump pads.

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