UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY LTD.

and

APPLE INC.

Petitioners

v.

MYW SEMITECH, LLC,
Patent Owner

Inter Partes Review Case No. IPR2026-00067
U.S. Patent No. 11,894,306

PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 11,894,306

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I. INTRODUCTION

IPR is requested of claims 1-27 of USPN 11,894,306. The '306 Patent claims a chip package comprising various well-known components of semiconductor and chip packaging designs. Neither the claimed components nor their claimed configuration is new or non-obvious.

II. LEVEL OF ORDINARY SKILL IN THE ART

A POSITA at the time of the '306 Patent would have had at least a bachelor's degree in electrical engineering, materials science, or physics (or an equivalent degree), and at least two years of experience in semiconductors or semiconductor manufacturing. A master's degree or Ph.D. in a relevant field may substitute for some work experience or vice versa. Additional education or experience might substitute for the above requirements.

III. REQUIREMENTS UNDER 37 C.F.R. § 42.104

A. Grounds for Standing Under 37 C.F.R. § 42.104(a)

Petitioners certify the '306 Patent is eligible for IPR.

B. Identification of Challenge Under 37 C.F.R. § 42.104(b)

Petitioners request the Challenged Claims be found unpatentable on the following grounds[1].

[1] All references qualify as prior art under at least one of pre-AIA §§102(a), 102(b), or 102(e).

Grounds	Claims Challenged	35 U.S.C. §	References
1A	1-7, 9-11, 13-15, 17-27	103	Sundaram (EX1004) and Lin-191 (EX1005)
1B	8, 12, 16	103	Sundaram, Lin-191, and Lin-863 (EX1007)
2A	1-7, 9-15, 17-20, 22-27	103	Yu (EX1010) and Lin-191
2B	8, 16	103	Yu, Lin-191, and Lin-863
2C	21	103	Yu, Lin-191, and Camacho (EX1006)

C. Claim Construction Under 37 C.F.R. § 42.104(b)(3)

For this IPR only, claim construction is unnecessary because, as set forth herein, the prior art falls within the indisputable scope of the Challenged Claims under any reasonable construction (including any proposed in litigation).

IV. ANALOGOUS PRIOR ART

The prior art is analogous to the claimed invention of the ’306 Patent. The prior art is from the same field of endeavor of the ’306 Patent, namely semiconductor packaging. *EX1001*, 1:28–2:3, 3:37-40, 14:16-17; *EX1004*, 1:33-42, 5:16-19, 7:61-67; *EX1005*, [0003], [0007]; *EX1006*, [0001], [0008]-[0009], [0016]; *EX1007*, 1:7-10, 1:14–2:25; *EX1010*, Abstract, 1:10-55, 1:63-67, 4:17-20; *EX1003*, ¶¶31-33, 93, 102, 107, 114, 121.

The prior art is also reasonably pertinent to at least one purported problem identified in the ’306 Patent, namely:

A. Minimizing temperature coefficient of expansion mismatching; *EX1001*, 1:67-2:3; *EX1004*, 5:62-63; *EX1007*, 2:29-48, 11:20-46, 12:11-32, 14:43-65; *EX1010*, 6:20-26;

B. Creating chip packages with pre-testability capability; *EX1001*, 1:67-2:3; *EX1004*, 7:41-43, 2:34-35; *EX1005*, [0006], [0105], [0173], [0239], [0401], [0462], [0492-0493]; *EX1010*, 2:17-20; and/or

C. The impact of miniaturization on circuit performance; *EX1001*, 1:37-41; *EX1004*, 1:15-32, 2:21–3:6; *EX1006*, [0028]; and/or

D. Parasitic capacitance of interconnections in a chip package; *EX1001*, 1:36-42; *EX1006*, [0038]; *EX1003*, ¶¶34-38, 94, 103, 108, 115, 122-123.

V. GROUND 1A: CLAIMS 1-7, 9-11, 13-15, AND 17-27 ARE OBVIOUS OVER SUNDARAM AND LIN-191

A. Claim 1

1. 1(Pre)

Sundaram teaches a *chip package*[2] formed by an "interconnect structure 100 compris[ing] an interposer 105" that interconnects a "first electronic device 125"

[2] Claim language provided in italics. All drawing annotations added. Citations to a claim limitation and/or section number are to the limitations mapping in this Petition and are incorporated by reference, including the motivations to combine (MTC) and showing of reasonable expectation of success (REOS) provided in the cross-

and a "second electronic device 130." *EX1004*, 5:45-58, 6:34-46 (devices 125, 130 are chips), FIG. 33. The interconnect structure 100 "enables the interposer 105 and the **package** can [*sic*] be one and the same." *EX1004*, 7:61-63.

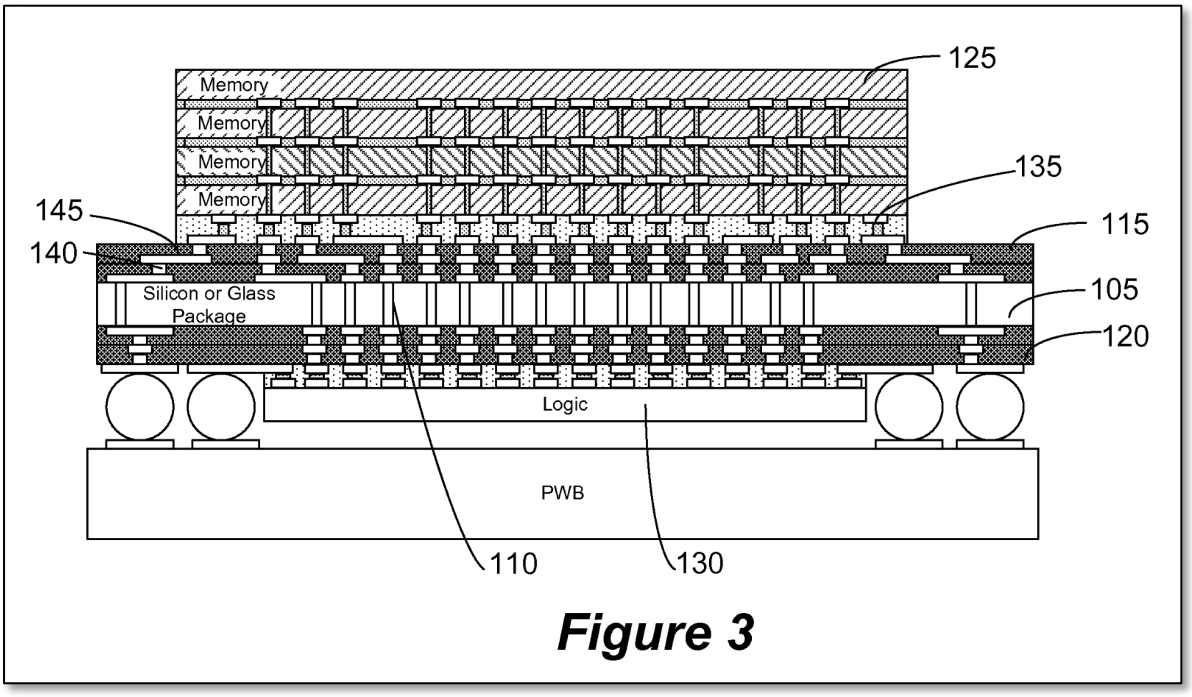


Figure 3

EX1004, FIG. 3; *EX1003*, ¶125 .

2. 1(a)

Sundaram's interconnect structure "comprises an interposer [105] having a first side and a second side" (*a first surface and a second surface*) and is "made of…glass" or "polymer-glass laminates," such that interposer 105 is a *solid layer*.

referenced section. All REOS include the benefits described for the respective MTC. All emphases added unless otherwise noted.

EX1004, 2:22-27, 5:54-58. Shown in FIG. 3, below, Sundaram's *second surface* is *opposite to said first surface*.

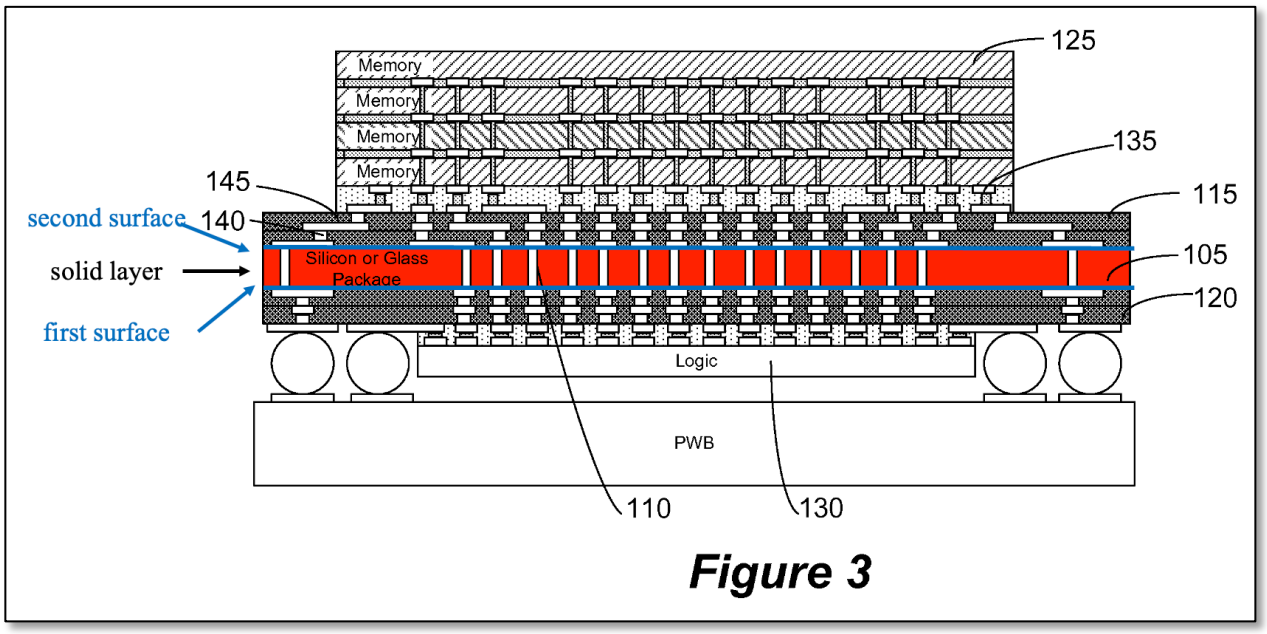


Figure 3

EX1004, FIG. 3; *EX1003*, ¶¶126-127.

3. 1(a)(i)

Interposer 105 comprises "glass," i.e., *a compound of silicon and oxygen*. *EX1004*, 5:54-58, 9:14-16 (borosilicate glass); *EX1003*, ¶128.

Alternatively, Sundaram teaches interposer 105 comprises "silicon" with an **SiO_2** layer. *EX1004*, 5:54-58, 14:58-62.

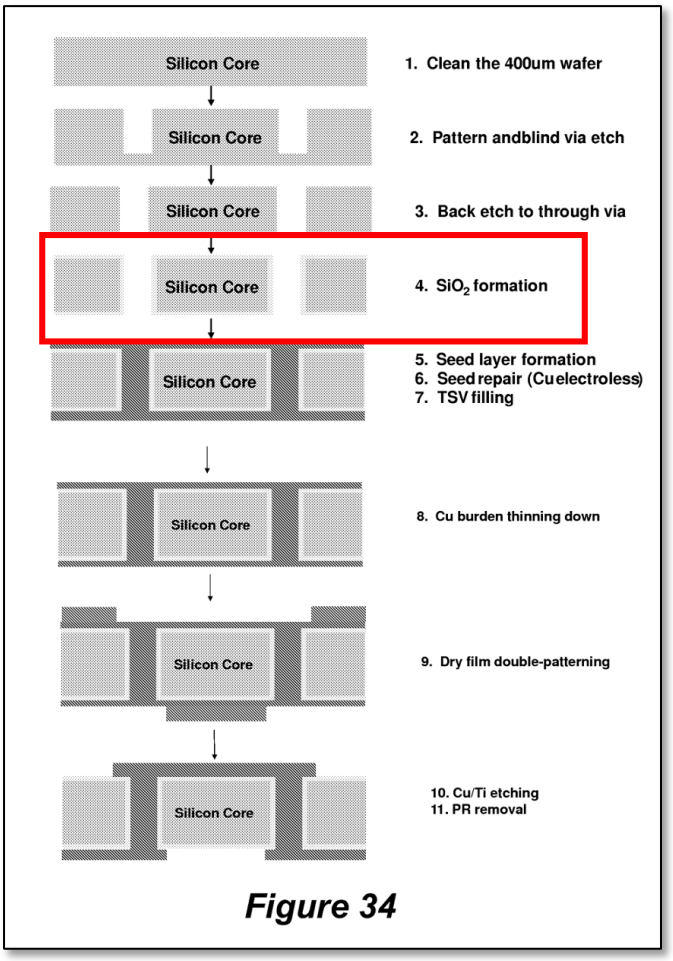


Figure 34

EX1004, FIG. 34; *EX1003*, ¶129.

4. 1(a)(ii)

Sundaram teaches or renders obvious the claimed thickness. Sundaram teaches interposer 105 (*solid layer*) is "about 20 to about 200 micrometers in thickness" or "about 20-100 micrometers," which overlaps with the claimed *thickness* range. *EX1004*, 2:22-25, 5:50-53. Additionally, the '306 Patent does not ascribe any criticality to the claimed range of 50 to 150 micrometers. Indeed, the '306 Patent describes a variety or ranges, including smaller (20 micrometers) and

much larger values (2000 micrometers), indicating to a POSITA that the thickness can vary widely and that the thickness is not otherwise critical. *EX1001*, 7:58-64; *EX1003*, ¶¶130-131; *Clearvalue, Inc. v. Pearl River Polymers, Inc.*, 668 F.3d 1340, 1345 (Fed. Cir. 2012) (finding the prior art reference's teaching of "150 ppm or less" anticipated claimed "less than or equal to 50 ppm" where the challenged patent did not indicate criticality of the claimed range); MPEP 2131.03(II); *UCB Inc., et al. v. Actavis Labs. UT, Inc., et al.*, 65 F.4th 679, 689-90 (Fed. Cir. 2023) ("A presumption of obviousness applies '[w]here a claimed range overlaps with a range disclosed in the prior art.'" (quoting *Ormco Corp. v. Align Tech., Inc.*, 463 F.3d 1299, 1311 (Fed. Cir. 2006)); MPEP 2144.05.

5. 1(a)(iii)

Sundaram's interposer includes *a first region* *and* *a second region* *between said first region and a first edge of said solid layer*:

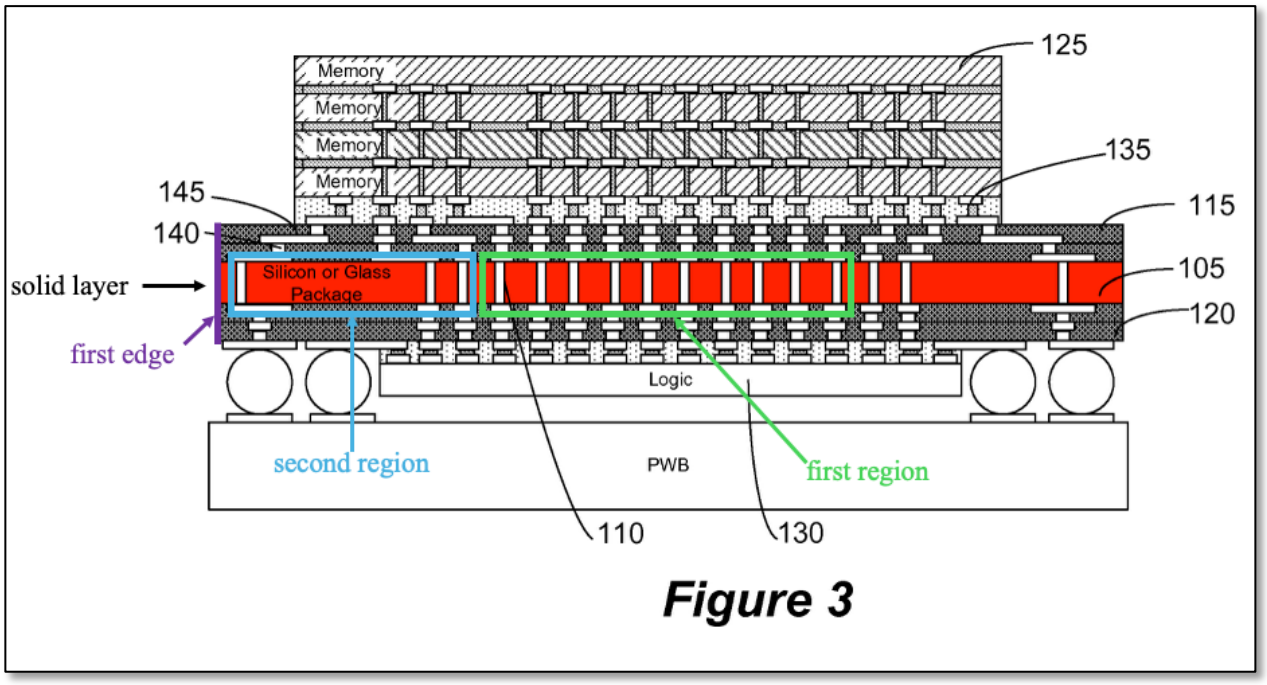


Figure 3

EX1004, FIG. 3; *EX1003*, ¶132.

6. 1(b)

Sundaram teaches a *plurality of metal posts in a plurality of through holes*, i.e., metalized through vias 110 where the metallization forms *metal posts* that are in *through holes*. Specifically, Sundaram teaches "through vias 110 can be defined within the interposer" and "metalized with a highly-conductive **metal**." *EX1004*, 6:6-9, 6:25-27, 13:30-34. Through vias 110 are *in said second region*:

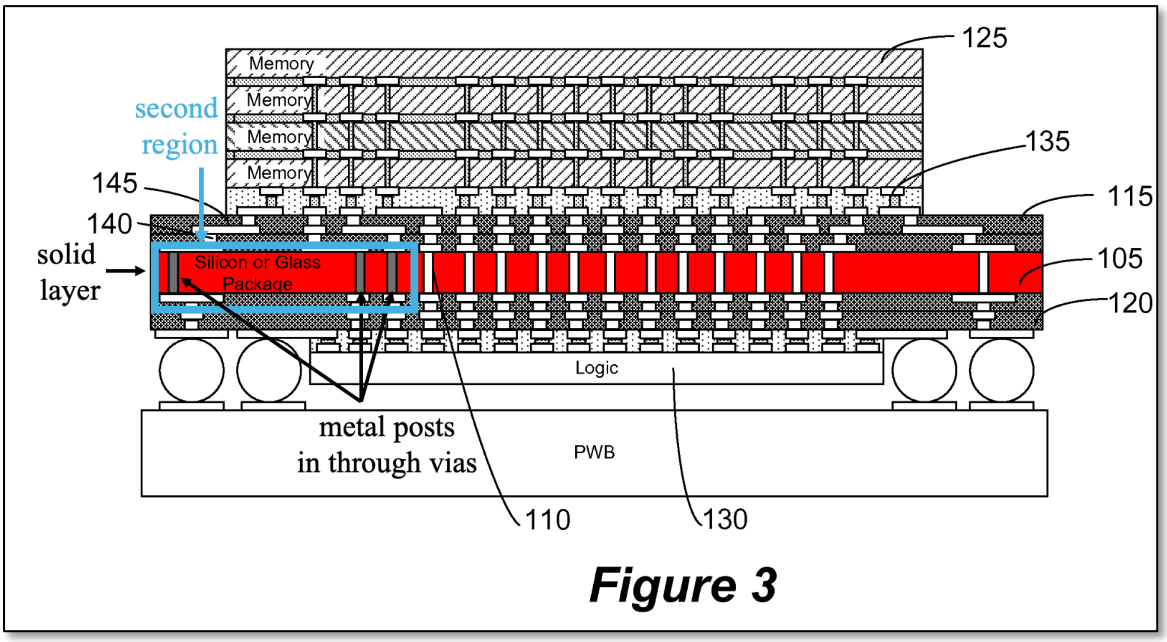


Figure 3

EX1004, FIG. 3; *EX1003*, ¶133.

7. 1(b)(i)

Sundaram teaches "metaliz[ing]" the through vias 110 with copper such *one of said plurality of metal posts comprises a first copper layer contacting a sidewall of* a through via 110. *EX1004*, 6:22-27, 13:30-34; *EX1003*, ¶¶134-135.

8. 1(b)(ii)

See Section V.A.5. The claimed *regions* are not described in the '306 Patent's written description. Applicant relied solely on Applicant-annotated FIG. 6l as support during original examination of the '306 Patent's parent application (USPN 11,538,763), illustrating the claimed *width*, *distance*, and *pitch*.

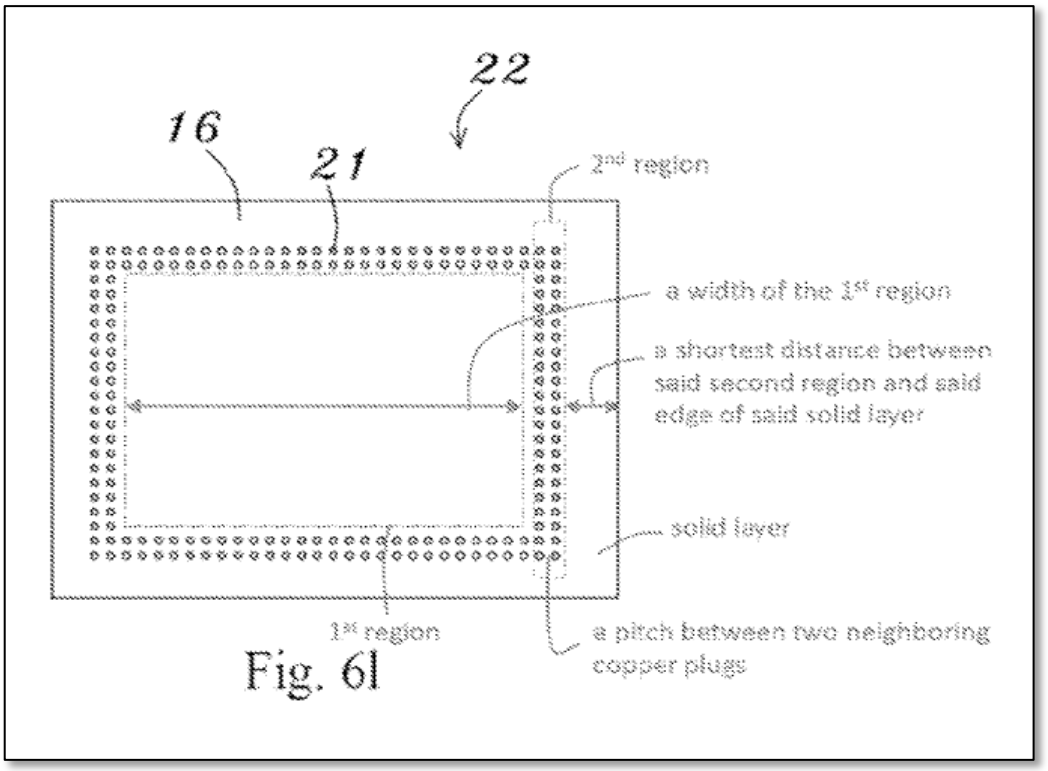


Fig. 6I

EX1117, 272; *Omega Eng'g, Inc. v. Raytek Corp.*, 334 F.3d 1314, 1333 (Fed. Cir. 2003) (prosecution disclaimer of parent application attaches to child application); *In re McDonald*, 43 F.4th 1340, 1347 (Fed. Cir. 2022); *EX1003*, ¶137.

Sundaram, including Sundaram's figures, similarly teaches the claimed *regions*. As shown below, Sundaram's *first region has a width in a direction* (denoted D1) *that is greater than a shortest distance between said sidewall of one of said plurality of through holes and said first edge in said direction* (denoted D2), and *a pitch between two neighboring metal posts* (denoted D3):

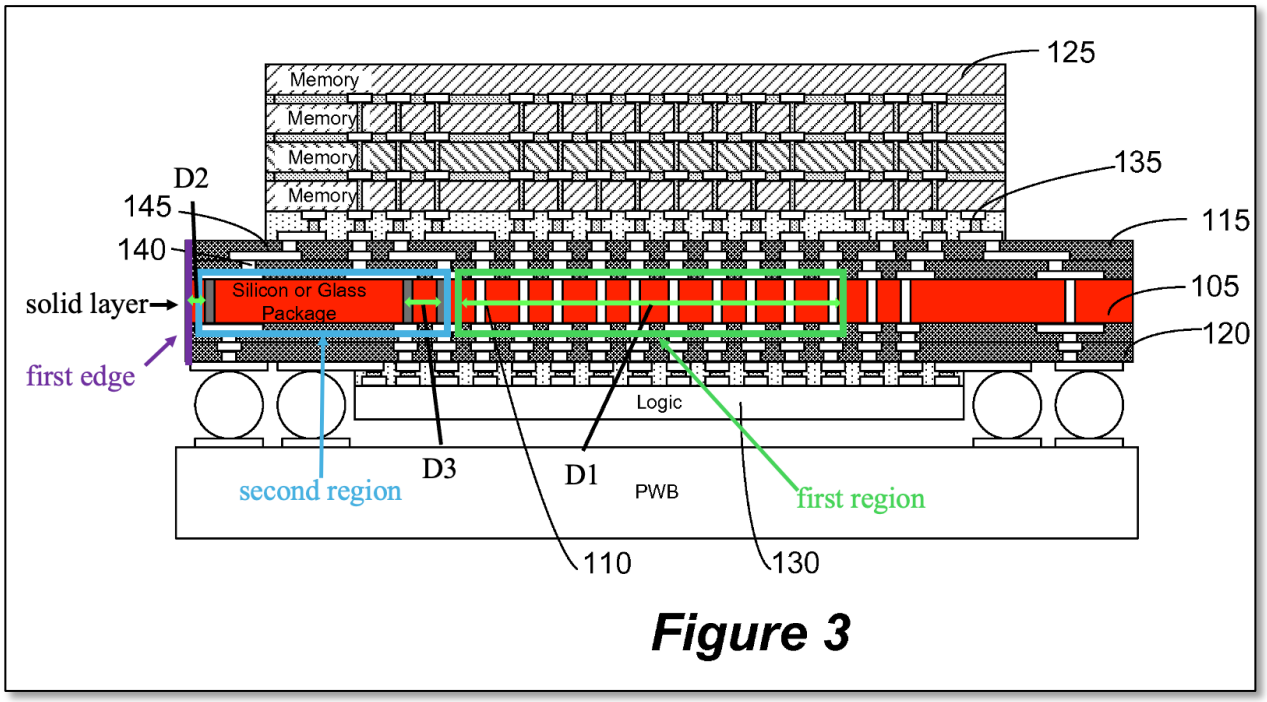


Figure 3

EX1004, FIG. 3; *EX1003*, ¶136; *Regents of Univ. of California v. Satco Prods., Inc.*, No. 2023-1356, 2024 WL 4972639 (Fed. Cir. Dec. 4, 2024) ("[P]atent drawings may be useful in shedding light about the general shapes and relative sizes of elements of the claimed invention, as well as their spatial relations to one another."); *Mahle Behr Charleston Inc. v. Catalano*, IPR2023-00861, Paper 15, at 6-7 (PTAB Apr. 5, 2024) (Director Review).

9. 1(c)

Sundaram teaches "polymer-metal redistribution layers" are "deposited on the first side 115 and second side 120 of the interposer 105" and include "blind vias 140 and conductor traces 145[.]" *EX1004*, 6:62-67. Electronic devices 125, 130 "are connected with through vias 110, blind vias 140, [] conductor traces 145," and "die

pads 135" that are formed *over said first surface*. *EX1004*, 7:4-8, 6:29-33. Thus, blind vias 140, conductor traces 145, pads 135, and the polymer in the polymer-metal redistribution layer (RDL) form *a first interconnection scheme over*[3] *said first surface*.

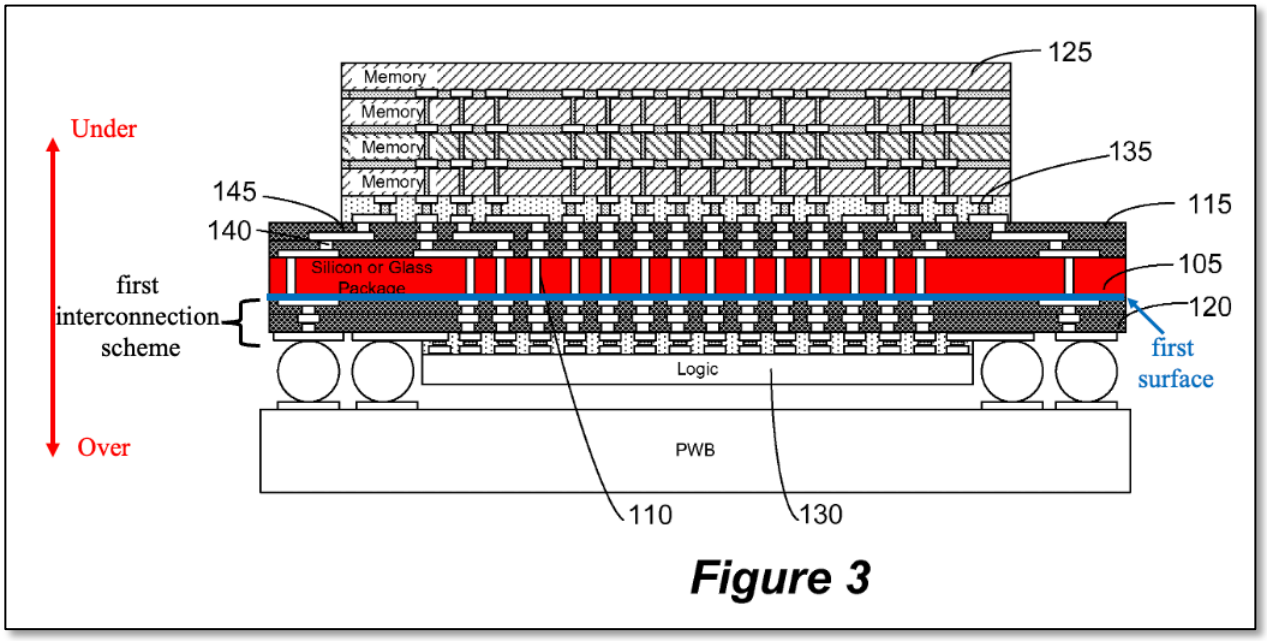


Figure 3

EX1004, FIG. 3; *EX1003*, ¶140.

[3] Each reference's figures indicate the *over/under* direction where appropriate. The *over* direction is towards the PWB. *EX1003*, ¶138. PO similarly used inverted figures during original prosecution of the related USPN 11,107,768 to explain the *over/under* relationship between various claim elements. *Compare EX1001*, FIG. 9t *with EX1032*, 395-400, 537-538; *EX1003*, ¶139.

10. 1(c)(i)

The "blind vias 140" and "conductor traces 145" are the "metal" in the "polymer-metal redistribution layers" such that vias 140 and traces 145 are *metal interconnects* of the *first interconnection scheme*. *EX1004*, 6:62-7:8. Shown below in Sundaram's RDL is a *first metal interconnect* comprising a trace 145 (longer rectangles in FIG. 3) and a via 140 (shorter rectangles), which is *over said second surface*. *EX1003*, ¶¶141-142. Further depicted is a *polymer layer over said first metal interconnect* (the "polymer" of the "polymer-metal redistribution layers."). *EX1004*, 6:62-67; *EX1003*, ¶¶144-145 (discussing the related '768 Patent's prosecution history). The *polymer layer* at least includes the below highlighted layer but may include an additional portion of the RDL (*see* Claim 10(f)(i), Section V.I.16.

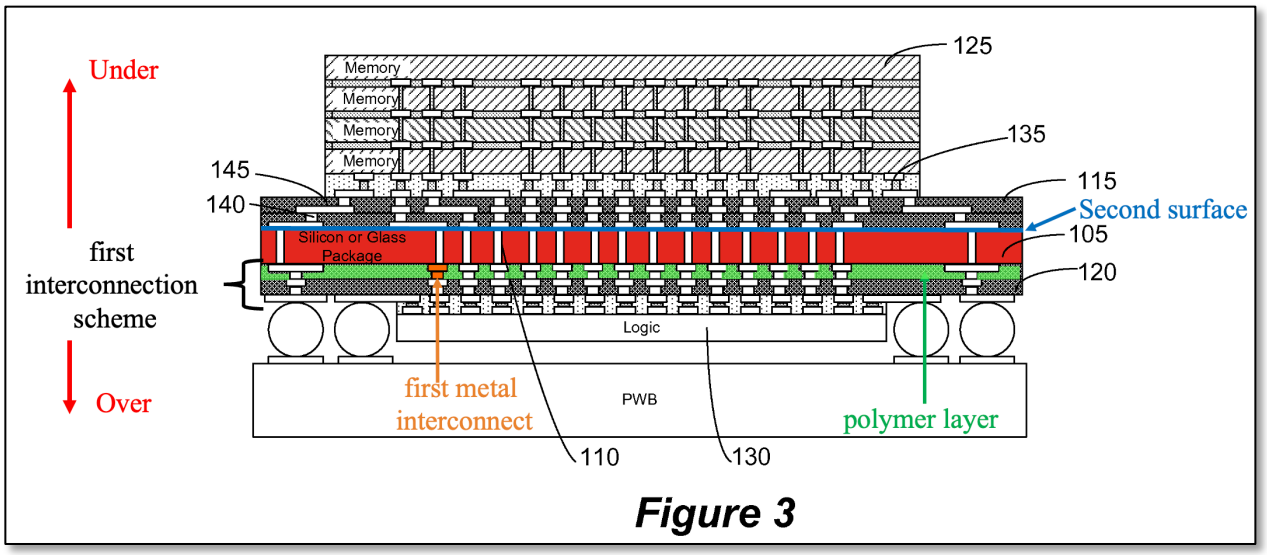


Figure 3

EX1004, FIG. 3.

Alternatively, Sundaram's outermost layer of the RDL is *a polymer layer* and is *over* the *metal interconnect*.

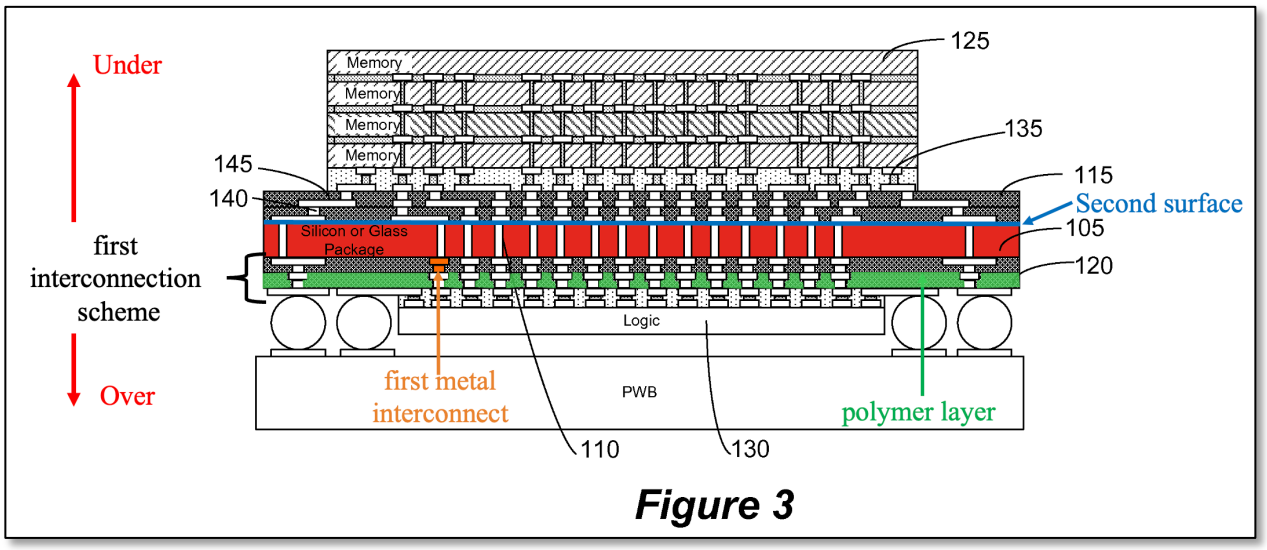
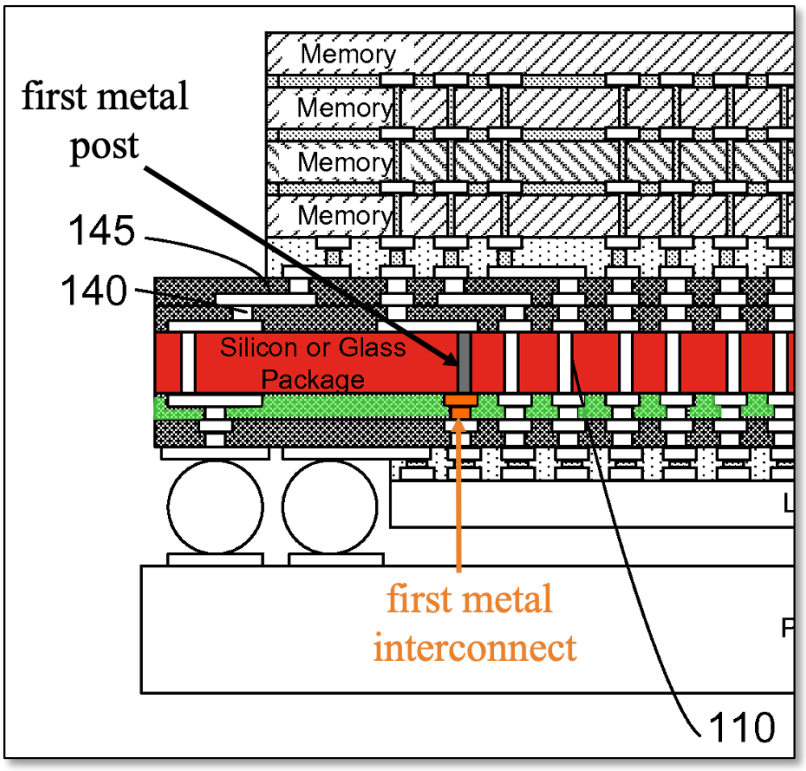


Figure 3

EX1004, FIG. 3; ¶143.

11. 1(c)(ii)

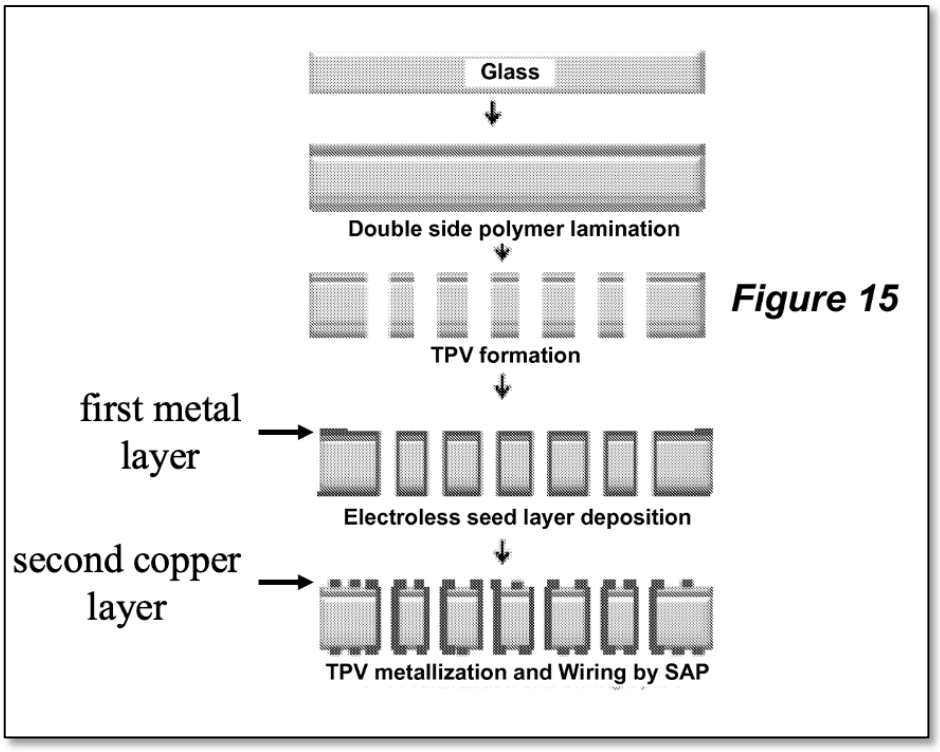
Sundaram's *first metal interconnect* is *connected to a first metal post* as Sundaram teaches devices 125, 130 "are connected with through vias, 110, blind vias 140, and conductor traces 145." *EX1004*, 7:4-9.



EX1004, FIG. 3 (excerpt); *EX1003*, ¶146.

12. 1(c)(iii)

Sundaram teaches a *first metal layer* formed by "direct metallization using wet electroless copper deposition" and *a second copper layer over said first metal layer* formed by "semi-additive plating" using "copper as metal." *EX1004*, 9:61-65, 10:26-28; *EX1003*, ¶147.



EX1004, FIG. 15.

To the extent PO argues Sundaram's FIGS. 3 and 15 embodiments are separate, a POSITA would have been motivated, found it obvious, and had a REOS in applying FIG. 15's *layer* teachings to FIG. 3's interconnect structure. *EX1003*, ¶148. A POSITA would have appreciated the advantages of FIG. 15's seed layer (*first metal layer*) for promoting growth of the *second copper layer*, which a POSITA would have understood as necessary in forming a copper via in a glass interposer because glass is insulating. *EX1003*, ¶148. There would have been a REOS because FIG. 15 teaches "process flow" for fabricating a "glass test vehicle," i.e., the same material as FIG. 3's glass interposer. *EX1004*, 10:9-15, 8:1, 5:54-59; *see* Section V.A.3; *EX1003*, ¶148.

13. 1(d)

Sundaram teaches *a first metal bump over said first interconnection scheme*, namely, a "copper **bump**[] with solder cap[]" that "can electrically connect devices." *EX1004*, 6:29-32.

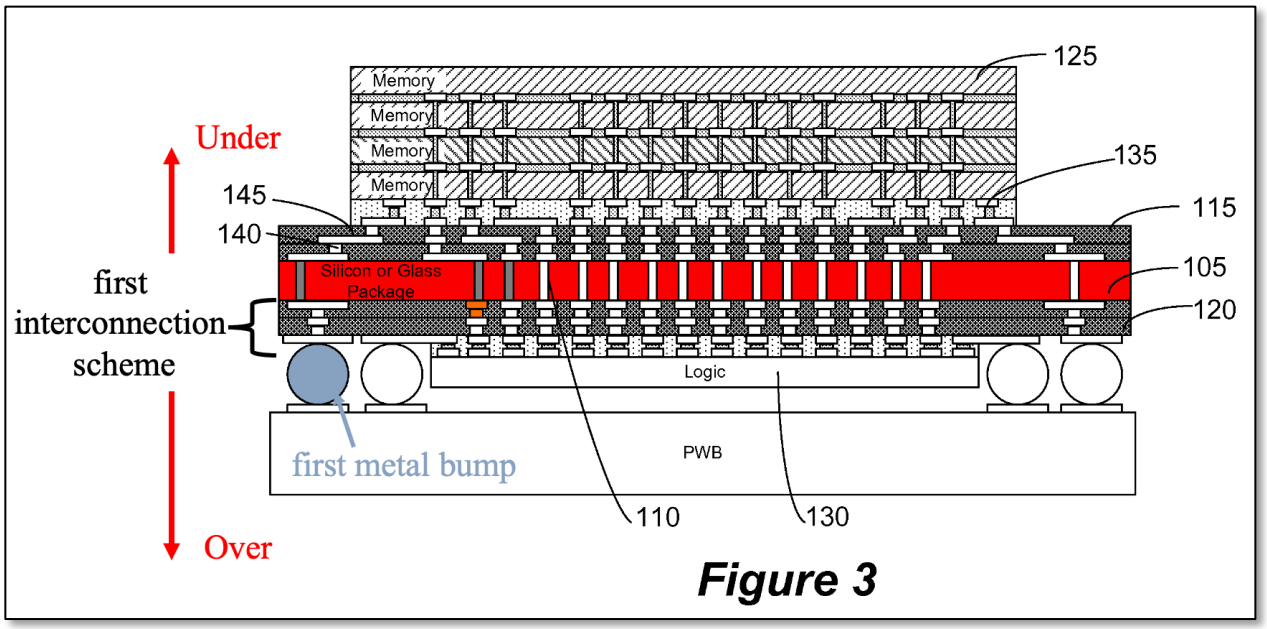


Figure 3

EX1004, FIG. 3; *EX1003*, ¶149.

14. 1(d)(i)

Sundaram's "copper bumps with solder caps" teach *a second metal layer* (the copper bump) *and a first tin-containing layer over said second metal layer* (the solder cap) as a POSITA would have understood solder to include tin. *EX1004*, 6:29-32. Sundaram thus teaches this limitation. *EX1003*, ¶150.

a) Lin-191's Teachings

Additionally, or alternatively to Sundaram's teachings, Lin-191 teaches a *bump* with the claimed layers. Specifically, Lin-191 teaches a system-in-package

including "solder bumps or balls 29a" formed by reflowing a "solder layer 29," which is "**a tin-containing layer**" formed on the metal layer 28 of the UBM structure. *EX1005*, [0320]. Metal layer 28, along with "adhesion layer 18, the seed layer 19, and **metal** layer[] 27…compose an under bump metallurgic (UBM) layer." *EX1005*, [0323]. Layers 18, 19 are *metal*. *EX1005*, [0308].

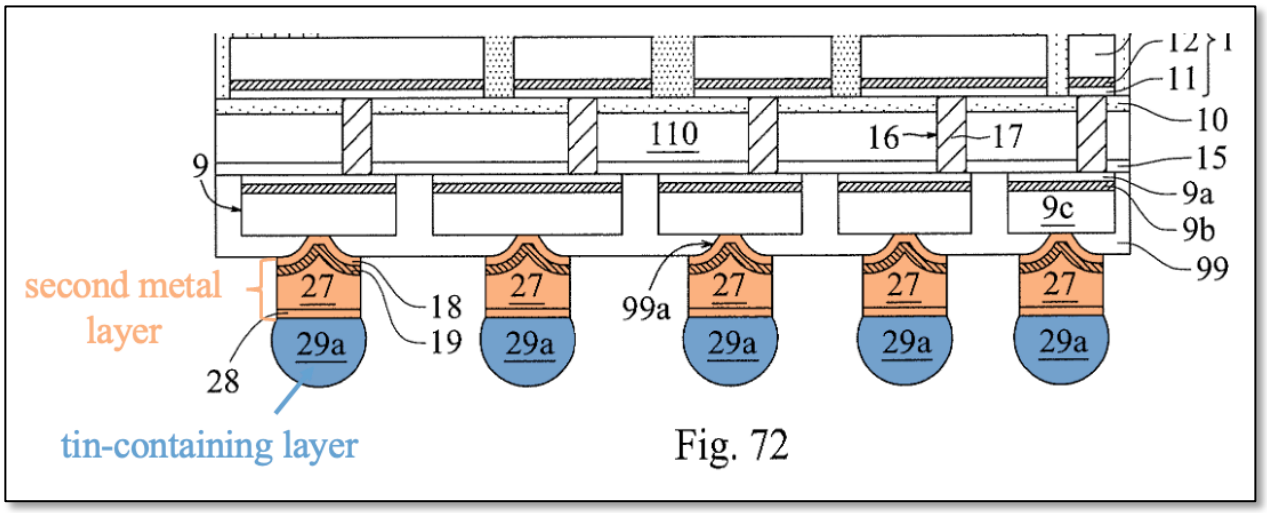


Fig. 72

EX1005, FIG. 72 (excerpt); *EX1003*, ¶¶151-152.

Thus, Lin-191 teaches *a metal bump compris[ing] a second metal layer* (UBM layer) *and a first tin-containing layer* (solder layer 29) *over said second metal layer*.

b) MTC

A POSITA would have been motivated and found it obvious to apply Lin-191's teachings of a metal bump having *a first tin-containing layer over a second metal layer* to Sundaram's copper bump. *EX1003*, ¶¶153-155. A POSITA would have appreciated the advantages of applying Lin-191's teachings of a solder ball

having a tin-containing layer 29 and the UBM metal layer to improve the strength of Sundaram's copper bump. *EX1005*, [0323], [0437]; *EX1003*, ¶¶153-155. A POSITA would have appreciated the advantage of a *tin-containing layer*, which was known to "wet and spread on a wide range of substrates…." *EX1098*, 104; *EX1003*, ¶153.

The Sundaram-Lin-191 combination is the application of a known technique (Lin-191's bump structure) to a known device (Sundaram's bump) ready for improvement to yield predictable result of Sundaram's bump (*first metal bump*) being formed according to Lin-191's teachings. *EX1003*, ¶156. Alternatively, the Sundaram-Lin-191 combination is the simple substitution of Lin-191's solder bump structure for Sundaram's "copper bumps with solder caps." *EX1004*, 6:29-33; *EX1003*, ¶157.

A POSITA would have had a REOS in either applying Lin-191's teachings to Sundaram's bump or substituting Sundaram's bump with Lin-191's bump at least because such a modification/substitution would have involved the application of well-known manufacturing techniques well within the skill of a POSITA. *EX1003*, ¶158. Furthermore, metal bump technology, including UBM layers were commonplace prior to the '306 Patent. *EX1003*, ¶158.

15. 1(e)

Sundaram's first electronic device 125 "can be…stacked memory IC devices" such that a memory chip of the stack is *a first semiconductor chip under said second surface*. *EX1004*, 6:34-46.

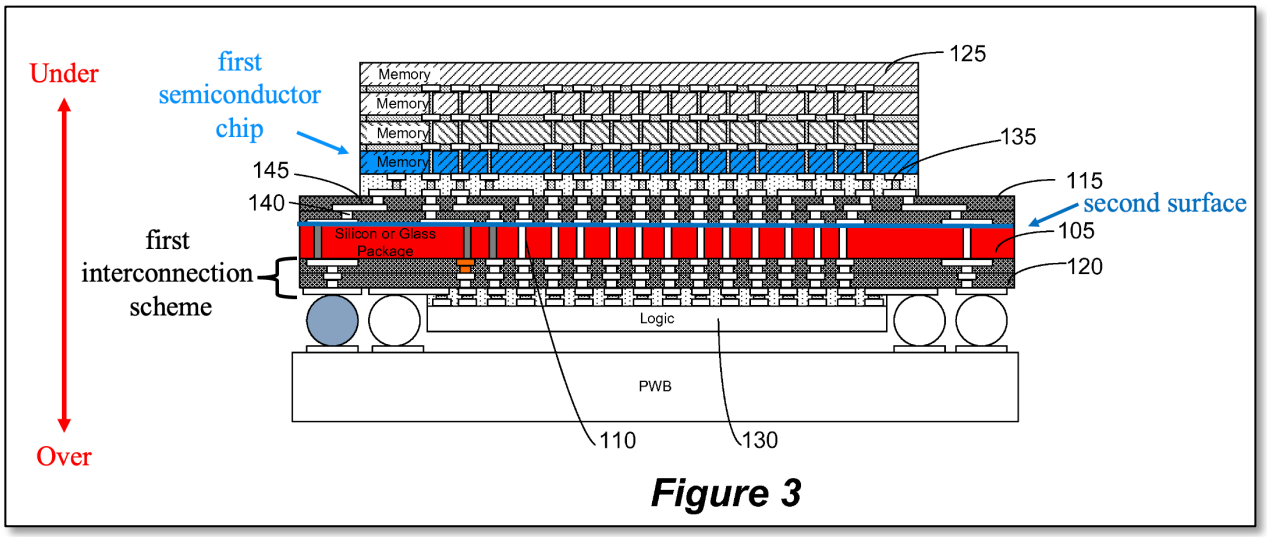


Figure 3

EX1004, FIG. 3; *EX1003*, ¶159.

16. 1(e)(i)

Sundaram's *first interconnection scheme* comprises a *second metal interconnect*, namely a die pad. Sundaram teaches "metallization provides die pad surfaces 135" on "the second side 120 of the interposer 105" that "electrically connect devices," and are therefore *metal interconnect[s]*. *EX1003*, ¶160. FIG. 3 illustrates numerous die pad surfaces. An example one of the many die pad surfaces is identified with reference numeral 135 in FIG. 3. *EX1004*, 6:22-33 (referencing die pads (plural)). A POSITA would have understood FIG. 3 expressly teaches a die pad such as the orange-highlighted die pad in the below FIG. 3 at least because of the

ubiquity of connecting bumps to pads. *EX1003*, ¶160. The orange-highlighted die pad is part of the *first interconnection scheme*. *EX1004*, 6:22-33; *EX1003*, ¶160.

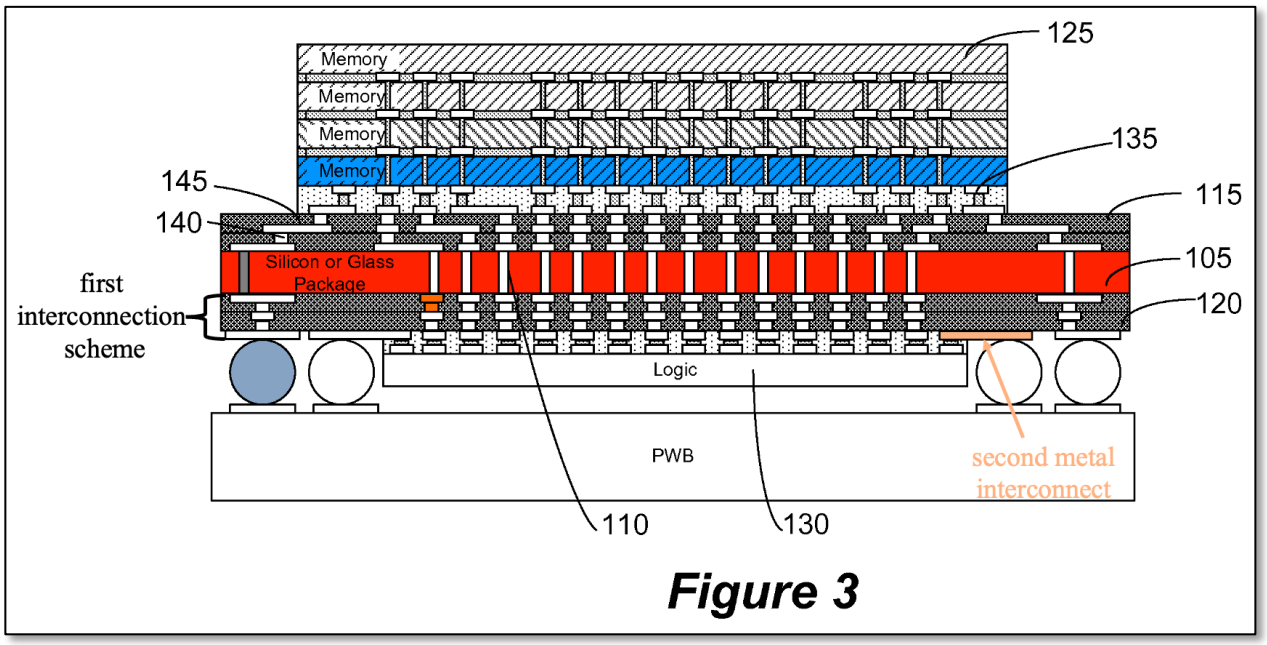
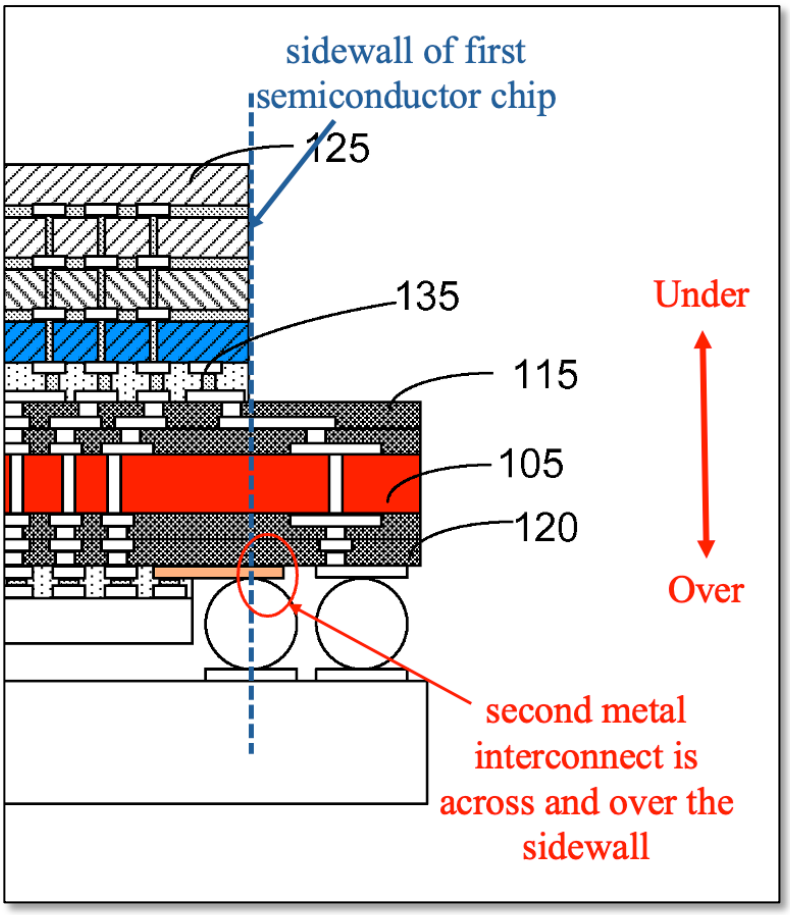


Figure 3

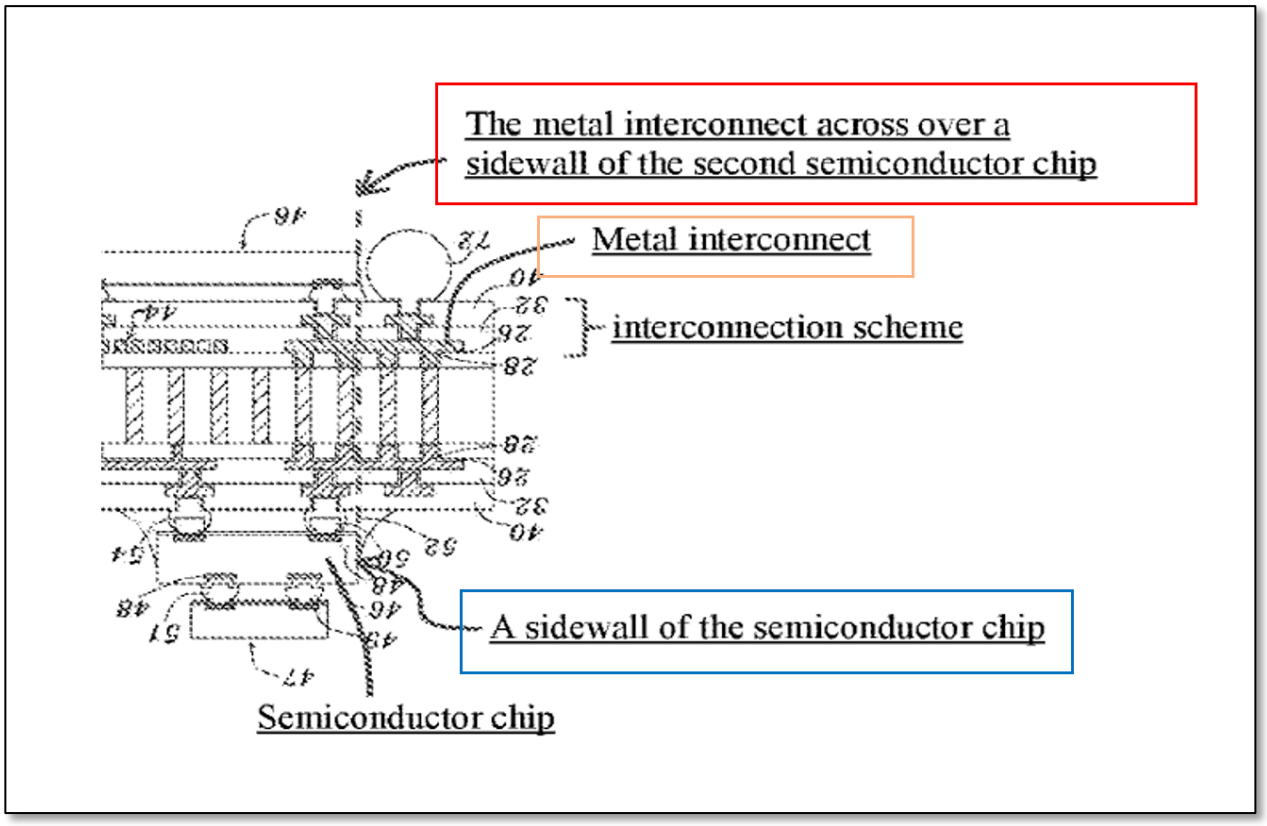
EX1004, FIG. 3.

Sundaram further teaches the orange-highlighted die pad is *across over a sidewall of the first semiconductor chip* (electrical device 125). Sundaram's purple-highlighted pad is *across over* device 125's *sidewall* because the pad is positioned on the opposite side of interposer 105 from device 125's sidewall (*over*) and comprise at least a portion extending laterally beyond device 125's *sidewall* (*across*). *EX1003*, ¶161; *see* cited caselaw in Section V.A.8



EX1004, FIG. 3 (excerpt).

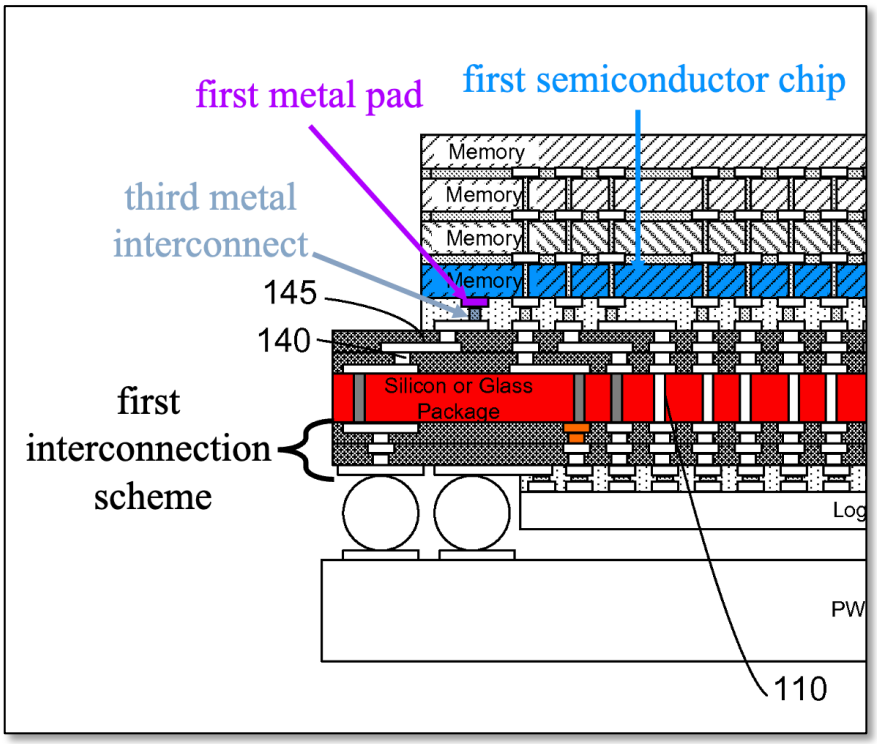
During prosecution of the '306 Patent's grandparent application (USPN 11,107,768), PO provided an annotated figure illustrating specification support for this limitation, similar to Sundaram's purple-highlighted pad relative to device 125.



EX1032, 537; *EX1003*, ¶162; *see* cited caselaw in Section V.A.8.

17. 1(e)(ii)

Sundaram's interposer 105 has die pads where "metallization provides die pad surfaces[.]" *EX1004*, 6:23-25. A POSITA would understand that device 125 also has die pads (purple) such that an electrical connection is made between interposer 105 and device 125, thus teaching the *first semiconductor chip* having a *first metal pad*. *EX1003*, ¶163. Further, Sundaram teaches "die pads 135…can electrically connect devices using solder, copper bumps with solder caps, [and] copper to copper bonding," each of which teaches *a third metal interconnect*. *EX1004*, 6:29-33. In FIG. 3, the *third metal interconnect* is a bump on the metal pad.



EX1004, FIG. 3 (excerpt).

Additionally or alternatively, FIG. 32 is a "side-by-side configuration" of the interconnect structure, which includes a memory stack where each chip has a *metal pad*:

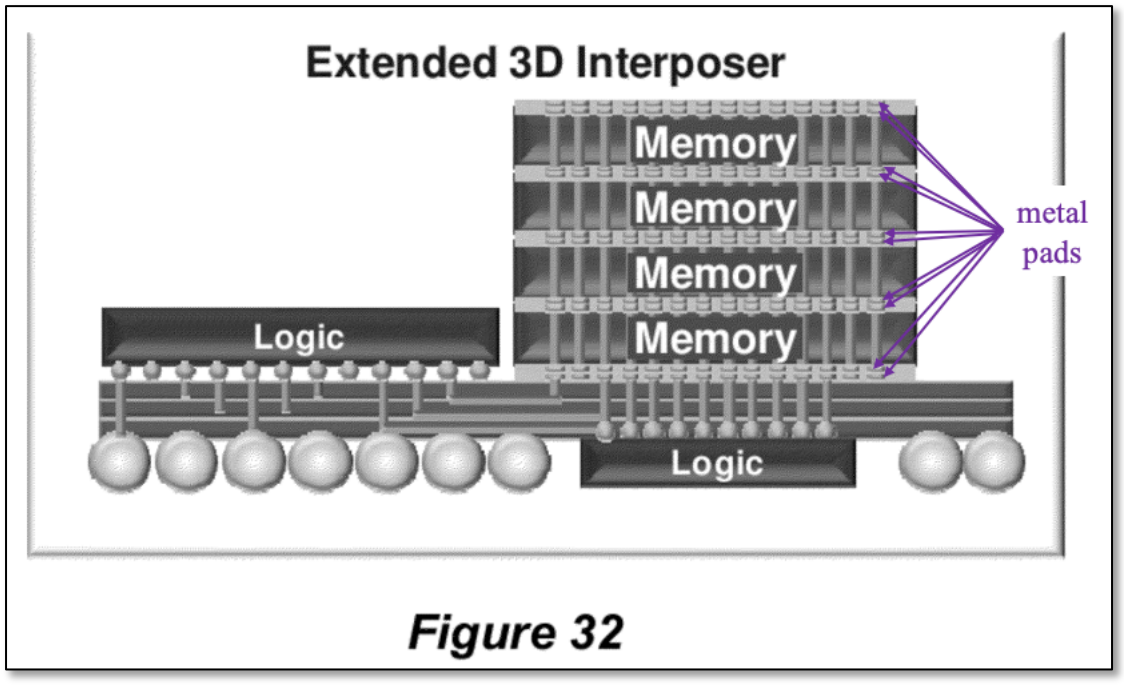
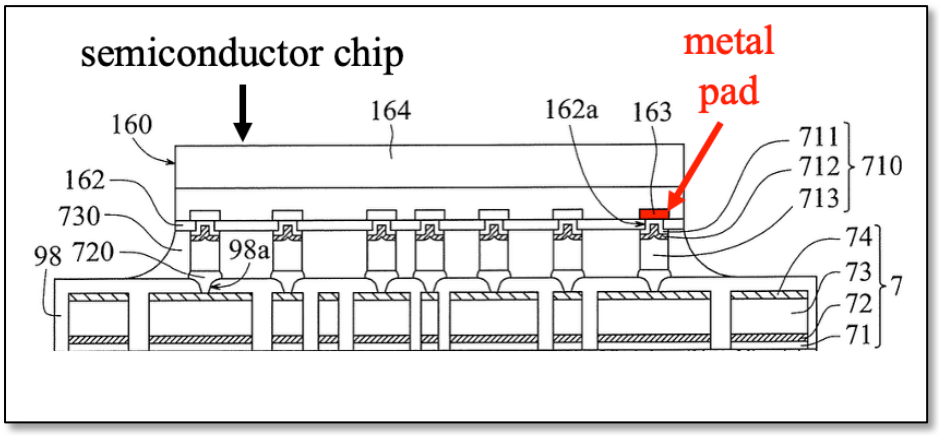


Figure 32

EX1004, FIG. 32, 4:26-27, 7:56-59; *EX1003*, ¶164. MTCs and REOS are below for modifying Sundaram's chip to have a *metal pad* and are incorporated. *See* Section V.A.17.b.

a) Lin-191's "Metal Pad" Teachings

Additionally or alternatively to Sundaram's teachings, Lin-191's system-in package has a semiconductor chip 160 with "**metal** traces or **pads** 163" that include "aluminum." *EX1005*, [0384].



EX1005, FIG. 71 (excerpt); *EX1003*, ¶165.

b) MTC

A POSITA would have been motivated and found it obvious to modify Sundaram per Lin-191's metal pad teachings. *EX1003*, ¶166. The modification is merely an implementation detail in Sundaram's chip package, and the combination is the application of a known technique (metal pads) to a known device (Sundaram's semiconductor chip having die pads) ready for improvement to yield the predictable result of Sundaram's device 125 having a *first metal pad*. *EX1005,* [0081]; *EX1003*, ¶166. Because chips having metal pads are ubiquitous and essential for interconnecting the chip to other components, the modification has an REOS. *EX1003*, ¶167.

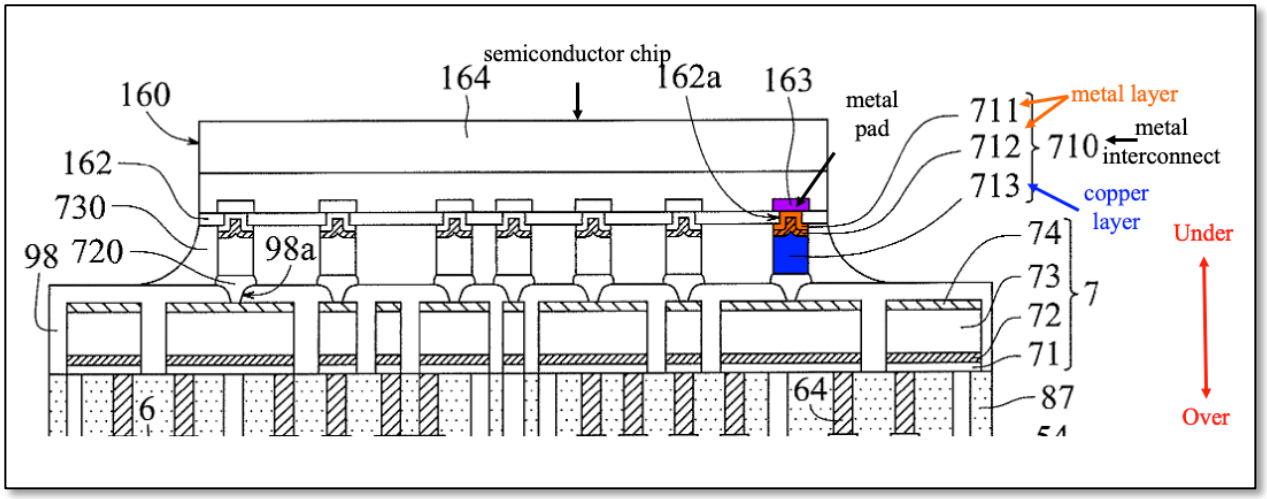
18. 1(e)(iii)

a) Lin-191's Teachings

Lin-191's semiconductor chip 160 has "**metal** traces or **pads** 163" that include "aluminum." *EX1005*, [0384]. Metal bumps 710 are *on* "the metal traces or pads

163," and bumps 710 *interconnect* chip 160 to another chip 140 such that bumps 710, like Sundaram's copper bumps, are *metal interconnect[s]*. *EX1005*, [0406]; *EX1003*, ¶168.

Bumps 710 include an "adhesion layer 711 under the contact points…of the metal traces or pads 163…a seed layer 712 under the adhesion layer 711, and a metal layer 713 under the seed layer[.]" *EX1005*, [0389]. Adhesion layer 711 includes "nickel" or "titanium." *EX1005*, [0390]. Seed layer 712 "can be a copper layer." *EX1005*, [0392]. Thus, the combination of layers 711 and 712 is a *third metal layer on* metal pad 163. *EX1003*, ¶168. Metal layer 713 is "a single **copper** layer having a thickness…between 2 and 30 micrometers;" thus it is a *copper layer* that teaches or renders obvious *a thickness between 5 and 30 micrometers*. *EX1005*, [0396]; Section V.A.4 (supporting caselaw); *EX1003*, ¶169 (citing *EX1001*, 14:21-33 and opining no criticality of the claimed copper thickness).



EX1005, FIG. 72 (excerpt); *EX1003*, ¶169.

b) MTC

A POSITA would have been motivated and found it obvious to modify Sundaram's bump per Lin-191's layered bump teachings (including the thickness of copper layer 713). *EX1003*, ¶170. This combination would yield Sundaram's bump (*third metal interconnect*) having *a third metal layer over said first metal pad and a third copper layer over said third metal layer*. *EX1003*, ¶170.

A POSITA would have recognized that Lin-191's metal bump provides improved metallurgical bonding and increased resistance to fatigue and stress-induced failure by employing a layered structure. *EX1003*, ¶171. This multi-layer configuration would reduce the risk of intermetallic formation at critical interfaces, mitigate electromigration, and better absorb mechanical strain during thermal cycling. *EX1003*, ¶¶171-172. Further, the mechanical integrity and reliability of the Sundaram's bumps would be improved, particularly in applications subject to repeated temperature fluctuations and mechanical stress, e.g., where the chip package includes "high power logic component[s]." *EX1004*, 6:19-22, FIGS. 30-31; *EX1003*, ¶173. Accordingly, the Sundaram-Lin-191 combination would have advantageously improved long-term bump performance. *EX1003*, ¶173.

The combination is the application of known techniques to improve similar structures in a predictable manner, i.e., improving Sundaram's solder ball in the same way as Lin-191's bump. *EX1003*, ¶175. Alternatively, a POSITA would have

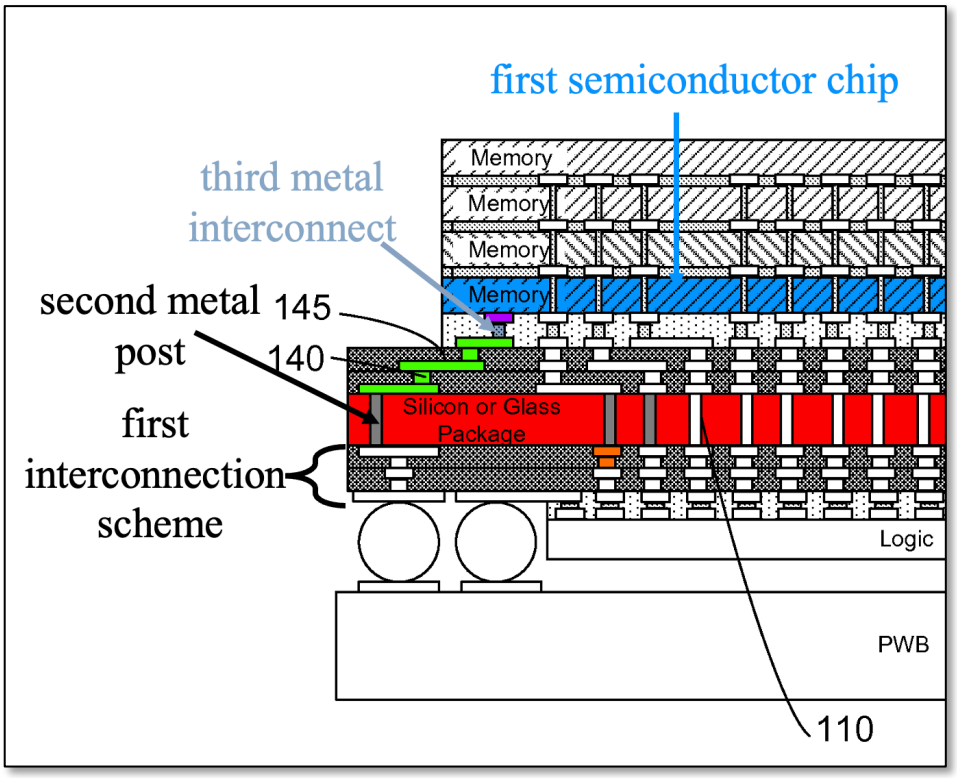
been motivated to substitute Lin-191's bump structure for Sundaram's bump to obtain the above-described advantages of Lin-191's teachings. *EX1003*, ¶175.

A POSITA would have had a REOS in either applying Lin-191's teachings to Sundaram's bump or substituting Lin-191's bump for Sundaram's similar bump, as both Lin-191 and Sundaram address semiconductor interconnect technology and because bump interconnects were well-known and fabricated using common manufacturing techniques. *EX1003*, ¶176. For example, Lin-191 teaches plating layers to form bump 714, and Sundaram likewise teaches plating techniques, further evidencing the REOS. *Compare EX1005,* [0400] *with EX1004*, 6:22-29, 10:26-29; *EX1003*, ¶176.

19. 1(e)(iv)

Sundaram's device 125 *is connected to*[4] *a second metal post through* the bump and various vias 140 and traces 145.

[4] Petitioners note *connected to* does not require a direct physical connection but is met by an electrical connection. *See, e.g., EX1001*, 2:40-42, 14:34-38, 15:57-58; *EX1003*, ¶177.



EX1004, FIG. 3 (excerpt), 7:1-9; *EX1003*, ¶177.

B. Claim 2

a) Lin-191's Teachings

Lin-191 teaches semiconductor chips as "system-on chip[s] (SOC) including **a graphics-processing-unit (GPU) circuit block**, a wireless local area network (WLAN) circuit block **and a central-processing-unit (CPU) circuit block**…" *EX1005*, [0106].

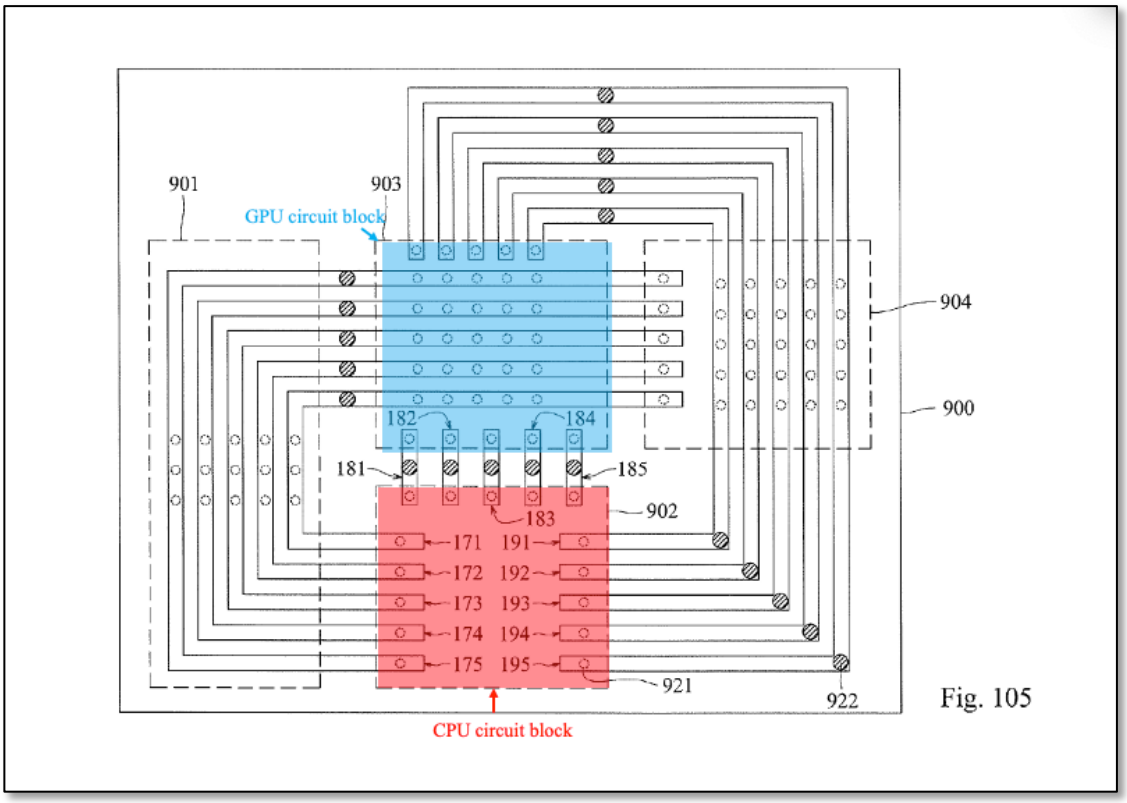


Fig. 105

EX1005, FIG. 105, [0541], [0543]; *EX1003*, ¶178.

b) MTC

A POSITA would have been motivated and found it obvious to modify Sundaram's electronic device 125 per Lin-191 to include *a CPU circuit block and a GPU circuit block*. *EX1003*, ¶179. While Sundaram's FIG. 3 depicts device 125 as stacked memory, Sundaram teaches "other electronic devices can also be used as the first electronic device 125." *EX1004*, 6:37-43; *EX1003*, ¶179. Thus, a POSITA would have been motivated and found it obvious to apply Lin-191's teachings to Sundaram. *EX1003*, ¶179. Indeed, Sundaram discloses "smart and mobile phone

applications, including video streaming, 3D graphics, camera-functions, and gaming" and contemplates "high power logic component[s]" for device 125:

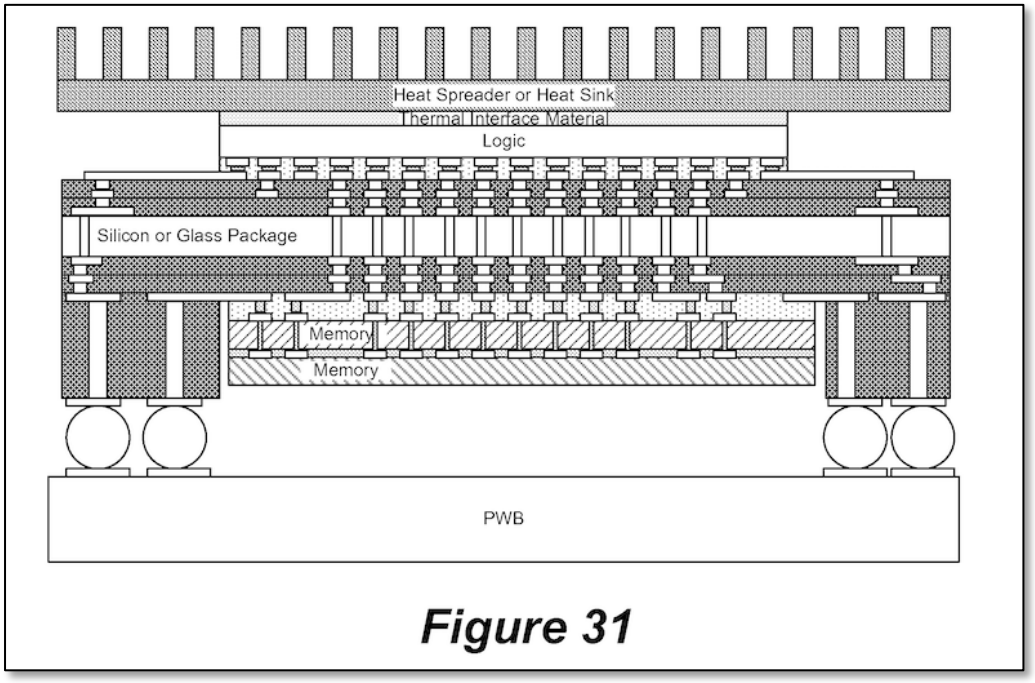


Figure 31

EX1004, 1:20-25, 6:19-22, FIG. 31. Such a combination would have predictably improved Sundaram's chip package by providing it with increased capabilities, i.e., to carry out the functions of both a CPU and a GPU. Further, the modification is an implementation detail a POSITA would have found obvious to implement given Sundaram's teachings of phone applications. *EX1003*, ¶180. Thus, a POSITA would have been motivated and found it obvious to apply Lin-191's teachings to Sundaram.

The Sundaram-Lin-191 combination is the application of a known technique (a semiconductor chip with GPU and CPU circuit blocks) to a known device (Sundaram's chip device 125) yielding the predictable results of Sundaram device

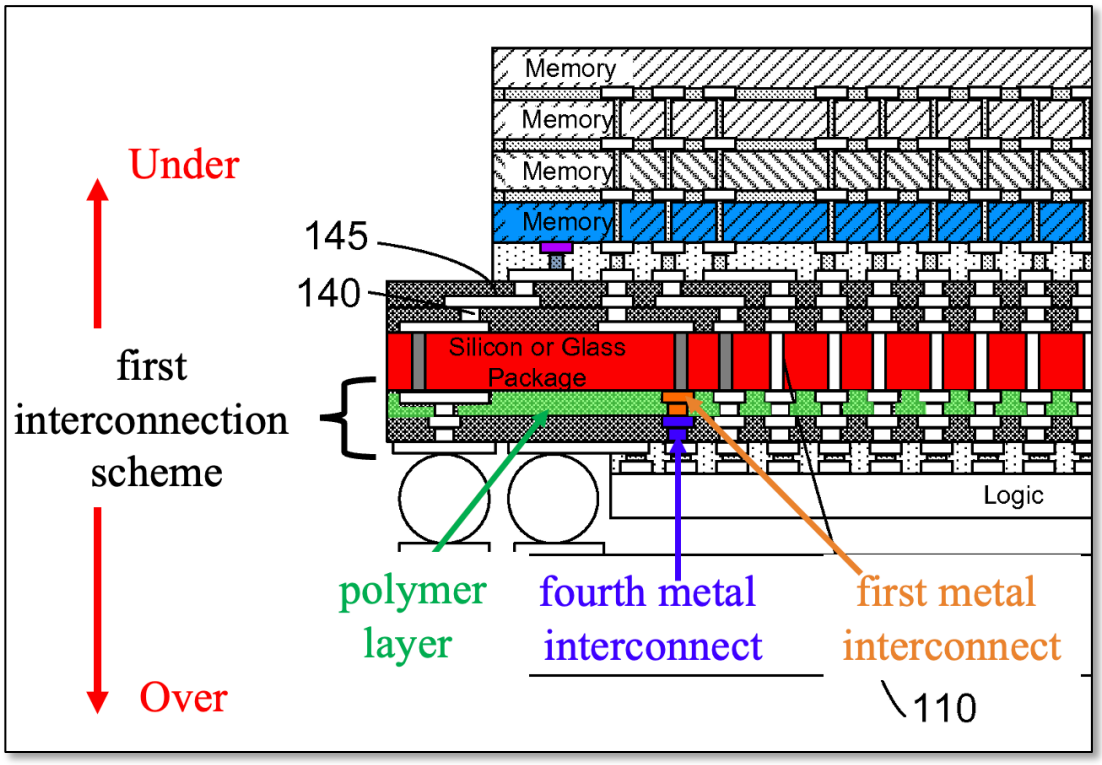
125 having both CPU and GPU circuit blocks. *EX1003*, ¶180. A POSITA would have been motivated to apply Lin-191's teachings based on the desired functionality of Sundaram's chip package. *EX1003*, ¶180.

SoCs that included CPUs and GPUs, such as taught by Lin-191, were well-known before the time of the '306 Patent, leading to a REOS. *EX1031*, 1; *EX1003*, ¶181.

C. Claim 3

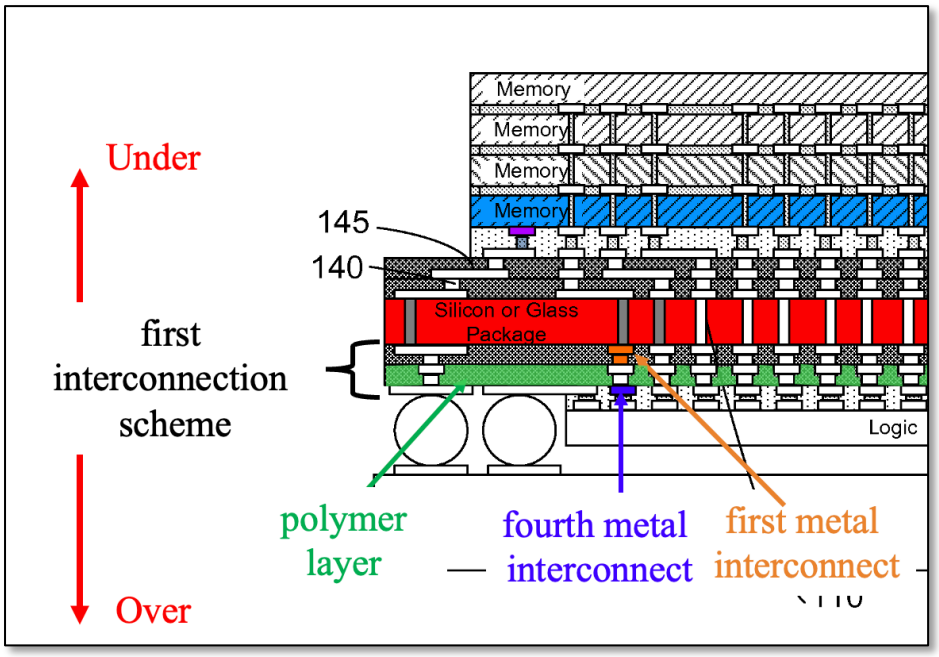
1. 3(a)

Sundaram's *first interconnection scheme* comprises a *fourth metal interconnect*, namely a blind via 140 and conductor trace 145 that are *over* the via 140 of the *first metal interconnect* (*see* Section V.A.10) and *over* the *polymer layer*, as shown below.



EX1004, FIG. 3 (excerpt); *EX1003*, ¶182.

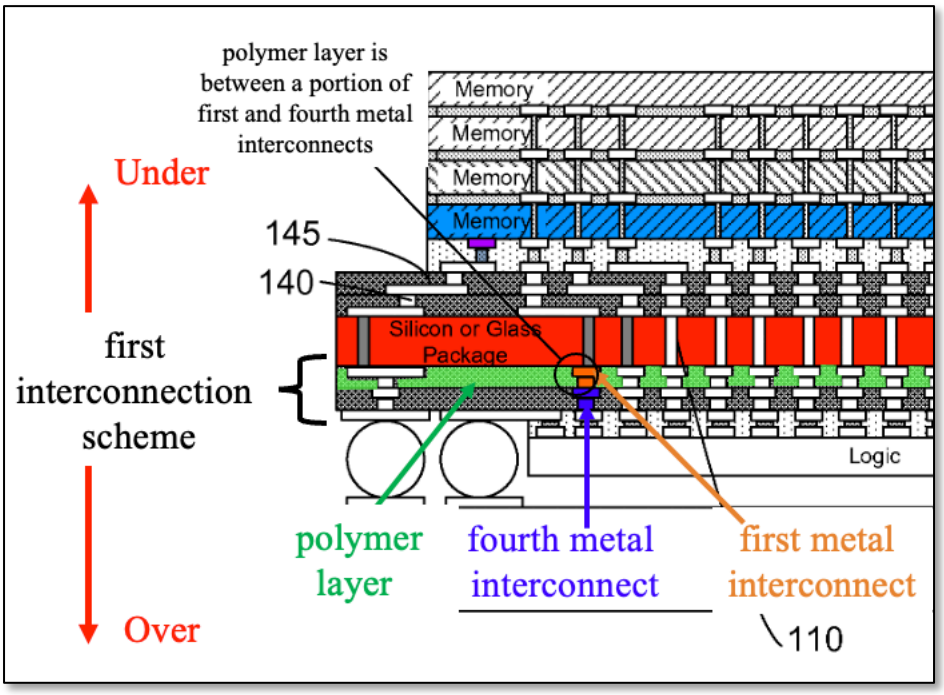
Alternatively, die pad 135 is a *fourth metal interconnect over said first metal interconnect and said polymer layer*.



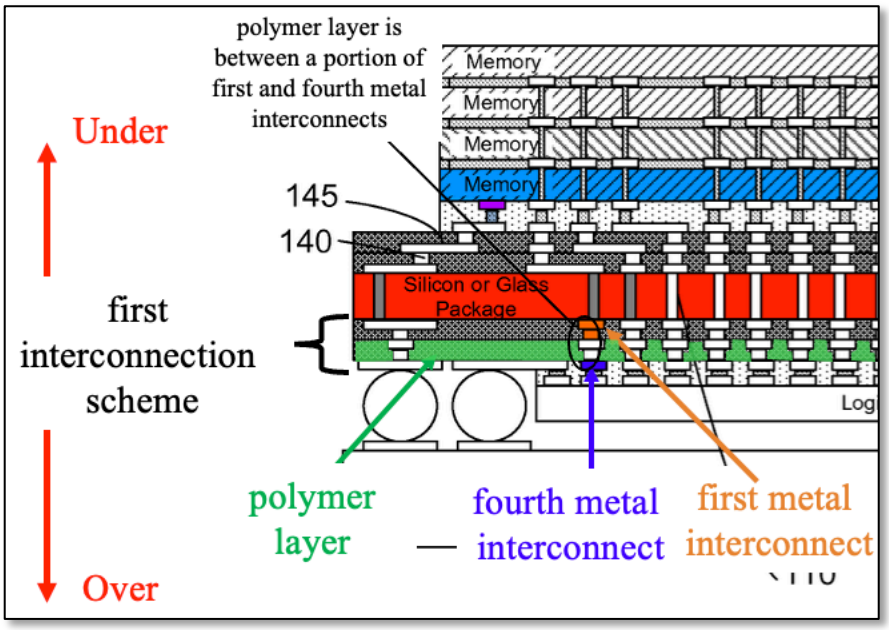
EX1004, FIG. 3; *EX1003*, ¶183.

2. 3(b)

Under either mapping of the *fourth metal interconnect* and the *polymer layer*, Sundaram's *polymer layer* is *between said first and fourth metal interconnects*, as shown:



EX1004, FIG. 3 (excerpt); *EX1003*, ¶184.



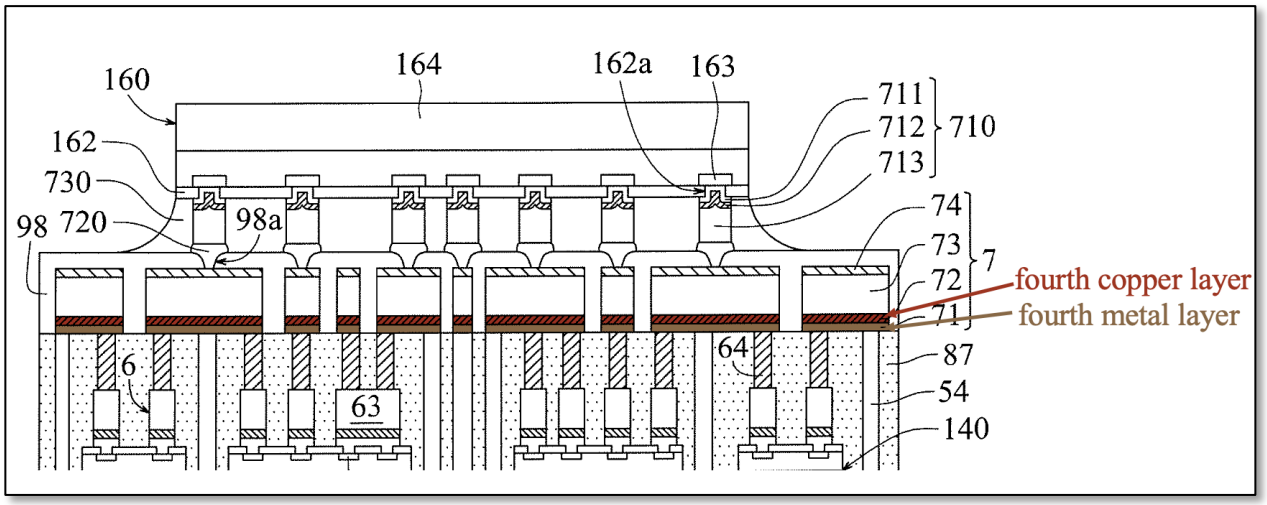
EX1004, FIG. 3 (excerpt); *EX1003*, ¶185.

3. 3(c)

See Section V.A.12. Sundaram's multilayer interconnect teachings teach Claim 3(c)'s *interconnect*, i.e., the copper seed layer is *a fourth metal layer*, and the metalized copper layer is *a fourth copper layer over said fourth metal layer*. *Id*.; EX1003, ¶186.

a) Lin-191's Teachings

Additionally, or alternatively to Sundaram, Lin-191 teaches a multilayered metal interconnect with two copper layers. Specifically, Lin-191 teaches a "patterned metal layer 7" having an "adhesion layer 71, the seed layer 72, the metal layer 73, and the barrier/wetting layer 74" *EX1005,* [0379]. Layer 7 interconnects metal pillars or bumps 64 to various other structures in Lin-191's package and, therefore, is a *metal interconnect*. *EX1005*, [0379]; *EX1003*, ¶187. Adhesion layer 71 is a *metal* (e.g., titanium or nickel) and is thus a *fourth metal layer*. *EX1005,* [0260]-[0264]. Seed layer 72 is "a copper layer" on adhesion layer 71 and is thus a *fourth copper layer over said fourth metal layer*. *EX1005*, [0261]-[0264].



EX1005, FIG. 72 (excerpt); *EX1003*, ¶187.

b) MTC

A POSITA would have been motivated and found it obvious to apply Lin-191's teachings of patterned metal layer 7 to Sundaram's via 140 and trace 145 or die pad 135 forming the *fourth metal interconnect*. *EX1003*, ¶188. Lin-191's FIG. 37 illustrates "a schematic top perspective view of the patterned metal layer 7," and, as shown, layer 7 makes lateral electrical connections (e.g., from a bump 54 to a bump 64) such that a POSITA would have understood layer 7 as being an RDL, like Sundaram's RDL.

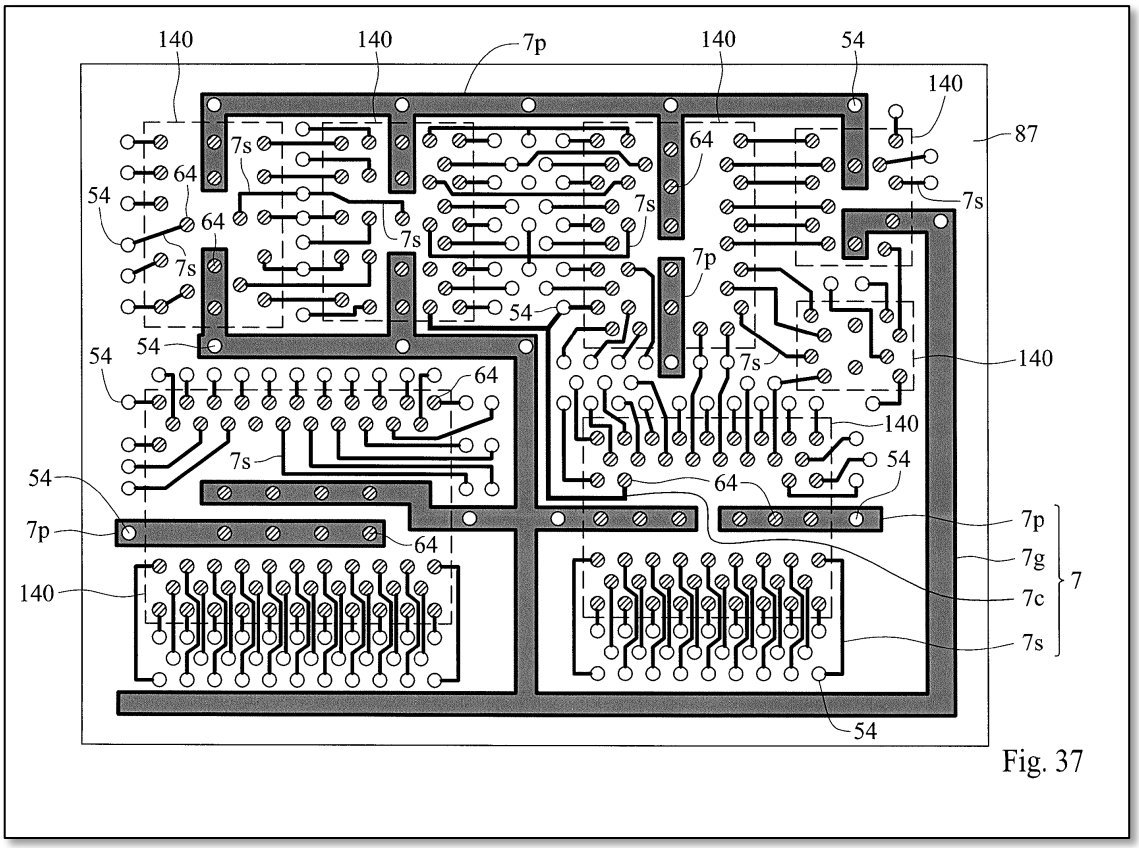


Fig. 37

EX1005, FIG. 37, [0017], [0272-0273]; *EX1003*, ¶189.

The modification would have predictably improved Sundaram's chip package by providing a low resistance current path for signals traveling between the *first metal interconnect* and *fourth metal interconnect*. *EX1003*, ¶¶190-191. Copper (i.e., layer 72) has a low resistivity, high conductivity, and high immunity to electromigration, making copper an attractive option for interconnect applications. *EX1003*, ¶¶190-191.

Additionally, the modification would have predictably improved Sundaram's chip package by reducing the risk of delamination between the copper interconnect

and the metal layers it interconnects and mitigating diffusion of copper into the metal layers it interconnects, both which may negatively impact electrical reliability and ruggedness of the chip package. *EX1003*, ¶192.

The modification is application of a known technique (Lin-191's multi-layer interconnect) to a known component (Sundaram's *fourth metal interconnect*) ready for improvement to yield the predictable result of Sundaram's *fourth metal interconnect* comprising the layers of Lin-191's layer 7. *EX1003*, ¶193. There would have been a REOS at least because methods of forming layered interconnects were well known. *EX1003*, ¶193. Further, because Lin-191's layer 7 is an RDL, and Sundaram's RDL is being modified per layer 7's teachings, there would have been a REOS. *EX1003*, ¶193.

D. Claim 4

Sundaram alone or Sundaram-Lin-191 teaches a *first metal pad*. *See* Section V.A.17. Lin-191 teaches metal pads 163 that "include **aluminum**." *EX1005*, [0384]. Metal pads are used for interconnecting chips to other components, where metal is used for the connection because it provides low resistance. *EX1003*, ¶195. Lin-191 specifically teaches a metal pad that is aluminum such that a POSITA would have found it obvious and been motivated to apply Lin-191's *aluminum pad* teachings to Sundaram's *first metal pad*. *EX1003*, ¶195. Aluminum was a well-known and widely used material for contact pads in chips, as it is compatible with established bond wire

attachment methods, low cost, and consistent with legacy materials used in semiconductor processing. *EX1003*, ¶195. It would have been a cost-effective and commonly-used choice to form Sundaram's pad, which would have had a REOS. *EX1003*, ¶195. The modification is combination of prior art elements according to known methods to yield predictable results. *EX1003*, ¶195.

E. Claim 5

See Section V.A.3. Sundaram teaches both a borosilicate glass interposer and a silicon interposer with an SiO_2 layer. *EX1004*, 9:14-16, 13:58-62, FIG. 34. Borosilicate glass includes silica (SiO_2), teaching Claim 5. *EX1003*, ¶196.

F. Claim 6

1. 6(a)

Sundaram teaches a *second semiconductor chip*: "a second electronic device 130…attached to the second side 120 of the interposer 105," which is *over said first semiconductor chip* and *comprises a second metal bump*. *EX1003*, ¶197. Sundaram alone or Sundaram-Lin-191 teaches *a second metal pad*. *See* Section V.A.17 (the *third metal interconnect* corresponds to the *second metal bump*).

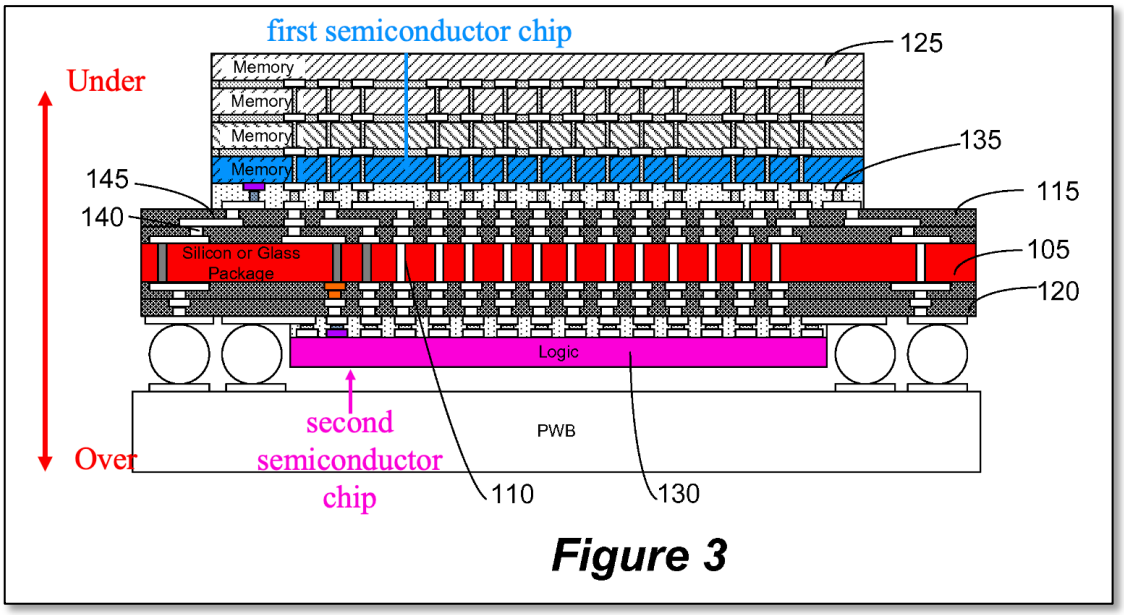
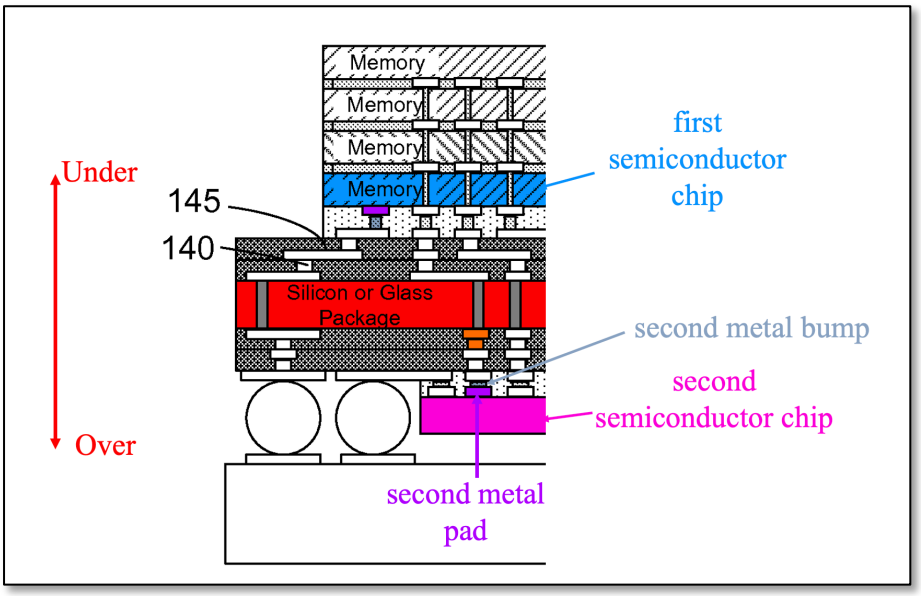


Figure 3

EX1004, FIG. 3; *EX1003*, 198.



EX1004, FIG. 3 (excerpt); *EX1003*, ¶199.

2. 6(b)

See Section V.A.14. *EX1003*, ¶200.

G. Claim 7

Sundaram teaches interposer 105 (*solid layer*) comprises *third region*[5], which is on the *opposite* side of the *first region* than the *second region* and is, therefore, *opposite to said second* region. The *third region* comprises *metal posts* in *through vias*.

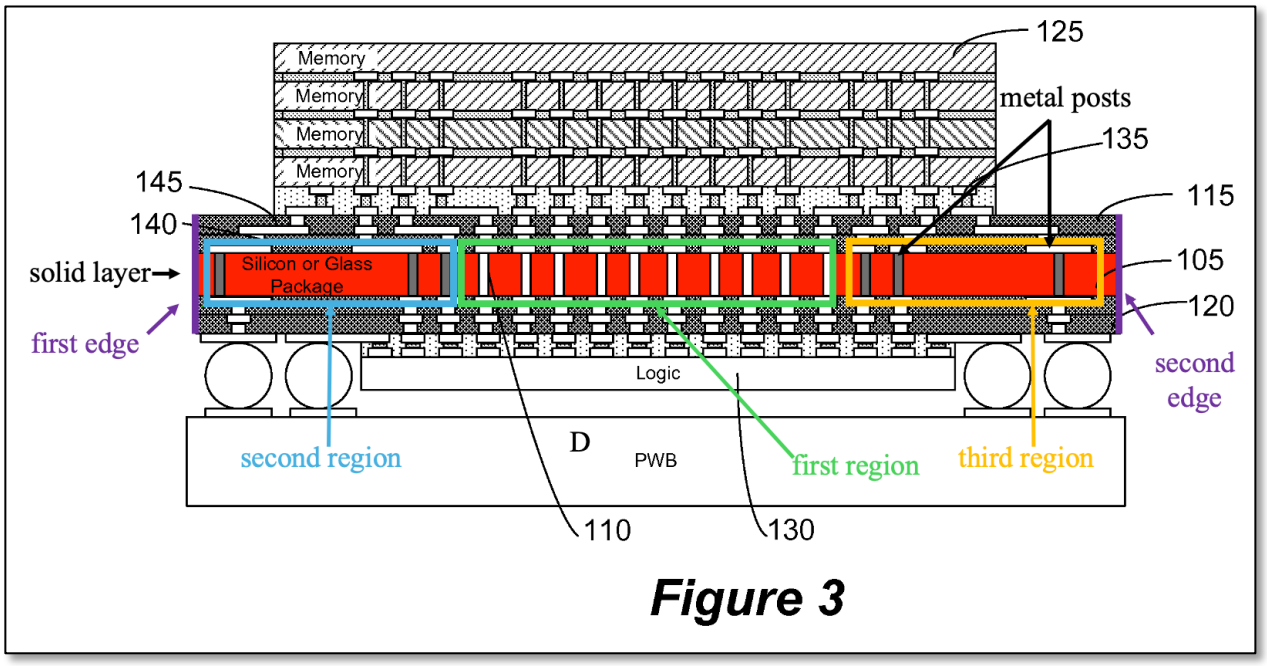


Figure 3

EX1004, FIG. 3; *EX1003*, ¶201.

[5] The *third region* is not described in the '306 Patent's specification but was introduced by Applicant during original prosecution of the related '763 Patent. *EX1117*, 351-360. Applicant relied solely on FIG. 6l to support the *third region*.

H. Claim 9

Another memory device 125 is *another said first semiconductor chip under said second surface*.

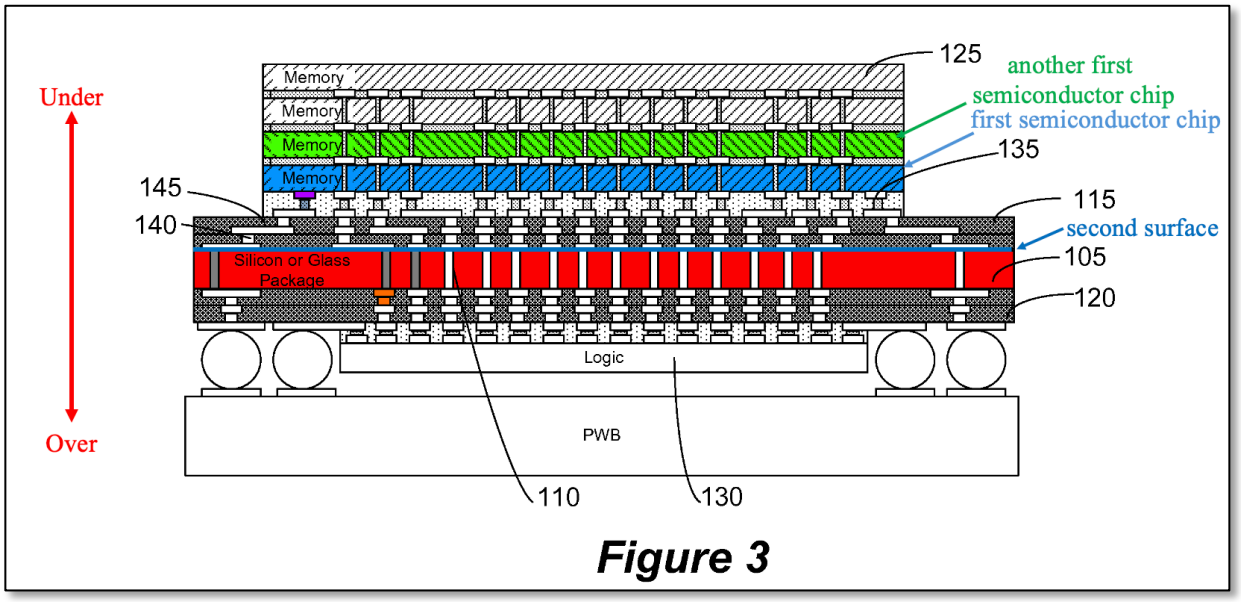


Figure 3

EX1004, FIG. 3; *EX1003*, ¶202.

I. Claim 10

1. 10(Pre)

See Section V.A.1.

2. 10(a)

See Section V.A.2.

3. 10(a)(i)

See Section V.A.3.

4. 10(a)(ii)

Sundaram teaches or renders obvious the claimed thickness. Sundaram's interposer 105 (*solid layer*) is "about 20 to about 200 micrometers in thickness" overlapping with the claimed *thickness* range. *EX1004*, 2:22-25, 14:34-36; *EX1003*, ¶¶206, 208 (citing *EX1001*, 7:58-64 and opining no criticality of the claimed *thickness*); Section V.A.4 (supporting caselaw).

Sundaram also teaches an embodiment where a glass interposer has a thickness of 175 micrometers, which is a specific point within the claimed range of *between 100 and 300 micrometers*, further teaching the claimed range. *EX1003*, ¶207; *UCB*, 65 F.4th at 687 ("If the prior art discloses a point within the claimed range, the prior art anticipates the claim"); MPEP 2131.03(I).

5. 10)(a)(iii)

See Section V.A.5.

6. 10(b)

See Section V.A.6. Sundaram's through vias 110 are metalized with "copper" and thus are *copper posts*. *EX1004*, 6:25-27, 13:30-41; *EX1003*, ¶210.

7. 10(b)(i)

See Section V.A.8.

8. 10(c)

See Section V.A.9.

9. 10(c)(i)

See Section V.A.10.

10. 10(c)(ii)

See Section V.A.11, reciting corresponding limitations. *EX1003*, ¶214.

11. 10(c)(iii)

See Section V.A.12, reciting corresponding limitations. *EX1003*, ¶215.

12. 10(d)

See Section V.A.13.

13. 10(d)(i)

See Section V.A.14.

14. 10(e)

Sundaram's package includes *a second metal bump over said first interconnection scheme.*

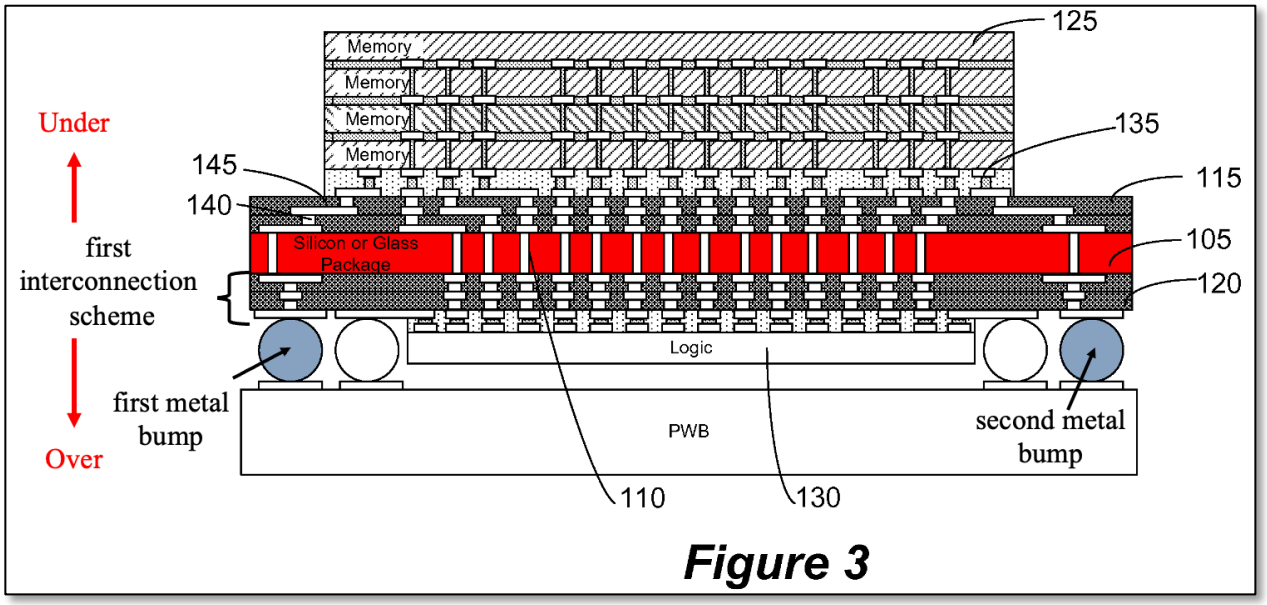


Figure 3

EX1004, FIG. 10B; *EX1003*, ¶218.

15. 10(f)

Electronic device 130 is *a first semiconductor chip over said first interconnection scheme and between said first and second metal bumps*.

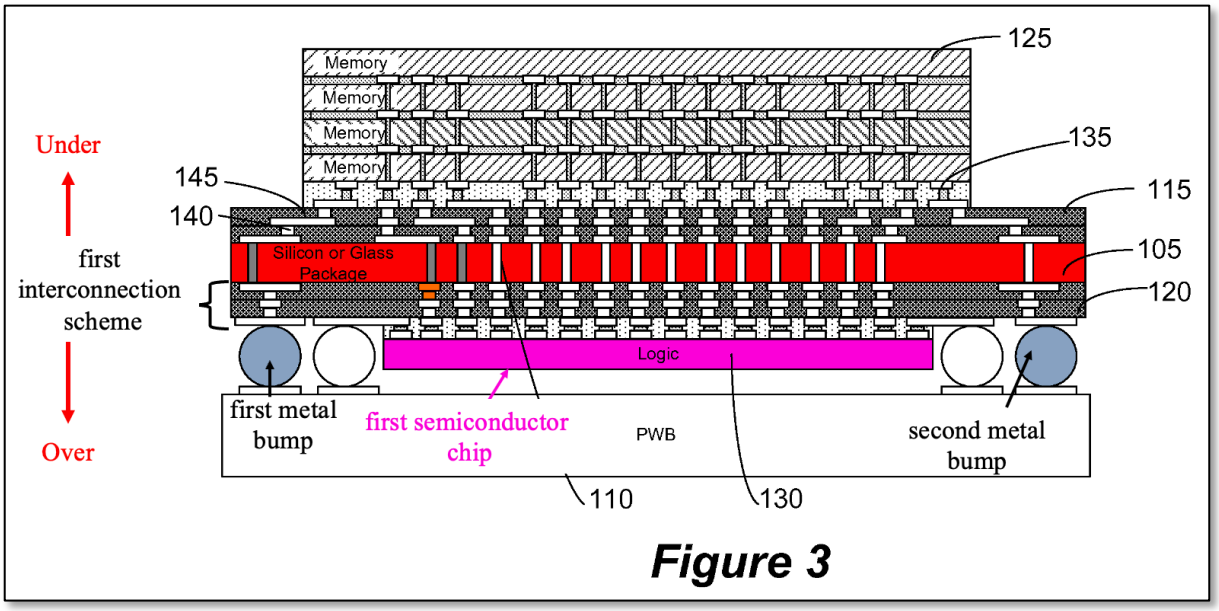
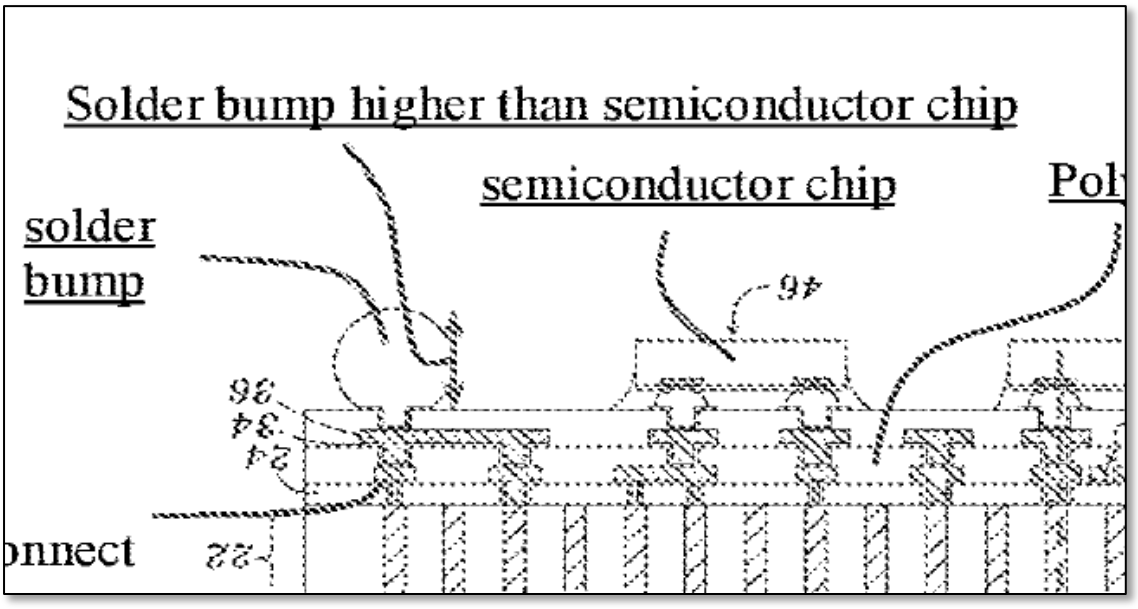


Figure 3

EX1004, FIG. 3; *EX1003*, ¶219.

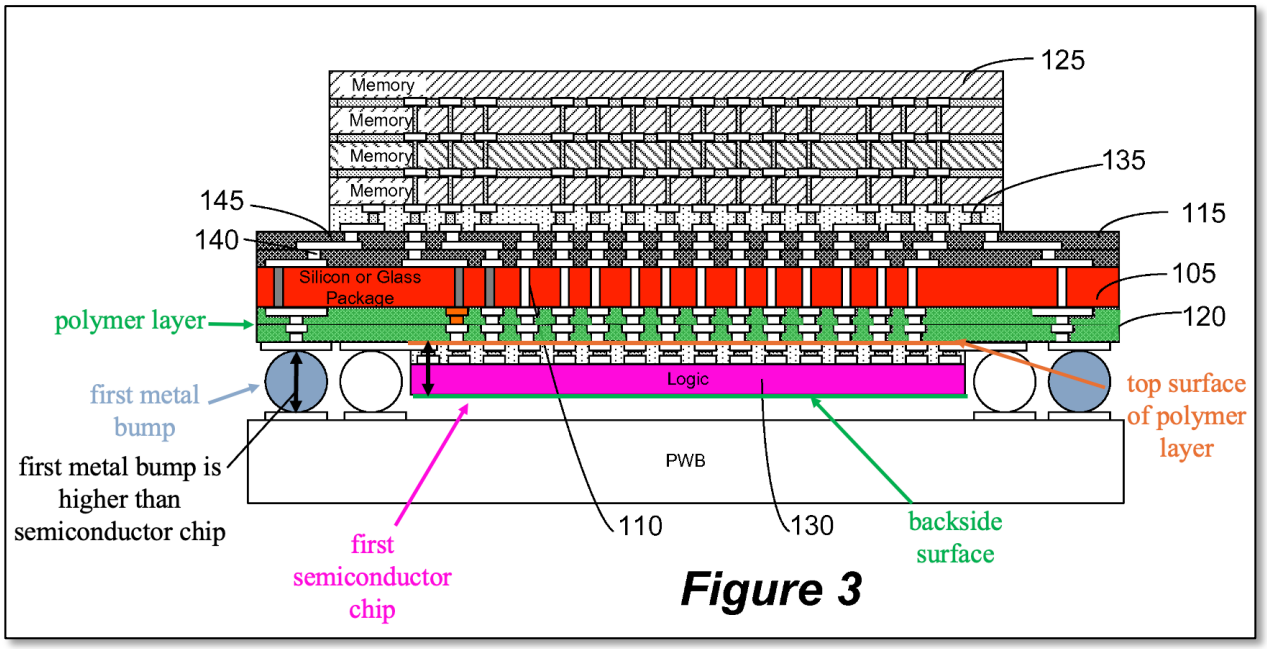
16. 10(f)(i)

During original prosecution of the related '768 Patent, PO filed an Amendment with an annotated figure illustrating specification support for claim language similar to 10(f)(i):



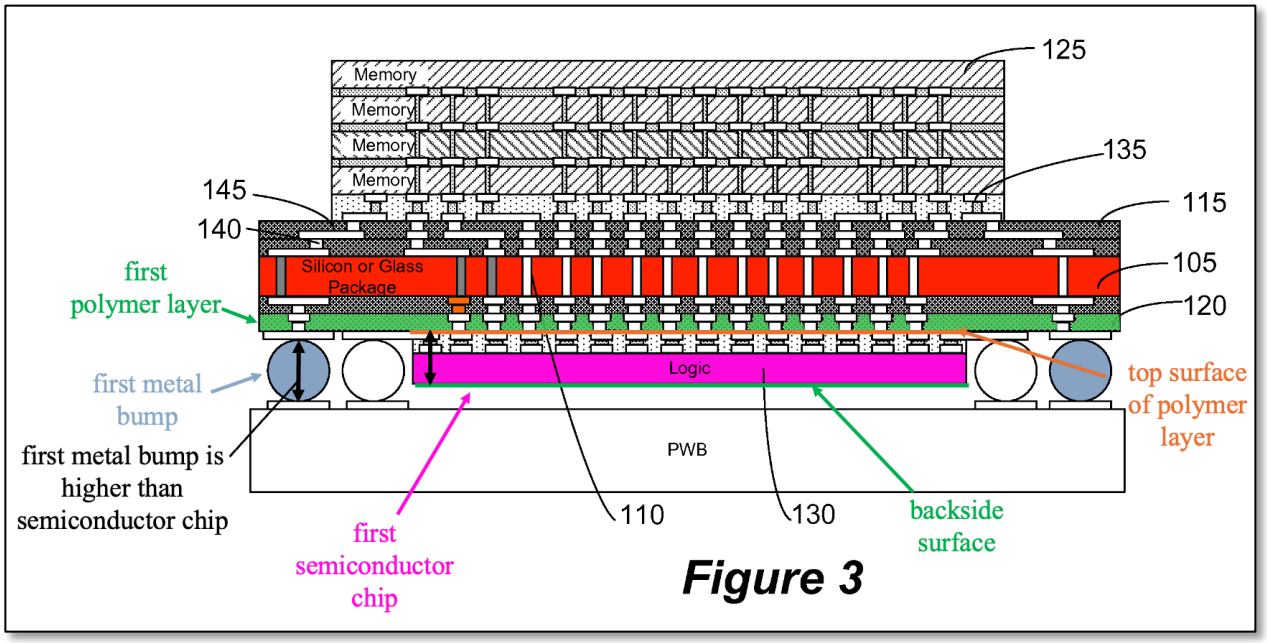
EX1032, 400; *EX1003*, ¶220; *see* cited caselaw in Section V.A.8.

Sundaram's *polymer layer* includes at least the portion described above at Claims 10(c)(i), 1(c)(i) and further includes the portion highlighted below. *See* Sections V.I.9, V.A.10; *EX1003*, ¶221. Also shown below, Sundaram's device 130 (*first semiconductor chip*) *has a height [that] is between a backside surface of* device 130 *and a top surface of said polymer layer*, which is *smaller than a thickness* of Sundaram's copper bump (*first metal bump*). *See* cited caselaw in Section V.A.8.



EX1004, FIG. 3; *EX1003*, ¶221.

Alternatively, Sundaram's *polymer layer* is as annotated below, which also meets the claim limitation.



EX1004, FIG. 3; *EX1003*, ¶222; *see* cited caselaw in Section V.A.8.

17. 10(f)(ii)

See Section V.F, reciting corresponding limitations. *EX1003*, ¶223.

18. 10(g)

Sundaram teaches "third and fourth electronic devices can be stacked on the first 125 and second 130 electronic devices"; thus, the fourth electronic device stacked on the second device 130 is *a second semiconductor chip over said first interconnection scheme*. *EX1004*, 7:16-18.

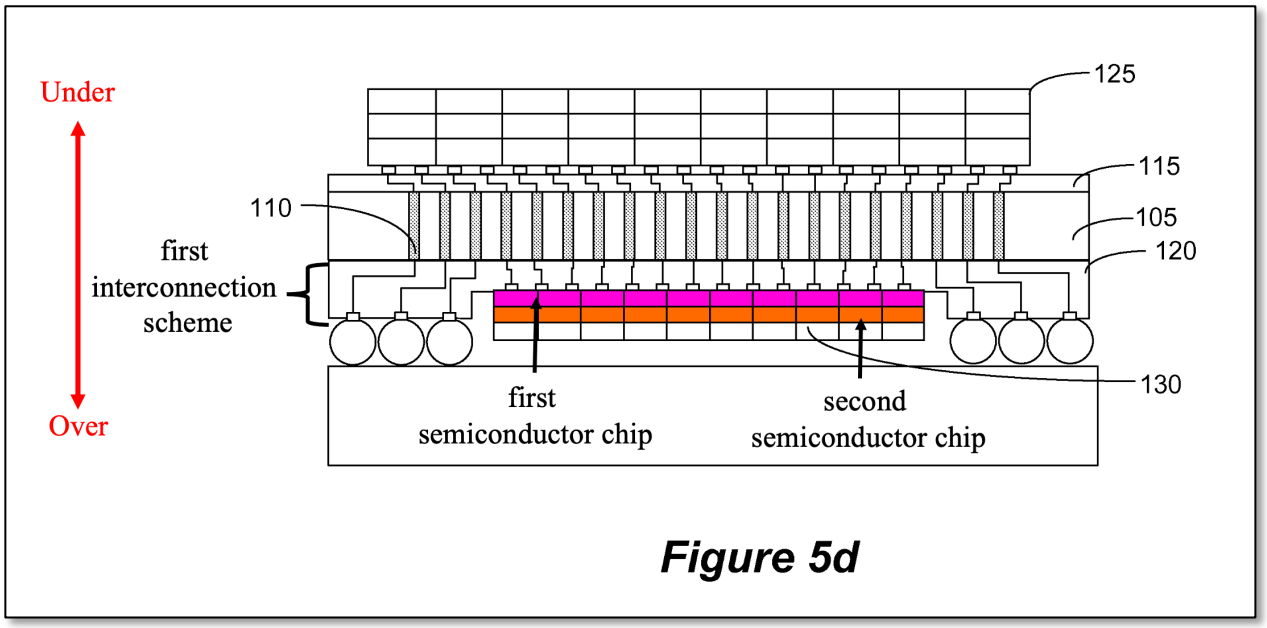


Figure 5d

EX1004, FIG. 5d; *EX1003*, ¶224.

19. 10(g)(i)

See Sections V.F, V.I.17, mapping a *fourth metal bump* as claimed. It would have been obvious for a *second semiconductor chip of* the stacked electronic devices taught by Sundaram (see 10(g)) to include *a fourth metal bump* and *second metal*

pad already taught by Sundaram. This modification would have advantageously provided Sundaram with an interconnection between the *first* and *second semiconductor chips* when stacked or would have enabled connecting the *second semiconductor chip* to the RDL in the same manner as Sundaram's logic chip, i.e., in a side-by-side arrangement. *EX1003*, ¶¶225-227.

J. Claim 11

See Section V.E.

K. Claim 13

1. 13(a)

See Sections V.A.15, V.I, reciting corresponding limitations. *EX1003*, ¶229.

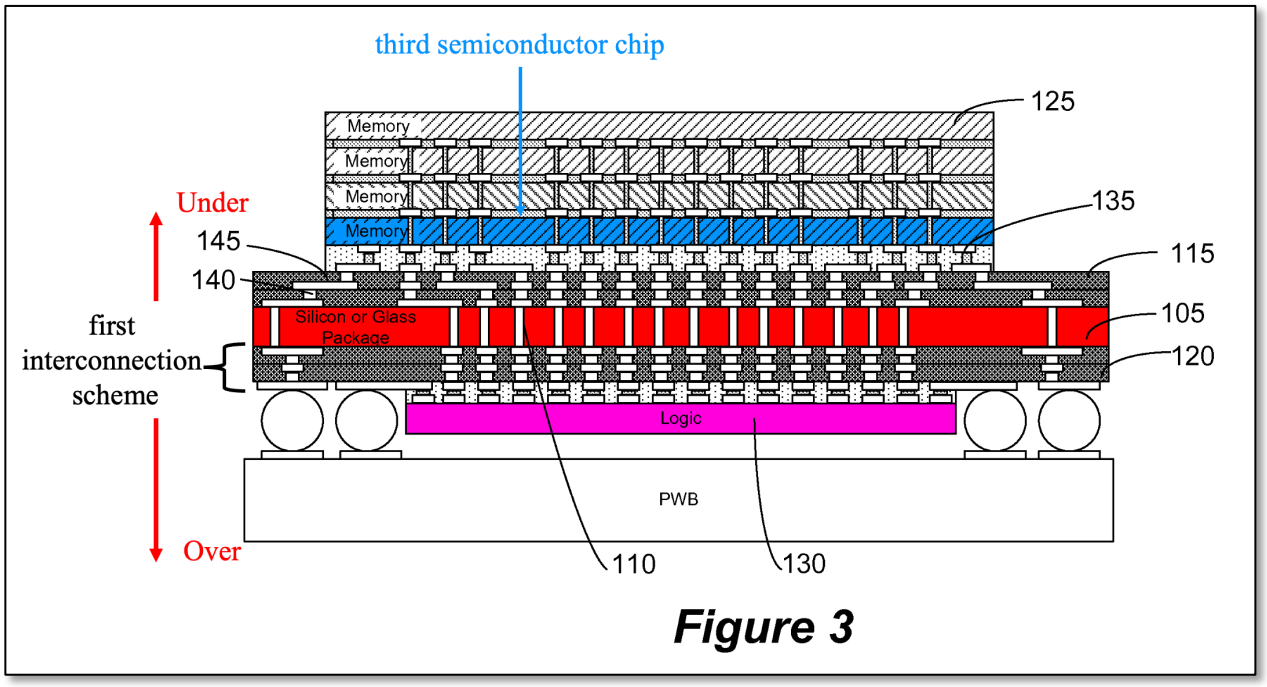


Figure 3

EX1004, FIG. 3.

2. 13(b)

See Section V.A.17, reciting corresponding limitations. *EX1003*, ¶230.

3. 13(c)

See Section V.A.18, reciting corresponding limitations. *EX1003*, ¶¶231, 169 (citing *EX1001*, 14:21-33 and opining no criticality of the claimed copper thickness). Claim 13(c)'s *second metal layer* and *second copper layer* correspond to Claim 1(e)(iii)'s *third metal layer* and *third copper layer*, respectively.

L. Claim 14

1. 14(a)

See Sections V.K.1, V.A.15.

2. 14(b)

See Sections V.K.2, V.A.17.

3. 14(c)

See Sections V.K.3, V.A.18.

4. 14(d)

See Section V.B.

M. Claim 15

See Sections V.I, V.G.

N. Claim 17

1. 17(a)

Sundaram teaches *a third semiconductor chip*. *See* Sections V.K.1, V.A.15.

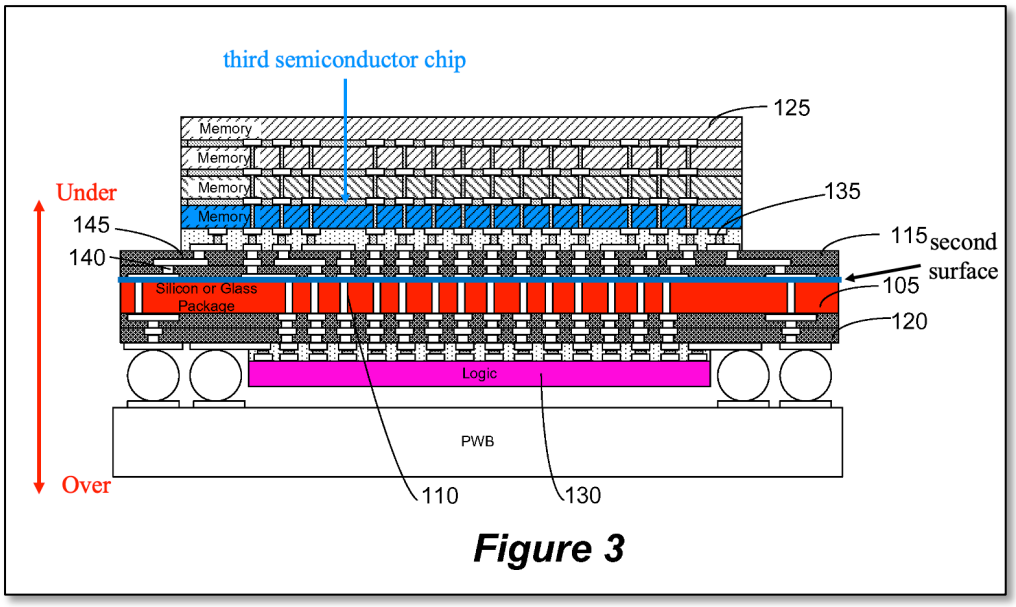


Figure 3

EX1004, FIG. 3; *EX1003*, ¶237.

Sundaram discloses "wire-bonded SIP [system-in-package]" structures with memory chips including a *metal wire* for bonding. *EX1004*, 1:33-50. Sundaram illustrates the *metal wire is connected to a third pad*.

Lin-191 also teaches *metal pads* in addition to Sundaram's teachings, and a POSITA would have been motivated, found it obvious, and had a REOS in modifying Sundaram per Lin-191's *metal pad* teachings. *See* Section V.A.17.

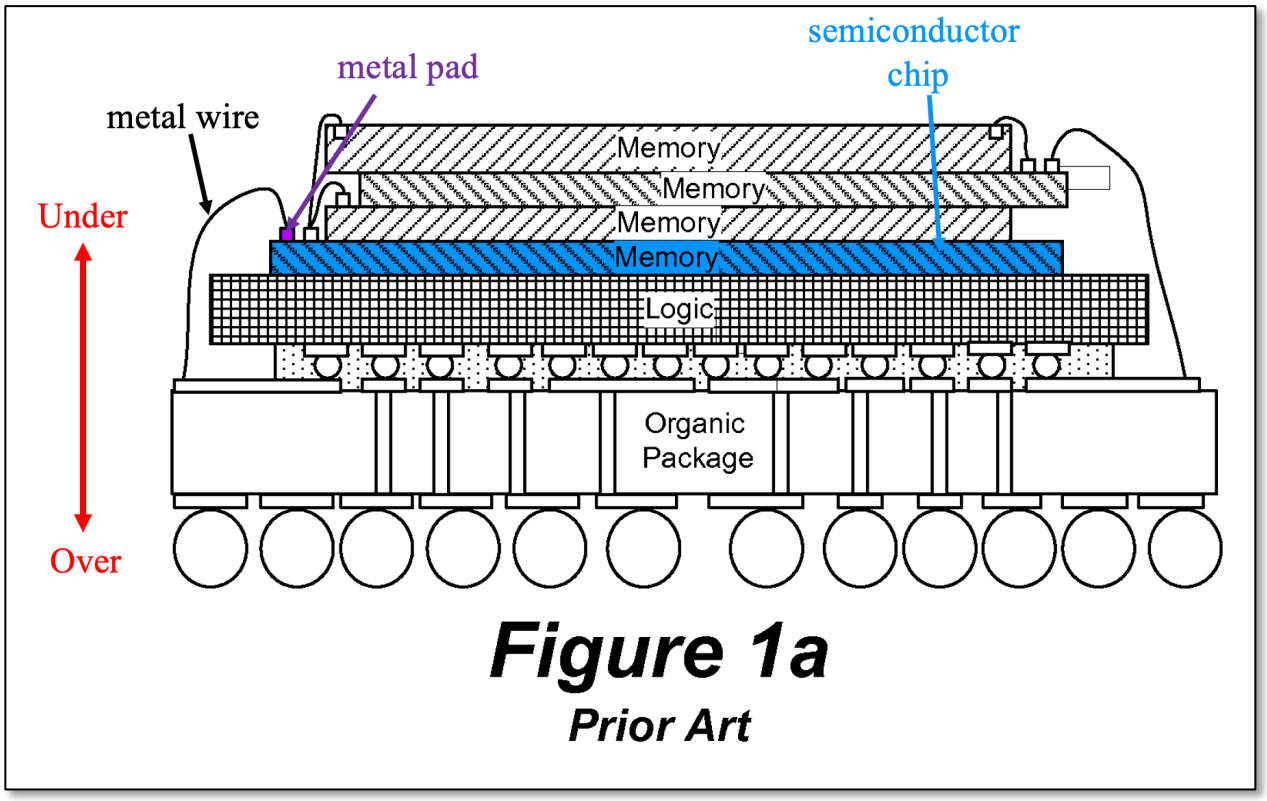


Figure 1a
Prior Art

EX1004, FIG. 1a; *EX1003*, ¶238.

a) MTC Sundaram's Internal Embodiments

A POSITA would have been motivated, found it obvious, and had a REOS in modifying Sundaram's FIG. 3 embodiment based on the FIG. 1a embodiment to wire bond Sundaram's *third semiconductor chip*. *EX1003*, ¶239. While Sundaram describes wire-bonded SIP structures as being limited in providing high bandwidth, a POSITA would have appreciated the benefits of the tradeoff of modifying Sundaram to wire bond (cost, reliability, etc.), e.g., for when high bandwidth is not required, which is envisioned by Sundaram. *EX1004*, 6:53-57; *EX1003*, ¶¶239-241.

Because wire-bonding was a universal method of connecting chips to other components, there would have been a REOS. *EX1003*, ¶¶239-241.

2. 17(b)

Sundaram teaches memory chips, and Lin-191 specifically teaches a "dynamic-random-access-memory (DRAM) chip." *EX1004*, 6:34-39; *EX1005*, [0106]. A POSITA would have found it obvious that Sundaram's memory chip can be a DRAM chip because DRAM chip is one kind of memory chips, e.g., when interconnect structure 100 is used in a cell phone. *EX1003*, ¶242. DRAM placement close to logic/CPU/GPU is critical because of strict skew and signal integrity requirements with the high-speed bus connections between the two chips. There would have been a REOS because DRAM chips were ubiquitous. *EX1003*, ¶¶242-243.

O. Claim 18

1. 18(Pre)

See Section V.A.1.

2. 18(a)

See Section V.A.2. Claim 18's mapping reverses Sundaram's mapped *first* and *second surfaces* and *over/under* directions relative to Claims 1 and 10's mapping.

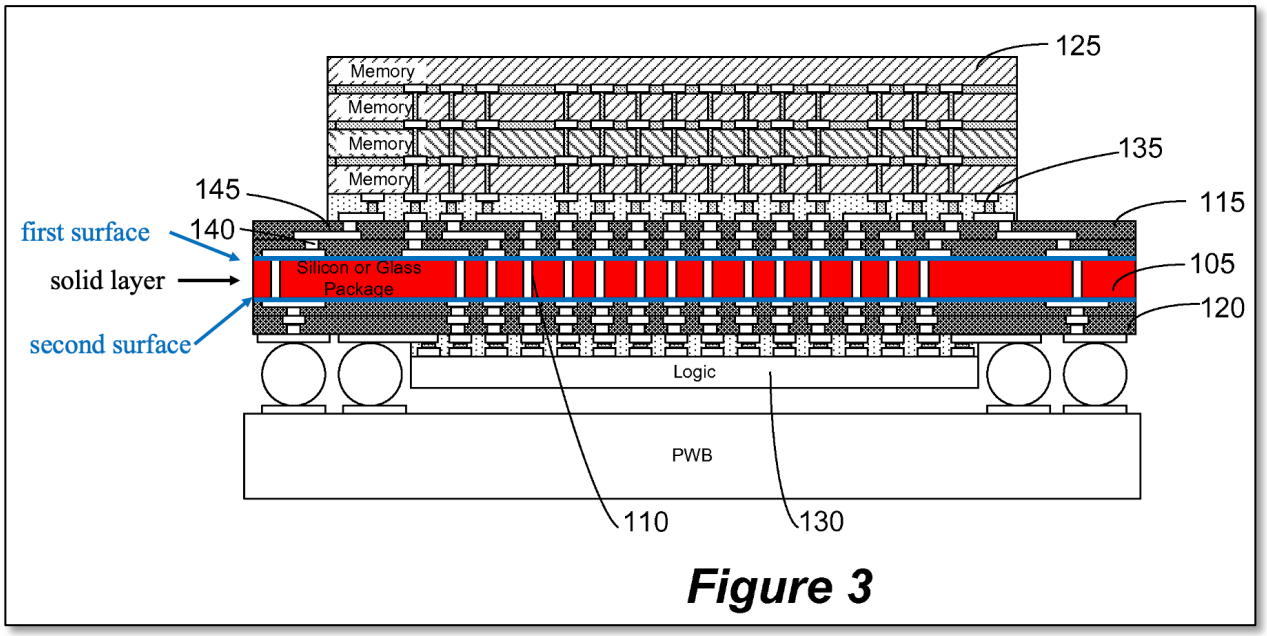


Figure 3

EX1004, FIG. 3; *EX1003*, ¶245.

3. 18(a)(i)

See Section V.A.3.

4. 18(a)(ii)

See Section V.A.4.

5. 18(a)(iii)

See Section V.A.5.

6. 18(b)

See Sections V.A.6, V.I.6.

7. 18(c)

See Section V.A.9. Sundaram's RDL "deposited on the first side 115" is *a first interconnection scheme over said first surface.*

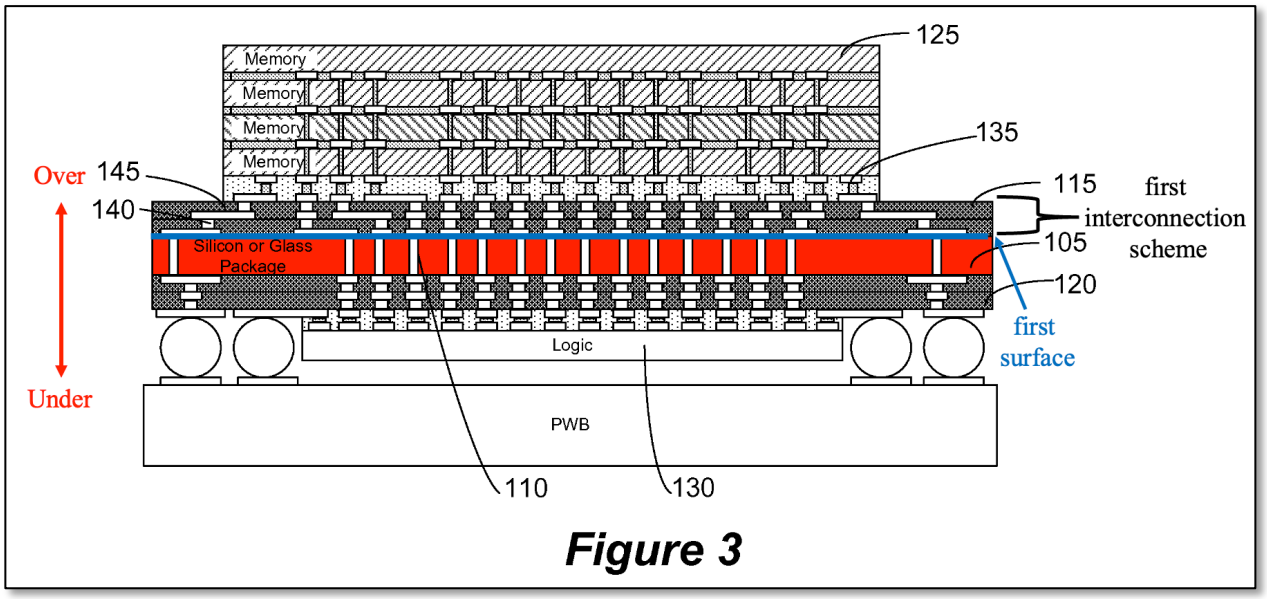


Figure 3

EX1004, FIG. 3; *EX1003*, ¶250.

8. 18(c)(i)

See Section V.A.10. *First and second metal interconnects* and a *first polymer layer* (green) *over* the *interconnects* are shown below:

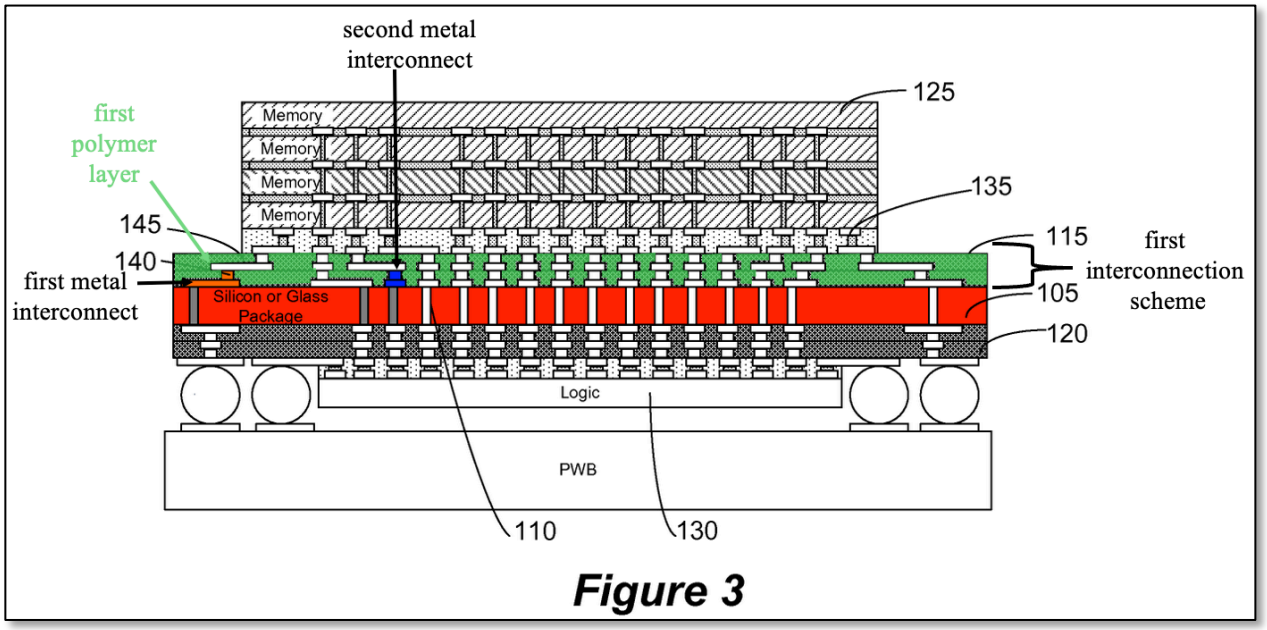
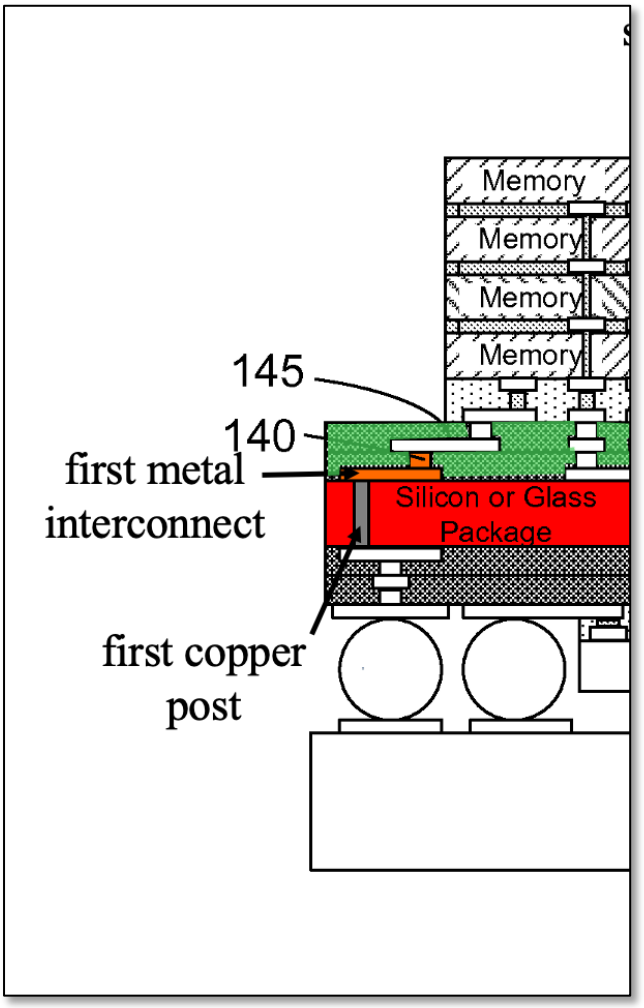


Figure 3

EX1004, FIG. 3; *EX1003*, ¶251.

9. 18(c)(ii)

See Section V.A.11.



EX1004, FIG. 3 (excerpt); *EX1003*, ¶252.

10. 18(c)(iii)

See Section V.A.12, reciting corresponding limitations. *EX1003*, ¶253.

11. 18(d)

A first chip in Sundaram's stack is *a first semiconductor chip over said first interconnection scheme*:

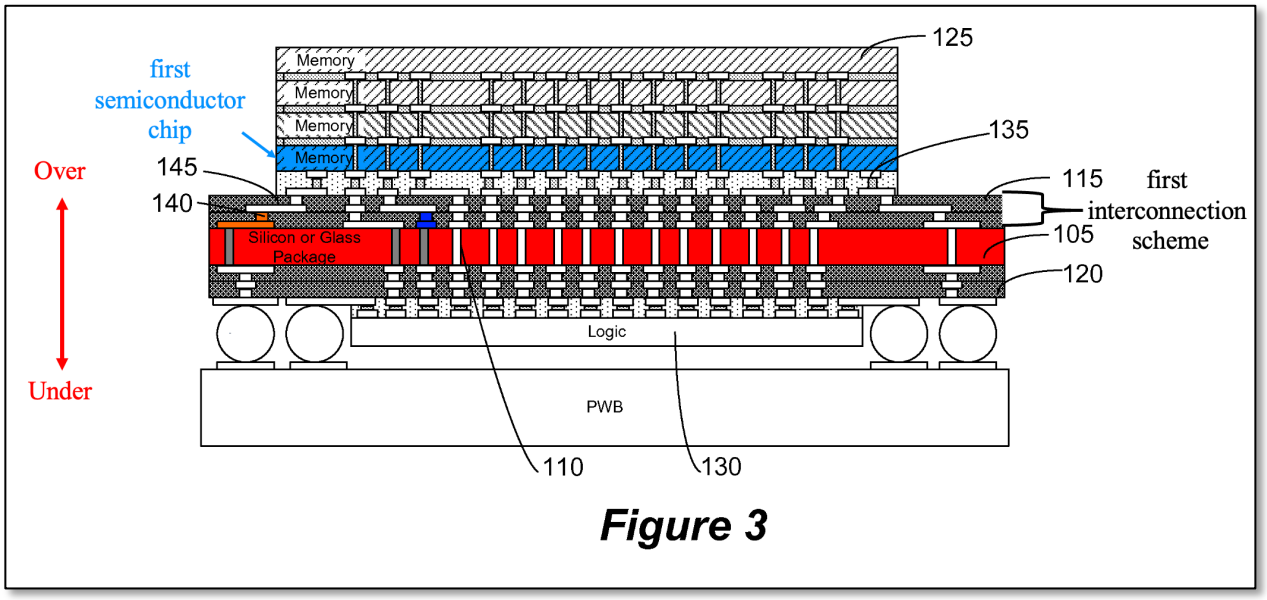
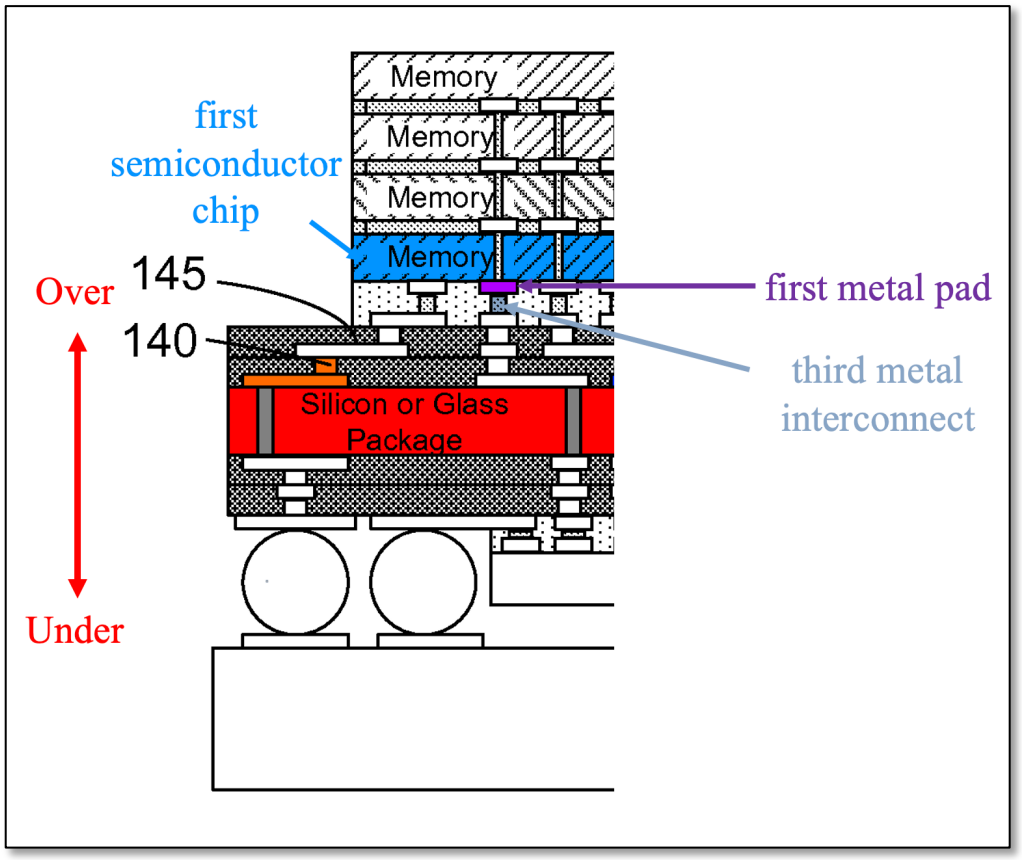


Figure 3

EX1004, FIG. 4, 6:37-39; *EX1003*, ¶254.

12. 18(d)(i)

See Section V.A.17.



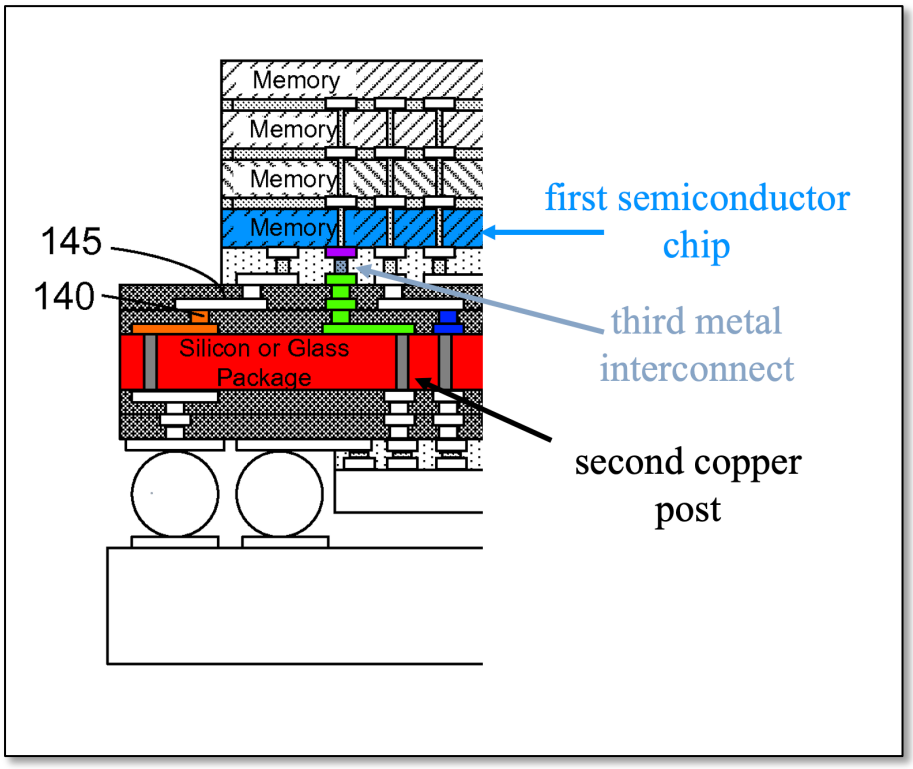
EX1004, FIG. 3 (excerpt); *EX1003*, ¶255.

13. 18(d)(ii)

See Section V.A.18, reciting corresponding limitations. *EX1003*, ¶256.

14. 18(d)(iii)

See Section V.A.19. The *first semiconductor chip is coupled to a second copper post…though said third metal interconnect* and through the interconnects.



EX1004, FIG. 3; *EX1003*, ¶257.

15. 18(e)

A second chip in the stack is *a second semiconductor chip over said first interconnection scheme*.

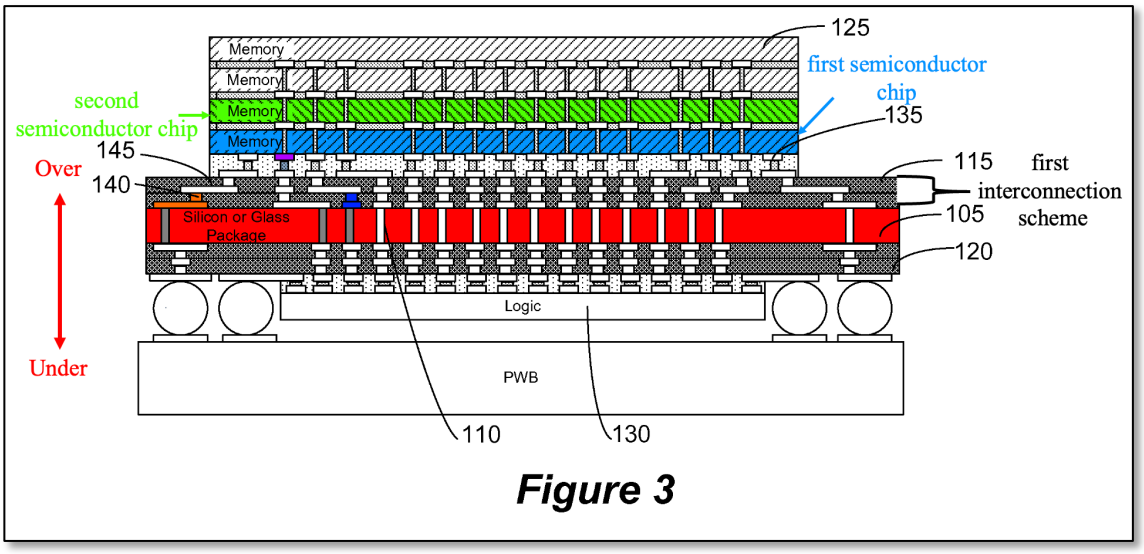
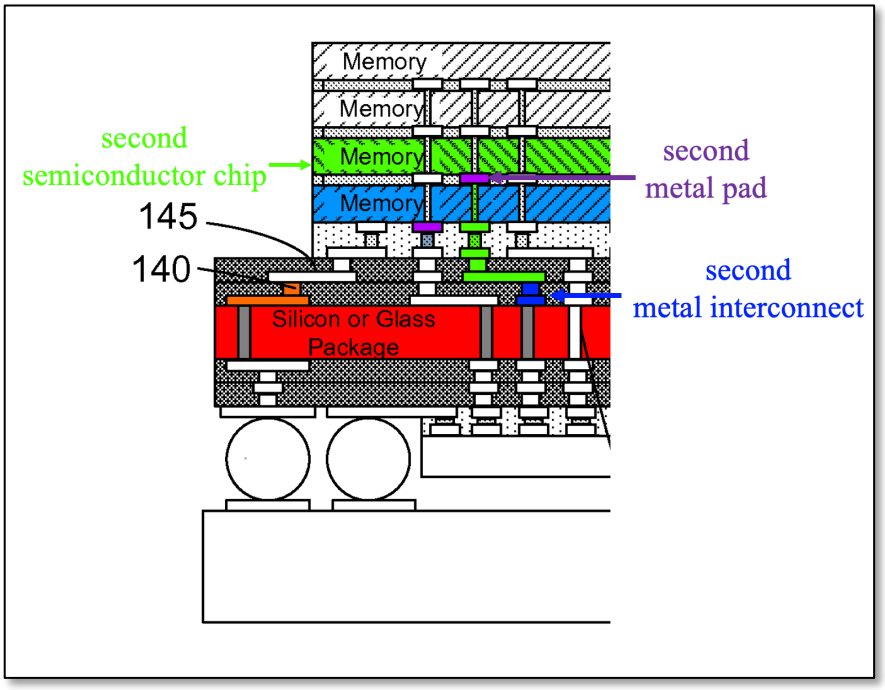


Figure 3

EX1004, FIG. 3; *EX1003*, ¶258.

16. 18(e)(i)

FIG. 3 depicts Sundaram's *second semiconductor chip compris[ing] a second metal pad coupled to said second metal interconnect* through the highlighted interconnects.



EX1004, FIG. 3 (excerpt); *EX1003*, ¶259.

Additionally or alternatively, FIG. 32 teaches a *second metal pad*. FIG. 32 depicts a chip stack similar to FIG. 3's where each chip has a distinct metal pad. A POSITA would have found it obvious, been motivated, and had a REOS in modifying FIG. 3's chip stack per FIG. 32's to provide each chip with its own set of pads, so that each chip has top and bottom pads connected to one another as each chip must include pads on its surface to provide connection to other electrical components in the chip package. *EX1003*, ¶260. The modification is a straightforward implementation detail to FIG. 3's chip stack.

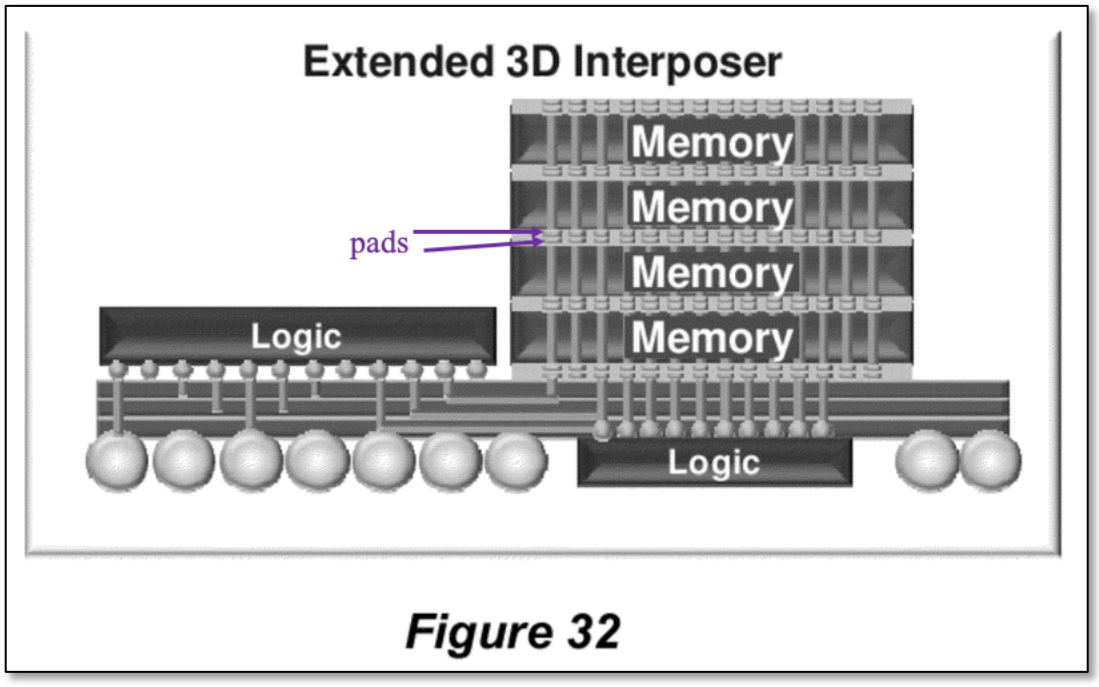


Figure 32

EX1004, FIG. 32; *EX1003*, ¶260.

17. 18(f)

Sundaram teaches *third semiconductor chip under said first interconnection scheme*, as shown below.

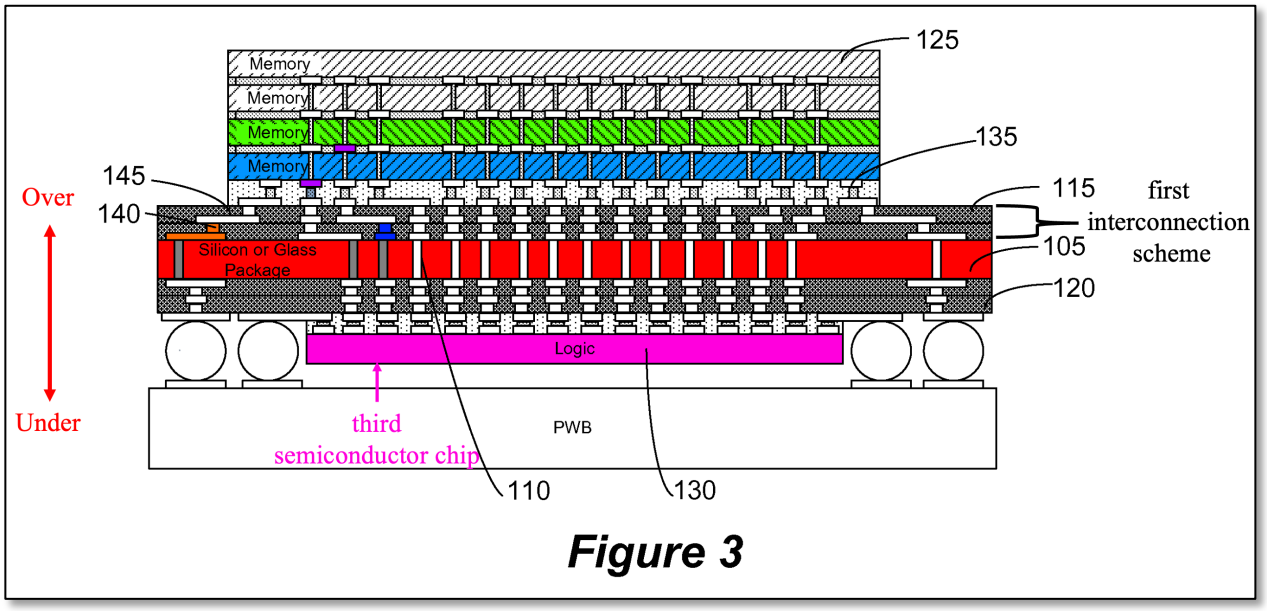


Figure 3

EX1004, FIG. 3; *EX1003*, ¶261.

18. 18(g)

Sundaram's copper bumps (*metal bumps*) are *under said second surface*. Sundaram alone or Sundaram-Lin-191 teaches *a tin-containing layer*. *See* Section V.A.14.

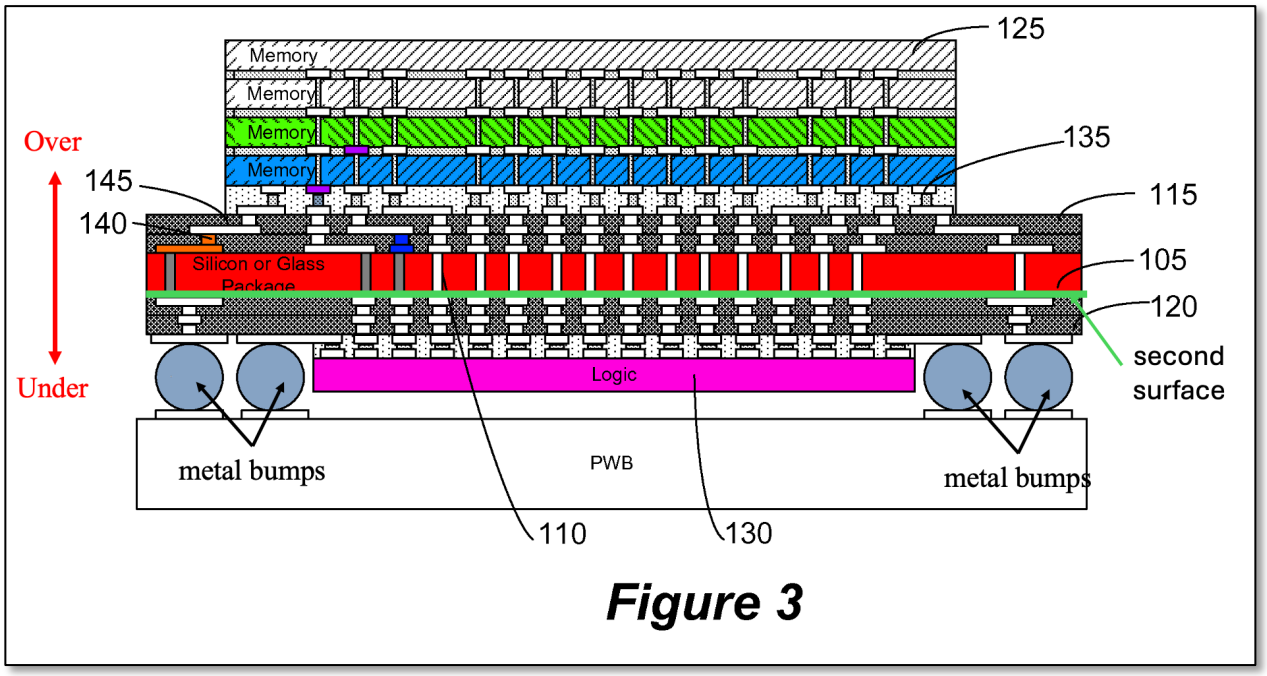


Figure 3

EX1004, FIG. 3; *EX1003*, ¶¶262-263.

P. Claim 19

See Section V.E.

Q. Claim 20

See Section V.G.

R. Claim 21

1. 21(a)

Sundaram's chip stack includes a third chip, i.e., *a fourth semiconductor chip over said first semiconductor chip*.

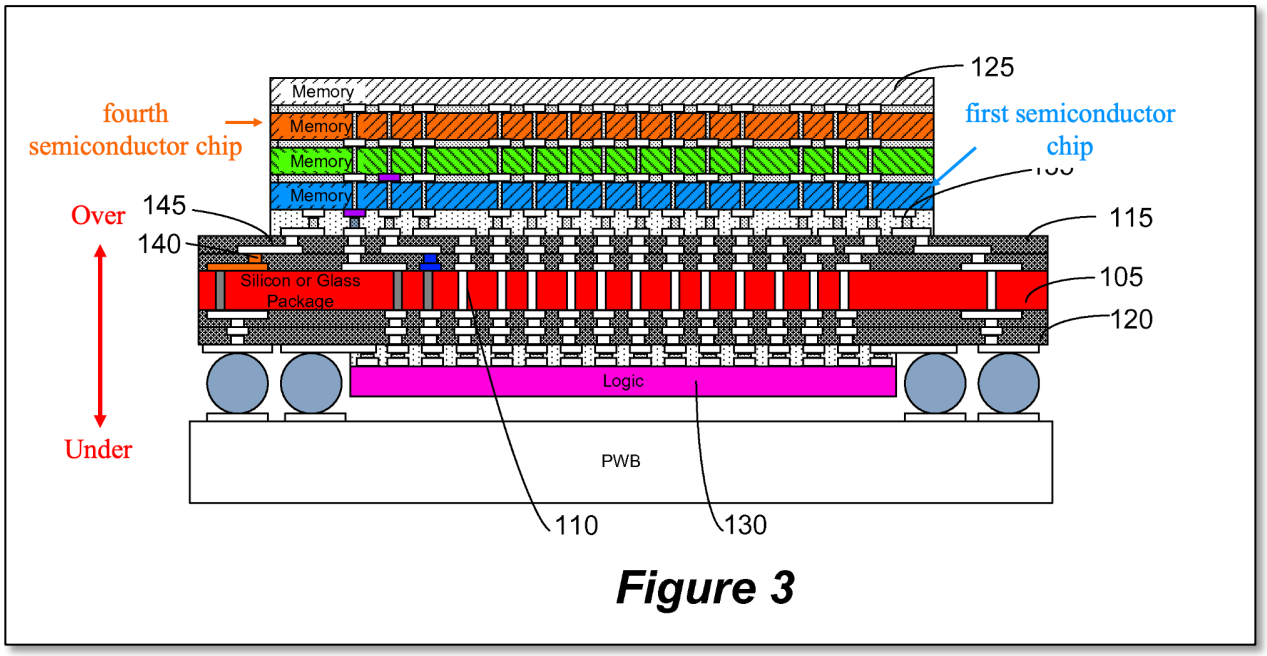


Figure 3

EX1004, FIG. 3; *EX1003*, ¶266.

2. 21(b)

Sundaram illustrates a *third pad at a bottom surface* of the fourth chip. Sundaram alone or Sundaram-Lin-191 teach a *metal pad*. *See* Section V.A.17.

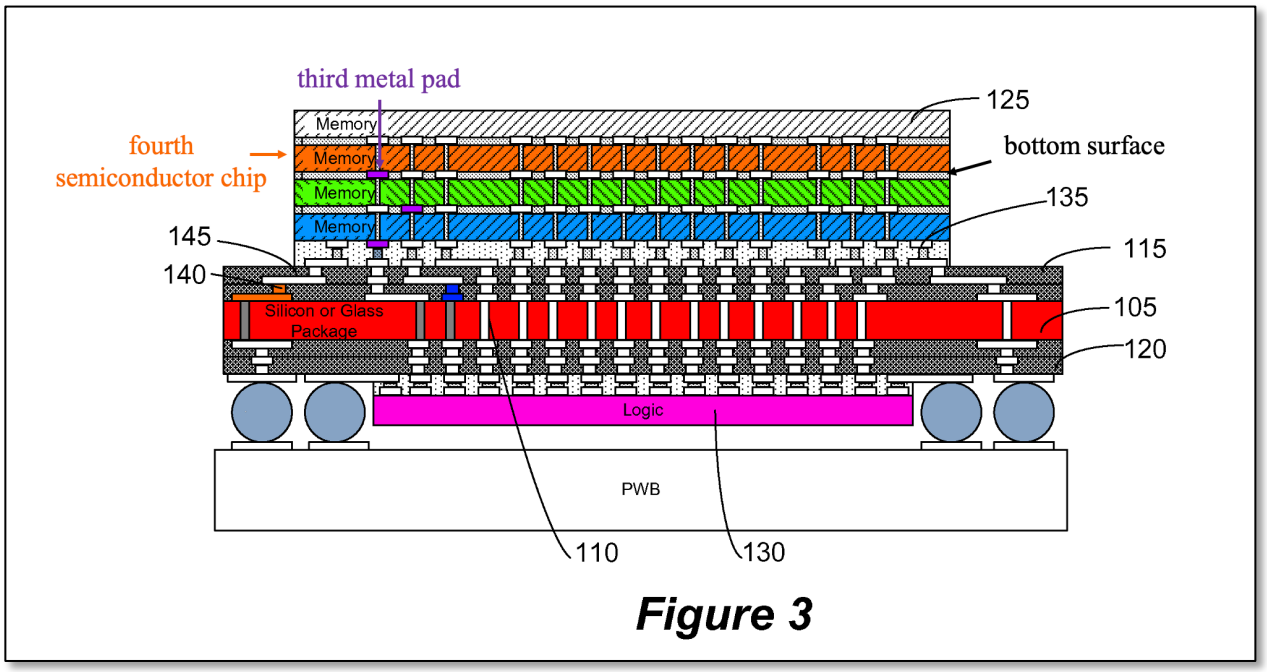


Figure 3

EX1004, FIG. 3; *EX1003*, ¶267.

FIG. 32 depicts a chip stack similar to FIG. 3's where each chip has a distinct metal pad.

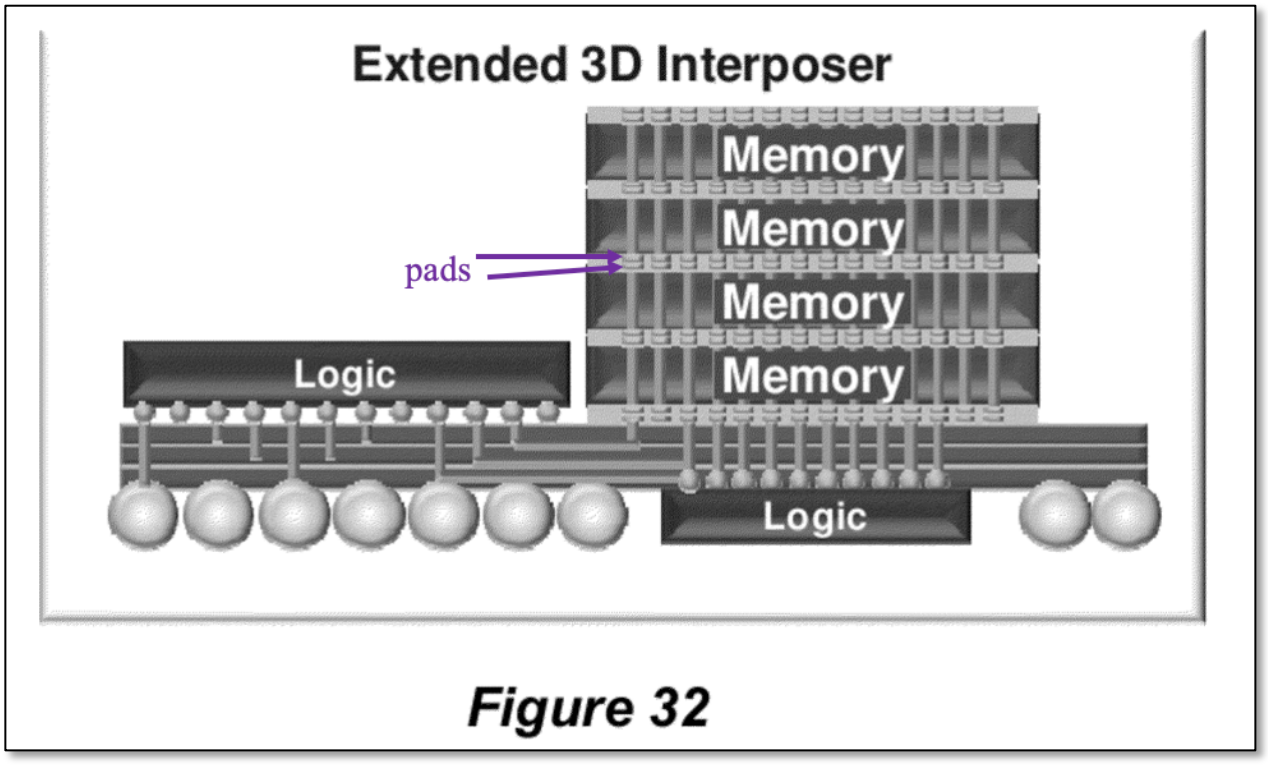


Figure 32

EX1004, FIG. 32; *see* Section V.O.16 (MTCs and REOS for combining FIGS. 3 and 32); *EX1003*, ¶¶268-270.

3. 21(c)

Sundaram depicts TSV layers in FIGS. 3, 32 and teaches "TSVS were fabricated on [] wafers." *EX1004*, 14:5-18. The TSVs have "plate[d] copper" such that they are *metal*. *EX1004*, 15:7-8. Sundaram depicts a *fourth pad at a top surface*

of said first semiconductor chip, and Sundaram alone or Sundaram-Lin-191 teaches a *metal pad*. *See* Sections V.A.17, V.R.2.

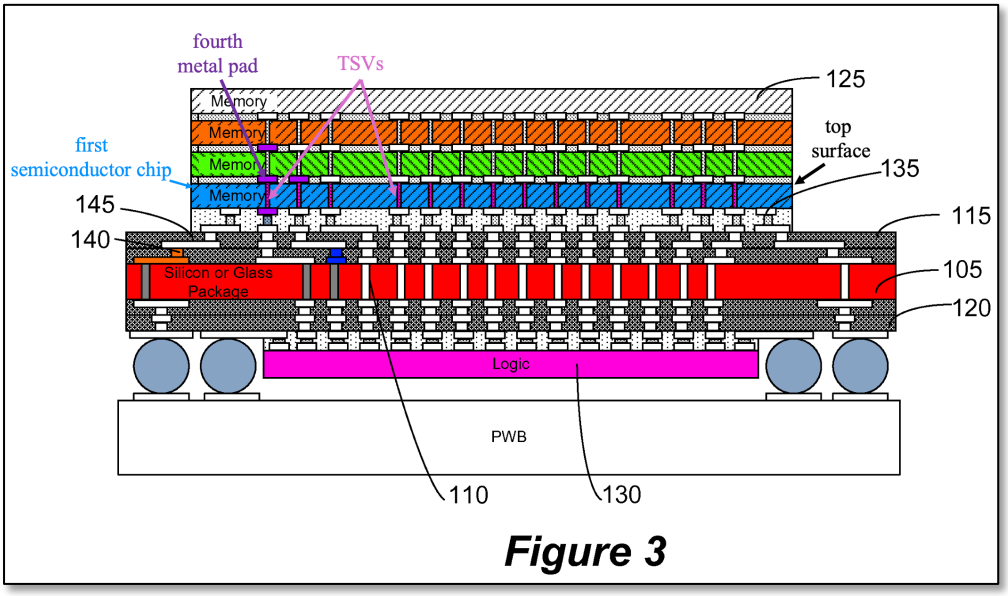


Figure 3

EX1004, FIG. 3; *EX1003*, ¶271.

FIG. 32 teaches a *fourth metal pad on a top surface* of a first semiconductor. *See* Section V.R.2 (internal MTC).

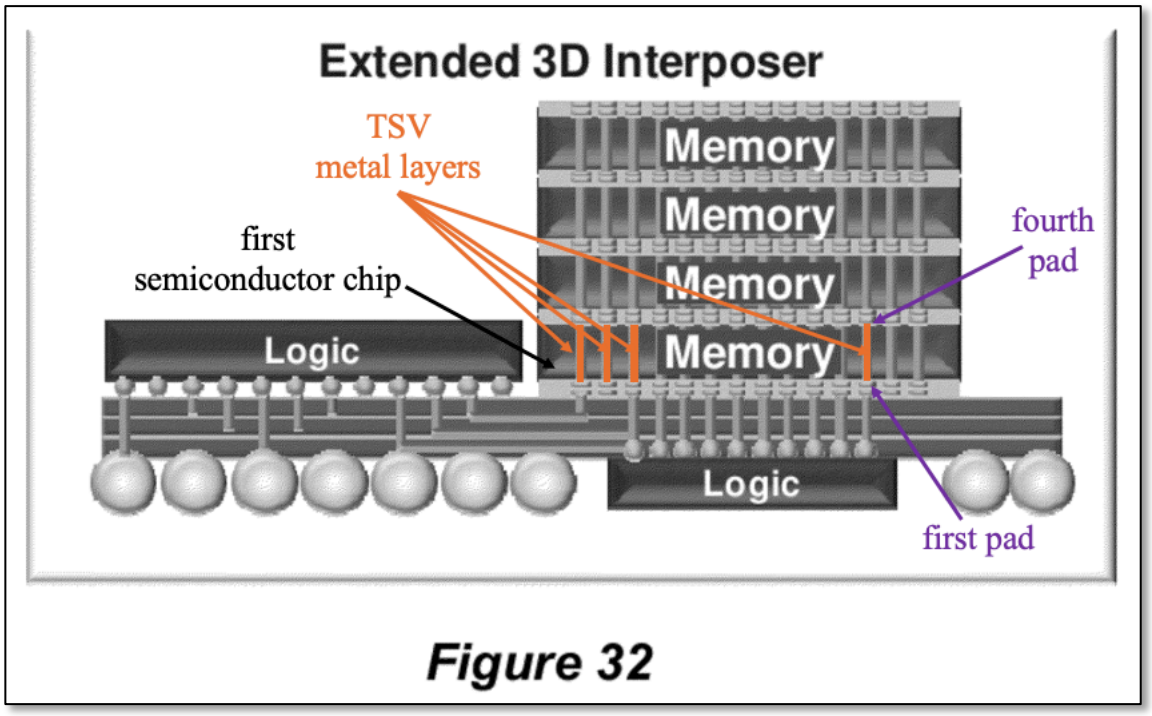


Figure 32

EX1004, FIG. 32; *EX1003*, ¶¶272-273.

4. 21(d)

The *first metal pad is at a bottom surface* of the first chip:

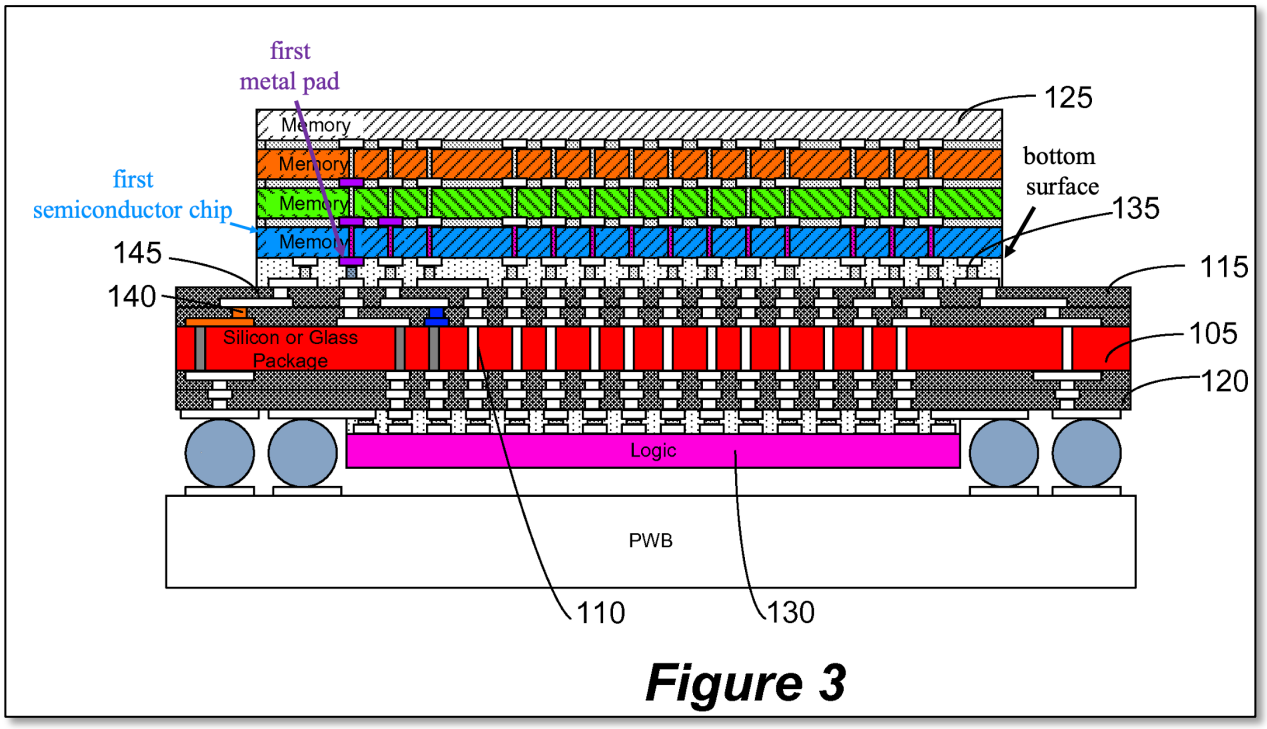
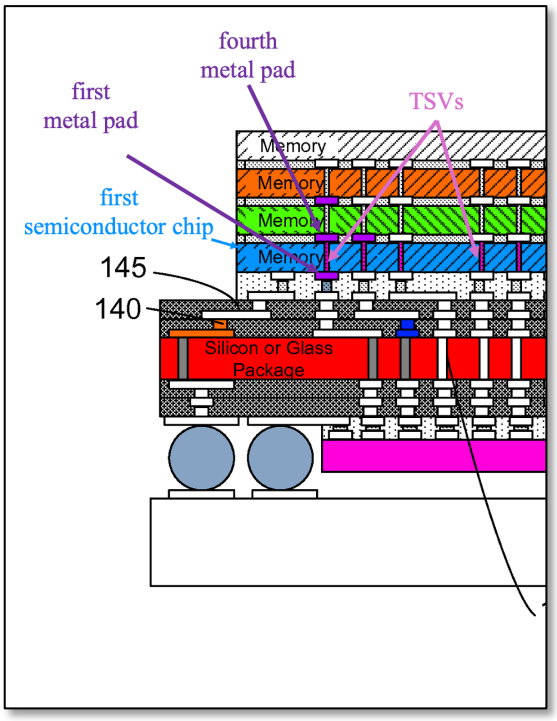


Figure 3

EX1004, FIG.3; *EX1003*, ¶274.

5. 21(e)

The *first metal pad is coupled to said fourth metal pad through* a TSV.



EX1004, FIG. 3 (excerpt); *EX1003*, ¶275.

6. 21(f)

FIG. 32's memory stack illustrates pads connected to one another, and Sundaram further teaches "die pads 135…can electrically connect devices using **solder**, copper bumps with **solder** caps…." *EX1004*, 6:29-34. A POSITA would have understood chip pads on devices 125, 130 likewise electrically connect using solder. *EX1003*, ¶277.

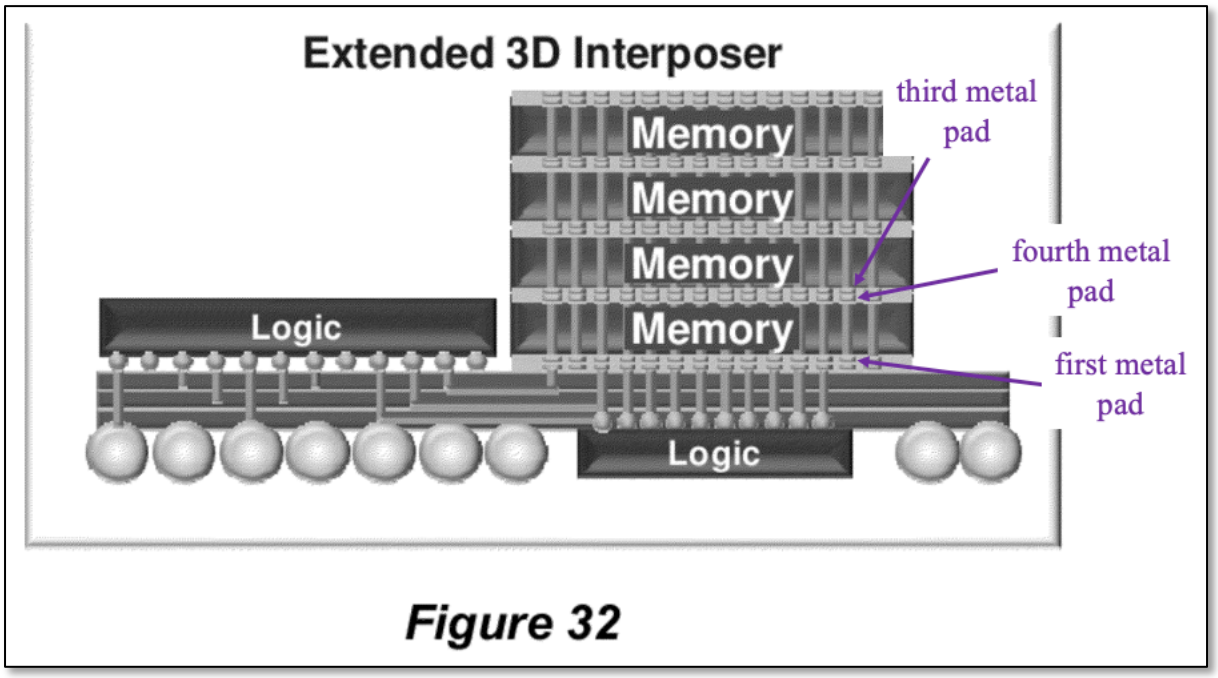


Figure 32

EX1004, FIG. 32; *EX1003*, ¶¶276-277.

A POSITA would have found it obvious, been motivated, and had a REOS in combining Sundaram's internal embodiments to *couple[]* Sundaram-Lin-191's *third metal pad* and *fourth metal pad through a solder layer*, teaching Claim 21(f). *EX1003*, 278. The modification is the combination of known prior art elements (solder connections for chip pads) according to known methods to yield predictable results. The modification would have advantageously provided Sundaram with a good electromechanical connection between chips, which would have had a REOS because such was a common method of connecting chips. *EX1003*, 279.

S. Claim 22

Sundaram teaches the 3D structure is usable for "graphics." *EX1004*, Abstract. Lin-191 teaches chip 160 is a "graphics-processing-unit (GPU) chip." *EX1005*, [0382]. MTCs and REOS for Sundaram-Lin-191 are provided. *See* Section V.B. Additionally, Sundaram teaches "high power logic component[s]" *over* the *first interconnection scheme*:

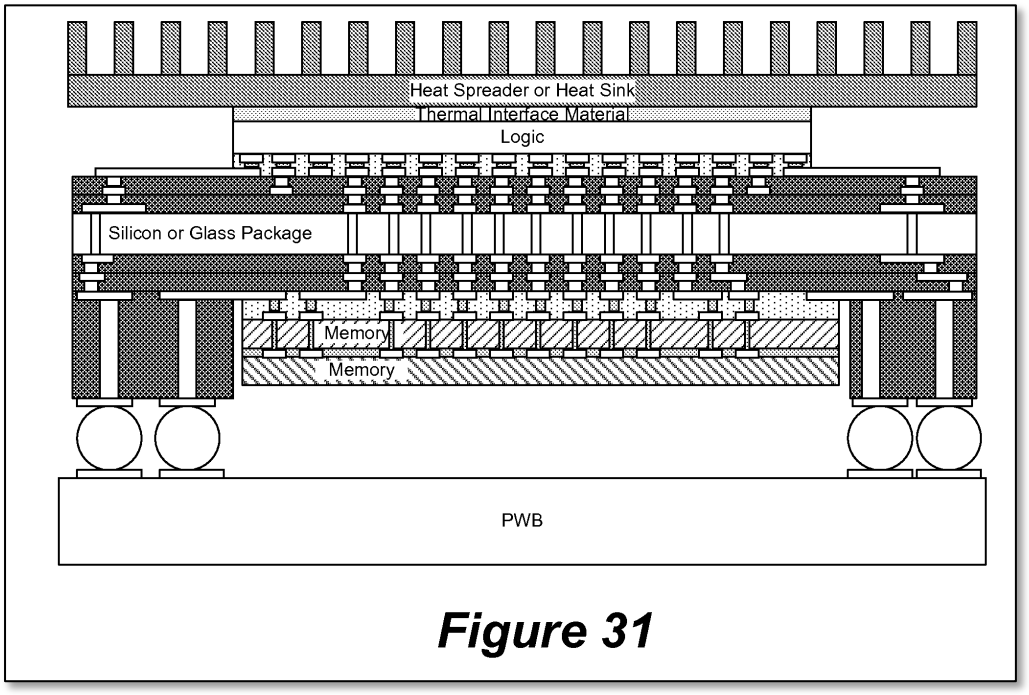


Figure 31

EX1004, FIG. 31; *EX1003*, ¶280.

T. Claim 23

Sundaram teaches logic chips, including a logic chip *over* the interconnection scheme.

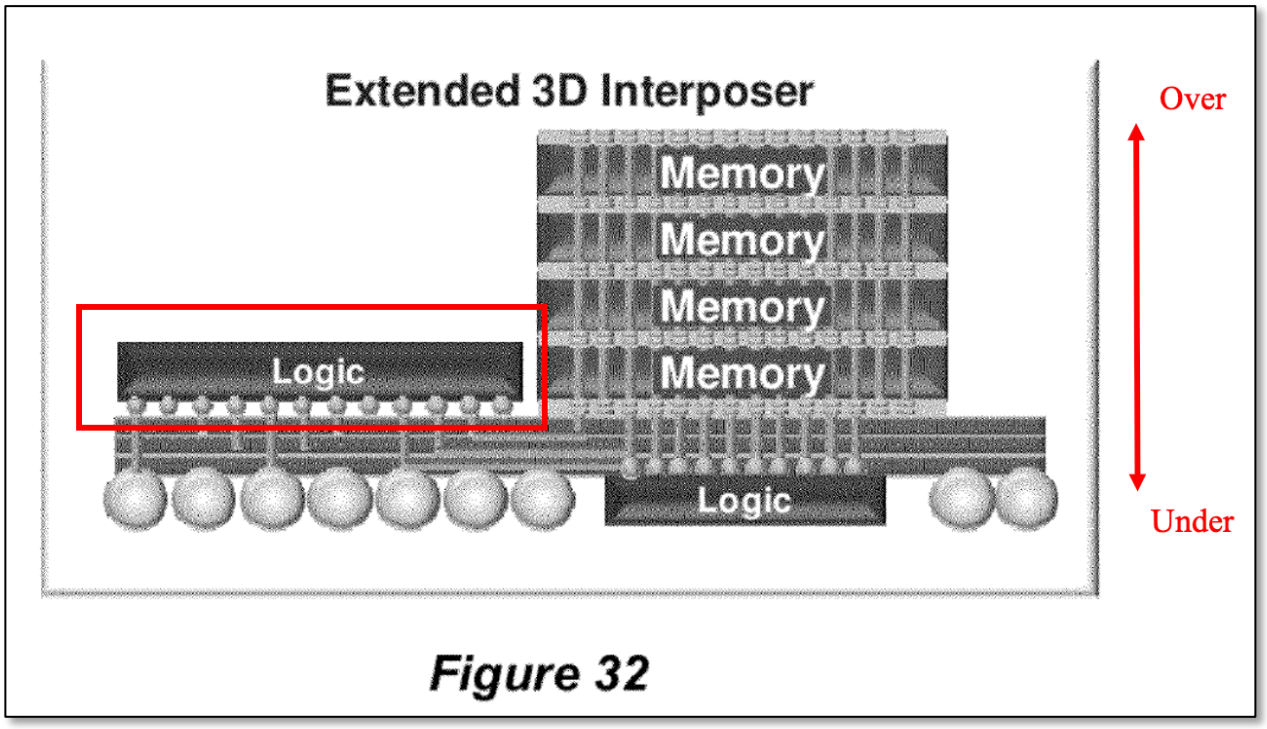


Figure 32

EX1004, FIG. 32, Abstract; *EX1003*, ¶281.

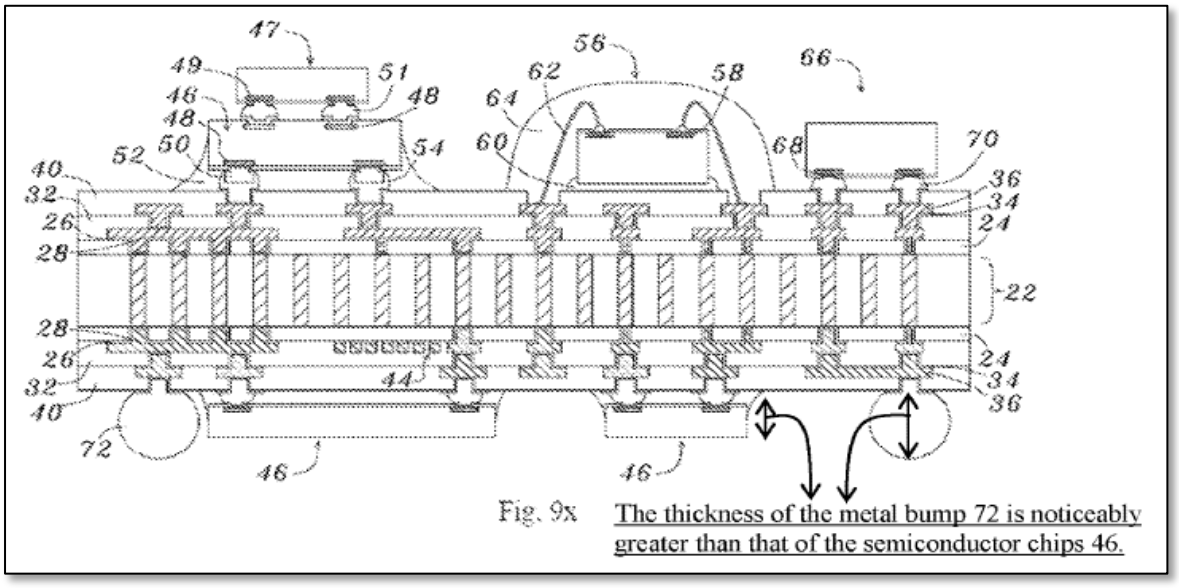
A POSITA would have been motivated and found it obvious to modify Sundaram's FIG. 3 embodiment per FIG. 32's teachings to have a *second semiconductor chip that is a logic chip*. *Id.* The modification would have predictably improved FIG. 3's chip package by adding additional compute via the *logic chip*. *Id.* There would have been a REOS because the modification would have been simple and straightforward and merely required connecting a logic chip to Sundaram's interposer 105 using well-known techniques. *Id.*

U. Claim 24

See Section V.T.

V. Claim 25

During original prosecution, PO filed an Amendment with an annotated figure arguing specification support for Claim 25:



EX1002, 336; *EX1003*, ¶284; *see* cited caselaw in Section V.A.8.

Sundaram's *third semiconductor chip* is shorter than the surrounding bumps, satisfying Claim 25.

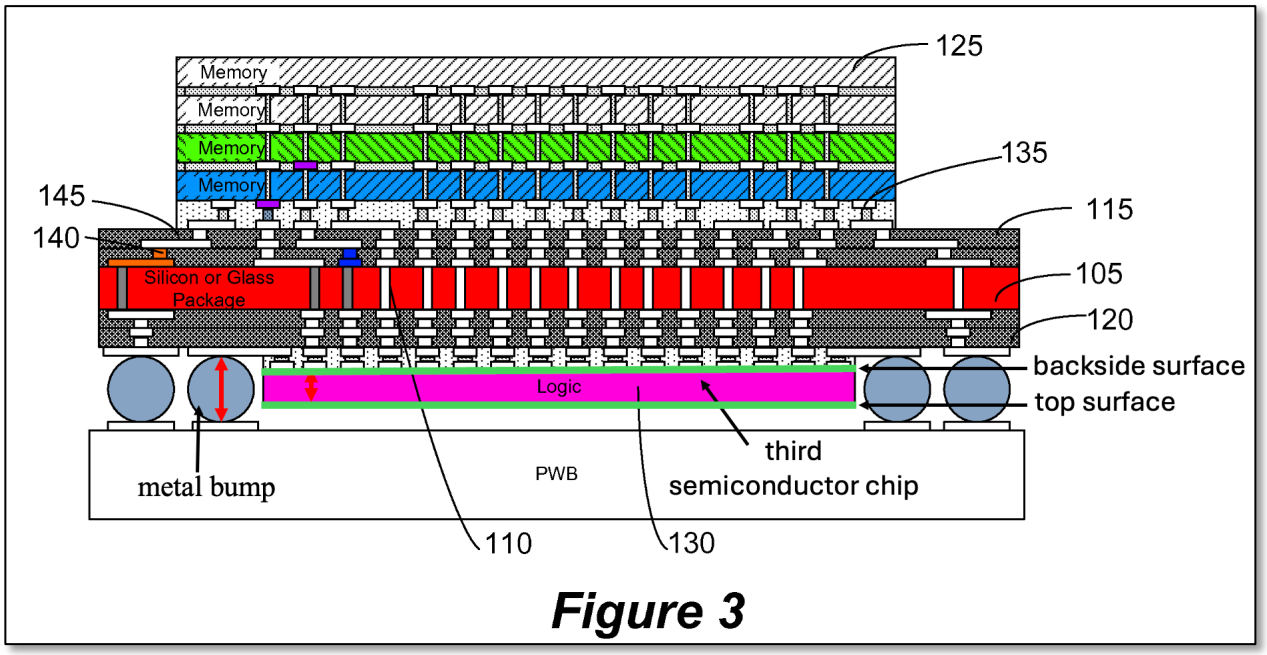


Figure 3

EX1004, FIG. 3; *EX1003*, ¶285.

W. Claim 26

See Section V.R.1, reciting corresponding limitations.

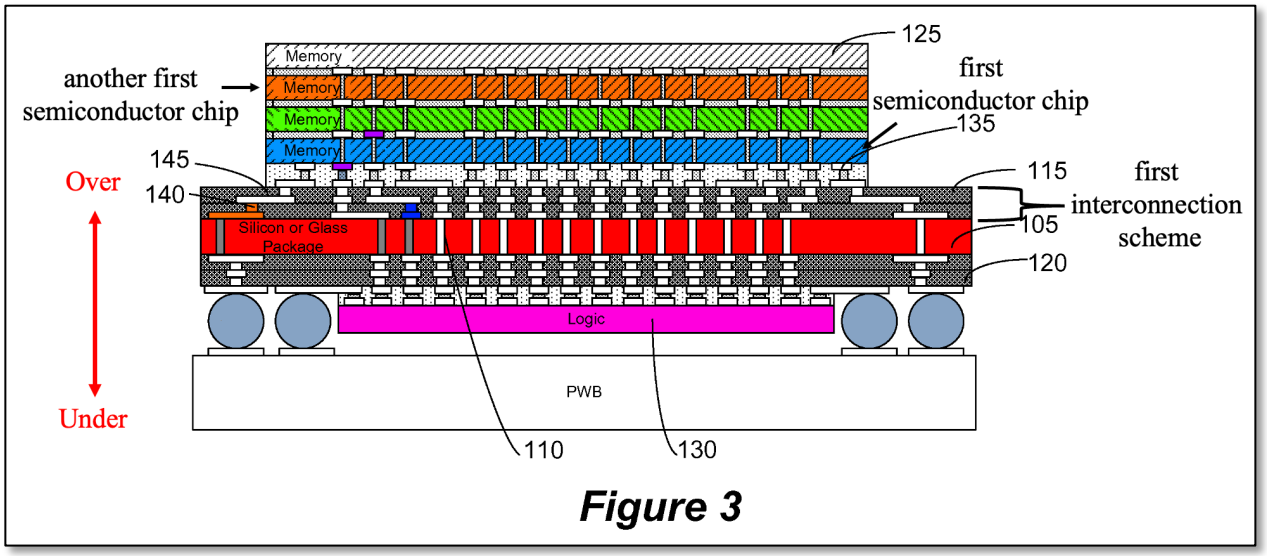


Figure 3

EX1004, FIG. 3; *EX1003*, ¶286.

X. Claim 27

1. 27(a)

Sundaram teaches "device 130 can be a logic IC device or devices," thereby teaching *a fourth semiconductor chip under said first interconnection scheme*, i.e., the second logic device. EX1004, 6:37-39. FIG. 5d illustrates *a fourth semiconductor chip under said first interconnection scheme*:

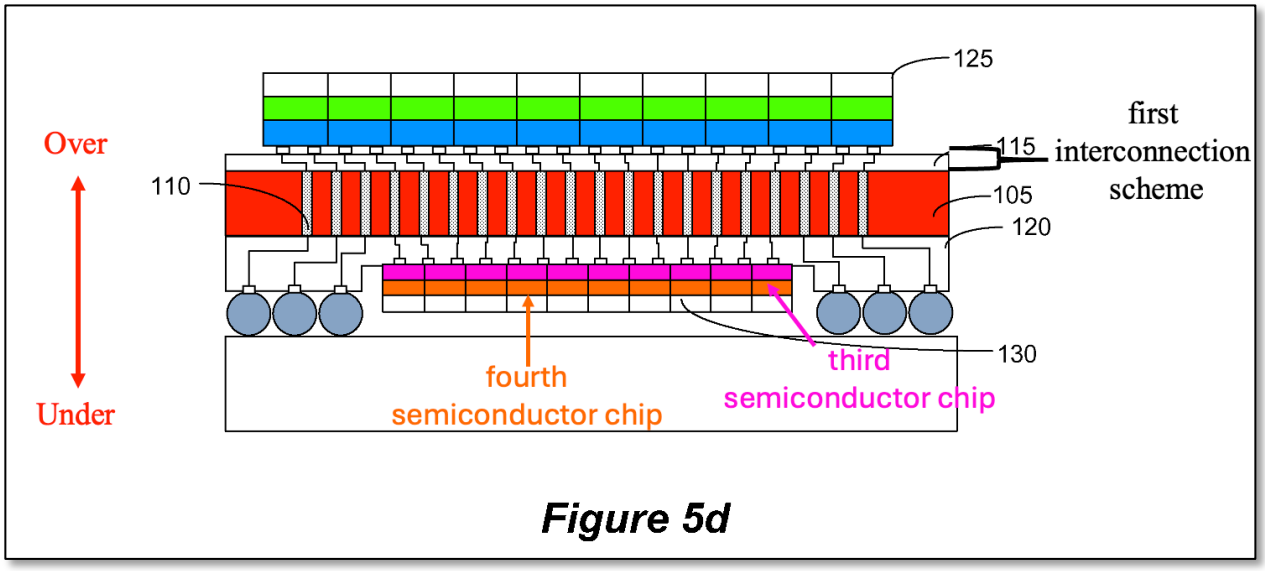


Figure 5d

EX1004, FIG. 5d; *EX1003*, ¶287.

2. 27(b)

Shown in FIG. 5d, Sundaram's fourth chip has a *thickness…smaller than a thickness of one of said plurality of metal bumps*:

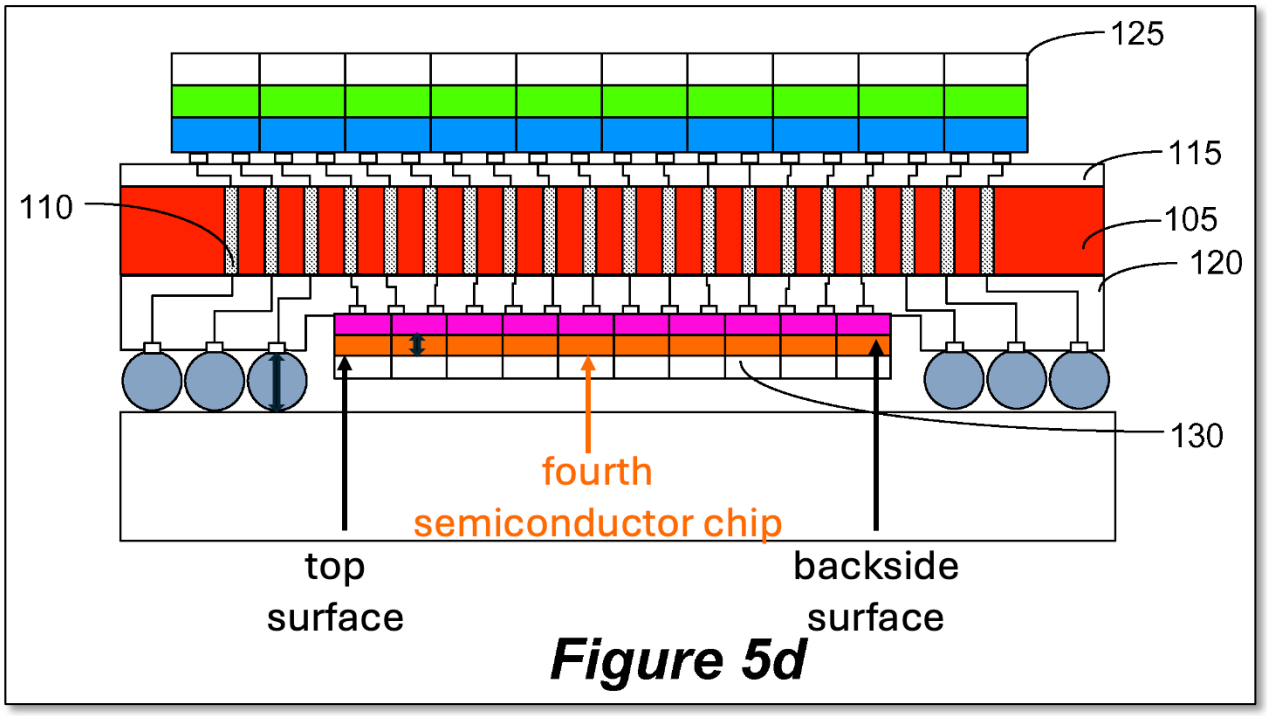
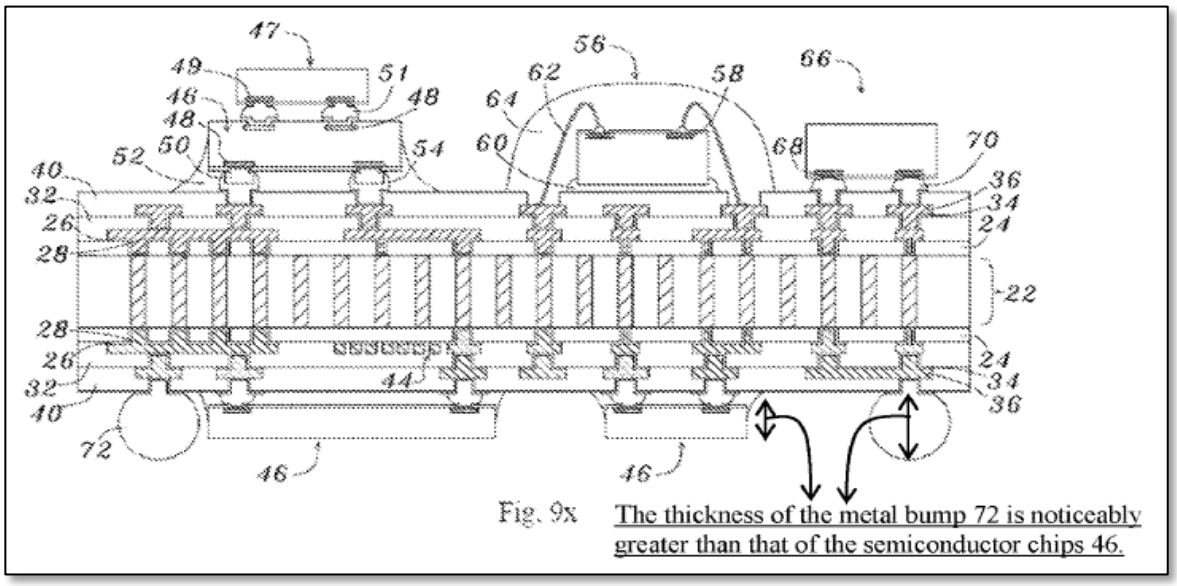


Figure 5d

EX1004, FIG. 5d; *EX1003*, ¶288.



EX1002[6], 336; *EX1003*, ¶289.

[6] Annotated figure PO argued supports language similar to Claim 27(b).

VI. GROUND 1B: CLAIMS 8, 12, AND 16 ARE OBVIOUS OVER SUNDARAM, LIN-191, AND LIN-863

A. Claim 8

During original examination of the ’306 Patent’s parent application (USPN 11,538,763), PO argued that annotated FIG. 6l shows support for the claimed *rectangle region*.

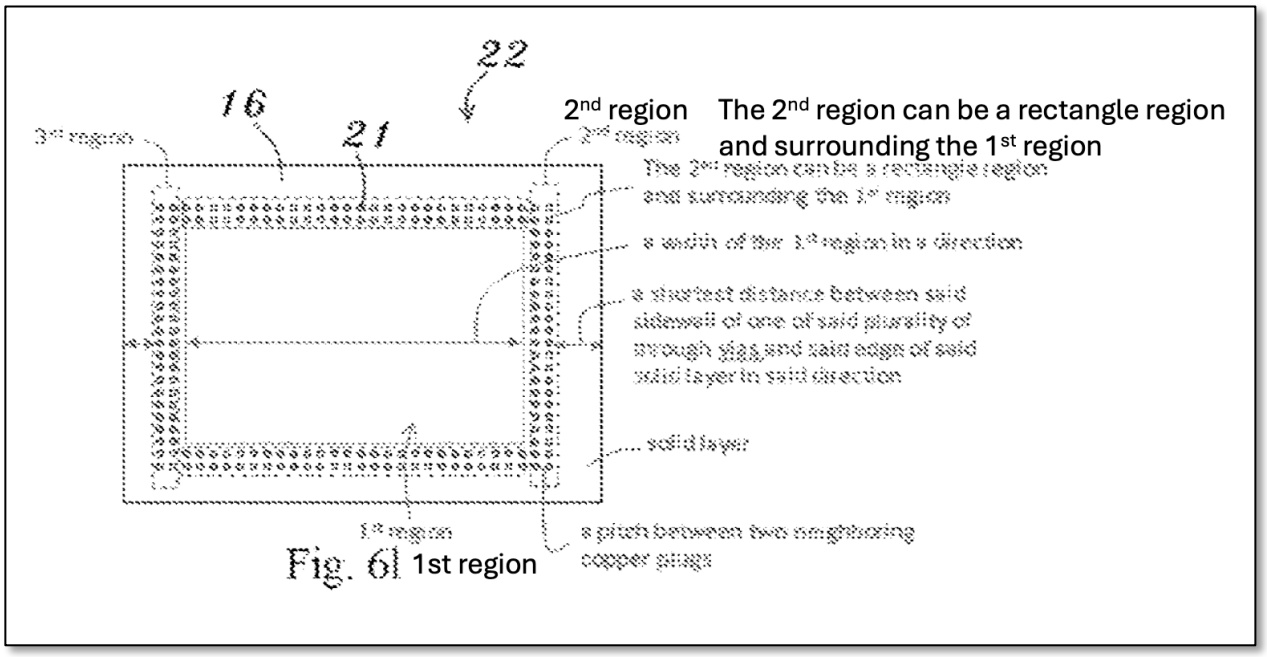


Fig. 6l

EX1117, 360; *EX1003*, ¶290.

Sundaram’s “FIG. 4 illustrates a top view of the interconnect structure illustrated in FIG. 3,” which includes the *first region* and the *second region that is a rectangle region surrounding said first region*. *EX1004*, 3:27-28.

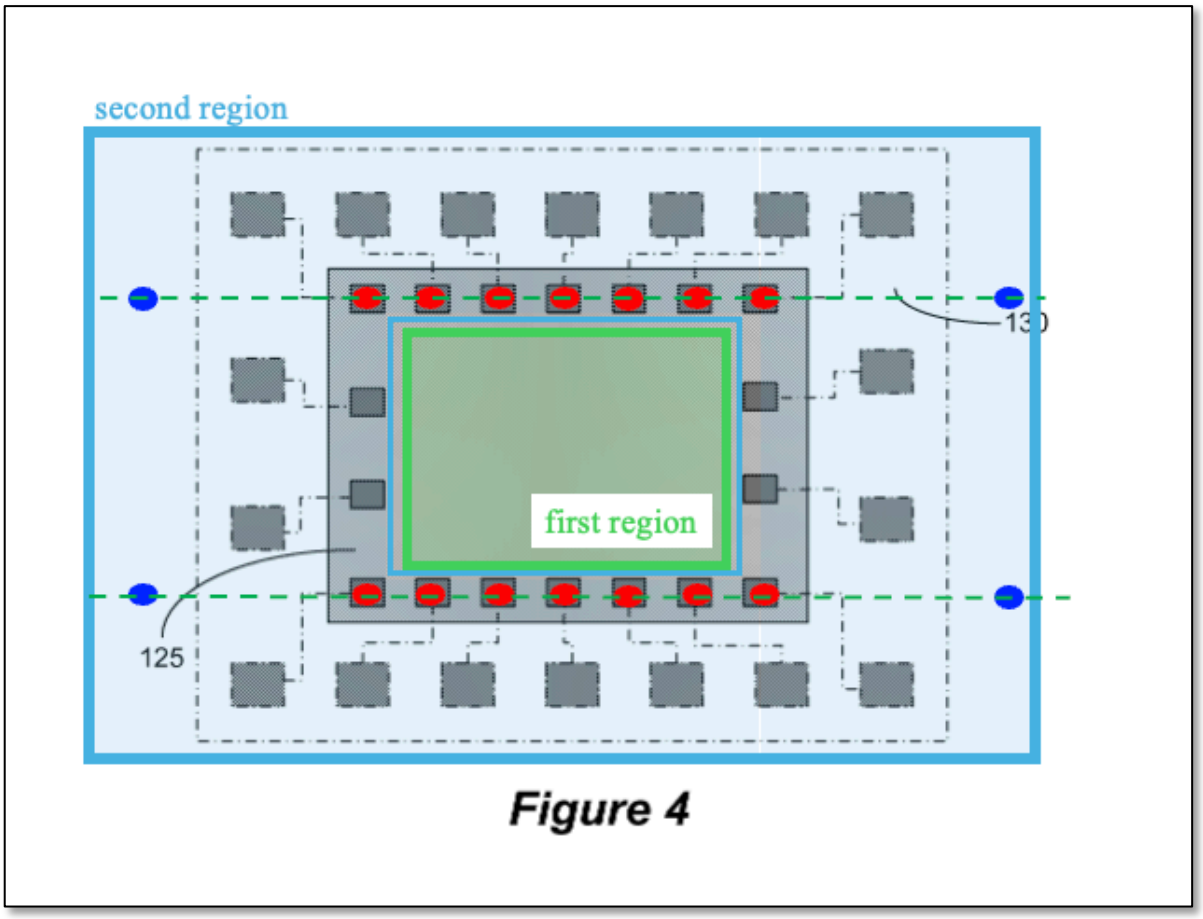


Figure 4

EX1004, FIG. 4.

Sundaram teaches "device 125 is of a different pad size and configuration than" device 130 and "connected with through vias 110, blind vias 140, and conductor traces 145." *EX1004*, 7:1-9, FIG. 4. Based on FIGS. 3-4, a POSITA would have understood Sundaram to teach two types of vias 110: (1) vias for die-to-die connections between devices 125, 130, and (2) vias for die to PWB connections. *EX1003*, ¶291. Further, per FIGS. 3-4, the die-to-die connections (dashed lines in FIG. 4) are made through pads located at the periphery of the dies, which are

connected to the die-to-die vias 110 in interposer 105 (FIG. 3). *Id*. Additionally, per FIG. 3, die-to-die vias 110 and the pads of the smaller device 130 are substantially within the same projection region, while the die-to-PWB vias 110 are located outside the peripheral area of the smaller device 130. *Id*.

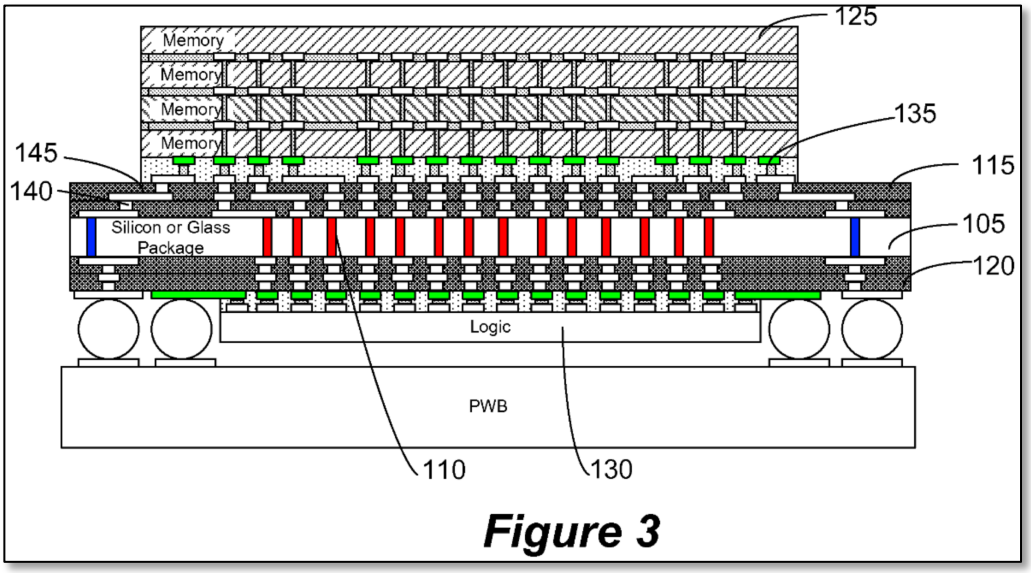


Figure 3

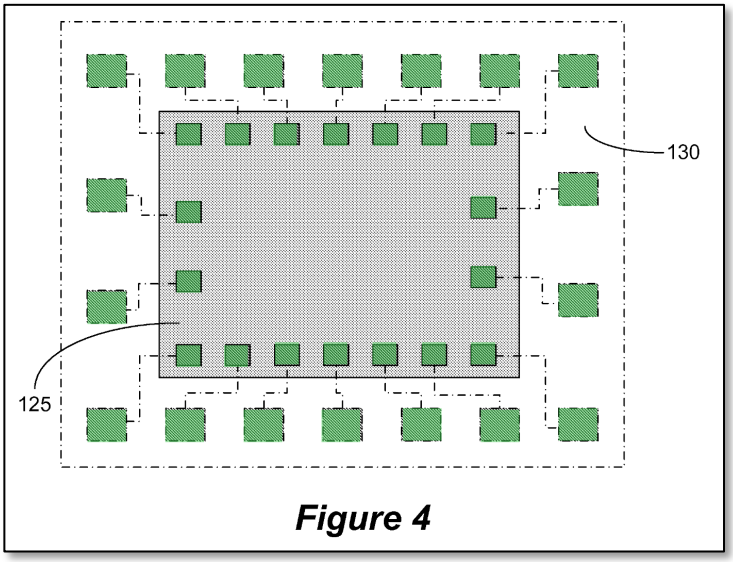


Figure 4

EX1004, FIGS. 3-4[7].

Thus, based on Sundaram's teachings, a POSITA would have understood a plan view of Sundaram's interposer to look as follows, which teaches the claimed *rectangle region*.

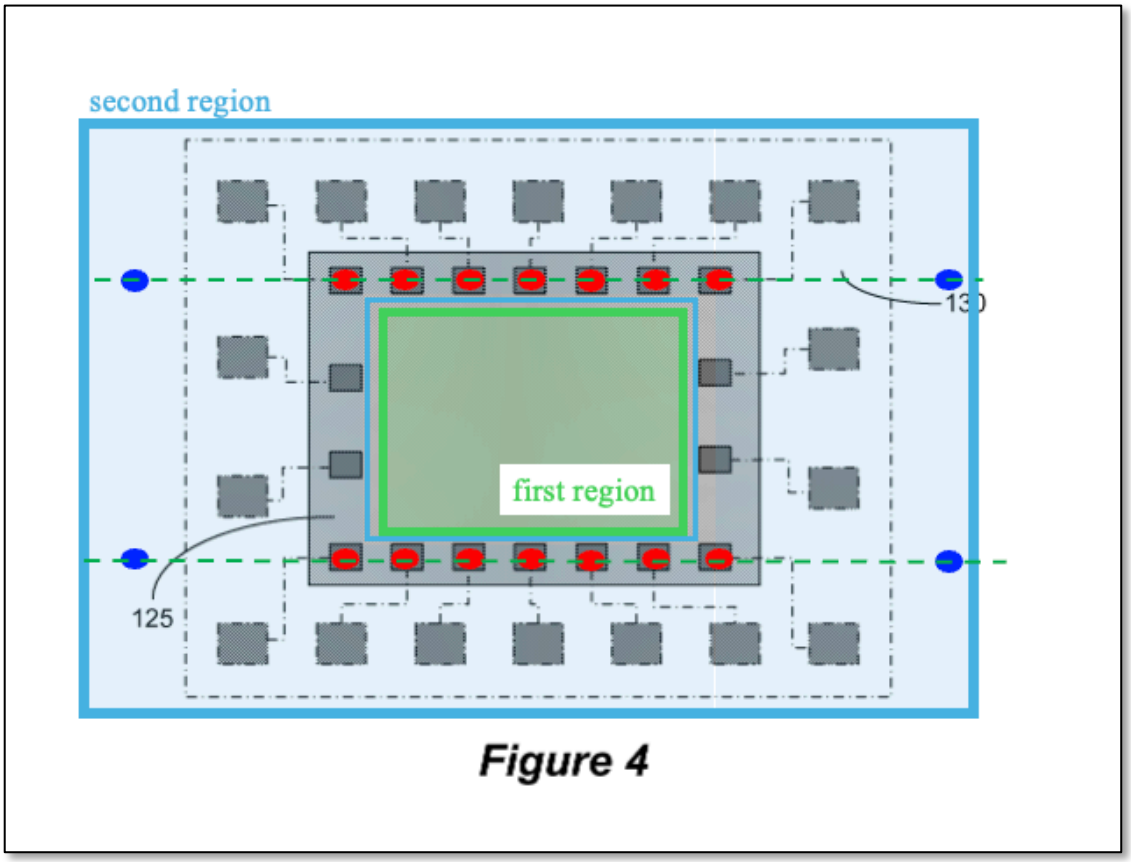


Figure 4

[7] A POSITA would have understood Sundaram's FIG. 4 to mislabel devices 125, 130 based on their depiction in FIG. 3; i.e., per FIG. 3, device 125 is larger than device 130, so the outer box (white) should be device 125, while the inner box (gray) should be device 130. *EX1003*, ¶293.

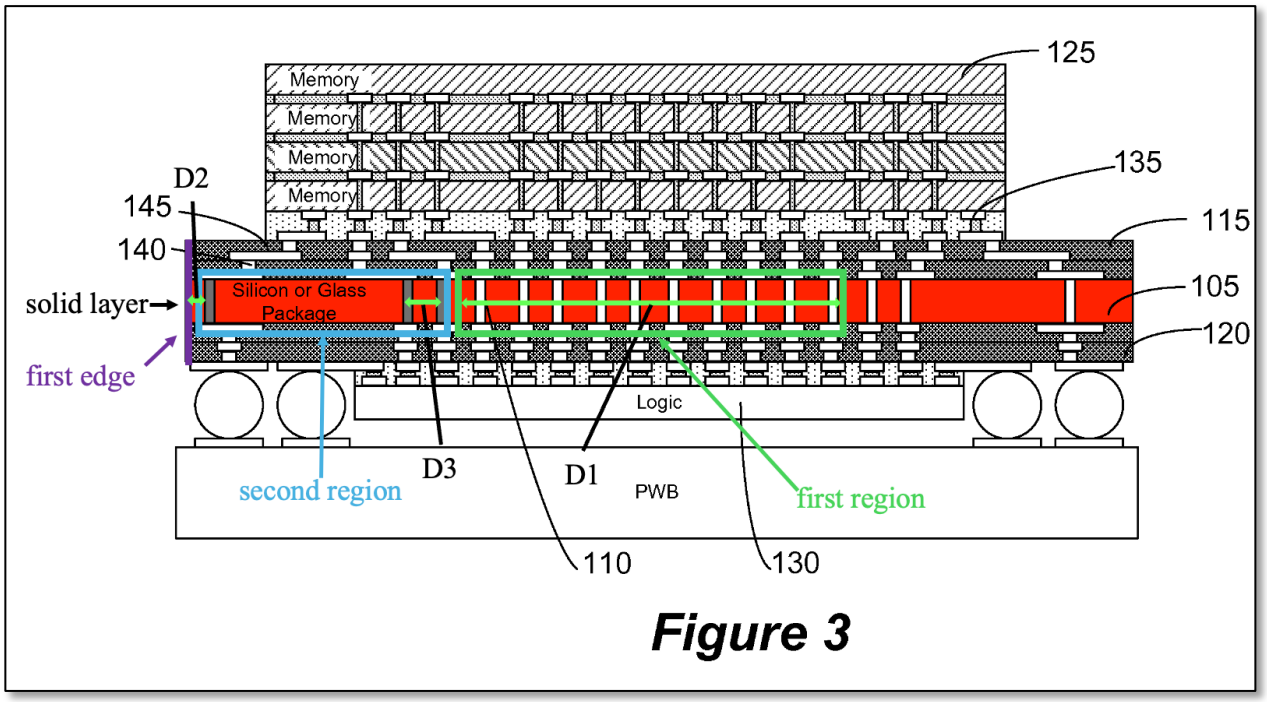


Figure 3

EX1004, FIGS. 3-4; *EX1003*, ¶292. The dashed lines in FIG. 4 illustrate exemplary cross-sectional lines corresponding to FIG. 3's cross-section. *Id*.

To the extent PO argues the *rectangle region* is the right-hand side (per *EX1117*, 360), Sundaram's teaches it:

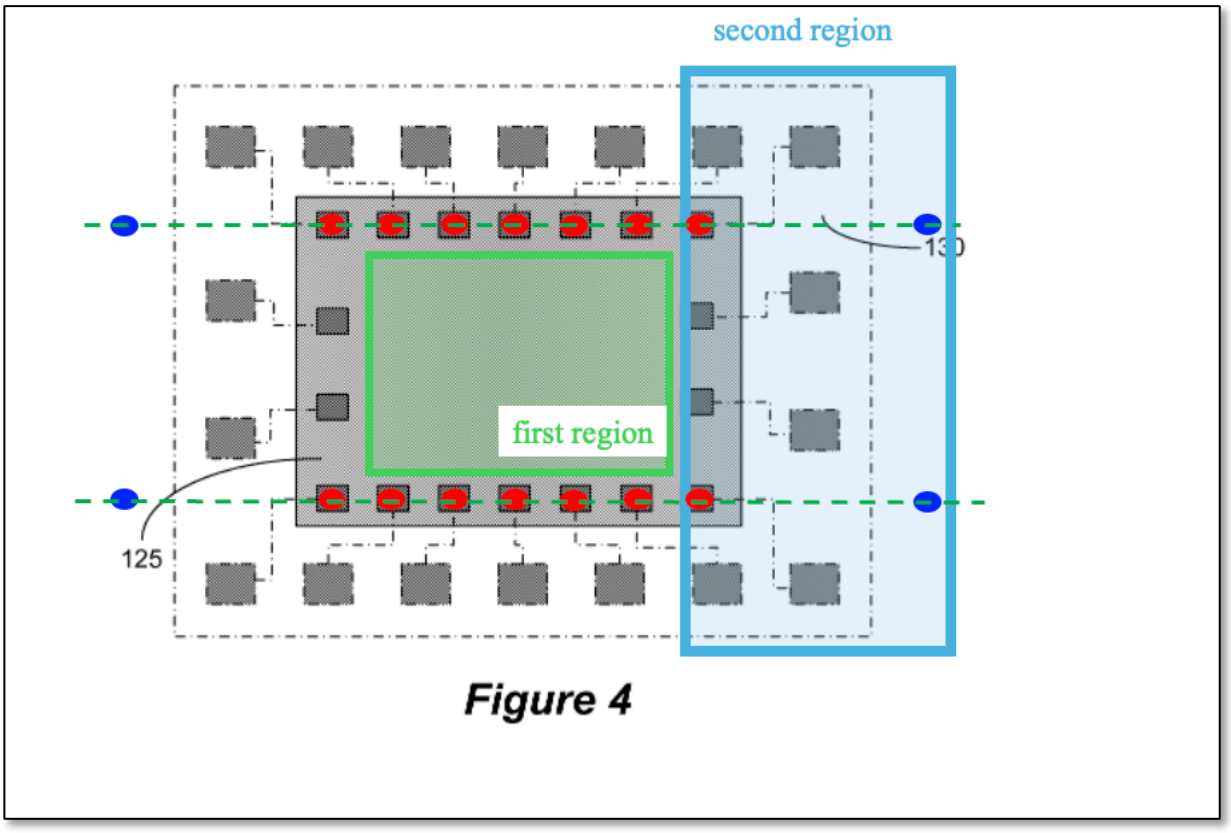


Figure 4

EX1004, FIG. 4; *EX1003*, ¶295.

a) Lin-863's Teachings

Additionally or alternatively to Sundaram, Lin-863 teaches a fan-out wafer level chip scale package 262 having a substrate 226 (*solid layer*) through with "conductive TMV[s] [through-mold vias] 225" and "semiconductor die 124" are disposed. *EX1007*, 12:33-42, 14:45-46, FIGS. 9a-9b. Shown below, package 262 includes a *first region* and *a second region* similar to the '306 Patent's regions identified in FIG. 6l. *EX1117*, 272. Lin-863's *first region* (blue) is surrounded by the *second region* (green), which is the region on substrate 226 where conductive TMVs

225 are located. *EX1003*, ¶296. Lin-863's *second region is a rectangle region surrounding said first region*.

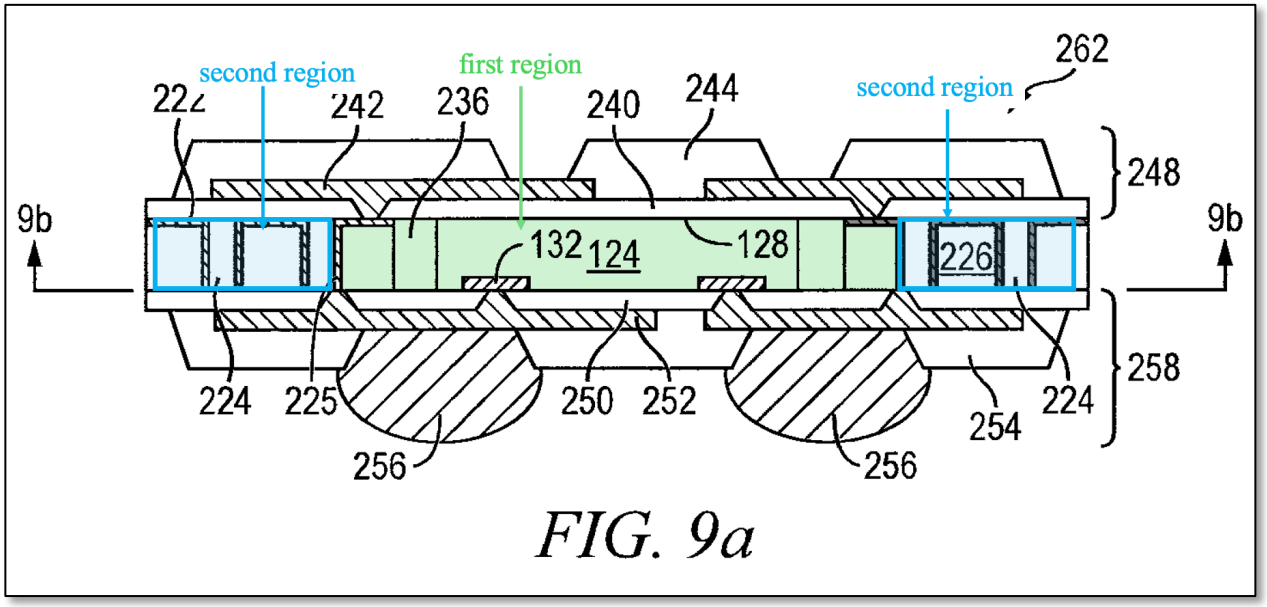


FIG. 9a

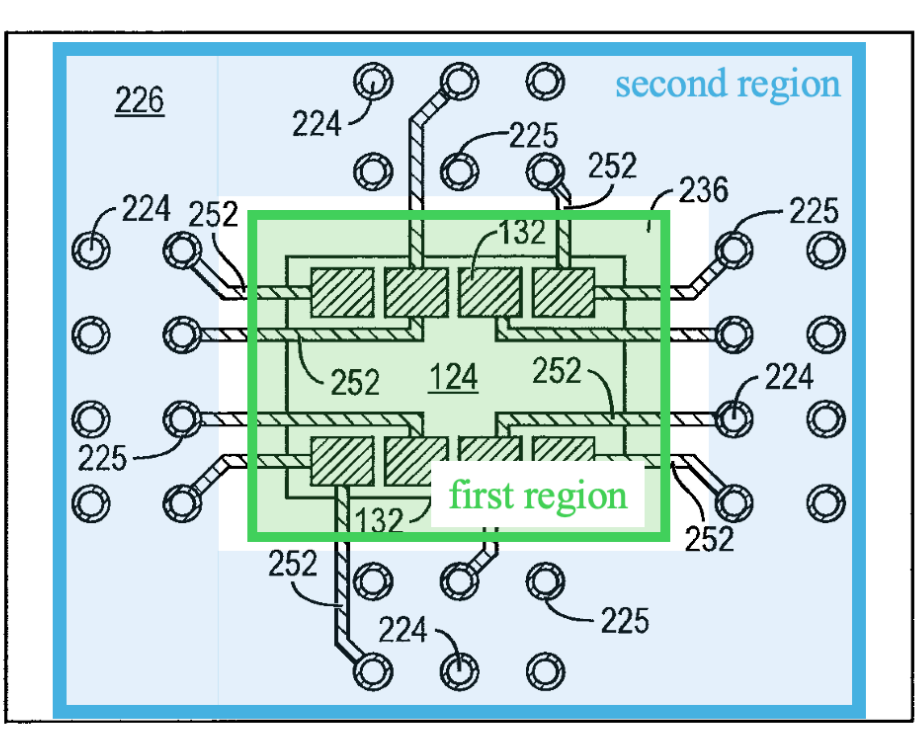

262
226
second region
224
225
252
236
224
252
225
132
252
124
252
224
225
first region
132
252
252
224
225

FIG. 9b

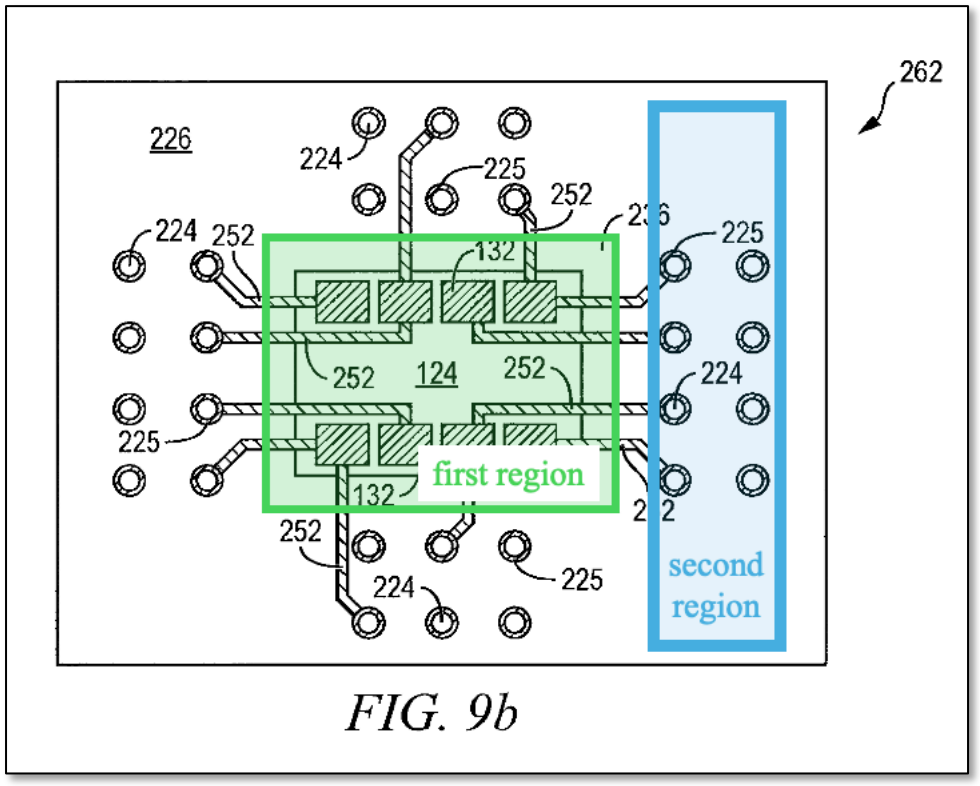


FIG. 9b

EX1007, FIGS. 9a-b.

b) MTC

Alternative to Petitioner's mapping that Sundaram teaches Claim 8 and if otherwise disputed, a POSITA would have found it obvious and been motivated to configure Sundaram's *second region* to be *a rectangle region surrounding said first region* per Lin-863's teachings. *EX1003*, ¶¶297-299. As discussed, Sundaram teaches or at least contemplates such a *rectangle region* in FIG. 4:

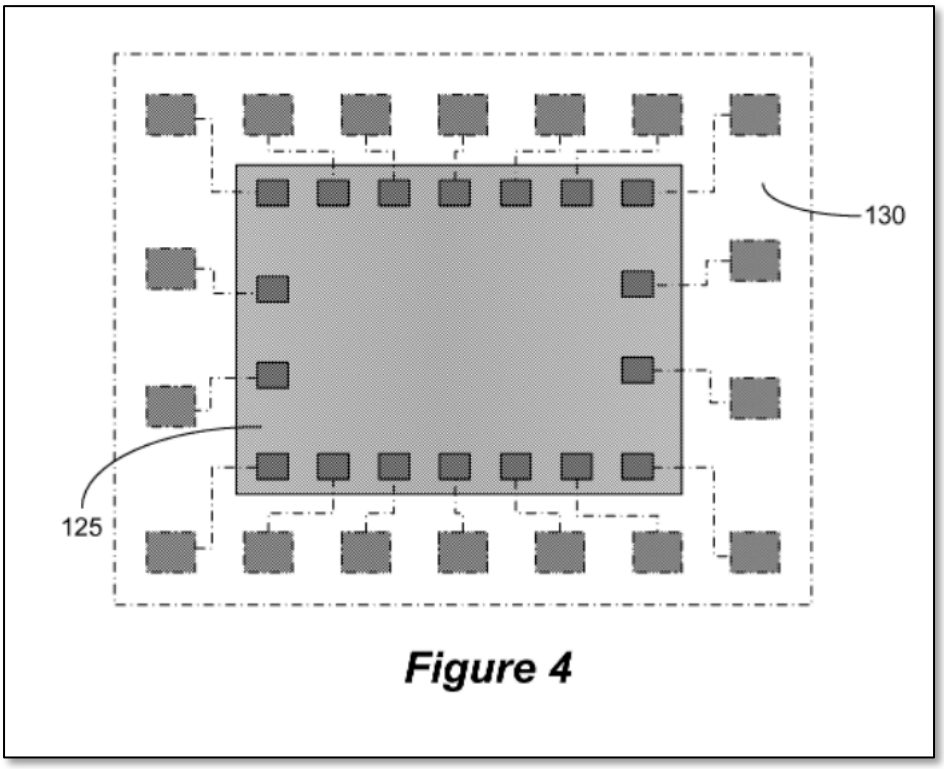


Figure 4

EX1004, FIG. 4; *see* Section VI.A. Thus, it would have been obvious to modify Sundaram per Lin-863 such that Sundaram's interposer 105 (*solid layer*) had a *rectangle region* for enabling the interconnection between the devices 125, 130. *EX1003*, ¶298. Such an arrangement also permits the addition of passive components directly under the chip or, it allows for placement of heat sink material directly under the chip, improved thermal dissipation, and shorter interconnect paths by embedding the chip within the interposer/package. *EX1003*, ¶298.

Further, a POSITA would have been motivated and found it obvious to modify Sundaram's chip package to have through vias 110 in a rectangular second region surrounding a first region to match the standard rectangular geometry of a chip.

EX1003, ¶299. Specifically, chips are cut into a rectangular shape as non-rectangular shapes do not maximize the use of valuable wafer area where circuitry can be fabricated. *Id.* Thus, it is practical and common practice to surround a chip with posts/vias arranged in a geometry that mirrors the chip's shape, e.g., to mirror the rectangular shape of device 125. *Id*.

The combination is the application of known technique (interconnects in a rectangular arrangement in a chip package) to a known device (Sundaram's chip package) to yield the predictable results of Sundaram's package having through vias 110 in a rectangular region. *EX1003*, ¶300. There would have been a REOS because Lin-863's fan-out package with a *rectangle region* represents a well-known package geometry. *Id*.

B. Claim 12

See Section VI.A. Sundaram's FIG. 4 teaches *no any copper post in said first region*[8]:

[8] Petitioners interpret the claimed *no any copper post* to be "no copper post."

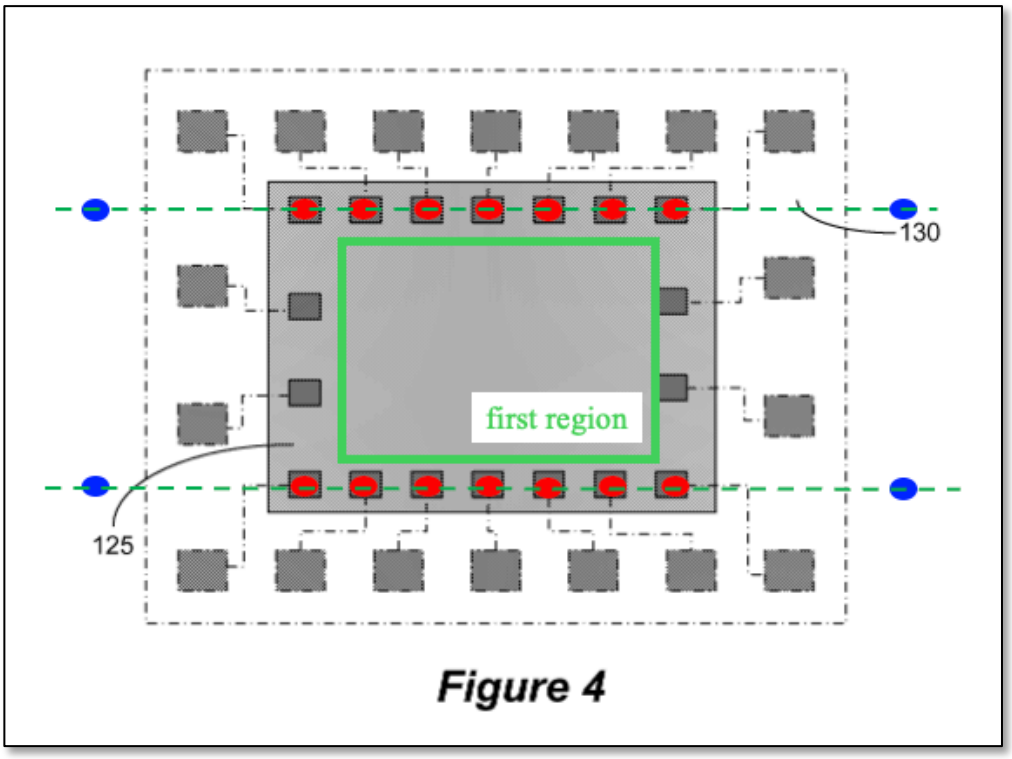


Figure 4

EX1004, FIG. 4; *EX1003*, ¶¶301-302. Because Sundaram teaches die-to-die vias connecting pads are at the periphery (as opposed to pads in the middle of the dies) and that the die-to-PWB vias are located outside the peripheral area of the smaller device, a POSITA would have understood Sundaram as teaching the *first region* as having no copper plugs. *EX1003*, ¶302.

a) Lin-863's Teachings

Additionally or alternatively to Sundaram's teachings, Lin-863's *first region* has no *copper…post[s]* as shown:

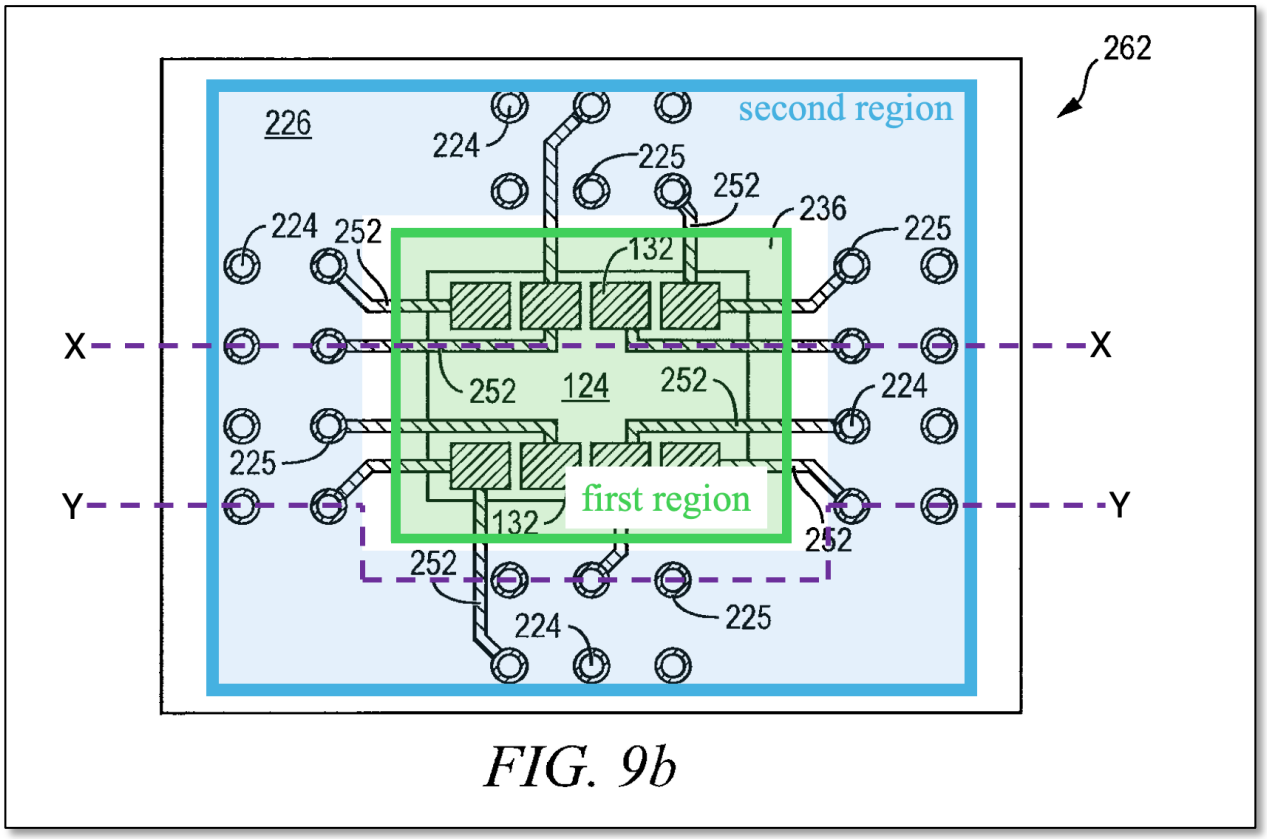


FIG. 9b

EX1007, FIG. 9b.

No copper post[s] in the *first region* is also depicted in the cross-sectional FIG. 9a, where TMVs 225 are on the sides of the *first region*. *EX1007*, 14:45-46. The 9b-9b cross-section line in FIG. 9a corresponds to the X-X line annotated in 9b, while a POSITA would understand Sundaram's FIG. 3 section to be taken along a line analogous to Y-Y. *Compare EX1007*, FIG. 9b *with EX1004*, FIG. 4; *EX1003*, ¶¶303-305.

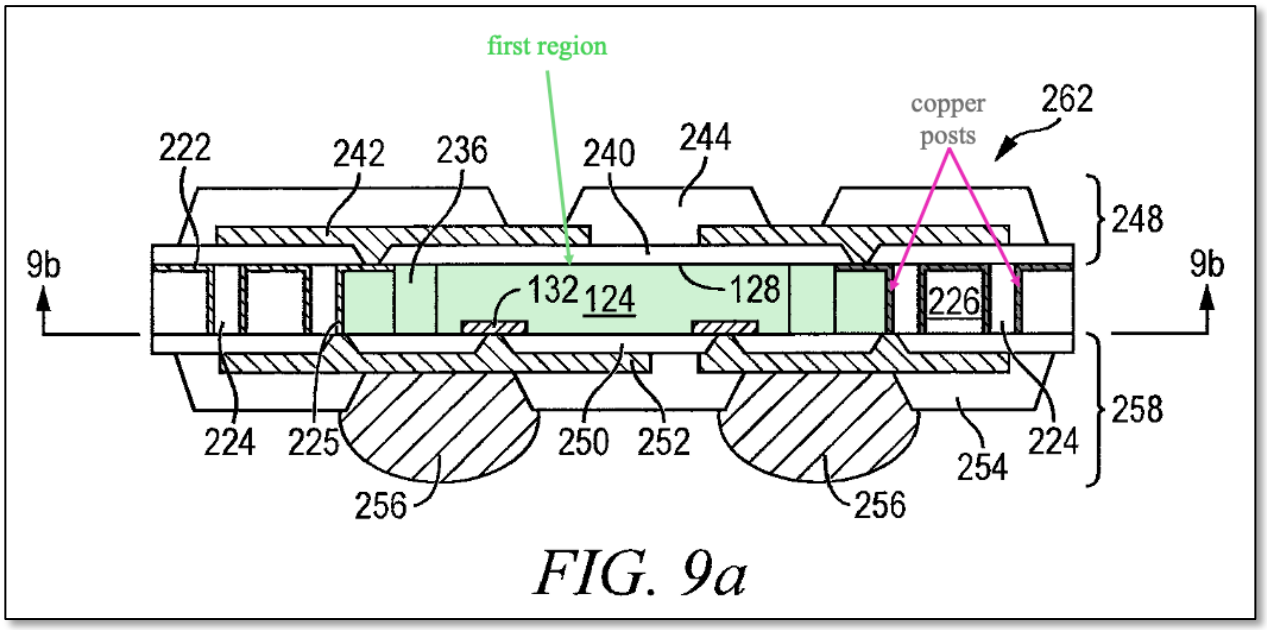


FIG. 9a

EX1007, FIG. 9a.

b) MTC

A POSITA would have found it obvious and been motivated to modify Sundaram's *first region* per Lin-863's teachings to accommodate space for an additional semiconductor chip to be included in Sundaram's package. *EX1003*, ¶306. A POSITA would have appreciated the additional functionality that another chip would provide and recognized that including an additional chip in interposer 105 would have been an efficient use of space while providing short interconnect paths for the embedded chip. *Id.*

The combination is the application of known techniques (no plugs/interconnects in a central region) to a known device (Sundaram's chip package) to yield the predictable results of Sundaram's package having a post-free

region where a die is positioned. *EX1003*, ¶307. There would have been a REOS because methods of controlling post placement in chip packages were well known. *Id*.

C. Claim 16

See Section VI.A.

VII. GROUND 2A: CLAIMS 1-7, 9-15, 17-20, AND 22-27 ARE OBVIOUS OVER YU AND LIN-191

A. Claim 1

1. 1(Pre)

Yu teaches a "PoP [Package-on-Package] structure" comprising "multiple packages 202", which includes dies (e.g., "a logic circuitry die, a memory die, or any other die") such that the PoP structure is a *chip package*. *EX1010*, 8:35-36, 2:50-51, 1:49-51 ("Package-on-Package (PoP) is an integrated circuit packaging technique to allow vertically combining discrete logic and memory ball grid array (BGA) packages."); *EX1003*, ¶¶309-310.

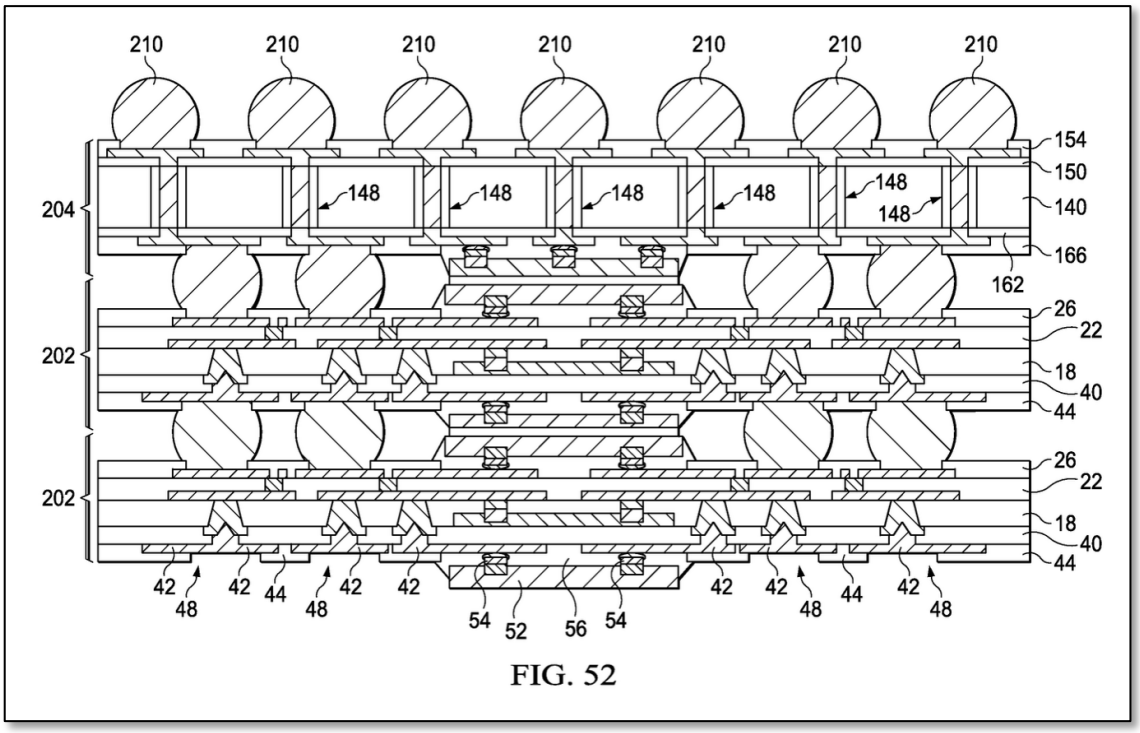


FIG. 52

EX1010, FIG. 52.

One of the packages 202 in Yu's *chip package* is shown in FIG. 16:

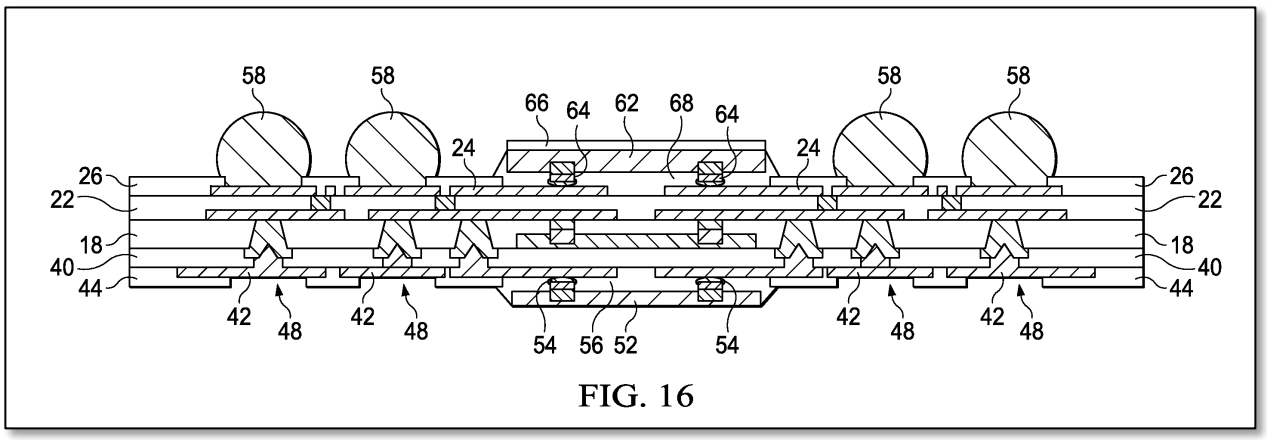


FIG. 16

EX1010, FIG. 16, 8:11-13, 4:67-5:7, 8:35-39 (describing relationship between FIGS. 16, 52); *EX1003*, ¶¶311-312.

2. 1(a)

Yu's package includes "molding compound 18 [that] can be an epoxy, polyimide, silicone rubber, the like, or a combination thereof," i.e., *a solid layer*. *EX1010*, 2:61-64. Molding compound 18 has *a first surface opposite to a second surface*:

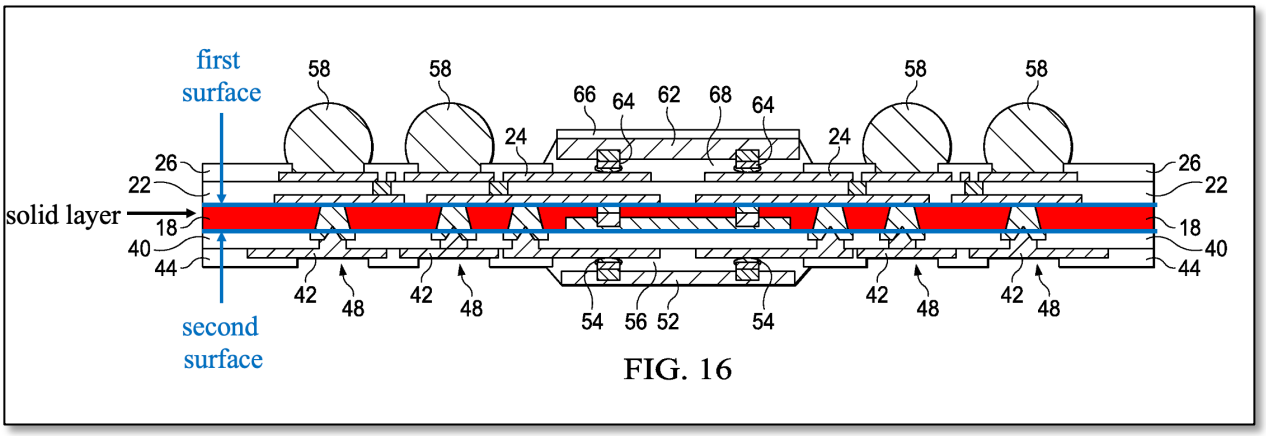


FIG. 16

EX1010, FIG. 16; *EX1003*, ¶¶313-314.

3. 1(a)(i)

Molding compound 18 comprises "epoxy, polyimide, silicone rubber, the like, or a combination thereof," such that silicone rubber alone or silicone rubber in combination with epoxy and/or polyimide teaches *a compound of silicon and oxygen*. *EX1010*, 2:61-65; *EX1003*, ¶315.

4. 1(a)(ii)

a) Lin-191's Teachings

Lin-191 teaches or renders obvious Claim 1(a)(ii).

Lin-191's package includes an "encapsulating layer 85" formed "on…metal pillars or bumps 14" (analogous to Yu's through mold vias (TMVs), discussed further at Claim 1(b))." *EX1005*, [0109]. Layer 85 includes "a polymer layer" such that layer 85 is a *solid layer*, similar to Yu's molding compound 18. *Id*. Encapsulating layer 85 has a thickness "between about 20 and about 500 micrometers, and preferably between 30 and 100 micrometers." *EX1005*, [0109-0111]; *EX1003*, ¶317. Because Lin-191 teaches a range (20-500 micrometers) that includes the narrower claimed range of *between 50 and 150 micrometers*, and a range (30-100 micrometers) that overlaps the claimed range, Lin-191 teaches or renders obvious Claim 1(a)(ii). *See* Section V.A.4 (supporting caselaw and discussion of '306 Patent not ascribing criticality to Claim 1(a)(ii)'s range); *EX1003*, ¶319.

Additionally or alternatively, layer 85 has a *thickness* equivalent to the combined thickness of layers 1 and bump 14 because layer 85 is "formed…on the metal layer 13 of the patterned metal layer 1," and "top surfaces 14a" of bumps 14 are "substantially coplanar…with a top surface 85a" of layer 85. *EX1005*, [0109-0110], FIG. 12; *EX1003*, ¶318. Lin-191 teaches bumps 14 are "between 20 and 110 micrometers"; layer 11 is "between 1 nanometer and 0.5 micrometers"; layer 12 is "between 10 nanometers and 0.8 micrometers"; and layer 13 is "between 3 and 10 micrometers." *EX1005*, [0121], [0050], [0060]. Thus, Lin-191 teaches layer 85 has

a *thickness* between 23.011 micrometers and 121.3 micrometers, overlapping with and teaching or rendering obvious the claimed *thickness*. *EX1003*, ¶318.

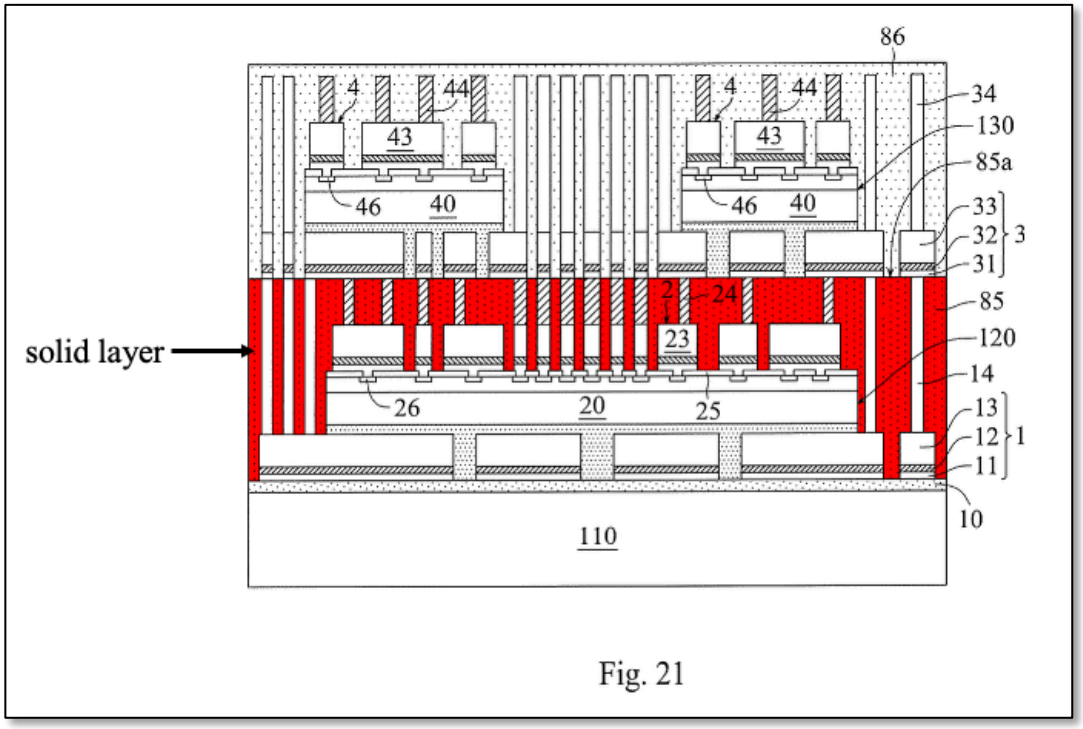


Fig. 21

EX1005, FIG. 12.

b) MTC

A POSITA would have been motivated and found obvious to apply Lin-191's thickness to Yu's molding compound 18. The modification would have provided the advantage of stress buffering, which would have been beneficial in Yu's package for protecting Yu's die 10 embedded in molding compound 18, as Lin-191's thickness was known to be appropriate for embedded chip architecture. *EX1003*, ¶¶320-321. Additionally, Lin-191's thickness would allow for the opportunity to incorporate shielding layers, which a POSITA would have found desirable. *EX1003*, ¶322.

The Yu-Lin-191 combination is the application of a known technique to a known device ready for improvement to yield predictable results. *EX1003*, ¶323. A POSITA would have had a REOS because Lin-191's thickness was a common thickness for molding/encapsulation layers before the '306 Patent. *EX1003*, ¶323.

5. 1(a)(iii)

Molding compound 18 includes *a first region* and *a second region between said first region and a first edge of said solid layer* as shown:

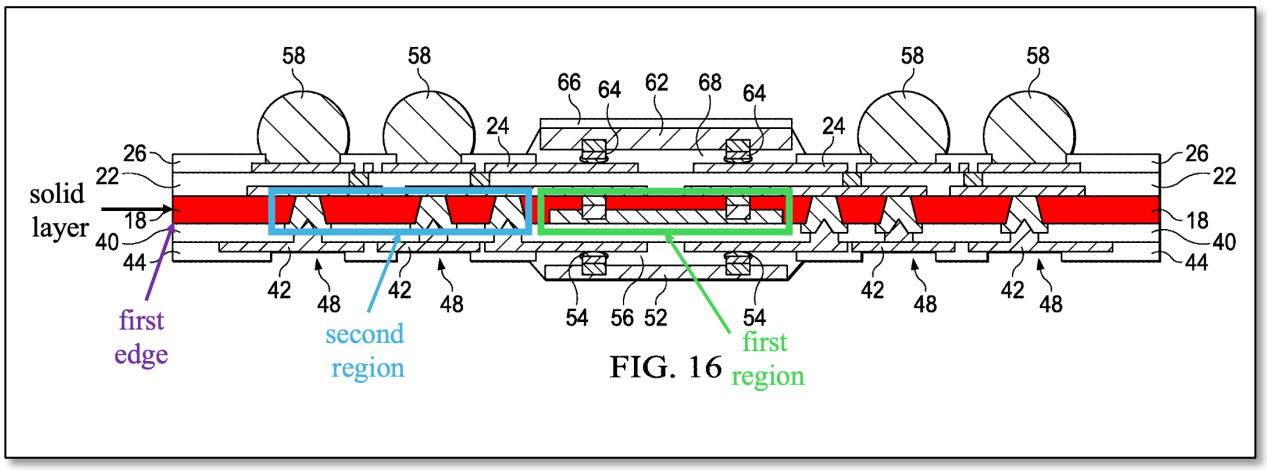


FIG. 16

EX1010, FIG. 16; *EX1003*, ¶324.

6. 1(b)

Yu teaches metal TMVs 38, which are *a plurality of metal post*s. Per Yu, "TMV openings 36 are formed through the molding compound 18," and a "seed layer is deposited…into the TMV openings 36," followed by deposition of a "conductive material," which forms TMVs 38. *EX1010*, 3:56-4:6. Both the seed layer and the conductive material are "copper." *Id*. Thus, TMVs 38 are *a plurality*

of metal posts in a plurality of through holes (TMV openings 36), which are *in said second region*, as shown:

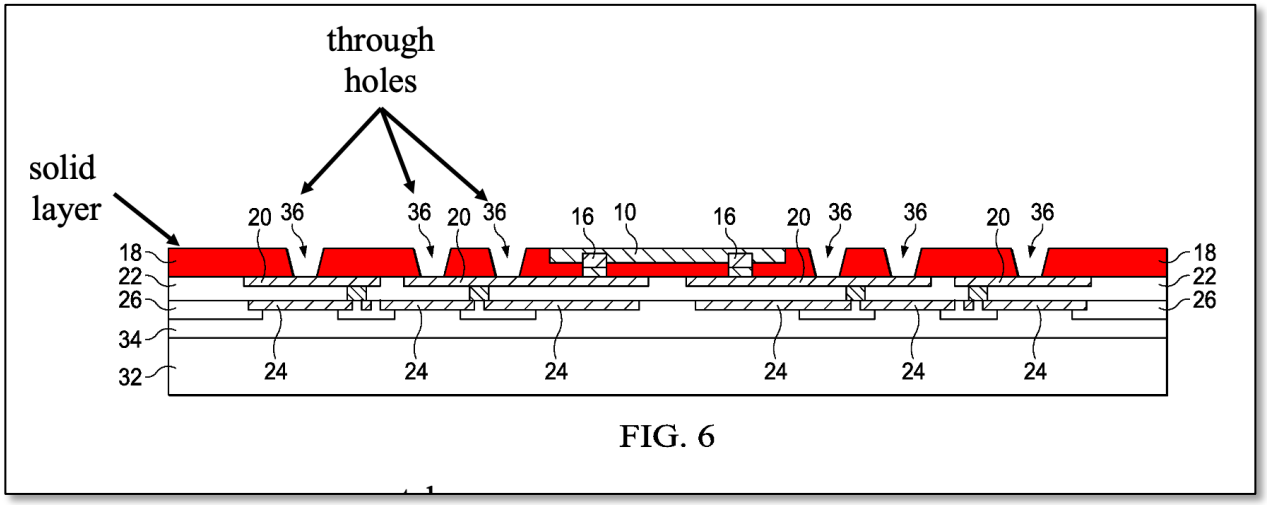


FIG. 6

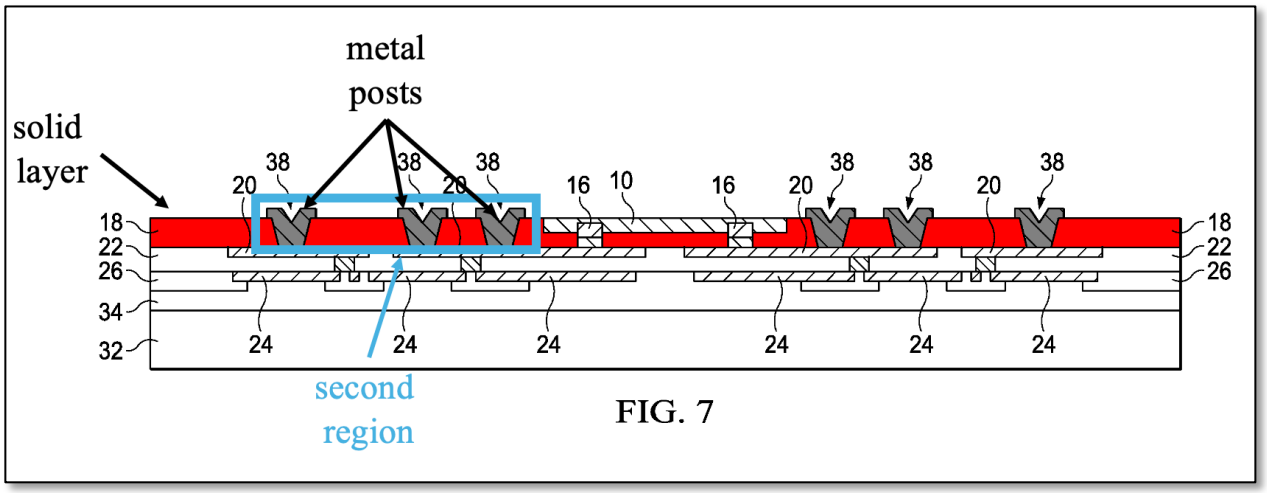
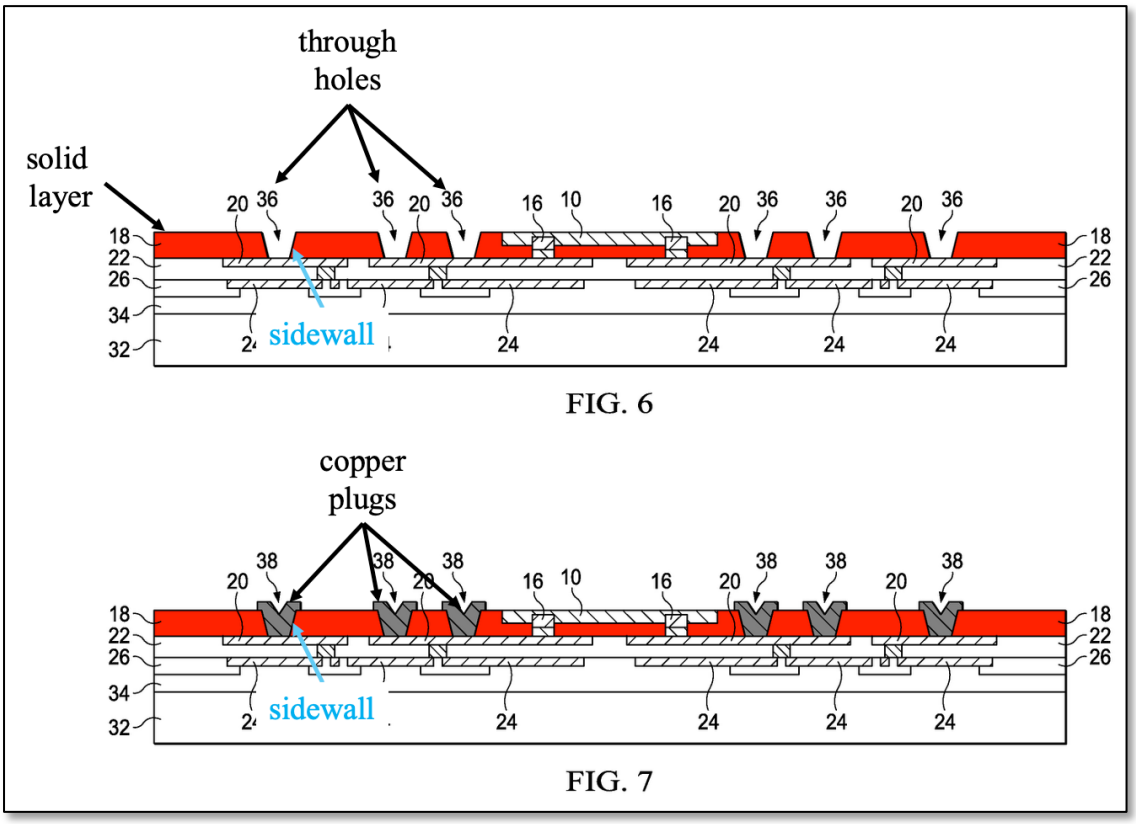


FIG. 7

EX1010, FIGS. 6-7; *EX1003*, ¶325.

7. 1(b)(i)

TMV 38's copper seed layer "deposited…into the TMV opening[] 36" is *a first copper layer contacting a sidewall of one of said plurality of through holes*. *EX1010*, 3:60-64.



EX1010, FIGS. 6-7; *EX1003*, 326.

8. 1(b)(ii)

Shown in FIG. 16, below, Yu's *first region has a width in a direction* (denoted D1) *greater than a shortest distance between said sidewall of one of said plurality of through holes and said first edge in said direction* (denoted D2), and *greater than a pitch between two neighboring metal posts* (denoted D3).

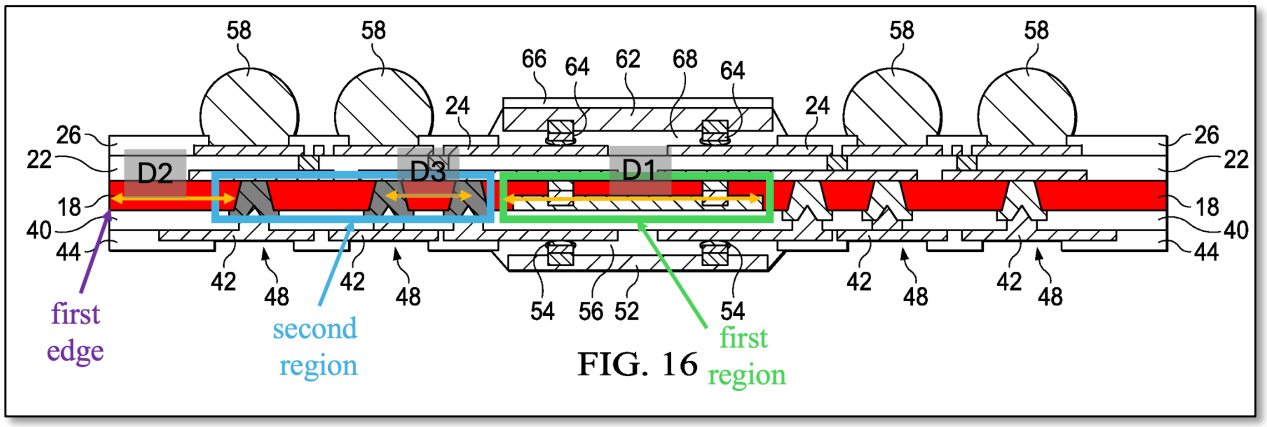


FIG. 16

EX1010, FIG. 16; *EX1003*, ¶328; *see* cited caselaw in Section V.A.8.

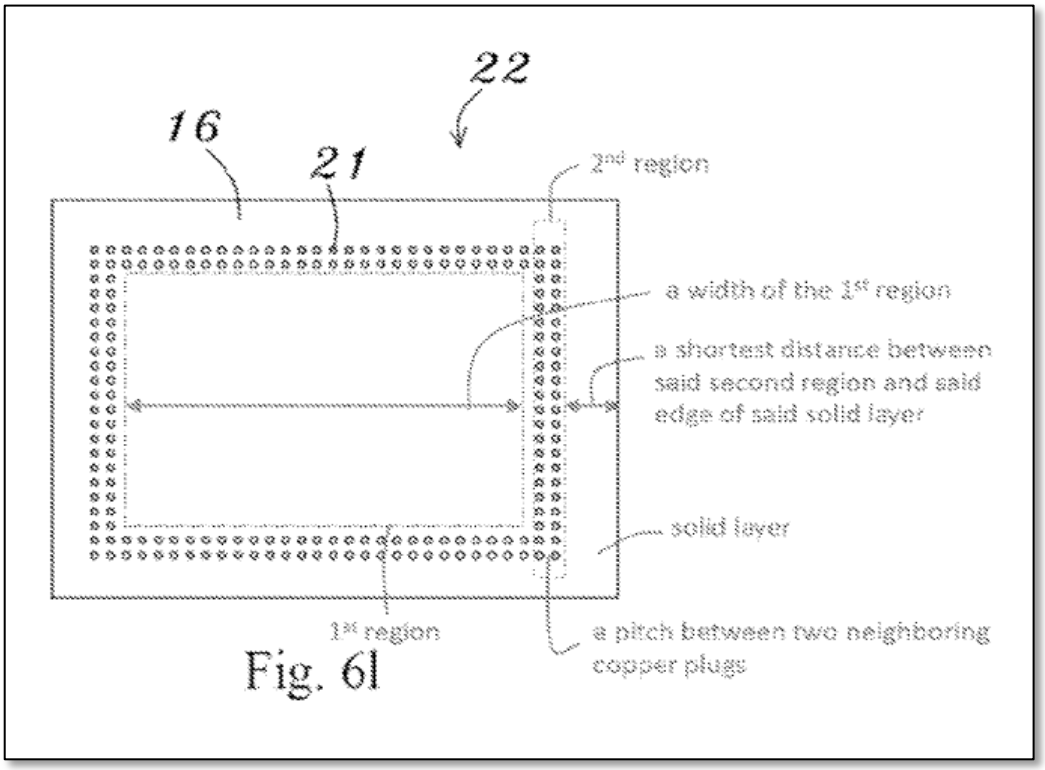


Fig. 6I

EX1117, 272[9]; *EX1003*, ¶329.

[9] Annotated figure PO argued supports language similar to Claim 1(b)(ii).

9. 1(c)

Yu teaches a "front side interlayer dielectric (ILD) and redistribution layer (RDL) structure" that are collectively *a first interconnection scheme over said first surface* because the structure "electrically couple[s]" components in Yu's *package*. *EX1010*, 3:4-15. The ILD/RDL structure includes a "first front side metallization layer 20," a "first ILD layer 22," and "[s]ubsequent metallization layers and ILD layers" including "a second metallization layer 24 and a second ILD layer 26." *EX1010*, 3:16-32, FIGS. 4, 7 (describing and showing the formation of layer 20).

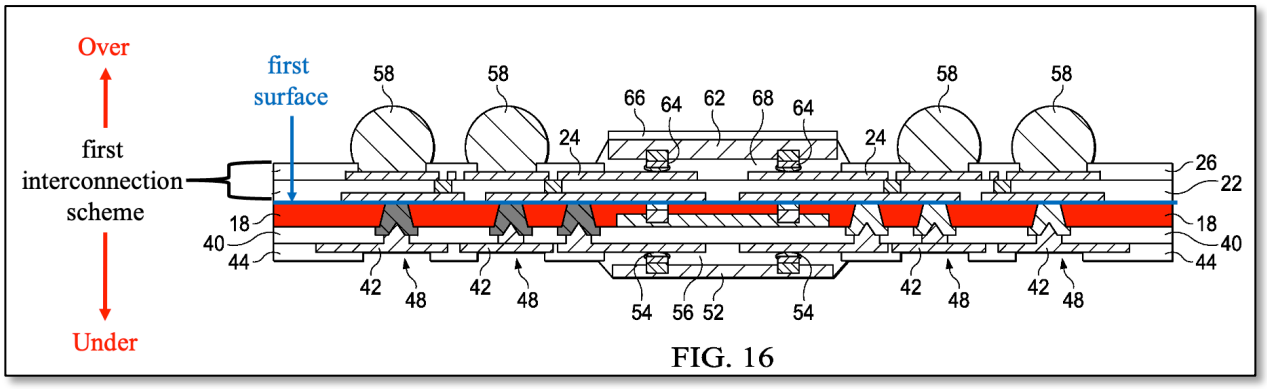


FIG. 16

EX1010, FIG. 16; *EX1003*, ¶330; *see* Section V.A.9, footnote 3.

10. 1(c)(i)

Metallization layer 20 comprises "copper," and a portion of layer 20 is, therefore, *a first metal interconnect* and is *over said second surface* as shown below. *EX1010*, 3:11-19. ILD layer 22, which comprises "a polyimide," is *a polymer layer* and is *over* metallization layer 20:

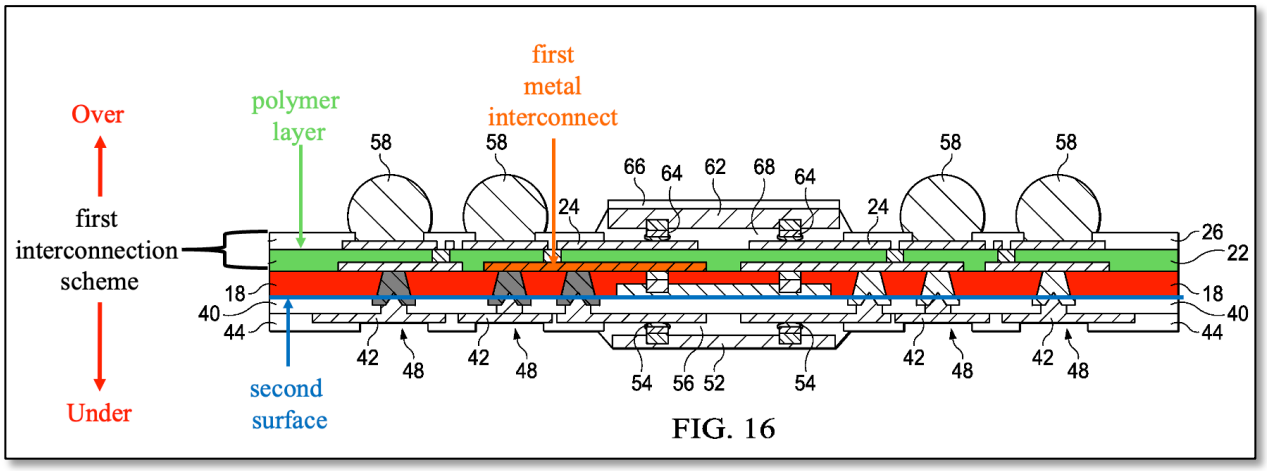


FIG. 16

EX1010, FIG. 16, 3:21-23; *EX1003*, ¶¶331-333.

11. 1(c)(ii)

Yu's *first metal interconnect is connected to a first metal post* as "TMV openings 36 are formed through the molding compound 18 to the first front side metallization layer 20," followed by formation of TMVs 38 via electroplating. *EX1010*, 3:56-4:6, FIGS. 6-7.

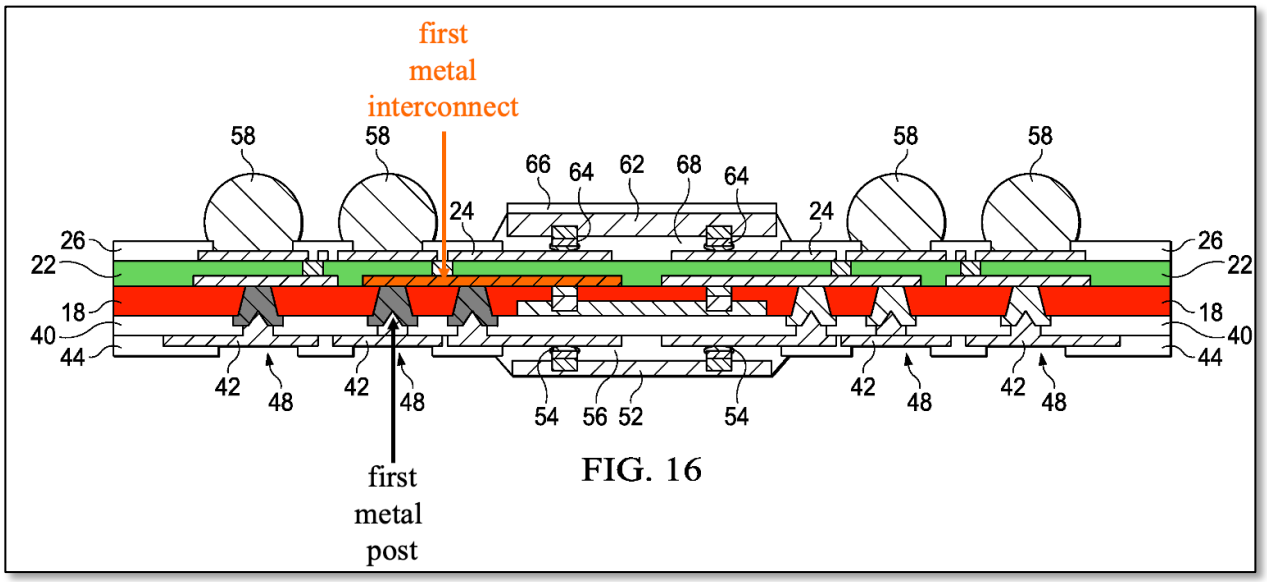


FIG. 16

EX1010, FIG. 16; *EX1003*, ¶334.

12. 1(c)(iii)

Yu teaches metallization layer 20 includes a "seed layer, such as copper…deposited on the molding compound 18," and a "[c]onductive material…such as copper…is deposited on the seed layer." *EX1010*, 3:5-19. Thus, metallization layer 20's copper "seed layer" is *a first metal layer*, and the copper "conductive material" deposited on the seed layer is *a second copper layer over* the copper seed layer. *EX1003*, ¶335.

13. 1(d)

Yu teaches "conductive connectors 58, such as ball grid array (BGA) balls" are formed "on the front side of the package in the openings 28" and "formed on [] bond pads." *EX1010*, 4:45-49. Connector 58 and its bond pad collectively form *a first metal bump*.

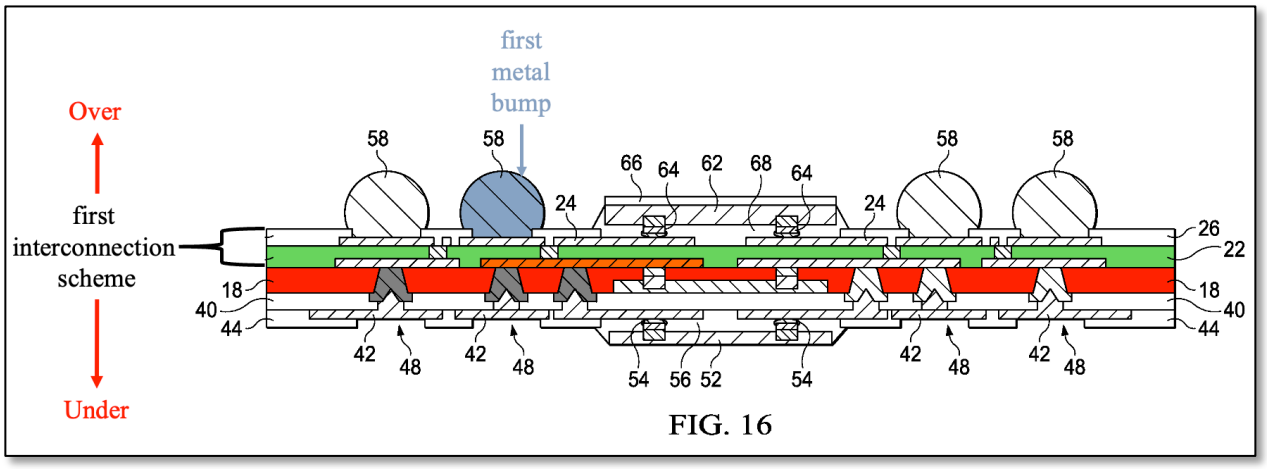


FIG. 16

EX1010, FIG. 16; *EX1003*, ¶¶336-337.

14. 1(d)(i)

Yu teaches "connector[] 58 may be formed on the bond pad[]" and "connectors 58 may be [] lead-free solder." *EX1010*, 4:47-50. A POSITA would have understood (A) the bond pad to be *metal* because bond pads were (and remain) ubiquitously *metal* for interconnecting solder balls in chip packages, and (B) lead-free solder to include *tin*. *EX1003*, ¶¶338-339. Thus, Yu teaches *a second metal layer* (the bond pad) *and a first tin-containing layer* (lead-free solder) *over said second metal layer* because the solder connector is on (*over*) the bond pad. *EX1003*, ¶340.

a) Lin-191's Teachings and MTC

Additionally, or alternatively, Lin-191 teaches Claim 1(d)(i). *See* Section V.A.14. A POSITA would have been motivated, found it obvious, and had a REOS in modifying Yu per Lin-191 for the reasons discussed for Sundaram-Lin-191. *Id.* The Yu-Lin-191 combination is application of known technique (Lin-191's solder bump structure) to a known device (Yu's connector and pad) ready for improvement to yield predictable results. *EX1003*, ¶341.

15. 1(e)

Yu's package includes "die 52, such as a memory die," which is *a first semiconductor chip under said second surface*. *EX1010*, 4:30-36.

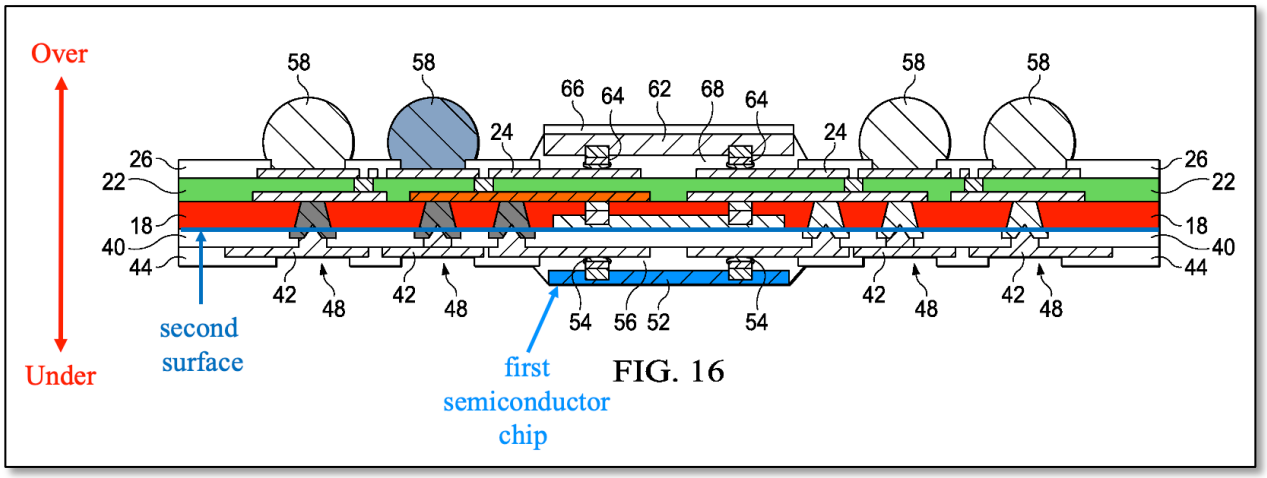


FIG. 16

EX1010, FIG. 16; *EX1003*, ¶342.

16. 1(e)(i)

A second metallization layer 20 portion is *a second metal interconnect*, which is *over* a sidewall of die 52 because it is positioned on the opposite side of molding compound 18 (*over*) from die 52's *sidewall*. Additionally, metallization layer 20 comprises a portion extending laterally beyond the *sidewall*; thus, metallization layer 20 is *across* the *sidewall*.

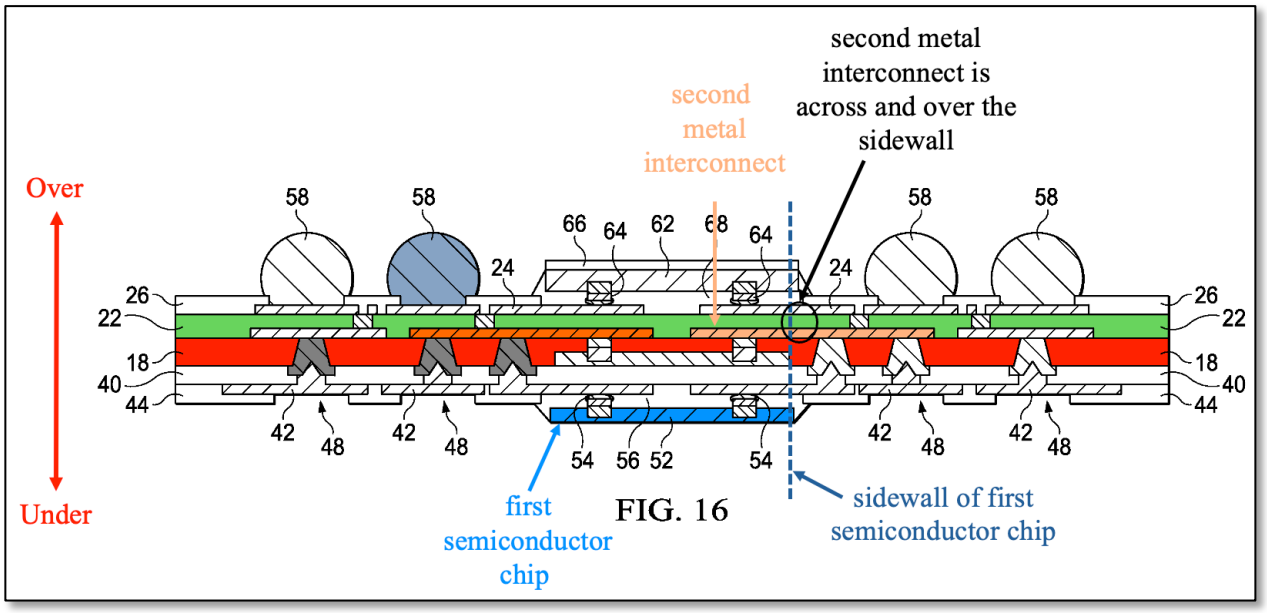
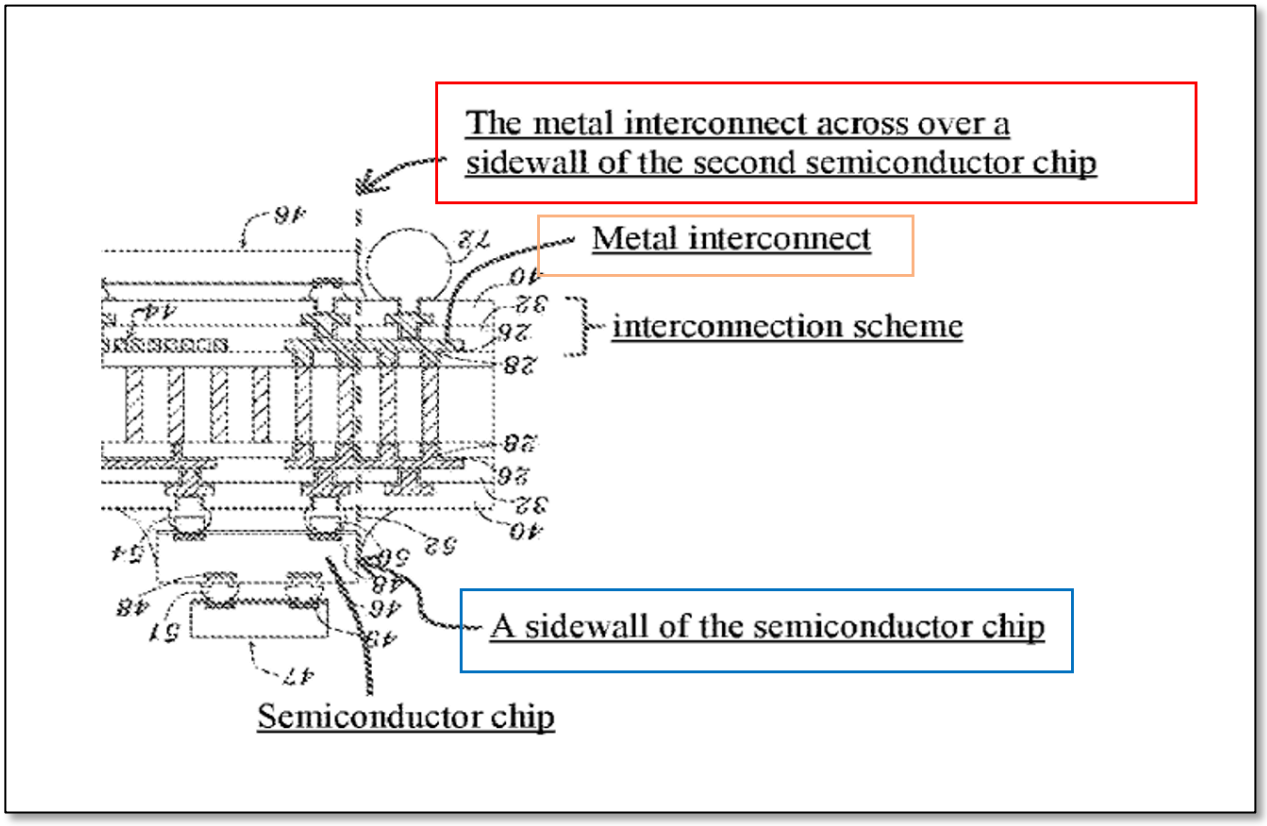


FIG. 16

EX1010, FIG. 16; *EX1003*, ¶343; *see* caselaw cited in Section V.A.8.

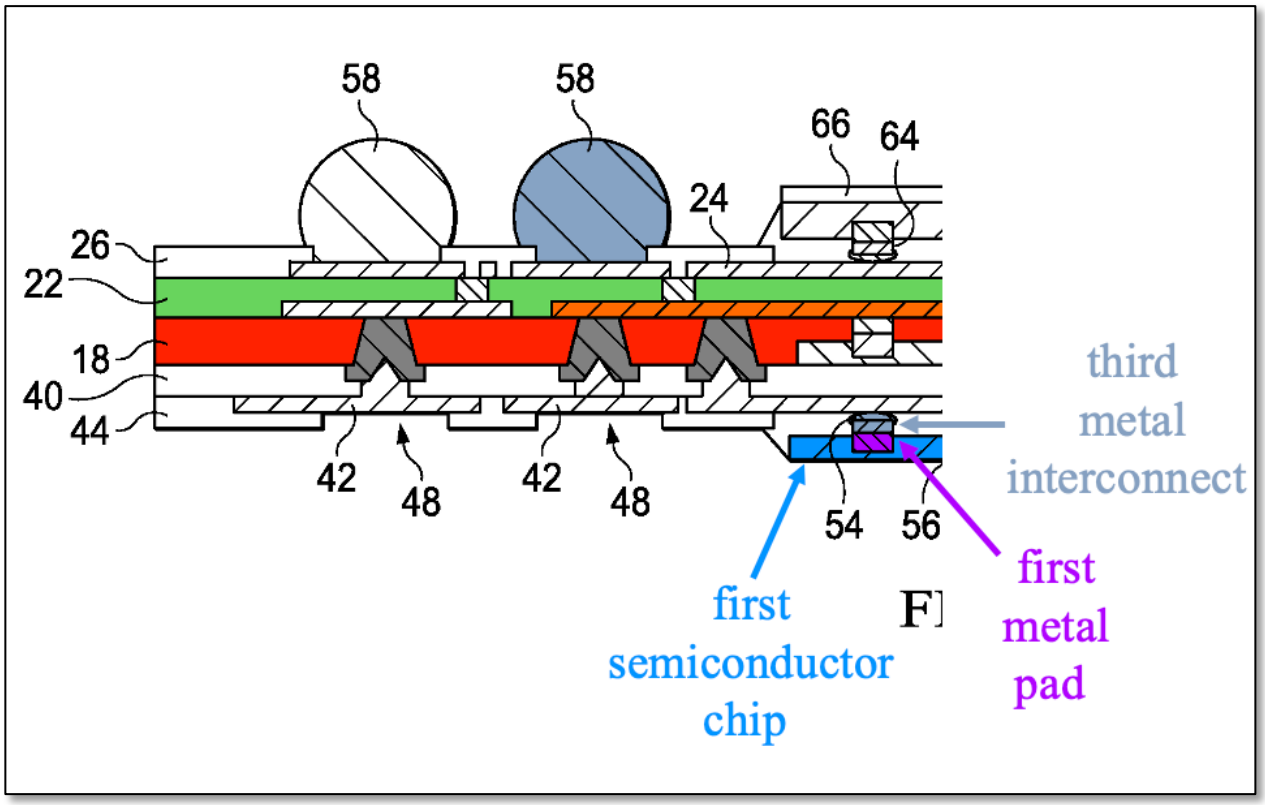


EX1032, 537[10]; *EX1003*, ¶344.

17. 1(e)(ii)

Die 52 is "attached…to conductive features in the second back side metallization layer 42, such as by conductive connectors 54, like controlled collapse chip connection (C4) bumps." *EX1010*, 4:30-34. A connector 54 is a *third metal interconnect* because it connects die 52 "to conductive features" in layer 42. Id. Further, a POSITA would have understood die 52 includes die pads (unlabeled) such that an electrical connection is made between die 52 and other devices (e.g., die 62), thus teaching the *first metal pad of said first semiconductor chip*. *EX1003*, ¶¶345-347; *EX1129*, 1:9-26. As shown below, connector 54 is *on* the die pad of die 52.

[10] Annotated figure PO argued supports language similar to Claim 1(e)(i).



EX1010, FIG. 16 (excerpt); *EX1003*, ¶¶347-348.

a) Lin-191's "Metal Pad" Teachings and MTC

Additionally, or alternatively, to Yu, Lin-191 teaches *metal pads*. *See* Sections V.A.17.a-b. Lin-191 teaches an implementation detail of Yu's chip (a metal pad) such that there would have been a motivation and REOS. *EX1003,* ¶349. The combination is the application of known metal pad techniques to Yu's die 52 to yield the predictable result of die 52 having a *metal pad*. *EX1003*, ¶350.

18. 1(e)(iii)

Lin-191 teaches or renders obvious interconnects/bumps with layers/thickness as recited in Claim 1(e)(iii). *See* Section V.A.18. The '306 Patent

ascribes no criticality to the claimed *thickness*. *Id*. A POSITA would have found it obvious and been motivated to modify Yu's connector for the reasons discussed with respect to Sundaram, i.e., improved metallurgical bonding and increased resistance to fatigue and stress-induced failure. *EX1003*, ¶¶351-352. Layered bumps, per Lin-191, were routinely manufactured using techniques contemplated by Yu, leading to a REOS. *Compare EX1005*, [0400] *with EX1010*, 3:11-14; *EX1003*, ¶¶351-352.

19. 1(e)(iv)

Die 52 *is connected* to a second TMV 38 (*second metal post*) *through* connector 54 and a portion of "second back side metallization layer 42." *EX1010*, 4:7-11.

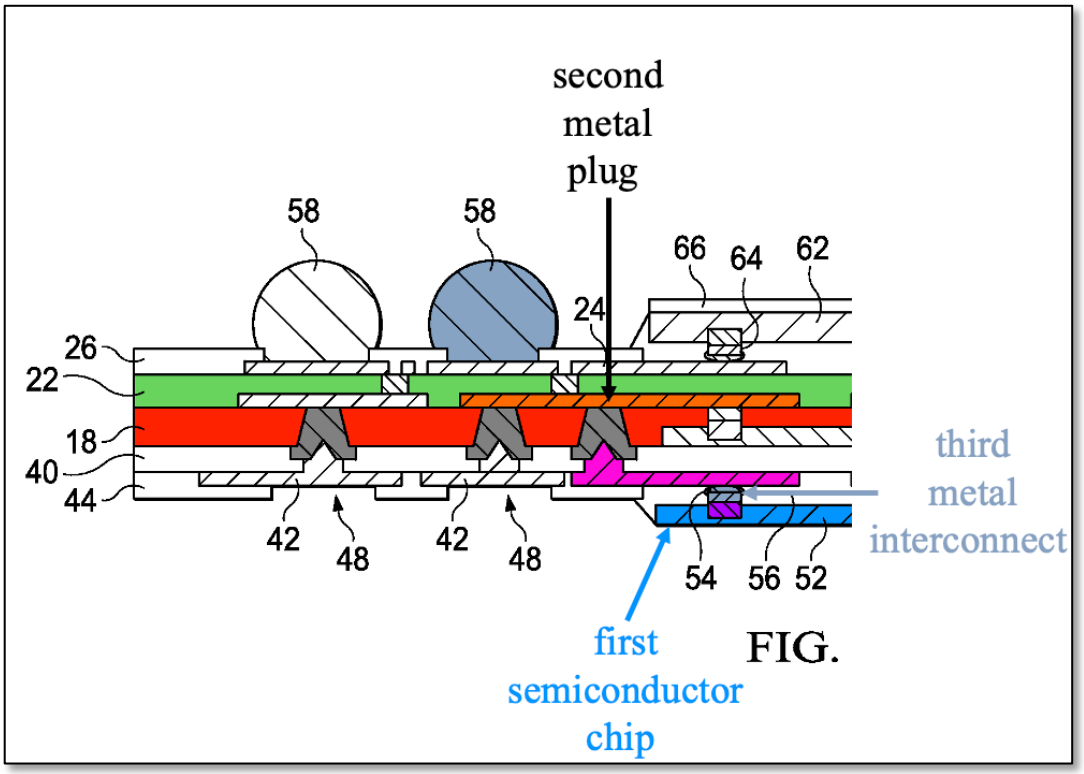


FIG.

EX1010, FIG. 16 (excerpt); *EX1003*, ¶¶353-354.

B. Claim 2

Lin-191 teaches Claim 2. See Section V.B.a. The same MTCs and REOS for modifying Sundaram per Lin-191 apply to modifying Yu per Lin-191, e.g., increasing the functionality of Yu's chip package. *See* Section V.B.b. Further evidencing the motivation and REOS, Yu teaches dies can be "logic circuitry die, a memory die, or any other die." *EX1010*, 2:50-51; *EX1003*, ¶¶355-356.

C. Claim 3

1. 3(a)

A portion of Yu's "second metallization layer 24" is *a fourth metal interconnect over* first metallization layer 20 and ILD layer 22. *EX1010*, 3:28-32; *see* Section VII.A.10.

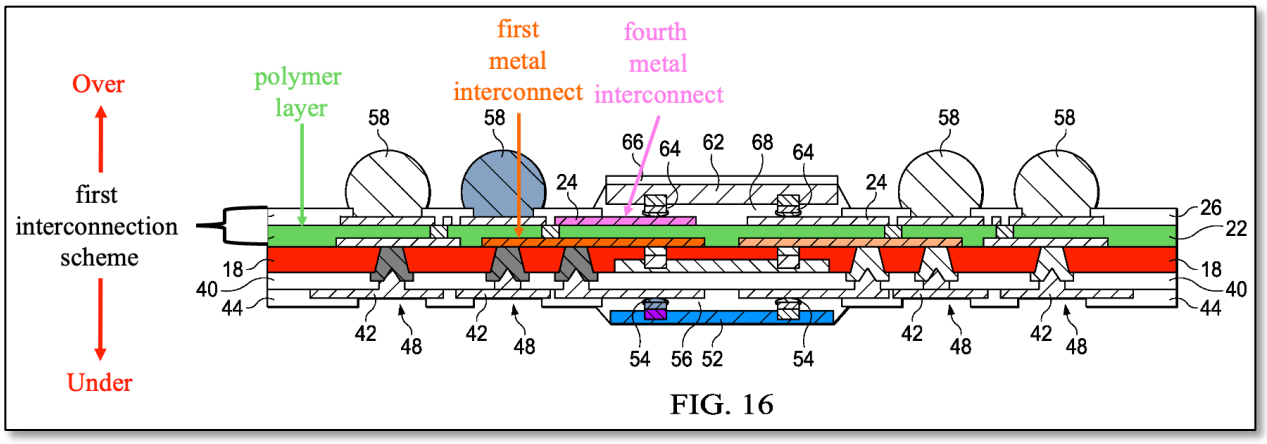


FIG. 16

EX1010, FIG. 16; *EX1003*, ¶¶357-358.

2. 3(b)

Metallization layer 24 is on (over) ILD layer 22, which is "over the first metallization layer 20" such that ILD layer 22 *is between* layers 20, 24. *EX1010*, 3:20-32.

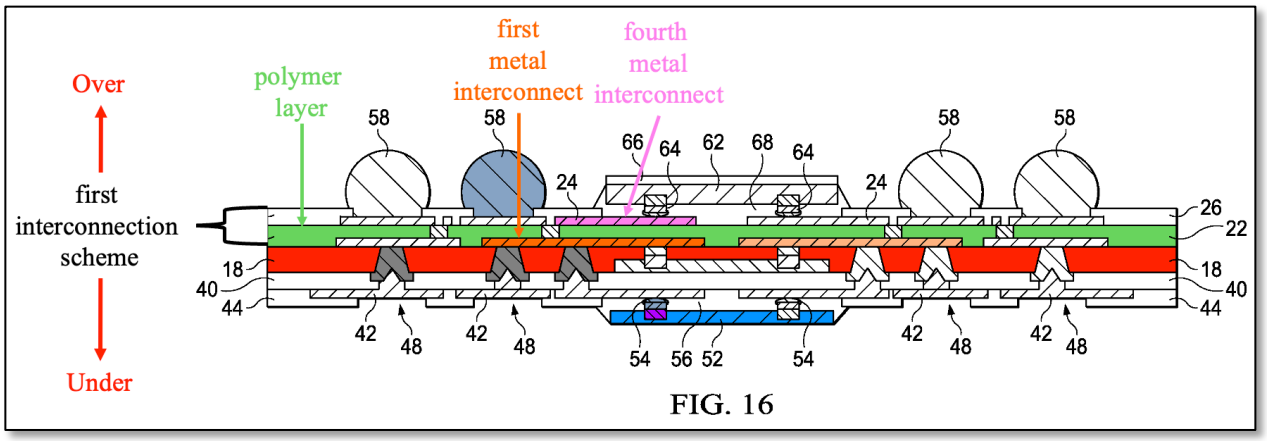


FIG. 16

EX1010, FIG. 16; *EX1003*, ¶359.

3. 3(c)

Metallization layer 24 is "formed using the same or similar processes as…first metallization layer 20" such that layer 24, like layer 20, *comprises a fourth metal layer* (copper seed layer) *and a fourth copper layer over said fourth metal layer* (electroplated copper layer). *EX1010*, 3:28-32, 3:5-18; *see* Section VII.A.12; *EX1003*, ¶360.

D. Claim 4

See Sections VII.A.17 (mapping the *first metal pad*), V.D (MTCs and REOS incorporated).

E. Claim 5

a) Lin-191's Teachings

Lin-191's *solid layer* includes encapsulating layer 85 (discussed at Claim 1(a)(ii)) and further includes an insulating layer 10, which is made of "silicon dioxide (SiO_2)" and over which layer 85 is "formed." *EX1005*, [0052], [0109]; *see* Section VII.A.4.

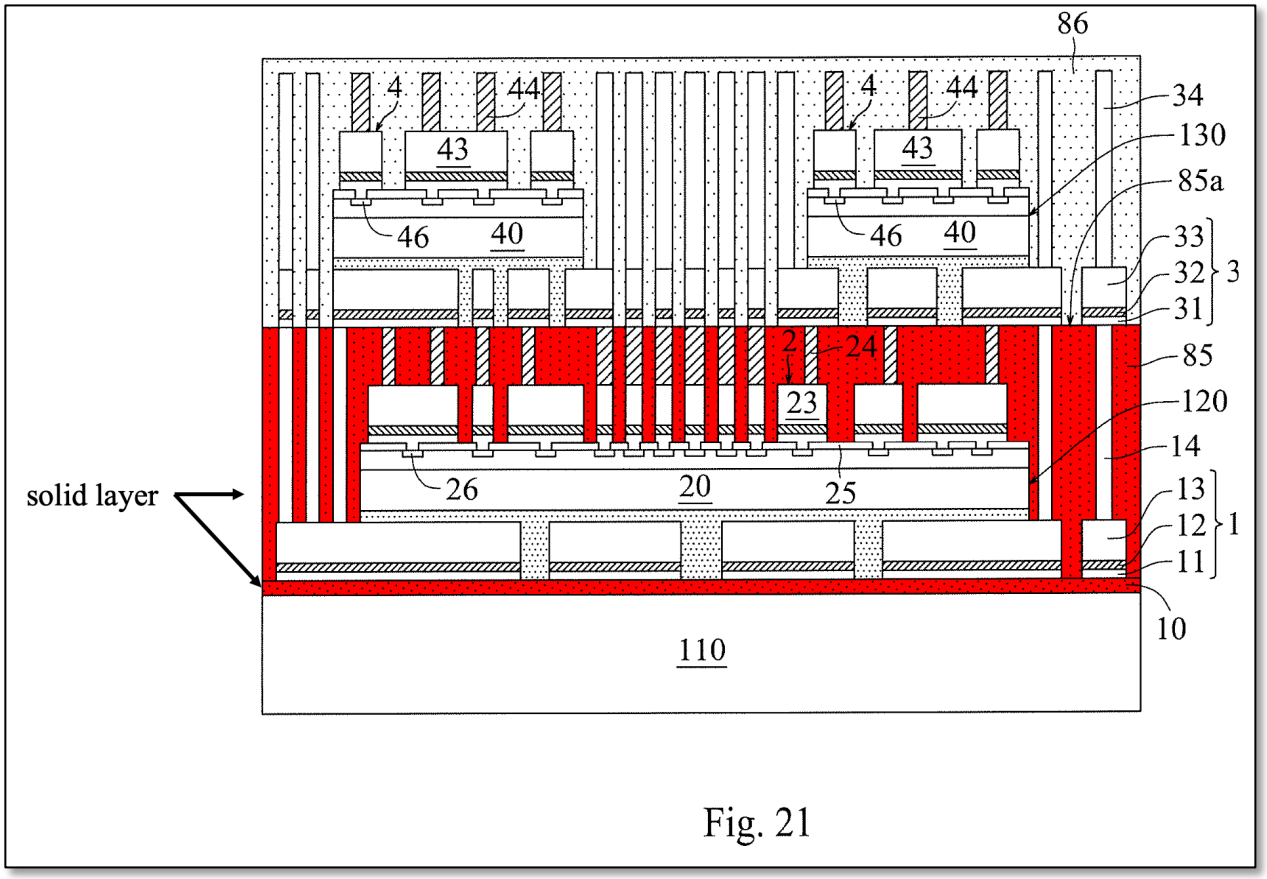


Fig. 21

EX1005, FIG. 21; *EX1003*, ¶362.

Yu teaches molding compound 18 comprises "epoxy, polyimide, silicone rubber, the like, or a combination thereof," i.e., *a compound of silicon and oxygen*. *EX1010*, 2:61-65; *see* Section VII.A.3. Lin-191 teaches specifically SiO_2. In the

combination, Yu is modified per Lin-191 such that *said compound* is the combination of Yu's molding compound 18 and Lin-191's insulating layer 10.

Because insulating layer 10 is SiO_2, the Yu-Lin-191 *compound comprises a SiO_2 compound*. *EX1003*, ¶363.

b) MTC

A POSITA would have been motivated and found it obvious to modify Yu to have an SiO_2 layer per Lin-191 such that Yu's *solid layer* (molding compound 18) is modified to include an SiO_2 layer similar to Lin-191's teachings of a *solid layer* comprising encapsulating layer 85 and insulating SiO_2 layer 10. *EX1003*, ¶364. A POSITA would have recognized the SiO_2 layer to advantageously improve Yu's package's water vapor permeability as an SiO_2 layer provides an improved water vapor barrier relative to only having a silicone rubber molding compound. *EX1003*, ¶366. Water vapor permeability is a common problem in die encapsulation as greater water presence leads to increased oxidation, corrosion, and enhanced ion-movement. *EX1003*, ¶366. Thus, the addition of an SiO_2 layer to Yu's package would reduce water vapor penetration, increasing the reliability of Yu's package. *EX1003*, ¶366. Further advantages result from the insulation provided by the SiO_2 layer. *EX1003*, 367. There would have been a REOS because Lin-191 teaches layer 10 is formed via "a chemical-vapor deposition (CVD) process, a spin-coating process or a lamination process," which are all techniques also disclosed by Yu, making the

modification simple and straightforward. *EX1005*, [0050]; *EX1010*, 7:16-18; *EX1003*, ¶368. The combination is the application of Lin-191's known SiO_2 layer technique to Yu's package ready for improvements to yield the predictable results of improved water vapor permeability and insulation. *EX1003*, ¶368.

F. Claim 6

1. 6(a)

Yu teaches a "die 62, such as a memory die…attached…to conductive features in the second front side metallization layer 24" such that die 62 is *a second semiconductor chip over* die 52. *EX1010*, 4:53-56. Like die 52, die 62 has C4 "connectors 64," i.e., *a second metal bump on a second metal pad*. *EX1010*, 4:56-60. *EX1003*, ¶¶369-370.

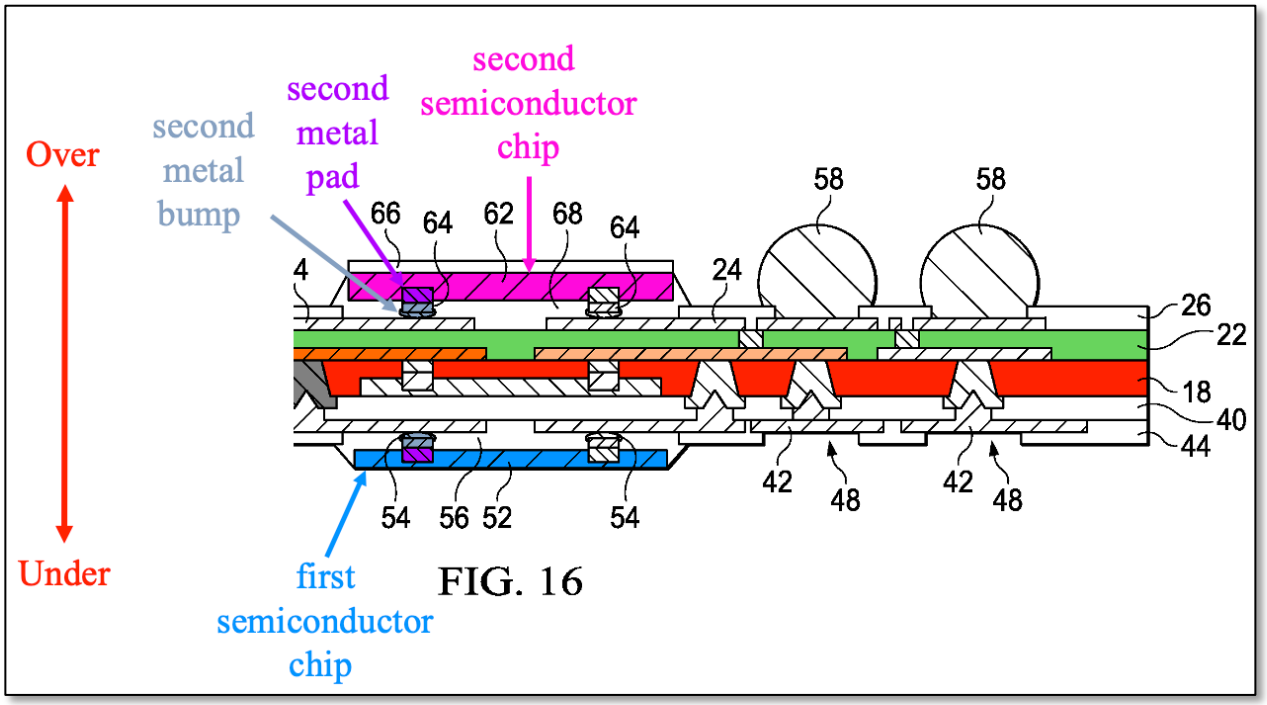


FIG. 16

EX1010, FIG. 16; *see* Section VII.A.17.

Additionally, or alternatively, Yu-Lin-191 teaches *a second metal bump on a second metal pad*. *See* Section VII.A.17, reciting corresponding limitations. *EX1003*, ¶371.

2. 6(b)

Yu alone or Yu-Lin-191 teaches this limitation. *See* Section VII.A.14.

G. Claim 7

Molding compound 18 includes *a third region opposite to said second region* and *between said first region and a second edge* of compound 18. The *third region* includes a *plurality of metal posts in said plurality of through holes*:

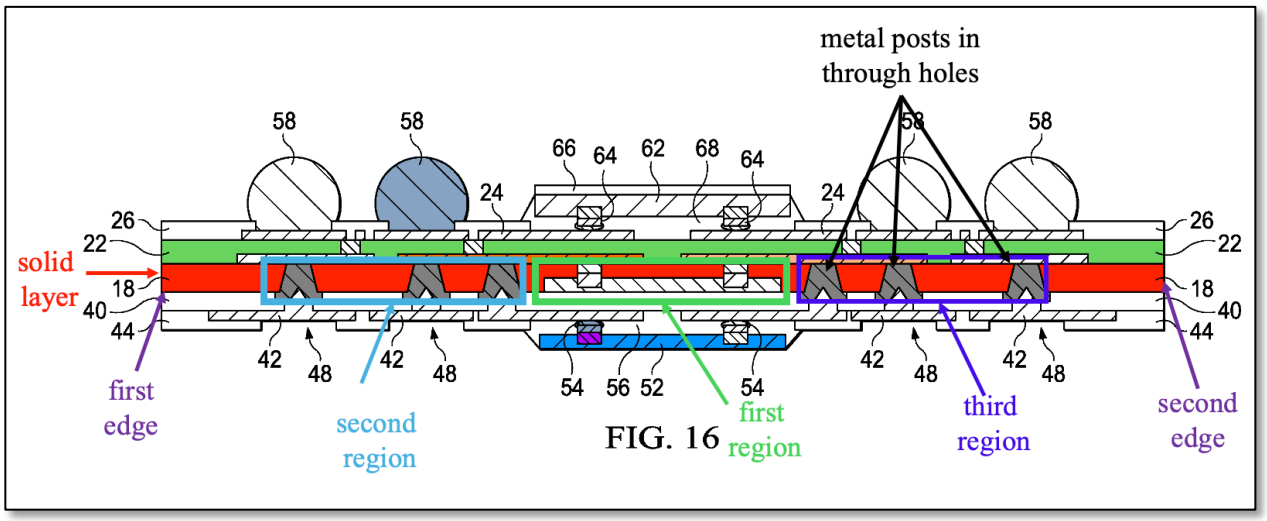


FIG. 16

EX1010, FIG. 16; *EX1003*, ¶373.

H. Claim 9

FIG. 16's package is part of FIG. 52's PoP structure (*chip package*). *See* Section VII.A.1. The PoP structure includes another package 202 below FIG. 16's

package 202, which includes another memory die 52, i.e., *another said first semiconductor chip under said second surface*. *EX1010*, 8:35-39 ("[M]ultiple packages 202…can be stacked in the PoP structure."), 8:11-12.

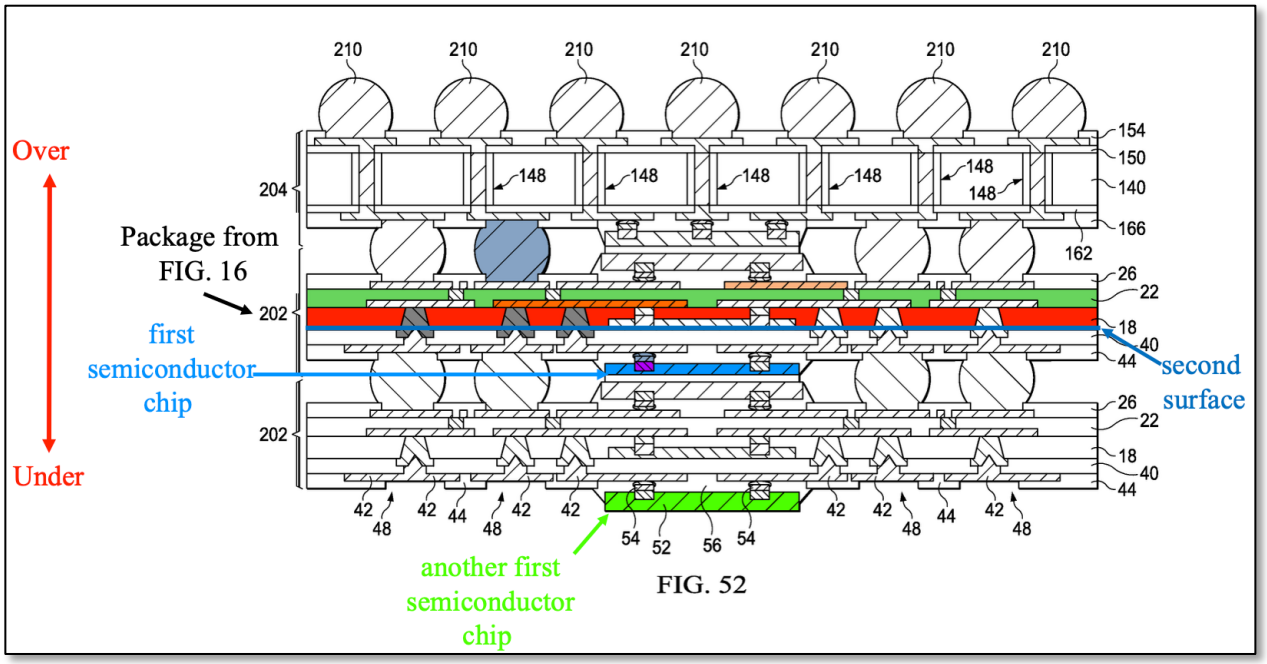


FIG. 52

EX1010, FIG. 52; *EX1003*, ¶379.

I. Claim 10:

1. 10(Pre)

See Section VII.A.1.

2. 10(a)

See Section VII.A.2. Claim 10's mapping reverses Yu's mapped *first* and *second surfaces* and *over/under* directions relative to Claims 1's mapping.

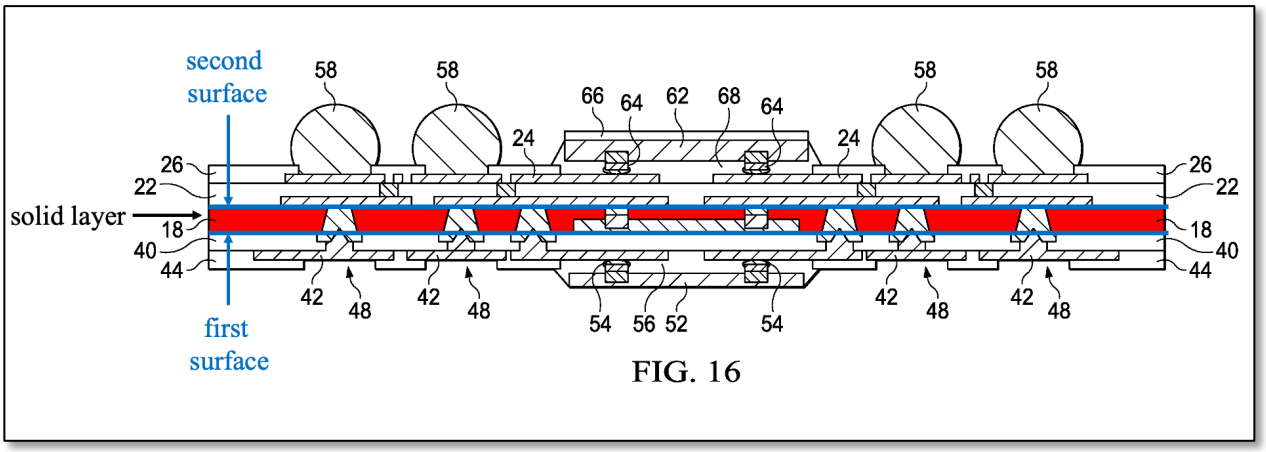


FIG. 16

EX1010, FIG. 16; *EX1003*, ¶376.

3. 10(a)(i)

See Section VII.A.3.

4. 10(a)(ii)

See Section VII.A.4. Lin-191 teaches or renders obvious Claim 10(a)(ii). Lin-191's encapsulating layer 85 is "between about 20 and about 500 micrometers," and the combined height of bumps 14 and layer 1 is between 23.011 micrometers and 121.3 micrometers; both ranges overlap the claimed *thickness* range, teaching or rendering obvious Claim 10(a)(ii). *EX1005*, [0109]; *EX1003*, ¶378; Section V.I.4 (no criticality of claimed *thickness*).

5. 10)(a)(iii)

See Section VII.A.5.

6. 10(b)

See Section VII.A.6. TMVs 38 comprise "copper" such that TMVs 38 are *copper posts*. *EX1010*, 3:60-4:6; *EX1003*, ¶380.

7. 10(b)(i)

See Section VII.A.8.

8. 10(c)

See Section VII.A.9. Yu teaches "a back side ILD and RDL structure" with a "first back side ILD layer 40, a second back side metallization layer 42, [and] a second ILD layer 44[.]" *EX1010*, 4:7-11. Thus, the back side ILD and RDL structure is *a first interconnection scheme over said first surface*.

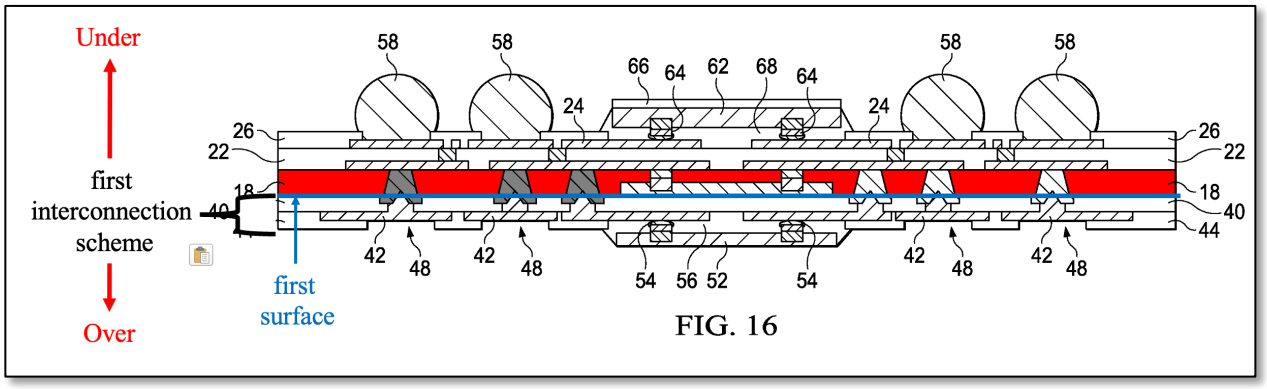


FIG. 16

EX1010, FIG. 16; *EX1003*, ¶382.

9. 10(c)(i)

A portion of metallization layer 42 is *a first metal interconnect over said first surface* and ILD layer 44 is *a polymer layer over* layer 42, both layers 42, 44 are "formed the similar to or in the same manner as the ILD layers and metallization layers on the front side." *EX1010*, 4:7-14; *see* Section VII.A.10.

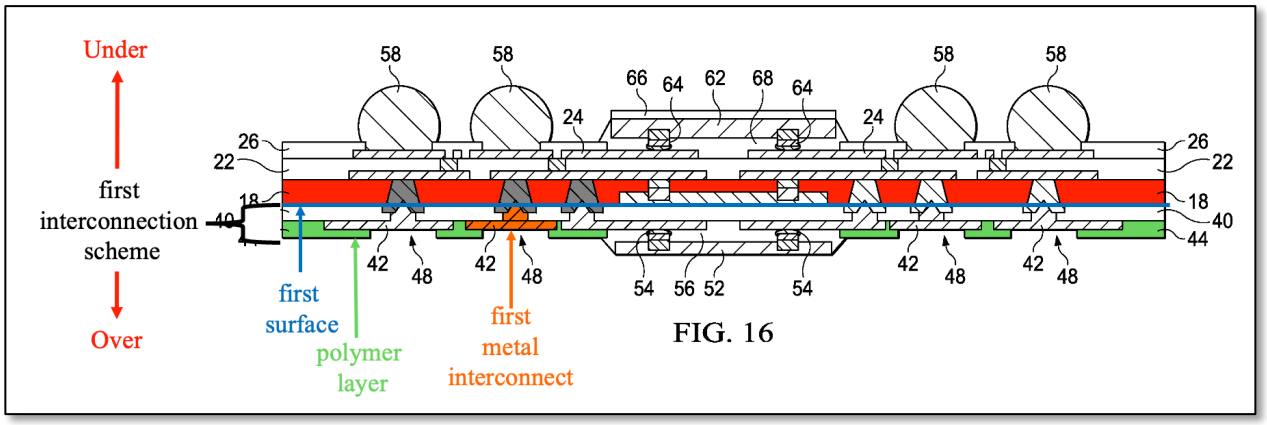


FIG. 16

EX1010, FIG. 16; *EX1003*, ¶383.

10. 10(c)(ii)

Layer 42 is connected to a TMV 38. *See* Section VII.A.11.

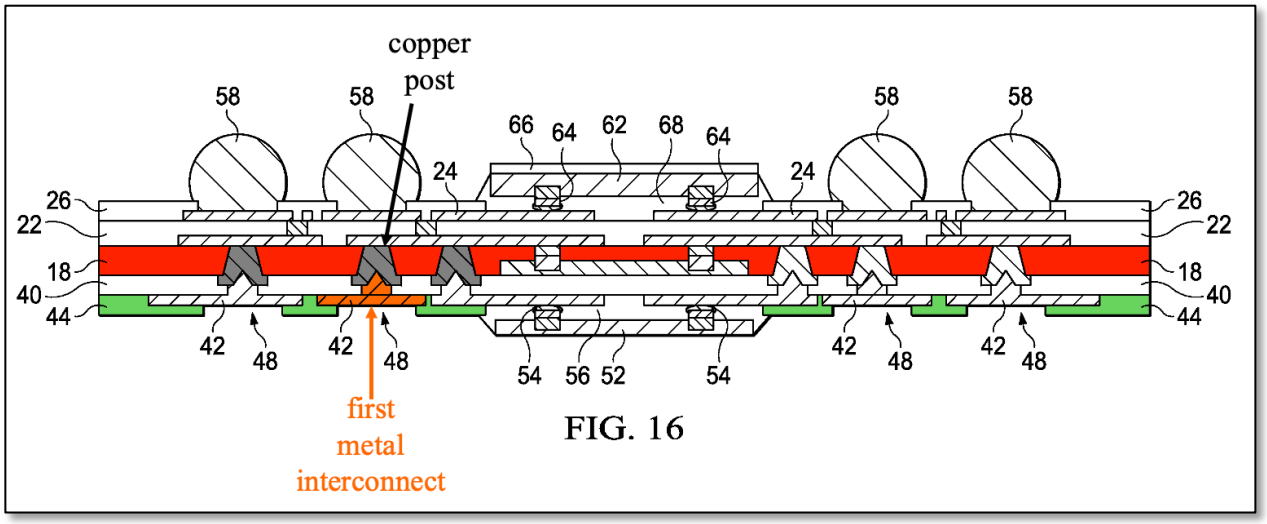


FIG. 16

EX1010, FIG. 16; *EX1003*, ¶384.

11. 10(c)(iii)

Layer 42 is "formed the similar to or in the same manner as the…metallization layers on the front side' such that layer 42 has *a first metal layer and a first copper*

layer over said first metal layer. *EX1010*, 4:7-14; *see* Section VII.A.12; *EX1003*, ¶385.

12. 10(d)

See Section VII.A.13. FIG. 52's PoP includes *a first metal bump over said first interconnection scheme*. *EX1010*, 4:45-49, FIG. 13 (teaching connectors 58 in openings 28 of layer 26).

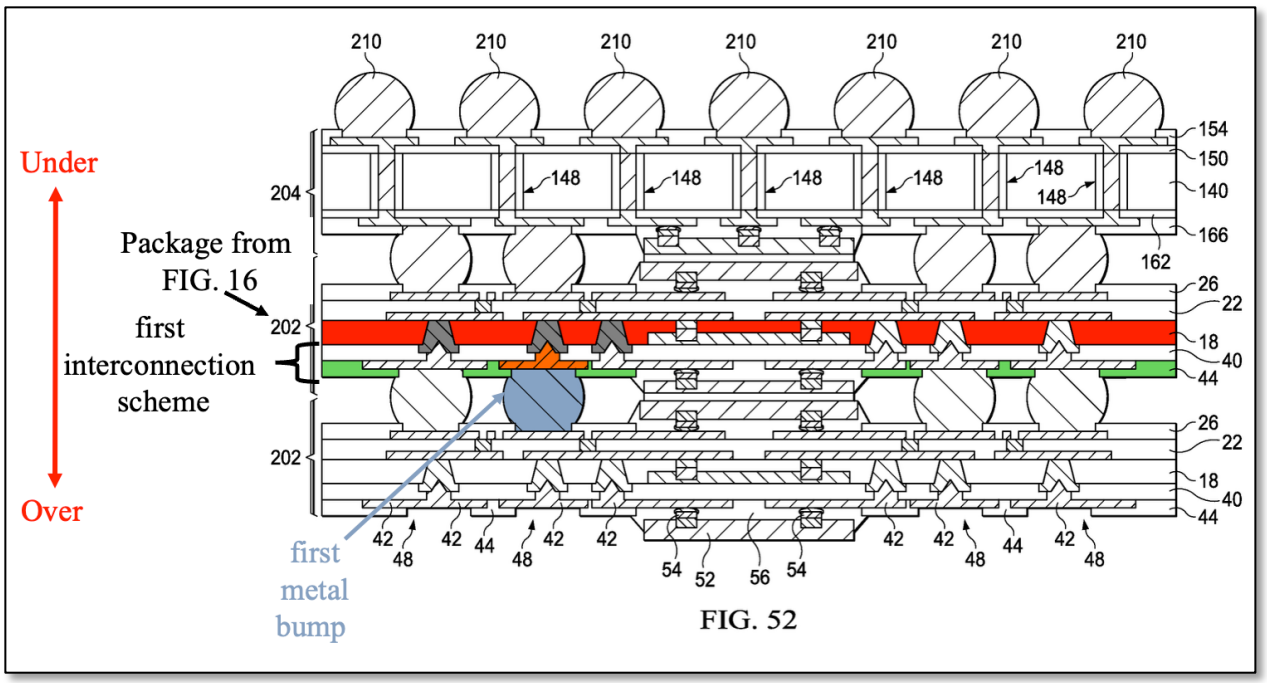


FIG. 52

EX1010, FIG. 52; *EX1003*, 386.

13. 10(d)(i)

See Section VII.A.14.

14. 10(e)

Another connector 58 is *a second metal bump over said first interconnection scheme*. *See* Section VII.I.12.

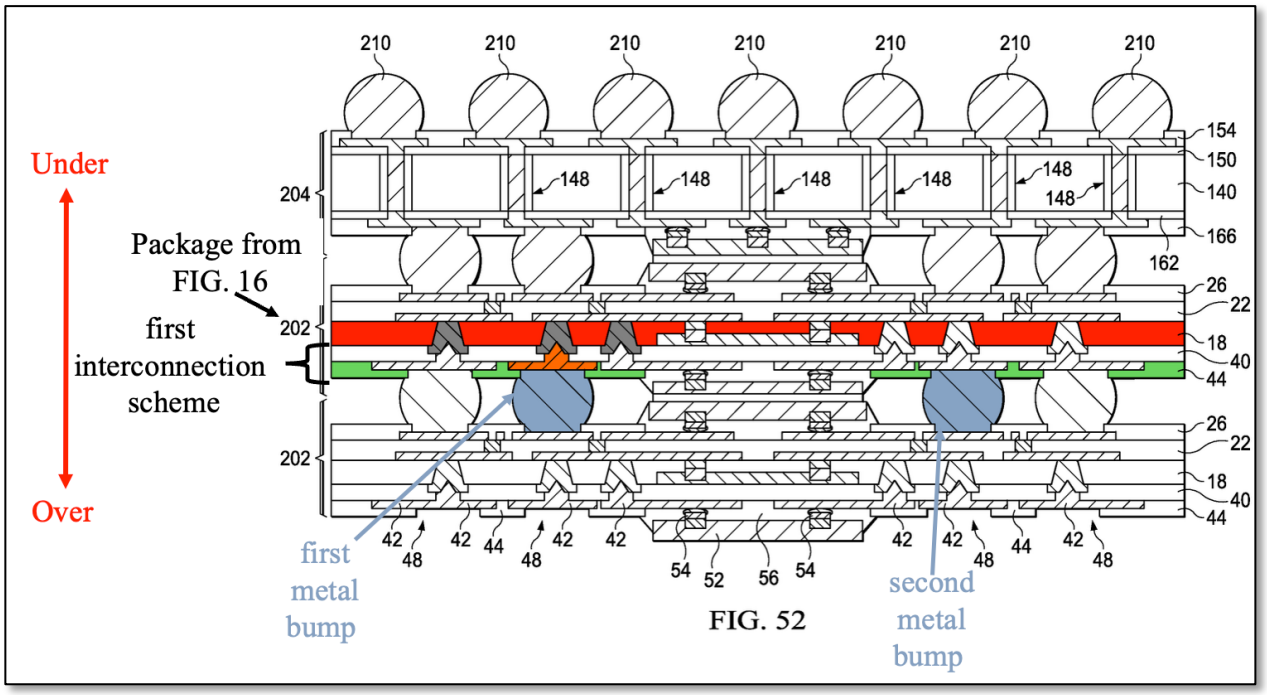


FIG. 52

EX1010, FIG. 52; *EX1003*, ¶388.

15. 10(f)

Yu's die 52 is *a first semiconductor chip over said first interconnection scheme and between said first and second metal bumps*. *EX1010*, 4:30-34.

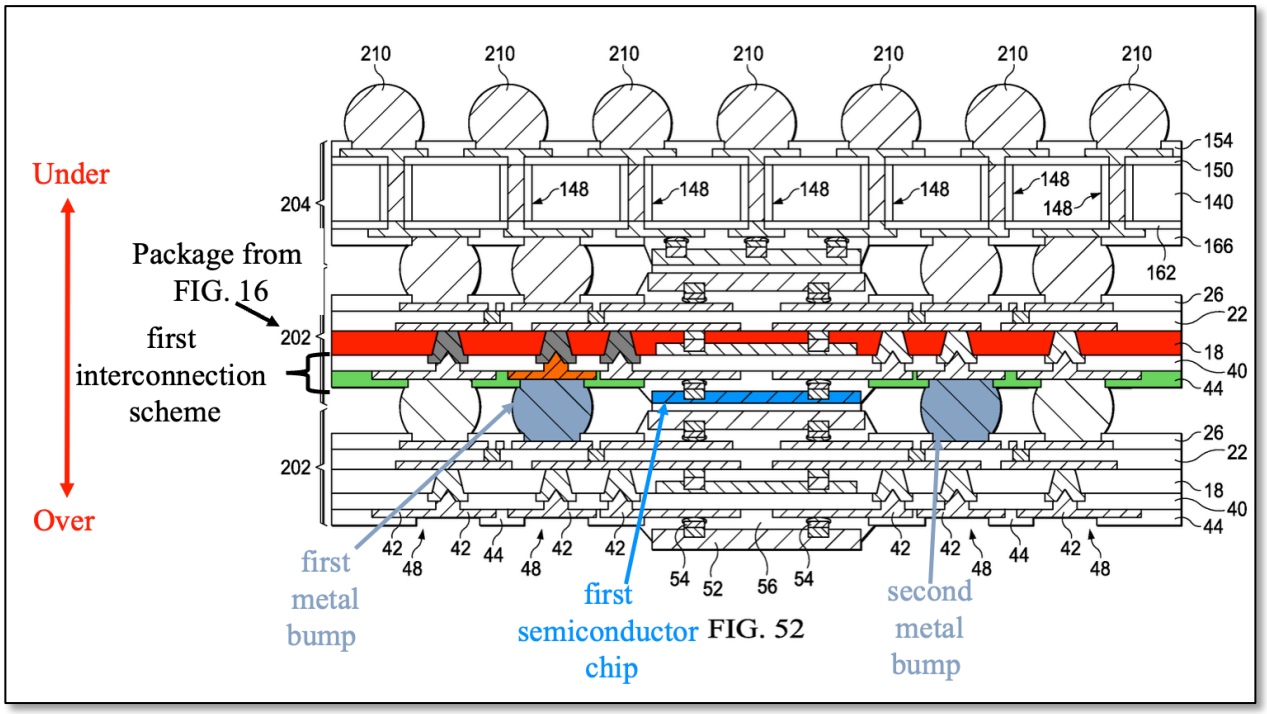
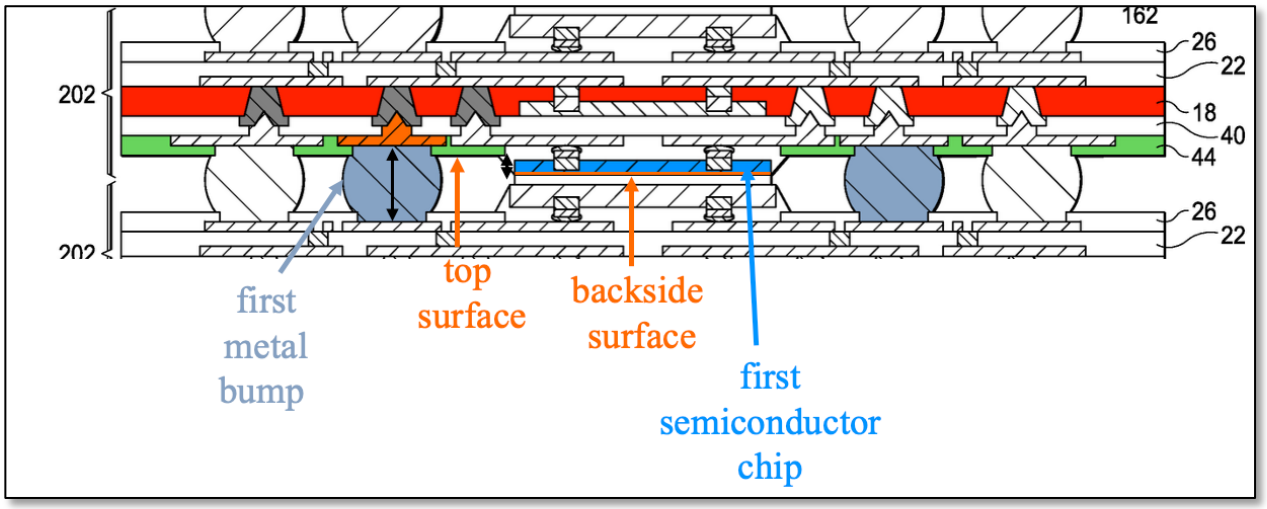


FIG. 52

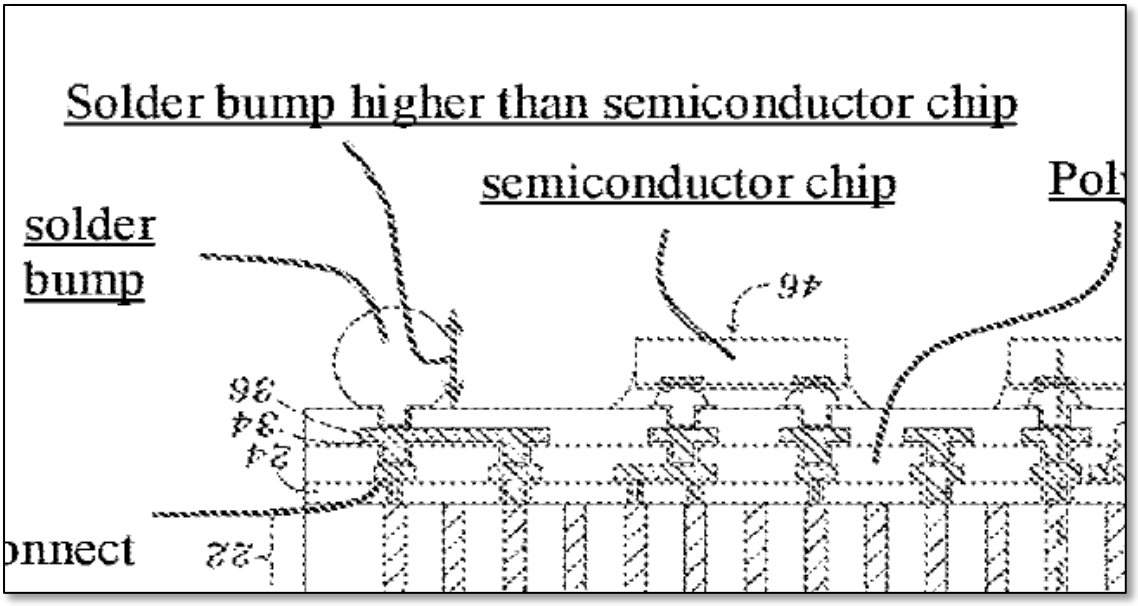
EX1010, FIG. 52; *EX1003*, ¶389.

16. 10(f)(i)

Die 52 has *a height between* its *backside surface and a top surface of* ILD 44 *smaller than a thickness of said first metal bump*:



EX1010, FIG. 52 (excerpt); *EX1003*, ¶390; *see* cited caselaw in Section V.A.8.



EX1032, 400[11]; *EX1003*, ¶391.

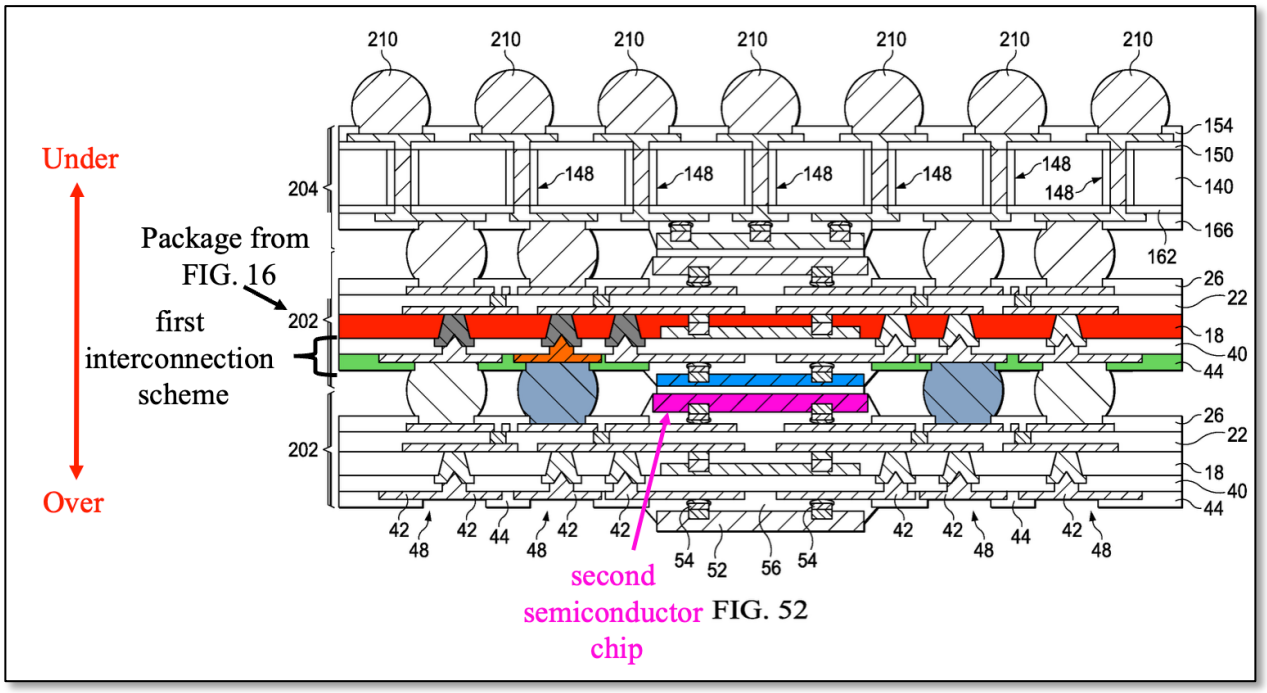
17. 10(f)(ii)

See Sections VII.A.14, VII.A.17, reciting corresponding limitations. *EX1003*, ¶392.

18. 10(g)

Another die 62 in a second package 202 in FIG. 52's PoP structure is *a second semiconductor over said first interconnection scheme*:

[11] Annotated figure PO argued supports language similar to Claim 10(f)(i).



EX1010, FIG. 52, 4:53-56, FIG. 15 (discussing die 62); *EX1003*, ¶393.

19. 10(g)(i)

See Section VII.F, reciting corresponding limitations. *EX1003*, ¶394.

J. Claim 11

See Section VII.E.

K. Claim 12

TMVs 38 (*copper posts*) are on either side of the *first region*, which encapsulates a die 10 such that there are *no any copper post[s] in said first region*. *EX1010*, 2:41-65 (describing die 10), FIGS. 1-2, 8:7-8 ("[P]ackage 202 compris[es] a first die encased in molding compound….").

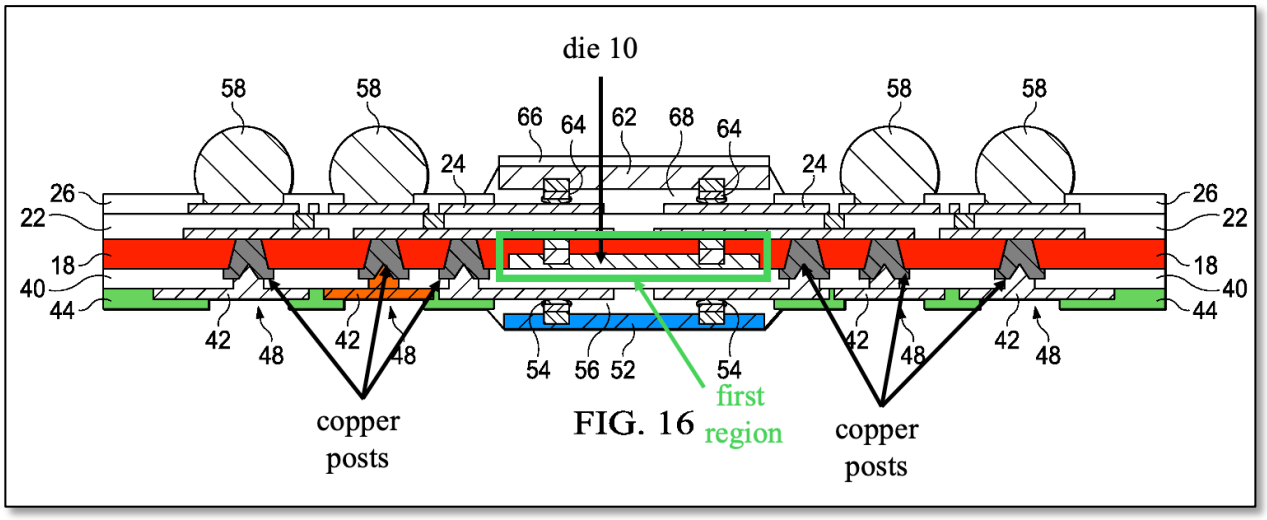


FIG. 16

EX1010, FIG. 16; *EX1003*, ¶¶396-398.

L. Claim 13

1. 13(a)

See Section VII.F.1, reciting corresponding limitations. *EX1003*, ¶399.

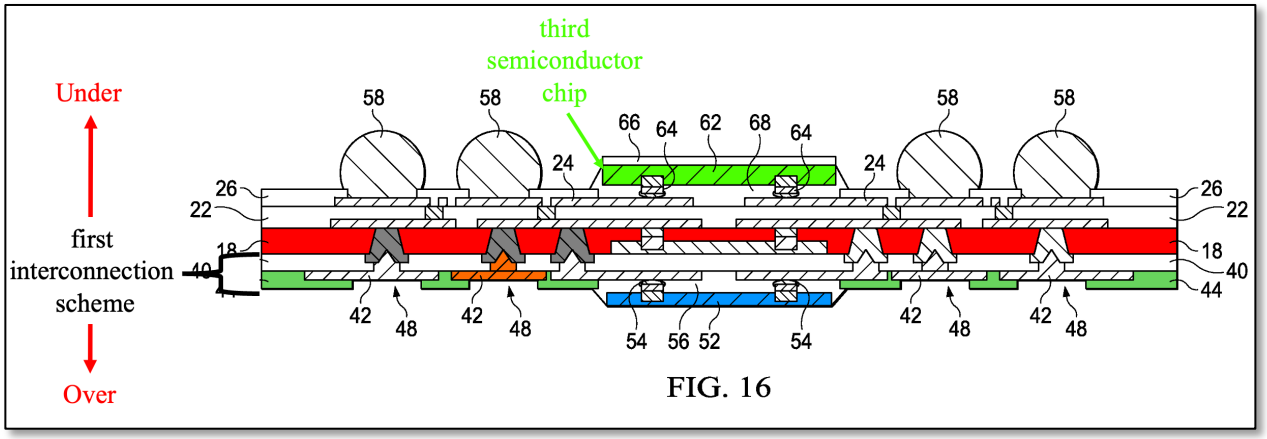


FIG. 16

EX1010, FIG. 16.

2. 13(b)

See Sections VII.F.1, VII.A.17, reciting corresponding limitations. *EX1003*, ¶400.

3. 13(c)

Sections VII.A.18, reciting corresponding limitations, V.K.3 (no criticality of claimed *thickness*); *EX1003*, ¶401. The motivations for modifying connector 64 apply for modifying the similar connector 54. *EX1003,* ¶401.

M. Claim 14

1. 14(a)

See Sections VII.L.1, VII.F.1.

2. 14(b)

See Sections VII.L.2, VII.F.1, VII.A.17.

3. 14(c)

See Sections VII.L.3, VII.A.18.

4. 14(d)

See Section VII.B.

N. Claim 15

See Section VII.G.

O. Claim 17

1. 17(a)

Yu teaches *a third semiconductor under said second surface*, i.e., memory "die 62." *EX1010*, 4:53-56.

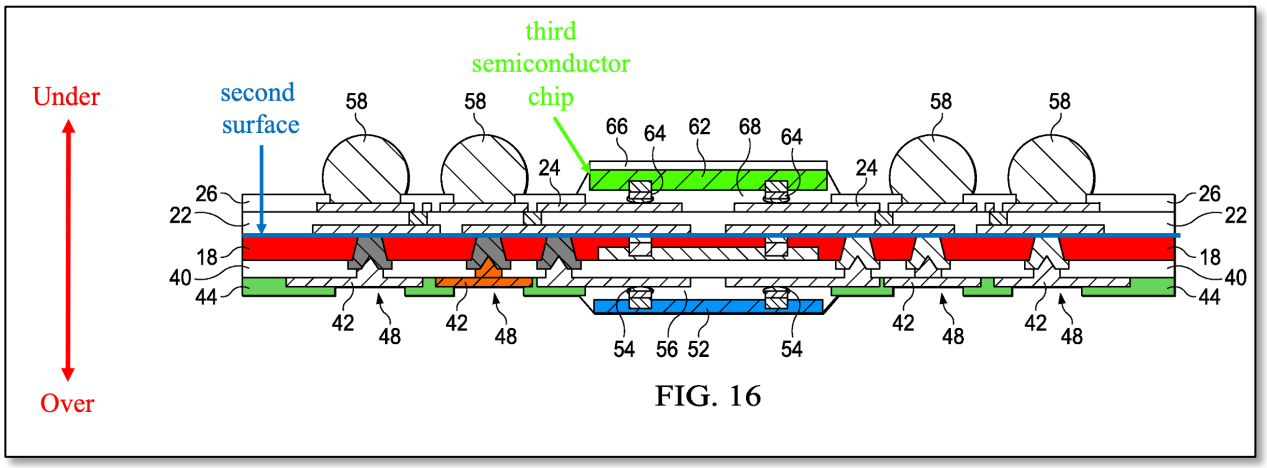


FIG. 16

EX1010, FIG. 16.

Yu teaches "[w]ire bonding can be used to make the electrical connections from chip components…to substrate." *EX1010*, 1:41-43. Yu alone or Yu-Lin-191 teaches *a third metal pad*, and a POSITA would have understood Yu's wire bond teachings as teaching wire bonding to a *metal pad* because wires were ubiquitously bonded to metal chip pads at the time of the '306 Patent. *See* Section VII.A.17; *EX1003*, ¶¶407-408.

a) Lin-191's Teachings and MTC

Additionally, or alternatively, to Yu, Lin-191 teaches "wirebonded wire[s] 820 can be ball bonded with one of the contact points…of the metal layer 73[.]"

EX1005, [0410]. Further, Lin-191 teaches "metal…pads 170c, 170d, 180c and 180d…can be connected to the ball-grid-array (BGA) substrate 810 shown in FIG. 74 through the wirebonded wires 830." *EX1005*, [0490]. Pads 170c, 170d, 180c, 180d are chip pads. *EX1005*, [0489]. Thus, Lin-191 teaches *a metal wire connected to a third metal pad of a third semiconductor chip*.

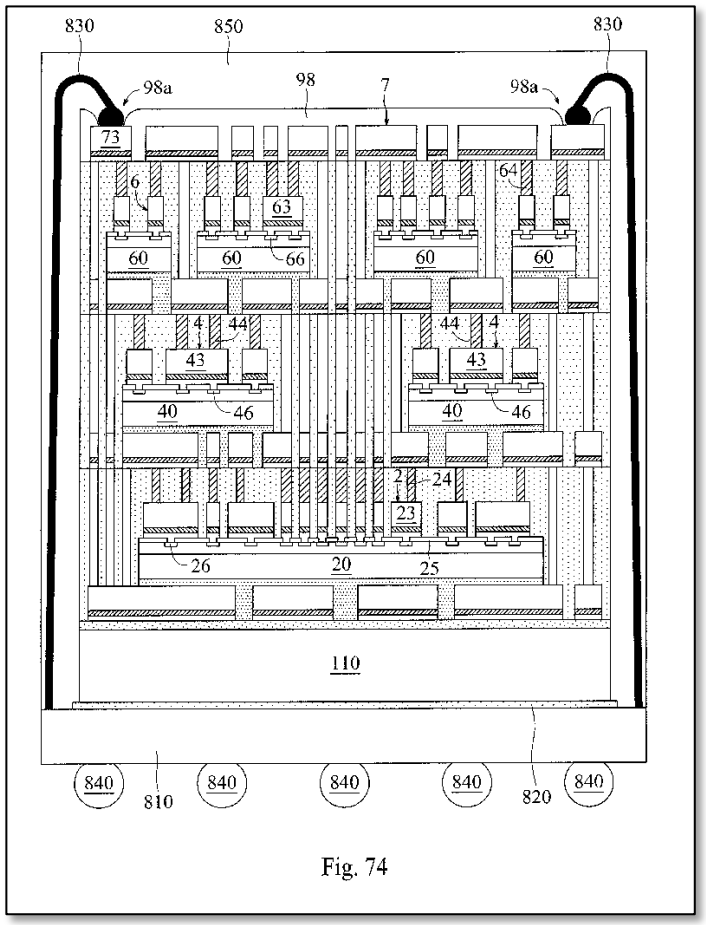


Fig. 74

EX1005, FIG. 74; *EX1003*, ¶409.

A POSITA would have been motivated and found it obvious to modify Yu's package to apply Lin-191's teachings of wirebonding metal pads. *EX1003*, ¶410. As

discussed, Yu expressly envisions wirebonding for connecting chips to substrates such that the modification is merely an implementation detail in Yu's package. *EX1010*, 1:41-43; *EX1003*, ¶410. The modification would have been advantageous and had a REOS because wire bonding was an inexpensive, reliable method of electrically connecting a chip in a package. *EX1003*, ¶¶411-412.

2. 17(b)

Yu teaches "Dynamic Random Access Memory." *EX1010*, 1:31-33. A POSITA would have found it obvious that Yu's memory chip can be a DRAM chip because DRAM chip is one kind of memory chip, e.g., when Yu's package is used in a "mobile telephone/PDA." *EX1010*, 1:53-55. Thus, a POSITA would have been motivated, found it obvious, and had a REOS in modifying Yu's memory die 62 to specifically be DRAM to provide a *chip package* for a phone. *EX1003*, ¶413.

P. Claim 18

1. 18(Pre)

See Section VII.A.1.

2. 18(a)

See Section VII.I.2. Claim 18's mapping maintains Claim 10's *over/under directions* and *first/second surface* mappings.

3. 18(a)(i)

See Section VII.A.3

4. 18(a)(ii)

See Section VII.A.4.

5. 18(a)(iii)

See Section VII.I.5.

6. 18(b)

See Sections VII.I.6, VII.A.6.

7. 18(c)

See Section VII.I.8.

8. 18(c)(i)

See Section VII.I.9. Another portion of metallization layer 42 is a *second metal interconnect over said first surface*. *EX1010*, 4:7-14. ILD layer 44 is *over said first and second metal interconnects*.

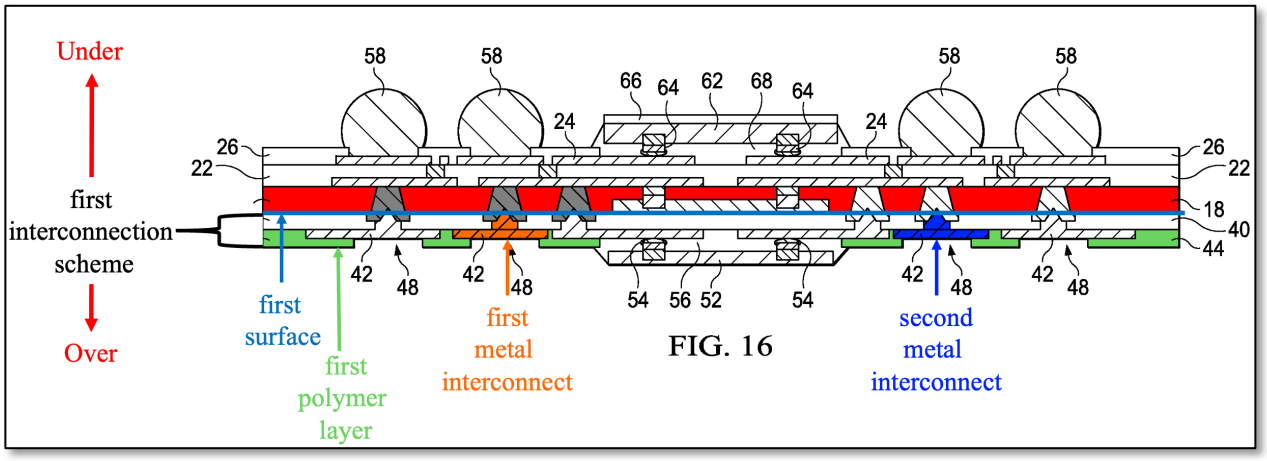
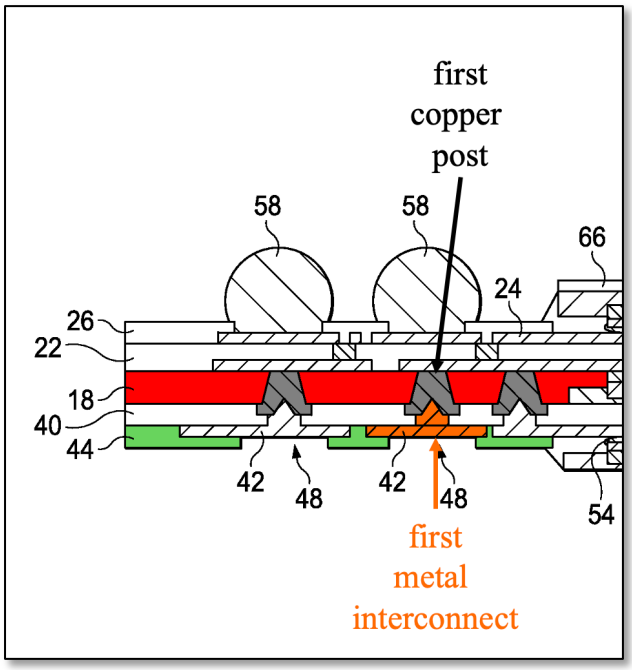


FIG. 16

EX1010, FIG. 16; *EX1003*, ¶¶421-422.

9. 18(c)(ii)

Yu's *first metal interconnect* is connected to a first TMV 48.



EX1010, FIG. 16 (excerpt); *see* Section VII.I.10; *EX1003*, ¶423.

10. 18(c)(iii)

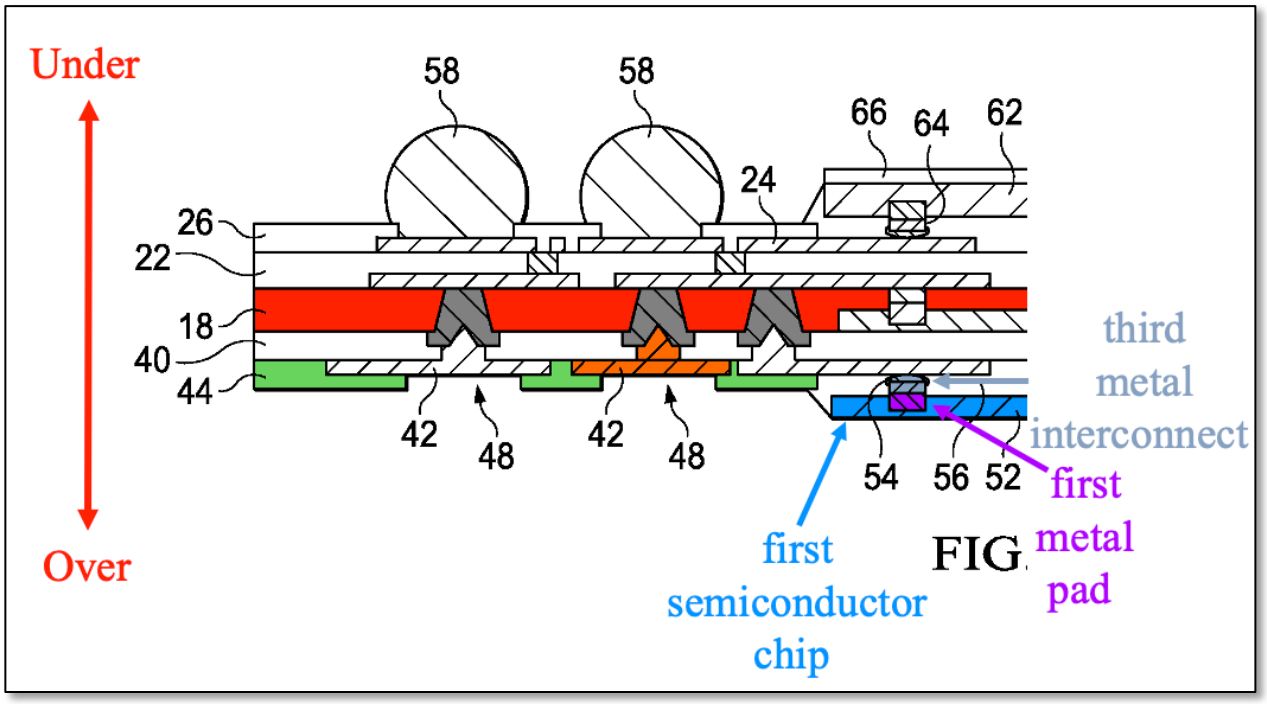
See Sections VII.I.11, VII.A.12.

11. 18(d)

See Section VII.I.15.

12. 18(d)(i)

Yu's die 52 (*first semiconductor chip*) has a connector 54 (*third metal interconnect*) *under a first metal pad*. *EX1010,* 4:30-34; *see* Section VII.A.17. Additionally, or alternatively to Yu, Yu-Lin-191 teach *a third metal interconnect under a first metal pad*. *See* Section VII.A.17.



EX1010, FIG. 16 (excerpt); *EX1003*, ¶¶426-427.

13. 18(d)(ii)

See Section VII.A.18, reciting corresponding limitations. *EX1003*, ¶428.

14. 18(d)(iii)

Die 52 *is coupled to* a second TMV *through* connector 54 and another portion of layer 42. Specifically, Yu teaches "die 52…is attached…to conductive features in the second back side metallization layer 42, such as by conductive connectors 54[.]" *EX1010*, 4:30-34. Because layer 42 is coupled to TMV 38, Yu teaches the limitation.

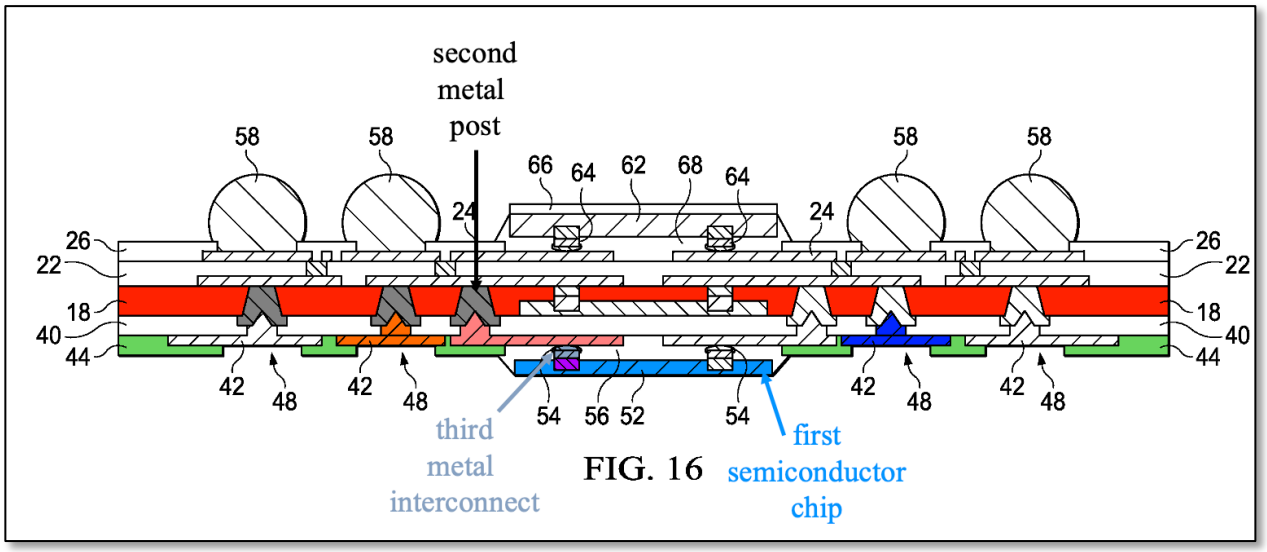


FIG. 16

EX1010, FIG. 16; *EX1003*, ¶429.

15. 18(e)

A die 52 in a second package 202 in the PoP structure is *a second semiconductor chip over said first interconnection scheme.*

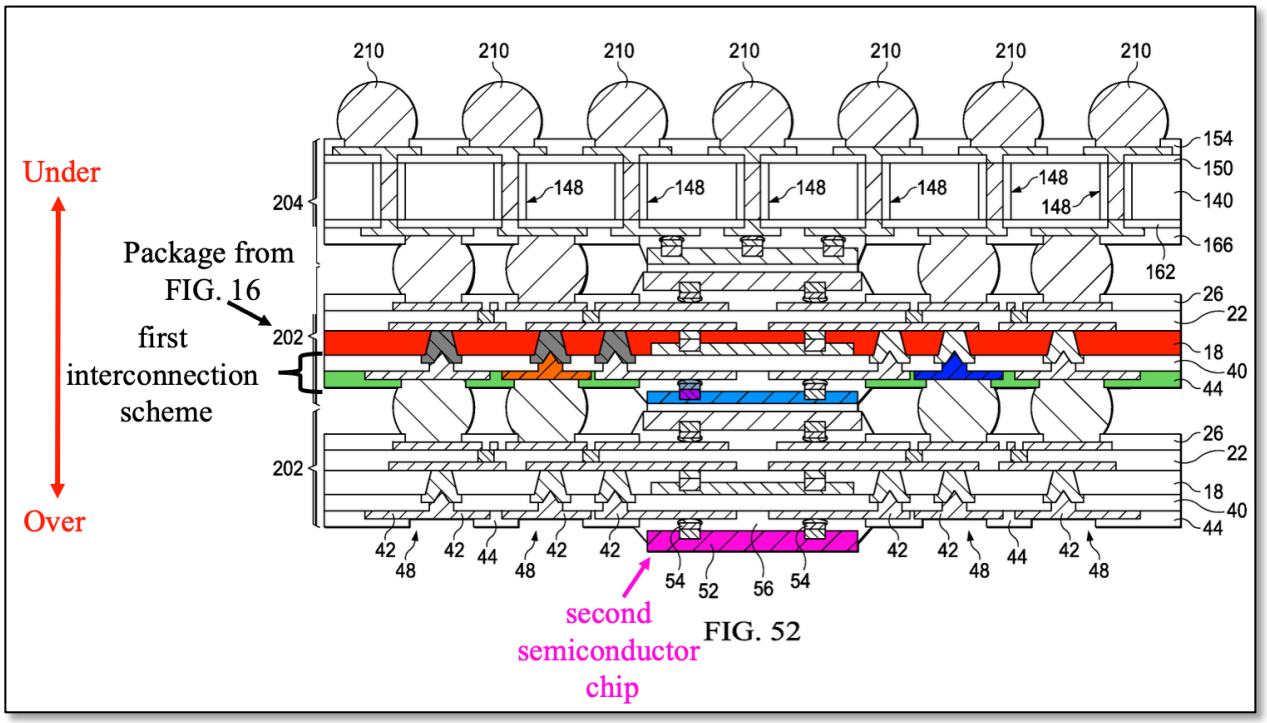


FIG. 52

EX1010, FIG. 52; *EX1003*, ¶430.

16. 18(e)(i)

Die 52 *comprises a second metal pad* (as taught by Yu alone or Yu-Lin-191) *coupled to said second metal interconnect* through die 52's connector 54, a first portion of layer 42, a TMV 38, layers 20, 24, and a connector 58. *EX1010*, 4:53-60; Section VII.A.17 (Yu and Lin-191's metal pad teachings); *EX1003*, ¶¶431-433.

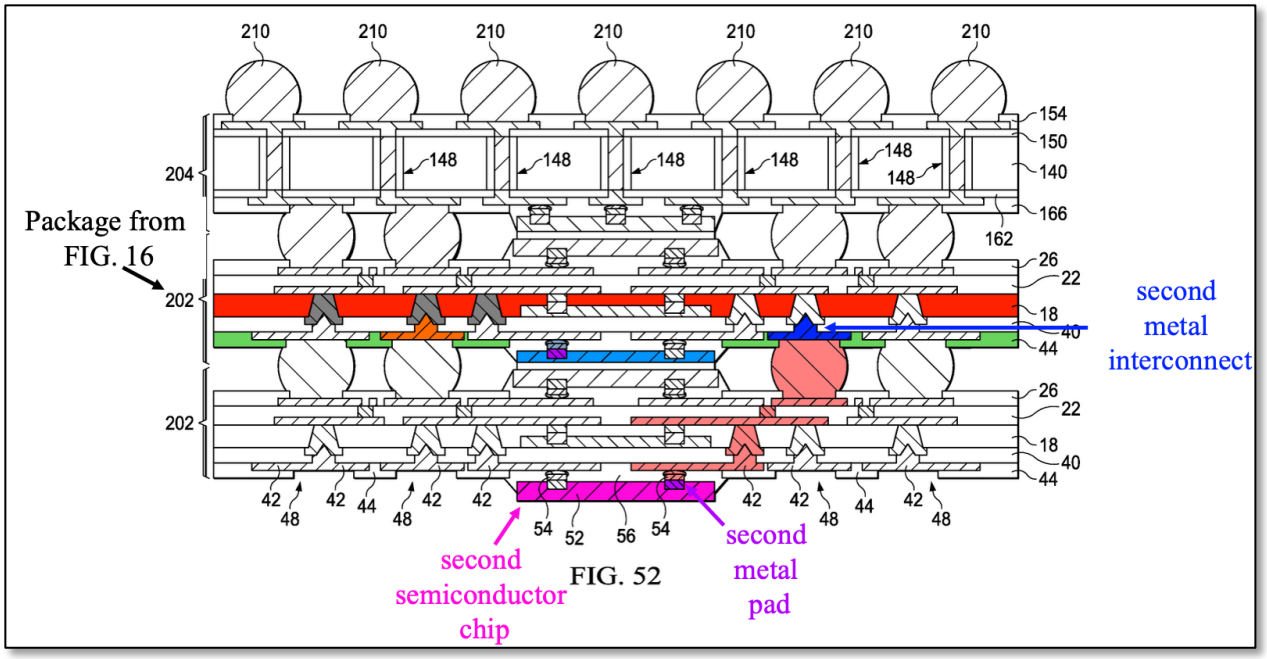


FIG. 52

EX1010, FIG. 52.

17. 18(f)

See Sections VII.L.1, VII.F.1, reciting corresponding limitations. *EX1003*, ¶434.

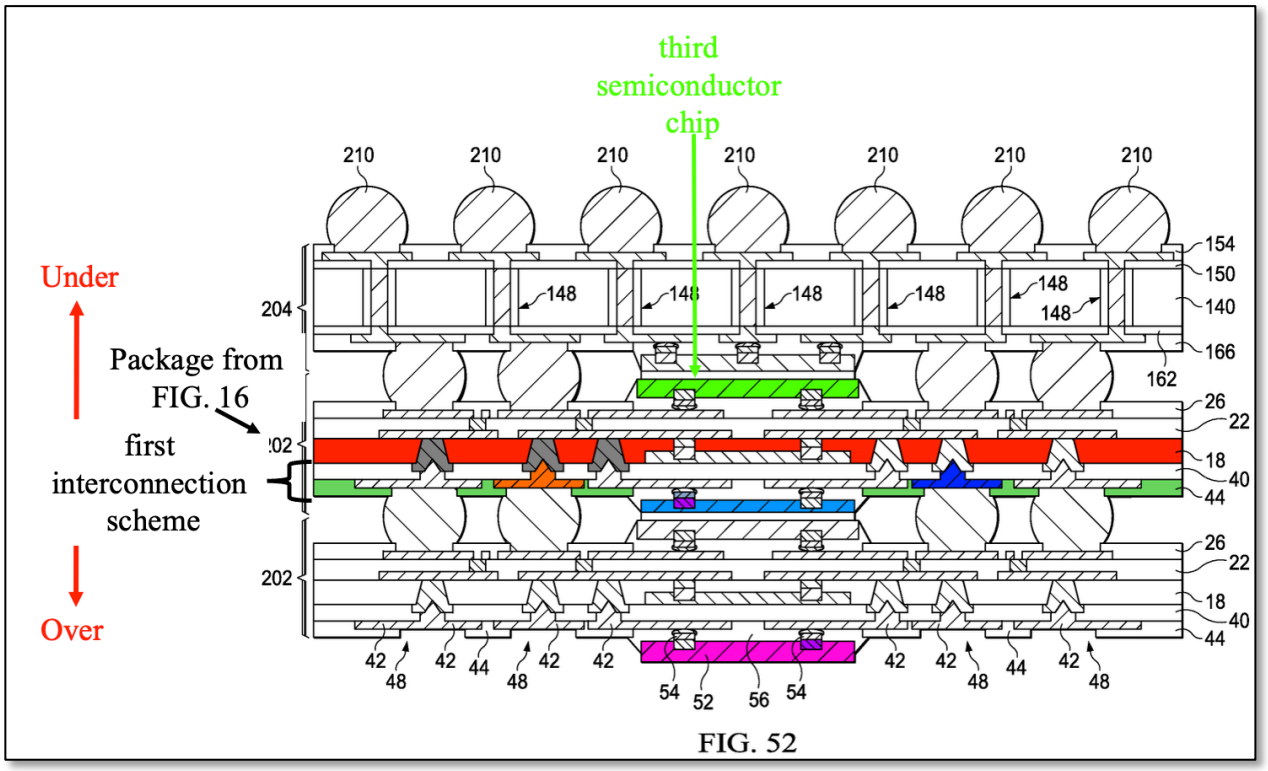


FIG. 52

EX1010, FIG. 52.

18. 18(g)

The "lead-free solder" connectors 58 are *a plurality of metal bumps under said second surface*. *EX1010*, 4:45-50. Yu alone or Yu-Lin-191 teaches a connector 58 comprises *a tin-containing layer*. *See* Section VII.A.14.

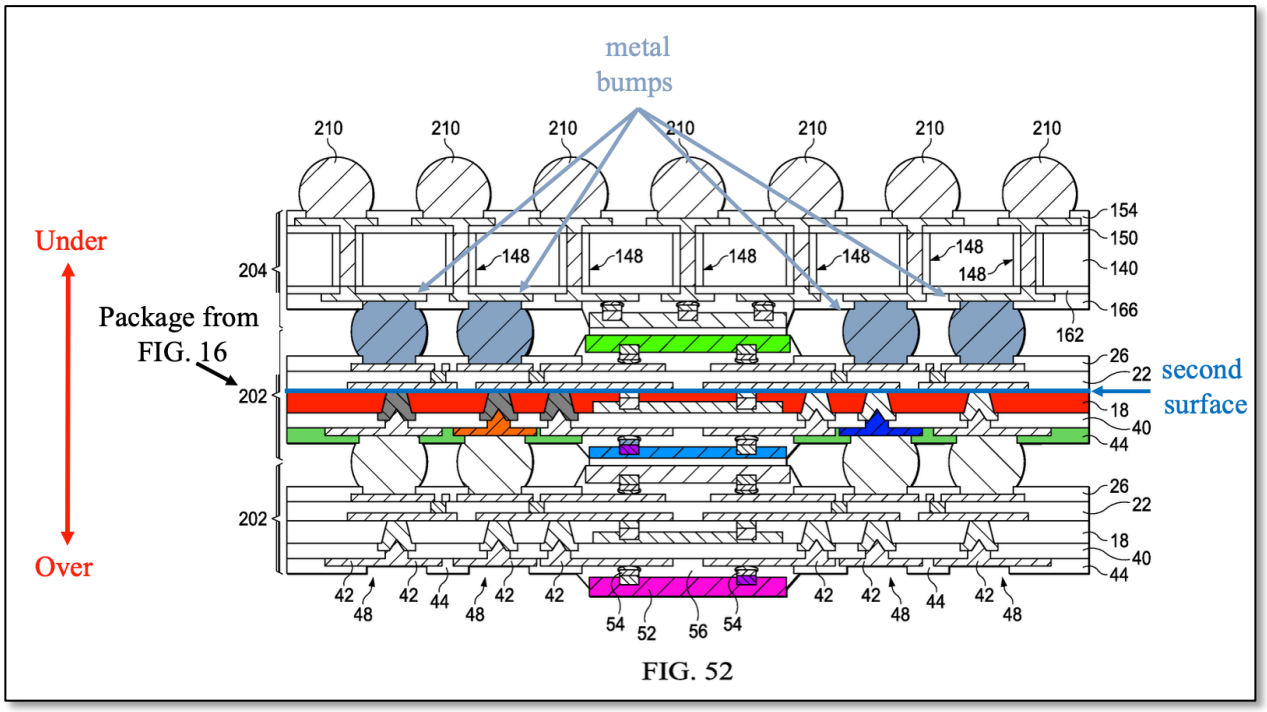


FIG. 52

EX1010, FIG. 52; *EX1003*, ¶435.

Q. Claim 19

See Section VII.E.

R. Claim 20

See Section VII.G.

S. Claim 22

a) Lin-191's Teachings and MTC

Lin-191 teaches semiconductor chips that are "graphics-processing-unit (GPU) chip[s]." *EX1005*, [0106]. The MTCs and REOS provided for Claim 2 are incorporated. *See* Section VII.B; *EX1003*, ¶438.

T. Claim 23

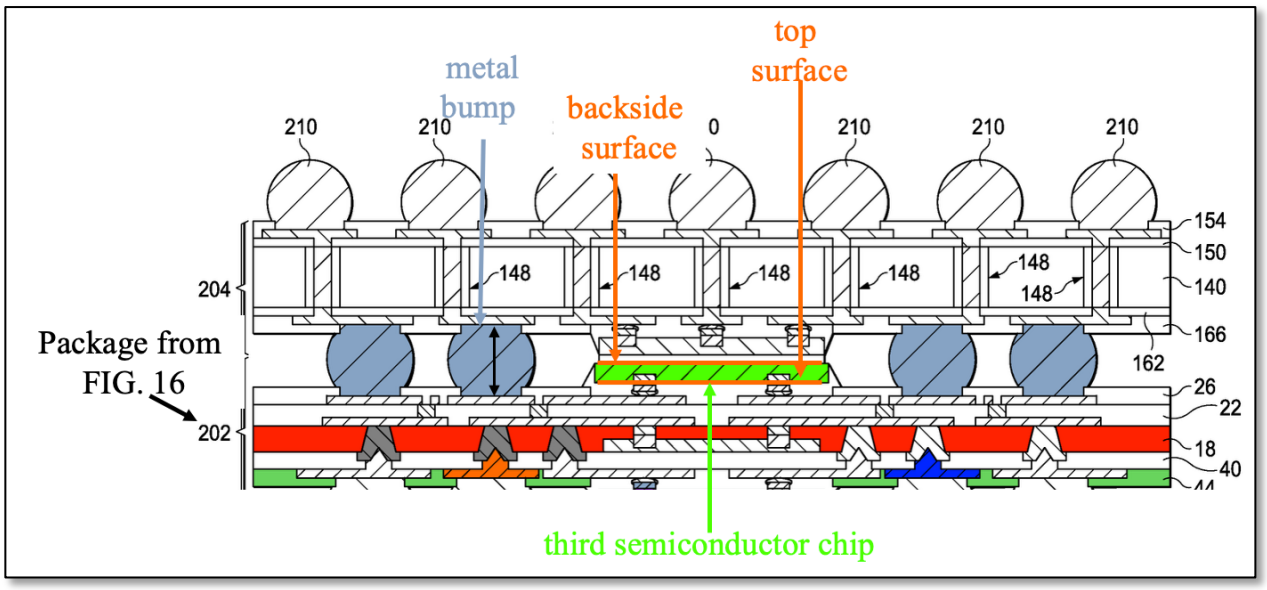
Yu teaches dies as "logic circuitry die[s]." *EX1010*, 2:50-51. A POSITA would have been motivated, found it obvious, and had a REOS in modifying die 52 to be a logic chip based on Yu's express teachings of such. *EX1003*, ¶¶439-441.

U. Claim 24

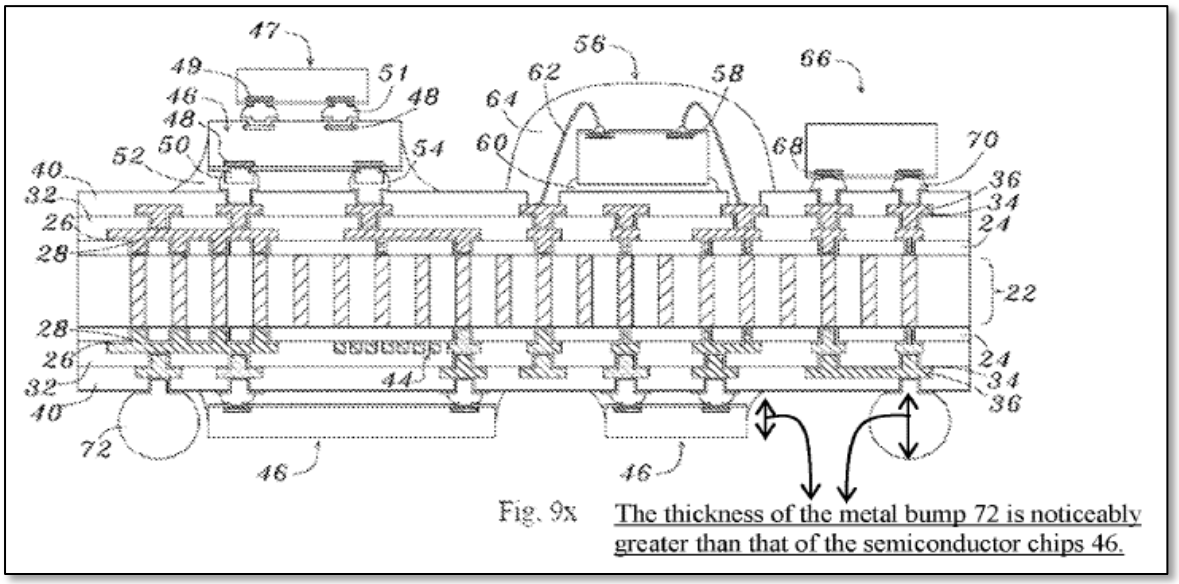
See Section VII.T.

V. Claim 25

Die 62 is smaller than a connector 58, i.e., *has a thickness…smaller than a thickness* of connector 58.



EX1010, FIG. 52 (excerpt); *EX1003*, ¶443.



EX1002, 336[12]; *see* cited caselaw in Section V.A.8; *EX1003*, ¶444.

W. Claim 26

A die 62 in the second package 202 of Yu's PoP structure is *another said first semiconductor chip over said first interconnection scheme*. Die 62 is, like die 52, "a memory die," such that die 62 is *another* die 52. *EX1010*, 4:53-56.

[12] Annotated figure PO argued supports language similar to Claim 25.

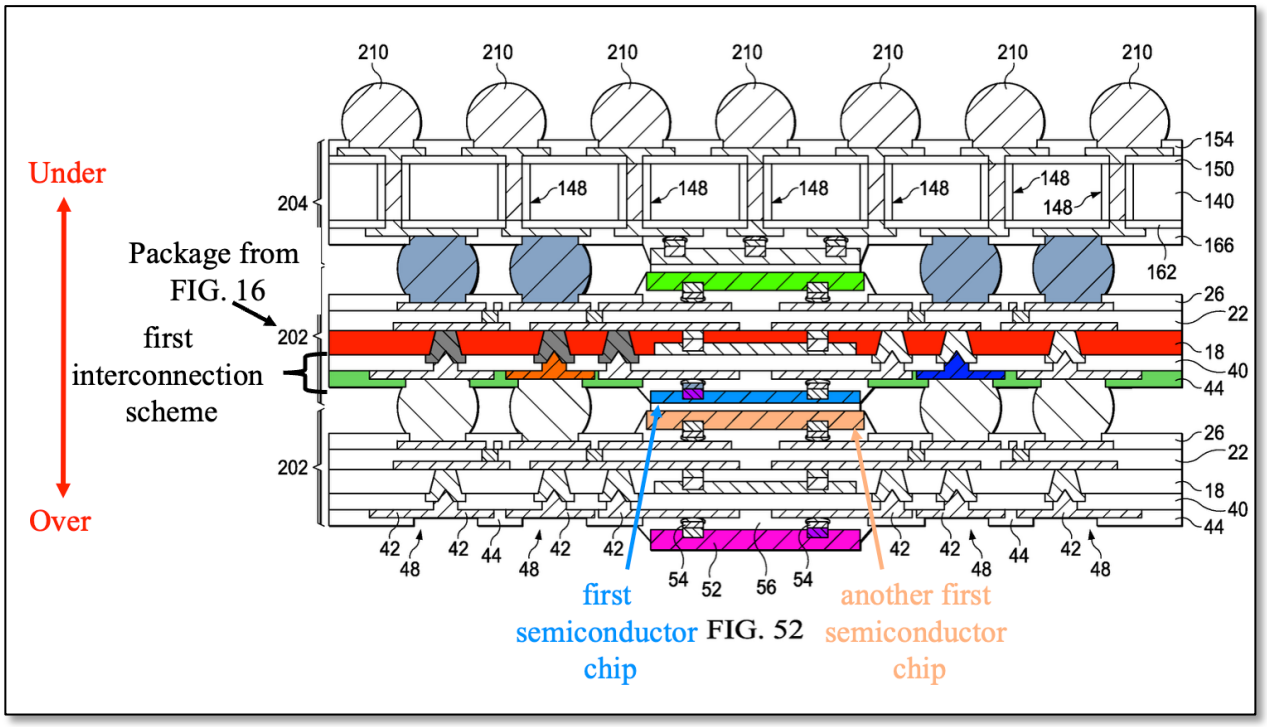


FIG. 52

EX1010, FIG. 52; *EX1003*, ¶445.

X. Claim 27

1. 27(a)

Yu's PoP structure includes "interposer package 204" with "a third die on a front side of the [interposer] package," which is *a fourth semiconductor chip under said first interconnection scheme*. *EX1010*, 8:6-11, FIGS. 34-48 (formation of interposer 204).

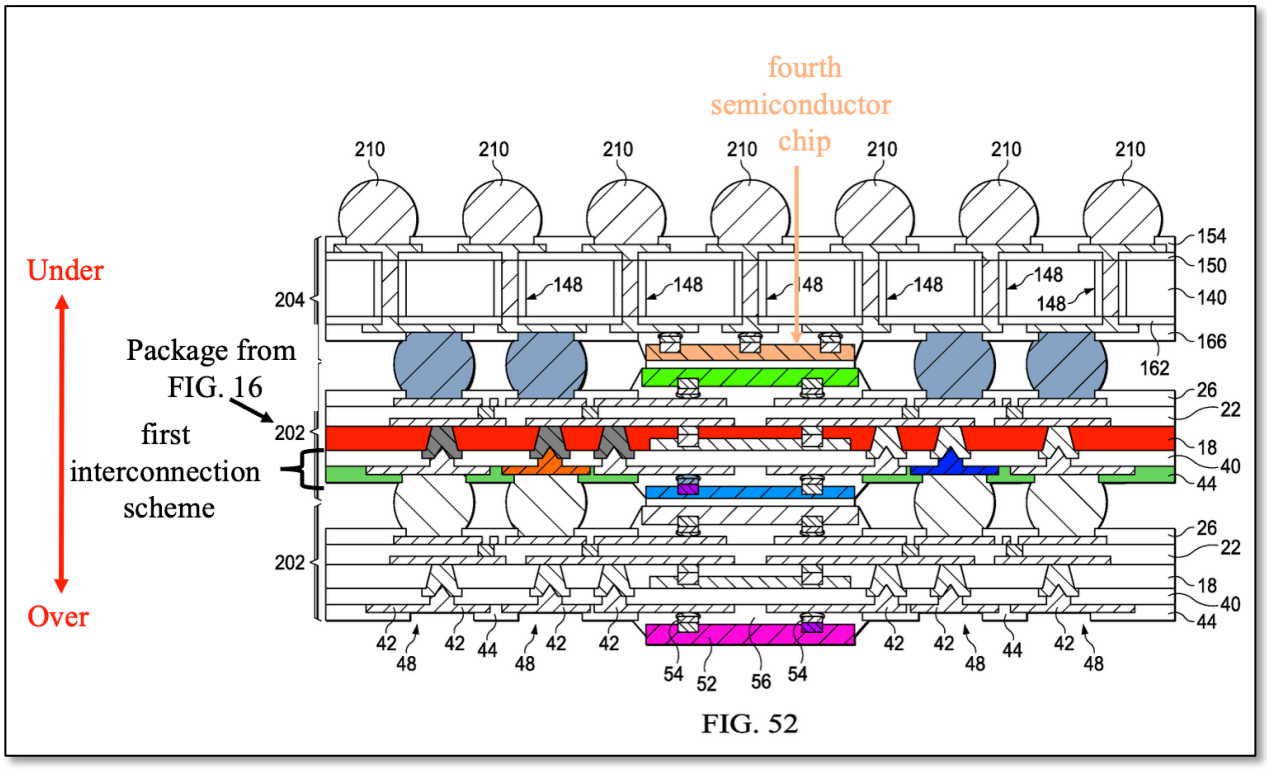
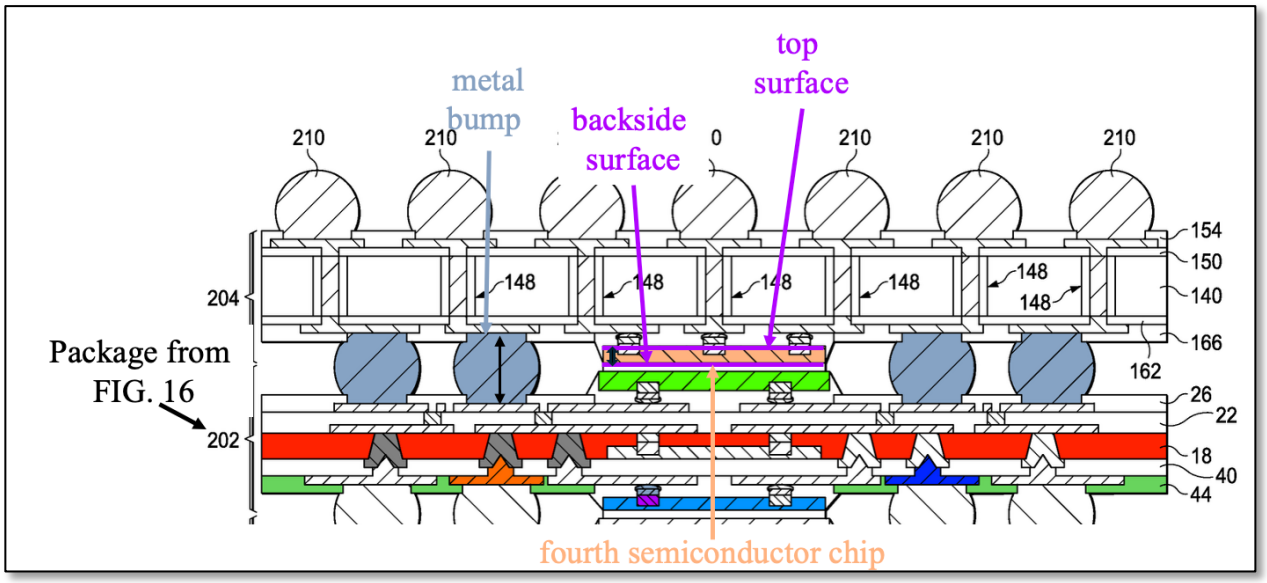


FIG. 52

EX1010, FIG. 52; *EX1003*, ¶446.

2. 27(b)

The interposer die *has a thickness…smaller than a thickness of* a connector 58.



EX1010, FIG. 52 (excerpt), *see* cited caselaw in Section V.A.8; *EX1003*, ¶¶447-448.

VIII. GROUND 2B: CLAIMS 8 AND 16 ARE OBVIOUS OVER YU, LIN-191, AND LIN-863

A. Claim 8

a) Lin-863's Teachings and MTC

Lin-863 teaches Claim 8. *See* Section VI.A. The MTCs and REOS for Sundaram-Lin-863 apply for Yu-Lin-863. Further evidencing the REOS, Yu, like Lin-863, already teaches both an encapsulated die 10 and a PoP structure, such that applying Lin-863's fan-out teachings would have been simple and straightforward to Yu's similar *chip package*. *Compare EX1007*, 11:47-48, FIGS. 6a-7 *with EX1010*, FIG. 52; *EX1003*, ¶¶449-450.

B. Claim 16

See Section VIII.B.

IX. GROUND 2C: CLAIM 21 IS OBVIOUS OVER YU, LIN-191, AND CAMACHO

A. Claim 21

1. 21(a)

See Section VII.I.18. Claim 10(g)'s *second semiconductor chip* corresponds to Claim 21(a)'s *fourth semiconductor chip*. *EX1003*, ¶452.

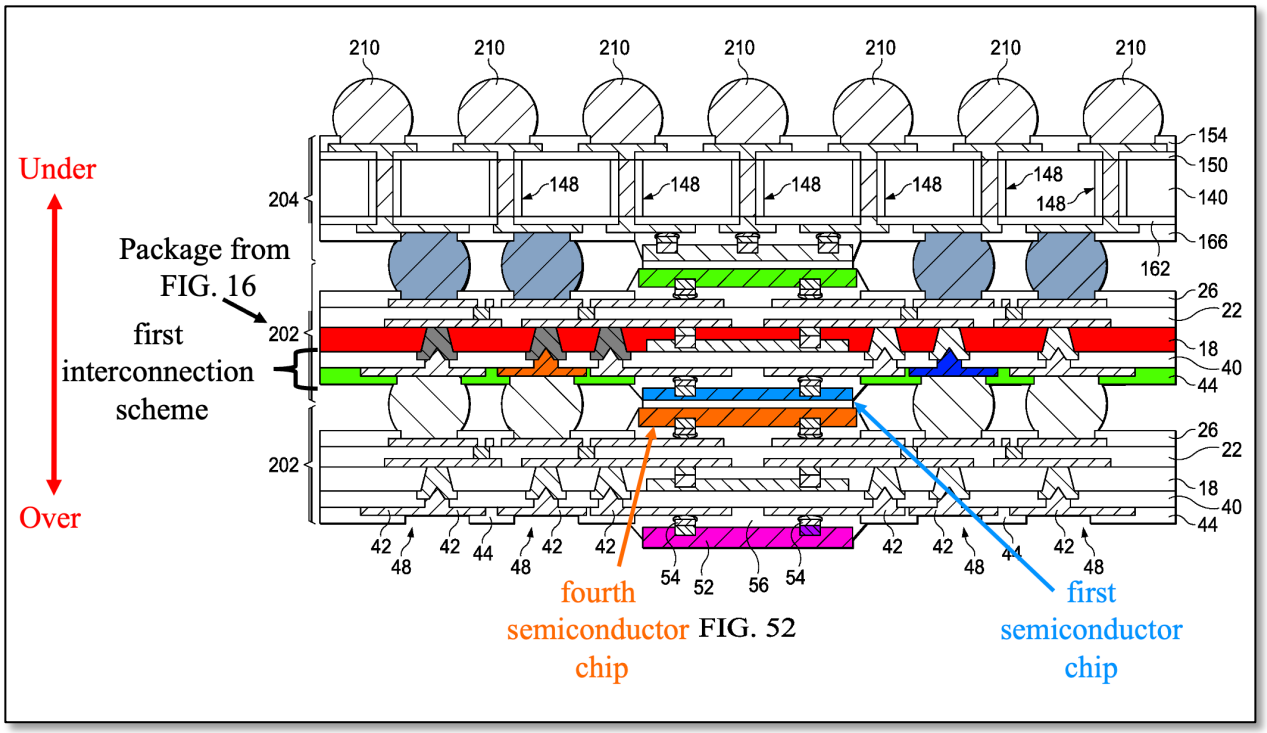


FIG. 52

EX1010, FIG. 52; *EX1003*, ¶452.

2. 21(b)

a) Camacho's Teachings

Camacho teaches a die 150 that has "contact pads 152," i.e., *metal pads*. *EX1006*, [0047]; *EX1003*, ¶453. To the extent it is argued contact pads are not *metal pads*, a POSITA would have found it obvious to configure contact pads 152 to be a *metal pad* at least because contact pads were well known in the art to be metal and because Camacho teaches "contact pads 76" on a "die 74" are "aluminum." *EX1006*, [0035]; *EX1003*, ¶453. Likewise, contact pads 152 are on semiconductor die 150; thus, a POSITA would have found it obvious for contact pads 152 to also be metal. *EX1003*, ¶454. Contact pads 152 electrically connect die 150 to die 122 through solder bumps 148 and conductive layer 130a such that a POSITA would have found it obvious for the pads 152 to be metal to make the electrical connection. *EX1006*, [0047-0048]; *EX1003*, ¶454.

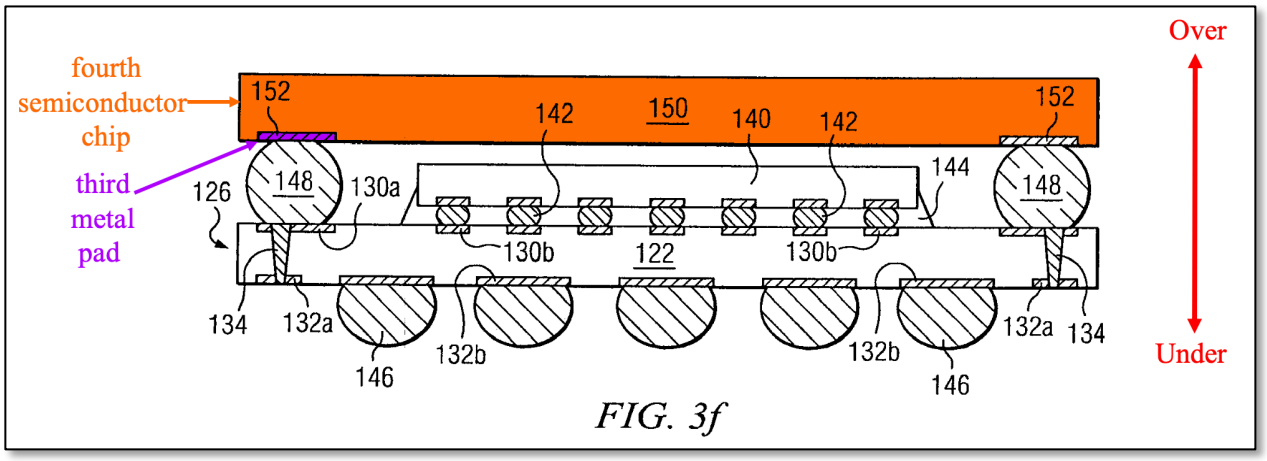


FIG. 3f

EX1006, FIG. 3f. A POSITA would have been motivated, found it obvious, and had a REOS in modifying Yu's die 62 to have *a third metal pad at a bottom surface* per Camacho because Camacho provides straightforward implementation details of chips having pads on surfaces. *EX1003*, ¶455.

3. 21(c)

a) Camacho's Teachings

Camacho teaches conductive metals "form **conductive TSV[s]** 134," which "electrically connect" layers 130, 132. *EX1006*, [0043], [0047]. Camacho thus teaches *a plurality of through-silicon-via metal layers* (TSVs 134). An "electrically conductive layer 130 is formed over the **top**…of semiconductor die 122." Layer 130 is aluminum. *Id*. Layer 130a is thus a *fourth metal pad at a top surface of a* first chip. *EX1003*, ¶456.

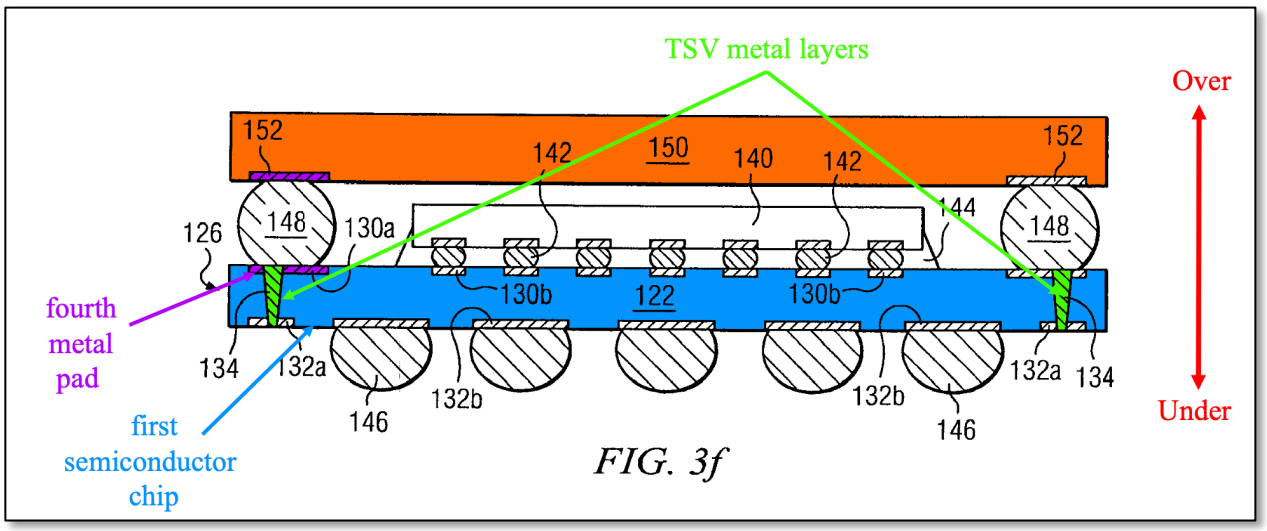
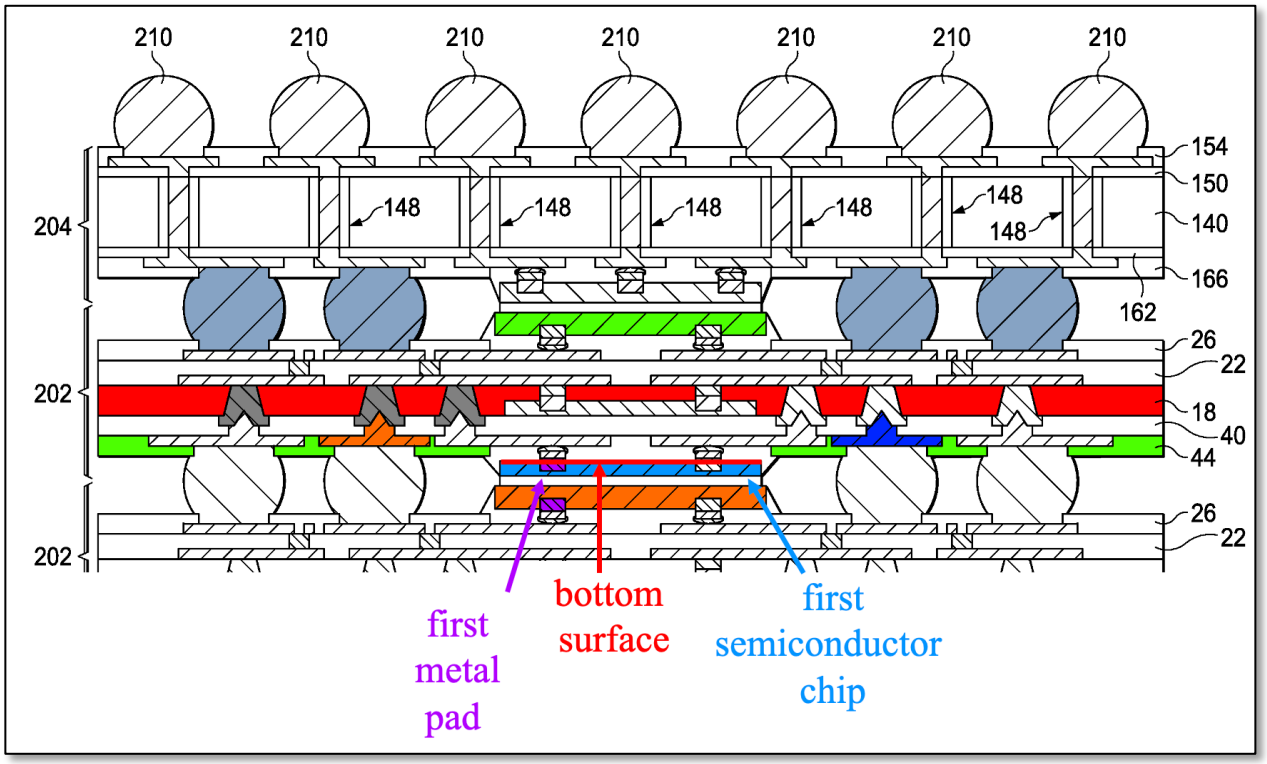


FIG. 3f

EX1006, FIG. 13. FIG. 2. A POSITA would have been motivated, found it obvious, and had a REOS in modifying Yu per Camacho to advantageously provide Yu's chips with TSVs, enabling interconnection directly between chips. Additionally, POSITA would have found it obvious, been motivated, and had a REOS in modifying Yu to provide die 52 with its own set of pads so that each chip has top and bottom pads connected to one another as each chip must include pads on its surface to provide connection to other electrical components in the chip package. *EX1003*, ¶457.

4. 21(d)

See Section VII.P.12. The *first metal pad is at a bottom surface* of die 52:



EX1010, FIG. 52 (excerpt); *EX1003*, ¶458.

5. 21(e)

a) Camacho's Teachings

See Section IX.A.3. Camacho additionally teaches an aluminum layer 132 "is formed over the **bottom** surface of semiconductor die 122, i.e., a *first metal pad* that *is coupled to said fourth metal pad through* a *through-silicon-via metal layer*. *EX1006*, [0041]; *EX1003*, ¶459.

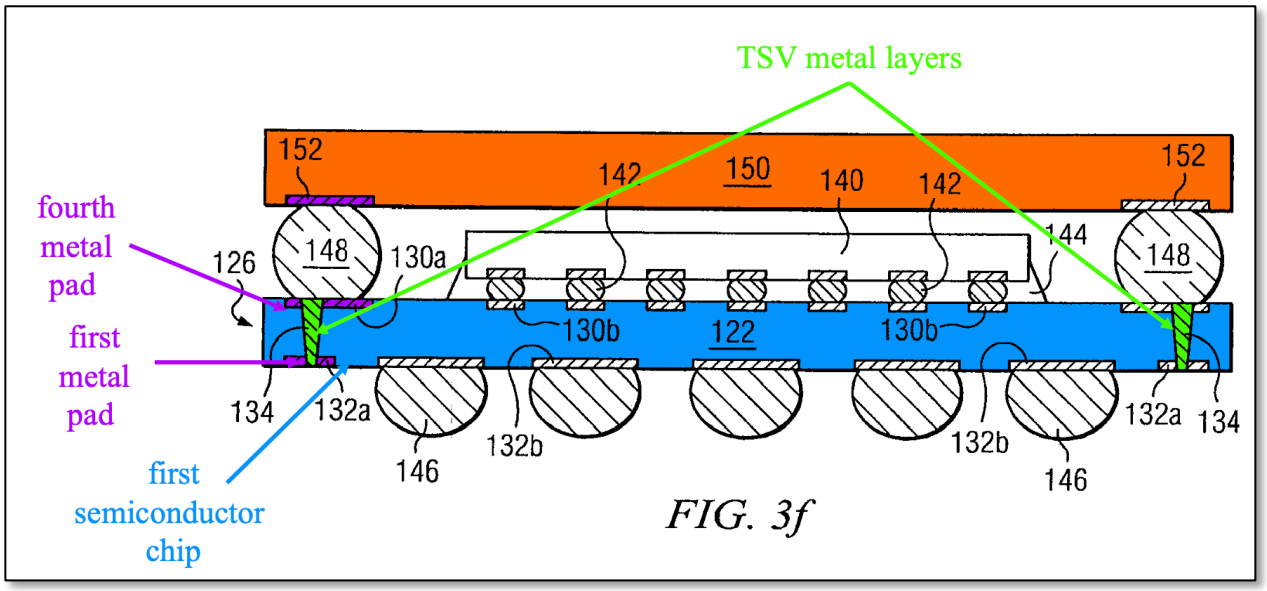


FIG. 3f

EX1006, FIG. 3f. In the combination, Yu's die 52 is modified, per Camacho, to have *a fourth metal pad* and a *TSV metal layer*, which connects to Yu's existing *first metal pad*. *EX1003*, ¶460. MTCs and REOS are below in Section IX.A.7.

6. 21(f)

a) Camacho's Teachings

Camacho's *third metal pad* is connected to the *fourth metal pad* by a bump 148 where the "bump material" is "solder," i.e., *a solder layer*. *EX1006*, [0046], [0047]; *EX1003*, ¶461. ("Contact pads 152 on semiconductor die 150 are electrically connected to bumps 148, conductor layer 130a…").

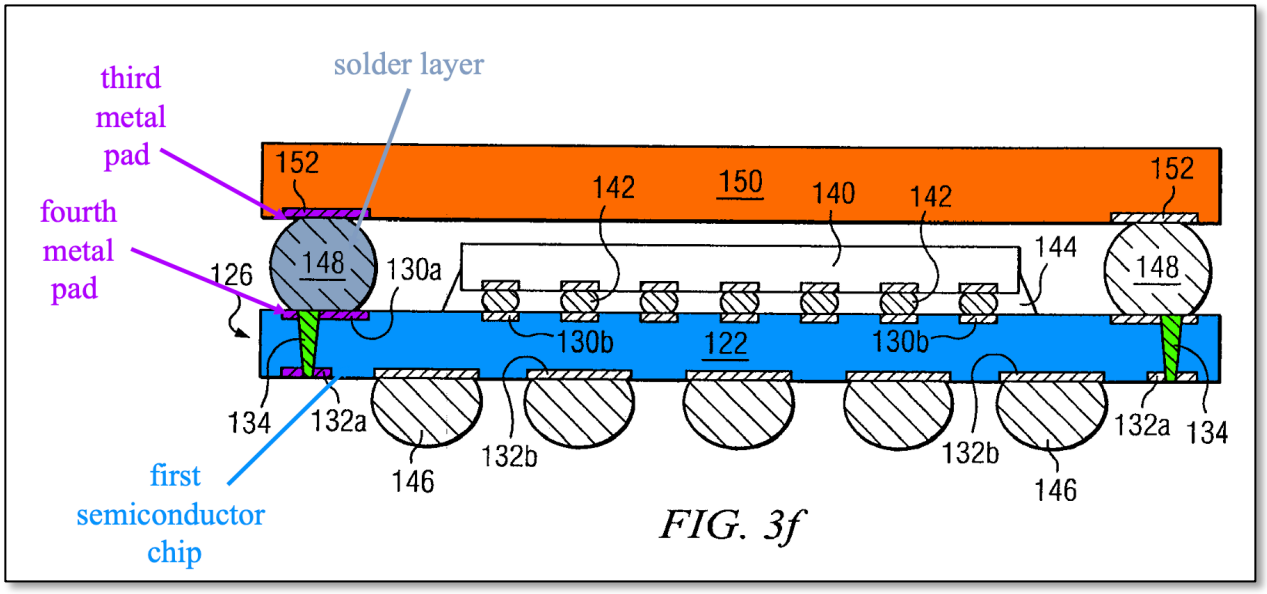


FIG. 3f

EX1006, FIG. 3f; *EX1003*, ¶461. A POSITA would have been motivated, found it obvious, and had a REOS in modifying Yu's per Camacho's teachings to reduce misalignment when stacking chips. *EX1003*, ¶462.

7. Claim 21 MTC

A POSITA would have been motivated and found it obvious to modify Yu per Camacho such that Yu's *fourth semiconductor chip* is connected to the *first semiconductor chip through a solder layer*. *EX1003*, ¶463. The modification would

have been obvious and advantageous for electrically connecting the two chips using a well-known, cost-efficient technique easily implementable in Yu's *chip package*. *EX1003*, ¶¶463-464. As Yu already teaches solder connections, a POSITA would have found it obvious and had a REOS in applying Camacho's teachings of solder connections to couple the first and fourth chips. *EX1003*, ¶465.

Further, a POSITA would have been motivated and found it obvious to modify Yu so that the *first semiconductor chip* has *TSV metal layers* connecting *metal pad[s]* on *top* and *bottom surface[s]* of die 52 to provide an electrical connection through the chip and to enable electrical connections to other components on both sides of die 52 using a ubiquitous technique. *EX1003*, ¶464. TSVs were another well-known structure for passing signals through chips and were advantageous by not increasing the height of the package. *EX1003*, ¶464. Additionally, the modification of the *first* and *fourth semiconductor chips* having *metal pads* is merely an implementation detail a POSITA would have found obvious and been motivated to make so the *chips* were directly electrically connected in Yu's *chip package*, i.e., to connect to components on either side of the chip. *EX1003*, ¶464.

The combination is the application of known techniques (TSV metal layers interconnecting pads and soldering chips) to a known device (Yu's *chip package*) to yield predictable results. *EX1003*, ¶466. There would have been a REOS because Camacho's teachings are simply commonplace methods to electrically connect chips

in a chip package via TSVs and solder layers. *EX1003*, ¶466. For example, Sundaram taught a similar chip package with TSVs and metal pads of different chips soldered to one another. *EX1004*, FIG. 32; *EX1003*, ¶466.

X. CONCLUSION

For the foregoing reasons, Petitioners respectfully request *inter partes* review of the Challenged Claims.

Respectfully submitted,

ERISE IP, P.A.

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COUNSEL FOR PETITIONERS,
TAIWAN SEMICONDUCTOR
MANUFACTURING COMPANY LTD. AND
APPLE INC.

XI. MANDATORY NOTICES UNDER 37 C.F.R. § 42.8(A)(1)

A. Real Parties-In-Interest

Petitioners Taiwan Semiconductor Manufacturing Company Limited and Apple Inc. are the real parties-in-interest. 37 C.F.R. § 42.8(b)(1).

B. Related Matters

The '306 Patent is presently the subject of a patent infringement lawsuit filed against Petitioner, Apple Inc., in the United States District Court for the District of Delaware: *MYW Semitech, LLC v. Apple Inc.*, Case No. 1:25-cv-00504.

C. Lead and Back-Up Counsel

Petitioners provide the following designation and service information for lead and back-up counsel. 37 C.F.R. §§ 42.8(b)(3) and (b)(4).

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	Telephone: (913) 777-5600 Fax: (913) 777-5601

D. 37 C.F.R. § 42.8(b)(4) – Service Information

Please address all correspondence to the lead and back-up counsel as shown above. Petitioners consent to electronic service by e-mail at the e-mail addresses provided above.

CLAIM LISTING APPENDIX
U.S. Patent No. 11,894,306 for Claims 1-27

Claim Designation	Claim Language
Claim 1(Pre)	A chip package comprising:
Claim 1(a)	a solid layer having a first surface and a second surface opposite to said first surface,
Claim 1(a)(i)	wherein said solid layer comprises a compound of silicon and oxygen,
Claim 1(a)(ii)	wherein said solid layer has a thickness between 50 and 150 micrometers,
Claim 1(a)(iii)	wherein said solid layer comprises a first region and a second region between said first region and a first edge of said solid layer;
Claim 1(b)	a plurality of metal posts in a plurality of through holes in said second region respectively,
Claim 1(b)(i)	wherein one of said plurality of metal posts comprises a first copper layer contacting a sidewall of one of said plurality of through holes,
Claim 1(b)(ii)	wherein said first region has a width in a direction greater than a shortest distance between said sidewall of one of said plurality of through holes and said first edge in said direction and greater than a pitch between two neighboring metal posts of said plurality of metal posts;
Claim 1(c)	a first interconnection scheme over said first surface,
Claim 1(c)(i)	wherein said first interconnection scheme comprises a first metal interconnect over said second surface and a polymer layer over said first metal interconnect,
Claim 1(c)(ii)	wherein said first metal interconnect is connected to a first metal post of said plurality of metal posts,
Claim 1(c)(iii)	wherein said first metal interconnect comprises a first metal layer and a second copper layer over said first metal layer;
Claim 1(d)	a first metal bump over said first interconnection scheme,
Claim 1(d)(i)	wherein said first metal bump comprises a second metal layer and a first tin-containing layer over said second metal layer; and
Claim 1(e)	a first semiconductor chip under said second surface,

Claim Designation	Claim Language
Claim 1(e)(i)	wherein said first interconnection scheme comprise a second metal interconnect across over a sidewall of the first semiconductor chip,
Claim 1(e)(ii)	wherein said first semiconductor chip comprises a third metal interconnect on a first metal pad of said first semiconductor chip,
Claim 1(e)(iii)	wherein said third metal interconnect comprises a third metal layer on said first metal pad and a third copper layer over said third metal layer, wherein said third copper layer has a thickness between 5 and 30 micrometers,
Claim 1(e)(iv)	wherein said first semiconductor chip is connected to a second metal post of said plurality of metal posts through said third metal interconnect.
Claim 2	The chip package of claim 1, wherein said first semiconductor chip comprises a central-processing-unit (CPU) circuit block and a graphics-processing-unit (GPU) circuit block.
Claim 3(a)	The chip package of claim 1, wherein said first interconnection scheme further comprises a fourth metal interconnect over said first metal interconnect and said polymer layer,
Claim 3(b)	wherein said polymer layer is between said first and fourth metal interconnects,
Claim 3(c)	wherein said fourth metal interconnect comprises a fourth metal layer and a fourth copper layer over said fourth metal layer.
Claim 4	The chip package of claim 1, wherein said first metal pad is an aluminum pad.
Claim 5	The chip package of claim 1, wherein said compound comprises a SiO2 compound.
Claim 6(a)	The chip package of claim 1, further comprising a second semiconductor chip over said first semiconductor chip, wherein said second semiconductor chip comprises a second metal bump on a second metal pad of said second semiconductor chip,
Claim 6(b)	wherein said second metal bump comprises a second tin-containing layer.

Claim Designation	Claim Language
Claim 7	The chip package of claim 1, wherein said solid layer further comprises a third region opposite to said second region, wherein said third region is between said first region and a second edge of said solid layer, wherein said plurality of metal posts in said plurality of through holes in said third region respectively.
Claim 8	The chip package of claim 1, wherein said second region is a rectangle region and surrounding said first region.
Claim 9	The chip package of claim 1, further comprising another said first semiconductor chip under said second surface.
Claim 10(Pre)	A chip package comprising:
Claim 10(a)	a solid layer having a first surface and a second surface opposite to said first surface,
Claim 10(a)(i)	wherein said solid layer comprises a compound of silicon and oxygen,
Claim 10(a)(ii)	wherein said solid layer has a thickness between 100 and 300 micrometers,
Claim 10(a)(iii)	wherein said solid layer comprises a first region and a second region between said first region and a first edge of said solid layer;
Claim 10(b)	a plurality of copper posts in a plurality of through holes in said second region respectively,
Claim 10(b)(i)	wherein said first region has a width in a direction greater than a shortest distance between a sidewall of one of said plurality of through holes and said first edge in said direction and greater than a pitch between two neighboring copper posts of said plurality of copper posts;
Claim 10(c)	a first interconnection scheme over said first surface,
Claim 10(c)(i)	wherein said first interconnection scheme comprises a first metal interconnect over said first surface, and a polymer layer over said first metal interconnect,
Claim 10(c)(ii)	wherein said first metal interconnect is connected to one of said plurality of copper posts,
Claim 10(c)(iii)	wherein said first metal interconnect comprises a first metal layer and a first copper layer over said first metal layer;
Claim 10(d)	a first metal bump over said first interconnection scheme,
Claim 10(d)(i)	wherein said first metal bump comprises a first tin-containing layer;

Claim Designation	Claim Language
Claim 10(e)	a second metal bump over said first interconnection scheme;
Claim 10(f)	a first semiconductor chip over said first interconnection scheme and between said first and second metal bumps,
Claim 10(f)(i)	wherein said first semiconductor chip has a height between a backside surface of said first semiconductor chip and a top surface of said polymer layer is smaller than a thickness of said first metal bump,
Claim 10(f)(ii)	wherein said first semiconductor chip comprises a third metal bump on a first metal pad of said first semiconductor chip, wherein said third metal bump comprises a second tin-containing layer; and
Claim 10(g)	a second semiconductor chip over said first interconnection scheme,
Claim 10(g)(i)	wherein said second semiconductor chip comprises a fourth metal bump on a second metal pad of said second semiconductor chip, wherein said fourth metal bump comprises a third tin-containing layer.
Claim 11	The chip package of claim 10, wherein said compound comprises a SiO2 compound.
Claim 12	The chip package of claim 10, wherein no any copper post in said first region.
Claim 13(a)	The chip package of claim 10, further comprising a third semiconductor chip under said first interconnection scheme,
Claim 13(b)	wherein said third semiconductor chip comprises a second metal interconnect on a third metal pad of said third semiconductor chip,
Claim 13(c)	wherein said second metal interconnect comprises a second metal layer on said third metal pad and a second copper layer over said second metal layer, wherein said second copper layer has a thickness between 5 and 30 micrometers.
Claim 14(a)	The chip package of claim 10, further comprising a third semiconductor chip under said first interconnection scheme,
Claim 14(b)	wherein said third semiconductor chip comprises a second metal interconnect on a third metal pad of said third semiconductor chip,

Claim Designation	Claim Language
Claim 14(c)	wherein said second metal interconnect comprises a second metal layer on said third metal pad and a second copper layer over said second metal layer,
Claim 14(d)	wherein said third semiconductor chip comprises a central-processing-unit (CPU) circuit block and a graphics-processing-unit (GPU) circuit block.
Claim 15	The chip package of claim 10, wherein said solid layer further comprises a third region opposite to said second region, wherein said third region is between said first region and a second edge of said solid layer, wherein said plurality of copper posts in said plurality of through holes in said third region respectively.
Claim 16	The chip package of claim 10, wherein said second region is a rectangle region and surrounding said first region.
Claim 17(a)	The chip package of claim 10, further comprising an electrical device under said second surface, wherein said electrical device comprise a third semiconductor chip and a metal wire connected to a third metal pad of said third semiconductor chip,
Claim 17(b)	wherein said third semiconductor chip is a DRAM chip.
Claim 18(Pre)	A chip package comprising:
Claim 18(a)	a solid layer having a first surface and a second surface opposite to said first surface,
Claim 18(a)(i)	wherein said solid layer comprises a compound of silicon and oxygen,
Claim 18(a)(ii)	wherein said solid layer has a thickness between 50 and 150 micrometers,
Claim 18(a)(iii)	wherein said solid layer comprises a first region and a second region between said first region and a first edge of said solid layer;
Claim 18(b)	a plurality of copper posts in a plurality of through holes in said second region respectively;
Claim 18(c)	a first interconnection scheme over said first surface,
Claim 18(c)(i)	wherein said first interconnection scheme comprises first and second metal interconnects over said first surface, and a first polymer layer over said first and second metal interconnects,
Claim 18(c)(ii)	wherein said first metal interconnect is connected to a first copper post of said plurality of copper posts,

Claim Designation	Claim Language
Claim 18(c)(iii)	wherein said first metal interconnect comprises a first metal layer and a first copper layer over said first metal layer;
Claim 18(d)	a first semiconductor chip over said first interconnection scheme,
Claim 18(d)(i)	wherein said first semiconductor chip comprises a third metal interconnect under a first metal pad of said first semiconductor chip,
Claim 18(d)(ii)	wherein said third metal interconnect comprises a second metal layer under said first metal pad and a second copper layer under said second metal layer, wherein said second copper layer has a thickness between 5 and 30 micrometers,
Claim 18(d)(iii)	wherein said first semiconductor chip is coupled to a second copper post of said plurality of copper posts through said third metal interconnect;
Claim 18(e)	a second semiconductor chip over said first interconnection scheme,
Claim 18(e)(i)	wherein said second semiconductor chip comprises a second metal pad coupled to said second metal interconnect;
Claim 18(f)	a third semiconductor chip under said first interconnection scheme; and
Claim 18(g)	a plurality of metal bumps under said second surface, wherein one of said plurality of metal bumps comprises a tin-containing layer.
Claim 19	The chip package of claim 18, wherein said compound comprises a SiO2 compound.
Claim 20	The chip package of claim 18, wherein said solid layer further comprises a third region opposite to said second region, wherein said third region is between said first region and a second edge of said solid layer, wherein said plurality of copper posts in said plurality of through holes in said third region respectively.
Claim 21(a)	The chip package of claim 18, further comprising a fourth semiconductor chip over said first semiconductor chip,
Claim 21(b)	wherein said fourth semiconductor chip comprises a third metal pad at a bottom surface of said fourth semiconductor chip,
Claim 21(c)	wherein said first semiconductor chip further comprising a plurality of through-silicon-via metal layers and a fourth metal pad at a top surface of said first semiconductor chip,

Claim Designation	Claim Language
Claim 21(d)	wherein said first metal pad is at a bottom surface of said first semiconductor chip,
Claim 21(e)	wherein said first metal pad is coupled to said fourth metal pad through one of said plurality of through-silicon-via metal layers,
Claim 21(f)	wherein said third metal pad is coupled to said fourth metal pad through a solder layer.
Claim 22	The chip package of claim 18, wherein said first semiconductor chip is a graphics-processing-unit (GPU) chip.
Claim 23	The chip package of claim 18, wherein said second semiconductor chip is a logic chip.
Claim 24	The chip package of claim 18, wherein said first semiconductor chip is a logic chip.
Claim 25	The chip package of claim 18, wherein said third semiconductor chip has a thickness between a backside surface of said third semiconductor chip and a top surface of said third semiconductor chip is smaller than a thickness of one of said plurality of metal bumps.
Claim 26	The chip package of claim 18, further comprising another said first semiconductor chip over said first interconnection scheme.
Claim 27(a)	The chip package of claim 18, further comprising a fourth semiconductor chip under said first interconnection scheme,
Claim 27(b)	wherein said fourth semiconductor chip has a thickness between a backside surface of said fourth semiconductor chip and a top surface of said fourth semiconductor chip is smaller than a thickness of one of said plurality of metal bumps.

APPENDIX OF EXHIBITS

Exhibit 1001	U.S. Patent No. 11,894,306
Exhibit 1002	File History of the '306 Patent
Exhibit 1003	Declaration of Stanley Shanfield, Ph.D.
Exhibit 1004	U.S. Patent No. 9,167,694 to Sundaram, et al.
Exhibit 1005	U.S. Patent Publication No. 2010/0290191 to Lin, et al.
Exhibit 1006	U.S. Patent Publication No. 2011/0215458 to Camacho, et al.
Exhibit 1007	U.S. Patent No. 9,679,863 to Lin, et al.
Exhibits 1008-1009	Intentionally left blank
Exhibit 1010	U.S. Patent No. 9,123,763 to Yu, et al.
Exhibit 1011	Intentionally left blank
Exhibit 1012	Andrea Chen, et al. *Semiconductor Packaging Materials Interaction and Reliability*, CRC Press, 2012
Exhibit 1013	Philip Garrou, et al., *RDL: an integral part of today's advanced packaging technologies*, Solid State Technology, May 2011
Exhibit 1014	U.S. Patent No. 8,780,576 to Haba, et al.
Exhibit 1015	U.S. Patent No. 7,902,648 to Lee
Exhibit 1016	U.S. Patent No. 7,964,961 to Lee, et al.
Exhibit 1017	U.S. Patent No. 7,241,641 to Savastiouk, et al.
Exhibit 1018	U.S. Patent Publication No. 2005/0110168 to Chuang
Exhibit 1019	U.S. Patent Publication No. 2011/0026232 to Lin, et al.
Exhibit 1020	U.S. Patent No. 5,086,558 to Grube, et al.
Exhibit 1021	U.S. Patent Publication No. 2011/0193219 to Lai, et al.
Exhibit 1022	U.S. Patent No. 6,818,545 to Lee, et al.
Exhibit 1023	U.S. Patent No. 6,974,659 to Su, et al.
Exhibit 1024	U.S. Patent Publication No. 2006/0175686 to Murata, et al.
Exhibit 1025	U.S. Patent Publication No. 2012/0098124 to Wu, et al.
Exhibit 1026	U.S. Patent No. 8,193,604 to Lin et al.
Exhibit 1027	U.S. Patent Publication No. 2004/0203224 to Halahan, et al.
Exhibit 1028	Philip Garrou, *Introduction to 3D Integration,* Handbook of 3D integration: Volumes 1 and 2, Technology and Application of 3D Integrated Circuits, 2012
Exhibit 1029	U.S. Patent Publication No. 2003/0068877 to Kinsman.
Exhibit 1030	U.S. Patent Publication No. 2010/0246152 to Lin, et al.
Exhibit 1031	Yi Yang, et al, *CPU-Assisted GPGPU on Fused CPU-GPU Architectures,* IEEE Xplore
Exhibit 1032	File History of U.S. Patent No. 11,107,768
Exhibit 1033	U.S. Patent No. 4,863,773 to Rousseau, et al.

Exhibit 1034	U.S. Patent No. 6,365,265 to Tose, et al.
Exhibit 1035	E.D. Blackshear, et al., *The evolution of build-up package technology and its design challenges*, International Business Machines Corporation, 2005
Exhibit 1036	Intentionally left blank
Exhibit 1037	U.S. Patent No. 7,374,969 to Cho, et al.
Exhibit 1038	U.S. Patent No. 7,199,036 to Chan, et al.
Exhibit 1039	U.S. Patent No. 8,158,508 to Lin, et al.
Exhibit 1040	U.S. Patent No. 6,619,538 to Test, et al.
Exhibit 1041	U.S. Patent Publication No. 2011/0101523 to Hwang, et al.
Exhibit 1042	U.S. Patent No. 6,831,003 to Huang, et al.
Exhibit 1043	U.S. Patent Publication No. 2009/0226611 to Suzuki, et al.
Exhibit 1044	U.S. Patent No. 6,077,726 to Mistry, et al.
Exhibit 1045	U.S. Patent Publication No. 2010/0244245 to Pendse, et al.,
Exhibit 1046	U.S. Patent Publication No. 2012/0206160 to Wu, et al.
Exhibit 1047	U.S. Patent Publication No. 2009/0174052 to Sogawa, et al.
Exhibits 1048-1053	Intentionally left blank
Exhibit 1054	U.S. Patent No. 6,489,240 to Iacoponi, et al.
Exhibit 1055	U.S. Patent No. 6,578,178 to Mau
Exhibit 1056	U.S. Patent Publication No. 2012/0001190 to Okabe, et al.
Exhibit 1057	U.S. Patent No. 7,307,348 to Wood, et al.
Exhibit 1058	U.S. Patent No. 8,138,014 to Chi, et al.
Exhibit 1059	U.S. Patent No. 6,506,672 to Dagenais, et al.
Exhibit 1060	U.S. Patent No. 8,518,798 to Graetz.
Exhibit 1061	U.S. Patent Publication No. 2009/0261473 to Lee, et al.
Exhibit 1062	Intentionally left blank
Exhibit 1063	U.S. Patent No. 6,812,143 to Lane, et al.
Exhibit 1064	Intentionally left blank
Exhibit 1065	Intentionally left blank
Exhibit 1066	U.S. Patent Publication No. 2009/0070727 to Solomon.
Exhibit 1067	U.S. Patent Publication No. 2012/0098114 to Ishibashi.
Exhibit 1068	U.S. Patent Publication No. 2011/0074028 to Pendse.
Exhibit 1069	U.S. Patent No. 7,485,955 to Kang, et al.
Exhibit 1070	U.S. Patent Publication No. 2012/0104623 to Pagaila, et al.
Exhibit 1071	Intentionally left blank
Exhibit 1072	U.S. Patent No. 7,772,880 to Solomon.
Exhibit 1073	U.S. Patent No. 7,989,270 to Huang, et al.
Exhibit 1074	U.S. Patent Publication No. 2011/0304999 to Yu, et al.

Exhibits 1075-1079	Intentionally left blank
Exhibit 1080	U.S. Patent Publication No. 2012/0319251 to Yu, et al.
Exhibits 1081-1082	Intentionally left blank
Exhibit 1083	U.S. Patent Publication No. 2009/0166069 to Kinoshita.
Exhibits 1084-1092	Intentionally left blank
Exhibit 1093	U.S. Patent No. 6,107,180 to Munroe, et al.
Exhibit 1094	U.S. Patent Publication No. 2011/0210283 to Ramirez, et al.
Exhibit 1095	U.S. Patent No. 6,542,502 to Dishongh, et al.
Exhibit 1096	Intentionally left blank
Exhibit 1097	Richard K. Ulrich, et al., *Advanced Electronic Packaging,* IEEE Press Series on Microelectrical Systems, 2006
Exhibit 1098	Mulugeta Abtew, et al., *Lead-free Solders in Microelectronics*, Materials Science and Engineering, 2000
Exhibit 1099	Karl J. Puttlitz, et al., *Handbook of Lead-Free Solder Technology for Microelectronic Assemblies*, 2005
Exhibit 1100	Intentionally left blank
Exhibit 1101	U.S. Patent Publication No. 2013/0151869 to Steinman, et al.
Exhibit 1102	Linely Gwennap, *Sandy Bridge Spans Generations: Intel Focuses on Graphics, Multimedia in New Processor Design*, Microprocessor, 2010
Exhibit 1103	U.S. Patent No. 6,330,164 to Khandros, et al.
Exhibit 1104	U.S. Patent No. 6,710,447 to Nogami.
Exhibits 1105-1116	Intentionally left blank
Exhibit 1117	U.S. Patent No. 11,538,763 File History
Exhibits 1118-1119	Intentionally left blank
Exhibit 1120	U.S. Patent No. 6,282,100 to Degani, et al.
Exhibit 1121	U.S. Patent No. 6,818,980 to Pedron.
Exhibit 1122	U.S. Patent No. 6,842,391 to Fujioka, et al.
Exhibit 1123	U.S. Patent No. 7,193,917 to Takahashi, et al.
Exhibit 1124	U.S. Patent No. 4,603,345 to Lee, et al.
Exhibit 1125	U.S. Patent Publication No. 2012/0146177 to Choi, et al.
Exhibit 1126	U.S. Patent No. 8,592,988 to Lee, et al.
Exhibit 1127	U.S. Patent No. 8,238,113 to Iihola, et al.
Exhibit 1128	U.S. Patent No. 6,528,179 to Jimarez, et al.

Exhibit 1129	U.S. Patent No. 6,468,413 to Fanti, et al.
Exhibit 1130	U.S. Patent No. 8,132,775 to Goldmann.
Exhibit 1131	U.S. Patent Publication No. 2011/0186977 to Chi, et al.
Exhibit 1132	U.S. Patent No. 7,169,627 to Duh, et al.
Exhibit 1133	U.S. Patent No. 6,614,243 to Klehn, et al.
Exhibit 1134	U.S. Patent Publication No. 2009/0162622 to Van Veen, et al.
Exhibit 1135	U.S. Patent No. 6,570,259 to Alcoe, et al.
Exhibit 1136	U.S. Patent No. 7,741,567 to Beddingfield, et al.
Exhibit 1137	U.S. Patent No. 6,407,341 to Anstrom, et al.

CERTIFICATION OF WORD COUNT

The undersigned certifies pursuant to 37 C.F.R. § 42.24 that the foregoing Petition for *Inter Partes* Review, excluding any table of contents, mandatory notices under 37 C.F.R. § 42.8, certificates of service or word count, or appendix of exhibits, contains 12,835 words according to the word-processing program used to prepare this document (Microsoft Word).

Dated: November 21, 2025

Respectfully submitted,

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CERTIFICATE OF SERVICE ON PATENT OWNER
UNDER 37 C.F.R. § 42.105

Pursuant to 37 C.F.R. §§ 42.6(e) and 42.105(b), the undersigned certifies that on November 21, 2025, a complete and entire copy of this Petition for *Inter Partes* Review and Exhibits were provided via Federal Express to the Patent Owner by serving the correspondence address of record for the '306 Patent:

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