

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY LTD.,

and

APPLE INC.,

Petitioners

v.

MYW SEMITECH, LLC,

Patent Owner

Inter Partes Review Case No. IPR2026-00067

U.S. Patent No. 11,894,306

DECLARATION OF STANLEY SHANFIELD, PH. D.

TABLE OF CONTENTS

I.	INTRODUCTION.....	33
A.	EDUCATIONAL BACKGROUND AND PROFESSIONAL EXPERIENCE	33
B.	MATERIALS CONSIDERED	36
II.	OVERVIEW AND LEGAL STANDARDS	43
A.	PERSON OF ORDINARY SKILL IN THE ART	44
B.	OBVIOUSNESS	45
C.	CLAIM CONSTRUCTION	50
III.	OVERVIEW OF THE ‘306 PATENT.....	50
A.	SUMMARY OF THE ’306 PATENT.....	50
B.	FIELD OF ENDEAVOR.....	55
C.	PROBLEM SOLVED BY THE INVENTORS OF THE ‘306 PATENT	56
IV.	LEVEL OF ORDINARY SKILL	57
V.	OVERVIEW OF THE TECHNOLOGY	58
A.	HISTORY OF CHIP PACKAGING	58
B.	INTERPOSERS AND DIELECTRIC MATERIALS.....	61
C.	COEFFICIENT OF THERMAL EXPANSION	65
D.	THROUGH VIAS AND METAL PLUGS.....	68
E.	SOLDER BUMPS.....	71
F.	METHODS OF FORMING SOLDER BUMPS	75
G.	INTERCONNECTION SCHEMES AND REDISTRIBUTION LAYERS	80
H.	SEMICONDUCTOR CHIPS.....	83
VI.	SUMMARY OF THE PRIOR ART REFERENCES	88
A.	SUNDARAM.....	88
B.	LIN-191	92
C.	LIN-863	98
D.	YU	100
E.	CAMACHO.....	105

VII. SUMMARY OF UNPATENTABILITY	109
VIII. OPINIONS REGARDING GROUND 1A: CLAIMS 1-7, 9-11, 13-15, AND 17-27 ARE OBVIOUS OVER SUNDARAM AND LIN-191.....	110
A. CLAIM 1	110
1. 1(Pre): “A chip package comprising”	110
2. 1(a): “a solid layer having a first surface and a second surface opposite to said first surface,”	111
3. 1(a)(i): “wherein said solid layer comprises a compound of silicon and oxygen,”	113
4. 1(a)(ii): “wherein said solid layer has a thickness between 50 and 150 micrometers,”	114
5. 1(a)(iii): “wherein said solid layer comprises a first region and a second region between said first region and a first edge of said solid layer;”	115
6. 1(b): “a plurality of metal posts in a plurality of through holes in said second region respectively,”	116
7. 1(b)(i): “wherein one of said plurality of metal posts comprises a first copper layer contacting a sidewall of one of said plurality of through holes,”	117
8. 1(b)(ii): “wherein said first region has a width in a direction greater than a shortest distance between said sidewall of one of said plurality of through holes and said first edge in said direction and greater than a pitch between two neighboring metal posts of said plurality of metal posts;”	119
9. 1(c): “a first interconnection scheme over said first surface,”	121
10. 1(c)(i): “wherein said first interconnection scheme comprises a first metal interconnect over said second surface and a polymer layer over said first metal interconnect,”	124

11.	<i>1(c)(ii): “wherein said first metal interconnect is connected to a first metal post of said plurality of metal posts,”</i>	128
12.	<i>1(c)(iii): “wherein said first metal interconnect comprises a first metal layer and a second copper layer over said first metal layer;”</i>	129
13.	<i>1(d): “a first metal bump over said first interconnection scheme,”</i>	131
14.	<i>1(d)(i): “wherein said first metal bump comprises a second metal layer and a first tin-containing layer over said second metal layer; and”</i>	132
	a) Sundaram’s Teachings	132
	b) Lin-191’s Teachings	133
	c) Motivation to Combine	134
15.	<i>1(e): “a first semiconductor chip under said second surface,”</i>	138
16.	<i>1(e)(i): “wherein said first interconnection scheme comprise a second metal interconnect across over a sidewall of the first semiconductor chip,”</i>	139
	a) “Second Metal Interconnect”	139
	b) “Across Over a Sidewall”	140
17.	<i>1(e)(ii): “wherein said first semiconductor chip comprises a third metal interconnect on a first metal pad of said first semiconductor chip,”</i>	143
	a) Lin-191’s Metal Pad Teachings	145
	b) Motivation to Combine	146
18.	<i>1(e)(iii): “wherein said third metal interconnect comprises a third metal layer on said first metal pad and a third copper layer over said third metal layer, wherein said third copper layer has a thickness between 5 and 30 micrometers,”</i>	147
	a) Lin-191’s Teachings	147

b)	Motivation to Combine	149
19.	<i>1(e)(iv): “wherein said first semiconductor chip is connected to a second metal post of said plurality of metal posts through said third metal interconnect.”</i>	<i>153</i>
B.	CLAIM 2: “THE CHIP PACKAGE OF CLAIM 1, WHEREIN SAID FIRST SEMICONDUCTOR CHIP COMPRISES A CENTRAL-PROCESSING-UNIT (CPU) CIRCUIT BLOCK AND A GRAPHICS-PROCESSING-UNIT (GPU) CIRCUIT BLOCK.”	155
a)	Lin-191’s Teachings.....	155
b)	Motivation to Combine	156
C.	CLAIM 3	159
1.	<i>3(a) “The chip package of claim 1, wherein said first interconnection scheme further comprises a fourth metal interconnect over said first metal interconnect and said polymer layer,”</i>	<i>159</i>
2.	<i>3(b): “wherein said polymer layer is between said first and fourth metal interconnects,”</i>	<i>161</i>
3.	<i>3(c): “wherein said fourth metal interconnect comprises a fourth metal layer and a fourth copper layer over said fourth metal layer.”</i>	<i>163</i>
a)	Sundaram’s Teachings	163
b)	Lin-191’s Teachings.....	163
c)	Motivation to Combine	164
D.	CLAIM 4: “THE CHIP PACKAGE OF CLAIM 1, WHEREIN SAID FIRST METAL PAD IS AN ALUMINUM PAD.”	168
E.	CLAIM 5: “THE CHIP PACKAGE OF CLAIM 1, WHEREIN SAID COMPOUND COMPRISES A SiO ₂ COMPOUND.”	170
F.	CLAIM 6	170
1.	<i>6(a): “The chip package of claim 1, further comprising a second semiconductor chip over said first semiconductor chip, wherein said second semiconductor chip comprises</i>	

	<i>a second metal bump on a second metal pad of said second semiconductor chip,”</i>	<i>170</i>
2.	<i>6(b): “wherein said second metal bump comprises a second tin-containing layer.”</i>	<i>172</i>
G.	CLAIM 7: “THE CHIP PACKAGE OF CLAIM 1, WHEREIN SAID SOLID LAYER FURTHER COMPRISES A THIRD REGION OPPOSITE TO SAID SECOND REGION, WHEREIN SAID THIRD REGION IS BETWEEN SAID FIRST REGION AND A SECOND EDGE OF SAID SOLID LAYER, WHEREIN SAID PLURALITY OF METAL POSTS IN SAID PLURALITY OF THROUGH HOLES IN SAID THIRD REGION RESPECTIVELY.”	173
H.	CLAIM 9: “THE CHIP PACKAGE OF CLAIM 1, FURTHER COMPRISING ANOTHER SAID FIRST SEMICONDUCTOR CHIP UNDER SAID SECOND SURFACE.”	174
A.	CLAIM 10:	175
1.	<i>10(Pre): “A chip package comprising:”</i>	<i>175</i>
2.	<i>10(a): “a solid layer having a first surface and a second surface opposite to said first surface,”</i>	<i>176</i>
3.	<i>10(a)(i): “wherein said solid layer comprises a compound of silicon and oxygen,”</i>	<i>176</i>
4.	<i>10(a)(ii): “wherein said solid layer has a thickness between 100 and 300 micrometers,”</i>	<i>176</i>
5.	<i>10(a)(iii): “wherein said solid layer comprises a first region and a second region between said first region and a first edge of said solid layer;”</i>	<i>177</i>
6.	<i>10(b): “a plurality of copper posts in a plurality of through holes in said second region respectively,”</i>	<i>177</i>
7.	<i>10(b)(i): “wherein said first region has a width in a direction greater than a shortest distance between a sidewall of one of said plurality of through holes and said first edge in said direction and greater than a pitch between two neighboring copper posts of said plurality of copper posts;”</i>	<i>178</i>
8.	<i>10(c): “a first interconnection scheme over said first surface,”</i>	<i>178</i>

9.	10(c)(i): “wherein said first interconnection scheme comprises a first metal interconnect over said first surface, and a polymer layer over said first metal interconnect,”	178
10.	10(c)(ii): “wherein said first metal interconnect is connected to one of said plurality of copper posts,”	178
11.	10(c)(iii): “wherein said first metal interconnect comprises a first metal layer and a first copper layer over said first metal layer;”	178
12.	10(d): “a first metal bump over said first interconnection scheme,”	179
13.	10(d)(i): “wherein said first metal bump comprises a first tin-containing layer;”	179
14.	10(e): “a second metal bump over said first interconnection scheme;”	179
15.	10(f): “a first semiconductor chip over said first interconnection scheme and between said first and second metal bumps,”	180
16.	10(f)(i): “wherein said first semiconductor chip has a height between a backside surface of said first semiconductor chip and a top surface of said polymer layer is smaller than a thickness of said first metal bump,”	180
	a) Sundaram’s Teachings	181
17.	10(f)(ii): “wherein said first semiconductor chip comprises a third metal bump on a first metal pad of said first semiconductor chip, wherein said third metal bump comprises a second tin-containing layer; and”	183
18.	10(g): “a second semiconductor chip over said first interconnection scheme,”	183
19.	10(g)(i): “wherein said second semiconductor chip comprises a fourth metal bump on a second metal pad of said second semiconductor chip, wherein said fourth metal bump comprises a third tin-containing layer.”	184

B.	CLAIM 11: “THE CHIP PACKAGE OF CLAIM 10, WHEREIN SAID COMPOUND COMPRISES A SiO ₂ COMPOUND.”	186
C.	CLAIM 13	186
1.	13(a): “The chip package of claim 10, further comprising a third semiconductor chip under said first interconnection scheme,”	186
2.	13(b): “wherein said third semiconductor chip comprises a second metal interconnect on a third metal pad of said third semiconductor chip,”	187
3.	13(c): “wherein said second metal interconnect comprises a second metal layer on said third metal pad and a second copper layer over said second metal layer, wherein said second copper layer has a thickness between 5 and 30 micrometers.”	188
D.	CLAIM 14	188
1.	14(a): “The chip package of claim 10, further comprising a third semiconductor chip under said first interconnection scheme,”	188
2.	14(b): “wherein said third semiconductor chip comprises a second metal interconnect on a third metal pad of said third semiconductor chip,”	189
3.	14(c): “wherein said second metal interconnect comprises a second metal layer on said third metal pad and a second copper layer over said second metal layer,”	190
4.	14(d): “wherein said third semiconductor chip comprises a central-processing-unit (CPU) circuit block and a graphics-processing-unit (GPU) circuit block.”	190
E.	CLAIM 15: “THE CHIP PACKAGE OF CLAIM 10, WHEREIN SAID SOLID LAYER FURTHER COMPRISES A THIRD REGION OPPOSITE TO SAID SECOND REGION, WHEREIN SAID THIRD REGION IS BETWEEN SAID FIRST REGION AND A SECOND EDGE OF SAID SOLID LAYER, WHEREIN SAID PLURALITY OF COPPER POSTS IN SAID PLURALITY OF THROUGH HOLES IN SAID THIRD REGION RESPECTIVELY.”	190

F.	CLAIM 17	191
1.	<i>17(a): “The chip package of claim 10, further comprising an electrical device under said second surface, wherein said electrical device comprise a third semiconductor chip and a metal wire connected to a third metal pad of said third semiconductor chip,”</i>	<i>191</i>
a)	Motivation to Combine Sundaram’s Internal Embodiments.....	192
2.	<i>17(b): “wherein said third semiconductor chip is a DRAM chip.”</i>	<i>194</i>
A.	CLAIM 18	195
1.	<i>18(Pre): “A chip package comprising”</i>	<i>195</i>
2.	<i>18(a): “a solid layer having a first surface and a second surface opposite to said first surface,”</i>	<i>195</i>
3.	<i>18(a)(i): “wherein said solid layer comprises a compound of silicon and oxygen,”</i>	<i>196</i>
4.	<i>18(a)(ii): “wherein said solid layer has a thickness between 50 and 150 micrometers;”</i>	<i>196</i>
5.	<i>18(a)(iii): “wherein said solid layer comprises a first region and a second region between said first region and a first edge of said solid layer;”</i>	<i>196</i>
6.	<i>18(b): “a plurality of copper posts in a plurality of through holes in said second region respectively,.....</i>	<i>197</i>
7.	<i>18(c): “a first interconnection scheme over said first surface,”</i>	<i>197</i>
8.	<i>18(c)(i): “wherein said first interconnection scheme comprises first and second metal interconnects over said first surface, and a first polymer layer over said first and second metal interconnects,”</i>	<i>198</i>
9.	<i>18(c)(ii): “wherein said first metal interconnect is connected to a first copper post of said plurality of copper posts,”</i>	<i>199</i>

10.	18(c)(iii): “wherein said first metal interconnect comprises a first metal layer and a first copper layer over said first metal layer;”	200
11.	18(d): “a first semiconductor chip over said first interconnection scheme,”	201
12.	18(d)(i): “wherein said first semiconductor chip comprises a third metal interconnect under a first metal pad of said first semiconductor chip,”	201
13.	18(d)(ii): “wherein said third metal interconnect comprises a second metal layer under said first metal pad and a second copper layer under said second metal layer, wherein said second copper layer has a thickness between 5 and 30 micrometers,”	202
14.	18(d)(iii): “wherein said first semiconductor chip is coupled to a second copper post of said plurality of copper posts through said third metal interconnect;”	203
15.	18(e): “a second semiconductor chip over said first interconnection scheme,”	204
16.	18(e)(i): “wherein said second semiconductor chip comprises a second metal pad coupled to said second metal interconnect;”	205
17.	18(f): “a third semiconductor chip under said first interconnection scheme; and”	207
18.	18(g): “a plurality of metal bumps under said second surface, wherein one of said plurality of metal bumps comprises a tin-containing layer.”	208
B.	CLAIM 19: “THE CHIP PACKAGE OF CLAIM 18, WHEREIN SAID COMPOUND COMPRISES A SiO ₂ COMPOUND.”	209
C.	CLAIM 20: “THE CHIP PACKAGE OF CLAIM 18, WHEREIN SAID SOLID LAYER FURTHER COMPRISES A THIRD REGION OPPOSITE TO SAID SECOND REGION, WHEREIN SAID THIRD REGION IS BETWEEN SAID FIRST REGION AND A SECOND EDGE OF SAID SOLID LAYER, WHEREIN SAID PLURALITY OF COPPER POSTS IN SAID PLURALITY OF THROUGH HOLES IN SAID THIRD REGION RESPECTIVELY.”	210

D.	CLAIM 21	210
1.	21(a): “The chip package of claim 18, further comprising a fourth semiconductor chip over said first semiconductor chip,”	210
2.	21(b): “wherein said fourth semiconductor chip comprises a third metal pad at a bottom surface of said fourth semiconductor chip,”	211
3.	21(c): “wherein said first semiconductor chip further comprising a plurality of through-silicon-via metal layers and a fourth metal pad at a top surface of said first semiconductor chip,”	213
4.	21(d): “wherein said first metal pad is at a bottom surface of said first semiconductor chip,”	215
5.	21(e): “wherein said first metal pad is coupled to said fourth metal pad through one of said plurality of through-silicon-via metal layers,”	216
6.	21(f): “wherein said third metal pad is coupled to said fourth metal pad through a solder layer.”	217
E.	CLAIM 22: “THE CHIP PACKAGE OF CLAIM 18, WHEREIN SAID FIRST SEMICONDUCTOR CHIP IS A GRAPHICS-PROCESSING-UNIT (GPU) CHIP.”	221
F.	CLAIM 23: “THE CHIP PACKAGE OF CLAIM 18, WHEREIN SAID SECOND SEMICONDUCTOR CHIP IS A LOGIC CHIP.”	222
	a) Motivation to Combine Sundaram’s Internal Embodiments	223
G.	CLAIM 24: “THE CHIP PACKAGE OF CLAIM 18, WHEREIN SAID FIRST SEMICONDUCTOR CHIP IS A LOGIC CHIP.”	224
H.	CLAIM 25: “THE CHIP PACKAGE OF CLAIM 18, WHEREIN SAID THIRD SEMICONDUCTOR CHIP HAS A THICKNESS BETWEEN A BACKSIDE SURFACE OF SAID THIRD SEMICONDUCTOR CHIP AND A TOP SURFACE OF SAID THIRD SEMICONDUCTOR CHIP IS SMALLER THAN A THICKNESS OF ONE OF SAID PLURALITY OF METAL BUMPS.”	224

I.	CLAIM 26: “THE CHIP PACKAGE OF CLAIM 18, FURTHER COMPRISING ANOTHER SAID FIRST SEMICONDUCTOR CHIP OVER SAID FIRST INTERCONNECTION SCHEME.”	226
J.	CLAIM 27	227
1.	27(a): “The chip package of claim 18, further comprising a fourth semiconductor chip under said first interconnection scheme,”	227
2.	27(b): “wherein said fourth semiconductor chip has a thickness between a backside surface of said fourth semiconductor chip and a top surface of said fourth semiconductor chip is smaller than a thickness of one of said plurality of metal bumps.”	228
IX.	OPINIONS REGARDING GROUND 1B: CLAIMS 8, 12, AND 16 ARE OBVIOUS OVER SUNDARAM, LIN-191, AND LIN-863	230
A.	CLAIM 8: “THE CHIP PACKAGE OF CLAIM 1, WHEREIN SAID SECOND REGION IS A RECTANGLE REGION AND SURROUNDING SAID FIRST REGION.”	230
a)	The ‘306 Patent’s “First Region” and “Second Region”	230
b)	Sundaram’s Teachings	231
c)	Lin-863’s Teachings	238
d)	Motivation to Combine	240
B.	CLAIM 12: “THE CHIP PACKAGE OF CLAIM 10, WHEREIN NO ANY COPPER POST IN SAID FIRST REGION.”	243
a)	Lin-863’s Teachings	245
b)	Motivation to Combine	247
C.	CLAIM 16: “THE CHIP PACKAGE OF CLAIM 10, WHEREIN SAID SECOND REGION IS A RECTANGLE REGION AND SURROUNDING SAID FIRST REGION.”	249
X.	OPINIONS REGARDING GROUND 2A: CLAIMS 1-7, 9-15, 17-20, and 22-27 ARE OBVIOUS OVER Yu and Lin-191	249
A.	CLAIM 1	249

1.	<i>1(Pre): “A chip package comprising”</i>	249
2.	<i>1(a): “a solid layer having a first surface and a second surface opposite to said first surface,”</i>	251
3.	<i>1(a)(i): “wherein said solid layer comprises a compound of silicon and oxygen,”</i>	252
4.	<i>1(a)(ii): “wherein said solid layer has a thickness between 50 and 150 micrometers,”</i>	253
	a) Lin-191’s Teachings	253
	b) Motivation to Combine	256
5.	<i>1(a)(iii): “wherein said solid layer comprises a first region and a second region between said first region and a first edge of said solid layer;”</i>	259
6.	<i>1(b): “a plurality of metal posts in a plurality of through holes in said second region respectively,”</i>	259
7.	<i>1(b)(i): “wherein one of said plurality of metal posts comprises a first copper layer contacting a sidewall of one of said plurality of through holes,”</i>	261
8.	<i>1(b)(ii): “wherein said first region has a width in a direction greater than a shortest distance between said sidewall of one of said plurality of through holes and said first edge in said direction and greater than a pitch between two neighboring metal posts of said plurality of metal posts;”</i>	263
9.	<i>1(c): “a first interconnection scheme over said first surface,”</i>	265
10.	<i>1(c)(i): “wherein said first interconnection scheme comprises a first metal interconnect over said second surface and a polymer layer over said first metal interconnect,”</i>	267
11.	<i>1(c)(ii): “wherein said first metal interconnect is connected to a first metal post of said plurality of metal posts,”</i>	268

12.	<i>1(c)(iii): “wherein said first metal interconnect comprises a first metal layer and a second copper layer over said first metal layer;”</i>	269
13.	<i>1(d): “a first metal bump over said first interconnection scheme”</i>	270
14.	<i>1(d)(i): “wherein said first metal bump comprises a second metal layer and a first tin-containing layer over said second metal layer; and”</i>	271
	a) Lin-191’s Teachings and Motivation to Combine	272
15.	<i>1(e): “a first semiconductor chip under said second surface,”</i>	273
16.	<i>1(e)(i): “wherein said first interconnection scheme comprise a second metal interconnect across over a sidewall of the first semiconductor chip,”</i>	274
	a) “Second Metal Interconnect”	274
17.	<i>1(e)(ii): “wherein said first semiconductor chip comprises a third metal interconnect on a first metal pad of said first semiconductor chip,”</i>	276
	a) Lin-191’s Metal Pad Teachings and Motivation to Combine	278
18.	<i>1(e)(iii): “wherein said third metal interconnect comprises a third metal layer on said first metal pad and a third copper layer over said third metal layer, wherein said third copper layer has a thickness between 5 and 30 micrometers,”</i>	279
	a) Lin-191’s Teachings and Motivation to Combine	279
19.	<i>1(e)(iv): “wherein said first semiconductor chip is connected to a second metal post of said plurality of metal posts through said third metal interconnect.”</i>	280
B.	CLAIM 2: “THE CHIP PACKAGE OF CLAIM 1, WHEREIN SAID FIRST SEMICONDUCTOR CHIP COMPRISES A CENTRAL-PROCESSING-UNIT (CPU) CIRCUIT BLOCK AND A GRAPHICS-PROCESSING-UNIT (GPU) CIRCUIT BLOCK.”	282

a)	Lin-191's Teachings.....	282
b)	Motivation to Combine	282
C.	CLAIM 3	283
1.	3(a): <i>"The chip package of claim 1, wherein said first interconnection scheme further comprises a fourth metal interconnect over said first metal interconnect and said polymer layer,"</i>	283
2.	3(b): <i>"wherein said polymer layer is between said first and fourth metal interconnects,"</i>	284
3.	3(c): <i>"wherein said fourth metal interconnect comprises a fourth metal layer and a fourth copper layer over said fourth metal layer."</i>	285
D.	CLAIM 4: "THE CHIP PACKAGE OF CLAIM 1, WHEREIN SAID FIRST METAL PAD IS AN ALUMINUM PAD."	285
a)	Lin-191's Teachings and MTC	285
E.	CLAIM 5: "THE CHIP PACKAGE OF CLAIM 1, WHEREIN SAID COMPOUND COMPRISES A SiO ₂ COMPOUND."	285
a)	Lin-191's Teachings and Motivation to Combine	285
b)	Motivation to Combine	287
F.	CLAIM 6	289
1.	6(a): <i>"The chip package of claim 1, further comprising a second semiconductor chip over said first semiconductor chip, wherein said second semiconductor chip comprises a second metal bump on a second metal pad of said second semiconductor chip,"</i>	289
2.	6(b): <i>"wherein said second metal bump comprises a second tin-containing layer."</i>	291
G.	CLAIM 7: "THE CHIP PACKAGE OF CLAIM 1, WHEREIN SAID SOLID LAYER FURTHER COMPRISES A THIRD REGION OPPOSITE TO SAID SECOND REGION, WHEREIN SAID THIRD REGION IS BETWEEN SAID FIRST REGION AND A SECOND EDGE OF SAID SOLID LAYER, WHEREIN SAID PLURALITY OF METAL POSTS IN SAID PLURALITY OF THROUGH HOLES IN SAID THIRD REGION RESPECTIVELY."	292

H.	CLAIM 9: “THE CHIP PACKAGE OF CLAIM 1, FURTHER COMPRISING ANOTHER SAID FIRST SEMICONDUCTOR CHIP UNDER SAID SECOND SURFACE.”	293
I.	CLAIM 10	294
1.	10(Pre): “A chip package comprising:”	294
2.	10(a): “a solid layer having a first surface and a second surface opposite to said first surface,”	294
3.	10(a)(i): “wherein said solid layer comprises a compound of silicon and oxygen,”	295
4.	10(a)(ii): “wherein said solid layer has a thickness between 100 and 300 micrometers,”	295
5.	10(a)(iii): “wherein said solid layer comprises a first region and a second region between said first region and a first edge of said solid layer;”	296
6.	10(b): “a plurality of copper posts in a plurality of through holes in said second region respectively,”	296
7.	10(b)(i): “wherein said first region has a width in a direction greater than a shortest distance between a sidewall of one of said plurality of through holes and said first edge in said direction and greater than a pitch between two neighboring copper posts of said plurality of copper posts;”	296
8.	10(c): “a first interconnection scheme over said first surface,”	297
9.	10(c)(i): “wherein said first interconnection scheme comprises a first metal interconnect over said first surface, and a polymer layer over said first metal interconnect,”	298
10.	10(c)(ii): “wherein said first metal interconnect is connected to one of said plurality of copper posts,”	299
11.	10(c)(iii): “wherein said first metal interconnect comprises a first metal layer and a first copper layer over said first metal layer;”	299

12.	<i>10(d): “a first metal bump over said first interconnection scheme,”</i>	299
13.	<i>10(d)(i): “wherein said first metal bump comprises a first tin-containing layer;”</i>	300
14.	<i>10(e): “a second metal bump over said first interconnection scheme;”</i>	300
15.	<i>10(f): “a first semiconductor chip over said first interconnection scheme and between said first and second metal bumps,”</i>	301
16.	<i>10(f)(i): “wherein said first semiconductor chip has a height between a backside surface of said first semiconductor chip and a top surface of said polymer layer is smaller than a thickness of said first metal bump,”</i>	302
17.	<i>10(f)(ii): “wherein said first semiconductor chip comprises a third metal bump on a first metal pad of said first semiconductor chip, wherein said third metal bump comprises a second tin-containing layer; and”</i>	303
18.	<i>10(g): “a second semiconductor chip over said first interconnection scheme,”</i>	304
19.	<i>10(g)(i): “wherein said second semiconductor chip comprises a fourth metal bump on a second metal pad of said second semiconductor chip, wherein said fourth metal bump comprises a third tin-containing layer.”</i>	305
J.	CLAIM 11: “THE CHIP PACKAGE OF CLAIM 10, WHEREIN SAID COMPOUND COMPRISES A SiO ₂ COMPOUND.”	306
K.	CLAIM 12: “THE CHIP PACKAGE OF CLAIM 10, WHEREIN NO ANY COPPER POST IN SAID FIRST REGION.”	306
L.	CLAIM 13	307
1.	<i>13(a): “The chip package of claim 10, further comprising a third semiconductor chip under said first interconnection scheme,”</i>	307

2.	<i>13(b): “wherein said third semiconductor chip comprises a second metal interconnect on a third metal pad of said third semiconductor chip,”</i>	308
3.	<i>13(c): “wherein said second metal interconnect comprises a second metal layer on said third metal pad and a second copper layer over said second metal layer, wherein said second copper layer has a thickness between 5 and 30 micrometers.”</i>	308
M.	CLAIM 14	309
1.	<i>14(a): “The chip package of claim 10, further comprising a third semiconductor chip under said first interconnection scheme,”</i>	309
2.	<i>14(b): “wherein said third semiconductor chip comprises a second metal interconnect on a third metal pad of said third semiconductor chip,”</i>	309
3.	<i>14(c): “wherein said second metal interconnect comprises a second metal layer on said third metal pad and a second copper layer over said second metal layer,”</i>	310
4.	<i>14(d): “wherein said third semiconductor chip comprises a central-processing-unit (CPU) circuit block and a graphics-processing-unit (GPU) circuit block.”</i>	310
N.	CLAIM 15: “THE CHIP PACKAGE OF CLAIM 10, WHEREIN SAID SOLID LAYER FURTHER COMPRISES A THIRD REGION OPPOSITE TO SAID SECOND REGION, WHEREIN SAID THIRD REGION IS BETWEEN SAID FIRST REGION AND A SECOND EDGE OF SAID SOLID LAYER, WHEREIN SAID PLURALITY OF COPPER POSTS IN SAID PLURALITY OF THROUGH HOLES IN SAID THIRD REGION RESPECTIVELY.”	310
O.	CLAIM 17	310
1.	<i>17(a): “The chip package of claim 10, further comprising an electrical device under said second surface, wherein said electrical device comprise a third semiconductor chip and a metal wire connected to a third metal pad of said third semiconductor chip,”</i>	310

a.	Lin-191's Teachings and Motivation to Combine Yu and Lin-191	311
2.	17(b): "wherein said third semiconductor chip is a DRAM chip."	314
P.	CLAIM 18	314
1.	18(Pre): "A chip package comprising"	314
2.	18(a): "a solid layer having a first surface and a second surface opposite to said first surface,"	314
3.	18(a)(i): "wherein said solid layer comprises a compound of silicon and oxygen,"	315
4.	18(a)(ii): "wherein said solid layer has a thickness between 50 and 150 micrometers;"	315
5.	18(a)(iii): "wherein said solid layer comprises a first region and a second region between said first region and a first edge of said solid layer;"	315
6.	18(b): "a plurality of copper posts in a plurality of through holes in said second region respectively,	315
7.	18(c): "a first interconnection scheme over said first surface,"	315
8.	18(c)(i): "wherein said first interconnection scheme comprises first and second metal interconnects over said first surface, and a first polymer layer over said first and second metal interconnects,"	315
9.	18(c)(ii): "wherein said first metal interconnect is connected to a first copper post of said plurality of copper posts,"	316
10.	18(c)(iii): "wherein said first metal interconnect comprises a first metal layer and a first copper layer over said first metal layer;"	317
11.	18(d): "a first semiconductor chip over said first interconnection scheme,"	317

12. 18(d)(i): “wherein said first semiconductor chip comprises a third metal interconnect under a first metal pad of said first semiconductor chip,”317
13. 18(d)(ii): “wherein said third metal interconnect comprises a second metal layer under said first metal pad and a second copper layer under said second metal layer, wherein said second copper layer has a thickness between 5 and 30 micrometers,”319
14. 18(d)(iii): “wherein said first semiconductor chip is coupled to a second copper post of said plurality of copper posts through said third metal interconnect;”320
15. 18(e): “a second semiconductor chip over said first interconnection scheme,”321
16. 18(e)(i): “wherein said second semiconductor chip comprises a second metal pad coupled to said second metal interconnect;”322
17. 18(f): “a third semiconductor chip under said first interconnection scheme; and”323
18. 18(g): “a plurality of metal bumps under said second surface, wherein one of said plurality of metal bumps comprises a tin-containing layer.”324
- Q. CLAIM 19: “THE CHIP PACKAGE OF CLAIM 18, WHEREIN SAID COMPOUND COMPRISES A SiO_2 COMPOUND.”325
- R. CLAIM 20: “THE CHIP PACKAGE OF CLAIM 18, WHEREIN SAID SOLID LAYER FURTHER COMPRISES A THIRD REGION OPPOSITE TO SAID SECOND REGION, WHEREIN SAID THIRD REGION IS BETWEEN SAID FIRST REGION AND A SECOND EDGE OF SAID SOLID LAYER, WHEREIN SAID PLURALITY OF COPPER POSTS IN SAID PLURALITY OF THROUGH HOLES IN SAID THIRD REGION RESPECTIVELY.”325
- S. CLAIM 22: “THE CHIP PACKAGE OF CLAIM 18, WHEREIN SAID FIRST SEMICONDUCTOR CHIP IS A GRAPHICS-PROCESSING-UNIT (GPU) CHIP.326
- T. CLAIM 23: “THE CHIP PACKAGE OF CLAIM 18, WHEREIN SAID SECOND SEMICONDUCTOR CHIP IS A LOGIC CHIP.326

U.	CLAIM 24: “THE CHIP PACKAGE OF CLAIM 18, WHEREIN SAID FIRST SEMICONDUCTOR CHIP IS A LOGIC CHIP.”	327
V.	CLAIM 25: “THE CHIP PACKAGE OF CLAIM 18, WHEREIN SAID THIRD SEMICONDUCTOR CHIP HAS A THICKNESS BETWEEN A BACKSIDE SURFACE OF SAID THIRD SEMICONDUCTOR CHIP AND A TOP SURFACE OF SAID THIRD SEMICONDUCTOR CHIP IS SMALLER THAN A THICKNESS OF ONE OF SAID PLURALITY OF METAL BUMPS.”	327
W.	CLAIM 26: “THE CHIP PACKAGE OF CLAIM 18, FURTHER COMPRISING ANOTHER SAID FIRST SEMICONDUCTOR CHIP OVER SAID FIRST INTERCONNECTION SCHEME.”	329
X.	CLAIM 27	330
1.	27(a): “ <i>The chip package of claim 18, further comprising a fourth semiconductor chip under said first interconnection scheme,</i> ”	330
2.	27(b): “ <i>wherein said fourth semiconductor chip has a thickness between a backside surface of said fourth semiconductor chip and a top surface of said fourth semiconductor chip is smaller than a thickness of one of said plurality of metal bumps.</i> ”	331
XI.	OPINIONS REGARDING GROUND 2B: CLAIMS 8 AND 16 ARE OBVIOUS OVER Yu, LIN-191, AND LIN-863.....	333
A.	CLAIM 8: “THE CHIP PACKAGE OF CLAIM 1, WHEREIN SAID SECOND REGION IS A RECTANGLE REGION AND SURROUNDING SAID FIRST REGION.”	333
B.	CLAIM 16: “THE CHIP PACKAGE OF CLAIM 10, WHEREIN SAID SECOND REGION IS A RECTANGLE REGION AND SURROUNDING SAID FIRST REGION.”	334
XII.	OPINIONS REGARDING GROUND 2C: CLAIM 21 IS OBVIOUS OVER YU, LIN-191, AND CAMACHO	334
A.	CLAIM 21	334
1.	21(a): “ <i>The chip package of claim 18, further comprising a fourth semiconductor chip over said first semiconductor chip,</i> ”	334

2.	<i>21(b): “wherein said fourth semiconductor chip comprises a third metal pad at a bottom surface of said fourth semiconductor chip,”</i>	335
	a) Camacho’s Teachings	335
3.	<i>21(c): “wherein said first semiconductor chip further comprising a plurality of through-silicon-via metal layers and a fourth metal pad at a top surface of said first semiconductor chip,”</i>	338
	a) Camacho’s Teachings	338
4.	<i>21(d): “wherein said first metal pad is at a bottom surface of said first semiconductor chip,”</i>	340
5.	<i>21(e): “wherein said first metal pad is coupled to said fourth metal pad through one of said plurality of through-silicon-via metal layers,”</i>	340
	a) Camacho’s Teachings	340
6.	<i>21(f): “wherein said third metal pad is coupled to said fourth metal pad through a solder layer.”</i>	341
	a) Camacho’s Teachings	341
7.	<i>Motivation to Combine</i>	342
XIII. CONCLUSION		345

CLAIM LISTING

Claim 1:

Claim 1(Pre): A chip package comprising:

Claim 1(a): a solid layer having a first surface and a second surface opposite to said first surface,

Claim 1(a)(i): wherein said solid layer comprises a compound of silicon and oxygen,

Claim 1(a)(ii): wherein said solid layer has a thickness between 50 and 150 micrometers,

Claim 1(a)(iii): wherein said solid layer comprises a first region and a second region between said first region and a first edge of said solid layer;

Claim 1(b): a plurality of metal posts in a plurality of through holes in said second region respectively,

Claim 1(b)(i): wherein one of said plurality of metal posts comprises a first copper layer contacting a sidewall of one of said plurality of through holes,

Claim 1(b)(ii): wherein said first region has a width in a direction greater than a shortest distance between said sidewall of one of said plurality of through holes and said first edge in said direction and greater than a pitch between two neighboring metal posts of said plurality of metal posts;

Claim 1(c): a first interconnection scheme over said first surface,

Claim 1(c)(i): wherein said first interconnection scheme comprises a first metal interconnect over said second surface and a polymer layer over said first metal interconnect,

Claim 1(c)(ii): wherein said first metal interconnect is connected to a first metal post of said plurality of metal posts,

Claim 1(c)(iii): wherein said first metal interconnect comprises a first metal layer and a second copper layer over said first metal layer;

Claim 1(d): a first metal bump over said first interconnection scheme,

Claim 1(d)(i): wherein said first metal bump comprises a second metal layer and a first tin-containing layer over said second metal layer; and

Claim 1(e): a first semiconductor chip under said second surface,

Claim 1(e)(i): wherein said first interconnection scheme comprise a second metal interconnect across over a sidewall of the first semiconductor chip,

Claim 1(e)(ii): wherein said first semiconductor chip comprises a third metal interconnect on a first metal pad of said first semiconductor chip,

Claim 1(e)(iii): wherein said third metal interconnect comprises a third metal layer on said first metal pad and a third copper layer over said third metal layer, wherein said third copper layer has a thickness between 5 and 30 micrometers,

Claim 1(e)(iv): wherein said first semiconductor chip is connected to a second metal post of said plurality of metal posts through said third metal interconnect.

Claim 2:

The chip package of claim 1, wherein said first semiconductor chip comprises a central-processing-unit (CPU) circuit block and a graphics-processing-unit (GPU) circuit block.

Claim 3:

Claim 3(a): The chip package of claim 1, wherein said first interconnection scheme further comprises a fourth metal interconnect over said first metal interconnect and said polymer layer,

Claim 3(b): wherein said polymer layer is between said first and fourth metal interconnects,

Claim 3(c): wherein said fourth metal interconnect comprises a fourth metal layer and a fourth copper layer over said fourth metal layer.

Claim 4:

The chip package of claim 1, wherein said first metal pad is an aluminum pad.

Claim 5:

The chip package of claim 1, wherein said compound comprises a SiO₂ compound.

Claim 6:

Claim 6(a): The chip package of claim 1, further comprising a second semiconductor chip over said first semiconductor chip, wherein said second semiconductor chip comprises a second metal bump on a second metal pad of said second semiconductor chip,

Claim 6(b): wherein said second metal bump comprises a second tin-containing layer.

Claim 7:

The chip package of claim 1, wherein said solid layer further comprises a third region opposite to said second region, wherein said third region is between said first region and a second edge of said solid layer, wherein said plurality of metal posts in said plurality of through holes in said third region respectively.

Claim 8:

The chip package of claim 1, wherein said second region is a rectangle region and surrounding said first region.

Claim 9:

The chip package of claim 1, further comprising another said first semiconductor chip under said second surface.

Claim 10:

Claim 10(Pre): A chip package comprising:

Claim 10(a): a solid layer having a first surface and a second surface opposite to said first surface,

Claim 10(a)(i): wherein said solid layer comprises a compound of silicon and oxygen,

Claim 10(a)(ii): wherein said solid layer has a thickness between 100 and 300 micrometers,

Claim 10(a)(iii): wherein said solid layer comprises a first region and a second region between said first region and a first edge of said solid layer;

Claim 10(b): a plurality of copper posts in a plurality of through holes in said second region respectively,

Claim 10(b)(i): wherein said first region has a width in a direction greater than a shortest distance between a sidewall of one of said plurality of through holes and said first edge in said direction and greater than a pitch between two neighboring copper posts of said plurality of copper posts;

Claim 10(c): a first interconnection scheme over said first surface,

Claim 10(c)(i): wherein said first interconnection scheme comprises a first metal interconnect over said first surface, and a polymer layer over said first metal interconnect,

Claim 10(c)(ii): wherein said first metal interconnect is connected to one of said plurality of copper posts,

Claim 10(c)(iii): wherein said first metal interconnect comprises a first metal layer and a first copper layer over said first metal layer;

Claim 10(d): a first metal bump over said first interconnection scheme,

Claim 10(d)(i): wherein said first metal bump comprises a first tin-containing layer;

Claim 10(e): a second metal bump over said first interconnection scheme;

Claim 10(f): a first semiconductor chip over said first interconnection scheme and between said first and second metal bumps,

Claim 10(f)(i): wherein said first semiconductor chip has a height between a backside surface of said first semiconductor chip and a top surface of said polymer layer is smaller than a thickness of said first metal bump,

Claim 10(f)(ii): wherein said first semiconductor chip comprises a third metal bump on a first metal pad of said first semiconductor chip, wherein said third metal bump comprises a second tin-containing layer; and

Claim 10(g): a second semiconductor chip over said first interconnection scheme,

Claim 10(g)(i): wherein said second semiconductor chip comprises a fourth metal bump on a second metal pad of said second semiconductor chip, wherein said fourth metal bump comprises a third tin-containing layer.

Claim 11:

The chip package of claim 10, wherein said compound comprises a SiO₂ compound.

Claim 12:

The chip package of claim 10, wherein no any copper post in said first region.

Claim 13:

Claim 13(a): The chip package of claim 10, further comprising a third semiconductor chip under said first interconnection scheme,

Claim 13(b): wherein said third semiconductor chip comprises a second metal interconnect on a third metal pad of said third semiconductor chip,

Claim 13(c): wherein said second metal interconnect comprises a second metal layer on said third metal pad and a second copper layer over said second metal layer, wherein said second copper layer has a thickness between 5 and 30 micrometers.

Claim 14:

Claim 14(a): The chip package of claim 10, further comprising a third semiconductor chip under said first interconnection scheme,

Claim 14(b): wherein said third semiconductor chip comprises a second metal interconnect on a third metal pad of said third semiconductor chip,

Claim 14(c): wherein said second metal interconnect comprises a second metal layer on said third metal pad and a second copper layer over said second metal layer,

Claim 14(d): wherein said third semiconductor chip comprises a central-processing-unit (CPU) circuit block and a graphics-processing-unit (GPU) circuit block.

Claim 15:

The chip package of claim 10, wherein said solid layer further comprises a third region opposite to said second region, wherein said third region is between said first region and a second edge of said solid layer, wherein said plurality of copper posts in said plurality of through holes in said third region respectively.

Claim 16:

The chip package of claim 10, wherein said second region is a rectangle region and surrounding said first region.

Claim 17:

Claim 17(a): The chip package of claim 10, further comprising an electrical device under said second surface, wherein said electrical device comprise a third semiconductor chip and a metal wire connected to a third metal pad of said third semiconductor chip,

Claim 17(b): wherein said third semiconductor chip is a DRAM chip.

Claim 18:

Claim 18(Pre): A chip package comprising:

Claim 18(a): a solid layer having a first surface and a second surface opposite to said first surface,

Claim 18(a)(i): wherein said solid layer comprises a compound of silicon and oxygen,

Claim 18(a)(ii): wherein said solid layer has a thickness between 50 and 150 micrometers,

Claim 18(a)(iii): wherein said solid layer comprises a first region and a second region between said first region and a first edge of said solid layer;

Claim 18(b): a plurality of copper posts in a plurality of through holes in said second region respectively;

Claim 18(c): a first interconnection scheme over said first surface,

Claim 18(c)(i): wherein said first interconnection scheme comprises first and second metal interconnects over said first surface, and a first polymer layer over said first and second metal interconnects,

Claim 18(c)(ii): wherein said first metal interconnect is connected to a first copper post of said plurality of copper posts,

Claim 18(c)(iii): wherein said first metal interconnect comprises a first metal layer and a first copper layer over said first metal layer;

Claim 18(d): a first semiconductor chip over said first interconnection scheme,

Claim 18(d)(i): wherein said first semiconductor chip comprises a third metal interconnect under a first metal pad of said first semiconductor chip,

Claim 18(d)(ii): wherein said third metal interconnect comprises a second metal layer under said first metal pad and a second copper layer under said second metal layer, wherein said second copper layer has a thickness between 5 and 30 micrometers,

Claim 18(d)(iii): wherein said first semiconductor chip is coupled to a second copper post of said plurality of copper posts through said third metal interconnect;

Claim 18(e): a second semiconductor chip over said first interconnection scheme,

Claim 18(e)(i): wherein said second semiconductor chip comprises a second metal pad coupled to said second metal interconnect;

Claim 18(f): a third semiconductor chip under said first interconnection scheme; and

Claim 18(g): a plurality of metal bumps under said second surface, wherein one of said plurality of metal bumps comprises a tin-containing layer.

Claim 19:

The chip package of claim 18, wherein said compound comprises a SiO₂ compound.

Claim 20:

The chip package of claim 18, wherein said solid layer further comprises a third region opposite to said second region, wherein said third region is between said first region and a second edge of said solid layer, wherein said plurality of copper posts in said plurality of through holes in said third region respectively.

Claim 21:

Claim 21(a): The chip package of claim 18, further comprising a fourth semiconductor chip over said first semiconductor chip,

Claim 21(b): wherein said fourth semiconductor chip comprises a third metal pad at a bottom surface of said fourth semiconductor chip,

Claim 21(c): wherein said first semiconductor chip further comprising a plurality of through-silicon-via metal layers and a fourth metal pad at a top surface of said first semiconductor chip,

Claim 21(d): wherein said first metal pad is at a bottom surface of said first semiconductor chip,

Claim 21(e): wherein said first metal pad is coupled to said fourth metal pad through one of said plurality of through-silicon-via metal layers,

Claim 21(f): wherein said third metal pad is coupled to said fourth metal pad through a solder layer.

Claim 22:

The chip package of claim 18, wherein said first semiconductor chip is a graphics-processing-unit (GPU) chip.

Claim 23:

The chip package of claim 18, wherein said second semiconductor chip is a logic chip.

Claim 24:

The chip package of claim 18, wherein said first semiconductor chip is a logic chip.

Claim 25:

The chip package of claim 18, wherein said third semiconductor chip has a thickness between a backside surface of said third semiconductor chip and a top surface of said third semiconductor chip is smaller than a thickness of one of said plurality of metal bumps.

Claim 26:

The chip package of claim 18, further comprising another said first semiconductor chip over said first interconnection scheme.

Claim 27:

Claim 27(a): The chip package of claim 18, further comprising a fourth semiconductor chip under said first interconnection scheme,

Claim 27(b): wherein said fourth semiconductor chip has a thickness between a backside surface of said fourth semiconductor chip and a top surface of said

fourth semiconductor chip is smaller than a thickness of one of said plurality of metal bumps.

I, Dr. Stanley Shanfield, declare as follows:

I. INTRODUCTION

1. I have been retained by counsel for Petitioners as a technical expert in the above-captioned case. Specifically, I have been asked to render certain opinions regarding the IPR petition with respect to U.S. Patent No. 11,894,306 (the “’306 Patent”). I understand that the Challenged Claims are 1-27, and my opinions are limited to those claims. A true and correct copy of my Curriculum Vitae, which provides further details about my background and experience, is appended to this Declaration.

A. Educational Background and Professional Experience

2. In 1977, I received a B.S. Degree in Physics *cum laude* from the University of California, Irvine. I received a Ph.D. in Physics from Massachusetts Institute of Technology in 1981.

3. After obtaining my Ph.D. in 1981, I was a Staff Scientist at Spire Corporation in Bedford, Massachusetts. From 1985-1999, I worked at Raytheon Corporation. As staff and later as section manager, among many other projects, I developed reactive ion etching (RIE) processes for patterning dielectrics (silicon dioxide, silicon nitride, silicon oxynitride, etc.), conductive layers (aluminum-copper, copper-silicon, W-silicide, TaN, doped polysilicon, etc.) and organic layers

(photoresist, polyimide, etc.). In 1996, I became the Manager of Semiconductor Operations at Raytheon. As Manager, I built and led a 300-employee, \$60 million revenue-generating semiconductor development, commercial system design, and electronic module manufacturing operation. I worked directly with engineers in the selection, installation, and optimization of several chemo-mechanical polishing systems (CMP), including analysis of operational maintenance and performance monitoring. The manufacturing facility eventually used multiple production CMP systems, and I directly participated in establishing the required metrology (optical thickness monitoring) for maintaining polishing uniformity standards.

4. In 1999, I was a co-founder and became Vice President of Operations at AXSUN Technologies in Bedford/Billerica, Massachusetts and later became Director of Manufacturing and Wafer Fab Technology.

5. In 2003, I joined the Draper Laboratory in Cambridge, Massachusetts. Currently, I am the Division Leader of Advanced Hardware Development, with around 80 staff members; a Distinguished Member of Technical Staff; and Technical Director. I led the Advanced Hardware Development division in relaunching a multi-chip integrated circuit module facility. The laboratory has acquired several semiconductor-grade CMP systems for the purpose of fabricating multi-chip modules and for planarization operations in MEMS devices, and I have been

involved in their operation and optimization. I invented and led the implementation of an ultra-miniature electronics fabrication technology. I also developed fabrication technology for semiconductor-based low-phase noise oscillator design. I have received many awards at Draper, including the 2010 Distinguished Performance Award and the 2010 Best Patent Award.

6. During the 1990's I developed early stacked-chip plastic packages while working for Raytheon. Additionally, I have led the implementation and qualification of MCM-D (multi-chip module – deposited) technology for military and space applications during my time at Draper Labs. Also during my time at Draper Labs, I have (1) developed improved fabrication and test methods for advanced multichip modules using ceramic and glass packages, (2) led efforts involving die thinning, copper interconnect plating, and component stacking at multiple interconnect levels, (3) managed thermos-mechanical modeling efforts to assess packaging reliability under demanding conditions, and (4) oversaw a large team of next-gen multichip module process development at Draper (2010-2015). Additionally, I am an inventor on U.S. Patent No. 7,727,806 which is directed to systems and methods for high density multi-component modules.

B. Materials Considered

7. I have relied upon my education, knowledge, and experience with semiconductor chip packaging, as well as the other materials as discussed in this declaration in forming my opinions.

8. In developing my opinions, I have considered the following materials:

Exhibit 1001	U.S. Patent No. 11,894,306
Exhibit 1002	File History of the '306 Patent
Exhibit 1004	U.S. Patent No. 9,167,694 to Sundaram, et al.
Exhibit 1005	U.S. Patent Publication No. 2010/0290191 to Lin, et al.
Exhibit 1006	U.S. Patent Publication No. 2011/0215458 to Camacho, et al.
Exhibit 1007	U.S. Patent No. 9,679,863 to Lin, et al.
Exhibit 1008-1009	Intentionally left blank
Exhibit 1010	U.S. Patent No. 9,123,763 to Yu, et al.
Exhibit 1011	Intentionally left blank
Exhibit 1012	Andrea Chen, et al. <i>Semiconductor Packaging Materials Interaction and Reliability</i> , CRC Press, 2012
Exhibit 1013	Philip Garrou, et al., <i>RDL: an integral part of today's advanced packaging technologies</i> , Solid State Technology, May 2011

Exhibit 1014	U.S. Patent No. 8,780,576 to Haba, et al.
Exhibit 1015	U.S. Patent No. 7,902,648 to Lee
Exhibit 1016	U.S. Patent No. 7,964,961 to Lee, et al.
Exhibit 1017	U.S. Patent No. 7,241,641 to Savastiouk, et al.
Exhibit 1018	U.S. Patent Publication No. 2005/0110168 to Chuang
Exhibit 1019	U.S. Patent Publication No. 2011/0026232 to Lin, et al.
Exhibit 1020	U.S. Patent No. 5,086,558 to Grube, et al.
Exhibit 1021	U.S. Patent Publication No. 2011/0193219 to Lai, et al.
Exhibit 1022	U.S. Patent No. 6,818,545 to Lee, et al.
Exhibit 1023	U.S. Patent No. 6,974,659 to Su, et al.
Exhibit 1024	U.S. Patent Publication No. 2006/0175686 to Murata, et al.
Exhibit 1025	U.S. Patent Publication No. 2012/0098124 to Wu, et al.
Exhibit 1026	U.S. Patent No. 8,193,604 to Lin et al.
Exhibit 1027	U.S. Patent Publication No. 2004/0203224 to Halahan, et al.
Exhibit 1028	Philip Garrou, <i>Introduction to 3D Integration</i> , Handbook of 3D integration: Volumes 1 and 2, Technology and Application of 3D Integrated Circuits, 2012
Exhibit 1029	U.S. Patent Publication No. 2003/0068877 to Kinsman.

Exhibit 1030	U.S. Patent Publication No. 2010/0246152 to Lin, et al.
Exhibit 1031	Yi Yang, et al, <i>CPU-Assisted GPGPU on Fused CPU-GPU Architectures</i> , IEEE Xplore
Exhibit 1032	File History of U.S. Patent No. 11,107,768
Exhibit 1033	U.S. Patent No. 4,863,773 to Rousseau, et al.
Exhibit 1034	U.S. Patent No. 6,365,265 to Tose, et al.
Exhibit 1035	E.D. Blackshear, et al., <i>The evolution of build-up package technology and its design challenges</i> , International Business Machines Corporation, 2005
Exhibit 1036	Intentionally left blank
Exhibit 1037	U.S. Patent No. 7,374,969 to Cho, et al.
Exhibit 1038	U.S. Patent No. 7,199,036 to Chan, et al.
Exhibit 1039	U.S. Patent No. 8,158,508 to Lin, et al.
Exhibit 1040	U.S. Patent No. 6,619,538 to Test, et al.
Exhibit 1041	U.S. Patent Publication No. 2011/0101523 to Hwang, et al.
Exhibit 1042	U.S. Patent No. 6,831,003 to Huang, et al.
Exhibit 1043	U.S. Patent Publication No. 2009/0226611 to Suzuki, et al.
Exhibit 1044	U.S. Patent No. 6,077,726 to Mistry, et al.

Exhibit 1045	U.S. Patent Publication No. 2010/0244245 to Pendse, et al.,
Exhibit 1046	U.S. Patent Publication No. 2012/0206160 to Wu, et al.
Exhibit 1047	U.S. Patent Publication No. 2009/0174052 to Sogawa, et al.
Exhibit 1048-1053	Intentionally left blank
Exhibit 1054	U.S. Patent No. 6,489,240 to Iacoponi, et al.
Exhibit 1055	U.S. Patent No. 6,578,178 to Mau
Exhibit 1056	U.S. Patent Publication No. 2012/0001190 to Okabe, et al.
Exhibit 1057	U.S. Patent No. 7,307,348 to Wood, et al.
Exhibit 1058	U.S. Patent No. 8,138,014 to Chi, et al.
Exhibit 1059	U.S. Patent No. 6,506,672 to Dagenais, et al.
Exhibit 1060	U.S. Patent No. 8,518,798 to Graetz.
Exhibit 1061	U.S. Patent Publication No. 2009/0261473 to Lee, et al.
Exhibit 1062	Intentionally left blank
Exhibit 1063	U.S. Patent No. 6,812,143 to Lane, et al.
Exhibit 1064	Intentionally left blank
Exhibit 1065	Intentionally left blank
Exhibit 1066	U.S. Patent Publication No. 2009/0070727 to Solomon.

Exhibit 1067	U.S. Patent Publication No. 2012/0098114 to Ishibashi.
Exhibit 1068	U.S. Patent Publication No. 2011/0074028 to Pendse.
Exhibit 1069	U.S. Patent No. 7,485,955 to Kang, et al.
Exhibit 1070	U.S. Patent Publication No. 2012/0104623 to Pagaila, et al.
Exhibit 1071	Intentionally left blank
Exhibit 1072	U.S. Patent No. 7,772,880 to Solomon.
Exhibit 1073	U.S. Patent No. 7,989,270 to Huang, et al.
Exhibit 1074	U.S. Patent Publication No. 2011/0304999 to Yu, et al.
Exhibit 1075-1079	Intentionally left blank
Exhibit 1080	U.S. Patent Publication No. 2012/0319251 to Yu, et al.
Exhibit 1081-1082	Intentionally left blank
Exhibit 1083	U.S. Patent Publication No. 2009/0166069 to Kinoshita.
Exhibit 1084-1092	Intentionally left blank
Exhibit 1093	U.S. Patent No. 6,107,180 to Munroe, et al.
Exhibit 1094	U.S. Patent Publication No. 2011/0210283 to Ramirez, et al.

Exhibit 1095	U.S. Patent No. 6,542,502 to Dishongh, et al.
Exhibit 1096	Intentionally left blank
Exhibit 1097	Richard K. Ulrich, et al., <i>Advanced Electronic Packaging</i> , IEEE Press Series on Microelectrical Systems, 2006
Exhibit 1098	Mulugeta Abtew, et al., <i>Lead-free Solders in Microelectronics</i> , Materials Science and Engineering, 2000
Exhibit 1099	Karl J. Puttlitz, et al., <i>Handbook of Lead-Free Solder Technology for Microelectronic Assemblies</i> , 2005
Exhibit 1100	Intentionally left blank
Exhibit 1101	U.S. Patent Publication No. 2013/0151869 to Steinman, et al.
Exhibit 1102	Linely Gwennap, <i>Sandy Bridge Spans Generations: Intel Focuses on Graphics, Multimedia in New Processor Design</i> , Microprocessor, 2010
Exhibit 1103	U.S. Patent No. 6,330,164 to Khandros, et al.
Exhibit 1104	U.S. Patent No. 6,710,447 to Nogami.
Exhibit 1105-1116	Intentionally left blank
Exhibit 1117	U.S. Patent No. 11,538,763 File History

Exhibit 1118-1119	Intentionally left blank
Exhibit 1120	U.S. Patent No. 6,282,100 to Degani, et al.
Exhibit 1121	U.S. Patent No. 6,818,980 to Pedron.
Exhibit 1122	U.S. Patent No. 6,842,391 to Fujioka, et al.
Exhibit 1123	U.S. Patent No. 7,193,917 to Takahashi, et al.
Exhibit 1124	U.S. Patent No. 4,603,345 to Lee, et al.
Exhibit 1125	U.S. Patent Publication No. 2012/0146177 to Choi, et al.
Exhibit 1126	U.S. Patent No. 8,592,988 to Lee, et al.
Exhibit 1127	U.S. Patent No. 8,238,113 to Iihola, et al.
Exhibit 1128	U.S. Patent No. 6,528,179 to Jimarez, et al.
Exhibit 1129	U.S. Patent No. 6,468,413 to Fanti, et al.
Exhibit 1130	U.S. Patent No. 8,132,775 to Goldmann.
Exhibit 1131	U.S. Patent Publication No. 2011/0186977 to Chi, et al.
Exhibit 1132	U.S. Patent No. 7,169,627 to Duh, et al.
Exhibit 1133	U.S. Patent No. 6,614,243 to Klehn, et al.
Exhibit 1134	U.S. Patent Publication No. 2009/0162622 to Van Veen, et al.
Exhibit 1135	U.S. Patent No. 6,570,259 to Alcoe, et al.

Exhibit 1136	U.S. Patent No. 7,741,567 to Beddingfield, et al.
Exhibit 1137	U.S. Patent No. 6,407,341 to Anstrom, et al.

9. I have considered these materials from the viewpoint of a POSITA as of the priority date of the '306 Patent. For the purposes of this declaration, I have been asked to assume that the priority date of the '306 Patent is September 26, 2012. I note that my opinions provided in this Declaration are made from the perspective of a POSITA as of this priority date of the '306 Patent unless expressly stated otherwise. To the extent that I use any verb tense in this Declaration that is present tense (e.g., “a POSITA would understand” instead of “a POSITA would have understood”), such verb tense should be understood to be my opinion as of the '306 Patent's priority date (again, unless expressly stated otherwise). I merely use the present verb tense for ease of reading.

II. OVERVIEW AND LEGAL STANDARDS

10. In formulating my opinions, I have been instructed to apply certain legal standards. I am not a lawyer. I do not offer any testimony regarding what the law is. Instead, the following sections summarize the law as I have been instructed to apply it in formulating and rendering my opinions found later in this declaration. I understand that, in an *inter partes* review (“IPR”) proceeding, patent claims may

be deemed unpatentable if it is shown that they are anticipated or rendered obvious in view of the prior art. I understand that prior art in an IPR review is limited to patents or printed publications that predate the priority date of the patent at issue. I understand that questions of claim clarity (definiteness) and enablement cannot be considered as a ground for considering the patentability of a claim in these proceedings.

A. *Person of Ordinary Skill in the Art*

11. I understand that the '306 Patent, the record of the proceedings at the Patent Office (which I understand is called the "File History" or "Prosecution History"), and the teachings of the prior art are evaluated from the perspective of a person of ordinary skill in the art ("POSITA"). I understand that the factors considered in determining the ordinary level of skill in the art may include: (i) the levels of education of the inventor; (ii) the types of problems encountered in the art; (iii) prior art solutions to those problems; (iv) the rapidity with which innovations are made; (v) the sophistication of the technology; and (vi) the educational level of persons working in the field.

12. I understand that a person of ordinary skill in the art is not a specific real individual, but rather a hypothetical individual having the qualities reflected by the factors above. The hypothetical person is presumed to have the same level of

skill as the typical practitioner of the art and is presumed to have knowledge of all prior art in the relevant field. I understand that the inventor's actual knowledge or lack of knowledge of prior art reference is irrelevant to the obviousness determination.

B. *Obviousness*

13. I understand that a claim may be invalid under 35 U.S.C. § 103(a) if the subject matter described by the claim as a whole would have been “obvious” to a POSITA in view of a single or combination of prior art references at the time the claimed invention was made. I further understand that a POSITA is assumed to know and to have all relevant prior art in the field of endeavor covered by the patent-in-suit and all analogous prior art. I understand that obviousness in an IPR review proceeding is evaluated using a preponderance of the evidence standard, which means that the claims must be more likely obvious than nonobvious.

14. I also understand that an obviousness determination includes the consideration of various factors including: (1) the scope and content of the prior art, (2) the differences between the prior art and the claim at issue, and (3) the level of ordinary skill in the pertinent art. I understand that secondary considerations of non-obviousness such as commercial success, long-felt but unresolved needs, failure of others, and so forth may be assessed as well. I have been informed that an

obviousness analysis must consider the full scope of the claims to avoid impermissibly using hindsight to invalidate a patent.

15. In considering whether certain prior art renders a particular patent claim obvious, I have been informed that I can consider the scope and content of the prior art, including the fact that a POSITA would regularly look to the disclosures in patents, trade publications, journal articles, conference papers, industry standards, product literature and documentation, texts describing competitive technologies, requests for comment published by standard setting organizations, and materials from industry conferences, as examples.

16. I have been informed that for a prior art reference to be proper for use in an obviousness analysis, the reference must be “analogous art” to the claimed invention. A reference is analogous art if: (1) the reference is from the same field of endeavor as the claimed invention (even if it addresses a different problem); or (2) the reference is reasonably pertinent to the problem faced by the inventor (even if it is not in the same field of endeavor as the claimed invention). For a reference to be “reasonably pertinent” to the problem, it must logically have commended itself to an inventor’s attention in considering the problem. In determining whether a reference is reasonably pertinent, one should consider the problem faced by the inventor, as reflected either explicitly or implicitly, in the specification. I believe that

the documents I considered in forming my opinions in this IPR are well within the range of documents a POSITA would have consulted to address the type of problems described in the Challenged Claims.

17. I have been informed that to establish that a claimed invention was obvious based on a combination of prior art elements, an articulation of the reason(s) why a claimed invention would have been obvious must be provided. Specifically, I have been informed that the prior art, either as a single reference or a combination of multiple items of prior art, renders a patent claim obvious when there was an apparent reason for a POSITA, at the time of the invention, to combine or modify the prior art. Rationales for combining or modifying the prior art include, but are not limited to, any of the following: (A) combining prior art methods according to known methods to yield predictable results; (B) substituting one known element for another to obtain predictable results; (C) using a known technique to improve a similar device in the same way; (D) applying a known technique to a known device ready for improvement to yield predictable results; (E) trying a finite number of identified, predictable potential solutions, with a reasonable expectation of success; (F) identifying that known work in one field of endeavor may prompt variations of it for use in either the same field or a different one based on design incentives or other market forces if the variations are predictable to one of ordinary skill in the art;

or (G) identifying an explicit teaching, suggestion, or motivation in the prior art that would have led one of ordinary skill to modify the prior art reference or to combine the prior art references to arrive at the claimed invention.

18. I have also been informed that where there is a motivation to combine, claims may be rejected as obvious provided a POSITA would have had a reasonable expectation of success regarding the proposed combination. I have also been informed that common sense may be considered. Common sense teaches that familiar items may have obvious uses beyond their primary purposes. I have been informed that if the combination was obvious to try (regardless of whether it was actually tried) or leads to anticipated success, then it is likely the result of ordinary skill and common sense rather than non-obvious innovation.

19. I have been informed that the existence of an explicit teaching, suggestion, or motivation to combine known elements of the prior art is a sufficient, but not a necessary, condition to a finding of obviousness. In determining whether the subject matter of a patent claim is obvious, neither the particular motivation nor the avowed purpose described in the patent-in-suit controls. I have been further informed that the obviousness analysis may consider the effects of demands known to the technological community or present in the marketplace and the background knowledge possessed by a POSITA. These issues may be considered to determine

whether there was an apparent reason to combine the known elements in the fashion claimed by the patent.

20. I have been informed that it is improper to combine references where the references teach away from their combination. A reference may be said to teach away when a POSITA, upon reading the reference, would be discouraged from following the path set out in the reference, or would be led in a direction divergent from the path that was taken by the patent applicant. I have also been informed that a reference does not teach away if it merely expresses a general preference for an alternative invention but does not criticize, discredit, or otherwise discourage investigation into the invention claimed.

21. I am informed that even if a case of obviousness is established, the final determination of obviousness must also consider “secondary considerations” if presented. Secondary considerations include: (a) commercial success of a product due to the merits of the claimed invention; (b) a long-felt, but unsatisfied need for the invention; (c) failure of others to find the solution provided by the claimed invention; (d) deliberate copying of the invention by others; (e) unexpected results achieved by the invention; (f) praise of the invention by others skilled in the art; (g) lack of independent simultaneous invention within a comparatively short space of time; and (h) teaching away from the invention in the prior art.

22. I have been further informed that secondary considerations evidence is only relevant if the offering party establishes a connection, or nexus, between the evidence and the claimed invention. The nexus cannot be based on prior art features. The establishment of a nexus is a question of fact. While I understand that Patent Owner here has not offered any secondary considerations at this time, I will supplement my opinions should Patent Owner raise secondary considerations during the course of this proceeding.

C. *Claim Construction*

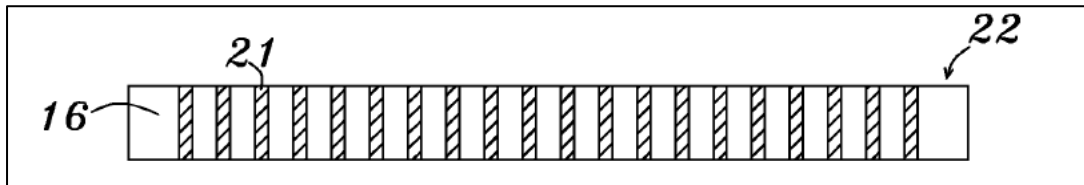
23. I understand that the claim terms in an IPR proceeding are construed according to their plain and ordinary meaning as understood in light of the claim language, the patent's description, and the prosecution history viewed from the perspective of a POSITA. I further understand that where a patent defines claim language, the definition of the patent controls, even if there are other definitions that might be understood by those working in the art.

III. OVERVIEW OF THE '306 PATENT

A. *Summary of the '306 Patent*

24. The '306 Patent describes a chip package having a "second substrate 22" with an "amorphous solid glass layer/body 16 and multiple metal plugs 21" wherein the "amorphous solid glass layer/body 16 having a top surface and an opposing bottom surface and the metal plugs 21 extending through the amorphous

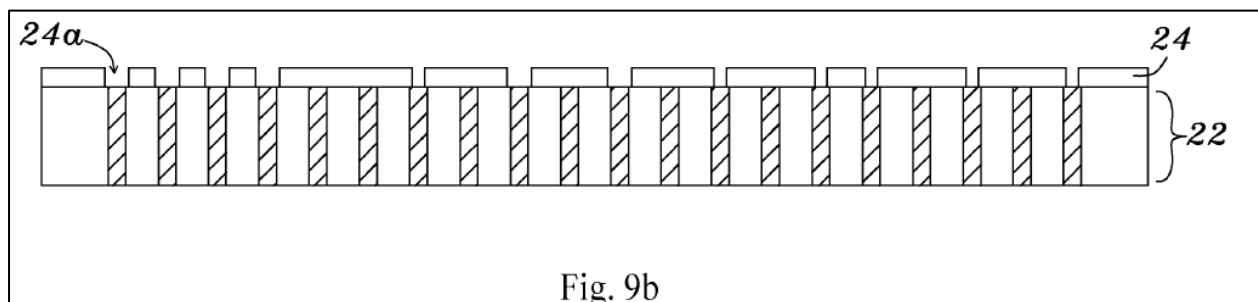
solid glass layer/body 16 beginning at the top surface and ending at the bottom surface.” *EX1001* at 11:7-14.



EX1001 at FIG. 8a.

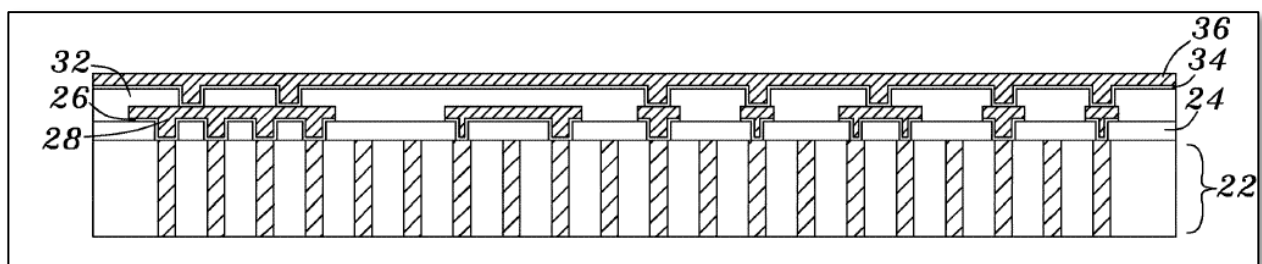
25. The '306 Patent further describes the metal plugs are “formed from metal traces 6.” *EX1001* at 8:3-5. To obtain the plugs, the metal traces 6 are (1) stretched (6:4-11, FIG. 6a); (2) placed in a mold (6:37-43, FIG. 6d); (3) a polymer is filled into the mold (6:56-60, 7:49-52); and (4) cut into “multiple first substrates 20,” which comprises “multiple seconds substrates 22” that each have “multiple metal plugs 21.” *EX1001* at 7:58–8:3, FIGS. 6j-6k.

26. As shown below in FIG. 9b, a “first dielectric layer 24” that may be a “polymer (such as polyimide...)” is formed “formed on the top surface of the first substrate 20.” *EX1001* at 11:44-51. “Multiple openings 24a are formed in the first dielectric layer 24 to expose the metal plugs 21” by “etching.” *EX1001* at 11:58-61.



EX1001 at FIG. 9b.

27. A “first metal layer 26 is formed on the first dielectric layer 24, on the metal plugs 21 and in the openings 24” that “may include an adhesion/barrier layer, such as a layer of titanium...” *EX1001* at 11:65–12:1. Next, a “second metal layer 28 is formed on the first metal layer 26” that “maybe comprises copper.” *EX1001* at 12:10-13. A “second dielectric layer 32 is formed on the first dielectric layer 24 and on the second metal layer 28” that may be “a polymer[.]” *EX1001* at 12:36-43. Multiple “openings 32a are formed in the second dielectric layer 32 to expose the second metal layer 28” then a “third metal layer 34 is formed on the second dielectric layer 32, on the second metal layer 28 and in the openings 32a.” *EX1001* at 12:51-60. A “fourth metal layer 36 is formed on the third metal layer 34.” *EX1001* at 13:3-4.

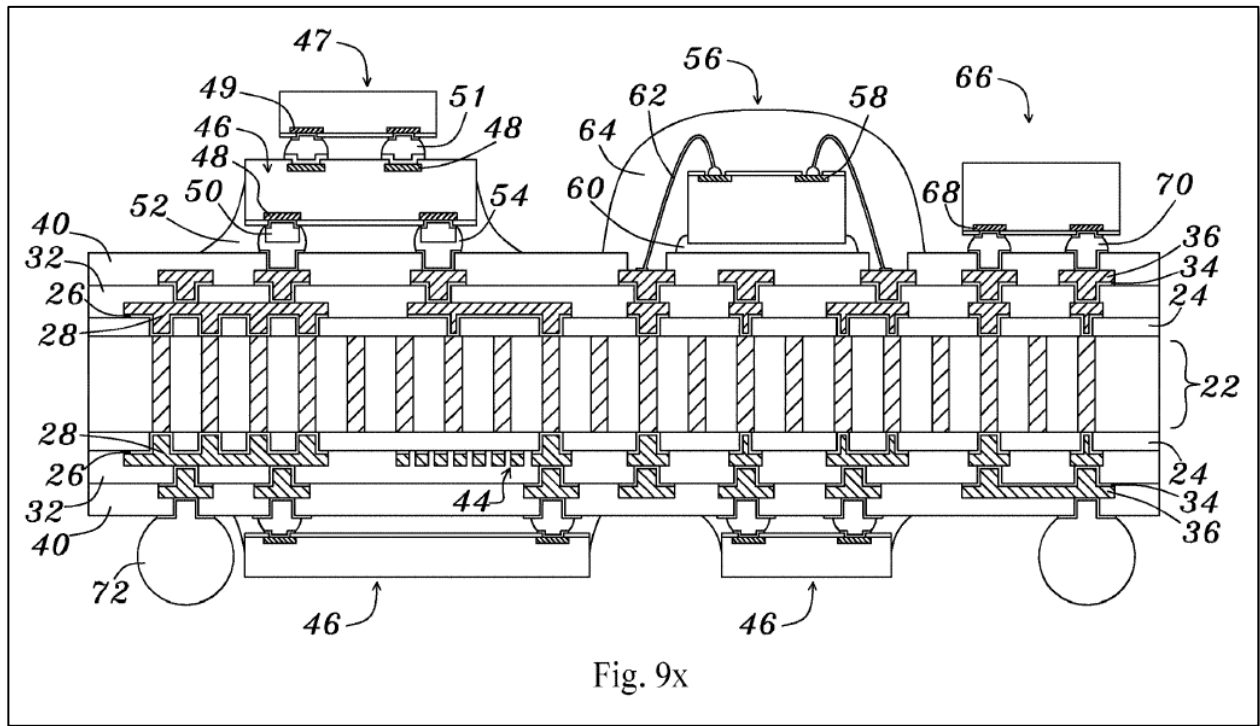


EX1001 at FIG. 9k.

28. A “third dielectric layer 40 is formed on the second dielectric layer 32 and on the fourth metal layer 36” that may be a “polymer[.]” *EX1001* at 13:28-35.

Multiple “openings 40a are formed in the third dielectric layer 40 to expose the fourth metal layer 36” then a “protecting layer 42 is formed in the openings 40a, on the third dielectric layer 40 and on the fourth metal layer 36[.]” *EX1001* at 13:43-52. Multiple “chips 46 and chips 56” are “set up over the third dielectric layer 40 through a flip-chip package process” where the “chip 46 comprises multiple metal pads 48 and multiple metal bumps 50 formed on the metal pads 48.” *EX1001* at 13:64-66, 14:17-19.

29. The ‘306 Patent further describes a “metal bump 72” that may have “an adhesion/barrier metal layer 61...a metal seed layer 63 formed on the adhesion/barrier metal layer 61, an electroplated metal layer 65 formed on the metal seed layer 63 and a solder layer 67 formed on the electroplated metal layer 65.” *EX1001* at 14:60-66. The “electroplated metal layer 65 comprises a copper layer” and the “solder layer 67 can be formed” of “gold-tin alloy, tin-silver alloy, tin-silver copper alloy, indium, tin-bismuth allow or other lead-free alloy.” *EX1001* at 15:3-8.



EX1001 at FIG. 9x.

30. As I will explain in detail below, there is nothing novel about the disclosure or claims of the '306 Patent. The claims as a whole recite a litany of claim elements that were both well-known on their own and well-known in combination with other recited claim elements. For example, the claims recite well-known features such as metal interconnects, copper plugs, semiconductor chips, and metal bumps, all of which were commonplace in chip packages before well before the '306 Patent. Furthermore, the claimed region[s] and relative distances of the region[s] describe a fan-out chip package, which was a common chip package type before the '306 Patent.

B. *Field of Endeavor*

31. I have been informed that the field of endeavor of the claimed invention can be determined by reference to explanations of the invention's subject matter in the patent application, including the embodiments, function, and structure of the claimed invention.

32. The '306 Patent, titled "Chip Package" generally relates to semiconductor packaging. *EX1001* at Title. The '306 Patent describes that "microelectronic devices have a tendency to be minimized and thinned with its functional development and a semiconductor package mounted on a mother board is also following the tendency in order to realize a mounting of high integration" *EX1001* at 1:29-33. The described embodiments "illustrates a cross-section view of multiple chips and a 3D-IC package..." *EX1001* at 3:37-40. Additionally, the '306 Patent describes that "chips 46 are set up...through a flip-chip package process." *EX1001* at 14:16-17.

33. Further still, the '306 Patent expressly places its work in the context of flip-chip technology, explaining that "flip-chip technology fabricates bumps... on Al pads of chip and interconnects the bumps directly to the package media" and that this arrangement provides "the highest density of interconnection to the device and a very low inductance interconnection to the package" *EX1001* at 1:54-67. For these

reasons, a POSITA would understand that the field of endeavor of the '306 Patent includes semiconductor packaging. *EX1001* at 1:28-2:3.

C. *Problem Solved by the Inventors of the '306 Patent*

34. I have been informed that a prior art reference is “reasonably pertinent” if a POSITA would have consulted it and applied its teachings when faced with the problem(s) that the inventor was trying to solve. As such, I have been asked to analyze the '306 Patent and determine the problem(s) that the inventors were trying to solve.

35. The '306 Patent recognizes the problem of "TCE (Temperature Coefficient of Expansion) matching to avoid solder bump fatigue [is] still [a] challenge[]" *EX1001* at 1:67–2:3. Thus, a POSITA would have understood the '306 Patent is directed, in part, to solving the problem of minimizing temperature coefficient of expansion mismatching in semiconductor packages.

36. The '306 Patent also explains that "pre-testability, post-bonding visual inspection... [is] still [a] challenge[]" *EX1001* at 1:67–2:3. Thus, a POSITA would have understood the '306 Patent to be directed, in part, to solving the problem of creating chip packages with pre-testability capability.

37. Further, the '306 Patent states that “with the further miniaturization of the IC” there is “an increasingly negative impact on the circuit performance.”

EX1001 at 1:39-40. Thus, a POSITA would have understood the '306 Patent to be directed, in part, to solving the problem the impact of miniaturization on circuit performance.

38. Additionally, the '306 Patent describes that “parasitic capacitance and resistance of the metal interconnections increase, which degrades the chip performance significantly.” *EX1001* at 1:40-43. Thus, a POSITA would have understood the '306 Patent to be directed, in part, to solving the problem the impact of parasitic capacitance of interconnections in a chip package.

IV. LEVEL OF ORDINARY SKILL

39. Based on my review and analysis of the '306 Patent, the cited prior art, and the ordinary skill factors described in this section, a POSITA in the field of the '306 Patent at the time of the earliest possible priority date (September 26, 2012) would have had a at least a bachelor's degree in electrical engineering, materials science, or physics (or an equivalent degree), and at least two years of experience in semiconductor design or semiconductor manufacturing. A master's degree or Ph.D. in a relevant field may substitute for some work experience or vice versa. Additional education or experience might substitute for the above requirements. When I refer to the understanding of a POSITA, I am referring to the understanding of such a person as of September 26, 2012.

V. OVERVIEW OF THE TECHNOLOGY

40. I was asked to briefly summarize the background of the prior art from the standpoint of a person having ordinary skill in the art prior to September 26, 2012. As explained below, the chip packaging technology described by the '306 Patent was based on well-known packaging techniques and chip package structures. Thus, the techniques discussed in the '306 Patent were well-known and conventional prior to the invention of the '306 Patent.

A. *History of Chip Packaging*

41. Chip packaging technology was known and widely used well before the priority date of the '306 Patent. In fact, semiconductor chip packaging had been in development at least 40 years in advance of the 2012 priority date of the '306 Patent with the 1960s seeing “rapid proliferation of new packages for ICs” as a response to the development of silicon planar technology and higher pin count versions of early metal can packages. *EX1097* at p. 8. Additionally, “[p]ackaging costs also received considerable attention during the 1960s while the industry was deciding which package or packages would become standard[.]” along with “early attempts to develop a low-cost, hermetic package[.]” *EX1097* at p. 11, *see also EX1012* at p. 4. Subsequently, plastic packaging, more specifically, the plastic version of the dual

in-line packaging (DIP) family was “introduced in the early 1970s[.]” *EX1012* at p. 4.

42. Eventually, “the early 1990s saw the emergence of both pin grid array (PGA) and ball grid array (BGA) packages” responsive to the ultimate goal for high-performance electronic systems to “pack devices as close together as possible in order to minimize circuit path length.” *EX1097* at p. 12. “MCM technology, still a viable technology today, played a major role in the evolution of multichip packaging in the 1990s, which includes three-dimensional (3D) stacking of ICs within a single package[.]” *EX1097* at p. 15.

43. Traditional wire bonding techniques were eventually replaced with flip-chip package technology, “[n]amely, the chip is not wire bonded for interconnect but instead flipped face-to-face with the substrate surface—hence the name *flip chip*—and the interconnection between the die and substrate is made through an array of bumps that are placed on the bonding pads of the die surface.” *EX1012* at p. 18.

44. “The concept of flip-chip (FC) can be traced back to what IBM called ‘controlled collapse chip connection’ (C-4) in the late 1960s. It has always been clear that FC is a superior interconnect based on size, I/O density, electrical and thermal performance. However, during the 1960s-1980s, the technology was mainly

confined to high end main frame computer companies because the CTE mismatch between Si and PWB laminate required that FC use expensive ceramic packaging.” *EX1013* at p. 1.

45. “For FC to find widespread acceptance by those interested in miniaturized portable products such as lap tops, cell phones, pagers, camcorders etc., reliable lower cost FC processes were needed. In the early 1990s, IBM Japan reported that FC chips could be reliably attached directly to PWB laminate if the chips were underfilled. Unitive and Flip Chip Technologies (FCT) subsequently developed lower cost UBMs [(under bump metallization)], lower cost solder deposition technologies (FCT – stencil printing; Unitive – plating) and redistribution (RDL). The FCT and Unitive technologies were licensed by all the key assembly houses... as they initiated production in the early 2000s. This brought flip-chip technology to the masses.” *EX1013* at p. 1.

46. Flip chip packages were recognized as providing a number of benefits and solutions, namely, “for low to high pin count, high electrical performance demands from high-end memory, ASICs, and microprocessor applications where high frequency and high speed are required.” *EX1012* at p. 18.

47. In particular, it was known that “[f]lip-chip interconnections allow better electrical performance through lower inductances due to the shorter electrical

path between the chip and the substrate. The array of bumps under the chip also allows the die to shrink in size, which can reduce wafer cost. The flip-chip structure also allows you to make power and ground connections to internal points on a die, resulting in better chip performance. To increase thermal performance, optional heat spreaders can be attached on the backside of the flipped die.” *EX1012* at p. 18.

B. *Interposers and Dielectric Materials*

48. “Interconnection components, such as interposers are used in electronic assemblies to facilitate connection between components with different connection configurations or to provide needed spacing between components in a microelectronic assembly. Interposers can include a dielectric element [electrically insulating] in the form of a sheet or layer of dielectric material having numerous conductive traces extending on or within the sheet or layer. The traces can be provided in one level or in multiple levels throughout a single dielectric layer, separated by portions of dielectric material within the layer.” *EX1014* at 1:5-14. Within chip packages, such as a BGA package, an interposer was known to be used for “matching the chip I/O pitch with the pitch on the PWB.” *EX1013* at p. 1.

49. “Conventionally, semiconductor dice have been packaged in plastic or, less commonly, in ceramic packages.” *EX1015* at 1:50-51. Therefore, materials such as plastic (i.e., polymer) and ceramic were known and commonly used within the

field of chip packaging. In particular, polymer materials, such as, epoxy and polyimide, as well as ceramic materials, such as, silica (silicon dioxide), were commonly used as dielectric/insulation layers within interposer structures for chip packaging. *See, e.g., EX1016* at 23:10-13 (providing epoxy or polyimide as options for “insulating layers 320 and 330”); *EX1016* at 24:1-10 (specifying that the substrate 300 (BGA) may be a “glass fiber reinforced epoxy” or alternatively, a “ceramic substrate”).

50. “Packages may support, protect, and dissipate heat from semiconductor dice. Packages may also provide external connective elements for providing power and signal distribution to and from semiconductor dice, as well as for facilitating electrical testing, such as burn-in testing and circuit evaluation, of semiconductor dice prior to or after assembly thereof with higher level components, such as carrier substrates or circuit boards.” *EX1015* at 1:51-58. Thus, it would have been understood that a polymer substrate layer would have a suitable thickness to support and protect the coupled semiconductor devices, as well as to support mechanical processes such as drilling to form vias or “receptacles.” Specifically, Lee teaches “[s]ubstrates 12 that are formed from resins, or polymers, may have receptacles 11 formed therein by mechanical processes, such as drilling (including laser drilling), punching, milling, or die cutting.” *EX1015* at 8:38-41.

51. Savastiouk teaches a silicon substrate of an interposer with a thickness that “can be 100 μm or less.” *EX1017* at 4:32-34. Savastiouk also suggests a larger thickness by specifying “silicon substrate 140 can be thicker than described above[.]” *EX1017* at 4:47-50. Therefore, in light of the teachings of Savastiouk interposer substrates were known to include thicknesses of at least 100 μm .

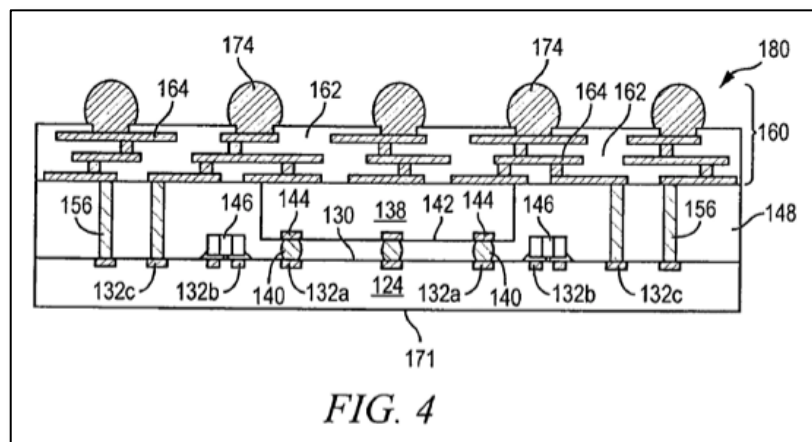
52. Further, it was known to provide interposers with materials other than silicon. Specifically, polymer-based interposers such as epoxy substrates with thicknesses within the range of 100 to 300 μm were known. Specifically, Lee-961 teaches “[t]he substrate 300 may be a ball grid array (BGA) substrate with a thickness [] of between 200 and 2,000 μm . Alternatively, **the substrate 300 may be a glass fiber reinforced epoxy based substrate with a thickness [] of between 200 and 2,000 μm .** Alternatively, the substrate 300 may be a silicon substrate with a thickness [] of between 200 and 2,000 μm . Alternatively, the substrate 300 may be a ceramic substrate with a thickness t15 of between 200 and 2,000 μm . Alternatively, the substrate 300 may be an organic substrate with a thickness t15 of between 200 and 2,000 μm .” *EX1016* at 24:1-10 (emphasis added.) Similarly, Haba-576 teaches “**First support portion 12 can, in some embodiments, have a thickness between 50 μm and up to 300 μm ,** although a greater thickness is possible. First support portion 12 can be of a dielectric material, **such as a polymeric resin material, for**

example polyimide, glass, or fiber-reinforced epoxy.” *EX1014* at 7:24-29 (emphasis added).

53. Additionally, Haba-576 teaches that “first support portion 12 further includes an inside surface 16 that is generally parallel to outside surface 14 and spaced apart therefrom to define a thickness of first support portion 12,” where “in an embodiment, first support portion 12 has a thickness of at least 5 μm ” and “can, in some embodiments, have a thickness between 50 μm and up to 300 μm ... [and] can be of a dielectric material such as a polymeric resin material, for example polyimide, glass, or fiber-reinforced epoxy” *EX1014* at 7:20-29. Haba-576 further teaches that “[f]irst in-process unit 10A’ includes first support portion 12 having first conductive vias 122 formed therein and first dielectric layer 52 formed over inside surface 16 of first support portion 12.” *EX1014* at 15:9-12. Thus, it was known that polymer layers, such as the first support portion 12 of Haba-576 could be fabricated at least up to 300 μm , while still supporting structures such as conductive vias 122.

54. Dielectric materials such as polymers were also used to form chip packages with dies/chip embedded in the dielectric layer. For example, Chi-977 teaches a chip package having a “semiconductor die 138” and an “encapsulant or molding compound 148 [that] is deposited over die 138.” *EX1131* at [0046]. The encapsulant 148 “can be a polymer composite material, such as epoxy resin with

filler, epoxy acrylate with filler, or polymer with proper filler.” *EX1131* at [0046]. As shown below, a plurality of “conductive pillars 156” are formed in encapsulant 148 having “a height ranging from 20-200 micrometers (μm).” *EX1131* at [0048]. As shown, the encapsulant/molding compound 148 has a height equal to the conductive pillars, demonstrating that dielectric/polymer layers were known to be formed at such a height. *EX1131* at FIG. 4. Further, dielectric/polymer layers having Chi-977’s thickness were known to “environmentally protect[] the semiconductor device from external elements and contaminants.” *EX1131* at [0046].

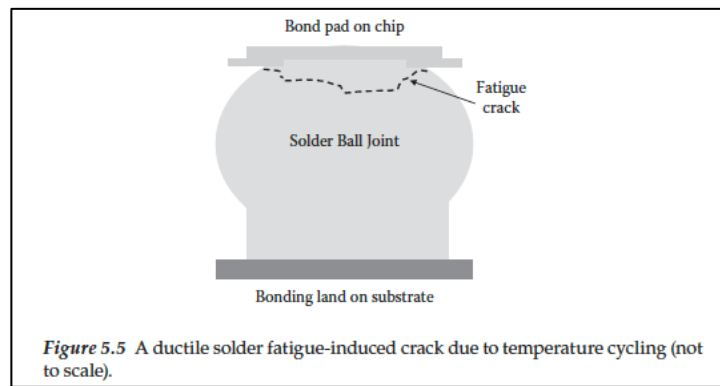


EX1131 at FIG. 4.

C. Coefficient of Thermal Expansion

55. The problem of mismatch of the coefficient of thermal expansion between packaging materials was well known. In particular, it was well known that “The thermal expansion mismatch between the chip and underfill causes stress

concentrations in certain locations, like at a die corner. As the crack propagates during continued stressing, the crack opens up the chip–underfill interface or another weakened section, causing either interconnect fatigue or an electrical failure in the chip’s dielectric.” *EX1012* at p. 45. As a result of this understanding, temperature cycling tests were typically employed in evaluating package reliability. “The purpose of temperature cycling is to check on package integrity in spite of the coefficient of thermal expansion mismatches between the various materials and their respective interfaces within the plastic package[.]” and that “[a]ll the components—the semiconductor chip, the metal lead frame or organic substrate, the polymer-based molding compound or die attach adhesive—within a package will likely have very different expansion and contraction rates while being heated or otherwise thermally stressed[.]” *EX1012* at p. 48-52. “Temperature cycling and thermal shock are the cause of numerous failure modes in semiconductor packages. Some of these modes include broken bond wire or lifted bonds from pads, solder joint/bump/ball fatigue (an example of which is shown in Figure 5.5), cracked molding compound, and the aforementioned interface delamination. *EX1012* at p. 54.



EX1012 at FIG. 5.5.

56. It was known that while “epoxy alone has a very high coefficient of thermal expansion, around $80 \times 10^{-6}/^{\circ}\text{C}$, compared to the silicon chip or copper lead frame or organic substrate[.]” (*EX1012* at p. 68) there were known techniques to reduce the coefficient of thermal expansion to more closely match that of silicon. Notably, “[f]illing the epoxy with silica filler brings down the thermal expansion coefficient into the teens, which would match the lead frame or substrate but would still be high compared to silicon. Using biphenyl or similar epoxy types allows more filler to be added and brings the coefficient down to the high single digits but still not as low as silicon, which is about $3 \times 10^{-6}/^{\circ}\text{C}$.” *EX1012* at p. 68.

57. Chuang teaches “a low-CTE packaging material for assembling a semiconductor die into a package[.]” *EX1018* at [0004]. Specifically, Chuang suggests that “[a] low-CTE die attach material 318 preferably comprises an epoxy with a negative-CTE filler, such as zirconium tungstate (ZrWOs), hafnium tungstate

(HfWOs), or a solid solution of zirconium and hafnium tungstate (Zos HfsWOs). Filler materials have a lower CTE than the packaging material in which they are mixed. This is generally done to more closely approximate the CTE of a silicon die, which may be about 3 ppm/C.” *EX1018* at [0019]. Thus, it was well understood that low-CTE polymer-based materials, such as a filled epoxy, could be used as a packaging material to more closely match the coefficient of thermal expansion of silicon.

D. *Through Vias and Metal Plugs*

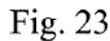
58. It was widely known that through vias could be disposed through an interposer substrate to provide a conductive path between the top and bottom of the interposer substrate. For example, Savastiouk teaches that “silicon substrate 140 includes metalized through-silicon vias 330 that pass between the top and bottom surfaces of substrate 140. Conductive paths are provided from contact pads 136C at the top of the interposer to contact pads 340 at the bottom of the interposer through the vias 330.” *EX1017* at 4:51-56.

59. Vias were also known to be used in non-silicon interposers. For example, Haba-576 teaches a first support portion 12, which “can be a dielectric material. Such as a polymeric resin material, for example polyimide, glass, or fiber-reinforced epoxy[.]” (*EX1014* at 7:26-29) and further that “[t]he interposer can also

include conductive elements such as conductive vias extending through the layer of dielectric material to interconnect traces in different levels.” *EX1014* at 1:14-17.

60. Through vias were metalized with materials such as copper to provide electrically conductive paths through an interposer. For example, Haba-576 teaches that “first conductive vias 22 are of a conductive material such as metal including copper, gold, nickel, aluminum, etc.” *EX1014* at 7:44-47. Additionally, Savastiouk teaches that “[c]onductive paths are provided from contact pads 136C at the top of the interposer to contact pads 340 at the bottom of the interposer through the vias 330.” *EX1017* at 4:54-56; *see also I.D.*, 5:54-61, 7:58-59.

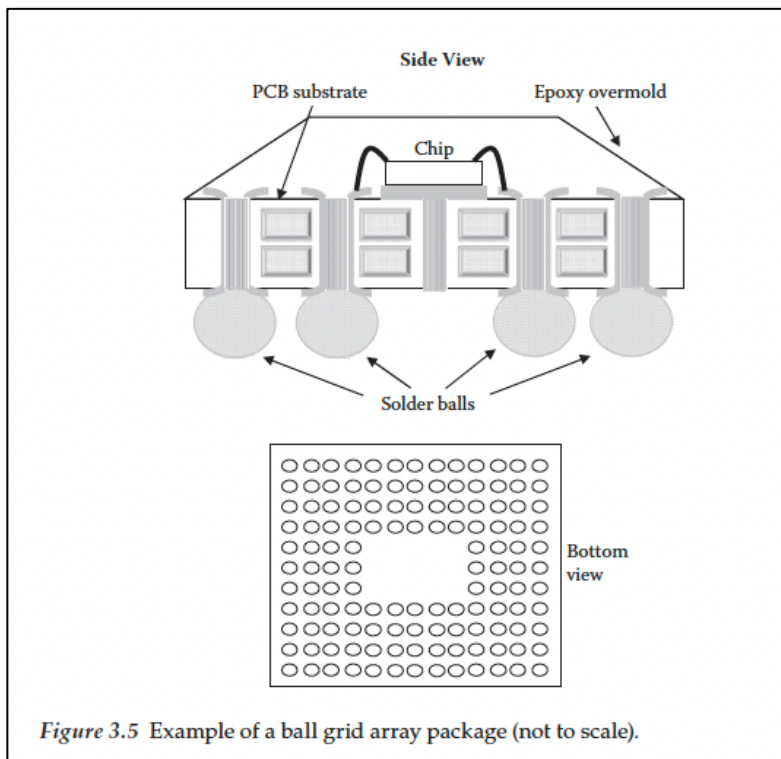
61. It was commonly understood that metal plugs could be positioned in vias. Specifically, Lin-232 teaches “The layers 52, 54 and 56 in the through vias 170 v compose multiple metal plugs (or metal vias) 5 p in the through vias 170v, including metal plugs (or metal vias) 5a, 5b, 5c, 5d, 5e and 5f in the through vias 170a, 170b, 170c, 170d, 170e and 170f as shown in FIG. 23, respectively.” *EX1019* at [0141].



EX1019 at FIG. 23.

62. Additionally, it was well known that the vias could be positioned into a pattern to match a contact pattern of a respective chip. For example, Grube teaches placing chips upon an interposer sheet with “each chip being positioned on a conforming via pattern[.]” *EX1020* at Abstract. The via patterns are taught as “conforming to the contact patterns of the chips.” *EX1020* at 2:42-47.

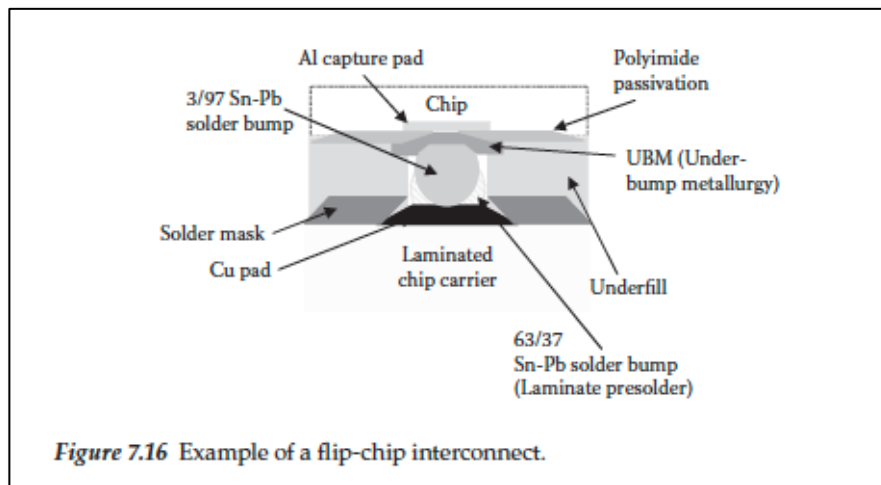
63. Similarly, vias could be arranged in other specific geometries, such as along the perimeter of the substrate. For example, Figure 3.5 of Chen, shown below, illustrates a ball grid array with respective solder balls coupled to vias arranged along the perimeter of the package with an open central region most clearly illustrated in the bottom view.



EX1012 at Figure 3.5, p. 29.

E. Solder Bumps

64. Within chip packaging solder bumps were widely used as an interconnection means between packaging components prior to September 26, 2012. Specifically, Chen teaches “[w]afer bumping is necessary to create an electrical and physical connection between a chip and a substrate in lieu of wire bonding. This method is used in flip-chip packaging and in wafer-level chip scale packaging.” EX1012 at p. 121. Additionally, Chen illustrates an exemplary flip-chip interconnect including a solder bump.



EX1012 at FIG. 7.16, p. 122.

65. As shown in the above image, solder bumps were formed on the metal pads of a chip (an “Al capture pad” in the above image). Indeed, in flip-chip packaging “solder bumps are firstly formed on the metal pad of a chip” then the chip “is put on a substrate” and the solder bumps “are aligned with pads of the substrate, and the chip and substrate are processed by means of heat treatment of reflow.” EX1132 at 1:40-45. “After the solder [is] melted, it forms a ball by means of surface tension, such that the connection between the chip and the substrate is complete.” EX1132 at 1:44-47.

66. It was well known that solder contained “pure tin, a tin-silver alloy, a tin-lead alloy or a tin silver-copper alloy[.]” EX1016 at 46:5-7. Additionally, referring to the European Union’s RoHS (Restriction of Hazardous Substances) directive made effective in 2006, “with RoHS and other ‘green’ initiatives, there is the move

toward Pb-free solders and alternate bump metallurgies.” *EX1012* at p. 123. Thus, motivation was present at least as early as 2006 to replace traditional lead-based solders with lead-free solder compositions, such as those taught by Lai, which contained tin (Sn). Specifically, Lai teaches a lead-free solder system with a lead-free solder layer 22 that “is SnAg with Ag content being controlled lower than 1.6 weight percent (wt%).” *EX1021* at [0022].

67. Additionally, it was known that solder bump structures could include multiple layers. For example, Lee’545 teaches a solder bump structure having layers including: barrier layers that “are typically used to prevent diffusion of an interconnect metal into surrounding layers of dielectric and silicon[.]” *EX1022* at 8:42-44; a pillar metal layer, notably, “a layer 38 of pillar metal has been deposited (electroplated) over the surface of the layer 36 of barrier material[.]” *EX1022* at 9:61-63; and an under-bump-metallurgy layer with “Layer 40 of UBM, typically of nickel and of a thickness between about 1 and 10 μm , is electroplated over the layer 38 of pillar metal.” *EX1022* at 10:19-21.

68. Multiple layers of distinct compositions were known to provide benefits within solder bump structures, such as “the improvement of adhesion of the various overlying layers or the prevention of diffusion of materials between adjacent layers.” *EX1022* at 3:49-56.

69. “The conductive bumps formed or placed on the bond pads fulfill several important electrical and mechanical functions. For one thing, it would be physically necessary to create a mechanical and electrical interconnect between the thin, recessed aluminum IC pads to a substrate land. Another issue is that connecting solder directly to aluminum is very tricky at best, but a thin metal layer would probably end up “leached” or dissolved by solder. A sandwich of various metallic layers, usually called the under-bump metallization or UBM, could prevent any material diffusion that would adversely affect the integrity of the connection. The bumps also insured a controlled gap between chip and substrate. If the chip and substrate were touching or nearly so, any CTE mismatch could result in high stress concentrations. By adding a gap, the bumps provide some stress relief.” *EX1012* at p. 122.

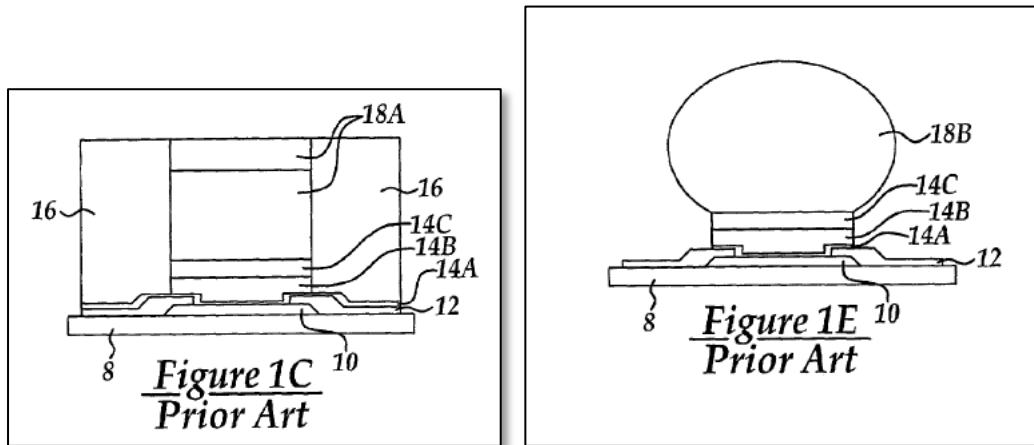
70. A common type of solder bump was known as ‘Controlled Collapse Chip Connection’ or “C4” bumps. The “basic idea of C4 is to connect chips (semiconductor devices), chip packages, or such other units by means of solder bumps between two surfaces of the units.” *EX1129* at 1:9-17. The “tiny bumps of electrically conductive solder bridge the gaps between respective pairs of metal pads on the units being connected. Each pad has a corresponding pad on the other unit’s surface; the pad arrangements are mirror images. As the units are pressed together

and heated the solder bumps on the pads of the first unit are contacted with corresponding conductive pads (having no bumps) on the second unit and reflowed, partially collapsing the solder bumps and making connections between respective pads” *EX1129* at 1:17-26. Conventionally, C4 bumps are “made from lead tin solder” but “lead-free requirements” required manufactures to “implement new ways to produce chip to substrates joints. For example, solder interconnects consisting of tin/copper, tin/silver and SAC alloys have been used as a replacement for leaded solder interconnects.” *EX1130* at 1:15-31.

F. *Methods of Forming Solder Bumps*

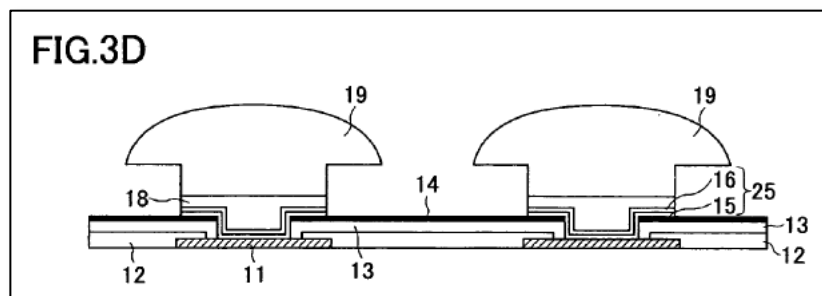
71. As I will detail herein, solder bumps/balls were typically formed by depositing layer(s) of solder material then performing a reflow step to form a spherical bump/ball geometry. For example, as shown below in FIG. 1C, a “column of solder material 18A may either be deposited in layers, for example, a layer of Pb followed by a layer of Sn, the solder material layers later being formed into a homogenous solder during a first reflow process[.]” *EX1023* at 2:45-39. “If the column of solder material is inhomogenous...a first reflow process is typically performed to harden the printed solder paste and form a homogenous column (plug) of solder material confined by the photoresist layer 16[.]” *EX1023* at 2:42-48. After

the photoresist layer 16 is removed, the “solder column 18 is then heated to reflow to form a solder bump 18B...as shown in FIG. 1E.” *EX1023* at 2:55-57.

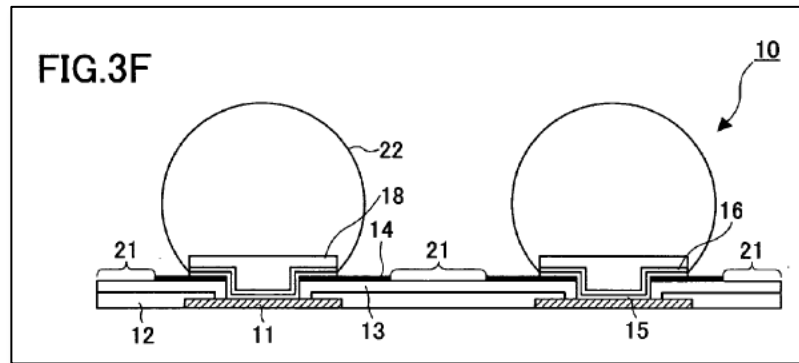


EX1023 at FIGS. 1C, 1E.

72. As another example, a solder bump may be formed by “plating” a “solder layer 19” that may be “an appropriate material, such as Sn/Cu, Sn/Ag, Sn/Ag/Cu, or Pb/Sn” in and on a resist 17. *EX1024* at [0046]; FIG. 3C. As shown below, in FIG. 3D, the “resist 17 may be removed” then “as illustrated in FIG. 3F, a “reflow treatment is performed to form a bump 22[.]” *EX1024* at [0049].



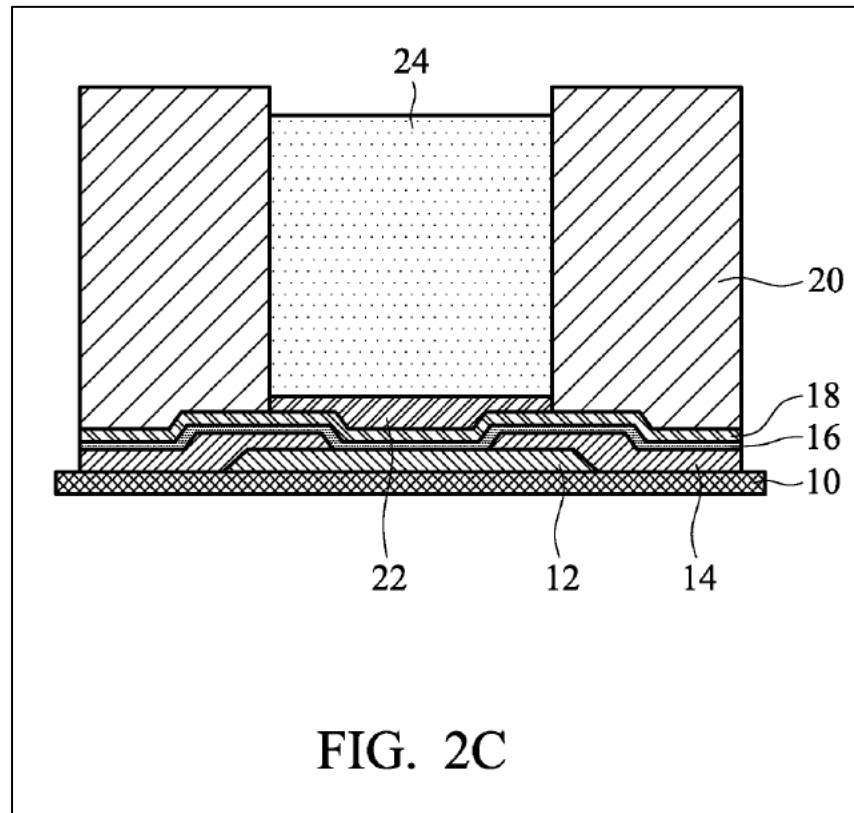
EX1024 at FIG. 3D.



EX1024 at FIG. 3F.

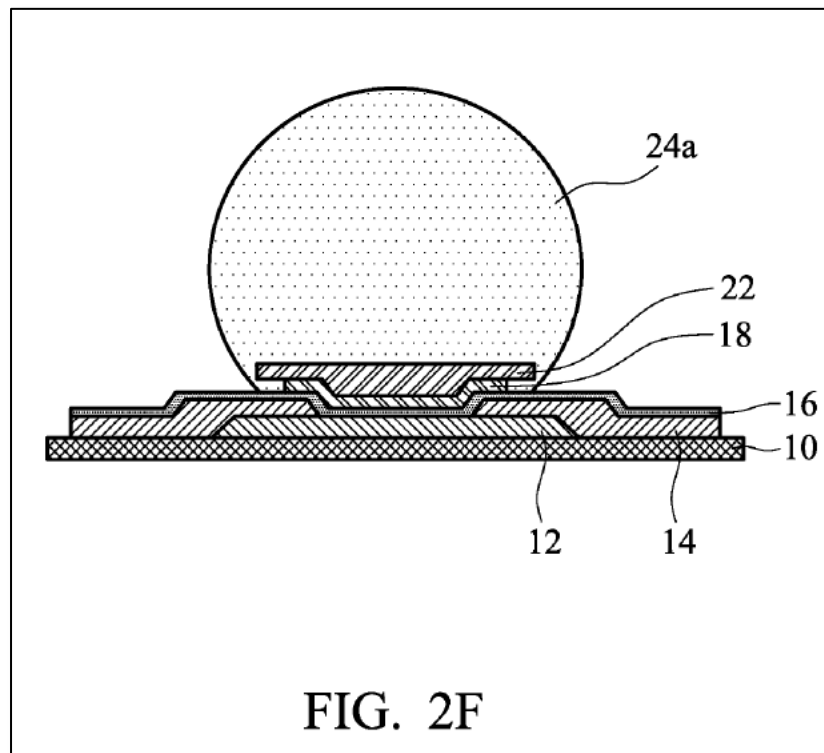
73. Wu-124 also demonstrates how solder balls/bumps are formed. Specifically, “as shown in FIG. 2C, a metallization layer 22 and a **solder material layer 24** are successfully formed in the opening 21” of a mask layer 20. “The solder material 24 is “electroplated within the opening 21 of the mask layer 20,” and as a result “the solder material layer retains a pillar shape within the opening 21.”

EX1025 at [0018]-[0019] (emphasis added).



*EX1025*at FIG. 2C.

74. The “mask layer 20 is then removed” and, as shown in FIG. 2F, a “thermal reflowing process is performed on the solder material layer 24, forming a hemi-sphere-shaped solder bump 24a.” *EX1025* at [0021].



EX1025 at FIG. 2F.

75. To control the size of the solder ball, it was known that “the actual amount of solder [] deposited will be a function of the desired end bump size. In other words, in order to form a large solder bump, a greater amount of solder [] material would be applied to the device than would be applied to form a small bump.” *EX1093* at 4:7-11.

76. Each of the above examples illustrate the process of forming solder bump/ball and particularly demonstrate that to form a solder bump/ball, a layer or layers of solder material (i.e., solder layers) are deposited, that are then subjected to a reflow treatment, thereby forming the bump/ball geometry. *See also EX1005* at

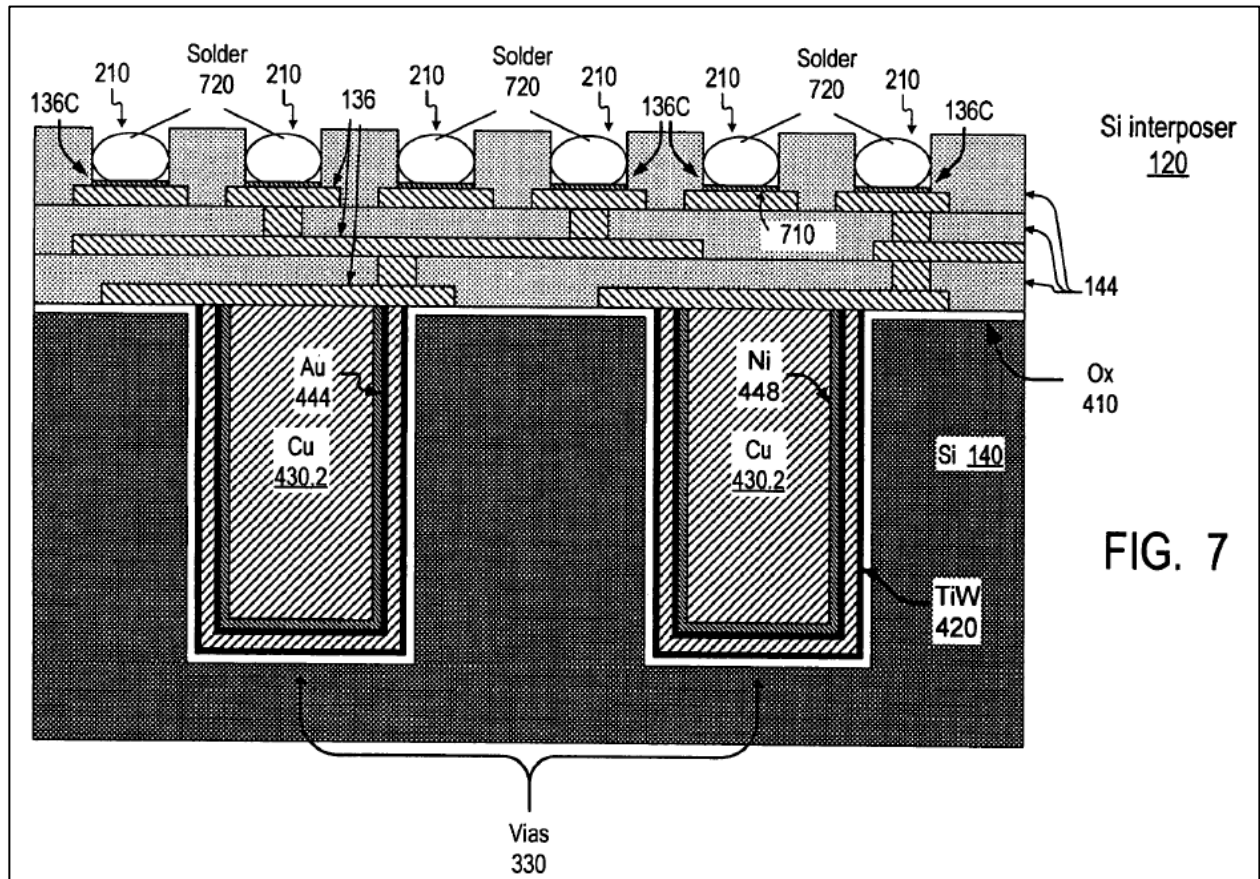
[0324] (“...the **solder layer** is reflowed to form multiple solid solder bumps or balls 29a[.]”) (emphasis added). The formation of solder bumps/balls via solder layers becomes relevant to the mapping of claims 2 and 12, reciting a “solder layer.”

G. *Interconnection Schemes and Redistribution Layers*

77. Interconnection schemes, such as those utilizing redistribution layers were well known and widely used prior to the ‘306 Patent. For example, Lin-604 teaches “[a]n RDL interconnection is formed over a surface of core 744. RDL interconnection may include passive circuitry as well, such as capacitor, resistor and inductor. As an example, insulation layer 747 is deposited over core 744 and patterned to expose metal layer 748. Metal layer 749 is deposited over insulation layer 747 and provides for re-routing electrical connections over a surface of core 744 within semiconductor package 700.” *EX1026* at 17:24-31.

78. The metal layers of an interconnection could be formed of copper and that a dielectric layer could be formed of a polymer, such as polyimide, among other suitable materials. Specifically, Savastiouk teaches “[m]etal layers 136 (FIG. 7) and dielectric layers 144 are deposited on the interposer wafer and patterned to provide interconnects and, possibly, other elements as described above. In some embodiments, metal 136 is copper and dielectric 144 is polyimide, but other materials can also be used. Some or all of dielectric layers 144 can be silicon dioxide,

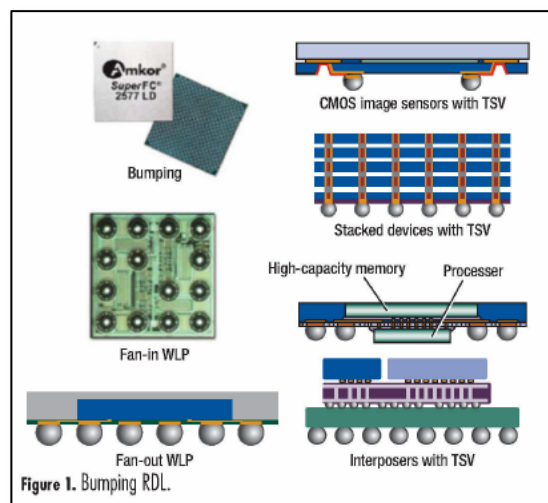
photosensitive benzocyclobutene (BCB), polybenzoxazole (PBO), or other materials.” *EX1017* at 6:18-26.



EX1017 at FIG. 7.

79. Further still, prior to the '306 Patent, it was well known that conductive metals, such as copper, were suitable as metallization for providing electrical conductivity to make electrical connections within a redistribution layer. For example, Garrou teaches “[t]he lack of area array designed chips was a major impediment to the early use of FC. RDL addressed this issue (**Fig. 1**) – defined by

the addition of metal and dielectric layers onto the surface of the wafer to re-route the I/O layout into a new, looser pitch footprint. Such redistribution requires thin film polymers (BCB, PI or newer polymers such as Asahi Glass ALX) and metallization (Al or Cu) to reroute the peripheral pads to an area array configuration.” *EX1013* at p. 1.



EX1013 at FIG. 1.

80. At the time of the ‘306 Patent, a number of manufacturing methods were known and widely used for providing interconnect structures. For example, Halahan teaches “electroplating and electroless plating of conductive materials into openings[.]” where the plated materials are “used to form through hole interconnects in integrated circuits.” *EX1027* at [0001]. Specifically, Halahan teaches “Dielectric 120 is deposited in the openings by chemical vapor deposition (CVD) or thermal oxidation. Metal 130 is sputtered on dielectric 120. Metal 140 is

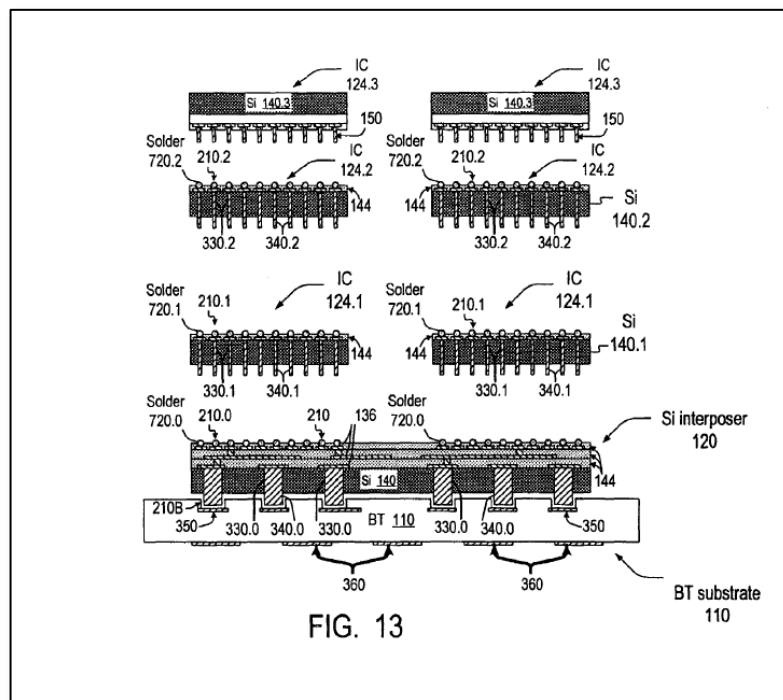
electrodeposited (electroplated) to fill up the openings.” *EX1027* at [0002]. Halahan further teaches that “[m]etal 140 increases the mechanical strength of the structure and improves heat dissipation.” *EX1027* at [0003]. Notably, Halahan lists advantages of electroplating as “high throughput and low tool cost” with electroless plating having “similar advantages.” *EX1027* at [0005].

H. *Semiconductor Chips*

81. Semiconductor chips were widely used well in advance of the ’306 Patent. Specifically, semiconductor chips, such as integrated circuits, were known to be coupled using chip packaging techniques such as flip-chip packaging as noted above. For example, Savastiouk teaches attachment of integrated circuits to other substrates in which “Integrated circuit dies (‘chips’) can be attached to a lead frame and then packaged in a ceramic or plastic carrier. The leads of the lead frame can then be soldered to a printed circuit board (PCB). Alternatively, the chip can be soldered directly to the PCB (‘flip chip’ packaging). The flip chip packaging reduces the package size and shortens the electrical connections between the die and the PCB.” *EX1017* at 1:26-32.

82. It was also known that packaging techniques could be used to couple multiple chips into a single package. For example, Savastiouk teaches coupling IC dies 124.1, 124.2, and 124.3 onto a single interposer 120. Specifically, Savastiouk

teaches “FIGS. 13–14 illustrate a possible manufacturing sequence with multiple die levels 124.1, 124.2, 124.3 attached to the packaging substrate.” *EX1017* at 10:22-24. The attachment of dies 124.1, 124.2, and 124.3 is further illustrated in FIG. 13 of Savastiouk shown below with multiple die levels stacked vertically over the interposer 120.



EX1017 at FIG. 13.

83. Further, Garrou teaches that “[i]ntegrating chips vertically in a single package multiplies the amount of silicon that can be crammed in a given package footprint, conserving hand held device real estate. At the same time, it enables shorter chip to chip routing, which speeds communication between them. Another

benefit is the simplification of board assembly because there are fewer components to be placed on the board.” *EX1028* at p. 4. Thus, a variety of benefits of vertically integrating chips was known.

84. In addition to vertically stacking chips, it was well known that integrated circuit chips could be attached on opposing sides of an interposer or circuit board. For example, Kinsman teaches attaching integrated circuits to opposing sides of a dielectric circuit board. “One way to satisfy the demand for increased integrated circuit density is to attach integrated circuits to opposing sides of a dielectric circuit board. A technique developed by the semiconductor industry to couple integrated circuits positioned on opposite sides of a circuit board to each other has been the creation of conductive vias through circuit boards. FIG. 1 is a partial isometric view of a circuit board 1 comprising a substrate 8 with holes 10 extending through its thickness 11 in any desired arrangement according to the prior art. The substrate 8 may comprise a BT or FR dielectric core, and the methods used to make the holes 10 include drilling, etching and laser ablation.” *EX1029* at [0003]. Thus, it was known that multiple semiconductor chips, such as integrated circuits, could be coupled to opposing sides of a substrate to increase integrated circuit density.

85. Savastiouk also suggests attaching integrated circuit structures on opposing sides of substrate by stating that PCB 130, which is positioned beneath

interposer 120 on an opposing side of integrated circuit dies 124 can be “replaced with another integrated circuit structure (a die or a wafer).” *EX1017* at 3:22-23; *see also I.D.* at FIGs. 2 and 3.

86. It was well known that semiconductor chips could include processing units such as central processing units and graphics processing units. More specifically, packaged systems included multiple distinct processing units. For example, Lin’152 teaches a system-on chip (SOC) including both a graphics processing unit and a central processing unit. “[A] system-on chip (SOC) including a graphics-processing-unit (GPU) circuit block, a wireless local area network (WLAN) circuit block and a central-processing-unit (CPU) circuit block designed by x86 architecture or by non x86 architectures, but not including any baseband circuit block,” *EX1030* at [1000].

87. Integration of central processing units and graphics processing units on a single chip, as well as the benefits associated with such integration, were well known in advance of the ‘306 Patent. For example, it was known as early as 2011 that the “integration trend of CMOS devices has led to fused architectures, in which the central processing units (CPUs) and graphics processing units (GPUs) are integrated onto the same chip.” *EX1031* at p. 1. “Recent examples include Intel’s sandy bridge [21], on which CPUs and GPUs are on one chip with a shared on-chip

L3 cache, and AMD accelerated processing unit (APU) [26] on which both on-chip CPUs and GPUs share the same off-chip memory [19].” *EX1031* at p. 1. Such combined GPU/GPU architectures were known to provide benefits such as the “opportunity to leverage both the high computational power from GPUs for regular applications and flexible execution from CPUs for irregular workloads” as well as bypassing “costly CPU-GPU data transfers[.]” *EX1031* at p. 1-2.

88. It was known that semiconductor chips may also comprise various insulating (dielectric) materials with interconnection structures therein that were used to connect such chips to each other and to chip packages. For example, Savastiouk teaches that “[e]ach die 124.1 has one or more metalized through vias 330.1 formed in the die’s semiconductor substrate 140.1 (e.g. monocrystalline silicon). Each via 330.1 passes between the top and bottom surfaces of substrate 140.1. Conductive paths are provided from contact pads at the top of each die 124.1 to contact pads 340.1 at the bottom of the die through the vias 330.1. Contact pads 340.1 protrude out of the respective vias 330.1. The dies 124.1 can be manufactured using the same techniques as described above for interposer 120 (involving the wafer thinning to expose the contact pads 340.1). Each die may have the same general structure as interposer 120 in FIGS. 10–12. Of course, the circuitry in dies 124.1 does not have to be identical to the interposer circuitry, and different dies 124.1 may

differ from each other. Also, contact pads 340.1 may have smaller dimensions, and may be placed closer to each other, as they do not have to meet the BT substrate dimension requirements. Pads 340.1 can be copper/nickel/gold structures as in FIG. 12, or they can be made from other materials. The metal in vias 330.1 is insulated from substrate 140.1 by a dielectric 410 (FIG. 12).” *EX1017* at 10:30-50. Additionally, Savastiouk teaches that “[d]ies 124.2 may be similar to dies 124.1. Dies 124.2 include metalized vias 330.2 in semiconductor substrates 140.2, and contact pads 340.2 protruding out of the vias on the bottom.” *EX1017* at 10:62-65.

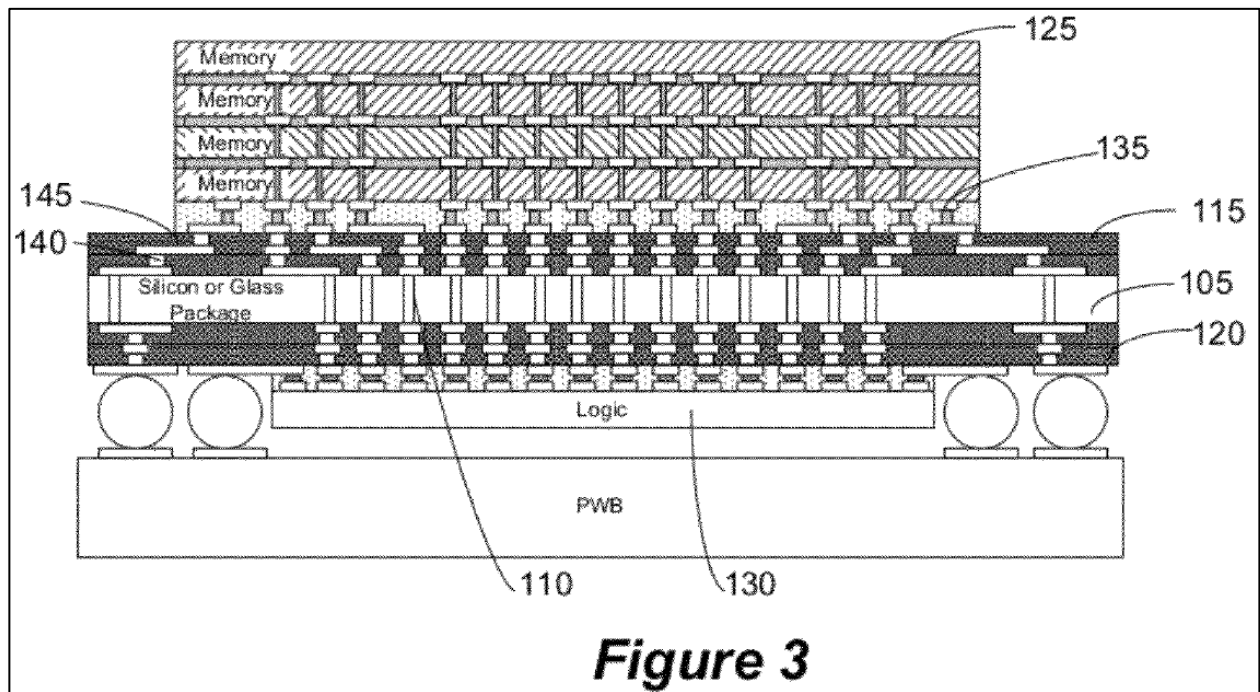
VI. SUMMARY OF THE PRIOR ART REFERENCES

A. *Sundaram*

89. Sundaram describes “various 3D packaging schemes” such as “a system-in-package (SIP) structure[,]” a “package-on-package (POP) structure[,]” a “face-to-face (F2F) structure[,]” and a “logic bottom stack [] structure.” *EX1004* at 1:33-42 Sundaram further describes that “multi-die stacking with TSVs imposes great challenges in forming TSVs within complementary metal oxide semiconductor (CMOS) chips, power delivery, testability, reliability, and thermal management of the logic chip, all of which remain major barriers in achieving high bandwidth for 3D ICs.” *EX1004* at 2:1-6. Sundaram teaches various “interposer interconnect structure[s]” and explains “embodiments of the present invention provide a testable

interposer interconnect structure[.]” *EX1004* at 2:24-67. The term “interposer interconnect structure” may “refer to connecting devices to form a package[.]” *EX1004* at 5:16-19

90. As shown below in FIG. 3, Sundaram teaches an “interconnect structure 100” having an “interposer 105” with a “first side 115 and a second side 120.” *EX1004* at 5:46-48. Interposer 105 “can be made of many substrate materials, for example, glass, silicon, ceramic, polymer-glass laminates, and flexible polymers.” *EX1004* at 5:54-56. There are a “plurality of small through vias 110...within the interposer 105” that “extends from the first side 115 to the second side 120.” *EX1004* at 6:6-9. Sundaram’s “through vias 110 can be metalized in such a way that the metallization provides die pad surfaces 135 that correspond to each of the vias 110” where the metallization material is “a highly-conductive metal, for example copper.” *EX1005* at 6:22-27.



EX1004 at FIG. 3.

91. As shown above, a “first electronic device 125 can be attached to the first side 115 of the interposer 105 and a second electronic device 130 can be attached to the second side 120 of the interposer 105.” *EX1004* at 6:34-36. first electronic device 125 “can be single or stacked memory IC devices, and the second electronic device 130 can be a logic IC device or devices.” *EX1004* at 6:37-39. Though “other electronic devices can also be used as the first electronic device 125 and/or the second electronic device 130.” *EX1004* at 6:39-42. Interposer 105 and through vias 110 “work to electrically connect the first electronic device 125 and second electronic device 130.” *EX1004* at 6:46-50. Additionally, as shown above,

Sundaram's interconnect structure 100 comprises "blind vias 140 and conductor traces 145 defined within polymer-metal redistribution layers deposited on the first side 115 and second side 120 of interposer 105." *EX1004* at 6:62-67. Sundaram's teachings allow for the "interposer 105 and the package [sic] can be one and the same." *EX1004* at 7:61-67.

92. I have been informed that for a prior art reference to be proper for use in an obviousness analysis, the reference must be "analogous art" to the claimed invention. I have been informed that a prior art reference is analogous to the claimed invention if the reference is from the same field of endeavor as the claimed invention or if it is reasonably pertinent to the particular problem that the inventor was trying to solve.

93. As discussed above, the field of endeavor of the claimed invention of the '306 Patent includes semiconductor packaging. *See* ¶¶ 31-33. As demonstrated above, Sundaram is directed to "interposer interconnect structure[s]" which may "refer to connecting devices to form a package[.]". *EX1004* at 5:16-19. Thus, Sundaram is directed to semiconductor chip packaging and accordingly is in the same field of endeavor as the claimed invention of the '306 Patent.

94. Sundaram is also reasonably pertinent to the problems solved by the inventors of the '306 Patent. As discussed above, the '306 Patent is directed to

minimizing temperature coefficient of expansion mismatching. *See* ¶¶ 34-38. Sundaram teaches that “[g]lass presents several advantages, namely, silicon-matched coefficient of thermal expansions (CTE)[.]” *EX1004* at 5:62-63. Thus, a POSITA would have consulted Sundaram and applied its teachings when faced with the problem of minimizing temperature coefficient of expansion mismatching. Additionally, the ‘306 Patent is directed to creating chip packages with pre-testability capability. *See* ¶¶ 34-38. Sundaram is concerned with the “testability” of 3D ICs and provides a “testable interposer interconnect structure.” *EX1004* at 7:41-43, 2:34-35. Thus, a POSITA would have consulted Sundaram and applied its teachings when faced with the problem of creating chip packages with pre-testability capability. Finally, the ‘306 Patent is concerned with the impact of miniaturization on circuit performance. *See* ¶¶ 34-38. Sundaram is likewise concerned with “ultra-fine pitch and ultra-short interconnections” in chip packages and associated “challenges[.]” *EX1004* at 1:65–2:20, *see also* 1:15-32, 2:21–3:6. Thus, a POSITA would have consulted Sundaram and applied its teachings when faced with the problem of the impact of miniaturization on circuit performance.

B. *Lin-191*

95. *Lin-191* describes system-in-package or multichip module architectures that incorporate multi-layer chips within a multi-layer polymer

structure, supported by on-chip and intra-chip metal bumps together with patterned metal layers. These modules provide electrical connection between multiple semiconductor chips and external circuits via “on-chip metal bumps the intra-chip metal bumps, and the patterned metal layers.” *EX1005* at Abstract. For example, chips are disclosed as being connected through multiple metal interconnects, including “patterned metal layers 2, 3, 4 and 5 and the metal pillars or bumps[.]” *EX1005* at [0462].

96. Lin-191 teaches specific thickness ranges for substrates and polymeric dielectric layers that are used in packaging semiconductor chips. For example, the substrate 110 may have a “thickness T1 between about 10 and about 1,000 micrometers between 10 and 100 micrometers or between 100 and 500 micrometers.” *EX1005* at [0051]. Dielectric or insulating layer such as layer 10 can be formed of “silicon dioxide (SiO₂), silicon nitride, silicon oxynitride, silicon carbon nitride, polyimide, epoxy, benzocyclobutane (BCB), polybenzoxazole (PBO), poly-phenylene oxide (PPO), silosane or SU-8 having a suitable thickness, e.g., between 0.3 and 30 micrometers, and preferably between 1 and 10 micrometers.” *EX1005* at [0052]. Additional dielectric layers such as insulating layer 15 are disclosed with thicknesses “between 1 and 20 micrometers, and preferably between 3 and 15 micrometers or between 5 and 10 micrometers[.]” *EX1005* at

[0291]. Encapsulation is provided by polymer molding layers such as encapsulating layer 85, which has a thickness “between about 20 and about 500 micrometers, and preferably between 30 and 100 micrometers.” *EX1005* at [0109]. Build-up polymer layers including polymer layer 78 are specified at thicknesses “between 5 and 50 micrometers, and preferably between 5 and 15 micrometers or between 5 and 10 micrometers[.]” *EX1005* at [0368]. A “passivation layer 501 over the semiconductor substrate 601” may be formed. *EX1005* at [0552].

97. Lin-191 also describes interconnects and bump structures that connect the layers described above. For example, bumps 24 are described as having a “height greater than 5 micrometers, such as between 5 and 50 micrometers, and preferably between 10 and 20 micrometers,” while bumps 14 are larger, with a “height greater than 15 micrometers, such as between 15 and 520 micrometers, and preferably between 20 and 110 micrometers[.]” *EX1005* at [0066], [0099]. At the package level, solder balls for external board connection are described. *EX1005* at [0007], [0048], [0490].

98. Lin-191 incorporates passive devices directly into the package. In one embodiment, a chip “can be replaced by a passive component 67, such as capacitor, inductor or resistor.” *EX1005* at [0340]. In another embodiment, discrete passive components 910 are mounted between upper-tier chips, coupled through “multiple

solder joints 915,” “patterned metal layer 7,” and “bumps 64[.]” *EX1005* at [0364]-[0368]. A polymer layer such as polymer layer 78 can be formed “on the discrete passive components 910.” *EX1005* at [0364]-[0368].

99. Lin-191 further discloses multiple semiconductor chips integrated into a single package. These chips “can be a central-processing-unit (CPU) chip designed by x86 architecture, a central-processing-unit (CPU) chip designed by non x86 architectures, such as ARM, Strong ARM or MIPs, a baseband chip, a graphics-processing-unit (GPU) chip, a digital-signal-processing (DSP) chip, a wireless local area network (WLAN) chip, a memory chip, such as flash memory chip, dynamic-random-access-memory (DRAM) chip or statistic-random-access-memory (SRAM) chip, a logic chip, an analog chip, a power device, a regulator, a power management device, a global-positioning-system (GPS) chip, a Bluetooth chip...” *EX1005* at [0240], [0382]. Electrical connections between chips are made through “metal layer 63 of the patterned metal layer 6 and on tops of the metal pillars or bumps 54 and 64[.]” *EX1005* at [0241].

100. Lin-191 discusses the use of the multichip modules for pre-testability capability. Lin-191 explains that wafer level packaging allows for the integration of pre-testability “before being singulated by dicing for final assembly into a chip carrier package[.]” *EX1005* at [0006]. Lin-191 describes that the “testing circuit is

either (i) the wafer level testing performed before the chip 700 or 800 is sawed or diced apart from a wafer, or (ii) the package level testing (the final testing) after the chips 700 and 800 are connected to each other” *EX1005* at [0492]. Each chip is equipped with dedicated test structures, as “the chip 700 may include ... two testing interface circuits 333a and 333b” while “the chip 800 may include ... two testing interface circuits 333c and 333d” *EX1005* at [0462]. These test interfaces may be implemented as scan test circuits where each “of the test interface circuits 333a, 333b, 333c and 333d ... can be a scan test circuit ... used for scan testing ... at wafer level ... or at the package level testing (the final testing)[.]” *EX1005* at [0493].

101. I have been informed that for a prior art reference to be proper for use in an obviousness analysis, the reference must be “analogous art” to the claimed invention. I have been informed that a prior art reference is analogous to the claimed invention if the reference is from the same field of endeavor as the claimed invention or if it is reasonably pertinent to the particular problem that the inventor was trying to solve.

102. As discussed above, the field of endeavor of the claimed invention of the '306 Patent includes semiconductor packaging. *See ¶¶ 31-33*. As demonstrated above, Lin-191 is directed to “system-in packages, or multichip modules... includ[ing] multi-layer chips in a multi-layer polymer structure, on-chip metal

bumps on the multi-layer chips, intra-chip metal bumps, in the multi-layer polymer structure, and patterned metal layers in the multi-layer polymer structure.” *EX1005* at [0007], [0003]. Thus, Lin-191 is directed to semiconductor packaging and accordingly is in the same field of endeavor as the claimed invention of the ’306 Patent.

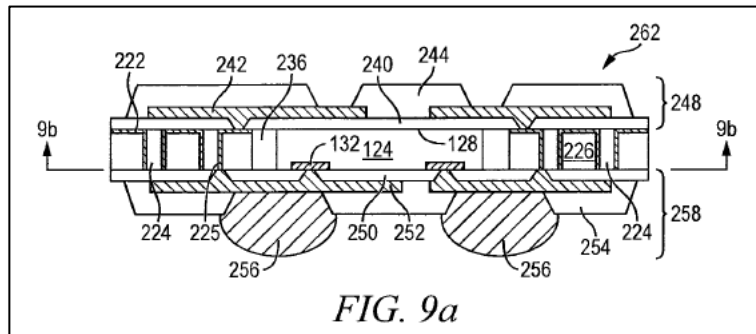
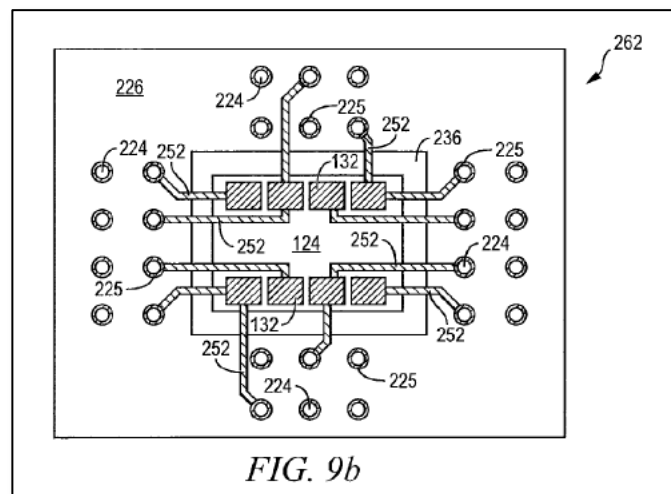
103. Lin-191 is also reasonably pertinent to the problems solved by the inventors of the ’306 Patent. As discussed above, the ’306 Patent is directed to solving the problem of providing chip packages with pre-testability capability. *See* ¶¶ 34-38. As demonstrated above, Lin-191 discloses that “the chip 160 may have built-in self test (BIST) circuits for reducing the testing time for the system-in-package or multichip module.” *EX1005* at [0401]. Further, Lin-191 describes test structures such as “testing interface circuits 333a–333d” that can be used for wafer-level or package-level scan testing before or after the chips are diced and packaged. *EX1005* at [0462], [0492-0493]. Thus, a POSITA would have consulted Lin-191 and applied its teachings when faced with the problem creating chip packages with pre-testability capability. *See also EX1005* at [0006], [0105], [0173], [0239], [0401] (all concerned with testing in a chip package).

C. Lin-863

104. Lin-863 is directed to “a semiconductor device and method of forming an interconnect substrate for a Fo-WLCSP” (fan-out wafer level chip scale package). *EX1007* at 1:7-10, 2:14-15. Lin-863 teaches that “a need exists to reduce CTE mismatch between the encapsulant and substrate in a Fo-WLCSP” because “CTE mismatch...causes stress during thermal cycling, leading to defects and higher manufacturing costs.” *EX1007* at 2:29-30, 2:23-25.

105. Accordingly, Lin-863 teaches “an interconnect substrate with conductive TMV for a Fo-WLCSP” *EX1007* at 3:31-32. As shown below, Lin-863’s interconnect substrate includes a “TMV interconnect substrate 220 with conductive layer 222” that is “formed over encapsulant 226 and conductive TMV 225 formed through the encapsulant.” *EX1007* at 12:34-38. There are a “plurality of openings 228 [] formed in encapsulant for disposing of semiconductor die 124” which is then covered with “an encapsulant or molding compound 236.” *EX1007* at 12:40-42, 12:61-62. An “electrically conductive layer or RDL 242 is formed over insulating layer 240 and conductive layer 222” made of “Al, Cu, Sn, Ni, Au, Ag, or other suitable electrically conductive material.” *EX1007* at 13:21-26. Additionally, an “electrically conductive bump material” is formed that “can be Al, Sn, Ni, Au, Ag, Pb, Bi, Cu, solder, and combinations thereof[.]” *EX1007* at 14:17-22. FIG. 9a below

shows a “cross-sectional view of Fo-WLCSP 262 after singulation” and FIG. 9b shows a “plan view[.]” *EX1007* at 14:45-46, 14:51.



EX1007 at FIGS. 9a-b.

106. I have been informed that for a prior art reference to be proper for use in an obviousness analysis, the reference must be “analogous art” to the claimed invention. I have been informed that a prior art reference is analogous to the claimed invention if the reference is from the same field of endeavor as the claimed invention

or if it is reasonably pertinent to the particular problem that the inventor was trying to solve.

107. As discussed above, the field of endeavor of the claimed invention of the ‘306 Patent includes semiconductor packaging. *See* ¶¶ 31-33. As demonstrated above, Lin-863 is directed to an “interconnect structure for a Fo-WLCSP.” *EX1007* at 1:7-10, 1:14–2:25. Thus, Lin-863 is directed to semiconductor chip packaging and accordingly is in the same field of endeavor as the claimed invention of the ‘306 Patent.

108. Lin-863 is also reasonably pertinent to the problems solved by the inventors of the ‘306 Patent. As discussed above, the ‘306 Patent is directed to solving the problem of minimizing temperature coefficient of expansion mismatching. *See* ¶¶ 34-38. As demonstrated above, Lin-863 is concerned with the “CTE mismatch between the encapsulant and substrate in a Fo-WLCSP.” *EX1007* at 2:29-30, 11:20-46, 12:11-32, 14:43-65. Thus, a POSITA would have consulted Lin-863 and applied its teachings when faced with the problem of minimizing temperature coefficient of expansion mismatching.

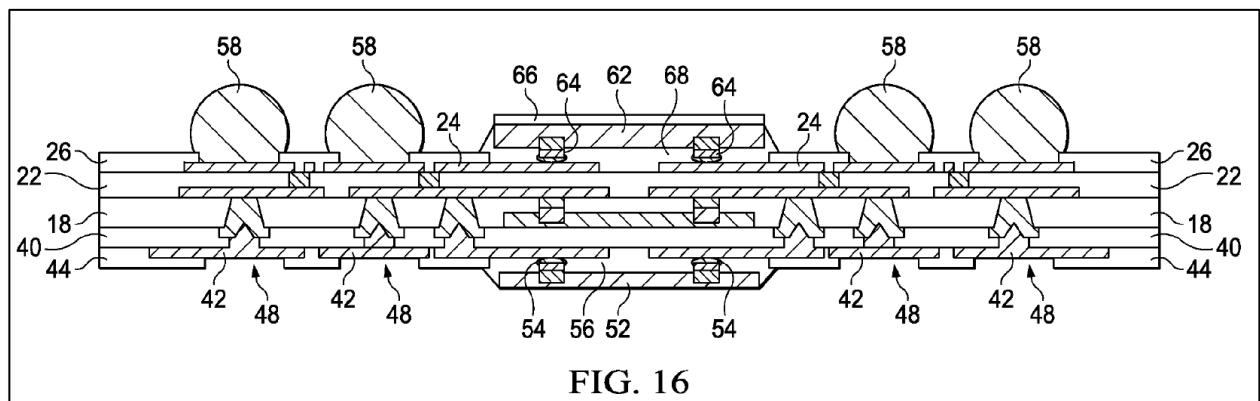
D. Yu

109. Yu describes that a “Package-on-Package (PoP) is an integrated circuit packaging technique to allow vertically combining discrete logic and memory ball

grid array (BGA) packages.” *EX1010* at 1:49-55. Accordingly, Yu teaches a PoP structure comprising a package 202. *EX1010* at 2:9-10, 2:15-16, 8:26-39. Yu’s package 202 comprises a “core material, such as molding compound 18” made of an “epoxy, polyimide, silicone rubber...or a combination thereof” that is cured over a “first die 10[.]” *EX1010* at 2:61-67. Yu’s package further comprises a “front side interlayer dielectric (ILD) and redistribution layer (RDL) structure” made of a “first front side metallization layer 20” and a “first ILD layer 22” made of polyimide. *EX1010* at 3:4-22. Additional metallization layers and ILD layers, “such as a second metallization layer 24 and a second ILD layer 26” are formed as part of the front side RDL. *EX1010* at 3:28-32.

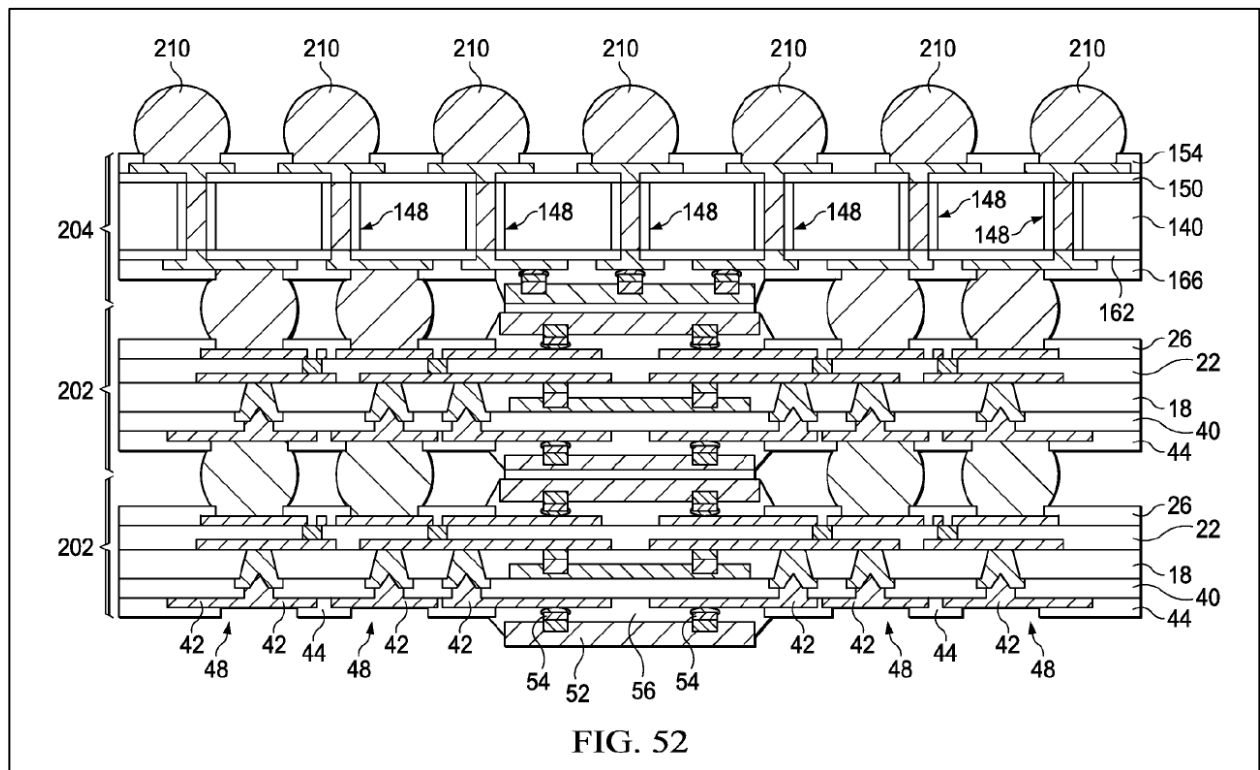
110. TMV openings 36 are “formed through the molding compound 18 to the front side metallization layer 20” then a copper “seed layer is deposited...into the TMV openings 36.” *EX1010* at 3:56-65. “A conductive material, such as copper” is then deposited on the back side by “electroplating” thereby forming “TMVs 38[.]” *EX1010* at 3:67–4:6. Yu’s package 202 additionally includes a “back side ILD and RDL structure” formed of a “first back side ILD layer 40, a second back side metallization layer 42, a second ILD layer 44, and openings 46 and 48 through the second ILD layer 44 to the second back side metallization layer 42.” *EX1010* at 4:7-11. As shown in the figure below, a “second die 52, such as a memory die...is

attached through the opening 46 to conductive features in the second back side metallization layer 42, such as by conductive connectors 54, like controlled collapse chip connection (C4) bumps.” *EX1010* at 4:30-34. “[C]onductive connectors 58, such as ball grid array (BGA) balls” are formed on package 202 which may be a “lead-free solder.” *EX1010* at 4:45-50. Finally, a “third die 62, such as a memory die [is]...attached through the openings 30 to conductive features in the second front side metallization layer 24” also by C4 bumps. *EX1010* at 4:53-60.



EX1010 at FIG. 16.

111. The package of FIG. 16 may be stacked alongside additional packages forming the PoP structure:



EX1010 at FIG. 52.

112. In one embodiment, Yu teaches forming an “interposer and a die attached to the interposer” and teaches, with reference to a “substrate 140” used in forming the interposer that “it is believed that using silicon substrates for the interposer may reduce stress because the coefficient of thermal expansion (CTE) mismatch between the silicon substrates and the silicon typically used for the dies is lower than with substrates formed of different materials.” *EX1010* at 6:14-26.

113. I have been informed that for a prior art reference to be proper for use in an obviousness analysis, the reference must be “analogous art” to the claimed invention. I have been informed that a prior art reference is analogous to the claimed

invention if the reference is from the same field of endeavor as the claimed invention or if it is reasonably pertinent to the particular problem that the inventor was trying to solve.

114. As discussed above, the field of endeavor of the claimed invention of the ‘306 Patent includes semiconductor packaging. *See* ¶¶ 31-33. As demonstrated above, Yu is directed to “Package-on-Package (PoP)” structures including “integrated circuit packaging[.]” *EX1010* at 1:49-55, *see also* 1:10-48, 1:63-67, 4:17-20. Thus, Yu is directed to semiconductor chip packaging and accordingly is in the same field of endeavor as the claimed invention of the ‘306 Patent.

115. Yu is also reasonably pertinent to the problems solved by the inventors of the ‘306 Patent. As discussed above, the ‘306 Patent is directed to solving the problem of minimizing temperature coefficient of expansion mismatching. *See* ¶¶ 34-38. As demonstrated above, Yu teaches that “it is believed that using silicon substrates for the interposer may reduce stress because the coefficient of thermal expansion (CTE) mismatch between the silicon substrates and the silicon typically used for the dies is lower than with substrates formed of different materials.” *EX1010* at 6:20-26. Thus, a POSITA would have consulted Yu and applied its teachings when faced with the problem of minimizing temperature coefficient of expansion mismatching. Additionally, the ‘306 Patent is directed to solving the problem

creating chip package with pre-testability capability. *See* ¶¶ 34-38. Yu teaches “a step to test the PoP structure[.]” *EX1010* at 2:17-20. Thus, a POSITA would have consulted Yu and applied its teachings when faced with the problem of creating chip package with pre-testability capability.

E. Camacho

116. Camacho teaches that a “need exists for PoP [Package-on-Package] vertical integration compatible with WLSCPs” (wafer level chip scale package). *EX1006* at [0010], [0008]. Camacho teaches techniques for forming through-silicon vias (TSVs) and vertically integrated packages. Specifically, Camacho teaches that “a plurality of vias is formed through semiconductor wafer 120” and that the “vias are filled with Al, Cu, Sn, Ni, Au, Ag, titanium (Ti), W...to form conductive TSV 134.” *EX1006* at [0043]. These TSVs provide vertical electrical interconnections between conductive layers, as “conductive layers 130 and 132 are electrically connected by TSV 134.” *EX1006* at [0043]. Camacho’s TSVs provide a method for establishing reliable electrical pathways through the semiconductor wafer using conductive materials well-known in the art.

117. Camacho further illustrates how stacked dies may be electrically connected using flip-chip technology. As shown in Figure 3d, Camacho describes mounting a “semiconductor die or package 140” to die 122 “in a flipchip

arrangement with bumps 142 electrically connected to a conductive layer 130b.” *EX1006* at [0044]. This arrangement shows a die-to-die interconnection scheme that leverages solder bumps to form connections to underlying conductive layers.

118. Additionally, Camacho teaches embodiments involving multiple semiconductor chips in stacked configurations. For example, Camacho teaches a “semiconductor die or package 150” that is positioned on top of die 122. *EX1006* at [0047]. Camacho also provides details on the electrical connectivity of the upper die/package. Specifically, Camacho explains that die 150 includes “[c]ontact pads 152...electrically connected to bumps 148, conductive layer 130a, TSVs 134, and conductive layer 132a.” *EX1006* at [0047]. Moreover, Camacho discloses earlier embodiments in which contact pads are explicitly described as metal. For instance, with respect to FIGS. 2A–2C, Camacho teaches “contact pads 76” that are “one or more layers...of aluminum (Al), copper (Cu), tin (Sn), nickel (Ni), gold (Au), or silver (Ag)[.]” *EX1006* at [0035].

119. Additionally, Camacho teaches that “the flip chip semiconductor device provides a short electrical conduction path from the active devices on semiconductor die 58 to conduction tracks on PCB 52 in order to...lower capacitance, and improve overall circuit performance.” *EX1006* at [0038]. A POSITA would have understood Camacho to be referring to parasitic capacitance,

as shortening electrical pathways was known to decrease parasitic capacitance that degrades signal quality.

120. I have been informed that for a prior art reference to be proper for use in an obviousness analysis, the reference must be “analogous art” to the claimed invention. I have been informed that a prior art reference is analogous to the claimed invention if the reference is from the same field of endeavor as the claimed invention or if it is reasonably pertinent to the particular problem that the inventor was trying to solve.

121. As discussed above, the field of endeavor of the claimed invention of the ‘306 Patent includes semiconductor packaging. *See* ¶¶ 31-33. As demonstrated above, Camacho is directed to the field of semiconductor device packaging, and in particular to wafer level chip scale packages (WLCSPs), through-silicon vias (TSVs), and package-on-package (PoP) vertical interconnections. *EX1006* at [0001], [0008]-[0009]. As explained, “the electrical interconnection between a wafer level chip scale package (WLCSP) containing semiconductor devices on multiple levels (3-D device integration) and external devices can be accomplished with conductive through silicon vias (TSV) or through hole vias (THV).” *EX1006* at [0008], *see also* [0016]. Thus, Camacho is directed to semiconductor chip packaging and accordingly is in the same field of endeavor as the claimed invention of the ‘306 Patent.

122. Camacho is also reasonably pertinent to the problems solved by the inventors of the '306 Patent. As discussed above, the '306 Patent is directed to solving the problem of the impact of miniaturization of circuit performance. See ¶¶ 34-38. Camacho is also directed to addressing the problem of the impact of miniaturization on circuit performance, specifically the need for planarization to enable smaller and more densely packed circuit components. Camacho explains that “depositing a thin film of material over an existing pattern can exaggerate the underlying pattern and create a non-uniformly flat surface” and that “a uniformly flat surface is required to produce smaller and more densely packed active and passive components.” *EX1006* at [0028]. To address this, Camacho teaches that “planarization can be used to remove material from the surface of the wafer and produce a uniformly flat surface,” where the process involves “polishing the surface of the wafer with a polishing pad” and adding an “abrasive material and corrosive chemical” such that “the combined mechanical action of the abrasive and corrosive action of the chemical removes any irregular topography, resulting in a uniformly flat surface.” *EX1006* at [0028]. Thus, a POSITA would have consulted Camcho and applied its teachings when faced with the problem of the impact of miniaturization of circuit performance.

123. Additionally, the ‘306 Patent is directed to solving the problem of parasitic capacitance of interconnections in a chip package. *See* ¶¶ 34-38. As discussed, Camacho is concerned with “lower[ing] capacitance” in a chip package. *See* ¶ 119; *EX1006* at [0038]. Thus, a POSITA would have consulted Camacho and applied its teachings when faced with the problem of parasitic capacitance of interconnections in a chip package.

VII. SUMMARY OF UNPATENTABILITY

124. I have reproduced the Proposed Grounds of Unpatentability from the Petition for ease of reference:

Grounds	Claims Challenged	35 U.S.C. §	References
<u>1A</u>	1-7, 9-11, 13-15, 17-27	103	Sundaram (EX1004) and Lin-191 (EX1005)
<u>1B</u>	8, 12, 16	103	Sundaram, Lin-191, and Lin-863 (EX1007)
<u>2A</u>	1-7, 9-15, 17-20, 22-27	103	Yu (EX1010) and Lin-191
<u>2B</u>	8, 16	103	Yu, Lin-191, and Lin-863
<u>2C</u>	21	103	Yu, Lin-191, and Camacho (EX1006)

VIII. OPINIONS REGARDING GROUND 1A: CLAIMS 1-7, 9-11, 13-15, AND 17-27 ARE OBVIOUS OVER SUNDARAM AND LIN-191

A. Claim 1

1. 1(Pre): “A chip package comprising”

125. Sundaram teaches various “interconnect structure[s]” to “form a package[.]” *EX1004* at 5:16-19. As shown in FIG. 3 below, Sundaram’s interconnect structure comprises an “interposer 105” that “electrically connect[s] the first electronic device 125 and the second electronic device 130[.]” enabling the “interposer 105 and the package can [*sic*] be one and the same.” *EX1004* at 5:45-48, 6:46-48, 7:61-63. The first electronic device 125 “can be single or stacked memory IC devices, and the second electronic device 125 can be a logic IC device or devices.” *EX1004* at 6:37-39. ICs (integrated circuit) were known to be formed on semiconductor chips such that Sundaram’s interconnect structure and electronic devices 125, 130 collectively form a *chip package*¹. See, e.g., *EX1133* at 1:14-17

¹ Claim language provided in italics. All drawing annotations added. Citations to a claim limitation and/or section number are to the limitations mapping in this Declaration and are incorporated by reference, including the motivations to combine and showing of reasonable expectation of success provided in the cross-referenced

(“...has led to increasingly more complex **integrated circuits being produced** in an increasingly smaller space **on semiconductor chips.**”).

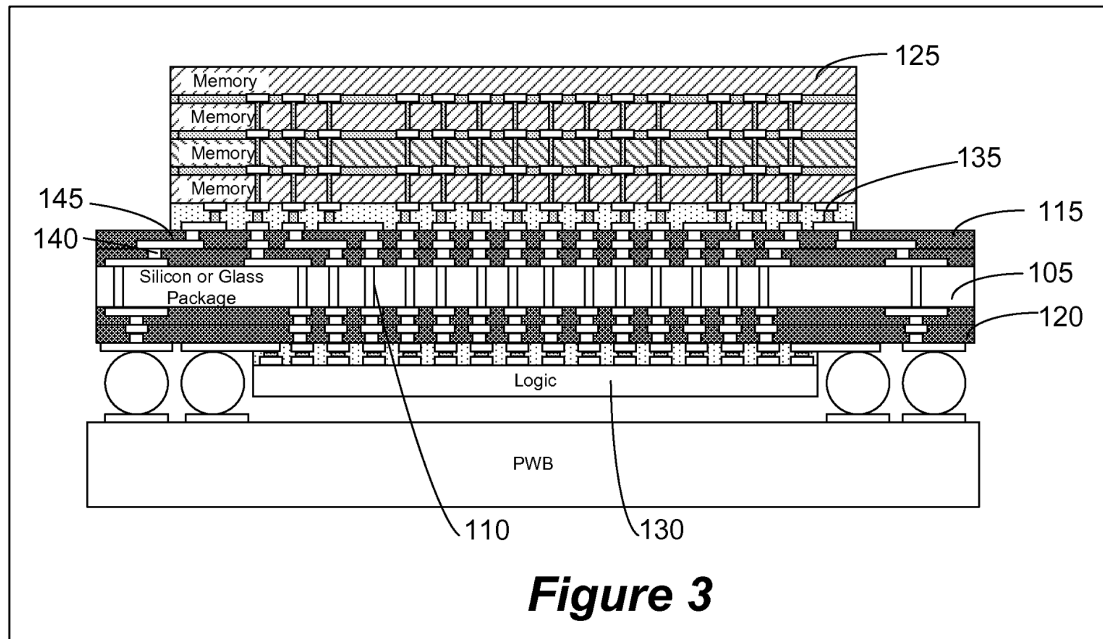


Figure 3

EX1004 at FIG. 3.

2. *1(a): “a solid layer having a first surface and a second surface opposite to said first surface,”*

126. Sundaram’s *chip package* (interconnect structure) comprises an “interposer 105 having a first side and a second side” (*a first surface and a second surface*) and is “made of...glass” or “polymer-glass laminates[.]” EX1004 at 2:22-

section. All reasonable expectations of success include the benefits described for the respective motivation to combine. All emphases added unless otherwise noted.

27, 5:54-58. Because interposer 105 is “made of...glass” or “polymer-glass laminates[,]” interposer is a *solid layer*. I note that the ‘306 Patent describes that a “glass layer 16 refers to an amorphous **solid**” and the “material of glass layer 16 may be...boro-silicate glass[.]” *EX1001* at 7:12-14. As discussed below at Claim 1(a)(ii), Sundaram teaches that interposer 105 (*solid layer*) comprises “glass,” such as “borosilicate glass[.]” *EX1004* at 5:54-58, 9:14-16; ¶ 128. Thus, Sundaram’s interposer 105 is a *solid layer* in at least the same way as described by the ‘306 Patent.

127. Thus, Sundaram’s interposer 105 (*solid layer*) comprises a *first surface* and a *second surface*. Further, as shown in the image below, Sundaram’s *second surface* is *opposite to said first surface*.

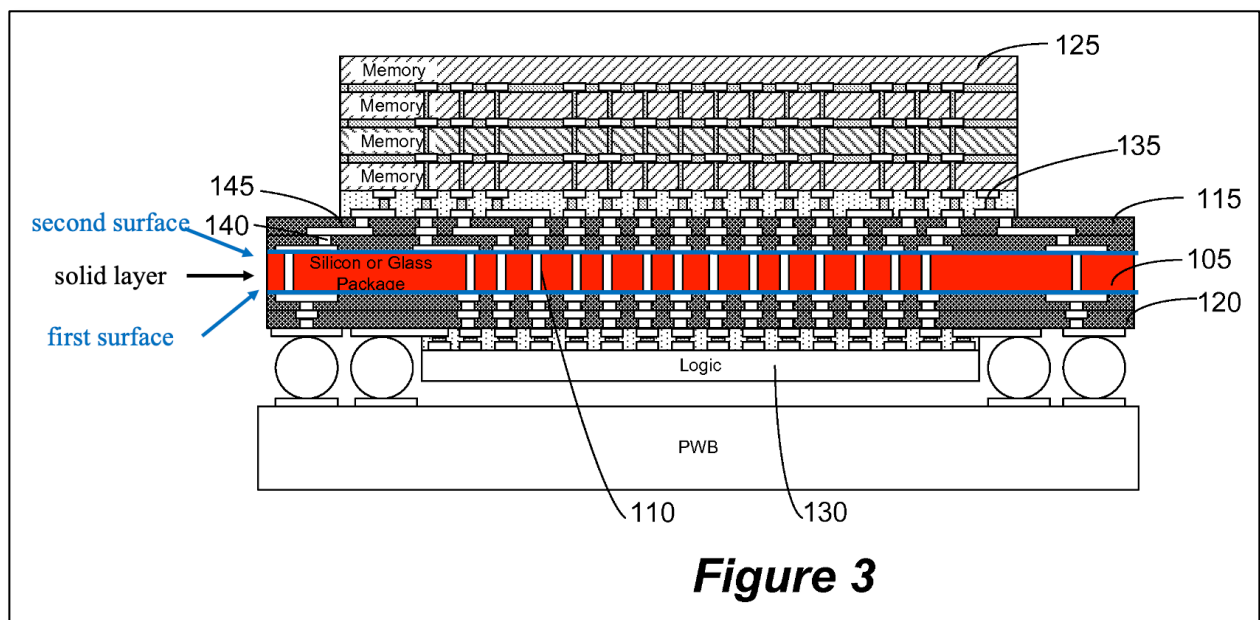


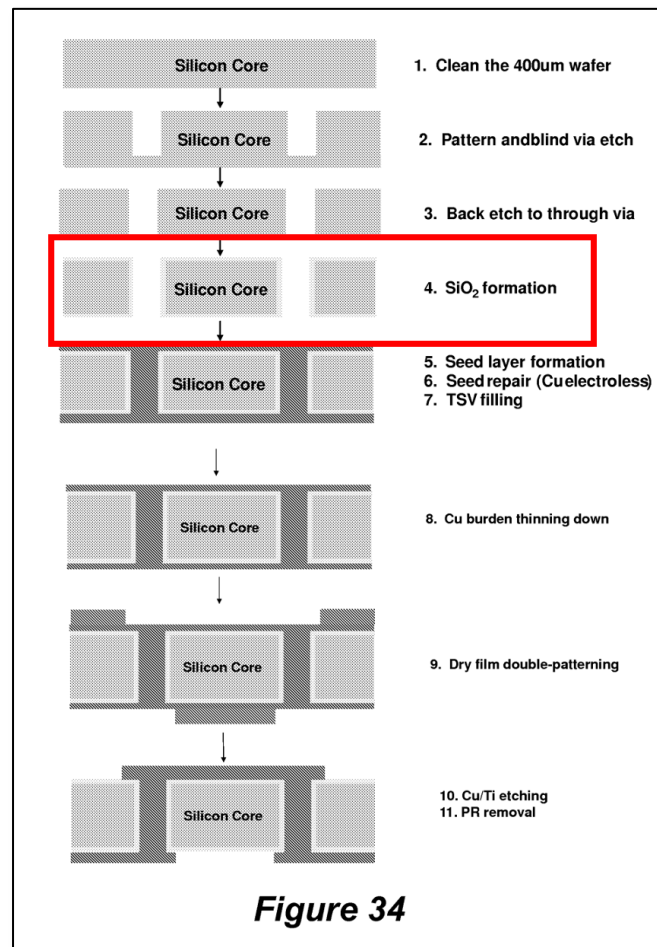
Figure 3

EX1004 at FIG. 3.

3. *1(a)(i): “wherein said solid layer comprises a compound of silicon and oxygen,”*

128. Sundaram’s interposer 105 comprises “glass,” such as “borosilicate glass” which is *a compound of silicon and oxygen*. *EX1004* at 5:54-58, 9:14-16; *EX1033* at 3:23-24 (“a borosilicate glass (**SiO₂**-B₂O₃).”); *EX1034* at 2:52-53 (“...the borosilicate glass powder contains **SiO₂**, B₂O₃, and K₂O[.]”).

129. Alternatively, Sundaram teaches an interposer 105 comprises a “silicon core” with an “**SiO₂** dielectric isolation layer” as shown below in FIG. 34. *EX1004* at 5:54-58, 14:58-62.



EX1004 at FIG. 34.

4. **1(a)(ii): “wherein said solid layer has a thickness between 50 and 150 micrometers,”**

130. Sundaram’s interposer (*solid layer*) is “about 20 to about 200 micrometers in thickness” or “about 20-100 micrometers.” EX1004 at 2:22-25, 5:50-53. Because Sundaram teaches a range that overlaps the claimed range, Sundaram at least renders obvious Claim 1(a)(ii). Specifically, the claim recites a *thickness between 50 and 150 micrometers*, which overlaps with Sundaram’s teaching of 20

to about 200 micrometers and 20-100 micrometers, namely the range of 50-150 micrometers within the 20-200 range and the range of 50-100 in the 20-100 range. Sundaram therefore expressly teaches a thickness, specifically 50-150 and 50-100 micrometers, that is within the claimed range of *between 50 and 150 micrometers* to thereby teach or render obvious Claim 1(a)(ii).

131. I also note that the '306 Patent does ascribe any criticality to the range of 50 and 150 micrometers. That is, the '306 Patent does not provide the range of 50 and 150 micrometers and then further provide an explanation for why such range is needed, important, or advantageous. Indeed, the '306 Patent describes a variety of ranges, including smaller (20 micrometers) and much larger ranges (2000 micrometers), indicating to a POSITA that the thickness can widely vary and that the thickness is not otherwise critical, further supporting the presumption of obviousness. *See EX1001* at 7:58-64.

5. 1(a)(iii): “wherein said solid layer comprises a first region and a second region between said first region and a first edge of said solid layer;”

132. As shown below, Sundaram’s *solid layer* (interposer 105) comprises a *first region* (green) and a *second region* (blue). The *second region*, as shown, is *between said first region and a first edge* (purple line) *of said solid layer*.

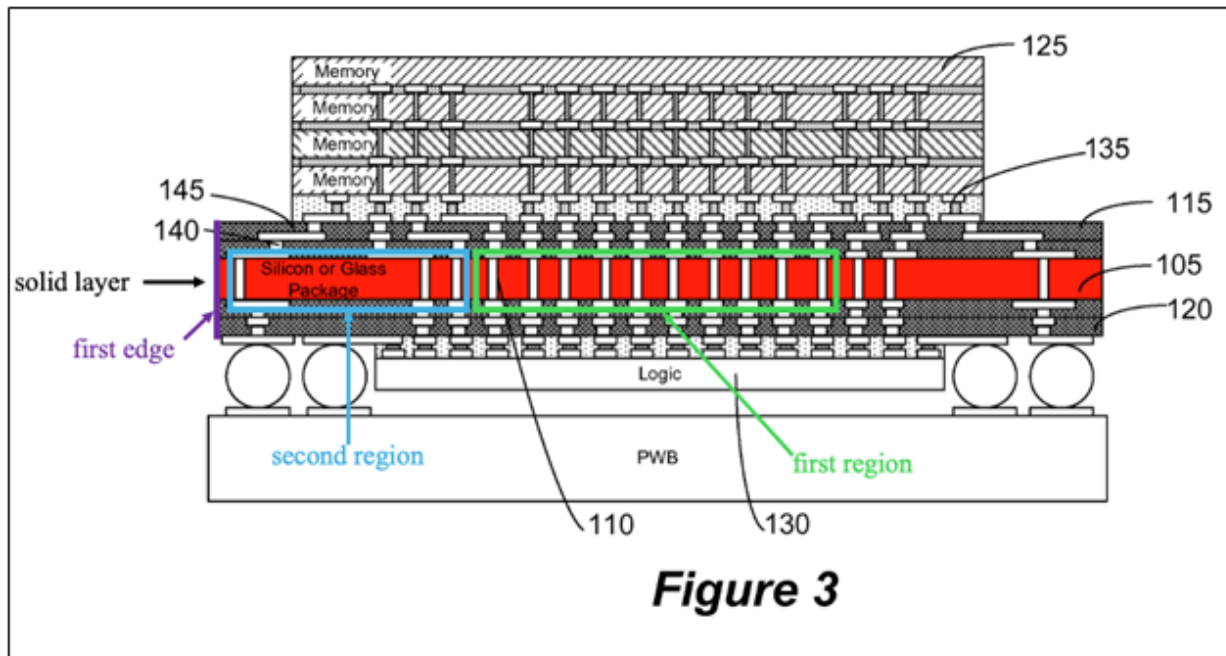


Figure 3

EX1004 at FIG. 3.

6. 1(b): “a plurality of metal posts in a plurality of through holes in said second region respectively,”

133. Sundaram teaches a “plurality of ultra-small through vias 110 can be defined within the interposer 105 such that each of the through vias 110 extends from the first side 115 to the second side 120 of the interposer 105.” EX1004 at 6:6-9. Sundaram’s through vias 110 are “metalized with a highly-conductive metal, for example copper.” EX1004 at 6:25-27. Because through vias 110 are “metalized with...copper[,]” i.e., because copper is *metal*, Sundaram’s through vias 110 are a *plurality of metal posts in a plurality of through holes*. Further, the indicated through vias 110, as depicted below, are *in said second region respectively*.

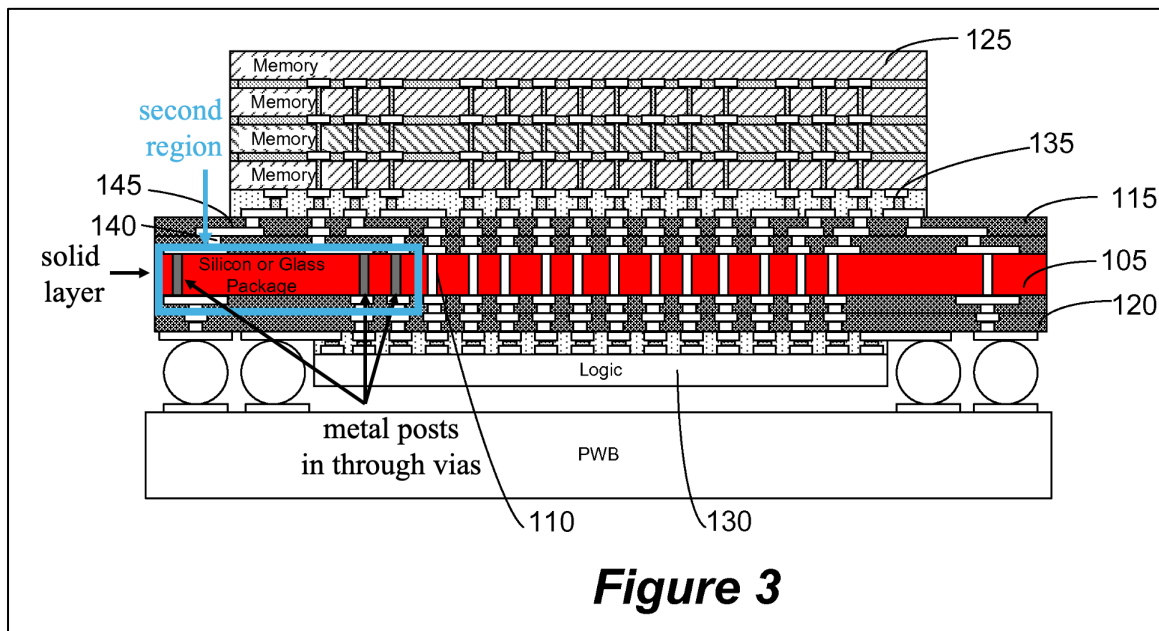


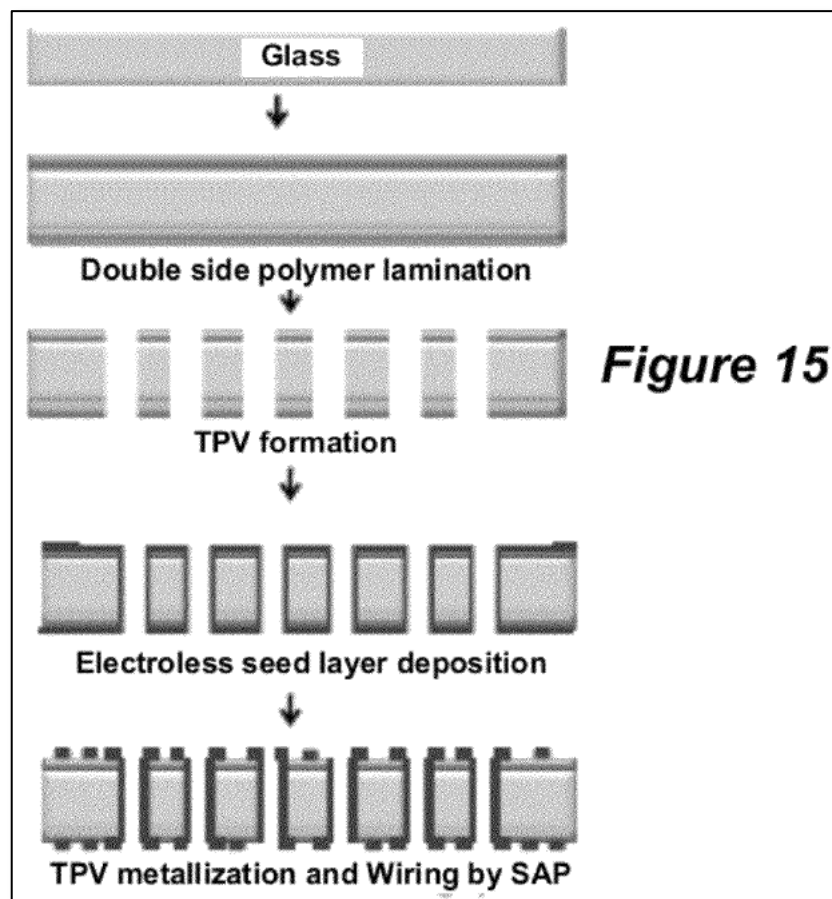
Figure 3

EX1004 at FIG. 3.

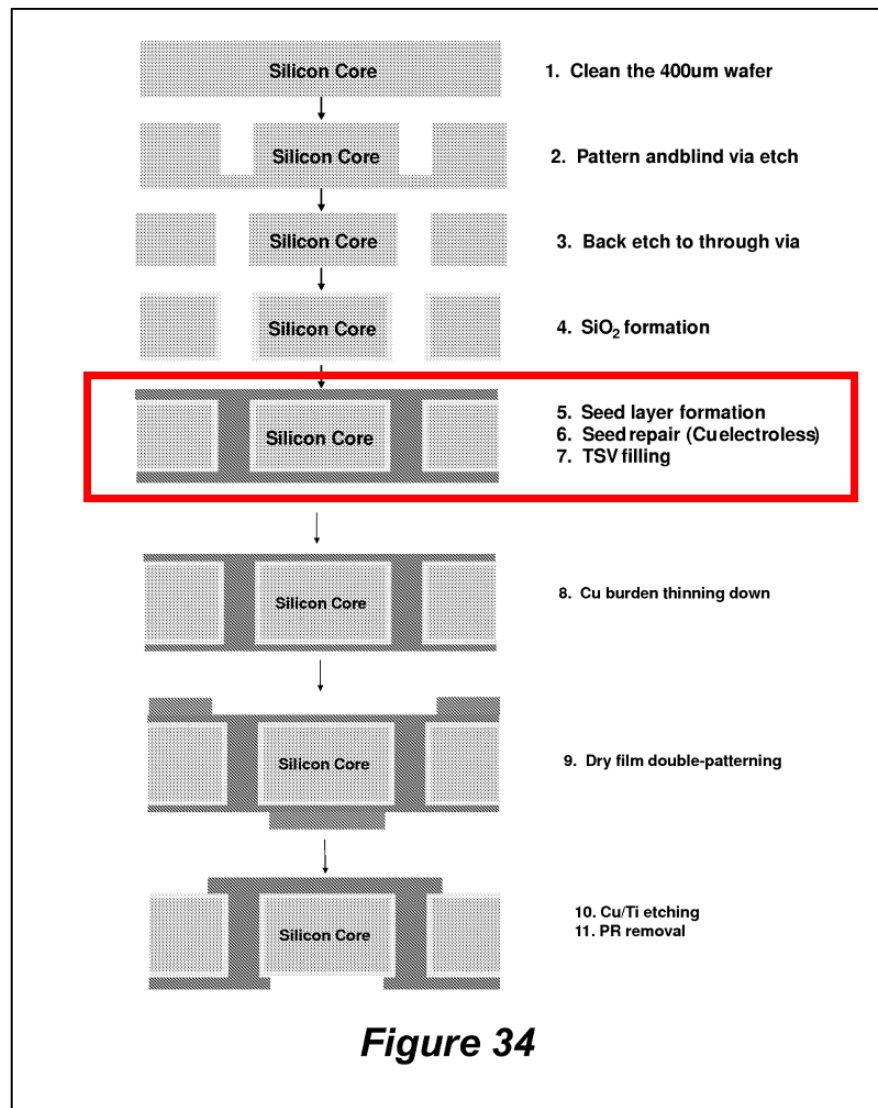
7. *1(b)(i): “wherein one of said plurality of metal posts comprises a first copper layer contacting a sidewall of one of said plurality of through holes,”*

134. Sundaram teaches the “through vias 110 can be metalized with a highly-conductive metal, for example copper.” EX1004 at 6:25-27. Because the through vias 110 are metalized with copper, through vias 110 comprise a *first copper layer contacting a sidewall* (i.e., sidewall of through via 110 provided by interposer 105) *of one of said plurality of through holes*. In other words, because through vias 110 are metalized with copper, the copper portion *contact[s] a sidewall* of through via 110, because the metallization process deposits copper onto the portion of interposer 105 providing the *sidewall*.

135. For example, as shown in FIGS. 15 and 34, a *first copper layer* is formed on the through vias, for example by “TPV metallization” in FIG. 15 and the “seed repair (Cu electroless)” and “TSV filling” in FIG. 34. *See also EX1004* at 10:26-28 (“Metallization of TPVs...was carried out using copper as metal SAP (semi additive plating) approach.”).



EX1004 at FIG. 15.

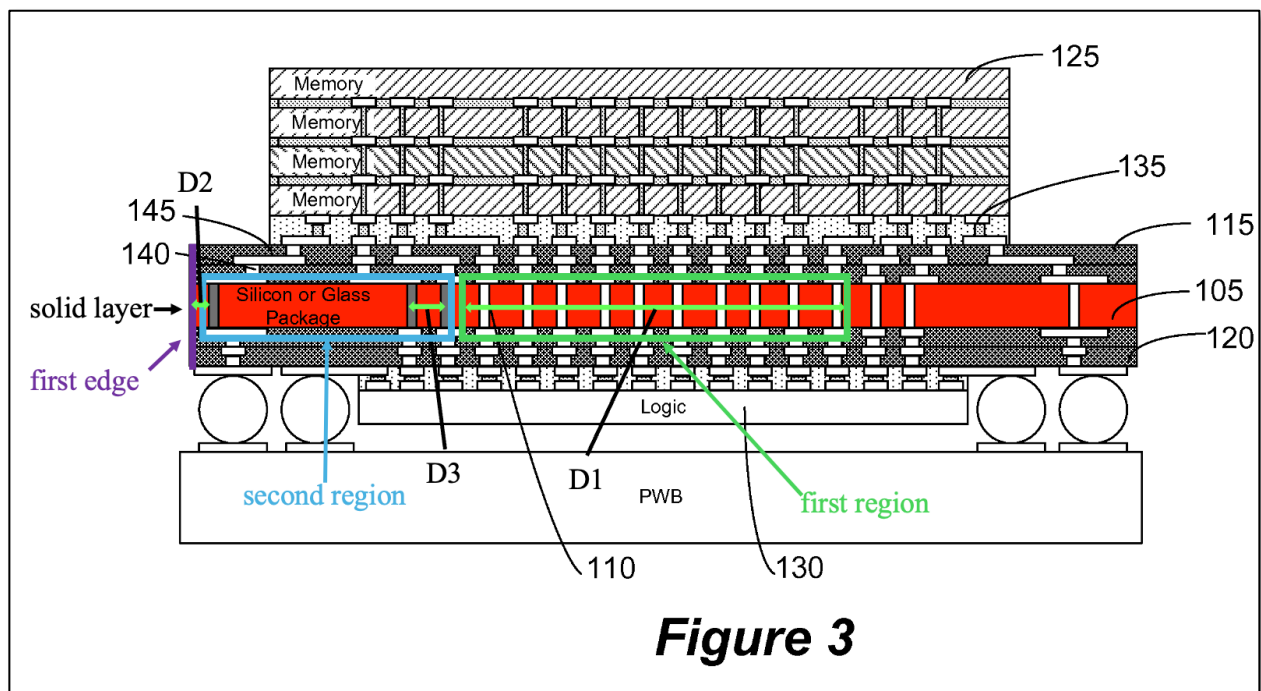


EX1004 at FIG. 34.

8. *1(b)(ii): “wherein said first region has a width in a direction greater than a shortest distance between said sidewall of one of said plurality of through holes and said first edge in said direction and greater than a pitch between two neighboring metal posts of said plurality of metal posts;”*

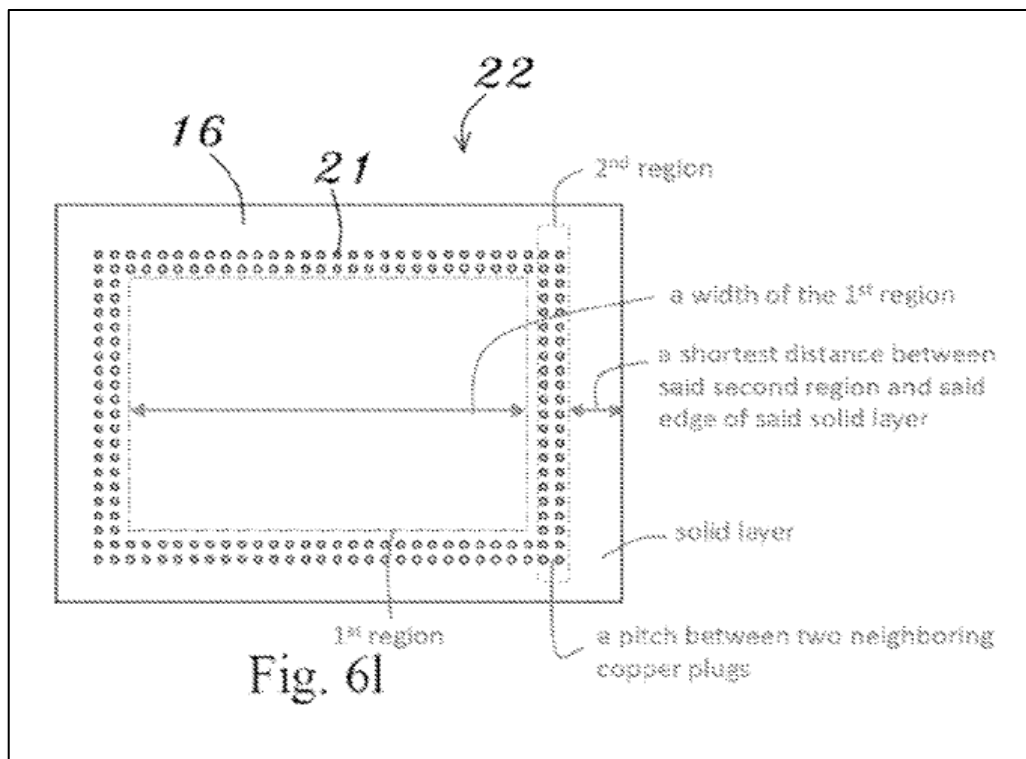
136. As shown below, Sundaram’s *first region has a width in a direction* (denoted D1). The width D1 is *greater than a shortest distance between said*

sidewall of one of said plurality of through holes and said first edge in said direction (denoted D2). As shown D1 is greater than D2. Additionally, Sundaram teaches a pitch between two neighboring metal posts of said plurality of metal posts (denoted D3). As shown, D1 is greater than D3. Thus, Sundaram teaches wherein said first region has a width in a direction greater than a shortest distance between said sidewall of one of said plurality of through holes and said first edge in said direction and greater than a pitch between two neighboring metal posts of said plurality of metal posts.



EX1004 at FIG. 3.

137. I note that the claimed *regions* are not described in the '306 Patent's written description. Applicant relied solely on applicant-annotated FIG. 6I as support during original examination of the '306 Patent's parent application (USPN 11,538,763), which Applicant argued illustrates the claimed *width*, *distance*, and *pitch*. As shown above, Sundaram's *first* and *second* regions mirror this arrangement.



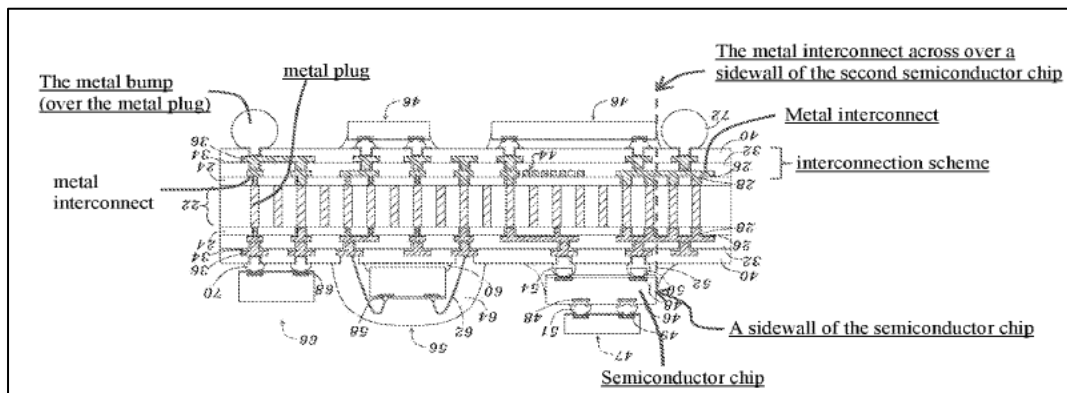
EX1117 at p. 272.

9. **1(c): “a first interconnection scheme over said first surface,”**

138. I note that various limitations of the Challenged Claims require claim elements to be *over* or *under* with respect to other claim elements. For clarity of

mapping, I annotate Sundaram's figures where appropriate indicating the *over* and *under* directions, where *over* is towards the PWB and *under* is away the PWB.

139. I note that the Patent Owner similarly used inverted figures during prosecution of related USPN 11,107,768 ("the '768 Patent") to explain the *over/under* relationship between various claim elements. For example, Patent Owner provided an annotated version of FIG. 9x inverted during prosecution as support for "a first metal bump over said first interconnection scheme and said second metal plug[.]" *EX1032* at pp. 537-538, *see also EX1032* at pp. 395-400.

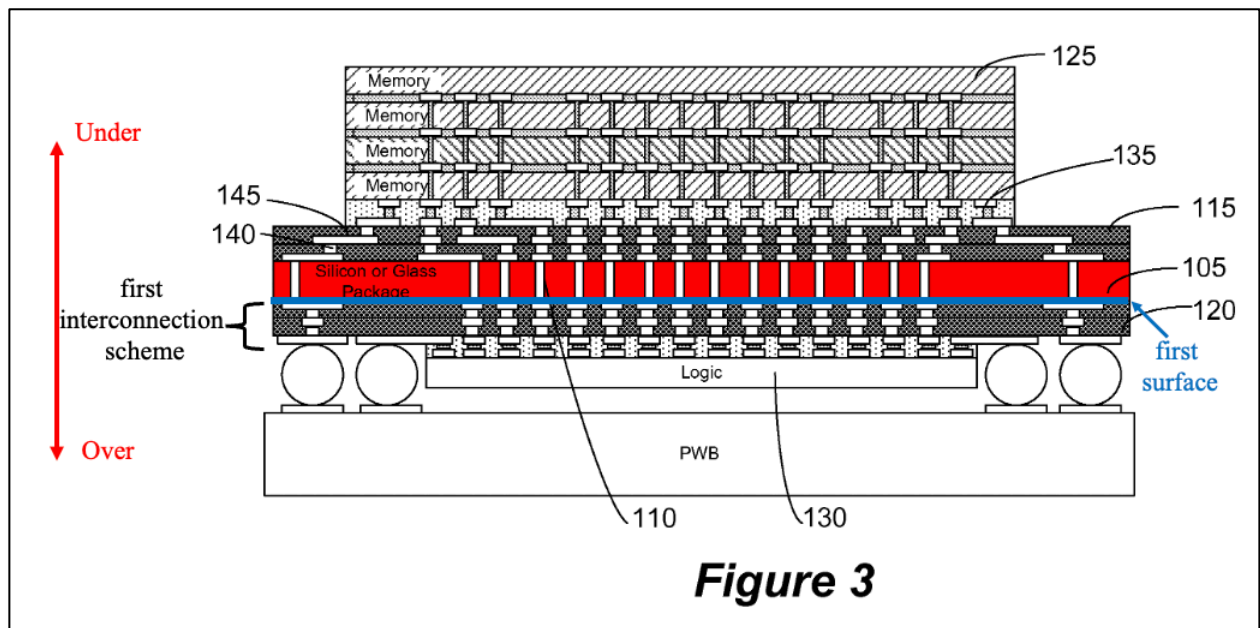




EX1001 at FIG. 9x.

140. Illustrated below, Sundaram teaches that “electronic devices having different I/O pad layouts and sizes can also be connected through the use of blind vias 140 and conductor traces 145 defined within **polymer-metal redistribution layers** deposited on the first side 115 and second side 120 of the interposer 105.” *EX1004* at 6:32-67. Additionally, Sundaram teaches “die pads 135 that are formed on the first 115 and second sides 120 of interposer 105 can electrically connect devices[.]” *EX1004* at 6:29-31. Because the blind vias 140 and conductor traces 145 within polymer-metal redistribution layers connect "electronic devices having different I/O pad layouts and sizes[.]” and because the die pads 135 formed on the second side 120 “electrically connect devices[.]” the vias 140, conductor traces 145, die pads 135, and polymer layer in the “polymer-metal redistribution layer” on

second side 120 (*first surface*) are a *first interconnection scheme* over said *first surface*. In other words, because vias 140 and traces 145 in the polymer layer and die pads 135 connect (i.e., *interconnect[]*) devices 125 and 130, they collectively form an *interconnection scheme*.



EX1004 at FIG. 3.

10. 1(c)(i): “wherein said first interconnection scheme comprises a first metal interconnect over said second surface and a polymer layer over said first metal interconnect,”

141. Because Sundaram teaches that “[m]etallization...on the surface of glass interposer” is done by “using copper as metal and SAP (semi additive plating approach)[,]” a POSITA would understand the blind vias 140 and conductive traces 145 to be the “metal” in the “polymer-metal redistribution layers[.]” EX1004 at

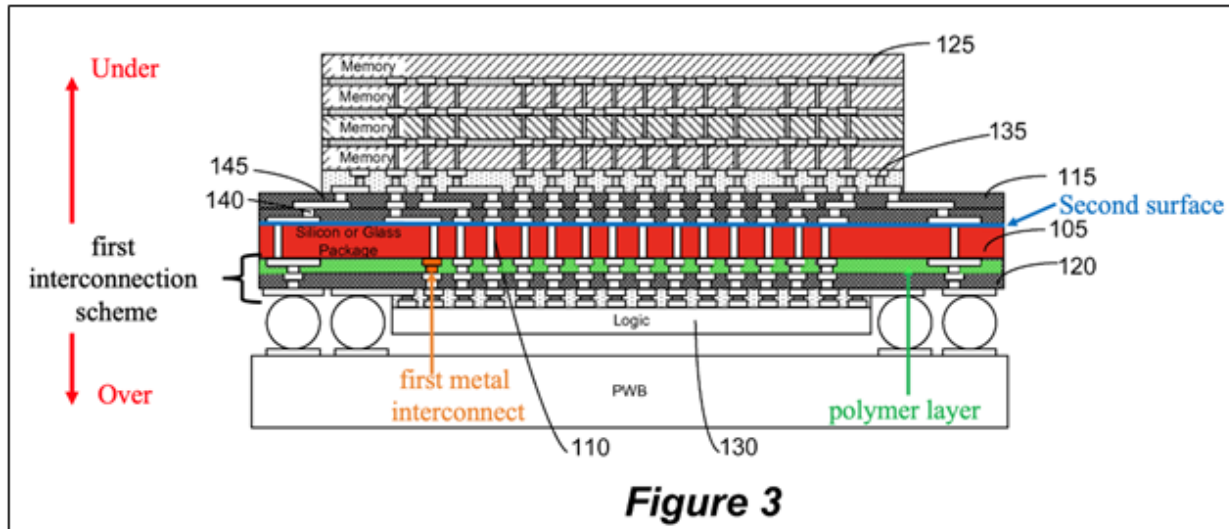
10:26-28, 9:63-65, FIG. 15, 6:62-67. Semi additive plating was a well-known technique used within a sequential build up (SBU) process flow to form circuitry in chip packages:

“Circuitry is formed in a **semi-additive** process. The entire polymer surface, both dielectric and via hole walls, is **seeded with a conductive material** in a process derived from conventional circuit board processing, and a thin layer **of electroless copper is deposited**. A photoresist layer is deposited, patterned, and etched to expose the electroless copper and via holes in the desired circuit pattern. **Electroplated copper is added to the desired finished metal thickness**. Finally, the sacrificial dielectric layer is entirely removed, initial seed metal is stripped, and the SBU substrate is ready for the addition of the next layer pair. The process is repeated for the desired number of layers.”

EX1035 at p. 643.

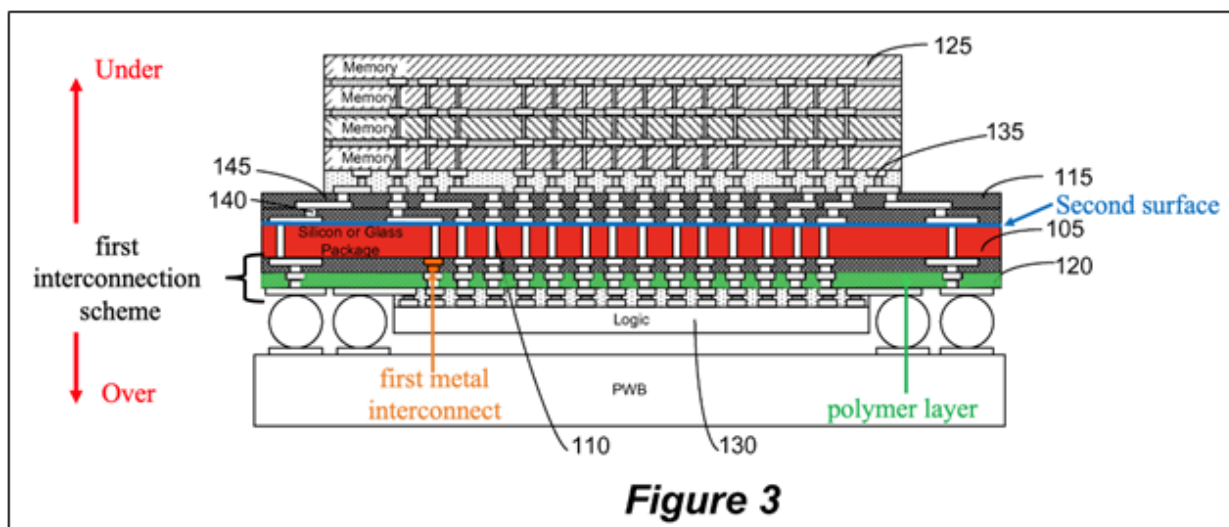
142. Thus, because the blind vias 140 and conductive traces 145 are *metal* and because they connect “electronic devices having different I/O pad layouts and sizes[,]” blind vias 140 and conductive traces 145 are *metal interconnects* of the *first interconnection scheme*. *EX1004* at 6:62-65, 7:4-8. A *first metal interconnect* comprising a trace 145 (longer rectangles in FIG. 3) and a via 140 (shorter rectangles) in Sundaram’s RDL is shown below, along with a *polymer layer* that is *over said first metal interconnect* (the “polymer” of the “polymer-metal redistribution layers.”). *EX1004*, 6:62-67. The *polymer layer* at least includes the

below green highlighted layer but may include an additional portion of the RDL (*see* Claim 14, ¶ 221).



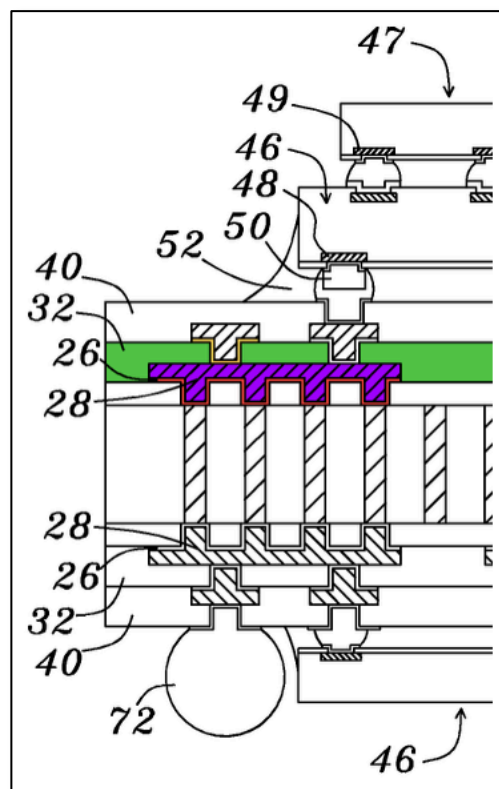
EX1004 at FIG. 3.

143. Alternatively, Sundaram's outermost layer of the RDL is *a polymer layer* and is *over the first metal interconnect*.



EX1004 at FIG. 3.

144. I note that Sundaram's teaching of the polymer as being over each of the first, second, and third metal interconnect[s] is consistent with what is described by the related '768 Patent. Specifically, during prosecution of the '768 Patent, Patent Owner expressly pointed to dielectric layer 72 as being the second polymer layer. *EX1032* at 397.



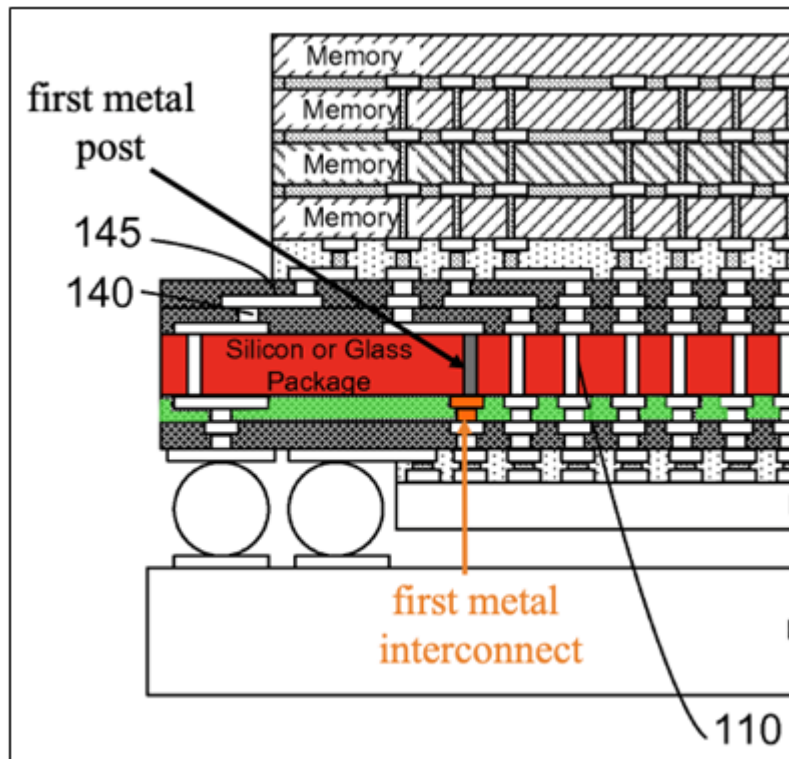
EX1001 at FIG. 9X (excerpt).

145. As can be seen in the above figure, dielectric layer 32 (the second polymer layer, according to the Patent Owner) is “over” metal layers 26, 28 and partially over metal layer 34, of the metal interconnect. As such, Sundaram's second

polymer layer is over each of the first, second, and third metal interconnect[s] in at least the same way as described by the '768 Patent.

11. 1(c)(ii): “wherein said first metal interconnect is connected to a first metal post of said plurality of metal posts,”

146. Sundaram teaches the “first electronic device 125 is of a different pad size and configuration than the second electronic device 130, and they are connected with through vias 110, blind vias 140, and conductor traces 145.” *EX1004* at 7:4-8. Because devices 125, 130 are connected by blind vias 140, traces 145, and through vias 110, the traces 145 and vias 140 on either side of interposer 105 are connected by vias 110. Thus, as shown below, the *first metal interconnect is connected to a first metal post of said plurality of metal posts*.



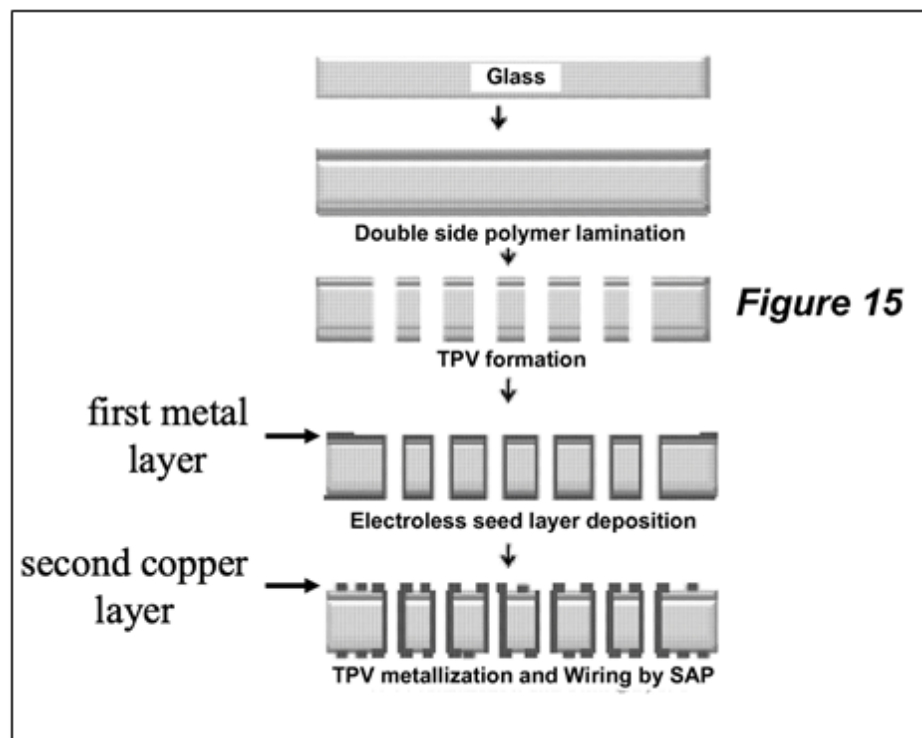
EX1004 at FIG. 3.

12. 1(c)(iii): “wherein said first metal interconnect comprises a first metal layer and a second copper layer² over said first metal layer;”

147. As I described above, the blind vias 140 and conductor traces 145 are the “metal” in the “polymer-metal redistribution layers.” See ¶¶ 141-142. Additionally, as shown in FIG. 15, Sundaram expressly teaches a *first metal layer* formed by “direct metallization using wet electroless copper deposition” and a

² The “first” copper layer is recited in 1(b)(i).

second copper layer over said first metal layer formed by “semi-additive plating” using “copper as metal.” *EX1004* at 9:61-65, 10:26-28. The *first metal layer* is provided by the electroless copper seed layer that is shown on the top of glass interposer in FIG. 15 and the *second copper layer* is shown as the SAP wiring on top of the copper seed layer. Further, because Sundaram teaches that “[m]etallization...on the surface of glass interposer” i.e., glass interposer 105 is carried out using SAP, a POSITA would understand that the *first metal interconnect* as mapped above at claim 1(c)(i) is formed using the method of FIG. 15 i.e., using copper as the metal, thus forming a *first metal layer* and a *second copper layer over said first metal layer*. See ¶¶ 141-142.

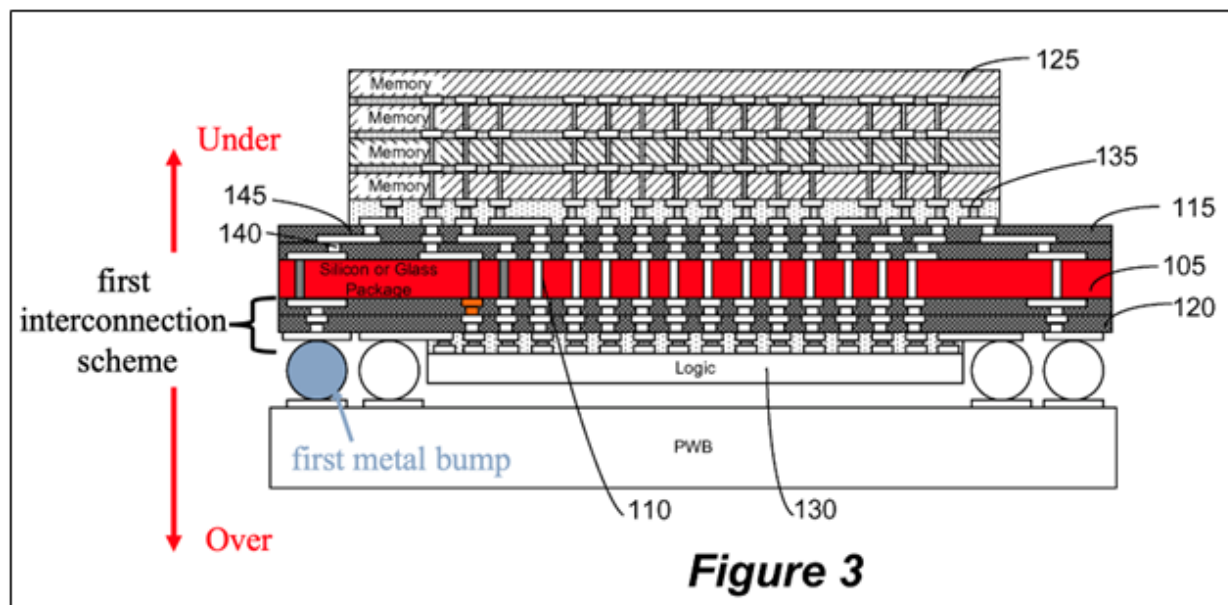


EX1004 at FIG. 15.

148. To the extent it is argued FIGS. 3 and 15 are separate embodiments, a POSITA would have been motivated and found it obvious to modify Sundaram's vias 110 in FIG. 3 per FIG. 15's SAP teachings. As discussed, Sundaram teaches interposer 105 in which vias 110 are formed is glass. Because glass is an insulator, a POSITA would have in fact understood it to be necessary to use a seed layer in order to grow the second copper layer via electroplating, as an electrode is needed for uniform formation of an electroplated copper layer. *EX1104* at 2:46-48 ("The copper seed layer provides an electrode for the subsequent copper electroplating..."). Indeed, it was known that a "missing seed layer" may "lead to a void in the electroplated metal" resulting in an "increase in their resistance and result in poor reliability." *EX1063* at 3:12-16. Thus, there would have been ample motivation to modify FIG. 3 per FIG. 15's teachings. Furthermore, a POSITA would have had a reasonable expectation of success because both FIG. 15 and FIG. 3 have the same substrate material, i.e., glass and because the use of metallic seed layers for plating metal interconnects was commonplace. *EX1004* at 10:9-15, 8:1, 5:54-59; *see, e.g., EX1005* at [0057], [0060].

13. 1(d): "a first metal bump over said first interconnection scheme,"

149. Sundaram teaches that “die pads 135 formed on the first 115 and second sides 120 of the interposer 105 can electrically connect devices using...**copper bumps** with solder caps[.]” *EX1004* at 6:29-31. An example of one of Sundaram’s copper bumps with solder caps is shown below, which is a *first metal bump* (i.e., because it’s made of copper) *over said first interconnection scheme*.



EX1004 at FIG. 3.

14. 1(d)(i): “wherein said first metal bump comprises a second metal layer and a first tin-containing layer over said second metal layer; and”

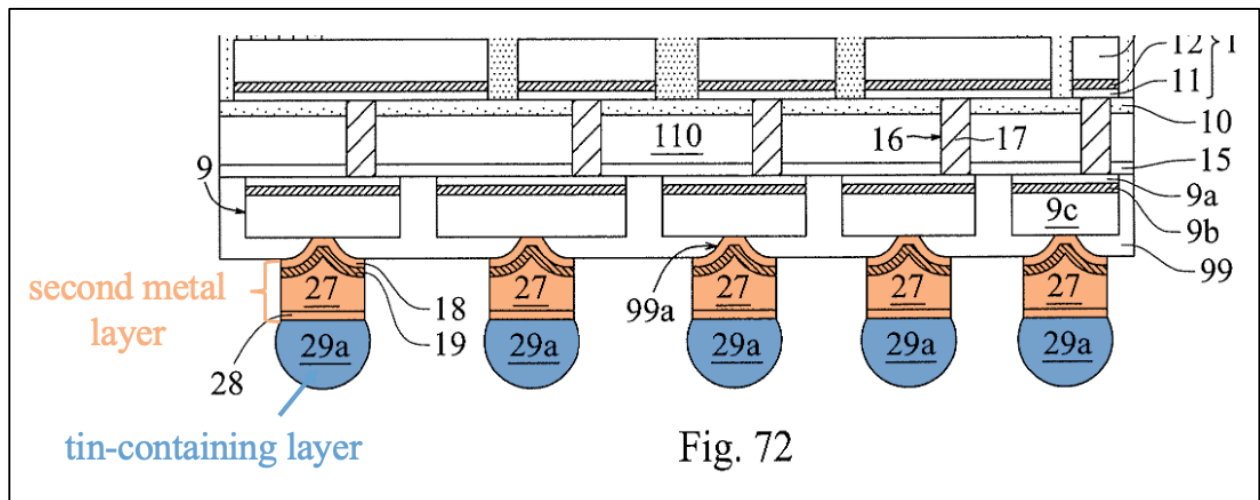
a) Sundaram’s Teachings

150. As discussed above, Sundaram’s *first metal bump* is a “copper bump[s] with [] solder cap[.]” See ¶ 149; *EX1004* at 6:29-31. Thus, Sundaram’s *first metal bump* comprises a second metal layer (the copper bump). A POSITA would have

further understood the “solder cap” to be a *tin-containing layer* because “traditional solders are ...most commonly a **tin**-lead alloy (Sn-37% Pb) having about 37% lead in a **tin** base material.” *EX1094* at [0003]. Additionally, Sn-based solders were dominant in commercial packages such as those taught by Sundaram. Thus, the context of the chip packages of Sundaram means that “solder” necessarily includes Sn-content, thereby teaching the *first tin-containing layer*. A POSITA would have understood Sundaram’s disclosure of “solder” to mean the solder contains tin unless stated otherwise. That is, if someone refers to non-tin-containing solder, it would be specified as such because the “default” solder contains tin.

b) Lin-191’s Teachings

151. Additionally or alternatively to Sundaram’s teachings, Lin-191 teaches a *bump* with the claimed layers. Specifically, Lin-191 teaches a system-in-package including “solder bumps or balls 29a” formed by reflowing a “solder layer 29,” which is “**a tin-containing layer**” formed “on the metal layer 28.” *EX1005* at [0320]. Layer 28, along with “adhesion layer 18, the seed layer 19, and metal layer[] 27...compose an under bump metallurgic (UBM) layer.” *EX1005* at [0323]. Layers 18, 19 are metal. *EX1005* at [0308]. The UBM layer is, collectively, a *second metal layer* and layer 29 is the *first tin-containing layer*.



EX1005 at FIG. 72.

152. Thus, Lin-191 teaches a metal bump compris[ing] a *second metal layer* (UBM) and a *tin-containing layer* (solder layer 29) over said *second metal layer*.

c) Motivation to Combine

153. A POSITA would have been motivated and found it obvious to apply Lin-191's teachings of a metal bump having a *tin-containing layer* over a *second metal layer* to Sundaram's *first metal bump*. As discussed, Sundaram teaches traditional solder that a POSITA would have understood to contain tin and Lin-191 further discloses a solder layer that is a *tin-containing layer*, further motivating the combination. A POSITA would have appreciated the advantage of a tin-containing layer, as tin was known to "wet and spread on a wide range of substrates[,]” which a POSITA would have considered desirable as wettability was an important factor for forming various types of interconnects. EX1098 at p. 104. Additionally, tin used

in limited thickness was known to form IMCs with metals used in electronic assemblies, thereby achieving “good bonding.” *EX1099* at p. 20. Tin-containing solder was further known to be advantageous due to tin’s “relatively low melting point” which would allow for solder reflow to occur without damaging other components of the chip package unable to withstand high temperatures. *EX1134* at [0026]. Further, “[a]nother advantage is the existence of substantial experience and database in the use of tin solders compiled over a long history.” *EX1099* at p. 20. Thus, Lin-191’s solder bump or ball 29a having a *tin-containing layer* would have predictably improved the mechanical connection of Sundaram’s *first metal bump* to die pad 135 by achieving “good bonding[,]” would have provided the benefit of a low melting point, and would have been a straightforward material choice given the substantial amount of data generated by extensive use. *EX1099* at p. 20.

154. Further, a POSITA would have been motivated to implement Lin-191’s UBM layers (*second metal layer*) as UBM layers were known to “improve the adhesive strength of solder balls” and to “prevent[] diffusion of unnecessary substances” of solder balls into nearby substrates. *EX1037* at 5:3-5. For example, Lin-191’s UBM structure includes an adhesion layer 18 that may be “chromium” or a “titanium-tungsten alloy[,]” which were known materials for use in UBM

structures that “improve the adhesion and reliability of solder bumps.” *EXI038* at 2:24-29; *EXI005* at [0308], [0311].

155. Further, regarding the copper layer 27 in Lin-191’s UBM structure, copper was known to have “good conductivity and good ductility” which provides “improved thermal performance by counteracting thermal stress[,]” thus further motivating the combination. *EXI039* at 13:38-41. Metal layer 28 which may be made of “nickel” would allow a POSITA to leverage the aforementioned advantage of copper layer 27, while minimizing the risk of copper diffusion into the solder balls. Indeed, nickel was known to prevent copper diffusion into adjacent structures. *EXI040* at Abstract (“The structure comprises a layer of barrier metal, preferably nickel, that resists copper diffusion.”). A POSITA would have been familiar with the issue of copper diffusing into adjacent structures, such as solder balls. Indeed, it was known that “when used with Sn solder material, sufficient Cu diffusion from Cu pillar bump into the solder forms thick IMC [(Inter Metallic Compound)] such as Cu_6Sn_5 and Cu_3Sn through the reaction between the diffused Cu and Sn in the solder. Thick IMC layers reduce mechanical strength of the Cu pillar bump because the IMC layers are brittle.” *EXI041* at [0005]. Further, “IMC formation will cause bump crack or unwanted stress” and “the thicker IMC also results in poor adhesion.” *EXI041* at [0005]. As such, a POSITA would have wanted to prevent such loss of

mechanical strength that leads to joint failure (i.e., by cracking or unwanted stress) and been motivated to include nickel layer 28 to prevent copper diffusion contributing to such issues.

156. The Sundaram-Lin-191 combination is merely the application of a known technique (Lin-191's solder bump structure) to a known device (Sundaram's bump) ready for improvement to yield the predictable result of Sundaram's *first metal bump* being formed with Lin-191's solder bump structure including *a first tin-containing layer over [a] second metal layer*.

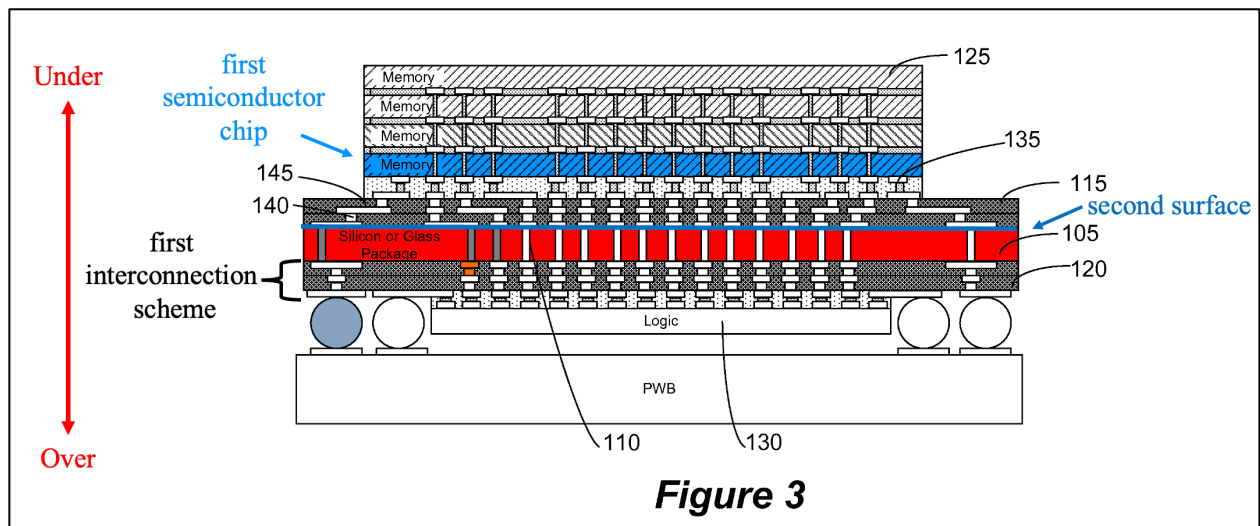
157. Alternatively, the Sundaram-Lin-191 combination is the simple substitution of Lin-191's solder bump structure, including the *tin-containing layer over said second metal layer*, for Sundaram's *first metal bump*. The substitution would have yielded predictable results at least because Lin-191's solder ball structure (i.e., solder ball 29a and UBM layers) and Sundaram's metal bump both serve the same function i.e., connecting interconnects to a PWB/PCB. *EX1005* at [0324]; *EX1004* at FIG. 3. Additionally, Lin-191 teaches forming the solder bump structure using well-known manufacturing techniques, such as electroplating. *EX1005* at [0320-0324].

158. A POSITA would have had a reasonable expectation of success in either applying Lin-191's teachings to Sundaram's *first metal bump* or substituting

Sundaram's *first metal bump* with Lin-191's structure at least because such a modification/substitution would have involved the application of well-known manufacturing techniques well within the skill of a POSITA. For example, sputtering, electroplating, and reflowing, taught by Lin-191 to form solder ball 29a and UBM layers were well-known techniques that a POSITA would have been familiar with. *See, e.g., EX1005* at [0309]-[0320], [0323]; *EX1042* at ("...filled with copper typically by an electroplating process, as known to one of ordinary skill in the art of integrated circuit fabrication."); *EX1043* at [0032] ("The metal-containing wetting film 104 may be deposited by a variety of different deposition methods known by one of ordinary skill in the art, including but not limited to, CVD, pulsed CVD, PECVD, ALD, PEALD, or sputtering methods."); ¶¶ 71-75. Because Sundaram and Lin-191's solder ball structures perform similar functions and because standard techniques were used to form Lin-191's solder ball and UBM layers, a POSITA would have had a reasonable expectation of success. Moreover, metal bump technology, including layered bump structures, were commonplace prior to the '306 Patent, thereby further contributing to a reasonable expectation of success. *See* ¶¶ 67-69.

15. 1(e): "a first semiconductor chip under said second surface,"

159. Sundaram's first electronic device 125 "can be...stacked memory IC devices" such that a memory chip of the stack is a *first semiconductor chip under said second surface*. EX1004 at 6:34-46. As shown, Sundaram's first electronic device 125 is a *first semiconductor chip under said first interconnection scheme*.



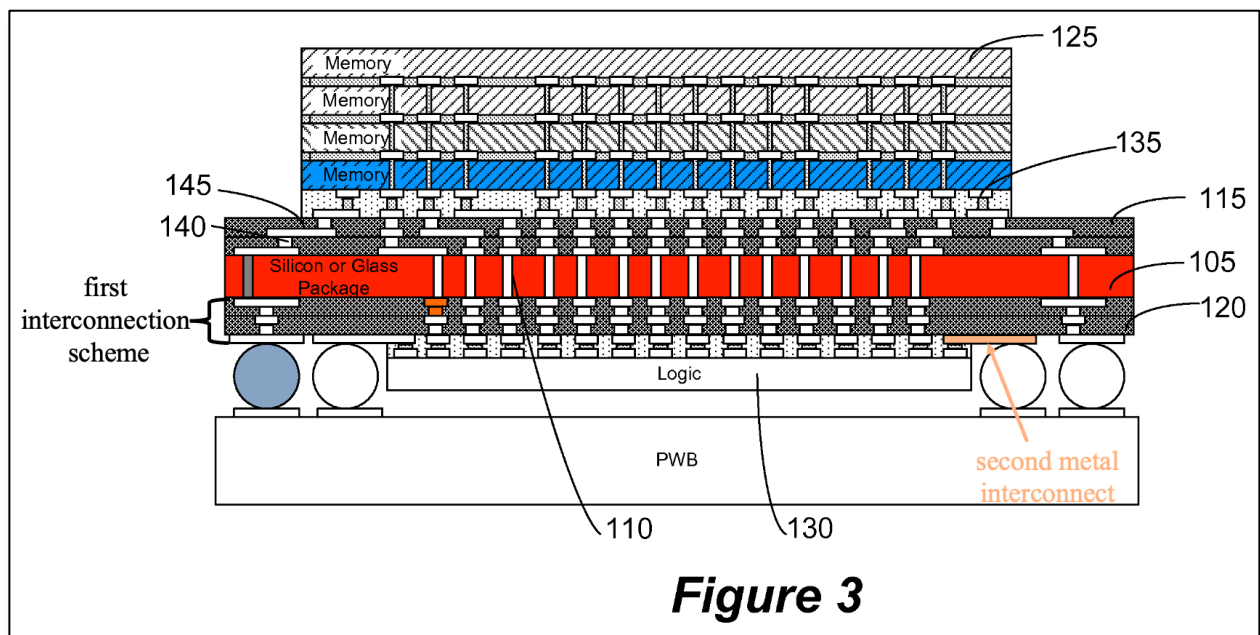
EX1004 at FIG. 3.

16. 1(e)(i): “wherein said first interconnection scheme comprise a second metal interconnect across over a sidewall of the first semiconductor chip,”

a) “Second Metal Interconnect”

160. As I discussed, Sundaram's *first interconnection scheme* comprises die pads 135 that “electrically connect devices” thus functioning as an *interconnect*. See ¶ 138. Sundaram additionally teaches “metallization provides die pad surfaces 135” such that the die pads 135 are *metal*. EX1004 at 6:22-24. FIG. 3 illustrates numerous die pad surfaces. An example one of the many die pad surfaces is identified with

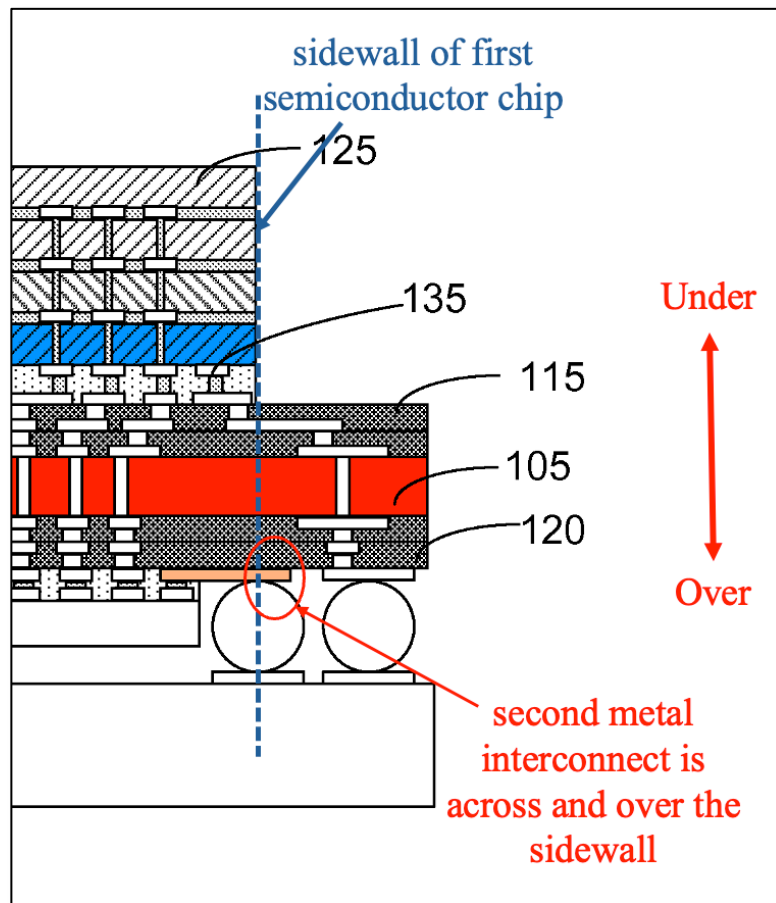
reference numeral 135 in FIG. 3. *EX1004* at 6:22-33 (referencing die pads (plural)). However, a POSITA would have understood that FIG. 3 expressly teaches a die pad surface such as the orange-highlighted die pad in the below FIG. 3 at least because of the ubiquity of connecting bumps to pads and because Sundaram labels a similar structure as such. *See* ¶ 65. Sundaram's die pad 135 shown in orange below is therefore a *second metal interconnect* that, like the trace 145 and via 140 making up the *first metal interconnect*, "electrically connect[s]" first and second devices 125, 130. *EX1004* at FIG. 3, 6:29-33; 6:62-67.



EX1004 at FIG. 3.

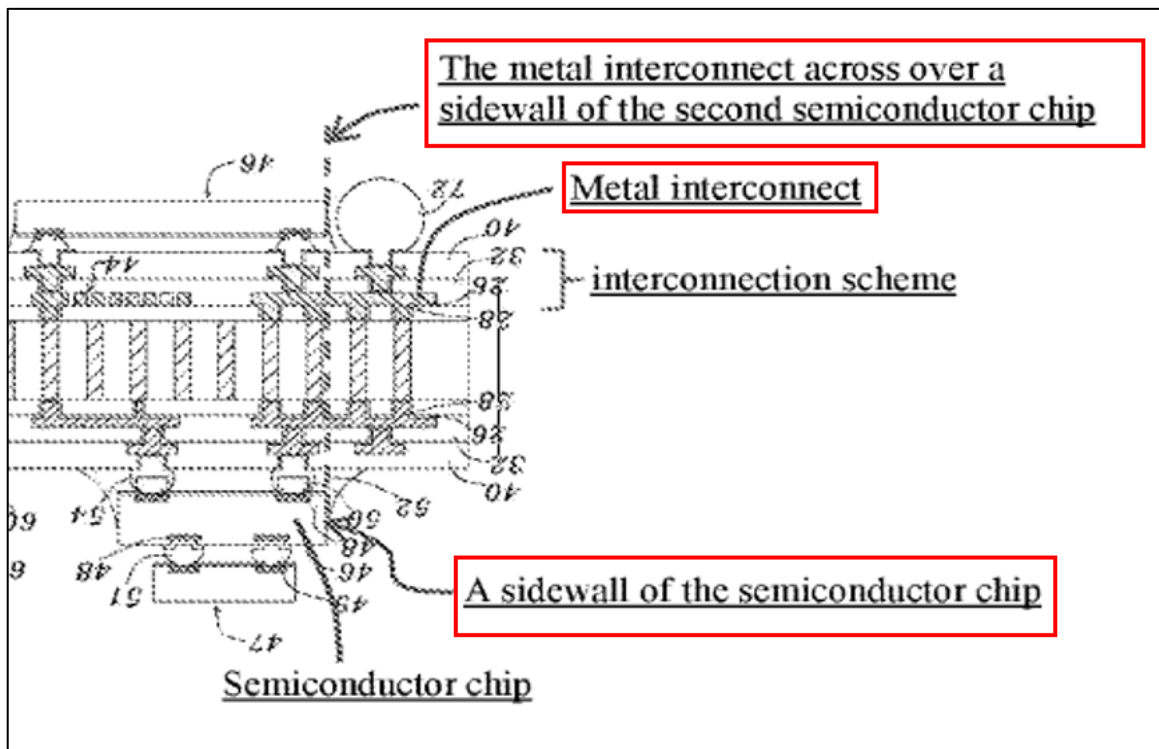
b) “Across Over a Sidewall”

161. The annotated figure below illustrates that the *second metal interconnect* is both *across* and *over* a *sidewall* of first electronic device 125 (*first semiconductor chip*). The blue dashed line indicates the *sidewall* of first electronic device 125, namely a boundary thereof. Notably, the *second metal interconnect* is positioned in the “over” direction relative to the *sidewall*, as indicated by the red arrow depicting the over/under directions. Additionally, the *second metal interconnect* extends laterally (i.e., left/right) to the right past the boundary of the *sidewall*. As such, the *second metal interconnect* is both *across* and *over a sidewall of the first semiconductor chip*.



EX1004 at FIG. 3 (excerpt).

162. I note that Sundaram's teachings of the *second metal interconnect* being *across and over the sidewall of the first semiconductor chip* are consistent with an annotated figure that Patent Owner provided during prosecution of the related '768 Patent, illustrating support for this specification. In the figure below, I have shown how the Patent Owner's annotations mirror the above mapping of Sundaram's *second metal interconnect*.

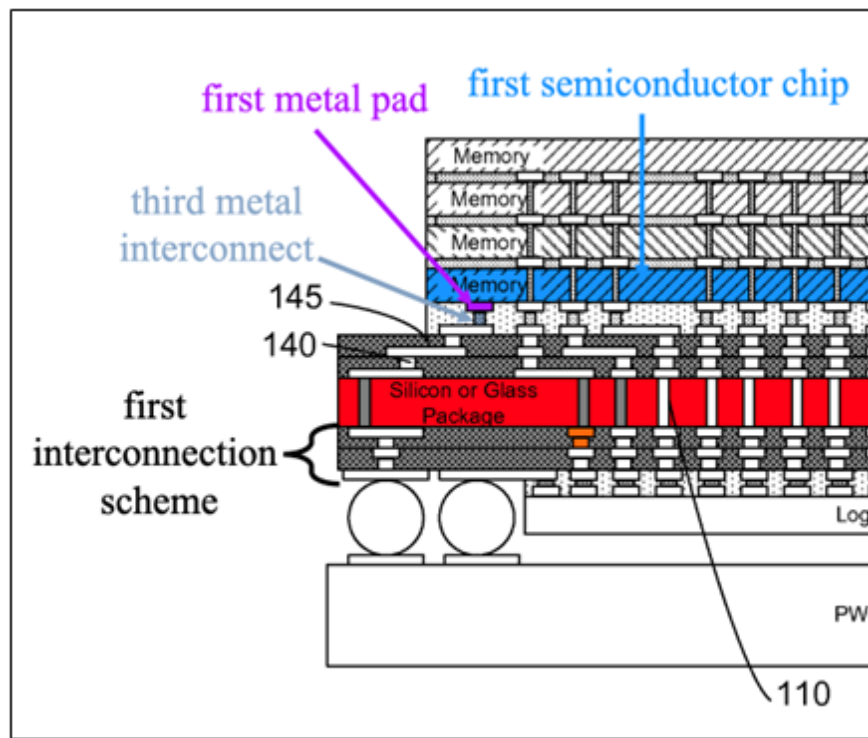


EX1032 at p. 537.

17. 1(e)(ii): “wherein said first semiconductor chip comprises a third metal interconnect on a first metal pad of said first semiconductor chip,”

163. Sundaram’s device 125 has die pads 135 where “metallization provides die pad surfaces 135[.]” EX1004 at 6:23-25. A POSITA would understand that like interposer 105, first electronic device 125 (*first semiconductor chip*) also has die *pad[s]* (one shown in purple below) such that an electrical connection is made between first electronic device 125 and interposer 105. Indeed, it was known that “I/O terminals were traditionally formed by way of metal pads along the periphery of an IC.” EX1095 at 1:24-25. Thus, a POSITA would understand the *pad* (purple)

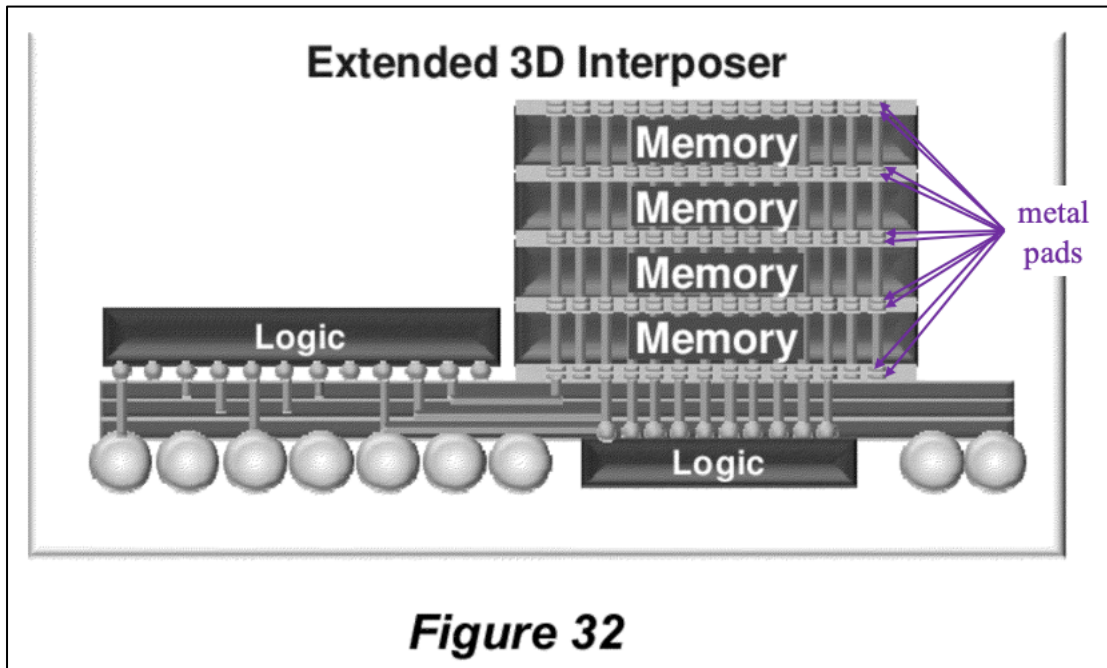
shown in FIG. 3 to be a *first metal pad*. Further, Sundaram teaches “die pads 135...can electrically connect devices using solder, copper bumps with solder caps, copper to copper bonding,” each of which teaches a *third metal interconnect* because they “electrically connect devices” and because they are made of *metal* i.e., solder, copper. *EX1004* at 6:29-33. In FIG. 3, below, the *third metal interconnect* is depicted as a bump on die pad 135.



EX1004 at FIG. 3.

164. Sundaram further depicts such *metal pad[s]* in FIG. 32, which shows a “side-by-side configuration” of the interconnect structure wherein each chip in the

memory chip stack comprises a metal pad on both top and bottom. *EX1004* at 4:26-27, 7:56-59.

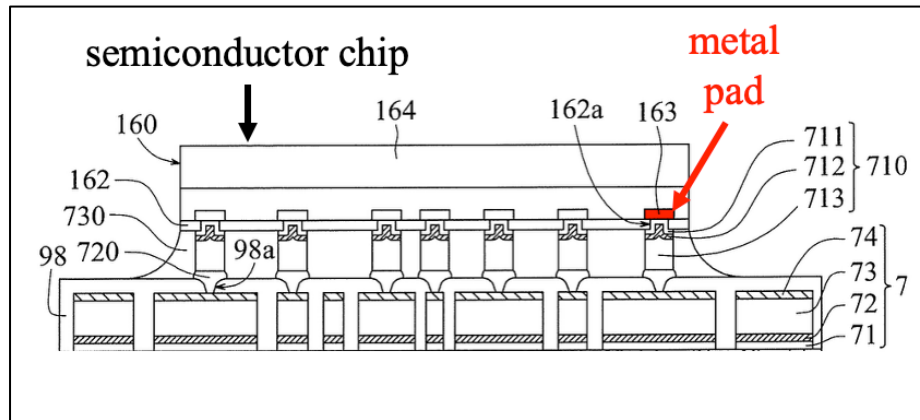


EX1004 at FIG. 32. The below MTC and reasonable expectation of success for modifying Sundaram’s chip to have a *metal pad* are incorporated herein. See ¶¶ 166-167.

a) Lin-191’s Metal Pad Teachings

165. Additionally or alternatively to Sundaram’s teachings, Lin-191 teaches a *metal pad*. Depicted below, Lin-191 teaches a “semiconductor chip 160” comprising “multiple metal traces or pads 163.” *EX1005* at [0383]. Lin-191’s “metal traces or pads 163” are made of “aluminum” and are connected to “metal pillars or

bumps 710[.]” *EX1005* at [0384]. Lin-191’s semiconductor chip 160 thus comprises a *metal pad*.



EX1005 at FIG. 71.

b) Motivation to Combine

166. A POSITA would have been motivated and found it obvious to apply Lin-191’s teachings of a *metal pad* to Sundaram’s *first semiconductor chip*, thereby yielding the predictable result of Sundaram’s *first semiconductor chip* (first electronic device 125) having a *metal pad*. Modifying Sundaram’s pad to be metal, thereby yielding a *first metal pad*, is merely an implementation detail in Sundaram’s overall system, i.e., Lin-191 provides the specificity of a semiconductor contact pad being *metal*. Given that metal contact pads were ubiquitous in semiconductor chips, a POSITA would have been motivated to turn to references teaching materials for contact pads (e.g., Lin-191) to ensure an electrical connection is made between Sundaram’s first electronic device 125 and the bump (i.e., by a conductive *metal*

pad). See, e.g., *EX1044* at 2:30-33 (“In FIG. 1, a **metal pad** 12 is formed on a semiconductor material 10. Metal pad 12 may be formed from a conductive metal...”)(emphasis added); *EX1045* at [0006] (“FIG. 1 illustrates a portion of flip chip 10 with a solder bump 12 formed on **metal contact pad** 14.”)(emphasis added); *EX1046* at [0018] (“Bumps 105 electrically and possibly physically contact the I/O pads (**metal pads**) 103 of the IC chip 100.”); *EX1095* at (“I/O terminals were **traditionally** formed by way of **metal pads** along the periphery of an IC.”).

167. The combination is application of a known technique (metal pads) to a known device (Sundaram’s semiconductor chip) ready for improvement to yield the predictable result of Sundaram’s first electronic device 125 having a *first metal pad*, per Lin-191. *EX1005* at [0081]. As I described above, metal contact pads were ubiquitous, so a POSITA would have had a reasonable expectation of success in modifying Sundaram’s first electronic device 125 to have *first metal pad*, such as aluminum, per Lin-191. See ¶ 166.

18. *1(e)(iii): “wherein said third metal interconnect comprises a third metal layer on said first metal pad and a third copper layer over said third metal layer, wherein said third copper layer has a thickness between 5 and 30 micrometers,”*

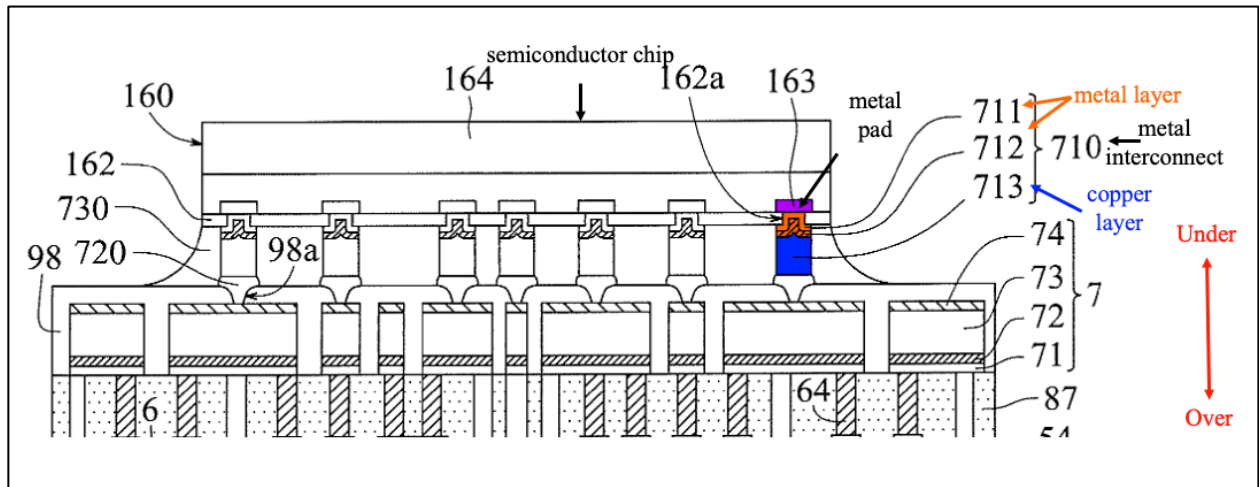
a) **Lin-191’s Teachings**

168. Lin-191 teaches “metal pillars or bumps 710” on “metal traces or pads 163” of a semiconductor chip 160, that connect chip 160 to various other structures

in Lin-191's multi-chip module, thus functioning as a *metal interconnect*. *EX1005* at [0408]. Lin-191's metal pillars or bumps 710 comprise an "adhesion layer 711[,]" a "seed layer 712[,]" and a "metal layer 713[.]" *EX1005* at [0389]. Adhesion layer 711 is formed on a "contact point" of "the metal traces or pads 163[.]" *EX1005* at [0389]. Adhesion layer 711 is "nickel" or "titanium[.]" *EX1005* at [0390], [0394]. Seed layer 712 "can be a copper layer." *EX1005* at [0392]. Thus, the combination of layers 711 and 712 is a *second metal layer on metal pad 163*. That is, because layer 711 is formed on a "contact point" of "metal traces or pads 136" and because both of layers 711 and 712 are *metal*, the mapped combination of layers 711/712 is a *second metal layer on said first metal pad*. *EX1005* at [0389]. The "metal layer 713 can be a single layer of copper" having a thickness "between 2 and 30 micrometers." *EX1005* at [0396]. Lin-191 thus teaches or renders obvious a *third copper layer ha[ving] a thickness between 50 and 30 micrometers*.

169. I note that the '306 Patent does not ascribe any criticality to the range of 5 and 30 micrometers. That is, the '306 Patent does not provide the range of 5 and 30 micrometers and then further provide an explanation for why such range is needed, important, or advantageous. Indeed, the '306 Patent describes a variety of ranges, including smaller (between 2 and 5 micrometers) and larger (between 10 and

50 micrometers), indicating to a POSITA that the thickness can vary widely and that the thickness is not otherwise critical. *See EX1001* at 14:21-33.



EX1005 at FIG. 72 (excerpt).

b) Motivation to Combine

170. A POSITA would have found it obvious and been motivated to modify Sundaram's *third metal interconnect* per Lin-191's metal pillar or bump 710 (including the thickness of copper layer 713), such that the bump has a *third metal layer* on Sundaram's *first metal pad* and a *third copper layer* having a *thickness between 5 and 30 micrometers* over the *third metal layer*. Thus, the combination yields Sundaram's *third metal interconnect* having a *third metal layer over said first metal pad and a third copper layer over said third metal layer*.

171. A POSITA would have recognized Lin-191's metal pillar or bump 710 would improve metallurgical bonding and enhance stress distribution by employing

a layered structure. Specifically, it was known that multi-layer metal bumps would provide the benefit of “improvement of adhesion of the various overlying layers or the prevention of diffusion of materials between adjacent layers[,]” thereby improving metallurgical bonding. *EX1022* at 3:49-56. Indeed, it was known that “when a solder bump made of, for example, SnPb, SnAg, SnCu, SnAgCu, SnZn, SnZnBi, SnIn...Sn, which the solder bump is primarily made of, diffuses into the electrode pad and wiring made of Al or Cu,” which may result “in electric problems in some cases.” *EX1047* at [0003]. “To prevent the diffusion, a UBM [] that is highly effective in preventing solder diffusion is used between the electrode pad and the solder bump,” i.e., reducing the risk of intermetallic formation. *EX1047* at [0004]. “As a typical example, of the UBM having the barrier capability, Ni...is often used.” *EX1047* at [0004]. Therefore, a POSITA would have recognized that a UBM structure, such as Lin-191’s metal pillar or bump 710, would improve the connection between Sundaram’s *first metal pad* and *third metal interconnect* by preventing diffusion of solder material into the *first metal pad*.

172. Additionally, a POSITA would have understood that by employing Lin-191’s layered structure the solder joint would have increased resistance to fatigue and stress-induced failure because the copper seed layer would insure a uniform plating of the thicker copper portion (layer 713) as electroplating copper without a

seed layer may “lead to a void in the electroplated metal[,” thereby compromising mechanical integrity. *EX1063* at 3:12-16. Additionally, a POSITA would have appreciated the advantages of coppers use in interconnects and been motivated to include the *third copper layer ha[ving] a thickness between 5 and 30 micrometers* in the *third metal interconnect*. Specifically, copper was known to have “high immunity to electromigration, high ductility, and high melting point[,” making it a desirable choice for interconnect material in high-density packaging. *EX1054* at 2:2-14.

173. Thus, the mechanical integrity of Sundaram’s *third metal interconnect* would be improved by employing such a layered structure, thereby enhancing the reliability of the interconnects, particularly in applications subjected to repeated temperature fluctuations and mechanical stress. As such, the modification of Sundaram’s *third metal interconnect*, per Lin-191’s metal pillar or bump 710, would have been an obvious and advantageous modification to improve long-term solder ball performance.

174. Moreover, a POSITA would have appreciated that the thickness of Lin-191’s *third copper layer* (i.e., between “2 and 30 micrometers” which teaches or renders obvious *between 5 and 30 micrometers*) would allow for optimal underfill placement, as demonstrated by Lin-191. *EX1005* at FIG. 72. Specifically, as shown

above in FIG. 72, Lin-191's metal pillars or bumps 710 are surrounded by "underfill 730[.]" *EX1005* at [0381]. A POSITA would recognize that Lin-191's thickness of layer 713 (*third metal layer*) allows for ample space for underfill 730 to be placed and would have found that desirable as limited space would prevent proper underfill filling. As shown in FIG. 3, Sundaram already teaches such an underfill between first electronic device 125 and interposer 105 such that applying Lin-191's third copper layer thickness would have allowed for Sundaram's underfill to be sufficiently deposited. Underfill integrity was an important feature as underfill materials were known to "redistribute the stress caused by CTE mismatch" by "allow[ing] [] stress to be more uniformly spread out over the entire surface of the chip, supporting substrate and solder balls." *EX1135* at 4:34-40. Accordingly, a POSITA would have appreciated that Lin-191's *third copper layer* thickness would achieve proper underfill filling, thereby decreasing CTE mismatch-induced stress to Sundaram's first electronic device 125, *third metal interconnect*, and RDL.

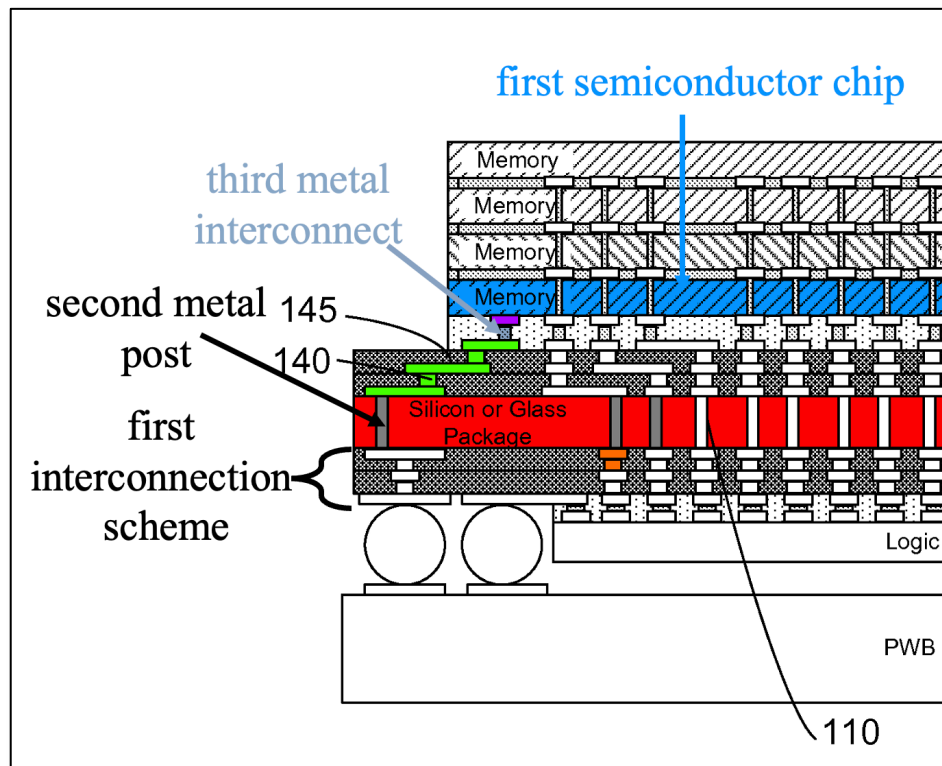
175. A POSITA would have found the modification obvious at least because it is nothing more than the application of a known technique (a layered bump structure) to improve similar structures (Sundaram's chip package, Lin-191's chip package) in a predictable manner. That is, Sundaram's *third metal interconnect* is improved in the same way as Lin-191's metal pillar or bump 710. Alternatively, a

POSITA would have been motivated to substitute Lin-191's bump structure for Sundaram's *third metal interconnect* to obtain the above-described advantages of Lin-191's teachings.

176. A POSITA would have had a reasonable expectation of success in both applying Lin-191's teachings to Sundaram's *third metal interconnect* or substituting Lin-191's metal pillar or bump 710 for Sundaram's *third metal interconnect*. Indeed, Lin-191 and Sundaram are both directed to semiconductor package interconnect technology. Further, bump interconnects were well-known and formed using common manufacturing techniques, such as physical-vapor deposition, sputtering, and electroplating. *EX1005* at [0413], [0420]; *EX1042* at (“...filled with copper typically by an electroplating process, as known to one of ordinary skill in the art of integrated circuit fabrication.”); *EX1043* at [0032] (“... a variety of different deposition methods known by one of ordinary skill in the art, including but not limited to, CVD, pulsed CVD, PECVD, ALD, PEALD, or sputtering methods.”); ¶¶ 71-75. For example, Lin-191's methods of forming metal or pillar bump 710, such as electroplating, were well-known and well-established, further contributing to a reasonable expectation of success. *EX1005* at [0400].

- 19. 1(e)(iv): “wherein said first semiconductor chip is connected to a second metal post of said plurality of metal posts through said third metal interconnect.”**

177. First electronic device 125 (*first semiconductor chip*) is connected to a second metal post of said plurality of metal posts because the first metal pad (purple) of claim 1(e)(ii) is connected to Sundaram's third metal interconnect which, through a series of traces 145 and vias 145 (shown in green), connects to the second metal post. See ¶ 163. Indeed, Sundaram expressly teaches that first electronic device 125 is connected to second electronic device 130 through traces 145 and vias 140, and FIG. 3 depicts such a connection as being achieved through the third metal interconnect and vias 110. *EX1004* at 7:1-9. Thus, device 125 (first semiconductor chip) is connected to a second metal post of said plurality of metal posts through said third metal interconnect. In my opinion, *connected to* does not require a direct physical connection but is instead met by an electrical connection. This is evidenced by the '306 Patent's descriptions at various spots, e.g., 2:40-42 (connection through a metal bump); 14:34-38 (connection of bumps 50 to layer 36 though layer 54); and 15:57-58 (connection of pads 49 to pads 48 through layer 51). Thus, Sundaram teaches the limitation.



EX1004 at FIG. 3 (excerpt).

B. Claim 2: “The chip package of claim 1, wherein said first semiconductor chip comprises a central-processing-unit (CPU) circuit block and a graphics-processing-unit (GPU) circuit block.”

a) Lin-191’s Teachings

178. Lin-191 teaches semiconductor chips as “system-on chip[s] (SOC) including a **graphics-processing-unit (GPU) circuit block**, a wireless local area network (WLAN) circuit block **and a central-processing-unit (CPU) circuit block...**” EX1005 at [0106], *see also* [0541], [0543].

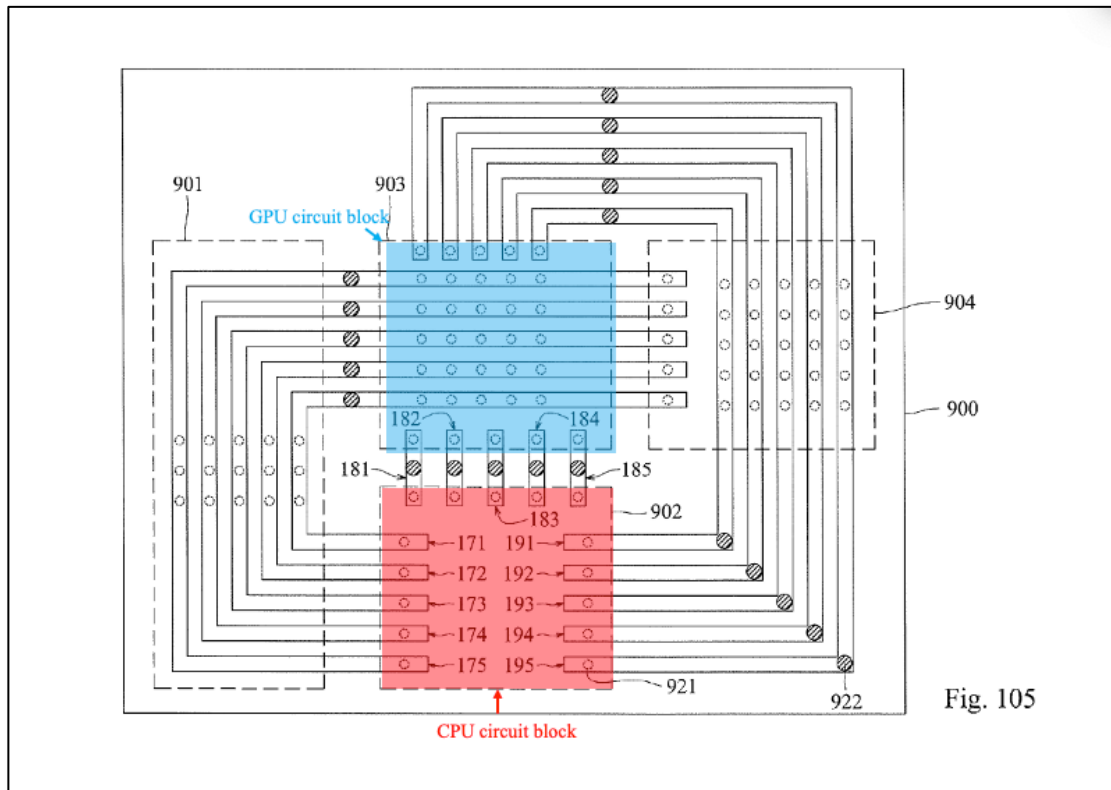


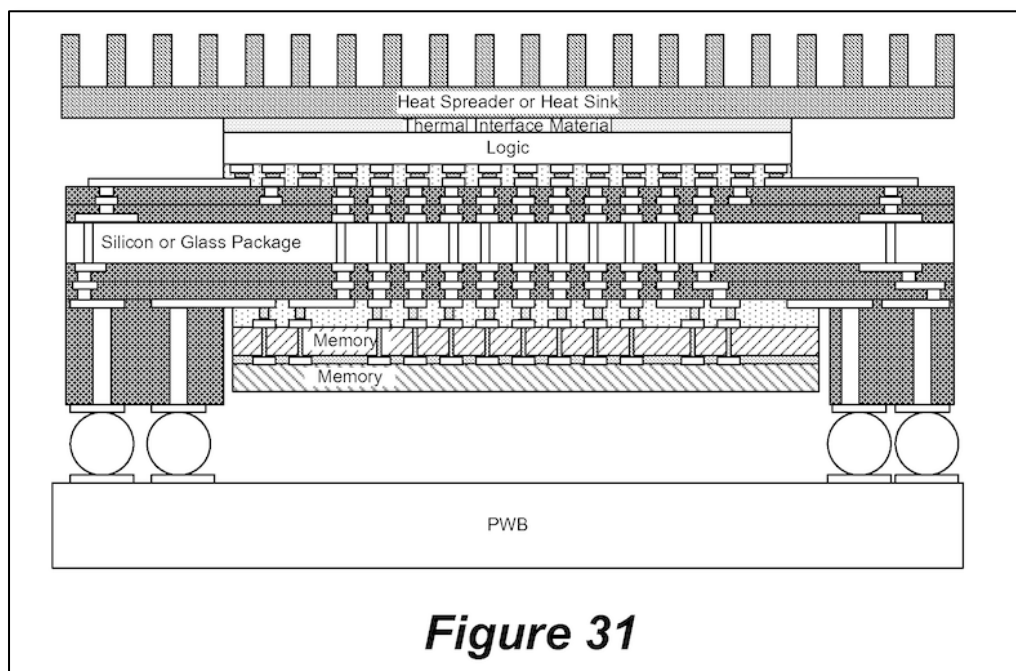
Fig. 105

EX1005 at FIG. 105, [0541], [0543] (describing FIG. 105).

b) Motivation to Combine

179. A POSITA would have found it obvious and been motivated to modify Sundaram's electronic device 125 to comprise *a CPU circuit block and a GPU circuit block* based on the teachings of Lin-191. The modification would have predictably improved Sundaram first electronic device 125 by providing first electronic device 125 with the ability to perform the functions of both a GPU and a CPU. While Sundaram's FIG.3 depicts device 125 as stacked memory, Sundaram teaches "other electronic devices can also be used as the first electronic device 125."

EX1004 at 6:37-43. Thus, a POSITA would have considered the depicted memory stack to be merely exemplary and would have been motivated to modify first electronic device 125 to have a CPU and GPU circuit block for applications requiring such processing power. Sundaram teaches “smart and mobile phone applications, including video streaming, 3D graphics, camera-functions, and gaming are driving the demand for logic to memory bandwidth [] at increasing levels without an increase in power consumption,” such that a POSITA would have found it obvious to modify Sundaram’s chips package, per Lin-191’s teachings, to carry out the requisite CPU/GPU tasks for such mobile phone applications. *EX1005* at 1:20-25. Further, Sundaram already contemplates “high power logic component[s]” on device 125’s side of interposer 105:



EX1004 at FIG. 31.

180. The Sundaram-Lin-191 combination is the application of a known technique (a semiconductor chip with a CPU circuit block and a GPU circuit block) to a known device (Sundaram's chip package including first electronic device 125) yielding the predictable results of Sundaram first electronic device 125 having both a CPU circuit block and a GPU circuit block. A POSITA would have been motivated to apply Lin-191's teachings based on the desired functionality of Sundaram's chip package, e.g., to obtain the benefits of having a CPU and a GPU on a single chip. As I described above, combined CPU/GPU architectures were known to provide the benefits such as the "opportunity to leverage both the high computational power from GPUs for regular applications and flexible execution from CPUs for irregular workloads" as well bypassing "costly CPU-GPU data transfers[.]" *EX1031* at p. 1-2; ¶¶ 86-87. As such, a POSITA would have been motivated to achieve such benefits by implementing Sundaram's first electronic device 125 (*first semiconductor chip*) with a *central-processing-unit (CPU) circuit block* and a *graphics-processing-unit (GPU) circuit block*.

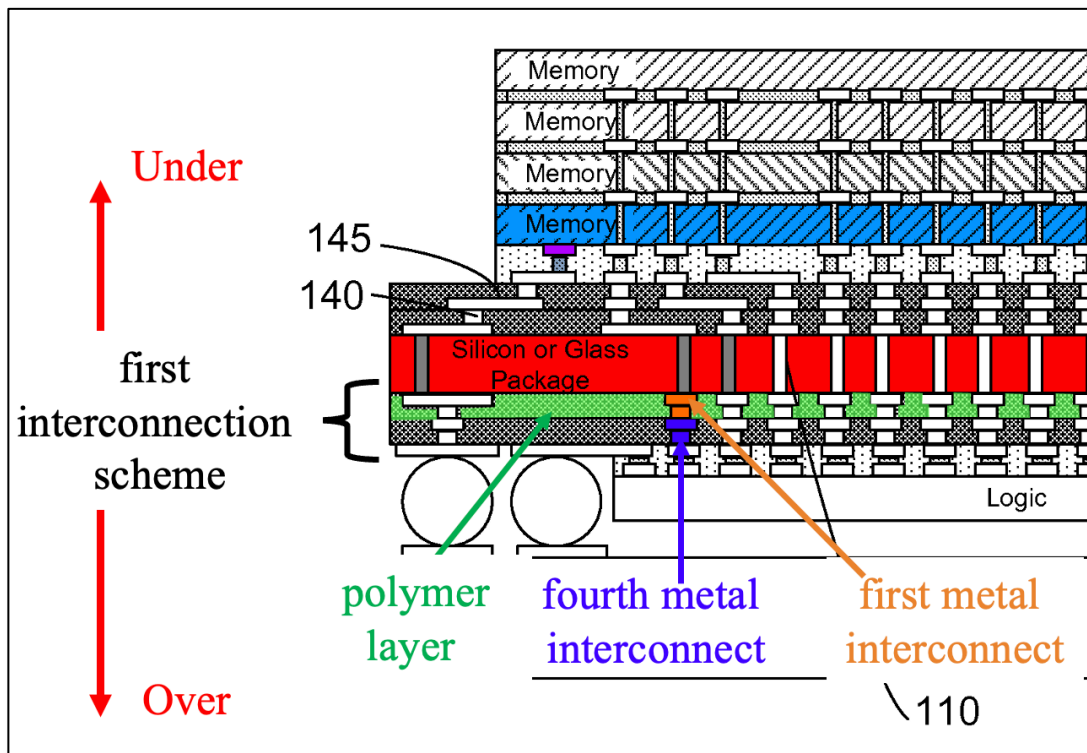
181. Because chips including both GPU and CPU circuit blocks were well known prior to the '306 Patent, there would have been a reasonable expectation of success. *See, e.g., EX1101* at [0022] ("In one embodiment, the APU 110 may include

a general purpose central processing unit (CPU) 130 and a graphics processing unit (GPU) 140 on a same semiconductor die.”). Indeed, by the time of the ’306 Patent, AMD and Intel had had both released chips having both GPU and CPU circuit blocks. *See* ¶¶ 86-87; *see also EX1102* at p. 1 (“The chip is Intel’s first to integrate the graphics processing unit (GPU) on the processor itself.”).

C. Claim 3

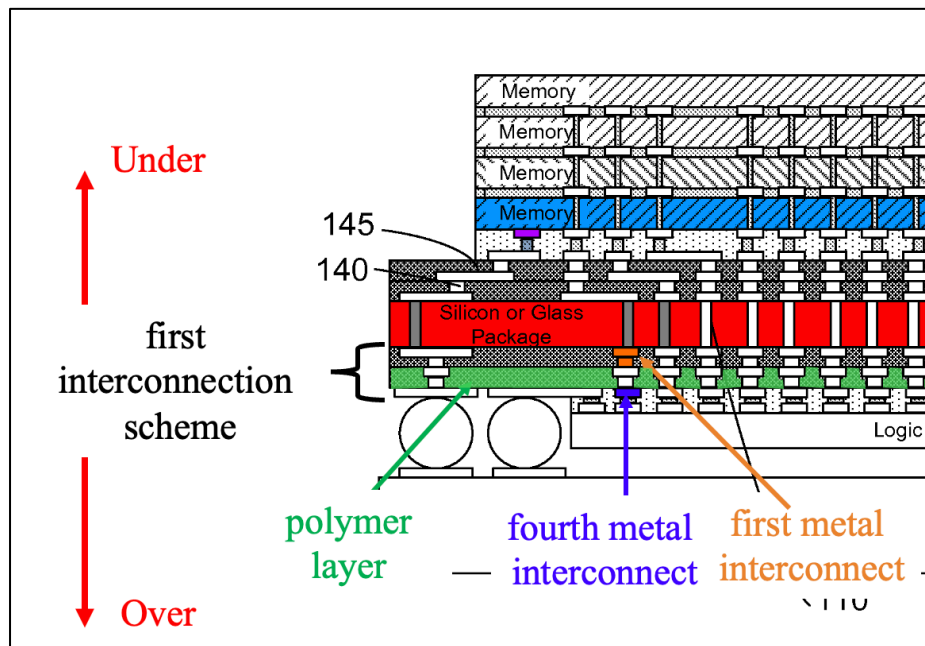
- 1. 3(a) “The chip package of claim 1, wherein said first interconnection scheme further comprises a fourth metal interconnect over said first metal interconnect and said polymer layer,”**

182. Shown below, a second set of a blind via 140 and conductor trace 145 in Sundaram’s polymer-metal redistribution layer is a *fourth metal interconnect* of the *first interconnection scheme*. That is, for the same reasons described above for the *first metal interconnect*, the via 140 and trace 145 identified below are the *fourth metal interconnect*. *See* ¶¶ 141-142. As shown, the *fourth metal interconnect* is *over said first metal interconnect and said polymer layer* as indicated by the red arrow depicting the over/under directions.



EX1004 at FIG. 3 (excerpt); ¶ 142.

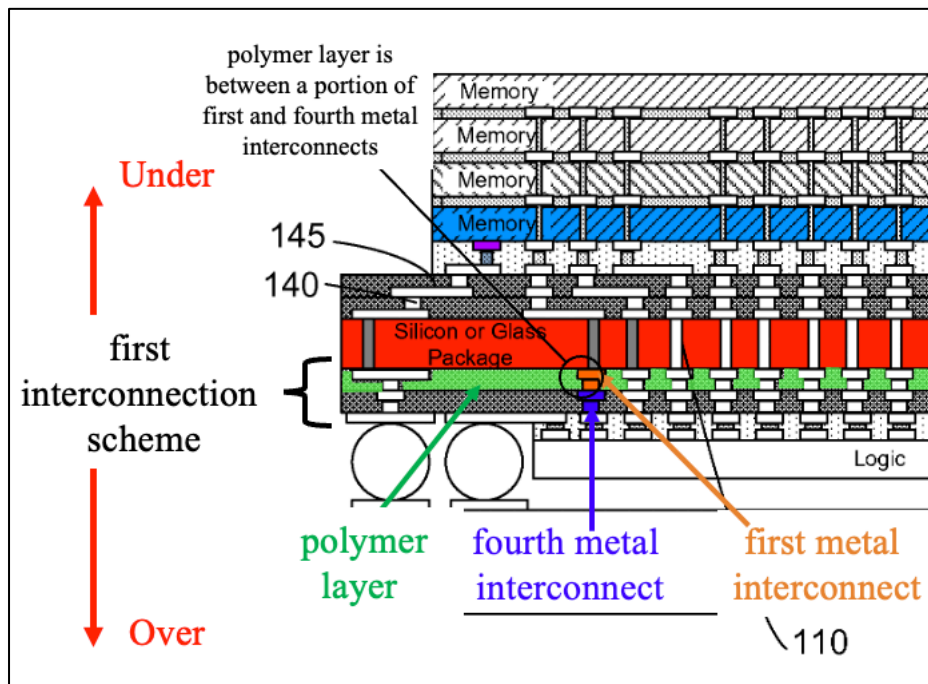
183. Alternatively, Sundaram's die pad 135 is a fourth metal interconnect over said first metal interconnect and said polymer layer:



EX1004 at FIG. 3 (excerpt); ¶ 143.

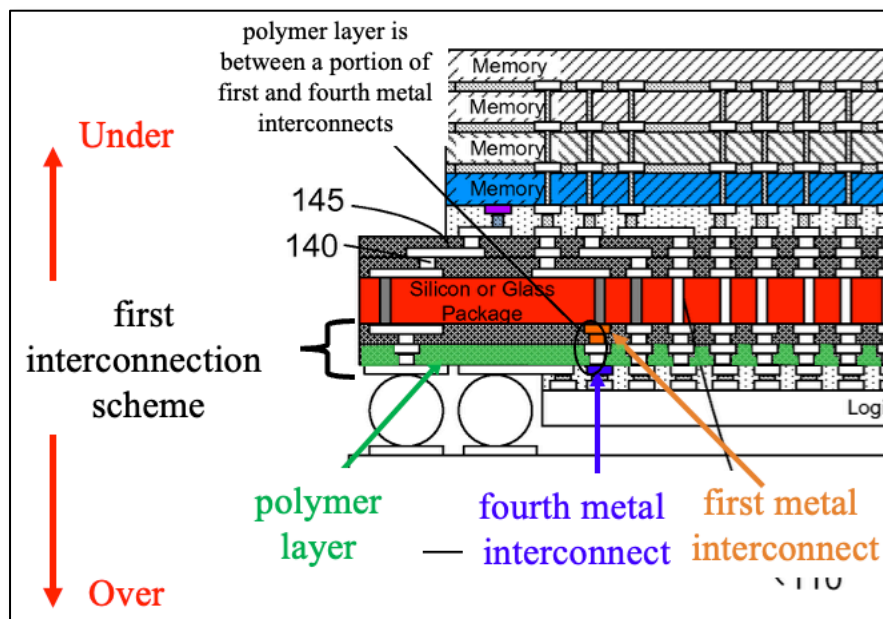
2. 3(b): “wherein said polymer layer is between said first and fourth metal interconnects,”

184. In both mappings of Sundaram’s *fourth metal interconnect* and the *polymer layer*, the *polymer layer* is between said first and fourth metal interconnects:



EX1004 at FIG. 3 (excerpt); ¶ 182.

185. Alternatively, said polymer layer is between said first and fourth metal interconnects, as shown:



EX1004 at FIG. 3 (excerpt); ¶ 183.

3. 3(c): “*wherein said fourth metal interconnect comprises a fourth metal layer and a fourth copper layer over said fourth metal layer.*”

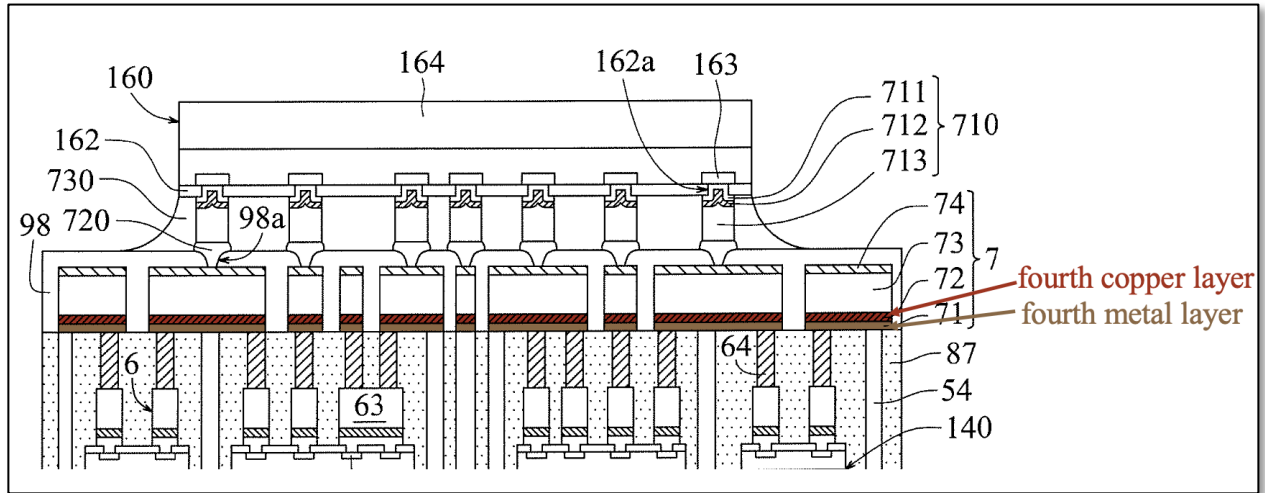
a) Sundaram’s Teachings

186. As I discussed above at claim 1(c)(iii), Sundaram’s teaches or renders obvious forming the metal interconnects (i.e., the *first metal interconnect* and including the *fourth metal interconnect*) of a *metal layer* formed by a copper seed layer and a *copper layer* formed by SAP. See ¶¶ 147-148. As such, Sundaram’s *fourth metal interconnect comprises a fourth metal layer and a fourth copper layer over said fourth metal layer.*

b) Lin-191’s Teachings

187. Lin-191 teaches a multilayered metal interconnect with two copper layers. Specifically, Lin-191 teaches a “patterned metal layer 7” having an “adhesion layer 71, the seed layer 72, the metal layer 73, and the barrier/wetting layer 74” EX1005 at [0379]. Layer 7 interconnects metal pillars or bumps 64 to various other structures, such “metal pillars or bumps 54” in Lin-191’s package and is therefore, like Sundaram’s trace 145 and vias 140, a *metal interconnect*. EX1005 at [0379]. Adhesion layer 71 is a *metal* (e.g., titanium or nickel) and is thus a *fourth metal layer*. EX1005 at [0260]-[0264]. Seed layer 72 is “a copper layer” on adhesion layer

71 and is thus a *fourth copper layer over said fourth metal layer*. EX1005 at [0261]-[0264].



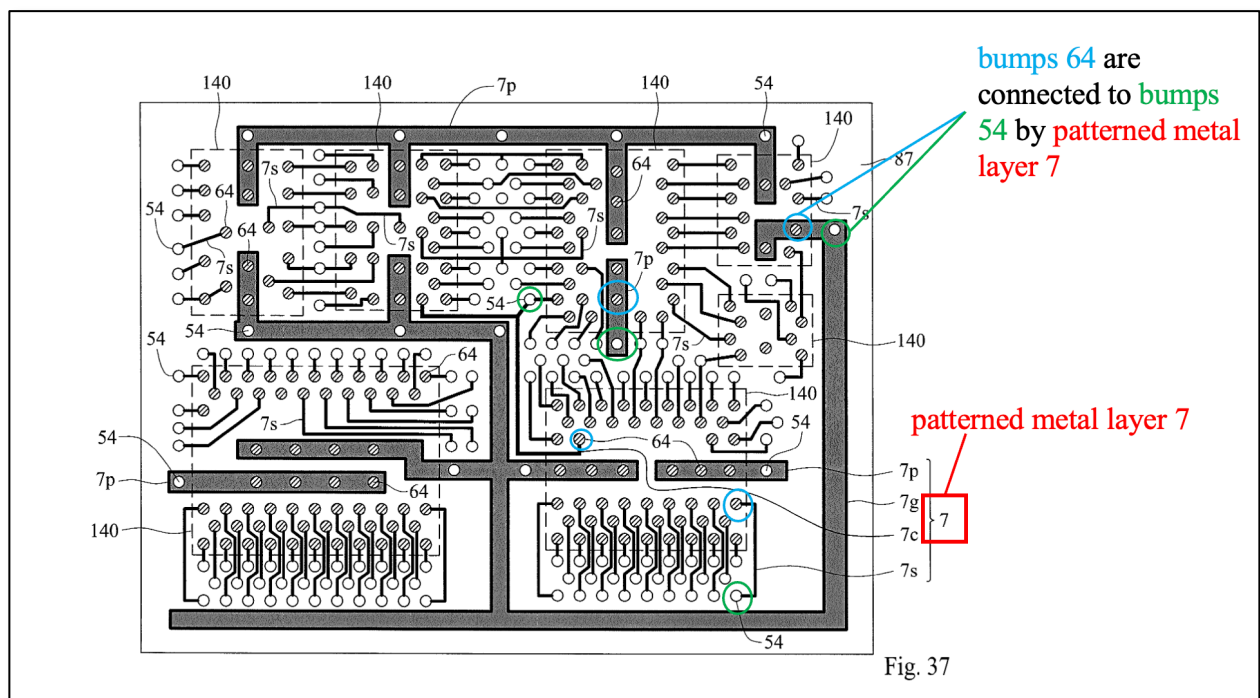
EX1005 at FIG. 72 (excerpt).

c) Motivation to Combine

188. A POSITA would have found it obvious and been motivated to modify Sundaram's *fourth metal interconnect* per Lin-191's teachings of patterned metal layer 7, thus yielding the *fourth metal interconnect compris[ing] a fourth metal layer and a fourth copper layer on said fourth metal layer*.

189. As shown below in FIG. 37, Lin-191 depicts a “schematic top perspective view of the patterned metal layer 7[.]” As shown, the patterned metal layers 7 makes lateral electrical connections (e.g., from bumps 54 (green) to bumps 64 (blue)). Several representative examples of such lateral electrical connections are annotated below. As such a POSITA would have understood layer 7 as being an

RDL. Additionally, because the top view of layer 7 depicts the lateral connections achieved by patterned metal layers 7, Lin-191 thereby demonstrates the applicability to Sundaram's conductor traces 145 and blind vias 140 which likewise make lateral electrical connections (e.g., between pads in the chips to through vias 110), thus motivating the combination. *EX1004* at FIG. 3.



EX1005 at FIG. 37.

190. The modification would have predictably improved Sundaram's chip package by providing a low resistance current path for signals traveling between the *first metal interconnect* and the *fourth metal interconnect*. Copper was known for its relatively low electrical resistivity and electromigration resistance. For example, it

was known that “as the size and cross-sectional dimensions of electrical interconnects get smaller, resistance increases and electromigration increases. Increased resistance and electromigration are undesirable for a number of reasons. For example, increased resistance may reduce device drive current, and source/drain current through the device, and may also adversely affect the overall speed and operation of the transistor.” *EXI054* at 1:39-46. Copper has a lower resistivity (1.73×10^{-6} ohm-cm at 20°C) compared to other materials, such as aluminum (2.824×10^{-6} ohm-cm at 20°C), as well as a “high immunity to electromigration, high ductility, and high melting point[,]” making it a desirable choice for interconnect material in high-density packaging. *EXI054* at 2:2-14.

191. Indeed, because copper has a relatively low electromigration rate, the risk of failures at elevated current densities is reduced. Specifically, it was known that “high current densities lead to electromigration-caused failures” in integrated circuits. *EXI055* at 1:30-32. Accordingly, a POSITA would have been motivated to choose a material, such as copper due to its lower resistivity, to reduce the risk of “electromigration-caused failures.” *EXI055* at 1:30-32. Similarly, because the resistivity of copper is relatively low, the electrical conductivity is relatively high compared to other materials (e.g., aluminum). *EXI056* at [0152] (“In addition, since the electrical conductivity of copper is higher than that of aluminum...”). It was

known that in “fabricating semiconductor components, interconnects having a high electrical conductivity...provide the best performance for a signal transmission system.” *EX1057* at 1:29-33.

192. Additionally, the modification would have predictably improved Sundaram’s chip package by reducing the risk of delamination between the copper interconnect and the metal layers it interconnects and mitigating diffusion of copper into the metal layers it interconnects, which may negatively impact electrical reliability and ruggedness of the chip package. Specifically, the risk of delamination is reduced because the diffusion of copper out of the interconnects is mitigated by the nickel layers 71 and 74, thereby preventing physical damage to the copper interconnects that leads to delamination. Indeed, the diffusion of copper into adjacent copper layers is reduced by adhesion layer 71 and barrier/wetting layer 74, which are both made of a “single layer of nickel[.]” *EX1005* at [0264], [0375]. As discussed, nickel was known to prevent copper diffusion into adjacent structures. *EX1040* at Abstract (“The structure comprises a layer of barrier metal, preferably nickel, that resists copper diffusion.”).

193. The modification is application of a known technique (Lin-191’s multi-layer interconnect) to a known device (Sundaram’s *fourth metal interconnect*) ready for improvement to yield the predictable result of Sundaram’s *fourth metal*

interconnect comprising the layers of Lin-191's layer 7. Further, a POSITA would have had a reasonable expectation of success because Lin-191's layer 7 and Sundaram's *fourth metal interconnect* perform the same function (interconnecting components in a chip package) and because layer 7 is formed using well-known techniques familiar to a POSITA, such as electroplating and sputtering. *EX1005* at [0414]-[0420]; *see, e.g., EX1042* at ("...filled with copper typically by an electroplating process, as known to one of ordinary skill in the art of integrated circuit fabrication."); *EX1043* at [0032] ("The metal-containing wetting film 104 may be deposited by a variety of different deposition methods known by one of ordinary skill in the art, including but not limited to, CVD, pulsed CVD, PECVD, ALD, PEALD, or sputtering methods."). Additionally, the use of multi-layer interconnects, as demonstrated by both Lin-191 and Sundaram, among other prior art references, was commonplace, further leading to a reasonable expectation of success. *EX1005* at FIG. 84; *EX1004* at FIG. 3; *see also EX1058* at FIGS. 5-6, 8:32-40.

D. Claim 4: "The chip package of claim 1, wherein said first metal pad is an aluminum pad."

194. Recall that Sundaram alone or Sundaram-Lin-191 teaches the claimed *first metal pad*. *See* ¶¶ 163-167. Lin-191, likewise, teaches metal pads 163 that "include **aluminum**." *EX1005* at [0384].

195. Metal pads are used for interconnecting chips to other components, where metal is used for the connection because it provides low resistance. Lin-191 teaches specifically a metal pad that is aluminum such that a POSITA would have found it obvious and been motivated to apply Lin-191's *aluminum pad* teachings to Sundaram's *first metal pad*. A POSITA would have found it obvious and been motivated specifically to implement Sundaram's *first metal pad* as an *aluminum pad*. at least because aluminum was a well-known, cost effective, and widely used material for forming contact pads in chips, because it is compatible with established bond wire attachment methods, is consistent with legacy materials used in semiconductor processing, and because methods of forming such aluminum pads were well known. *See, e.g., EX1059* at 3:65–4:2 (“Aluminum is the metal of choice for...bond pad metal in IC devices because of its superior electrical and thermal conductivity, low cost, wire-bondability, and other performance and reliability factors.”); *EX1061* at [0012] (“Materials that are commonly used for bond pads include...aluminum[.]”), [0013] (“The conventional processing sequence that is used to create an aluminum bond pad starts with a semiconductor surface.... A layer of Intra Metal Dielectric (IMD) is deposited over the surface, a layer of metal, typically aluminum, is deposited over the surface of the layer of IMD. The layer of metal is patterned and etched typically using a layer of photoresist and conventional

methods of photolithography and etching.”). The modification is the combination of prior art elements (aluminum pads, chip packages) according to known methods to yield predictable results i.e., Sundaram’s *first metal pad* being made of aluminum. Because aluminum was such a well-known material and because methods of forming aluminum pads were well-known, a POSITA would have had a reasonable expectation of success.

E. Claim 5: “The chip package of claim 1, wherein said compound comprises a SiO₂ compound.”

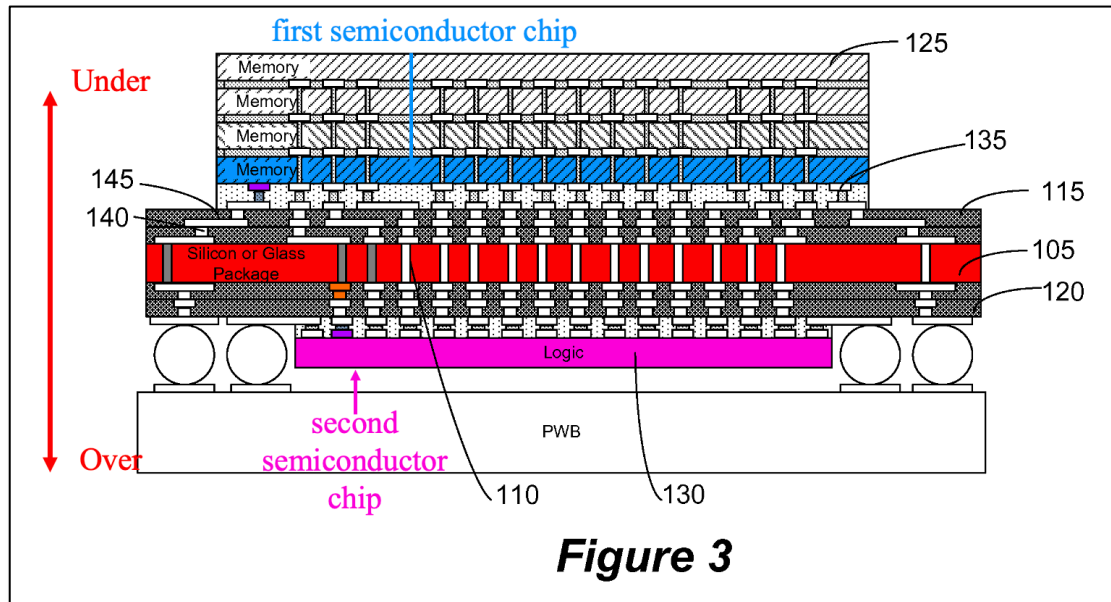
196. See Claim 1(a)(i), ¶¶ 128-129. Sundaram teaches both a borosilicate glass interposer and a silicon interposer with an SiO₂ layer. *EX1004* at 9:14-16, 13:58-62, FIG. 34. Borosilicate glass includes silica (SiO₂), thereby satisfying Claim 17. *EX1033* at 3:23-24 (“a borosilicate glass (SiO₂-B₂O₃).”); *EX1034* at 2:52-53 (“...the borosilicate glass powder contains SiO₂, B₂O₃, and K₂O[.]”).

F. Claim 6

1. 6(a): “The chip package of claim 1, further comprising a second semiconductor chip over said first semiconductor chip, wherein said second semiconductor chip comprises a second metal bump on a second metal pad of said second semiconductor chip,”

197. Shown below, Sundaram teaches a second electronic device 130 which may be a “logic IC device or devices” and is thus a *second semiconductor chip*.

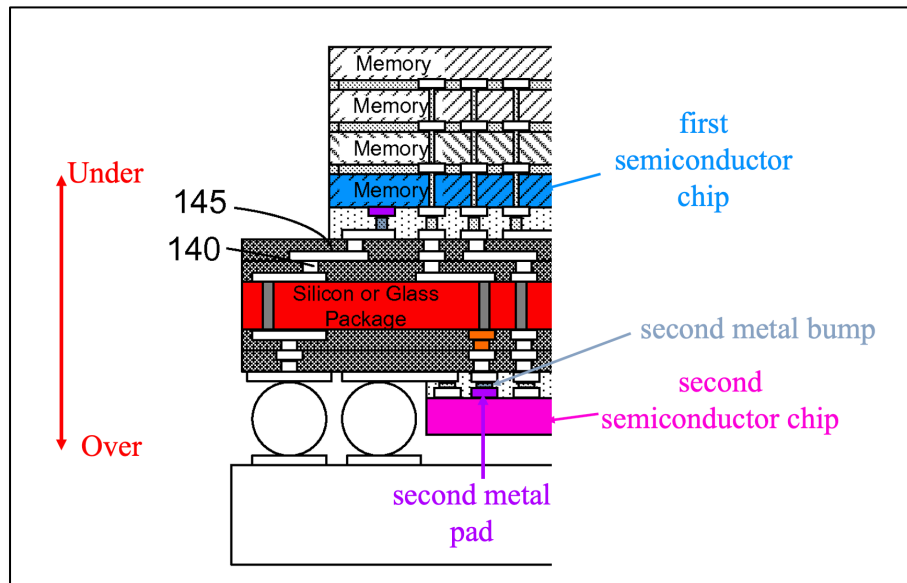
EX1004 at 6:38-39. As shown, Sundaram's *second semiconductor chip* is over said *first semiconductor chip*.



EX1004 at FIG. 3.

198. Further, for the same reasons discussed above at claim 1(e)(ii), Sundaram's *second semiconductor chip* comprises a *second metal bump on a second metal pad of said semiconductor chip*. See ¶¶ 163-167. The *second metal bump* of claim 6(a) corresponds to the *third metal interconnect* of claim 1(e)(ii). Specifically, recall that Sundaram teaches "die pads 135...can electrically connect devices using solder, copper bumps with solder caps, copper to copper bonding." EX1004 at 6:29-33. In FIG. 3, below, the *second semiconductor chip* is depicted as being connected to a bump on die pad 135. Because Sundaram teaches "copper bumps with solder caps[,]" the bump on die pad 135 is a *second metal bump*. EX1004 at 6:29-33.

199. In other words, the pad (purple) of Sundaram-Lin-191 shown in FIG. 3 below is a *second metal pad* and the *second metal bump* is shown as connecting the *second semiconductor chip* to die pads 135 of interposer 105. *EX1004* at 6:29-33.



EX1004 at FIG. 3 (excerpt).

2. 6(b): “wherein said second metal bump comprises a second tin-containing layer.”

200. As I discussed above at claim 1(d)(i), a POSITA would have found it obvious and been motivated to modify Sundaram’s *first metal bump* to comprise a *tin-containing layer* based on the teachings of Lin-191. See ¶¶ 150-158. Based on the same teachings, motivation to combine, and with the same reasonable expectation of success, a POSITA would have been motivated to modify Sundaram’s *second metal bump* to comprise[] a *second tin-containing layer*. See ¶¶ 150-158,

Lin-191's teachings, MTC, and reasonable expectation of success incorporated herein.

G. Claim 7: “The chip package of claim 1, wherein said solid layer further comprises a third region opposite to said second region, wherein said third region is between said first region and a second edge of said solid layer, wherein said plurality of metal posts in said plurality of through holes in said third region respectively.”

201. Sundaram teaches interposer 105 (*solid layer*) comprises a *third region*³, shown below, which is on the *opposite* side of the *first region* than the *second region* and is, therefore, *opposite to said second region*. The *third region* is *between said first region* (green) and a *second edge* (purple line on right-hand side) of said *solid layer*. Additionally, the *third region* comprises *copper plugs in through vias* (through vias 110), as shown.

³ The *third region* is not described in the '306 Patent's specification but was introduced by Applicant during original prosecution of the '306 Patent's parent (USPN 11,538,763). *EX1117* at 351-360. Applicant relied solely on FIG. 61 to support the *third region*.

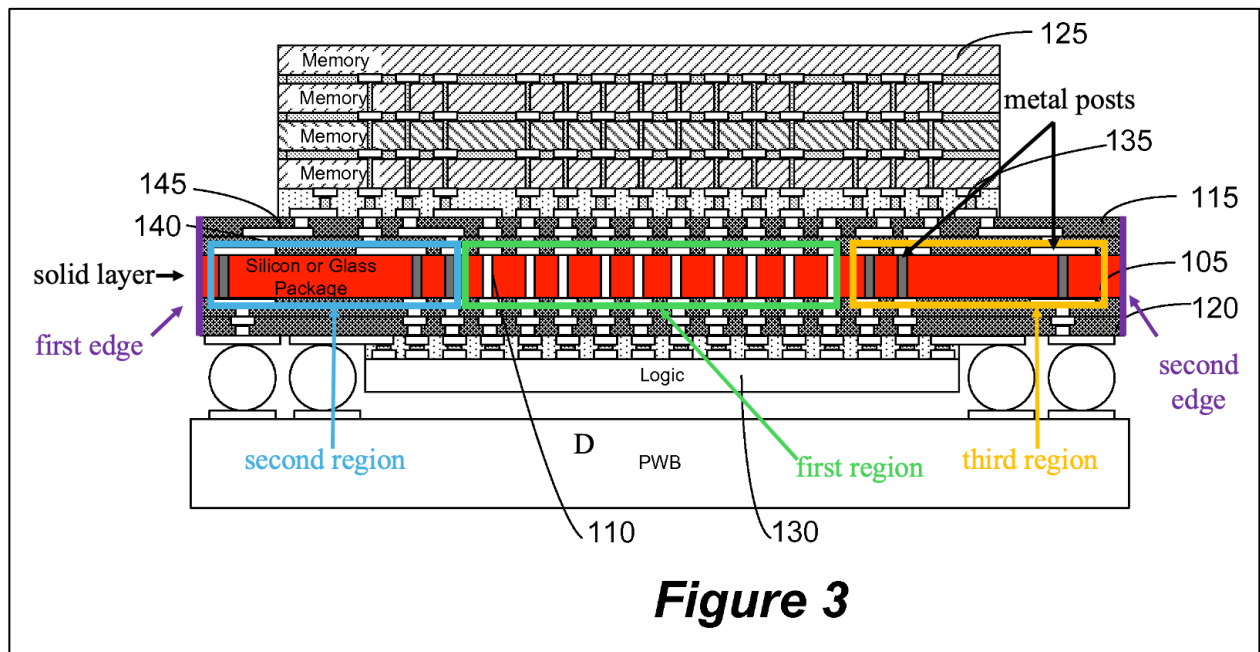
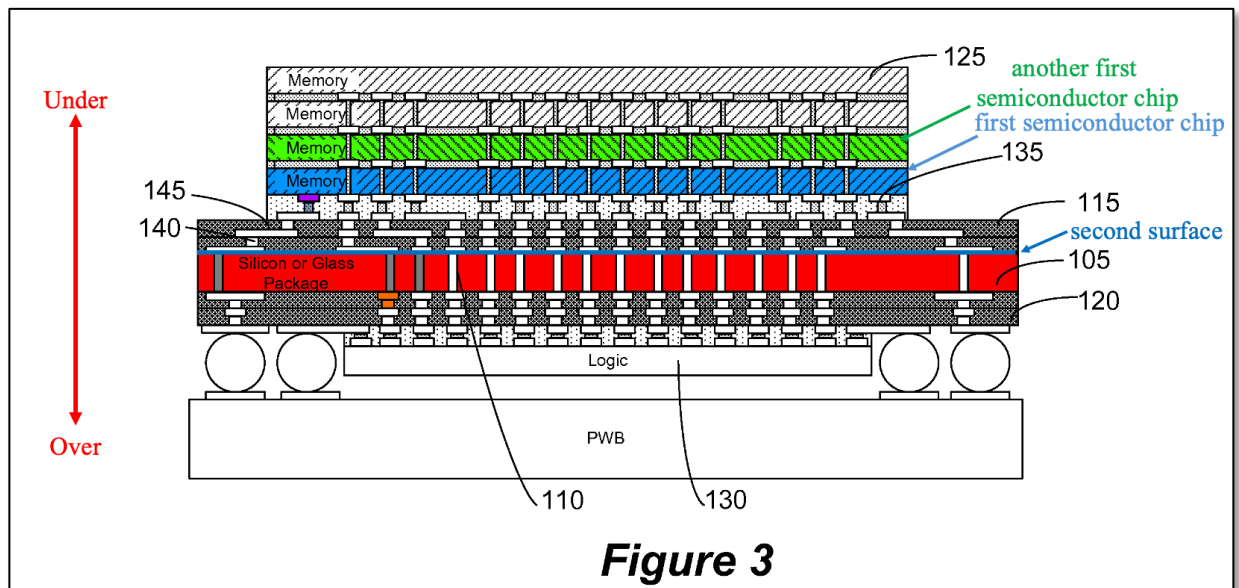


Figure 3

EX1004 at FIG. 3.

H. Claim 9: “The chip package of claim 1, further comprising another said first semiconductor chip under said second surface.”

202. Another of Sundaram’s first electronic device 125, as illustrated in the memory chip stack below, is *another said first semiconductor chip*. The *another first semiconductor chip* is *under said second surface* as indicated by the red arrow depicting the over/under directions.



EX1004 at FIG. 3.

A. **Claim 10:**

1. **10(Pre): “A chip package comprising:”**

203. See Claim 1(Pre)⁴, ¶ 125, incorporated herein.

⁴ I note that numerous claim limitations of later claims are the same or substantially the same as claim limitations from earlier claims. For examples, Claim 10(Pre) is substantially the same as Claim 1(Pre). For each claim limitation that is the same or substantially the same as an earlier claim limitation, I provide a cross-reference citation to my opinions for the earlier claim limitation, which should be understood to incorporate by reference for the later claim limitation.

2. ***10(a): “a solid layer having a first surface and a second surface opposite to said first surface,”***

204. See Claim 1(a), ¶¶ 126-127, incorporated herein.

3. ***10(a)(i): “wherein said solid layer comprises a compound of silicon and oxygen,”***

205. See Claim 1(a)(i), ¶¶ 128-129, incorporated herein.

4. ***10(a)(ii): “wherein said solid layer has a thickness between 100 and 300 micrometers,”***

206. Sundaram’s interposer (*solid layer*) is “about 20 to about 200 micrometers in thickness.” *EX1004* at 2:22-25. Because Sundaram teaches a range that overlaps the claimed range, Sundaram at least renders obvious Claim 1(a)(iii). Specifically, the claim recites a *thickness between 100 and 300 micrometers*, which overlaps with Sundaram’s teaching of 20 to about 200 micrometers, namely the range of 100-200 micrometers within the 20-200 range. Sundaram therefore expressly teaches a thickness, specifically 100-200 micrometers, that is within the claimed range of *between 100 and 300 micrometers* to thereby teach or render obvious Claim 10(a)(ii).

207. Additionally, Sundaram teaches an embodiment where a glass interposer has a thickness of 175 micrometers, which is a specific point within the claimed range of *between 100 and 300 micrometers*, further teaching the claimed range. *EX1004* at 9:14-16, FIG. 3. The FIG. 13 embodiment, like FIG. 3, is made of

glass (e.g., “borosilicate glass”) such that a POSITA would have recognized the applicability of the FIG. 13 embodiment to FIG. 3. *EX1004* at 9:14-16, 5:54-55. That is, a POSITA would have recognized that because FIG. 13 and FIG. 3’s interposer are made of the same material (glass) that the specific thickness of 175 μm , which is within the thickness range of 20-200 μm , was an applicable example of a specific thickness at which FIG. 3’s interposer 105 would be formed. *EX1004* at 9:14-16, 2:22-25.

208. I also note that the ’306 Patent does ascribe any criticality to the range of 100 and 300 micrometers. That is, the ’306 Patent does not provide the range of 100 and 300 micrometers and then further provide an explanation for why such range is needed, important, or advantageous. Indeed, the ’306 Patent describes a variety of ranges, including smaller (20 micrometers) and much larger ranges (2000 micrometers), indicating to a POSITA that the thickness can widely vary and that the thickness is not otherwise critical, further supporting the presumption of obviousness. *See EX1001* at 7:58-64.

5. ***10)(a)(iii): “wherein said solid layer comprises a first region and a second region between said first region and a first edge of said solid layer;”***

209. *See* Claim 1(a)(iii), ¶ 132, incorporated herein.

6. ***10(b): “a plurality of copper posts in a plurality of through holes in said second region respectively,”***

210. See Claim 1(b), ¶ 133, incorporated herein. Because Sundaram's through vias 110 are "metalized with...copper[,]" through vias 110 are a *plurality of copper posts in a plurality of through vias*.

7. **10(b)(i): "wherein said first region has a width in a direction greater than a shortest distance between a sidewall of one of said plurality of through holes and said first edge in said direction and greater than a pitch between two neighboring copper posts of said plurality of copper posts;"**

211. See Claim 1(b)(ii), ¶¶ 136-137, incorporated herein.

8. **10(c): "a first interconnection scheme over said first surface,"**

212. See Claim 1(c), ¶ 138, incorporated herein.

9. **10(c)(i): "wherein said first interconnection scheme comprises a first metal interconnect over said first surface, and a polymer layer over said first metal interconnect,"**

213. See Claim 1(c)(i), ¶¶ 138-143, incorporated herein.

10. **10(c)(ii): "wherein said first metal interconnect is connected to one of said plurality of copper posts,"**

214. See Claim 1(c)(ii), ¶ 146, incorporated herein. Claim 10(c)(ii)'s *one of said plurality of copper posts* corresponds to claim 1(c)(ii)'s *first metal post*.

11. **10(c)(iii): "wherein said first metal interconnect comprises a first metal layer and a first copper layer over said first metal layer;"**

215. See Claim 1(c)(iii), ¶ 147, incorporated herein. Claim 10(c)(iii)'s *first copper layer* corresponds to Claim 1(c)(iii)'s *second copper layer*.

12. 10(d): “a first metal bump over said first interconnection scheme,”

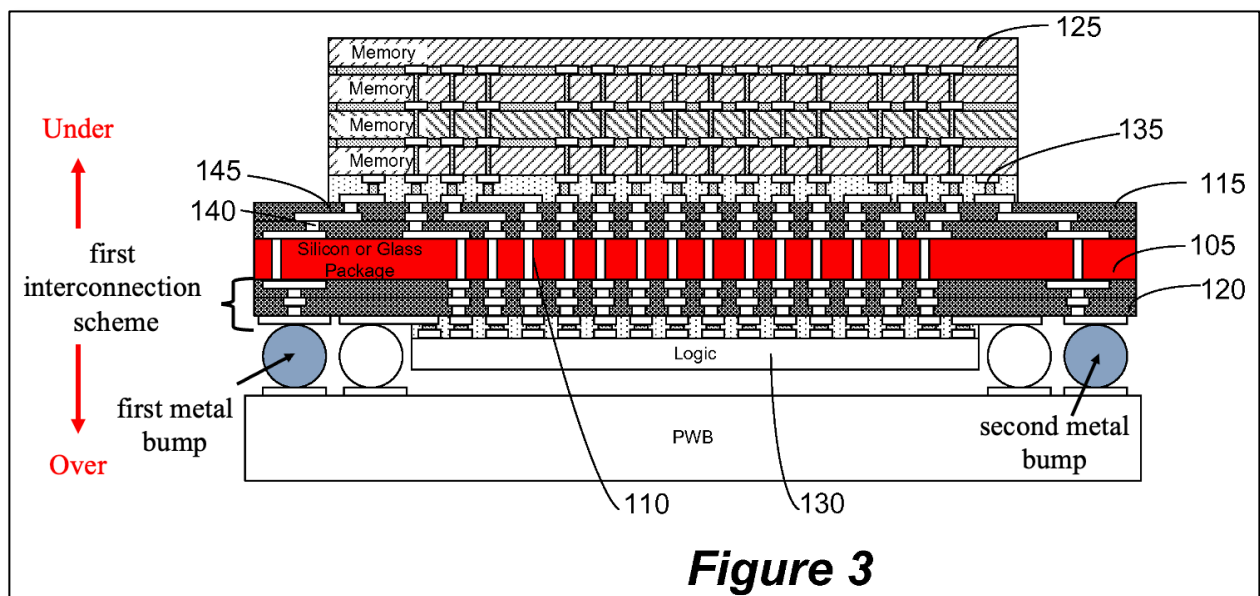
216. See Claim 1(d), ¶ 149, incorporated herein.

13. *10(d)(i): “wherein said first metal bump comprises a first tin-containing layer;”*

217. See Claim 1(d)(i), ¶¶ 150-158, incorporated herein.

14. 10(e): “a second metal bump over said first interconnection scheme;”

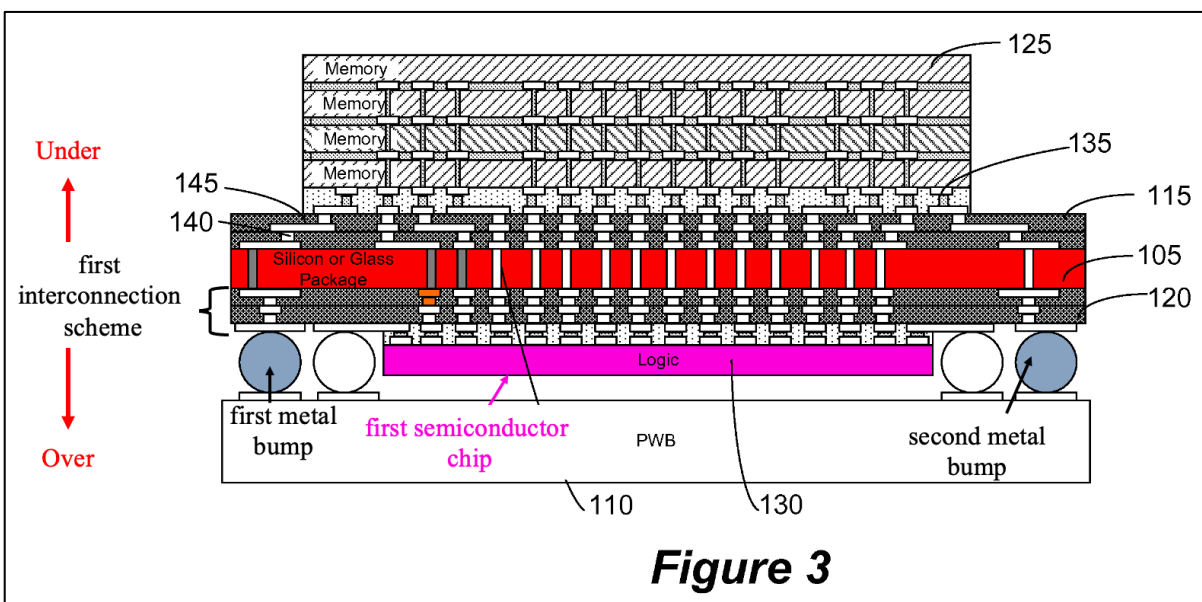
218. Sundaram’s chip package includes a *second metal bump over said first interconnection scheme*, shown below. The annotated bump is a *second metal bump* for the same reasons described above at claims 10(d), 1(d), i.e., because it’s a “copper bump with [a] solder cap[.]” See ¶¶ 216, 149, incorporated herein; *EX1004* at 6:29-31.



EX1004 at FIG. 3.

15. 10(f): “a first semiconductor chip over said first interconnection scheme and between said first and second metal bumps,”

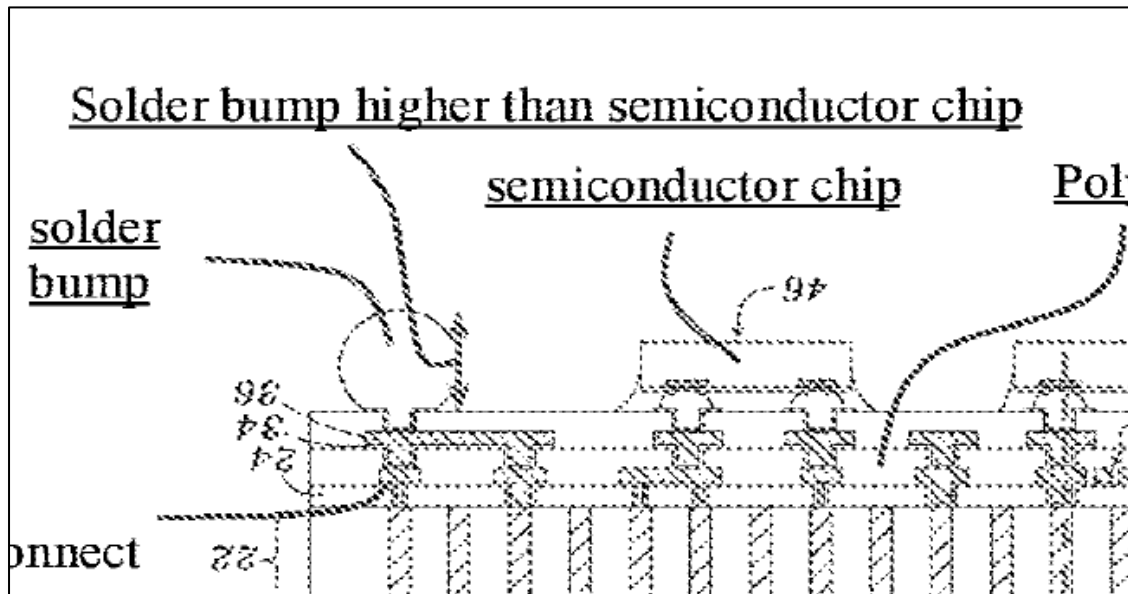
219. Second electronic device 130 is a “logic IC device or devices” and is thus a *first semiconductor chip*. EX1004 at 6:37-39. As shown below, second electronic device 130 is positioned over said first interconnection scheme and between said first and second metal bumps.



EX1004 at FIG. 3.

16. 10(f)(i): “wherein said first semiconductor chip has a height between a backside surface of said first semiconductor chip and a top surface of said polymer layer is smaller than a thickness of said first metal bump,”

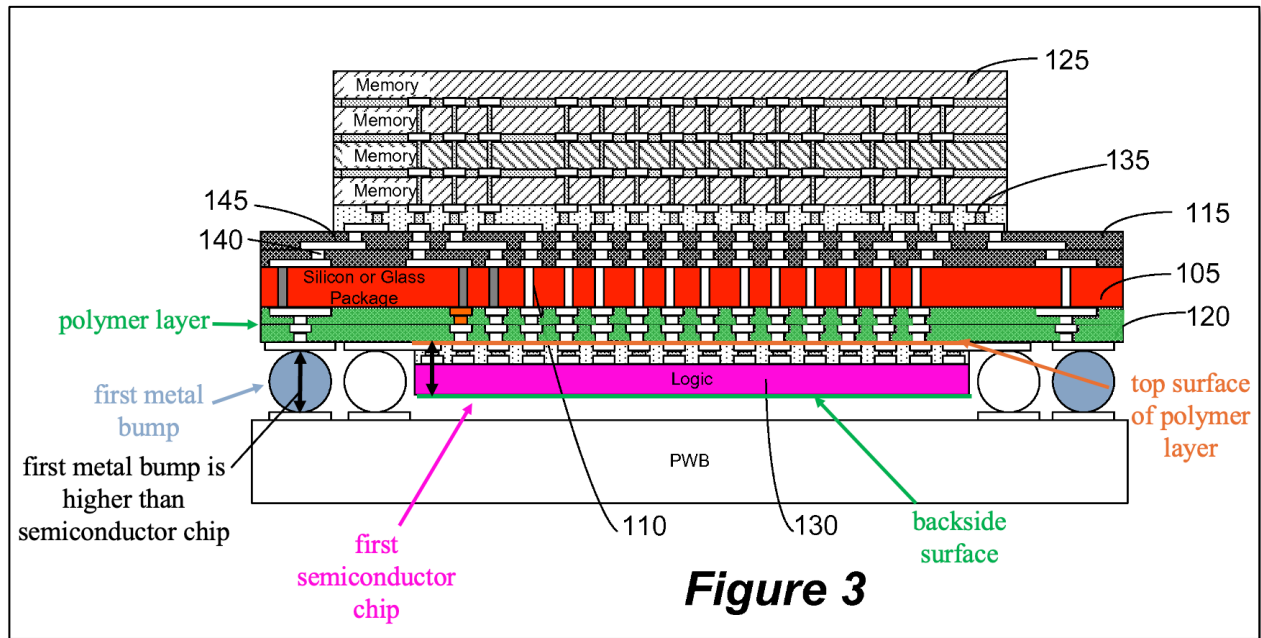
220. I note that during prosecution of the '306 Patent's grandparent patent (USPN 11,107,768 ("the '768 Patent")), the Patent Owner provided an annotated figure illustrating support for claim language similar to 10(f)(i), as shown below.



EX1032 at 400.

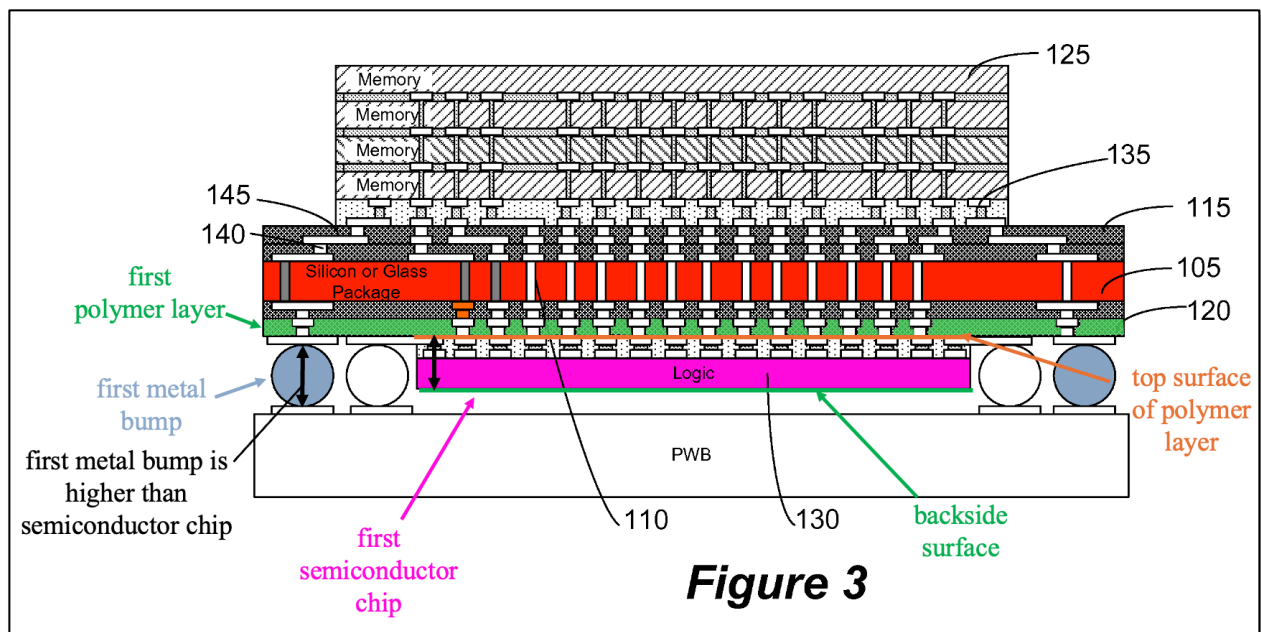
a) Sundaram's Teachings

221. The *polymer layer* includes at least the portion described above at Claim 1(c)(i) and further includes the portion highlighted below. See ¶ 142. Shown in FIG. 3, below, Sundaram's second electronic device 130 (*first semiconductor chip*) has a height between a backside surface of second electronic device 130 and a top surface of Sundaram's first polymer layer, which is smaller than thickness of Sundaram's solder ball (*first metal bump*).



EX1004 at FIG. 3; ¶ 142.

222. Alternatively, Sundaram's *first polymer layer* is as annotated below, which also meets the claim limitation.



EX1004 at FIG. 3; ¶ 143.

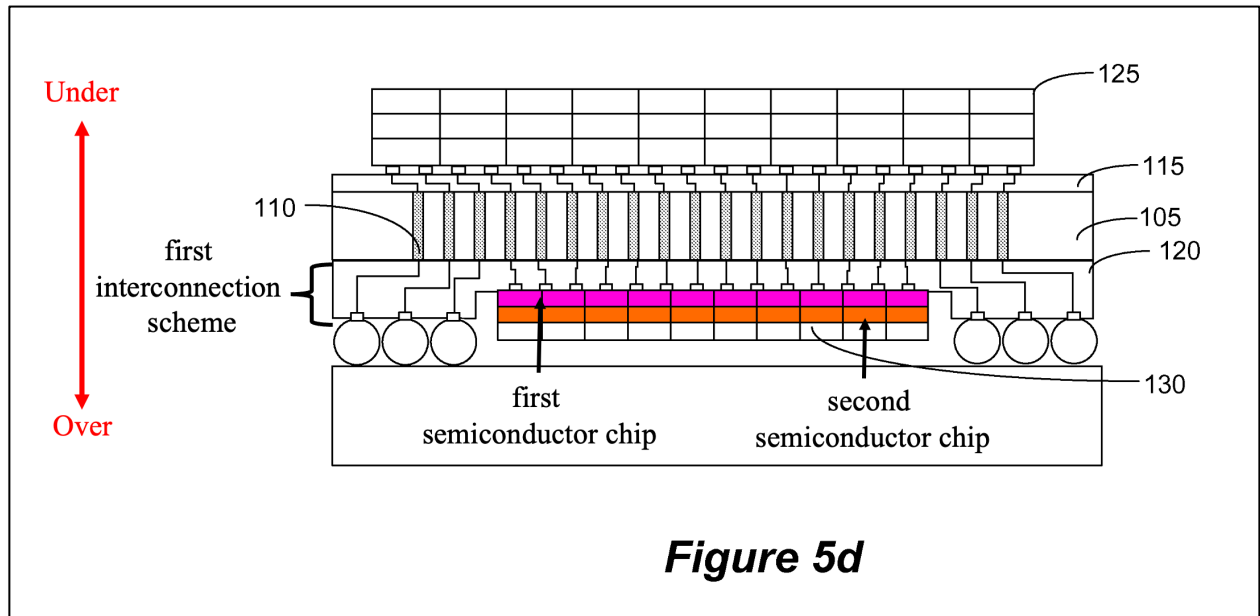
17. 10(f)(ii): “wherein said first semiconductor chip comprises a third metal bump on a first metal pad of said first semiconductor chip, wherein said third metal bump comprises a second tin-containing layer; and”

223. See Claims 6(a)-(b), ¶¶ 197-200, incorporated herein. Claim 10(f)(ii)’s *first semiconductor chip*, *third metal bump* and *first metal pad* correspond to claim 6’s *second semiconductor chip*, *second metal bump*, and *second metal pad*, respectively. In other words, the limitations of Claim 10(f)(ii) correspond to those of Claim 6, including the interrelationship to the claimed components, because they recite the same claimed structure other than the nomenclature of *first*, *second*, and *third*.

18. 10(g): “a second semiconductor chip over said first interconnection scheme,”

224. Sundaram teaches “third and fourth electronic devices can be stacked on the first 125 and second 130 electronic devices,” thus, the fourth electronic device stacked on the second device 130 is *a second semiconductor chip over said first interconnection scheme*. EX1004 at 7:16-18. Indeed, the *second semiconductor chip* is shown below in FIG. 5d. Because FIG. 5 “show[s] various exemplary embodiments of the interconnect structure 100,” a POSITA would have understood that the stacked chips in second electronic device 130 shown in FIG. 5d represent a

second semiconductor chip over the first interconnection scheme in Sundaram's interconnect structure 100 depicted in FIG. 3. EX1004 at 7:7-9, 5:45-46, FIG. 3.



EX1004 at FIG. 5d.

19. 10(g)(i): “*wherein said second semiconductor chip comprises a fourth metal bump on a second metal pad of said second semiconductor chip, wherein said fourth metal bump comprises a third tin-containing layer.*”

225. As discussed above at claim 6(a), Sundaram teaches a *metal bump* connecting second electronic device 130 (a *semiconductor chip*) to interposer 105. See ¶¶ 197-199. Additionally, recall that a POSITA would have found it obvious and been motivated to modify Sundaram’s *metal bump[s]* to comprise a *tin-containing layer*. See ¶¶ 150-158.

226. It would have been obvious for a *second semiconductor chip* of the stacked electronic devices taught by Sundaram (see 10(g)) to include a *fourth metal bump* and *second metal pad* already taught by Sundaram. This modification would have advantageously provided Sundaram with an interconnection between the *first* and *second semiconductor chips* when stacked. Specifically, it was well known to stack semiconductor chips having metal bumps between them for forming electrical connections. *See, e.g., EX1126* at FIG. 2, 6:65–7:1 (“...first and second semiconductor devices 100 and 200, and first and second bumps 400 and 410 for electrically connecting the first and second semiconductor devices 100 and 200[.]”). Alternatively, the modification would have advantageously provided Sundaram with an interconnection between the *second semiconductor chip* to Sundaram’s RDL on surface 120 in the same manner as Sundaram’s second electronic device 130, i.e., in a side-by-side arrangement. That is, when the *second semiconductor chip* is positioned adjacent to the *first semiconductor chip*, a *fourth metal bump* having a *tin-containing layer* would connect the *second semiconductor chip* to the RDL in the same manner that second electronic device 130 is connected.

227. The modification is the application of a known technique (connecting chips using metal bumps) to a known device (Sundaram’s chip package) ready for improvement to yield predictable results, i.e., Sundaram’s *second semiconductor*

chip having a second metal pad connected by a fourth metal bump having a tin-containing layer.

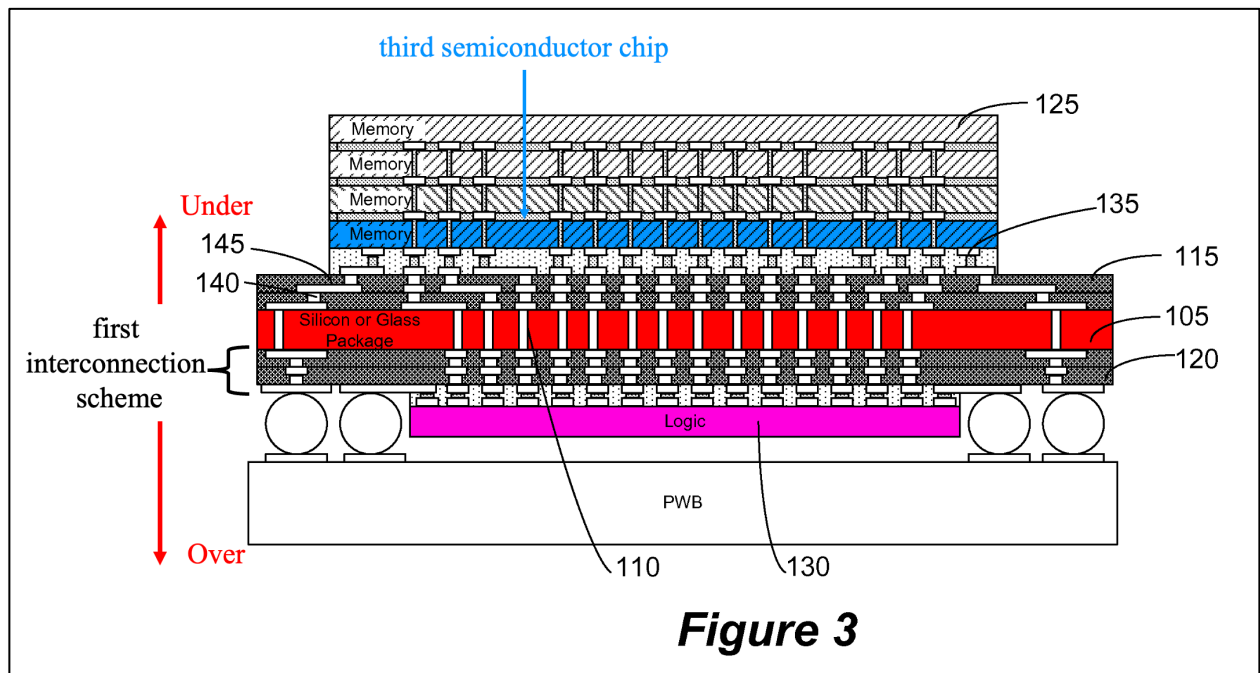
B. Claim 11: “The chip package of claim 10, wherein said compound comprises a SiO₂ compound.”

228. See Claim 5, ¶ 196, incorporated herein.

C. Claim 13

1. 13(a): “The chip package of claim 10, further comprising a third semiconductor chip under said first interconnection scheme,”

229. See Claim 1(e), ¶ 159, incorporated herein. Claim 13’s *third semiconductor chip* corresponds to claim 1(e)’s *first semiconductor chip* and is *under said first interconnection scheme*, as shown. In other words, the limitations of Claim 13(a) correspond to those of Claim 1(e), including the interrelationship to the claimed components, because they recite the same claimed structure other than the nomenclature of the *first* and *third*.



EX1004 at FIG. 3.

2. **13(b): “wherein said third semiconductor chip comprises a second metal interconnect on a third metal pad of said third semiconductor chip,”**

230. See Claim 1(e)(ii), ¶¶ 163-166, incorporated herein. Claim 13’s *third semiconductor chip*, *second metal interconnect*, and *third metal pad* correspond to Claim 1(e)(ii)’s *first semiconductor chip*, *third metal interconnect*, and *first metal pad*, respectively. In other words, the limitations of Claim 13(b) correspond to those of Claim 1(e)(ii), including the interrelationship to the claimed components, because they recite the same claimed structure other than the nomenclature of the *first*, *second*, and *third*.

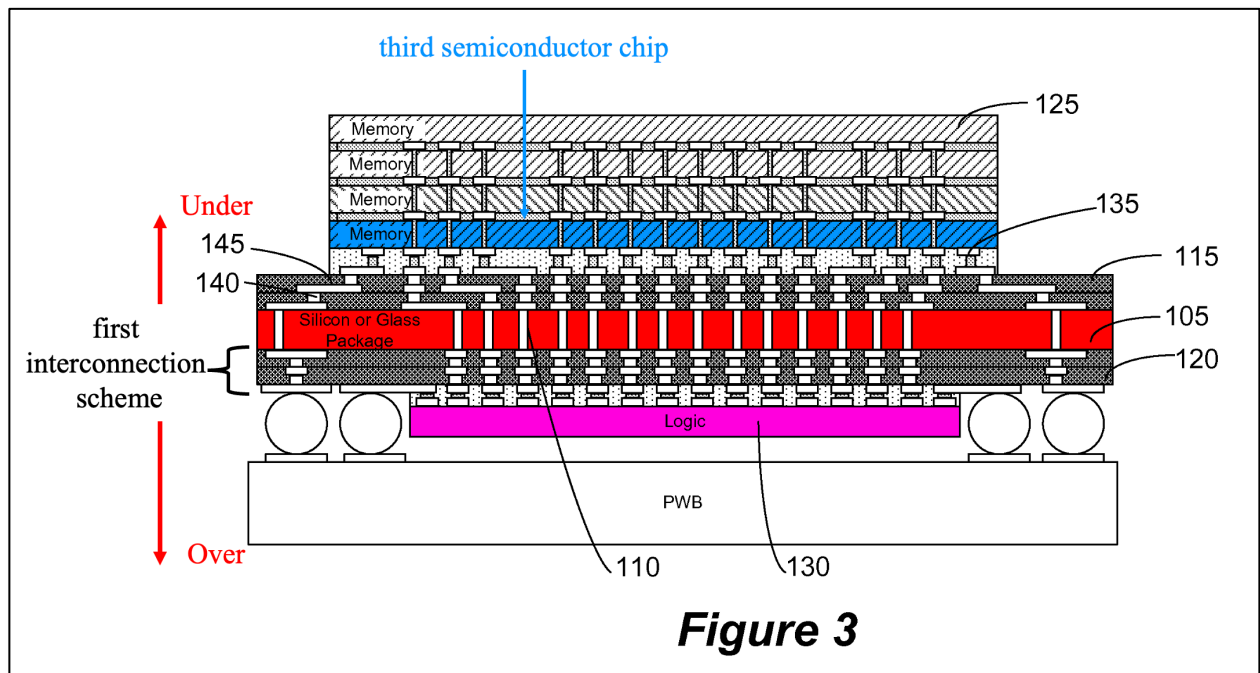
3. **13(c): “wherein said second metal interconnect comprises a second metal layer on said third metal pad and a second copper layer over said second metal layer, wherein said second copper layer has a thickness between 5 and 30 micrometers.”**

231. See Claim 1(e)(iii), ¶¶ 168-176, incorporated herein. Claim 13’s *second metal layer* and *second copper layer* correspond to Claim 1(e)(iii)’s *third metal layer* and *third copper layer*, respectively. In other words, the limitations of Claim 13(c) correspond to those of Claim 1(e)(iii), including the interrelationship to the claimed components, because they recite the same claimed structure other than the nomenclature of the *second* and *third*.

D. Claim 14

1. **14(a): “The chip package of claim 10, further comprising a third semiconductor chip under said first interconnection scheme,”**

232. See Claims 13(a), 1(e), ¶¶ 229,159, incorporated herein. Claim 14’s *third semiconductor chip* corresponds to Claim 13’s *third semiconductor chip* and to Claim 1(e)’s *first semiconductor chip*. The *third semiconductor chip* is *under said first interconnection scheme*. In other words, the limitations of Claim 14(a) correspond to those of Claims 13(a) and 1(e), including the interrelationship to the claimed components, because they recite the same claimed structure other than the nomenclature of the *first* and *third*.



EX1004 at FIG. 3.

2. 14(b): “wherein said third semiconductor chip comprises a second metal interconnect on a third metal pad of said third semiconductor chip,”

233. See Claim 13(b), 1(e)(ii), ¶¶ 230, 163-166, incorporated herein. Claim 14’s *second metal interconnect* and *third metal pad* correspond to Claim 13’s *second metal pad* and *third metal pad*, respectively, and to Claim 1(e)(ii)’s *third metal interconnect* and *first metal pad*, respectively. In other words, the limitations of Claim 14(b) correspond to those of Claims 13(b) and 1(e)(ii), including the interrelationship to the claimed components, because they recite the same claimed structure other than the nomenclature of the *second* and *third*.

3. ***14(c): “wherein said second metal interconnect comprises a second metal layer on said third metal pad and a second copper layer over said second metal layer,”***

234. See Claims 13(c), 1(e)(iii), ¶¶ 231, 168-176, incorporated herein. Claim 14’s *second metal layer* and *second copper layer* correspond to Claim 13’s *second metal layer* and *second copper layer*, respectively, and to Claim 1(e)(iii)’s *third metal layer* and *third copper layer*, respectively. In other words, the limitations of Claim 14(c) correspond to those of Claims 13(c) and 1(e)(iii), including the interrelationship to the claimed components, because they recite the same claimed structure other than the nomenclature of the *second* and *third*.

4. ***14(d): “wherein said third semiconductor chip comprises a central-processing-unit (CPU) circuit block and a graphics-processing-unit (GPU) circuit block.”***

235. See Claim 2, ¶¶ 178-180, incorporated herein. Claim 14’s *third semiconductor chip* corresponds to Claim 2’s *first semiconductor chip*.

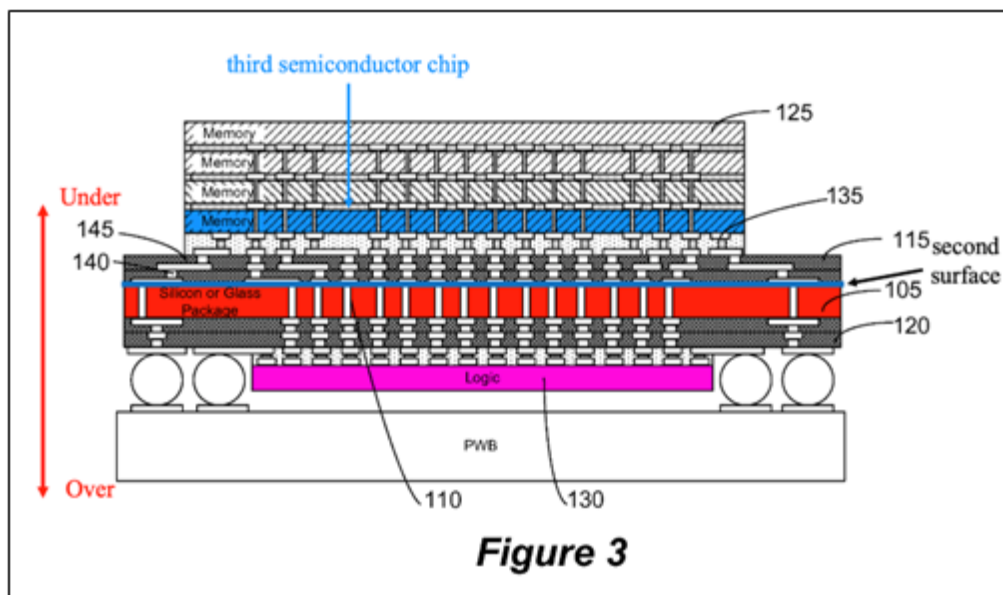
E. Claim 15: “The chip package of claim 10, wherein said solid layer further comprises a third region opposite to said second region, wherein said third region is between said first region and a second edge of said solid layer, wherein said plurality of copper posts in said plurality of through holes in said third region respectively.”

236. See Claim 7, ¶ 201, incorporated herein. Claim 15’s *plurality of copper posts* corresponds to Claim 7’s *plurality of metal posts*.

F. Claim 17

1. 17(a): “The chip package of claim 10, further comprising an electrical device under said second surface, wherein said electrical device comprise a third semiconductor chip and a metal wire connected to a third metal pad of said third semiconductor chip,”

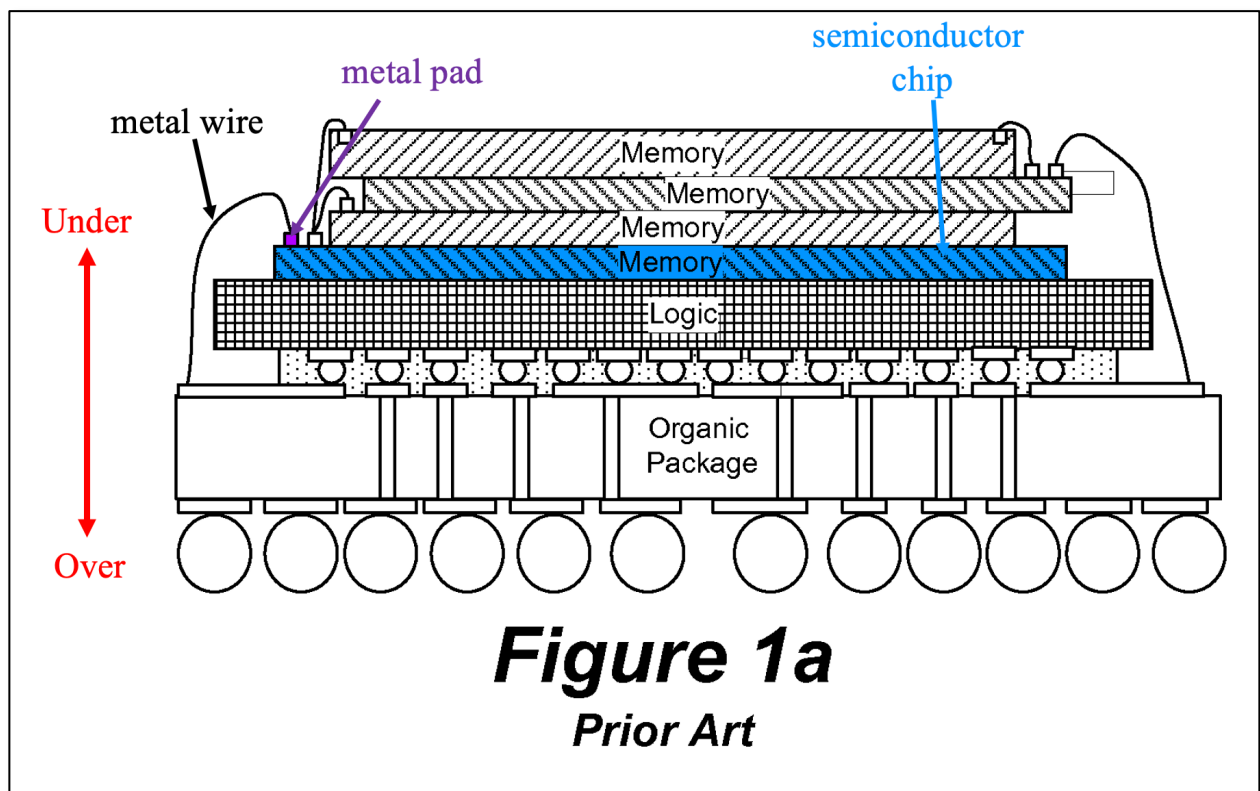
237. Sundaram teaches an *electrical device under said second surface* wherein the *electrical device* is a *third semiconductor chip*, shown below. See ¶¶ 229, 159, incorporated herein.



EX1005 at FIG. 3.

238. Sundaram further teaches a “wire-bonded SIP [system-in-package]” structures with memory chips including a *metal wire* for bonding. EX1004 at 1:33-50. As shown below, the *metal wire* is connected to a *third pad*. Additionally, recall a POSITA would have understood Sundaram’s pads to be *metal pad[s]* or would

have found obvious and been motivated to configure Sundaram's pads per Lin-191 to be *metal* with a reasonable expectation of success. See ¶¶ 163-167, incorporated herein. As such, Sundaram at FIG. 1a or Sundaram in view of Lin-191's metal pad teaches the *metal wire connected to a third metal pad of said third semiconductor chip*.



EX1004 at FIG. 1a.

a) Motivation to Combine Sundaram's Internal Embodiments

239. A POSITA would have found it obvious and been motivated to modify Sundaram's *third semiconductor chip* of FIG. 3 per FIG. 1a to comprise a *wire*

connected to a third metal pad of said third semiconductor chip. While Sundaram describes wire-bonded SIP structures as being limited in providing high bandwidth, a POSITA would have appreciated the benefits of the tradeoff of modifying Sundaram to wire bond (discussed below), for applications when high bandwidth is not required, which is envisioned by Sundaram. *EX1004* at 6:53-57 (“...the interconnect structure 100 is scalable (e.g., to decrease bandwidth speed) to meet the demands of specific applications.”).

240. First, wire bonds were known to be “a low-cost, stable technology for forming electrical connections” in chip packages. *EX1125* at [0108]. Additionally, prior to the alleged invention of the ‘306 Patent, wire bonding had “been used in integrated circuit packaging since the inception of IC technology” and thus “[w]ire bonding techniques and wire bonding machines” had been “refined to the point where wire bonds [were] relatively inexpensive and highly reliable.” *EX1120* at 1:9-13. As such, a POSITA would have appreciated the low-cost and high reliability of wire bonds in chip packaging technology and been motivated to implement such well-known technology into Sundaram’s chip package.

241. The modification is the application of a known technique (wire bonding) to a known device (Sundaram’s third semiconductor chip) ready for improvement to yield predictable results, i.e., Sundaram’s *third semiconductor chip*

being connected to interposer 105 with a *metal wire*). Because wire bonding had “been used in integrated circuit packaging since the inception of IC technology” and because wire bonding techniques were well-known, there would have been a reasonable expectation of success. *EX1120* at 1:9-13.

2. 17(b): “wherein said third semiconductor chip is a DRAM chip.”

242. Sundaram teaches memory chips and “smart and mobile phone applications[.]” *EX1004* at FIG.3, 6:37-38, 1:20-21. Lin-191 specifically teaches a “dynamic-random-access-memory (DRAM) chip.” *EX1004* at 6:34-39; *EX1005* at [0106]. A POSITA would have found it obvious that Sundaram’s memory chip can be a DRAM chip because Dram chip is one kind of memory chips e.g., when interconnect structure 100 is used in a cell phone. DRAM chips were “commonly used in...cellular phones, personal digital assistants (PDAs) and digital cameras.” *EX1121* at 1:18-21. Indeed, as early as 2003 it was known that DRAMS were “most suitable for cellular phones etc. because of low power consumption, the feasibility of large storage capacity, cheapness, and so on.” *EX1122* at 1:24-28. Given that Sundaram already contemplates chip packages for use in “cell phones,” a POSITA would have been motivated to configure Sundaram’s *third semiconductor chip* as a *DRAM chip* to achieve the aforementioned benefits of DRAM, i.e., low power consumption, large storage capacity, and cheapness. *EX1004* at 6:42-44.

Additionally, DRAM placement close to logic/CPU/GPU is critical because of strict skew and signal integrity requirements with the high-speed bus connections between the two chips.

243. The modification is the application of a known technique (a DRAM chip) to a known device (Sundaram's chip package) ready for improvement to yield the predictable result of a DRAM chip connected to a metal wire. The modification would have had a reasonable expectation of success because DRAM chips were ubiquitous and were known as "the most typical of randomly accessible semiconductor memory devices." *EX1123* at 1:12-13. Further, DRAM chips connected with wire bonds to other components in a chip package was also well known, further leading to a reasonable expectation of success. *See, e.g., EX1121* at FIG. 2J, 3:16-18, 3:55-59 ("first semiconductor die 24, a dynamic random access memory (DRAM) chip" is wire bonded by "connectors 30" to conductive traces.").

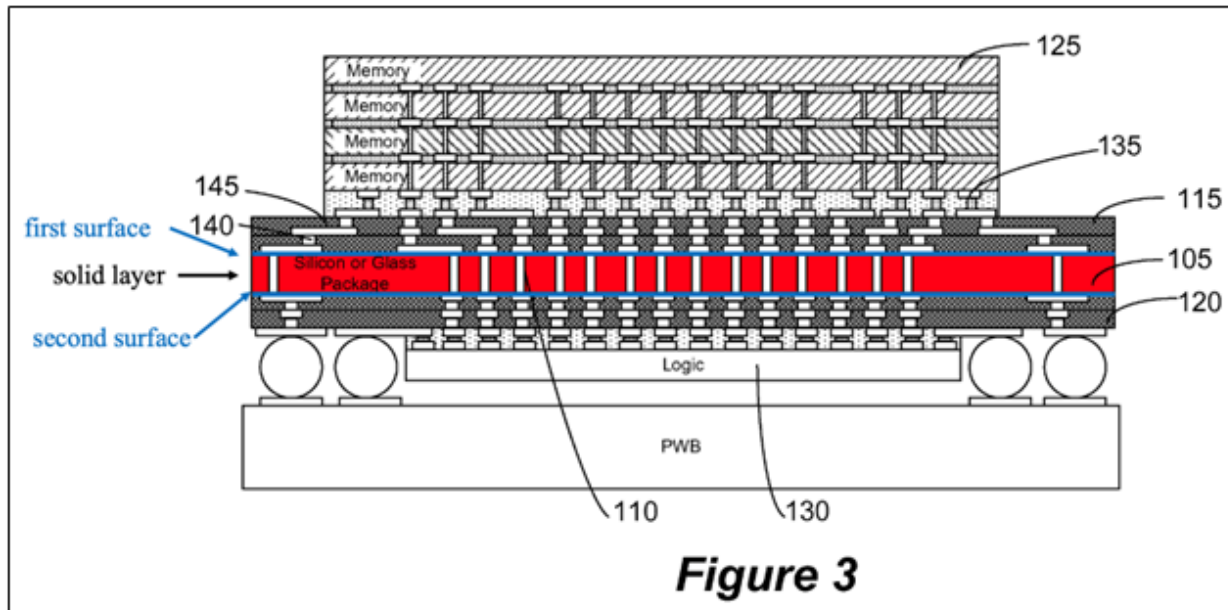
A. Claim 18

1. 18(Pre): "A chip package comprising"

244. *See* Claim 1(Pre), ¶ 125, incorporated herein.

2. 18(a): "a solid layer having a first surface and a second surface opposite to said first surface,"

245. See Claim 1(a), ¶¶ 126-127, incorporated herein. Claim 18's mapping reverses Sundaram's mapped *first* and *second* surfaces and *over/under* directions relative to Claims 1 and 10's mapping.



EX1004 at FIG. 3.

3. 18(a)(i): “wherein said solid layer comprises a compound of silicon and oxygen,”

246. See Claim 1(a)(i), ¶¶ 128-129, incorporated herein.

4. 18(a)(ii): “wherein said solid layer has a thickness between 50 and 150 micrometers;”

247. See Claim 1(a)(ii), ¶¶ 130-131, incorporated herein.

5. 18(a)(iii): “wherein said solid layer comprises a first region and a second region between said first region and a first edge of said solid layer;”

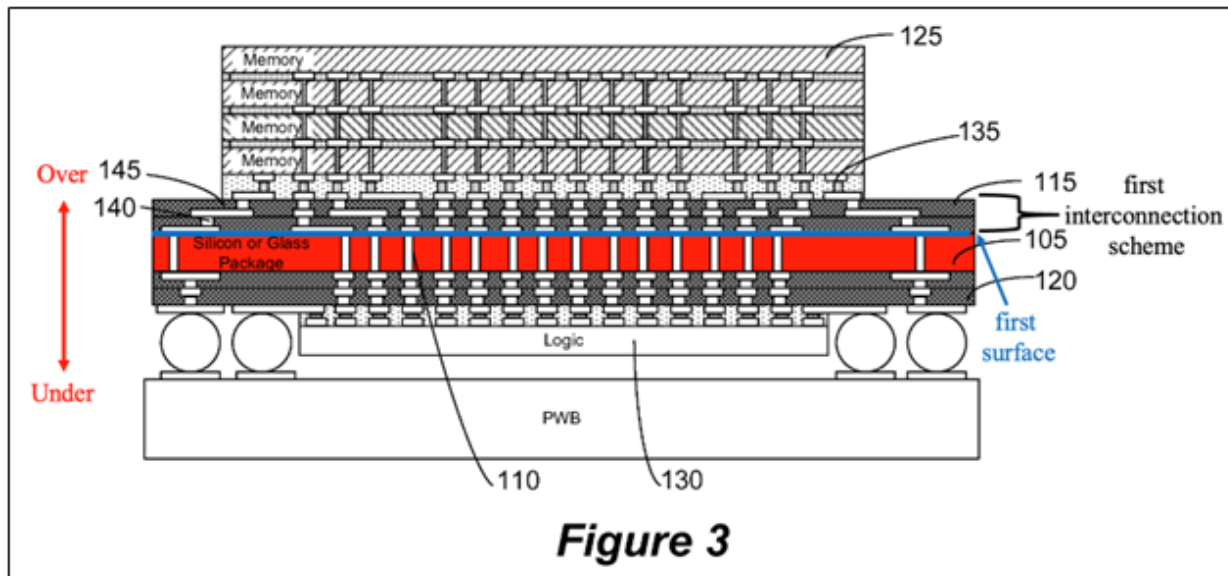
248. See Claim 1(a)(iii), ¶ 132, incorporated herein.

6. *18(b): “a plurality of copper posts in a plurality of through holes in said second region respectively,*

249. See Claims 1(b)-1(b)(i), 10(b), ¶ 133-134, 210 incorporated herein.

7. *18(c): “a first interconnection scheme over said first surface,”*

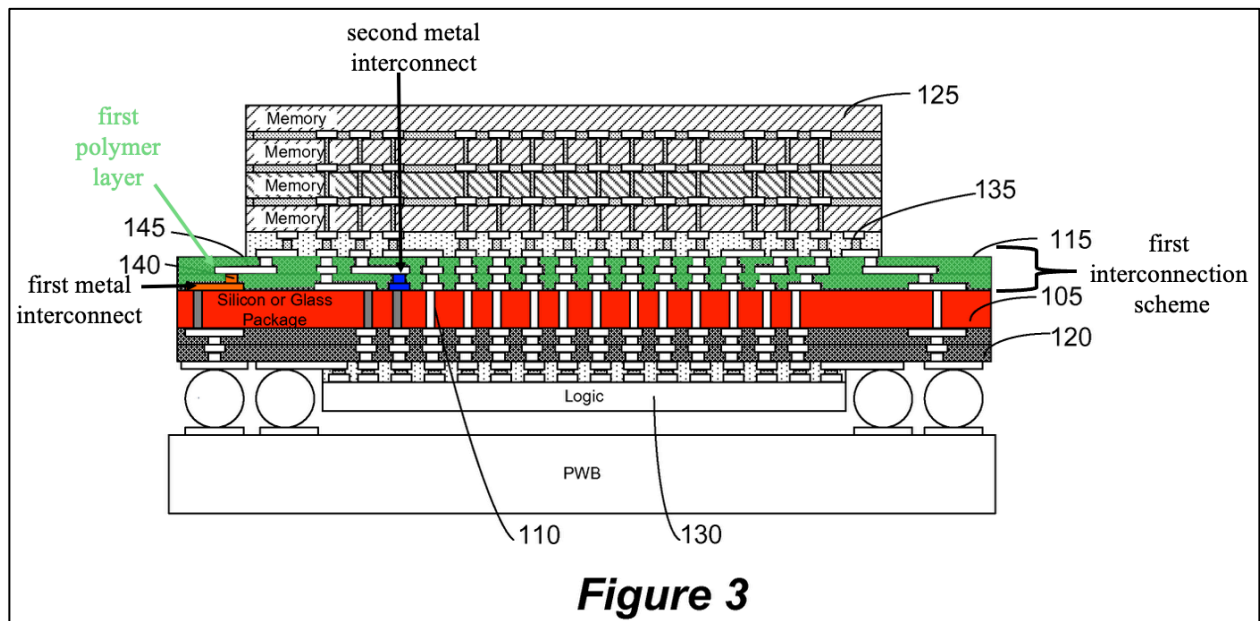
250. See Claim 1(c), ¶ 138. As discussed, Sundaram teaches that “electronic devices having different I/O pad layouts and sizes can also be connected through the use of blind vias 140 and conductor traces 145 defined within **polymer-metal redistribution layers** deposited on the first side 115 and second side 120 of the interposer 105.” *EX1004* at 6:32-67. Additionally, Sundaram teaches “die pads 135 that are formed on the first 115 and second sides 120 of interposer 105 can electrically connect devices[.]” *EX1004* at 6:29-31. Because the blind vias 140 and conductor traces 145 within polymer-metal redistribution layers connect “electronic devices having different I/O pad layouts and sizes[.]” and because the die pads 135 formed on the second side 120 “electrically connect devices[.]” the vias 140, conductor traces 145, die pads 135, and polymer layer on first side 115 (*first surface*) are a *first interconnection scheme over said first surface*. In other words, because vias 140 and traces 145 in the polymer layer and die pads 135 connect (i.e., *interconnect*[]) devices 125 and 130, they collectively form an *interconnection scheme*.



EX1004 at FIG. 3.

8. **18(c)(i):** “wherein said first interconnection scheme comprises first and second metal interconnects over said first surface, and a first polymer layer over said first and second metal interconnects,”

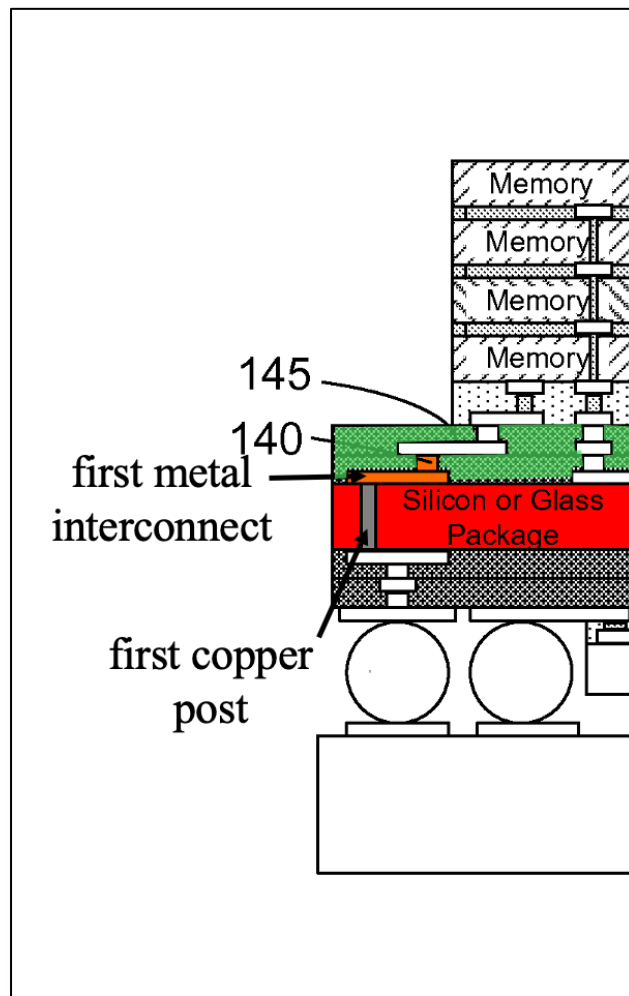
251. See Claim 1(c)(i), ¶¶ 141-143, incorporated herein. *First and second metal interconnects* are formed over said first surface by conductive traces 145 and blind vias 140. Additionally, a *first polymer layer* (green) is over said first and second metal interconnects, as shown:



EX1004 at FIG. 3 (excerpt).

9. **18(c)(ii): “wherein said first metal interconnect is connected to a first copper post of said plurality of copper posts,”**

252. See Claim 1(c)(ii), ¶ 146. As shown, Sundaram’s first metal interconnect is connected to a first copper post of said plurality of copper posts:



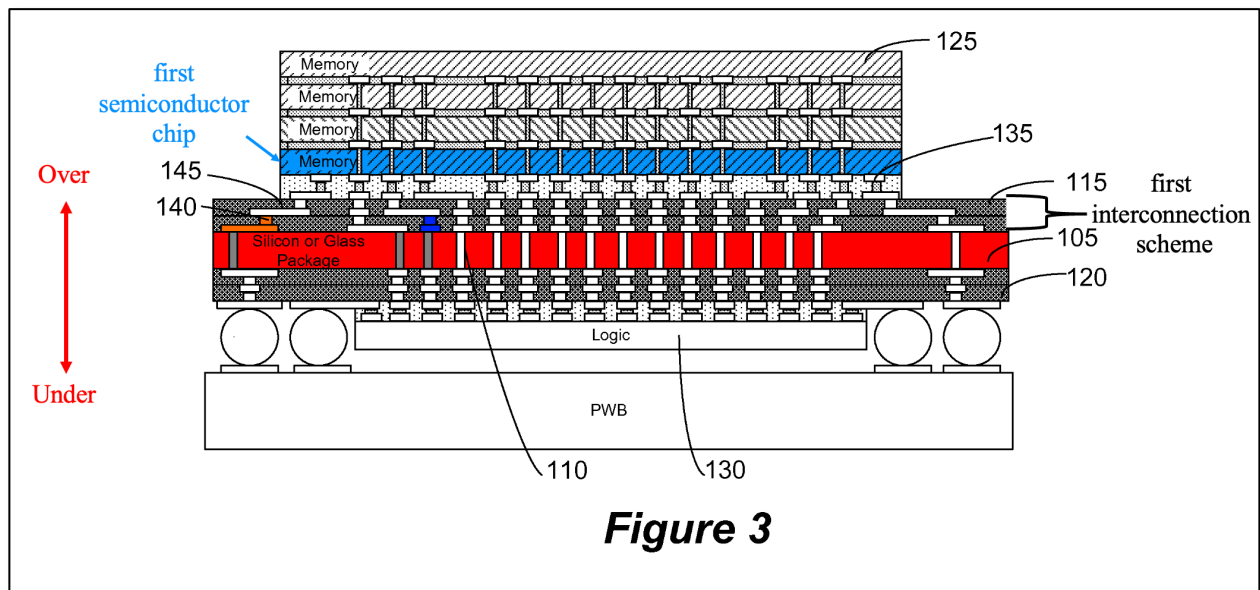
EX1004 at FIG. 3.

10. 18(c)(iii): “wherein said first metal interconnect comprises a first metal layer and a first copper layer over said first metal layer;”

253. See Claim 1(c)(iii), ¶ 147-148, incorporated herein. For the same reasons described above at Claim 1(c)(iii), Sundaram’s *first metal* interconnect as mapped in Claim 18 comprises a *first metal layer and a first copper layer over said first metal layer*.

11. 18(d): “a first semiconductor chip over said first interconnection scheme,”

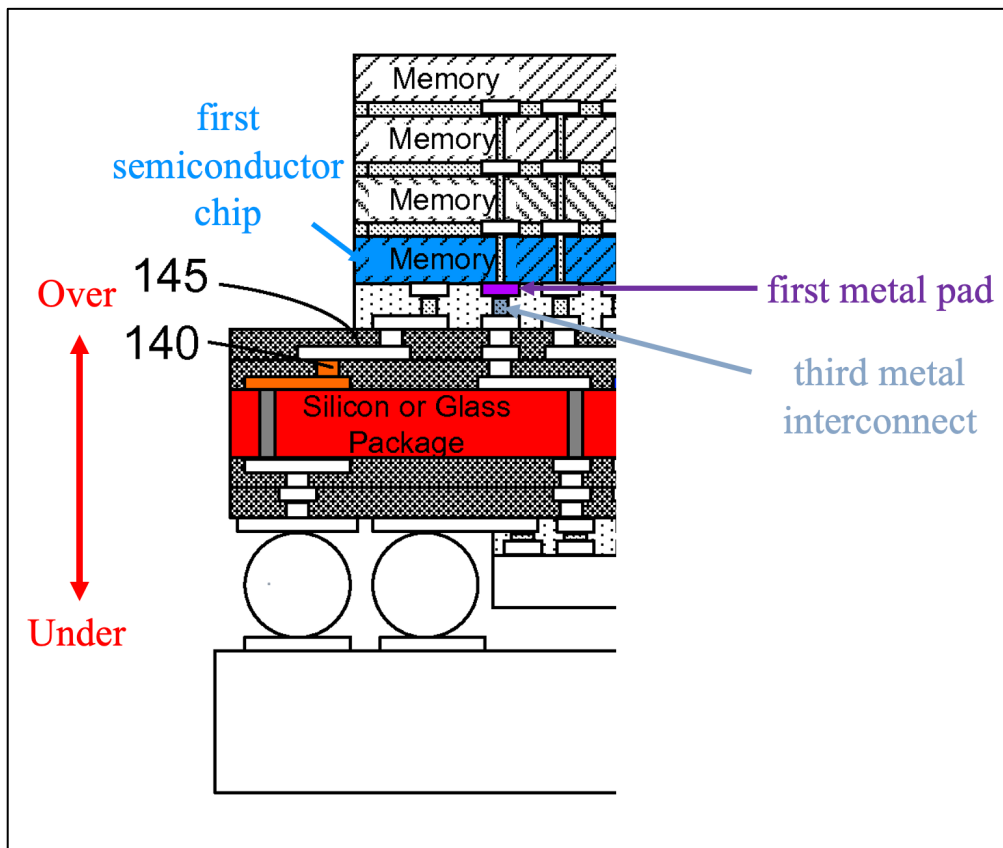
254. Sundaram’s teaches a first electronic device 125 which “can be single or stacked memory IC device.” *EX1004* at 6:37-39. Thus, a first IC device in Sundaram’s chip stack is a *first semiconductor chip over said first interconnection scheme*:



EX1004 at FIG. 3.

12. 18(d)(i): “wherein said first semiconductor chip comprises a third metal interconnect under a first metal pad of said first semiconductor chip,”

255. See Claim 1(e)(ii), ¶¶ 163-166, incorporated herein. As shown, the *third metal interconnect* is under the *first metal pad* of said first semiconductor chip.



EX1004 at FIG. 3 (excerpt).

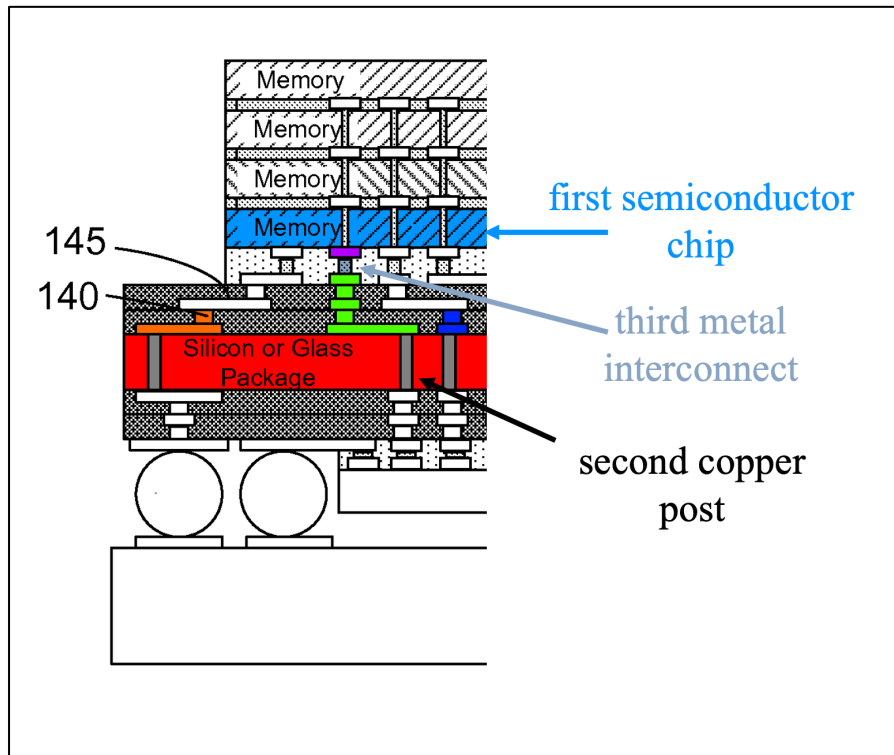
13. 18(d)(ii): “wherein said third metal interconnect comprises a second metal layer under said first metal pad and a second copper layer under said second metal layer, wherein said second copper layer has a thickness between 5 and 30 micrometers,”

256. See Claim 1(e)(iii), ¶¶ 168-176, incorporated herein. Claim 18(d)(ii)’s *second metal layer* and *second copper layer* correspond to Claim 1(e)(iii)’s *third metal layer* and *third copper layer*, respectively. I note that relative to Claim 1(e)(iii), Claim 18(d)(ii) requires the *second copper layer* to be **under** said *second metal layer* whereas Claim 1(e)(iii) requires the *third copper layer* to be **over** said *third metal*

layer. Thus, because (1) Claim 18's over/under directions are inverted relative to Claim 1, and (2) the orientation of second copper layer in Claim 18 (i.e., under said second metal layer) is inverted relative to the third copper layer in Claim 1 (i.e., over said third metal layer), the above-described combination of Sundaram-Lin-191 yields wherein said third metal interconnect comprises a second metal layer under said first metal pad and a second copper layer under said second metal layer, wherein said second copper layer has a thickness between 5 and 30 micrometers.

14. 18(d)(iii): “wherein said first semiconductor chip is coupled to a second copper post of said plurality of copper posts through said third metal interconnect;”

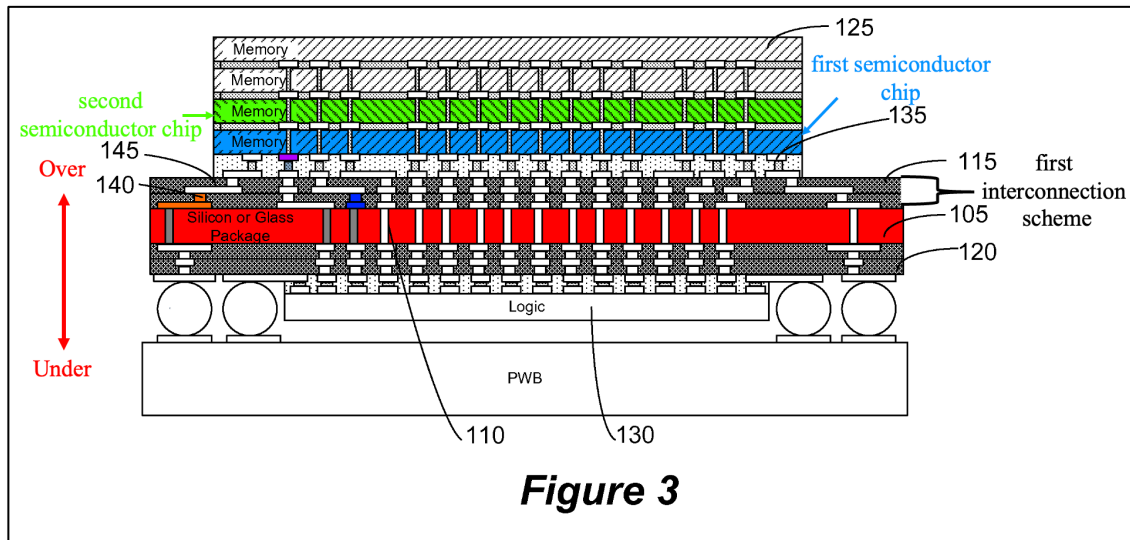
257. See Claim 1(e)(iv), ¶ 177, incorporated herein. As shown, the *first semiconductor chip is coupled to a second copper post of said plurality of copper posts through said third metal interconnect* and through the metal interconnects highlighted in green:



EX1004 at FIG. 3 (excerpt).

15. 18(e): “a second semiconductor chip over said first interconnection scheme,”

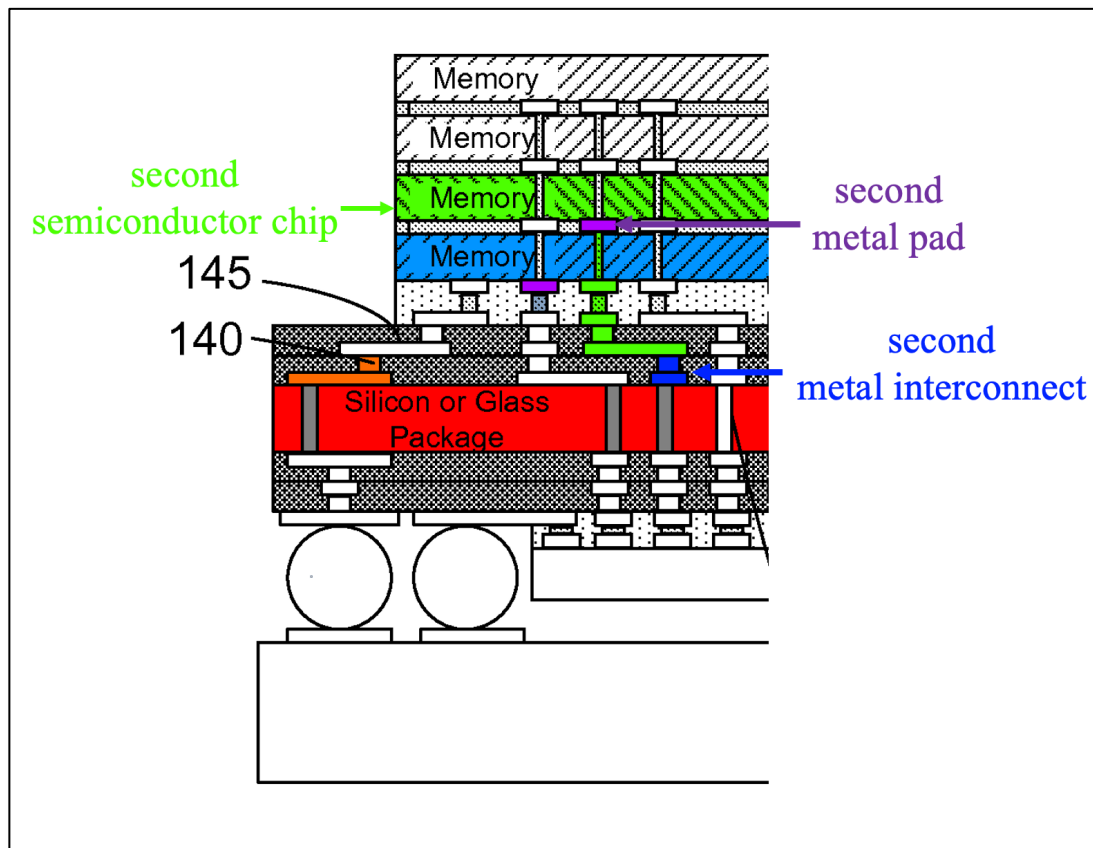
258. As shown, a second chip in Sundaram’s chip stack/first electronic device 125 is a *second semiconductor chip over said first interconnection scheme*:



EX1004 at FIG. 3.

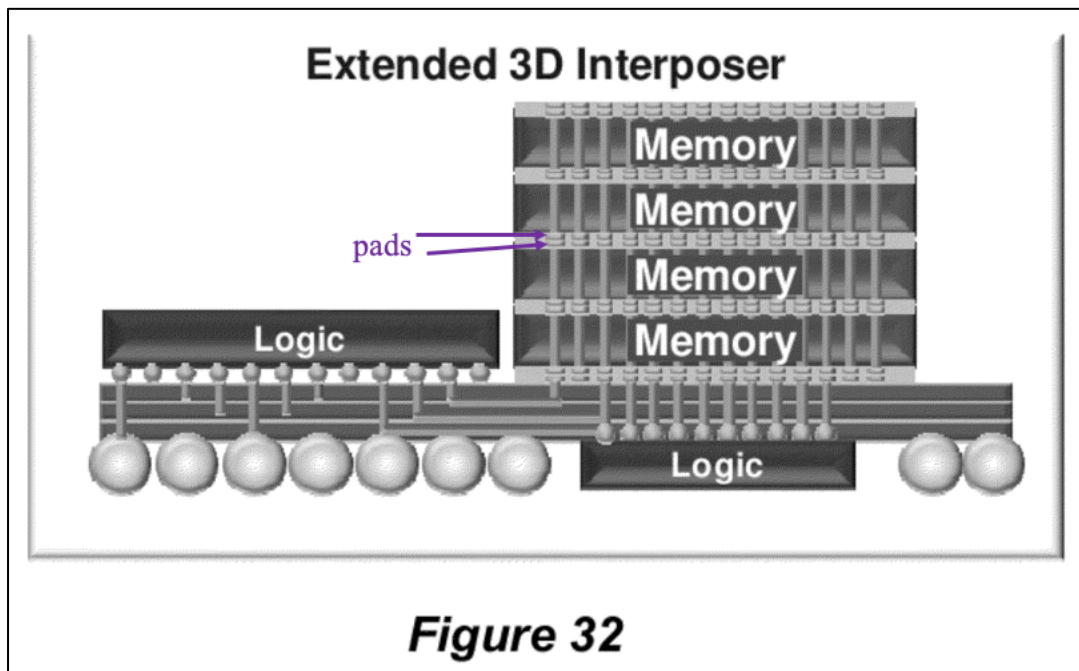
16. 18(e)(i): “wherein said second semiconductor chip comprises a second metal pad coupled to said second metal interconnect;”

259. As discussed, a POSITA would have understood Sundaram’s pads in first electronic device 125 to be *metal pad[s]* or a POSITA would have been motivated and found it obvious to implement Sundaram’s pads as *metal*. See ¶¶ 163-167. Accordingly, a *second metal pad* of Sundaram’s *second semiconductor chip* is shown below as *coupled to said second metal interconnect* through each of the interconnects highlighted in green:



EX1004 at FIG. 3.

260. Additionally or alternatively, FIG. 32 teaches a *second metal pad*. FIG. 32 depicts a chip stack similar to FIG. 3's where each chip has a distinct metal pad. A POSITA would have found it obvious, been motivated, and had a REOS in modifying FIG. 3's chip stack per FIG. 32's to provide each chip with its own set of pads, so that each chip has top and bottom pads connected to one another as each chip must include pads on its surface to provide connection to other electrical components in the chip package. The modification is a straightforward implementation detail to FIG. 3's chip stack.

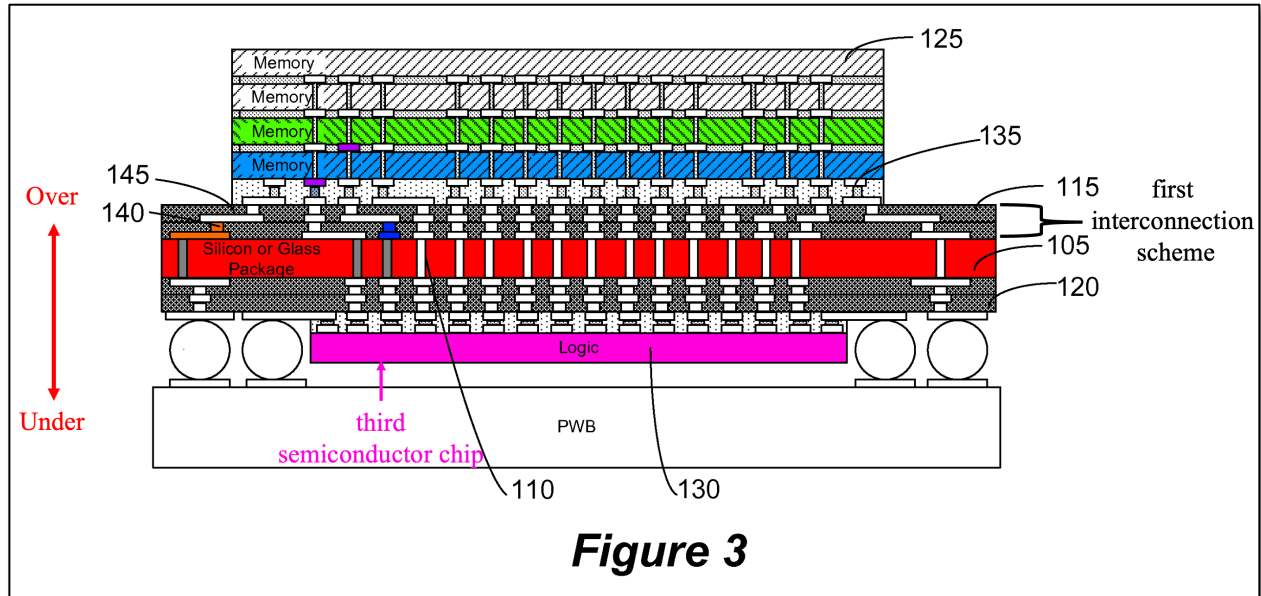


EX1004 at FIG. 32.

17. 18(f): “a third semiconductor chip under said first interconnection scheme; and”

261. Sundaram’s second electronic device 130, which may be a “logic IC device or devices” is a *third semiconductor chip under said first interconnection*

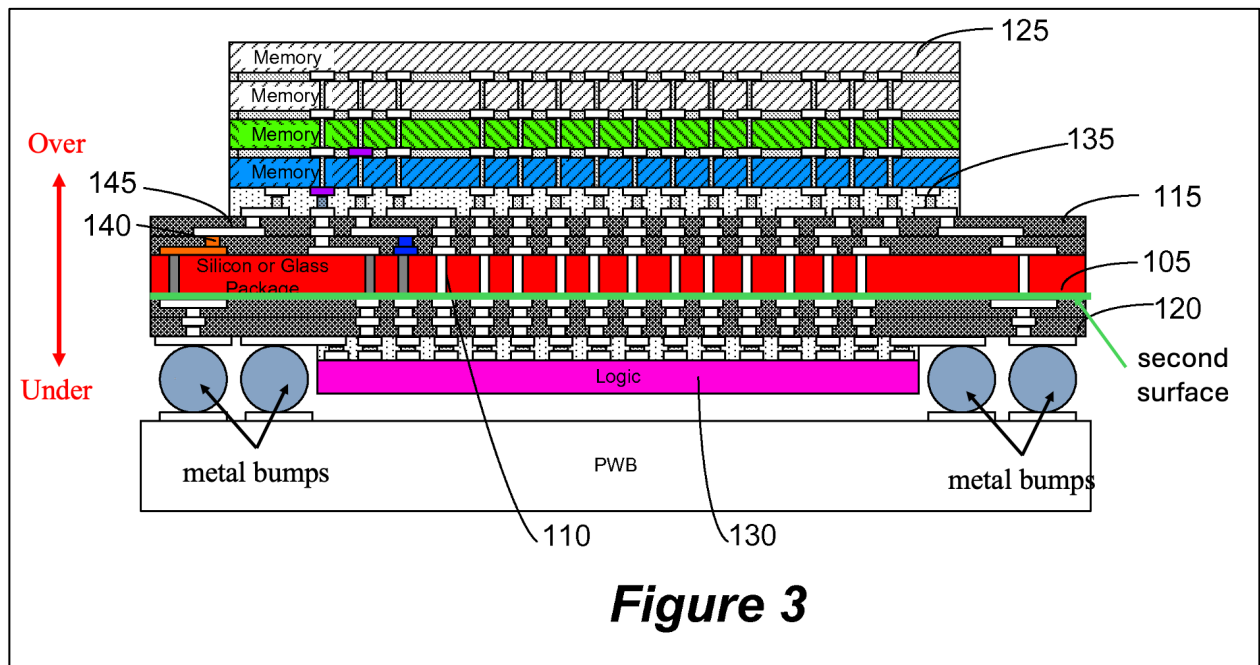
scheme:



EX1004 at FIG. 3; EX1004 at 6:38-39.

18. 18(g): “a plurality of metal bumps under said second surface, wherein one of said plurality of metal bumps comprises a tin-containing layer.”

262. Recall that Sundaram teaches “copper bumps with solder caps” (i.e., a metal bumps). EX1004 at 6:29-31; ¶ 149. As shown below, Sundaram’s chip package comprises a plurality of metal bumps under said second surface:



EX1004 at FIG. 3.

263. Sundaram further teaches that the *metal bumps* comprise a *tin-containing* layer. See ¶ 150; EX1004 at 6:29-31. Additionally or alternatively, as I discussed at Claim 1(d)(i), a POSITA would have found it obvious and been motivated to modify Sundaram's bumps per Lin-191 to comprise a *tin-containing* layer. See ¶¶ 150-158, incorporated herein. Thus, *one of said plurality of metal bumps* comprises a *tin-containing* layer.

B. Claim 19: "The chip package of claim 18, wherein said compound comprises a SiO_2 compound."

264. See Claim 5, ¶ 196, incorporated herein.

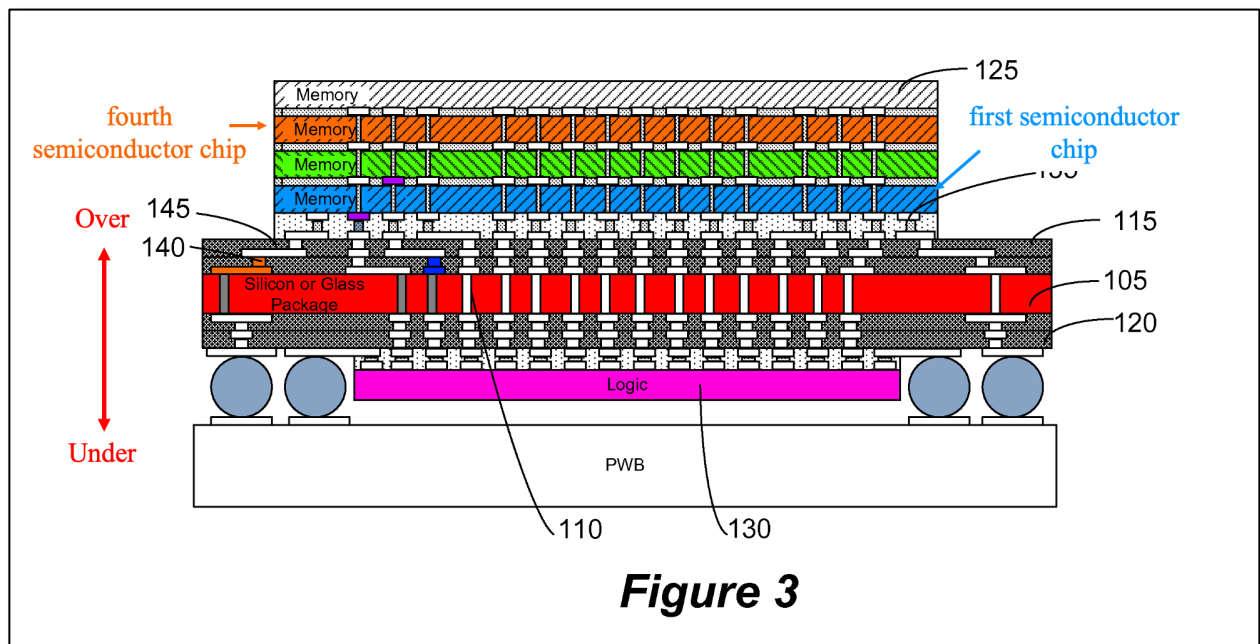
- C. **Claim 20:** “The chip package of claim 18, wherein said solid layer further comprises a third region opposite to said second region, wherein said third region is between said first region and a second edge of said solid layer, wherein said plurality of copper posts in said plurality of through holes in said third region respectively.”

265. See Claim 7, ¶ 201, incorporated herein.

D. **Claim 21**

1. **21(a):** “The chip package of claim 18, further comprising a fourth semiconductor chip over said first semiconductor chip,”

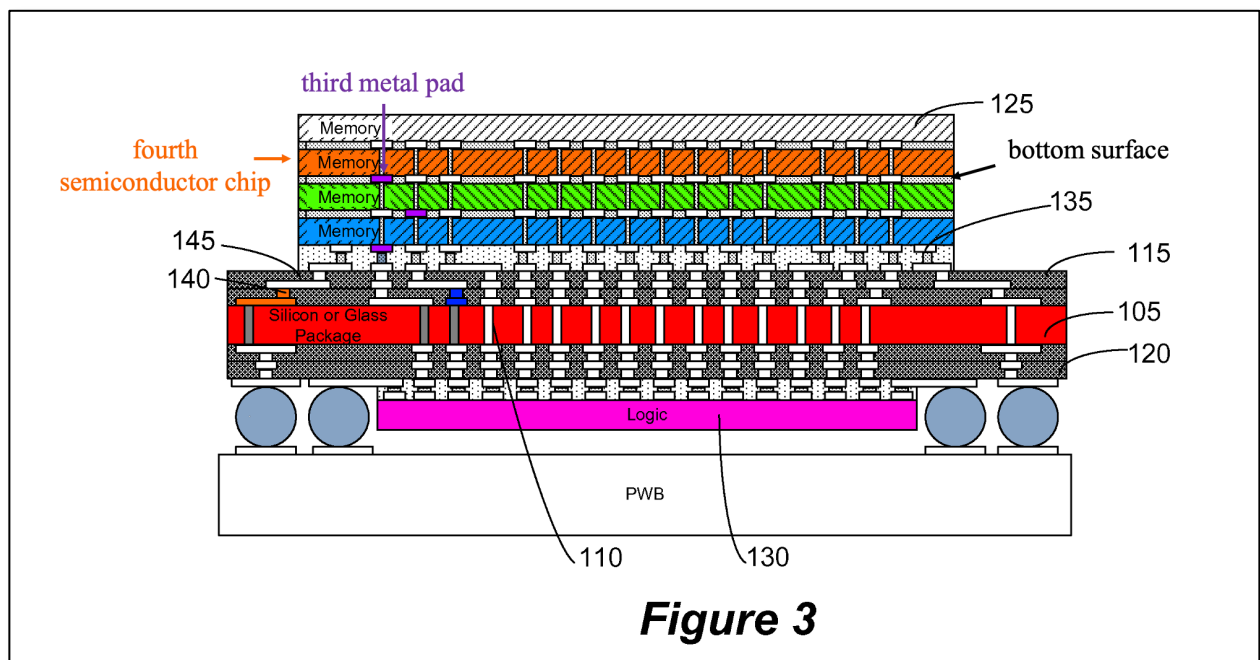
266. As shown below, Sundaram’s chip stack 125 includes a third chip that is a *fourth semiconductor chip over said first semiconductor chip*. The *fourth semiconductor chip* is over the *first semiconductor chip* as depicted by the red arrow indicating the over/under directions:



EX1004 at FIG. 3.

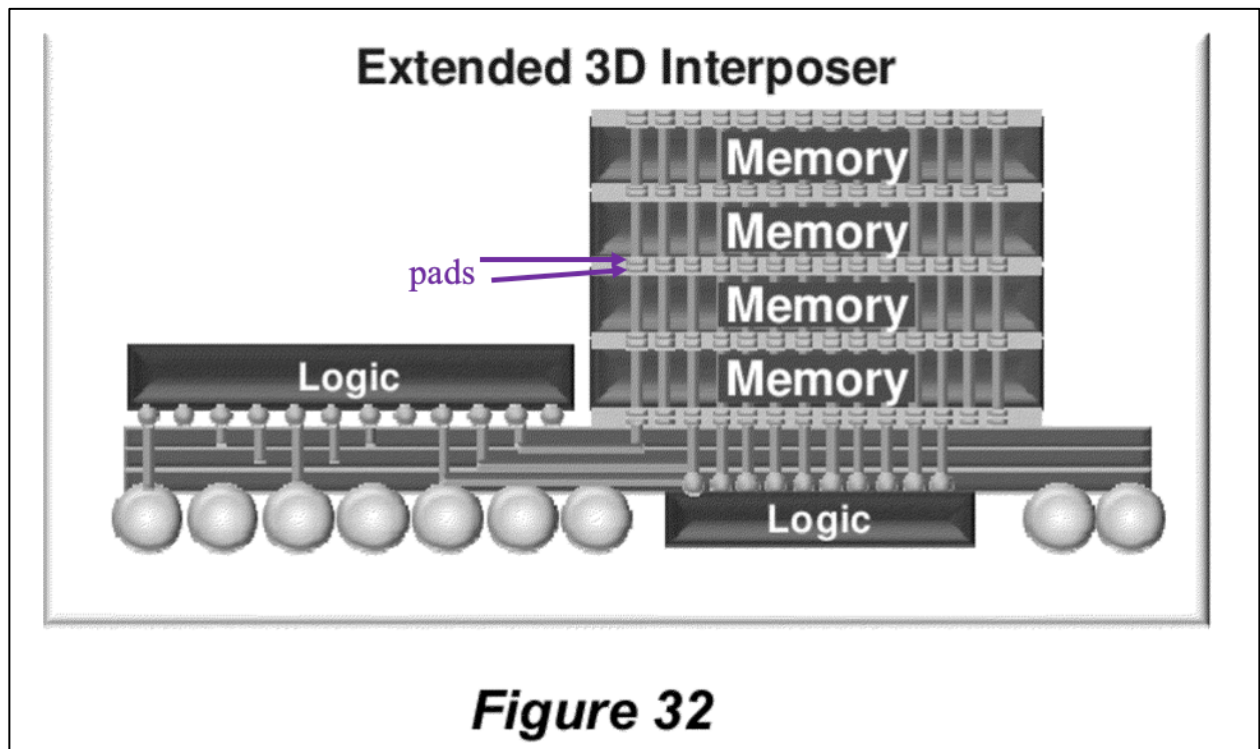
2. 21(b): “wherein said fourth semiconductor chip comprises a third metal pad at a bottom surface of said fourth semiconductor chip,”

267. As discussed at claim 1(e)(ii), a POSITA would have understood Sundaram’s pads in the chip stack 125 to be *metal pad[s]* or would have been motivated, found it obvious, and had a reasonable expectation of success in modifying Sundaram’s pads to be *metal* per Lin-191. See ¶¶ 163-167. As such, Sundaram alone or Sundaram-Lin-191 teaches a *third metal pad at a bottom surface* of the *fourth semiconductor chip*:



EX1004 at FIG. 3.

268. FIG. 32 depicts a chip stack similar to FIG. 3’s where each chip has a distinct metal pad:



EX1004 at FIG. 32.

269. A POSITA would have found it obvious and been motivated to modify FIG. 3's chip stack per FIG. 32 such that each chip in FIG. 3's stack comprises its own set of metal pads. The modification is a straightforward implementation detail to FIG. 3's chip stack as connecting TSVs in a chip stack with a metal pad on either end was a common technique. *See, e.g., EX1126* at FIG. 2, 6:16-22.

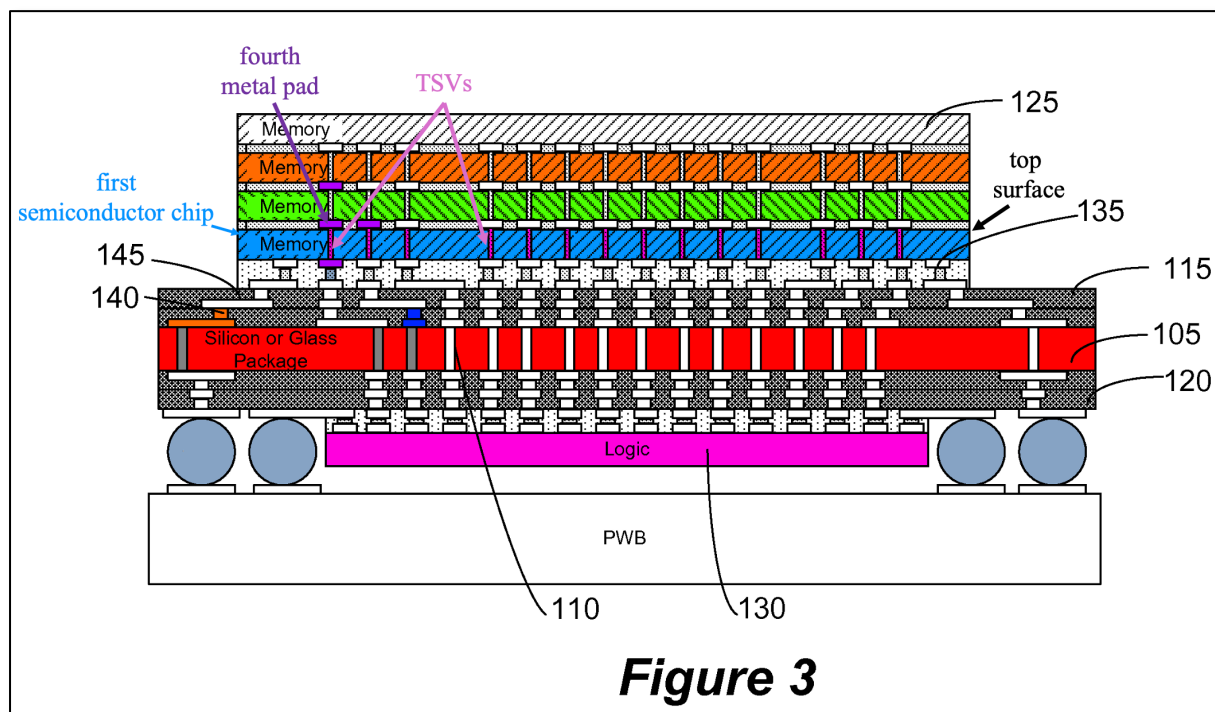
270. The modification is the application of a known technique (providing each chip with its own set of metal pads) to a known device (Sundaram's chip stack) ready for improvement to yield the predictable results. The modification is also merely an implementation detail. Further, there would have been a reasonable

expectation of success at least because Sundaram is already familiar with chips having their own set of metal pads, as evidenced by FIG. 32, and because metal pads and methods of forming metal pads were well-known. *See, e.g., EX1005* at [0383]. Indeed, semiconductor chips were regularly manufactured with metal pads formed on the periphery. *EX1095* at (“I/O terminals were **traditionally** formed by way of **metal pads** along the periphery of an IC.”). Because the standard method of manufacturing chips included forming metal pads along the periphery, a POSITA would have found it obvious to include metal pads on either surface of each chip in the chip stack of FIG. 3., thereby ensuring electrical communication via such I/O terminals. For the same reason, i.e., because that is how chips were formed, a POSITA would have had a reasonable expectation of success.

3. *21(c): “wherein said first semiconductor chip further comprising a plurality of through-silicon-via metal layers and a fourth metal pad at a top surface of said first semiconductor chip,”*

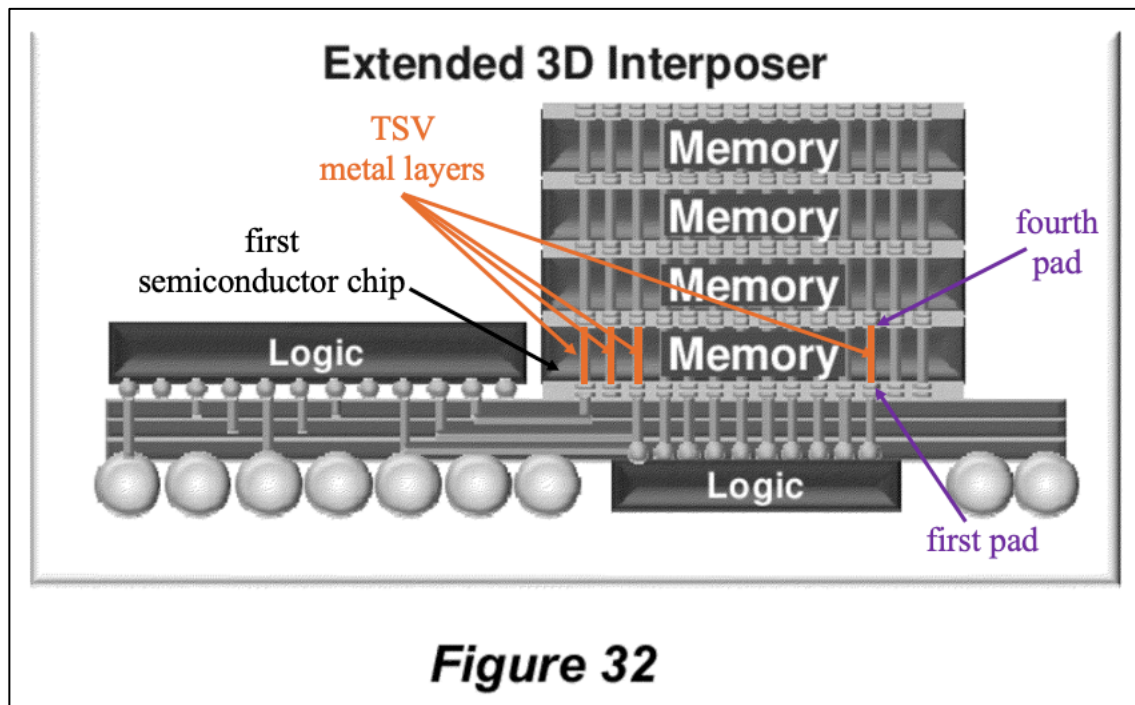
271. Sundaram teaches TSV metal layers connecting metal pads. For example, with respect to FIG. 1d, Sundaram describes “3D ICs with complex and expensive through silicon vias (TSVs)[,]” demonstrating Sundaram’s familiarity and depiction of TSVs. *EX1004* at 1:38-41, FIG. 1d, FIG. 32, *see also* 1:62-67. Further, Sundaram was already familiar with *TSV metal layers*, teaching “TSVs in...CMOS grade Si” filled with “Cu[.]” *EX1004* at 11:15-20, *see also* 14:13-34, 15:7-8 (“A DC

electroplating process was then used to plate copper and fill the TSVs.”), FIG. 34. Thus, a POSITA would understand the TSV’s as shown in FIG. 3 to be *through-silicon-via metal layers*. Another of Sundaram’s or Sundaram-Lin-191’s *metal pad[s]* is a *fourth metal pad at a top surface of said first semiconductor chip*. See ¶¶ 163-167, 267.



EX1004 at FIG. 3.

272. Additionally to FIG. 3’s teachings, FIG. 32 teaches a *fourth metal pad on a top surface* of a first semiconductor chip:

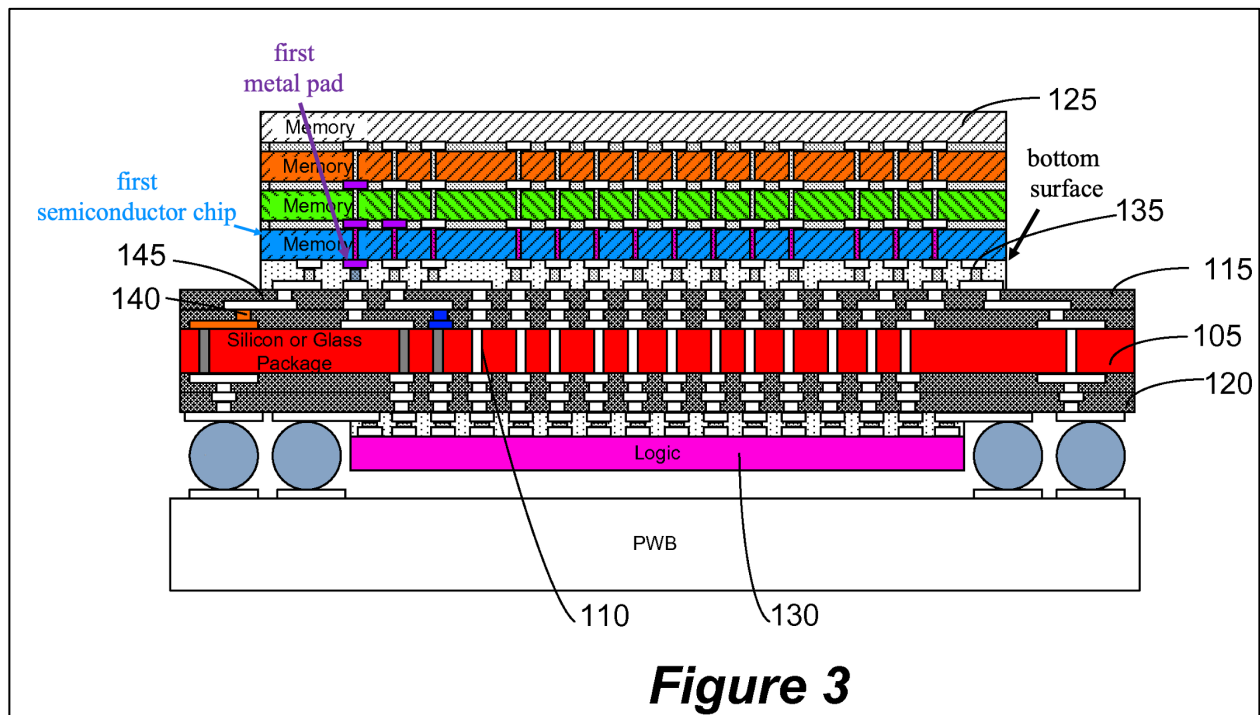


EX1004 at FIG. 32.

273. As discussed, a POSITA would have been motivated, found it obvious, and had a reasonable expectation of success in configuring the FIG. 3 chip stack such that each chip had metal pads on top and bottom surfaces. See ¶¶ 267-270. Accordingly, Sundaram teaches a fourth metal pad at a top surface of said first semiconductor chip.

4. 21(d): “wherein said first metal pad is at a bottom surface of said first semiconductor chip,”

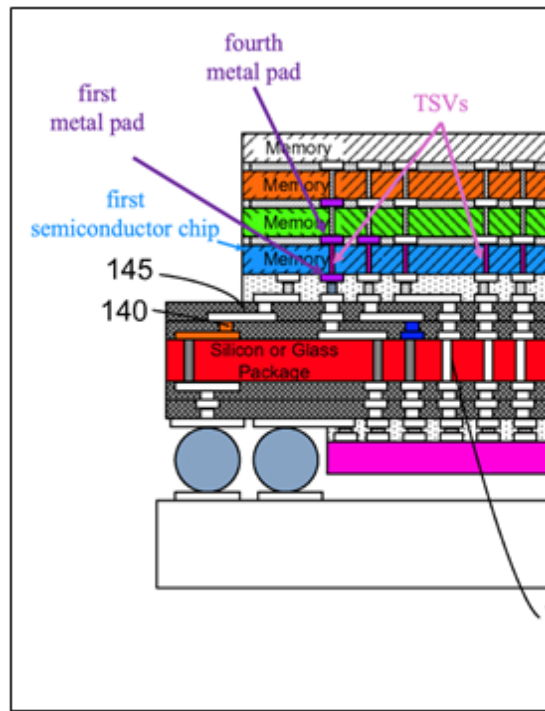
274. The first metal pad as identified above at claim 18(d)(i) is at a bottom surface of said first semiconductor chip, shown below. See ¶ 255.



EX1004 at FIG. 3.

5. 21(e): “wherein said first metal pad is coupled to said fourth metal pad through one of said plurality of through-silicon-via metal layers,”

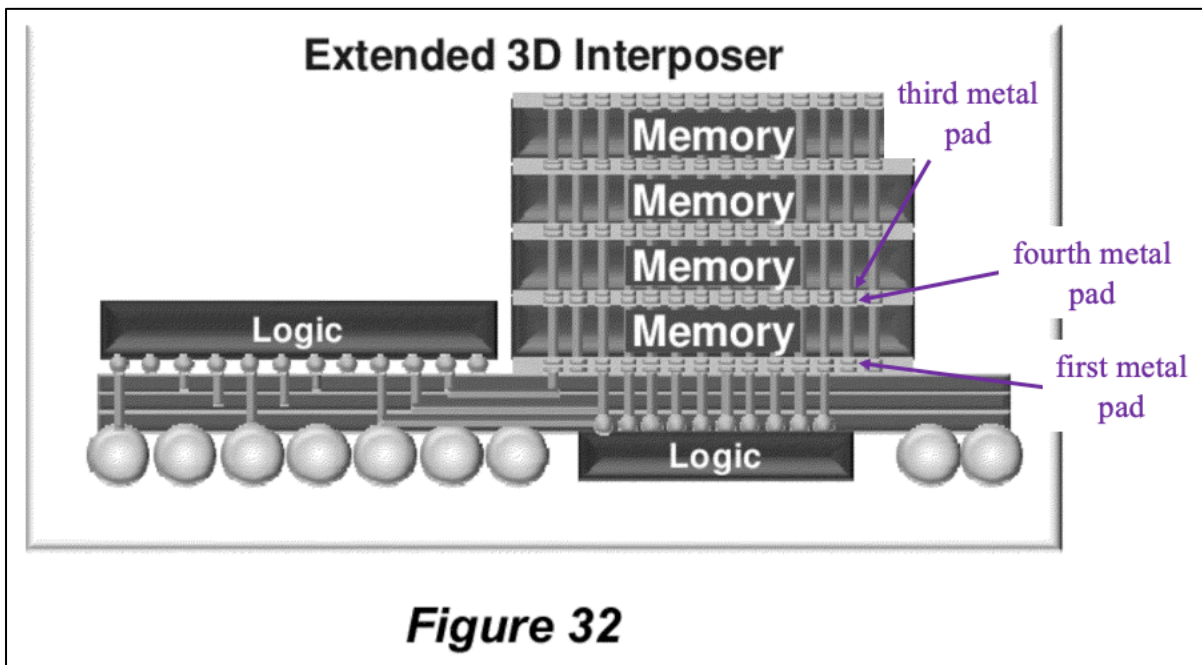
275. As shown, the first metal map is coupled to said fourth metal pad through one of said plurality of through-silicon-via metal layers:



EX1004 at FIG. 3 (excerpt).

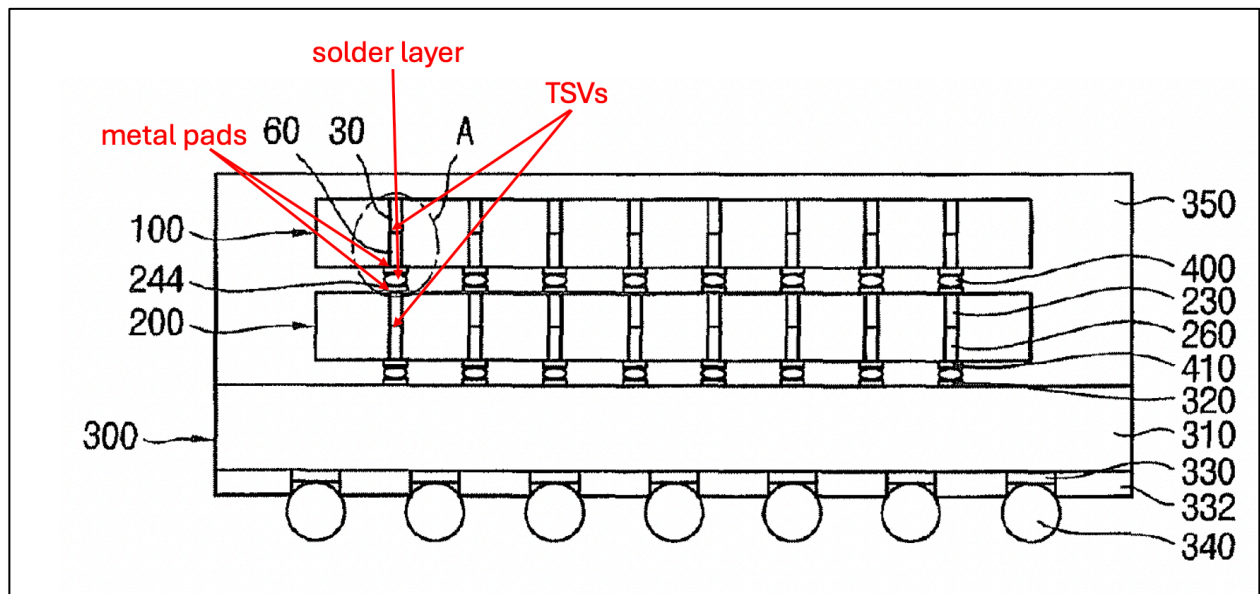
6. *21(f): “wherein said third metal pad is coupled to said fourth metal pad through a solder layer.”*

276. FIG. 32’s memory stack illustrates pads connected to one another, and Sundaram further teaches “die pads 135...can electrically connect devices using **solder**, copper bumps with **solder** caps....” *EX1004* at 6:29-34.



EX1004 at FIG. 32.

277. A POSITA would have understood chip pads on devices 125, 130 likewise electrically connect using solder because connecting metal pads using solder bumps was standard practice. For example, Lee depicts a chip stacking in which each chip has its own set of metal pads connecting TSVs through a solder layer, shown below, which demonstrates the standard practice of connecting metal pads of chips by a solder layer.



EX1126 at FIG. 2, 6:16-22, 7:40-42.

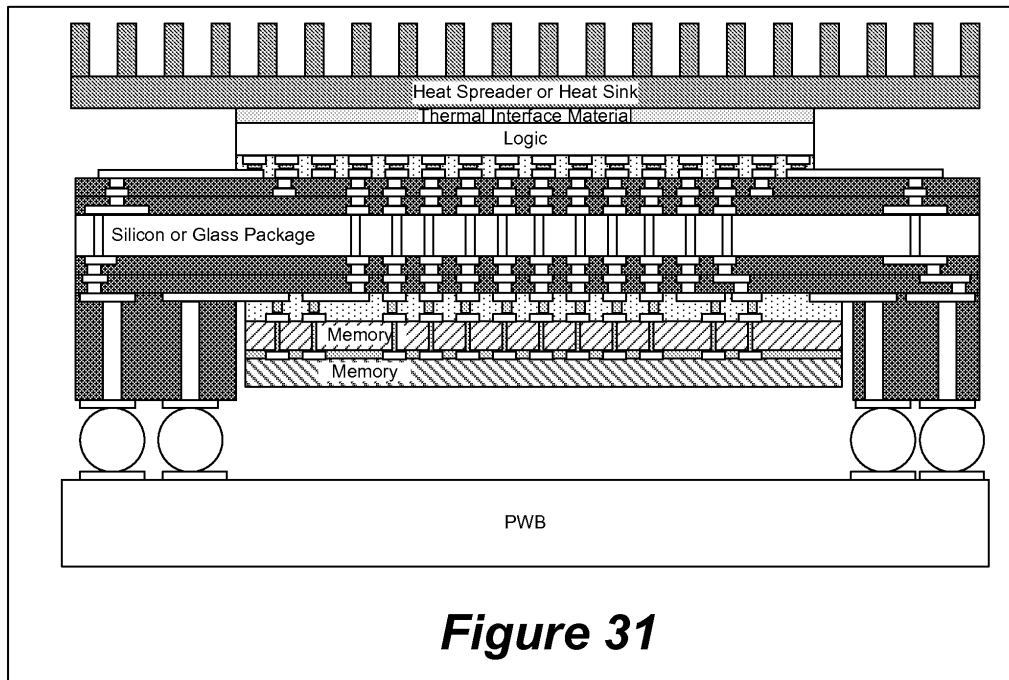
278. A POSITA would have found it obvious, been motivated, and had a reasonable expectation of success in combining Sundaram's internal embodiments to *couple[]* Sundaram-Lin-191's *third metal pad* and *fourth metal pad through a solder layer*, teaching Claim 21(f). A POSITA would have recognized that including a solder layer between the metal pads of Sundaram's chip stack would have provided the benefit of self-alignment of the metal bumps, thereby reducing the risk of misaligned pad-to-pad bonding between the chips. Indeed, it was known when forming metal bumps, "self-alignment" occurs which is "such an effect that the electronic component is lifted by surface tension and stress of the molten solder, and then self-aligns itself on the mounted position on the board by restitution from the stress." EX1083 at [0003]. A POSITA would have had the knowledge and skillset to

successfully implement such solder layers between the metal pads, including any necessary corresponding changes, such as implementing an underfill material which was standard, well-established practice. Additionally, a POSITA would have recognized the modification would have been standard practice, as the alternative to solder-based interconnection between stacked chips was bumpless Cu-Cu hybrid bonding. Bumpless pad-to-pad bonding required more expensive high precision processing to obtain ultra-flat, ultra-clean copper interfaces, and was only used for applications requiring extremely high I/O density.

279. As such, a POSITA would have been motivated to achieve such a benefit (self-alignment) by *coupl[ing]* the *third metal pad* to the *fourth metal pad through a solder layer*. The modification is the combination of known prior art elements (solder connections for chip pads) according to known methods to yield predictable results. The modification would have advantageously provided Sundaram with a good electromechanical connection between chips, which would have had a reasonable expectation of success because such was a common method of connecting chips, as described above. *See* ¶ 277. Methods of forming solder bumps/layers were also well known, further contributing to a reasonable expectation of success. *See* ¶¶ 71-76.

E. Claim 22: “The chip package of claim 18, wherein said first semiconductor chip is a graphics-processing-unit (GPU) chip.”

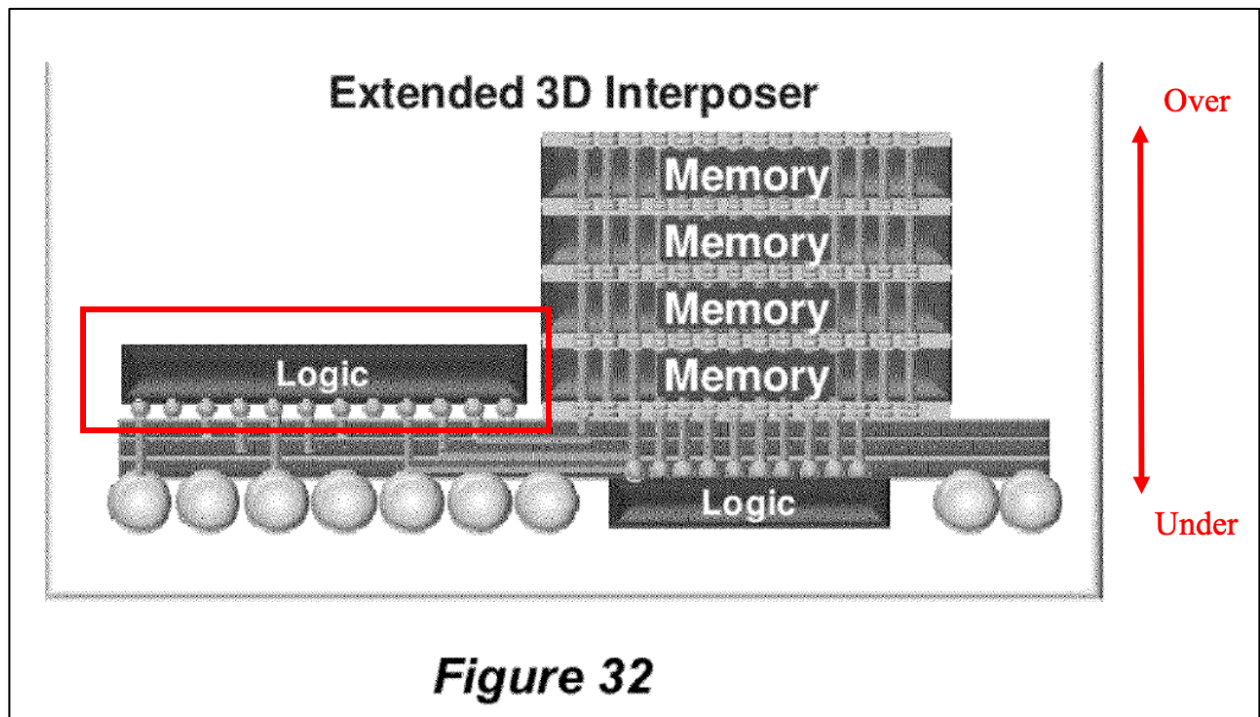
280. Sundaram teaches the 3D interconnect structure “can be used for...graphics.” *EX1004* at Abstract. Lin-191 teaches a semiconductor chip 160 that is a “graphics-processing-unit (GPU) chip.” *EX1005* at [0382]. As I discussed above at Claim 2, a POSITA would have found it obvious and been motivated to modify Sundaram’s *first semiconductor chip* to have a GPU circuit block with a reasonable expectation of success. See ¶¶ 179-180. For the same MTCs and with the same reasonable expectation of success, a POSITA would have found it obvious and been motivated to implement Sundaram’s *first semiconductor chip* as a *GPU chip*. See ¶¶ 179-180, incorporated herein Further, as discussed, Sundaram already contemplates “high power logic component[s]” over the *first interconnection scheme* as depicted in FIG. 31, further leading to a reasonable expectation of success.



EX1004 at FIG. 3.

F. Claim 23: “The chip package of claim 18, wherein said second semiconductor chip is a logic chip.”

281. As shown below, Sundaram teaches a *logic chip* including a *logic chip* over the interconnection scheme:



EX1004 at FIG. 32, Abstract.

a) Motivation to Combine Sundaram's Internal Embodiments

282. A POSITA would have been motivated and found it obvious to modify Sundaram's FIG. 3 embodiment per FIG. 32's teachings to have a *second semiconductor chip that is a logic chip*. The modification would have predictably improved Sundaram's chip package by providing additional computational power via the *logic chip*, as logic chips were known to "perform arithmetic computation functions[.]". EX1124 at 1:21-22. Thus, by providing the *second semiconductor chip* as additional logic chip, the processing power available in Sundaram's chip package would be favorably increased, such that more functions would be carried out

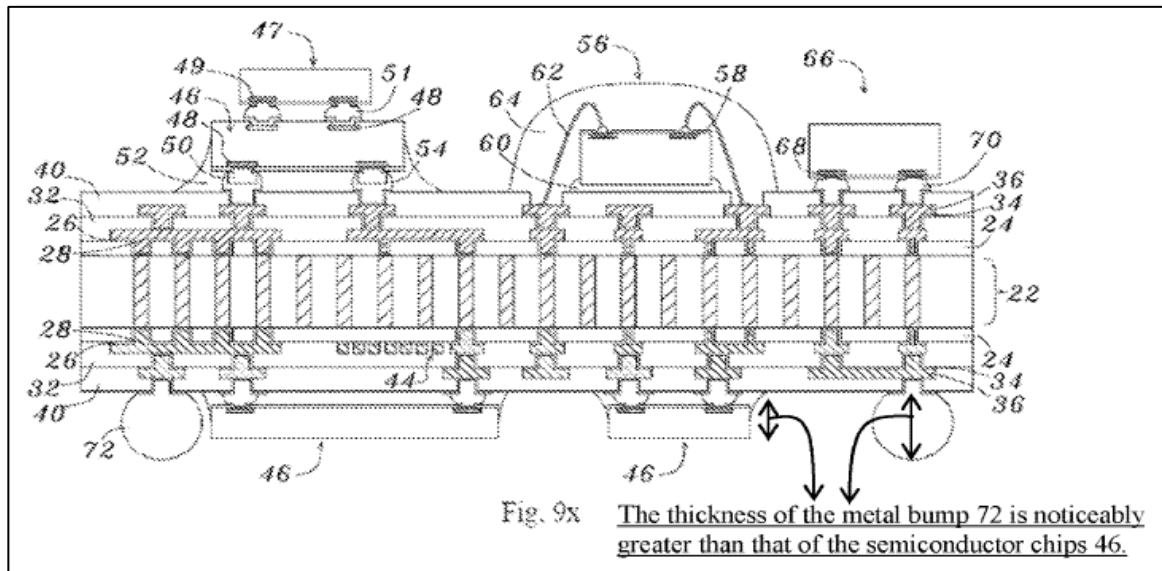
without increasing the size of the package. Further, there would have been a reasonable expectation of success at least because Sundaram already teaches connecting logic chips to the chip package using well-known methods, as demonstrated by FIG. 32, and because Sundaram already teaches including logic chips in a chip stack, as evidenced by FIG. 5d which depicts multiple devices 130 which may be “logic IC...devices.” *EX1004* at FIG. 5d, 6:39.

G. Claim 24: “The chip package of claim 18, wherein said first semiconductor chip is a logic chip.”

283. See Claim 23, ¶¶ 281-282, incorporated herein. For the same MTCs and with the same reasonable expectation of success, a POSITA would have found it obvious and been motivated to configure the *first semiconductor chip* as a *logic chip*.

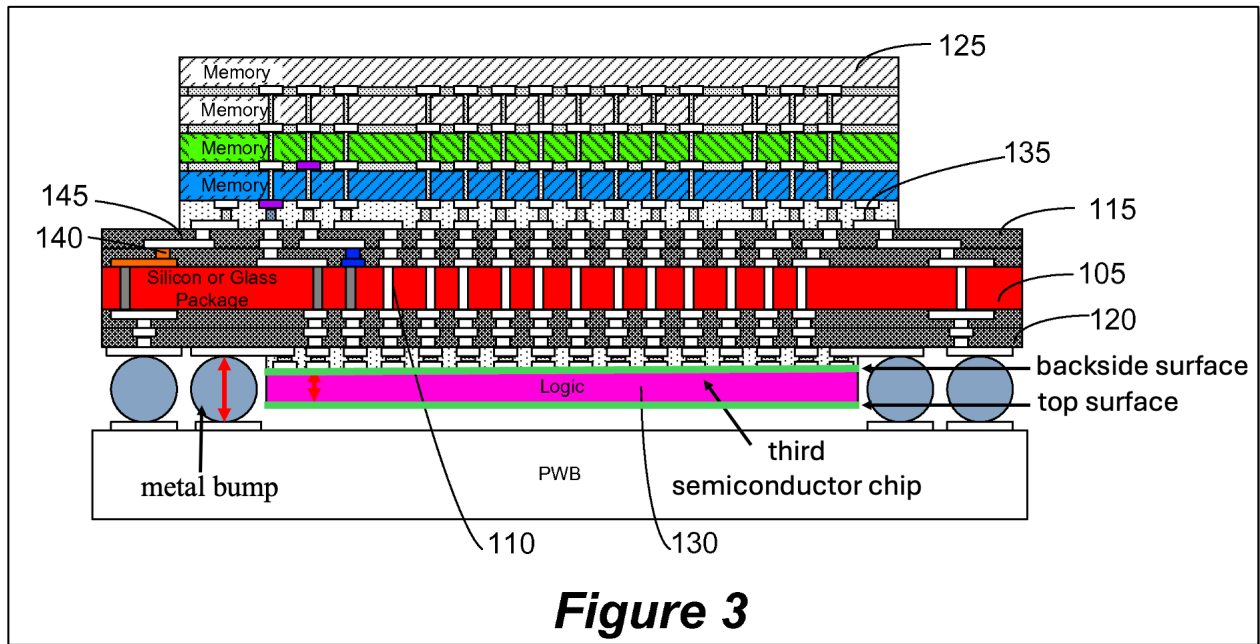
H. Claim 25: “The chip package of claim 18, wherein said third semiconductor chip has a thickness between a backside surface of said third semiconductor chip and a top surface of said third semiconductor chip is smaller than a thickness of one of said plurality of metal bumps.”

284. During original prosecution, Patent Owner filed an Amendment with an annotated figure arguing specification support for Claim 25:



EX1002 at 336.

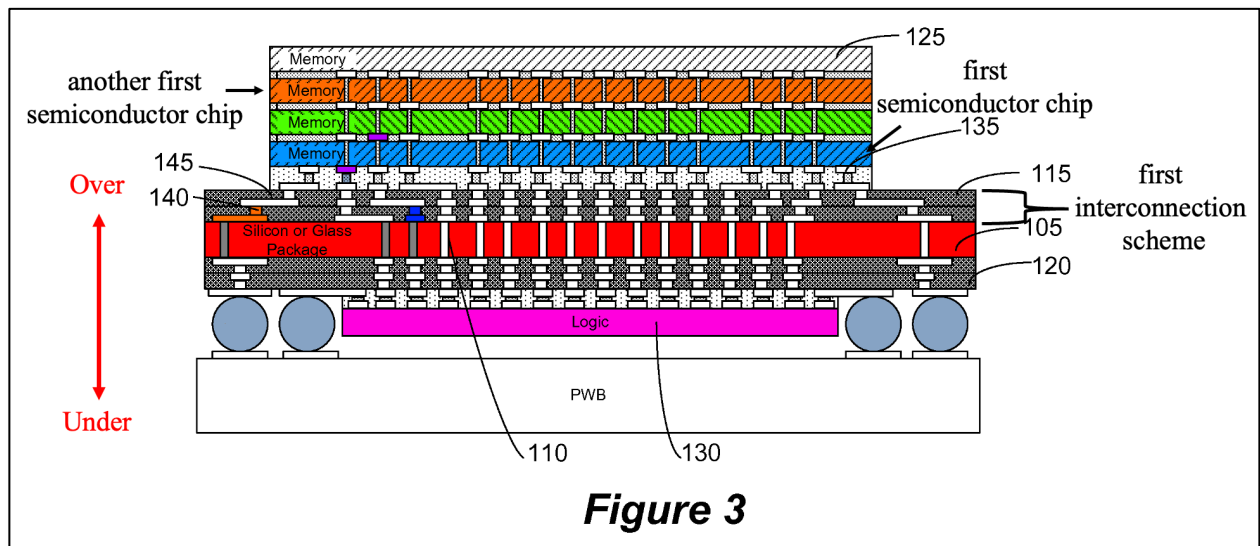
285. Sundaram's second electronic device 130 (*third semiconductor chip*) has a *thickness* (smaller red arrow) *between a backside surface of said third semiconductor chip and a top surface of said third semiconductor chip that is smaller than a thickness* (larger red arrow) *of one of said plurality of metal bumps*:



EX1004 at FIG. 3; *see also* ¶¶ 220-222.

I. Claim 26: “The chip package of claim 18, further comprising another said first semiconductor chip over said first interconnection scheme.”

286. See Claim 21(a), ¶ 266, incorporated herein. Claim 26's *another said first semiconductor chip* corresponds to Claim 21(a)'s *fourth semiconductor chip* which is *over said first interconnection scheme*:



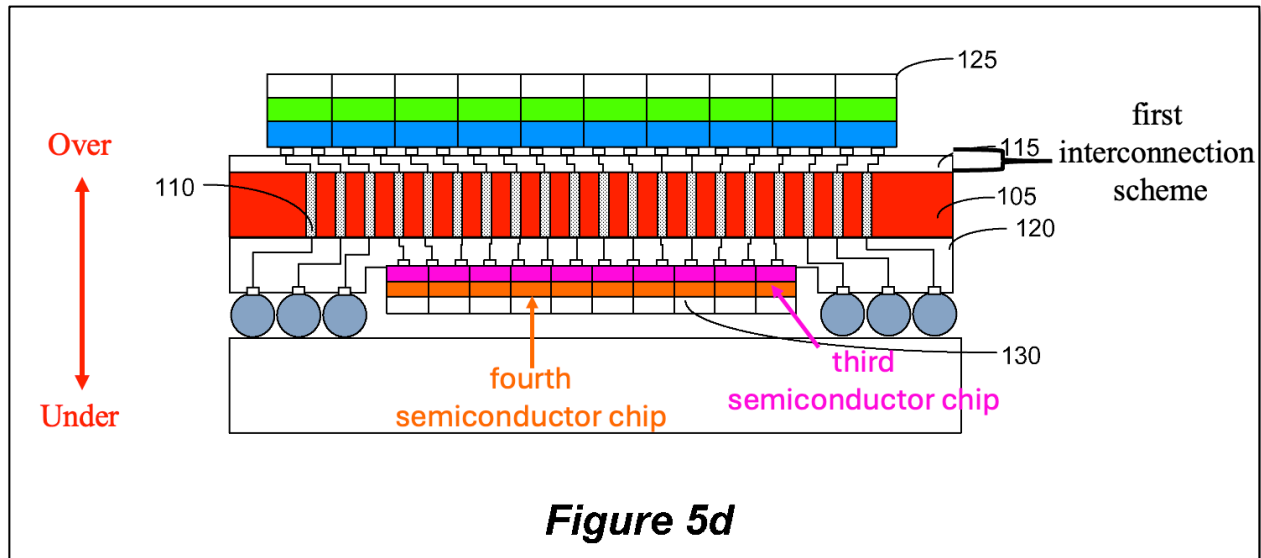
EX1004 at FIG. 3.

J. Claim 27

1. 27(a): *“The chip package of claim 18, further comprising a fourth semiconductor chip under said first interconnection scheme,”*

287. Sundaram teaches that “device 130 can be a logic IC device or **devices**,” and that “third and fourth electronic devices can be stacked on the first 125 and second 130 electronic devices,” thus, the fourth electronic device stacked on the second device 130 is a *fourth semiconductor chip under said first interconnection scheme*. EX1004 at 6:37-39, 7:16-18. Indeed, the *fourth semiconductor chip* is shown below in FIG. 5d. Because FIG. 5 “show[s] various exemplary embodiments of the interconnect structure” of FIG. 3, a POSITA would have understood that the stacked chips in second electronic device 130 shown in FIG. 5d represents a *fourth*

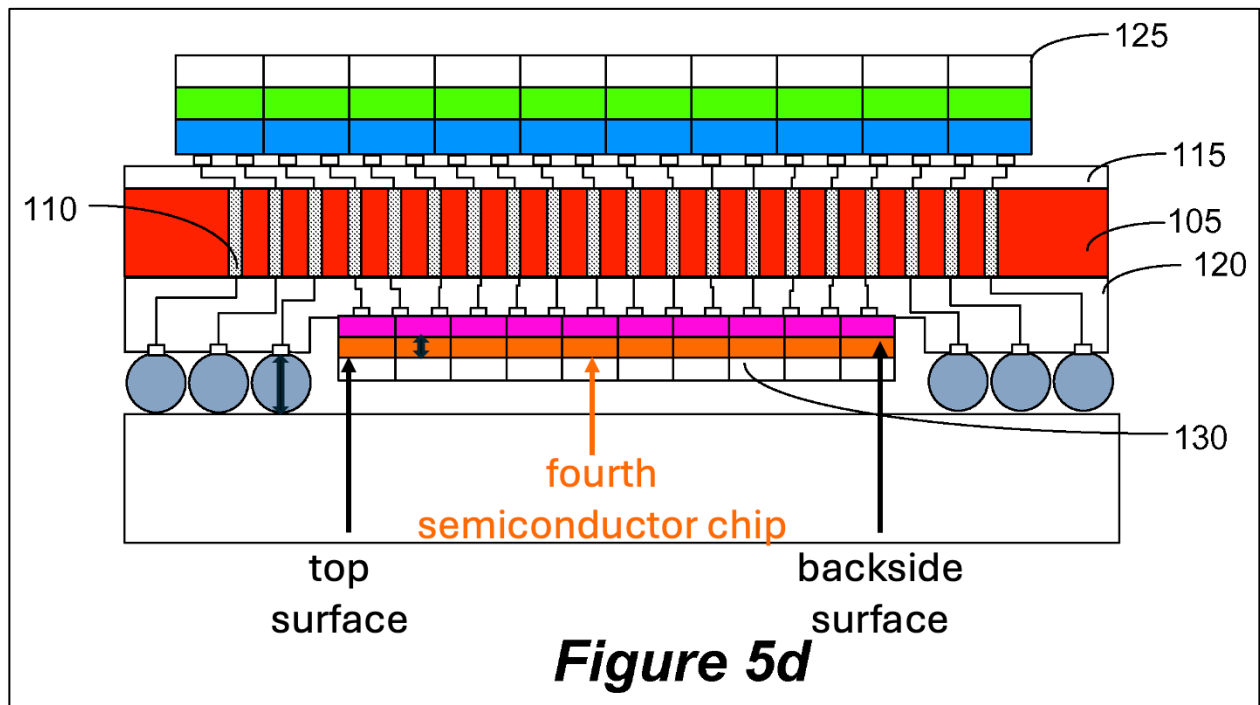
semiconductor chip under said first interconnection scheme in Sundaram's interconnect structure depicted in FIG. 3. EX1004 at 7:7-9, 5:45-46, FIG. 3.



EX1004 at FIG. 5d.

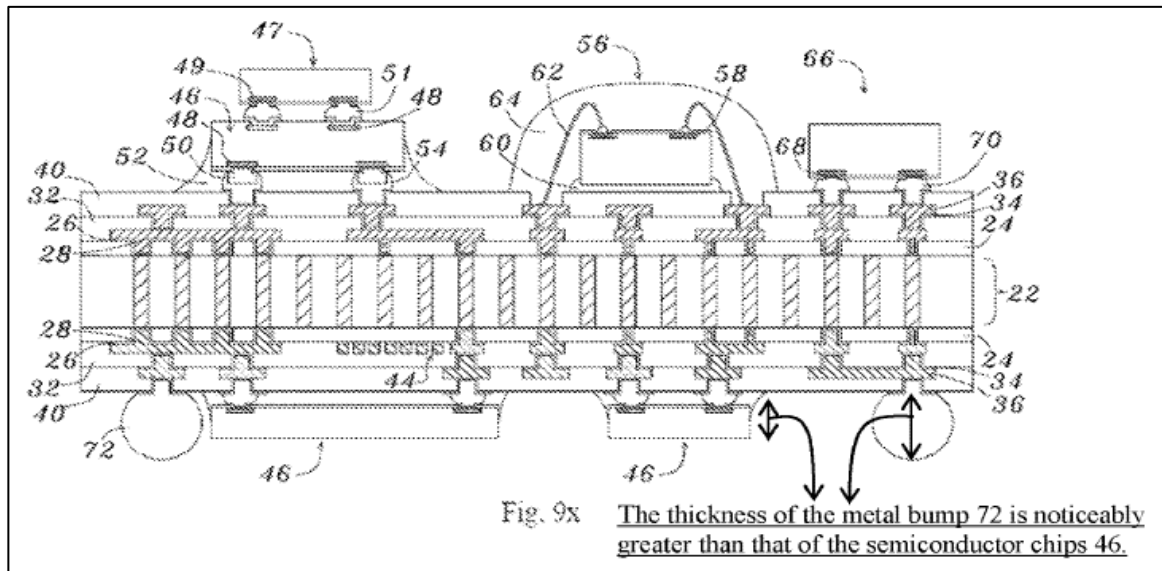
2. 27(b): “wherein said fourth semiconductor chip has a thickness between a backside surface of said fourth semiconductor chip and a top surface of said fourth semiconductor chip is smaller than a thickness of one of said plurality of metal bumps.”

288. As shown, the fourth semiconductor chip has a thickness between a backside surface of said fourth semiconductor chip and a top surface of said fourth semiconductor chip is smaller than a thickness of one of said plurality of metal bumps:



EX1004 at FIG. 5d.

289. I note that Sundaram's teachings are consistent with an annotated figure provided by Patent Owner during prosecution arguing support for language similar to Claim 27(b). See ¶ 284.



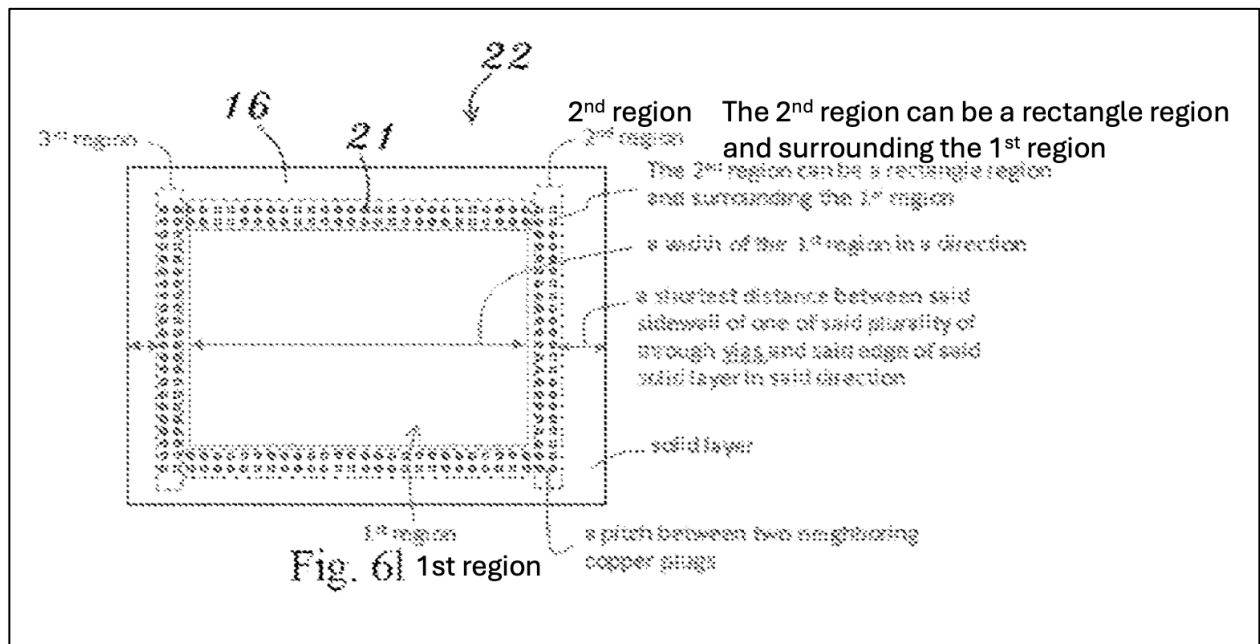
EX1002 at 336.

IX. OPINIONS REGARDING GROUND 1B: CLAIMS 8, 12, AND 16 ARE OBVIOUS OVER SUNDARAM, LIN-191, AND LIN-863

A. Claim 8: “The chip package of claim 1, wherein said second region is a rectangle region and surrounding said first region.”

a) The ‘306 Patent’s “First Region” and “Second Region”

290. I note that the claim terms “first region” and “second region” do not appear in the specification of the ‘306 Patent and thus only appear in the claims. During prosecution of the ‘306 Patent’s Parent application, USPN 11,538,763, the Patent Owner provided an annotated version of FIG. 6l illustrating specification support for the claimed *rectangle region*, shown below.

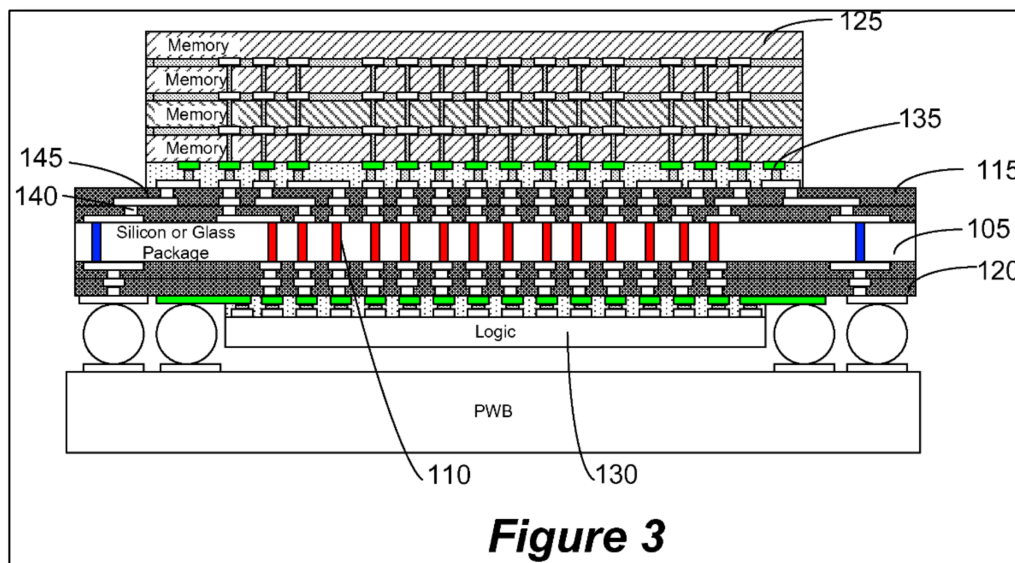


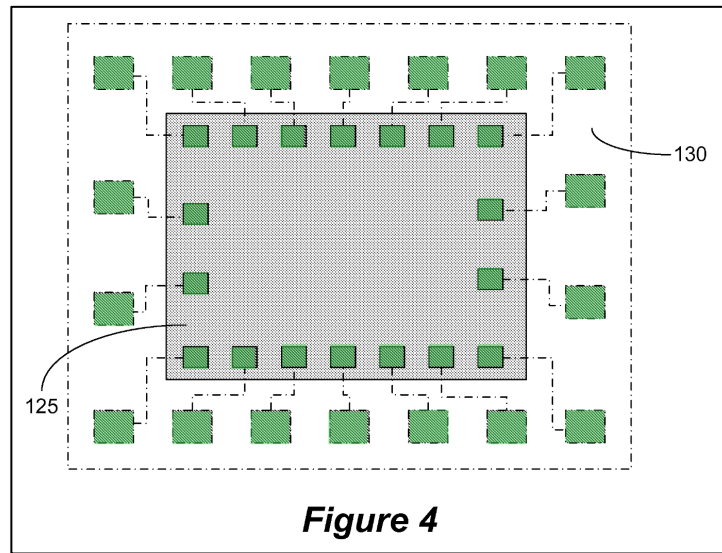
EX1117 at p. 360.

b) Sundaram's Teachings

291. Sundaram teaches “device 125 is of a different pad size and configuration than” device 130 and “connected with through vias 110, blind vias 140, and conductor traces 145.” *EX1004* at 7:1-9, FIG. 4. Based on FIGS. 3-4, a POSITA would have understood Sundaram to teach two types of vias 110: (1) **through vias for die-to-die connections** between first electronic device 125 and second electronic device 130, and (2) **through vias for die to PWB connections**. Indeed, as shown below, Sundaram’s **through vias for die to PWB connections** connect first electronic device 125 to the PWB because the blue through vias are connected to conductive traces 145 and blind vias 140 in the polymer-metal

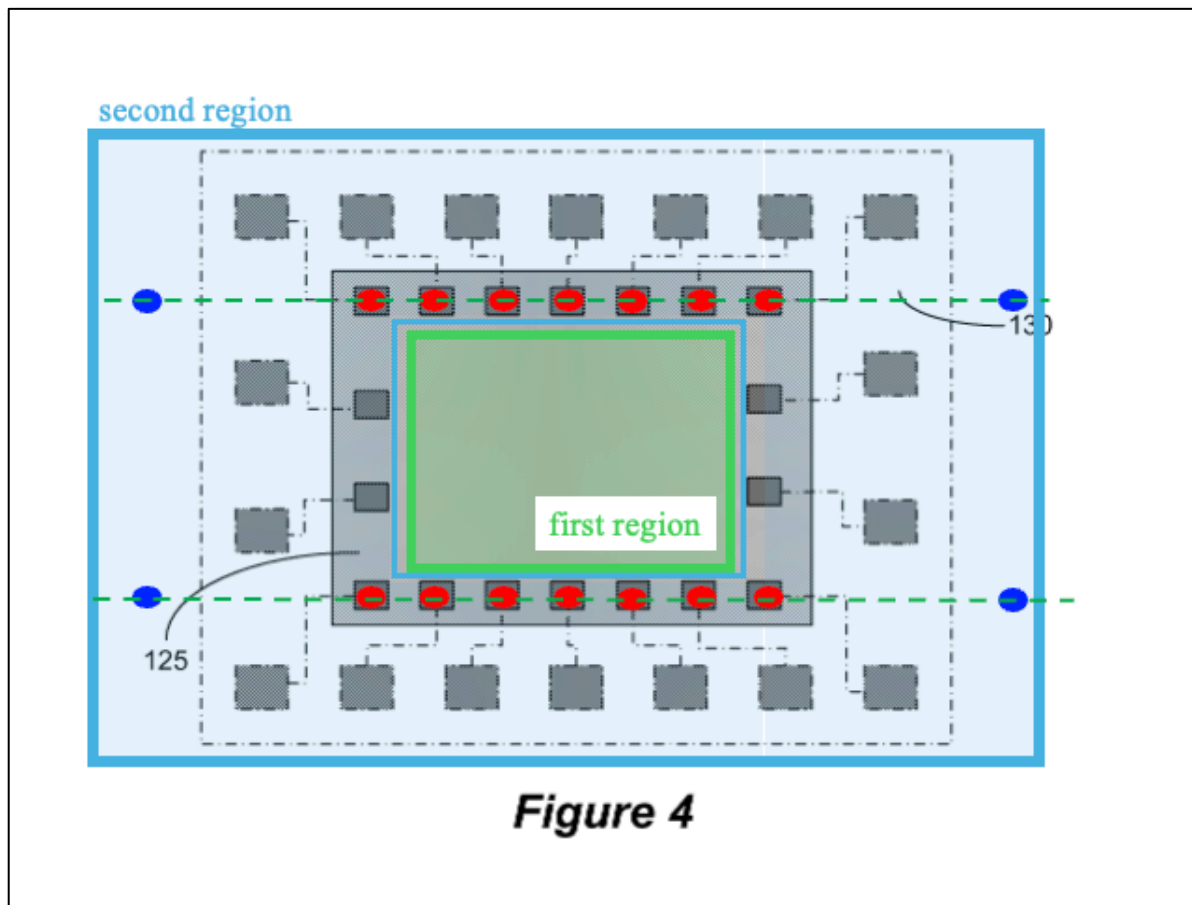
redistribution layer that first electronic device 125 connects to. *EX1004* at 6:62-67. Further, per FIGS. 3-4, the die-to-die connections (dashed lines in FIG. 4) are made through **pads** located at the periphery of the dies, which are connected to the **die-to-die vias 110** in interposer 105 (FIG. 3). That is, Sundaram teaches the **pads** illustrated at the periphery of the dies in FIG. 4 are connected “with through vias” which corresponds to the **die-to-die vias 110** shown in FIG. 3. *EX1004* at 7:4-7. Additionally, per FIG. 3, **die-to-die vias 110** and the **pads** of the smaller device 130 are substantially within the same projection region, while the **die-to-PWB vias 110** are located outside the peripheral area of the smaller device 130.



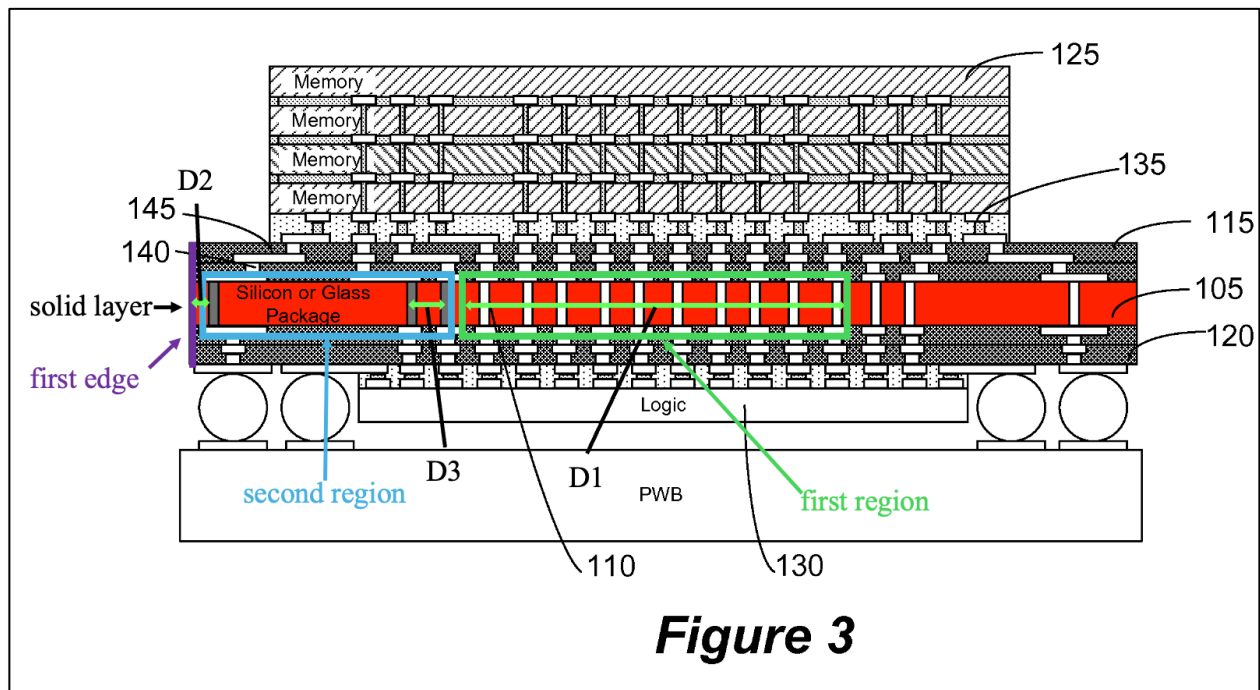


EX1004 at FIGS. 3-4.

292. Thus, because (1) **die-to-die vias 110** are located substantially within the same area as second electronic device 130, and (2) the **vias for die to PWB connections** are located peripherally to second electronic device 130, a POSITA would have understood a plan view of Sundaram's interposer 105 to look as follows:



EX1004 at FIG. 4. The dashed lines illustrate exemplary cross-sectional lines corresponding to FIG. 3's cross-section, where both vias for die-to-die connections and vias for die to PWB connections are depicted.



EX1004 at FIG. 3.

293. I note that a POSITA would have understood Sundaram's FIG. 4 to mislabel first electronic device 125 and second electronic device 130 based on their depiction in FIG. 3. Specifically, as shown in FIG. 3, first electronic device 125 is larger than second electronic device 130, whereas in FIG. 4, second electronic device 130 is larger than first electronic device 125. Based on FIG. 3, a POSITA would understand that instead of as labeled, in FIG. 4, the larger outer white box represents first electronic device 125 whereas the smaller inner gray box represents second electronic device 130. Such a configuration is consistent with FIG. 3, where second

electronic device 130 is smaller than first electronic device 125, thereby accommodating space for the solder balls to connect to the PWB.

294. Based on these teachings, a POSITA would have understood Sundaram as teaching the *second region is a rectangle region and surrounding said first region* because the **vias for die-to-die connections** as depicted are positioned around the periphery of first electronic device 125, such that each through **via for die-to-die connections** corresponds to a die pad located on the periphery of first electronic device 125. *See ¶ 292.*

295. To the extent PO argues the *rectangle region* is the right-hand side (per *EX1117* at 360), Sundaram's teaches:

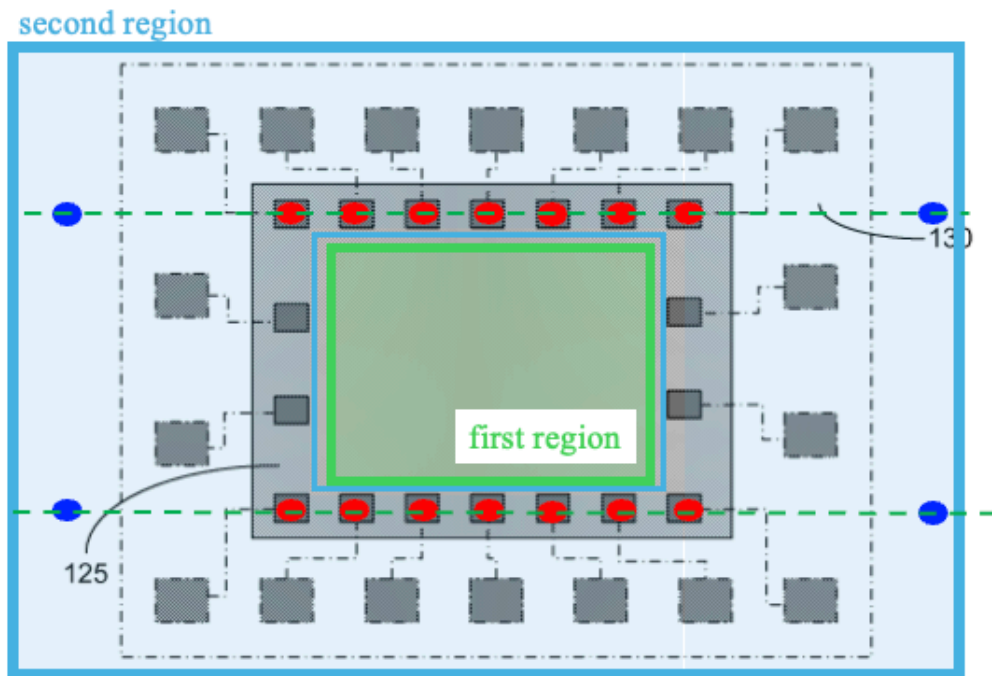
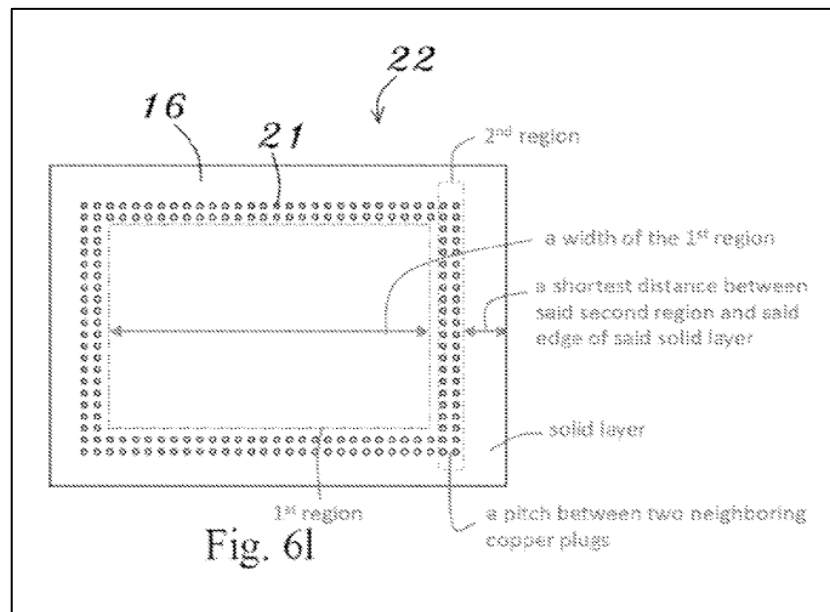


Figure 4

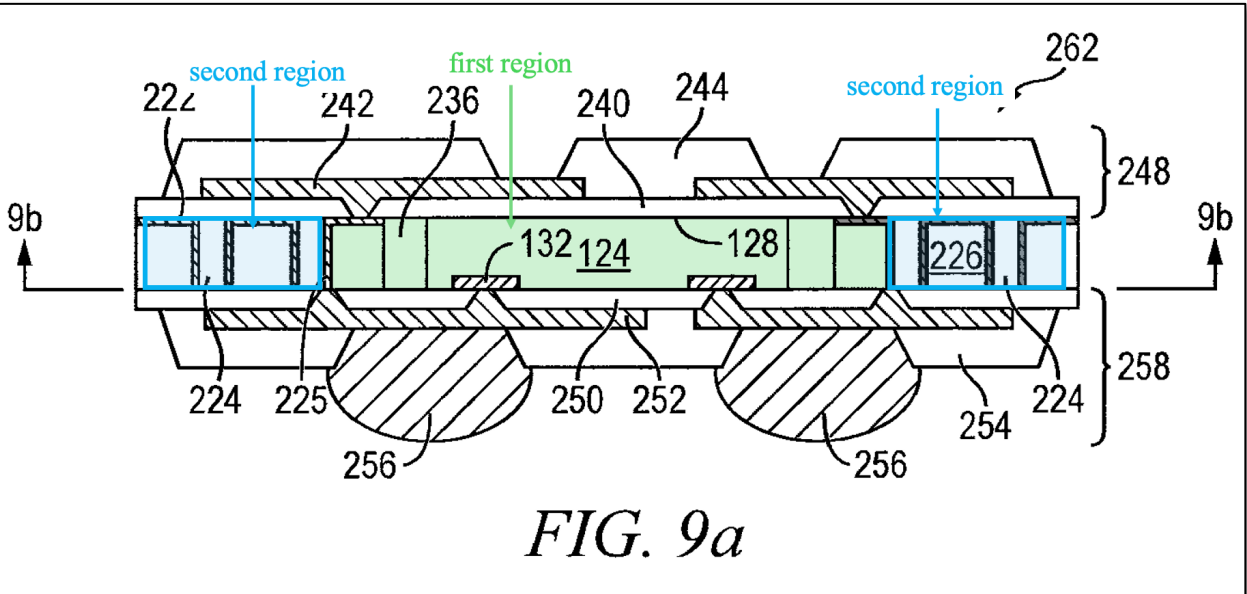
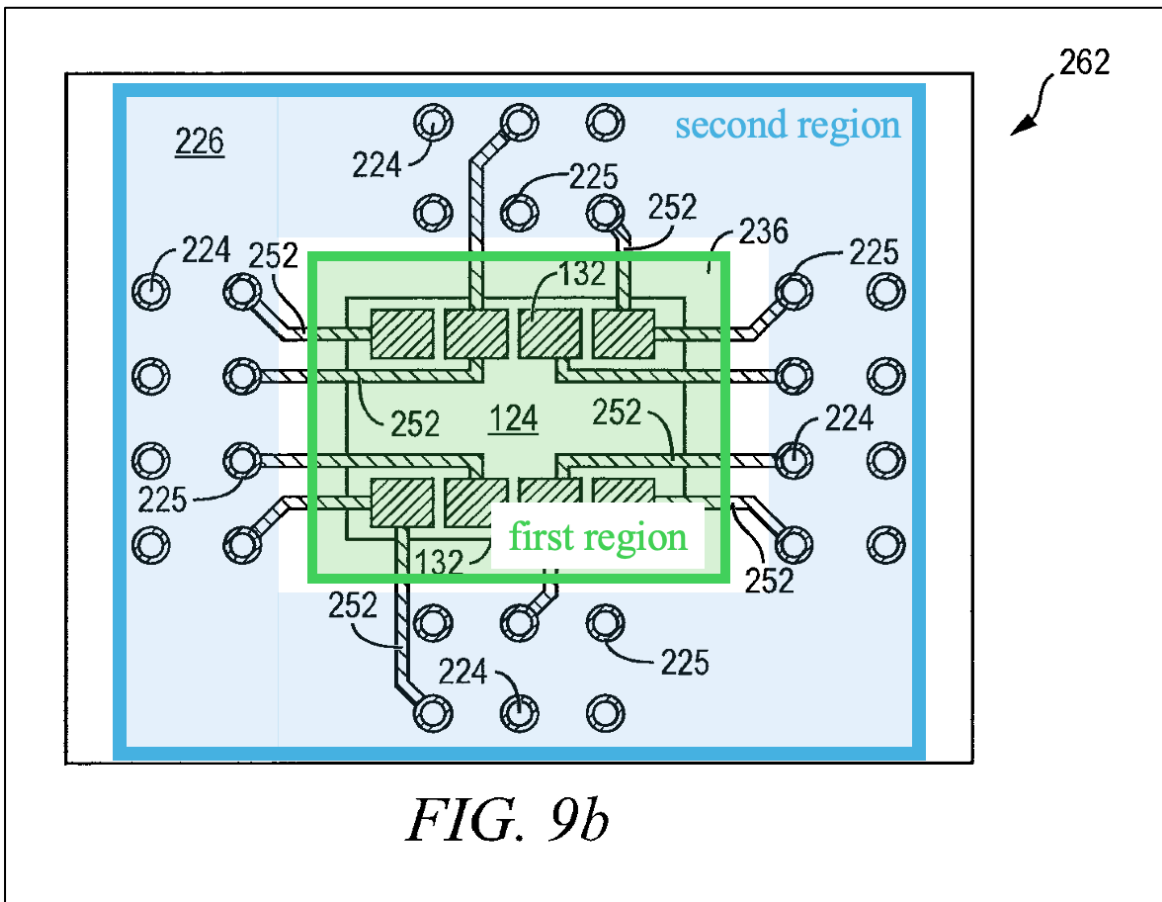
EX1004 at FIG. 4.

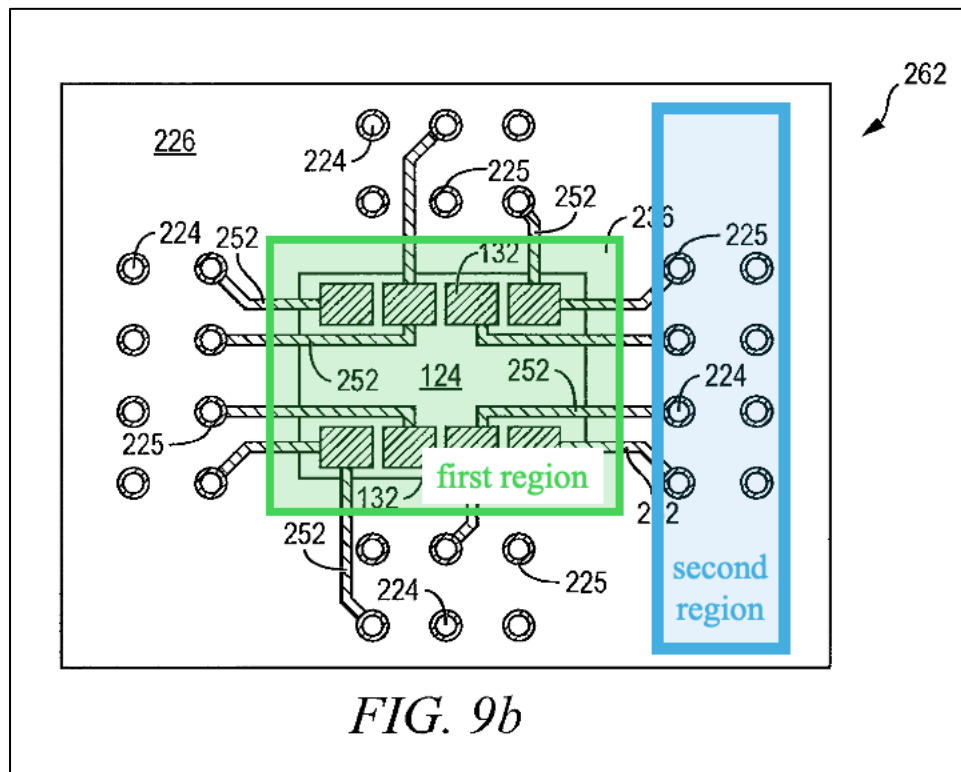


EX1117 at p. 360.

c) Lin-863's Teachings

296. Additionally or alternatively to Sundaram, Lin-863 teaches a fan-out wafer level chip scale package (Fo-WLCSP) 262 having an encapsulant 226 (i.e., a *solid layer*) through with “conductive TMV[s] [through-mold vias] 225” and “semiconductor die 124” are disposed. EX1007 at 12:33-42, 14:45-46, FIGS. 9a-9b. As shown below, Lin-863's package 262 includes a *first region* and a *second region*. EX1002 at 272. Lin-863's *first region* (green) is surrounded by the *second region* (blue). Lin-863's *second region* is the region on substrate 226 where, as shown below, conductive TMVs 225 are located. As can further be seen in FIG. 9b, because Lin-863's conductive TMVs in the *second region* surround the *first region*, Lin-863's *second region* is a *rectangle region* and surrounding said *first region*.



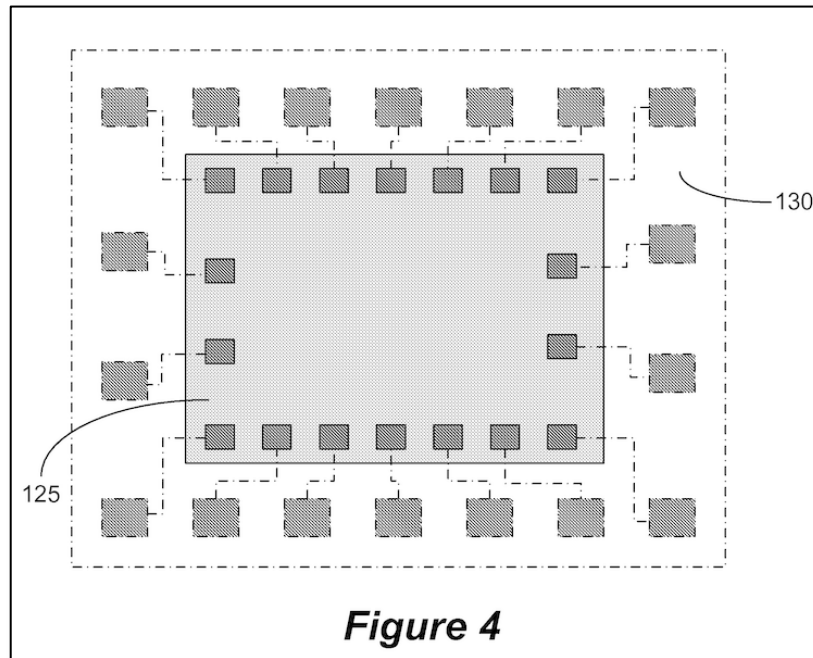


EX1007 at FIGS. 9a-b.

d) Motivation to Combine

297. Alternative to the above mapping that Sundaram teaches Claim 8 and if otherwise disputed, a POSITA would have found it obvious and been motivated to configure Sundaram's *second region* having through vias 110 to be a *rectangle region surrounding said first region* based on Lin-863's *rectangle region* having TMVs 225 surrounding Lin-863's *first region*. As shown below and as discussed above, Sundaram already at least contemplates such a *rectangle region* in FIG. 4, which "illustrates a top view of the interconnect structure illustrated in FIG. 3" and

depicts chips pads that are connected. “with through vias 110[.]” *EX1004* at 3:27-28, 7:1-8. See ¶¶ b)-293.



EX1004 at FIG. 4.

298. Based on Sundaram’s contemplation of such a *rectangle region*, a POSITA would have found it obvious to structure Sundaram’s chip package with through vias 110 in a rectangular second region, per Lin-863, such that the through vias 110 would interconnect the peripheral chip pads of Sundaram’s first electronic device 125 and second electronic device 130 to be connected. Such an arrangement also permits the addition of passive components directly under the chip or, it allows for placement of heat sink material directly under the chip, improved thermal

dissipation, and shorter interconnect paths by embedding the chip within the interposer/package.

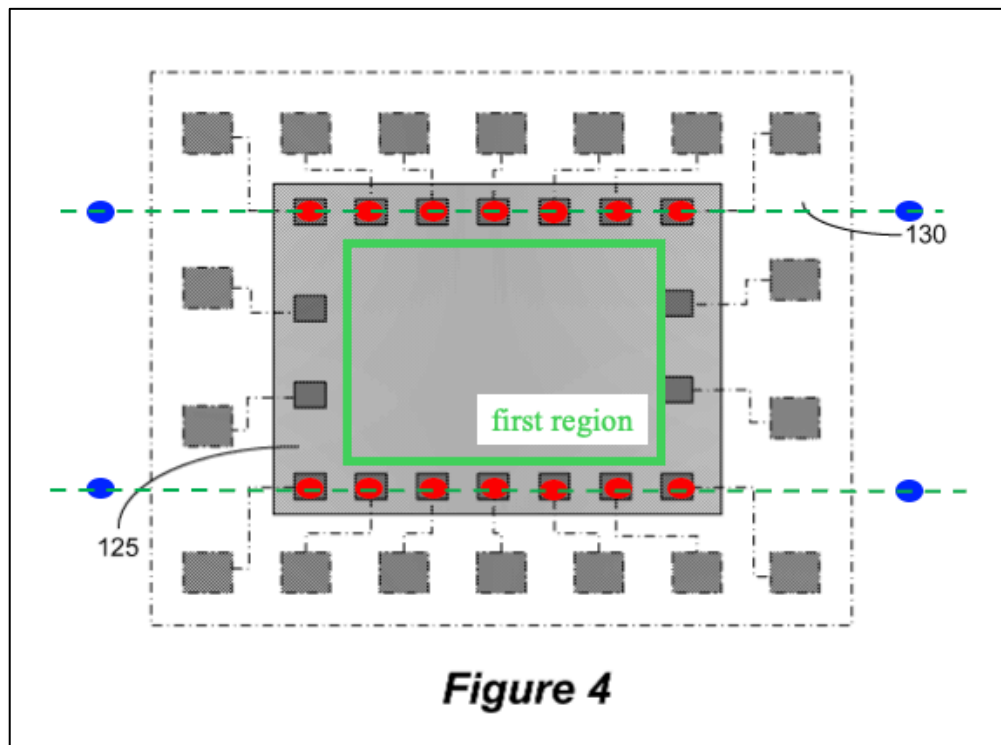
299. Further, a POSITA would have been motivated and found it obvious to modify Sundaram's chip package to have through vias 110 in a rectangular second region surrounding a first region to match the standard rectangular geometry of a chip. *EX1069* at 1:65-66 ("Most conventional IC chips have a generally square or rectangular shape when observed in a plan view."). Specifically, chips are cut into a rectangular shape as non-rectangular shapes are difficult to dice using standard dicing machines (e.g., saws) and because non-rectangular shapes do not maximize the use of valuable wafer area where circuitry can be fabricated. *EX1069* at 1:66–2:9 ("This configuration [square or rectangular] is due, at least in part, to the conventional wafer dicing technique[.], "...the dicing machine is typically limited to making long, straight cuts and cannot effectively or efficiently cut more complex IC chip profiles."). Thus, it is practical and common practice to surround a chip with posts arranged in a geometry that mirrors the chip's shape, e.g., to mirror the rectangular shape of device 125. *See, e.g., EX1070* at FIG. 6G; *EX1007* at FIG. 8b; *EX1010* at FIGS. 2, 22; *EX1069* at 2:31-33 ("The generally square or rectangular shape of the conventional IC chip tends to be reflected in the shape of the packages incorporating such IC chips...").

300. The combination is the application of known technique (interconnects in a rectangular arrangement in a chip package) to a known device (Sundaram's chip package) to yield the predictable results of Sundaram's package having through vias 110 in a rectangular region surrounding Sundaram's *first region*. A POSITA would have had a reasonable expectation of success in modifying Sundaram's chip package, per Lin-863, to have a *rectangle region* as the *second region* because Lin-863's fan-out package was well-known and widely used for chip packaging applications. *See, e.g., EX1070* at FIG. 6G; *EX1007* at FIG. 8b; *EX1010* at FIGS. 2, 22.

B. *Claim 12: "The chip package of claim 10, wherein no any copper post⁵ in said first region."*

301. As I discussed above, a POSITA would understand a plan view of Sundaram's interposer 105 to look as follows:

⁵ I have been instructed to interpret "no any copper post" as "no copper post."



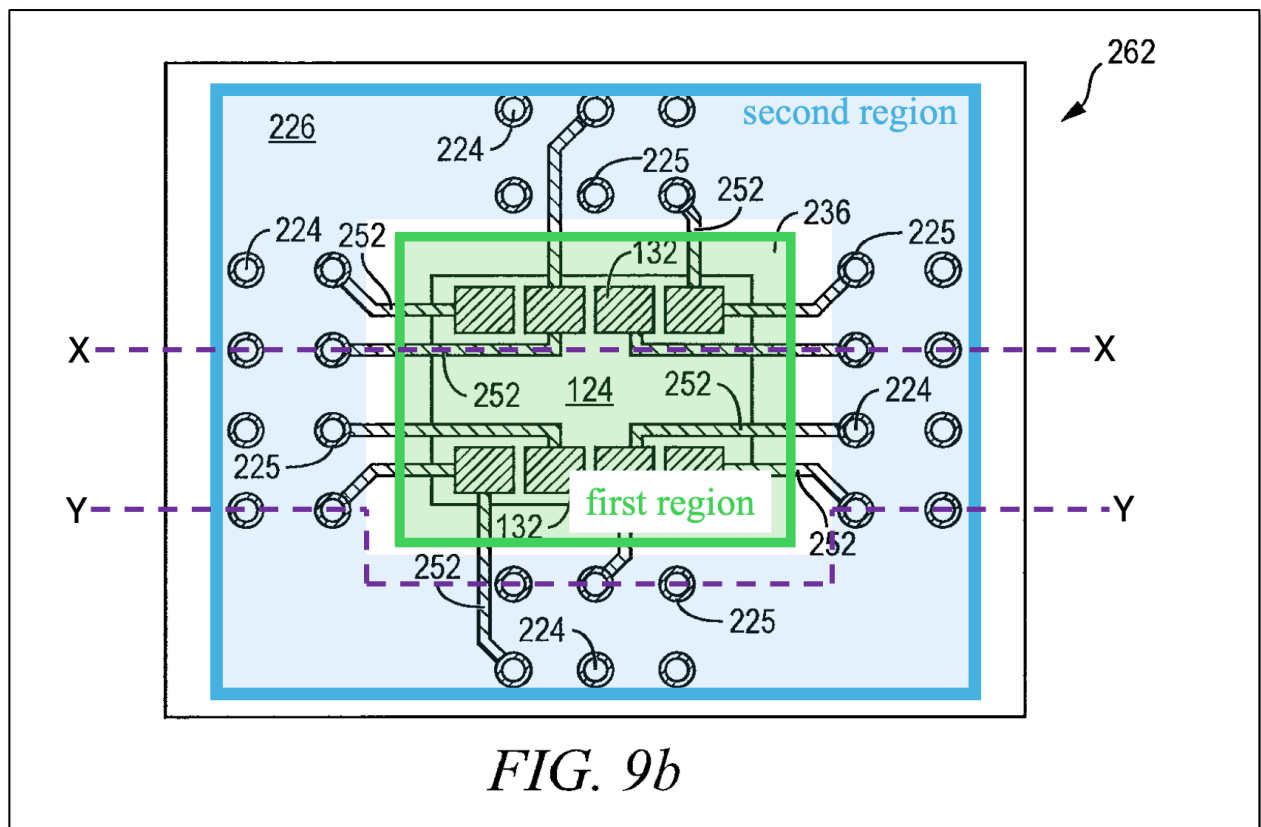
EX1004 at FIG. 4. See ¶¶ 291-292.

302. Because Sundaram teaches **die-to-die vias** connecting **pads** at the periphery (as opposed to pads in the middle of the dies), a POSITA would have understood Sundaram as teaching the *first region* as having no copper posts. Indeed, Sundaram's depictions of pads located at the periphery of first electronic device 125 and second electronic device 130 is consistent with traditional metal pad layout architecture, where the "traditional structure is a peripheral array, with contact terminals arranged along or near the periphery of the active circuitry" of a semiconductor device. EX1103 at 3:67–4:2. A POSITA would understand that where there is no metal pads (i.e., in the middle of Sundaram's dies) there is,

correspondingly, no need for interconnections such as through vias 110. As such, Sundaram's *first region* as depicted above is a region with *no any copper post*.

a) Lin-863's Teachings

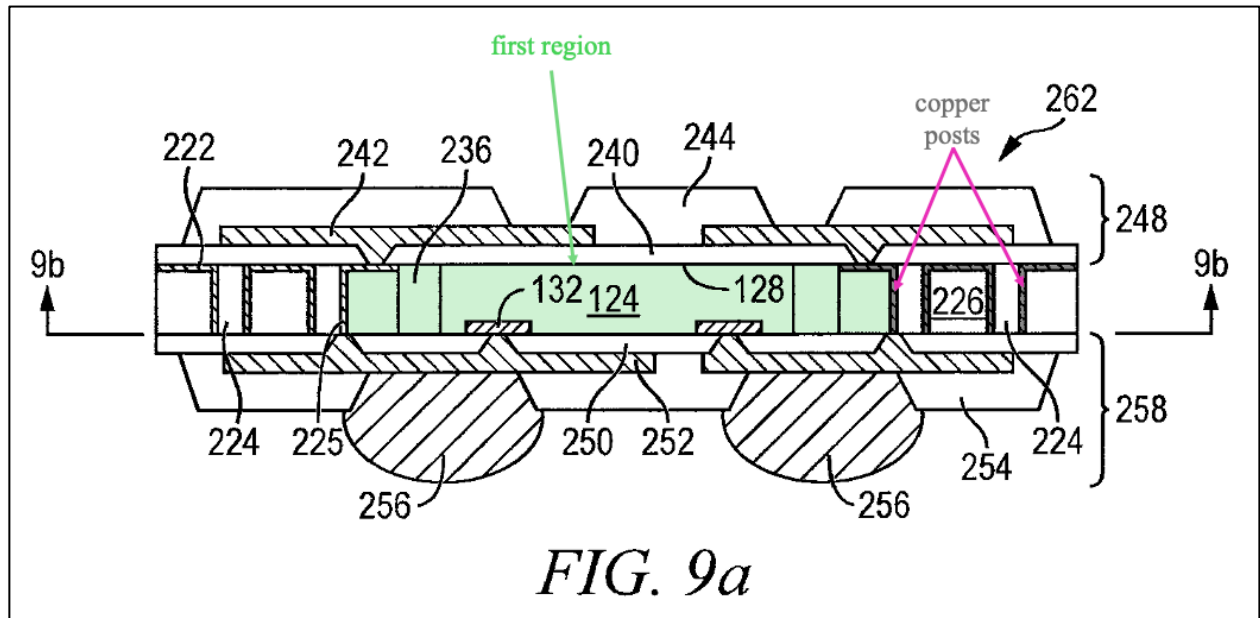
303. Additionally or alternatively to Sundaram, Lin-863's *first region* has no *copper...post[s]* as shown in FIG. 9a, where there are no conductive TMVs 225 present in the *first region*.



EX1007 at FIG. 9b.

304. The lack of *copper post[s]* in the *first region* is further confirmed in FIG. 9a, which is a “cross-sectional view of Fo-WLCSP 262[,]” where Lin-863's

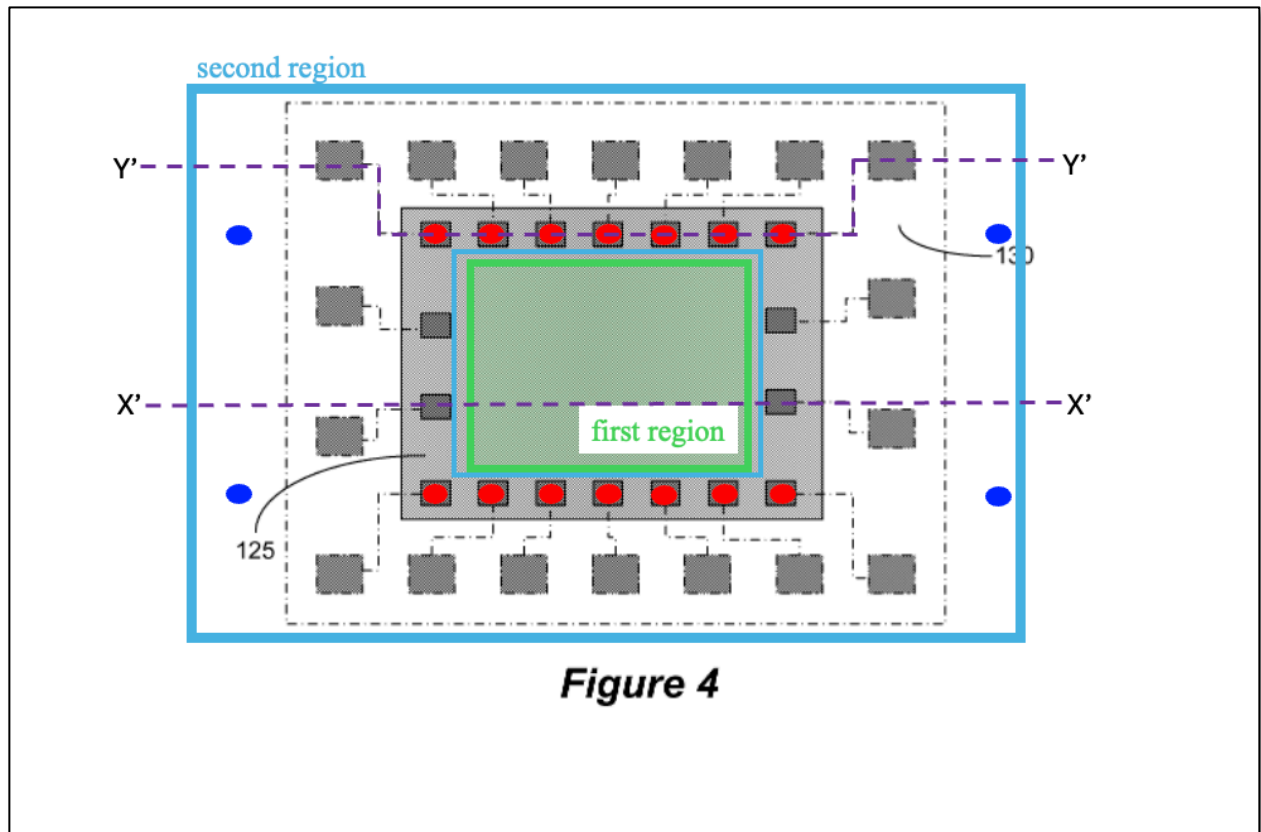
TMVs 224 are positioned peripherally to Lin-863's *first region*. *EX1007* at 14:45-46.



EX1007 at FIG. 9a.

305. The 9b-9b cross-section line in FIG. 9a corresponds to the X-X line annotated in FIG. 9b. A POSITA would understand the view shown in Sundaram's FIG. 3 to be taken along a line analogous to Y-Y. *Compare EX1007* at FIG. 9b with *EX1004* at FIG. 4. Specifically, as shown below in FIG. 4 of Sundaram, pads on the first and second electronic device 125, 130 which are "connected with through vias 110," follow the **dashed lines** illustrating exemplary cross-sectional lines corresponding to FIG. 3's cross-section, which corresponds to Y-Y as depicted above. Similarly, when modified per Lin-863, a cross-section of Sundaram's FIG. 4

would reveal the *first region* having no through vias 110, corresponding to line X-X' in Lin-863's plan view illustrated above. Thus, Sundaram as modified by Lin-863 teaches *wherein no any copper post in said first region*.



EX1004 at FIG. 4.

b) Motivation to Combine

306. A POSITA would have found it obvious and been motivated to modify Sundaram's *first region* per Lin-863's *first region* having no *any copper posts* to accommodate space for an additional semiconductor chip to be included in Sundaram's package. Specifically, a POSITA would have been motivated to form

an opening in Sundaram's interposer 105 such that an additional chip would be positioned in the chip package, thereby forming a *first region* with no *[] copper posts* like that in Lin-863's package. A POSITA would have appreciated the additional functionality (i.e., by having more chips) that adding another chip would provide and would have recognized including the additional chip within interposer 105 would have been an efficient use of space, because the overall size of the chip package would not have increased, which would have been desirable to a POSITA, as it was "desirable to minimize thickness of the chip scale package." *EX1068* at [0011]. Additionally, a POSITA would have recognized that by including the additional chip within interposer 105, interconnects between the additional chip and the PWB would be shorter because signals would not have to travel through vias 110 to the other side of interposer 105. A POSITA would have found this advantageous because "shorter interconnects mean it takes less time to process a task, which leads to higher performance" and "reduce[s] power consumption." *EX1072* at 7:61-64.

307. The combination is the application of known technique (no plugs/interconnects in a central region) to a known device (Sundaram's chip package) to yield the predictable results of Sundaram's package having a post-free region where a die is positioned. In the combination, an additional die is positioned in an opening in Sundaram's interposer 105, such that the *first region* has no through

vias 110 (i.e., *no [] copper posts*). There would have been a reasonable expectation of success for the reasons previously discussed, as well as because methods of controlling plug placement in chip packages were well known and would have merely involved forming through vias 110 only in the *second region*. Further, chip packages having a solid layer with a region with no plugs was well-known, as demonstrated by Lin-863 and others. *See, e.g., EX1073* at FIGS. 6, 8-9, 11:49-51; *EX1127* at FIGS. 1-2, 21M, 22, 7:12-15. Additionally, including a chip in a glass substrate, such as Sundaram's was well-known and methods for producing a chip in a glass substrate, including glass substrates having RDLs, were established, further leading to a reasonable expectation of success. *See, e.g., EX1074* at FIG. 8, [0015], [0023], [0025].

C. Claim 16: “The chip package of claim 10, wherein said second region is a rectangle region and surrounding said first region.”

308. *See* Claim 8, ¶¶ 290-300, incorporated herein.

X. OPINIONS REGARDING GROUND 2A: CLAIMS 1-7, 9-15, 17-20, AND 22-27 ARE OBVIOUS OVER YU AND LIN-191

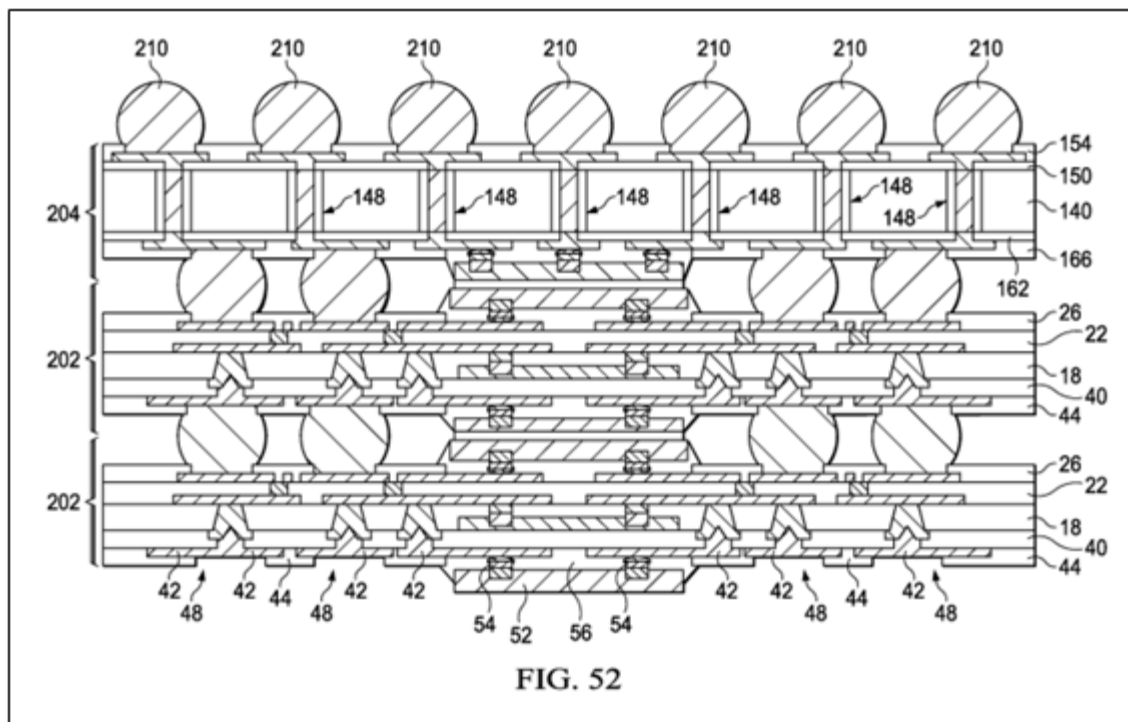
A. Claim 1

1. 1(Pre): “A chip package comprising”

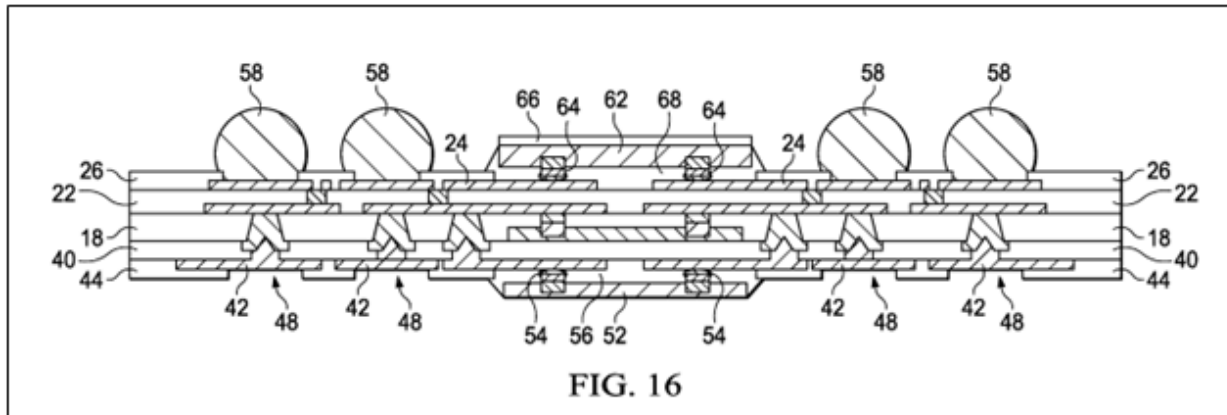
309. Yu teaches a “PoP [Package-on-Package] structure” comprising “multiple packages 202,” each of which contains one or more semiconductor dies. *EX1010* at 8:35-36. Yu explains the dies may include “a logic circuitry die, a

memory die, or any other die,” thereby encompassing a variety of semiconductor devices integrated within the stacked package arrangement. *EX1010* at 2:50–51. Yu further defines “Package-on-Package (PoP)” as “an integrated circuit packaging technique to allow vertically combining discrete logic and memory ball grid array (BGA) packages.” *EX1010* at 1:49–51.

310. Accordingly, Yu’s disclosure of a “PoP structure” comprising “multiple packages 202” and including logic and memory dies teaches a *chip package* in which multiple packaged semiconductor devices are combined into a vertically integrated assembly. *EX1010* at 1:49–51, 2:50–51, 8:35–36.



EX1010 at FIG. 52.



EX1010 at FIG. 32.

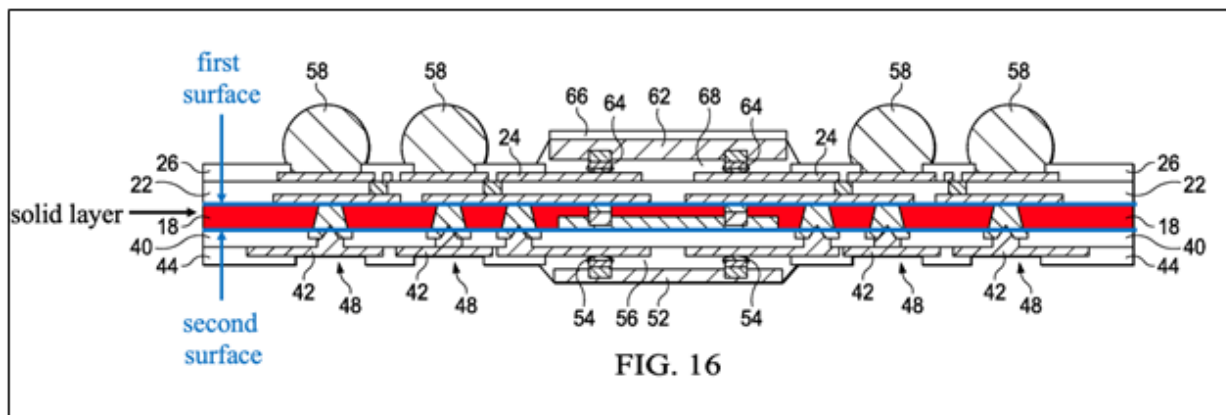
311. Yu's FIG. 52 comprises multiple of the packages 202 shown in FIG. 17. *EX1010* at 8:11-13. The package of FIG. 17 is the same as FIG. 16 except for depicting "pins 70 of a probe card" probing connectors 58 "to test the structure." *EX1010* at 5:4-6. Thus, Yu's FIG. 52 depicts multiple of the packages 202 as depicted in FIG. 16.

312. The hierarchy of figures illustrates a progressive structural relationship: FIG. 16 depicts the core single-package cross-section and FIG. 52 shows multiple such packages stacked in a vertical PoP configuration. Accordingly, Yu's PoP structure, as shown in FIG. 52, comprises multiple chip packages each corresponding to the single-package configuration of FIG. 16, thereby forming a *chip package*. EX1010 at 1:49–51, 2:50–51, 4:67–5:7, 8:11–13, 8:35–36.

2. *1(a): “a solid layer having a first surface and a second surface opposite to said first surface,”*

313. As shown below, Yu's package 202 includes "molding compound 18 [that] can be [] epoxy, polyimide, silicone rubber, the like, or a combination thereof," i.e., *a solid layer*. EX1010 at 2:61-64. Yu identifies molding compound 18 as part of package 202 and depicts the molding compound 18 as a defined, solid region surrounding the internal components of the package. As shown in Yu's FIG. 16, molding compound 18 clearly includes opposing surfaces, *a first surface opposite and a second surface opposite to said first surface*, that bound the solid layer.

314. Thus, Yu's molding compound 18 (*solid layer*) comprises *a first surface and a second surface opposite to said first surface*.



EX1010 at FIG. 16.

3. **1(a)(i): "wherein said solid layer comprises a compound of silicon and oxygen,"**

315. Molding compound 18 comprises "silicone rubber," which is *a compound of silicon and oxygen*. EX1010 at 2:61–65. Silicone rubber is a polymeric

material known in the art to be a type of polysiloxane having a “siloxane backbone of repeating Si–O–Si units.” *EX1060* at 6:10-17. Accordingly, Yu’s molding compound 18, which comprises silicone rubber, is a *solid layer comprising a compound of silicon and oxygen (i.e., Si-O-Si)*. Yu further teaches that molding compound 18 comprises “epoxy, polyimide, silicone rubber, the like, or a combination thereof,” such that silicone rubber alone or silicone rubber in combination with epoxy and/or polyimide teaches *a compound of silicon and oxygen*. *EX1010* at 2:61-65.

4. 1(a)(ii): “wherein said solid layer has a thickness between 50 and 150 micrometers,”

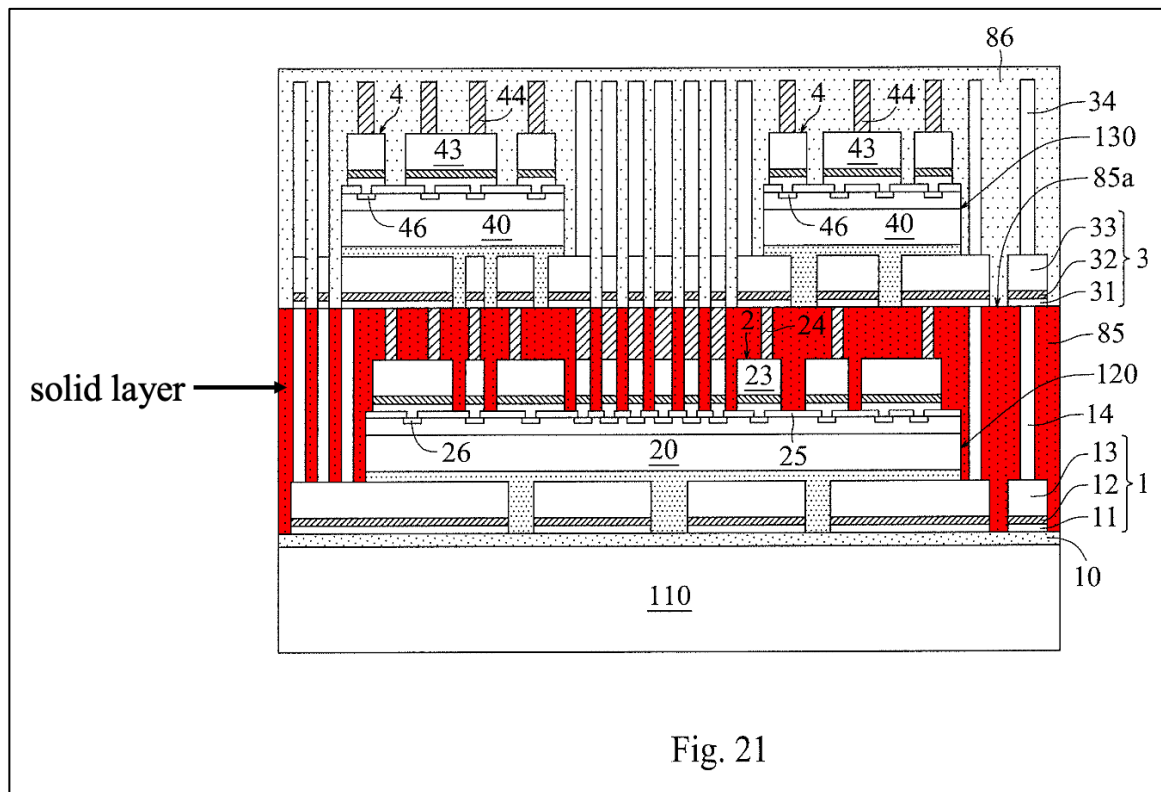
a) Lin-191’s Teachings

316. Lin-191 teaches an “encapsulating layer 85” formed “on top[] of the metal pillars or bumps 14,” which correspond structurally to conductive vias or posts such as Yu’s TMVs (discussed further at Claim 1(b)). *EX1005* at [0109]. Lin-191 explains that the encapsulating layer 85 covers the bumps and the surrounding regions of the substrate to protect and planarize the device structure. *Id.* Because encapsulating layer 85 includes “a polymer layer,” it constitutes a solid layer similar to Yu’s molding compound 18, which likewise encapsulates conductive structures within a solid layer. *Id.*

317. Lin-191's encapsulating layer 85 has a thickness "between about 20 and about 500 micrometers, and preferably between 30 and 100 micrometers" Similar to my opinions provided for Sundaram for Ground 1A (§§ 130-131), Lin-191 teaches or renders obvious the claimed *thickness between 50 and 150 micrometers*. *EX1005* at [0109]-[0111]. Because Lin-191 teaches a range ("between about 20 and about 500 micrometers") that includes the narrower claimed range of *between 50 and 150 micrometers* and a range ("between 30 and 100 micrometers) that overlaps the claimed range, Lin-191 teaches or obvious Claim 1(a)(iii).

318. Additionally or alternatively, Lin-191's encapsulating layer 85 has a *thickness* equal to the combined thickness of layers 1 and metal pillars or bumps 14. Encapsulating layer 85 is "formed...on the metal layer 13 of the patterned metal layer 1," and "top surfaces 14a" of bumps 14 are "substantially coplanar...with a top surface 85a" of layer 85. *EX1005*, [0109-0110], FIG. 12. Thus, as can be seen in FIG. 21 below, encapsulating layer 85's thickness is equivalent to that of layer 1 plus bump 14. Indeed, Lin-191 teaches layer 85 is "ground or polished" such that "top surfaces 14a of" pillars 14 and "top surfaces 24a" of bumps 24 "are substantially coplanar with...a top surface 85a" of encapsulating layer 85. *EX1005* at [0110]. Pillars 14 have a thickness "between 20 and 110 micrometers[.]" *EX1005* at [0121]. Additionally, pillars 14 are on layer 1, which is formed of adhesion layer 11, seed

layer 12, and metal layer 13. *EX1005* at [0075], FIG. 21. Layer 11 has a thickness “less than 1 micrometer, such as between 1 nanometer and 0.5 micrometers,” layer 12 has a thickness “less than 1 micrometer, such as between 10 nanometers and 0.8 micrometers,” and layer 13 has a thickness “between 3 and 10 micrometers.” *EX1005* at [0050], [0060]. Thus, layer 1 plus pillar/bump 14 has a thickness of, at most, 121.3 micrometers ($0.5 + 0.8 + 10 + 110$) or at least 23.011 micrometers ($0.001 + 0.01 + 3 + 20$). Because layer 85’s thickness is the same as the combined thickness of pillars 14 and layer 1, layer 85 thus also has a maximum thickness of 121.3 micrometers, or a minimum thickness of about 23.011 micrometers. *EX1005* at [0050]. Thus, a POSITA would have understood that Lin-191’s encapsulating layer 85, like Yu’s molding compound 18, is a polymeric solid encapsulant layer of comparable structure and function, disposed over the metal pillars 14 and having a thickness between 23.011 micrometers and 121.3 micrometers, thus teaching or rendering obvious a *thickness between 50 and 150 micrometers*.



EX1005 at FIG. 21.

319. Similar to my opinions provided at ¶ 131, I note that the '306 Patent does not indicate any specific criticality for the claimed range. Therefore, for the reasons provided here and in ¶ 131, it is my opinion a POSITA would have found the claimed range obvious.

b) Motivation to Combine

320. A POSITA would have been motivated to apply Lin-191's thickness to Yu's molding compound 18. The modification would have given Yu's molding compound 18 stress buffering capabilities as polymer layers (such as Yu's molding

compound 18) having a thickness “between about 30 μm and about 200 μm ” (overlapping with Lin-191’s and the claimed range) were known to “act[] as an efficient stress buffer.” *EX1080* at [0018]. Stress buffering provided by Yu’s molding compound 18 would have been advantageous for a variety of reasons.

321. First, stress buffering provided by Yu’s compound 18 and Lin-191’s thickness would be beneficial for protecting Yu’s die 10 that is in molding compound 18. *EX1010* at 2:61-63, FIG. 2. As demonstrated by Lin-191, the thickness is appropriate for an embedded chip, as encapsulating layer 85 covers chip 120. *EX1005* at FIG. 21. Given that Yu similarly embeds a die 10 in molding compound 18, a POSITA would appreciate that Lin-191’s solid layer thickness would apply to Yu’s *solid layer*. Given that solid layers with the claimed thickness were known for embedding chips and buffering stress, a POSITA would appreciate the Yu’s die 10 would be protected from stress by molding compound 18, thereby reducing the likelihood of stress-induced damage to die 10. *EX1080* at [0018]. Further, molding/encapsulation layers at the claimed thickness were known to environmentally protect embedded die from “external elements and contaminants.” *EX1131* at [0046]; ¶ 54.

322. Additionally, Lin-191’s thickness would allow for the opportunity to incorporate metal shielding into Yu’s molding compound 18 (*solid layer*) which

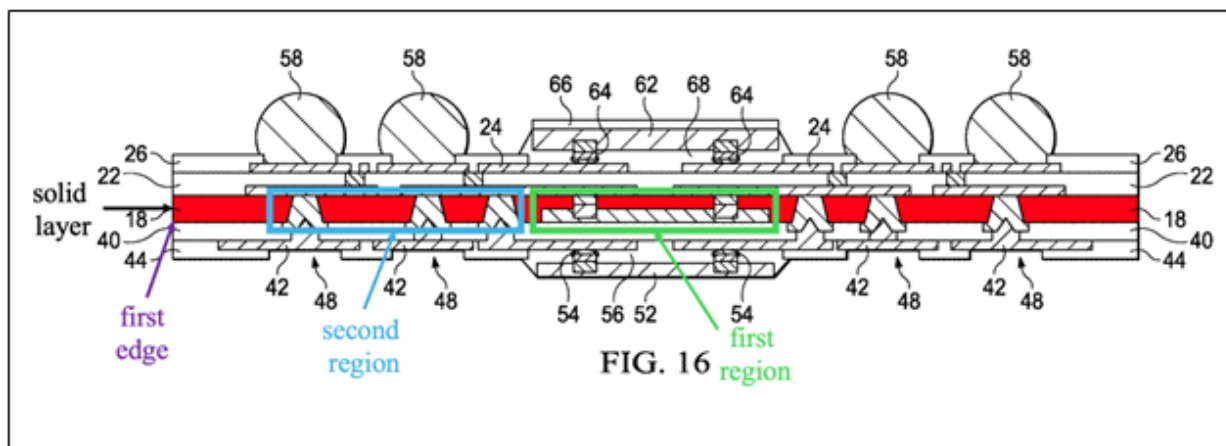
would reduce electromagnetic interference (in the chip package. EMI negatively impacts signal quality in chip packages such that a POSITA would have found the opportunity to prevent EMI-induced signal degradation. Indeed, ICs were known to “radiate a relatively large amount of electromagnetic energy” that may “interfere with the operation of other devices or circuits in the vicinity of the radiating IC” which prompted the use of “electromagnetic interference (EMI) shielding layer[s].” *EX1136* at 1:28-37, 2:28-30. Such shielding layers were known to be incorporated within and between dielectric layers such that a POSITA would have recognized applying Lin-191’s thickness to Yu’s molding compound 18 would have advantageously provided the opportunity for such shielding in Yu’s package. *See, e.g., EX1137* at 6:1-10, 3:38-41, FIGS. 6-7 (providing a metal power plane 61 (i.e., a shielding layer) that “eliminates crosstalk” within dielectric layers 67, 68).

323. The combination is the application of a known technique (an encapsulant thickness) to a known device (Yu’s molding compound 18) ready for improvement to yield predictable results. A POSITA would have had a reasonable expectation of success in applying Lin-191’s solid layer thickness to Yu’s compound 18 because the range was a common thickness for molding layers in chip packaging before the ’306 Patent. *See* ¶¶ 51-53. Additionally, Lin-191’s encapsulating layer 85 is, like Yu’s molding compound 18 (*solid layer*) formed by a “molding process[.]”

EX1005 at [0109]; *EX1010* at 2:65-66 (“The molding compound 18 can be applied using...compression molding.”). Because Lin-191’s and Yu’s solid layers are formed using the same process, a POSITA would have had a reasonable expectation of success in using Yu’s molding process to form molding compound 18 according to Lin-191’s layer 85 thickness.

5. ***1(a)(iii): “wherein said solid layer comprises a first region and a second region between said first region and a first edge of said solid layer;”***

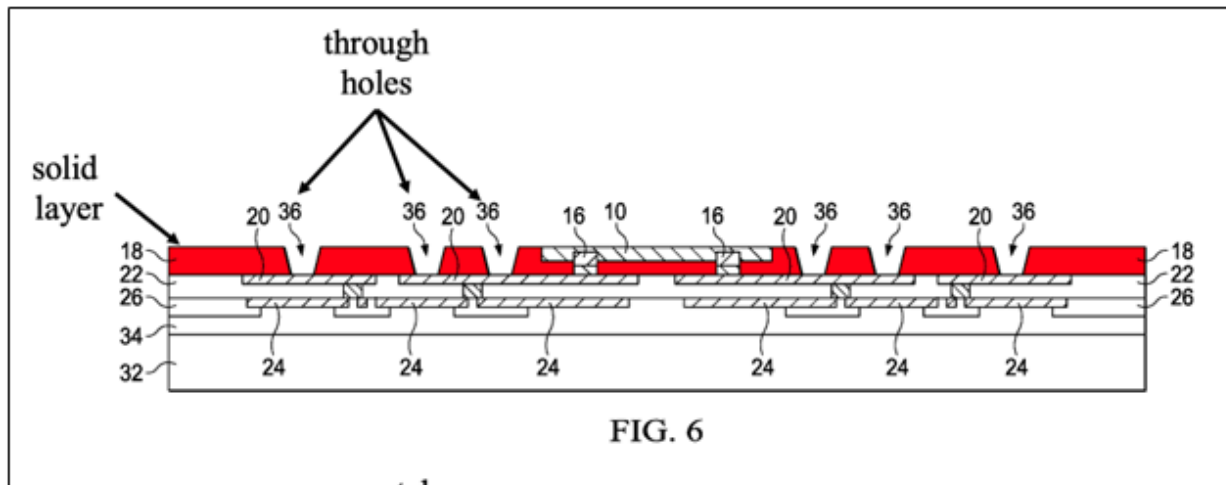
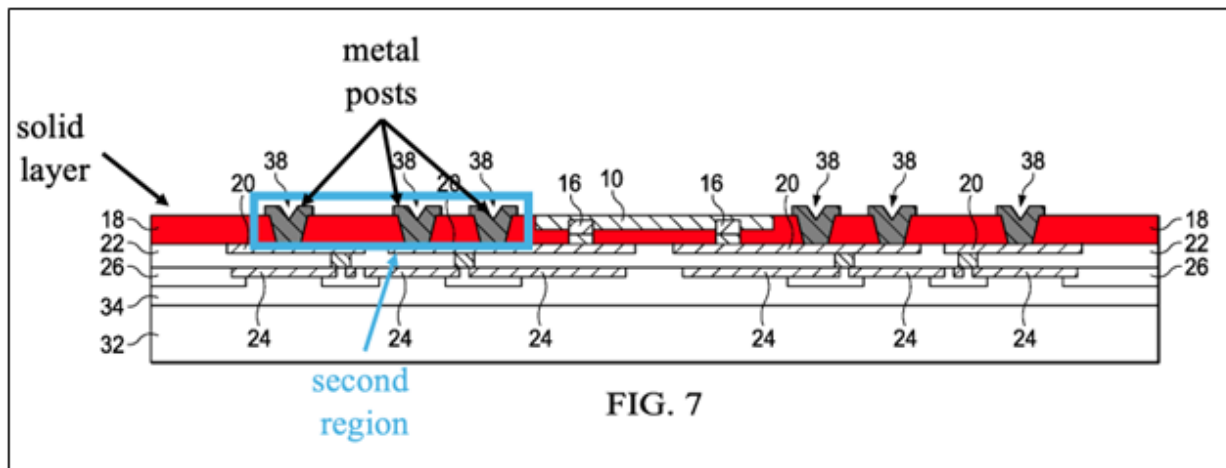
324. Shown below, Yu’s molding compound 18 (*solid layer*) comprises a *first region* (green) and a *second region* (blue). The *second region* is *between said first region and a first edge* (indicted by the purple line) of said solid layer:



EX1010 at FIG. 16.

6. ***1(b): “a plurality of metal posts in a plurality of through holes in said second region respectively,”***

325. Yu teaches that “TMV [through molding via] openings 36 are formed through the molding compound 18,” and that “a seed layer is deposited ... into the TMV openings 36,” followed by deposition of a “conductive material.” *EX1010* at 3:56–4:6. Yu further teaches that both the seed layer and the conductive material are copper, thereby forming copper-filled through vias within the molding compound. *Id.* As a result, the TMVs 38 shown in Yu correspond to a *plurality of metal posts* extending through the molding compound 18, each positioned within a corresponding TMV opening 36. The copper seed and conductive layers together form solid metallic structures within the through holes, yielding *a plurality of metal posts in a plurality of through holes*, i.e., the TMV openings 36. These through holes are located in the *second region*, as depicted in Yu’s figure below, which illustrates TMVs 38 formed in molding compound 18 in *said second region*.

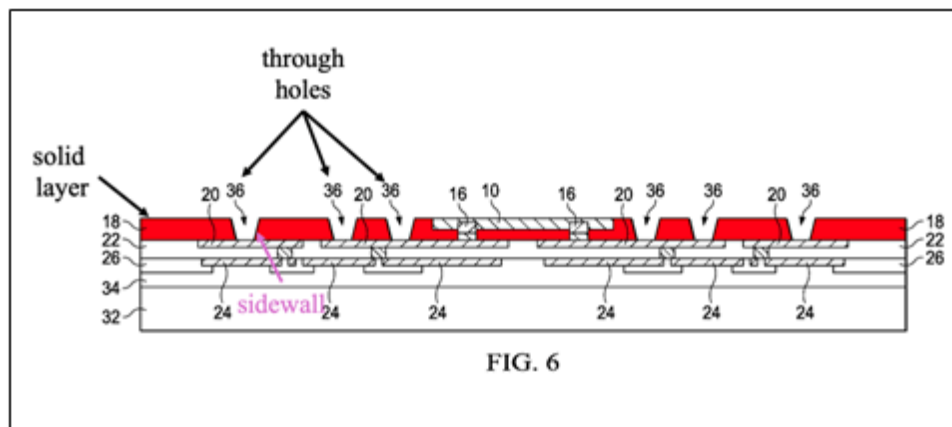


EX1010 at FIGS. 6-7.

7. *1(b)(i): “wherein one of said plurality of metal posts comprises a first copper layer contacting a sidewall of one of said plurality of through holes,”*

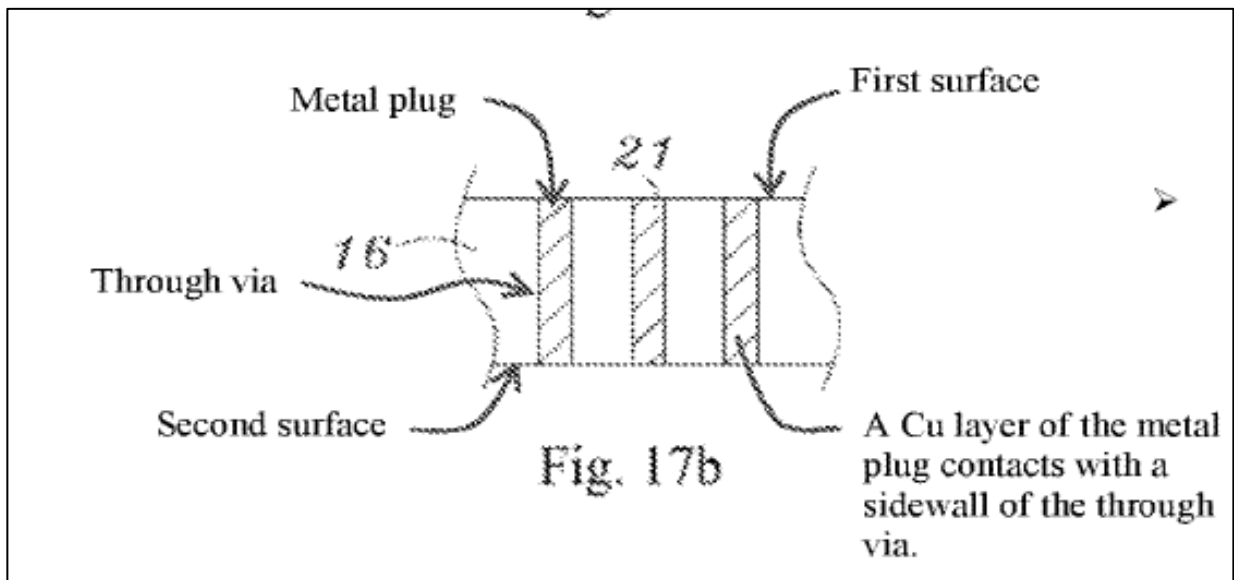
326. Yu teaches that a “seed layer is deposited ... into the TMV openings 36,” and further identifies the seed layer material as copper. EX1010 at 3:60–64. In Yu, the TMV openings 36 extend through the molding compound 18 to expose the surfaces of underlying conductive regions, and the deposition of the copper seed

layer coats the interior surfaces of those openings. *EX1010* at 2:64-3:19; 10:29-33. Thus, the deposited copper seed layer forms a copper layer that contacts the sidewalls of the TMV openings 36. In this way, the copper seed layer of the *metal posts* is a *first copper layer contacting a sidewall of one of said plurality of through holes*. The copper seed layer forms the conductive base upon which additional copper material is subsequently plated to fill the TMV openings 36.



EX1010 at FIG. 6.

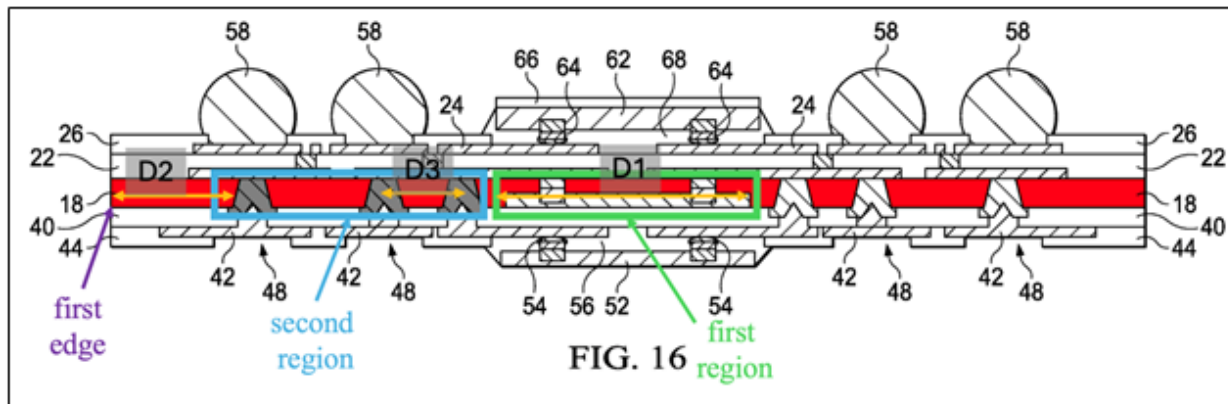
327. I note that Yu's teachings mirror Patent Owner's statements during original prosecution in the related '768 Patent, where FIG. 17B is annotated to state "A Cu layer of the metal plug contacts with a sidewall of the through via." *EX1032* at p. 537.



EX1032 at p. 537.

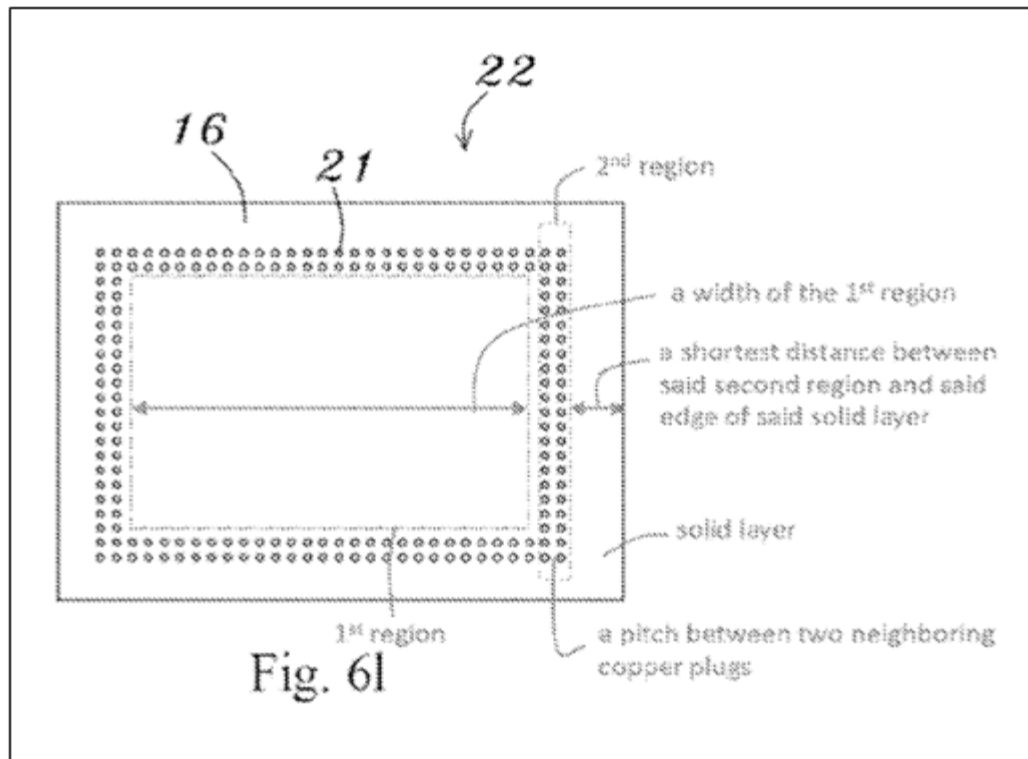
8. ***1(b)(ii): “wherein said first region has a width in a direction greater than a shortest distance between said sidewall of one of said plurality of through holes and said first edge in said direction and greater than a pitch between two neighboring metal posts of said plurality of metal posts;”***

328. As shown below in FIG. 16, Yu’s *first region* has a width in a direction (denoted D1) greater than a shortest distance between said sidewall of one of said plurality of through holes and said first edge in said direction (denoted D2), and greater than a pitch between two neighboring metal posts (denoted D3) of said plurality of metal posts.



EX1010 at FIG. 16.

329. Shown below is annotated FIG. 61 provided by PO during original examination of the '306 Patent's parent application, illustrating alleged support for the claimed *width*, *shortest distance*, and *pitch*. As shown above, Yu's *first* and *second* regions mirror this arrangement. The claimed *regions* are not described in the '306 Patent's written description. Applicant relied solely on Applicant-annotated FIG. 61.

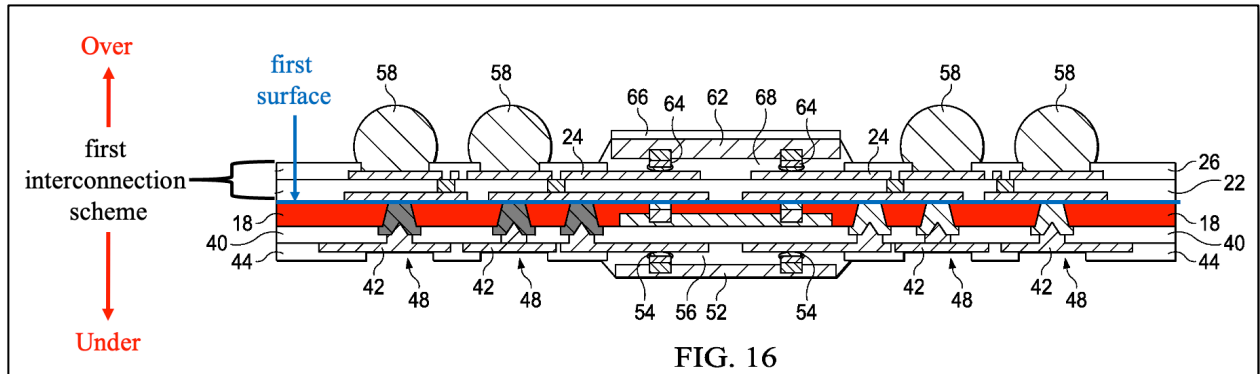


EX1117 at p. 272.

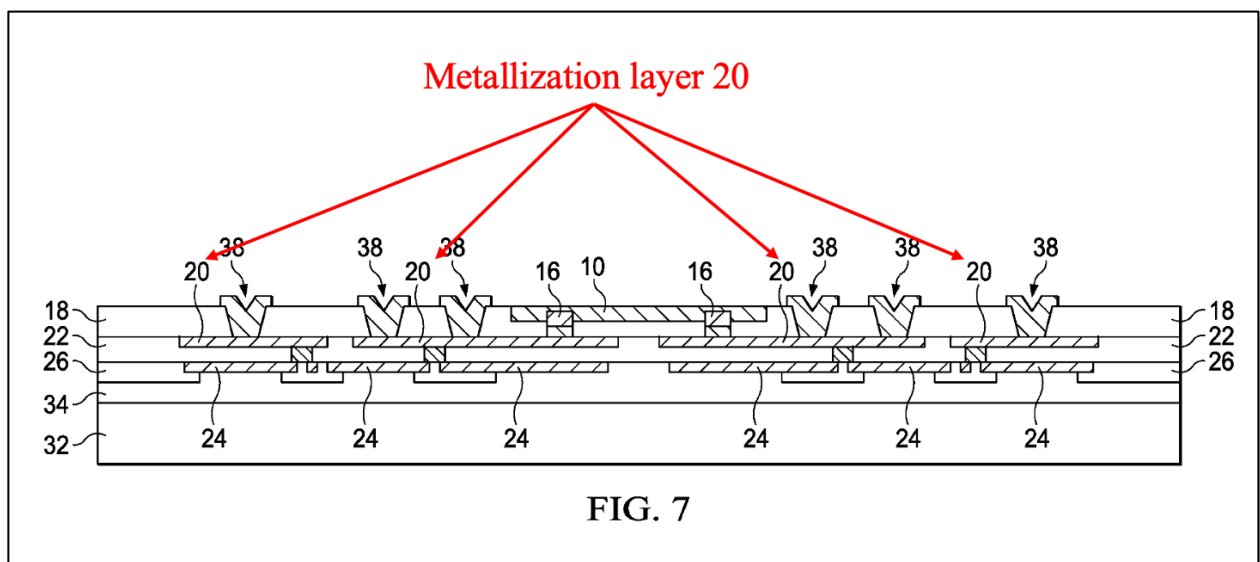
9. **1(c): “a first interconnection scheme over said first surface,”**

330. Yu teaches a “front side interlayer dielectric (ILD) and redistribution layer (RDL) structure.” *EX1010* at 3:4-5. In particular, a seed layer is deposited on the molding compound 18 and patterned to form a “first front-side metallization layer 20.” *EX1010* at 3:5-19. A “first ILD layer 22” is then deposited over layer 20 and subsequent metallization and ILD layers are formed, including a second metallization layer 24 and a second ILD layer 26, with openings 28 and 30 formed in the topmost front-side ILD for connectors. *EX1010* at 3:4-19. These layers are all on the molding compound 18 and constitute a *first interconnection scheme* over the

first surface. EX1010 at 3:4-19 (front-side ILD/RDL over molding compound 18; first metallization layer 20), 3:20-27 (first ILD layer 22), 3:28-43 (subsequent metallization/ILD including layers 24 and 26; openings 28, 30).



EX1010 at FIG. 16. I note that metallization layer 20 is assigned a reference numeral in FIGS. 4-7 and 10-11 which depict steps of forming the package 202 of FIG. 16, while the reference numeral for layer 20 in FIG. 16 above is omitted. *See, e.g.,*



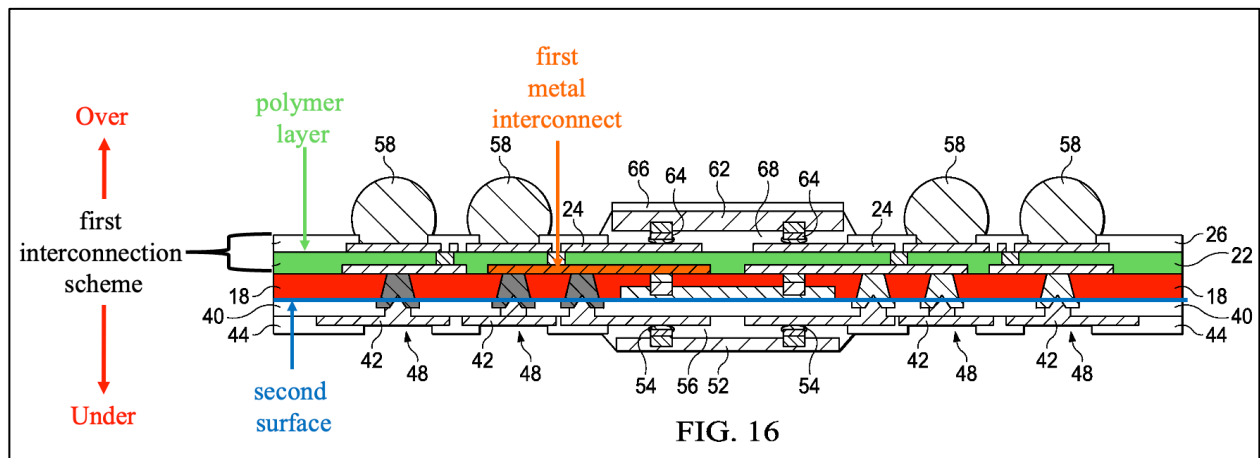
EX1010 at FIG. 7.

10. 1(c)(i): “wherein said first interconnection scheme comprises a first metal interconnect over said second surface and a polymer layer over said first metal interconnect,”

331. Yu teaches that “a seed layer, such as a copper” is “deposited on the molding compound 18” then a “[c]onductive material of the first metallization layer, such as copper... is deposited on the exposed seed layer.” *EX1010* at 3:8–18. Yu further explains that “the remaining conductive material forms the first front-side metallization layer 20.” *EX1010* at 3:18–20.

332. Because metallization layer 20 comprises copper, a portion of metallization layer 20 is a *first metal interconnect* and is disposed over the *second surface* of the molding compound 18 (*solid layer*), as shown below.

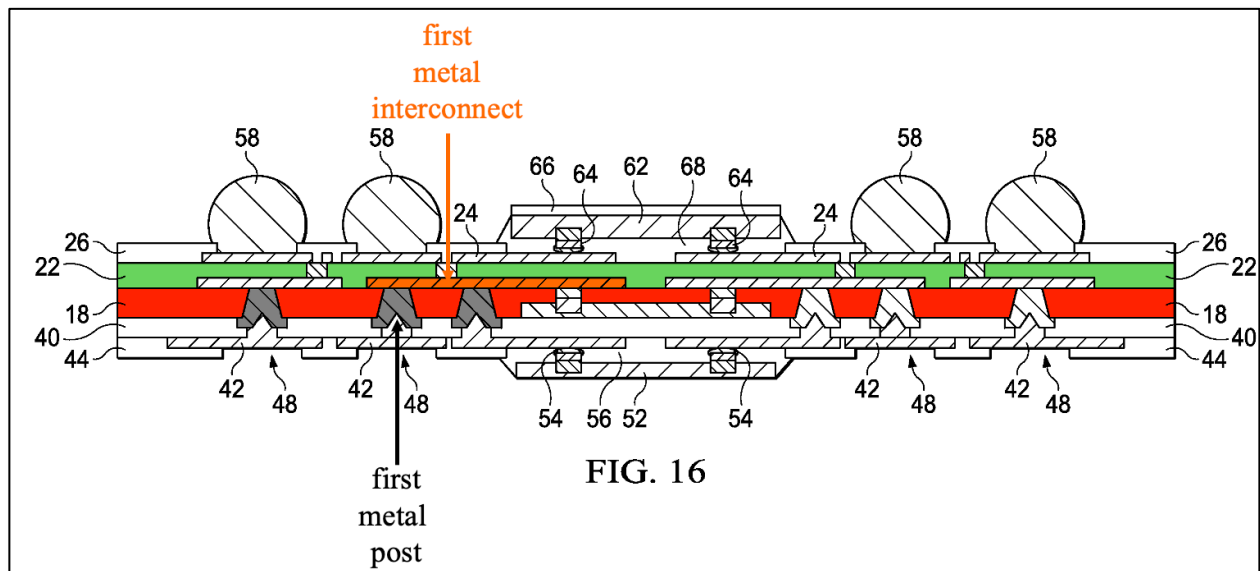
333. Yu further teaches that “a first ILD layer 22 is deposited on the front side and over the first metallization layer 20. The first ILD layer 22 may be a polyimide, polybenzoxazole (PBO), benzocyclobutene (BCB), the like, or a combination thereof.” *EX1010* at 3:21–27. Thus, ILD layer 22 comprises a polyimide and is a *polymer layer* formed over metallization layer 20. Accordingly, Yu teaches a copper metallization layer 20, a portion of which is the *first metal interconnect*, and a polymer ILD layer 22 disposed over metallization layer 20.



EX1010 at FIG. 16.

11. 1(c)(ii): “wherein said first metal interconnect is connected to a first metal post of said plurality of metal posts,”

334. As shown below, Yu teaches that “TMV [through molding via] openings 36 are formed through the molding compound 18 to the first front side metallization layer 20,” followed by deposition of a seed layer and electroplating of a conductive material such as copper to form TMVs 38. EX1010 at 3:5-19. The TMVs 38 extend through the molding compound 18 and make electrical contact with the first front-side metallization layer 20. Accordingly, metallization layer 20 (*first metal interconnect*) is connected to a first metal post of said plurality of metal posts. In other words, because Yu teaches that the TMV openings 36 are formed to the first front-side metallization layer 20 and subsequently filled with copper to form TMVs 38 in contact with that layer, the *first metal post* is connected to the *first metal interconnect*.



EX1010 at FIG. 16.

12. 1(c)(iii): “wherein said first metal interconnect comprises a first metal layer and a second copper layer over said first metal layer;”

335. Yu teaches “a front side interlayer dielectric (ILD) and redistribution layer (RDL) structure.” 3:4-5. To form the RDL, a “seed layer, such as copper...is deposited on the molding compound 18” then “conductive material of the first metallization layer, such as copper...is deposited on the exposed seed layer, such as by...electroplating” EX1010 at 3:5–14. Yu further explains that the remaining conductive material forms “the first front side metallization layer 20.” EX1010 at 3:18–20. Thus, metallization layer 20 includes a copper seed layer deposited directly on the molding compound 18 and a copper conductive layer deposited on top of the seed layer. Accordingly, the copper seed layer is a *first metal layer*, and the copper

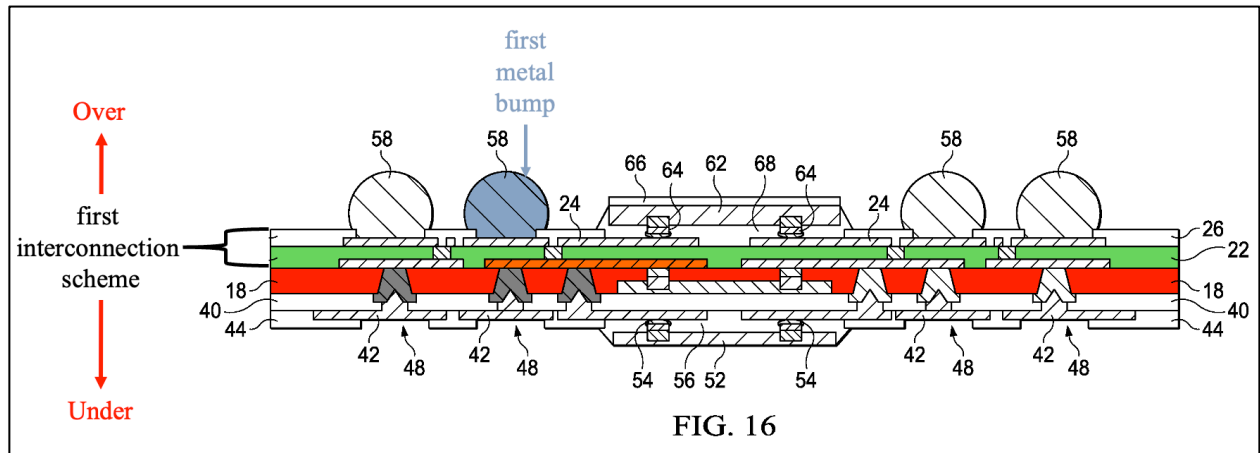
conductive material plated on the seed layer is *a second copper layer over the first metal layer*.

13. 1(d): “a first metal bump over said first interconnection scheme”

336. Yu teaches that “conductive connectors 58, such as ball grid array (BGA) balls,” are “formed on the front side of the package in the openings 28,” and are “formed on [] bond pads.” *EX1010* at 4:45–49. Yu further explains that the openings 28 are formed through the topmost ILD layer 26 to expose portions of the “topmost front-side metallization layer, such as the second metallization layer 24,” to which the connectors are electrically coupled. *Id.* at 3:31–36. Yu also teaches that the conductive connectors 58 may be “lead-free solder” and “may be formed on the bond pads” provided by metallization layer 24. *Id.* at 4:47–50. These connectors 58 are positioned on the front side of the package above the multilayer ILD/RDL stack, including metallization layers 20 and 24 and ILD layers 22 and 26, that together form the *first interconnection scheme*.

337. Accordingly, connector 58 is *a first metal bump over said first interconnection scheme*, because Yu expressly teaches that conductive connectors (BGA balls) 58 are formed on the front side of the package and in electrical contact with the upper metallization layer of the interconnection structure. Alternatively,

connector 58 together with its underlying bond pad (formed from metallization layer 24) collectively form a *first metal bump* over said first interconnection scheme.



EX1010 at FIG. 16.

14. 1(d)(i): “wherein said first metal bump comprises a second metal layer and a first tin-containing layer over said second metal layer; and”

338. Yu teaches that “connectors 58 may be a lead-free solder.” EX1010 at 4:47–50. Yu further explains that the connectors 58 are “formed on the front side of the package in the openings 28” and “formed on [] bond pads,” thereby showing that the solder connectors 58 are disposed over and electrically connected to the upper metallization layer of the front-side interconnection structure. *Id.* at 4:45–49.

339. A POSITA would have understood (A) the bond pad to be metal, as metal bond pads were, and remain, ubiquitous in semiconductor packaging for connecting solder balls to underlying redistribution layers, and (B) the “lead-free

solder” to include tin. A POSITA would have understood Yu’s lead-free solder to be a *tin-containing layer* Sn-based solders were dominant in commercial packages such as those taught by Yu. Thus, the context of the chip packages of Yu means that “solder” necessarily includes Sn-content, thereby teaching the *tin-containing layer*. A POSITA would have understood Yu’s disclosure of “lead-free solder” to mean the solder contains tin unless stated otherwise. That is, if someone refers to non-tin-containing solder, it would be specified as such because the “default” solder contains tin.

340. Accordingly, Yu teaches a structure in which the metallization bond pad is a second metal layer and the solder connector 58 is a tin-containing layer over said second metal layer, because the lead-free solder connector is formed on the bond pad. *EX1010* at 4:45–50. Thus, Yu teaches *wherein said first metal bump comprises a second metal layer and a first tin-containing layer over said second metal layer*.

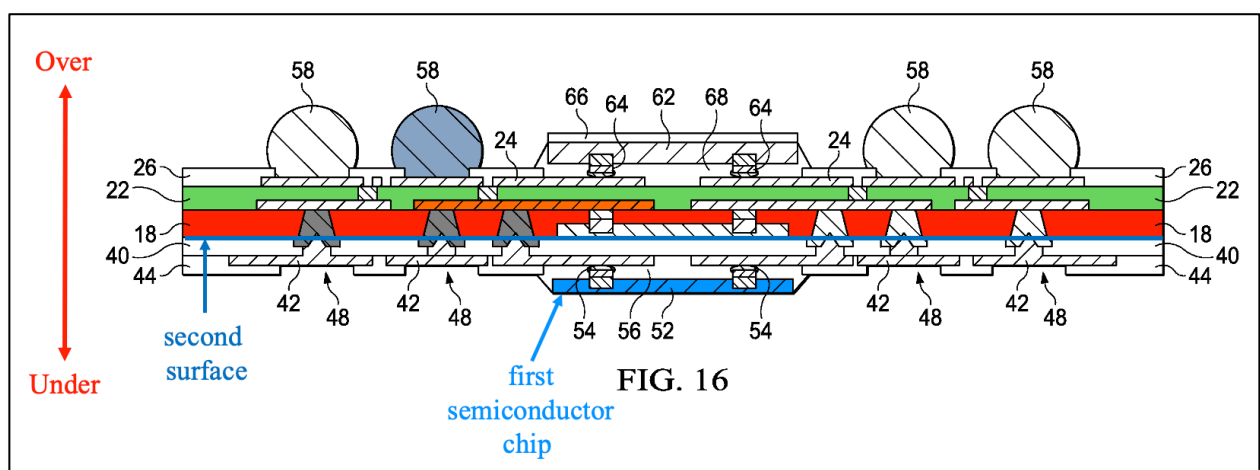
a) Lin-191’s Teachings and Motivation to Combine

341. Additionally, Lin-191 teaches a metal bump comprising *a second metal layer and a first tin-containing layer over said second metal layer*. See ¶ 151, incorporated herein. A POSITA would have been motivated, found it obvious, and had a reasonable expectation of success in modifying Yu per Lin-191 for the same reasons discussed for Sundaram-Lin-191. See ¶¶ 153-158, incorporated herein. The

Yu-Lin-191 combination is application of known technique (Lin-191's solder bump structure) to a known device (Yu's connector and pad) ready for improvement to yield predictable results, i.e., Yu's connector 58 comprising a *first tin-containing layer* over a *second metal layer* (UBM layer).

15. 1(e): “a first semiconductor chip under said second surface,””

342. Yu's package includes “die 52, such as a memory die,” (*first semiconductor chip*) which is attached on the back side of the package. *EX1010* at 4:30–36. Yu explains that the back side of the package includes “TMVs 38” extending through the molding compound 18 and that conductive connectors are formed between the die 52 and those vias to establish electrical communication. *Id.* at 4:28–44. As shown in Yu's FIG. 16, die 52 is positioned *under said second surface*.

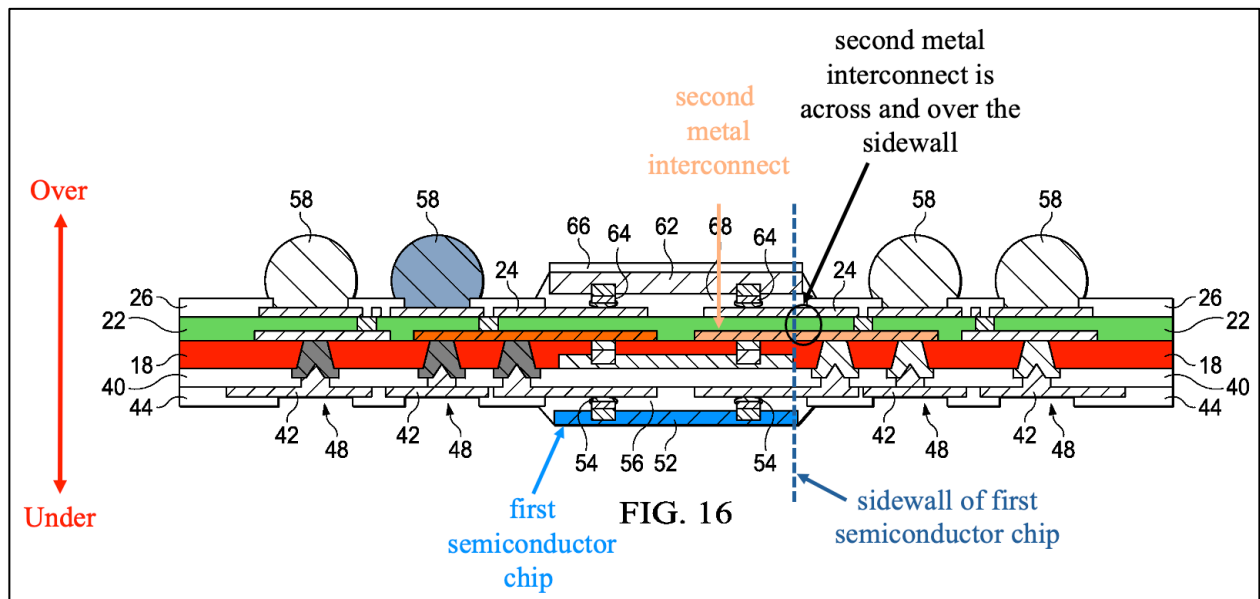


EX1010 at FIG. 16.

16. 1(e)(i): “wherein said first interconnection scheme comprise a second metal interconnect across over a sidewall of the first semiconductor chip,”

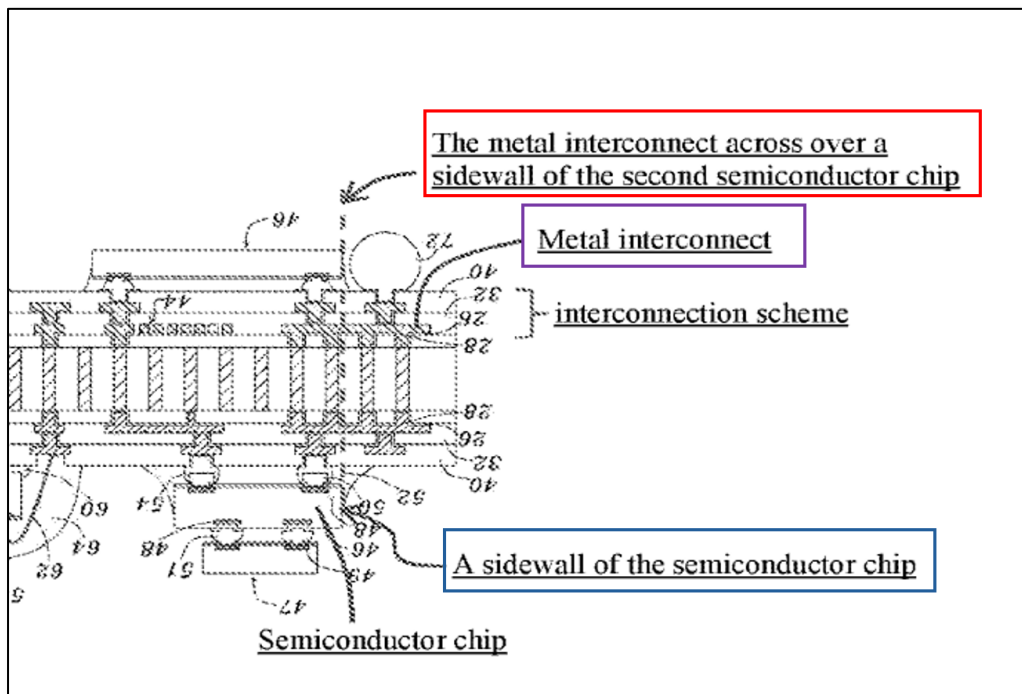
a) “Second Metal Interconnect”

343. For the same reasons described above, another portion of metallization layer 20 is a *fourth metal interconnect* that is part of the *first interconnection scheme*. See ¶¶ 331-332; *EX1010* at 3:5–20. Further, as shown below, the *second metal interconnect* is both *across* and *over* a *sidewall* of die 52 (*first semiconductor chip*). The blue dashed line indicates the *sidewall* of die 52, namely a boundary thereof. Notably, the *second metal interconnect* is positioned in the “over” direction relative to the *sidewall*, as indicated by the red arrow depicting the over/under directions. Additionally, the *second metal interconnect* extends laterally (i.e., left/right) to the right past the boundary of the *sidewall*. Thus, the *second metal interconnect* is both *across* and *over* a *sidewall* of the *first semiconductor chip*.



EX1010 at FIG. 16.

344. I note that Yu's teachings of the *second metal interconnect* being *across* and *over* the *sidewall of the first semiconductor chip* are consistent with an annotated figure that Patent Owner provided during prosecution of the related '768 Patent, arguing support for this specification. In the figure below, I have shown how the Patent Owner's annotations mirror the above mapping of Yu's *fourth metal interconnect*.



EX1032 at p. 537.

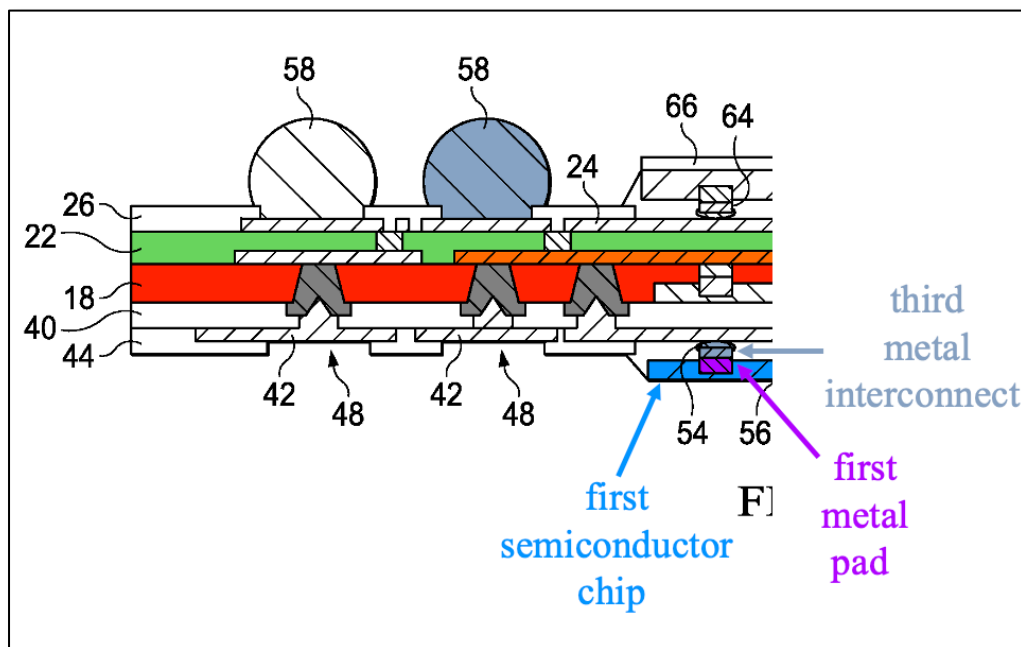
17. 1(e)(ii): “wherein said first semiconductor chip comprises a third metal interconnect on a first metal pad of said first semiconductor chip,”

345. Yu teaches that die 52 “is attached...to conductive features in the second back side metallization layer 42, such as by conductive connectors 54, like controlled collapse chip connection (C4) bumps.” EX1010 at 4:30–34. Connector 54 thus provides the conductive pathway that couples die 52 to metallization layer 42 and functions as *a third metal interconnect on a first metal pad of said first semiconductor chip*.

346. Connector 54 is formed on the underside of die 52, establishing both mechanical and electrical contact to the back-side metallization. Yu’s explicit

reference to “C4 bumps” reflects the standard flip-chip interconnect process in which solder bumps (metal interconnects) are deposited directly on metal bond pads of the semiconductor die. *See* ¶ 70. Accordingly, a POSITA would have understood that Yu’s die 52 includes a metal bond pad underlying each C4 bump, since such pads are required for reliable solder attachment and electrical continuity in C4 packaging.

347. Thus, Yu teaches that die 52 comprises *a first metal pad* and a connector 54 functioning as *a third metal interconnect on that first metal pad*. EX1010 at 4:30–34; FIG. 16.



EX1010 at FIG. 16 (excerpt).

348. A POSITA would have understood the **rectangle** portion of die 52 to be a *metal pad* of die 52 given that “I/O terminals were traditionally formed by way of metal pads along the periphery of an IC.” *EX1095* at 1:24-25. As shown, the C4 bump/connector 54 (*third metal interconnect*) is *on the first metal pad*. *EX1010* at 4:30-34.

a) Lin-191’s Metal Pad Teachings and Motivation to Combine

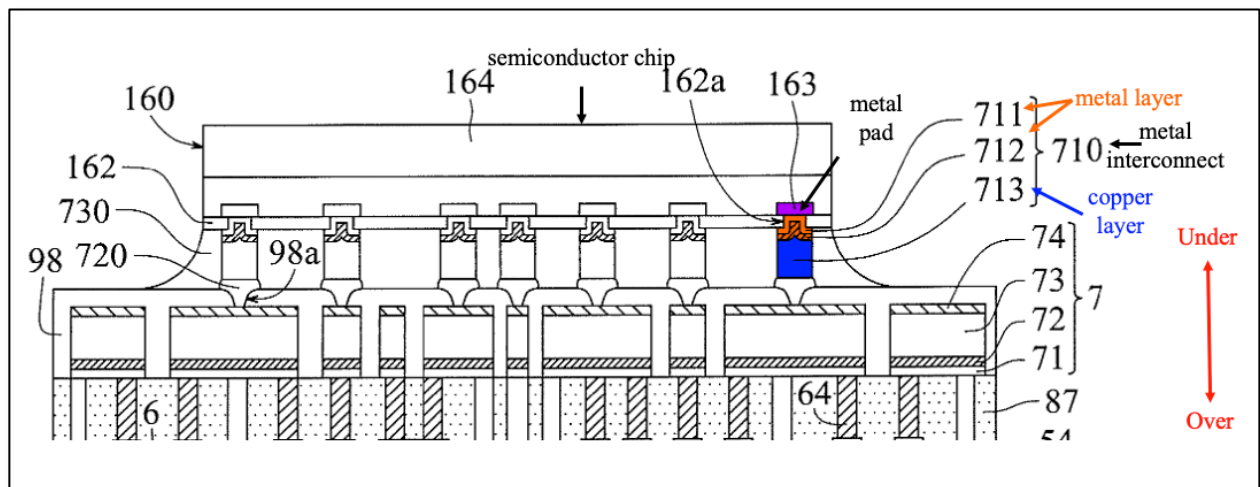
349. In addition to Yu, Lin-191 teaches a semiconductor chip 160 with “metal traces or pads 163” that include “aluminum.” *EX1005*, [0384]; *see* ¶ 165, incorporated herein. A POSITA would have been motivated and found it obvious to apply Lin-191’s teachings of a *metal pad* to Yu’s C4 bumps, thereby yielding the predictable result of Yu’s *first semiconductor chip* (die 52) having C4 bumps on the *first...pad* that is *metal*. As I described above, Yu already teaches die 52 comprising connector 54, i.e., the claimed *first pad*, and Lin-191 merely provides additional specificity that the pad is *metal*. *See* ¶¶ 345-347. Modifying Yu’s connector 54 to be metal, thereby yielding a *first metal pad*, is merely an implementation detail in Yu’s overall system, i.e., Lin-191 provides the specificity of a semiconductor contact pad being *metal*. Thus, for the same motivations described above, a POSITA would have been motivated to modify Yu’s connector 54 to be a *first metal pad*. *See* ¶¶ 166-167, incorporated herein.

350. The combination is the application of known metal pad techniques to Yu's die 52 to yield the predictable result of die 52 having a *metal pad*. *EX1005* at [0081]. As I described above, metal contact pads were ubiquitous, so a POSITA would have had a reasonable expectation of success in modifying Yu's pad to be *metal*, such as aluminum, per Lin-191. *See* ¶¶ 166-167.

18. *1(e)(iii): “wherein said third metal interconnect comprises a third metal layer on said first metal pad and a third copper layer over said third metal layer, wherein said third copper layer has a thickness between 5 and 30 micrometers,”*

a) Lin-191's Teachings and Motivation to Combine

351. Lin-191 teaches or renders obvious interconnects/bumps with layers/thickness as recited in Claim 1(e)(iii). *See* ¶¶ 168-169, incorporated herein.



EX1005 at FIG. 72 (excerpt).

352. A POSITA would have found it obvious and been motivated to modify Yu's connector for the reasons discussed with respect to Sundaram, i.e., improved

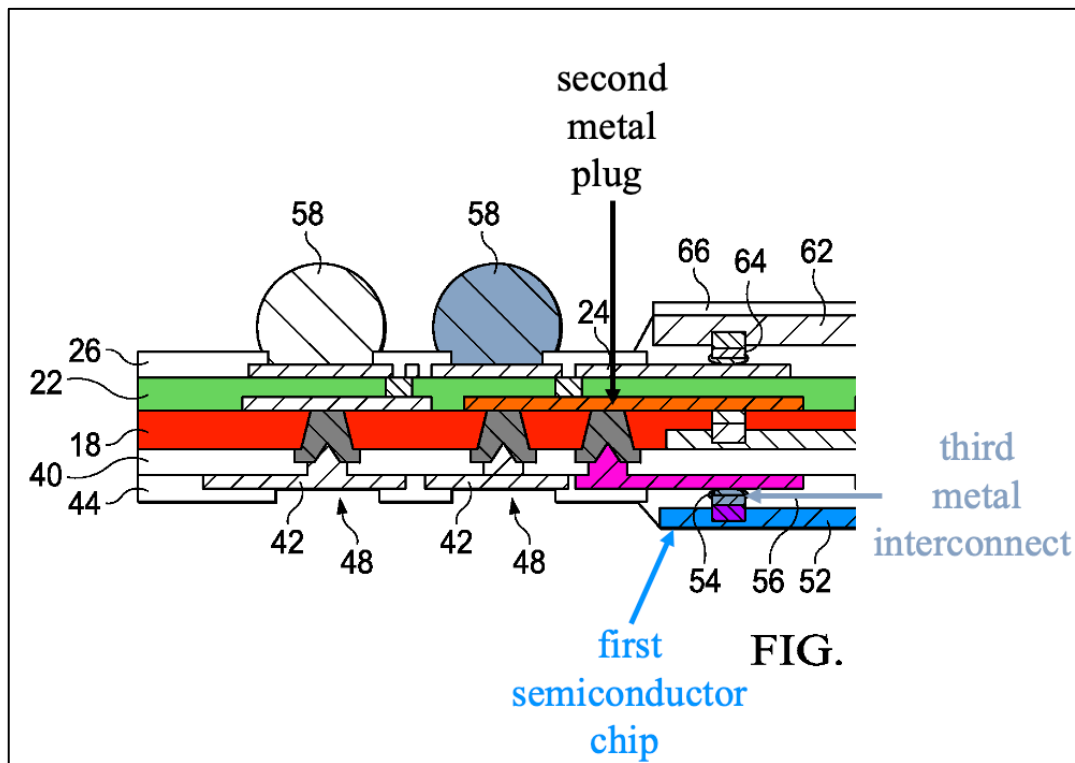
metallurgical bonding and increased resistance to fatigue and stress-induced failure. See ¶¶ 170-176, incorporated herein. Yu, like Lin-191's underfill 730, teaches an underfill material 56 such that the thickness of the *third copper layer* would advantageously provide ample space for Yu's underfill material 56 to be positioned. *EX1010* at 4:39-40; see ¶ 174. Layered bumps, per Lin-191, were routinely manufactured using techniques already contemplated by Yu, leading to a reasonable expectation of success. For example, Lin-191 teaches using a "sputtering process[.]" "physical-vapor deposition (PVD) process," and electroplating, which are all techniques taught by Yu. *EX1005* at [0400], [0413]; *EX1010* at 3:5-8 ("A seed layer...is deposited...such as by sputtering or another physical vapor deposition process.), 3:11-14 ("Conductive material...is deposited...such as by...electroplating[.]").

19. 1(e)(iv): "wherein said first semiconductor chip is connected to a second metal post of said plurality of metal posts through said third metal interconnect."

353. Yu teaches that the die 52 is electrically coupled to the TMVs 38 through the second back side metallization layer 42 and conductive connectors 54. *EX1010* at 4:7-11, FIG. 16. As shown in Yu's FIG. 16, the TMVs 38 extend through the molding compound 18 from the front-side metallization structure to the back-side metallization layer 42, where they provide conductive vertical posts connecting

the two sides of the package. Die 52 is mounted beneath the back-side metallization layer 42 and joined to it by conductive connectors 54, which Yu describes as controlled-collapse chip connection (C4) bumps. *EX1010* at 4:30-35.

354. Accordingly, Yu discloses that die 52 is connected to *a second metal post* (TMV 38) through connector 54 and a portion of the second back side metallization layer 42. The metallization layer 42 serves as the horizontal routing layer that interfaces with the vertical TMV 38, while connector 54 provides the physical and electrical coupling between the die 52 and that metallization structure. A POSITA would have recognized that this configuration establishes a conductive path from die 52, through connector 54, across metallization layer 42, and into TMV 38, thereby electrically linking the semiconductor die to the front-side interconnection network of the package.



EX1010 at FIG. 16.

B. Claim 2: “The chip package of claim 1, wherein said first semiconductor chip comprises a central-processing-unit (CPU) circuit block and a graphics-processing-unit (GPU) circuit block.”

a) Lin-191’s Teachings

355. See ¶ 178, incorporated herein.

b) Motivation to Combine

356. The same MTCs and reasonable expectation of success for modifying Sundaram per Lin-191 apply to modifying Yu per Lin-191, e.g., increasing the functionality of Yu’s chip package. See ¶¶ 179-180, incorporated herein.

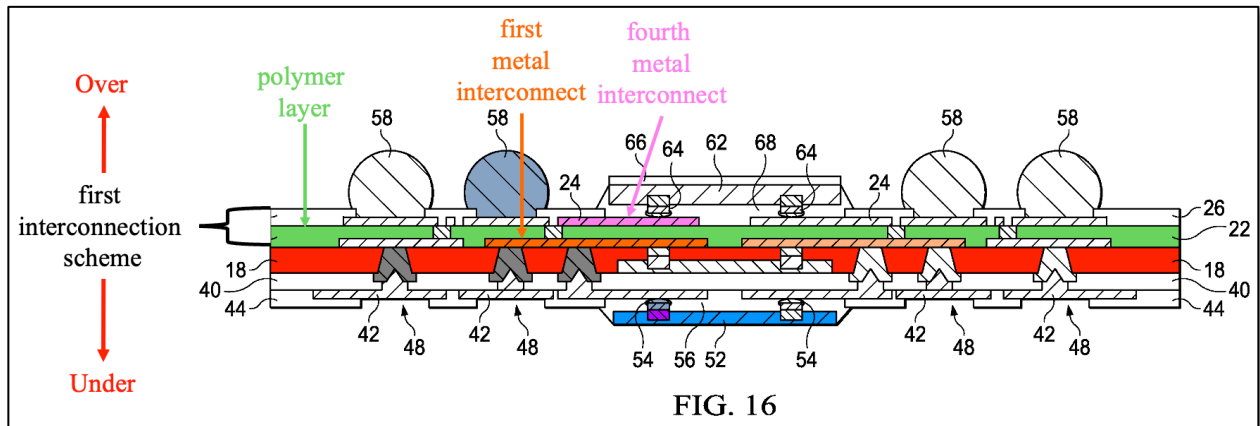
Additionally, Yu, like Sundaram, contemplates “mobile telephone/PDA[s].” *EX1010* at 1:53-55.

C. Claim 3

- 1. 3(a): “The chip package of claim 1, wherein said first interconnection scheme further comprises a fourth metal interconnect over said first metal interconnect and said polymer layer,”**

357. As I described above, Yu teaches a sequence of stacked metallization and dielectric layers forming a multi-level interconnect structure on the front side of the package. *EX1010* at 3:28–32; see ¶ 330. The second metallization layer 24 is “formed using the same process” as metallization layer 20 is formed (i.e., with a seed layer and conductive material such as copper formed over the seed layer) such that a portion of layer 24 is a *fourth metal interconnect*. *EX1010* at 3:5–32; ¶ 331.

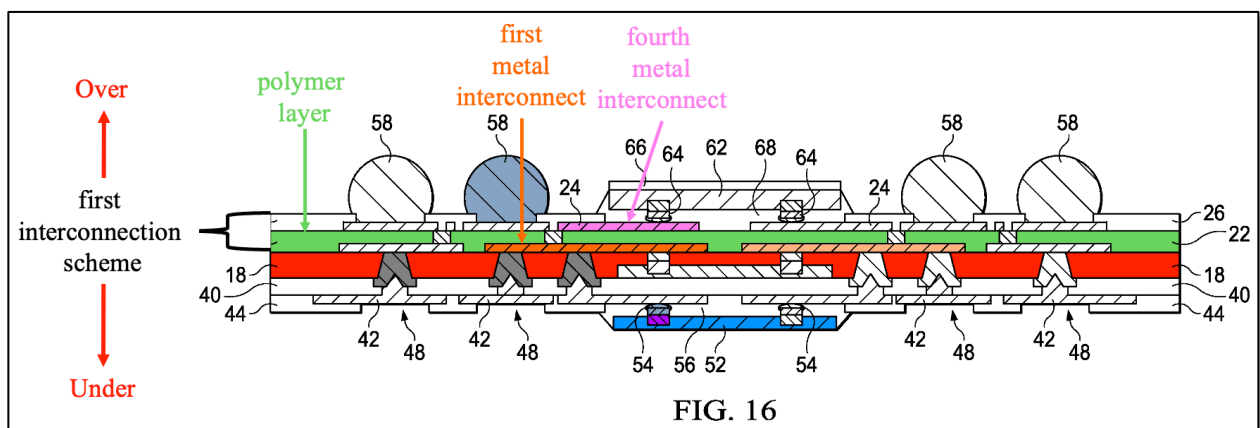
358. As shown, Yu’s metallization layer 24 (*fourth metal interconnect*) is *over said first metal interconnect and said polymer layer*, as indicated by the red arrow depicting the over/under directions:



EX1010 at FIG. 9B.

2. 3(b): “wherein said polymer layer is between said first and fourth metal interconnects,”

359. Metallization layer 24 is on ILD layer 22, which is “over the first metallization layer 20” such that ILD layer 22 is between layers 20, 24. EX1010 at 3:20-32. Thus, the polymer layer is between said first and fourth metal interconnects:



EX1010 at FIG. 16.

3. **3(c): “wherein said fourth metal interconnect comprises a fourth metal layer and a fourth copper layer over said fourth metal layer.”**

360. As I described above, Yu teaches metallization layers (e.g., metallization layer 24) are formed using a “seed layer, such as copper” and then a “conductive material[,]” also copper, is formed on the copper seed layer. *See* ¶ 331; *EX1010* at 3:8-18. Metallization layer 24 is “formed using the same process” as metallization layer 20[.]” *EX1010* at 3:5–32; ¶ 357. Thus, the *second metal interconnect comprises a fourth metal layer* (copper seed layer) and a *fourth copper layer over said fourth metal layer* (copper portion).

- D. Claim 4: “The chip package of claim 1, wherein said first metal pad is an aluminum pad.”**

a) Lin-191’s Teachings and MTC

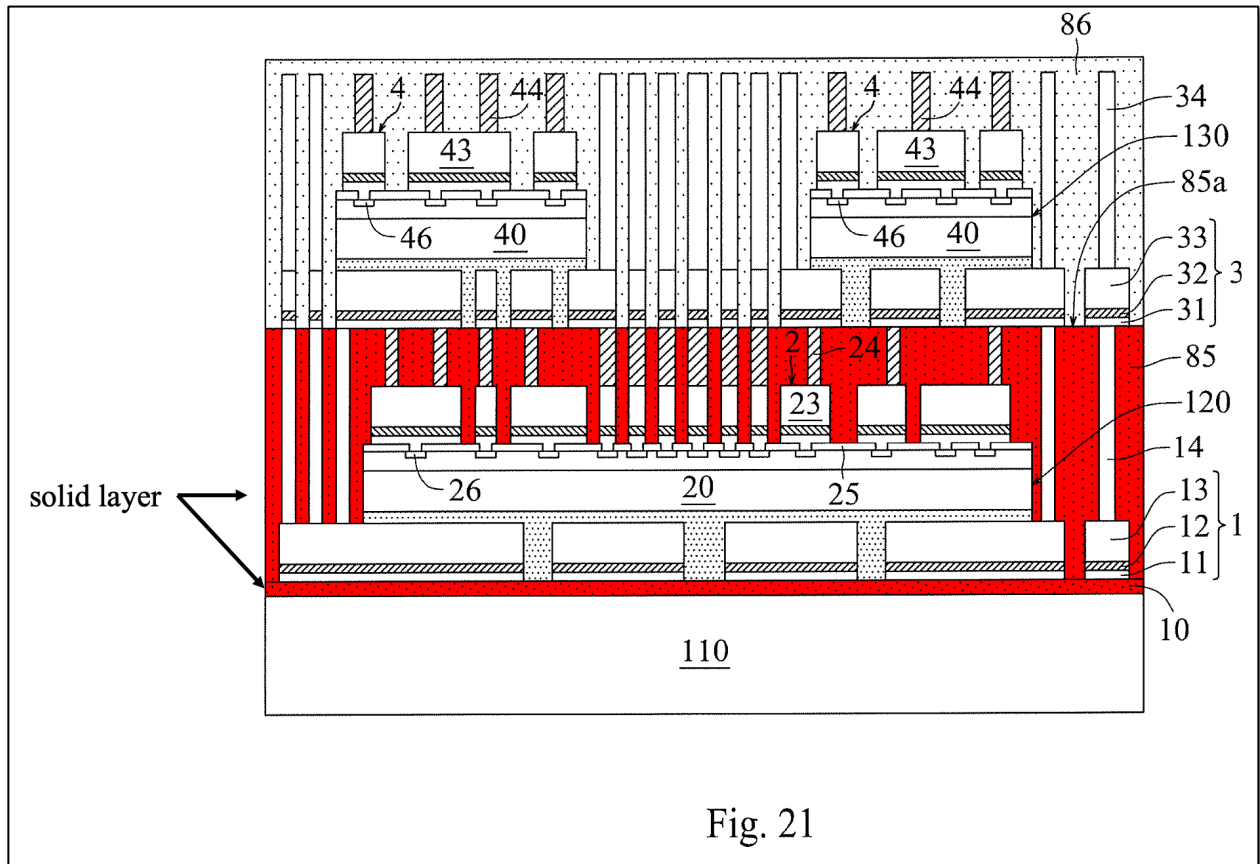
361. *See* ¶ 194 for Lin-191’s teachings of an *aluminum pad*, incorporated herein. The same MTCs and reasonable expectation of success for Sundaram-Lin-191 apply to Yu. *See* ¶ 195, incorporated herein.

- E. Claim 5: “The chip package of claim 1, wherein said compound comprises a SiO₂ compound.”**

a) Lin-191’s Teachings and Motivation to Combine

362. *See* ¶¶ 316-318. Lin-191’s *solid layer* includes encapsulating layer 85 (discussed at Claim 1(a)(ii)) and further includes an insulating layer 10, which is

made of “silicon dioxide (SiO₂)” and over which layer 85 is “formed.” *EX1005* at [0052], [0109].



EX1005 at FIG. 12.

363. Yu teaches molding compound 18 comprises “epoxy, polyimide, silicone rubber, the like, or a combination thereof,” i.e., *a compound of silicon and oxygen*. *EX1010*, 2:61-65; see ¶ 315. Lin-191 specifically teaches SiO₂. In the combination, Yu is modified per Lin-191 such that *said compound* is the combination of Yu’s molding compound 18 and Lin-191’s insulating layer 10,

Because insulating layer 10 is SiO₂, the Yu-Lin-191 compound *comprises a SiO₂ compound*. *EX1010* at FIGS. 34–35; 8:35–39 (formation of silicon-based interposer structure using oxide isolation layers).

b) Motivation to Combine

364. A POSITA would have been motivated and found it obvious to modify Yu's molding compound 18 to include an SiO₂ insulating layer as taught by Lin-191 for multiple reasons such that Yu's *solid layer* (molding compound 18) is modified to include an SiO₂ layer similar to Lin-191's teachings of a *solid layer* comprising encapsulating layer 85 and insulating SiO₂ layer 10.

365. First, Yu itself expressly recognizes silicon-oxide-based materials as standard insulating and structural components in its own PoP and interposer packages. Yu discloses that the carrier substrate may comprise “glass, silicon oxide, aluminum oxide, [a] combination thereof, and/or the like” and later describes the interposer's “isolation layer 144 [which] can be, for example, silicon oxide...” *EX1010* at 5:2-5, 6:35-39. Thus, Yu already employs SiO₂ as a dielectric and barrier material within its package architecture. A POSITA would have recognized that forming a thin SiO₂ insulating layer beneath or within Yu's molding compound 18 would be a routine design choice consistent with Yu's own teaching of silicon oxide use throughout the package.

366. Second, a POSITA would have understood that incorporating an SiO₂ layer improves water-vapor and ion barrier performance relative to Yu's polymeric molding compound. Water vapor permeability is a common problem in die encapsulation as greater water presence leads to increased oxidation, corrosion, and enhanced ion-movement. Yu teaches using silicone rubber and epoxy materials for molding compound 18. *EX1010* at 2:61-65. Combining these with a deposited SiO₂ layer, such as Lin-191's insulating layer 10, would reduce moisture diffusion, minimizing oxidation and corrosion of Yu's copper through-mold vias 38 and metallization layers 20, 24. Thus, the addition of an SiO₂ layer to Yu's package would reduce water vapor penetration, increasing the reliability of Yu's package. Additionally, because Yu's package contains multiple Cu interfaces within the molding compound and interposer, a POSITA would have recognized the benefit of adding an silicon dioxide barrier to increase reliability and prevent ion migration and delamination during thermal cycling. *See EX1010* at 3:5-18; 6:36-41.

367. Third, a POSITA would have appreciated that the SiO₂ layer would enhance electrical and thermal insulation between Yu's conductive structures without departing from Yu's process flow. Yu teaches depositing and curing polyimide and oxide-type dielectrics by CVD, spin-coat, or lamination processes throughout its ILD and RDL formation steps. *EX1010* at 3:21-32; 6:35-39. These are

the same fabrication techniques Lin-191 teaches for forming its SiO₂ insulating layer. *EX1005* at [0050]. Accordingly, the addition of a SiO₂ film beneath Yu's molding compound would have been straightforward and predictable for one of ordinary skill.

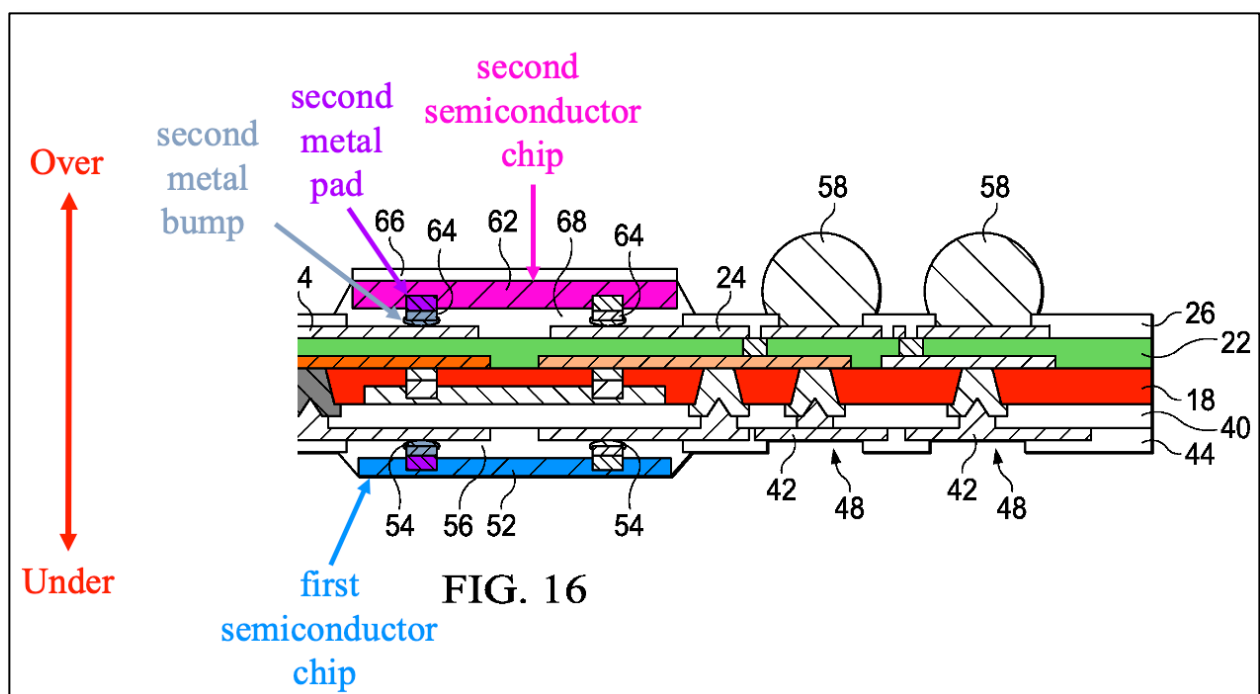
368. Thus, the Yu-Lin-191 combination represents the application of a known technique (silicon dioxide barrier layer) to a known device (Yu's chip package) ready for improvement to yield predictable results, i.e., a silicon dioxide layer on Yu's molding compound 10. The combination would result in reduced moisture permeation, improved dielectric strength, and enhanced thermal stability—using materials and processes explicitly taught in Yu. A POSITA would have had a reasonable expectation of success because Yu already uses SiO₂ layers in its carrier substrates and interposer structures), making integration of an SiO₂ compound within the molding system a predictable optimization. *EX1010* at 5:2-5; 6:35-39. Further, Lin-191 teaches layer 10 is formed via “a chemical-vapor deposition (CVD) process, a spin-coating process or a lamination process,” which are all techniques also disclosed by Yu, making the modification simple and straightforward. *EX1005*, [0050]; *EX1010*, 7:16-18.

F. Claim 6

1. **6(a): “The chip package of claim 1, further comprising a second semiconductor chip over said first semiconductor chip,**

wherein said second semiconductor chip comprises a second metal bump on a second metal pad of said second semiconductor chip,”

369. Yu teaches a “die 62, such as a memory die,” that is “attached...to conductive features in the second front-side metallization layer 24,” such that die 62 is a *second semiconductor chip over die 52 (first semiconductor chip)*. EX1010 at 4:53-56. Yu’s FIG. 16 shows die 62 positioned over the first die 52, establishing a stacked configuration characteristic of a package-on-package (PoP) or multi-chip package architecture. In this arrangement, die 52 resides beneath the molding compound 18, while die 62 is mounted above the front-side redistribution structure that includes metallization layers 20 and 24. Accordingly, Yu teaches a *second semiconductor chip over said first semiconductor chip*:



EX1010 at FIG. 16.

370. Shown above, die 62, like die 52, includes interconnect structures that enable electrical coupling to the underlying metallization features. Yu specifies that die 62 is connected through “connectors 64, such as controlled collapse chip connection (C4) bumps,” which “attach to the conductive features in the second front-side metallization layer 24.” *EX1010* at 4:56-60. As I discussed above, C4 bumps (e.g., Yu’s connectors 54, 64) were known to comprise a metal bump and metal pad, such that Yu’s *second semiconductor chip* comprises a *second metal bump on a second metal pad*. See ¶¶ 70, 346.

371. Additionally or alternatively, the combination of Yu-Lin-191 teaches a *second metal bump on a second metal pad*. See ¶¶ 349-350. For the same MTCs and with the same reasonable expectation of success, a POSITA would have found it obvious and been motivated to obvious to apply Lin-191’s teachings of a *metal pad* to Yu’s C4 bumps, thereby yielding the predictable result of Yu’s *second semiconductor chip* (die 62) having C4 bumps on the *second...pad* that is *metal*. See ¶¶ 349-350, incorporated herein.

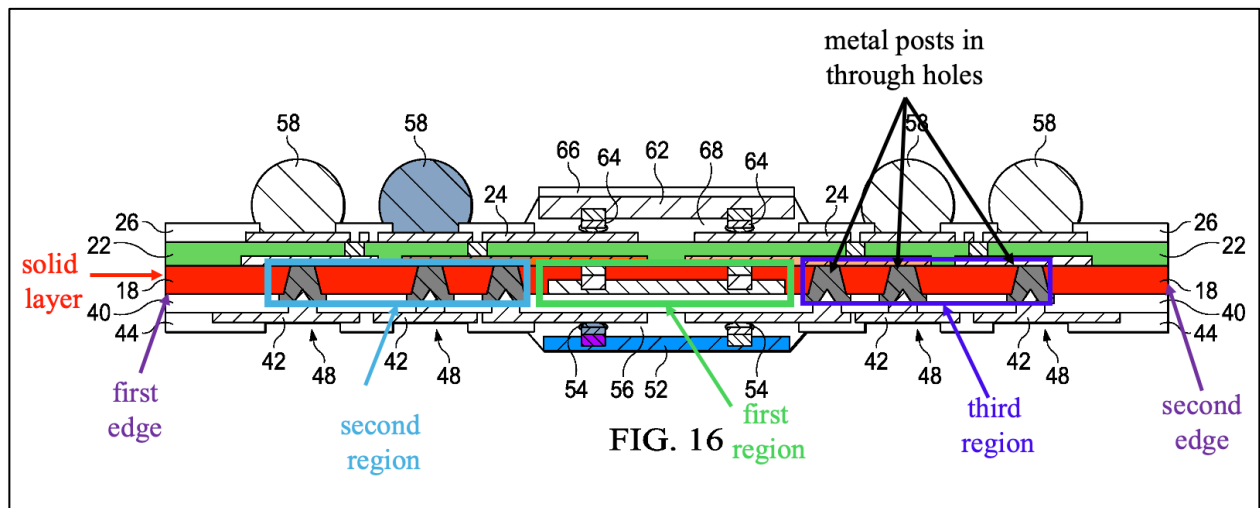
2. 6(b): “wherein said second metal bump comprises a second tin-containing layer.”

372. Yu alone, or in combination with Lin-191, teaches *wherein said second metal bump comprises a second tin-containing layer*. See ¶¶ 338-341. Yu teaches

that die 62 is connected to metallization layer 24 by “connectors 64, such as controlled collapse chip connection (C4) bumps.” *EX1010* at 4:53-60. A POSITA would have understood these C4 connectors to be solder-based interconnects formed of tin-containing alloys (e.g., SnAg or SnAgCu), as such materials were the dominant lead-free solders used in commercial packaging. *EX1094* at [0003]; ¶ 70. Accordingly, each connector 64 is a *second metal bump comprising a second tin-containing layer* formed over a metal pad of die 62.

G. Claim 7: “The chip package of claim 1, wherein said solid layer further comprises a third region opposite to said second region, wherein said third region is between said first region and a second edge of said solid layer, wherein said plurality of metal posts in said plurality of through holes in said third region respectively.”

373. Yu’s molding compound 18 (*solid layer*) comprises a *third region*, shown below, which is on the *opposite* side of the *first region* than the *second region* and is, therefore, *opposite to said second region*. The *third region* is *between said first region* (green) *and a second edge of said solid layer*. Additionally, the *third region* comprises a *plurality of metal posts in said plurality of through holes*, as shown:

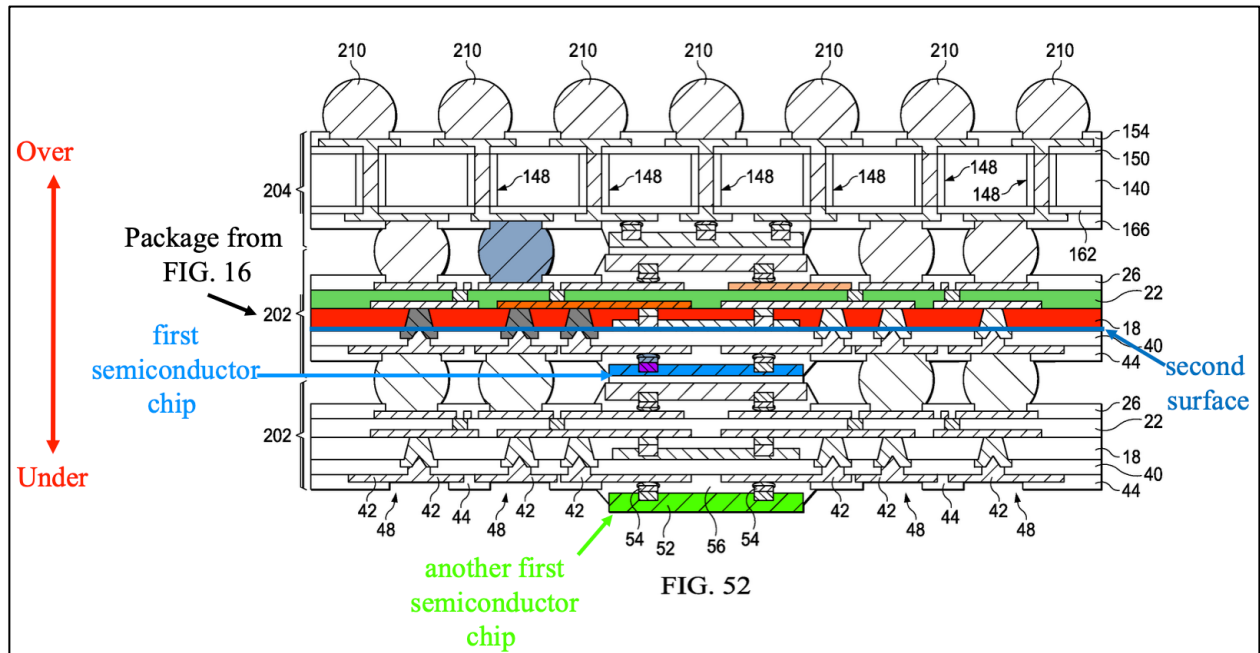


EX1010 at FIG. 16.

H. Claim 9: “The chip package of claim 1, further comprising another said first semiconductor chip under said second surface.”

374. Yu’s FIG. 52 illustrates a package-on-package (PoP) structure that includes multiple stacked instances of the FIG. 16 package, as discussed above. *See* ¶¶ 311-312. FIG. 16’s package 202 is one unit of the PoP stack shown in FIG. 52, and Yu teaches that “multiple packages 202 ... can be stacked in the PoP structure.” *EX1010* at 8:35–39; 8:11–12. Each stacked package 202 includes the same configuration shown in FIG. 16. namely, molding compound 18, metallization layers 20 and 24, and a die 52 disposed under the second surface of the package. *EX1010* at FIG. 17 and FIG. 17. Accordingly, FIG. 52’s PoP embodiment includes another package 202 positioned below FIG. 16’s package 202, and that lower package

includes another memory die 52, i.e., *another said first semiconductor chip under said second surface*.



EX1010 at FIG. 52.

I. Claim 10

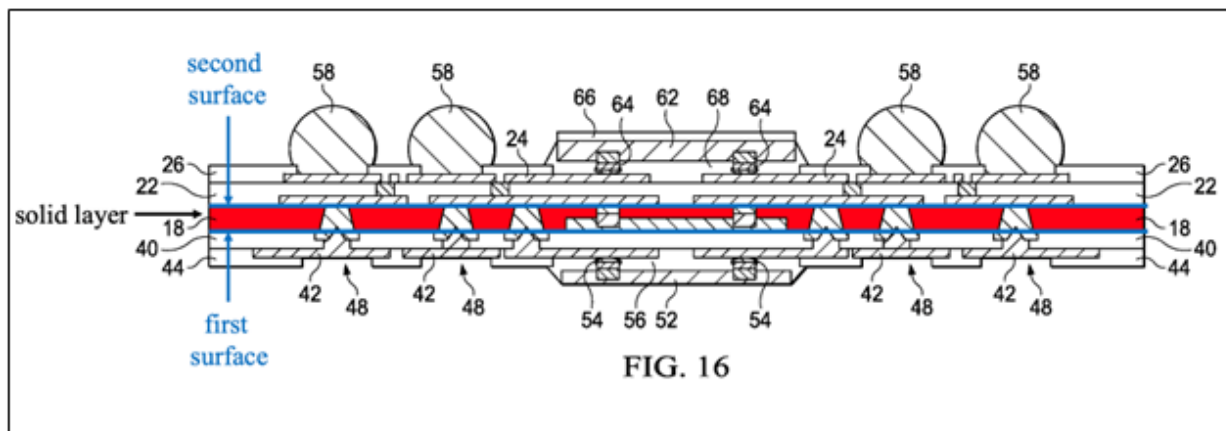
1. 10(Pre): “A chip package comprising:”

375. See ¶¶ 309-311, incorporated herein.

2. 10(a): “a solid layer having a first surface and a second surface opposite to said first surface,”

376. See ¶¶ 313-314, incorporated herein. In the mapping for Claim 1, Yu’s front side (where the ILD/RDL structure and connectors 58 are located) was identified as the *first surface*, and the back side (where die 52 is attached) as the *second surface*. For Claim 10, however, the orientation is reversed such that Yu’s

back side corresponds to the *first surface* and the front side corresponds to the *second surface*. This reversal maintains internal consistency with the structural hierarchy required by Claim 10, where the semiconductor chip resides below the interconnection structure, and ensures that “over” and “under” relationships are preserved in accordance with Yu’s figures and descriptions. *See, e.g., EX1010* at FIGS. 7–8, 16).



EX1010 at FIG. 16

3. **10(a)(i): “wherein said solid layer comprises a compound of silicon and oxygen,”**

377. See ¶ 315, incorporated herein.

4. **10(a)(ii): “wherein said solid layer has a thickness between 100 and 300 micrometers,”**

378. See ¶¶ 316-318, incorporated herein. Lin-191’s encapsulating layer 85 has a thickness “between about 20 and about 500 micrometers.” *EX1005* at [0109]. Similar to my opinions provided for Sundaram for Ground 1A (¶ 206), Lin-191

teaches or renders obvious the claimed *thickness between 100 and 300 micrometers*. *EX1005* at [0109]-[0111]. Because Lin-191 teaches a range (“between about 20 and about 500 micrometers”) that includes the narrower claimed range of *between 100 and 300 micrometers*, Lin-191 at least renders obvious Claim 10(a)(ii). Additionally, the range of between 23.011 micrometers and 121.3 similarly teaches or renders obvious the claimed range of *between 100 and 300 micrometers*. See ¶ 318. Similar to my opinions provided at ¶ 208, I note that the ’306 Patent does not indicate any specific criticality for the claimed range. Therefore, for the reasons provided here and in ¶ 208, it is my opinion a POSITA would have found the claimed range obvious.

5. ***10)(a)(iii): “wherein said solid layer comprises a first region and a second region between said first region and a first edge of said solid layer;”***

379. See ¶ 324, incorporated herein.

6. ***10(b): “a plurality of copper posts in a plurality of through holes in said second region respectively,”***

380. See ¶ 325, incorporated herein. Because Yu’s TMVs 38 are formed of *copper*, the TMVs 38 are a *plurality of copper posts in a plurality of through holes* (openings 36) *in said second region respectively*.

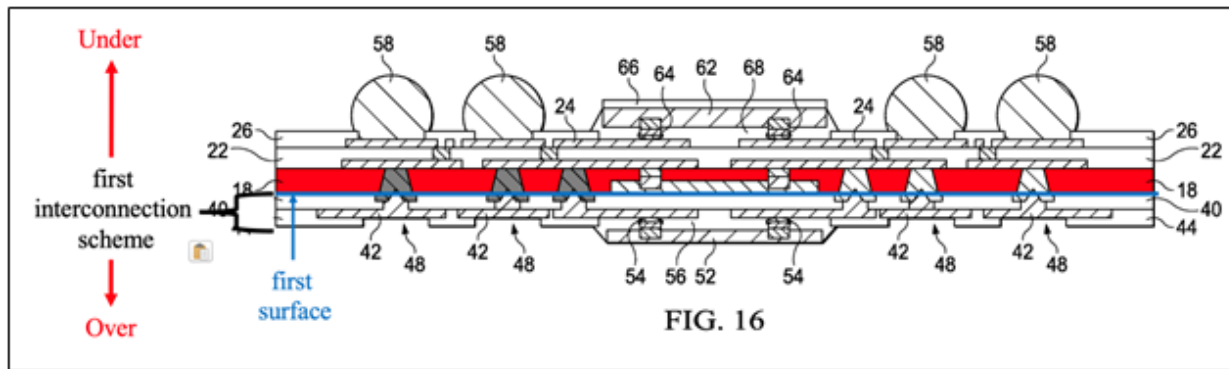
7. ***10(b)(i): “wherein said first region has a width in a direction greater than a shortest distance between a sidewall of one of said plurality of through holes and said first edge in said***

direction and greater than a pitch between two neighboring copper posts of said plurality of copper posts;”

381. See ¶ 328, incorporated herein.

8. *10(c): “a first interconnection scheme over said first surface,”*

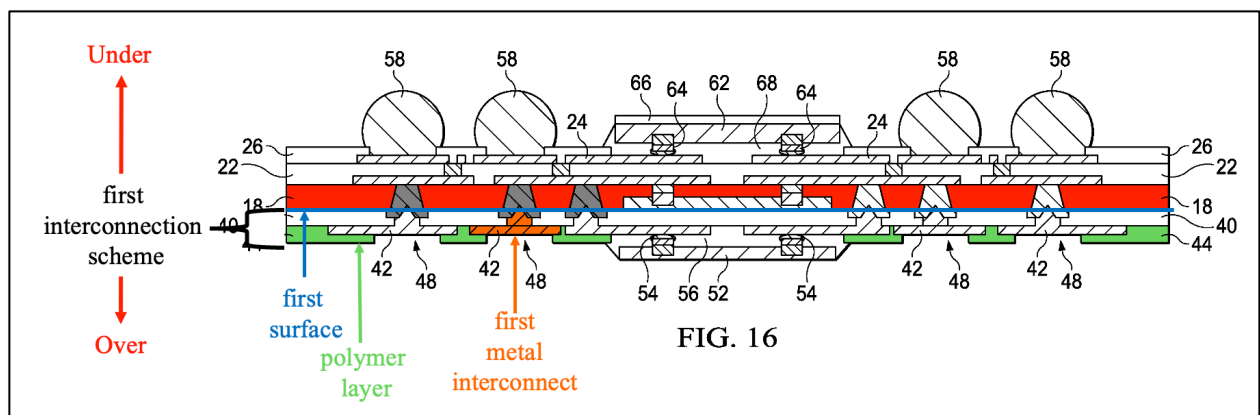
382. See ¶ 330, incorporated herein. Yu teaches that “a back side ILD and RDL structure” includes “a first back side ILD layer 40, a second back side metallization layer 42, [and] a second ILD layer 44.” *EX1010* at 4:7–11. Yu further explains that this multilayer structure is formed on the back side of the molding compound 18 and provides conductive routing for electrical connection to the die 52 through the C4 connectors 54 and to the TMVs 38 extending through the package. *EX1010* at 4:7–14, FIG. 16. Like the front-side ILD and RDL structure, the back side ILD and RDL structure comprises alternating dielectric and metallization layers configured to distribute electrical signals between the package’s conductive elements. A POSITA would therefore have understood that the back side ILD and RDL structure performs the same interconnection function as the front-side ILD/RDL stack, providing patterned metallization over an insulating dielectric to route electrical signals, and thus likewise constitutes *a first interconnection scheme over said first surface*. *EX1010* at 4:7–14, FIG. 16.



EX1010 at FIG. 16

9. 10(c)(i): “wherein said first interconnection scheme comprises a first metal interconnect over said first surface, and a polymer layer over said first metal interconnect,”

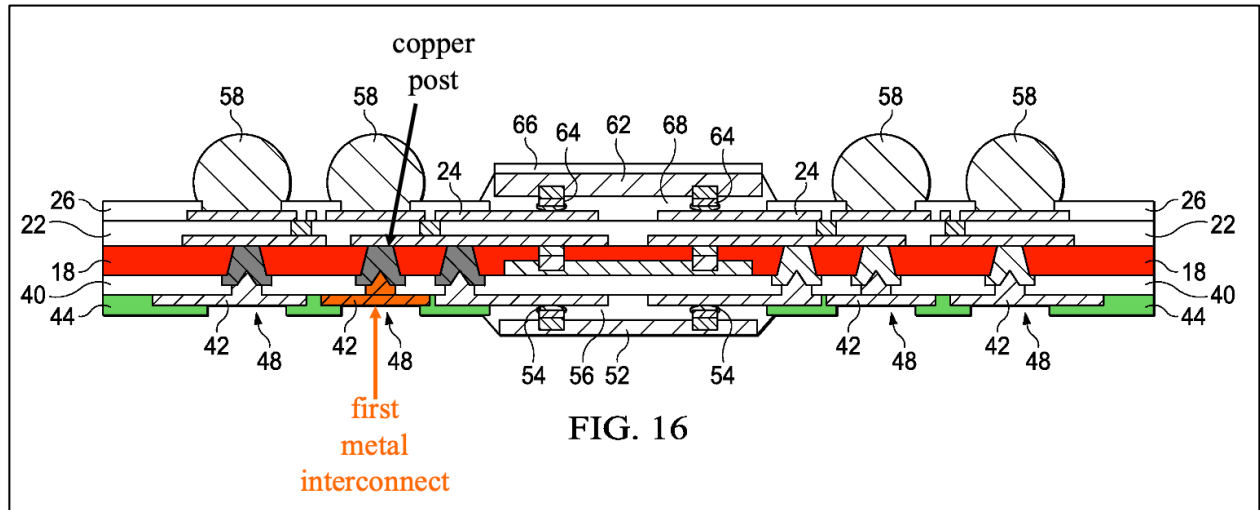
383. See ¶ 331, incorporated herein. A portion of metallization layer 42 is a first metal interconnect over said first surface and ILD layer 44 is a polymer layer over layer 42, which are “formed the similar to or in the same manner as the ILD layers and metallization layers on the front side” (i.e., with a copper seed layer and an electroplated copper layer). EX1010 at 4:7-14, 3:4-19.



EX1010 at FIG. 16.

10. 10(c)(ii): “wherein said first metal interconnect is connected to one of said plurality of copper posts,”

384. See ¶ 334, incorporated herein. Layer 42 is connected to a TMV 38.



EX1010 at FIG. 16.

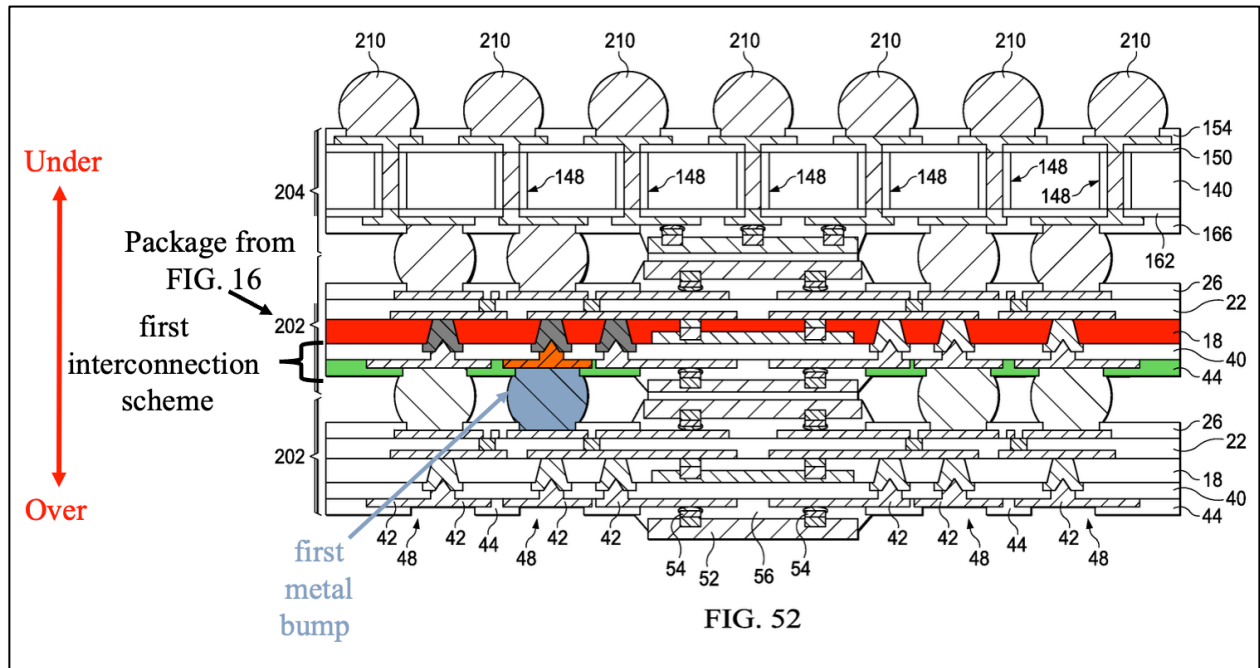
11. 10(c)(iii): “wherein said first metal interconnect comprises a first metal layer and a first copper layer over said first metal layer;”

385. See ¶¶ 335, incorporated herein. Metallization layer 42 (*first metal interconnect*) is formed “in the same manner” as metallization layer 20 and thus likewise comprises a *first metal layer* (electroplated copper portion) and a *first copper layer* (copper seed layer) over said first metal layer.

12. 10(d): “a first metal bump over said first interconnection scheme,”

386. See ¶¶ 336-337, incorporated herein. A connector 58 (*first metal bump*) connects packages 202 in Yu’s FIG. 52 PoP structure. EX1010 at 4:45-47, 8:35-39,

FIGS. 16, 52. Accordingly, FIG. 52's PoP embodiment includes a *first metal bump over said first interconnection scheme*:



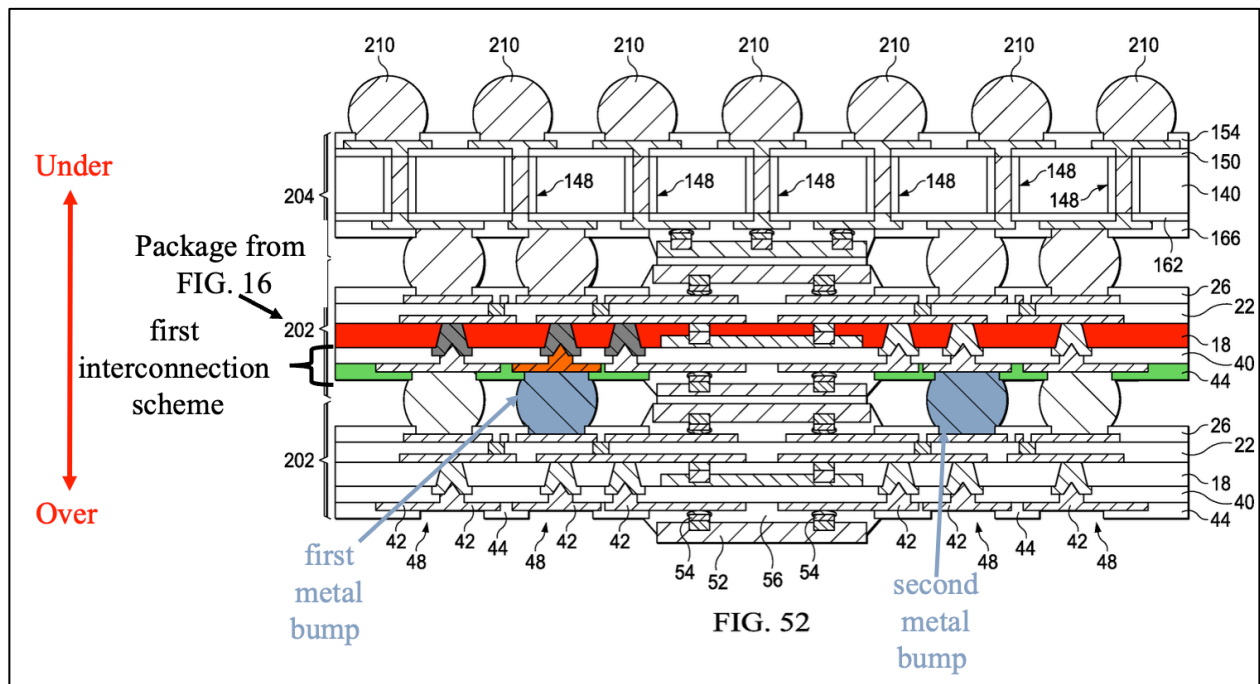
EX1010 at FIG. 52.

13. *10(d)(i): “wherein said first metal bump comprises a first tin-containing layer;”*

387. See ¶¶ 338-341, incorporated herein.

- 14. 10(e): “a second metal bump over said first interconnection scheme;”**

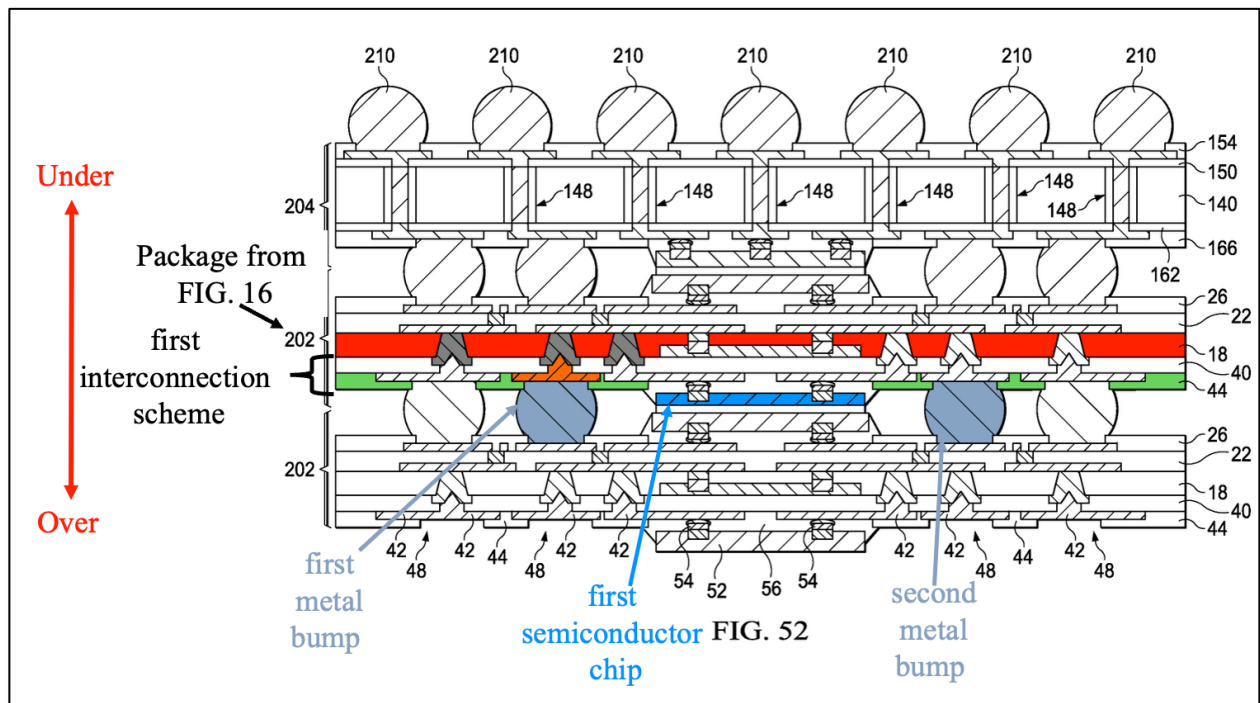
388. For the same reasons described above, Yu teaches a *second metal bump over said first interconnection scheme*:



EX1010 at FIG. 52; see ¶ 386, incorporated herein.

15. 10(f): “a first semiconductor chip over said first interconnection scheme and between said first and second metal bumps,”

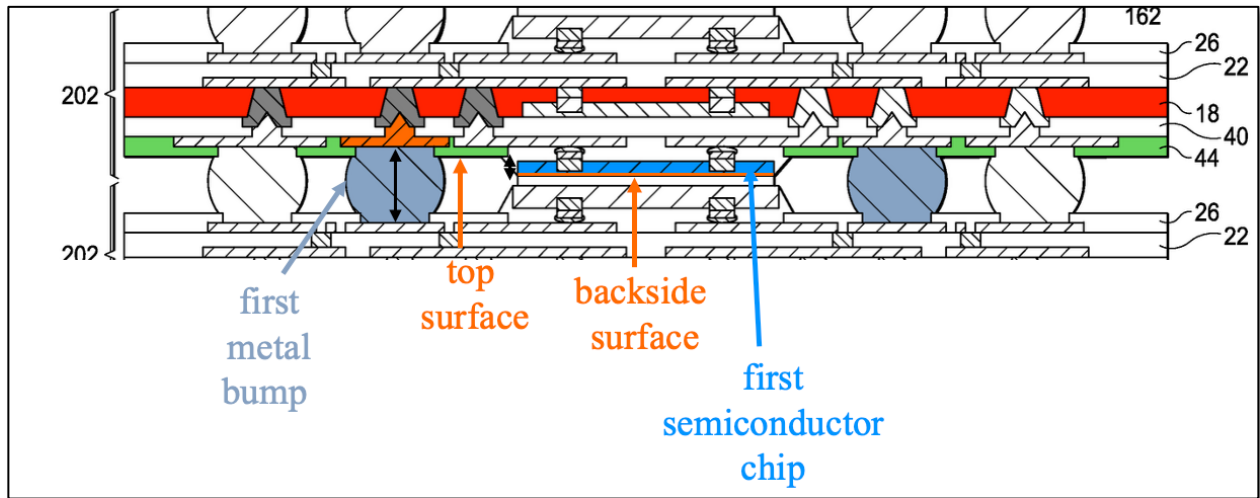
389. Shown below, Yu’s die 52, which is a “memory die,” is a first semiconductor chip over said first interconnection scheme and between said first and second metal bumps. EX1010 at 4:30–34.



EX1010 at FIG. 52.

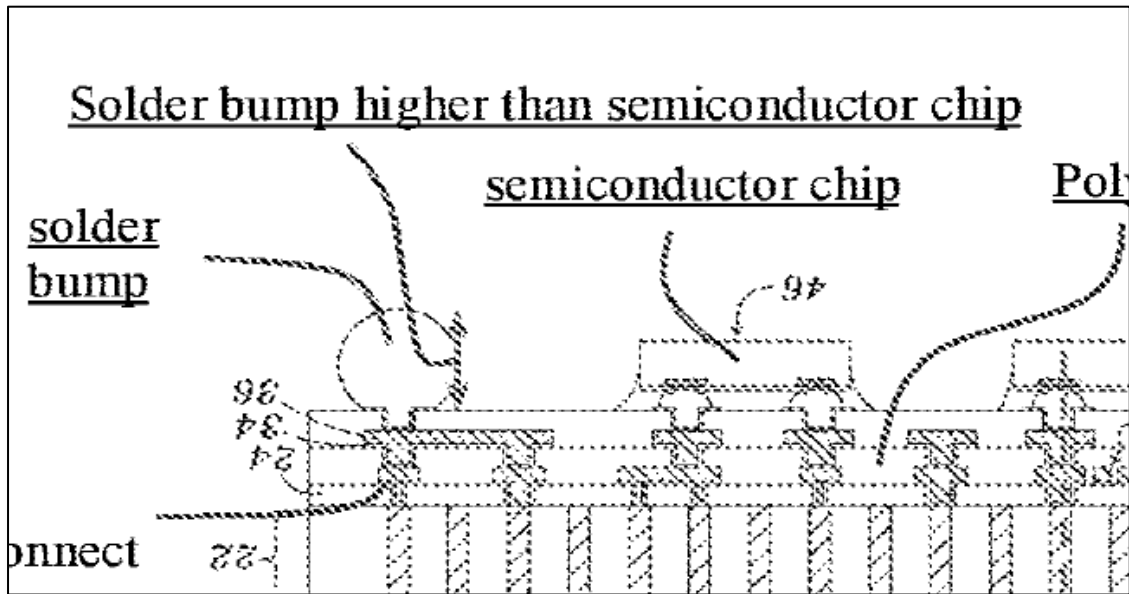
16. 10(f)(i): “wherein said first semiconductor chip has a height between a backside surface of said first semiconductor chip and a top surface of said polymer layer is smaller than a thickness of said first metal bump,”

390. Yu’s die 52 has a height between a backside surface and a top surface of ILD 44 that is smaller than a thickness of said first metal bump:



EX1010 at FIG. 52 (excerpt).

391. Yu's teachings are consistent with an annotated figure that Patent Owner argued supports language similar Claim 10(f)(i):



EX1032 at p. 400.

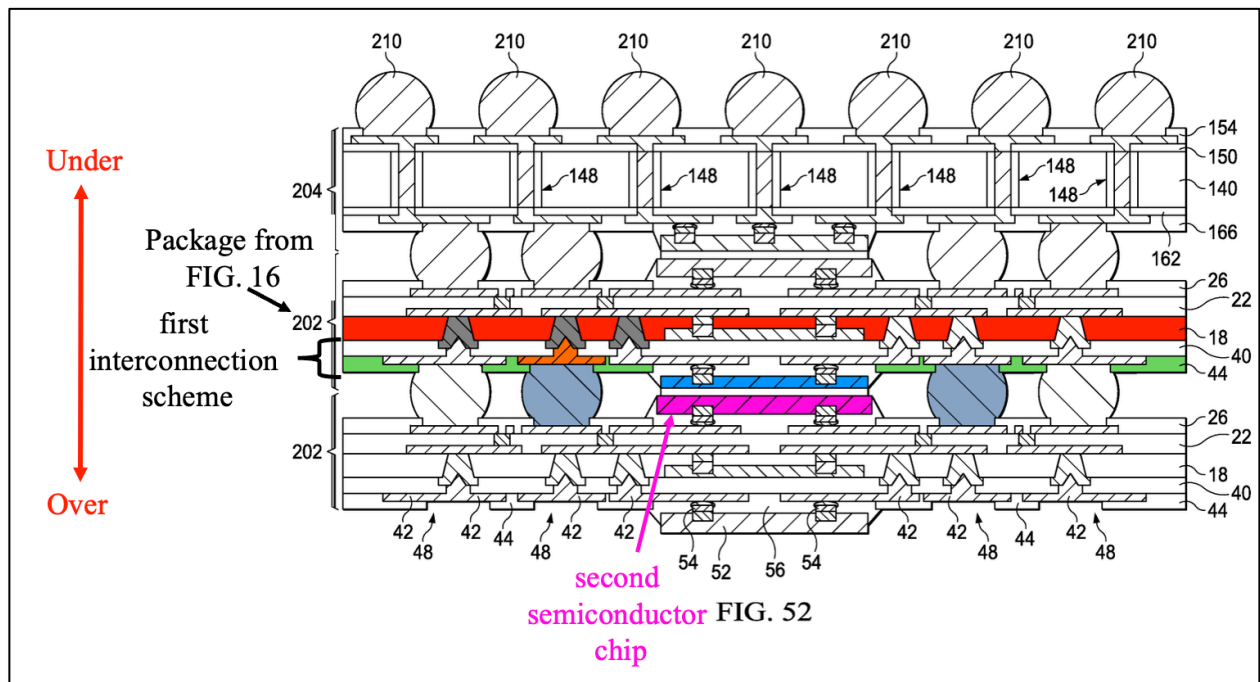
17. *10(f)(ii): “wherein said first semiconductor chip comprises a third metal bump on a first metal pad of said first*

semiconductor chip, wherein said third metal bump comprises a second tin-containing layer; and”

392. See ¶¶ 345-350, incorporated herein. Claim 10’s *third metal bump* corresponds to Claim 1’s *third metal interconnect*. See ¶¶ 338-341, incorporated herein, for Yu and Yu-Lin-191’s teachings of a *tin-containing layer*. For the same MTCs and with the same reasonable expectation of success, a POSITA would have found it obvious and been motivated to configure Yu’s *third metal bump* to *comprise[] a second tin-containing layer*.

18. 10(g): “a second semiconductor chip over said first interconnection scheme,”

393. Yu’s die 62 in another package 202 in FIG. 52’s PoP structure is a *second semiconductor chip*. As described in Yu, die 62 is a “die 62, such as a memory die...attached...to conductive features in the second front side metallization layer 24” using conductive connectors 64 such as C4 bumps. *EX1010* at 4:53–56, FIGS. 14-15 (depicting die 62 being connected to layer 24 via opening 30 in ILD 26). As shown, die 62 is *over said first interconnection scheme*:



EX1010 at FIG. 52.

19. 10(g)(i): “wherein said second semiconductor chip comprises a fourth metal bump on a second metal pad of said second semiconductor chip, wherein said fourth metal bump comprises a third tin-containing layer.”

394. See ¶¶ 369-372, incorporated herein. Claim 10’s *fourth metal bump*, *second metal pad*, and *third tin-containing layer* corresponds to Claim 6’s *second metal bump*, *second metal pad*, and *second tin-containing layer*, respectively. In other words, the limitations of Claim 10(g)(i) correspond to those of Claim 6, including the interrelationship of the claimed components, because they recite the same claimed structure other than the nomenclature of *second*, *third*, and *fourth*.

J. Claim 11: “The chip package of claim 10, wherein said compound comprises a SiO₂ compound.”

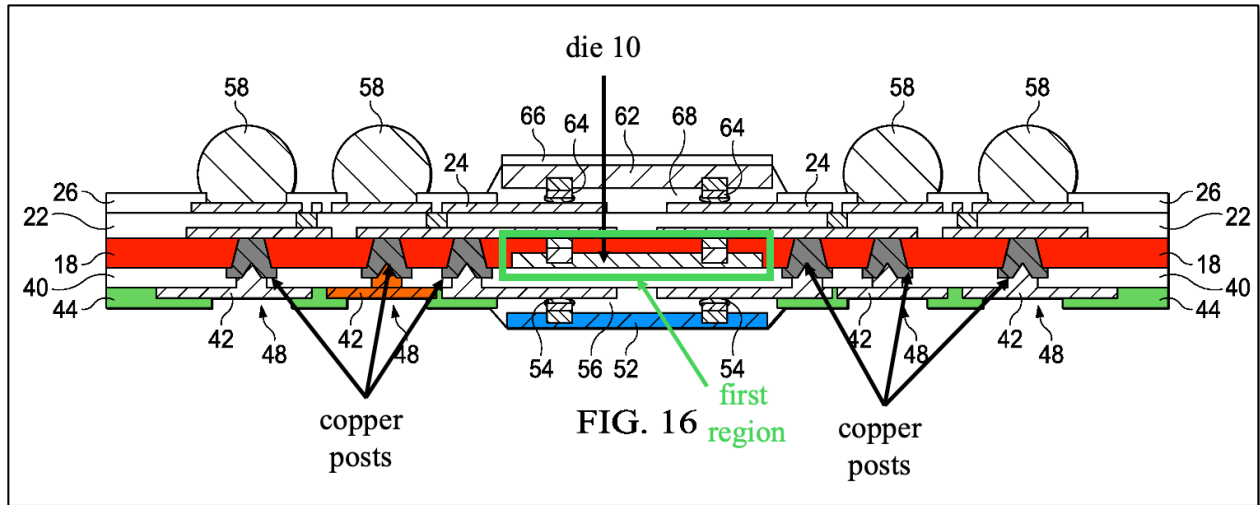
395. See ¶¶ 362-368, incorporated herein.

K. Claim 12: “The chip package of claim 10, wherein no any copper post in said first region.”

396. Yu teaches that TMVs 38 (copper posts) are on either side of the first region, which encapsulates a die 10 such that there are *no any copper posts in said first region*. As shown in FIGS. 1 and 2, Yu describes that package 202 includes “a first die encased in molding compound 18,” with through-mold vias (TMVs) 38 extending vertically through the surrounding molding compound. *EX1010* at 2:41–65; 8:7–8. The molding compound 18 defines a distinct encapsulation region surrounding and above die 10, within which the die is embedded.

397. Yu further teaches that the TMVs 38 are “formed through the molding compound 18”, showing that the copper-filled posts are positioned in the molding regions adjacent to, rather than within, the die-encapsulating area. *EX1010* at 3:56–4:6. FIGS. 1–2 visually confirm that the TMVs 38 are distributed around the periphery of die 10, connecting the upper and lower metallization structures but avoiding the central die region. The die 10 itself occupies the central *first region* while the TMVs are confined to either side of the *first region*, separated by the molding compound 18 that laterally isolates the die.

398. Accordingly, Yu teaches that TMVs 38 (copper posts) are on either side of the first region, which encapsulates a die 10 such that *there are no any copper posts in said first region*.

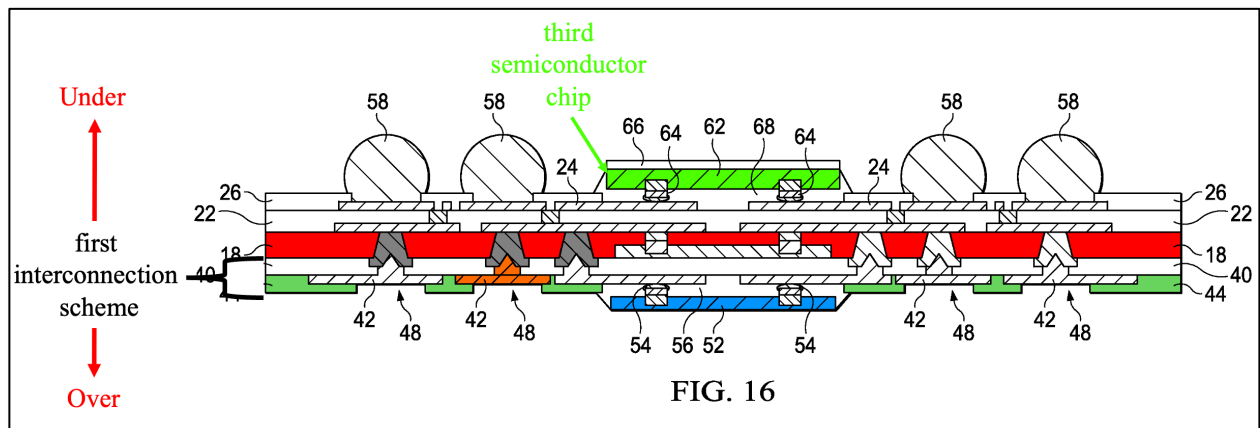


EX1010 at FIG. 16.

L. *Claim 13*

1. 13(a): “The chip package of claim 10, further comprising a third semiconductor chip under said first interconnection scheme,”

399. See ¶ 369, incorporated herein. Claim 13's *third semiconductor chip* corresponds to Claim 6(a)'s *second semiconductor chip*. As shown, the *third semiconductor chip* (die 62) is positioned *under said first interconnection scheme*:



EX1010 at FIG. 16.

2. **13(b): “wherein said third semiconductor chip comprises a second metal interconnect on a third metal pad of said third semiconductor chip,”**

400. See ¶¶ 369-371, incorporated herein. Claim 13(b)’s *second metal interconnect* and *third metal pad* correspond to Claim 6’s *second metal bump* and *second metal pad*, respectively. In other words, the limitations of Claim 13(b) correspond to those of Claim 6, including the interrelationship of the claimed components, because they recite the same claimed structure other than the nomenclature of *first*, *second*, and *third*.

3. **13(c): “wherein said second metal interconnect comprises a second metal layer on said third metal pad and a second copper layer over said second metal layer, wherein said second copper layer has a thickness between 5 and 30 micrometers.”**

401. See ¶¶ 351-352, ¶¶ 168-169 incorporated herein. For the same MTCs and with the same reasonable expectation of success, a POSITA would have found

it obvious and been motivated to configure Yu's *second metal interconnect*, per Lin-191, to comprise a *second metal layer on said third metal pad and a second copper layer over said second metal layer, wherein said second copper layer has a thickness between 5 and 30 micrometers.*

M. Claim 14

1. ***14(a): "The chip package of claim 10, further comprising a third semiconductor chip under said first interconnection scheme,"***

402. See ¶¶ 399, 369, incorporated herein., incorporated herein. Claim 14's *third semiconductor chip* corresponds to Claim 13(a)'s *third semiconductor chip* and Claim 6(a)'s *second semiconductor chip*. In other words, the limitations of Claim 14(a) correspond to those of Claims 13(a), 6(a), including the interrelationship of the claimed components, because they recite the same claimed structure other than the nomenclature of *first*, *second* and *third*.

2. ***14(b): "wherein said third semiconductor chip comprises a second metal interconnect on a third metal pad of said third semiconductor chip,"***

403. See ¶¶ 400, 369-371, incorporated herein., incorporated herein. Claim 14(b)'s *second metal interconnect* and *third metal pad* correspond to Claim 13(b)'s *second metal interconnect* and *third metal pad* and Claim 6's *second metal bump* and *second metal pad*, respectively.

3. ***14(c): “wherein said second metal interconnect comprises a second metal layer on said third metal pad and a second copper layer over said second metal layer,”***

404. See ¶¶ 401, incorporated herein. Claim 14(c)’s *second metal layer*, *third metal pad*, and *second copper layer* correspond to Claim 13(c)’s *second metal layer*, *third metal pad*, and *second copper layer*, respectively.

4. ***14(d): “wherein said third semiconductor chip comprises a central-processing-unit (CPU) circuit block and a graphics-processing-unit (GPU) circuit block.”***

405. See ¶¶ 355-356, incorporated herein.

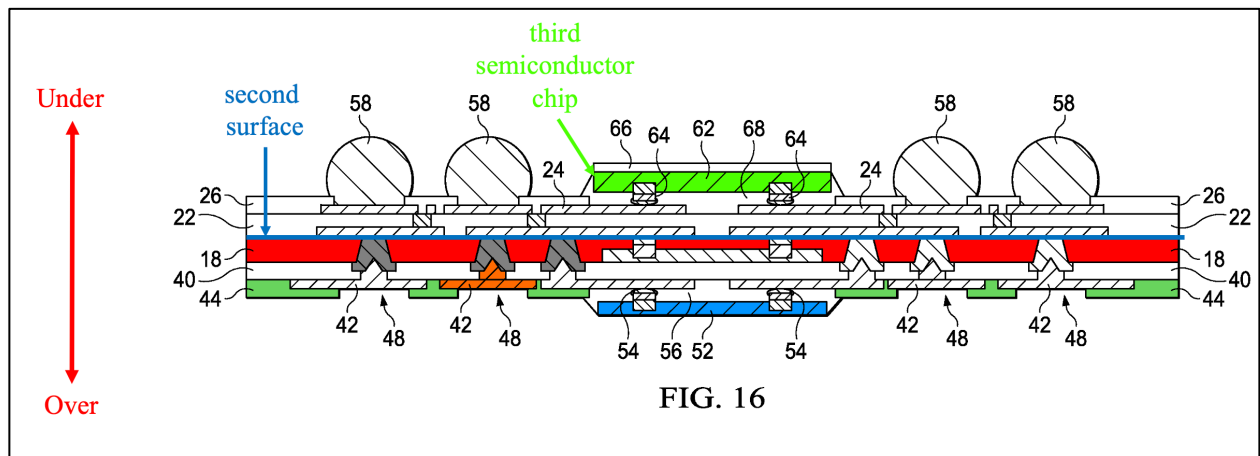
N. ***Claim 15: “The chip package of claim 10, wherein said solid layer further comprises a third region opposite to said second region, wherein said third region is between said first region and a second edge of said solid layer, wherein said plurality of copper posts in said plurality of through holes in said third region respectively.”***

406. See ¶ 373, incorporated herein.

O. Claim 17

1. ***17(a): “The chip package of claim 10, further comprising an electrical device under said second surface, wherein said electrical device comprise a third semiconductor chip and a metal wire connected to a third metal pad of said third semiconductor chip,”***

407. Yu teaches *a third semiconductor under said second surface*, i.e., memory “die 62.” *EX1010* at 4:53-56.



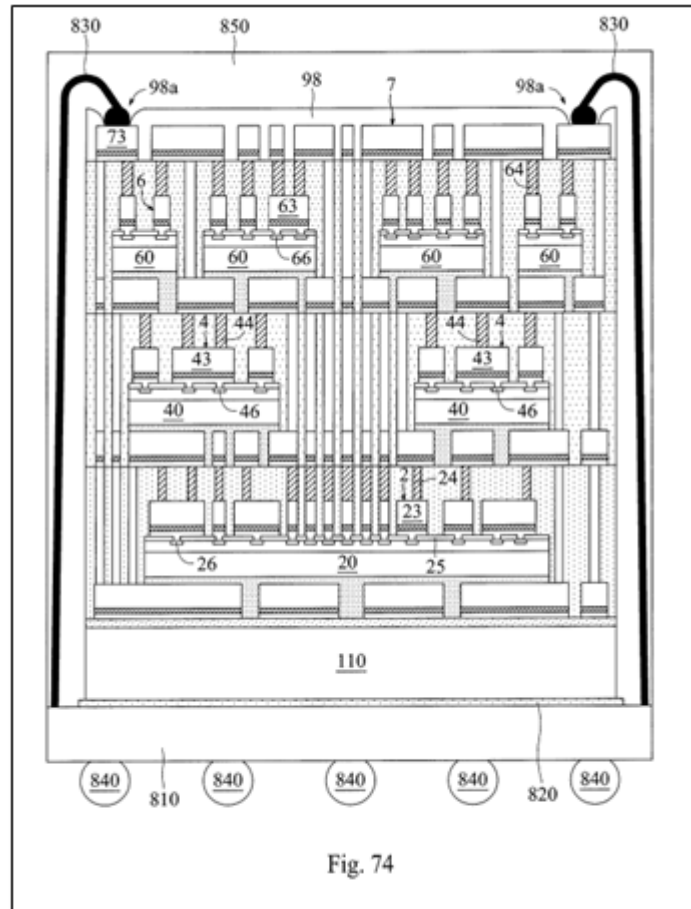
EX1010 at FIG. 16.

408. Yu teaches “[w]ire bonding can be used to make the electrical connections from chip components...to substrate.” EX1010 at 1:41-43. Yu alone or Yu-Lin-191 teaches *a third metal pad*, and a POSITA would have understood Yu’s wire bond teachings as teaching wire bonding to a *metal pad* because wires were ubiquitously bonded to metal chip pads at the time of the ’306 Patent.

a. Lin-191’s Teachings and Motivation to Combine Yu and Lin-191

409. Additionally, or alternatively, to Yu, Lin-191 teaches “wirebonded wire[s] 820 can be ball bonded with one of the contact points...of the metal layer 73[.]” EX1005 at [0410]. Further, Lin-191 teaches “metal...pads 170c, 170d, 180c and 180d...can be connected to the ball-grid-array (BGA) substrate 810 shown in FIG. 74 through the wirebonded wires 830.” EX1005 at [0490]. Pads 170c, 170d,

180c, 180d are chip pads. *EX1005* at [0489]. Thus, Lin-191 teaches *a metal wire connected to a third metal pad of a third semiconductor chip*.



EX1005 at FIG. 74.

410. A POSITA would have found it obvious and been motivated to modify Yu's *third semiconductor chip* to comprise a *wire connected to a third metal pad of said third semiconductor chip*. A POSITA would have been motivated and found it obvious to modify Yu's chip package to apply Lin-191's teachings of wirebonding metal pads. *EX1005* at [0490]. Yu likewise teaches that "wire bonding can be used

to make the electrical connections from chip components...to substrate”. *EX1010* at 1:41-43. A POSITA would have recognized that both Yu and Lin-191 describe functionally equivalent structures, stacked semiconductor dies connected by wirebonds to corresponding metal pads, and that Yu’s description invites the use of standard wirebond connections to implement those inter-die electrical paths. Further, because Yu expressly envisions wirebonding for connecting chips to substrates such that the modification is merely an implementation detail in Yu’s package.

411. Additionally, wire bonds were known to be “a low-cost, stable technology for forming electrical connections” in chip packages. *EX1125* at [0108]. Additionally, prior to the alleged invention of the ‘306 Patent, wire bonding had “been used in integrated circuit packaging since the inception of IC technology” and thus “[w]ire bonding techniques and wire bonding machines” had been “refined to the point where wire bonds [were] relatively inexpensive and highly reliable.” *EX1120* at 1:9-13. As such, a POSITA would have appreciated the low-cost and high reliability of wire bonds in chip packaging technology and been motivated to implement such well-known technology into Sundaram’s chip package.

412. The modification is the application of a known technique (wire bonding) to a known device (Yu’s package) ready for improvement to yield predictable results, i.e., Yu’s *third semiconductor chip* being connected to substrates

with a *metal wire*). Because wire bonding had “been used in integrated circuit packaging since the inception of IC technology” and because wire bonding techniques were well-known, there would have been a reasonable expectation of success. *EX1120* at 1:9-13.

2. 17(b): “wherein said third semiconductor chip is a DRAM chip.”

413. Yu teaches “Dynamic Random Access Memory.” *EX1010* at 1:31-33. A POSITA would have found it obvious to configure Yu’s memory chip as a DRAM chip because DRAM chip is one kind of memory chip, e.g., when Yu’s package is used in a “mobile telephone/PDA.” *EX1010* at 1:53-55. Further, for the same MTCs and with the same reasonable expectation of success described above for Sundaram-Lin-191, a POSITA would have found it obvious and been motivated to implement Yu’s die 62 to be a *DRAM chip*. See ¶¶ 242-243.

P. Claim 18

1. 18(Pre): “A chip package comprising”

414. See Claim 1(Pre), ¶¶ 309-311, incorporated herein.

2. 18(a): “a solid layer having a first surface and a second surface opposite to said first surface,”

415. See Claim 1(a), ¶¶ 313-314, incorporated herein. Claim 18’s mapping reverses Yu’s mapped *first* and *second surfaces* and *over/under* directions relative to Claims 1 mapping and maintains Claim 10’s *over/under* directions.

3. ***18(a)(i): “wherein said solid layer comprises a compound of silicon and oxygen,”***

416. See Claim 1(a)(i), ¶ 315, incorporated herein.

4. ***18(a)(ii): “wherein said solid layer has a thickness between 50 and 150 micrometers;”***

417. See Claim 1(a)(ii), ¶¶ 316-318, incorporated herein.

5. ***18(a)(iii): “wherein said solid layer comprises a first region and a second region between said first region and a first edge of said solid layer;”***

418. See Claim 1(a)(iii), ¶ 324, incorporated herein.

6. ***18(b): “a plurality of copper posts in a plurality of through holes in said second region respectively,***

419. See ¶ 325, incorporated herein. Claim 18’s *plurality of copper posts* corresponds to Claim 1’s *plurality of metal posts* (because copper is *metal*).

7. ***18(c): “a first interconnection scheme over said first surface,”***

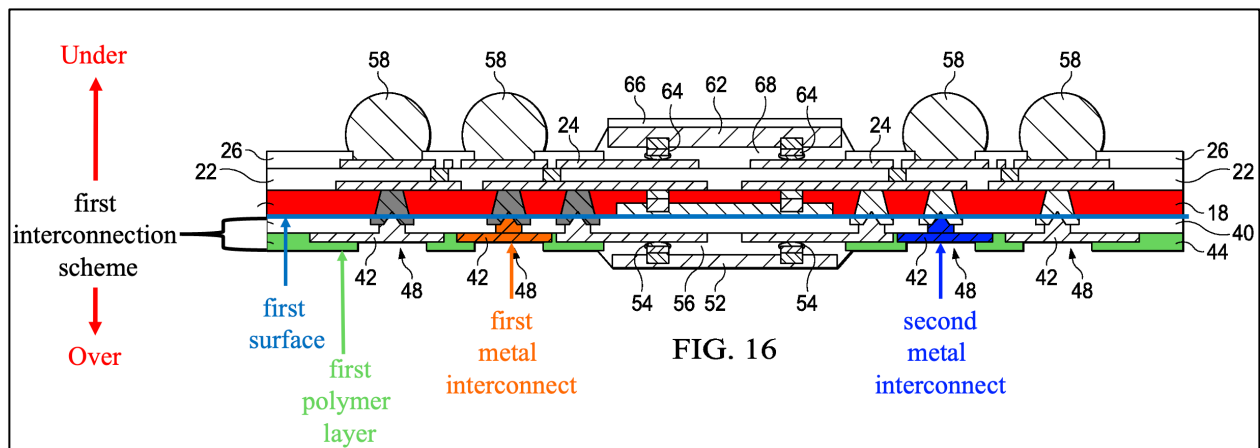
420. See ¶ 330, incorporated herein.

8. ***18(c)(i): “wherein said first interconnection scheme comprises first and second metal interconnects over said first surface, and a first polymer layer over said first and second metal interconnects,”***

421. See ¶ 383. Yu teaches that the back side ILD and RDL structure includes “a first back side ILD layer 40, a second back side metallization layer 42, [and] a second ILD layer 44.” *EX1010* at 4:7–11. Metallization layer 42 is formed “in the same manner” as metallization layer 20 (i.e., with a copper seed layer and an

electroplated copper layer) and is therefore *metal*. *EX1010* at 4:7-14, 3:4-19. Accordingly, a portion of metallization layer 42 corresponds to a *first metal interconnect* that is *over said first surface*. For the same reasons, a second portion of metallization layer 42 is a *second metal interconnect* that is *over said first surface*.

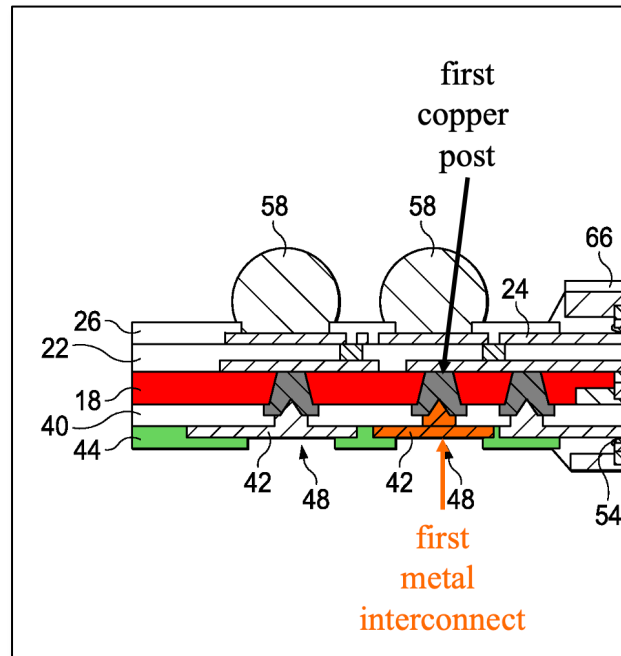
422. Yu further teaches “a second ILD layer 44” that is formed over the *first and second metal interconnects*. *Id.* at 4:10–12. Second ILD layer 44 is formed “in the same manner” as “the ILD layers...on the front side” (e.g., ILD layer 22) such that ILD layer 44 is a *first polymer layer*. *EX1010* at 4:11-14, 3:21-23 (“The first ILD layer 22 may be a polyimide...”). Thus, ILD layer 44 is a *first polymer layer over said first and second metal interconnects*:



EX1010 at FIG. 16.

9. **18(c)(ii): “wherein said first metal interconnect is connected to a first copper post of said plurality of copper posts,”**

423. See ¶ 384, incorporated herein. Yu's *first metal interconnect* is connected to a *first copper post* of said plurality of copper posts:



EX1010 at FIG. 16 (excerpt).

10. 18(c)(iii): “wherein said first metal interconnect comprises a first metal layer and a first copper layer over said first metal layer;”

424. See ¶ 385, incorporated herein.

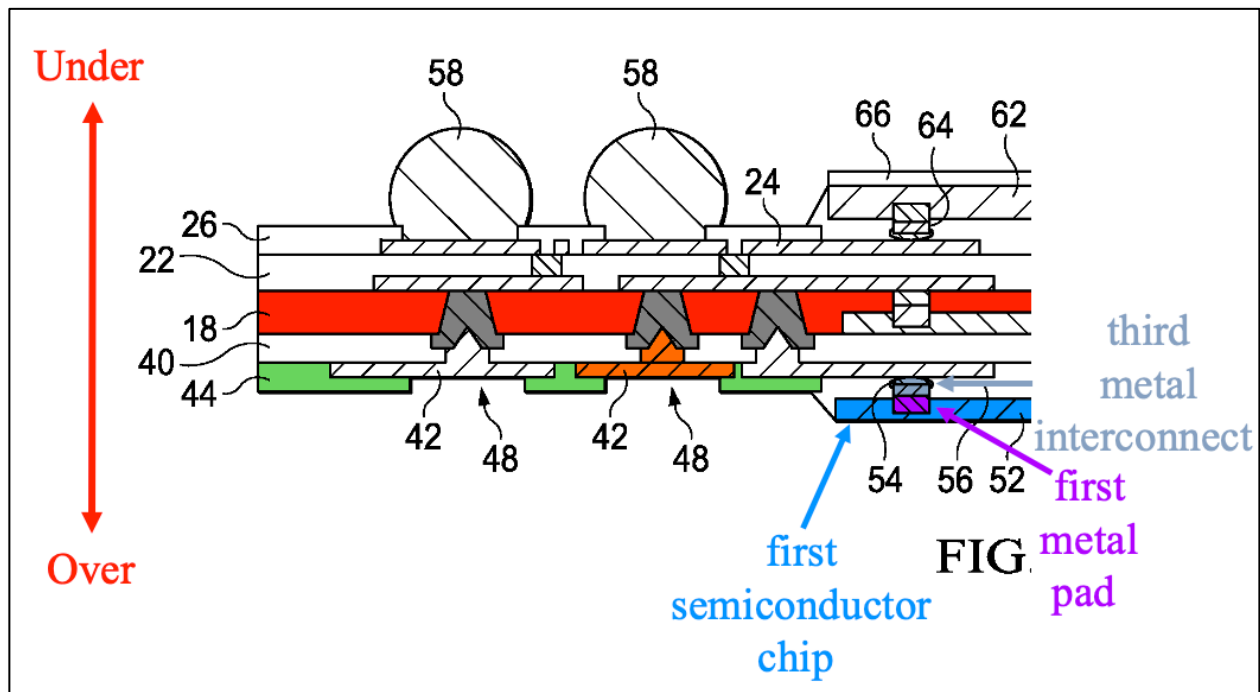
11. 18(d): “a first semiconductor chip over said first interconnection scheme,”

425. See ¶ 389, incorporated herein. Die 52 is a first semiconductor chip over said first interconnection scheme.

12. 18(d)(i): “wherein said first semiconductor chip comprises a third metal interconnect under a first metal pad of said first semiconductor chip,”

426. See ¶¶ 345-348, incorporated herein. Yu's die 52 (*first semiconductor chip*) has a connector 54 (*third metal interconnect*) disposed under a first metal pad. *EX1010* at 4:30–34. Yu teaches that die 52 “is attached...to conductive features in the second back side metallization layer 42, such as by conductive connectors 54, like controlled collapse chip connection (C4) bumps,” indicating that connector 54 lies beneath the bond pad structure of die 52 to provide electrical coupling. *EX1010* at 4:30–34. The C4 bump thus functions as a *third metal interconnect under a first metal pad*.

427. Additionally, or alternatively, the combination of Yu and Lin-191 teaches a *third metal interconnect under a first metal pad of said first semiconductor chip*. See ¶¶ 349-350, incorporated herein.



EX1010 at FIG. 16 (excerpt).

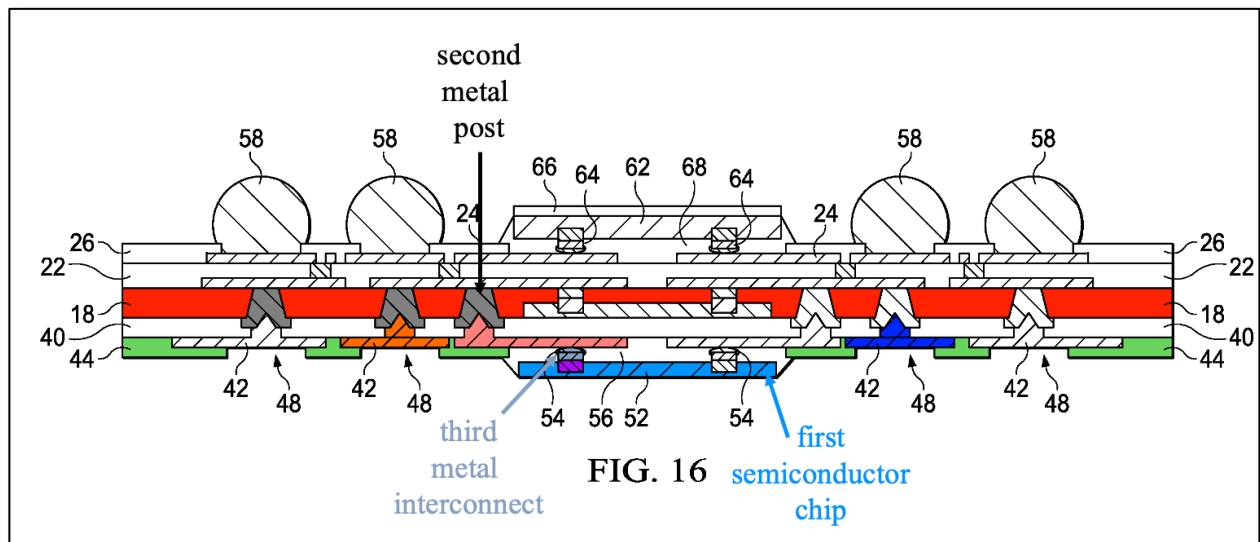
13. 18(d)(ii): “wherein said third metal interconnect comprises a second metal layer under said first metal pad and a second copper layer under said second metal layer, wherein said second copper layer has a thickness between 5 and 30 micrometers,”

428. See ¶¶ 351-352, incorporated herein. Claim 18(d)(ii)’s *second metal layer* and *second copper layer* correspond to Claim 1(e)(iii)’s *third metal layer* and *third copper layer*, respectively. I note that relative to Claim 1(e)(iii), Claim 18(d)(ii) requires the *second copper layer* to be **under** said *second metal layer* whereas Claim 1(e)(iii) requires the *third copper layer* to be **over** said *third metal layer*. Thus, because (1) Claim 18’s over/under directions are inverted relative to Claim 1, and (2) the orientation of *second copper layer* in Claim 18 (i.e., *under said second metal*

layer) is inverted relative to the *third copper layer* in Claim 1 (i.e., *over said third metal layer*), the above-described combination of Yu-Lin-191 yields *wherein said third metal interconnect comprises a second metal layer under said first metal pad and a second copper layer under said second metal layer, wherein said second copper layer has a thickness between 5 and 30 micrometers.*

14. 18(d)(iii): “wherein said first semiconductor chip is coupled to a second copper post of said plurality of copper posts through said third metal interconnect;”

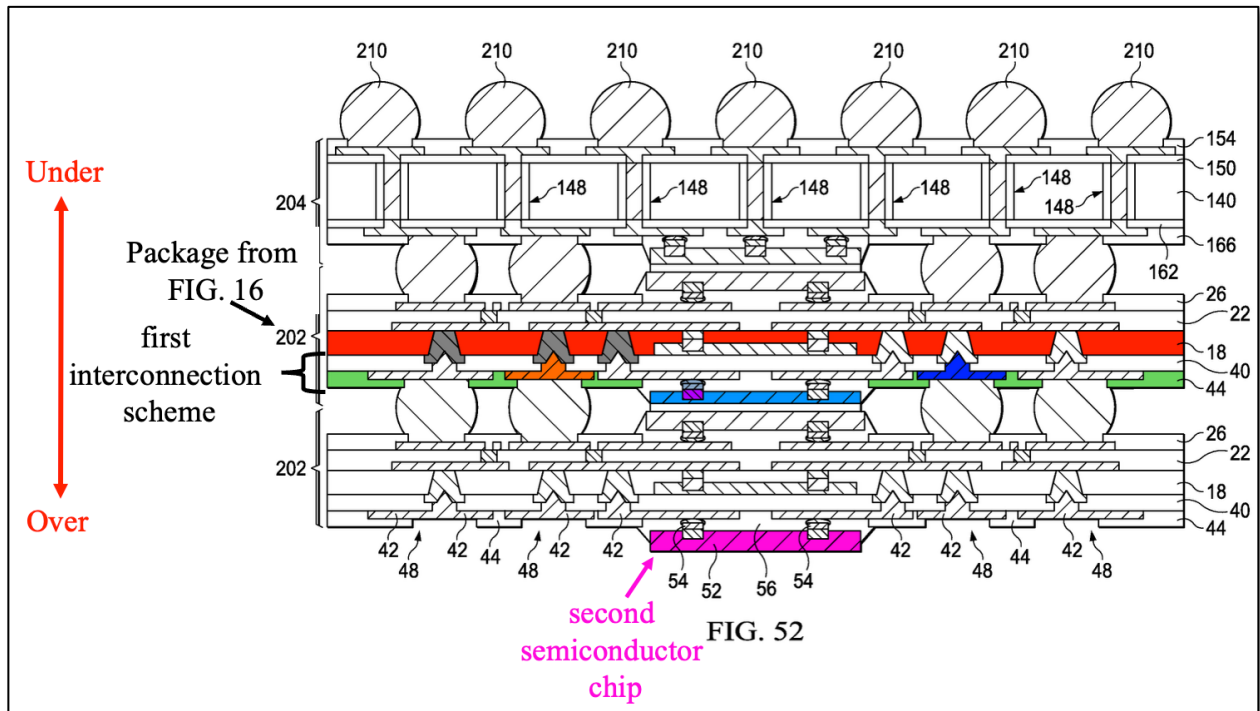
429. As shown, die 52 *is coupled to* a second TMV 38 (*a second copper post of said plurality of copper posts*) through connector 54 (*third metal interconnect*) and **another portion of layer 42**. *EX1010* at FIGS. 8-9 (assigning reference numeral 42 to the **another portion of layer 42**). Specifically, Yu teaches “die 52...is attached...to conductive features in the second back side metallization layer 42, such as by conductive connectors 54[.]” *EX1010* at 4:30-34. Thus, Yu’s die 52 (*first semiconductor chip*) *is coupled to a second copper post...through said third metal interconnect:*



EX1010 at FIG. 16.

15. 18(e): “a second semiconductor chip over said first interconnection scheme,”

430. A die 52 in a second package 202 in the PoP structure is *a second semiconductor chip over said first interconnection scheme*. Yu teaches that “multiple packages 202...can be stacked in the PoP structure” and that “each package 202 comprises a first die encased in molding compound 18 and conductive connectors 58 on the front side of the package.” EX1010 at 8:11–15, 8:35–39. In Yu’s stacked configuration (FIG. 52), the upper package 202 contains a die 52 that is positioned *over the first interconnection scheme*:



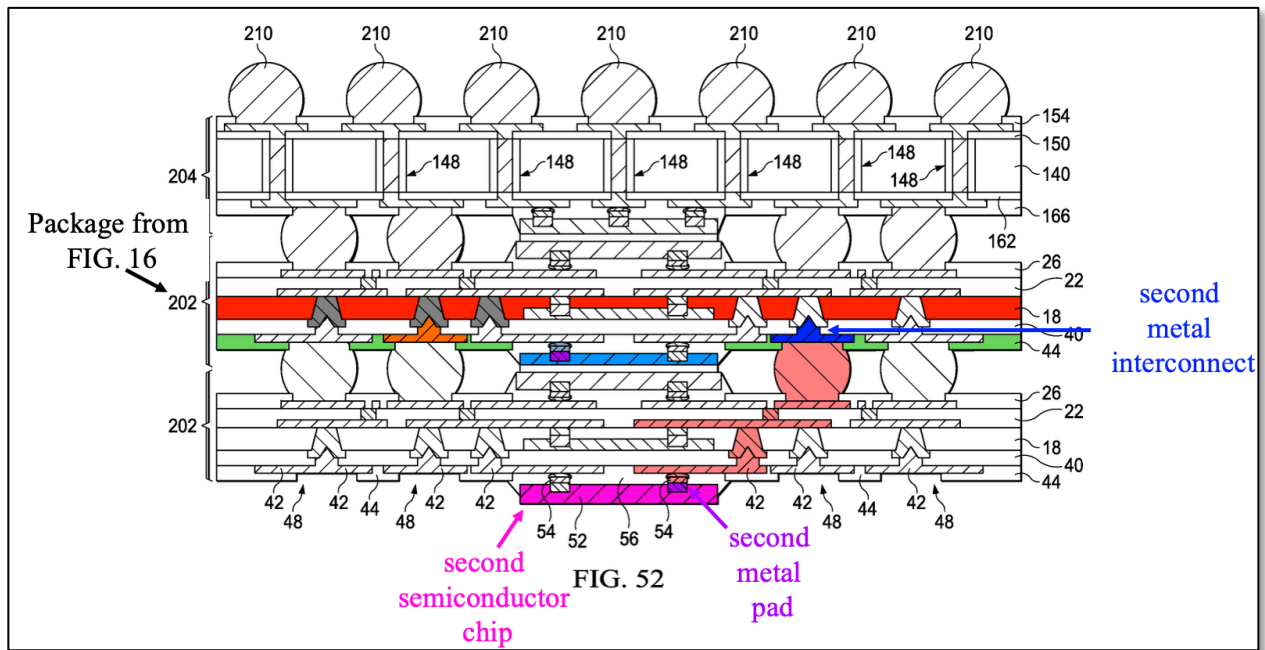
EX1010 at FIG. 52.

16. 18(e)(i): “wherein said second semiconductor chip comprises a second metal pad coupled to said second metal interconnect;”

431. As I described above, Yu's die 52 *comprises a metal pad*. See ¶¶ 345-348. Additionally, or alternatively, a POSITA would have found it obvious and been motivated to implement Yu's *pad* as a *metal pad*. See ¶¶ 349-350. Yu alone or Yu-Lin-19 thus teaches *wherein said second semiconductor chip comprises a second metal pad*.

432. Additionally, as shown below, Yu's *second metal pad* is coupled to said *second metal interconnect* through die 52's **connector 54**, a **first portion of layer 42**, a **TMV 38**, **layers 20, 24**, and a **connector 58**. *EX1010* at 4:53-60.

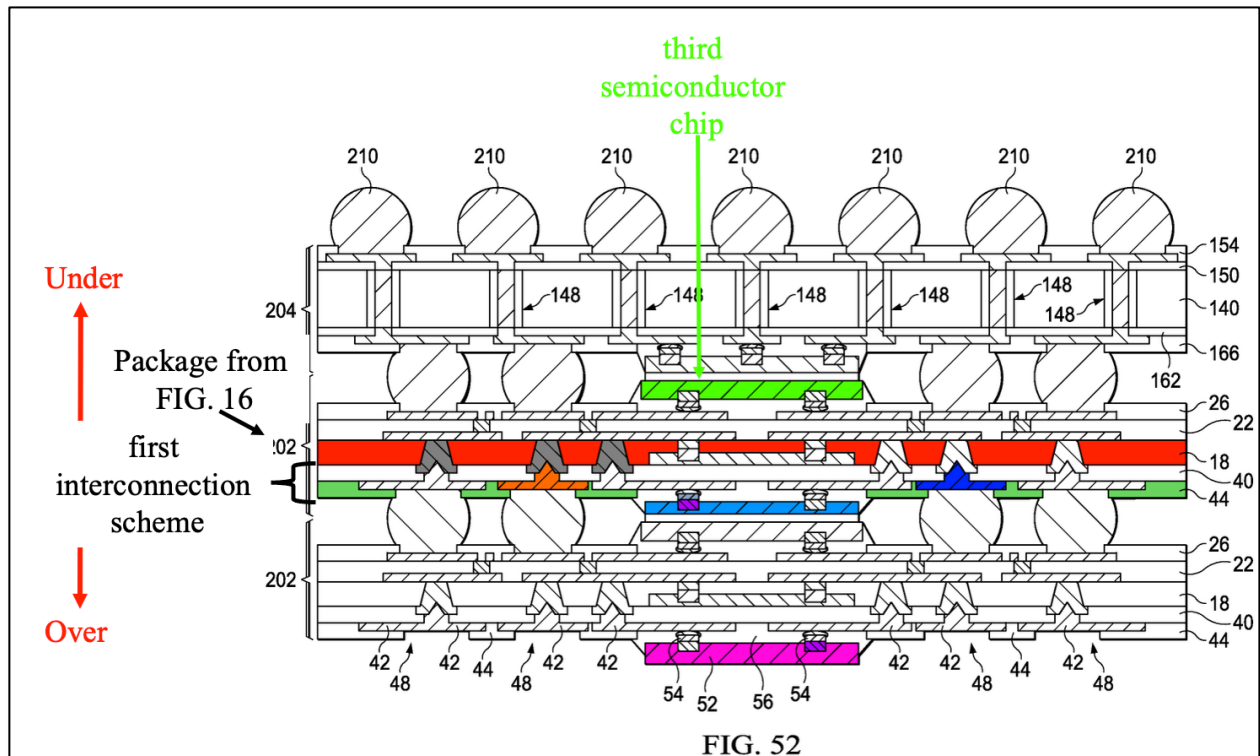
433. Indeed, Yu teaches that “die 52, such as a logic or memory die, is attached...to conductive features in the second back-side metallization layer 42, such as by conductive connectors 54, like C4 bumps.” *EX1010* at 4:53-60. In Yu’s configuration, die 52’s metal pad is electrically coupled through the C4 bump (54) to metallization layer 42, which in turn connects to TMV 38, front-side metallization layers 20 and 24, and ultimately to connector 58 which is coupled to an in contact with the *second metal interconnect*:



EX1010 at FIG. 52.

17. 18(f): “a third semiconductor chip under said first interconnection scheme; and”

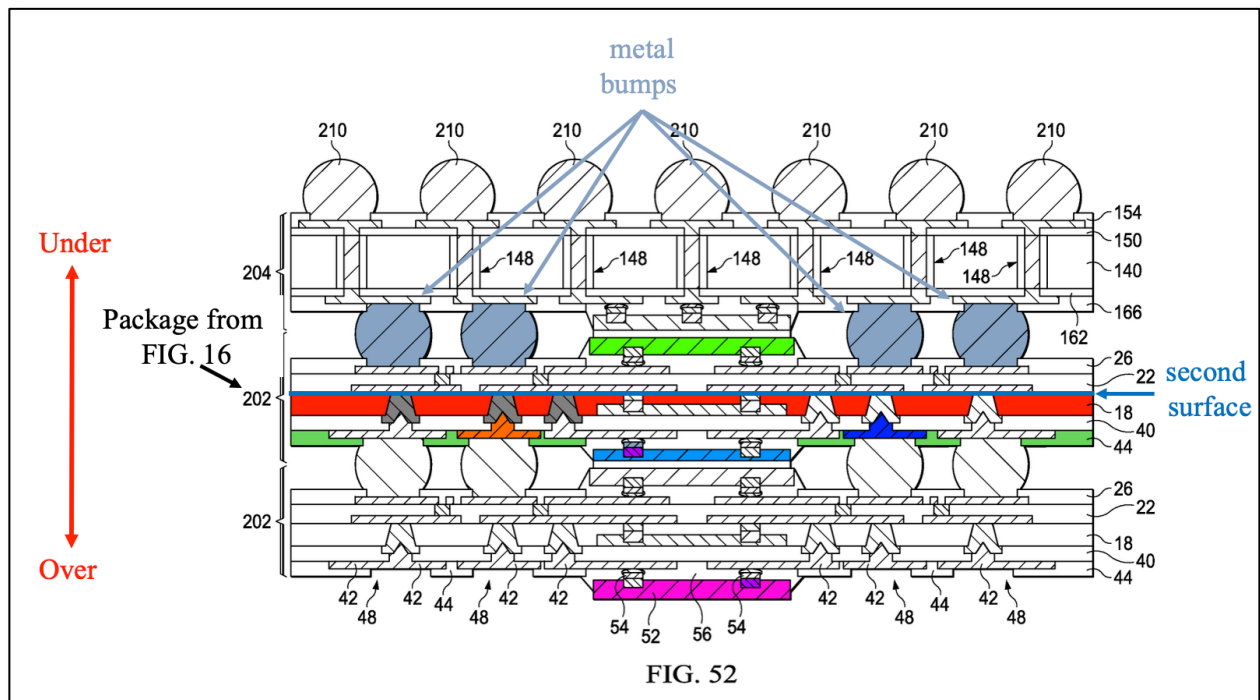
434. See ¶¶ 399, 369, reciting corresponding limitations. Yu's third die 62 is a third semiconductor chip under said first interconnection scheme. EX1010 at 4:53-60.



EX1010 at FIG. 52.

18. 18(g): “a plurality of metal bumps under said second surface, wherein one of said plurality of metal bumps comprises a tin-containing layer.”

435. The “lead-free solder” connectors 58 are a plurality of metal bumps under said second surface. EX1010 at 4:45-50. Yu alone or Yu-Lin-191 teaches that connector 58 comprises a tin-containing layer. See ¶¶ 338-341.



EX1010 at FIG. 52.

Q. *Claim 19: “The chip package of claim 18, wherein said compound comprises a SiO_2 compound.”*

436. See ¶¶ 362-368, incorporated herein.

R. *Claim 20: “The chip package of claim 18, wherein said solid layer further comprises a third region opposite to said second region, wherein said third region is between said first region and a second edge of said solid layer, wherein said plurality of copper posts in said plurality of through holes in said third region respectively.”*

437. See ¶ 373, incorporated herein.

S. Claim 22: “The chip package of claim 18, wherein said first semiconductor chip is a graphics-processing-unit (GPU) chip.”

438. Lin-191 teaches semiconductor chips that are “graphics-processing-unit (GPU) chip[s].” *EX1005* at [0106]. The MTCs and reasonable expectation of success provided for Claim 2 are incorporated. See ¶ 356.

T. Claim 23: “The chip package of claim 18, wherein said second semiconductor chip is a logic chip.”

439. Yu teaches dies as “logic circuitry die[s].” *EX1010* at 2:50–51. Yu states that “package-on-package (PoP) is an integrated circuit packaging technique to allow vertically combining discrete logic and memory ball grid array (BGA) packages,” and further that “each package may include a die 10 such as a logic circuitry die, a memory die, or any other die.” *EX1010* at 1:49–51, 2:50–52. A POSITA would have understood Yu’s disclosure to mean that Yu’s structure is adaptable to different functional die types, including logic chips.

440. Because Yu explicitly identifies logic circuitry dies as suitable for use in its PoP structure, a POSITA would have been motivated, found it obvious, and had a reasonable expectation of success in modifying Yu’s *second semiconductor chip* as a *logic chip*. *EX1010* at 2:50–52, 4:53–60, FIGS. 15–17, 52. The PoP architecture supports this substitution, as Yu teaches combining logic and memory packages in a vertically integrated stack. *EX1010* at 1:49–51 (“PoP ... allow[s]

vertically combining discrete logic and memory BGA packages.”). A POSITA would have recognized that positioning the logic die in the upper package facilitates thermal management and modular design while maintaining electrical connectivity through Yu’s RDL and TMV structures.

441. Accordingly, Yu teaches the use of a logic circuitry die in the described package configuration, and a POSITA would have understood that modifying die 52 to be a logic chip would merely apply Yu’s express teachings to a known and intended use. *EX1010* at 1:49–52, 2:50–52, 4:53–60, FIGS. 15–17, 52. Thus Yu teaches that the *second semiconductor chip is a logic chip*.

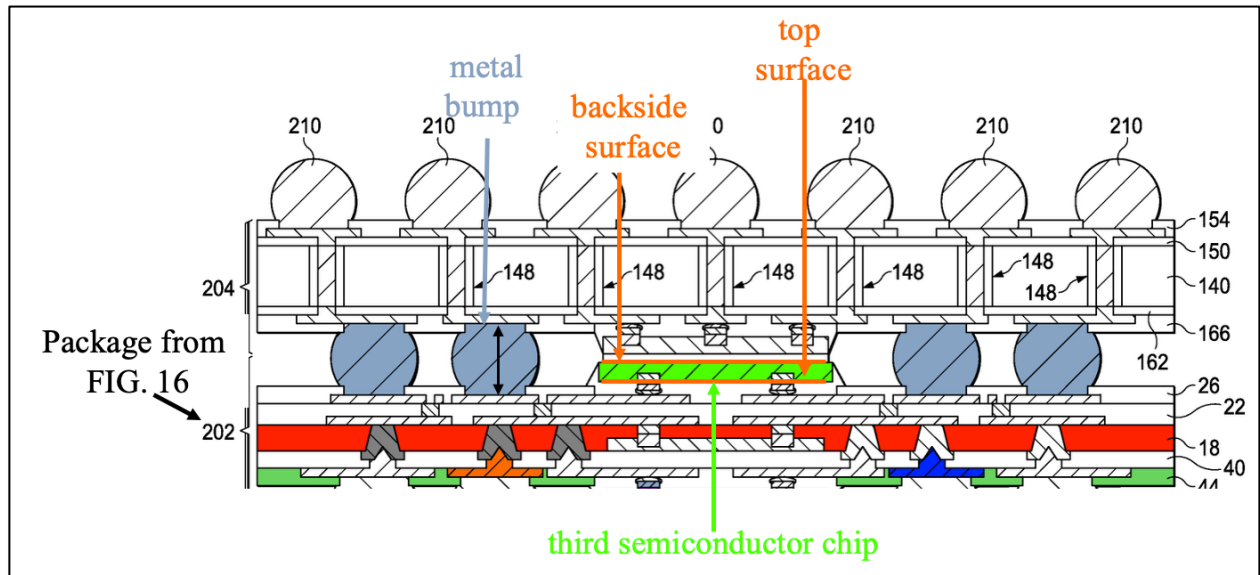
U. Claim 24: “The chip package of claim 18, wherein said first semiconductor chip is a logic chip.”

442. See ¶¶ 439–441, incorporated herein. For the same reasons described above and with the same reasonable expectation of success, a POSITA would have been motivated to implement the *first semiconductor chip as a logic chip*.

V. Claim 25: “The chip package of claim 18, wherein said third semiconductor chip has a thickness between a backside surface of said third semiconductor chip and a top surface of said third semiconductor chip is smaller than a thickness of one of said plurality of metal bumps.”

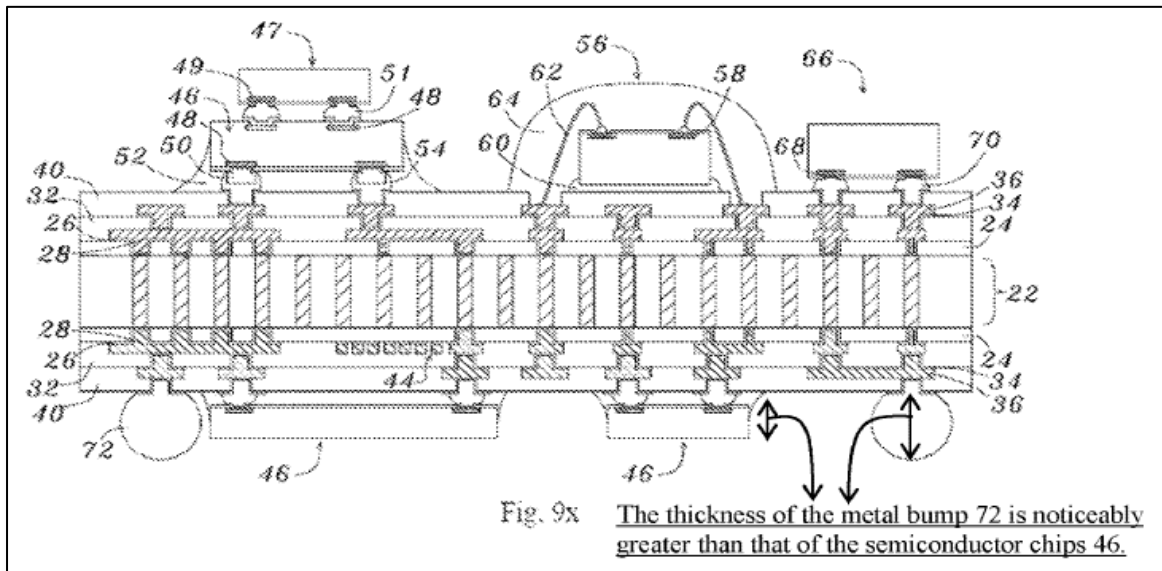
443. As shown below, Yu’s die 62 (*third semiconductor chip*) has a *thickness between a backside surface of said third semiconductor chip and a top*

surface of said third semiconductor chip that is smaller than a thickness of one of said plurality of metal bumps:



EX1010 at FIG. 52.

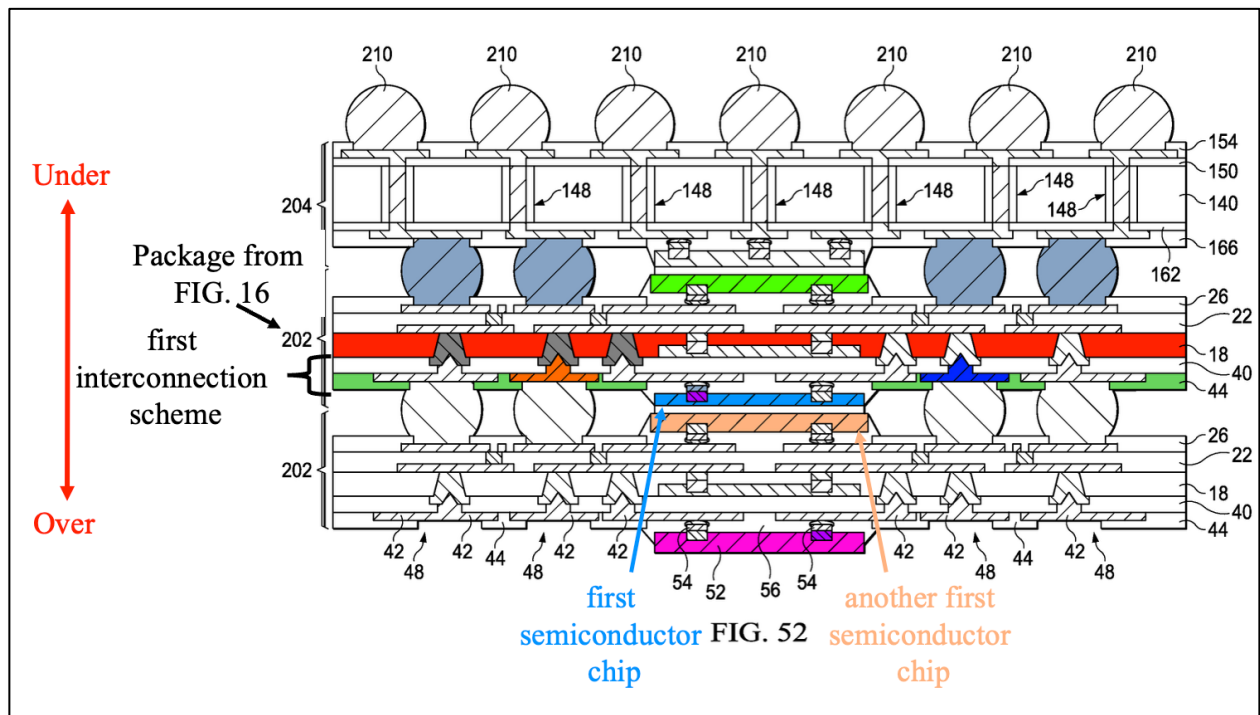
444. Yu's teachings are consistent with an annotated figure provided by Patent Owner during prosecution of the '306 Patent arguing support for language similar to Claim 25:



EX1002 at p. 336.

W. Claim 26: “The chip package of claim 18, further comprising another said first semiconductor chip over said first interconnection scheme.”

445. A die 62 in the second package 202 of Yu’s PoP structure shown in FIG. 52 is *another said first semiconductor chip*. Die 62 is, like die 52, “a memory die,” such that die 62 is *another die 52*. EX1010 at 4:53-56. As shown, die 62 in the second package 202 is *over said first interconnection scheme*:

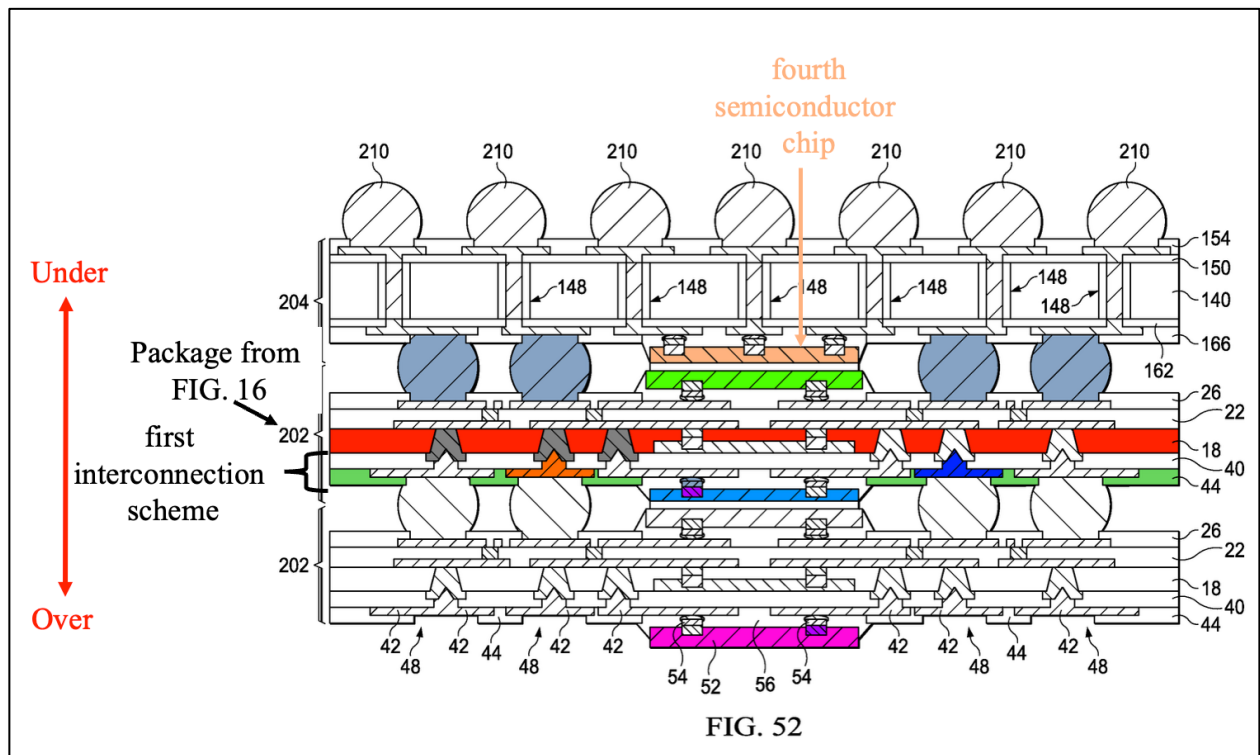


EX1010 at FIG. 52.

X. Claim 27

1. 27(a): “The chip package of claim 18, further comprising a fourth semiconductor chip under said first interconnection scheme,”

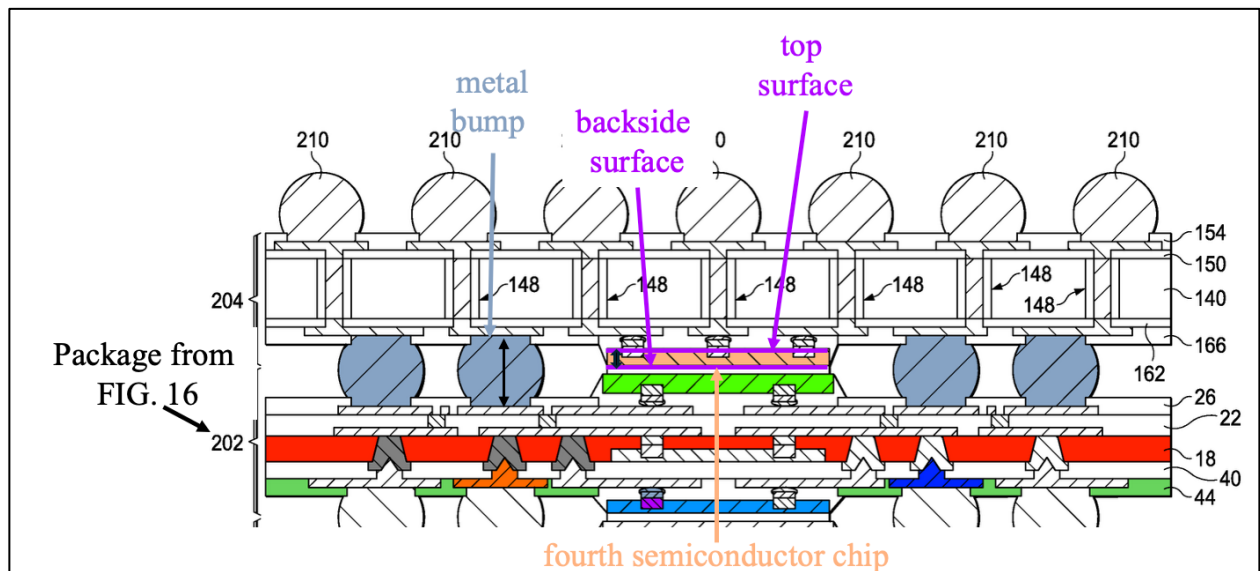
446. Yu’s PoP structure includes “interposer package 204” with “a third die on a front side of the [interposer] package,” which is a *fourth semiconductor chip*. EX1010 at 8:6–11, FIGS. 34–48 (formation of interposer 204). The die mounted to the front side of interposer 204 is therefore positioned below the front-side metallization layers of the upper package 202, i.e., *under said first interconnection scheme*, within the stacked PoP configuration illustrated in FIG. 52:



EX1010 at FIG. 52.

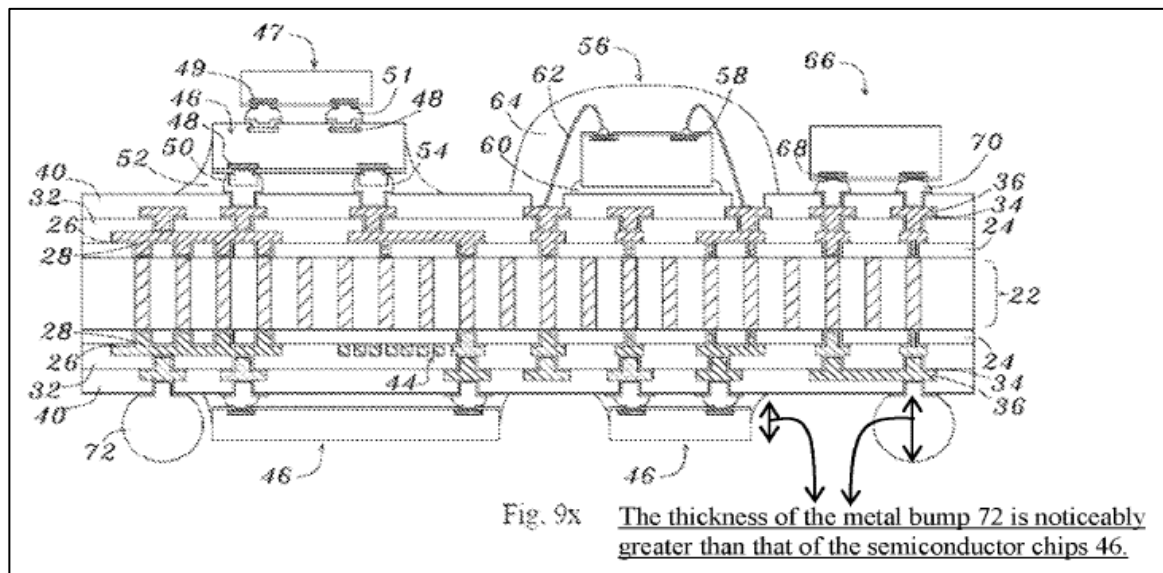
2. 27(b): “wherein said fourth semiconductor chip has a thickness between a backside surface of said fourth semiconductor chip and a top surface of said fourth semiconductor chip is smaller than a thickness of one of said plurality of metal bumps.”

447. The interposer die (fourth semiconductor chip) has thickness between a backside surface of said fourth semiconductor chip and a top surface of said fourth semiconductor chip is smaller than a thickness of one of said plurality of metal bumps:



EX1010 at FIG. 52 (excerpt).

448. I note that Yu's teachings are consistent with an annotated figure provided by Patent Owner during prosecution arguing support for language similar to Claim 27(b). *See* ¶ 284.



EX1002 at 336.

XI. OPINIONS REGARDING GROUND 2B: CLAIMS 8 AND 16 ARE OBVIOUS OVER YU, LIN-191, AND LIN-863

A. Claim 8: “The chip package of claim 1, wherein said second region is a rectangle region and surrounding said first region.”

449. Lin-863 teaches Claim 8. See ¶¶ 296-300, incorporated herein. The MTCs and reasonable expectation of success for Sundaram-Lin-863 apply equally to Yu-Lin-863. Further evidencing the reasonable expectation of success, Yu, like Lin-863, teaches both an encapsulated die 10 and a Package-on-Package (PoP) structure. *EX1010* at 2:41–65, 8:6–15. Yu describes that “package 202 comprises a first die encased in molding compound 18” and that “multiple packages 202 can be stacked in the PoP structure,” where each stacked package contains redistribution

layers and through-mold vias interconnecting multiple metallization levels. *EX1010* at 8:7–13, 8:35–392.

450. A POSITA would have recognized that Yu’s encapsulated, multi-layered package corresponds closely to Lin-863’s fan-out package structure, which likewise integrates encapsulated dies, redistribution layers, and vertical interconnections. Because Yu already teaches encapsulated dies and stacked PoP assemblies using redistribution and metallization layers, applying Lin-863’s fan-out teachings, such as external redistribution and connection routing, would have been a straightforward and predictable modification to Yu’s similar chip package. The integration would simply extend Yu’s existing fan-out design principles, yielding an expected enhancement in interconnect density and packaging flexibility. *Compare EX1007* at 11:47–48, FIGS. 6A–7 *with EX1010* at FIG. 52.

B. Claim 16: “The chip package of claim 10, wherein said second region is a rectangle region and surrounding said first region.”

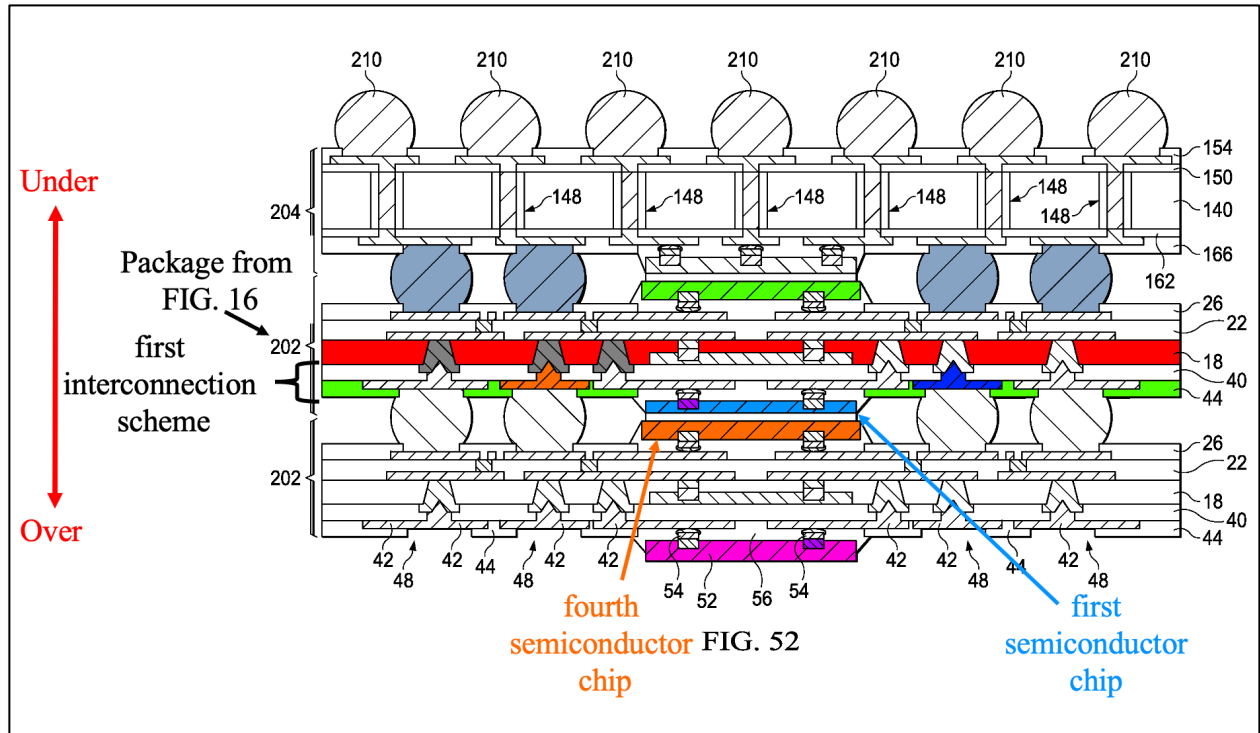
451. See ¶¶ 449-450, incorporated herein.

XII. OPINIONS REGARDING GROUND 2C: CLAIM 21 IS OBVIOUS OVER YU, LIN-191, AND CAMACHO

A. Claim 21

- 1. 21(a): “The chip package of claim 18, further comprising a fourth semiconductor chip over said first semiconductor chip,”**

452. See ¶ 304, incorporated herein. Claim 21(a)'s *fourth semiconductor chip* corresponds to Claim 10(g)'s *second semiconductor chip*. As shown, *fourth semiconductor chip* is over said *first semiconductor chip*:



EX1010 at FIG. 52.

2. 21(b): “wherein said *fourth semiconductor chip* comprises a *third metal pad* at a *bottom surface* of said *fourth semiconductor chip*,”

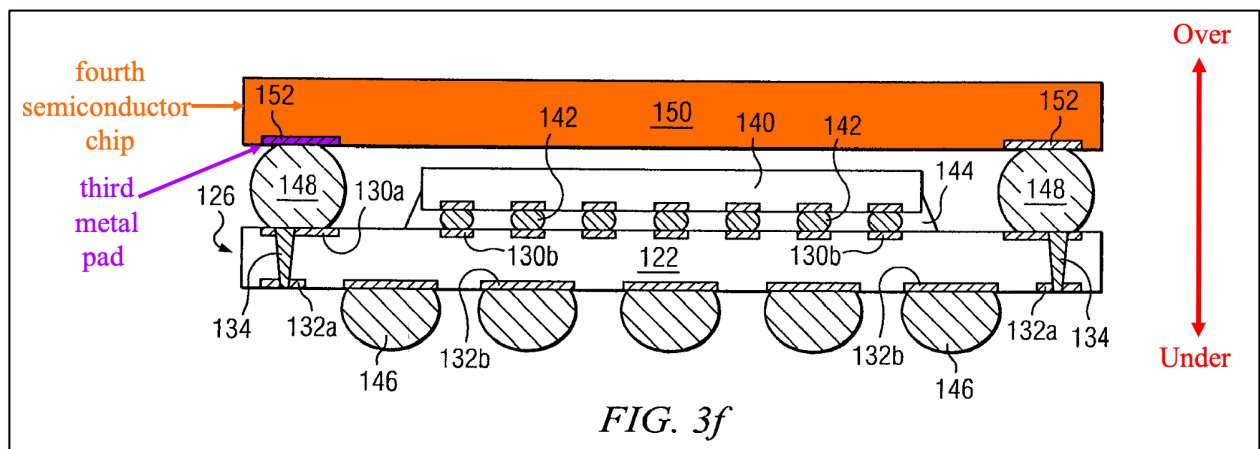
a) Camacho’s Teachings

453. Camacho teaches a forming a “conductive TSV through a WLSCP [wafer level chip scale package]” semiconductor die. EX1006 at [0039], [0008], [0010]. Camacho’s package includes a die 150 (*fourth semiconductor chip*) that has

“contact pads 152.” *EX1006* at [0047]. A POSITA would have understood contact pads 152 to be *metal pad[s]* because metal pads were a standard feature of semiconductor chips to facilitate electrical communication with other components. *See, e.g., EX1044* at 2:30-33 (“In FIG. 1, a **metal pad** 12 is formed on a semiconductor material 10. Metal pad 12 may be formed from a conductive metal...”)(emphasis added); *EX1045* at [0006] (“FIG. 1 illustrates a portion of flip chip 10 with a solder bump 12 formed on **metal contact pad** 14.”)(emphasis added); *EX1046* at [0018] (“Bumps 105 electrically and possibly physically contact the I/O pads (**metal pads**) 103 of the IC chip 100.”); *EX1095* at (“I/O terminals were **traditionally** formed by way of **metal pads** along the periphery of an IC.”).

454. To the extent it is argued contact pads are not *metal pads*, a POSITA would have found it obvious to configure contact pads 152 to be a *metal pad* at least because contact pads were well known in the art to be metal. *See ¶ Error! Reference source not found.* Indeed, in the embodiment of FIG. 2a, Camacho teaches “contact pads 76” on a “semiconductor die 74 are made of metal, e.g., “aluminum.” *EX1006* at [0035]. Further, Camacho expressly teaches that the *metal pad[s]* on semiconductor die 122 are *metal*. *EX1006* at [0041] (“Conductive layers 130 and 132 can be one or more layers of Al, Cu, Sn, Ni, Au, Ag, or other suitable electrically conductive material.”). A POSITA would have recognized that Camacho’s method

of forming *metal* conductive layers 130 and 132 on semiconductor die 122 and metal contact pads 76 on die 74 would have been a simple and congruent way to form contact pads 152 on semiconductor die 150. Further, contact pads 152 electrically connect die 150 to die 122 through solder bumps 148 and conductive layer 130a such that a POSITA would have found it obvious for the pads 152 to be metal to make the electrical connection, as metal pads were ubiquitous for forming electrical connections in chip packages. *EX1006* at [0047]-[0048]; ¶ **Error! Reference source not found.** Accordingly, Camacho teaches *wherein said fourth semiconductor chip comprises a third metal pad at a bottom surface of said fourth semiconductor chip*:



EX1006 at FIG. 3f.

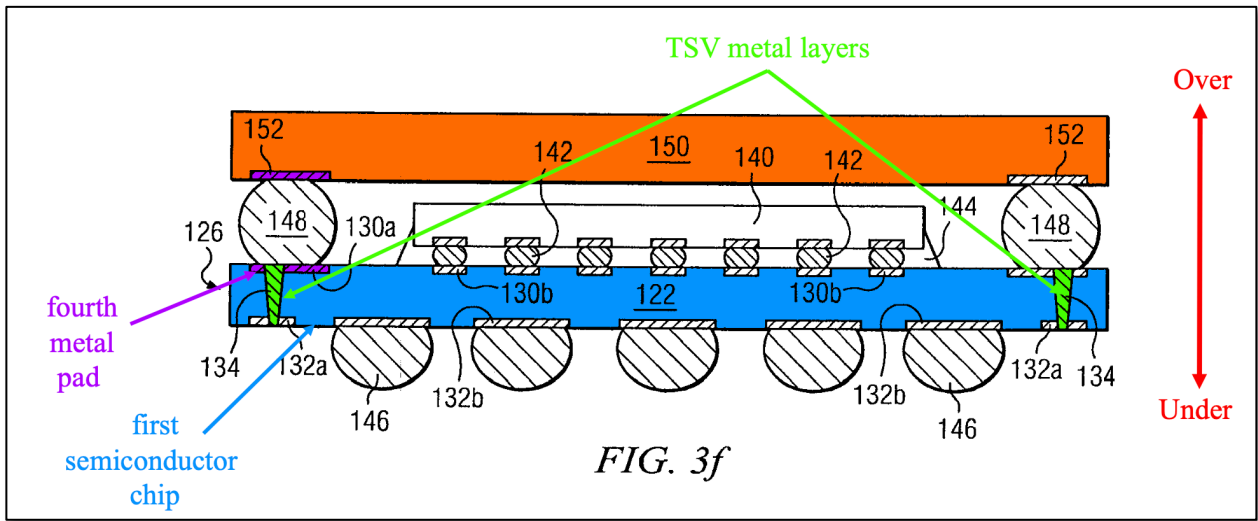
455. A POSITA would have been motivated, found it obvious, and had a reasonable expectation of success in modifying Yu's die 62 to have *a third metal pad at a bottom surface* per Camacho because, as I described above, metal pads were

a standard feature of semiconductor chips for electrically connecting chips to other components. *See* ¶ 453.

3. *21(c): “wherein said first semiconductor chip further comprising a plurality of through-silicon-via metal layers and a fourth metal pad at a top surface of said first semiconductor chip,”*

a) **Camacho’s Teachings**

456. Camacho teaches “a plurality of vias is formed through semiconductor wafer 120[,]” and “filled with” conductive metals “to form *conductive TSV 134*.” *EX1006* at [0043], [0047] (“Conductive layers 130 and 132 are electrically connected by TSV 134.”). Camacho thus teaches *a plurality of through-silicon-via metal layers* (TSVs 134) An “electrically conductive layer 130 is formed over the top active surface of semiconductor die 122[,]” and formed into “individual portions or sections 130a-130b.” *EX1006* at [0041]. Similarly, “an electrically conductive layer 132 is formed over the bottom surface of semiconductor die 122[,]” yielding individual sections 132a-132b. *EX1006* at [0041]. Conductive layers 130, 130 are both “one or more layers of Al” (i.e., aluminum). *Id.* Conductive layer 130a, shown below, is thus a *fourth metal pad at a top surface of a first chip*. *EX1006* at [0041].



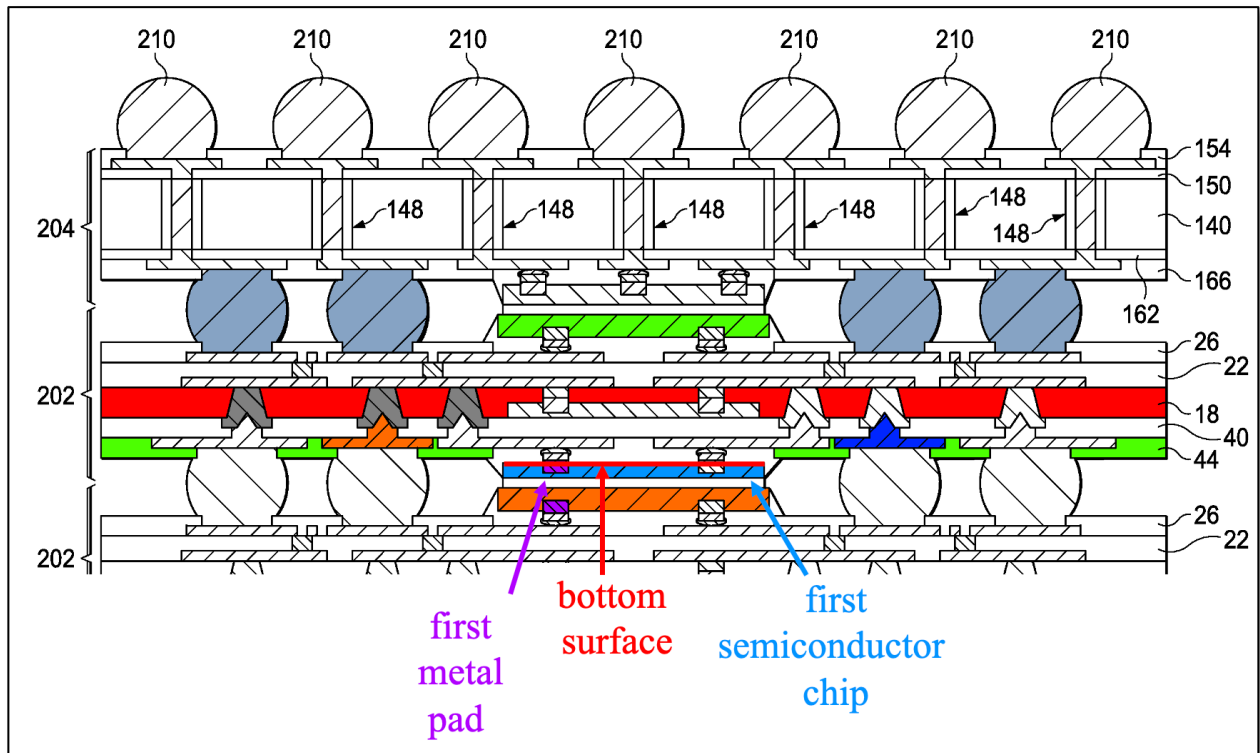
EX1006 at FIG. 3f.

457. A POSITA would have been motivated, found it obvious, and had a reasonable expectation of success in modifying Yu per Camacho to advantageously provide Yu's chip with TSVs, enabling interconnection directly between chips. Indeed, it was known that using TSV technology, 3D ICs can pack a great deal of functionality into a small 'footprint.' Thus, critical electrical paths through the device can be drastically shortened, leading to faster operation." *EX1067* at [0005]. Additionally, POSITA would have found it obvious, been motivated, and had a reasonable expectation of success in modifying Yu to provide die 52 with its own set of pads so that each chip has top and bottom pads connected to one another. By providing metal pads on either surface, Yu's chip would thus have the ability to electrically connect to additional electrical components (e.g., additional components

on either side of the chip) in the chip package. *See, e.g., EX1095* at (“I/O terminals were traditionally formed by way of metal pads along the periphery of an IC.”).

4. *21(d): “wherein said first metal pad is at a bottom surface of said first semiconductor chip,”*

458. The *first metal pad*, discussed above at Claim 18(d)(i), is *at a bottom surface of said first semiconductor chip*:

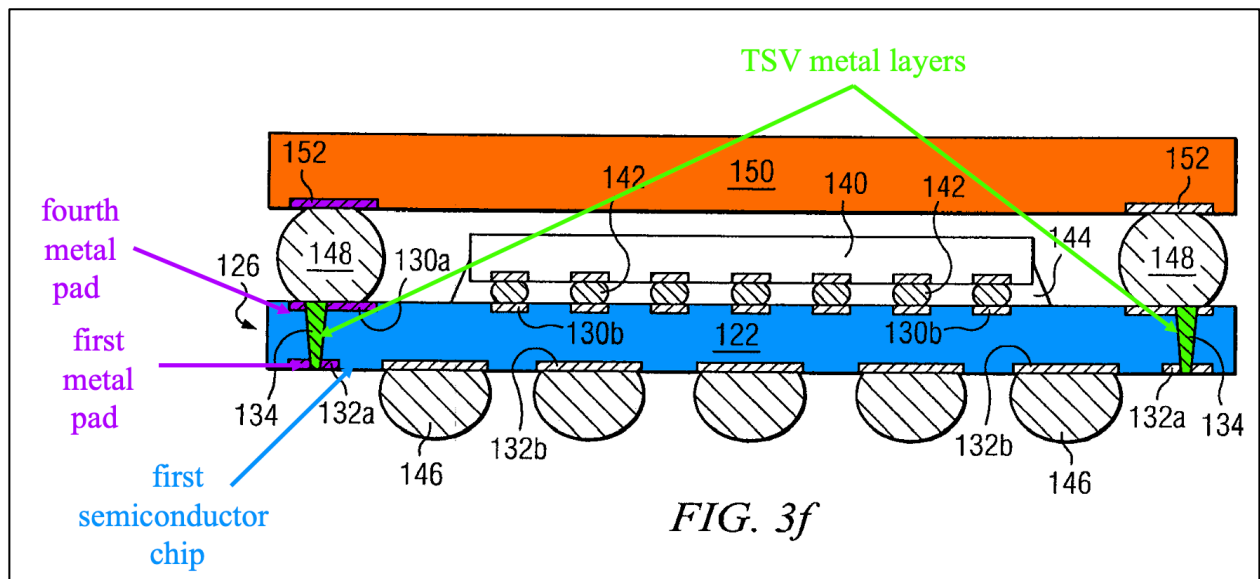


EX1010 at FIG. 52 (excerpt); ¶¶ 426-427.

5. *21(e): “wherein said first metal pad is coupled to said fourth metal pad through one of said plurality of through-silicon-via metal layers,”*

a) Camacho's Teachings

459. As described above, Camacho teaches that layers 130, 132 are “electrically connected” by TSV 134, such that Camacho’s *first metal pad* is coupled to said fourth metal pad through one of said plurality of through-silicon-via metal layers. EX1006 at [0047]; ¶ 456.



EX1006 at FIG. 3f.

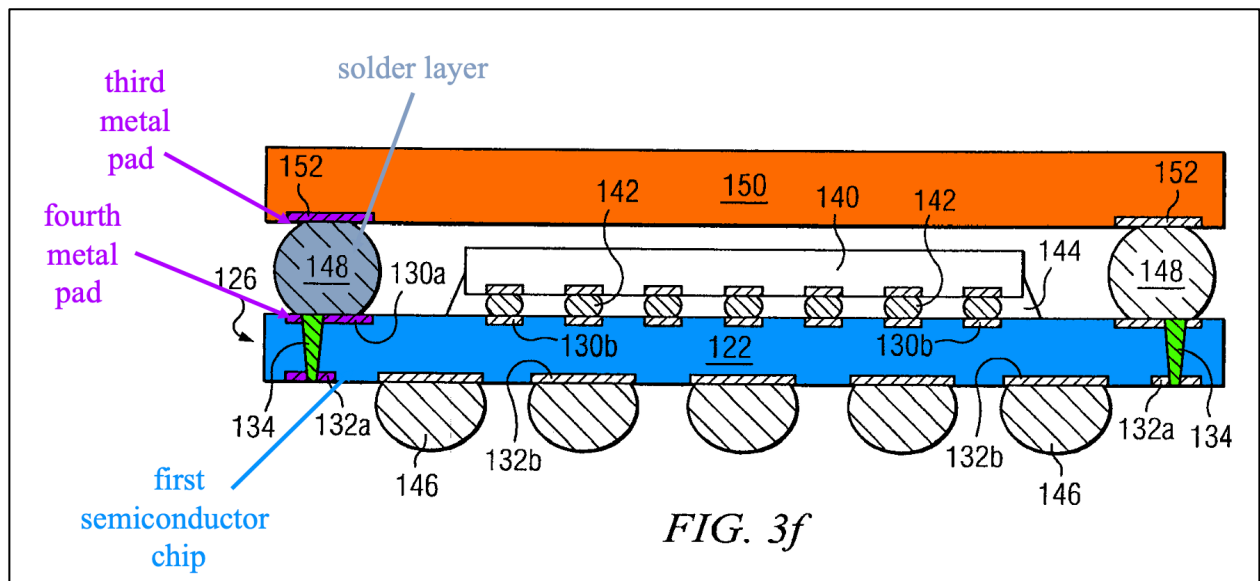
460. In the combination, Yu’s die 52 is modified, per Camacho, to have a *fourth metal pad* and a *TSV metal layer*, which connects to Yu’s existing *first metal pad*. The MTCs and reasonable expectation of success are below. See ¶¶ 463-466.

6. 21(f): “wherein said third metal pad is coupled to said fourth metal pad through a solder layer.”

a) Camacho’s Teachings

461. Camacho’s *third metal pad* is connected to the *fourth metal pad* by a bump 148 where the “bump material” is “solder[.]” EX1006, [0046], [0047]

(“Contact pads 152 on semiconductor die 150 are electrically connected to bumps 148, conductor layer 130a...”). As discussed, solder bumps are formed of a *solder layer* such that Camacho’s bump 148 is a *solder layer* coupling third and fourth metal pads. See ¶¶ 71-76.



EX1006 at FIG. 3f.

462. A POSITA would have been motivated, found it obvious, and had a reasonable expectation of success in modifying Yu’s per Camacho’s teachings to reduce misalignment when stacking chips. See ¶¶ 277-279

7. Motivation to Combine

463. A POSITA would have been motivated and found it obvious to modify Yu per the teachings of Camacho such that Yu’s *fourth semiconductor chip* is connected to the *first semiconductor chip* through a *solder layer*. This modification

would have advantageously provided a shorter electrical path between Yu's *first* and *fourth semiconductor chip[s]* as the chips would be directly connected via the solder layer, instead of electrically connected by the RDLs, TMVs 38, connectors 58 and connectors 54/64. A POSITA would have found this to be advantageous for applications requiring relatively fast communication between the first and fourth chips.

464. Indeed, a POSITA would have been motivated and found it obvious to modify Yu so that the *first semiconductor chip* has *TSV metal layer* connecting *metal pad[s]* on *top* and *bottom surface[s]* of the chip to enable an electrical connection through the chip. TSVs were a well-known method by which to pass signals through chips and were advantageous by not increasing the height added to the package. Indeed, it was known that TSV's "which are vertical connections 'etched through the silicon wafer and filled with metal'" allows for "the addition of many more pathways between 2D layers" in a chip package." *EX1066* at [0017]. Additionally, by "using TSV technology, 3D ICs can pack a great deal of functionality into a small 'footprint.' Thus, critical electrical paths through the device can be drastically shortened, leading to faster operation." *EX1067* at [0005]. As such, a POSITA would have recognized that by forming a TSV connecting metal pads in Yu's die 52 would have allowed for additional chips to be stacked thereon and for "critical electrical

paths” to be short, leading to efficient communication between such chips. *EX1067* at [0005]. Additionally, the modification to Yu so the *first* and *fourth semiconductor chips* have *metal pads* is merely an implementation detail a POSITA would have found obvious and been motivated to implement so the *chips* were electrically connected to Yu’s *chip package*, as TSV’s connecting *metal pad[s]* on semiconductor chips was standard practice for facilitating electrical communication between chips. *See, e.g., EX1006* at FIG. 3f; *EX1004* at FIGS. 3, 32; *EX1126* at FIG. 1, [0056].

465. Further, coupling the *fourth semiconductor chip* to the *first semiconductor chip through a solder layer* would have been obvious and advantageous to electrically connect the two chips using a well-known, cost-efficient technique that would have been easily implementable in Yu’s chip package. Indeed, as I discussed above, electrically connecting metal pads on chips using solder bumps (i.e., *solder layer*) was standard practice and provided the benefit of self-alignment, thereby reducing the risk of misaligned chips in the chip stack. *See ¶¶ 277-279*. As Yu already teaches solder connections e.g., connectors 58, 54/64, a POSITA would have found it obvious to apply Camacho’s teachings of the same to couple the first and fourth chips.

466. The combination is the application of known techniques (TSV metal layers interconnecting pads) to a known device (Yu's chip package) to yield predictable results. There would have been a reasonable expectation of success because Camacho's teachings are representative of commonplace methods to electrically connect chips in a semiconductor package, i.e., the use of TSVs and solder layers. *See* ¶¶ 276-277. Further, Camacho teaches well known methods of forming the TSV metal layer, such as "laser drilling," which is a technique that a POSITA would have been familiar with. *EX1006* at [0043]; *EX1128* at 5:32-34 ("...method known to one of ordinary skill in the art, such as by laser drilling[.]"). Moreover, the metal portion of TSV metal layer 134 is formed by "PVD, CVD, electrolytic plating" which are techniques already taught by Yu, further leading to reasonable expectation of success. *EX1006* at [0043]; *EX1010* at 3:5-8 ("A seed layer...is deposited...such as by sputtering or another **physical vapor deposition** process.), 3:11-14 ("Conductive material...is deposited...such as by...electroplating[.]").

XIII. CONCLUSION

467. I declare that all statements made herein of my knowledge are true, and that all statements made on information and belief are believed to be true, and that these statements were made with the knowledge that willful false statements and the

like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Dated: November 21, 2025

By: 

Dr. Stanley R. Shanfield

Stanley Shanfield



Curriculum Vitae for Stanley Shanfield

Education:

Massachusetts Institute of Technology, Ph.D., Physics, 1981

University of California, Irvine, B.S. Cum Laude, Physics, 1977

Educational Awards:

Outstanding Research Project, U.C. Regents Award, 1977

Phi Beta Kappa, 1977

Four Year Scholarship, Tuition & Research, ERDA/DOE, 1977-1981

Hands-On Professional Expertise:

Semiconductor Physics & Chemistry
Semiconductor Fabrication: Silicon and III-V Materials
Semiconductor Device & Integrated Circuit Engineering
Semiconductor Equipment: Front & Back End
Semiconductor Packaging Design and Manufacturing
Passive Component Design and Manufacturing
RF Design and Fabrication
Digital Design & Fabrication
Semiconductor Manufacturing in Silicon and III-V Materials
MEMS Design and Fabrication: Electrical, Optical, & Sensing Devices
Fiber Optic Device Design and Fabrication
Integrated Optics & Electro-Optical Devices
Plasma Physics

Specialized Training:

Global Positioning Electronics, Systems and Components
Six Sigma Semiconductor Manufacturing
Microwave Engineering
US Patent Law in Technology
Patent Application and Prosecution
Semiconductor Plasma Processing
Thin Film Physics and Technology
MEMS-based Gyroscopes and Accelerometers
Thermoelectric Materials & Technology
Phased Array Radar Engineering
Antennas and Electromagnetic Propagation
Solid State Optical Devices
Fiber Optic Communication System Operation
HALT and HAST Reliability Testing Methods

Professional Experience:

Draper Laboratory Cambridge, MA

2003 – present

Division Leader, Advanced Hardware Development Distinguished Member of Technical Staff Technical Director

Led division (about 80 staff) in re-invigorating multi-chip integrated circuit module facility, more than doubling associated revenues in two years. By most accounts, made division a viable business & technological entity again. Invented & led implementation of an ultra-miniature electronics fabrication technology which became a top laboratory priority. Led team in realization & fabrication of a newly designed precision MEMS-based gyroscope and associated ASIC. Found funding and led team in developing a miniature power source with energy density at least two orders of magnitude higher than any source previously built. Developed fabrication technology for semiconductor-based low phase noise oscillator design, allowing for receiver operation with extremely low signal strength. Many awards received, most recently, the Draper 2010 Distinguished Performance Award, and 2010 Best Patent Award.

Clarendon Photonics Newton, MA

2001 – 2003

Director, Packaging & Integration

30 person photonic chip startup with \$18 million 2nd round funding. Invented and productized new, low cost and reliable semiconductor processing, packaging and pig-tailing technology for optical add-drop multiplexer. Established assembly and packaging process, and developed control electronics. Partner with Micron Technologies, using their R&D semiconductor facility.

AXSUN Technologies Bedford/Billerica, MA

1999 – 2001

Vice President, Operations 1999 – 2000

Initially three staff members with \$6 million funding. Designed, fabricated and productized AXSUN's micro-electromechanical (MEM) Fabry-Perot optical filter. Patents granted on semiconductor processing and control electronics. Completed facility and semiconductor processing design, then completely equipped. Raised 2nd round funding for \$36 million. Established process and fabrication facility in Belfast, Northern Ireland for producing thick oxide silicon-on-insulator material.

Director, Manufacturing & Wafer Fab Technology

2000 – 2001

After 3rd round funding, led device manufacturing, creating wafer fab and assembly infrastructure; hired 70+ people, led production. Delivered first generation product for revenue to multiple customers. Converted pure technology to dominant company revenue with high yield.

Company purchased by Volcano Technologies, San Diego.

Raytheon Corporation Lexington/Andover, MA

1985 - 1999

Manager, Semiconductor Operations

1996 – 1999

Built and led a 300 employee, \$60 million revenue 24/7 semiconductor development and manufacturing operation resulting from the consolidation of a number of smaller organizations. Key player in technological development and recipient of Raytheon's 6 Sigma Leadership training. Decision maker in Texas Instrument group acquisition, providing significant expert opinion on semiconductor and design facilities. Obtained state-of-art yields using best available steppers, deep reactive ion etching, plasma assisted CVD, and ion-implantation equipment, and disciplined design-for steppers, deep reactive ion etching, plasma assisted CVD, and ion-implantation equipment, and disciplined design-for-manufacturing circuit design and layout methodology.

Research Laboratory Manager

1992 – 1996

Leader of a 90 employee development and contract research organization in high performance semiconductor devices and circuits, measurement, assembly and wafer fab. Led a team which invented and implemented a major revenue generating technology (\$.100 million) based on semiconductor device development (pseudomorphic high electron mobility transistor). Increased outside research funding by 50% in 3 years through superior technical performance relative to competitors.

Section Manager, Semiconductors & ICs

1985 – 1992

Led a MM-Wave Circuit and Module Development program over 2 years, leading to production win of a satellite terminal electronics generating \$320 million in sales. Developed processes for fabricating high power, high frequency multi-function integrated circuits, and combining high performance digital and analog devices in a single integrated circuit.

Spire Corporation Bedford, MA

1981 – 1984

**Staff Scientist
Senior Staff Scientist**

Developed new methods for low temperature deposition of plasma-assisted CVD epitaxial silicon. Wrote joint papers with MIT professor, and had process adopted by equipment manufacturers. Built, operated and characterized ion-assisted deposition system for making coating for semiconductor and machine tool industries. Process eventually purchased by Kennametal, Inc.

Publications

Restricted Publications & Reports

Process Sequence for Formation of Ultra-High Density Multi-Chip Modules:

A high yield, low cost method for creating a system-in-a-package consisting of numerous semiconductor die, passive components, and sensors. Process formed basis for new (2008) facility.

Design and Method of Fabrication of Ultra-High Density Radioisotope Power Source:

In test, a miniature power source that achieves energy density more than 1000X the best chemical battery. Method uses planar semiconductor processing of bulk thermoelectric materials.

Design and Method of Achieving Extremely Low Crystal Oscillator Phase Noise:

Method developed for very low power refrigeration of quartz or sapphire crystal resonators, resulting in extremely low phase noise oscillators. The low phase noise allows extremely high sensitivity in digital receivers, including GPS receivers, leading to use in extremely low signal conditions.

Design, Evaluation & Production of MEMS-based Fabry-Perot Interferometer:

Design and method for ultra-compact spectral analyzer made using semiconductor and optical thin film processing.

Design & Evaluation of Ultra-Fast Control Electronics for Integrated Optical Multiplexer:

Design and performance evaluation of silicon-based integrated optical multiplexer using chip-based local heating

Design and Fabrication of Q-band MILSTAR Communications Terminal Transmitter:

Record power and efficiency 44 GHz transmitter design using new transistor design, and combined waveguide

Key Publications (selected)

Process Characterization of PSG and BPSG Plasma Deposition, J. Electrochem. Soc., Volume 131, Issue 9, pp. 2202-2203

A double-recessed Al_{0.24}GaAs/In_{0.16}GaAs pseudomorphic HEMT for Ka- and Q-band power Applications, Electron Device Letters, IEEE, Volume 14, Issue 9, pp. 456 - 458

Formation of Thick Metal Structures on GaAs MMICs Using Image Reversal Lithography and Evaporated Metal Deposition, J. Electrochem. Soc., Volume 136, Issue 9, pp. 2687-2690

Contact Hole Etching in Load-Locked Hexagonal Reactive Ion Etch System, J. Electrochem. Soc., Vol. 131, No. 8, 1984

An AlGaAs/InGaAs pseudomorphic high electron mobility transistor with Improved Breakdown Voltage for X and Ku-band power applications, Microwave Theory and Techniques, IEEE Transactions on, Volume 41, Issue 5, May 1993, pp. 752 - 759

Hot-electron-induced Degradation of Metal-Semiconductor Field-Effect Transistors, Integrated Circuit Symposium, 1994. Technical Digest 1994., 16th Annual Volume , Issue , 16-19 Oct. 1994, pp. 259

Ion Beam Deposition of Cubic Boron Nitride, J. Vac. Sci. Technol. A Volume 1, Issue 2, pp. 323-325

Patents**US Patent 6504235 - Passivation layer and process for semiconductor devices**

Method of coating semiconductor devices that prevented parametric shift in electrical performance. Solved key processing problem.

US Patent 4440108 - Ion Beam Deposition Apparatus

Design of equipment for deposition of thin films in the presence of ion bombardment. System produced thin films of interest for mechanical, electrical and optical properties and was sold as an equipment product.

US Patent 6525880 - Integrated Tunable Fabry-Perot filter and Method of Making Same

Design and method for fabricating very small, very high performance variable optical filter using semiconductor fabrication technology. In current use in fiber optical networks, chemical sensors, and 3-D medical imaging applications.

US Patent 5175020 - Boron Nitride Films and Process of Making Same

Ion assisted deposition of ultra-hard cubic boron nitride films for semiconductor and machine tool applications. Significant use in both areas.

US Patent 4526673 - Coating Method

Method for deposition of thin films used in semiconductor device fabrication. Method based on direct control of the kinetics of thin film deposition.

US Patent 7727806 - Systems and Methods for High Density Multi-Component Modules

Method for fabrication of electronic modules using multiple thinned integrated circuits, patterned multi-level interconnects, passive electronic components, and sensors

US Patent Application 2009/TBD - Devices, systems, and methods for controlling the temperature of resonant elements

Devices and systems for achieving low phase noise crystal oscillators using unique low power thermoelectric structures

Expert Witness Experience:

See attachment

Contact information for Stanley Shanfield

STANLEY SHANFIELD

342 Otis Street
Newton, MA 02465

Phone:

617-969-9574 (home)
617-258-3392 (office)
617-699-7262 (mobile)

Email: shanfield@alum.mit.edu