IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

MYW SEMITECH, LLC, Plaintiff, **v.** **APPLE INC.,** Defendant.	**Case No. 25-cv-504-RGA** **JURY TRIAL DEMANDED**

AMENDED COMPLAINT FOR PATENT INFRINGEMENT

Plaintiff MYW Semitech, LLC ("MYW Semitech"), by and through its undersigned counsel, files this Amended Complaint against Defendant Apple Inc. ("Apple" or "Defendant") for patent infringement of United States Patent Nos. 11,107,768; 11,538,763; and 11,894,306 (the "Patents-In-Suit") and alleges, based on information and belief, as follows:

NATURE OF THE ACTION

1. This is an action for patent infringement arising under the patent laws of the United States, 35 U.S.C. §§ 1 *et seq*.

PARTIES

2. Plaintiff MYW Semitech is a Delaware corporation with a place of business at 8 The Green, Suite A, Dover, Delaware 19901.

3. Apple, Inc. is a publicly traded company organized and existing under the laws of the state of California. Apple may be served with process through its registered agent, CT Corporation System at 818 W. Seventh St., Los Angeles, CA 90017.

JURISDICTION AND VENUE

4. This Court has jurisdiction over the subject matter of this action pursuant to 28 U.S.C. §§ 1331 and 1338(a) because the action arises under the patent laws of the United States, 35 U.S.C. §§ 1 *et seq*.

5. On information and belief, Apple is subject to this Court's personal jurisdiction in accordance with due process and/or the Delaware Long-Arm Statute.

6. This Court has personal jurisdiction over Apple because Apple has sufficient minimum contacts with this forum as a result of business conducted within the State of Delaware and this judicial district. In particular, this Court has personal jurisdiction over Apple because, *inter alia*, Apple has substantial, continuous, and systematic business contacts in this judicial district, and derives substantial revenue from goods provided to individuals including in this judicial district.

7. Apple has purposefully availed itself of the laws of, and of the privileges of conducting business within, this judicial district, has established sufficient minimum contacts with this judicial district such that it should reasonably and fairly anticipate being hauled into court in this judicial district, has purposefully directed activities at residents of this judicial district, and at least a portion of the patent infringement claims alleged in this Complaint arise out of or are related to one or more of the foregoing activities.

8. On information and belief, Apple has litigated cases before this Court in which it admitted that venue was proper, did not contest personal jurisdiction and/or venue, and/or filed a complaint or counterclaims, including *Openwave Systems, Inc. v. Apple Inc., et al.*, 1:11-cv-00765-RGA (D. Del.); *Apple Inc. v. Masimo Corporation and Sound United, LLC* 1:22-cv-01377-JLH (D. Del.); *Memory Integrity, LLC v. Apple, Inc.*, 1:13-cv-01796-GMS (D. Del.).

9. This Court has personal jurisdiction over Apple because Apple (directly and/or through its subsidiaries, affiliates, or intermediaries) has committed and continues to commit acts of infringement in this judicial district in violation of at least 35 U.S.C. § 271(a). In particular, on information and belief, Apple manufacturers, uses, sells, offers for sale, imports, advertises, and/or otherwise promotes infringing products in the United States, the State of Delaware, and this judicial district.

10. On information and belief, Apple has a regular and established place of business within the District of Delaware, including 125 Christiana Mall, Newark, Delaware 19702. On information and belief, Apple has physical stores and employees in this judicial district.

11. Venue is proper in this judicial district under 28 U.S.C. §§ 1391(b)-(d) and/or 1400(b) at least because Apple has committed acts of infringement within this judicial district giving rise to this action.

THE ASSERTED PATENTS

United States Patent No. 11,107,768

12. On August 31, 2021, the United States Patent and Trademark Office duly and legally issued United States Patent No. 11,107,768 ("the '768 patent") entitled "Chip Package" to inventor Ping-Jung Yang. A true and correct copy of the patent is attached as Exhibit A.

13. The '768 patent is presumed valid under 35 U.S.C. § 282.

14. MYW Semitech owns all rights, title, and interest in the '768 patent.

United States Patent No. 11,538,763

15. On December 27, 2022, the United States Patent and Trademark Office duly and legally issued United States Patent No. 11,538,763 ("the '763 patent") entitled "Chip Package" to inventor Ping-Jung Yang. A true and correct copy of the patent is attached as Exhibit B.

16. The '763 patent is presumed valid under 35 U.S.C. § 282.

17. MYW Semitech owns all rights, title, and interest in the ’763 patent.

United States Patent No. 11,894,306

18. On February 6, 2024, the United States Patent and Trademark Office duly and legally issued United States Patent No. 11,894,306 (“the ’306 patent”) entitled “Chip Package” to inventor Ping-Jung Yang. A true and correct copy of the patent is attached as Exhibit C.

19. The ’306 patent is presumed valid under 35 U.S.C. § 282.

20. MYW Semitech owns all rights, title, and interest in the ’306 patent.

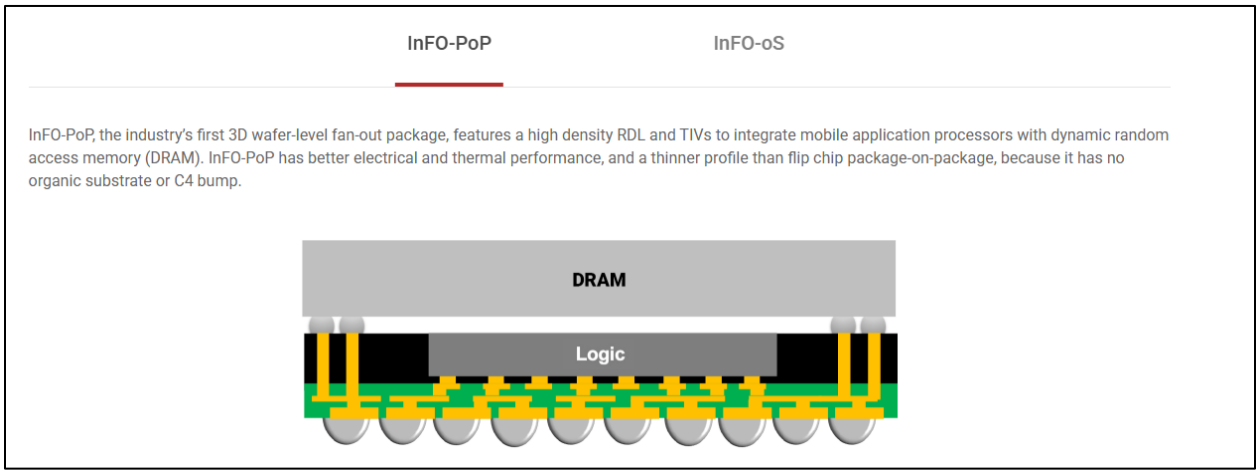
THE ACCUSED APPLE PRODUCTS

21. Apple makes, sells, and offers for sale phones, tablets and computers, including the iPhone 7, iPhone 7 Plus, iPad 6th generation, iPad 7th generation, iPad Pro 2nd generation, Apple TV 4K 1st generation, iPhone 8, iPhone 8 Plus, iPhone X, iPhone XR, iPhone XS, iPhone XS Max, iPad Air 3rd generation, iPad mini 5th generation, Apple TV 4K 2nd generation, iPad Pro third generation, iPad Pro 4th generation, 2020 Mac mini-based Developer Transition Kit, iPhone 11, iPhone 11 Pro, iPhone 11 Pro Max, iPhone SE 2nd generation, iPad Air, iPhone 12, iPhone 12 Mini, iPhone 12 Pro, iPhone 12 Pro Max, iPhone 13, iPhone 13 Mini, iPhone 13 Pro, iPhone 13 Pro Max, iPad mini 6th generation, iPhone SE 3rd generation, iPhone 14 Pro, iPhone 14 Pro Max, iPhone 15, iPhone 15 Plus, iPhone 15 Pro, iPhone 15 Pro Max, Apple Watch Series 4, Apple Watch Series 5, Apple Watch SE, HomePod mini, Apple Watch Series 6, Apple Watch Series 7, HomePod 2nd generation, Apple Watch Series 8, Apple Watch SE 2nd generation, Apple Watch Ultra, Apple Watch Series 9, and Apple Watch Ultra 2 (“the Accused Apple Products).

22. The Accused Products include chips that have adopted InFO PoP technology. Specifically, Apple utilizes InFO PoP technology in at least the following chips that are included in the Accused Products: Apple A10 Fusion, A10X Fusion, A11 Bionic, A12 Bionic, A12X Bionic, A12Z Bionic, A13 Bionic, A14 Bionic, A15 Bionic, A16 Bionic, A17 Pro, as well as the

Apple S4, S5, S6, S7, S8, and S9 (the "Accused Chips"). *See, e.g.* https://medias.yolegroup.com/*uploads/2019/03/Yole_TSMC_Fan-out_inFO_Apple_A10_iPhone7Plus_Sample.pdf*

23. Exemplary images of the InFO PoP technology that is utilized in the Accused Chips are seen below:



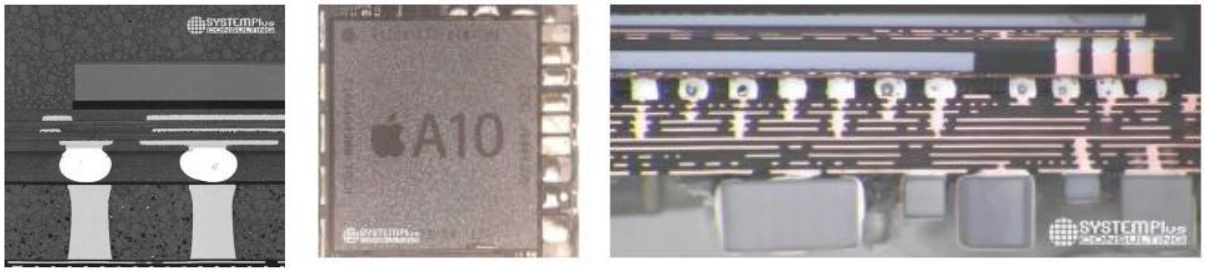
Source: https://3dfabric.tsmc.com/english/dedicatedFoundry/technology/InFO.htm

Attributes	Package Size 14x14mm
CPU voltage droop reduction	1.06X
Max. chip size, mm²	135
CPI sensitivity	Low
TIV/TMV pitch, µm	180
Si thickness, µm	Up to 200

Source: https://semiwiki.com/semiconductor-manufacturers/tsmc/299955-highlights-of-the-tsmc-technology-symposium-2021-packaging/

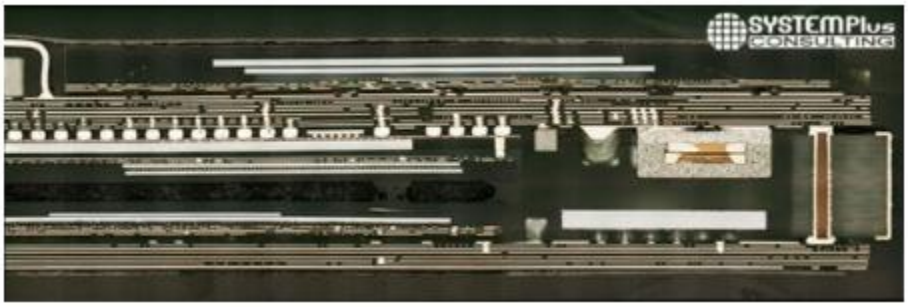
24. Exemplary images of the Accused Chips are seen below:

- **Apple A10**



Source:https://medias.yolegroup.com/uploads/2019/03/Yole_TSMC_Fan-out_inFO_Apple_A10_iPhone7Plus_Sample.pdf

- **Apple A11**

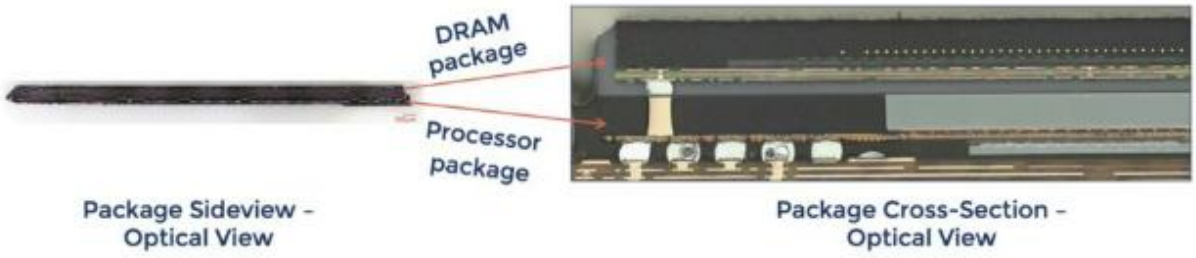


Source: https://www.yolegroup.com/product/report/second-generation-of-tsmcs-integrated-fan-out-info-packaging-for-the-apple-a11-found-in-the-iphone-x/

- **Apple A14**

Source: https://www.yolegroup.com/press-release/apples-a14-and-a15-bionic-the-game-changing-soc-solutions-from-apple/

- **Apple A17**



Source: https://www.yolegroup.com/technology-outlook/unveiling-the-iphone-15-pro-max-and-a17-pro-processor-the-chronicles-by-yole-systemplus/

25. The Accused Apple Products infringe each of the Patents-in-Suit.

CLAIMS FOR RELIEF

COUNT I – Infringement of United States Patent No. 11,107,768

26. The allegations set forth above are re-alleged and incorporated by reference as if they were set forth fully here.

27. Defendant has infringed (literally and/or under the doctrine of equivalents) and continues to infringe the ’768 patent in the State of Delaware, in this judicial district, and elsewhere in the United States, by and among other things, making, using, importing, offering for sale, and/or selling the Accused Apple Products, which are covered by at least claims 1-5, 7-8, 10-11, 14-15, 16-17, 19-20, 22-23, 25-28 of the ’768 patent (the “Asserted Claims”).

28. Claim 1 recites:

> 1. A chip package comprising:
> a first polymer layer having a first surface and a second surface opposite to said first surface, wherein said first surface is substantially parallel to said second surface, wherein said first polymer layer has a thickness between 100 and 300 micrometers and has a coefficient of expansion between 3 and 10 ppm/° C.;
> a first metal plug vertically in a first through via in said first polymer layer, wherein said first metal plug comprises a first copper layer, wherein

the first copper layer contacts with a sidewall of said first through via;

a second metal plug vertically in a second through via in said first polymer layer, wherein said second metal plug comprises a second copper layer, wherein a top surface of said second metal plug and a top surface of said first metal plug are in the same horizontal plane;

a first interconnection scheme over said first surface, wherein said first interconnection scheme comprises a first metal interconnect over said first surface, a second metal interconnect over said first surface, a third metal interconnect over said first surface and a second polymer layer over said first, second and third metal interconnects, wherein said first metal interconnect is connected to said first metal plug, wherein said second metal interconnect is connected to said second metal plug, wherein said first metal interconnect comprises a first metal layer, a third copper layer on said first metal layer, and a fourth copper layer on said third copper layer;

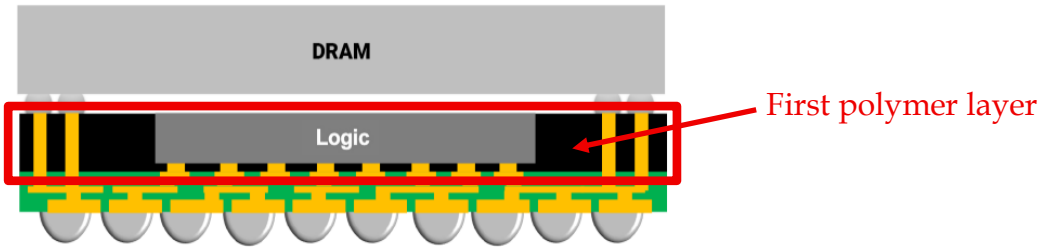
a first metal bump over said first interconnection scheme and said second metal plug, wherein said first metal bump comprises a tin-containing layer; and

a first semiconductor chip under said first interconnection scheme, wherein said first semiconductor chip comprises a fourth metal interconnect on a first metal pad of said first semiconductor chip, wherein said fourth metal interconnect comprises a second metal layer on said first metal pad and a fifth copper layer over said second metal layer, wherein said fifth copper layer has a thickness between 5 and 30 micrometers, wherein said fourth metal interconnect is connected to said third metal interconnect.

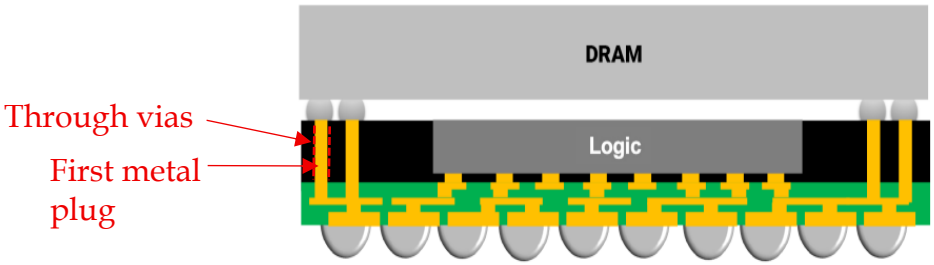
29. More particularly, Defendant infringes at least claim 1 of the ’768 Patent.

30. Each of the Accused Chips is a chip package.

31. Each of the Accused Chips has a polymer layer (“first polymer layer” shown below) having two surfaces that are opposite to and substantially parallel to each other. This polymer layer has a thickness between 100 and 300 micrometers and has a coefficient of expansion between 3 and 10 ppm/° C.

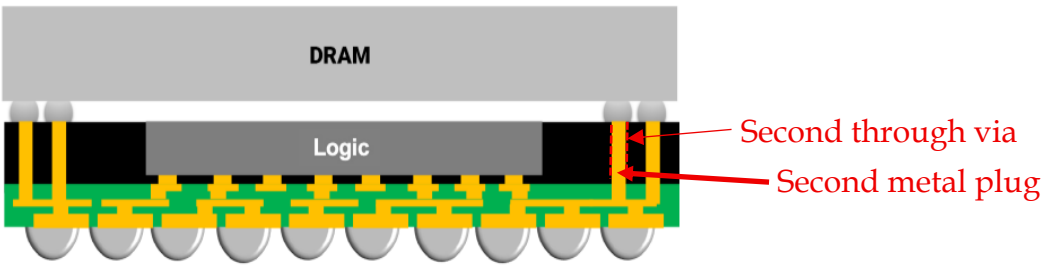


32. Each of the Accused Chips has a metal plug ("first metal plug" shown below) positioned vertically in a through via ("first through via" shown below) in the polymer layer.



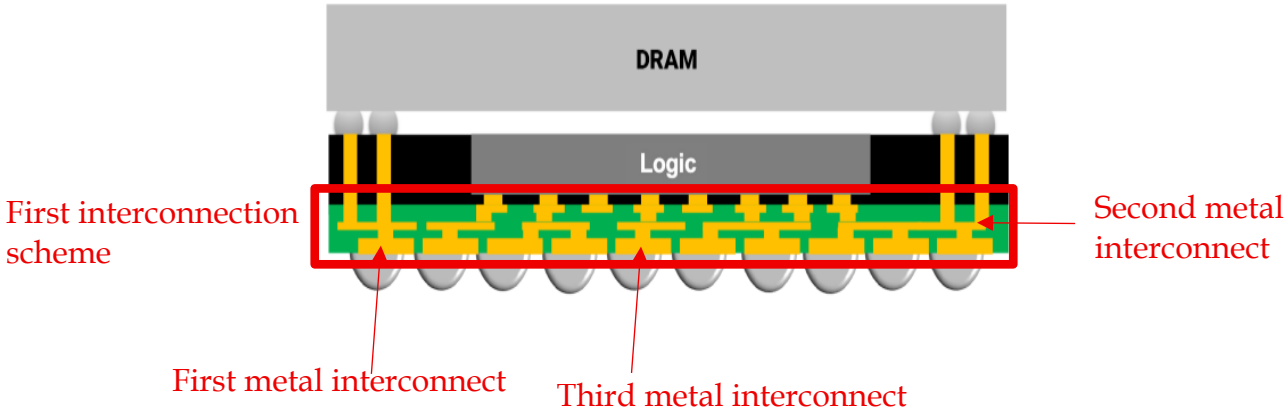
33. The first metal plug has a copper layer ("first copper layer") that contacts the sidewall of the first through via.

34. Each of the Accused Chips has another metal plug ("second metal plug" shown below) positioned vertically in another through via ("second through via" shown below) in the polymer layer.



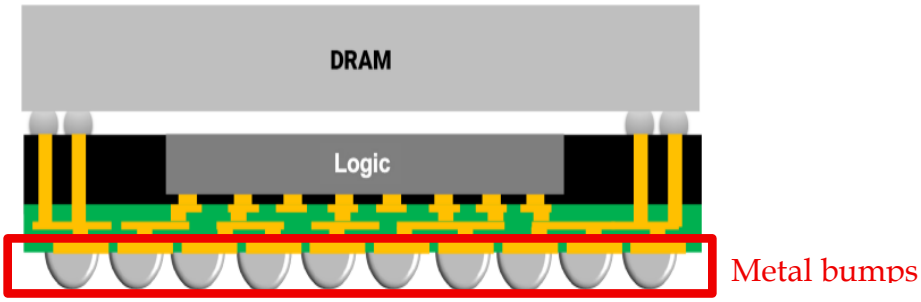
35. The second metal plug ("second metal plug") has a copper layer. The second metal plug has a top surface that is in the same horizontal place with a top surface of the first metal plug.

36. Each of the Accused Chips has an interconnection scheme ("first interconnection scheme" shown below) made up of metal interconnects ("first metal interconnect", "second metal interconnect", and "third metal interconnect" shown below) over a first surface and a polymer layer ("second polymer layer" shown below in green) over the metal interconnects.



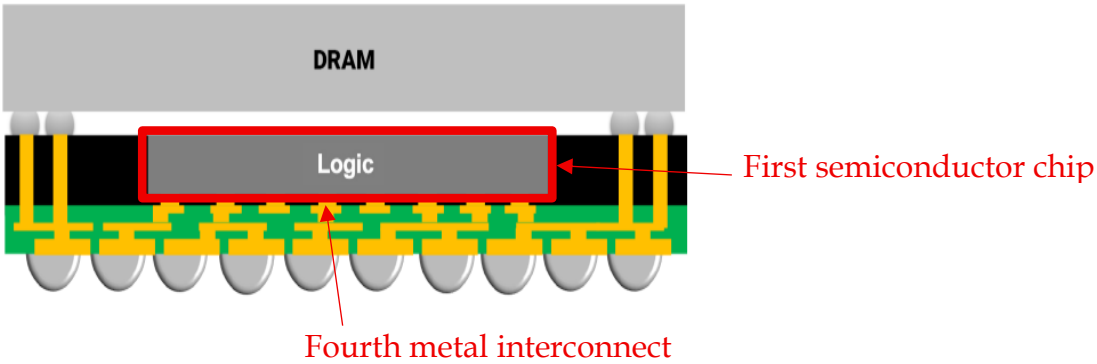
37. The second metal interconnect is connected to the first metal plug and the second metal interconnect is connected to the second metal plug. The first metal interconnect is made up of a first metal layer, a third copper layer on the first metal layer, and a fourth copper layer on the third copper layer.

38. Each of the Accused Chips contains a metal bump ("first metal bump" shown below) over an interconnection scheme and metal plug.



39. The metal bumps comprise a tin-containing layer.

40. Each of the Accused Chips contains a semiconductor chip ("first semiconductor chip" shown below) under an interconnection scheme made up of a metal interconnect ("fourth metal interconnect" shown below) on a metal pad.



41. The metal interconnect comprises a second metal layer on said first metal pad and a fifth copper layer over said second metal layer. The fifth copper layer has a thickness between 5 and 30 micrometers and the fourth metal interconnect is connected to the third metal interconnect.

42. The Accused Apple Products infringe each of the claims 2-5, 7-8, 10-11, 14-15, 16-17, 19-20, 22-23, 25-28 for the reasons similar to those stated above.

43. By making, using, importing, offering for sale and/or selling such products that are covered by one or more claims of the '768 patent, MYW Semitech has been damaged by the direct infringement of Apple and is suffering and will continue to suffer irreparable harm and damages as a result of this infringement.

COUNT II - Infringement of United States Patent No. 11,538,763

44. The allegations set forth above are re-alleged and incorporated by reference as if they were set forth fully here.

45. Defendant has infringed (literally and/or under the doctrine of equivalents) and continues to infringe the '763 patent in the State of Delaware, in this judicial district, and elsewhere in the United States, by and among other things, making, using, importing, offering for sale, and/or

selling the Accused Apple Products, which are covered by at least claims 1-5, 7, 9-15, 17 of the ’763 patent.

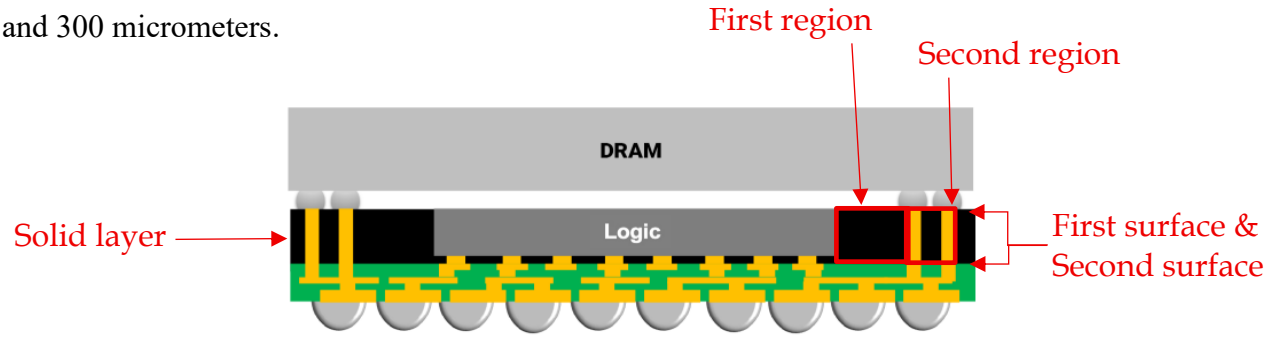
46. Claim 1 recites:

> 1. A chip package comprising:
>
> a solid layer having a first surface and a second surface opposite to said first surface, wherein said first surface is substantially parallel to said second surface, wherein said solid layer comprises a compound of silicon and oxygen, wherein said solid layer has a thickness between 100 and 300 micrometers, wherein said solid layer comprises a first region and a second region between said first region and an edge of said solid layer;
>
> a plurality of copper plugs in a plurality of through vias in said second region of said solid layer respectively, wherein one of said plurality of copper plugs comprises a first copper layer contacting a sidewall of one of said plurality of through vias, wherein said first region has a width in a direction greater than a shortest distance between said sidewall of one of said plurality of through vias and said edge of said solid layer in said direction and greater than a pitch between two neighboring copper plugs of said plurality of copper plugs;
>
> a first interconnection scheme over said first surface, wherein said first interconnection scheme comprises a first metal interconnect over said first surface, a second metal interconnect over said first surface and a first polymer layer over said first and second metal interconnects, wherein said first metal interconnect is connected to a first copper plug of said plurality of copper plugs, wherein said second metal interconnect is connected to a second copper plug of said plurality of copper plugs, wherein said first metal interconnect comprises a first metal layer and a second copper layer over said first metal layer, wherein a top surface of said second copper plug and a top surface of said first copper plug are substantially in the same horizontal plane;
>
> a first metal bump over said first interconnection scheme, wherein said first metal bump comprises a second metal layer and a tin-containing layer over said second metal layer; and
>
> a first semiconductor chip under said first interconnection scheme, wherein said first semiconductor chip comprises a third metal interconnect on a first metal pad of said first semiconductor chip, wherein said third metal interconnect comprises a third metal layer on said first metal pad and a third copper layer over said third metal layer, wherein said third copper layer has a thickness between 5 and 30 micrometers.

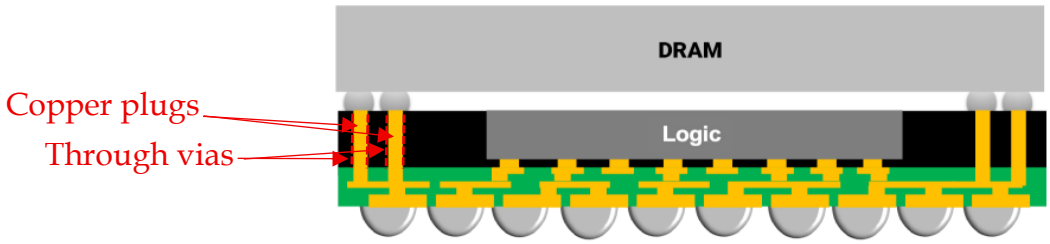
47. More particularly, Defendant infringes at least claim 1 of the ’763 Patent.

48. Each of the Accused Chips is a chip package.

49. Each of the Accused Chips has a solid layer having two surfaces that are opposite and substantially parallel to each other. The polymer layer has two regions ("a first region" and "a second region" shown below) and is comprised of silicon and oxygen, with a thickness between 100 and 300 micrometers.



50. Each of the Accused Chips has copper plugs (shown below) in multiple through vias (shown below) within the second region of the solid layer.

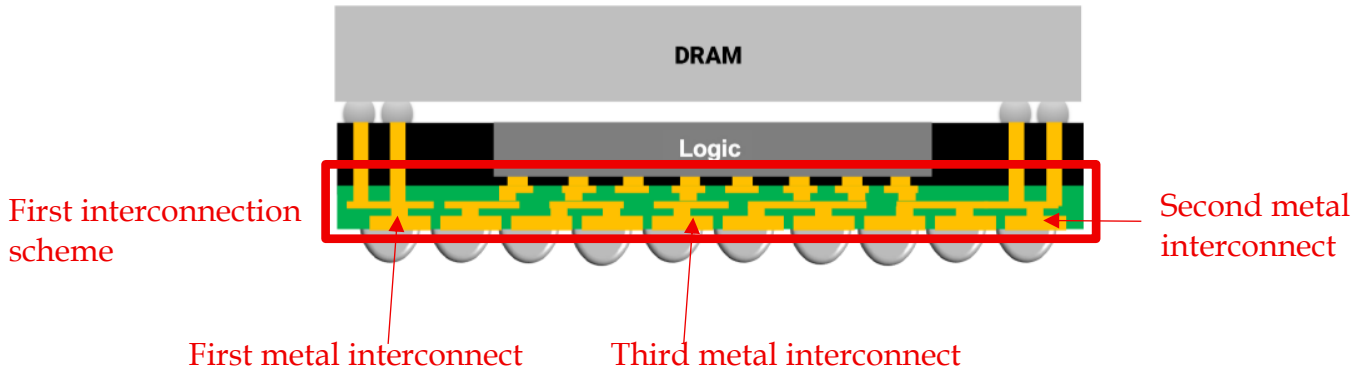


51. One of the copper plugs has a copper layer contacting a sidewall of one of the through vias.

52. The first region has a width in a direction greater than the shortest distance between the sidewall of one of the through vias and edge of the solid layer in a direction greater than the pitch between neighboring copper plugs.

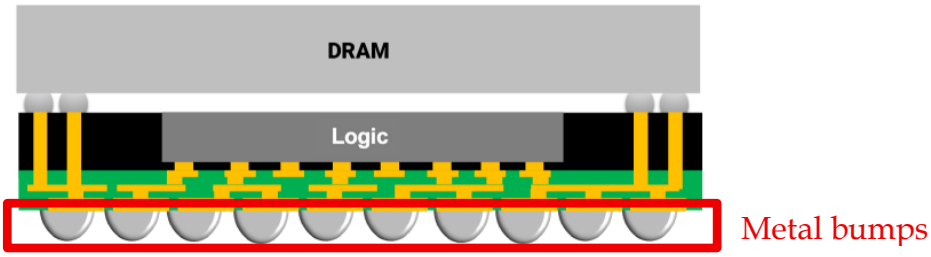
53. Each of the Accused Chips has an interconnection scheme ("first interconnection scheme" shown below) made up of metal interconnects ("first metal interconnect" and "second

metal interconnect" shown below) over a first surface and a polymer layer ("first polymer layer" shown below in green) over the metal interconnects.

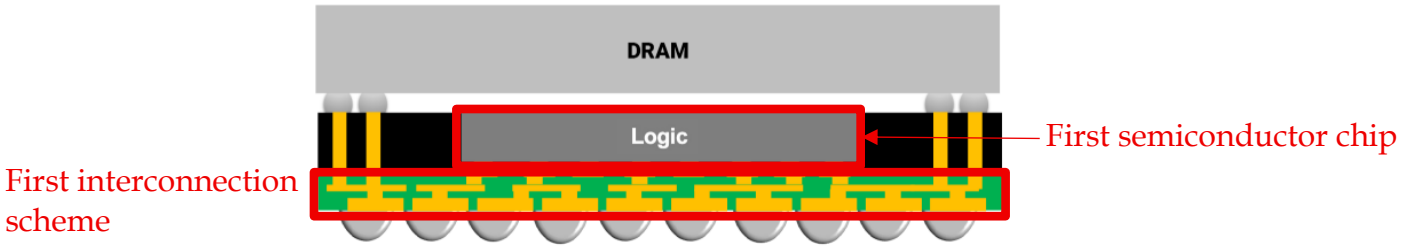


54. The first metal interconnect is connected to a one of multiple copper plugs ("first copper plug") and the second metal interconnect is connected to another copper plug ("second copper plug"). The metal interconnect is made up of a first metal layer and a second copper layer over the first metal layer and the top surface of the second copper plug and the top surface of the first copper plug are in the same horizontal plane.

55. Each of the Accused Chips contains a metal bump (shown below) over the interconnection scheme, wherein the first metal bump has a second metal layer and a tin-containing layer over said second metal layer.



56. Each of the Accused Chips contains a semiconductor chip ("first semiconductor chip" shown below) under the interconnection scheme ("first interconnection scheme" shown below).



57. The semiconductor chip has a third metal interconnect on a first metal pad of the semiconductor chip, wherein said third metal interconnect comprises a third metal layer on said first metal pad and a third copper layer over said third metal layer, wherein said third copper layer has a thickness between 5 and 30 micrometers.

58. The Accused Apple Products infringe each of the claims 2-5, 7, 9-15, 17 for the reasons similar to those stated above.

59. By making, using, importing, offering for sale and/or selling such products that are covered by one or more claims of the ’763 patent, MYW Semitech has been damaged by the direct infringement of Apple and is suffering and will continue to suffer irreparable harm and damages as a result of this infringement.

COUNT III - Infringement of United States Patent No. 11,894,306

60. The allegations set forth above are re-alleged and incorporated by reference as if they were set forth fully here.

61. Defendant has infringed (literally and/or under the doctrine of equivalents) and continues to infringe the ’306 patent in the State of Delaware, in this judicial district, and elsewhere in the United States, by and among other things, making, using, importing, offering for sale, and/or selling the Accused Apple Products, which are covered by at least claims 10-17 of the ’306 patent.

62. Claim 10 recites:

10. A chip package comprising:

a solid layer having a first surface and a second surface opposite to said first surface, wherein said solid layer comprises a compound of silicon and oxygen, wherein said solid layer has a thickness between 100 and 300 micrometers, wherein said solid layer comprises a first region and a second region between said first region and a first edge of said solid layer;

a plurality of copper posts in a plurality of through holes in said second region respectively, wherein said first region has a width in a direction greater than a shortest distance between a sidewall of one of said plurality of through holes and said first edge in said direction and greater than a pitch between two neighboring copper posts of said plurality of copper posts;

a first interconnection scheme over said first surface, wherein said first interconnection scheme comprises a first metal interconnect over said first surface, and a polymer layer over said first metal interconnect, wherein said first metal interconnect is connected to one of said plurality of copper posts, wherein said first metal interconnect comprises a first metal layer and a first copper layer over said first metal layer;

a first metal bump over said first interconnection scheme, wherein said first metal bump comprises a first tin-containing layer;

a second metal bump over said first interconnection scheme;

a first semiconductor chip over said first interconnection scheme and between said first and second metal bumps, wherein said first semiconductor chip has a height between a backside surface of said first semiconductor chip and a top surface of said polymer layer is smaller than a thickness of said first metal bump, wherein said first semiconductor chip comprises a third metal bump on a first metal pad of said first semiconductor chip, wherein said third metal bump comprises a second tin-containing layer; and

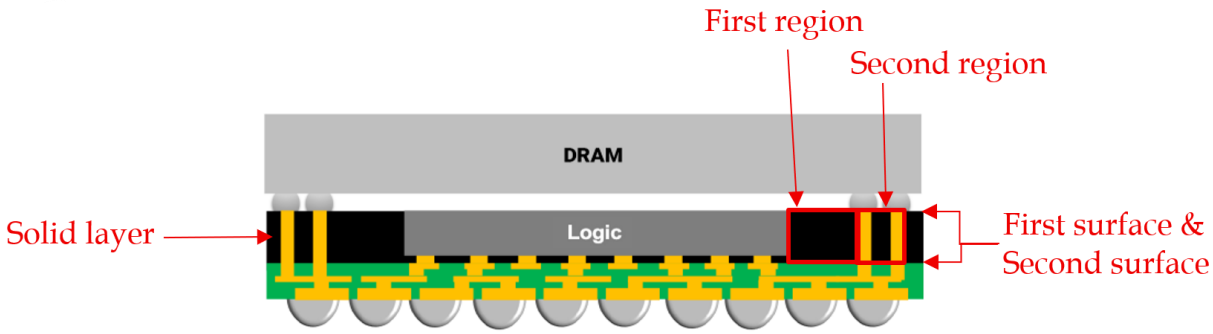
a second semiconductor chip over said first interconnection scheme, wherein said second semiconductor chip comprises a fourth metal bump on a second metal pad of said second semiconductor chip, wherein said fourth metal bump comprises a third tin-containing layer.

63. More particularly, Defendant infringes at least claim 10 of the ’306 Patent.

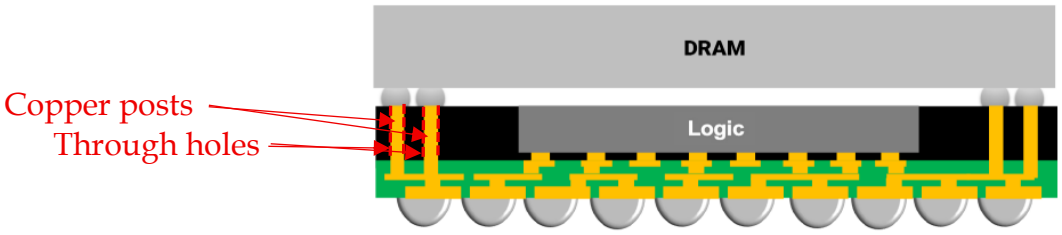
64. Each of the Accused Chips is a chip package.

65. Each of the Accused Chips has a solid layer having two surfaces that are opposite and substantially parallel to each other. This polymer layer has two regions (“a first region” and

"a second region" shown below) and is comprised of silicon and oxygen, with a thickness between 100 and 300 micrometers.

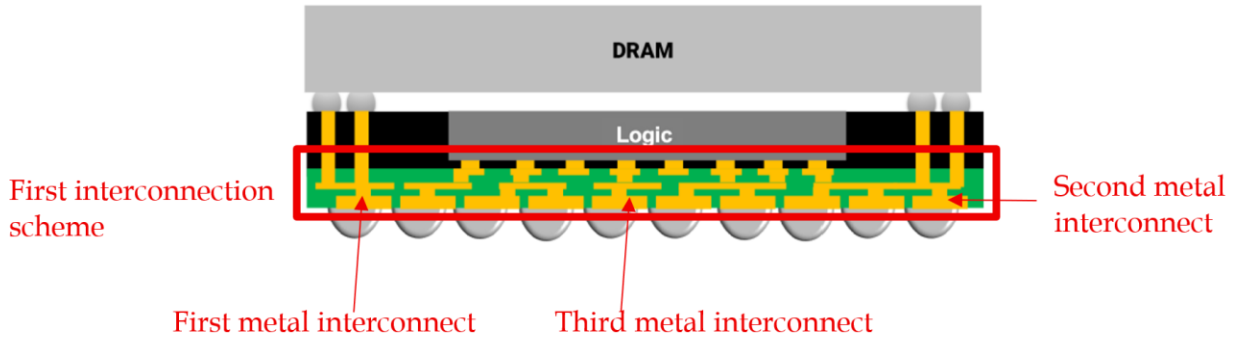


66. Each of the Accused Chips has multiple copper posts (shown below) and through holes (shown below) in the second region.



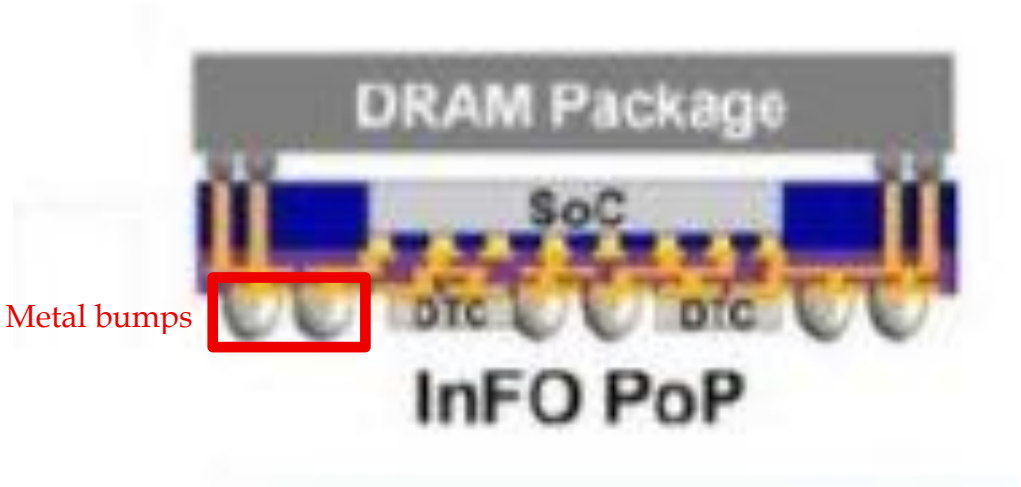
67. The first region has a width and a direction greater than a shortest distance between the sidewall of one of the through holes and the first edge in said direction, and greater than the pitch between two neighboring copper posts.

68. Each of the Accused Chips has an interconnection scheme ("first interconnection scheme" shown below) made up of metal interconnects ("first metal interconnect" and "second metal interconnect" shown below) over a first surface and a polymer layer (shown below in green) over the metal interconnect.

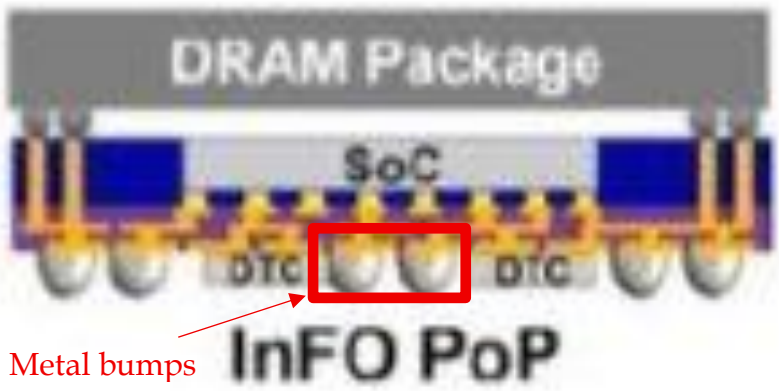


69. The metal interconnect is connected to one of the copper posts and is made up of a metal layer ("first metal layer") and a copper layer over the metal layer.

70. Each of the Accused Chips contains a metal bump ("first metal bump" shown below) over the interconnection scheme, where the metal bump comprises a tin-containing layer.



71. Each of the Accused Chips contains a metal bump ("second metal bump" shown below) over the interconnection scheme.

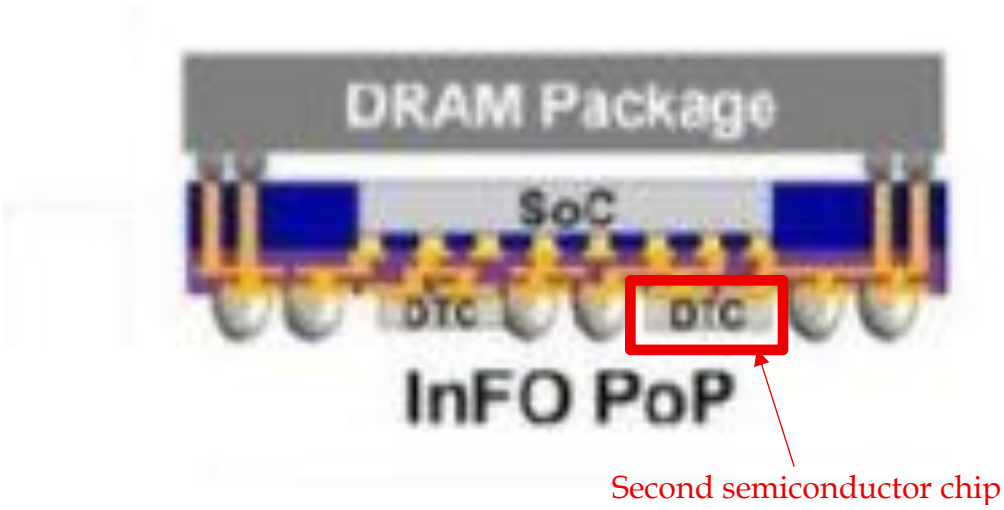


72. Each of the Accused Chips contains a semiconductor chip ("first semiconductor chip" shown below) over the interconnection scheme and between the first and second metal bumps.

73. The semiconductor chip has a height between a backside surface of the semiconductor chip and a top surface of the polymer layer is smaller than the thickness of the first metal bump,

74. The semiconductor chip comprises a third metal bump on a first metal pad of the semiconductor chip, wherein said third metal bump comprises a second tin-containing layer.

75. Each of the Accused Chips contains a second semiconductor chip ("second semiconductor chip" shown below) over the interconnection scheme.



76. The second semiconductor chip comprises a fourth metal bump on a second metal pad of the second semiconductor chip, wherein the fourth metal bump comprises a third tin-containing layer.

77. The Accused Apple Products infringe each of the claims 11-17 for the reasons similar to those stated above.

78. By making, using, importing, offering for sale and/or selling such products that are covered by one or more claims of the '306 patent, MYW Semitech has been damaged by the direct infringement of Apple and is suffering and will continue to suffer irreparable harm and damages as a result of this infringement.

JURY DEMANDED

Pursuant to Rule 38(b) of the Federal Rules of Civil Procedure, MYW Semitech hereby requests a trial by jury on all issues so triable.

PRAYER FOR RELIEF

WHEREFORE, MYW Semitech respectfully requests that the Court enter judgment in its favor and against Apple as follows:

a. finding that Apple directly infringes one or more claims of each of the Patents-in-Suit;

b. awarding MYW Semitech damages under 35 U.S.C. § 284, or otherwise permitted by law, including supplemental damages for any continued post-verdict infringement;

c. awarding MYW Semitech pre-judgment and post-judgment interest on the damages award and costs;

d. awarding cost of this action (including all disbursements) and attorney fees pursuant to 35 U.S.C. § 285, or as otherwise permitted by the law; and

e. awarding such other costs and further relief that the Court determines to be just and equitable.

Dated: July 7, 2025

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