IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

MYW SEMITECH, LLC, Plaintiff, v. APPLE INC., Defendant.	)))))))))	C.A. No. 25-504-RGA-EGT **JURY TRIAL DEMANDED**

DEFENDANT APPLE INC.'S
INITIAL INVALIDITY CONTENTIONS

Pursuant to Section 1(e) of the Court's Scheduling Order (Dkt. No. 26) and amendments thereto (Dkt. Nos. 29, 30, 31, 35, 57, and 58) (collectively, "the Scheduling Order") and the Delaware Default Standard For Discovery Rule 4.d, Defendant Apple Inc. ("Apple") hereby discloses its Initial Invalidity Contentions regarding U.S. Patent Nos. 11,107,768 ("the '768 Patent"), 11,538,763 ("the '763 Patent"), and 11,894,306 ("the '306 Patent") (collectively, the "Patents-in-Suit" or "Asserted Patents"). These Initial Invalidity Contentions are made only as to the claims of the Patents-in-Suit that Plaintiff MYW Semitech, LLC ("Semitech") identified in its Claim Narrowing, as modified on January 23, 2026, pursuant to Section 3(g)(ii) of the Scheduling Order: Claims 1, 2, 4, 5, 14, 16, 19, 20, 22, 25, and 28 of the '768 Patent (the "'768 Asserted Claims"), Claims 1, 2, 4, 5, 7, 9-14, and 17 of the '763 Patent (the "'763 Asserted Claims"), and Claims 10, 11, and 13-17 of the '306 Patent (the "'306 Asserted Claims") (collectively, the

"Asserted Claims"). Apple contends that each Asserted Claim is invalid under at least 35 U.S.C. §§ 101, 102, 103, and/or 112, for at least the reasons set forth herein.[1]

I. RESERVATION OF RIGHTS AND OBJECTIONS

A. General Reservation of Rights

These Initial Invalidity Contentions, along with the information and documents that Apple produces herewith, are provisional in nature and subject to further revision or supplementation. Apple reserves the right to amend these contentions should Semitech: (1) provide any information that it failed to properly provide in its January 9, 2026 Initial Infringement Contentions; (2) amend its Initial Infringement Contentions; (3) produce documents evidencing conception and reduction to practice that it failed to produce; or (4) attempt to rely upon any information during claim construction proceedings, at trial, in a hearing, or during a deposition that it failed to provide in its Initial Infringement Contentions or amendments thereto. Apple further reserves the right to amend these contentions in light of the Court's claim construction rulings or based on further discovery or Court rulings (or any other related reason).

B. Ongoing Investigation

Discovery in this case has just begun and is ongoing; and Apple's investigations are continuing. Apple expressly reserves the right to amend or supplement these disclosures based on additional information obtained through continued formal discovery or other means pursuant to Fed. R. Civ. P. 26(e) and/or, e.g., Fed R. Civ. P. 33, 34, 45. Apple is continuing to make a good

[1] While these Contentions refer to pre-AIA sections of 35 U.S.C. § 102, this should not be understood to be an admission that the Asserted Claims are entitled to claim priority to March 16, 2013 and, to the contrary, Apple expressly disputes whether the Asserted Claims are entitled to such priority. To the extent the Asserted Claims are subject to post-AIA 35 U.S.C. § 102, the same reasoning set forth herein applies, and the claims are also invalid under post-AIA 35 U.S.C. § 102(a).

MYW Semitech Exhibit 2017
TSMC and Apple v. MYW Semitech - IPR2026-00067

faith and diligent effort to search for and analyze relevant prior art and other information, some of which is in the possession of third parties, requires additional analysis or testing that takes time to perform, and/or is otherwise not readily accessible to Apple.[2]

Apple further reserves the right to revise, amend, or supplement the information provided herein, including by identifying, charting, and relying on additional information, references, systems, and devices, should Apple's further search and analysis yield such additional information, references, systems, or devices, consistent with the Scheduling Order, Delaware Default Standard For Discovery, and the Federal Rules of Civil Procedure. In addition, Apple reserves the right to supplement or amend the positions taken and information disclosed in these Initial Invalidity Contentions, including without limitation, the prior art and grounds of invalidity set forth herein under 35 U.S.C. §§ 101, 102, 103 or 112 (including with respect to indefiniteness, written description, and/or enablement), to consider information or defenses that may come to light because of Apple's discovery efforts; additional information obtained as to the priority date(s) of the Challenged Claims; testimony or documents produced by a party or non-party; and positions that Semitech might take or amend concerning infringement or invalidity issues. For example, Apple may seek further discovery from third parties believed to have, or capable of obtaining, knowledge, documentation, or corroborating evidence concerning items of prior art, including prior art listed in the Exhibits hereto. Such third parties may include, without limitation, the authors, inventors, assignees, owners, or developers of the references and technologies listed in these disclosures, and third party testing and analysis vendors. As another example, Semitech's infringement contentions and discovery responses remain deficient. Semitech first produced

[2] Unless otherwise specified, the term "prior art" refers to any patents, patent publications, other publications, products and/or systems identified in these Initial Invalidity Contentions and any amendments or supplements thereto.

MYW Semitech Exhibit 2017
TSMC and Apple v. MYW Semitech - IPR2026-00067

documents other than the public file histories for the Asserted Patents only four days before these Invalidity Contentions were due, and its document production remains substantially deficient. Semitech also has yet to provide fulsome responses to any of its interrogatories, including with respect to interrogatories relevant to the alleged validity and priority dates of the Asserted Patents. Indeed, on January 27, 2026, Apple asked Semitech to supplement its Interrogatory responses to provide a fulsome response to Apple's Interrogatory asking Semitech for its position regarding the alleged priority date of each of the Asserted Claims, including by identifying support for its contention regarding priority dates. Semitech declined to provide any response to this request on January 29, 2026. Prior to service of these Contentions, Semitech did not provide any supplemental Interrogatory responses or provide any further clarification of its positions regarding the alleged priority dates for the Asserted Claims. Apple has prepared these Contentions based upon Semitech's existing position regarding alleged priority date, including both its identification of September 26, 2012 as the alleged priority date for all Asserted Claims and its refusal to identify any basis for that contention, or any alternative priority dates to which the Asserted Claims are allegedly entitled to claim priority. To the extent Semitech later identifies any other alleged priority date for the Asserted Claims or any basis for its current or future allegations, Apple reserves the right to supplement and/or amend its Invalidity Contentions, including by identifying new, alternative, and/or additional prior art grounds.

Semitech's infringement contentions are also deficient because they do not present a coherent and complete infringement theory for any claim. Apple reserves the right to supplement its Invalidity Contentions to present additional theories of invalidity under 35 U.S.C. §§ 101, 102, 103 or 112 (including with respect to indefiniteness, written description, and/or enablement), if and when Semitech belatedly supplements its discovery responses and infringement contentions

MYW Semitech Exhibit 2017
TSMC and Apple v. MYW Semitech - IPR2026-00067

in this matter in order to account for new invalidity positions that may arise in view of positions taken by Semitech. Moreover, Apple reserves the right to assert invalidity under 35 U.S.C. §§ 101, 102, 103 or 112 (including with respect to indefiniteness, written description, and/or enablement) for reasons in addition to the reasons set forth in these Contentions to the extent that discovery or further investigation yields information forming the basis for such grounds for invalidity.

Apple further reserves the right to rely upon prior art cited in the file histories of the Asserted Patents and related U.S. and foreign patent applications as invalidating references or to show the state of the art. Apple further reserves the right to rely upon additional prior art to show the state of the art, including a POSITA's understanding of the same. Apple further intends to rely on inventor admissions concerning the scope of the prior art relevant to the Asserted Patents found in, *inter alia*: the patent prosecution history for the Asserted Patents and any related patents or patent applications; any deposition testimony of the named inventor on the Asserted Patents; and the papers filed and any evidence submitted by Semitech and/or third parties in connection with this litigation. Apple hereby incorporates by reference the relevant testimony of any fact witnesses who are deposed, provide declarations, or otherwise testify in this lawsuit. Apple also hereby incorporates by reference the reports and testimony of Apple's expert witnesses regarding invalidity of the Asserted Patents.

C. Claim Construction

Claim construction is ongoing in this action, briefing is not yet complete, and the Court has yet to hold a *Markman* hearing. Accordingly, Apple reserves the right to modify, amend, or supplement its Initial Invalidity Contentions in accordance with claim construction rulings from this Court, claim construction positions taken by Semitech, or to the extent permitted by this Court. Apple also reserves the right to modify, amend or supplement its Initial Invalidity Contentions

MYW Semitech Exhibit 2017
TSMC and Apple v. MYW Semitech - IPR2026-00067

upon Semitech's modification of its asserted claim constructions, including as adopted by Semitech in its Initial Infringement Contentions and amendments thereto.

Apple's Initial Invalidity Contentions do not represent its agreement or view as to the meaning of any claim term contained therein. By including prior art that anticipates or renders obvious claims based on constructions of claim terms apparently applied by Semitech to the Asserted Claims, Apple's Initial Invalidity Contentions are not—and should not be interpreted as—adoptions or admissions as to the accuracy of any such construction. To the contrary, Apple offers these contentions in response to and under Semitech's apparent interpretation of the Asserted Claims and Semitech's Initial Infringement Contentions, which remain insufficient under the Patent Rules, as explained in Apple's correspondence to Semitech. Nothing in Apple's Initial Invalidity Contentions should be deemed to be an admission regarding the scope of any claims or the proper construction of those claims or any terms contained therein. Nor should anything contained herein be understood or deemed to be an express or implied admission or contention regarding the proper construction of any terms in any Asserted Claim, or regarding the alleged infringement of that claim.

Unless otherwise stated herein, Apple takes no position on any matter of claim construction in these Initial Invalidity Contentions. Apple reserves the right to propose any claim construction it considers appropriate and to contest any claim construction it considers inappropriate. Apple reserves the right to further supplement or modify the positions and information in these Initial Invalidity Contentions, including without limitation, the prior art and grounds of invalidity set forth herein, after the Asserted Claims have been construed, in accordance with the Scheduling Order, Delaware Default Standard For Discovery, or any of the Court's Orders. Apple also reserves the right to argue that certain additional claim terms, phrases, and elements are indefinite, lack

MYW Semitech Exhibit 2017
TSMC and Apple v. MYW Semitech - IPR2026-00067

written description, are not patentable, are not novel or are otherwise invalid under 35 U.S.C. §§ 101 or 112.

II. PRIORITY DATE OF THE ASSERTED CLAIMS

Semitech has taken the position that "Mr. Ping-Jung Yang is the sole inventor of the Patents-in-Suit. Mr. Ping-Jung Yang conceived, reduced to practice, and developed the technology of the Patents-in-Suit as of the filing date of U.S. provisional patent application No. 61/705,649, which was filed September 26, 2012." Semitech's October 2, 2025 Response to Interrogatory No. 1. Semitech has not presented any evidence showing entitlement to claim priority to either this provisional application, or even to U.S. Patent No. 9,615,453 ("'453 Patent"), for which the Asserted Patents are continuations in part. *See PowerOasis, Inc. v. T-Mobile USA, Inc.*, 522 F.3d 1299, 1305–06 (Fed. Cir. 2008) (affirming finding that patentee did not show entitlement to priority before continuation-in-part was filed, holding that "[t]he district court therefore correctly placed the burden on PowerOasis to come forward with evidence to prove entitlement to claim priority to an earlier filing date.").

The Asserted Claims are not entitled to an earlier filing date for at least two reasons. First, Semitech has adduced no evidence establishing that the Asserted Claims are entitled to any earlier priority date than the actual filing of the applications that ultimately issued as the Asserted Patents themselves in which those Asserted Claims appear. Second, as further discussed in Section IV below, the Asserted Patents each lack sufficient written description and enablement support.

In addition, '768 Patent claims 1, 2, 4, 5, 14, and 20 are also not entitled to claim priority to the September 26, 2012 provisional because there was no written description support for the limitation reciting a "coefficient of expansion between 3 and 10 ppm/ºC" in that provisional application. Indeed, the Applicant admitted as much during prosecution of the '768 Patent. *See* '768 File History at 598 (APL-SEMITECH_00531986 at 2583) ("The condition/item of the

MYW Semitech Exhibit 2017
TSMC and Apple v. MYW Semitech - IPR2026-00067

'coefficient of expansion between 3 and 10 ppm/°C' in claims 21 and 35 is disclosed in the Non-Provisional patent application of application No. 14/036256, filed Sept. 25, 2013, not disclosed in the provisional patent application No. 61/705,649, filed Sept. 26, 2012. The applicant apologizes for this error.").

III. PRIOR ART INVALIDITY UNDER 35 U.S.C. §§ 102/103

Each of the Asserted Patents is invalid under pre- and post-AIA 35 U.S.C. §§ 102 and 103 as anticipated by and/or obvious in view of several different prior art references and combinations thereof. Apple identifies and hereby incorporates by reference, as if set forth fully herein, the complete prosecution histories for the Asserted Patents and related patents, including the prior art and supporting documents cited in those prosecution histories. Apple may cite or rely upon the prosecution histories, the examiner's findings, and the prior art cited therein to support or provide context for these Initial Invalidity Contentions. Apple also incorporates by reference, as if set forth fully herein, all filings, the prior art references identified as anticipating or rendering obvious the Asserted Claims, and supporting expert declarations in any Patent Office filing or proceeding challenging the validity of the Asserted Patent in the U.S. or anywhere in the world ("Other Proceedings"), including at least *Taiwan Semiconductor Manufacturing Co., Ltd. et al. v. MYW Semitech, LLC*, IPR2026-00065 (P.T.A.B. filed Nov. 21, 2025); *Taiwan Semiconductor Manufacturing Co., Ltd. et al. v. MYW Semitech, LLC*, IPR2026-00066 (P.T.A.B. filed Nov. 21, 2025); *Taiwan Semiconductor Manufacturing Co., Ltd. et al. v. MYW Semitech, LLC*, IPR2026-00067 (P.T.A.B. filed Nov. 21, 2025) (APL-SEMITECH_00531729-APL-SEMITECH_00545175). Such references may be from any prior or future reissue, reexamination, or *inter partes* review of the Asserted Patents. Further, Apple incorporates by reference, as if originally set forth herein, all filings made in such proceedings, including prior art references identified and analyzed therein, prior art analysis, claim charts and motivations to combine

MYW Semitech Exhibit 2017
TSMC and Apple v. MYW Semitech - IPR2026-00067

presented therein, and supporting expert declarations submitted therewith. Apple also incorporates by reference, as if set forth fully herein, all prior art cited during the prosecution. Apple further relies on and incorporates by reference, as if originally set forth herein, all invalidity positions, and all associated prior art, claim charts and motivations to combine, disclosed to Semitech by present or former defendants in any lawsuits or other proceedings, or by potential or actual licensees to any of the Asserted Claims. This includes Exhibits A1-A10 for the '768 Patent, Exhibits B1-B10 for the '763 Patent, and Exhibits C1-C8 for the '306 Patent (including as referenced in the next section relating to motivations to combine), and Exhibits S1-S5. In addition to these references, Apple also identifies the prior art references set forth in Exhibit D to these Invalidity Contentions. Each of the prior art references identified in this paragraph provides additional support for the understanding of a person of ordinary skill in the art ("POSITA") as of the alleged priority date for each of the Asserted Claims of the Asserted Patents. Apple reserves the right to rely on these references as evidence of the same.

Apple reserves the right to use any portion of the patent(s), publication(s), related publications, commercial embodiments of the publication(s), test results, third party analyses, teardowns, and other evidence discovered in this litigation to demonstrate or evidence the components, functionality, and capabilities of the devices and systems disclosed in the references charted. Where Apple identifies a particular figure in a prior art reference, the identification should be understood to encompass the caption and description of the figure and any text relating to the figure in addition to the figure itself. Similarly, where an identified portion of text refers to a figure or other material, the identification should be understood to include the referenced figure or other material as well.

MYW Semitech Exhibit 2017
TSMC and Apple v. MYW Semitech - IPR2026-00067

A POSITA would generally read a prior art reference as a whole and in the context of other publications, literature, and general knowledge in the field. To understand and interpret any specific statement or disclosure in a prior art reference, a POSITA would rely upon other information including other publications and general scientific or engineering knowledge. Apple therefore reserves the right to rely upon other unidentified portions of the prior art references and on other publications and expert testimony to provide context and to aid understanding and interpretation of the identified portions. Identified portions are exemplary only. Apple also reserves the right to rely upon other portions of the prior art references, other publications, and the testimony of experts to establish that the alleged inventions would have been obvious to a POSITA, including the basis of modifying or combining certain cited references.

To the extent any limitation of an Asserted Claim is deemed not to be exactly disclosed by an item of prior art, then any purported differences are such that the claimed subject matter as a whole would have been obvious to one skilled in the art at the time of the alleged invention, in view of the state of the art and knowledge of those skilled in the art. Numerous prior art references, including those identified by Apple herein, reflect common knowledge and the state, scope and content of the prior art before the priority dates of the Asserted Patents. *See Graham v. John Deere Co.,* 383 U.S. 1, 35-36 (1966).

Furthermore, to the extent any limitation of an Asserted Claim is deemed to not be exactly disclosed by an item of prior art, then the claim is rendered obvious by combination of the prior art item with one or more other items of prior art as set forth below.

Though these claim charts provide illustrative citations to where each element may be found in the prior art references or in their combination, the cited references may contain other disclosures of each claim element as well, and Apple reserves the right to argue any claim elements

MYW Semitech Exhibit 2017
TSMC and Apple v. MYW Semitech - IPR2026-00067

of the Challenged Claims of the Asserted Patents are disclosed in non-cited portions of these references. For at least the reasons described above and below in the examples provided as well as in the claim charts appended hereto, it would have been obvious to one of ordinary skill in the art to combine any of a number of prior art references.

A. Identification of Prior Art Grounds Per Asserted Claim

Pursuant to paragraph 3(g)(ii) of the Scheduling Order, Apple identifies the following prior art grounds under 35 U.S.C. §§ 102/103 per asserted claim:

	Ground	Yu '763 (US9123763) in view of Lin '191 (US20100290191)	Yu '763 in view of Lin '191 and Haba '993 (US8709933)	Yu '763 in view of Lin '191 and Lin '863 (US9679863)	Haba '993 in view of Lin '191	X-GOLD in view of Lin '191	Snapdragon	Snapdragon in view of Lin '191	Snapdragon in view of Ahn '785 (US7888785)	Snapdragon in view of Ahn '785 and Lin '191	OMAP 3 in view of Lin '191	OMAP 4 in view of Lin '191	OMAP 4 in view of Lin '191 and Yoshida '753 (US8623753)	Apple A5	Apple A5 in view of Lin '191	Apple A5 in view of Ahn '785	Apple A5 in view of Lin '191 and Ahn '785
768	**1**				X	X	X	X			X	X		X	X		
	2				X		X		X	X			X	X		X	X
	4				X		X		X	X			X	X		X	X
	5				X	X	X	X			X	X		X	X		
	14				X	X	X	X			X	X		X	X		
	16	X					X		X	X			X	X		X	X
	19	X					X		X	X			X	X		X	X
	20		X				X		X	X			X	X		X	X
	22	X					X		X	X			X	X		X	X
	25	X					X		X	X			X	X		X	X
	28	X					X		X	X			X	X		X	X
763	**1**	X				X	X	X			X	X		X	X		
	2	X					X		X	X			X	X		X	X
	4	X					X		X	X			X	X		X	X
	5	X				X	X	X			X	X		X	X		

	7	X				X	X	X			X	X		X	X		
	9	X				X	X	X			X	X		X	X		
	10	X				X	X	X			X	X		X	X		
	11	X				X	X	X			X	X		X	X		
	12	X				X	X	X			X	X		X	X		
	13			X		X	X	X			X	X		X	X		
	14	X					X		X	X			X	X		X	X
	17	X				X	X	X			X	X		X	X		
306	**10**	X					X		X	X			X	X		X	X
	11	X					X		X	X			X	X		X	X
	13	X					X		X	X			X	X		X	X
	14	X					X		X	X			X	X		X	X
	15	X					X		X	X			X	X		X	X
	16	X					X		X	X			X	X		X	X
	17	X					X		X	X			X	X		X	X

As set forth below and in Section III.B below, each of the references identified in the above table constitutes prior art to each of the Asserted Claims.

- **U.S. Patent No. 9,123,763 ("Yu '763"):** Yu '763 was filed October 12, 2011, and issued September 1, 2015. It is therefore prior art under at least pre-AIA 35 U.S.C. § 102(e).
- **U.S. Patent Pub. No. 2010/0290191 ("Lin '191"):** Lin '191 was filed May 13, 2010, and published November 18, 2010. It is therefore prior art under at least pre-AIA 35 U.S.C. § 102(b).
- **U.S. Patent No. 8,709,933 ("Haba '933"):** Haba '933 was filed April 21, 2011, and issued May 29, 2014. It is therefore prior art under at least pre-AIA 35 U.S.C. § 102(e).
- **U.S. Patent No. 7,888,785 ("Ahn '785"):** Ahn '785 was filed July 18, 2008, and issued February 15, 2011. It is therefore prior art under at least pre-AIA 35 U.S.C. § 102(a) and/or (b). In addition, prior to issuance, Ahn '785 was published as U.S. Patent Pub. No. 2009/0065920 on March 12, 2009. While these Contentions cite to the issued

MYW Semitech Exhibit 2017
TSMC and Apple v. MYW Semitech - IPR2026-00067

patent version of Ahn ’785, to the extent there is any dispute about whether Ahn ’785 constitutes prior art, Ahn ’785’s patent publication also constitutes prior art under at least 35 U.S.C. § 102(b). Citations in this declaration to disclosures in Ahn ’785 should be understood to also refer to the corresponding disclosures in U.S. Patent Pub. No. 2009/0065920.

- **U.S. Patent No. 8,623,753 (“Yoshida ’753”):** Yoshida ’753 was filed April 28, 2009, and issued January 7, 2014. It is therefore prior art under at least pre-AIA 35 U.S.C. § 102(e).

The following exhibits comprise claim charts that set forth exemplary disclosures from each of the references identified in the grounds above that demonstrate that each limitation of each of the Asserted Claims is disclosed by and/or obvious in view of the prior art:

- **’768 Patent (Exhibit A):**
    1. Exhibit A1: Yu ’763
    2. Exhibit A2: Lin ’191
    3. Exhibit A3: Haba ’933
    4. Exhibit A4: Ahn ’785
    5. Exhibit A5: Yoshida ’753
    6. Exhibit A6: X-GOLD
    7. Exhibit A7: Snapdragon
    8. Exhibit A8: OMAP 3
    9. Exhibit A9: OMAP 4
    10. Exhibit A10: Apple A5

MYW Semitech Exhibit 2017
TSMC and Apple v. MYW Semitech - IPR2026-00067

- **’763 Patent (Exhibit B):**
    1. Exhibit B1: Yu ’763
    2. Exhibit B2: Lin ’191
    3. Exhibit B3: Lin ’863
    4. Exhibit B4: Ahn ’785
    5. Exhibit B5: Yoshida ’753
    6. Exhibit B6: X-GOLD
    7. Exhibit B7: Snapdragon
    8. Exhibit B8: OMAP 3
    9. Exhibit B9: OMAP 4
    10. Exhibit B10: Apple A5
- **’306 Patent (Exhibit C):**
    1. Exhibit C1: Yu ’763
    2. Exhibit C2: Lin ’191
    3. Exhibit C3: Lin ’863
    4. Exhibit C4: Ahn ’785
    5. Exhibit C5: Yoshida ’753
    6. Exhibit C6: Snapdragon
    7. Exhibit C7: OMAP 4
    8. Exhibit C8: Apple A5

In addition to the above prior art charts in Exhibits A to C, with respect to the system prior art references, as explained in greater detail below, the following exhibits set forth slides presenting

MYW Semitech Exhibit 2017
TSMC and Apple v. MYW Semitech - IPR2026-00067

exemplary mappings setting forth how the evidence relating to each system discloses and renders obvious the Asserted Claims:

- **System Art Summaries (Exhibit S):**
    1. Exhibit S1: X-GOLD
    2. Exhibit S2: Snapdragon
    3. Exhibit S3: OMAP 3
    4. Exhibit S4: OMAP 4
    5. Exhibit S5: Apple A5

Finally, in addition to the above exhibits, Exhibits A to C further include Exhibits A0, B0, and C0 identifying exemplary teachings from the prior art demonstrating how each limitation of the ’768, ’763, and ’306 Patents, respectively, was well understood and conventional in the art.

B. Prior Art Products

As set forth in Section III.A, Apple contends that the Asserted Claims are invalid as anticipated and/or obvious in view of references and combinations of references that include public knowledge and uses and/or offers for sale of products and services under 35 U.S.C. §§ 102(a) and/or (b) (“Product References”).

In addition to the claim charts set forth in Exhibits A1-A10 for the ’768 Patent, Exhibits B1-B10 for the ’763 Patent, and Exhibits C1-C8 for the ’306 Patent, Exhibits S1 through S5 set forth exemplary mappings of each Product Reference. The mappings set forth in each of these exhibits are representative only and not limiting. For example, the exemplary mappings for each of these system art references can be modified by, e.g., applying teachings of other references as identified in Section III.A, or identifying or changing the identification portions of the references identified as disclosing each limitation by modifying the exemplary mappings by, e.g., :

MYW Semitech Exhibit 2017
TSMC and Apple v. MYW Semitech - IPR2026-00067

1. The “first polymer layer” or “solid layer” is a different polymer or solid layer, such as a layer containing, below, or above, the processor die, and/or one or more polymer or solid layers in which there are metal interconnects above or below a processor or a memory die;
2. The material for the “first polymer layer” is substituted for a material with a coefficient of expansion between 3 and 10 ppm/ºC and/or a material with a thickness between 100 and 300 micrometers as taught by, e.g., Lin ’191;
3. The “first metal plug” and/or “second metal plug” are different solder balls on either side of the processor die;
4. The direction identified as “over” in the Asserted Claims is inverted;
5. The “interconnection scheme” is part or all of the set of metal connections below, around, or above the processor package, including some or all of the connections including the connections to the memory package;
6. Within the “interconnection scheme,” other metal plugs are identified as the “first metal plug” and “second metal plug”;
7. Within a “metal bump” or “metal interconnect,” applying additional teachings of layers used in those metal bumps, and the thicknesses of the metals used in those bumps or interconnects, as taught by, e.g., Lin ’191;
8. Identifying different metal plugs as, e.g., the “first” or “second” “metal plugs”;
9. Applying additional teachings of adding chips above or below interconnection schemes in a chip package, including CPUs, GPUs, memories, and/or other types of chips, as taught by, e.g., Yoshida ’753 and Ahn ’785;

MYW Semitech Exhibit 2017
TSMC and Apple v. MYW Semitech - IPR2026-00067

10. Applying additional teachings of adding passive devices above or below interconnection schemes in a chip package, including capacitors, resistors, inductors, and/or other types of passive devices, as taught by, e.g., Yoshida '753 and Ahn '785;

11. Adjusting the separation between the "first" and "second" regions in a "solid layer" to, e.g., encompass additional copper or metal plugs; and

12. Including additional copper plugs within a "second" region as taught by, e.g., Lin '191.

1. Snapdragon

The Qualcomm MSM7230 Snapdragon Processor ("Snapdragon") processor was first announced in 2009, was included in products that were sold or offered for sale as early as late 2010, and therefore qualifies as prior art to all Asserted Claims, including at least under pre-AIA 35 U.S.C. § 102(b). *See, e.g.*, APL-SEMITECH_00528637-APL-SEMITECH_00528643; APL-SEMITECH_00528627-APL-SEMITECH_00528629; APL-SEMITECH_00528625-APL-SEMITECH_00528626; APL-SEMITECH_00528614-APL-SEMITECH_00528624. Snapdragon implemented TMV-PoP technology, which was a technology that was developed at least in part by Amkor. *See, e.g.*, APL-SEMITECH_00552656-APL-SEMITECH_00552785, "Snapdragon Structural Analysis") at APL-SEMITECH_00552672; APL-SEMITECH_00528612-APL-SEMITECH_00528613; APL-SEMITECH_00528579-APL-SEMITECH_00528581. Snapdragon also used a memory module implemented by Samsung. Snapdragon Structural Analysis, APL-SEMITECH_00552656 at 2667, 2669.

Exhibits A7, B7, and C6 show how Snapdragon discloses and renders obvious the Asserted Claims. For example, based on the evidence in Exhibits A7, B7, and C6, Exhibit S2 depicts an exemplary reading demonstrating how Snapdragon discloses and renders obvious each of the

MYW Semitech Exhibit 2017
TSMC and Apple v. MYW Semitech - IPR2026-00067

Asserted Claims of the Asserted Patents. The mapping in this Exhibit is non-limiting. Applying the evidence in Exhibits A7, B7, C6 and S2, alone and/or in combination with the teachings of other references and/or the understandings of a POSITA as set forth in Exhibits A-C, other mappings are also possible, and the evidence set forth in those Exhibits shows how all Asserted Claims are anticipated and/or obvious in view of Snapdragon alone and/or in combination with other prior art references as forth in Sections III.A and III.C.

Documents comprising descriptions of Snapdragon that Apple has identified to date include the following: APL-SEMITECH_00552656-APL-SEMITECH_00552785, "Snapdragon Structural Analysis"); APL-SEMITECH_00528637-APL-SEMITECH_00528643; APL-SEMITECH_00528627-APL-SEMITECH_00528629; APL-SEMITECH_00528625-APL-SEMITECH_00528626; APL-SEMITECH_00528614-APL-SEMITECH_00528624; APL-SEMITECH_00528612-APL-SEMITECH_00528613; APL-SEMITECH_00528647-APL-SEMITECH_00528703; APL-SEMITECH_00528579-APL-SEMITECH_00528581. These documents are not limiting; Apple reserves the right to rely on additional documents and/or information describing Snapdragon, including but not limited to additional articles, technical documentation, technical analyses, publications, or other descriptions of Snapdragon. Apple also reserves the right to rely on a physical Snapdragon at trial.

To the extent that there is any dispute that the disclosures identified above and/or set forth in Exhibits A7, B7, C6, or S2 describe Snapdragon, a POSITA would have found it obvious and would have been motivated to apply the teachings from those disclosures to Snapdragon. For example, those disclosures describe related aspects of the same or similar technologies, and describe products and technologies used by the same companies. A POSITA therefore would have been motivated to look to these teachings for additional details of how to implement a chip package

MYW Semitech Exhibit 2017
TSMC and Apple v. MYW Semitech - IPR2026-00067

structure similar to the structure appearing in products implementing Snapdragon. And to the extent applying those teachings would have required modifying a product implementing Snapdragon, a POSITA further would have been motivated to modify that product's architecture for the same reasons, as well as because those teachings provide additional straightforward and obvious modifications that provide additional advantages for, e.g., performance, interoperability, space, thermal performance, efficiency, and/or speed. Additionally, applying those additional teachings for their intended purposes would have been a straightforward modification of Snapdragon. A POSITA therefore would have had a reasonable expectation of success applying those additional teachings to Snapdragon.

2. Texas Instruments OMAP 4

The Texas Instruments OMAP 4 series processor, including the representative OMAP 4430 ("OMAP 4"), was a Texas Instruments chip that was announced and publicly offered for sale in the United States at least as early as April 2011. *See, e.g.*, APL-SEMITECH_00530710-APL-SEMITECH_00530717 (https://web.archive.org/web/20110710030224/https://www.cnx-software.com/2011/04/06/phytec-texas-instruments-omap4430-computer-module/). For example, the chip was included in multiple products publicly offered for sale including, e.g., Phytec PhyCORE-OMAP 4, the Blackberry Playbook, the Nook, and other products. *See, e.g.*, *id.*; APL-SEMITECH_00528572-APL-SEMITECH_00528573 (https://www.arteris.com/blog/blackberry-playbook-tablet-has-omap4430-ti-confirms-at-ces/). It therefore qualifies as prior art to all Asserted Claims, including at least under pre-AIA 35 U.S.C. § 102(b).

Exhibits A9, B9, and C7 show how OMAP 4 discloses and renders obvious the Asserted Claims. For example, based on the evidence in Exhibits A9, B9, and C7, Exhibit S4 depicts an exemplary reading demonstrating how OMAP 4 discloses and renders obvious each of the Asserted Claims of the Asserted Patents. The mapping in this Exhibit is non-limiting. Applying

MYW Semitech Exhibit 2017
TSMC and Apple v. MYW Semitech - IPR2026-00067

the evidence in Exhibits A9, B9, C7 and S4, alone and/or in combination with the teachings of other references and/or the understandings of a POSITA as set forth in Exhibits A-C, other mappings are also possible, and the evidence set forth in those Exhibits shows how all Asserted Claims are anticipated and/or obvious in view of OMAP 4 alone and/or in combination with other prior art references as forth in Sections III.A and III.C.

Documents comprising descriptions of OMAP 4 that Apple has identified to date include the following: APL-SEMITECH_00552643-APL-SEMITECH_00552654; APL-SEMITECH_00531718-APL-SEMITECH_00531727; APL-SEMITECH_00529710-APL-SEMITECH_00530709; APL-SEMITECH_00530710-APL-SEMITECH_00530717; APL-SEMITECH_00528572-APL-SEMITECH_00528573. These documents are not limiting; Apple reserves the right to rely on additional documents and/or information describing OMAP 4, including but not limited to additional articles, technical documentation, technical analyses, publications, or other descriptions of OMAP 4. Apple also reserves the right to rely on a physical OMAP 4 at trial.

To the extent that there is any dispute that the disclosures set forth above and in Exhibits A9, B9, C7, and S4 describe OMAP 4, a POSITA would have found it obvious and would have been motivated to apply the teachings from those disclosures to OMAP 4. For example, those disclosures describe related aspects of the same or similar technologies, and describe products and technologies used by the same companies. A POSITA therefore would have been motivated to look to these teachings for additional details of how to implement a chip package structure similar to the structure appearing in products implementing OMAP 4. And to the extent applying those teachings would have required modifying a product implementing OMAP 4, a POSITA further would have been motivated to modify that product's architecture for the same reasons, as well as

MYW Semitech Exhibit 2017
TSMC and Apple v. MYW Semitech - IPR2026-00067

because those teachings provide additional straightforward and obvious modifications that provide additional advantages for, e.g., performance, interoperability, space, thermal performance, efficiency, and/or speed. Additionally, applying those additional teachings for their intended purposes would have been a straightforward modification of OMAP 4. A POSITA therefore would have had a reasonable expectation of success applying those additional teachings to OMAP 4.

3. Texas Instruments OMAP 3

The Texas Instruments OMAP 3 series processor, including the representative OMAP 3630 ("OMAP 3"), was a Texas Instruments chip that was announced and publicly offered for sale in the United States at least as early as 2009. *See, e.g.*, APL-SEMITECH_00528704-APL-SEMITECH_00528709; APL-SEMITECH_00528710-APL-SEMITECH_00529709. For example, the chip was included in multiple products publicly offered for sale including, e.g., the Nokia N900, Motorola XT810, and Motorola XT701. *See, e.g.*, APL-SEMITECH_00528586-APL-SEMITECH_00528587; APL-SEMITECH_00528584-APL-SEMITECH_00528585; APL-SEMITECH_00528582-APL-SEMITECH_00528583. It therefore qualifies as prior art to all Asserted Claims, including at least under pre-AIA 35 U.S.C. § 102(b).

Exhibits A8 and B8 show how OMAP 3 discloses and renders obvious Asserted Claims. For example, based on the evidence in Exhibits A8 and B8, Exhibit S3 depicts an exemplary reading demonstrating how OMAP 3 discloses and renders obvious Asserted Claims of the '763 and '768 Asserted Patents. The mapping in this Exhibit is non-limiting. Applying the evidence in Exhibits A-B, alone and/or in combination with the teachings of other references and/or the understandings of a POSITA as set forth in Exhibits A-B, other mappings are also possible, and the evidence set forth in those Exhibits shows how Asserted Claims of the '763 and '768 Asserted Patents are anticipated and/or obvious in view of OMAP 3 alone and/or in combination with other prior art references as forth in Sections III.A and III.C.

MYW Semitech Exhibit 2017
TSMC and Apple v. MYW Semitech - IPR2026-00067

Documents comprising descriptions of OMAP 3 that Apple has identified to date include the following: APL-SEMITECH_00552787-APL-SEMITECH_00552816); APL-SEMITECH_00528710-APL-SEMITECH_00529709); APL-SEMITECH_00528704-APL-SEMITECH_00528709; APL-SEMITECH_00528586-APL-SEMITECH_00528587; APL-SEMITECH_00528584-APL-SEMITECH_00528585; APL-SEMITECH_00528582-APL-SEMITECH_00528583. These documents are not limiting; Apple reserves the right to rely on additional documents and/or information describing OMAP 3, including but not limited to additional articles, technical documentation, technical analyses, publications, or other descriptions of OMAP 3. Apple also reserves the right to rely on a physical OMAP 3 at trial.

To the extent that there is any dispute that the disclosures set forth above and in Exhibits A8, B8, and S3 describe OMAP 3, a POSITA would have found it obvious and would have been motivated to apply the teachings from those disclosures to OMAP 3. For example, those disclosures describe related aspects of the same or similar technologies, and describe products and technologies used by the same companies. A POSITA therefore would have been motivated to look to these teachings for additional details of how to implement a chip package structure similar to the structure appearing in products implementing OMAP 3. And to the extent applying those teachings would have required modifying a product implementing OMAP 3, a POSITA further would have been motivated to modify that product's architecture for the same reasons, as well as because those teachings provide additional straightforward and obvious modifications that provide additional advantages for, e.g., performance, interoperability, space, thermal performance, efficiency, and/or speed. Additionally, applying those additional teachings for their intended purposes would have been a straightforward modification of OMAP 3. A POSITA therefore would have had a reasonable expectation of success applying those additional teachings to OMAP 3.

4. X-GOLD

MYW Semitech Exhibit 2017
TSMC and Apple v. MYW Semitech - IPR2026-00067

The Infineon X-GOLD processor, including the representative X-GOLD 618 ("X-GOLD"), was an Infineon Technologies chip that was announced and publicly offered for sale in the United States at least as early as 2009. *See, e.g.*, APL-SEMITECH_00553890-APL-SEMITECH_00553891; APL-SEMITECH_00528574-APL-SEMITECH_00528575. For example, the chip was included in multiple products publicly offered for sale including, e.g., the iPhone 4 released in June 2010 and other products. *See, e.g.*, APL-SEMITECH_00528644-APL-SEMITECH_00528646; APL-SEMITECH_00528553-APL-SEMITECH_00528557. It therefore qualifies as prior art to all Asserted Claims, including at least under pre-AIA 35 U.S.C. § 102(b).

Exhibits A6 and B6 show how X-GOLD discloses and renders obvious Asserted Claims. For example, based on the evidence in Exhibits A6 and B6, Exhibit S1 depicts an exemplary reading demonstrating how X-GOLD discloses and renders obvious Asserted Claims of the of the '763 and '768 Asserted Patents. The mapping in this Exhibit is non-limiting. Applying the evidence in Exhibits A6, B6 and S1, alone and/or in combination with the teachings of other references and/or the understandings of a POSITA as set forth in Exhibits A-B, other mappings are also possible, and the evidence set forth in those Exhibits shows how Asserted Claims are anticipated and/or obvious in view of X-GOLD alone and/or in combination with other prior art references as forth in Sections III.A and III.C.

Documents comprising descriptions of X-GOLD that Apple has identified to date include the following: APL-SEMITECH_00528588-APL-SEMITECH_00528611); APL-SEMITECH_00528574-APL-SEMITECH_00528575; APL-SEMITECH_00552924-APL-SEMITECH_00552930); APL-SEMITECH_00528644-APL-SEMITECH_00528646; APL-SEMITECH_00528553-APL-SEMITECH_00528557. These documents are not limiting; Apple reserves the right to rely on additional documents and/or information describing X-GOLD,

MYW Semitech Exhibit 2017
TSMC and Apple v. MYW Semitech - IPR2026-00067

including but not limited to additional articles, technical documentation, technical analyses, publications, or other descriptions of X-GOLD. Apple also reserves the right to rely on a physical X-GOLD at trial.

To the extent that there is any dispute that the disclosures set forth above and in Exhibits A6, B6, and S1 describe X-GOLD, a POSITA would have found it obvious and would have been motivated to apply the teachings from those disclosures to X-GOLD. For example, those disclosures describe related aspects of the same or similar technologies, and describe products and technologies used by the same companies. A POSITA therefore would have been motivated to look to these teachings for additional details of how to implement a chip package structure similar to the structure appearing in products implementing X-GOLD. And to the extent applying those teachings would have required modifying a product implementing X-GOLD, a POSITA further would have been motivated to modify that product's architecture for the same reasons, as well as because those teachings provide additional straightforward and obvious modifications that provide additional advantages for, e.g., performance, interoperability, space, thermal performance, efficiency, and/or speed. Additionally, applying those additional teachings for their intended purposes would have been a straightforward modification of X-GOLD. A POSITA therefore would have had a reasonable expectation of success applying those additional teachings to X-GOLD.

5. A5 Chip

The Apple A5 Chip was first offered for sale in an Apple iPad 2 on March 11, 2011, and in iPhone 4s on October 4, 2011, and therefore qualifies as 102(b) prior art to all Asserted Claims. *See* APL-SEMITECH_00528558-APL-SEMITECH_00528561.

Exhibits A10, B10, and C8 show how the A5 Chip discloses and renders obvious the Asserted Claims. For example, based on the evidence in Exhibits A10, B10, and C8, Exhibit S5

MYW Semitech Exhibit 2017
TSMC and Apple v. MYW Semitech - IPR2026-00067

depicts an exemplary reading demonstrating how the A5 Chip discloses and renders obvious each of the Asserted Claims of the Asserted Patents. The mapping in this Exhibit is non-limiting. Applying the evidence in A10, B10, C8, S5, alone and/or in combination with the teachings of other references and/or the understandings of a POSITA as set forth in Exhibits A-C, other mappings are also possible, and the evidence set forth in those Exhibits shows how all Asserted Claims are anticipated and/or obvious in view of the A5 chip alone and/or in combination with other prior art references as forth in Sections III.A and III.C.

Documents comprising descriptions of the A5 Chip that Apple has identified to date include the following: APL-SEMITECH_00552818-APL-SEMITECH_00552840; APL-SEMITECH_00528558-APL-SEMITECH_00528561; APL-SEMITECH_00528553-APL-SEMITECH_00528569; APL-SEMITECH_00553892-APL-SEMITECH_00553893. These documents are not limiting; Apple reserves the right to rely on additional documents and/or information describing the A5 Chip, including but not limited to additional articles, technical documentation, technical analyses, publications, or other descriptions of the A5 Chip. In addition, concurrent with the service of these Initial Invalidity Contentions, Apple has made available for inspection source code information for the A5 Chip providing detailed information about the A5 Chip that further demonstrates that each of the Asserted Claims is invalid. Apple also reserves the right to rely on a physical A5 Chip at trial.

To the extent that there is any dispute that the disclosures set forth above and in Exhibits A10, B10, C8, S5 describe the A5 Chip, a POSITA would have found it obvious and would have been motivated to apply the teachings from those disclosures to the A5 Chip. For example, those disclosures describe related aspects of the same or similar technologies, and describe products and technologies used by the same companies. A POSITA therefore would have been motivated to

MYW Semitech Exhibit 2017
TSMC and Apple v. MYW Semitech - IPR2026-00067

look to these teachings for additional details of how to implement a chip package structure similar to the structure appearing in products implementing the A5 Chip. And to the extent applying those teachings would have required modifying a product implementing the A5 Chip, a POSITA further would have been motivated to modify that product's architecture for the same reasons, as well as because those teachings provide additional straightforward and obvious modifications that provide additional advantages for, e.g., performance, interoperability, space, thermal performance, efficiency, and/or speed. Additionally, applying those additional teachings for their intended purposes would have been a straightforward modification of the A5 Chip. A POSITA therefore would have had a reasonable expectation of success applying those additional teachings to the A5 Chip.

C. Motivation to Modify / Combine

In *KSR Int'l Co. v. Teleflex Inc.,* 127 S. Ct. 1727, 1739 (2007) ("*KSR*"), the U.S. Supreme Court held that a claimed invention can be obvious even if there is no explicit written teaching, suggestion, or motivation for combining the prior art to produce that invention. Accordingly, no showing of an express motivation to combine prior art is required to combine the references disclosed in Exhibits A-C and S1-5 as each combination of art would have no unexpected results, and at most would simply represent a known alternative to one of ordinary skill in the art. *See KSR*, 127 S.Ct. at 1739-40 (rejecting the Federal Circuit's "rigid" application of the teaching, suggestion, or motivation to combine test, and instead espousing an "expansive and flexible" approach).

The Supreme Court in *KSR* held that a POSITA is "a person of ordinary creativity, not an automaton" and "in many cases a person of ordinary skill in the art will be able to fit the teachings of multiple patents together like pieces of a puzzle." *Id*. at 1742. "In determining whether the subject matter of a patent claim is obvious, neither the particular motivation nor the avowed

MYW Semitech Exhibit 2017
TSMC and Apple v. MYW Semitech - IPR2026-00067

purpose of the patentee controls. What matters is the objective reach of the claim." *Id.* at 1741-42. "Under the correct analysis, any need or problem known in the field of endeavor at the time of invention and addressed by the patent can provide a reason for combining the elements in the manner claimed." *Id.* at 1742. In particular, the Supreme Court emphasized the principle that "[t]he combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results." *Id.* at 1739. A key inquiry is whether the "improvement is more than the predictable use of prior art elements according to their established functions." *Id.* at 1740.

The rationale to combine or modify prior art references is significantly stronger when the references seek to solve the same problem, come from the same field, and correspond well. In *In re Inland Steel Co.,* 265 F.3d 1354 (Fed. Cir. 2001), the Federal Circuit allowed two references to be combined as invalidating art when "[the prior art] focus[es] on the same problem that the . . . patent addresses. . . . Moreover, both [prior art references] come from the same field. . . . Finally, the solutions to the identified problems found in the two references correspond well." *Id.* at 1362.

Although Apple contends that no specific showing of motivation to modify or combine is necessary for the references cited in the attached Exhibits, Apple hereby preliminarily identifies specific motivations and reasons to modify or combine the cited art. One or more modifications or combinations of the prior art references identified herein would have been obvious because these references would have been modified or combined using: known methods to yield predictable results; known techniques in the same way; a simple substitution of one known, equivalent element for another to obtain predictable results; or a teaching, suggestion, or motivation in the prior art generally. In addition, it would have been obvious to try modifying or combining the prior art references identified herein because there were only a finite number of

MYW Semitech Exhibit 2017
TSMC and Apple v. MYW Semitech - IPR2026-00067

predictable solutions or because known work in one field of endeavor prompted variations based on predictable design incentives or market forces either in the same field or a different one. In addition, the modification or combination of prior art references identified herein would have been obvious because the modifications or combinations represent known potential options with a reasonable expectation of success.

Additional evidence that there would have been a motivation to modify or combine the prior art references identified in the attached exhibits includes the interrelated teachings of multiple prior art references; the effects of demands known to the community or present in the marketplace; the existence of a known problem for which there was an obvious solution encompassed by the Challenged Claims; the existence of a known need or problem in the field of the endeavor at the time of the invention(s); and the background knowledge that would have been possessed by a person having ordinary skill in the art. The claimed subject matter required nothing more than modifying or combining prior art elements according to known methods to yield predictable results. One of ordinary skill in the art would have been motivated to modify or combine the prior art, in that it required only simple substitutions of one known element for another to obtain predictable results. Thus, a skilled artisan seeking to solve this problem would look to these cited references in combination.

To the extent any limitation of an Asserted Claim is deemed not to be exactly disclosed by an item of prior art, then any purported differences are such that the claimed subject matter as a whole would have been obvious to one skilled in the art at the time of the alleged invention, in view of the state of the art and knowledge of those skilled in the art. Numerous prior art references, including those identified by Apple herein, reflect common knowledge and the state, scope and content of the prior art before the priority dates of the Patents-in-Suit. *See Graham v. John Deere*

MYW Semitech Exhibit 2017
TSMC and Apple v. MYW Semitech - IPR2026-00067

Co., 383 U.S. 1, 35-36 (1966). Indeed, all discussions herein of motivations to combine references also provide support demonstrating that it would have been obvious to modify a reference in view of the understanding of a POSITA as well.

Furthermore, to the extent any limitation of an Asserted Claim is deemed not to be exactly disclosed by an item of prior art, then the claim is rendered obvious by modifying or combining the prior art item with one or more other items of prior art identified in these disclosures as identified above in Section III.A. Apple further reserves the right to rely on any claim chart in Exhibits A-C and S1-S5 standing alone or as identified in the Other Proceedings, in combination with the reference(s) in any other claim chart, in combination with any of the references listed in Exhibit D, in combination with Applicant's Admitted Prior Art, in combination with any reference identified in the Other Proceedings, and/or in view of the knowledge of a POSITA. Though the claim charts in Exhibits A-C and S1-S5 provide illustrative citations to where each element may be found in the prior art references or in their combination, the cited references may contain other disclosures of each claim element as well, and Apple reserves the right to argue any claim elements of the Asserted Claims of the Asserted Patents are disclosed in non-cited portions of these references. For at least the reasons described above and in the claim charts appended hereto, it would have been obvious to one of ordinary skill in the art to modify or combine any of a number of prior art references. The reasons or motivation to modify or combine the prior art would include, for example, the fact that the prior art for the Asserted Claims is in the same field, and one of ordinary skill in the art implementing a device, system, or method in accordance with the Asserted Claims would have been motivated to investigate the various related existing devices, systems, methods, publications or patents identified in these contentions to address the particular needs. Indeed, the claimed subject matter required nothing more than combining prior art elements

MYW Semitech Exhibit 2017
TSMC and Apple v. MYW Semitech - IPR2026-00067

according to known methods to yield predictable results. One of ordinary skill in the art would have been motivated to modify or combine the prior art, in that it required only simple substitutions of one known element for another to obtain predictable results. Moreover, these references cross-reference and discuss one another, illustrating the close technical relationship among them.

To the extent any piece of prior art refers to or discusses other pieces of prior art, either expressly or inherently, it would have been obvious to combine those pieces of prior art for that reason. In addition, design incentives and other market forces would have prompted those combinations and modifications. Furthermore, prior art references may arise from common assignees or multiple companies operating within the relevant subject matter. The motivation to combine references includes the common objectives and subject matter of the identified references. Accordingly, the teachings of the individual prior art references, combined with the industry knowledge of a POSITA at the time of the alleged invention of the Asserted Patents, would render obvious the Asserted Claims.

As discussed above, Apple hereby incorporates by reference, as if set forth fully herein, materials from the Other Proceedings (including IPR2026-00065 to -00067 challenging the Asserted Claims), including without limitation the discussions of the motivations to combine and/or modify set forth therein. This includes, for example, prior art teaching the following concepts being used to modify a reference and/or being applied to other references as disclosed in Section II.A:

1. Multi-layered interconnects in an interconnection scheme, interconnects of a semiconductor chip, thickness of a solid layer, openings in the polymer layers of an interconnection scheme, and interconnection type (collectively, "Interconnect Layout Concepts");

MYW Semitech Exhibit 2017
TSMC and Apple v. MYW Semitech - IPR2026-00067

2. Metal bump materials, materials of metal interconnects on semiconductor chips, material composition and properties of a solid layer, material composition of interconnection scheme polymer layers, and material composition of chip pads (collectively, "Packaging Materials");

3. Type of chips, placement of chips, and placement of passive components (collectively, "Packaged Components"); and

4. Pitch of metal plugs/copper posts and the shape of regions within the chip packaging (collectively, "Plan Layout").

Accordingly, the motivation to combine and/or modify the teachings of the prior art references disclosed herein is found in the references themselves and: (1) the nature of the problem being solved; (2) the express, implied and inherent teachings of the prior art; (3) the knowledge of persons of ordinary skill in the art; (4) the fact that the prior art is generally directed towards relevant methods and systems; or (5) the predictable results obtained in combining the different teachings of the prior art.

Apple reserves the right to rely on one or more references identified in Exhibits A-D and S1-S5 or one or more references identified in the Other Proceedings as further evidence of obviousness under 35 U.S.C. § 103, as background references demonstrating the state of the art, or for any other purpose. Based on further investigation and discovery, based on positions that Semitech may take regarding the scope of the Asserted Claims, and/or based on the Court's claim construction, Apple reserves the right to modify, amend and/or supplement these contentions and to rely on these references to prove the invalidity of the Asserted Patents' Claims in a manner consistent with this Court's Rules and with the Federal Rules of Civil Procedure. Apple expects to provide a detailed explanation of motivations to combine through expert discovery.

1. Interconnection Layout Concepts

MYW Semitech Exhibit 2017
TSMC and Apple v. MYW Semitech - IPR2026-00067

Several limitations of the Asserted Claims recite known semiconductor packaging layout details, such as the use of multi-layered metal interconnects, metal plugs, polymer dimensions, and metal wire interconnections. These details of packaging interconnects were well known, as demonstrated by the Interconnect Layout references (e.g., Sundaram '694 (US9167694), Haba '933, Yu '763, Lin '191, Ahn '785, Yoshida '753, Snapdragon, OMAP 4, OMAP 3, the A5 Chip, and X-GOLD).

A POSITA would have been motivated to modify and/or combine the teachings of the Interconnect Layout references with one another and with the Packaging Materials, Packaged Components, and Plan Layout references as summarized in Section II.A. For example, a POSITA would have been motivated to modify or combine these references for, e.g., the reasons set forth in the discussion of, e.g., limitations 1(a), 1(d), 1(f), 16(a), 16(d), 16(e), 16(f), 16(h), and (25) of the '768 Patent in IPR2026-00065, limitations 1(a), 1(c), and (7) of the '763 Patent in IPR2026-00066, and limitations 10(c), 10(f) (13), and (17) of the '306 Patent in IPR2026-00067.[3] In addition, these limitations recite well-known interconnect designs that would have been nothing more than a routine design choice. A POSITA would have been motivated to select between these different interconnect designs as nothing more than choosing between a finite number of identified, predictable solutions. Applying these teachings from the Interconnect Layout references would have been nothing more than using the references for their intended purposes. A POSITA applying the teachings of the Interconnect Layout references would have had a reasonable expectation of success.

[3] References to the limitations herein are consistent with those in Exhibits A-C and S1-S5 to these Invalidity Contentions. While the IPRs used more granular limitation numbering, cross-references herein are inclusive such that they should be interpreted to include all of the limitations falling within the sublimitations. For example, references to limitation 1(a) includes a cross-reference to limitations 1(a), 1(a)(i), 1(a)(ii), and 1(a)(iii) used in the IPRs.

MYW Semitech Exhibit 2017
TSMC and Apple v. MYW Semitech - IPR2026-00067

For example, it was known in the art to fabricate interconnects using multiple layers of metal. A POSITA would have been motivated to apply teachings of multi-layered metal interconnect layers to, e.g., leverage the advantages of fabricating interconnects using multiple layers of processing including sequentially deposited seed and plating layers formed during electroplating, providing adhesion to the underlying metal layer and buildup of conductor thickness. *See, e.g.*, IPR2026-00065, Pap. 1 at 16-18, 129-130; IPR2026-00066, Pap. 1 at 50-52, 113-114; IPR2026-00067, Pap. 1 at 28-29, 38-40; *see also, e.g.*, U.S. 6,291,884 ("Glenn") at 3:12-24 ("First conductive terminals formed on the bottom surface of the rigid substrate are then electrically connected directly to corresponding conductive pads on the top surface of the chip by fusing balls of a conductive metal disposed between the first terminals and the pads…flip-chip solder interconnections extending between the chip and the substrate."); U.S. 8,093,691 ("Fuentes") at 3:29-52 ("…The substrate 12 may have a plurality of metal traces 16 formed on the first surface of the insulation layer 14. A plurality of metal traces 16 may also be formed on the second surface of the insulation layer 14….A soldermask may be placed over the top surface of the metal traces 16 formed on the substrate 12. The soldermask may be used to protect the metal traces 16. One or more vias 17 may be formed through the insulation layer 14. The vias 17 may be used as an interconnect to connect different layers of metal traces 16."); U.S. 7,888,785 ("Ahn '785") at 9:16-29 ("Referring to FIG. 11D, openings, e.g., trenches, vias, etc., may be formed in the insulating layer 110 in accordance with a pattern of the metal layer 130, which is subsequently formed on the insulating layer 110. The openings may be formed using, e.g., photolithography and etching, micromachining, etc….The metal layer 130 may be formed using, e.g., copper plating and patterning…."); U.S. 2012/0018885 ("Lee-885") at [0067] ("The logic chip 100 may include a through via 160 that penetrates at least a portion of the logic chip 100. The through via 160 may

MYW Semitech Exhibit 2017
TSMC and Apple v. MYW Semitech - IPR2026-00067

include a conductive connection 162 that fills at least a portion of the via hole 161 penetrating the semiconductor substrate 110. A via insulation layer 163 may be disposed between the semiconductor substrate 110 exposed by the via hole 161 and the conductive connection 162. One end of the through via 160 may be directly connected to the first internal wiring 140, and the other end of the through via 160 may be directly connected to the connection pads 154, 155 and 156."); U.S. 2011/0304015 ("Kim") at [0044] ("In some exemplary embodiments, the semiconductor chips 200 a, 200 b, and 200 c are electrically connected to the conductive elements 101, 102, 103, and 104 formed in the substrate 100 a. The plurality of semiconductor chips 200 a, 200 b, and 200 c may be vertically stacked on the substrate 100 a. In some exemplary embodiments, the semiconductor chips 200 a, 200 b, and 200 c and the conductive elements 101, 102, 103, and 104 formed in the substrate 100 a may be connected to one another via conductive pads and conductive wires. In addition, the semiconductor chips 200 a, 200 b, and 200 c may be connected to the conductive elements 101, 102, 103, and 104 using conductive bumps and/or solder balls disposed on the conductive pads…."); U.S. 8,319,338 ("Berry") at 11:28-55 ("…Rather, each via 120 c in the semiconductor package 100 c is filled or lined with a conductive metal material (e.g., copper). Also included in the semiconductor package 100 c is a plurality of conductive traces 128 c which are embedded in the bottom surface 118 c of the package body 114 c….Additionally, formed on each of the traces 128 c is a solder ball 130 c which is to facilitate the electrical connection of the semiconductor package 100 c to an underlying substrate such as a printed circuit board. In the semiconductor package 100 c, the exposed portions of the bottom surface 118 c of the package body 114 c and traces 128 c, as well as portions of each of the solder balls 130 c, may be covered by a layer 132 c of a solder mask or polymer flux."); U.S. 8,183,678 ("Lee-678") at 2:38-54 ("The conductive vias 114 penetrate the insulating layer 111 and electrically connect the lands 112 to the

MYW Semitech Exhibit 2017
TSMC and Apple v. MYW Semitech - IPR2026-00067

conductive patterns 113. The conductive vias 114 may be formed by filling metal in via holes in forming the conductive patterns 113. The solder mask 115 is formed on the lower surface of the insulating layer 111….The first semiconductor die 120 is formed on the substrate 110 using conductive bumps 120 a. The first semiconductor die 120 has a through silicon via (TSV) structure. That is, the first semiconductor die 120 includes a plurality of bond pads 121 formed on one surface of the first semiconductor die 120 and through electrodes 122 that pass through the semiconductor die 120."); U.S. 2008/0308950 ("Yoo") at [0054]-[0055] ("Furthermore, deposition methods may also be used, such as CVD (chemical vapor deposition), PECVD (plasma-enhanced chemical vapor deposition), MOCVD (metal organic chemical vapor deposition), ALD (atomic layer deposition), etc….Also, vias 43 that penetrate the interposer 40 may electrically interconnect the upper and lower sides of the interposer 40…."); U.S. 7,842,541 ("Rusli") at 1:20-31 ("A stiffener is formed, the stiffener including via apertures having electrically conductive via aperture sidewalls and an electronic component opening….An electronic component is mounted to the bump pads and within the electronic component opening thus minimizing the height of the package. Further, the stiffener minimizing undesirable bending of the package and acts as an internal heat sink.").

As another example, it was known to use metal posts through a polymer layer, including through the use of openings in polymer layers, as part of semiconductor packaging. A POSITA would have been motivated to apply teachings of a polymer layer comprising the metal plugs/posts to, e.g., advantageously improve reliability of the chip package, such as preventing delamination and cracking between an interconnection scheme and dielectric layer. A POSITA also would have been motivated to apply teachings of openings in polymer layers to, e.g., advantageously improve the mechanical connection between metal bumps/interconnects and an interconnection scheme.

MYW Semitech Exhibit 2017
TSMC and Apple v. MYW Semitech - IPR2026-00067

See, e.g., IPR2026-00065, Pap. 1 at 63, 87; *see also, e.g.*, Glenn at 10:39-57 ("…However, rather than attaching the substrate to the chip with an adhesive, as described above, the conductive balls 229 between each pair of corresponding connection pads 234 and 206 are then fused, typically by a reflow method, which serves not only to interconnect the substrate 226 electrically with its corresponding chip 204, but also to attach the substrate to the chip mechanically, as shown in FIG. 17."); Fuentes at 6:1-14 ("…In the embodiment shown in FIG. 2A, the portions 25 of the mold compound 24 is removed down a central area of the device 10A to form a channel and to provide compartmental RF shielding…."); Ahn '785 at 7:33-49 ("A thickness of the solder resist 140′ may be increased to provide a surface more conducive to bonding. Further, openings may be provided in the solder resist 140′ to enable connections between the die 142 to be electrically connected to the metal layer 130 using conductive wires 144. In another implementation (not shown), the die 142 may be bonded to exposed pads or portions of the metal layer 130 using a flip-chip or similar arrangement."); Lee-885 at [0069] ("The second through via 165 may be connected to the logic chip pad 145 through the fourth internal wiring pattern 140_4….Alternatively, the second through via 165 may be formed to have a diameter greater than that of the first through via 164. According to an embodiment of the inventive concepts, the resistance of the power transmission path can reduced."); Kim at [0061] ("The connection pads of the semiconductor chip 200 d may be electrically connected to a plurality of conductive elements formed in the substrate 100 c by using the conductive electrodes 205, which may be, for example, solder balls. In the illustrated flip chip configuration, an electrical connection path is relatively short, and thus excellent thermal and electrical characteristics are obtained, and the size of the semiconductor package 10 c is reduced."); Berry at 5:54-6:10 ("…The subsequent completion of a solder reflow process effectively mechanically and electrically connects the solder balls 50 of the top substrate 40 to the solder 38

MYW Semitech Exhibit 2017
TSMC and Apple v. MYW Semitech - IPR2026-00067

in respective ones of the vias 36, thereby electrically connecting the bottom contacts 48 of the top substrate 40 to respective ones of the top contacts 18 of the bottom substrate 12….”); Lee-678 at 9:47-54 (“…In the semiconductor device 100 according to an embodiment of the present invention, the integrated circuits 134 are provided in the interposer 130 to provide the functions of the decoupling capacitor, the ESD preventing circuit, the impedance matching circuit, and the termination and to improve reliability.”); Yoo at [0050] (“Next, as illustrated in FIG. 4D, bumps may be formed by performing soldering on predetermined positions that are electrically connected with the pattern formed on the first substrate (S120). The bumps 13 thus formed can be used as vias that electrically connect the upper layer package with the lower layer package. Therefore, the bumps 13 can be formed to a height that is sufficient for connecting the lower layer package with the upper layer package.”); Rusli at 12:59-13:3 (“…More particularly, electronic component 1824 is located within electronic component opening 710 of stiffener 502 thus minimizing the height of partial cavity flip chip package 1300. Further, stiffener 502 adds rigidity and strength to partial cavity flip chip package 1300 minimizing undesirable bending of partial cavity flip chip package 1300. Accordingly, the reliability of electrical interconnections formed with partial cavity flip chip package 1300 is maximized. Further, stiffener 502 acts as an internal heat sink thus maximizing heat dissipation from partial cavity flip chip package 1300.”).

As another example, it was known in the art to select a thickness for a polymer or solid layer within a semiconductor package for a variety of different reasons. For example, a POSITA would have been motivated to apply teachings of a polymer/solid layer between 100 and 300 micrometers to, e.g., advantageously improve thermal management, provide stress buffering, and/or incorporate shielding layers. *See, e.g.*, IPR2026-00065, Pap. 1 at 78-79, 122; IPR2026-00066, Pap. 1 at 91-92; IPR2026-00067, Pap. 1 at 97-98; *see also, e.g.*, Glenn at 4:64-5:13

MYW Semitech Exhibit 2017
TSMC and Apple v. MYW Semitech - IPR2026-00067

("…Generally speaking, the larger the area of the chip, the more important it is that the TCE of the substrate 126 match that of the chip…."); Fuentes at 1:33-38 ("Existing solutions such as wire fence and via ablation have reduced performance as the mold cap gets thicker because the gap between ground structures increases…Thus, it is beneficial to reduce the maximum gap between ground structures in order to increase shield effectiveness."); Ahn '785 at 6:64-7:2 ("The assembly 190 of the fifth embodiment may also reduce the overall lateral dimensions of the assembly as compared to embedding a plurality of chips side-by-side, e.g., as in the fourth embodiment. Further, the assembly 190 may permit the use of shorter interconnections between semiconductor packages, which may improve signal quality, etc."); Lee-885 at [0131] ("According to this embodiment, since power is delivered through the second through vias 165 and 165′ electrically insulated from the logic chip 100, the length of a power delivery path may be shortened between the package substrate 400 and the memory chips 200 and 300, thereby enabling a high-speed operation."); Kim at [0061] ("In the illustrated flip chip configuration, an electrical connection path is relatively short, and thus excellent thermal and electrical characteristics are obtained, and the size of the semiconductor package 10 c is reduced."); Berry at 6:6-10 ("As further seen in FIG. 1, it is contemplated that an adhesive layer 52 may be interposed between the top surface 34 of the package body 30 and the bottom surface 44 of the top substrate 40 to strengthen the mechanical interconnection therebetween."); Lee-678 at 5:56-60 ("Therefore, when the third semiconductor die 350 larger than the second semiconductor die 340 is stacked, the third semiconductor die 350 is stably supported so that the physical force applied to the second semiconductor die 340 can be reduced."); Yoo at [0039] ("An interposer 40 may be placed…Using a metal oxide layer may provide a benefit of efficiently dispersing heat…problems of reliability in stacking, which may be caused by warpage in the lower layer package, may be alleviated. This particular embodiment

MYW Semitech Exhibit 2017
TSMC and Apple v. MYW Semitech - IPR2026-00067

suggests the use of aluminum oxide (Al_2O_3) for the metal oxide layer, in consideration of cost effectiveness and heat-releasing efficiency, etc."); Rusli at 12:60-13:3 ("More particularly, electronic component 1824 is located within electronic component opening 710 of stiffener 502 thus minimizing the height of partial cavity flip chip package 1300. Further, stiffener 502 adds rigidity and strength to partial cavity flip chip package 1300 minimizing undesirable bending of partial cavity flip chip package 1300. Accordingly, the reliability of electrical interconnections formed with partial cavity flip chip package 1300 is maximized. Further, stiffener 502 acts as an internal heat sink thus maximizing heat dissipation from partial cavity flip chip package 1300."). Selecting a thickness of a substrate would have been a design choice based on factors such as use environment of the package, manufacturability (e.g., layer thickness impacts defect and void formation), and type of chip (e.g., high vs low power chips generate varying degrees of heat).

As another example, the use of metal wire interconnects within a semiconductor package was known. A POSITA would have been motivated to apply teachings of metal wire interconnection, which were known in the art, to, e.g., advantageously decrease cost and/or increase reliability when high bandwidth is not required. *See, e.g.*, IPR2026-00067, Pap. 1 at 54-55, 128-130; *see also, e.g.*, Ahn '785 at 5:39-43 ("Still other advantages may flow from the ability of the package substrate 122 to serve as a redistribution wiring layer, which may simplify assembly and improve reliability by transitioning between a fine pitch of pads on the die to a relatively larger pitch of the metal pattern 130."); Lee-885 at [0101] ("Since the memory chip 200 and the function circuits 120, 130, 132 and 136 are connected to each other through a first internal wiring 140 and logic chip pads 142 and 146, a through via for interfacing the memory chip 200 and the logic chip 100 may not be required. Accordingly, it is possible to reduce the number of the through vias and increase the degree of freedom in the layout design of the function circuits 120, 130, 132 and

MYW Semitech Exhibit 2017
TSMC and Apple v. MYW Semitech - IPR2026-00067

136."); Kim at [0052] ("For example, the conductive elements 101 and 104 may be ground wires electrically connected to the ground voltage GND. When the shielding can 300 a is connected to the ground wires, a degree to which the shielding can 300 a removes EMI may be greater when compared to a configuration in which the shielding can 300 a is not connected to the ground wires."); Berry at 1:29-41 ("Semiconductor dies are conventionally…The elements of such a package include…bond wires which electrically connect pads on the semiconductor die to individual leads of the leadframe…"); Lee-678 at 7:48-51 ("If necessary, the second regions 132 may be selectively connected through the conductive wires 540 b. Therefore, since a fabrication method is simple, a large amount of interposers 130 can be produced."); Yoo at [0070] ("While FIG. 5 illustrates the chip 340 mounted on the bottom of the interposer 332 by a flip chip method, it is apparent that wire bonding methods may be used just as well, and that any of a variety of methods for mounting the chip may be used according to design requirements."); Rusli at 17:57-59 ("Accordingly, the reliability of electrical interconnections formed with partial cavity wirebond package 2700 is maximized.").

2. Packaging Materials Concepts

Several limitations of the Asserted Claims recite the use of specific packaging materials, such as copper, tin, aluminum, SiO_2, multi-layered metals, as well as polymers with particular coefficients of thermal expansion (CTE). These limitations were known—as demonstrated by the Packaging Materials references (e.g., Sundaram '694, Haba '933, Yu '763, Lin '191, Ahn '785, Yoshida '753, Snapdragon, OMAP 4, OMAP 3, the A5 Chip, and X-GOLD).

A POSITA would have been motivated to modify or combine the teachings of the Packaging Materials references with one another and with the Interconnection Layout, Packaged Components, and Plan Layout references as summarized in Section II.A. A POSITA would have been motivated to modify or combine these references for, e.g., the reasons set forth in the

discussion of, e.g., limitations 1(a), 1(d), 1(e), 1(f), 16(e), (20), and (25) of the ’768 Patent in IPR2026-00065, limitations 1(d), (9), and (17) of the ’763 Patent in IPR2026-00066, and limitations 10(d), 10(g), (11), (13), and (14) of the ’306 Patent in IPR2026-00067. For example, it was well known to use different packaging materials for semiconductor packaging. A POSITA would have recognized that the selection of different packaging materials would have been selected for a variety of different reasons including, e.g., cost, electrical conductivity, the ease of fabricating detailed interconnects, ensuring matching of different coefficients of thermal expansion (CTE) to avoid warping, avoiding void formation, and improving bonding effectiveness between different layers of an interconnect. A POSITA also would have recognized that there were a finite number of known materials to be used for semiconductor packaging for a given part of the packaging structure, and that choosing between such materials was nothing more than selecting between a finite number of identified, predictable solutions.

For example, a POSITA would have been motivated to apply teachings of a polymer/solid layer with a coefficient of thermal expansion (CTE) between 3 and 10 ppm/°C to, e.g., advantageously reduce the difference in CTE between components. *See, e.g.*, IPR2026-00065, Pap. 1 at 7-8; *see also, e.g.*, Glenn at 5:1-13 (“Thus, rigid substrate 126 ceramic materials suitable for use in connection with silicon chips in the present invention include a 98% alumina (TCE=5 PPM/° C.), AIN (TCE=4.5 PPM/° C.), silicon carbide (TCE=4 PPM/° C.), and a “laminate” structure of one or more of the foregoing materials (TCE≈6 PPM/° C.). Generally speaking, the larger the area of the chip, the more important it is that the TCE of the substrate 126 match that of the chip.”); Ahn ’785 at 5:34-37 (“The assembly 150 provides the package substrate 122, which may have a CTE between that of the dies 124A and the substrate 100. Accordingly, the harmful effects of CTE mismatch may be reduced or eliminated.”).

MYW Semitech Exhibit 2017
TSMC and Apple v. MYW Semitech - IPR2026-00067

As another example, it was known in the art to use copper and nickel layers within packaging interconnects. Using separate nickel and copper layers advantageously mitigates copper diffusion out of metal interconnects, reducing void formation. Copper also has well-known benefits, including electrical conductivity and electromigration resistance, that are desirable for interconnect material in high-density packaging. Copper has a lower electromigration rate than conventional conductive materials (e.g., aluminum), reducing failures occurring at elevated temperature and high current density. The electrical conductivity of copper is also superior to other metals (e.g., aluminum), enabling faster signal transmission and lower power dissipation. *See, e.g.*, IPR2026-00065, Pap. 1 at 16-18; IPR2026-00066, Pap. 1 at 50-52, 113-114; IPR2026-00067, Pap. 1 at 28-29, 37-40; *see also, e.g.*, Glenn at 5:41-47 ("The traces 130 are formed from an electrically conductive material, preferably copper, tungsten, gold, platinum, silver, or any bondable metal compound. Copper may be used on ceramics that are fired at a relatively low temperature, whereas, tungsten that is subsequently plated with gold is preferably used on AIN and other ceramics that are fired at relatively high temperatures."); Ahn '785 at 9:24-25 ("The metal layer 130 may be formed using, e.g., copper plating and patterning."); Kim at [0049] ("A metal that may be combined with an iron oxide may be, for example, nickel (Ni), zinc (Zn), manganese (Mn), cobalt (Co), magnesium (Mg), aluminum (Al), barium (Ba), copper (Cu), iron (Fe), or the like. The ferrite material may have a high specific resistance and low saturation magnetization. In addition, in some exemplary embodiments, a metal may be combined with the ferrite material to provide mechanical strength."); Berry at 11:36-43 ("Rather, each via 120 c in the semiconductor package 100 c is filled or lined with a conductive metal material (e.g., copper). Also included in the semiconductor package 100 c is a plurality of conductive traces 128 c which are embedded in the bottom surface 118 c of the package body 114 c. Each of the traces 128 c,

MYW Semitech Exhibit 2017
TSMC and Apple v. MYW Semitech - IPR2026-00067

which may also be fabricated from copper, is integrally connected to the copper material filled into a respective one of the vias 120 c."); Lee-678 at 2:29-31 ("The lands 112 are commonly made of copper having high conductivity or an equivalent thereof."); Rusli at 2:64-66 ("In one embodiment, the openings in first buildup layer 206 are filled by electroplating an electrically conductive material such as copper to form lower circuit pattern 202.").

As another example, the use of tin within semiconductor packaging was a well known way to connect components within a semiconductor package, including on a substrate. A POSITA would have been motivated to apply teachings of metal bumps with a tin-containing layer because, e.g., it was known that applying a tin-containing layer advantageously improves the ability for the metallic layer to be more easily melted to be spread across the intended area of substrate, improving interconnectivity. *See, e.g.*, IPR2026-00065, Pap. 1 at 19-20; IPR2026-00066, Pap. 1 at 20-21; IPR2026-00067, Pap. 1 at 18-19, 105; *see also, e.g.*, Mulugeta Abtew, et al., *Lead-free Solders in Microelectronics*, Materials Science and Engineering, 2000, at 104.

As another example, it was known in the art to fabricate metal bumps as part of a packaging connection using multiple layers of metal. A POSITA would have been motivated to apply teachings of a layered metal bump to, e.g., advantageously improve metallurgical bonding and increased resistance to fatigue and stress-induced failure. *See, e.g.*, IPR2026-00065, Pap. 1 at 26-27; IPR2026-00066, Pap. 1 at 27-28; IPR2026-00067, Pap. 1 at 26, 28-29; *see also, e.g.*, Glenn at 11:46-55 ("The underfill 246 serves not only to seal and protect the active surface 207 of the chip and the flip- chip interconnections 206, 229, 234 between the chip and the substrate from penetration by damaging moisture, but also to prevent shorting of the solder interconnects between each other and/or the collapse of the chip onto the substrate when the package 200 is surface-mounted to a main board by a high-temperature reflow soldering process that re-melts some or all

MYW Semitech Exhibit 2017
TSMC and Apple v. MYW Semitech - IPR2026-00067

of the chip-to-substrate interconnection balls 229."); Fuentes at 3:45-50 ("The number of multiple layers of metal traces 16 and insulation layers 14 is not limited to that shown in FIG. 1A. A soldermask may be placed over the top surface of the metal traces 16 formed on the substrate 12. The soldermask may be used to protect the metal traces 16."); Ahn '785 at 7:38-42 ("The die 142 may be bonded at an exposed surface of the assembly 210, e.g., on a solder resist 140′. Such bonding may be achieved using, e.g., a liquid or film-type adhesive. A thickness of the solder resist 140′ may be increased to provide a surface more conducive to bonding."); Kim at [0056] ("In some exemplary embodiments, high-temperature heat treatment, such as, for example, a wave soldering or reflow soldering process, may be performed to bond the semiconductor package 10 a to a mother board or other semiconductor packages via the conductive external connection electrodes 600."); Berry at 5:57-6:2 ("As will be recognized by those of ordinary skill in the art, such advancement is limited by the abutment of each solder ball 50 against the solder 38 filled into the corresponding via 36…The subsequent completion of a solder reflow process effectively mechanically and electrically connects the solder balls 50 of the top substrate 40 to the solder 38 in respective ones of the vias 36, thereby electrically connecting the bottom contacts 48 of the top substrate 40 to respective ones of the top contacts 18 of the bottom substrate 12."); Yoo at [0050] ("The bumps 13 thus formed can be used as vias that electrically connect the upper layer package with the lower layer package. Therefore, the bumps 13 can be formed to a height that is sufficient for connecting the lower layer package with the upper layer package.").

As another example, it was well known in the art to use metal pads for chip contact pads. A POSITA would have been motivated to apply teachings of an aluminum metal pad to, e.g., advantageously use a well-known and widely used material for forming contact pads in chips compatible with established bond wire attachment methods, low cost, and consistent with legacy

MYW Semitech Exhibit 2017
TSMC and Apple v. MYW Semitech - IPR2026-00067

materials used in semiconductor processing. IPR2026-00066, Pap. 1 at 53-54, 114; *see also, e.g.*, Kim at [0042] ("Also, in some embodiments, the plurality of conductive elements 101, 102, 103, and 104 may include at least one metal selected from the group consisting of aluminum (Al)"); Yoo at [0039] ("This particular embodiment suggests the use of aluminum oxide (Al_2O_3) for the metal oxide layer, in consideration of cost effectiveness and heat-releasing efficiency, etc.").

As another example, the use of SiO_2 layers was well known in the art and were commonly used, e.g., as a known and easily grown insulative dielectric and protective layer that can be grown on silicon wafers to fabricate precise, micro-scale structures as needed for both semiconductors and chip packaging. A POSITA would have been motivated to apply teachings of a SiO_2 layer to, e.g., advantageously improve water vapor permeability and realize these known advantages of using SiO_2. *See, e.g.*, IPR2026-00066, Pap. 1 at 121-122; IPR2026-00067, Pap. 1 at 114-115; *see also, e.g.*, Glenn at 4:54-61 ("The rigid substrate 126 is provided in the form of a "coupon" of a fairly rigid, electrically insulating material, for example, a ceramic, silicon oxide…or a low-TCE laminate of one or more layers of the above rigid substrate materials that are available from, e.g., the NTK Technical Ceramics Division of NGK Spark Plugs (U.S.A.), Inc., Irvine, Calif."); Lee-885 at [0065] ("The insulation layer 149 may include, for example, a silicon oxide layer, a silicon nitride layer, or a silicon oxynitride layer. The insulation layer 149 may prevent the semiconductor substrate 110 from being contaminated by conductive materials used in a subsequent process."); Kim at [0053] ("The adhesive layer 305 a also prevents the shielding can 300 a from being electrically connected to the region 400 a. In some particular exemplary embodiments, the adhesive layer 305 a may include at least one of a silicon oxide (SixOy)…"); Lee-678 at 4:35-38 ("The encapsulant 170 protects the internal elements. To this end, the encapsulant 170 may be

MYW Semitech Exhibit 2017
TSMC and Apple v. MYW Semitech - IPR2026-00067

made of one selected from the group consisting of common epoxy resin, silicon resin, and equivalents thereof.”).

3. Packaged Components Concepts

Several limitations of the Asserted Claims are directed to features of semiconductor packages relating to the different components within the package including, e.g., a chip that uses metal pads, a passive component, a chip with a CPU circuit block and GPU circuit block, or including additional semiconductor chips within the package. Each of these features are disclosed by the Packaged Components references (e.g., Sundaram ’694, Haba ’933, Yu ’763, Lin ’191, Ahn ’785, Yoshida ’753, Snapdragon, OMAP 4, OMAP 3, the A5 Chip, X-GOLD).

A POSITA would have been motivated to modify or combine the teachings of the Packaged Components references with one another and with the Interconnection Layout, Packaging Materials, and Plan Layout references as summarized in Section II.A. A POSITA would have been motivated to modify or combine these references for, e.g., the reasons set forth in the discussion of limitations 1(f), (2), (4), (5), 16(g), 16(i), (22), and (25) of the ’768 Patent in IPR2026-00065, limitations 1(e), (2), and (5) of the ’763 Patent in IPR2026-00066, and limitations 10(f), 10(g), and (17) of the ’306 Patent in IPR2026-00067. For example, it was known to use semiconductor packaging technologies with a variety of different types of chips depending on the intended use of a given chip package. For example, including multiple different chips and components within a package was well known as this was part of the purpose of implementing a single chip package integrating multiple chips. Including these components within a package would have been nothing more than implementing the package for its intended purpose.

For example, it was known to include chips that use metal pads for interconnects within a chip package. A POSITA would have been motivated to apply well-understood teachings of a metal pad on a chip to, e.g., advantageously provide an interconnection point on the chip used for

MYW Semitech Exhibit 2017
TSMC and Apple v. MYW Semitech - IPR2026-00067

interconnecting the chip with other components within the package. *See, e.g.*, IPR2026-00065, Pap. 1 at 24; IPR2026-00066, Pap. 1 at 25, 102-103; IPR2026-00067, Pap. 1 at 26, 109; *see also, e.g.*, Glenn at 10:62-11:6 ("However, since the connection pads 234 are located on the bottom surface 228 of the substrate 226 in this embodiment, it is necessary to provide a conductive path through the thickness of the insulative substrate between the conductive traces 230 and the connection pads 234 to electrically interconnect the chip 204 with the contact terminals 231 on the top surface 227 of the substrate. This is accomplished by forming plated-through holes, or "vias," 242 in the substrate 226 between the connection pads 234 and the partial leads of the conductive traces 230 using known via-hole forming techniques adapted for use with ceramic materials."); Ahn '785 at 4:10-14 ("The semiconductor package 120 may include the dies 124A and 124B, which may be connected using, e.g., wire bonds 126, to conductive features, e.g., pads, that are exposed on a first surface of a package substrate 122, which faces downward in FIG. 1."); Lee-885 at [0067] ("One end of the through via 160 may be directly connected to the first internal wiring 140, and the other end of the through via 160 may be directly connected to the connection pads 154, 155 and 156."); Kim at [0044] ("In some exemplary embodiments, the semiconductor chips 200 a, 200 b, and 200 c and the conductive elements 101, 102, 103, and 104 formed in the substrate 100 a may be connected to one another via conductive pads and conductive wires."); Berry at 1:49-56 ("In certain semiconductor packages, a portion of the die attach pad or die pad of the leadframe also remains exposed within the package body…which includes pads or terminals for mimicking the functionality of the leads and establishing electrical communication with another device."); Yoo at [0034] ("The chip 20 may be directly connected, by way of solder 21, to the pads 12 formed on the substrate 10. That is, the chip 20 may be mounted by a flip chip method. As such, not only can a sufficient amount of space be obtained on the substrate 10 for forming the

pattern 11, etc., that allows connection with the upper layer package, but also numerous passive components 14, such as RLC, can be mounted, making it possible to systemize the lower layer package by itself."); Rusli at 1:27-29 ("An electronic component is mounted to the bump pads and within the electronic component opening thus minimizing the height of the package.").

As another example, it was known to include passive components (capacitors, resistors, inductors) within a chip package to improve the operation of the package. For example, a POSITA would have been motivated to apply teachings of a passive component (including connected through a solder layer) to, e.g., advantageously mitigate signal desynchronization and preserve signal integrity. *See, e.g.*, IPR2026-00065, Pap. 1 at 29-30, 98; IPR2026-00066, Pap. 1 at 29-31, 106-107; *see also, e.g.*, Fuentes at 3:53-56 ("One or more electronic component 18 may be attached to a first surface of the first substrate 12. The electronic component 18 may be prepackaged semiconductor device, bare semiconductor die, or a passive component."); Ahn '785 at 6:4-9 ("In an implementation, the substrate 100 may include the circuit pattern 104 on both sides of the substrate, and may further include the solder resist 140 on both sides of the substrate, as shown in FIG. 2. Such a configuration may increase the number of options for the routing of wiring and mounting of other active or passive devices."); Lee-885 at [0061] ("The function circuits 120, 130, 132 and 136 may include integrated circuits. The function circuits 120, 130, 132 and 136 may include passive elements such as transistors, resistors, and capacitors."); Kim at [0093] ("According to the exemplary embodiment of FIG. 7, the semiconductor package 20 may further include passive elements 230 a and 230 b which are used to improve signal integrity that may be degraded when at least one circuit is integrated in the IC package 10 and signals are transmitted. The passive elements 230 a and 230 b may also be used to improve power integrity, which may be degraded due to power supply interference. For example, in some exemplary embodiments, the

MYW Semitech Exhibit 2017
TSMC and Apple v. MYW Semitech - IPR2026-00067

passive elements 230 a and 230 b may include a decoupling capacitor. Signal integrity and power integrity may be improved by including the passive elements 230 a and 230 b."); Berry at 9:45-52 ("The top substrate assembly 66 f comprises a top substrate 40 f which is substantially similar to the top substrate 40 of the semiconductor package 10, except that one or more electronic components such as semiconductor dies, passive devices and the like are mounted to the top surface of the top substrate 40 f and electrically connected to the bottom contacts 48 f disposed on the bottom surface 44 f of the top substrate 40 f in a prescribed pattern or arrangement."); Lee-678 at 5:15-25 ("The passive elements 235 can realize parts of the functions of the integrated circuits 234 and can constitute various other elements of the semiconductor device 200 according to another embodiment of the present invention. The passive elements 235 may be so complicated that the passive elements 235 cannot be realized by the first semiconductor die 120 and the second semiconductor die 140. In this case, when the number of processes of the semiconductor dies is reduced, fabrication cost can be reduced. In addition, in order to provide the passive elements 235, the interposer 230 is larger than the first semiconductor die 120."); Yoo at [0034] ("As such, not only can a sufficient amount of space be obtained on the substrate 10 for forming the pattern 11, etc., that allows connection with the upper layer package, but also numerous passive components 14, such as RLC, can be mounted, making it possible to systemize the lower layer package by itself."); Rusli at 7:40-46 ("Electronic component 1824 can be an active component such as an integrated circuit die or a passive component such as a resistor, capacitor, or inductor."). Indeed, such passive components have commonly been used for this purpose either within the package itself or on the motherboard underneath or next to the package to, e.g., stabilize power delivery, filter electrical noise, manage voltage, and ensure reliable high speed operation of the processor. A POSITA would have recognized that including the passive component within the chip package

MYW Semitech Exhibit 2017
TSMC and Apple v. MYW Semitech - IPR2026-00067

itself advantageously would have reduced the space needed on the motherboard itself for this component, reduced the length of interconnects needed between other components within the chip package and the passive component, and increased the responsiveness and ability for the passive component to be used for its intended purpose. Indeed, by placing the passive components closer to the processor and its interconnects to the chip package, the passive components can be more effectively wired to interface with portions of the processor for which the passive component's functionalities are most needed.

As another example, it was known to use multicore processors that included CPU and GPU cores within a multichip package—including by integrating such a package with both CPU/GPU—and memory chips such as DRAM chips, including e.g. by stacking these chips over and/or under an interconnection scheme. For example, a POSITA would have been motivated to apply teachings of a CPU circuit block and a GPU circuit block to, e.g., advantageously provide increased capabilities, i.e., to carry out the functions of both a CPU and a GPU. Including each of these chips over the interconnection scheme advantageously adds functionality while maximizing space and providing a shorter path length between the passive component and chips within the chip package. *See, e.g.*, IPR2026-00065, Pap. 1 at 36-37, 109-110, 130; IPR2026-00066, Pap. 1 at 37-39; IPR2026-00067, Pap. 1 at 31-33; *see also, e.g.*, Ahn '785 at 8:33-41 ("The memory 820, the processor 810, the I/O device 830, and the bus 840 may be packaged together as an MCP. The memory 820, the processor 810, and/or the I/O device 830 may be formed according to one or more of the embodiments described herein. In an implementation, one, some, or all of the components (memory 820, the processor 810 and the I/O device 830) may be packaged together, e.g., they may be vertically stacked together as an MCP."); Lee-885 at [0153] ("The SSD controller 1620 may include a CPU 1621, a host interface 1622, a buffer manager 1623, and a memory

MYW Semitech Exhibit 2017
TSMC and Apple v. MYW Semitech - IPR2026-00067

interface 1624. The CPU 1621 may control the respective components according to firmware for driving the SSD 1600. For example, the CPU 1621 may deliver various control signals for read/write operations to the host 1610 and the memory interface 1624, and may perform an access operation on the buffer memory 1630 or the memories 1640…the buffer memory 1630 may include a synchronous DRAM for providing a sufficient buffering space for the SSD 1600 used as a large-capacity auxiliary memory…"); Kim at [0097] ("The CPU 710 controls the operation of the memory device 700 via the data bus 740. The CPU 710 may communicate with an external device and may receive a control signal from the external device, such as a host. For example, the CPU 710 may communicate with the external device via various interface protocols…"). This would have advantageously allowed the chip package to operate for its intended purpose—e.g., to efficiently package the CPU and GPU circuit blocks in a way that provided them with lower latency access to memory and other functions in a lower power configuration that also reduced the form factor of the component itself.

4. Plan Layout Concepts

Several limitations of the Asserted Claims are directed to concepts describing the top-down (or plan layout) arrangement of a semiconductor package including, e.g., the arrangement of regions relative to one another, and specifying the pitch of pins within the different regions of the package. These features are well-understood and were disclosed by the Plan Layout references (e.g., Sundaram '694, Haba '933, Yu '763, Lin '191, Ahn '785, Yoshida '753, Snapdragon, OMAP 4, OMAP 3, the A5 Chip, and X-GOLD).

A POSITA would have been motivated to modify or combine the teachings of the Plan Layout references with one another and with the Interconnection Layout, Packaging Materials, and Packaged Components references as summarized in Section II.A. A POSITA would have been motivated to modify or combine these references for, e.g., the reasons set forth in the discussion

MYW Semitech Exhibit 2017
TSMC and Apple v. MYW Semitech - IPR2026-00067

of limitations (14) and (19) of the ’768 Patent in IPR2026-00065, limitations (12) and (13) of the ’763 Patent in IPR2026-00066, and limitation (16) of the ’306 Patent in IPR2026-00067. Indeed, it has been well-known to use rectangular-shaped silicon die within a chip, and that the rectangular shape of silicon die will dictate where some interconnects can be located such that they can be effectively used to interconnect that silicon die. By implementing such arrangements, this also opens up space for additional components to be placed underneath chip die in a way that advantageously improves the efficient use of space. Techniques for implementing such plan view features have been well-known and understood, and selecting a rectangular arrangement, or using a known pitch for the grid of interconnects, would have been nothing more than the use of a known solution for its intended purpose.

For example, the use of a grid of pins with a defined pitch was well known. A POSITA would have been motivated to apply teachings of a pitch between plugs/posts of 200 to 1000 micrometers to, e.g., advantageously enable high bandwidth speeds and allow the package to be used for its intended purpose. *See, e.g.*, IPR2026-00065, Pap. 1 at 57-58, 139-140; IPR2026-00066, Pap. 1 at 57, 116-117; *see also, e.g.*, Ahn ’785 at 5:38-46 (“Still other advantages may flow from the ability of the package substrate 122 to serve as a redistribution wiring layer, which may simplify assembly and improve reliability by transitioning between a fine pitch of pads on the die to a relatively larger pitch of the metal pattern 130. For example, the pitch of features in the metal pattern 130 may be those of a printed circuit board (PCB), e.g., about 500 μm, whereas the pitch of features on the surface of the dies 124A and 124B may be, e.g., about 50 μm.”); Lee-885 at [0133] (“When having the same pitch as the conductive members 370 of the second memory chip 300, the fifth through vias 260 may be disposed in a vertical alignment with the conductive

MYW Semitech Exhibit 2017
TSMC and Apple v. MYW Semitech - IPR2026-00067

members 370 of the second memory chip 300. Accordingly, the length of signal and/or power delivery path(s) can be reduced to enable a high-speed operation.”).

As another example, because of the known techniques of stacking die and the need to create interconnects around such die, it was known to arrange regions in a plan view of a chip package in rectangles. A POSITA would have been motivated to apply teachings of a second region being a rectangle surrounding a first region to, e.g., advantageously permit the addition of passive components directly under the chip, allow for placement of heat sink material directly under the chip, improve thermal dissipation, provide for shorter interconnect paths, and maximize the use of valuable wafer area where circuitry can be fabricated. *See, e.g.*, IPR2026-00066, Pap. 1 at 77-79, 130; IPR2026-00067, Pap. 1 at 87-89; *see also, e.g.*, Glenn at 6:49-65 (“FIG. 5 is an enlarged plan view of a rectangular portion 100 of a semi-conductor wafer having a plurality of dies, or chips, 104 formed therein…Fabrication of chips on a semiconductor wafer, testing of the chips, and marking of defective chips, are well known to those skilled in the semiconductor manufacturing art.”); Ahn ’785 at 6:64-7:2 (“…Further, the assembly 190 may permit the use of shorter interconnections between semiconductor packages, which may improve signal quality, etc.”); Kim at [0061] (“In the illustrated flip chip configuration, an electrical connection path is relatively short, and thus excellent thermal and electrical characteristics are obtained, and the size of the semiconductor package 10 c is reduced.”); Berry at 9:45-52 (“The top substrate assembly 66 f comprises a top substrate 40 f which is substantially similar to the top substrate 40 of the semiconductor package 10, except that one or more electronic components such as semiconductor dies, passive devices and the like are mounted to the top surface of the top substrate 40 f and electrically connected to the bottom contacts 48 f disposed on the bottom surface 44 f of the top substrate 40 f in a prescribed pattern or arrangement.”); Lee-678 at 5:15-28 (“The passive elements

MYW Semitech Exhibit 2017
TSMC and Apple v. MYW Semitech - IPR2026-00067

235 can realize parts of the functions of the integrated circuits 234 and can constitute various other elements of the semiconductor device 200 according to another embodiment of the present invention…In addition, in order to provide the passive elements 235, the interposer 230 is larger than the first semiconductor die 120. Therefore, since the second semiconductor die 140 formed on the interposer 230 can be larger than the first semiconductor die 120, the restriction on the size of the semiconductor die 140 can be reduced."); Yoo at [0008] ("However, in the semiconductor package according to the related art, the metal pads for mounting the upper layer package may reduce the mounting area, making it difficult to obtain a sufficient space for mounting passive components such as RLC.").

IV. INVALIDITY UNDER 35 U.S.C. § 112

The Asserted Claims of the Asserted Patents are invalid under 35 U.S.C. § 112 because (1) the claims are indefinite, (2) the claims lack adequate written description; and/or (3) the claims are not enabled. Apple's contentions that the following claims are invalid under 35 U.S.C. § 112 are made in the alternative and do not constitute, and should not be interpreted as, admissions regarding the construction or scope of the claims of the Asserted Patents, or that any of the claims of the Asserted Patents are not anticipated or rendered obvious by prior art.

The following contentions, made pursuant to the Scheduling Order, are subject to revision and amendment pursuant to Rule 26(e), Fed. R. Civ. P., and the Orders of record in this matter to the extent appropriate, *e.g.*, in light of further investigation and discovery regarding the defenses, the Court's construction of the claims at issue, and/or review and analysis of expert witnesses. Apple offers these contentions in response to Semitech's apparent interpretation of the Asserted Claims and Semitech's Initial Infringement Contentions, which remain insufficient under the Patent Rules, as explained in Apple's correspondence to Semitech.

MYW Semitech Exhibit 2017
TSMC and Apple v. MYW Semitech - IPR2026-00067

For example, the following exemplary limitations of the Asserted Claims, individually and collectively, do not satisfy the enablement or written description requirements of Section 112:

a. ’768 Patent:

- Claim 1: “a first polymer layer having a first surface and a second surface opposite to said first surface, wherein said first surface is substantially parallel to said second surface”

- Claim 1: “a first metal plug vertically in a first through via in said first polymer layer”

- Claim 1: “a second metal plug vertically in a second through via in said first polymer layer, wherein said second metal plug comprises a second copper layer, wherein a top surface of said second metal plug and a top surface of said first metal plug are in the same horizontal plane”

- Claim 1: “a first interconnection scheme over said first surface, wherein said first interconnection scheme comprises a first metal interconnect over said first surface, a second metal interconnect over said first surface, a third metal interconnect over said first surface and a second polymer layer over said first, second and third metal interconnects, wherein said first metal interconnect is connected to said first metal plug, wherein said second metal interconnect is connected to said second metal plug, wherein said first metal interconnect comprises a first metal layer, a third copper layer on said first metal layer, and a fourth copper layer on said third copper layer”

- Claim 1: “a first semiconductor chip under said first interconnection scheme, wherein said first semiconductor chip comprises a fourth metal interconnect on a first metal pad of said first semiconductor chip”

- Claim 2: “The chip package of claim 1, further comprising a passive component over said first interconnection scheme and connected to said first interconnection scheme through a solder layer”

- Claim 4: “The chip package of claim 1, further comprising a second semiconductor chip over said first interconnection scheme”

- Claim 14: “The chip package of claim 1, further comprising a third metal plug vertically in a third through via in said first polymer layer”

- Claim 16: “a first polymer layer having a first surface and a second surface opposite to said first surface, wherein said first surface is substantially parallel to said second surface, wherein said first polymer layer has a thickness between 100 and 300 micrometers”

- Claim 16: “a first metal plug vertically in a first through via in said first polymer layer,”

MYW Semitech Exhibit 2017
TSMC and Apple v. MYW Semitech - IPR2026-00067

- Claim 16: “a second metal plug vertically in a second through via in said first polymer layer, wherein said second metal plug comprises a second copper layer, wherein a top surface of said second metal plug and a top surface of said first metal plug are in the same horizontal plane”

- Claim 16: “a first interconnection scheme over said first surface, wherein said first interconnection scheme comprises a first metal interconnect over said first surface, a second metal interconnect over said first surface and a second polymer layer over said first and second metal interconnects, wherein said first metal interconnect is connected to said first metal plug, wherein said first metal interconnect comprises a first metal layer, a third copper layer on said first metal layer, and a fourth copper layer on said third copper layer”

- Claim 16: “a first metal bump over said first interconnection scheme, wherein said first metal bump is connected to said first interconnection scheme through a first opening in said second polymer layer”

- Claim 16: “a second metal bump over said first interconnection scheme, wherein said second metal bump is connected to said first interconnection scheme through a second opening in said second polymer layer”

- Claim 16: “a first semiconductor chip over said first interconnection scheme and between said first and second metal bumps”

- Claim 16: “a third metal bump between said first semiconductor chip and said first interconnection scheme, wherein said third metal bump connected to said second metal interconnect through a third opening in said second polymer layer”

- Claim 16: “a second semiconductor chip under said first interconnection scheme and said first semiconductor chip, wherein said first interconnection scheme is between said first and second semiconductor chips”

- Claim 19: “The chip package of claim 16, further comprising a third metal plug vertically in a third through via in said polymer layer”

- Claim 20: “wherein said first polymer layer has a thickness between 100 and 300 micrometers and has a coefficient of expansion between 3 and 10 ppm/° C” (’768 Patent, claim 1) / “wherein said first polymer layer has a coefficient of expansion between 3 and 10 ppm/°C”

- Claim 22: “The chip package of claim 16, further comprising a passive component over said first surface”

- Claim 25: “The chip package of claim 16, wherein said second semiconductor chip comprises a third metal interconnect on a metal pad of said second semiconductor chip, wherein said third metal interconnect comprises a second metal layer on said metal pad and a fifth copper layer over said second metal layer”

MYW Semitech Exhibit 2017
TSMC and Apple v. MYW Semitech - IPR2026-00067

b. ’763 Patent:

- Claim 1: “a solid layer having a first surface and a second surface opposite to said first surface, wherein said first surface is substantially parallel to said second surface, wherein said solid layer comprises a compound of silicon and oxygen, wherein said solid layer has a thickness between 100 and 300 micrometers, wherein said solid layer comprises a first region and a second region between said first region and an edge of said solid layer”

- Claim 1: “a plurality of copper plugs in a plurality of through vias in said second region of said solid layer respectively, wherein one of said plurality of copper plugs comprises a first copper layer contacting a sidewall of one of said plurality of through vias”

- Claim 1: “a first interconnection scheme over said first surface, wherein said first interconnection scheme comprises a first metal interconnect over said first surface, a second metal interconnect over said first surface and a first polymer layer over said first and second metal interconnects, wherein said first metal interconnect is connected to a first copper plug of said plurality of copper plugs, wherein said second metal interconnect is connected to a second copper plug of said plurality of copper plugs, wherein said first metal interconnect comprises a first metal layer and a second copper layer over said first metal layer, wherein a top surface of said second copper plug and a top surface of said first copper plug are substantially in the same horizontal plane”

- Claim 1: “a first semiconductor chip under said first interconnection scheme, wherein said first semiconductor chip comprises a third metal interconnect on a first metal pad of said first semiconductor chip, wherein said third metal interconnect comprises a third metal layer on said first metal pad and a third copper layer over said third metal layer”

- Claim 2: “The chip package of claim 1, further comprising a passive component over said first interconnection scheme and connected to said first interconnection scheme through a solder layer”

- Claim 4: “The chip package of claim 1, further comprising a second semiconductor chip over said first interconnection scheme, wherein said second semiconductor chip comprises a second metal bump between said second semiconductor chip and said first interconnection scheme”

- Claim 7: “The chip package of claim 1, wherein said first interconnection scheme further comprises a fourth metal interconnect over said first metal interconnect and said first polymer layer, wherein said first polymer is between said first and fourth metal interconnects, wherein said fourth metal interconnect comprises a fourth metal layer, a fourth copper layer on said fourth metal layer, and a fifth copper layer on said fourth copper layer”

- Claim 10: “The chip package of claim 1, wherein said solid layer further comprises a third region opposite to said second region, wherein said third region is between said first region and another edge of said solid layer, wherein said plurality of copper plugs in said plurality of through vias in said third region respectively”

MYW Semitech Exhibit 2017
TSMC and Apple v. MYW Semitech - IPR2026-00067

- Claim 13: "The chip package of claim 1, wherein said second region is a rectangle region and surrounding said first region"

- Claim 14: "The chip package of claim 1, further comprising a second semiconductor chip over said first interconnection scheme and connected to said first interconnection scheme through a second metal bump, wherein said second semiconductor chip has a height is between a backside surface of said second semiconductor chip and a top surface of said first polymer layer is smaller than a thickness of said first metal bump."

c. '306 Patent:

- Claim 10: "a solid layer having a first surface and a second surface opposite to said first surface, wherein said solid layer comprises a compound of silicon and oxygen, wherein said solid layer has a thickness between 100 and 300 micrometers, wherein said solid layer comprises a first region and a second region between said first region and a first edge of said solid layer"

- Claim 10: "a plurality of copper posts in a plurality of through holes in said second region respectively"

- Claim 10: "a first interconnection scheme over said first surface, wherein said first interconnection scheme comprises a first metal interconnect over said first surface, and a polymer layer over said first metal interconnect, wherein said first metal interconnect is connected to one of said plurality of copper posts"

- Claim 10: "a first semiconductor chip over said first interconnection scheme and between said first and second metal bumps, wherein said first semiconductor chip has a height between a backside surface of said first semiconductor chip and a top surface of said polymer layer is smaller than a thickness of said first metal bump"

- Claim 10: "a second semiconductor chip over said first interconnection scheme"

- Claim 13: "The chip package of claim 10, further comprising a third semiconductor chip under said first interconnection scheme, wherein said third semiconductor chip comprises a second metal interconnect on a third metal pad of said third semiconductor chip"

- Claim 14: "The chip package of claim 10, further comprising a third semiconductor chip under said first interconnection scheme, wherein said third semiconductor chip comprises a second metal interconnect on a third metal pad of said third semiconductor chip"

- Claim 15: "The chip package of claim 10, wherein said solid layer further comprises a third region opposite to said second region, wherein said third region is between said first region and a second edge of said solid layer, wherein said plurality of copper posts in said plurality of through holes in said third region"

- Claim 16: "The chip package of claim 10, wherein said second region is a rectangle region and surrounding said first region.

- Claim 17: "The chip package of claim 10, further comprising an electrical device under said second surface, wherein said electrical device comprise a third semiconductor chip and a metal wire connected to a third metal pad of said third semiconductor chip"

For example, the Asserted Claims lack written description and enablement support because they were broadened and amended during prosecution. On information and belief, this is due at least in part to the fact that, prior to submitting the claims that issued as the Asserted Claims, the Applicant and/or the named inventor reviewed products of third parties, including at least the Accused Products, TSMC's InFo-PoP technology identified in the Complaint, and other third-party products ("Prior Third-Party Products"). At least some Prior Third-Party Products, including at least products comprising the Apple A10 chip, were publicly announced years before the application that later issued as the '768 Patent, the earliest of the Asserted Patents, was filed in 2020. On information and belief, the Applicant and named inventor were aware of the Prior Third-Party Products, including prior to filing the applications that ultimately issued as the Asserted Patents, and broadened and amended its claims during prosecution to try to capture the Accused Products.

First, as one example, the Asserted Claims vary from the claims of the patents to which they purport to claim priority because unlike those earlier claims, the Asserted Claims were drafted such that they are not limited to glass-based technology. The Asserted Patents claim priority as continuations to U.S. Patent No. 10,622,310 ("'310 Patent"), which in turn claim priority as a continuation-in-part to U.S. Patent No. 9,615,453 ("'453 Patent"). When the '453 Patent was filed, the claim set was directed to a specific glass-type substrate having, e.g., "a solid glass core," and "multiple conductors extending through said solid glass core." File History of the '453 Patent (APL-SEMITECH_00553136-APL-SEMITECH_00553416), at APL-SEMITECH_00553186 (Sept. 25, 2013 Claims). The issued claims of the '453 Patent were also directed to a similar glass-type "structure" comprising, e.g., "a first glass substrate" with "multiple conductors extending

through said first glass substrate," a "first chip" over the substrate, and "a second glass substrate" under the first glass substrate. *Id.* at APL-SEMITECH_00553394 (Feb. 10, 2017 Claims).

The claims of the '310 Patent likewise were directed to glass substrates, in a "OLED display panel device." The as-filed claims of the '310 Patent were directed to a "display device" comprising, e.g., a "glass substrate comprising multiple metal conductors through in said glass substrate." File History of '310 Patent (APL-SEMITECH_00553417-APL-SEMITECH_00553889), at APL-SEMITECH_00553457(Sept. 11, 2016 Claims). The issued claims of the '310 Patent are similarly directed to an "OLED display panel device" comprising, e.g., "a first glass substrate" having "multiple metal conductors extending through the said first glass substrate" and "a first chip bonded and under said first glass substrate." *Id.* at APL-SEMITECH_00553865-866 (Feb. 29, 2020 Claims).

The Asserted Patents claim priority to the '453 and '310 Patents via continuation applications, but, when filing the application that issued as the '768 Patent, the applicant substantially changed the scope of the claim sets to no longer be directed to glass-related technologies. For example, instead of reciting a device comprising a "glass substrate," the claims now recite a broader genus of structures comprising, e.g., a "polymer layer," a "solid layer," or a layer that comprises a "compound of silicon and oxygen." The specifications of the Asserted Patents, and the patents to which they claim priority, do not contain sufficient written description support for these limitations. For example, there is no written description support for using, e.g., a "solid layer" comprising all types of compounds containing both silicon and oxygen such as, e.g., various forms of silica, silicates, or silicones. The claims of at least the application that led to the '768 Patent itself also do not provide written description support for these features of the Asserted Claims. For example, none of the original 20 claims that were submitted with the original

MYW Semitech Exhibit 2017
TSMC and Apple v. MYW Semitech - IPR2026-00067

application for the ’768 Patent recited, e.g., a “solid layer.” Additionally, all the originally-filed claims in the application issuing as the ’768 Patent were canceled and new, substantially different claims were added. *See* ’768 File History at APL-SEMITECH_00531986 at 2112-2118 (Jan. 26, 2020), APL-SEMITECH_00531986 at 2200-2207 (March 8, 2020 claims).

The specifications of the Asserted Patents also do not enable a POSITA to practice the full scope of these limitations. This broader scope thus now encompasses a much broader genus of materials including all glass, polymer, or “solid” materials comprising silicon and oxygen. Myriad such materials exist, and the Asserted Patents contain no disclosure demonstrating that the named inventor possessed or how to implement the full scope of those claims. For example, the specification does not provide a starting point or guidance for how to test all such potential materials, and provides no guidance on how to practice the Asserted Claims using the numerous different materials encompassed by the Asserted Claims. A person of ordinary skill would not have been able to implement the full scope of these limitations without undue experimentation.

Second, as another example, the Asserted Claims have been broadened to encompass chip-first manufacturing processes in which a chip is first placed and then a substrate or solid layer is then formed around the chip. The claims of the Asserted Patents have been drafted such that, contrary to the disclosure of the specification, chips can be placed within the substrate or solid layer, and not merely above or below the substrate or solid layer. For example, the Asserted Claims are each drafted to recite an “interconnection scheme” that is “above” both (1) a “first surface” of a “solid layer” or “substrate” (e.g., above the top surface of the solid layer or substrate) and (2) a component such as a “metal bump,” “semiconductor chip,” or “passive component.” The Asserted Claims do not, however, recite the arrangement of these components relative to the solid layer or substrate itself. As a result, the Asserted Claims encompass embodiments in which such a

MYW Semitech Exhibit 2017
TSMC and Apple v. MYW Semitech - IPR2026-00067

component is within the substrate or solid layer itself: because the solid layer or substrate is below the interconnection scheme, anything within the solid layer or substrate (including, e.g., components within that solid layer or substrate) is also below the "interconnection scheme." Indeed, throughout the claim charts attached to Semitech's Initial Infringement Contentions, Semitech repeatedly alleges that several limitations of the claims are met by components that are within the alleged solid layer or substrate, and not above or below it.

There is no written description support for the scope of the Asserted Claims encompassing chip-first processes in which chips and other components are within the solid layer or substrate. The specifications of the Asserted Patents disclose only chip-last processes in which a substrate is first formed, and then chips and other components are placed above or below the substrate. Every figure in the specifications of the Asserted Patents, and the patents to which they claim priority, relating to the arrangement of a chip and a substrate discloses those chips and components being either above or below the substrate in a chip-last manufacturing process. *See, e.g.*, '453 Patent, Figs. 18u-v, 18x-y, 21-23; '310/'768/'763/'306 Figs. 9t-u, 9w-x, 12-17a (the Asserted Patents each are continuations of, and contain only the same disclosures as, the '310 Patent).

Prior to the filing of the '768 Patent, the earliest of the three Asserted Patents, the claims of each of patents to which the Asserted Patents claim priority likewise were directed to chip last processes. For example, '453 Patent claim 1 recites a "glass substrate" with a "metal layer" below it, connected using a conductor through the substrate to a "first chip" on top of the substrate. '453 Patent claim 3 recites a "second chip" in addition to the first chip on top of the substrate. And '453 Patent claim 4 recites a "second chip" over the top surface of the substrate and an "electronic component under" the bottom "surface." Each of the other claims of the '453 Patent that recite additional components or chips similarly recites that those chips are above the top surface, or below

MYW Semitech Exhibit 2017
TSMC and Apple v. MYW Semitech - IPR2026-00067

the bottom surface, of the substrate. Similarly, ’310 claim 1 recites that the first chip is “bonded and under said first glass substrate” (claim 1), and a second chip is “under said second glass substrate” (claim 10).

Accordingly, the specifications of both the ’453 Patent and ’310 Patent to which the Asserted Patents claimed priority did not provide written description support for chip-first manufacturing processes as encompassed by the Asserted Claims. The originally-filed claims of at least the ’768 Patent likewise do not provide written description support for such chip-first manufacturing technologies because, e.g., the originally-filed claims were substantially different, and were later canceled and replaced with a new claim set by the Applicant. *See* ’768 File History at APL-SEMITECH_00531986 at 2112-2118 (Jan. 26, 2020), APL-SEMITECH_00531986 at 2200-2207 (March 8, 2020 claims).

The Asserted Patents also do not provide sufficient enabling disclosure for this broader scope of the Asserted Claims. The Asserted Patents disclose only embodiments in which components are placed on either side of the substrate itself. A person of ordinary skill would not have been able to implement the full scope of these limitations without undue experimentation because the process of performing chip-first manufacturing of semiconductor packaging is a substantially different process from chip-last manufacturing processes. For example, this inverted process may require, e.g., a different process flow, the use of different materials, different types of interconnects, and/or different individual processing steps in order to ensure the device is properly fabricated such that it both does not fail during the manufacturing process and results in a product that operates as intended. A POSITA would not have been able to implement such chip-first manufacturing processes without undue experimentation.

MYW Semitech Exhibit 2017
TSMC and Apple v. MYW Semitech - IPR2026-00067

Third, as another example, the Asserted Claims have been broadened to encompass multiple ways to create interconnections or vias through the device. Several of the Asserted Claims recite a "metal plug" in a "through via," as well as multiple layers in those vias including a layer "contacting a sidewall" of the via. *E.g.*, '768 Patent Claims 1, 16; '763 Patent, Claim 1; '306 Patent, Claim 10. As drafted however, there are at least two ways to form such vias encompassed by the Asserted Claims: (1) forming the metal plugs themselves, and then filling the substrate or solid layer around those plugs; and (2) forming the substrate or solid layer, then forming holes in the substrate or solid layer into which metal plugs are formed. The specifications do not contain written description support to show that the named inventor actually possessed the full scope of the Asserted Claims.

Additionally, the disclosure of the Asserted Patents would not have enabled a POSITA to form vias in both ways encompassed by the Asserted Claims. Indeed, especially in view of, and in addition to, the chip-first vs. chip-last process issues discussed above, this limitation further requires multiple ways of forming such vias, including both by forming the vias prior to formation of the substrate or solid layer, as well as placing such vias and plugs into already-formed substrates or solid layers, including such layers that may already have certain components embedded within them. A person of ordinary skill would not have been able to implement the full scope of these limitations without undue experimentation.

As a result, in view of the at least the above deficiencies in the disclosures of the Asserted Patents, both individually and collectively, the Asserted Claims lack sufficient enablement and written description support.

As noted above in Sections I-II, Semitech has declined to provide any basis for its allegation that the Asserted Claims are entitled to claim priority to the alleged September 26, 2012

MYW Semitech Exhibit 2017
TSMC and Apple v. MYW Semitech - IPR2026-00067

priority date. For example, Semitech has declined to provide any contentions regarding alleged written description and/or enablement support. To the extent that Semitech later takes the position that any Asserted Claim is entitled to a priority date other than September 26, 2012 or provides any support for its allegations, Apple reserves the right to supplement these contentions. For example, to the extent that any Asserted Claim is entitled to a priority date on or after September 11, 2016, Apple's accused A10 chip was launched before that date, Semitech has alleged in its Initial Infringement Contentions that the A10 chip infringes for the same reasons as all Accused Products, and thus to the extent there is any infringement, the A10 chip would invalidate the claims for the same reasons.

V. INVALIDITY RELATING TO IMPROPER INVENTORSHIP

The Asserted Claims are invalid for various reasons relating to the inventorship of the Asserted Patents and related patents. Defendant incorporates by reference as if fully set forth herein the contentions, arguments, and factual underpinnings from: (1) Defendant's Answer (D.I. 19), including any associated exhibits; and (2) all documents filed in IPR2026-00065, IPR2026-00066, and IPR2026-00067, including without limitation Defendant's IPR petitions and any forthcoming briefing, including the discussions therein of issues relating to the inventorship of the Asserted Patents. For example, on information and belief, the named inventor of the Asserted Patents, Ping-Jung Yang, was working with others, including at least Mou-Shiung Lin, Jin-Yuan Lee, Hsin-Jung Lo, Te-Sheng Liu, and Chiu-Ming Chou when the concepts for the Asserted Patents were allegedly conceived and/or reduced to practice. *See, e.g.*, U.S. Patent Nos. 9,612,615, 12,176,278; U.S. Patent Pub. Nos. 2010/0246152, 2012/0193785. On information and belief, at least one or more of these other persons conceived of and/or reduced to practice various aspects of the alleged inventions of the Asserted Claims and therefore should have been named an inventor thereof. Because these individuals were not named, and even if the Asserted Patents are entitled to priority

MYW Semitech Exhibit 2017
TSMC and Apple v. MYW Semitech - IPR2026-00067

dates before March 16, 2013, the Asserted Patents are invalid for incorrect inventorship under 35 U.S.C. §§ 101, 102(f), 102(g)(2), and/or 115(a).

VI. LACK OF PATENTABLE SUBJECT MATTER UNDER 35 U.S.C. § 101

Based upon Semitech's apparent interpretations of the claims and its alleged infringement theories set forth in, e.g., Semitech's January 9, 2026 Initial Infringement Contentions, the Asserted Claims are invalid under 35 U.S.C. § 101 because the claims are not directed to patentable subject matter. A claim is patent-eligible if it recites a "new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof." 35 U.S.C. § 101. In *Alice*, the Supreme Court reaffirmed the two-step framework used to "distinguish[] patents that claim laws of nature, natural phenomena, and abstract ideas from those that claim patent-eligible applications of those concepts." *Alice Corp. Pty., Ltd. v. CLS Bank Int'l*, 573 U.S. 208, 217 (2014). This framework requires determining (1) if the claim is directed to ineligible subject matter such as an abstract idea, and, if so, (2) whether the remainder of the claim recites sufficient inventive elements that amount to "significantly more" than the abstract idea identified in Step 1. *Id*.

At least under Semitech's apparent interpretation of the Asserted Claims, the Asserted Claims are invalid under 35 U.S.C. § 101 because the claims are not directed to patentable subject matter. For example, at *Alice* step one, under Semitech's apparent interpretation, each of the Asserted Claims is directed to nothing more than the abstract idea of, e.g., stacking connected components in a device.

At *Alice* step two, under Semitech's apparent interpretation of the Asserted Claims, once the abstract ideas are removed from the Asserted Claims, none of what remains recites anything inventive—such as new components, or a technological improvement to the functioning of the recited conventional components—that might transform the claims into patent-eligible subject

MYW Semitech Exhibit 2017
TSMC and Apple v. MYW Semitech - IPR2026-00067

matter. To the extent the Asserted Claims recite components at all, those components are conventional, and the claims recite them to perform only their conventional functions. For example, as set forth in the Admitted Prior Art and Exhibits A-D and S1-S5 (including Exhibits A0, B0, and C0), each and every claim limitation of the Asserted Patents, taken individually and/or collectively, is well-understood, routine, and conventional, and known in the prior art as set forth therein.

Defendant's investigation regarding the invalidity of the Asserted Claims under 35 U.S.C. § 101 is ongoing, and the parties have not yet entered the claim construction phase of the litigation. Defendant reserves the right to supplement or amend its invalidity contentions based on 35 U.S.C. § 101 in light of further investigation and discovery, the Court's construction of the claims at issue, and/or review and analysis of expert witnesses.

VII. DOCUMENT PRODUCTION ACCOMPANYING INVALIDITY CONTENTIONS

As required by the Scheduling Order and Delaware Default Standard for Discovery, Apple has produced each item of prior art identified that does not appear in the file history of the Asserted Patents—those items of prior art are Bates numbered as APL-SEMITECH_00528533 - APL-SEMITECH_00553135.

Subject to all reservation of rights and objections set forth herein, and/or after Semitech's identification of all accused devices with specificity, Apple further reserves the right to supplement its document production pursuant to the Scheduling Order and Federal Rules of Civil Procedure.

MYW Semitech Exhibit 2017
TSMC and Apple v. MYW Semitech - IPR2026-00067

Respectfully submitted,

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MYW Semitech Exhibit 2017
TSMC and Apple v. MYW Semitech - IPR2026-00067

CERTIFICATE OF SERVICE

I, Daniel W. Richards, hereby certify that on March 5, 2026, true and correct copies of the within document were served on the following counsel of record at the addresses and in the manner indicated:

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