

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TAIWAN SEMICONDUCTOR
MANUFACTURING COMPANY LTD. and APPLE INC.,
Petitioners,

v.

MYW SEMITECH, LLC,
Patent Owner.

Case No. IPR2026-00067
U.S. Patent No. 11,894,306

DECLARATION OF DAVID S. RICKETTS

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PATENT OWNER'S EXHIBIT LIST

Exhibit No.	Description
2001	U.S. Patent No. 9,615,453
2002	Information Disclosure Statement for U.S. Application No. 17/929,180 dated December 21, 2023
2003	[SEALED] Email chain between Richard Juang, counsel for MYW Semitech, and Daniel Richards, counsel for Apple Inc., regarding production of materials
2004	[SEALED] Defendant Apple Inc.'s First Supplemental Responses to Plaintiff MYW Semitech, LLC's First Set of Interrogatories (Nos. 1-12)
2005	[SEALED] Email chain between Richard Juang, counsel for MYW Semitech, and Daniel Richards, counsel for Apple Inc., regarding availability of source code
2006	[SEALED] Email chain between Richard Juang and Peter Yang, counsel for TSMC, regarding inventorship.
2007	Oral Order for Motion to Stay Pending <i>Inter Partes</i> Review, <i>MYW Semitech, LLC v. Apple Inc.</i> , 1-25-cv-00504 (DDE) Dkt. 68 (January 21, 2026)
2008	Stipulation and [Proposed] Order to Amend Scheduling Order, <i>MYW Semitech, LLC v. Apple Inc.</i> , 1-25-cv-00504 (DDE) Dkt. 58 (December 3, 2025)
2009	Apple Inc.'s Infringement Contentions, <i>MYW Semitech, LLC v. Apple Inc.</i> , 1-25-cv-00504 (DDE) (January 9, 2026)
2010	Agreed Stipulation Regarding the Discovery of Electronically Stored Information, <i>MYW Semitech, LLC v. Apple Inc.</i> , 1-25-cv-00504 (DDE) Dkt. 39 (October 14, 2025)
2011	Revision to Rules of Practice Before the Patent Trial and Appeal Board, 90 Fed. Reg. 48,335 (proposed Oct. 17, 2025) (to be

	codified at 37 C.F.R. pt. 42).
2012	Declaration of Richard Juang
2013	Default Protective Order
2014	Apple Inc.'s Proposed Constructions in <i>MYW Semitech, LLC v. Apple Inc.</i> , C.A. No. 25-504-RGA-EGT (Feb. 12, 2026)
2015	Joint Claim Construction Chart in <i>MYW Semitech, LLC v. Apple Inc.</i> , C.A. No. 25-504-RGA-EGT (Feb. 26, 2026)
2016	Defendant Apple Inc.'s Answering Claim Construction Brief
2017	Defendant Apple Inc.'s Initial Invalidity Contentions (Cover Document)
2018	Declaration of Professor David S. Ricketts
2019	CV of Professor David S. Ricketts
2020	Deposition Transcript of Stanley Shanfield, Ph. D., dated July 14, 2026.
2021	<i>Coefficient of Thermal Expansion (CTE)</i> , BYU Integr. Microfabrication Lab, https://cleanroom.byu.edu/cte_materials (last visited Aug. 6, 2026).
2022	Rogers Corp., <i>ULTRALAM® 3000 Liquid Crystalline Polymer Circuit Material</i> , Double-Clad Laminates, Data Sheet No. RF1.3000, Publication No. 92-125 (rev. May 10, 2011).
2023	J. Yoon et al, "Enhancing bonding strength of the electroplated Cu pillars for semiconductor package by controlling grain orientation," Scientific Reports (2026).
2024	<i>Excerpts from CRC Handbook of Chemistry and Physics</i> , 2005, < http://www.hbcpnetbase.com >, CRC Press, Boca Raton, FL, 2005.

I have personal knowledge of the facts set forth in this declaration and, if called to testify as a witness, would testify under oath as follows:

I. BACKGROUND

1. I have been retained as an expert by MYW Semitech, LLC (“Semitech”) in the above-captioned matter (IPR2026-00067).

2. I have been asked by Semitech to provide my expert opinion regarding the patentability of claims 1-27 of U.S. Patent No. 11,894,306 (“the ’306 Patent”) in view of the grounds asserted in IPR2026-00067. For the reasons set forth below, it is my opinion that claims 1-27 of the ’306 Patent are patentable over the grounds asserted in IPR2026-00067.

II. PROFESSIONAL QUALIFICATIONS

3. I am currently Full Professor of Electrical and Computer Engineering at North Carolina State University (“NCSU”), a position I have held since 2012. In this position, I conduct research and teach undergraduate and graduate students in the field of electrical and computer engineering. My professional career spans approximately three decades and encompasses both industry and academic experience in the design, development, testing, and management of power electronics and power conversion systems, including uninterruptible power supplies (“UPS”), AC-DC converters, DC-DC converters, DC-AC converters,

battery charging and battery management systems, and power management integrated circuits (“ICs”).

4. The courses I teach at NCSU include Advanced Analog Integrated Circuit (“IC”) Design, Radio System Design, Analog Circuit Laboratory, and Power Management IC Design. My Power Management IC Design course addresses the design and analysis of power conversion circuits and the integrated circuits that control them, including the converter topologies, control circuits, feedback systems, and protection circuits that are foundational to AC-DC and DC-DC power conversion products. In teaching these courses, I instruct students in the same fundamental principles of power conversion, regulation, and control that I applied throughout my industry career designing UPS systems and power converters.

5. At NCSU, I lead a research group that conducts research on and designs electrical and electronic circuits, including millimeter wave and microwave circuits and systems, radio frequency identification (“RFID”) circuits, wireless power transfer circuits, power management controllers, DC-DC and AC-DC converters, analog circuits, and radio frequency (“RF”) circuits. A substantial portion of my research program is devoted to power electronics and power conversion. I lead research in power electronics and power conversion integrated circuits, and my group designs power management systems that include both

integrated circuits and discrete power converters. This work involves the same classes of circuits found in commercial power conversion products, including switching converters, rectification circuits, regulation and control loops, and battery charging circuitry.

6. My research group at NCSU also designs microcontroller-based Bluetooth systems and other mixed-signal RF/digital systems. This work requires the integration of digital control, embedded firmware, and analog and power circuitry within a single system, which is the same engineering discipline required to design microcontroller-supervised power conversion products such as UPS systems, battery chargers, and power management controllers.

7. Prior to my current position, I served as an Assistant Professor of Electrical and Computer Engineering and Assistant Professor of Materials Science and Engineering at Carnegie Mellon University from 2006 to 2012, where I likewise conducted research and taught in the areas of circuits and systems.

8. I received my B.S. and M.S. degrees in Electrical Engineering from Worcester Polytechnic Institute in Worcester, Massachusetts, in 1995 and 1997, respectively. I received my Ph.D. in Electrical Engineering from Harvard University in Cambridge, Massachusetts, in 2006.

9. Throughout my doctoral studies and academic career, I have personally worked hands-on in the cleanroom and semiconductor fabrication

facilities at Harvard University, Carnegie Mellon University, and North Carolina State University. In these facilities, I fabricated, processed, and characterized semiconductor devices and nanoscale structures, gaining direct experience with semiconductor processing techniques, including lithography, thin-film deposition, etching, surface preparation, and metrology, as well as the handling, mounting, and characterization of semiconductor die and wafers.

10. Prior to entering academia, I spent approximately eight years as an engineer in private industry, holding several engineering and managerial positions in which I developed, and oversaw the development of, electrical and electronic circuits, including those related to power transfer, power conversion, and semiconductor design in wired and wireless circuits and systems. The core of my industry career was the design and development of power conversion products — in particular, uninterruptible power supplies and the AC-DC, DC-DC, and DC-AC converters within them, as well as the power management integrated circuits that control such converters.

11. From 1995 to 1999, I held positions as an engineer and senior engineer at American Power Conversion (“APC”), which at the time was one of the world’s leading manufacturers of uninterruptible power supplies. At APC, I personally designed AC-DC and DC-DC converters for use in APC’s UPS products.

12. As a design engineer at APC, I designed and tested complete uninterruptible power supply products. The UPS products I worked on were complex, multi-converter power systems: each contained an AC-DC converter to rectify and convert incoming AC line power, a DC-AC converter (inverter) to synthesize AC output power from the internal battery, DC-DC conversion stages, and an embedded microcontroller that supervised the operation of the system, including monitoring line conditions, managing the transfer between line power and battery power, controlling battery charging, and implementing protection functions. My work on these products encompassed circuit design, prototyping, testing, and validation of the power conversion stages and their interaction with the supervisory microcontroller.

13. Through this work at APC, I gained direct, hands-on experience with the full range of engineering issues involved in AC-DC converter design, including rectification, power factor considerations, switching converter topologies, transformer and magnetics design, feedback and regulation, component selection and stress analysis, thermal design, protection circuitry, and safety and regulatory requirements applicable to products that connect to the AC mains.

14. While at APC, I also headed the battery technology group. Batteries are the energy storage element at the heart of every UPS, and the charging, monitoring, and health assessment of the battery are central to UPS product

performance and reliability. In leading the battery technology group, I developed models for battery health that could be adapted into microcontroller-based systems, allowing a UPS or similar product to assess the condition of its battery in real time using its embedded controller. This work required detailed understanding of battery charging circuits and algorithms, battery discharge behavior, and the integration of battery management functions into microcontroller firmware and supervisory control.

15. From 1999 to 2001, I held a position as a Principal Consultant at Renaissance Design, Inc., where I designed power management ICs. Power management ICs are the integrated circuits that implement the control, regulation, drive, and protection functions of power converters, including AC-DC and DC-DC converters and battery chargers. In this role I was responsible for circuit design at the silicon level for such devices.

16. From 2000 to 2002, I held a position as Manager of New Product Development at ON Semiconductor Corp., a major manufacturer of power management semiconductors. In that position, I was responsible for six product development teams and oversaw the development of over twenty power management ICs in bipolar, CMOS, and BiCMOS technologies. The products developed under my direction included controllers for power conversion applications. My group designed power management controllers and built

application boards for battery chargers and buck converters. Buck converters are a fundamental class of DC-DC converter, and battery charger circuits are a core building block of battery-powered and battery-backed products, including UPS systems, portable power products, and consumer electronics.

17. In overseeing these product development teams at ON Semiconductor, my responsibilities extended beyond circuit design to the full product development cycle for power management semiconductors, including product definition, design reviews, silicon validation, application board development and bench evaluation, and support of customers designing the ICs into end products such as battery chargers and DC-DC converter power stages.

18. From 2002 to 2003, I held the position of Advanced System Engineering Manager at ON Semiconductor Corp., where I directed a team of system engineers developing multi-phase power management ICs for Intel and AMD microprocessors. Multi-phase power management ICs control multi-phase buck (DC-DC) converters that deliver tightly regulated, high-current power to microprocessors, and their design requires expertise in converter topology, current sharing and balancing among phases, feedback control, and transient response.

19. Taken together, my industry experience includes the design and testing of complete UPS products; the design of the AC-DC, DC-DC, and DC-AC converter stages within such products; leadership of battery technology

development, including battery charging and microcontroller-based battery health monitoring; the silicon-level design of power management ICs; and the management of engineering teams developing power management controllers, battery chargers, and DC-DC converter products.

20. My academic research and teaching have continued and deepened this expertise. At NCSU, my group designs power management systems, including integrated circuits as well as discrete power converters, and designs microcontroller-based systems in which embedded controllers supervise analog and power circuitry — the same architecture used in UPS systems, battery chargers, and other microcontroller-supervised power conversion products.

21. A substantial portion of my academic research has been devoted to nanofabrication and nanoscale devices — that is, the fabrication, characterization, and application of structures and devices with dimensions on the nanometer scale. At Carnegie Mellon University, I led research on Tip-directed, Field-emission Assisted Nanofabrication (“TFAN”) as part of the DARPA Tip-Based Nanofabrication (TBN) program, in collaboration with Professors Bain, Carley, Davis, Fedder, Sitti, and Islam. This research used tip-directed, field-emission-assisted chemical vapor deposition (CVD) for the precise fabrication of structures on the nanometer scale, in which device geometry is determined by probe manipulation and controlled energy delivery at the probe tip, enabling control of

the length, width, orientation, and height of nanoscale structures during fabrication. The work included the deposition of silicon nanowires by using field-emitted electrons to locally crack adsorbed silane (SiH_4) and disilane (Si_2H_6), and methods for localized surface preparation, including targeted desorption of hydrogen on hydrogen-terminated silicon substrates to localize silane adsorption. This research required extensive hands-on work with scanning tunneling microscopes (STM), atomic force microscopes (AFM), ultra-high vacuum systems, and semiconductor surface preparation and characterization.

22. My nanofabrication research has resulted in numerous peer-reviewed publications and presentations. Representative journal publications relating to nanofabrication and nanoscale devices include:

- W. Hu, J. Bain and D. S. Ricketts, “An AFM/STM multi-mode nanofabrication approach allowing in situ surface modification and characterization,” *Micro and Nano Letters*, vol. 8, pp. 43–46, Jan. 2013.
- W. Hu, J. A. Bain and D. S. Ricketts, “In-situ quantification of electrical isolation in STM-fabricated TiO_x nanostructures,” *Micro and Nano Letters*, vol. 7, no. 4, pp. 334–336, Apr. 2012.
- O. Ozcan, W. Hu, M. Sitti, J. Bain, and D. S. Ricketts, “Investigation of tip current and normal force measured simultaneously

during local oxidation of titanium using dual-mode scanning probe microscopy,” *Micro & Nano Letters*, vol. 9, no. 5, pp. 332–336, May 2014.

- D. S. Ricketts, J. A. Bain, Y. Luo, S. Blanton, K. Mai and G. K. Fedder, “Enhancing CMOS using nanoelectronic devices, a perspective on hybrid integrated systems,” *Proceedings of the IEEE*, vol. 98, no. 12, pp. 2061–2075, Dec. 2010.

- M. E. Karagozler, S. C. Goldstein and D. S. Ricketts, “Scalable self-assembly process for the fabrication of sub-millimetre three-dimensional cylindrical tubes,” *IET Micro & Nano Letters*, vol. 11, no. 1, pp. 4–8, 2016.

- R. S. Friedman, M. C. McAlpine, D. S. Ricketts, D. Ham, and C. M. Lieber, “High-speed integrated nanowire circuits,” *Nature*, vol. 434, p. 1085, Apr. 2005.

23. Representative peer-reviewed conference publications and presentations relating to nanofabrication and nanomanufacturing include:

- J. R. Smith, W. Hu, Y.-Y. Dang, O. Ozcan, M. Sitti, J. A. Bain, D. S. Ricketts, and R. Davis, “Scanning Probe Nanomanufacturing on Si: Surface Characterization of the Process Technique,” *Materials Research Symposium*, paper G1.5, Nov. 2010.

- J. R. Smith, W. Hu, Y. Y. Dang, O. Ozcan, M. Sitti, J. Bain, R. Davis and D. S. Ricketts, “Writing Si nanowires on Si (100) with an STM tip: surface preparation and initial results,” Materials Research Symposium, M11.50, Boston, MA, Nov. 2009.
- J. R. Smith, et al. (with D. S. Ricketts), Proc. SPIE 7637, Alternative Lithographic Technologies II, 76371D (2010) (scanning-probe-based nanofabrication on silicon).
- W. Hu, J. Gu, Z. George and D. S. Ricketts, “Directed scanning probe nanomanufacturing of lateral Ti-TiO₂-Ti junctions for low capacitance MIM rectenna diodes,” Micro and Nano Engineering Conf., Berlin, Sept. 2011.
- W. Hu, Y. Tang, Y. Zhang, J. Gu, S. Tamaru, J. A. Bain, L. R. Carley, R. F. Davis, G. K. Fedder and D. S. Ricketts, “Ti/TiO₂ nanodevice fabrication using compliant probes and CMOS probe-arrays,” Technologies for Future Micro-Nano Manufacturing, Napa Valley, CA, Aug. 2011.
- W. Hu, S. Tamaru, J. A. Bain and D. S. Ricketts, “High Current Pulse Generation for Thermal Surface Modification using Standard STM,” Int. Conf. Electron, Ion, Photon Beam Technology and Nanofabrication, May 2011.

- J. R. Smith, D. S. Ricketts and J. A. Bain, “Localized thermal modification of surfaces via pulsed electron bombardment from an STM tip,” Int. Conf. Electron, Ion, Photon Beam Technology and Nanofabrication, May 2011.
- W. Hu, J. A. Bain and D. S. Ricketts, “In-situ characterization using AFM probes in multiple modes,” Int. Conf. Electron, Ion, Photon Beam Technology and Nanofabrication, May 2012.
- O. Ozcan, W. Hu, M. Sitti, J. A. Bain and D. S. Ricketts, “Experimental Investigation of Force, Conduction and Growth in Nano-oxidation using scanning probe microscopy,” Enabling Nanomanufacturing for Rapid Innovation, Aug. 2013 (Best Poster).
- D. S. Ricketts, T. Schlesinger, Y. Luo and J. Bain, “Materials and Devices for Hybrid CMOS Circuits: Expanding the Functionality of Nanoscale CMOS,” Nano-DDS Conference, Ft. Lauderdale, FL, Oct. 2009 (Invited).

24. During my doctoral research at Harvard University, I collaborated with the research group of Professor Charles Lieber, a leading group in nanowire synthesis, on the design and characterization of high-speed integrated nanowire circuits. This work, published in Nature (R. S. Friedman, M. C. McAlpine, D. S. Ricketts, D. Ham, C. M. Lieber, “High-speed integrated nanowire circuits,”

Nature, vol. 434, p. 1085, Apr. 2005), demonstrated integrated circuits built from semiconductor nanowires and required detailed understanding of nanoscale semiconductor devices, their fabrication, and their integration into functional circuits.

25. My research has also included nanoscale magnetic and spintronic devices, including spin-torque nano-oscillators and magnetic tunnel junctions with dimensions below 30 nanometers. This work was supported in part by my 2008 DARPA Young Faculty Award, “Spin-torque Oscillators for Spectrum-Agile RF,” and involved the fabrication and characterization of nanoscale magnetic devices, including spin-transfer-torque switching of magnetic tunnel junctions using conductive atomic force microscopy. Representative publications include: S. Tamaru and D. S. Ricketts, “Measurement of ultra-low power oscillators using adaptive drift cancellation with applications to nano-magnetic spin torque oscillators,” Review of Scientific Instruments, vol. 84, p. 054704, May 2013; E. R. Evarts, L. Cao, D. S. Ricketts, N. D. Rizzo, J. A. Bain, and S. A. Majetich, “Spin transfer torque switching of magnetic tunnel junctions using a conductive atomic force microscope,” Applied Physics Letters, vol. 95, 132510 (2009); E. R. Evarts, L. Cao, D. S. Ricketts, N. D. Rizzo, J. A. Bain, and S. A. Majetich, “Characterization of conducting atomic force microscopy for use with magnetic tunnel junctions,” IEEE Transactions on Magnetics, vol. 46, no. 6, pp. 1741–1744,

June 2010; and E. R. Evarts, et al., “Spin Torque Switching of 26 nm Diameter Magnetic Tunnel Junction Using a Conductive Atomic Force Microscope,” Conference on Magnetism and Magnetic Materials, paper FC-13, Nov. 2010.

26. I have been recognized as a leader in the field of nanofabrication and nanomanufacturing. I served as Technical Program Chair of the Enabling Nanomanufacturing for Rapid Innovation TRC/NSF Workshop in August 2013, and delivered the keynote address, “Enabling Rapid Innovation in Nanomanufacturing,” at the ENRI NSF workshop in Napa, California in August 2013. I served as Session Chair for Nanotechnology at the CMOS Emerging Technologies Conference (Banff, Canada, 2009) and at the NANO-DDS conference (2011). I have also given invited presentations on nanofabrication at the National Institute of Standards and Technology (NIST) (“Tip-directed, Field-assisted Nanofabrication,” Mar. 2011), Zyvex Corp. (“Tip-assisted, field emission nanofabrication,” Apr. 2010), Worcester Polytechnic Institute (“Tip-assisted Nanofabrication,” Mar. 2010), and the Army Research Laboratory (“Nanoscale magnetism for integrated power conversion and RF,” Jan. 2011).

27. In recognition of my research, I received the National Science Foundation Faculty Early Career Development (CAREER) Award, one of the NSF’s most prestigious awards in support of early-career faculty, as well as the DARPA Young Faculty Award (2008).

28. My research has also encompassed advanced semiconductor packaging at the micro- and nanoscale. As part of the DARPA Efficient Linearized All-Silicon Transmitter ICs (“ELASTx”) program — a program directed at developing monolithic, high power-added-efficiency, high-linearity, millimeter-wave silicon-based transmitter ICs — I designed and built 100 GHz integrated packaging using liquid crystal polymer (LCP) substrates of 25 μm thickness, solder microbumps, and multi-layer metal interconnect. This advanced 3D packaging work involved semiconductor die mounting on substrates, including the use of solder balls and microbumps, and required detailed understanding of semiconductor die attachment, interconnect design, substrate materials, and the assembly and integration of semiconductor die into packaged systems.

29. I have published at least 49 academic journal papers, as shown in my curriculum vitae, relating to various topics including millimeter wave and microwave circuits and systems, RFID circuits, wireless power transfer circuits, analog circuits, and RF circuits.

30. I have also authored at least 78 conference articles, as shown in my curriculum vitae, relating to various topics including millimeter wave and microwave circuits and systems, RFID circuits, wireless power transfer circuits, analog circuits, and RF circuits.

31. In sum, I have approximately three decades of combined industry and academic experience in power electronics and power conversion, with particular depth in uninterruptible power supplies, AC-DC and DC-DC converter design, battery charging and battery management, and the power management integrated circuits that control such systems, as well as in analog, RF, and microcontroller-based mixed-signal systems, and in semiconductor fabrication, nanofabrication, nanoscale devices, and advanced semiconductor packaging.

32. My curriculum vitae, which includes a complete list of my qualifications and publications, is being filed as EX2019 in this IPR.

III. MATERIAL CONSIDERED

33. In preparing this declaration, I have reviewed the public papers and exhibits filed in this IPR to date, including the specification, claims and prosecution history of the '306 Patent, the Petition, the Declaration of Dr. Stanley Shanfield, the references asserted in the Petition, and the exhibits filed concurrently with this Declaration as part of the Patent Owner Response.

IV. LEGAL STANDARDS

34. I am not an attorney, and I have not independently researched the law. MYW's counsel has explained certain legal principles to me that I have relied on in forming my opinions set forth in this declaration. I have applied these legal

principles in arriving at my opinions expressed in this declaration. They are set forth below.

35. I have been informed and understand that an invention cannot be patented if the subject matter as a whole would have been obvious to a person of ordinary skill in the art at the time of the invention. Also, while the prior art is compared to each claim on an element-by-element basis, the claimed invention as a whole must have been obvious to one of ordinary skill in order for a claim to be invalid.

36. I understand that the fundamental question in analyzing obviousness is whether, at the time of the invention, the subject matter of the claimed invention as a whole would have been obvious to a person of ordinary skill in the art to which the subject matter pertains, taking into account: (a) the scope and content of the prior art; (b) the differences between the prior art and the claims at issue; (c) the level of ordinary skill in the art; and (d) any objective indicia of non-obviousness referred to as secondary considerations. The secondary considerations may include: (1) a long-felt but unmet need in the prior art that was satisfied by the claimed invention; (2) the failure of others; (3) skepticism; (4) commercial success of a product covered by the patent; (5) industry praise of the claimed invention; and (6) copying of the invention.

37. A combination of prior art references must teach or suggest all of the recited limitations of the claim for the invention to be found obvious.

38. It is important in the obviousness inquiry to identify whether a reason existed at the time of the invention that would have motivated a person of ordinary skill in the art in the relevant field to combine or modify the prior art references in the manner proposed by the petitioner so as to arrive at the claimed invention. Put another way, a finding of obviousness should be supported by an apparent reason to combine or modify the prior art references as proposed by the petitioner.

39. It is important in the obviousness inquiry to understand how the combination of references is supposed to work. An explanation of the operation of the combined references is often a prerequisite to showing that a person of ordinary skill in the art would have had an apparent reason to make the proposed combination and would have had a reasonable expectation of success.

40. A finding of obviousness requires the additional showing that a person of ordinary skill at the time of the invention would have selected and combined those prior art elements in the normal course of research and development to yield the claimed invention. In addition, a person of ordinary skill in the art should have had a reasonable expectation of success in combining the references as proposed.

41. In assessing obviousness, one must consider both the ordinary creativity and common sense of the person of ordinary skill in the art. I understand

that in *inter partes* reviews, it is impermissible for common sense to be applied to fill gaps in prior art that fails to teach or suggest a limitation of the claim.

42. Multiple references can be combined, with one another and/or with the knowledge of a person of ordinary skill in the art, in rendering a claim obvious. However, obviousness cannot be established by simply demonstrating that each element was independently known in the prior art. Rather, it may be necessary to identify a reason, such as a teaching, suggestion, or motivation, which would have prompted a person of ordinary skill in the art to combine the elements in the way the claimed invention does.

43. Obviousness cannot be established through hindsight. That means the claimed invention cannot be used as a roadmap to combine elements from different pieces of prior art, or different embodiments of a single prior art reference, to create the claimed invention. The claimed invention as a whole must be compared to the prior art as a whole, and one must avoid aggregating pieces of prior art through hindsight that would not have been combined absent the patent inventor's insight.

V. LEVEL OF ORDINARY SKILL IN THE ART

44. Petitioners allege the following level of ordinary skill:

A POSITA at the time of the '306 Patent would have had at least a bachelor's degree in electrical engineering, materials science, or physics (or an equivalent degree), and at least two years of experience in semiconductors or semiconductor manufacturing. A master's degree or Ph.D. in a relevant field may substitute for some work experience or vice versa. Additional education or experience might substitute for the above requirements.

Pet., 1. For the purposes of this declaration, I have applied Petitioners' level of ordinary skill.

45. For purposes of this declaration, I have applied a priority date of September 26, 2012. My opinions in this declaration regarding a POSITA assume a POSITA as of September 26, 2012. As of September 26, 2012, I was at least a POSITA.

VI. CLAIM CONSTRUCTION

46. Petitioners allege that claim construction is unnecessary for this IPR.
Pet., 2.

47. I agree that no construction is necessary for the claim terms except for the claim term "first region." For the term "first region," the prosecution history for the parent patent – U.S. Patent No. 11,538,763 ("the '763 Patent") – is relevant here. The application that issued as the '306 Patent is a continuation of the application that issued as the '763 Patent:

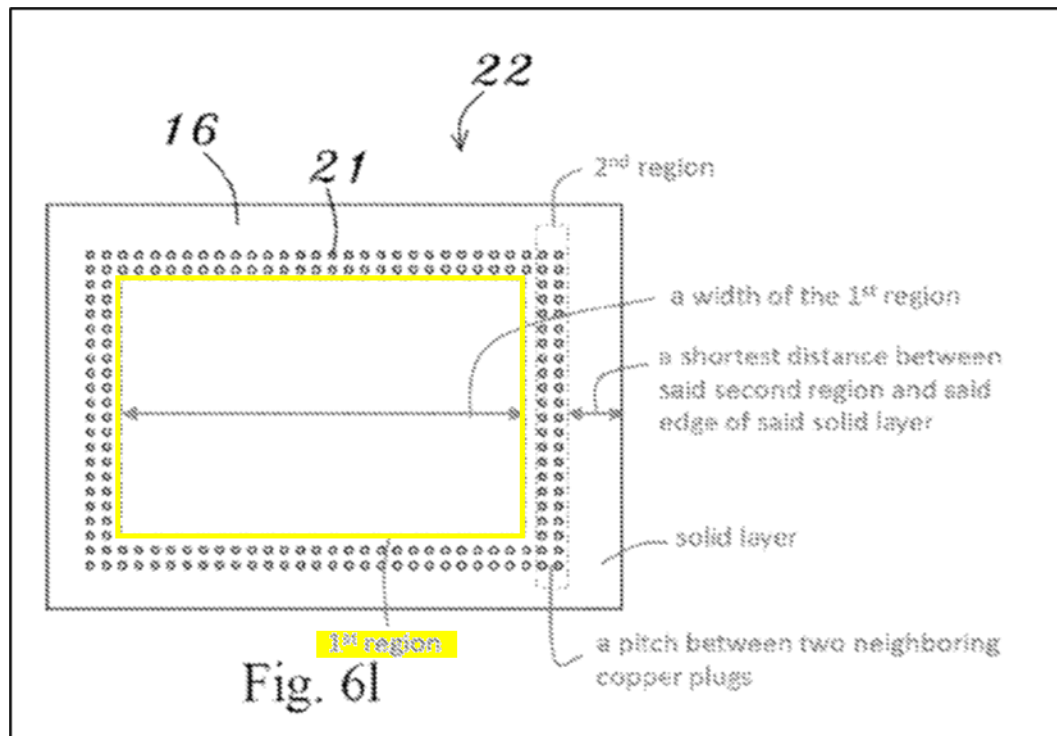
Related U.S. Application Data

(63) Continuation of application No. 17/372,459, filed on Jul. 11, 2021, now Pat. No. 11,538,763, which is a
(Continued)

EX1001 ['306 Patent], (63). The two patents appear to share substantially the same specification.

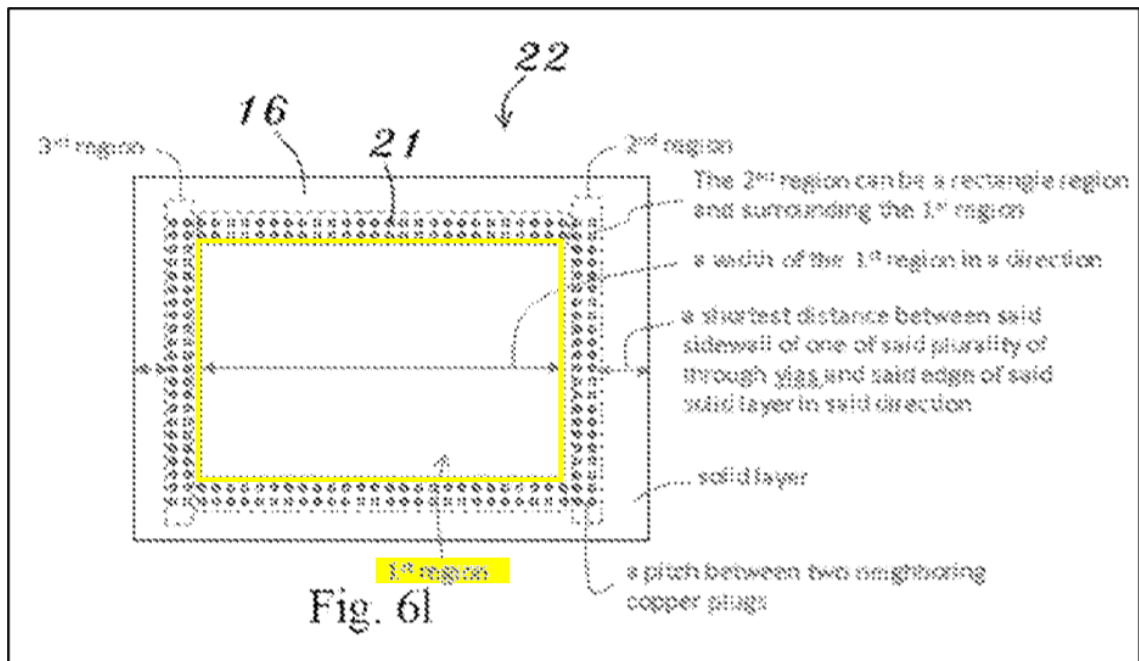
48. In my opinion, the prosecution history for the '763 Patent clearly and unmistakably disclaimed a first region that contains metal plugs/posts. During prosecution, the Applicant was clear that the “first region” is a region that does not include metal posts, and thus disclaimed any claim interpretation where the claimed “first region” includes metal posts.

49. During prosecution, the Applicant, relying on '763 Patent Figure 6l for support, identified that the claimed first region is the region inside the rectangle (yellow) of Figure 6l.



EX1117 [FH], 272. The annotation is clear that the 1st region has no metal plugs/posts.

50. In the amendments in Applicant's request for continued examination, the Applicant made the same point. Applicant again identifies the 1st region as the region in Figure 6l free of metal posts located inside of the rectangle (yellow).



Id., 360. Applicant cited only Figure 6l in support of this argument (*Id.*, 272, 360). Thus, the Applicant clearly and unambiguously intended the first region to be a region that does not include metal posts.

51. Other portions of the prosecution history support this disclaimer. For example, in a July 16, 2021 amendment, the Applicant replaced the term “central region” with the term “first region” in pending claims 1 and 16. EX1117 [FH], 241, 246. The Applicant cited only Figure 6l for support of this amendment. *Id.*, 246. Thus, Applicant clearly intended the first region to be the central region of Fig. 6l that does not include any metal posts. *Id.*

52. Claims 10 and 15 further confirm the Applicant’s meaning. Though claim 10 recites “a plurality of copper posts in a plurality of through holes in said second region” and claim 15 recites “said plurality of copper posts in said plurality

of through holes in said third region,” they do not claim any copper (or metal) plugs or posts in the *first* region. EX1001 [’306 Patent], cl. 10 and 15. Thus, the Applicant clearly intended the metal plugs/posts to be part of the second region and that the claimed first region be a region that is free from metal plugs/posts such as copper posts.

53. Claim 12 further confirms the disclaimer. Claim 12 requires “the chip package of claim 10, wherein no any copper post in said first region.” EX1001 [’306 Patent], cl. 12. Thus, claim 12 further confirms that the first region has no metal posts such as copper posts.

54. Accordingly, the intrinsic record is clear and unmistakable that the Applicant disclaimed a first region with any metal plugs/posts.

VII. TECHNOLOGY BACKGROUND

55. The following discussion reflects background knowledge and understanding that a POSITA would have possessed as of the priority date, based on my own education, training, and experience in the field of semiconductor design and packaging.

56. Though advances in transistor scaling have dramatically increased the computational capability of integrated circuits, no semiconductor chip operates in isolation. Every chip must communicate with the world outside it—with sensors, memory, other processors, power management circuitry, antennas, displays, or

other semiconductor devices. Reliably transmitting electrical signals, power, and heat between the circuits on a chip and its external environment has long been one of the most critical aspects of semiconductor packaging.

57. Semiconductor packaging serves primarily as a protective enclosure that provides electrical connections between a chip and the outside world. Over time, packaging has grown into a sophisticated engineering discipline that materially affects electrical performance, power efficiency, thermal management, manufacturing cost, and overall system capability. As transistor dimensions have continued to shrink while system complexity has increased, conventional packaging approaches reached practical and economic limits, which motivated the development of more advanced packaging technologies, including flip-chip assembly, wafer-level packaging, chiplet architectures, and three-dimensional integration.

58. One of the earliest, and still widely used, methods of connecting an integrated circuit to external circuitry is wire bonding. In wire bonding, the semiconductor die is mounted on a carrier substrate having relatively coarse conductive traces, and fine gold, aluminum, or copper wires are bonded between bond pads located around the perimeter of the die and corresponding traces on the substrate. Wire bonding became a mainstay of the industry because of its low production cost and high manufacturing yield.

59. Because wire bonds can only be formed to bond pads located around the edges of a die, the number of external connections that can be achieved scales approximately with the die's perimeter rather than its area. Since transistor count scales with die area while the number of available bond pads scales with perimeter, larger and more complex chips eventually became limited by the number of available input/output ("I/O") connections rather than by transistor density.

60. Wire bonds are also typically several millimeters long, and the inductance of a conductor of that length limits the speed, or bandwidth, of the signal that can be carried to and from the chip. Wire bonds are further susceptible to mechanical vibration and to thermal fatigue and stress incurred during encapsulation. Although wire bonding remains highly reliable for many applications, these characteristics make it increasingly disadvantageous for extremely high-frequency or high-power devices.

61. To address these limitations, the industry developed flip-chip packaging. Rather than wiring only the perimeter of the die, flip-chip technology fabricates solder bumps directly across the active surface of the chip. The die is then mounted face-down, or "flipped," onto the package substrate, so that connections are distributed across the entire surface of the chip rather than confined to its edges. Because the achievable I/O count in a flip-chip design scales

with chip area rather than perimeter, flip-chip packaging affords substantially higher interconnection density than wire bonding.

62. In a typical flip-chip implementation, solder bumps—commonly lead/tin alloy bumps formed on aluminum bond pads on the chip, sometimes referred to in the industry as C4 (“Controlled Collapse Chip Connection”) bumps—are reflowed to bond the chip face-down, along the shortest available path, to the package substrate. Because the resulting interconnects are far shorter than wire bonds, flip-chip bumps introduce substantially less parasitic inductance, enabling higher-speed signaling, and their shorter current paths and greater areal density reduce voltage drop and improve power distribution to increasingly power-hungry integrated circuits.

63. Flip-chip assemblies are also frequently underfilled: after the die is bonded, a polymer material—typically an epoxy resin loaded with fine silica or ceramic filler particles—is dispensed into the gap between the die and the substrate. Once cured, the underfill forms a rigid mechanical support around the solder bumps that improves the assembly’s resistance to thermal and mechanical stress.

64. Notwithstanding these advantages, flip-chip packaging presents its own challenges. Pre-bond testability and post-bond visual inspection of the concealed solder joints are difficult, and because the chip, the solder bumps, and

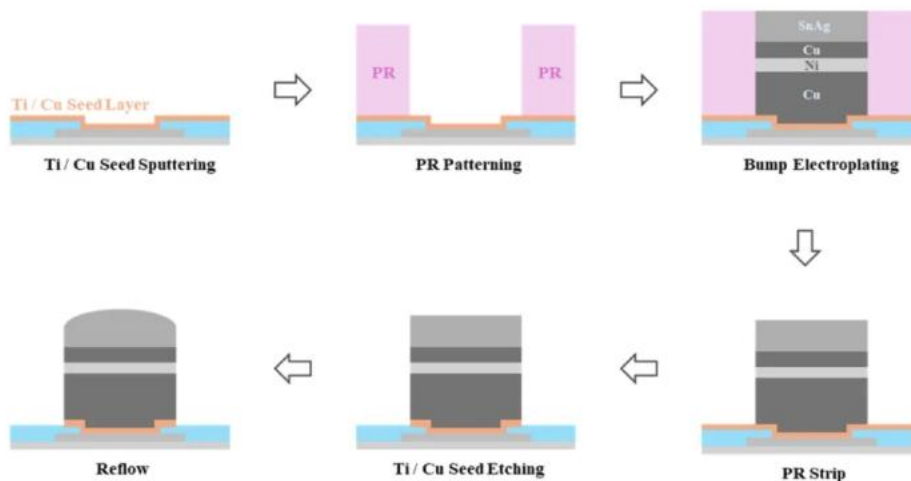
the package substrate are typically composed of different materials having different coefficients of thermal expansion (“CTE,” sometimes also referred to as “TCE”), repeated thermal cycling can fatigue and eventually fracture the solder joints unless the materials in the assembly are reasonably well CTE-matched.

65. Flip-chip packaging also did not eliminate every interconnect bottleneck. As integrated circuits came to require thousands of signal connections among processors, memory, analog circuitry, and power-management circuitry, conventional printed circuit board (“PCB”) technology was unable to keep pace with the interconnect density achievable on the chips themselves. Adding routing layers to a PCB increases both its thickness and the signal propagation delay between chips—a particular concern for high-speed communication between a processor and memory operating at multi-gigahertz clock frequencies.

66. To reduce interconnect length and increase routing density beyond what a conventional PCB can offer, the industry developed interposer-based, or “2.5D” integration, in which multiple dies are mounted side by side on an interposer rather than directly on a PCB. Because an interposer can be fabricated using photolithography and thin-film metallization, it supports far finer routing pitches than a PCB. Silicon has traditionally been used as an interposer material, although other materials—including glass—have also been used as interposer

substrates, offering potential advantages such as lower material cost and, depending on composition, a CTE that can be closely matched to silicon.

67. Dies are typically attached to an interposer using copper pillar bumps, or “microbumps,” which are generally smaller than conventional C4 solder bumps and are fabricated differently. Whereas a C4 bump is composed primarily of solder, a copper pillar consists mainly of electroplated copper with only a thin solder cap. Electroplating is an electrochemical process used to create the bulk part of the pillar. In this process all dies on a wafer are first covered by a uniform conductor layer, connected to a voltage source and immersed into an electrolyte containing copper ions. Copper ions receive electrons from copper atom on the surface of the wafer. The thin conductive layer is called a seed layer and is removed from the wafer after the process is completed. The process of the copper bump formation is schematically shown below. EX2023, 3.



68. Formation of a copper pillar directly on a bare dielectric, or on a dissimilar metal such as an aluminum bond pad, is often preceded by depositing a thin titanium, or similar, adhesion layer and a thin copper seed layer, on which the pillar is then electroplated. Sometimes a third layer containing TiN or TaN is added in between the adhesion and seed layers to block the Cu from unwanted diffusion in the material underneath. Deposition of adhesion, barrier and seed layers is an example of a broader family of wafer-level microfabrication. Although these layers may be deposited using the same technique, their metal composition and purpose is distinctively different. The choice of layers in such a sequence is typically driven by the specific materials present at the interface being built—for example, the poor adhesion of copper to a bare dielectric or oxide surface, or the tendency of certain dissimilar metal pairs, such as aluminum and copper.

69. These are real, well-studied phenomena, but they are specific to the particular materials being joined at a given interface—they are not a universal property of every metal-to-metal or metal-to-substrate contact. Where the metal already present at an interface is the same metal being added—for example, copper deposited on, or reflowed against, a surface that is already copper—neither the adhesion concern nor the interdiffusion concern described above is presented in the same way. In these cases, there is only a need for the seed layer because copper adheres readily to copper and there is no dissimilar-metal pair to interdiffuse.

70. Attaching a solder ball or solder bump to a metal pad is, in any event, a different kind of joining process altogether, with a different bonding mechanism than a thin film seeking to mechanically adhere to whatever lies beneath it. A solder joint forms when molten solder wets the pad and reacts with it, and that reaction is itself the bond. Where the pad is copper, tin-based solder reacts with the copper to form one or more copper-tin intermetallic compounds—principally Cu_6Sn_5 , and, with additional time or temperature, Cu_3Sn —at the solder-to-pad interface. The presence of that intermetallic layer is recognized in the industry as the evidence that a genuine metallurgical solder joint has been made. A solder ball or solder bump accordingly does not need a separate adhesion layer to bond to a copper pad. Forming that intermetallic bond to the copper is the result of reflowing solder against it, not a failure mode to be engineered around.

71. Beyond 2.5D integration, the industry has also developed true three-dimensional die stacking, in which multiple chips are stacked vertically and interconnected using through-silicon vias (“TSVs”)—vertical conductive structures that extend completely through a silicon die. Because the resulting interconnects between stacked dies are extremely short, 3D stacking offers the highest interconnect bandwidth among the packaging approaches described above.

72. Advanced packaging techniques of this kind, however, introduce their own engineering challenges. Chief among them is heat removal: in a conventional

package, heat generated by the die flows in a relatively direct path to a heat spreader. In a stacked or interposer-based assembly, however, internal dies have more limited cooling paths, and dies positioned closer to the heat spreader can thermally shield those farther away.

73. A related challenge is that advanced packages combine many different materials—semiconductor, metal, polymer, ceramic, and, in some instances, glass—at different locations within the same assembly. Different materials expand and contract by different amounts as temperature changes. Because integrated circuits are predominantly fabricated in silicon, it is generally desirable for the other materials in a package to have a CTE reasonably close to that of silicon. A significant CTE mismatch between adjoining materials can cause delamination, warping, or bowing and, as noted above, can fatigue and crack solder interconnects over repeated thermal cycling. This is one of the reasons that underfill materials are often loaded with silica or ceramic filler—to bring the underfill’s effective CTE closer to that of the surrounding materials it contacts.

VIII. THE ’306 PATENT

74. The ’306 Patent was filed as application no. 17/985,827 on November 12, 2022. The 17/985,827 application is a continuation of application no. 17/372,459 (now U.S. Patent No. 11,538,763), filed on July 11, 2021. The 17/372,459 application is a continuation of application no. 16/752,650 (now U.S.

Patent No. 11,107,768), filed on January 26, 2020. The 16/752,650 application is a continuation of application no. 15/261,956 (now U.S. Patent No. 10,622,310), filed on September 11, 2016, which is a continuation-in-part of application No. 14/036,256 (now U.S. Patent No. 9,615,453), filed on September 25, 2013. The '306 Patent claims priority to provisional application no. 61/705,649, filed on September 26, 2012, and provisional application no. 62/219,249, filed on September 16, 2015.

A. Specification

75. I have reviewed the patent specification along with the claims. The '306 Patent discloses a “method and structure to manufacture a glass substrate” and a “chip building a system on the glass substrate.” *See* EX1001 ['306 Patent], 1:23-25. The glass substrate comprises “multiple metal conductors through in said glass substrate and multiple metal bumps are between said glass substrate and said display panel substrate, wherein said one of said metal conductors is connected to one of said contact pads through one of said metal bumps.” *Id.*, Abstract

B. Prosecution History

76. I have reviewed the prosecution history of the '306 Patent. After filing the 17/985,827 application that issued as the '306 Patent, Applicant filed several preliminary amendments before the first office action. EX1002 [FH], 249-258, 265-274.

77. On November 7, 2023, the Examiner issued a non-final rejection rejecting all pending claims. *Id.*, 321-324. The Examiner rejected the claims based on nonstatutory double patenting over the claims of the parent '763 Patent. *Id.*, 323

78. On November 8, 2023, the Applicant filed an amendment, including a terminal disclaimer over the claims of the '763 Patent. *Id.*, 326-339. Applicant's amendment cancelled pending claims 5-6, 13 and 17, amended pending claims 21 and 26, and added new claims 27-31. *Id.*, 336-337. The amendment to pending independent claim fixed a typographical error. *Id.*, 332. The terminal disclaimer was approved on November 9, 2023 (*id.*, 349) and the Examiner issued a notice of allowance on November 24, 2023 allowing the pending claims. *Id.*, 382-389.

C. Claims of the '306 Patent

79. Representative claim 1 of the '306 patent recites a chip package whose elements, read together, describe a single integrated architecture: a solid layer comprising a compound of silicon and oxygen (e.g., glass) wherein the layer has a first region and a second region, with the second region carrying metal or copper through-conductors, planarized to a common plane so that a thin-film interconnection scheme can be fabricated across it, which scheme simultaneously receives a flip-chip semiconductor die through the die's thick-copper pad interconnect and routes the die's signals through the through-conductors to

solderable, tin-containing bumps for the next assembly level. The claim is properly understood as this combination, not as a collection of independent components.

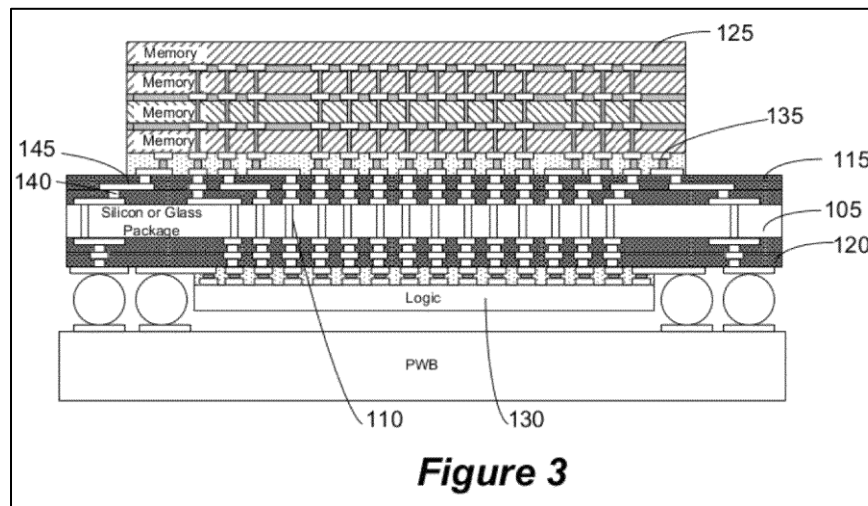
80. Independent claims 10 and 18 have similar claim elements.

81. Each claim is properly understood as the combination of elements, not as a collection of independent components. The interdependence of the elements confirms that each claim must be considered as a whole. The claimed invention resides in their combination, and the claim limitations take their meaning from other limitations.

IX. OVERVIEW OF THE ALLEGED PRIOR ART

A. Sundaram (EX1004)

82. Sundaram is directed to a 3D interconnect structure comprising an ultra-thin interposer having a plurality of ultra-high density through-via interconnections defined therein. EX1004 [Sundaram], Abstract. Sundaram Figure 3 (relied on in the Petition) shows Sundaram's interconnect structure comprising an interposer defining a plurality of through vias.



Id., Fig. 3. “[T]he interconnect structure comprises an interposer 105 having a first side 115 and a second side 120.” *Id.*, 5:47-48. “A plurality of ultra-small through vias 110 can be defined within the interposer 105 such that each of the through vias 110 extends from the first side 115 to the second side 120 of the interposer 105.” *Id.*, 6:6-9. These “through vias 110 are ultra-small and can range from about 1-25 micrometers in diameter at about 3-50 micrometers in pitch.” *Id.*, 6:11-13. “A first electronic device 125 can be attached to the first side 115 of the interposer 105 and a second electronic device 130 can be attached to the second side 120 of the interposer 105.” *Id.*, 6:34-36. “[E]lectronic devices having different I/O pad layouts and sizes can also be connected through the use of blind vias 140 and conductor traces 145 defined within polymer-metal redistribution layers deposited on the first side 115 and second side 120 of the interposer 105.” *Id.*, 6:62-67.

B. Lin-191 (EX1005)

83. Lin-191 discloses “system-in packages” comprising multi-layer chips in a multi-layer polymer structure. EX1005 [Lin-191], Abstract. Lin-191 explains that:

System-in packages, or multichip modules, are described which can include multi-layer chips in a multi-layer polymer structure, on-chip metal bumps on the multi-layer chips, intra-chip metal bumps in the multi-layer polymer structure, and patterned metal layers in the multi-layer polymer structure. The multi-layer chips in the multi-layer polymer structure can be connected to each other or to an external circuit through the on-chip metal bumps, the intra-chip metal bumps and the patterned metal layers. The system-in packages can be connected to external circuits through solder bumps, meal bumps or wirebonded wires.

Id.

C. Yu (EX1010)

84. Yu discloses a package-on-package (POP) structure having at least one package comprising one die being disposed in a core material between first and second surfaces of the core material. EX1010 [Yu], Title. The Petition relies primarily on Yu Figures 16 and 52.



Id., Figs. 16, 52. Yu provides limited discussion of these figures. Yu Figure 16

package, such as between the third die 62 and the second metallization layer 24.”
Id., 4:67-5:4.

85. Yu Figure 52 shows “step to form electrical connectors on the PoP structure of FIG. 51.” *Id.*, 2:15-16. “In FIG. 52, connectors 210, such as BGA balls, formed coupled to a metallization layer on a front side of the interposer of the interposer package 204, similar to FIG. 50.” *Id.*, 8:36-39.

D. Camacho (EX1006)

86. Camacho (EX1006) discloses a stacked package structure with a semiconductor die 122 having through-silicon vias 134 connecting conductive layers on its top and bottom surfaces, with a further die stacked above. Camacho states that its conductive layers 130 and 132 “can be one or more layers of Al, Cu, Sn, Ni, Au, Ag, or other suitable electrically conductive material, and that in one embodiment they “are under bump metallization (UBM) layers made with multi metal stack.” EX1006 [Camacho], ¶¶[0041]-[0042].

E. Lin-863 (EX1007)

87. Lin-863 describes a fan-out wafer-level chip-scale package having a substrate 226 on which “conductive TMV[s] [through-mold vias] 225” and a “semiconductor die 124” are disposed. EX1007 [Lin-863], 12:33-42, 14:45-46, Figs. 9a-9b.

X. CLAIMS

88. I understand that the '306 Patent has three independent claims (claims 1, 10, and 18) and 24 dependent claims. Representative claim 1 is reproduced below.

Claim Designation	Claim Language
Claim 1(Pre)	A chip package comprising:
Claim 1(a)	a solid layer having a first surface and a second surface opposite to said first surface,
Claim 1(a)(i)	wherein said solid layer comprises a compound of silicon and oxygen,
Claim 1(a)(ii)	wherein said solid layer has a thickness between 50 and 150 micrometers,
Claim 1(a)(iii)	wherein said solid layer comprises a first region and a second region between said first region and a first edge of said solid layer;
Claim 1(b)	a plurality of metal posts in a plurality of through holes in said second region respectively,
Claim 1(b)(i)	wherein one of said plurality of metal posts comprises a first copper layer contacting a sidewall of one of said plurality of through holes,
Claim 1(b)(ii)	wherein said first region has a width in a direction greater than a shortest distance between said sidewall of one of said plurality of through holes and said first edge in said direction and greater than a pitch between two neighboring metal posts of said plurality of metal posts;
Claim 1(c)	a first interconnection scheme over said first surface,
Claim 1(c)(i)	wherein said first interconnection scheme comprises a first metal interconnect over said second surface and a polymer layer over said first metal interconnect,
Claim 1(c)(ii)	wherein said first metal interconnect is connected to a first metal post of said plurality of metal posts,

Claim 1(c)(iii)	wherein said first metal interconnect comprises a first metal layer and a second copper layer over said first metal layer;
Claim 1(d)	a first metal bump over said first interconnection scheme,
Claim 1(d)(i)	wherein said first metal bump comprises a second metal layer and a first tin-containing layer over said second metal layer; and
Claim 1(e)	a first semiconductor chip under said second surface,
Claim 1(e)(i)	wherein said first interconnection scheme comprise a second metal interconnect across over a sidewall of the first semiconductor chip,
Claim 1(e)(ii)	wherein said first semiconductor chip comprises a third metal interconnect on a first metal pad of said first semiconductor chip,
Claim 1(e)(iii)	wherein said third metal interconnect comprises a third metal layer on said first metal pad and a third copper layer over said third metal layer, wherein said third copper layer has a thickness between 5 and 30 micrometers,
Claim 1(e)(iv)	wherein said first semiconductor chip is connected to a second metal post of said plurality of metal posts through said third metal interconnect.

XI. PETITIONERS FAIL TO DEMONSTRATE THAT ANY OF THE CHALLENGED CLAIMS ARE UNPATENTABLE

89. I have reviewed the Petition and understand that it advances the following five grounds:

Grounds	Claims Challenged	35 U.S.C. §	References
<u>1A</u>	1-7, 9-11, 13-15, 17-27	103	Sundaram (EX1004) and Lin-191 (EX1005)
<u>1B</u>	8, 12, 16	103	Sundaram, Lin-191, and Lin-863 (EX1007)
<u>2A</u>	1-7, 9-15, 17-20, 22-27	103	Yu (EX1010) and Lin-191
<u>2B</u>	8, 16	103	Yu, Lin-191, and Lin-863
<u>2C</u>	21	103	Yu, Lin-191, and Camacho (EX1006)

Pet., 2.

A. Ground 1A (Sundaram And Lin-191)

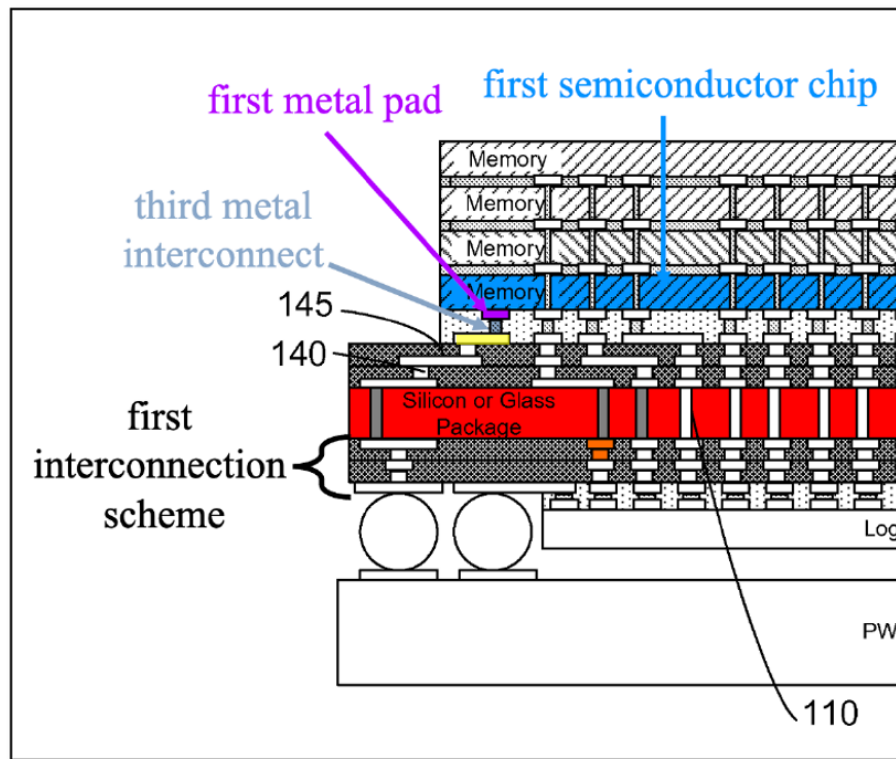
90. Ground 1A relies on Sundaram and Lin-191, and challenges claims 1-7, 9-11, 13-15, and 17-27. *Id.*

1. Sundaram and Lin-191 Do Not Teach or Suggest a “First Semiconductor Chip Comprises a Third Metal Interconnect” or “Third Metal Interconnect on a First Metal Pad of Said First Semiconductor Chip.”

a. Sundaram’s memory chip does not comprise a third metal interconnect or third metal interconnect on a first metal pad of said first semiconductor chip.

91. Limitation 1(e)(ii) requires that the “first semiconductor chip comprises a third metal interconnect.” EX1001 [’306 Patent], cl. 1. This limitation is not disclosed by Sundaram because Sundaram’s alleged semiconductor chip does not comprise or include Sundaram’s alleged third metal interconnect.

92. Petitioners argue that Sundaram Figure 3’s “die pads 135 [that are formed on the first 115 and second sides 120 of the interposer 105] can electrically connect devices using solder, copper bumps with solder caps, [and] copper to copper bonding,’ each of which teaches a third metal interconnect.” Pet., 23 (citing EX1004 [Sundaram], 6:29-33) (emphasis removed). In particular, the Petition states that “[i]n FIG. 3, the third metal interconnect is a bump on the metal pad.” Pet., 23 (emphasis removed). That is, as shown below, the Petition alleges that the solder/bumps (gray) (located on top of the die pad 135 (yellow) of interposer 105) is the claimed “third metal interconnect”:



Pet., 24 (excerpting and annotating EX1004 [Sundaram] Fig. 3; I have added the yellow annotation showing die pad 135).

93. The structure that the Petition identifies as the alleged “first semiconductor chip” (blue) does not comprise the alleged “third metal interconnect” (bump/solder shown in gray). This is because the bumps/solder are not part of the memory – the alleged “first semiconductor chip” (shown in blue).

94. Instead, the bumps (or solder) (the alleged “third metal interconnect”) are formed *on the die pad 135 of the interposer 105* to electrically connect devices to the interposer 105. EX1004 [Sundaram], 6:29-33 (describing die pads 135 using bumps/solder to make electrical connections). And Sundaram specifically states that

the die pads 135 are associated *with the interposer 105*: “[t]he through vias 110 can be metalized in such a way that the metallization provides die pad surfaces 135 that correspond to each of the vias 110 on both the first side 115 and the second side 120 of the interposer 105.” EX1004 [Sundaram], 6:23-25; *see also id.*, 6:29-33. Thus, Sundaram’s bumps/solder are part of or associated with the interposer 105, not the alleged “first semiconductor chip.”

95. Petitioners’ own exhibits demonstrate that solder/bumps (as described in Sundaram) are not considered part of the alleged “first semiconductor chip.” Instead, solder/bumps (as described in Sundaram) are structures that are separate from a semiconductor chip and that are used to connect other components to contacts/pads of the semiconductor chip. EX1161 [Haba], 6:39-47 (“In the interconnection component of FIG. 8 end surfaces 10B can be wettable *contacts used to connect posts 10 to another component using solder balls or other conductive materials*. For example, in FIG. 10A, *end surfaces 10B are used to join posts 10 to solder balls 32, which are, in turn, joined to contacts 50 on a microelectronic element 6*. Other materials can be used in place of solder balls 32 to join features of the components of the assembly such as tin indium or a conductive matrix.”) (emphasis added); 7:42-56 (“As shown in FIGS. 10A and 10B, interconnect component 2 in either of the forms shown 9 and 10A, respectively, can be used to connect two components with respective contacts

having different pitches or other different configurations. In the example shown in FIG. 10A microelectronic element 6 has contacts 50 having a smaller pitch than the pitch of contacts 52 on printed circuit board (“PCB”) 12. Contacts 52 of PCB 12 are joined to end surfaces 10B, which act as wettable contacts therefor, and contacts 50 of microelectronic element 50 are joined to vias pads 34 of interconnection component 2, which is inverted with respect to the depiction of FIG. 8. The embodiment shown in FIG. 10B is similar to that which is shown in 10A, except that *pads 34 which overlie end surfaces 10B act as wettable contacts for attachment to contacts 52 of PCB 12 using solder balls 32.*) (emphasis added); 8:27-29 (“For example, an interconnection component can be disposed on and connected to a PCB that includes an electrically conductive EMI shield. *The end surfaces of the posts can then be solder bonded to contact pads of the PCB* with the EMI shield being ball-bonded to a peripheral trace of the interconnection component for grounding to the shield.”) (emphasis added); 11:33-35 (“Further, *circuit panel 96* can be of a similar structure to PCB having contacts 52 thereon, and *can connect to interconnection component 2 using solder balls 32 or the like.*”) (emphasis added).

96. Limitation 1(e)(ii) requires “wherein said first semiconductor chip comprises a third metal interconnect on a first metal pad of said first semiconductor chip.” EX1001 [’306 Patent], cl. 1. Based on Sundaram’s disclosure, bump/solder

(gray) is formed on a die pad 135 of the interposer 105 and, thus, is not on a metal pad of the semiconductor chip. The Petition identifies the “first metal pad” as the component shown in purple above and memory (blue) of electronic device 125 as the claimed “first semiconductor chip.” Pet., 23 (emphasis removed). Sundaram (and the Petition) therefore places the alleged “third metal interconnect” on the interposer 105 and the alleged “first metal pad” on the alleged semiconductor chip. Thus, the alleged “third metal interconnect” is not on the alleged “first metal pad.” The alleged “third metal interconnect” is on the die pad 135 (yellow) of the interposer 105. In addition, the “first semiconductor chip” does not comprise a third metal interconnect because the memory (the alleged semiconductor chip) does not comprise the bump/solder (gray) (the alleged third metal interconnect) – the bump/solder (gray) is part of the interposer.

97. The mismatch described above – the alleged “third metal interconnect” on the interposer 105 and the alleged “first metal pad” on the alleged semiconductor chip – follows at least partially from the fact that Sundaram does not describe the pads or interconnects of electronic device 125. The Petition does not identify any disclosure of those structures and certainly does not explain the component shown above or what it is made of. The Petition states instead that “[a] POSITA would understand that device 125 also has die pads . . . such that an electrical connection is made between interposer 105 and device 125.” Pet., 23 (citing EX1003 [Shanfield

Decl.], ¶163). That is an assumption about what a device could have, not a teaching of Sundaram.

98. Dr. Shanfield’s declaration confirms that this mismatch rests on assumption rather than on any disclosure in Sundaram. Dr. Shanfield does not identify any Sundaram teaching of a pad or an interconnect on electronic device 125. He states only that “[a] POSITA would understand that[,] like interposer 105, first electronic device 125 (first semiconductor chip) also has die pad[s],” and he supports the existence of that pad not with Sundaram but with other references — for example EX1095. EX1003 [Shanfield Decl.], ¶¶163, 166. Reasoning by analogy to the interposer, and by reference to what pads other art shows, is not a teaching that Sundaram’s electronic device 125 comprises the claimed “first metal pad,” or the claimed “third metal interconnect” on it.

99. The Sundaram passage that the Petition relies on is directed to the interposer. Sundaram states that “[t]he die pads 135 that are formed on the first 115 and second sides 120 of the interposer 105 can electrically connect devices using solder, copper bumps with solder caps, copper to copper bonding, adhesive bonding, metallurgical bonding, non-conductive bonding, or combinations thereof.” EX1004 [Sundaram], 6:29-33. That sentence lists methods that are used to make electrical connections for joining a device to the die pads *of the interposer*. It does not describe

any structure formed on electronic device 125 or the memory shown in blue above, and it does not describe the layered construction required by limitation 1(e)(ii).

100. The Petition's combination of Sundaram and Lin-191 fails because it does not teach or suggest the "first semiconductor chip comprises a third metal interconnect" or "third metal interconnect on a first metal pad of said first semiconductor chip."

b. Lin-191 does not teach or suggest limitation 1(e)(ii).

101. Petitioners do not allege that Lin-191 teaches or suggests the "first semiconductor chip comprises a third metal interconnect." EX1001 ['306 Patent], cl. 1. Although Petitioners include a section on Lin-191 for Ground 1A limitation 1(e)(ii), the statements in that section are directed to the claimed "metal pad," not the claimed "third metal interconnect." Pet., 25-26. The section does not allege Lin-191 teaches or suggests the "first semiconductor chip comprises a third metal interconnect."

c. The Petition's motivation to combine Lin-191 and Sundaram is conclusory and wrong.

102. According to the Petitioners, there is a motivation to combine Lin-191 and Sundaram because the modification "is the application of a known technique (metal pads) to a known device (Sundaram's semiconductor chip having die pads) ready for improvement to yield the predictable result of Sundaram's device 125

having a first metal pad.” Pet. 26. This statement offers no substantive explanation as to why the structure (shown in purple above) required the application of the Lin-191’s metal pad teachings. It presupposes that one would modify Sundaram without identifying any issues, shortcomings, or reasons to combine the references.

103. Sundaram and Lin-191 reflect fundamentally different engineering approaches to building a multi-chip structure, and a POSITA would not have been motivated to merge them. Lin-191 teaches a chip-first, tier-by-tier build in which the substrate is a work-in-progress rather than a finished component: chips carrying on-chip metal bumps are adhered to the substrate, encapsulated, and then polished or ground to expose the bumps before interconnections are formed, with the sequence repeated for each successive tier. EX1005 [Lin-191], ¶[0009]. Consistent with that approach, Lin-191 does not form its through-substrate connections until late in the process — substrate 110 is first thinned to as little as 1 to 10 micrometers by mechanical grinding or chemical-mechanical polishing of its backside, EX1005 [Lin-191], ¶[0290], and only then are through holes 16 and through-hole connections 17 formed from that newly exposed surface. EX1005 [Lin-191], ¶¶[0292]–[0293]. Sundaram proceeds in the opposite order and for the opposite reason. Sundaram builds and electrically verifies its interposer before any die is attached, and describes this chip-last sequence as the mechanism by which its structure “alleviates the Known Good Die (KGD) concerns in 3DIC integration.” EX1004 [Sundaram], 7:51-

53, FIG. 6 (steps 605, 610, 615). Sundaram's claims reinforce that its interposer is meant to be a completed, verifiable article, requiring test pads on both sides to permit testing of devices attached to either side. EX1004 [Sundaram], cl. 21–22. A POSITA seeking the benefits Sundaram describes would have understood that those benefits depend on the interposer being finished and tested before die attachment, and would therefore have seen no advantage in placing that interposer into Lin-191's process, where the substrate is deliberately left unfinished and is subsequently thinned, ground, and metallized from the backside after the chips are already in place. The features a POSITA would have been looking to Sundaram for — its through-vias, its redistribution layers, and its test pads — are the same features Lin-191's later processing steps would have been expected to disturb. A POSITA would not have expected the combined arrangement to retain them or to function as Sundaram describes. Conversely, a POSITA starting from Lin-191 and reordering its process to preserve Sundaram's pre-tested interposer would have had to abandon the tiered, chip-first integration that Lin-191 identifies as its contribution, including the high routing density between chips that Lin-191 attributes to its fine-pitched on-chip and intra-chip metal bumps. EX1005 [Lin-191], ¶¶[0010]–[0011]. A POSITA would not have had a reason to make either change, nor a reasonable expectation that the resulting structure would work as either reference intends. There is no evidence that a POSITA would have a reason to combine the references.

2. Sundaram and Lin-191 Do Not Teach or Suggest “Wherein Said Third Metal Interconnect Comprises a Third Metal Layer on Said First Metal Pad and a Third Copper Layer Over Said Third Metal Layer.”

104. The Petition relies solely on Lin-191 for limitation 1(e)(iii). Pet., 26-27. As discussed below, Lin-191 does not teach or suggest this limitation.

a. Lin-191 does not teach or suggest “said third metal interconnect.”

105. As discussed above, the Petition fails to demonstrate that Sundaram teaches a “first semiconductor chip compris[ing] a third metal interconnect” because Sundaram’s memory chip does not comprise the solder/bumps alleged to be the claimed “said third metal interconnect.”

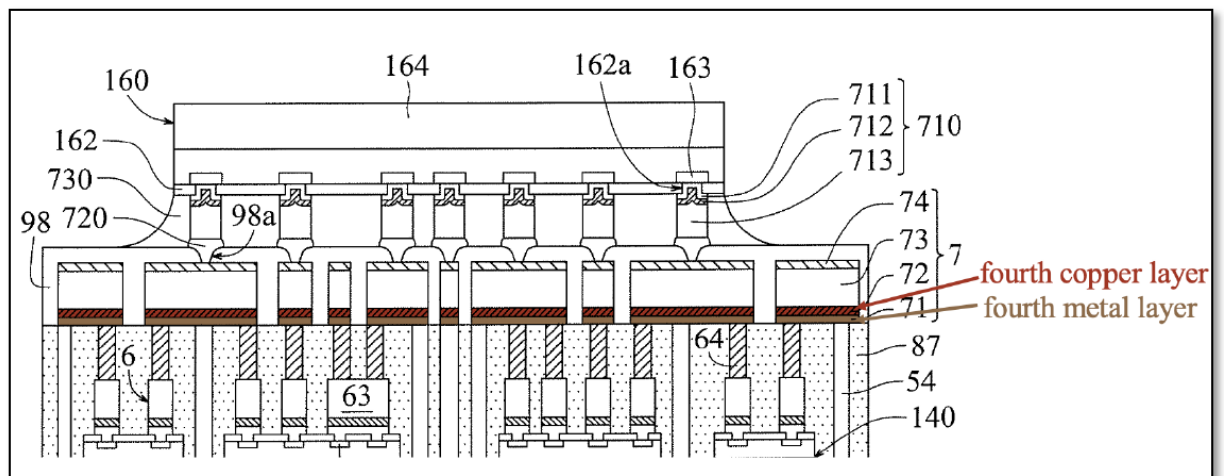
106. Although the Petition alleges Lin-191’s bumps 710 are metal interconnects for limitation 1(e)(iii) (Pet., 26-27), the Petition does not rely on Lin-191 as teaching or suggesting that Sundaram’s first semiconductor chip comprises the claimed third metal interconnect, cl. 1(e)(ii). *Id.* The Petition’s treatment of Lin-191 for limitation 1(e)(ii) is directed to the claimed “metal pad,” stating only that “Lin-191’s system-in package has a semiconductor chip 160 with ‘metal traces or pads 163’ that include ‘aluminum.’” Pet., 25 (emphasis removed). Lin-191 therefore does not remedy the deficiency in Sundaram that I have identified above.

b. Lin-191 does not teach or suggest “a third metal layer on said first metal pad and a third copper layer over said third metal layer.”

107. The Petition’s mapping of limitation 1(e)(iii) is inconsistent with the Petition’s own mapping of claim 3(c). Claim 3(c) recites a two-layer interconnect. Petitioners assert that adhesion and seed layers are *two separate* layers for claim 3(c) “Adhesion layer 71 is a metal (e.g., titanium or nickel) and is thus a fourth metal layer. Seed layer 72 is ‘a copper layer’ on adhesion layer 71 and is thus a fourth copper layer on said fourth metal layer.” Pet., 37 (citing EX1005 [Lin-191], ¶¶[0260]-[0264]); EX1003 [Shanfield Decl.], ¶187) (emphasis removed).

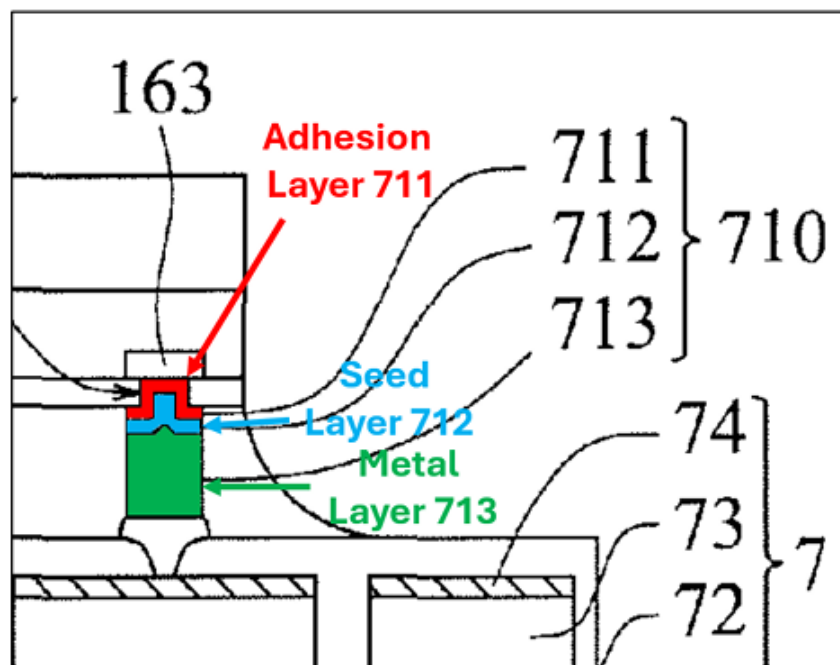
108. But, when it comes to limitation 1(e)(iii), Petitioners assert that adhesion and seed layers are *one* layer. Those two positions cannot both be correct.

109. In the annotated diagram of the Petition, adhesion layer 71 and seed layer 72 as well as adhesion layer 711 and seed layer 712 can be seen together:



Pet. 38 (citing EX1005 [Lin-191], FIG. 72 (excerpt); EX1003, ¶187).

110. The Petition errs in its assertions that “the combination of layers 711 and 712 [in Lin-191 Fig. 72] is a *third metal layer on metal pad 163.*” Pet., 27 (emphasis in original). In other words, in view of Lin-191’s configuration, the Petition errs in asserting that two layers 711 and 712 are one layer — “a third metal layer.” Based on Petitioners’ own position regarding claim 3(c), as shown below, adhesion layer 711 (red) and seed layer 712 (blue) in Lin-191 Fig. 72 are two different layers, not one layer.



EX1005 [Lin-191], Fig. 72 (excerpted and annotated), ¶[0389] (“metal layer 713 under the seed layer 712 and over the solder joints 720.”); (“a seed layer 712 under the adhesion layer 711.”)

111. Notably, Petitioners combine layers 711 and 712 because the claim language requires that a third metal layer is on the first metal pad and that a copper layer is over the third metal layer. The alleged first metal pad is metal pad 163. Adhesion layer 711 (red above) is on the metal pad 163 and the alleged copper layer 713 (green above) is over seed layer 712 (blue above), not the adhesion layer 711. Thus, if layers 711 and 712 are not one layer, under Petitioners' apparent view, the claim limitation is not met. But, according to Petitioners' own admission, adhesion and seed layers are not the same layer. Thus, Lin-191 fails to disclose "a third metal layer on said first metal pad and a third copper layer over said third metal layer."

112. In view of Lin-191's configuration and Petitioner's admission, a POSITA would not consider Lin-191's adhesion layer 711 and seed layer 712 to be a single layer. Lin-191 does not refer to adhesion layer 711 and seed layer 712 as a single layer. EX1005 [Lin-191], ¶¶[0389]-[0400]. Instead, adhesion layer 711 and seed layer 712 are two different layers made of different materials serving different purposes. *Id.*, ¶[0389] ("a seed layer 712 under the adhesion layer 711"), Fig. 72. A POSITA would understand an adhesion layer as a layer made to allow materials that are not compatible (in adhesion) to adhere to one another. This is a common occurrence in microfabrication where dissimilar materials are deposited on one another. An example is copper deposited on aluminum pads. *Id.*, ¶[0059]. For example, Lin-191 explains that adhesion layer 711 is made of "titanium, a titanium-

tungsten alloy, titanium nitride, chromium, tantalum, tantalum nitride, nickel or nickel vanadium” and has a thickness of “less than 1 micrometer, such as between 1 nanometer and 0.5 micrometers.” *Id.*, ¶[0390]. Conversely, Lin-191 explains that seed layer 712 is made of different materials (“copper, silver, gold, nickel or titanium-copper alloy”) having a different thickness (“less than 1 micrometer, such as between 10 nanometers and 0.8 micrometers.”). *Id.* Thus, according to Lin-191’s configuration, a seed layer is used for a starting layer for electroplating. *Id.*, ¶[0058].

113. The materials that Lin-191 specifies for an adhesion layer 711 are metals and compounds selected for adhesion and diffusion barrier performance rather than for conductivity. *Id.*, ¶[0390]. Lin-191 uses these materials because, for example, copper does not adhere well to, and can diffuse into, the underlying dielectric or pad material.

114. The separate seed layer in Lin-191 is present for a different reason. Electroplating requires a continuous conductive surface from which the plated metal can nucleate and grow, and the seed layer supplies that surface. This is why Lin-191 specifies seed layer 712 as “copper, silver, gold, nickel or titanium-copper alloy” — metals selected for their compatibility with the metal to be plated. *Id.*, ¶[0390]. The materials Lin-191 specifies for the adhesion layer would not serve as a plating seed, and the copper and noble metals it specifies for the seed layer would not provide the adhesion and barrier function.

115. The Petition treats Lin-191's adhesion and seed layers as two separate claimed layers. For claim 3(c), the Petition states that "Lin-191 teaches a multilayered metal interconnect with two copper layers. Specifically, Lin-191 teaches a 'patterned metal layer 7' having an 'adhesion layer 71, the seed layer 72, the metal layer 73, and the barrier/wetting layer 74....'" Pet., 37 (citing EX1005 [Lin-191], ¶[0379]; EX1003 [Shanfield Decl.], ¶187). The Petition then maps each of those layers to a separate claimed layer: "Adhesion layer 71 is a metal (e.g., titanium or nickel) and is thus a fourth metal layer.... Seed layer 72 is 'a copper layer' on adhesion layer 71 and is thus a fourth copper layer on said fourth metal layer." Pet., 37 (emphasis removed).

116. It is notable that the petition takes a completely different approach by regarding adhesion layer and seed layer as two separate layers in limitation 1(d)(i) when it maps Lin-191's under-bump metallurgy for the "first metal bump", describing Lin-191's "adhesion layer 18, the seed layer 19, and metal layer[] 27" as the separate metal layers that "compose an under bump metallurgic (UBM) layer." Pet., 18 (quoting EX1005 [Lin-191], ¶[0323]; EX1003 [Shanfield Decl.], ¶¶151-152). In those mappings, the Petition treats Lin-191 adhesion and seed layers as two distinct layers. For limitation 1(e)(iii), by contrast, the Petition merges an adhesion layer and a seed layer into a single claimed "third metal layer."

117. I also note that the Petition elsewhere describes this construction as a “multilayered metal interconnect.” Pet., 37. Based on Petitioners’ own statements, a POSITA would understand Lin-191’s adhesion layer and seed layer to be two layers, and would not understand an adhesion layer and a seed layer together to be a single layer.

118. Petitioners’ position that “the combination of layers 711 and 712 is a third metal layer on metal pad 163” (Pet., 27) merges what Petitioners identify as two distinct layers into one claimed layer, which is inconsistent with Petitioners’ own mapping of claim 3(c) and limitation 1(d)(i).

119. For these reasons, the structure of the chip package claimed at ’306 Patent claim 1 is different than the structure of the semiconductors described in Lin-191. Because of this, the Petition fails to map Lin-191 to limitation 1(e)(iii). Because neither Sundaram nor Lin-191 teaches or suggests limitation 1(e)(iii), the Petition has not shown that claim 1 (or the claims depending therefrom) are unpatentable.

3. There Is No Motivation to Combine Sundaram and Lin-191.

120. The Petition advances a separate motivation to combine for limitation 1(e)(iii) that is distinct from the motivation it advances for limitation 1(e)(ii). Pet., 28. The Petition asserts that “[a] POSITA would have been motivated and found obvious to modify Sundaram’s bump per Lin-191’s layered bump teachings,” and that the result would be “Sundaram’s bump (third metal interconnect) having a third

metal layer over said first metal pad and a third copper layer over said third metal layer.” Pet., 28 (citing EX1003 [Shanfield Decl.], ¶170) (emphasis removed). The Petition states that the rationale is that “Lin-191’s metal bump provides improved metallurgical bonding and increased resistance to fatigue and stress-induced failure by employing a layered structure,” and that the configuration “would reduce the risk of intermetallic formation at critical interfaces, mitigate electromigration, and better absorb mechanical strain during thermal cycling.” Pet., 28 (citing EX1003 [Shanfield Decl.], ¶¶171-172). The Petition also states “the mechanical integrity and reliability of the Sundaram’s bumps would be improved, particularly in applications subject to repeated temperature fluctuations and mechanical stress, e.g., where the chip package includes “high power logic component[s].” Pet., 28 (citing EX1003 [Shanfield Decl.], ¶173; EX1004 [Sundaram], 6:19-22, FIGS. 30-31).

121. I have reviewed Lin-191 and have not located any statement that demonstrates to a POSITA that Lin-191’s adhesion layer 711 and seed layer 712 provide increased resistance to fatigue or stress-induced failure, reduced intermetallic formation, mitigation of electromigration, or improved absorption of mechanical strain during thermal cycling. Lin-191 describes those layers structurally and by material and thickness, and does not attribute the asserted advantages to them. EX1005 [Lin-191], ¶¶[0389]-[0400].

122. Dr. Shanfield's declaration confirms that the asserted advantages are not drawn from Lin-191. To support the propositions that a layered bump prevents diffusion, and increases resistance to fatigue, Dr. Shanfield does not rely on Lin-191. He relies on other references directed to under-bump metallurgy and diffusion barriers generally. EX1003 [Shanfield Decl.], ¶171 (citing EX1022 and EX1047 for metallurgical bonding and diffusion prevention); ¶172 (citing EX1063 for uniform plating and void prevention). Moreover, the diffusion Dr. Shanfield identifies is the diffusion of "solder material into the first metal pad," EX1003 [Shanfield Decl.], ¶171, whereas the Petition describes Sundaram's own interconnect on die pad 135 as copper. *See* Pet., 27. But the Petition identifies no solder-diffusion, oxide, or adhesion problem in that copper structure that Lin-191's added layers would remedy. The asserted motivation therefore does not rest on any teaching that Lin-191's adhesion layer 711 and seed layer 712 supply those advantages in the structure the Petition maps.

123. Petitioners' asserted motivation also presupposes a bump structure in Sundaram to be modified. The Petition describes the combination as "modify[ing] Sundaram's bump per Lin-191's layered bump teachings." Pet., 28. As discussed above, Sundaram does not describe the construction of any bump on electronic device 125. A POSITA could not modify a structure that the reference does not describe, and the Petition does not explain what would be modified.

124. A POSITA would not be motivated to combine Sundaram and Lin-191. The Petition has not shown that a POSITA would have looked to Lin-191's adhesion-layer/seed-layer/electroplated-layer bump structure to modify the bump on die pad 135 of Sundaram. A POSITA would have known that an adhesion or diffusion-barrier layer, such as the titanium or nickel adhesion layer 711 that Lin-191 describes, is needed only in particular circumstances, for example: where copper would otherwise diffuse into an adjacent, dissimilar metal; where copper would otherwise diffuse into an oxide or other inorganic dielectric; or where copper does not otherwise bond adequately to the material beneath it. The Petition does not show that any of these circumstances exists in Sundaram.

125. The Petition's own description of this combination confirms that Sundaram's own bump is copper. The Petition states that Lin-191's bumps 710, "like Sundaram's copper bumps, are metal interconnect[s]." Pet., 27. The Petition's stated motivation for adding Lin-191's layered structure is that it would provide "improved metallurgical bonding and increased resistance to fatigue and stress-induced failure," would "reduce the risk of intermetallic formation at critical interfaces," and would "mitigate electromigration" and "better absorb mechanical strain during thermal cycling." Pet., 28 (citing EX1003 [Shanfield Decl.], ¶¶171-172); *see also* Pet., 28 ("the mechanical integrity and reliability of the Sundaram's bumps would be improved, particularly in applications subject to repeated temperature fluctuations

and mechanical stress, e.g., where the chip package includes ‘high power logic component[s].’” (citing EX1004 [Sundaram], 6:19-22, FIGS. 30-31)). This rationale does not identify any specific diffusion, oxide, or adhesion problem with Sundaram’s own copper bump on die pad 135 that Lin-191’s layers would remedy. Moreover, electronic device 125 is not described structurally at all, because Sundaram pertains to the interposer not the electronic device 125.

126. [Intentionally omitted.]

127. [intentionally omitted.]

128. For these reasons, the Petition has not shown that a POSITA would have been motivated to combine Sundaram and Lin-191 in the manner the Petition proposes, and has not shown that the combination teaches or suggests limitation 1(e)(iii).

4. Sundaram Does Not Teach or Suggest the “First Metal Interconnect Comprises a First Metal Layer and a Second Copper Layer Over Said First Metal Layer.”

129. For other claim limitations discussed above, the Petition relies on Sundaram Figure 3. With regard to limitation 1(c)(iii), however, the Petition shifts its analysis to Sundaram Figure 15. These two figures, however, relate to *alternative* embodiments that a POSITA would not consider together.

130. Limitation 1(c)(iii) requires that “said first metal interconnect comprises a first metal layer and a second copper layer over said first metal layer.”

EX1001 ['306 Patent], cl. 1. For this two-layer construction, the Petition does not rely on the interconnect structure it identifies in Sundaram's Figure 3. Instead, the Petition relies on Sundaram's Figure 15, asserting that Sundaram teaches "a first metal layer formed by 'direct metallization using wet electroless copper deposition' and a second copper layer over said first metal layer formed by 'semi-additive plating' using 'copper as metal.'" Pet., 15 (quoting EX1004 [Sundaram], 9:61-65, 10:26-28) (citing EX1003 [Shanfield Decl.], ¶147) (emphasis removed).

131. The Petition states that "a POSITA would have been motivated, found obvious, and had a REOS in applying FIG. 15's layer teachings to FIG. 3's interconnect structure." Pet., 16 (citing EX1003 [Shanfield Decl.], ¶148) (emphasis removed). I disagree.

132. The Figure 3 interconnect structure is not described as comprising the seed-plus-electroplated two-layer construction of Figure 15. Sundaram describes FIG. 15 as not as a package embodiment (like Figure 3) but as the process flow for a research *test vehicle*. Sundaram states that "[a] glass test vehicle was designed and fabricated to characterize the substrate and TPVs in glass," and that "FIG. 15 shows the process flow used for fabricating the test vehicle." EX1004 [Sundaram], 10:5-15. Sundaram identifies the purpose of that test vehicle as characterization — it describes "[r]ing resonators ... designed to extract the dielectric constant and loss tangent of the interposer" and additional "structures ... designed and fabricated to

characterize the electrical characteristics of the interconnections (lines and TPVs) in glass interposer.” *Id.*, 10:35-39. A POSITA would understand a “test vehicle” or “demonstrator” of this kind to be an experimental construct built to measure material and electrical properties, not a manufacturing template for the chip package of Figure 3. Notably, Sundaram shows the “resulting two metal layer structure” of that process in Figure 16a-c — not in Figure 3. *Id.* A POSITA would not have understood Sundaram to teach transplanting the Figure 15 characterization process onto the separate Figure 3 package embodiment.

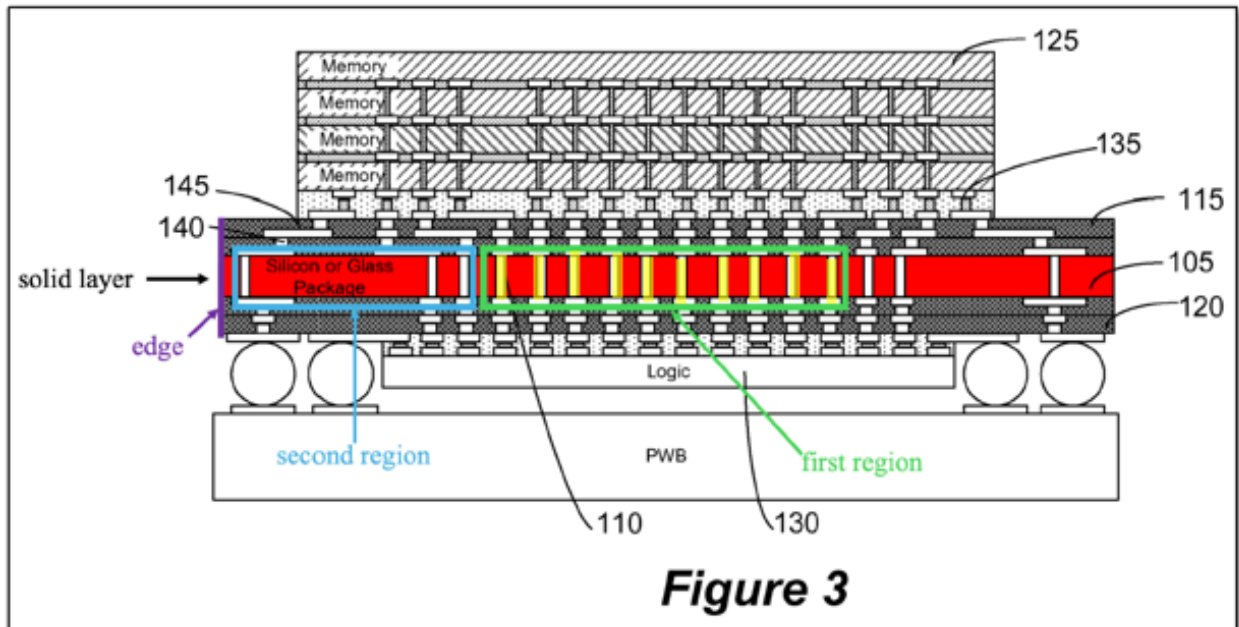
133. Sundaram ties the specific Figure 15 process — electroless copper seed formation followed by semi-additive plating — to a particular metallization challenge that Sundaram solves with polymer-laminated glass, and not to the Figure 3 interconnect. Sundaram explains that “direct wet metallization on glass has been a challenge due to surface chemistry of glass and its interaction with metals,” and that “[t]he presence of a surface polymer ... on glass facilitates metallization.” EX1004 [Sundaram], 9:55-62. It is in that context that Sundaram states the glass “TPV side walls were subjected to direct metallization using wet electroless copper deposition” and that “[a] semi-additive plating (SAP) approach was used.” *Id.*, 10:26-28, 9:61-64. A POSITA would understand Sundaram's electroless-seed-plus-SAP sequence to have been selected to metallize the polymer-laminated glass of the test

vehicle, addressing a known difficulty of metallizing glass, rather than as a general instruction to reconstruct the Figure 3 interconnect.

134. Sundaram describes the metallization of the Figure 3 embodiment on its own terms, and the Petition identifies no deficiency in that description that Figure 15's process would cure. For the Figure 3 embodiment, Sundaram states that its through vias and die pads "can be metalized with a highly-conductive metal, for example copper," and "can also be metalized with a polymer liner or a metal seeding liner." EX1004 [Sundaram], 6:22-33. Sundaram does not describe the Figure 3 interconnect as formed by Figure 15's electroless-seed-plus-SAP two-layer process, and it does not cross-reference Figure 15 as the method for building Figure 3. The Petition identifies no problem, shortcoming, or unmet need in Figure 3's own metallization that Figure 15's process would solve. Absent any such reason, a POSITA would not have been motivated to displace Figure 3's described metallization in favor of the Figure 15 test-vehicle process.

5. Sundaram Does Not Teach or Suggest a "First Region."

135. As discussed in Section VI, a "first region" is a region that does not include metal plugs/posts.



Pet., 9; EX1004 [Sundaram], Fig. 3 (annotated by Petitioners; I have added the yellow highlights).

136. A POSITA understands that the cross section of the structure shown in Figure 3 above would be taken vertically through the middle of the structure. As shown above, Petitioners randomly identify various portions of Sundaram as regions. Petitioners identifies a “first region” in a green box. This region, however, includes numerous metal posts, which I have annotated in yellow. Sundaram specifically states that through vias 110 (sixteen (16) of which are shown in Figure 3; ten (10) of which are highlighted in yellow) are “electrically and thermally conducting” and are metalized. EX1004 [Sundaram], 6:16-29. Thus, a POSITA understands that there must be metal posts through the vias 110 in order to electrically connect devices. *See also e.g. id.*, 6:46-48 (“The interposer 105 and the

through vias 110 work to electrically connect the first electronic device 125 and the second electronic device 130.”) Because the Petition identifies a region having metal posts, the Petition has not shown the claimed “first region.” And because the Petition has not shown a “first region,” it also has not shown any limitations in claim 1 related to a “first region”; “a second region between said first region and a first edge of said solid layer,”; or a “first region has a width in a direction greater than a shortest distance between said sidewall of one of said plurality of through holes and said first edge in said direction and greater than a pitch between two neighboring metal posts of said plurality of metal posts.” Because the Petition identifies a region having metal posts, the Petition has also not shown any limitations in claim 7, 8, 10, 12, 15, 16, 18, and 20 related to a “first region.”

137. I note that Figure 4 of Sundaram simply illustrates “a top view of the interconnect structure 100” in which first electronic device 125 and second electronic device 130 are marked and “the first electronic device 125 is of a different pad size and configuration than the second electronic device 130”. EX1004 [Sundaram], 7:1-5. Figure 4 does not show any details of the interposer 105, and specifically does not annotate location and number of the metal posts 110. Sundaram in fact teaches “through vias 110 ... are electrically and thermally conducting, and are distributed within the interposer”. EX1004 [Sundaram], 6:14-19. This statement confirms that, as clearly shown in Fig. 3, metal posts 110 exist

within and are distributed across the alleged “first region” so the alleged “first region” is not the “first region” of claims 7, 8, 10, 12, 15, 16, 18, and 20.

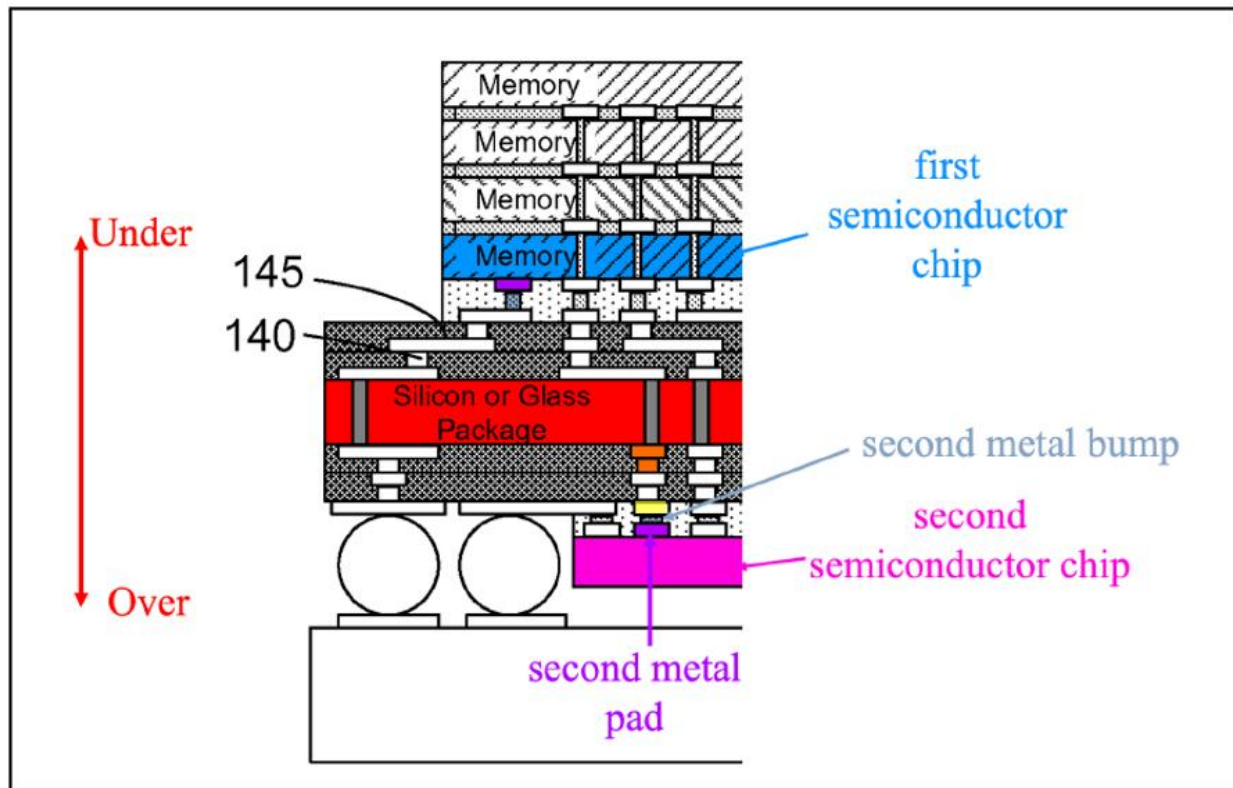
138. Refer to my discussion in Section XI.B.1.

6. Claim 6 is Patentable for the Same Reason as Claim 1.

139. My discussion in Section XI.A.1 (claim 1(e)(ii)) regarding the claim elements associated with the first semiconductor chip applies to the claim elements associated with the second semiconductor chip.

140. Claim 6 requires that the “second semiconductor chip comprises a second metal bump.” EX1001 [’306 Patent], cl. 6. This limitation is not disclosed by Sundaram because Sundaram’s alleged semiconductor chip does not comprise or include Sundaram’s alleged second metal bump.

141. As shown below, the Petition alleges that the solder/bumps (gray) (located on the die pad 135 (yellow) of interposer 105) is the claimed “second metal bump”:



Pet., 42 (excerpting and annotating EX1004 [Sundaram] Fig. 3; I have added the yellow annotation showing die pad 135).

142. The structure that the Petition identifies as the alleged “second semiconductor chip” (pink) does not comprise the alleged “second metal bump” (bump/solder shown in gray). This is because the bumps/solder are not part of the alleged “second semiconductor chip” (shown in pink).

143. Instead, the bumps (or solder) (the alleged “second metal bump”) are formed *on the die pad 135 of the interposer 105* to electrically connect devices to the interposer 105. EX1004 [Sundaram], 6:29-33 (describing die pads 135 using bumps/solder to make electrical connections). And Sundaram specifically states that

the die pads 135 are associated *with the interposer 105*: “[t]he through vias 110 can be metalized in such a way that the metallization provides die pad surfaces 135 that correspond to each of the vias 110 on both the first side 115 and the second side 120 of the interposer 105.” EX1004 [Sundaram], 6:23-25; *see also id.*, 6:29-33. Thus, Sundaram’s bumps/solder are part of or associated with the interposer 105, not the alleged “second semiconductor chip.”

144. Indeed, Haba (a reference on which Petitioners rely in co-pending IPR2026-00065) demonstrates that solder/bumps (as described in Sundaram) are not considered part of the alleged “second semiconductor chip.” Instead, solder/bumps (as described in Sundaram) are structures that are separate from a semiconductor chip and that are used to connect other components to contacts/pads of the semiconductor chip. EX1161 [Haba], 6:39-47 (“In the interconnection component of FIG. 8 end surfaces 10B can be wettable *contacts used to connect posts 10 to another component using solder balls or other conductive materials*. For example, in FIG. 10A, *end surfaces 10B are used to join posts 10 to solder balls 32, which are, in turn, joined to contacts 50 on a microelectronic element 6*. Other materials can be used in place of solder balls 32 to join features of the components of the assembly such as tin indium or a conductive matrix.”) (emphasis added); 7:42-56 (“As shown in FIGS. 10A and 10B, interconnect component 2 in either of the forms shown 9 and 10A, respectively, can be used to connect two components with

respective contacts having different pitches or other different configurations. In the example shown in FIG. 10A microelectronic element 6 has contacts 50 having a smaller pitch than the pitch of contacts 52 on printed circuit board (“PCB”) 12. Contacts 52 of PCB 12 are joined to end surfaces 10B, which act as wettable contacts therefor, and contacts 50 of microelectronic element 50 are joined to vias pads 34 of interconnection component 2, which is inverted with respect to the depiction of FIG. 8. The embodiment shown in FIG. 10B is similar to that which is shown in 10A, except that *pads 34 which overlie end surfaces 10B act as wettable contacts for attachment to contacts 52 of PCB 12 using solder balls 32.*) (emphasis added); 8:27-29 (“For example, an interconnection component can be disposed on and connected to a PCB that includes an electrically conductive EMI shield. *The end surfaces of the posts can then be solder bonded to contact pads of the PCB* with the EMI shield being ball-bonded to a peripheral trace of the interconnection component for grounding to the shield.”) (emphasis added); 11:33-35 (“Further, *circuit panel 96* can be of a similar structure to PCB having contacts 52 thereon, and *can connect to interconnection component 2 using solder balls 32 or the like.*”) (emphasis added).

145. Claim 6 also requires “wherein said second semiconductor chip comprises a second metal bump on a second metal pad of said second semiconductor chip.” EX1001 [’306 Patent], cl. 6. Based on Sundaram’s disclosure, bump/solder (gray) is formed on a die pad 135 of the interposer 105 and, thus, is not on a metal

pad of the semiconductor chip. The Petition identifies the “second metal pad” as the component shown in purple above and the “second semiconductor chip” in pink above. Pet., 42. Sundaram (and the Petition) therefore places the alleged “second metal bump” on the interposer 105 and the alleged “second metal pad” on the alleged semiconductor chip. Thus, the alleged “second metal bump” is not on the alleged “second metal pad.” The alleged “second metal bump” is on the die pad 135 (yellow) of the interposer 105. In addition, the “second semiconductor chip” does not comprise a second metal bump because the alleged second semiconductor chip does not comprise the bump/solder (gray) (the second metal bump) – the bump/solder (gray) is part of the interposer.

146. The mismatch described above – the alleged “second metal bump” on the interposer 105 and the alleged “second metal pad” on the alleged second semiconductor chip – follows at least partially from the fact that Sundaram does not describe the pads or interconnects of electronic device 130. The Petition does not identify any disclosure of those structures and certainly does not explain the component shown above or what it is made of.

147. Dr. Shanfield’s declaration refers back to his analysis of claim 1(e)(ii). EX1003 [Shanfield Decl.], ¶198. Thus, my analysis in Section XI.A.1 (claim 1(e)(ii)) addresses his analysis of claim 6.

148. The Petition's combination of Sundaram and Lin-191 fails because it does not teach or suggest the "second semiconductor chip comprises a second metal bump on a second metal pad of said second semiconductor chip."

7. Claims 10 and 18 are Patentable For the Same Reasons as Claims 1 and 6.

149. For limitations 10(a)(iii), 10(c)(iii), 10(f)(ii), 18(a)(iii), 18(c)(iii), 18(d)(i), and 18(d)(ii), the Petition cross-references claim 1 and relies on the same analysis that it uses for claims 1 or 6. Pet., 45-46, 50, 56, 58-60. Because the Petition relies on the same analysis for claims 10 and 18 as it does for claims 1 and 6, claims 10 and 18 are patentable for the same reasons I have given for limitations 1(a)(iii), 1(c)(iii), 1(e)(ii), 1(e)(iii) and claim 6 above.

8. Claims 2 and 14 are Patentable.

150. Claims 2 and 14 recite a chip comprising "a central-processing-unit (CPU) circuit block and a graphics-processing-unit (GPU) circuit block." EX1001 ['306 Patent], cls. 2, 14. The Petition relies on Lin-191's disclosure of a system-on-chip including CPU and GPU circuit blocks and proposes substituting such a chip for Sundaram's memory device. Pet., 30-33, 52. That substitution is supported by a generic assertion of "increased capabilities." But the Petition does not explain why a POSITA would convert Sundaram's specific stacked-memory embodiment into a CPU/GPU system-on-chip.

151. The Petition states that although “Sundaram’s FIG. 3 depicts device 125 as stacked memory, Sundaram teaches ‘other electronic devices can also be used as the first electronic device 125.’” Pet., 31. The Petition also notes that “Sundaram discloses ‘smart and mobile phone applications, including video streaming, 3D graphics, camera-functions, and gaming’ and contemplates ‘high power logic component[s]’ for device 125.” Pet., 31-32 (citing EX1003 [Shanfield Decl.], ¶179).

152. This rationale, however, is inconsistent with the architecture Sundaram describes. Sundaram pairs a memory device on one side of the interposer with a logic device on the other: “the first electronic device 125 can be single or stacked memory IC devices, and the second electronic device 130 can be a logic IC device or devices.” EX1004 [Sundaram], 6:37-39. The purpose of that arrangement is to provide very high bandwidth between a logic device and a memory device across a short, dense interconnect.

153. Using a central-processing-unit circuit block and a graphics-processing-unit circuit block as part of (or instead of) device 125 would place logic circuitry on both sides of the interposer and would remove the memory device that Sundaram’s architecture is designed to serve. Sundaram’s references to mobile phone applications and to high power logic components describe the demands that motivate Sundaram’s logic-to-memory architecture. Thus, these references do not

suggest converting the memory side of that architecture into a second logic device. For this reason, and for the reasons discussed above, a POSITA would not have been motivated to combine Lin-191 and Sundaram to arrive at claims 2 and 14.

B. Ground 1B (Sundaram, Lin-191, and Lin-863)

1. Sundaram and Lin-863 Do Not Teach or Suggest “No [] Copper Post in Said First Region.”

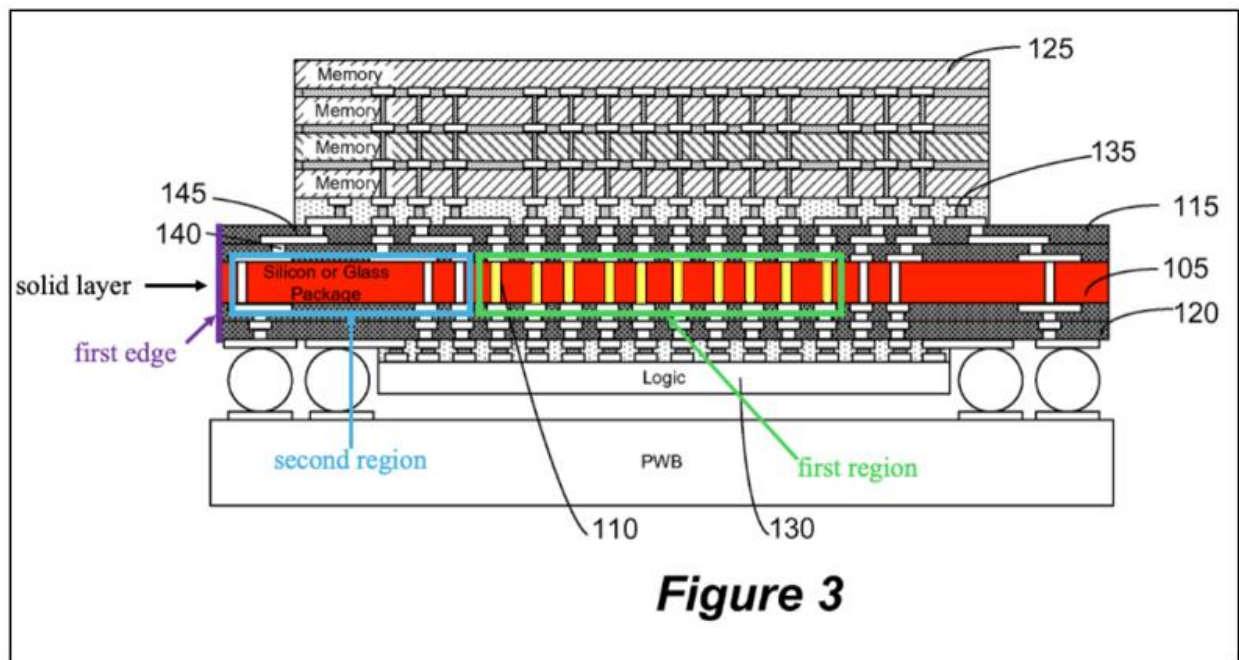
154. Claim 12 requires “no[] copper post in said first region.” EX1001 [’306 Patent], cl. 12; *see* Pet., 89 n.8 (Petitioners “interpret the claimed no any copper post to be ‘no copper post.’”) (emphasis removed).

155. The Petition asserts two bases to demonstrate that that there are no copper posts in the alleged first region in the allege prior art. First, the Petition relies on Sundaram’s Figure 4, reasoning that because “die-to-die vias connecting pads are at the periphery” and “die-to-PWB vias are located outside the peripheral area of the smaller device, a POSITA would have understood Sundaram as teaching the first region as having no copper plugs.” Pet., 90 (citing EX1003 [Shanfield Decl.], ¶¶301-302). Second, the Petition relies on Lin-863’s Figures 9a-9b as showing a first region with “no copper . . . post[s].” Pet., 90-92 (citing EX1007 [Lin-863], Figs. 9a-9b; EX1003 [Shanfield Decl.], ¶¶303-305) (emphasis removed). Petitioners’ analysis is flawed.

a. Sundaram Does Not Teach or Suggest the Limitation.

156. My analysis in Section XI.A.5 with regard to “first region” applies to Claim 12 as well.

157. Figure 3 of Sundaram specifically shows through vias 110 having metal posts (yellow highlights) in the alleged first region.

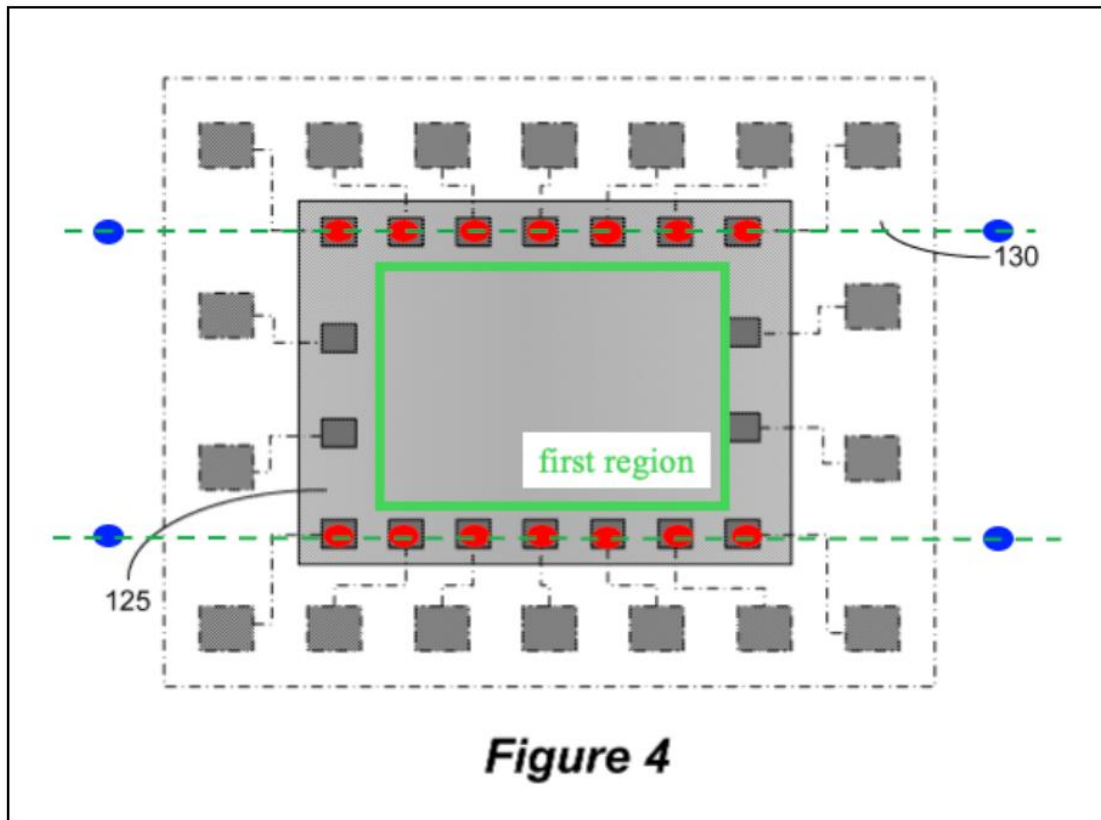
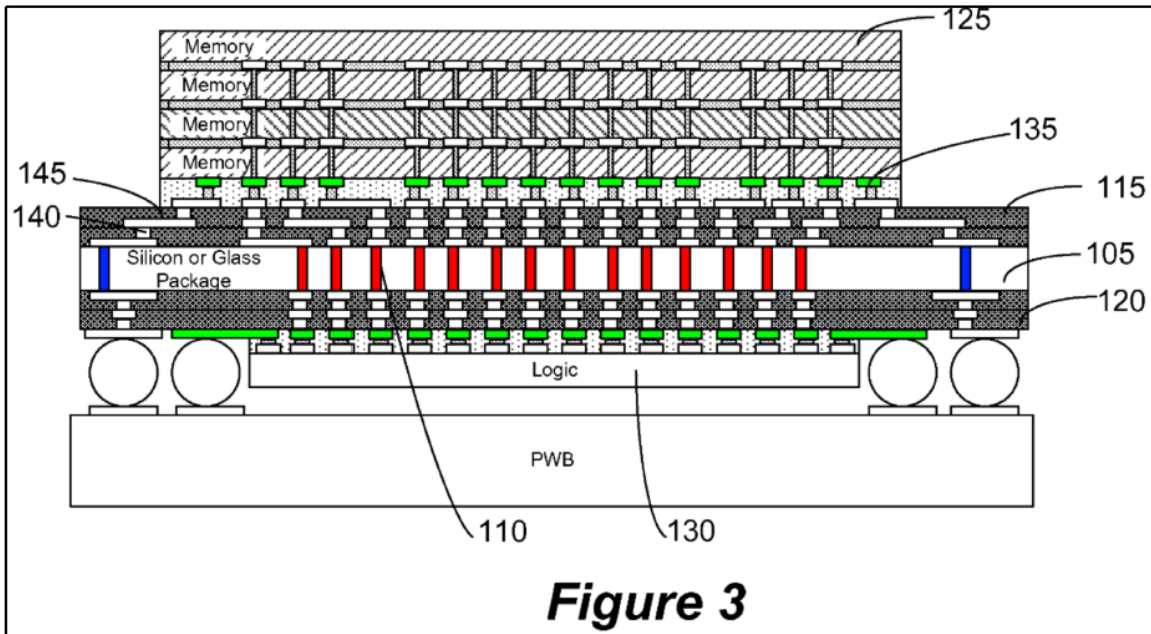


Pet., 8 (citing EX1004 [Sundaram], Fig. 3 (annotated by Petitioners; I have added the yellow highlights)).

158. Sundaram teaches that these metal posts can be copper. (EX1004 [Sundaram], 6:22-27).

159. Sundaram’s disclosure demonstrates that there would be metal (copper) posts in the alleged “first region.” Sundaram states that its interposer “electrically

connects the first and second set of devices at the same or similar through-via density as in the first and second electronic devices,” and expressly distinguishes this arrangement from prior-art interposers, whose vias “were generally of the same surface-mount pitch as the board, typically from 400-1000 microns.” EX1004 [Sundaram], 5:25-35. Sundaram’s interposer instead operates “at device pitch of 10-30 microns.” *Id.* Sundaram further states that its through vias 110 “are electrically and thermally conducting, and are distributed within the interposer such that they provide localized thermal isolation or thermal conduction between the first and second electronic devices.” *Id.*, 6:16-19. A via arrangement designed to match a device’s own fine, area-distributed I/O pitch, and to provide “localized” thermal management at points across the device, is inconsistent with having no metal posts in the alleged first region of Sundaram. Figure 3’s cross-section, reproduced above, is consistent with this description: through vias 110 run continuously across the entire width of the alleged first region.



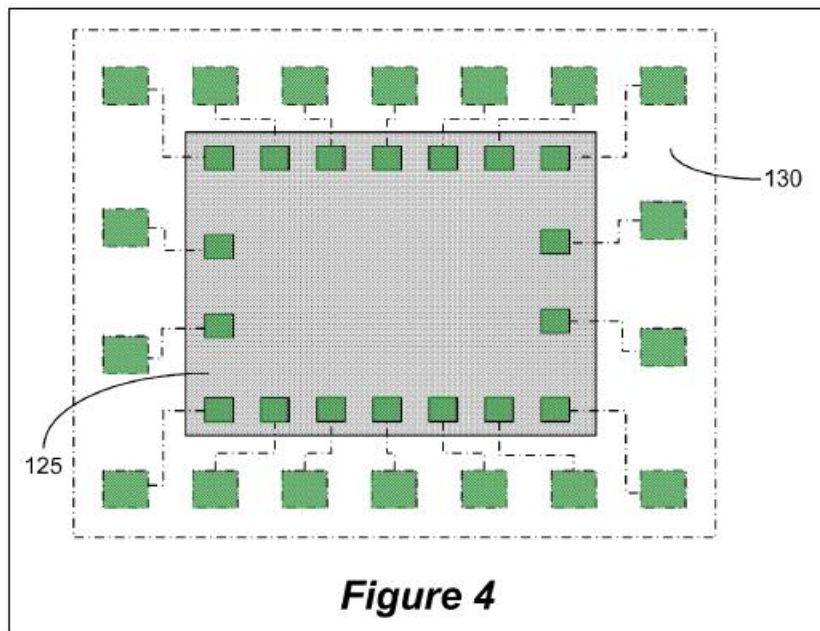
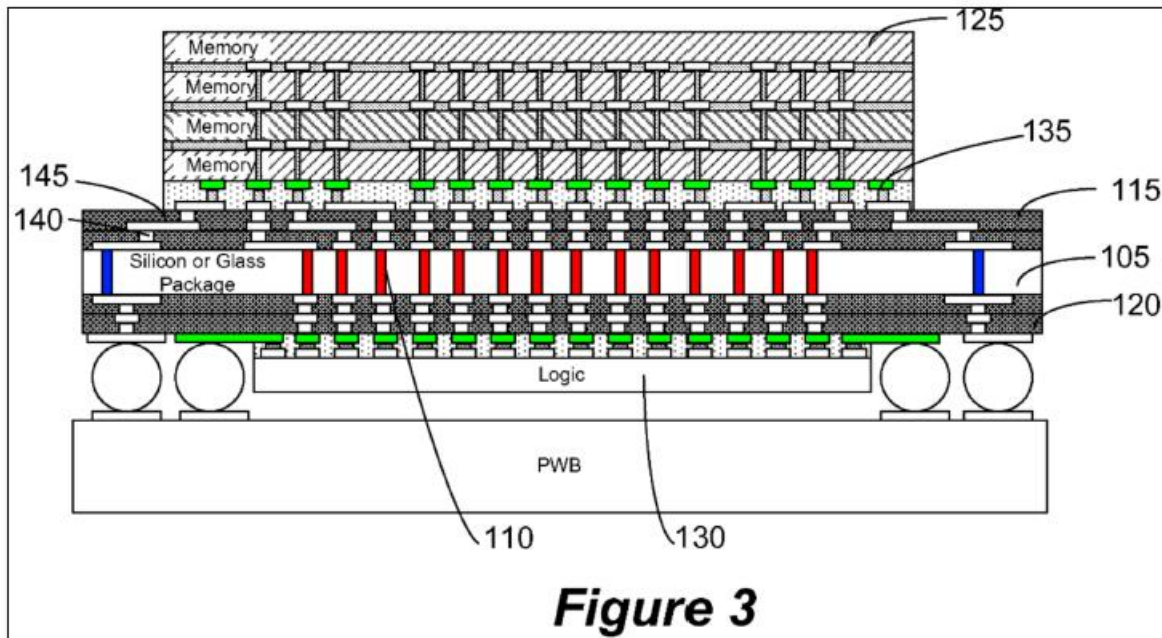
Pet., 81, 90 (annotated by Petitioners).

160. Sundaram does not annotate location of the metal posts 110 in Fig. 4. Without any support in the specification and without providing any reasoning, as shown above, Petitioners annotate Figure 4 to (1) include blue circles and red circles representing metal posts shown in Figure 3, and (2) add dashed lines which purportedly show the location from where the cross section of Figure 3 is taken. Petitioners' annotations of Figure 4 are wrong.

161. As a threshold matter, without any indication in Sundaram where the cross-section of Figure 3 was taken from in Figure 4, a POSITA would assume Figure 3 would be a cross-section through the middle of Figure 4, not along some random location (green dashed lines) as Petitioners have done. Pet., 83 (“The **dashed lines in FIG. 4** illustrate exemplary cross-sectional lines corresponding to FIG. 3’s cross-section.”) (color in original). The Petition treats the dashed lines in Figure 4 as depicting the specific location of “die-to-die vias 110.” Pet., 80-81 (citing EX1003 [Shanfield Decl.], ¶¶291-292). Sundaram’s specification, however, does not support that reading. Nowhere does Sundaram teach or suggest the location of Petitioners’ annotated green dashed lines.

162. Figure 4 is simply a top view of Figure 3. Thus, the features shown on Figure 4 should match up with the features of Figure 3. Even using Petitioner’s own view of the cross section location of Figure 3, Petitioners’ annotations of Figure 3 and 4 do not match up, thus, demonstrating that Petitioners’ annotations on Figure 4

are wrong and Petitioners' analysis is flawed. For example, annotated Figure 4 shows seven (7) metal posts in red ovals. But annotated Figure 3 shows fourteen (14) metal posts in red. Further, the location and spacing of the annotated metal posts (red) in Figure 4 do not match up with the annotated metal posts (red) shown in Figure 3. For these reasons, Petitioners' drawing of metal posts as red ovals outside of the alleged "first region" in Figure 4 is incorrect. The metal posts (red) shown in Figure 3 are within the alleged "first region." Given that Figure 4 is a top view of Figure 3, the configuration of the interposer 105 (and its metal posts 110) in Figure 3 are simply not visible in Figure 4.



Pet., 81 (annotated by Petitioners).

163. As shown above, Petitioners provide additional annotations that further demonstrate that their understanding of Figures 3 and 4 is wrong. Petitioners asserts that the green highlight boxes in annotated Figure 4 above are the green pads shown

in annotated Figure 3. Pet., 70-71. Once again, the annotations for Figures 3 and 4 do not match. As shown above in annotated Figure 3, there are sixteen (16) green pads at the bottom of interposer 105 and sixteen (16) green pads underneath the memory of device 125. Annotated Figure 4, however, only shows seven (7) green pads on the bottom of interposer 105 and seven (7) green pads underneath memory of device 125.

164. Based on Petitioner's annotation, Petitioners position is that their annotated green boxes in Figure 4 (above) must necessarily line up with through vias 110 (and their metal post (annotated in red ovals above). This is also wrong. In particular, Sundaram discloses that devices 125 and 130 can be connected with "through vias 110, blind vias 140, and conductor traces 145." EX1004 [Sundaram], 7:1-9. Sundaram elsewhere explains that this combination of structures exists to let a die's pad layout differ from, and be routed laterally to, the through-via pattern of the interposer: "electronic devices having different I/O pad layouts and sizes can also be connected through the use of blind vias 140 and conductor traces 145 defined within polymer-metal redistribution layers deposited on the first side 115 and second side 120 of the interposer 105." *Id.*, 6:62-67. Because a pad's connection may be completed through a lateral trace rather than a via positioned directly beneath it, the position of a pad in Figure 4 does not establish where the physical location of associated through vias 110.

165. Notably, Petitioners assert that Figure 4, as labeled by Sundaram, is inconsistent with Figure 3. In Figure 3, first electronic device 125 is drawn larger than second electronic device 130, while in Figure 4 as labeled, device 130 is the larger of the two. Pet., 82 n.7 (citing EX1003 [Shanfield Decl.], ¶293). The Petition resolves this inconsistency by relabeling Figure 4, concluding that “a POSITA would have understood Sundaram’s FIG. 4 to mislabel devices 125, 130.”¹ *Id.* The Petition’s analysis with regard to claim 12, depends on accepting this relabeling as correct. To a POSITA, a figure that must be relabeled before it can be read consistently with Figure 3 is not a reliable basis to demonstrate unpatentability and satisfy the claim limitations.

¹ Under this position, Figure 4 would also be described incorrectly. Figure 4 is supposed to simply be “a top view of the interconnect structure illustrated in FIG. 3.” EX1004 [Sundaram], 3:27-28; *see also id.*, 7:1-4.

b. Combining Sundaram and Lin-863 Does Not Disclose a First Region with No Copper Posts and There is No Motivation to Combine.

166. The Petition seeks to combine Lin-863 (shown below) with Sundaram. But this combination does not result in a structure with no copper posts in the alleged first region of Sundaram.

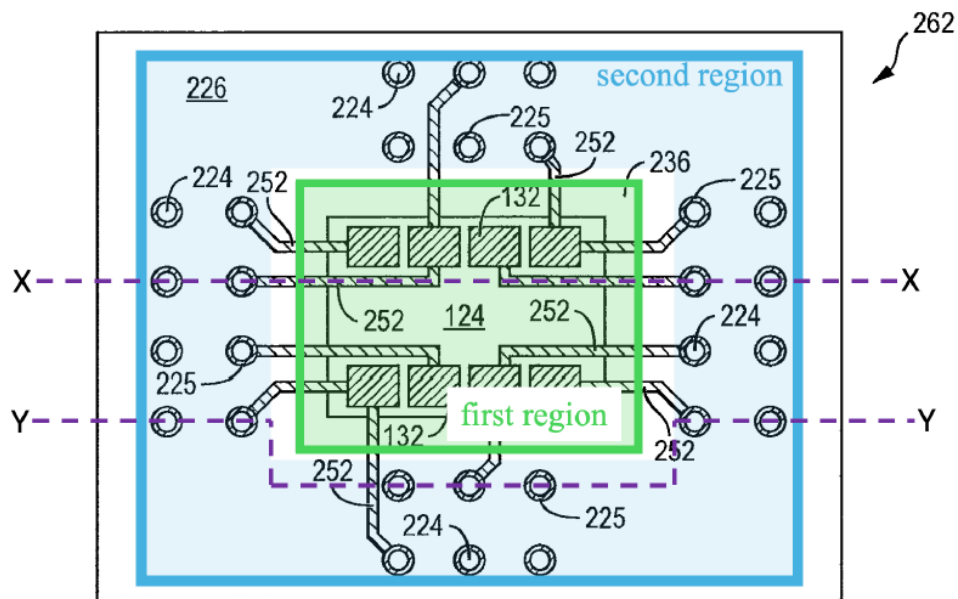


FIG. 9b

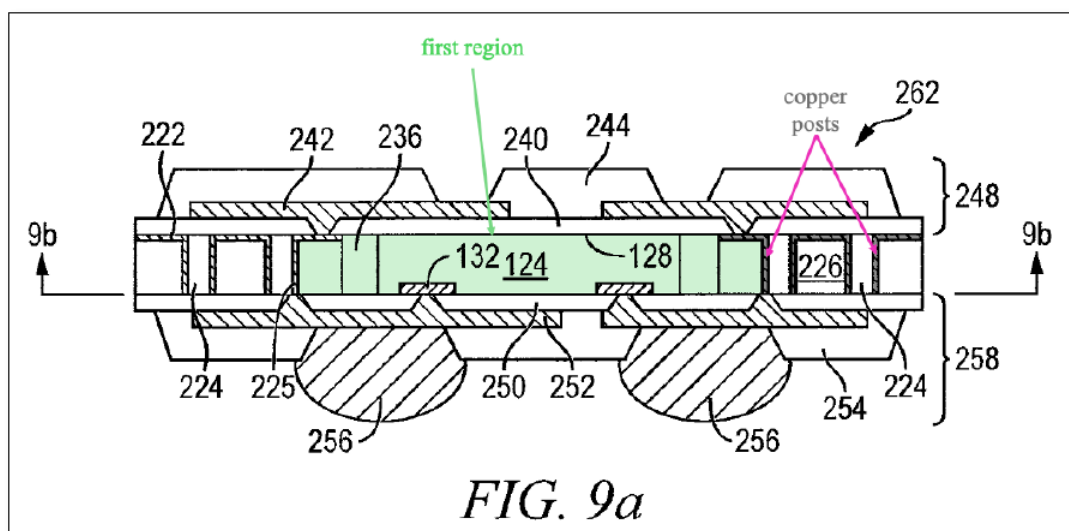


FIG. 9a

Pet., 91-92.

167. The Petition asserts that “[a] POSITA would have found obvious and been motivated to modify Sundaram’s first region per Lin-863’s teaching to accommodate space for an additional semiconductor chip to be included in Sundaram’s package.” Pet., 92 (citing EX1003 [Shanfield Decl.], ¶274) (emphasis removed). I disagree and Petitioners’ analysis misses the point.

168. Sundaram discloses a configuration where two devices 125, 130 are connected using an interposer 105. The electrical connections between these devices are specifically made using numerous metal posts in the alleged first region. A POSITA would not remove the metal posts in the alleged first region of Sundaram merely because Petitioners can identify some region in Lin-863 between metal posts (coppers posts) that do not have metal posts. If the metal posts were removed, the configuration shown in Sundaram would no longer operate to allow the 125, 130 devices to communicate with each other, which is the entire point of Sundaram. Further, even assuming that Lin-863 taught a person the need to accommodate space for additional devices in Sundaram’s package shown in Figure 3, that would not lead a POSITA to remove the metal posts that connect those devices through the interposer 105. Given the way Sundaram is configured, there would be still be metal posts in the alleged first region to connect these additional devices.

169. There is no motivation to combine Sundaram and Lin-863. Sundaram discloses a thin glass (silicon-oxide) interposer whose fine, device-pitch through vias 110 are designed to match the I/O density of the attached chips. EX1004 [Sundaram], 5:25-29, 6:11-15. Lin-863, on the other hand, discloses a fan-out, chip-scale package in which conductive TMVs are drilled through a thick organic molding compound to route signals to external contacts for package-on-package stacking. EX1007 [Lin-863], 8:4-9, 12:51-54. The Petition identifies no problem in Sundaram that Lin-863's rectangular TMV arrangement would solve, and no teaching in either reference suggesting that Sundaram's copper-post-in-through-via arrangement should be reorganized to resemble Lin-863's mold-compound via layout. A POSITA presented with Sundaram would have had no reason to look to Lin-863.

170. There would have been no reasonable expectation of success in combining Sundaram and Lin-863. Lin-863 is a product of Lin-863's *material* and the *process* used to build it, both of which are fundamentally different from Sundaram. Lin-863's TMVs are formed by laser or mechanical drilling through a comparatively thick (100–450 micrometer) organic molding compound — an epoxy resin loaded with silica filler — and are “about 50–350 μm ” wide. EX1007 [Lin-863], 7:67–8:9, 12:51-54. That is a soft, machinable, organic composite whose surfaces are readily metallized. Unlike Lin-863, Sundaram's interposer is the opposite kind of material: a thin (in preferred embodiments “about 30

micrometers”), monolithic, *inorganic* glass or silicon layer, in which fine 1–25 micrometer through vias are formed by excimer-laser ablation of glass or by etching (not by drilling a compliant compound). EX1004 [Sundaram], 5:25-54. Sundaram itself cautions that glass is “a brittle material [] prone to cracking,” requiring double-side polymer lamination merely to be handled without fracturing (EX1004 [Sundaram], 10:15-22) and that “direct wet metallization on glass has been a challenge due to [the] surface chemistry of glass and its interaction with metals”. EX1004 [Sundaram], 9:57-60. A POSITA would therefore understand that Lin-863’s coarse, drilled via pattern in a thick organic compound cannot simply be reproduced in Sundaram’s thin, brittle, monolithic glass or silicon: the drilling geometry and 50–350 μm via width Lin-863 relies on would risk fracturing Sundaram’s ultra-thin glass. Lin-863’s vias are an order of magnitude coarser than the 1–25 μm vias Sundaram forms to match its chip’s I/O pitch. Further, Sundaram’s inorganic glass or silicon surface requires metallization chemistry that Lin-863’s organic-compound process does not address. The Petition offers nothing to bridge these material-level and process-level differences. Thus, a POSITA would not have had a reasonable expectation of successfully when combining Lin-863 and Sundaram.

C. Ground 2A (Yu and Lin-191)

1. Yu Does Not Teach or Suggest That a “First Semiconductor Chip Comprises a Third Metal Interconnect on a First Metal Pad of Said First Semiconductor Chip.”

171. Limitation 1(e)(ii) requires a “first semiconductor chip comprises a third metal interconnect on a first metal pad of said first semiconductor chip.” EX1001 [’306 Patent], cl. 1. Yu does not disclose this limitation. As with Sundaram in Ground 1A, the structure the Petition identifies as the alleged “third metal interconnect” is not an interconnect that is part of the alleged semiconductor chip.

172. For limitation 1(e)(ii), the Petition asserts that Yu’s “die 52, such as a memory die,” is the “first semiconductor chip,” and Yu’s connector 54 is the “third metal interconnect.” Pet., 105, 108 (quoting EX1010 [Yu], 4:30-36, Fig. 16) (citing EX1003 [Shanfield Decl.], ¶¶342, 345-348) (emphasis removed). The Petition states that die 52 is ““attached . . . to conductive features in the second back side metallization layer 42, such as by conductive connectors 54, like controlled collapse chip connection (C4) bumps,”” and that “[a] connector 54 is a third metal interconnect because it connects die 52 ‘to conductive features’ in layer 42.” Pet., 108 (quoting EX1010 [Yu], 4:30-34) (emphasis removed).

173. Whether connector 54 connects die 52 to layer 42 is not the point. The claims require that the semiconductor chip (alleged to be die 52) *comprise* the “third metal interconnect” (alleged to be connector 54). Connector 54, however, is not part

of die 52. Petitioners ignore that connector 54 is described as a material deposited on (bonded to) the layer 42 and then die 52 is attached to the connector.

[A] second die 52, such as a memory die...is attached through the opening 46 to conductive features in the second back side metallization layer 42, such as by conductive connectors 54, like *controlled collapse chip connection (C4) bumps*. The second die 52 may be attached using an acceptable pick-and-place tool and *reflowing connectors 54* between the second die 52 and the conductive features in the second back side metallization layer 42. Accordingly, the connectors 54 may be a *bump on trace (BOT)*.

EX1010 [Yu], 4:30-39 (emphasis added). C4 bumps, reflowing connectors, and BOTs are all features that are deposited on layer 42. These type of connectors sit between die 52 (the alleged semiconductor chip) and layer 42 and are used to attach die 52 to layer 42.

174. By the Petition's own description, Yu's connector 54 is a structure that joins die 52 to the "conductive features in the second back side metallization layer 42" of the package. EX1010 [Yu], 4:30-34. A POSITA would understand connector 54 to sit between the die 52 and layer 42, serving to connect the two. It is not a metal interconnect that is part of die 52 nor is it formed on a metal pad of die 52.

175. Indeed, Dr. Shanfield admits that connector 54 sits between die 52 and layer 42 and, thus, connector 54 is not part of die 52 (the alleged semiconductor chip).

The “basic idea of C4 is to connect chips (semiconductor devices), chip packages, or such other units by means of *solder bumps **between** two surfaces* of the units.”. The “tiny bumps of electrically conductive solder *bridge the gaps between respective pairs of metal pads on the units being connected*. Each pad has a corresponding pad on the other unit’s surface; the pad arrangements are mirror images. *As the units are pressed together and heated the solder bumps on the pads of the first unit are contacted with corresponding conductive pads (having no bumps) on the second unit and reflowed*, partially collapsing the solder bumps and making connections between respective pads”

EX1003 [Shanfield Decl.], ¶70 (citing EX1129 [Fanti], 1:9-17, 1:17-26) (emphasis added).

176. Thus, connectors 54 are not part of die 52 and the claim limitation is not met.

177. Yu also does not disclose that the semiconductor has a first metal pad. As with Sundaram, Yu does not describe any pads or interconnects of die 52. The Petition does not identify any disclosure in Yu of a metal pad on die 52. Instead, the

Petition states that “a POSITA would have understood die 52 includes die pads (unlabeled) such that an electrical connection is made between die 52 and other devices.” Pet., 108 (citing EX1003 [Shanfield Decl.], ¶¶345-347). Thus, the Petition assumes what a die would include rather than relying on the teaching of Yu. The existence of the alleged metal pad as part of the semiconductor is merely an assumption drawn from C4 packaging practice and from EX1095 (EX1003 [Shanfield Decl.], ¶348) rather than a disclosure of Yu.

178. Notably, Dr. Shanfield’s declaration maps Yu’s connector 54 in two inconsistent ways. He asserts that connector 54 is both the claimed “third metal interconnect” and “first metal pad.” Connector 54 cannot be both. For limitation 1(e)(ii), Dr. Shanfield identifies connector 54 as the “third metal interconnect.” EX1003 [Shanfield Decl.], ¶347 (“connector 54 functioning as *a third metal interconnect*”). But Dr. Shanfield also identifies connector 54 as the claimed “first metal pad,” stating that “Yu already teaches die 52 comprising connector 54, i.e., the claimed first pad,” and that a POSITA “would have been motivated to modify Yu’s connector 54 to be a first metal pad.” EX1003 [Shanfield Decl.], ¶349 (emphasis removed). The same structure – connector 54 – cannot be both the “third metal interconnect” and the “first metal pad” on which the “third metal interconnect” sits. This inconsistency confirms that the Petition has not identified in Yu a

semiconductor chip comprising a “third metal interconnect” or a “third metal interconnect on a first metal pad of said first semiconductor chip.”

179. The Petition’s reliance on Lin-191 for the “metal pad” does not remedy the deficiency regarding a different component – “third metal interconnect,” for the reasons discussed above in connection with limitation 1(e)(ii) of Ground 1A.

2. Yu and Lin-191 Do Not Teach or Suggest the Layered “Third Metal Interconnect” and There Is No Motivation to Combine.

180. Limitation 1(e)(iii) requires that “said third metal interconnect comprises a third metal layer on said first metal pad and a third copper layer over said third metal layer, wherein said third copper layer has a thickness between 5 and 30 micrometers.” EX1001 [’306 Patent], cl. 1. For the layering, the Petition does not rely on Yu. Instead, it relies on Lin-191 and expressly incorporates its Ground 1A analysis: “Lin-191 teaches or renders obvious interconnects/bumps with layers/thickness as recited in Claim 1(e)(iii). *See* Section V.A.18.” Pet., 109. For the reasons I gave above in connection with limitation 1(e)(iii) of Ground 1A, Lin-191 does not supply the claimed “third metal layer” — according to Petitioners, its adhesion layer 711 and seed layer 712 are two distinct layers of different materials serving different functions, EX1005 [Lin-191], ¶¶[0389]-[0392]. The Petition’s merger of these layers and treating them as a single layer is inconsistent with its own mapping of claim 3(c) and limitation 1(d)(i). Pet., 17-18, 37-38.

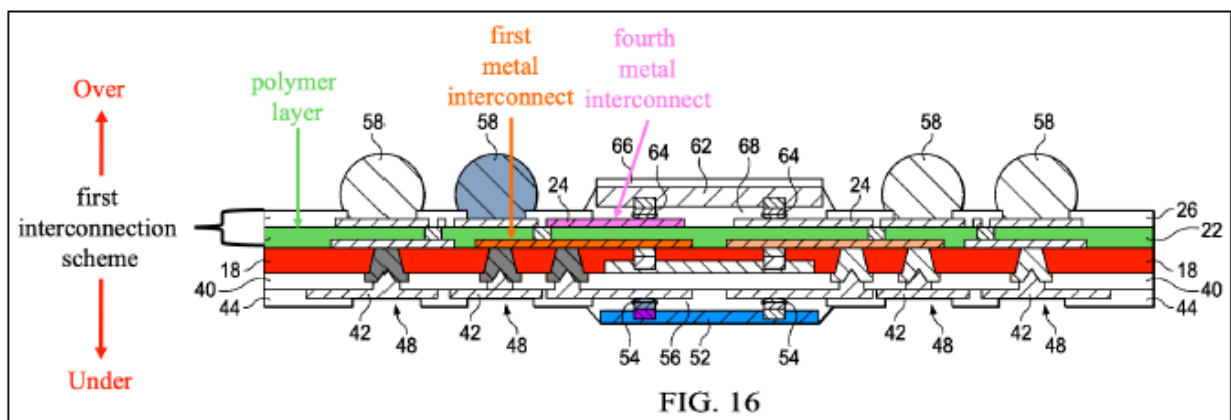
181. The Petition’s reliance on Yu’s connector 54 introduces a further problem. The Petition identifies connector 54 as a “controlled collapse chip connection (C4) bump[.]” Pet., 108 (quoting EX1010 [Yu], 4:30-34). A POSITA would understand a C4 bump to be composed of solder, not a layered structure of an adhesion layer, a seed layer, and a thick electroplated copper layer of the kind Lin-191 describes and limitation 1(e)(iii) requires. The Petition does not explain how a C4 solder bump would be reconstructed to comprise “a third metal layer on said first metal pad and a third copper layer . . . between 5 and 30 micrometers,” and Yu does not describe connector 54 as having that construction.

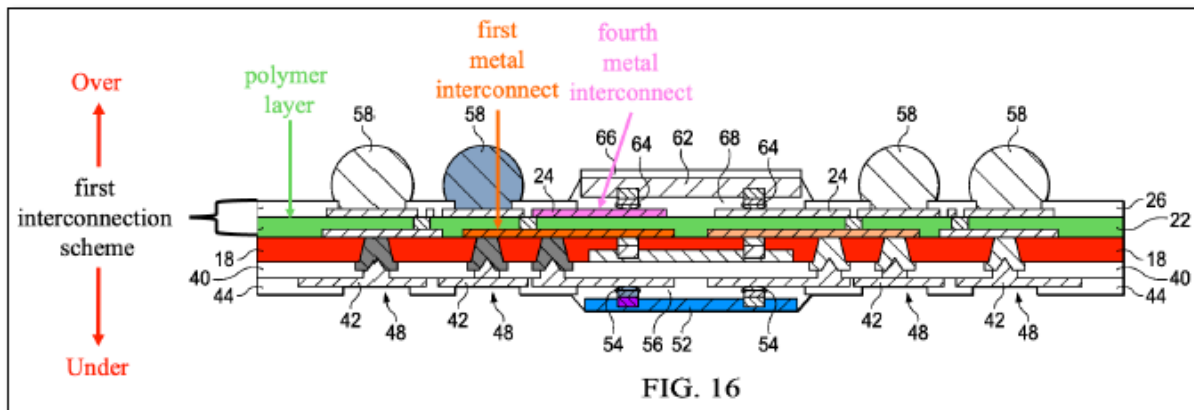
182. As to motivation, the Petition states that “[a] POSITA would have found obvious and been motivated to modify Yu’s connector for the reasons discussed with respect to Sundaram, i.e., improved metallurgical bonding and increased resistance to fatigue and stress-induced failure.” Pet., 110 (citing EX1003 [Shanfield Decl.], ¶¶351-352). Because the rationale is the same as for Sundaram, the deficiencies that I identified in Ground 1A apply here as well. Lin-191 does not attribute the asserted advantages to its adhesion and seed layers, and the Petition identifies no specific diffusion, oxide, or adhesion problem with Yu’s connector that Lin-191’s added layers would remedy. The Petition’s further assertion that “[l]ayered bumps, per Lin-191, were routinely manufactured using techniques contemplated by Yu” (Pet., 110 (citing EX1003 [Shanfield Decl.], ¶¶351-352)),

establishes at most that such bumps were known, not that a POSITA would have reconstructed Yu's C4-bump connector into the specific layered "third metal interconnect" the claim recites.

3. The Petition Does Not Identify a "Fourth Metal Interconnect."

183. Claim 3(a) requires "a fourth metal interconnect." As shown below, the Petition identifies the "first metal interconnect" in orange. The Petition identifies the "fourth metal interconnect" as "second metallization layer 24" (pink in the upper figure below) or "a third metallization layer" on layer 26 (abstractly notated by "location of fourth metal interconnect" in pink in the lower figure below). Pet. 111-112 (citing EX1010 [Yu], 3:28-32; EX1003 [Shanfield Decl.], ¶¶357-359).





184. The claim requires both a first metal interconnect and a fourth metal interconnect—that is, the claim requires two separate interconnects. As discussed below, what the Petition identifies as the first metal interconnect and the fourth metal interconnect are actually different metal layers that are part of one (the same) metal interconnect. Thus, the Petition has not identified two separate interconnects – a first and fourth interconnect.

185. Claim 3 confirms that the first and fourth metal interconnects are separate. Claim 3 recites “a fourth metal interconnect over said first metal interconnect and said first polymer layer, wherein said first polymer is between said first and fourth metal interconnects.” EX1001 [’306 Patent], cl. 3. The claim thus places the first polymer layer between the first and fourth metal interconnects and recites no electrical connection between them. A POSITA would understand claim 3 to require a fourth metal interconnect that is a separate interconnect from the first metal interconnect, not an upper level of the same conductive path.

186. The Petition, however, identifies the “first metal interconnect” as a portion of Yu’s first metallization layer 20 and the “fourth metal interconnect” as Yu’s second metallization layer 24 (or a further metallization layer). Yu describes metallization layers 20 and 24 (and a further metallization layer) as successive levels of a single redistribution structure – the metallization layers that the Petition points to are in the same conductive path. Thus, they are part of the same metal interconnect – they cannot be two different metal interconnects are required by the claim.

187. Yu states that “[a] first ILD layer 22 is deposited on the front side and over the first metallization layer 20,” that “[o]penings may be formed through the first ILD layer 22 to the first metallization layer 20,” and that “[c]onductive material deposited during the formation of a subsequent metallization layer may be deposited in openings of the previously formed ILD layer to electrically couple respective metallization layers.” EX1010 [Yu], 3:20-35.

188. The conductive material occupying the openings in the first ILD layer 22 joins the first metallization layer 20 and the second metallization layer 24 into a single conductive path. Those two portions are not separate conductive paths. They are an upper and a lower portion of the same path, and a signal entering one portion passes directly into the other. A POSITA would not understand vertically stacked, electrically coupled portions of one conductive path to be the separate “first metal interconnect” and “fourth metal interconnect” that claim 3 requires.

189. Indeed, the Petition’s mapping depends on the very connection that claim 3 forecloses. The Petition relies on Yu’s teaching that successive metallization layers are “electrically couple[d]” through the conductive material in the ILD openings. EX1010 [Yu], 3:25-32. But claim 3 requires the first polymer layer to lie between the first and fourth metal interconnects, with no connection between them recited. The structure the Petition identifies—two metallization layers joined through the intervening dielectric—is therefore not the separate first and fourth metal interconnect claim 3 requires. They are different layers of the same interconnect.

190. For these reasons, the Petition has not shown that Yu teaches or suggests the “fourth metal interconnect” of claim 3. When the Petition identifies the claimed “first metal interconnect” as a portion of metallization layer 20 and the claimed “fourth metal interconnect” as metallization layer 24, it is identifying two layers of the *same* metal interconnect. The Petition has identified only one metal interconnect but the claim requires two metal interconnects.

4. Yu and Lin-191 Do Not Teach or Suggest the Claimed Thickness of the Claimed Solid Layer.

191. Claims 1 and 18 recite a solid-layer thickness “between 50 and 150 micrometers.” EX1001 [’306 Patent], cls. 1 and 18. Claim 10 recites a solid-layer thickness of “between 100 and 300 micrometers.” EX1001 [’306 Patent], cl. 10. Yu

discloses no thickness for its molding compound. The Petition therefore relies on thickness from Lin-191. In particular, the Petition relies on Lin-191's *encapsulating layer 85* being "between about 20 and about 500 micrometers, and preferably between 30 and 100 micrometers," and, alternatively, on a computed range of "between 23.011 micrometers and 121.3 micrometers." Pet., 95-97; EX1005 [Lin-191], ¶¶[109-111] [0121], [0050], [0060]; EX1003 [Shanfield Decl.], ¶¶317-319.

192. The "23.011 to 121.3 micrometers" range does not appear in Lin-191. The Petition computes this range by adding the separately disclosed dimensions of Lin-191's bump 14 and metallization sublayers 11, 12, and 13. Pet., 96 (citing EX1005 [Lin-191], ¶¶[0050], [0060], [0121]). The resulting sum is the height of a stacked bump and metallization assembly. It is not a thickness that Lin-191 teaches for its encapsulating layer 85, and it is not a thickness for any structure resembling the claimed solid layer. The Petition's cross-reference to Section V.A.4 does not supply the missing teaching. That section addresses Ground 1A, where Sundaram itself discloses a thickness of "about 20 to about 200 micrometers" for its interposer, the structure the Petition maps to the claimed solid layer, and no second reference was needed. Pet., 6 (citing EX1004 [Sundaram], 2:22-25, 5:50-53). In Ground 2A, however, Yu discloses no thickness for its molding compound 18, and Lin-191 does not disclose the number the Petition supplies. The Petition does not explain why a POSITA would add the dimensions of Lin-191's bump and metallization sublayers

and treat the sum as the thickness of Yu's molding compound. The bump and metallization stack provides electrical interconnection, and its height is set by interconnect requirements rather than by the considerations that govern the thickness of a molding compound or solid layer. Thus, the Petition has not shown that Yu and Lin-191 teach or suggest the claimed solid-layer thickness.

5. Yu and Lin-191 Do Not Teach or Suggest the Claimed Thickness of the Third Copper Layer.

193. The Petition makes the same wrong assumption here that it makes in Ground 1A. As discussed above in connection with Ground 1A's limitation 1(e)(iii), the Petition's showing for the third copper layer's thickness depends on treating Lin-191's adhesion layer 711 and seed layer 712 as a single combined "third metal layer" so that metal layer 713 can be characterized as sitting "over" it. But a POSITA would not treat 711 and 712 as a single layer, for the reasons given above: Lin-191 does not describe them as a single layer, and the Petition's own mapping of claim 3(c) and limitation 1(d)(i) treats materially identical adhesion-and-seed-layer pairs as two separate layers..

194. Claim 1(e)(iii) recites that the "third copper layer has a thickness between 5 and 30 micrometers." Ground 2A relies on the same Lin-191 analysis as Ground 1A. Pet., 109-110; EX1005 [Lin-191], ¶[0400]. Dr. Shanfield states that "Lin-191 teaches or renders obvious interconnects/bumps with layers/thickness as

recited in Claim 1(e)(iii),” citing paragraphs incorporated from his Ground 1A analysis. EX1003 [Shanfield Decl.], ¶351 (incorporating EX1003 [Shanfield Decl.], ¶¶168-169). Thus, my analysis above with regard to Ground 1A applies to Ground 2A as well.

195. intentionally omitted.

6. Claims 10 and 18 are Patentable For the Same Reasons as Claim 1.

196. Because the Petition relies on the same analysis for claims 10 and 18 as it does for claim 1, claims 10 and 18 are patentable for the same reasons I have given above for ground 2A.

7. The Claims Are Patentable For Additional Reasons.

a. The Petition Reverses Yu’s First and Second Surfaces Between Claims.

197. Claim 10 recites a “first interconnection scheme ... [comprising] a first metal interconnect over said first surface.” EX1001 [’306 Patent], cl. 10. Dr. Shanfield maps this limitation onto Yu’s Figure 16 only by reversing, from claim to claim, which physical face of Yu he treats as the “first surface.” Dr. Shanfield acknowledges this reversal:

In the mapping for Claim 1, Yu’s front side (where the ILD/RDL structure and connectors 58 are located) was identified as the first surface, and the back side (where die 52 is attached) as the second

surface. For Claim 10, however, the orientation is reversed such that Yu's back side corresponds to the first surface and the front side corresponds to the second surface.

EX1003 [Shanfield Decl.], ¶376; *see also* Pet., 117 (“Claim 10’s mapping reverses Yu’s mapped first and second surfaces and over/under directions relative to Claims 1’s mapping.”). Thus, for the same Figure 16 of the same reference, Dr. Shanfield designates opposite physical faces of molding compound 18 as the “first surface” — and correspondingly flips which direction is “over” and which is “under” — depending on which claim he is applying. He applies language inconsistently without providing any reason to do so.

198. Dr. Shanfield’s own explanation confirms that the surface assignment is driven by the claim language rather than by Yu’s structure. He states that the claim 10 reversal “maintains internal consistency with the structural hierarchy required by Claim 10” and “ensures that ‘over’ and ‘under’ relationships are preserved in accordance with Yu’s figures and descriptions.” EX1003 [Shanfield Decl.], ¶376. In other words, he selects which face of Yu is the “first surface” so that he can attempt to reach each claim’s “over”/“under” recitations on Yu — not because Yu’s structure fixes one face as the “first surface.” Yu’s Figure 16 has a single physical orientation, and the claims use fixed spatial language. A mapping that must assign opposite faces

of that one figure to the “first surface” depending on the claim is not derived from Yu nor would a POSITA do so.

b. Yu and Lin-191 Do Not Teach or Suggest Claim 5.

199. Claim 5 recites that “said compound comprises a SiO₂ compound.” EX1001 [’306 Patent], cl. 5. Because Yu’s molding compound does not supply a silicon-oxygen compound, the Petition proposes to add Lin-191’s SiO₂ insulating layer and define “said compound” as “the combination of Yu’s molding compound 18 and Lin-191’s insulating layer 10.” Pet., 113-114 (citing EX1003 [Shanfield Decl.], ¶¶364-368). This changes the meaning of “said compound” as the Petition sets forth in claim 1 (Yu’s molding compound alone). A POSITA would not have treated Yu’s molding compound 18 — an organic polymer such as epoxy, polyimide, or silicone rubber — and Lin-191’s insulating layer 10 — inorganic silicon dioxide — as a single “compound,” because the two materials have fundamentally different mechanical and chemical properties, including markedly different coefficients of thermal expansion and elastic moduli. EX1010 [Yu], 2:61-65; EX1005 [Lin-191], ¶¶[0052], [0109]. Simply stacking an organic molding compound against an inorganic SiO₂ layer does not yield a homogeneous “compound of silicon and oxygen” as claimed, but rather two chemically and mechanically dissimilar materials merely combined together. The SiO₂ would remain in a separate film rather than in the solid layer as claim 5 requires. Lin-191 itself maintains this distinction. Its

encapsulating layer 85 is separate from insulating layer 10, and Lin-191 lists SiO₂ as a material for layer 10 but not for layer 85. EX1005 [Lin-191], ¶¶[0052], [0109]-[0110]. The Petition identifies no reason for the combination other than to reach the language of claim 5, which is improper hindsight.

D. Ground 2C (Yu, Lin-191, And Camacho)

200. Claim 21 requires that the first semiconductor chip have “a plurality of through-silicon-via metal layers” coupling metal pads at its top and bottom surfaces, with a fourth chip's pad coupled “through a solder layer.” EX1001 [’306 Patent], cl. 21. Yu’s die 52, however, is a plain memory die (C4-attached to the back-side metallization). Die 52 has no through-silicon vias and no top-side pad. The Petition therefore supplies the entire through-silicon-via architecture from Camacho, and recasts Yu’s die 62 as Camacho’s stacked die. Pet., 143-149 (citing EX1006 [Camacho], ¶¶[0041]-[0047]; EX1003 [Shanfield Decl.], ¶¶452-466).

201. This is a wholesale re-architecture of Yu’s package, not the “implementation detail” the Petition calls it.

202. Every structural element of claim 21’s through-silicon-via pathway — the vias, the top and bottom pads coupled through the vias — comes from Camacho’s die 122. Yu contributes only the bare notion of a chip stacked over another chip. Redesigning Yu’s simple C4-attached memory die into a through-silicon-via die bearing pads on both surfaces changes Yu’s structure fundamentally. A POSITA

would not have redesigned Yu's die 52 in this manner. Camacho's through-silicon-via architecture is fabricated at the wafer level, before singulation, by forming conductive layers on opposite surfaces of die 122 and filling vias through the die to connect them. EX1006 [Camacho], ¶¶[0039]-[0043]. Yu's die 52 is a completed, singulated memory die attached at package assembly by C4 bumps (EX1010 [Yu], 4:30-34), so incorporating Camacho's architecture would require refabricating the die itself, replacing Yu's die rather than modifying Yu's package. Yu also already provides vertical interconnection through its through molding vias 38 and metallization layers on both sides of the package (EX1010 [Yu], 3:56-60), so die-level through-silicon vias would duplicate that interconnection while adding cost and processing complexity. The Petition identifies no deficiency in Yu that Camacho's through-silicon vias would remedy; the only reason to rebuild die 52 as a through-silicon-via die is to reach the language of claim 21, which is improper hindsight.

XII. CONCLUSION

203. For at least the foregoing reasons, Petitioners have failed to demonstrate that any challenged claim is unpatentable.

I, Dr. David S. Ricketts PhD, do hereby declare and state, that all statements are made herein of my own knowledge are true and that all statements made on information and belief are believed to be true. I am over the age of 21 and am competent to make this declaration. These statements were made with the knowledge that willful false statements are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Dated: August 21, 2026



Dr. David S. Ricketts