

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re *Inter Partes* Review of:)
U.S. Patent No. 9,318,609)
Issued: Apr. 19, 2016)
Application No.: 14/620,209)
Filing Date: Feb. 12, 2015)

For: **Semiconductor Device With Epitaxial Structure**

**PETITION FOR *INTER PARTES* REVIEW
OF U.S. PATENT NO. 9,318,609**

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Exhibit List

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1001	U.S. Patent No. 9,318,609
1002	Prosecution History of U.S. Patent No. 9,318,609
1003	Expert Declaration of Dr. Jack Lee
1004	U.S. Patent No. 9,166,022 (“Xu”)
1005	U.S. Patent No. 9,281,378 (“Ching”)
1006	U.S. Patent No. 8,809,139 (“Huang”)
1007	T. Ghani et al, <i>A 90nm High Volume Manufacturing Logic Technology Featuring Novel 45nm Gate Length Strained Silicon CMOS Transistors</i> , IEEE International Electron Devices Meeting 2003, pp. 11.6.1-11.6.3 (2003).
1008	Excerpts from N. Collaert, <i>CMOS Nanoelectronics</i> (2012).
1009	Intentionally left blank
1010	Intentionally left blank
1011	Intentionally left blank
1012	Intentionally left blank
1013	D. Hisamoto et al., <i>A Folded-channel MOSFET for Deep-sub-tenth Micron Era</i> , International Electron Devices Meeting 1998 – Technical Digest, pp. 1032-1034, (1998).
1014	X. Huang et al., <i>Sub 50-nm FinFET: PMOS</i> , International Electron Devices Meeting 1999 – Technical Digest, pp. 67-70, (1999).
1015	D. Hisamoto et al., <i>FinFET – A Self-Aligned Double-Gate MOSFET Scalable to 20 nm</i> , IEEE Transactions on Electron Devices, Vol. 47, No. 12, pp. 2320-2325 (2000).
1016	J. Markoff, <i>Intel Increases Transistor Speed by Building Upward</i> , New York Times (2011).
1017	Intel, <i>Intel’s Revolutionary 22 nm Transistor Technology</i> (2011).

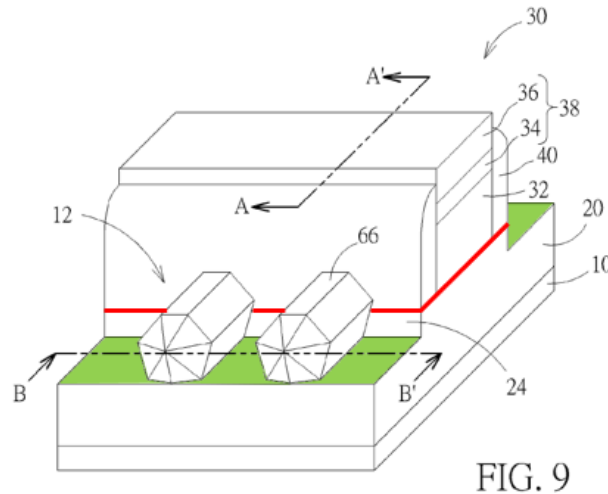
1018	A. Shimpi, <i>Intel Announces first 22nm 3D Tri-Gate Transistors, Shipping in 2H 2011</i> , AnandTech (2011) (archived May 18, 2011).
1019	K. Mistry et al., <i>A 45nm Logic Technology with High-k+ Metal Gate Transistors, Strained Silicon, 9 Cu Interconnect Layers, 193nm Dry Patterning, and 100% Pb-free Packaging</i> , 2007 IEEE International Electron Devices Meeting, pp. 247-250, (2007)
1020	Intentionally left blank
1021	S. Thompson et al., <i>Key Differences for Process-induced Uniaxial vs. Substrate-induced Biaxial Stressed Si and Ge Channel MOSFETs</i> , Technical Digest of the 2004 IEEE International Electron Devices Meeting (IEDM), pp. 221-224 (2004).
1022	C. Auth et al., <i>45nm High-k + Metal Gate Strain-Enhanced Transistors</i> , 2008 Symposium on VLSI Technology (2008)
1023	S. Mayuzumi et al., <i>High-Performance Metal/High-k n- and p-MOSFETs With Top-Cut Dual Stress Liners Using Gate-Last Damascene Process on (100) Substrates</i> , IEEE Transactions on Electron Devices, Vol. 56, No. 4, pp. 620-626, (2009)
1024	Intentionally left blank
1025	Excerpts from S. Wolf, <i>Microchip Manufacturing</i> , (2004).
1026	<i>Curriculum Vitae</i> of Dr. Jack Lee, Ph.D.
1027	MOSFET Scaling Presentation (2003)
1028	J. Steigerwald, <i>Chemical Mechanical Polish: The Enabling Technology</i> , 2008 IEEE International Electron Devices Meeting (2008)
1029	H. Wong et al., <i>Nanoscale CMOS</i> , IEEE, Vol. 87, No. 4, pp. 537-570 (1999)
1030	P. Zantye et al., <i>Chemical Mechanical Planarization for Microelectronics Applications</i> , Materials Science and Engineering R 45, pp. 89-220 (2004)
1031	Excerpts from S. Sze and K. Ng, <i>Physics of Semiconductor Devices (3d.)</i> (2007)
1032	Declaration of S. Bradley

I. Introduction

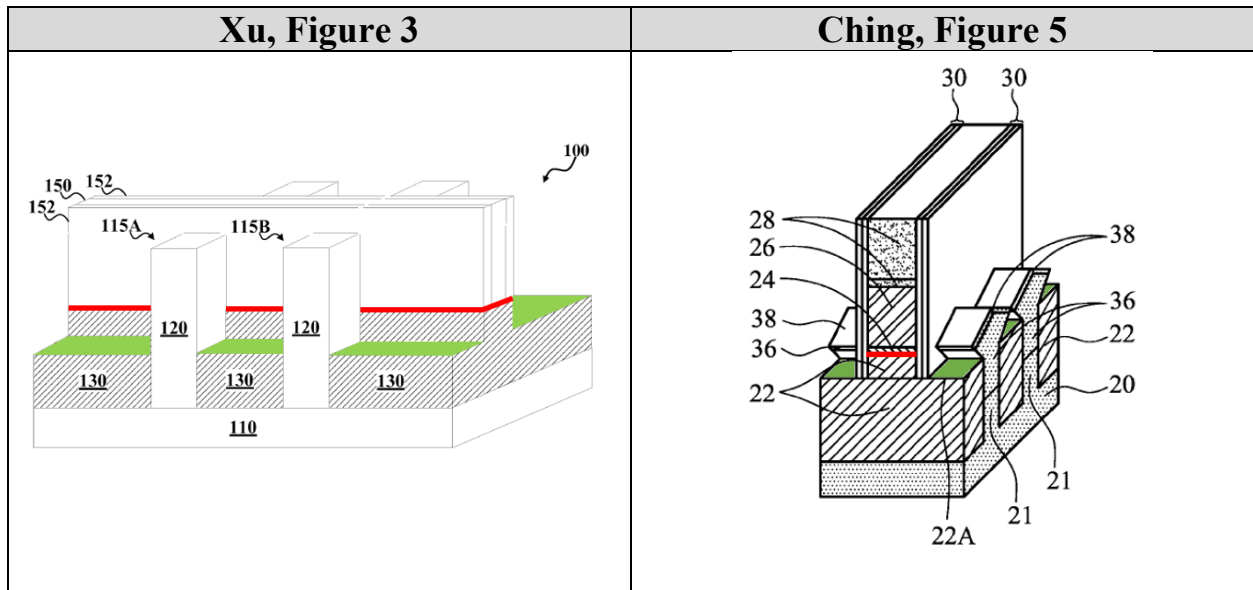
Taiwan Semiconductor Manufacturing Company Limited (“TSMC” or “Petitioner”) requests *inter partes* review of claims 1-10 (“Challenged Claims”) of U.S. Patent No. 9,318,609 (Ex. 1001, “’609 patent”).

The ’609 patent relates to semiconductor devices including a “fin structure” that “protrudes from the surface of the substrate.” Ex. 1001 at 1:60-61. The fin structure enables the formation of a “multi-gate MOSFET” (metal-oxide-semiconductor field effect transistor) such as a FinFET (fin field effect transistor). Ex. 1001 at 3:41-42, 1:20-21. As explained by TSMC’s expert Dr. Jack Lee, however, FinFETs were invented in 1999—more than ten years before the ’609 patent’s effective filing date. During those ten years, TSMC and others continued to innovate to improve FinFET manufacturing and the resultant devices. See Ex. 1003 at ¶¶ 39-41. The ’609 patent does nothing more than attempt to patent various FinFET improvements that were actually invented by others.

The main feature of the ’609 patent concerns the high-level structure of a FinFET. Ex. 1003 at ¶ 50; Ex. 1001 at 3:30-42. Specifically, the ’609 patent discloses an “isolation structure” that “surrounds the fin structure” has a “first top surface” under the gate structure and a “second top surface” at the sides of the gate structure, wherein the “first top surface” (red) is “higher” than the “second top surface” (green). This is shown in Figure 9 of the ’609 patent as annotated below.



But before the '609 patent was filed, FinFET transistors with a fin structure, an isolation structure, a gate structure, and an epitaxial structure were already well-known. Ex. 1003 at ¶ 41. In fact, before the '609 patent was filed, TSMC had already filed patent applications describing FinFET transistors featuring this same structure, in U.S. Patent No. 9,166,022 (Ex. 1004, “Xu”) and U.S. Patent No. 9,281,378 (Ex. 1005, “Ching”) discussed in greater detail below:



This Petition therefore requests inter partes review of challenged claims 1-10 and demonstrates their unpatentability.

II. Identification of Challenges (37 C.F.R. § 42.104(b))

Under Rules 42.22(a)(1) and 42.104(b)(1)-(2), Petitioner challenges claims 1-10 (“Challenged Claims”) of the ’609 patent and requests each Challenged Claim be cancelled.

A. Prior Art Patents Relied Upon

Petitioner relies upon the following patents and printed publications, which are prior art under the June 9, 2013 earliest possible filing date of the ’609 patent:

1. U.S. Patent No. 9,166,022 (“Xu”), issued on October 20, 2015 and filed on November 2, 2010, is prior art to the ’609 patent under AIA 35 U.S.C. § 102(a)(2).
2. U.S. Patent No. 9,281,378 (“Ching”), issued on March 8, 2016 and filed on November 9, 2012, is prior art to the ’609 patent under AIA 35 U.S.C. § 102(a)(2).
3. U.S. Patent No. 8,809,139 (“Huang”), issued on August 19, 2014 and filed on November 29, 2012 is prior art to the ’609 patent under AIA 35 U.S.C. § 102(a)(2).

B. Grounds for Challenge

This Petition, supported by the declaration of Dr. Jack Lee (Ex. 1003), presents the following grounds of unpatentability:

Ground	Claim(s) Challenged	35 U.S.C. §	References
1A	1-6, 8-10	102/103	Xu
1B	7	103	Xu in view Huang
2A	1, 3, 5, 6, 8-10	102/103	Ching
2B	2, 4	103	Ching in view of Xu
2C	7	103	Ching in view of Huang

III. Background

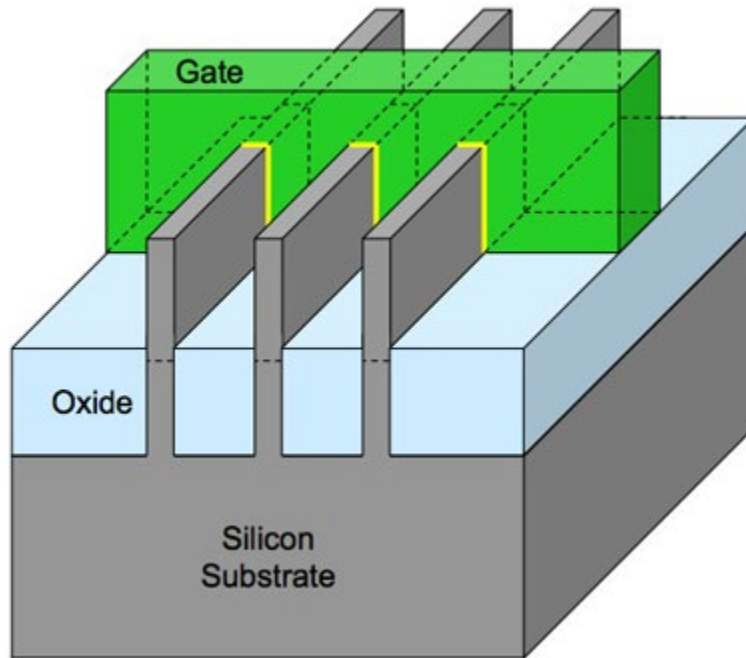
A. Technology Background

The '609 patent relates to semiconductor devices. Ex. 1003 at ¶ 35. Semiconductor devices are generally manufactured over substrates that are employed as a building foundation and comprise billions of transistors—the fundamental building blocks for semiconductor chips. *Id.* at ¶¶ 35-36.

A typical transistor has three main components: a “source,” a “drain,” and a “gate.” *Id.* at ¶ 37. When the transistor is “off,” no current flows between the source and drain. *Id.* When a proper voltage is applied to the “gate,” the transistor is turned on, allowing current to flow through a “channel region” between the source and drain. *Id.*

Around 1999, Chenming Hu, who later served as TSMC’s CTO, introduced a new type of transistor that he called “FinFETs.” Ex. 1003 at ¶ 39 (citing Ex. 1013, Ex. 1014, Ex. 1015). FinFETs are so named because the transistor channel is formed

in a thin vertical “fin” of silicon protruding from the substrate. *Id.* A representative FinFET structure is shown below:



Ex. 1017 at 7. As shown above, the gate overlays multiple surfaces of the fin, allowing for more effective control of the channel region between the source and drain. Ex. 1003 at ¶ 38. FinFET transistors on the substrate are separated by dielectric materials on the substrate. *Id.*

By 2004, it was already known that another improvement to transistor performance is achieved by introducing strain into the transistor channel by using epitaxial techniques. Ex. 1003 at ¶ 40. For example, silicon germanium (or “SiGe”) was commonly used in the source and drain regions to induce compressive strain, particularly for pMOS devices, thereby improving carrier mobility and drive current.

See id. (citing Ex. 1007 at 978-980; Ex. 1019 at 247-250). Such epitaxial strain techniques were specifically applied to FinFETs. Ex. 1003 at ¶ 43 (citing Exs. 1004, 1005, 1006).

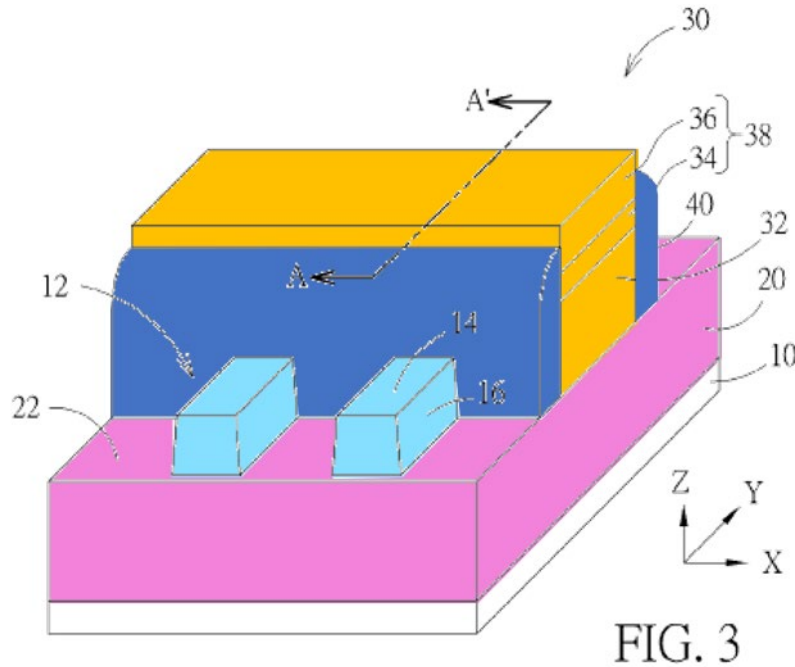
Thus, long before the priority date of the '609 patent, FinFET transistors fabricated by forming fin structures, isolation structures, gate structures, and epitaxially formed source/drains were already well-known. Ex. 1003 at ¶ 41. In fact, by 2013, the priority date of the '609 patent, Intel had already commercialized FinFET-based products with this architecture. *Id.* (citing Exs. 1016, 1017, 1018). TSMC, likewise, had developed and held numerous patents on FinFET transistors featuring these same structures, as discussed in greater detail below with respect to the Xu and Ching references. *Id.*

B. The '609 Patent (Ex. 1001)

The '609 patent is titled “Semiconductor Device with Epitaxial Structure.” It describes FinFET transistors comprising “a fin structure, an isolation structure, a gate structure and an epitaxial structure.” Ex. 1001 at Abst.

Figures 1 through 3 of the '609 patent depict the fabrication of a conventional FinFET device, which was known by the priority date. Ex. 1003 at ¶ 51. As shown in Figure 3, the FinFET comprises a “a plurality of fin structures 12” (light blue), a “gate structure 30” (gold) formed over the fins, and “a spacer 40” (dark blue) formed “on the sidewalls of the gate structure 30.” Ex. 1001 at 3:11-13, 4:62-66. Figure 3

also depicts “isolation structure 20” (magenta) formed on the substrate. *Id.* at 3:51-52.



Next, “a first etching process 42 ... may be carried out to selectively remove” the exposed portions of “isolation structure 20,” resulting in the structure shown in Figure 5. *Id.* at 5:17-28. As a result, “[t]here is a height difference H2 between the first top surface 22 α [red] and the second top surface 22 b [green]” of the isolation structure 20 (magenta) also depicted as a first depth “D1” in Figure 5.¹ *Id.* at 5:22-39.

¹ Reference numbers 22 α and 22 b are depicted in Figure 6.

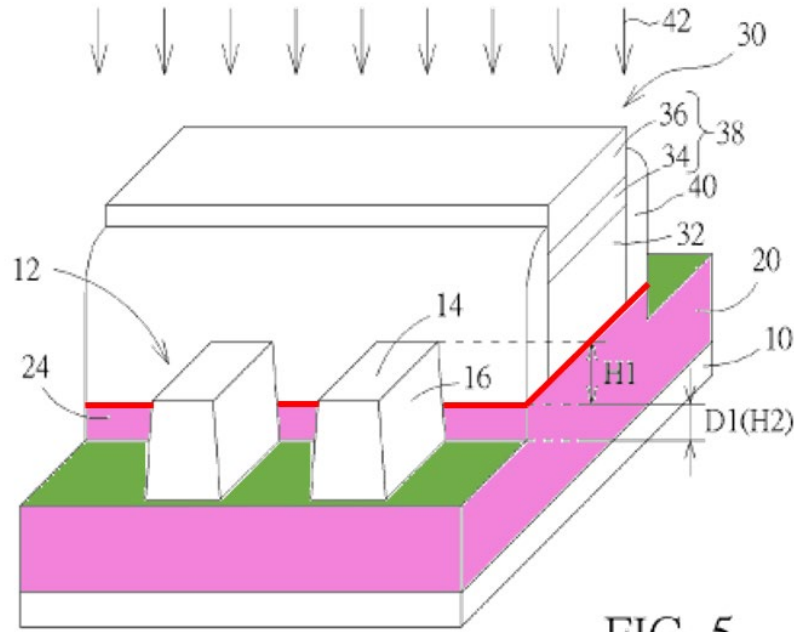


FIG. 5

The fin structures are then etched and “a recess 60 may be formed in each fin structure 12.” *Id.* at 5:47-51. An “epitaxial growth process” is then “carried out in order to grow an epitaxial structure 6[6] [*sic.*] in each corresponding recess 60.” *Id.* at 6:34-41. The recess is shown below in light blue (Figure 6) and the epitaxial structures are shown below in purple (Figure 9).

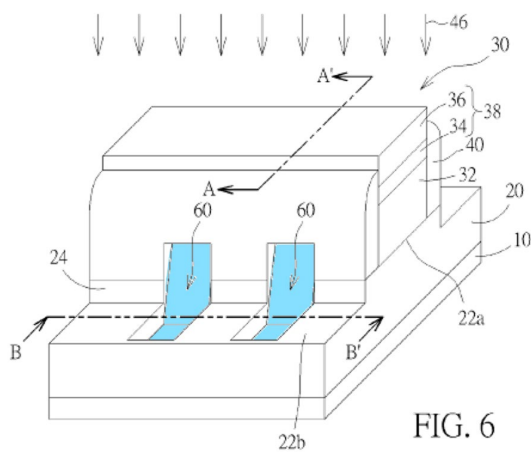


FIG. 6

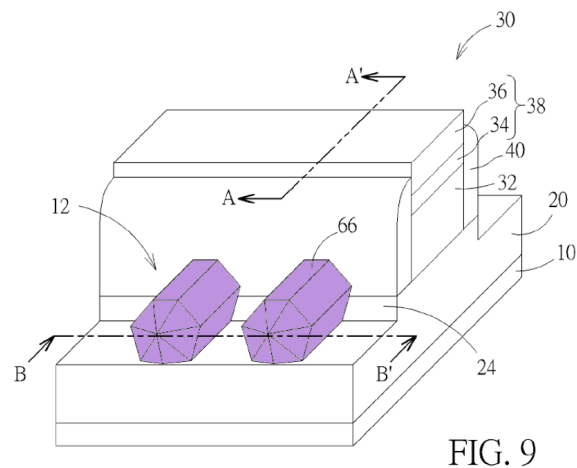
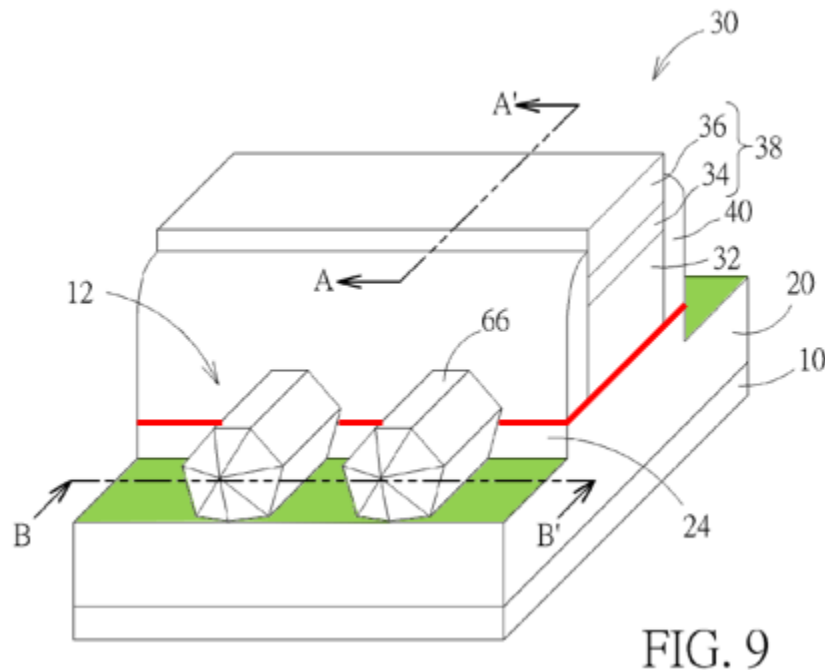


FIG. 9

The '609 patent tries to distinguish itself from the prior art by teaching that its “isolation structure” that “surrounds the fin structure” has a “first top surface” under the gate structure and a “second top surface” at the sides of the gate structure. *Id.* at Abst. According to the '609 patent, the “first top surface” (red, under the gate) is “higher” than the “second top surface” (green, on sides of the gate). *Id.* at Abst. This is shown in figure 9 of the '609 patent as annotated below, which depicts the completed FinFET.



C. Prosecution History

The Challenged Claims were allowed after one non-final rejection. Specifically, the Examiner rejected the pending claims based on U.S. Patent App. Pub. No. 2012/0193713 (“Kulkarni”). Ex. 1002 at 38. In response, Applicant amended pending claim 1 (the only independent claim) to recite “an isolation

structure, disposed on the surface of the substrate and surrounding the fin structure.” *Id.* at 25. Notably, Applicant admitted that the claims without the added limitation “disposed on the surface of the substrate” “may not sufficiently distinguish the claimed structure from the one disclosed in the cited references, i.e., *Kulkarni*”—effectively conceding that all other elements of the issued claims were already known in the art. *Id.* at 31. The claims were subsequently allowed. *Id.* at 7.

D. Person of Ordinary Skill in the Art

A POSITA would have had at least a Master’s degree in electrical engineering, physics, chemistry, materials science, or a related field, and three years of work experience in semiconductor manufacturing, such as, for example, in integrated circuit device (or transistor) design and/or manufacturing. Additional graduate education could substitute for work experience, and additional work experience/training could substitute for formal education.

E. Claim Construction

In this proceeding, claims are interpreted under the same standard applied by Article III courts. See 37 C.F.R. § 42.100(b); *see also* 83 Fed. Reg. 197 (Oct. 11, 2018); *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005) (en banc). Under this standard, words in a claim are given their plain meaning, which is the meaning understood by a POSITA in view of the patent and file history. *Id.* at 1312-

13. In this Petition, all of the claim terms are given their plain meaning, as understood by the POSITA, unless otherwise noted below.

IV. Ground 1A: Claims 1-6 and 8-10 Are Anticipated and/or Rendered Obvious by Xu

A. Overview of Xu

Xu was filed on November 2, 2010 by TSMC. Xu qualifies as analogous art because it is in the same field (FinFET technology) and is reasonably pertinent to a problem the '609 patent purports to address, namely, the structure and fabrication of FinFET devices. *See* Ex. 1001 at Abstr., 3:40-55; Ex. 1004 at Abstr. Xu describes “a FinFET device and method for fabricating a FinFET device.” Ex. 1004 at Abst. “The term FinFET device refers to any fin-based transistor.” *Id.* at 2:53-55.

Figure 2 of Xu depicts a “fin structure 115A and 115B [blue] that extends from the substrate 110.” *Id.* at 3:9-10. Figure 2 also shows “[i]solation features 130” that can be a “shallow trench isolation (STI) structure” (magenta) that “surround the fin structures 115A and 115B.” *Id.* at 3:54-58. The FinFET device also includes a “gate structure 150” (gold). *Id.* at 3:66-4:3.

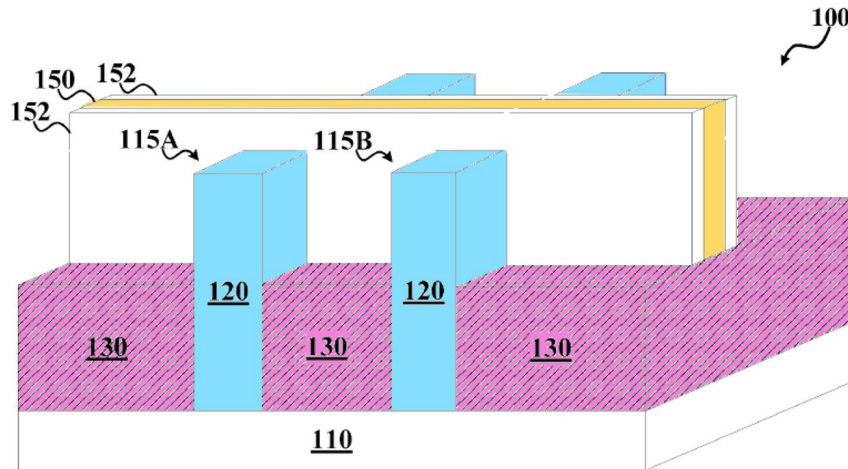


FIG. 2

As shown in Figure 3, “a process is [then] performed to recess the isolation features 130” using an “etching process.” *Id.* at 4:54-56. The “etching process selectively etches the isolation features 130.” *Id.* at 4:58-61. The process creates a height difference (or depth) between a top surface (red) under the gate and a top surface to the sides of the gate (green):

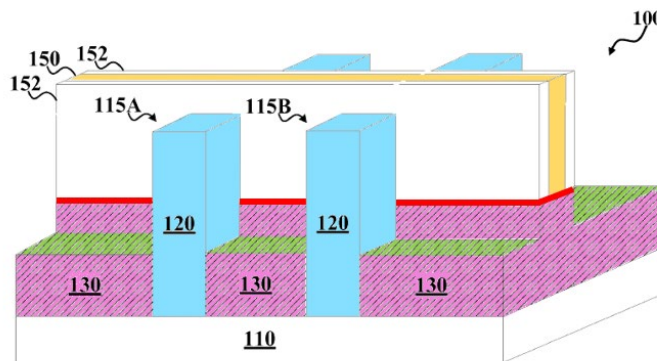


FIG. 3

Ex. 1003 at ¶ 58.

Next, as shown in Figure 4, a “fin template 135” (purple) is formed to “merg[e] the fins 120 together” by “epitaxially (epi) growing a semiconductor material on exposed portions of the fins 120 in the source and drain regions of the fin structures 115A and 115B.” Ex. 1004 at 5:1-15.

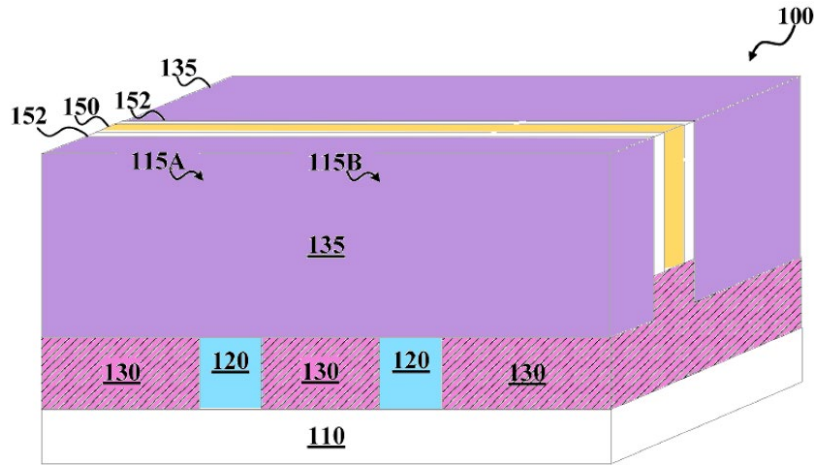


FIG. 4

The resulting fin template 135 (purple) and fins 120 (blue) are recessed in Figure 5 and, as shown in Figure 6, another “semiconductor material 160 [(checkered purple)] is epitaxially grown over the fin template 135,” which “generates channel strain.” *Id.* at 5:34-35, 5:49-55.

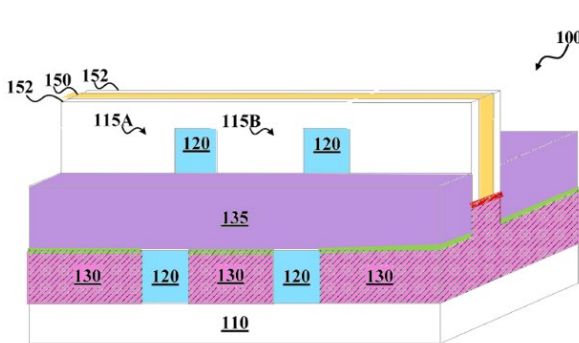


FIG. 5

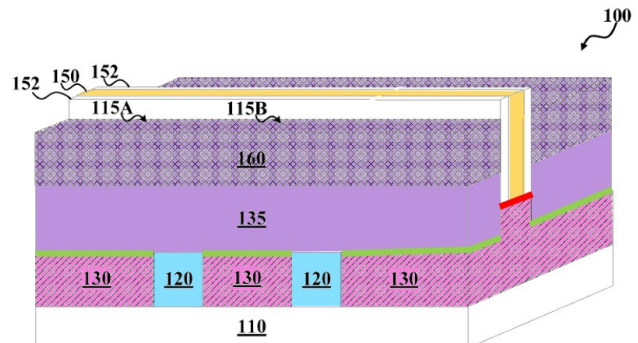


FIG. 6

Xu teaches that “[t]he semiconductor material 160 may be referred to as raised source and drain features of the source and drain regions of the fin structure 115A and 115B,” and that the “fin template 135 in the source and drain regions of the fin structures 115A and 115B may also be considered as part of the raised source and drain features.” *Id.* at 6:2-7. Notably, like the ’609 patent, Xu discloses a fin structure, an isolation structure, a gate structure, and an epitaxial structure, where the isolation structure has a first top surface that is higher than a second top surface. Ex. 1003 at ¶ 62.

B. Claim 1

1. 1[pre]: A semiconductor device, comprising:

The preamble is not limiting. Regardless, Xu discloses and renders obvious a semiconductor device. Ex. 1003 at ¶ 80. For example, Xu discloses “[a] FinFET device and method for fabricating a FinFET device” (Ex. 1004 at Abstr.), which is a semiconductor device. Ex. 1003 at ¶ 80.

2. 1[a]: a fin structure, protruding from a surface of a substrate, wherein the fin structure comprises a top surface and two side surfaces;

Xu discloses and renders obvious this limitation. Ex. 1003 at ¶ 81. For example, Xu discloses that “FinFET device 100 includes fin structure 115A and 115B that extend from the substrate 110.” Ex. 1004 at 3:9-10. The “fin structures 115A and 115B include fins 120.” *Id.* at 3:10-12. The “fins 120” are shown in

Figure 3 (light blue) and comprise a top surface and two side surfaces. *Id.* at 2:63-3:8.

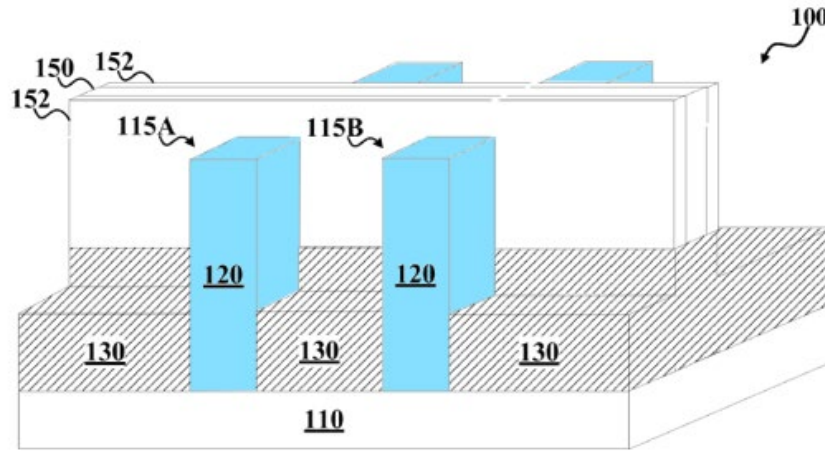


FIG. 3

The complete structure of the embodiment depicted by Figures 2 to 6 includes the “fins 120” (light blue) as shown in Figure 6 of Xu. *Id.* at Fig. 6 (note that fins 120 retain their full original height in the section under the gate (not shown in Fig. 6)).

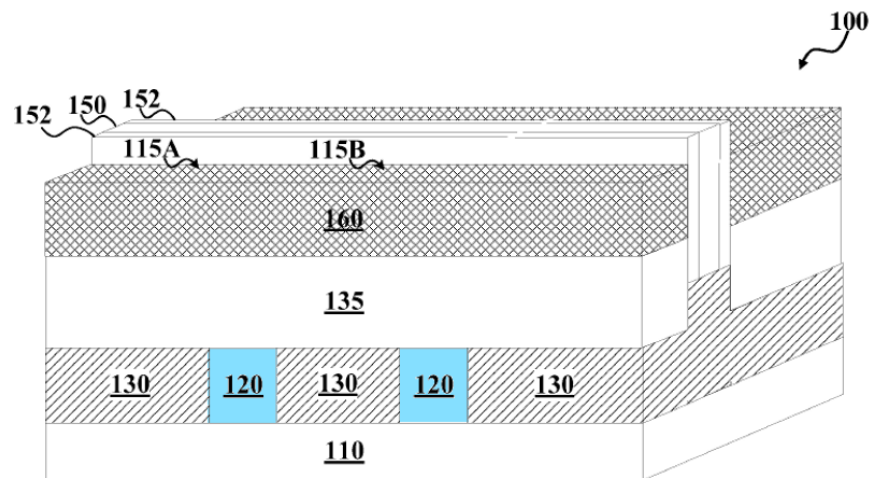


FIG. 6

3. 1[b]: an isolation structure, disposed on the surface of the substrate and surrounding the fin structure;

Xu discloses and renders obvious this limitation. Ex. 1003 at ¶ 83. For example, Xu discloses that “[i]solation features 130, such as shallow trench isolation (STI) structures, **surround the fin structures** 115A and 115B (in the depicted embodiment, the fins 120).” Ex. 1004 at 3:54-58. As shown in Fig. 3, the “isolation features 130” (magenta) are disposed on the surface of “substrate 110” and surround the fins 120 (light blue). *Id.* at 2:63-3:8 (describing substrate 110).

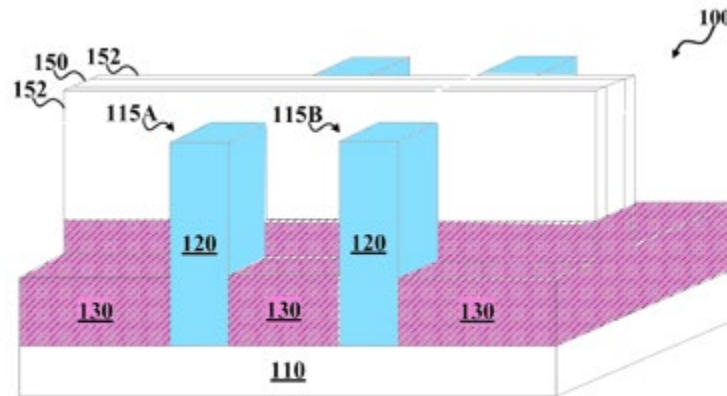


FIG. 3

The complete structure of the embodiment depicted by Figures 2 to 6 includes “isolation features 130” (magenta) as shown in Figure 6. *Id.* at Fig. 6.

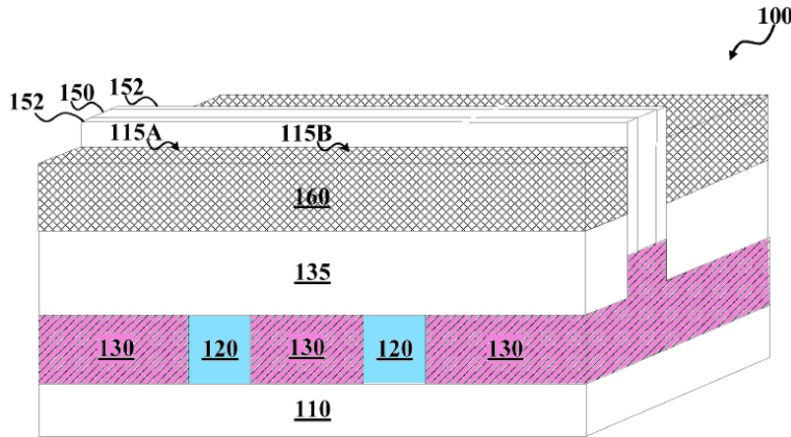


FIG. 6

4. **1[c(i)]: a gate structure, overlaying the top surface and the two side surfaces of a portion of the fin structure and covering a portion of the isolation structure;**

Xu discloses and renders obvious this limitation. Ex. 1003 at ¶ 85. For example, Xu discloses “a gate structure 150” that “traverses the fins 120, and in the depicted embodiment, is formed on a central portion of the fins 120.” Ex. 1004 at 3:66-4:1. As shown in Figure 3, the “gate structure 150” (gold) overlays the top surface and two side surfaces of the “central portion of the fins 120” (light blue) and also covers a portion of the isolation structure 130 (magenta). *Id.*

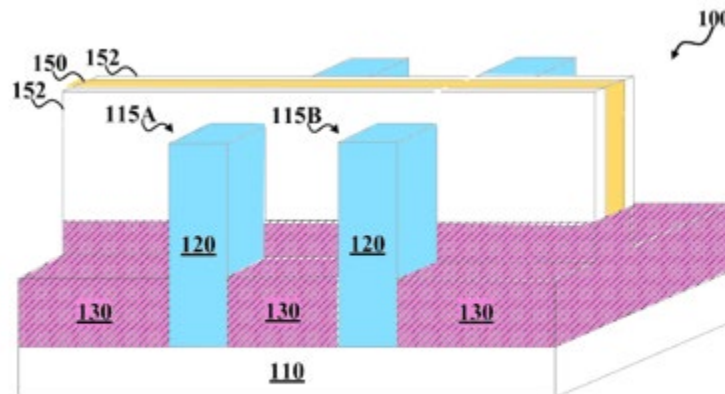


FIG. 3

The complete structure of the embodiment depicted by Figures 2 to 6 includes “gate structure 150” (gold) as shown in Figure 6. Ex. 1003 at ¶ 86. And, Figure 5, which shows the structure immediately preceding Figure 6, shows that the gate structure (gold) overlays the top surface and two side surfaces of a portion of the fins 120 (light blue), and also covers a portion of the isolation structure 130 (magenta). *Id.*; Ex. 1004 at Fig 5, Fig. 6.

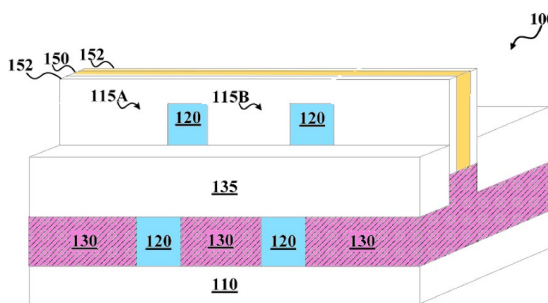


FIG. 5

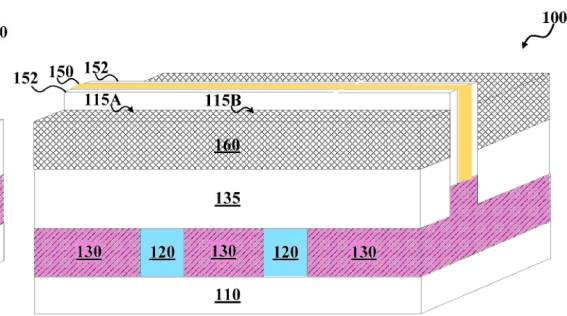


FIG. 6

5. **1[c(ii)]: wherein the isolation structure under the gate structure has a first top surface and the isolation structure at two sides of the gate structure has a second top surface, and the first top surface is higher than the second top surface; and**

Xu discloses and renders obvious this limitation. Ex. 1003 at ¶ 87. For example, Xu discloses that “a process is performed to recess the isolation features 130” using an “etching process.” Ex. 1004 at 4:54-56. The “etching process selectively etches the isolation features 130” and “avoid[s] etching the silicon nitride spacers 152.” *Id.* at 4:58-61.

As shown in Fig. 3, this results in the “isolation features 130” (magenta) under the “gate structure 150” (gold) having a first top surface (red) and the “isolation features 130” (magenta) at the two sides of the “gate structure 150” (gold) having a “second top surface” (green). Ex. 1003 at ¶ 88. The first top surface (red) is higher than the second top surface (green). *Id.*

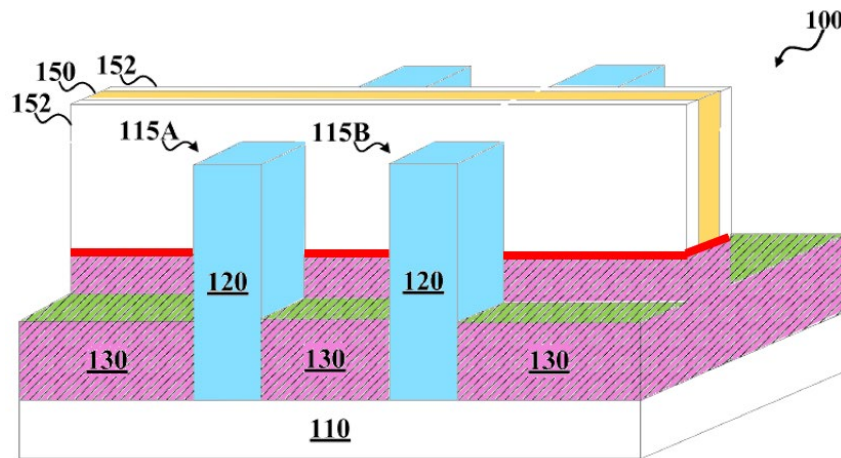


FIG. 3

The complete structure of the embodiment depicted by Figures 2 to 6 includes “isolation structure 130” (magenta) with the first and second top surfaces, where the first top surface (red line) is higher than the second top surface (green line) as shown in Figure 6. *Id.*

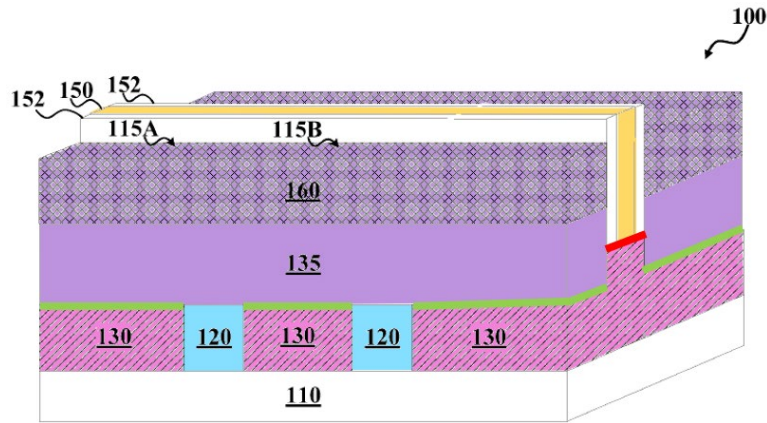


FIG. 6

6. 1[d]: an epitaxial layer, disposed at one side of the gate structure and in direct contact with the fin structure.

Xu discloses and renders obvious this limitation. Ex. 1003 at ¶ 90. As discussed below, the fin template 135 and the semiconductor material 160, both individually, and together, meet limitation 1[d].

For example, Xu discloses that a “fin template 135” is formed by “epitaxially (epi) growing a semiconductor material **on exposed portions of the fins 120** in the source and drain regions of the fin structures 115A and 115B.” Ex. 1004 at 5:1-15. The “fin template 135” is thus an epitaxial layer disposed at one side of the gate structure because the “source and drain regions” are located on either side of the “gate structure 150.” Ex. 1003 at ¶ 90. As shown below, the “fin template 135” is also in direct contact with the “fins 120” (light blue). Ex. 1004 at Fig. 5.

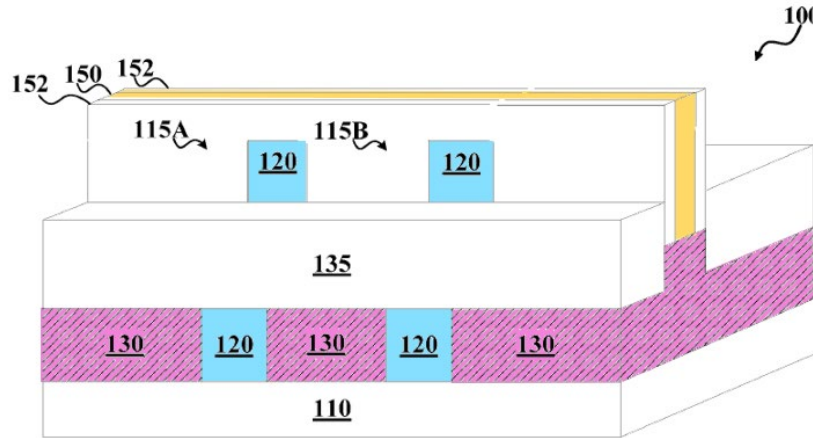


FIG. 5

As another example, Xu discloses that “a process is performed to recess the fin template 135” and “a semiconductor material 160 is epitaxially grown over the fin template 135.” *Id.* at 5:34-35, 5:49-50. The “semiconductor material is epi grown on the exposed fin template 135 **in the source and drain regions** of the fin structures 115A and 115B.” *Id.* at 5:50-55. Thus, “semiconductor material 160” is an “epitaxial layer” that is disposed at one side of the gate structure because the “source and drain regions” are located on either side of the “gate structure 150.” Ex. 1003. Further, portions of “fin structures 115A and 115B” are exposed prior to the formation of “semiconductor material 160 ... over the fin template 135” as shown in Figure 5 above. Ex. 1004 at Fig. 5. When “semiconductor material 160” is formed as shown in Figure 6, it will therefore be in “direct contact with fin structure” 120 (light blue) as shown in Figure 6 below. *Id.* at Fig. 6; Ex. 1003.

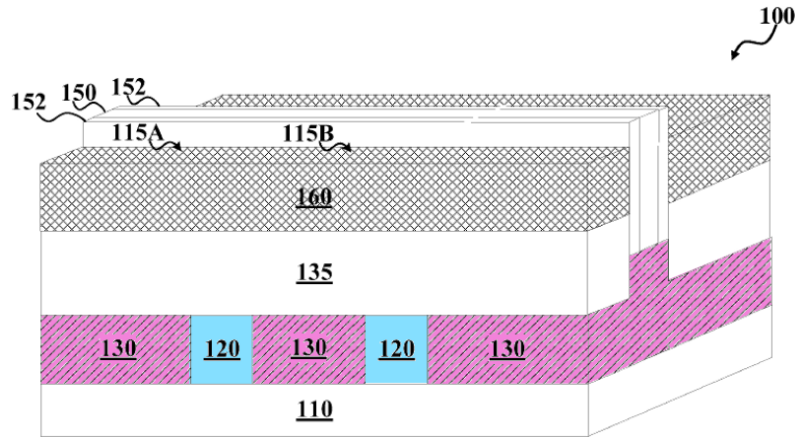


FIG. 6

Moreover, Xu teaches that the “epi grown semiconductor material 160 generates channel strain for the fin structures 115A and 115B.” Ex. 1004 at 5:50-55. This material 160 forms “raised source and drain features” that “can effectively introduce strain into the channels of the fin structures 115A and 115B.” Ex. 1004 at 5:45-48. A POSITA would have understood and found obvious that to accomplish this goal, “semiconductor material 160” directly contacts the fins in order to physically expand or compress the crystal lattice of the channel and introduce strain. Ex. 1003 at ¶¶ 93-94.

The complete structure of the embodiment depicted by Figures 2 to 6 includes both epitaxial “fin template 135” (purple) and epitaxial “semiconductor material 160” (checkered purple) disposed at one side of the “gate structure” (gold) and in contact with the “fins 120” as shown in Figure 6. *Id.*

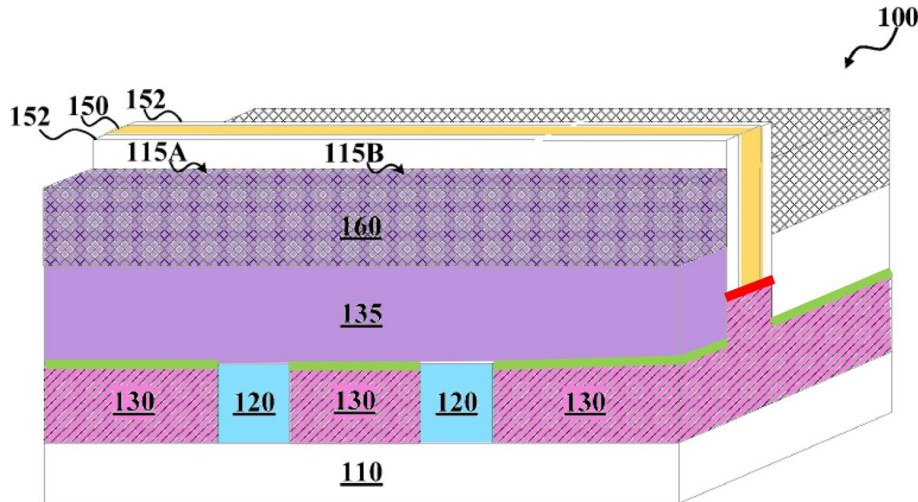


FIG. 6

In addition to meeting the requirements of element 1[d] individually, the combination of “fin template 135” and “semiconductor material 160” is also “an epitaxial layer, disposed at one side of the gate structure and in direct contact with the fin structure” as claimed. Ex. 1003 at ¶ 96.

A POSITA would have understood that “an epitaxial layer” may comprise “one or more” epitaxial layers and therefore would have understood the combined layer of Xu to be “an epitaxial layer” as claimed. *Id.* at ¶ 97. Further, Xu discloses that “fin template 135” and “semiconductor material 160” may be formed of the same materials, using the same deposition techniques and doping processes. *See* Ex. 1004 at 5:10-23, 5:55-67. From this overlap in materials and deposition processes, a POSITA would have understood that the combined structure of “fin template 135” and “semiconductor material 160” collectively forms “an epitaxial layer” as claimed.

C. Claim 2: The semiconductor device according to claim 1, wherein there is a height difference between the first top surface and second top surface, and the height difference ranges from 100 Angstroms to 250 Angstroms.

As discussed above, Xu discloses and renders obvious a semiconductor device in accordance with claim 1.

Xu further discloses and renders obvious the additional limitations of claim 2. Ex. 1003 at ¶ 99. For example, as discussed above, Xu discloses a height difference between the first top surface and second top surface of the “isolation features 130” that results from the “etching process” that “selectively etches the isolation features 130.” *See* 1[c(ii)]; Ex. 1004 at 4:56-61. Xu further discloses that “in the depicted embodiment, the etching process uses a hydrofluoric acid (HF) etching solution of a suitable concentration (for example, 100:1)” and “the HF solution **recesses the isolation features 130 about 100 Å.**” *Id.* at 4:61-65 (emphasis added). Because the “etching process” recesses only the exposed “second top surface” (green)—and not the “first top surface” under the “gate structure 150”—the complete structure of the embodiment depicted by Figures 2 to 6 discloses a height difference between the “first top surface and second top surface” of 100 Å. Ex. 1003 at ¶ 99.

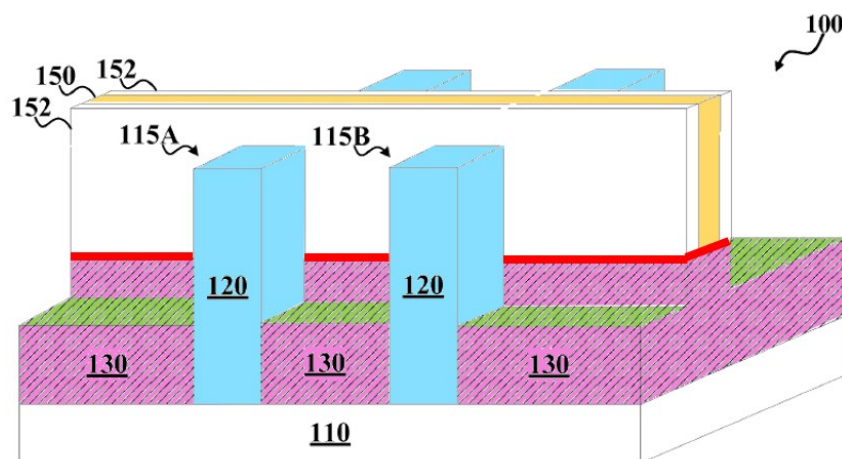


FIG. 3

Xu's disclosure of recessing the second top surface (green) "about 100 Å" discloses the additional limitation of claim 2 because it lies inside the claimed range of "100 Angstroms to 250 Angstroms." *Ineos USA LLC v. Berry Plastics Corp.*, 783 F.3d 865, 869 (Fed. Cir. 2015) ("When a patent claims a range, as in this case, that range is anticipated by a prior art reference if the reference discloses a point within the range."). This same height difference is reflected in the completed structure of Xu:

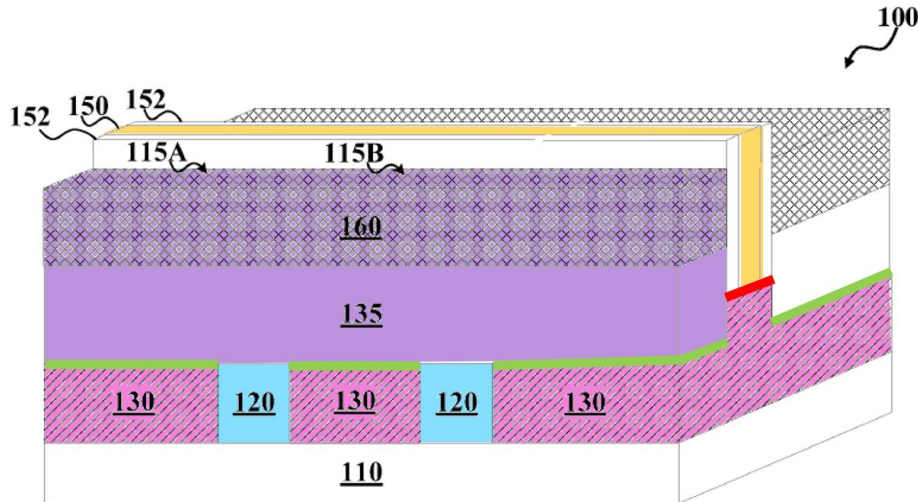


FIG. 6

Ex. 1003 at ¶ 101.

D. Claim 3: The semiconductor device according to claim 1, wherein the gate structure is a metal gate structure.

As discussed above, Xu discloses and renders obvious a semiconductor device in accordance with claim 1.

Xu further discloses and renders obvious the additional limitation of claim 3.

Ex. 1003 at ¶ 103. For example, Xu discloses that “[t]he gate structure 150 may include a gate dielectric layer and a gate electrode” and that “[t]he gate electrode includes ... a *metal* including Al, Cu, Ti, Ta, W, Mo, TaN, NiSi, CoSi, TiN, WN, TiAl, TiAlN, TaCN, TaC, TaSiN, other conductive materials, or combinations thereof.” Ex. 1004 at 4:2-3, 10-13.

A POSITA would have understood that “metal gate structure” refers to a gate structure comprising metal. Ex. 1001 at 7:12-25 (describing the common practice

of substituting metal in place of polysilicon in a gate structure); Ex. 1003 at ¶ 104 (same). As the '609 Patent and Xu both disclose, the “gate structure” may comprise metal along other associated layers. Ex. 1001 at 7:10-25; Ex. 1004 at 4:2-3. And by disclosing that the gate electrode may comprise metals (Ex. 1004 at 4:10-13), Xu discloses a metal gate structure. Ex. 1003 at ¶ 105.

E. Claim 4: The semiconductor device according to claim 1, wherein the isolation structure under the gate structure comprises a sidewall and the epitaxial structure² is in direct contact with the sidewall.

As discussed above, Xu discloses and renders obvious a semiconductor device in accordance with claim 1.

Xu further discloses and renders obvious the additional limitations of claim 4. Ex. 1003 at ¶ 107. For example, “isolation features 130” undergo an “etching process” which results in the “isolation features 130” under the “gate structure 150” comprising a sidewall, as shown below in Figure 3 (yellow). Ex. 1004 at 4:54-61; Ex. 1003 at ¶ 107.

² Petitioner notes that claims 4-8 and 10 use the term “epitaxial structure” as opposed to “epitaxial layer” as used in claim 1. Petitioner interprets these instances of “epitaxial structure” as referring back to the “epitaxial layer” of claim 1.

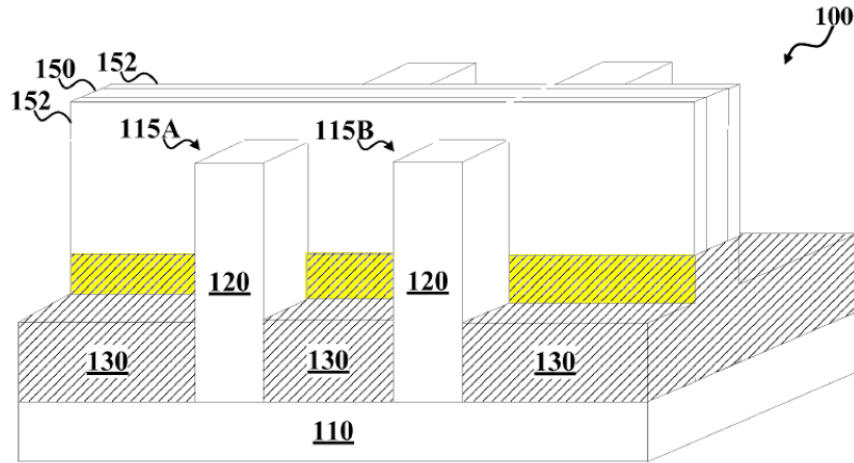


FIG. 3

In Xu, “fin template 135 is ... formed by a silicon epitaxial deposition process” or “by a silicon germanium epitaxial deposition process.” Ex. 1004 at 5:15-20. Then, in Xu’s device, the “fin template 135” (*i.e.*, the claimed “an epitaxial structure”) is in direct contact with the sidewall of the “isolation features 130” under the “gate structure 150,” as shown in annotated Figure 6 below. Ex. 1004 at Fig. 6; Ex. 1003 at ¶ 108.

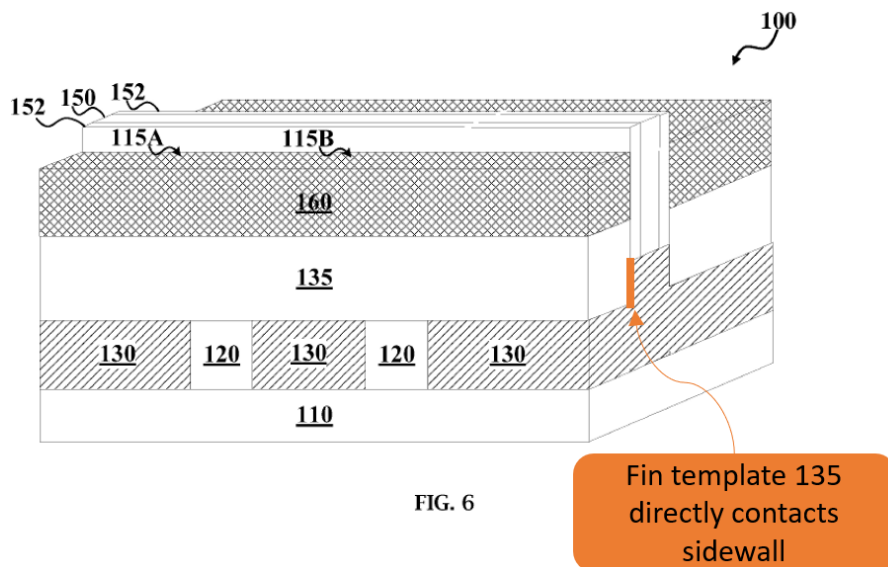


FIG. 6

Additionally, when “fin template 135” and “semiconductor material 160” are taken together as “the epitaxial structure,” this combined structure still meets the limitations of claim 4 through the contact between the sidewall of “fin template 135” and the “isolation features 130.” *Id.* at ¶ 109; Ex. 1004 at 4:49-50.

F. Claim 5: The semiconductor device according to claim 1, further comprising a recess formed at one end of the fin structure, wherein the epitaxial structure fills up the recess.

As discussed above, Xu discloses and renders obvious a semiconductor device in accordance with claim 1.

Xu further discloses and renders obvious the additional limitations of claim 5. Ex. 1003 at ¶ 111. Specifically, Xu discloses a second embodiment of the FinFET device 200 where the “fin structures 215A and 215B” have two portions 220 and 230 (as shown in Figure 8A) and **“an etching process completely removes the fin portions 230 from the source and drain regions** of the fin structures 215A and 215B, exposing the fin portions 220” (as shown in Figure 9A). Ex. 1004 at 7:58-61, 10:34-36; Fig. 7 (“[c]ompletely remove the second material portion [230] from the source and drain regions of the first and second fin structure”).

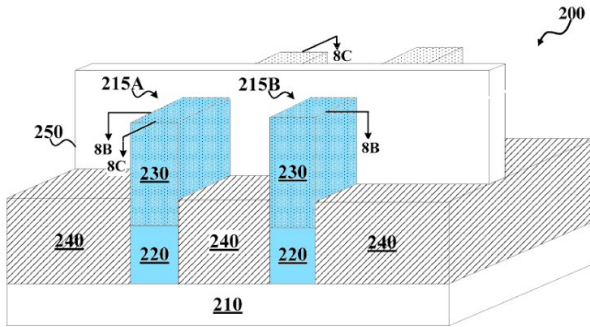


FIG. 8A

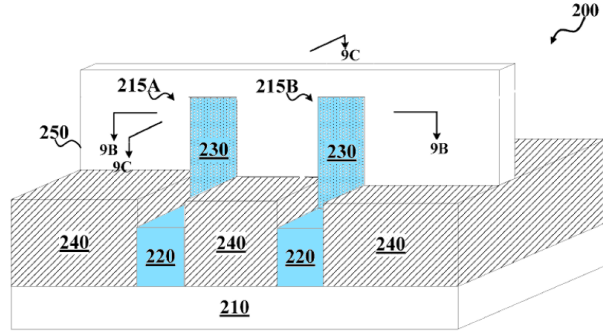


FIG. 9A

This etching process forms recesses in fin structure 215A, 215B, at one end of the fin structure. *Id.* at Fig. 10; Ex. 1003 at ¶ 111.

Xu further discloses that, in the second embodiment, “fin template 280” is “a semiconductor material [that] is epitaxially (epi) grown on the exposed fin portions 200” and fills up the recess formed by the prior etching process. Ex. 1004 at 11:2-8. This is depicted in annotated Fig. 10A below:

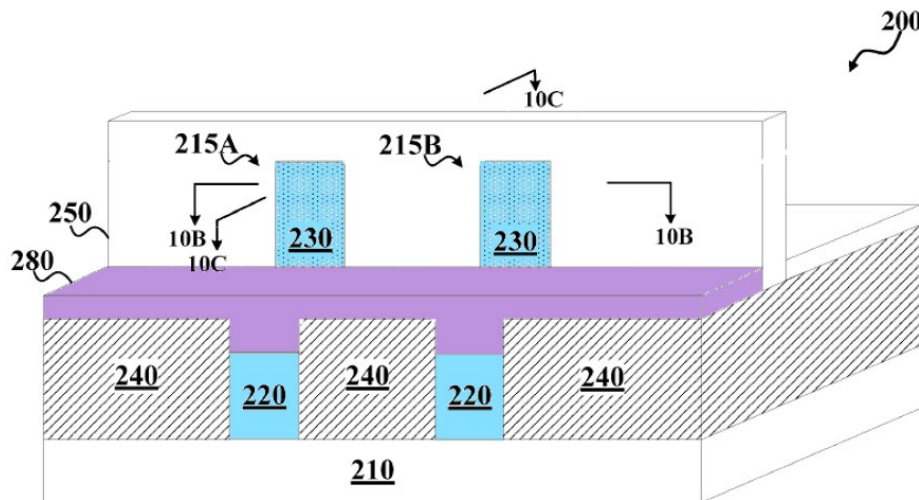


FIG. 10A

Specifically, Xu discloses that after the fins are recessed, fin template 280 “may be formed by a process similar to that described above with reference to FIG. 5” of

Xu's first embodiment. Ex. 1004 at 11:2-4. In other words, Xu expressly discloses that the same epitaxial growth process of the first embodiment is used to fill the recess with the "fin template" (purple). *Id.*; Ex. 1003 at ¶ 113. Accordingly, Xu's second embodiment discloses a recess formed at one end of the fin structure, wherein the epitaxial structure fills up the recess. Ex. 1003 at ¶ 113.

It would have been obvious to a POSITA to combine the recess-and-fill of Xu's second embodiment with Xu's first embodiment such that the first embodiment includes an epitaxial structure filling the recess. Ex. 1003 at ¶ 114. First, as the Federal Circuit has found, "[c]ombining two embodiments disclosed adjacent to each other in a prior art patent does not require a leap of inventiveness." *Boston Scientific Scimed, Inc. v. Cordis Corp.*, 554 F.3d 982, 991 (Fed. Cir. 2009). This is especially true where, as here, the reference itself suggests such a combination. Ex. 1003 at ¶¶ 114, 117-118, 122 (describing Xu's disclosure of combining steps of the first and second embodiments).

Additionally, Xu explains the benefits of using such recesses, noting that "by controlling source and drain trench depth"—which is dictated by the depth of the recess—"strain for both PMOS and NMOS FinFET devices can be achieved and optimized" and "different types of strain can be achieved." Ex. 1004 at 15:56-66. "Accordingly, the trench depth can be tuned to independently optimize performance of each FinFET device in an integrated circuit device." *Id.* at 15:67-16:2. Thus, the

POSITA would have understood that recessing “fins 120” of Xu’s first embodiment will result in “achiev[ing] and optimiz[ing]” strain. *Id.* at 15:56-60, 15:67-16:2; Ex. 1003 at ¶ 115. Xu therefore expressly recognizes an advantage or expected benefit that would have motivated a POSITA to combine the recess-and-fill of the second embodiment with Xu’s first embodiment. *Id.*

Moreover, after describing the subject matter illustrated in Figs. 1-16C, Xu summarizes the invention in a way that suggests combining steps of Xu’s first embodiment with steps of Xu’s second embodiment in a single embodiment. Ex. 1004 at 16:5-44, 16:45-17:10; Ex. 1003 at ¶ 117. As Xu explains, its “disclosure provides for **many** different embodiments.” Ex. 1004 at 16:5-6 (emphasis added). For example, Xu discloses a method (Ex. 1004 at 16:7-26) that can include “etching back the isolation structure” as in Xu’s first embodiment. Ex. 1004 at 16:17-19. Following this description, Xu provides alternative modifications to this method. *Id.* at 16:27-44. Specifically, Xu discloses “[t]he method may include completely removing the second material portion from the source and drain regions of the fins before forming the fin template.” *Id.* at 16:40-43. These techniques correspond to the fin recess-and-fill steps described in Xu’s second embodiment, as shown in Figures 7, 8A and 9A. Ex. 1003 at ¶ 117. *See also* Ex. 1004 at 16:45-17:10 (describing “another embodiment” that may include “etching back the isolation structure” and “removing a portion of the first and second fin structures before

epitaxially growing the first semiconductor material” which may include “completely removing the second material portion”). Xu’s express disclosure of using these steps together suggests and renders obvious the combination of the first and second embodiments. Ex. 1003 at ¶ 118.

Additionally, a POSITA would have had a reasonable expectation of success in making this combination. Ex. 1003 at ¶ 119. Xu discloses exemplary etch processes which can be used to perform the step of recessing the fin. Ex. 1004 at 10:36-61; 13:44-55. A POSITA would have understood these to be conventional processes that could be applied to the fins of Xu’s first embodiment in order to control a recess depth. Ex. 1003 at ¶ 119.

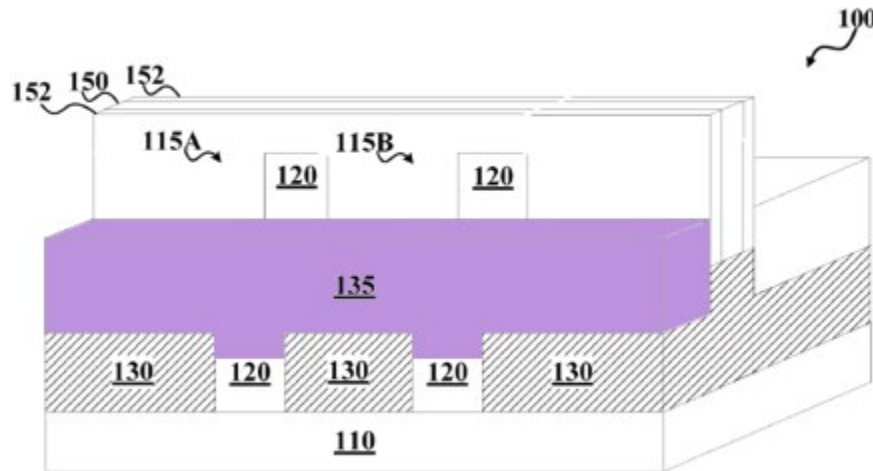
Put differently, Xu’s first embodiment is a known fabrication method ready for improvement by applying the known technique from the second embodiment of forming a trench or recess in the fin, which yields the predictable result taught by Xu of “provid[ing] different starting substrates for forming the fin templates, such that different types of strain can be achieved.” Ex. 1004 at 15:64-16:2; Ex. 1003 at ¶ 121.

Claim 19 of Xu, dependent from independent claim 11, further reinforces the obviousness of this combination. Ex. 1003 at ¶ 122. Like the portions of the specification described above, dependent Claim 19 sets forth a method that combines “completely removing the second material portion from the source and drain regions

of the fins” (Ex. 1004 at 20:19-21) with “recessing the isolation structure by removing a portion of the isolation structure” (*id.* at 19:8-10, independent claim 11). Thus, Claim 19 of Xu explicitly recites a fabrication method that combines the step of “recessing the isolation structure by removing a portion of the isolation structure”—as disclosed in the first embodiment—with the step of removing materials from the source and drain regions of the fins to form recesses in the fin structures—as described in the second embodiment. Ex. 1004 at Claim 19; Ex. 1003 at ¶ 122. That Xu claims these steps together demonstrates that a POSITA would have found it obvious to combine the first embodiment with the fin recess-and-fill of the second embodiment to arrive at the claimed method. *Id.* Put simply, a POSITA reading Claim 19 would have “readily envisage[d] the combination of” Xu’s first and second embodiments and “it would have been obvious to that person that these two could be combined with a reasonable expectation of success.” *Kennametal, Inc. v. Ingersoll Cutting Tool Co.*, 780 F.3d 1376, 1385 (Fed. Cir. 2015).

When the recesses of the second embodiment are formed in the first embodiment, a POSITA would have understood and found it obvious that an epitaxial layer (purple) will “fill the recesses” because Xu teaches that, in both embodiments, the epitaxial layer is formed on the “exposed portions of the fins 120.” Ex. 1004 at 5:1-2 (first embodiment); 11:4-8 (second embodiment); Ex. 1003 at ¶

123. This is shown in modified figure 5 below depicting the combination of the second embodiment's recesses with the first embodiment:



G. Claim 6: The semiconductor device according to claim 5, wherein a bottom surface of the epitaxial structure is shallower than a bottom surface of the isolation structure.

As discussed above, Xu discloses a semiconductor device in accordance with claim 6.

Xu further discloses and renders obvious the additional limitations of claim 6. Ex. 1003 at ¶ 125. As discussed above, a POSITA would have been motivated to combine Xu's first embodiment with the technique for recessing the "fins 120" and filling the recesses with an epitaxial structure taught by Xu's second embodiment. *See supra* cl. 5. For example, as shown in Figure 10A, the bottom surface of epitaxial structure 280 is shallower than the bottom surface of the isolation structure 240 when the fin recess techniques of the second embodiment are applied. Ex. 1004 at Fig. 10A; Ex. 1003 at ¶ 125. This is because fin portion 220 is not completely

removed during the etching process and forms a bottom surface (yellow) for epitaxial structure 280 (purple). *Id.* The bottom surface of epitaxial structure 280 is higher (and therefore shallower) than the bottom surface of isolation structure 240 (brown). *Id.*

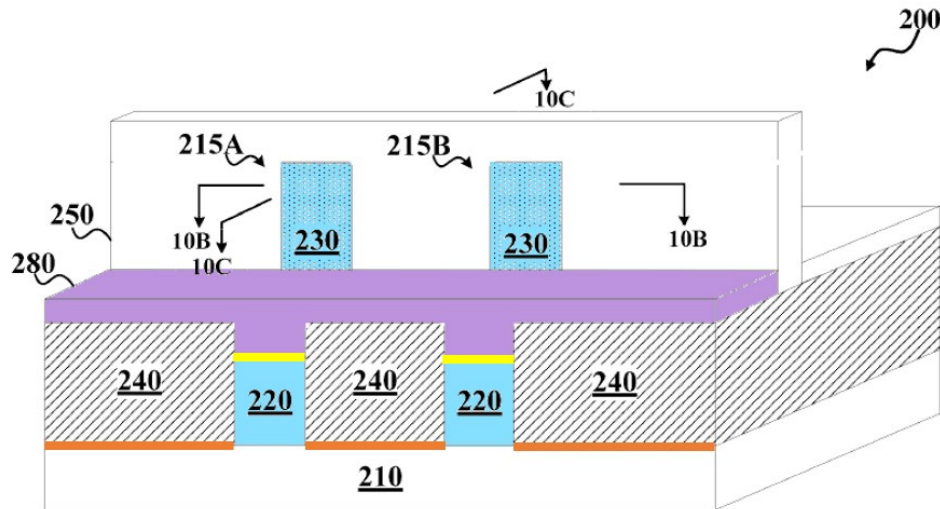
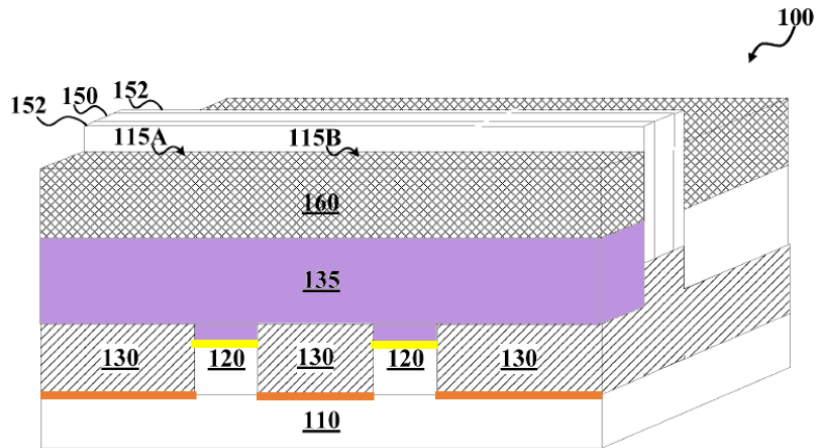


FIG. 10A

The modified figure below shows the combination of Xu's first and second embodiments. Ex. 1003 at ¶ 127. The fin template (epitaxial structure) will also have a bottom surface (yellow) that is shallower than the bottom surface of the isolation structure (brown) for the same reasons as the second embodiment in Figure 10A. *Id.*



H. Claim 8: The semiconductor device according to claim 1, wherein the epitaxial structure comprises silicon germanium, silicon phosphide or phosphor-doped silicon carbide.

As discussed above, Xu discloses and renders obvious a semiconductor device in accordance with claim 1.

Xu further discloses and renders obvious the additional limitations of claim 8. Ex. 1003 at ¶ 130. For example, Xu discloses that the “fin template 135,” which is an epitaxial structure as discussed above, *supra* 1[d], “could be silicon germanium (SiGe)” or silicon phosphide. Ex. 1004 at 5:18-20, 5:23-35 (“the epi silicon fin template 135 may be doped with phosphorous (to form a Si:P epi layer)”). As another example, Xu discloses that the “semiconductor material 160,” which is an epitaxial structure as discussed above, *supra* 1[d], “is silicon germanium (SiGe).” Ex. 1004 at 5:59-62. As both the “fin template 135” and “semiconductor material 160” may be SiGe, Xu also discloses and renders obvious this claim when the

combination of “fin template 135” and “semiconductor material 160” are taken as the “epitaxial structure.”

I. Claim 9: The semiconductor device according to claim 1, further comprising a spacer disposed on a sidewall of the gate structure.

As discussed above, Xu discloses and renders obvious a semiconductor device in accordance with claim 1.

Xu further discloses and renders obvious the additional limitations of claim 9. Ex. 1003 at ¶ 132. For example, Xu discloses that “[s]pacers 152 are disposed on the sidewalls of the gate structure 150, such as along the gate electrode.” Ex. 1004 at 4:39-40. The complete structure of the embodiment depicted by Figures 2 to 6 includes “spacers 152” (dark blue) disclosed on a sidewall of the “gate structure 150” as shown in Figure 6. *Id.* at Fig. 6.

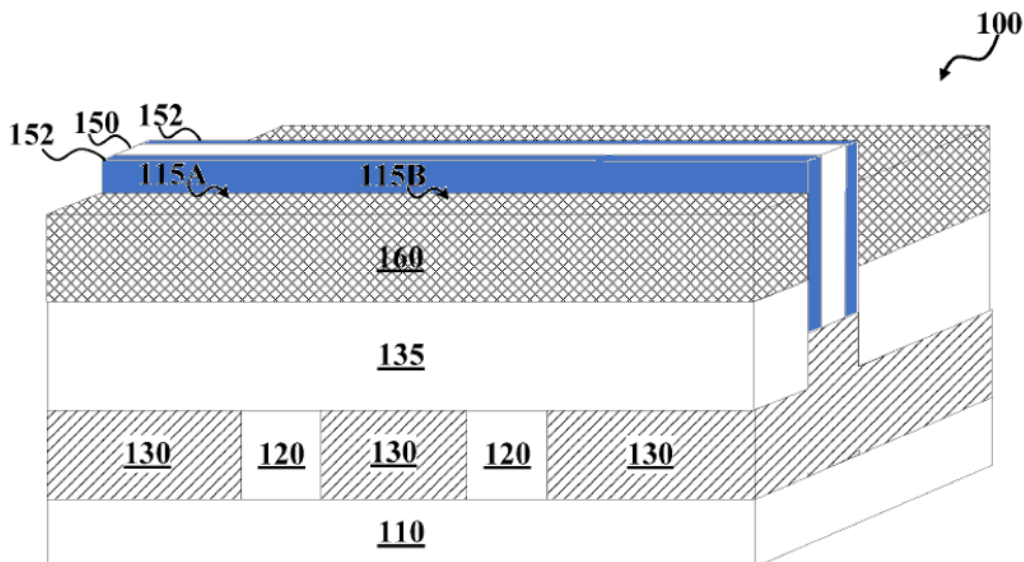


FIG. 6

J. Claim 10

- 1. 10[pre]: The semiconductor device according to claim 1, further comprising:**

As discussed above, Xu discloses and renders obvious a semiconductor device in accordance with claim 1.

- 2. 10[a]: another epitaxial structure, disposed at another side of the gate structure and in direct contact with the fin structure; and**

Xu discloses and renders obvious this limitation. Ex. 1003 at ¶ 134. For example, as explained above for limitation 1[d], Xu discloses a “fin template 135” and “semiconductor material 160” which are epitaxially grown, disposed on one side of the “gate structure 150,” and in direct contact with “fins 120.” *See supra* 1[d]. As described above, the combination of “fin template 135” and “semiconductor material 160” is also “an epitaxial [structure]” as set forth in claim 1. *Id.*

Xu further discloses that both “fin template 135” and “semiconductor material 160” are epitaxially grown in the “**source and drain** regions of the fin structures 115A and 115B.” Ex. 1004 at 5:49-53 (emphasis added). Xu recognizes that source and drain regions are “separated by the gate structure.” *Id.* at 16:34-39. Indeed, a POSITA would have understood that the source and drain regions of a transistor are on opposite sides of the gate structure in a FinFET device. *See supra* III.A; Ex. 1003. Thus, “fin template 135” (purple) and “semiconductor material 160” (checkered purple) are disposed at “another side of the gate structure” and in direct

contact with the fin structure for the same reason that these structures are in direct contact with the fin structure on the first side of the gate structure as shown in Figure 6 below. *See supra* 1[d]; Ex. 1003 at ¶ 135.

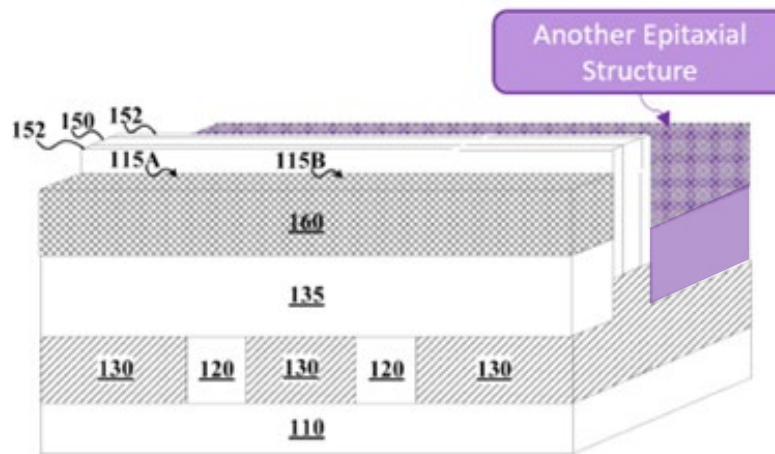


FIG. 6

3. **10[b]: a channel region, contiguous to the top surface and the side surfaces of the fin structure, and between the epitaxial structure and said another epitaxial structure.**

Xu discloses and renders obvious this limitation. Ex. 1003 at ¶ 136. For example, Xu discloses that the “fins 120 include a source region, a drain region, and a channel defined between the source and drain regions.” Ex. 1004 at 3:14-16. The channels can be seen in Figure 5 (light blue), as Xu discloses that when the “fin template 135 is etched back,” the “channels of the fin structures” are “expose[d].” *Id.* at 5:43-45. As shown below, the channel (light blue) is contiguous with the top surface and both side surfaces (orange) of the fin structure. *Id.* at Fig. 5. The channel is then covered by semiconductor material 160 (a portion of the source and drain

epitaxial structure). *Id.* at Fig. 6. Xu thus discloses that the channel region is between the epitaxial structure (one of source/drain) and said another epitaxial structure (the other of the source/drain).

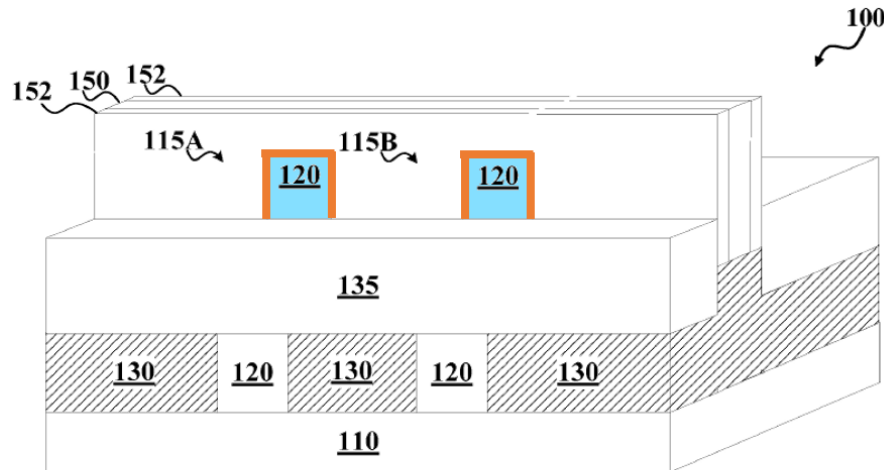


FIG. 5

As Xu recognizes, a “typical” FinFET device includes a “channel” that “is formed in the vertical fin” and “[a] gate is provided over (e.g., wrapping) the fin.” *Id.* at 1:22-26. Xu further teaches that “[i]t is beneficial to have a gate on both sides of the channel allowing gate control of the channel from both sides.” *Id.* at 1:26-28. A POSITA would have understood this arrangement to be a conventional tri-gate FinFET structure where the gate overlays the channel on three surfaces (top and two sides). Ex. 1003 at ¶ 137.

A POSITA would further understand the channel extends below the “gate structure 150” and is therefore positioned “between the epitaxial structure and said another epitaxial structure.” Ex. 1003 at ¶ 138. For example, Xu discloses that the

“source and drain regions of each of the first and second fins **defines a channel therebetween.**” Ex. 1004 at 17:25-27 (emphasis added).

After the channel is exposed as shown in Figure 5 above, Xu’s fabrication process deposits epitaxial “fin template 135” (purple) and epitaxial “semiconductor material 160” (checkered purple) on fin structures 120 on both sides of the gate—i.e., in the source and drain regions. Ex. 1004 at 5:49-55. Thus, as shown in Figure 6 below, the channel region (no longer exposed) is between the epitaxial structure 135 and/or 160 and the “another epitaxial structure” on the other side of the gate. *Id.* at Fig. 6; Ex. 1003 at ¶ 139.

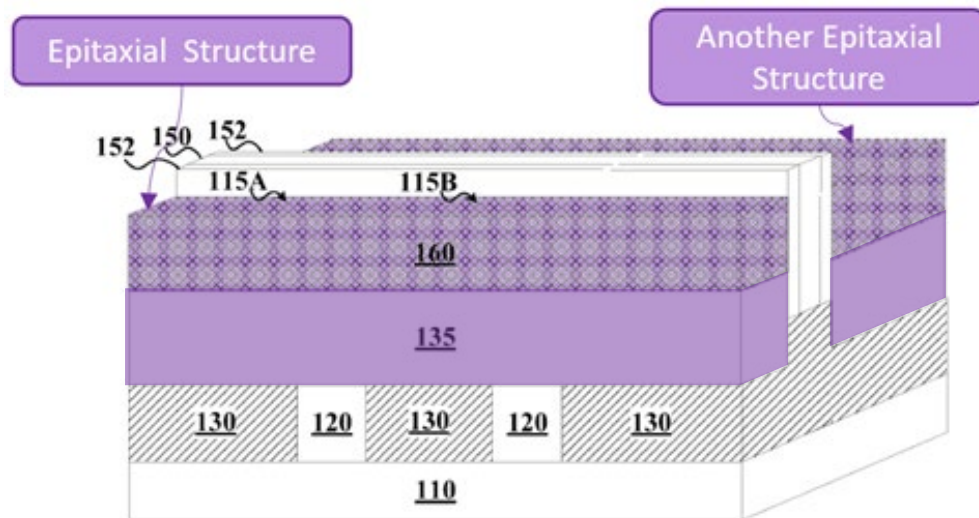


FIG. 6

This holds true whether the “fin template 135” alone, “semiconductor material 160” alone, or the combination of these elements is considered the “epitaxial structure.”

V. Ground 1B: Claim 7 Is Obvious Over Xu in View of Huang

A. Overview of Huang

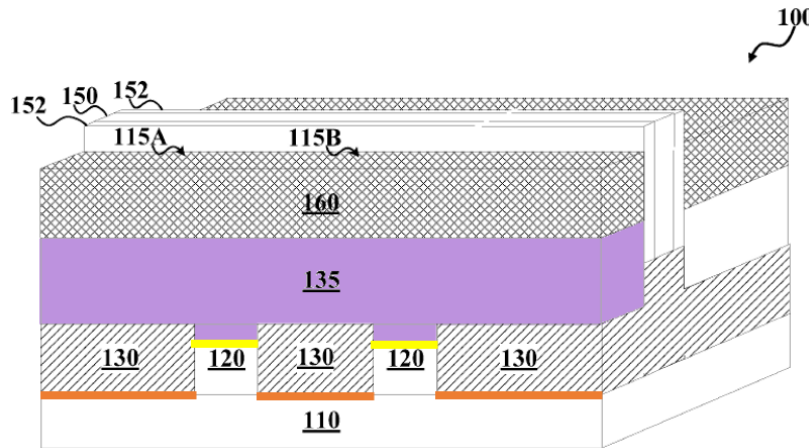
Huang, filed on November 29, 2012 by TSMC, is prior art under 102 and qualifies as analogous art to the '609 patent. *See* Ex. 1006. Huang lies in the same technical field of FinFET technology and addresses problems directly relevant to those faced by the '609 patent, such as the formation and integration of FinFET structures. *See* Ex. 1001 at Abstr., 3:40-55; Ex. 1006 at Abstr; Ex. 1003 at ¶ 72.

Huang depicts “various stages in the manufacture of a Fin-Last FinFET device” (Ex. 1006 at 2:20-22) including a step of forming “semiconductor strips 24 ... by patterning the semiconductor substrate” (*id.* at 2:45-46) and a step of “etching of portions of the semiconductor strips 24 in a strained source drain (SSD) etch step to form recesses 36 in the semiconductor strips 24” (*id.* at 4:10-12). Huang further discloses specific dimensions for the initial height of the semiconductor strips (*id.* at 2:58-59) and the depth of the recesses in the semiconductor strips (*id.* at 4:15-16).

B. Claim 7: The semiconductor device according to claim 6, wherein there is a height difference between the bottom surface of the epitaxial structure and the bottom surface of the isolation structure, and the height difference ranges from 100 Angstroms to 250 Angstroms.

As discussed above, Xu discloses and renders obvious the fabrication method of claim 6. Ex. 1003 at ¶ 142. Xu in view of Huang renders claim 7 obvious. *Id.*

Specifically, as discussed above with respect to claims 5 and 6, the combination of Xu’s first and second embodiments comprises an epitaxial structure formed within a recess in the fin structure such that the bottom surface of the epitaxial structure (yellow) is shallower than the bottom surface of the isolation structure (orange):



Ex. 1004 at Fig. 11A (modified); Ex. 1003 at ¶ 143.

Xu discloses that the recesses are formed to a controllable “depth (d_1)” (Ex. 1004 at 10:55-57) and that the “depth can be controlled” to yield different source/drain configurations and induce tailored channel strain for various FinFET devices (*id.* at 14:6-9). While the depth of the recesses is a controlled variable, Xu does not disclose numerical values for the depth of these recesses or for the dimensions of the nearby structures. Ex. 1003 at ¶ 144.

Xu therefore differs from claim 7 only in that Xu does not explicitly disclose the specifically claimed dimensions of the height difference between the bottom surface of the epitaxial structure and the bottom surface of the isolation structure.

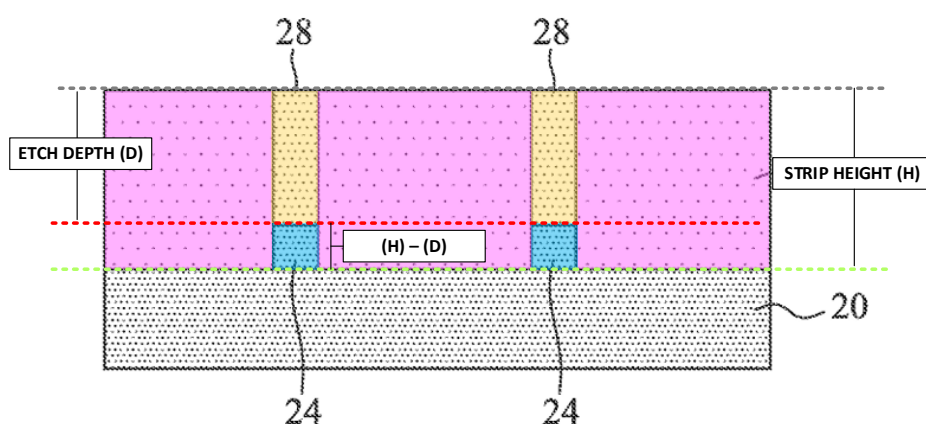
Id. at ¶ 145. To fill this gap, a POSITA would have found it obvious to optimize the etch depth through routine experimentation to yield a desired strain. *In re Aller*, 220 F.2d 454, 456 (CCPA 1955) (“where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation.”); Ex. 1003 at ¶ 145.

In doing so, the POSITA would have found it obvious to turn to additional prior art, such as Huang, for concrete dimensional guidance concerning fin recess depths and FinFET device architecture. *Id.* at ¶ 146. Huang provides precisely the kind of dimensional specificity that Xu lacks. *Id.* Like Xu, Huang discloses a method of fabricating a FinFET device including epitaxially growing source and drain regions in recesses formed within fin structures. Ex. 1006 at 4:30-36. Huang further expressly discloses specific dimensions for these features. Ex. 1003 at ¶ 146.

For example, Huang discloses forming “semiconductor strips 24” to “have a height from about 10 nm to about 500 nm.” *Id.* at 2:58-59. These semiconductor strips are interspersed with “dielectric layer 22” which may be “blanket deposited on the FinFET device” and planarized “until the tops of the semiconductor strips are exposed.” *Id.* at 3:7-8, 26-27. Huang’s “dielectric layer 22” occupies the same space as the “isolation features 130” of Xu and may be formed of the same materials, such as silicon oxide or silicon nitride. Ex. 1003 at ¶ 147 (citing Ex. 1004 at 3:58-62; Ex. 1006 at 3:8-13). The materials disclosed for Huang’s “dielectric layer 22” are well-

known to be insulative and to provide electrical isolation. *Id.* at ¶ 147. A POSITA therefore would have understood Huang’s dielectric layer to be both (1) analogous to Xu’s “isolation features” and (2) the claimed “isolation structure.” *Id.* Accordingly, Huang discloses an initial height of both the “semiconductor strips 24” and “dielectric layer 22” (*i.e.*, “isolation structure”) of 10 nm to about 500 nm. *Id.*

Huang further discloses “etching of portions of the semiconductor strips 24 in a strained source drain (SSD) etch step to form recesses 36 in the semiconductor strips 24.” Ex. 1006 at 4:10-12. Again, Huang expressly provides dimensions for these recesses, disclosing that the etch depth may be “from about 5 nm to about 25 nm.” *Id.* at 4:15-16. The resultant structure, shown in modified Fig. 4B, below, includes epitaxial structure (gold) grown atop the recessed semiconductor strips (blue), which remain surrounded by dielectric (magenta):



The vertical offset between the bottom surface of the epitaxial structure (red line) and the bottom surface of the dielectric (green line) corresponds to the difference between the strip height H (*i.e.*, “from about 10 nm to about 500 nm”) and the etch

depth D (*i.e.*, “from about 5 nm to about 25 nm”). Accordingly, the height difference between the bottom surface of the epitaxial region and the bottom surface of the dielectric layer (*i.e.*, “isolation structure”) is in the range from about 5 nm to about 475 nm. Ex. 1003 at ¶ 149. Huang thus discloses the general conditions for recess depths in FinFET processing. *Id.*

It would have been obvious from the teachings of Xu and Huang to optimize the recess depth through routine experimentation and arrive at the claimed height difference. Ex. 1003 at ¶ 150. A POSITA would have understood that, in Xu, the claimed height difference is a direct result of the depth of the fin recess. *Id.*

Xu explicitly discloses that the depth of this fin recess “can be controlled to achieve various source and drain features for the fin structures, such that different kinds of channel strain can be achieved for different FinFET devices.” Ex. 1004 at 14:6-9. In fact, Xu explains that this depth “can be tuned to independently *optimize* performance of each FinFET device in an integrated circuit.” *Id.* at 15:67-16:2. Accordingly, a POSITA would have understood that the trench depth is a results-effective variable that Xu itself contemplates controlling in order to optimize performance. Ex. 1003 at ¶ 151. Moreover, Xu discloses particular etching techniques that may be used to create this recess and a POSITA would have been familiar with ways to tune etch depths and etch profiles. Ex. 1004 at 10:34-47; Ex. 1006 at 2:45-67, 4:10-29; Ex. 1003 at ¶ 151.

While Xu does not disclose numerical values for the recess depth and the resulting height difference, Huang discloses the general conditions of these parameters, namely, a recess depth of between 5 nm and 25 nm and a resulting height difference of between 5 and 475 nm. Ex. 1006 at 2:59, 4:16. Additionally, the '609 Patent does not posit any criticality or unexpected results of the claimed range. Ex. 1003 at ¶ 152. It therefore would have been obvious to a POSITA from the general conditions and Xu's express desire to control the recess depth to achieve optimal performance to optimize the recess depth and resulting height difference through routine experimentation and arrive at the claimed height difference. *In re Aller*, 220 F.2d at 456.

Moreover, the '609 Patent's claimed range (100 Angstroms to 250 Angstroms) lies entirely within the range disclosed by Huang (5 nm to 475 nm, or 50 Angstroms to 4,750 Angstroms). *Id.* at ¶ 153. And, as Dr. Lee explains, a POSITA would have found the lower end of Huang's range, where the claimed range lies, desirable because smaller dimensions improve packing density. *Id.* (citing Exs. 1027, 1028, 1029, 1030, and 1031 describing scaling transistors in both horizontal and vertical dimensions to improve integration density and performance). Xu and Huang both recognize the industry-wide desire to scale down FinFET device size to permit more transistors to fit on the same chip area. Ex. 1004 at 1:17-19, 34-38; Ex. 1006 at 1:7-15. A POSITA therefore would have been motivated to minimize the footprint of

Xu to achieve higher density and performance. Ex. 1003 at ¶ 154. In doing so, the POSITA would have pursued the lower end of Huang's range, including from 100 to 250 Angstroms, which corresponds to a device with smaller vertical dimensions and a more compact overall footprint that the POSITA would have reasonably expected to operate successfully. *Id.*

Arriving at the claimed height difference in Xu's device also would have been obvious to a POSITA from the overlap between the claimed range and the range disclosed by Huang. The Federal Circuit has long recognized that a *prima facie* case of obviousness exists where a claimed range overlaps or lies inside ranges disclosed by the prior art. *In re Peterson*, 315 F.3d 1325, 1329-30 (Fed. Cir. 2003). In fact, "even a slight overlap in range establishes a *prima facie* case." *Id.* at 1329. Obviousness can also be established where ranges do not overlap, but merely abut. *In re Geisler*, 116 F.3d 1465, 1469-71, (Fed. Cir. 1997) (claimed range of "50 to 100 Angstroms" obvious in view of prior disclosure of a range 100 to 600 Angstroms). Where, "as here, the claimed ranges are completely encompassed by the prior art, the conclusion is even more compelling than in cases of mere overlap." *In re Peterson*, 315 F.3d at 1330.

To the extent Patent Owner argues Huang's disclosed range is too large to render the claimed range obvious, Patent Owner would be wrong. This is not an instance of a claim to a species within a "potentially infinite genus" disclosed by the

prior art. *Cf. In re Baird*, 16 F.3d 380, 382 (Fed. Cir. 1994). Rather, claim 7 recites a range of its own that lies completely within the range disclosed by Huang. Ex. 1003 at ¶ 155. Moreover, Xu explicitly motivates a POSITA to control the recess depth to achieve a desired strain (Ex. 1004 at 14:6-9) and both Huang and Xu explicitly motivate a POSITA to explore the lower end of Huang’s range, as described above. *Id.* at ¶ 156. That the claimed range lies within the portion of Huang’s range exhibiting “particularly desirable features” further underscores the obviousness of this range. *Maxell, Ltd. v. Amperex Tech. Ltd.*, 2025 WL 271614 at *5 (Fed. Cir. Jan. 23, 2025). And a POSITA would have had a reasonable expectation of success in arriving at these desirable features using exemplary etch processes disclosed by Huang to achieve the claimed height difference. Ex. 1006 at 2:45-67, 4:10-29; Ex. 1003 at ¶ 156.

VI. Ground 2A: Claims 1, 3, 5, 6, 8-10 Are Anticipated and/or Rendered Obvious by Ching

A. Overview of Ching

Ching was filed on November 9, 2012 by TSMC. Ex. 1005. Ching qualifies as analogous art because it is in the same field (FinFET technology) and is reasonably pertinent to a problem the ’609 patent purports to address, namely, the structure and fabrication of FinFET devices. See Ex. 1001 at Abstr., 3:40-55; Ex. 1005 at Abstr. Ching describes a “Fin Field-Effect Transistor (FinFET) and the methods of forming the same.” *Id.* at 1:53-55.

Figure 1 shows an “initial structure” with a “substrate 20.” *Id.* at 1:63-67. Figure 1 also depicts “[i]solation regions such as Shallow Trench Isolation (STI) regions 22” (magenta) on the surface of substrate 20, as well as a “semiconductor strip 21” (light blue) protruding from the surface of the substrate which may be “the same as the material of substrate 20.” *Id.* at 2:1-13.

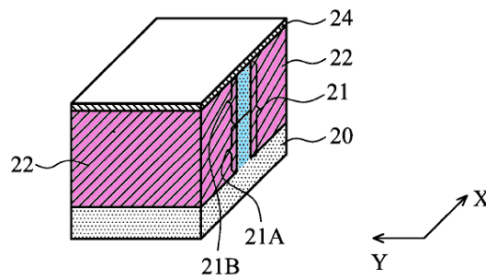


Fig. 1

Figure 2 shows that a “polysilicon layer 26” and “[h]ard mask layer 28” are then deposited over the “semiconductor strip.” *Id.* at 2:35-58.

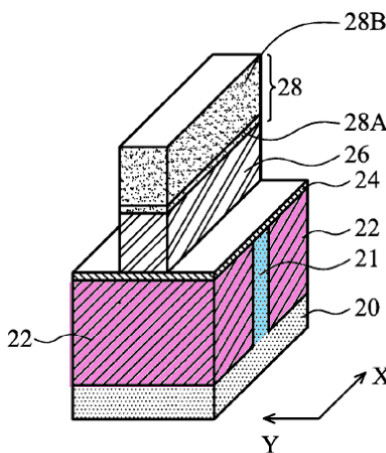


Fig. 2

Subsequently, as shown in Figure 3, “[a] first STI recessing may be performed” and “top surfaces 22A [green] of STI regions 22 are also recessed from

the original top surface 22A' [red line] of STI regions.” *Id.* at 2:59-67. “[G]ate spacers 30” (dark blue) are also formed as shown in Figure 3. *Id.* at 3:9-12.

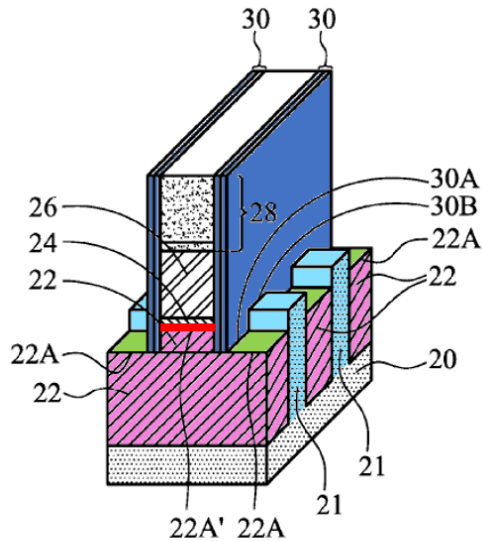


Fig. 3

Next, “exposed portions of semiconductor strip 21 [light blue] are recessed” (Figure 4) and “epitaxy regions 36” (purple) are formed “from recesses 32” (Figure 5). *Id.* at 3:20-22, 30-32.

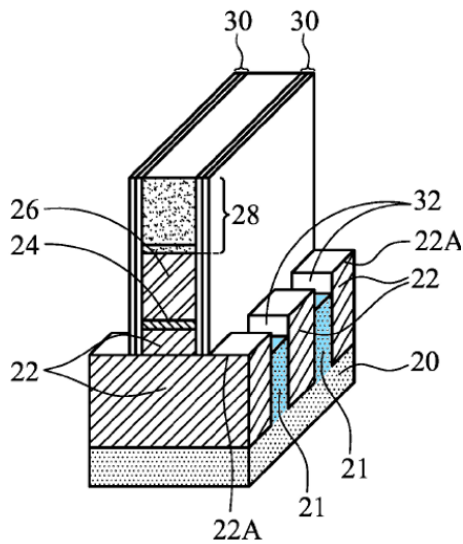


Fig. 4

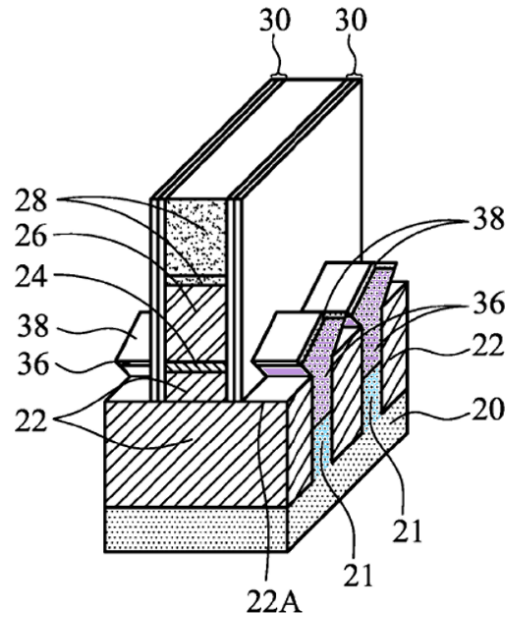


Fig. 5

Figures 8E illustrates a cross-sectional view of a device according to Ching at a later stage of fabrication. *Id.* at 4:22-25. Ching discloses that “top surfaces 22B [red lines] are higher than top surfaces 22A [green lines] of STI regions 22 [magenta].” *Id.* at 4:29-31. Further, “[i]n Fig. 8E, portions 22' of STI regions 22 [magenta] are located between opposite gate spacers 30 [dark blue], and the sidewalls of portions 22' are in contact with the sidewalls of gate spacers 30.” *Id.* at 4:31-34.

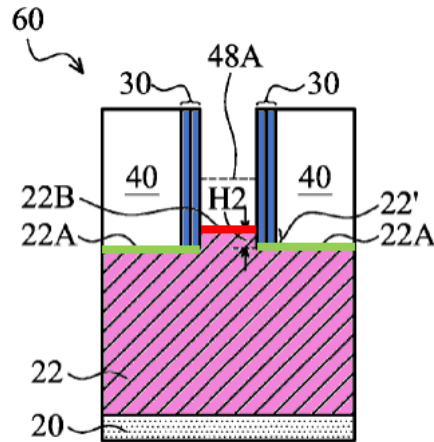


Fig. 8E

To complete formation of a FinFET, a “gate dielectric layer 50 and gate electrode 52” is formed. *Id.* at 4:39-40. Cross sectional views following this step are shown in modified Figures 9A and 9D below. Ex. 1003 at ¶ 70.

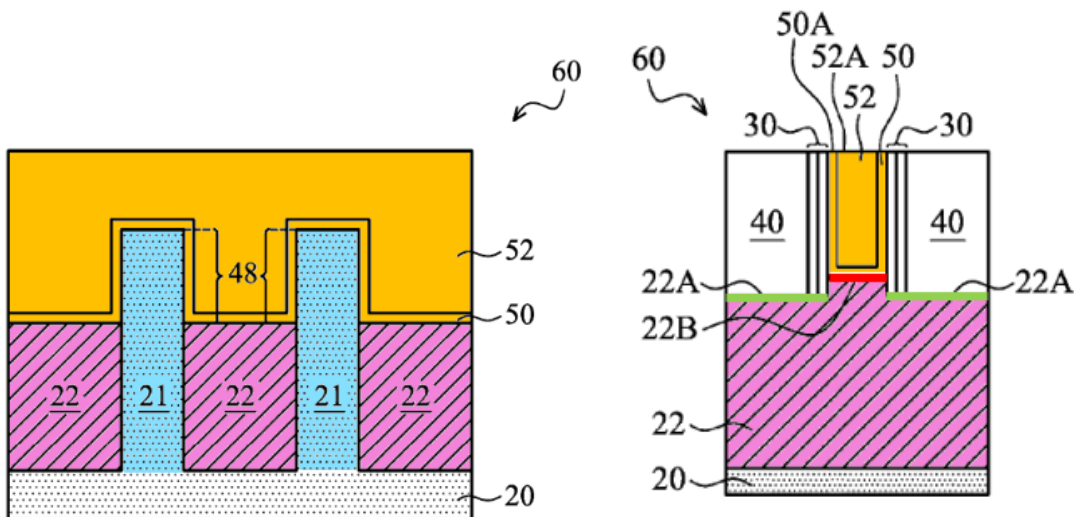


Fig. 9A

Fig. 9D

Ching concludes that “[i]t is observed that in the resulting FinFET 60, the portions of STI regions 22 that are on the opposite sides of a same gate electrode 52

(FIGS.9B, 9C, and 9D) have top surfaces 22A that are either higher than, level with, or lower than, top surface 22B that are underlying (and aligned to) gate electrode 52.” Ex. 1005 at 5:26-31.

B. Claim 1

1. 1[pre]: A semiconductor device, comprising:

The preamble is not limiting. Regardless, Ching discloses and renders obvious a semiconductor device. Ex. 1003 at ¶ 158. For example, Ching discloses a “Fin Field-Effect Transistor (FinFET),” which is a semiconductor device. Ex. 1005 at 1:53-55, 60-62; Ex. 1003 at ¶ 158.

2. 1[a]: a fin structure, protruding from a surface of a substrate, wherein the fin structure comprises a top surface and two side surfaces;

Ching discloses and renders obvious this limitation. Ex. 1003 at ¶ 159. For example, Ching discloses “semiconductor strips 21” (blue) protruding from a surface of “substrate 20,” (green) as shown in Figure 9A, below. Ex. 1005 at Fig. 9A. The “semiconductor strips 21” comprise a top surface and two side surfaces as shown below.

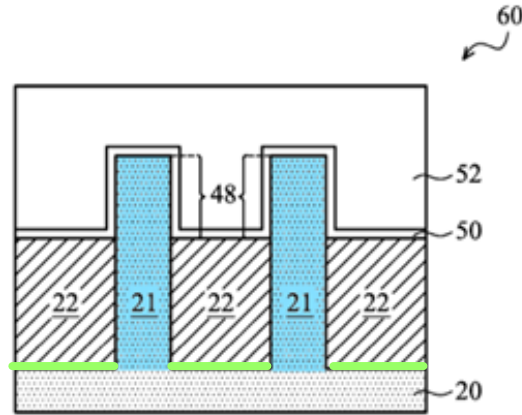


Fig. 9A

According to Ching “the portions of semiconductor strips 21 over top surface 22B form semiconductor fins 48,” confirming that semiconductor strips 21 are “fin structures.” *Id.* at 4:12-16.

This is consistent with the '609 Patent which uses the term “fin structure” to refer to the entirety of semiconductor material portions that protrude from the substrate after an etching process is performed to form such protrusions. Ex. 1003 at ¶ 161 (citing Ex. 1001 at 3:21-35).

3. 1[b]: an isolation structure, disposed on the surface of the substrate and surrounding the fin structure;

Ching discloses and renders obvious this limitation. Ex. 1003 at ¶ 162. For example, Ching discloses “STI regions 22” (magenta) disposed on the surface of substrate 20 (green) and surrounding the “semiconductor strip 21” (blue) as shown in Figure 1. Ex. 1005 at Fig. 1. According to Ching, “semiconductor strip 21 [blue]

is formed between, and contacting, neighboring STI regions 22 [(magenta)].” *Id.* at 2:5-6.

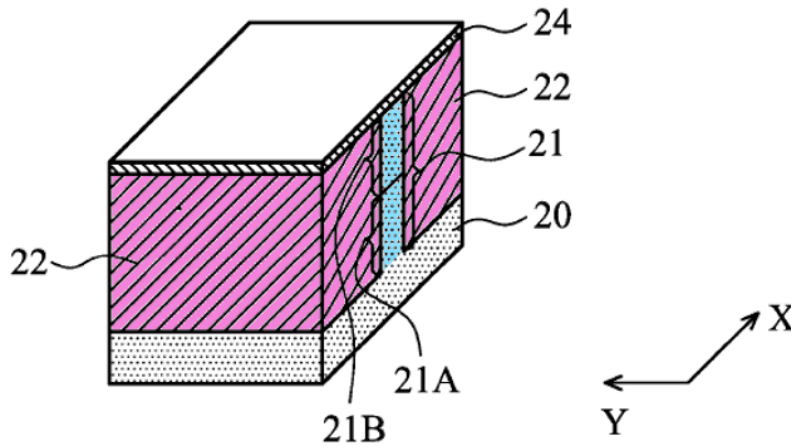
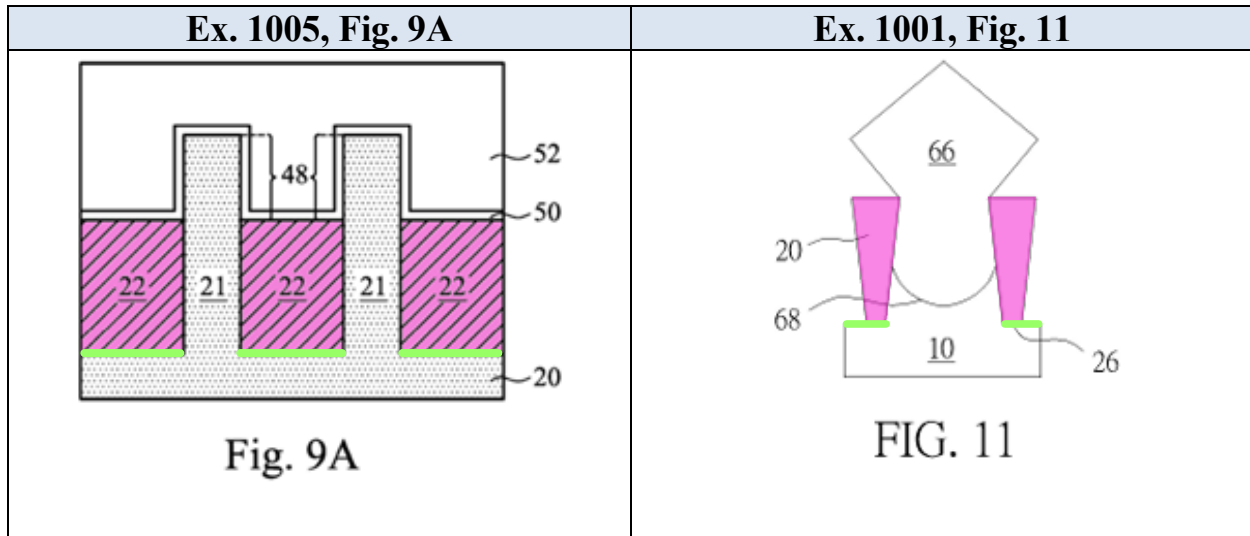


Fig. 1

While Ching discloses the STI regions are “formed in substrate 20 and extend from a top surface of substrate 20 into substrate 20” (Ex. 1005 at 2:2-4), a POSITA would have understood this as referring to an initially formed substrate which is modified to accommodate STI regions 22 resulting in a substrate 20 having the surface indicated by the green lines above. Ex. 1003 at ¶ 163 (citing Ex. 1025 and explaining well-established processes for forming STI regions). The result in Ching is a device in which the STI regions 22 (magenta) are formed on the surface (green) of the remaining substrate from which the fin structures protrude. Ex. 1003 at ¶ 163. As depicted below, this is consistent with the positioning of the isolation structures of the ’609 Patent:



Accordingly, a POSITA would have understood Ching as disclosing an isolation structure disposed on the surface of the substrate, as claimed. *See, e.g.*, Ex. 1005 at Fig. 1, Fig. 9A.

Ching further discloses the “STI regions 22” (*i.e.*, “isolation structure”) surrounding the “semiconductor strips 21” (*i.e.*, “fin structures”). Ex. 1003 at ¶ 164. For example, a cross-section of the completed transistor³ in accordance with the 8E/9D embodiment is shown below, which shows “STI regions 22” (magenta)

³ Ching discloses that the FinFET device is “finished” upon subsequent formation of ILD and contact plugs. Ex. 1005 at 5:12-17. These subsequent (and not shown) steps to not alter the structures depicted in Figs. 9A-9D and these figures therefore depict these structures as they are in the completed device.

disposed on the surface of the substrate 20 and surrounding “semiconductor strips 21.” Ex. 1005 at Fig. 9A.

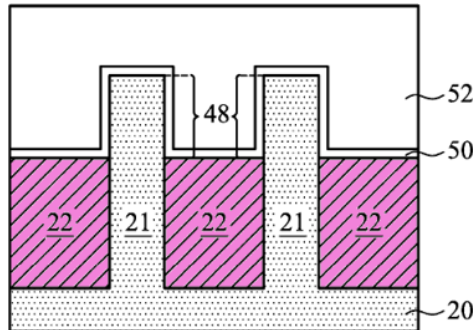


Fig. 9A

To the extent the claim language requires the isolation structure to *fully* circle the fin structures—and TSMC contends it does not—Ching discloses and renders this obvious as well. A POSITA would have further understood that, in Ching, the shallow trench *isolation* regions (“STI regions 22”) isolate “semiconductor strips 21” from one another *and* isolate the transistors that will ultimately be formed from “semiconductor strips 21” from one another. Ex. 1003 at ¶ 165. Therefore, a POSITA would have understood that “STI regions 22” surround the “semiconductor strips 21” in order for the resulting transistors to function properly. *Id.*

4. **1[c(i)]: a gate structure, overlaying the top surface and the two side surfaces of a portion of the fin structure and covering a portion of the isolation structure;**

Ching discloses and renders obvious this limitation. Ex. 1003 at ¶ 166. For example, Ching discloses a “gate dielectric layer 50 and gate electrode 52.” Ex.

1005 at 4:39-40. Ching discloses that the “gate dielectric layer 50 is formed . . . on the top surfaces and the sidewalls of semiconductor fins 48” and a “conductive material 52 is formed over gate dielectric layer 50.” *Id.* at 4:42-44, 4:56-57. Thus, the “gate structure” comprising the “gate dielectric layer 50 and gate electrode 52” overlays the top surface and two side surfaces of “semiconductor fins 48,” which is a portion of the fin structure (“semiconductor strip 21”), and covers a portion of the “STI regions 22.” Ex. 1003 at ¶ 166.

A cross-section of the completed transistor in accordance with the 8E/9D embodiment is shown below, which shows the “gate structure” (gold) overlaying the top surface and two side surfaces of a portion of “semiconductor strip 21” (blue) and covering a portion of the isolation structure, “STI regions 22” (magenta). Ex. 1005 at Fig. 9A.

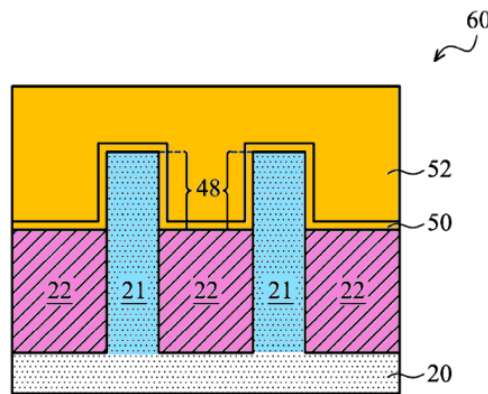


Fig. 9A

5. 1[c(ii)]: wherein the isolation structure under the gate structure has a first top surface and the isolation structure at two sides of the gate structure has a second top surface, and

**the first top surface is higher than the second top surface;
and**

Ching discloses and renders obvious this limitation. Ex. 1003 at ¶ 168. For example, Ching states:

It is observed that in the resulting FinFET 60, the portions of *STI regions 22 that are on the opposite sides of a same gate electrode 52 (FIGS. 9B, 9C, and 9D) have top surfaces 22A* that are either higher than, level with, or *lower than, top surface 22B that are underlying (and aligned to) gate electrode 52.*

Ex. 1005 at 5:26-31. As such, Ching discloses “top surface 22B that are underlying” the gate electrode (“a first top surface”) and “top surface 22A” on “the opposite sides of a same gate electrode” (“a second top surface”). *Id.*; Ex. 1003 at ¶ 168. In one embodiment, top surface 22A (“the second top surface”) is “lower than” top surface 22B (“the first top surface”). Ex. 1005 at 5:26-31. Conversely, that means “the first top surface” is higher than “the second top surface” as claimed. Ex. 1003 at ¶ 168.

A cross-section of the completed transistor in accordance with the 8E/9D embodiment is shown below. The STI (magenta) under the gate structure (gold) has a “first top surface” 22B (red) and the STI (magenta) at two sides of the gate structure (gold) has a “second top surface” 22A (green), and the “first top surface” 22B (red) is higher than the “second top surface” 22A (green). *Id.* at Fig. 9D.

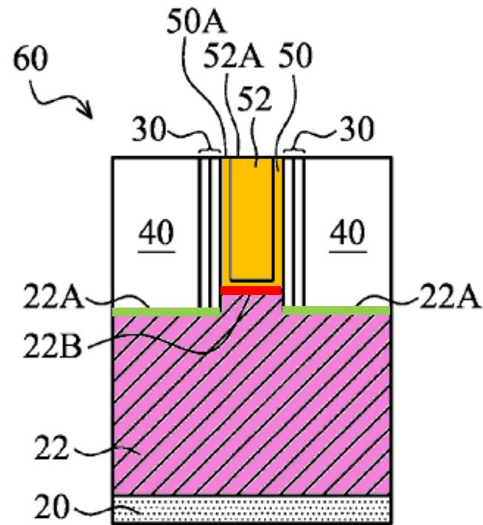


Fig. 9D

6. **1[d]: an epitaxial layer, disposed at one side of the gate structure and in direct contact with the fin structure.**

Ching discloses and renders obvious this limitation. Ex. 1003 at ¶ 170. During fabrication, portions of semiconductor strips 21 are recessed to form “recesses 32” from which epitaxy regions 36 are selectively grown. Ex. 1005 at 3:20-32. These “epitaxy regions 36” (purple) are in direct contact with “semiconductor strips 21” (blue), as shown in Figure 5. *Id.* at Fig. 5.

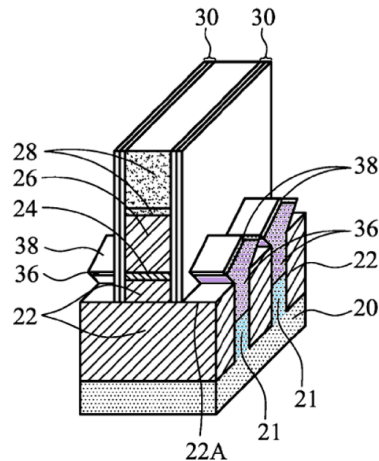


Fig. 5

As shown in Figure 5, “epitaxy regions” 36 are formed on both sides of the gate structure (dummy gate and spacers). Ex. 1003 at ¶ 171. After gate replacement steps, the epitaxy regions remain adjacent to the gate structure in the completed device, consistent with the claimed configuration. *Id.* See also Ex. 1005 at 5:12-17 (describing the formation of contact plugs that couple to “silicide regions 38” which are formed on epitaxy regions 36, thereby disclosing the presence of these epitaxy regions in the completed device).

C. Claim 3: The semiconductor device according to claim 1, wherein the gate structure is a metal gate structure.

As discussed above, Ching discloses and renders obvious a semiconductor device in accordance with claim 1.

Ching further discloses and renders obvious the additional limitations of claim 3. Ex. 1003 at ¶ 173. For example, Ching discloses forming the gate via a “replacement-gate formation process.” Ex. 1005 at 5:10. This process involves first

forming a “dummy polysilicon strip” that “is removed in an etching step, so that [a] recess 44 is formed between opposite gate spacers 30.” *Id.* at 3:65-4:3.

The “dummy polysilicon strip” is then replaced by “conductive material 52” which “may comprise a metal-containing material such as TiN, TaN, TaC, Co, Ru, Al, combinations thereof, and multi-layers thereof.” *Id.* at 4:56-60. “Conductive material 52” forms part of “the replacement gate, which includes gate electrode 52 and [high-k] gate dielectric 50, respectively, of the resulting FinFET 60.” *Id.* at 4:65-5:3. A POSITA therefore have understood Ching as disclosing “a metal gate structure” as claimed at least because the “gate electrode 52” comprises “a metal-containing material” or even specifically enumerated metals (*i.e.*, Co, Ru, Al). Ex. 1003 at ¶ 175.

Further, Ching’s disclosure of replacing “dummy polysilicon strip” with a “metal-containing material” for the gate electrode is consistent with the ’609 patent’s disclosure that a “replacement metal gate (RMG) process may be carried out so that the gate structure composed of polysilicon inside may be replaced with a metal gate structure” (Ex. 1001 at 7:12-15). Ex. 1003 at ¶ 175.

D. Claim 5: The semiconductor device according to claim 1, further comprising a recess formed at one end of the fin structure, wherein the epitaxial structure fills up the recess.

As discussed above, Ching discloses and renders obvious a semiconductor device in accordance with claim 1.

Ching further discloses and renders obvious the additional limitations of claim 5. Ex. 1003 at ¶ 177. For example, Ching discloses that “exposed portions of semiconductor strip 21 are recessed, for example, using anisotropic etching.” Ex. 1005 at 3:20-22. “The etching of semiconductor strips 21 may be continued until the top surfaces of semiconductor strips 21 are lower [*sic.*] the top surfaces 22A of STI regions 22, forming recesses 32 in STI regions 22.” *Id.* at 3:24-27. As shown in Figure 4, “recesses 32” are formed at one end of “semiconductor strips 21,” which is a “fin structure” as discussed above. *Id.* at Fig. 4; *supra* 1[a].⁴

⁴ Figure 4 contains an error where the spacers 30 are shown to extend down into the recesses 32. Ex. 1003 at ¶ 178. A POSITA would have understood that since the spacers 30 are formed (FIG. 3) before the fin structures 21 are etched down (FIG. 4), the etching of the fin structure 21 to form the recesses 32 would expose a side surface of fin structures 21 beneath the spacers 30 because that side surface was covered by the un-etched fin structure 21. *Id.* This error is not material to Petitioner’s invalidity ground. *Id.*

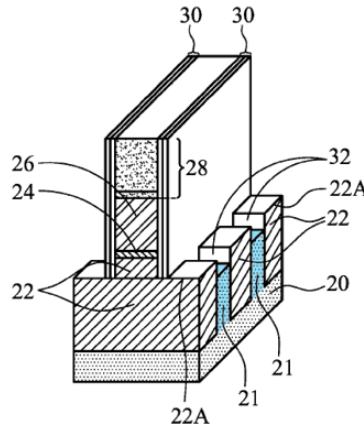


Fig. 4

Next, “recesses 32” are then filled by epitaxial structures. Ex. 1005 at 3:30-32. According to Ching, “epitaxy regions 36 are formed by selectively growing epitaxy regions 36 from recesses 32” and “recesses 32 are filled with epitaxy regions 36.” *Id.* at 3:34-35. Figure 5 shows “epitaxy regions 36” (purple) filling the “recesses 32” at the ends of the “semiconductor strips 21.” *Id.* at Fig. 5.

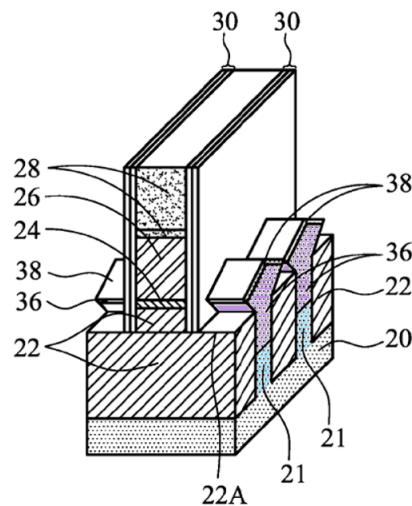


Fig. 5

The completed device shown in Figs. 9A-9D illustrate cross-sections of the device that do not intersect with the epitaxial structures. Ex. 1003 at ¶ 180.

However, a POSITA would have understood that the “epitaxy regions 36” remain in the finished device because the “epitaxy regions 36” “form source and drain regions” of the transistor, which are required for the transistor to operate. Ex. 1005 at 3:40-42; Ex. 1003 at ¶ 180.

E. Claim 6: The semiconductor device according to claim 5, wherein a bottom surface of the epitaxial structure is shallower than a bottom surface of the isolation structure.

As discussed above, Ching discloses and renders obvious a semiconductor device in accordance with claim 5.

Ching further discloses and renders obvious the additional limitations of claim 6. Ex. 1003 at ¶ 182. As described above section IV.G., a POSITA would have understood that “shallower” is in reference to the depth of the etching process that forms a recess in the fin. Accordingly, and as shown in Figure 5 below, Ching discloses that the bottom surface (yellow line) of the epitaxial structure 36 is shallower than the bottom surface (red line) of the isolation structure 22. Ex. 1005 at Fig. 5.

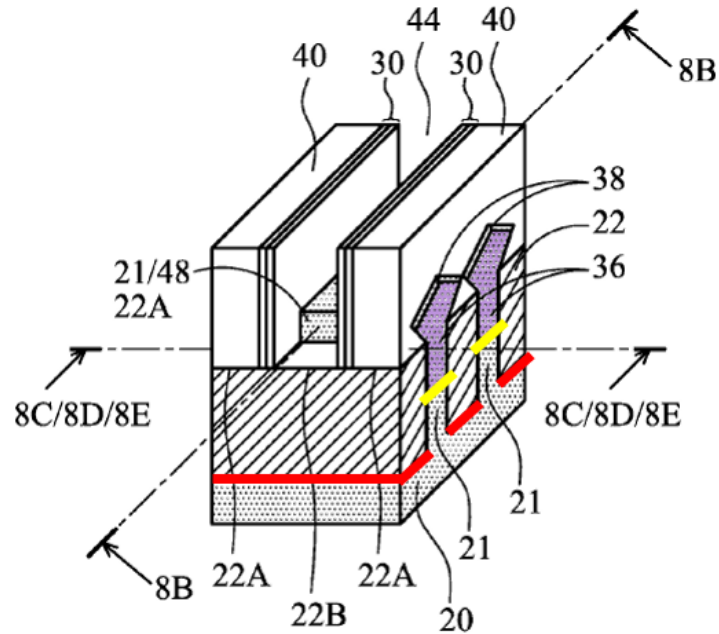


Fig. 8A

This is because, according to Ching, the bottom surface of the “Shallow Trench Isolation (STI) regions 22” extend “from a top surface of substrate 20.” *Id.* at 2:1-4. The bottom surfaces of the “epitaxy regions 36,” on the other hand, are formed “from recesses 32” at the top portions of “semiconductor strips 21,” above the top surface the substrate. *Id.* at 3:30-32; Ex. 1003 at ¶ 183.

F. Claim 8: The semiconductor device according to claim 1, wherein the epitaxial structure comprises silicon germanium, silicon phosphide or phosphor-doped silicon carbide.

As discussed above, Ching discloses and renders obvious a semiconductor device in accordance with claim 1.

Ching further discloses and renders obvious the additional limitations of claim 8. Ex. 1003 at ¶ 185. For example, Ching discloses that “[i]n some exemplary

embodiments, epitaxy regions 36 comprise **silicon germanium** or silicon carbon.”

Ex. 1005 at 3:32-33 (emphasis added).

G. Claim 9: The semiconductor device according to claim 1, further comprising a spacer disposed on a sidewall of the gate structure.

As discussed above, Ching discloses and renders obvious a semiconductor device in accordance with claim 1.

Ching further discloses and renders obvious the additional limitations of claim 9. Ex. 1003 at ¶ 187. For example, Ching discloses that “gate spacers 30 are formed on the sidewalls of hard mask strip 28 [and] polysilicon strip 26.” Ex. 1005 at 3:9-12. The “[g]ate spacers 30 are formed of dielectric materials.” Subsequently, “polysilicon strip 26 is removed in an etching step” and “hard mask layer 24 is removed,” resulting in “recess 44.” *Id.* at 3:65-4:9. As Ching recognizes, the “recess 44 is formed between opposite gate spacers 30,” as shown below in Figure 8A in dark blue. *Id.* at 3:65-67.

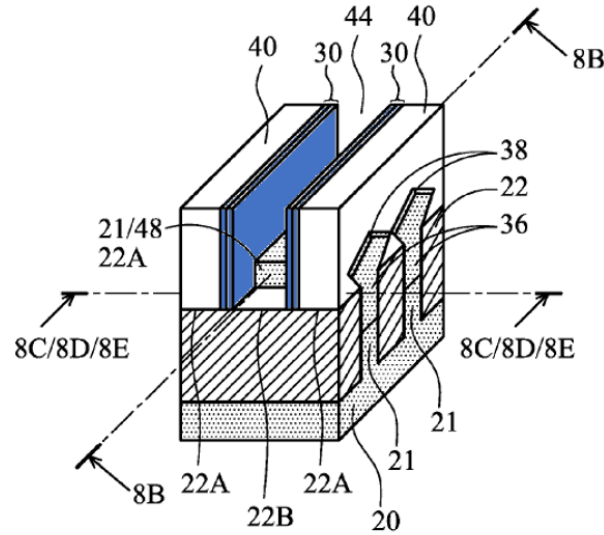


Fig. 8A

Ching further discloses that “gate dielectric layer 50 is **formed in recess 44**” and “conductive material 52 is formed over gate dielectric layer 50, **and fills the remaining recess 44.**” *Id.* at 4:42-44, 56-57 (emphasis added). The gate structure comprises the “gate dielectric layer 50” and “conductive material 52” (also referred to as the “gate electrode 52”). *Id.* at 4:65-5:3. Because the gate structure fills “recess 44,” the “gate spacers 30” are disposed on the sidewalls of the gate structure in the complete device. Ex. 1003 at ¶ 188.

A cross-section of the completed transistor in accordance with the 8E/9D embodiment is shown below, which shows spacers (dark blue) disposed on a sidewall of the gate structure 50/52. Ex. 1005 at Fig. 9D.

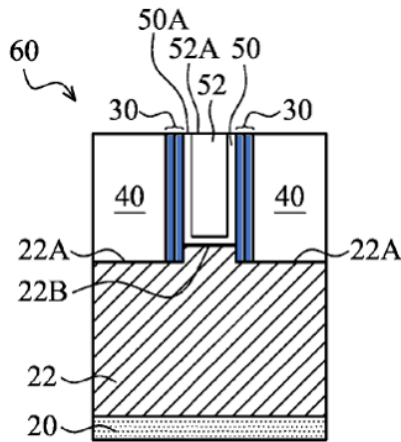


Fig. 9D

H. Claim 10

1. **10[pre]: The semiconductor device according to claim 1, further comprising:**

As discussed above, Ching discloses and renders obvious a semiconductor device in accordance with claim 1.

2. **10[a]: another epitaxial structure, disposed at another side of the gate structure and in direct contact with the fin structure; and**

Ching discloses and renders obvious this limitation. Ex. 1003 at ¶ 191. Ching explicitly illustrates another epitaxial structure 36 (purple, below silicide 38) disposed at another side of the gate structure in Figure 5. Ex. 1005 at Fig. 5. A POSITA would have understood that the epitaxial structure 36 (purple) is also in “direct contact with” the “semiconductor strip 21” (a fin structure, as discussed above) because “epitaxy regions 36 are formed by selectively growing epitaxy

regions 36 from recesses 32,” which are formed in the “semiconductor strip 21” on both sides of the gate structure. Ex. 1005 at 3:20-32; Ex. 1003 at ¶ 192.

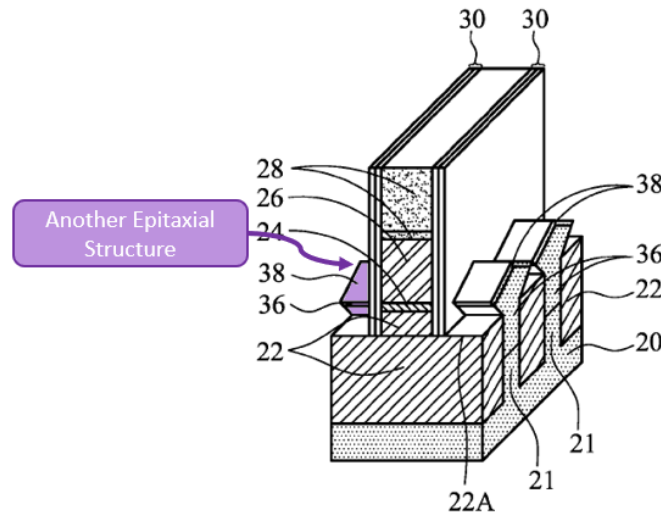


Fig. 5

Moreover, Ching’s “epitaxial structures 36” are “implanted to form source and drain regions.” Ex. 1005 at 3:40-42. A POSITA would have readily understood that the source and drain regions of a transistor are on opposite sides of the gate structure in a FinFET device. *See supra* III.A; Ex. 1003 at ¶ 192.

3. 10[b]: a channel region, contiguous to the top surface and the side surfaces of the fin structure, and between the epitaxial structure and said another epitaxial structure.

Ching discloses and renders obvious this limitation. Ex. 1003 at ¶ 193. As shown above for claim limitations 1[a] and 1[c(ii)], the gate structure overlays a top surface and two side surfaces of the fin structure. *Id.* A POSITA would have understood this region of the fin structure to constitute a channel region. *Id.* For example, Ching explicitly discloses that FinFETs have “increased channel widths”

that are “achieved by forming channels that include portions on the sidewalls of semiconductor fins and portions on the top surfaces of the semiconductor fins.” Ex. 1005 at 1:18-23. A POSITA would have therefore understood that the channel region of Ching is contiguous with the side surfaces and the top surface of the fins. Ex. 1003 at ¶ 193.

Further, as shown above for limitation 10a, the epitaxial structures 36 comprising the source and drain regions are on both sides of the gate. Ex. 1003 at ¶ 194. Therefore, the channel region of the fins 21 beneath the gate is between the epitaxial structure (one of the source/drain) and said another epitaxial structure (the other one of the source/drain). *Id.* A POSITA would have understood that this configuration establishes continuity between the fin channel and the epitaxy regions 36 because the epitaxial material is grown directly from the exposed fin surfaces following the formation of the recess. *Id.*

VII. Ground 2B: Claims 2 And 4 Are Obvious Over Ching In View Of Xu

A. Claim 2: The semiconductor device according to claim 1, wherein there is a height difference between the first top surface and second top surface, and the height difference ranges from 100 Angstroms to 250 Angstroms.

As discussed above, Ching discloses and renders obvious a semiconductor device in accordance with claim 1. Ching in view of Xu further renders obvious the additional limitations of claim 2. Ex. 1003 at ¶ 197.

For example, as discussed above with respect to claim element 1[c(ii)] and depicted in annotated Fig. 9D below, Ching discloses a vertical offset between the top surface of the isolation structure beneath the gate (red) and the top surface of isolation structure flanking the gate (green).

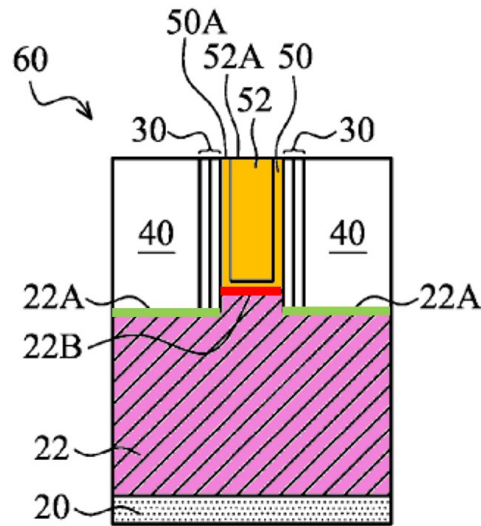


Fig. 9D

Ching discloses that the vertical offset between the top surface of the isolation structure beneath the gate and that flanking the gate differentiates its FinFETs from conventional FinFETs. Ex. 1005 at 5:26-35. Ching differs from claim 2 only in that Ching does not explicitly disclose a numerical value for this vertical offset. Ex. 1003 at ¶ 200. Accordingly, a POSITA would have consulted additional prior art, including Xu, for dimensional guidance applicable to Ching's structure. *Id.* Both Ching and Xu are directed to FinFET devices and manufacturing methods (Ex. 1005 at 1:53-56; Ex. 1004 at 1:1-3) and are aimed at keeping up with the increasing down-scaling of

integrated circuits and semiconductor devices (Ex. 1005 at 1:15-20; Ex. 1004 at 1:17-22, 34-38). A POSITA would have been motivated to look to Xu and apply its dimensional guidance to the teachings of Ching on account of these interrelated teachings and the design demands known in the industry. *See KSR Int'l Co. v. Teleflex, Inc.*, 550 U.S. 398, 418 (2007).

Specifically, Xu discloses a height difference between the first top surface and second top surface of the “isolation features 130” that results from the “etching process” that “selectively etches the isolation features 130.” Ex. 1004 at 4:58-61. Xu further discloses that “in the depicted embodiment, the etching process uses a hydrofluoric acid (HF) etching solution of a suitable concentration (for example, 100:1)” and “the HF solution **recesses the isolation features 130 about 100 Å.**” *Id.* at 4:61-65 (emphasis added).

The top surfaces of Ching’s etched isolation features 22 provide a surface for facets of the later-grown epitaxial structure. Ex. 1005 at 3:34-40. A POSITA would have understood that the etch-depth of the isolation features in combination with the depth of the fin-recess defines the starting substrate for the formation of Ching’s epitaxial structure. Ex. 1003 at ¶ 202. As Xu discloses, the starting substrate, in turn, impacts the strain that can be achieved by the device. Ex. 1004 at 15:56-66. A POSITA therefore would have found it obvious to apply the isolation etch depth of Xu to the teachings of Ching in order to optimize strain in the device, which enhances

carrier mobility and improves device performance. Ex. 1004 at 15:56-66; 1:28-30; Ex. 1003 at ¶ 202.

Moreover, while Ching does not specify the numerical extent of the STI recess or the resulting height difference, Xu provides a concrete value for this parameter (*i.e.*, about 100 Angstroms), which overlaps the claimed range of between 100 Angstroms and 250 Angstroms. Ex. 1003 at ¶ 203. And a POSITA would have understood that such a vertical offset was common in the FinFET industry when recessing isolation structures surrounding fins. *See, e.g.*, Ex. 1006 at 4:62-5:1 (disclosing recessing isolation structures surrounding the fins “by about 10 nm to about 30 nm”).

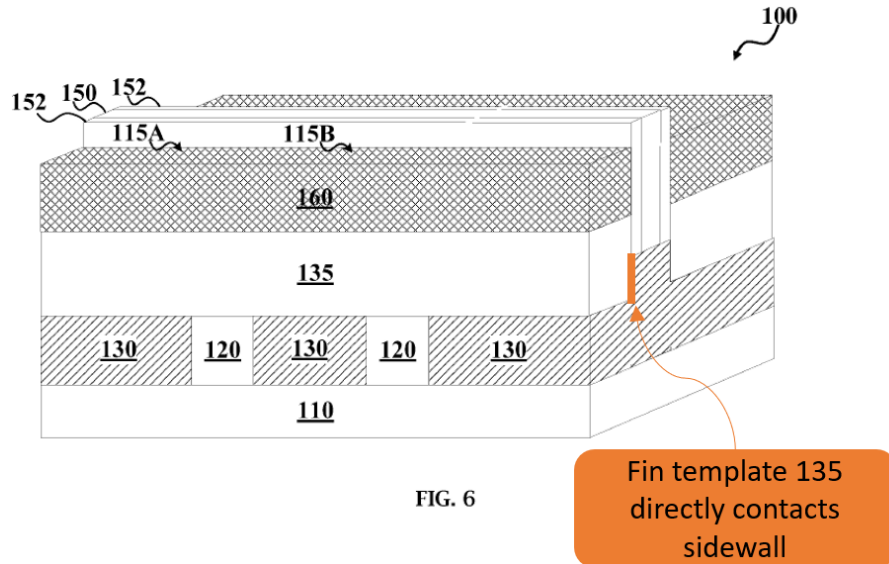
The '609 patent does not provide any evidence that the claimed range is critical or otherwise achieves unexpected results. Ex. 1003 at ¶ 204. Arriving at the claimed height difference in Ching's device therefore would have also been obvious to a POSITA from the teachings of Xu because a *prima facie* case of obviousness exists where a claimed range overlaps or lies inside ranges disclosed by the prior art. *In re Peterson*, 315 F.3d at 1329-30; *In re Geisler*, 116 F.3d at 1469-71. And a POSITA would have had a reasonable expectation of success in doing so as Xu discloses an exemplary etch process which can be used to achieve the claimed height difference. Ex. 1004 at 4:61-65; Ex. 1003 at ¶ 204.

B. Claim 4: The semiconductor device according to claim 1, wherein the isolation structure under the gate structure comprises a sidewall and the epitaxial structure is in direct contact with the sidewall.

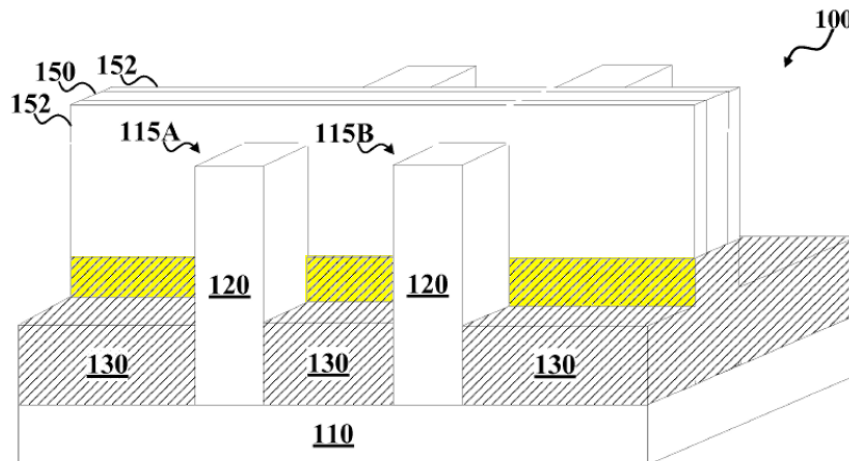
As discussed above for Ground 2A, Ching discloses and renders obvious the device of claim 1. Ching in view of Xu renders obvious claim 4. Ex. 1003 at ¶ 205.

Ching discloses the isolation structure under the gate structure comprises a sidewall. *Id.* at ¶ 206. For example, as shown in Fig. 3, Ching’s etching of the isolation structure recesses portions of STI regions 22 while leaving “un-recessed portions of STI regions 22” under the gate structure. *Id.* at ¶ 206 (quoting Ex. 1005 at 3:9-12). Ching, however, does not teach a sidewall in direct contact with the epitaxial structure (because its gate spacers 30 are located between the relevant sidewall and the epitaxial structure). Ex. 1005 at 2:59-3:19; Ex. 1003 at ¶ 206.

In contrast, Xu discloses the claimed direct contact. Ex. 1003 at ¶ 207. Specifically, Xu discloses the “fin template 135” (*i.e.*, the claimed “epitaxial structure”) is in direct contact with the sidewall of the “isolation features 130” under the “gate structure 150,” as shown in annotated Figure 6 below. Ex. 1004 at Fig. 6; Ex. 1003 at ¶ 207.



Xu achieves this result because it performs certain steps in a different order than Ching. Specifically, Xu applies “an etching process [] to recess isolation features 130” after gate spacers 152 are already formed. Ex. 1004 at 4:54-61. In doing so, the etching process exposes sidewalls of the isolation structure under the gate structure (yellow below) that directly abut the later-formed epitaxial structure:



It would have been obvious to a POSITA to apply the teachings of Xu to the teachings of Ching relative to the processing steps that result in the claimed direct contact. This is because, among other reasons, the processing steps applied in Xu provide advantages when forming the gate structure. Ex. 1003 at ¶ 208.

For example, a POSITA would have recognized that Ching's process of executing the STI recess etch before spacer formation exposes the sidewalls of the polysilicon strip 26 during etching. Ex. 1005 at 2:45-64. The POSITA would have understood that polysilicon strip is a "dummy polysilicon strip" used to preserve space for a later-formed gate electrode. Ex. 1005 at 3:65-4:3. Such gate-last schemes are advantageous because the "final metal gate is not exposed to the high activation anneal for the junctions." Ex. 1008 at 16. "As a result, a better controlled work function for nMOS and pMOS can be achieved." *Id.*

Accordingly, the POSITA would have found it obvious to modify Ching to perform gate spacer formation prior to etching the STI structure, as taught by Xu, in order to maintain the shape and alignment of the dummy gate for later replacement with a high-performance gate metal, thereby allowing for more reliable gate-last processing and its associated electrical advantages. *Id.* at ¶ 210 (citing Ex. 1008 at 16).

As a result, the Ching-Xu combination would include portions of the STI of Ching exposed under the sidewall spacers, similar to the structure shown in Xu. Ex.

1003 at ¶ 211. Specifically, forming the sidewall spacers first ensures that the sidewalls do not extend vertically below the original height of the STI. *Id.* This principle is demonstrated in modified Fig. 2 of Xu, below:

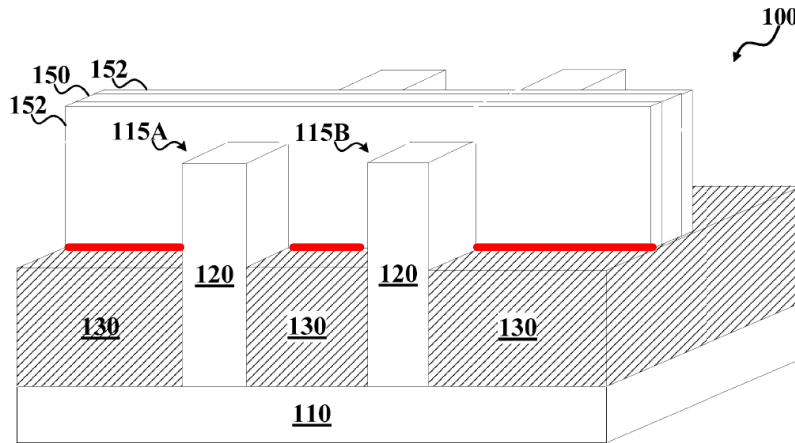
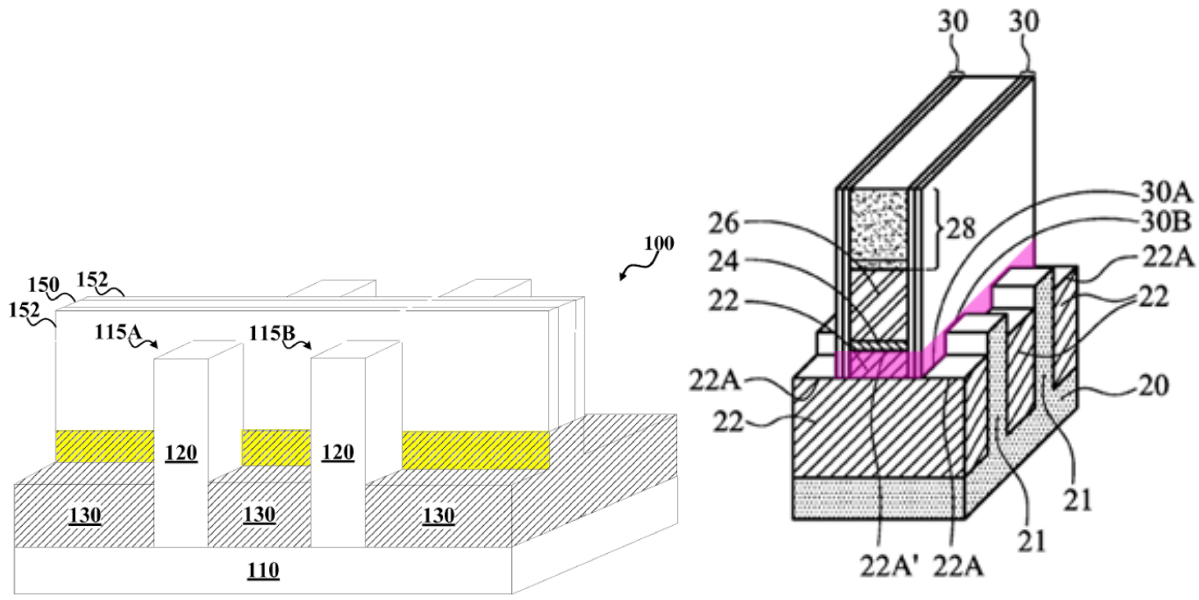


FIG. 2

When the etch occurs, portions of 130 directly underlying 152 are then exposed. *Id.* Applying this feature to Ching would result in similar exposure of the portions of the STI underlying Ching's sidewall spacers. *Id.* The modified figures below show the exposed isolation structure of Xu (yellow) and the corresponding exposed STI in the combination of Ching and Xu:



A POSITA would have understood that the Ching-Xu combination would then undergo the processing steps as taught by Ching, resulting in epitaxial structures 36 directly contacting the exposed sidewalls of the STI under the gate structure, as claimed. Ex. 1003 at ¶ 212.

Moreover, a POSITA would have found it obvious to make this modification and had a reasonable expectation of success in doing so because the combination involves no more than changing the sequence of steps of Ching. *Id.* Both the deposition of gate sidewall spacers and the isolation etch are well-known, conventional processes that a POSITA would have been able to perform in either order, and performing the sidewall deposition first does not achieve any unexpected results. *Id.* Accordingly, reordering these steps would have been obvious to a POSITA. *Ex Parte Wilson*, Appeal 2014-003909, 2016 WL 1107699, at *11 (PTAB Mar. 17, 2016)

(“a mere change in the timing or sequence of method steps without any new or unexpected results is *prima facie* obvious.”).

VIII. Ground 2C: Claim 7 Is Obvious Over Ching in View of Huang

A. Claim 7: The semiconductor device according to claim 6, wherein there is a height difference between the bottom surface of the epitaxial structure and the bottom surface of the isolation structure, and the height difference ranges from 100 Angstroms to 250 Angstroms.

As discussed above, Ching discloses and renders obvious the fabrication method of claim 1. Ching in view of Huang renders obvious claim 7. Ex. 1003 at ¶ 214.

As further discussed above with respect to claim 6, Ching discloses the bottom surface of the epitaxial structure (yellow) is shallower than the bottom surface of the isolation structure (red):

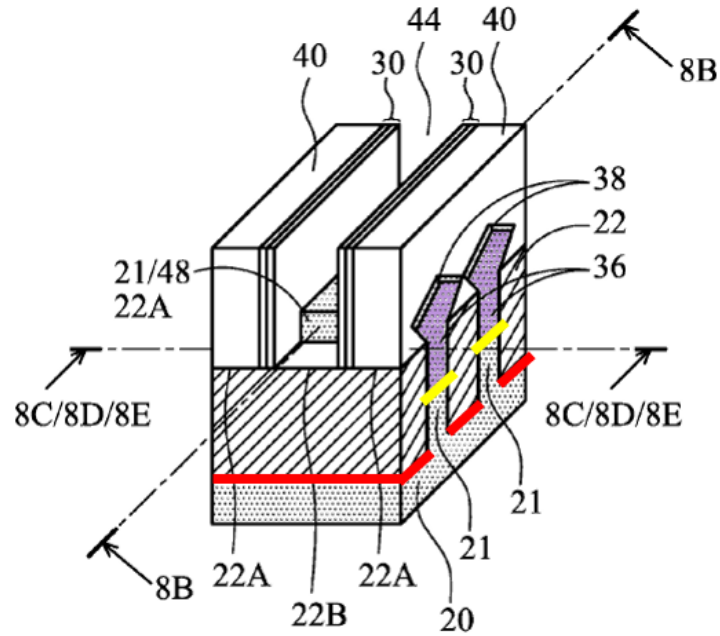


Fig. 8A

Ex. 1005 at Fig. 8A (modified).

Ching, differs from claim 7 only in that Ching does not explicitly disclose specific numerical values for the depth of the recess or the dimensions of the surrounding features. Ex. 1003 at ¶ 216. A POSITA would have understood that this recess depth is a results-effective variable that can be used to tailor strain induced on the FinFET channel and optimize performance. *Id.* (citing Ex. 1004 at 10:34-47, 15:67-16:4). Moreover, Ching discloses an example etch technique that can be used to achieve this recess (Ex. 1005 at 3:20-29) and a POSITA would have been familiar with ways to tune etch depths and etch profiles (Ex. 1003 at ¶ 216 (citing Ex. 1025)). A POSITA therefore would have found it obvious to optimize the etch depth through

routine experimentation to yield a desired strain. *In re Aller*, 220 F.2d at 456; Ex. 1003 at ¶ 216.

In doing so, a POSITA would have found it obvious to turn to additional prior art, such as Huang for guidance concerning the recess depth. *Id.* at ¶ 217. Both Ching and Huang are directed to FinFET devices and methods (Ex. 1005 at 1:53-56; Ex. 1006 at 2:1-4) and are aimed at keeping up with the increasing down-scaling of integrated circuits and semiconductor devices (Ex. 1005 at 1:15-20; Ex. 1006 at 1:6-9). A POSITA would have been motivated to look to Huang and apply its dimensional guidance to the teachings of Ching on account of these interrelated teachings and the design demands known in the industry. *See KSR*, 550 U.S. 398 at 418.

In particular, it would have been obvious to a POSITA from the teachings of Huang to optimize Ching's height difference through routine experimentation and arrive at the claimed height difference. *In re Aller*, 220 F.2d at 456. *See also* Section V.B., *supra* (detailing obviousness of such optimization with respect to the Xu-Huang combination); Ex. 1003 at ¶ 218. The POSITA would have had a reasonable expectation of success in so given the desirability of the lower-end of Huang's range (Ex. 1005 at 1:15-20; Ex. 1006 at 1:6-9) and Huang's disclosure of exemplary etch processes to achieve the claimed height difference (Ex. 1006 at 2:45-67, 4:10-29). Ex. 1003 at ¶ 218.

A POSITA also would have found it obvious to apply the height difference of Huang, which entirely encompasses the claimed range of from 100 Angstroms to 250 Angstroms (*id.* at ¶ 219), to the teachings of Ching to arrive at the claimed height difference because a *prima facie* case of obviousness exists where a claimed range “overlaps or lies inside ranges disclosed by the prior art.” *In re Peterson*, 315 F.3d at 1330; *In re Geisler*, 116 F.3d at 1469-71. *See also* Section V.B., *supra* (describing obviousness in light of Huang’s overlapping range with respect to the Xu-Huang combination); Ex. 1003 at ¶ 219.

IX. Mandatory Notices under 37 C.F.R. § 42.8

A. Real Parties-in-Interest

The real party-in-interest is Taiwan Semiconductor Manufacturing Company Limited.

B. Related Matters

- The ’609 patent is not currently the subject of any litigation.

C. Grounds for Standing

Petitioner certifies that the ’609 patent is available for *inter partes* review and that TSMC is not barred from requesting this proceeding.

D. Lead and Backup Counsel and Service Information

Pursuant to 37 C.F.R. §§ 42.8(b)(3), 42.8(b)(4), and 42.10(a), Petitioner designates the following lead and backup counsel:

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Pursuant to 37 C.F.R. § 42.10(b), a Power of Attorney from TSMC is attached. TSMC consents to electronic service.

E. Fee for *Inter Partes* Review

The Director is authorized to charge the fee specified by 37 C.F.R. § 42.15(a) to Deposit Account No. 505013.

X. Conclusion

For the reasons set forth above, Petitioner TSMC respectfully requests *inter partes* review of the Challenged Claims of the '609 patent.

Dated: November 14, 2025

Respectfully submitted,

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CERTIFICATE OF SERVICE

The undersigned hereby certifies that a copy of the foregoing petition for *Inter Partes* Review of U.S. Patent No. 9,318,609, including all Exhibits, was served on November 14, 2025 via DHL Express delivery directed to the attorney of record for the patent at the following address:

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CERTIFICATE OF WORD COUNT UNDER 37 C.F.R. § 42.24(a)

I, the undersigned, do hereby certify that the attached petition contains 13,976 words, as measured by the Word Count function of Microsoft Word, excluding this Certification and the following: Table of Contents, List of Exhibits, Mandatory Notices, and Certificate of Service. This is less than the limit of 14,000 words as specified by 37 C.F.R. § 42.24(a)(i).

Date: November 14, 2025

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