A 90nm High Volume Manufacturing Logic Technology Featuring Novel 45nm Gate Length Strained Silicon CMOS Transistors

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I. Abstract

This paper describes the details of a novel strained transistor architecture which is incorporated into a 90nm logic technology on 300mm wafers [1]. The unique strained PMOS transistor structure features an epitaxially grown strained SiGe film embedded in the source drain regions. Dramatic performance enhancement relative to unstrained devices are reported. These transistors have gate length of 45nm and 50nm for NMOS and PMOS respectively, 1.2nm physical gate oxide and Ni salicide. World record PMOS drive currents of 700μA/μm (high V_T) and 800μA/μm (low V_T) at 1.2V are demonstrated. NMOS devices exercise a highly tensile silicon nitride capping layer to induce tensile strain in the NMOS channel region. High NMOS drive currents of 1.26mA/μm (high V_T) and 1.45mA/μm (low V_T) at 1.2V are reported. The technology is mature and is being ramped into high volume manufacturing to fabricate next generation Pentium® and Intel®Centrino™ processor families.

II. Strained Silicon Transistors

Figure 1 shows a TEM cross-section of our PMOS transistor. The unique feature of this transistor entails embedding a compressively strained SiGe film in the source drain regions by using a selective epitaxial growth process. A combination of compressive SiGe strain and embedded SiGe S/D geometry induces a large uniaxial compressive strain in the channel region, thereby resulting in significant hole mobility improvement. Dramatic (>50%) strain induced hole channel mobility improvement is demonstrated for our devices with 17% Ge composition. Fig. 2 shows significant improvement in measured PMOS linear drive (>50%) and I_{DSAT} (>25%) due to channel strain for our devices. As shown in Fig. 3, the uniaxial strain for this PMOS device results in higher mobility enhancement vs. vertical electric field relative to a biaxially strained device. In contrast to the results reported in [2,3], the hole mobility improvement is maintained at higher vertical electric fields for our devices. Fig. 4 shows key features of the process flow sequence used in fabricating strained transistors reported in this work. It entails inserting a substrate recess etch & selective epitaxial SiGe deposition to the standard PMOS process sequence after spacer formation.

Fig. 5 shows a TEM cross-section of our NMOS transistor. One unique feature of this NMOS structure is the integration of a post salicide "highly-tensile" silicon nitride capping layer. The stress from this capping layer is uniaxially transferred to the NMOS channel through the source-drain regions to create tensile strain in NMOS channel [4,5]. Figure 6 shows modulation of measured integrated film stress and the resultant NMOS Idsat improvement with increasing tensile film thickness for our devices. Capping layer thickness is selected to be ~75nm for our devices to provide 10% NMOS I_{DSAT} gain from tensile channel strain.

The combined techniques of selective SiGe source-drain and high stress silicon nitride capping layer are low cost and highly manufacturable means to induce strain in transistors and allow for separate optimization of PMOS and NMOS devices. This approach to strain engineering has an advantage over the conventional biaxially strained substrate technique reported by others [2,3] in that it uses standard Si wafers and avoids the cost, defect and other process integration issues associated with SiGe wafers.

III. Transistor Performance

Superb short channel effects are achieved through extension and halo doping profile engineering to support physical gate length of 45nm and 50nm for our NMOS & PMOS devices respectively. Figure 7 shows good short channel effects for NMOS & PMOS devices at target gate length with sub-threshold slope below 100mV/dec. Figures 8 and 9 show NMOS and PMOS threshold voltage vs. gate length indicating good V_T rolloff down to 45nm gate length.

Fig. 10 shows PMOS drive current of 700μA/μm at 1.2V with 40nA/μm of leakage for high V_T devices. Low V_T devices with 400nA/μm of leakage have an astounding 800μA/μm drive current at 1.2V. Fig. 11 shows NMOS drive current of 1.26mA/μm at 1.2V with 40nA/μm of leakage for high V_T devices. Low V_T devices offer 15% higher drive current at 400nA/μm leakage.

IV. Yield & Manufacturability

One concern with our strained PMOS structure is the need for selective SiGe epitaxy. Fig.12 shows a dramatic reduction in SiGe defect adders on product wafers as a result of our focused effort in minimizing these defects by optimizing epitaxial deposition during the course of process development. Fig. 12b shows evidence of superb epi film selectivity across 300mm wafer achieved for our process as a result of this effort. As shown in Fig. 13, this process is demonstrating stable high yields on microprocessor products with yield learning in line with our historical trend. Fig. 14 shows a die photo of next generation Pentium® processor fabricated using 90nm logic technology on 300mm wafers. This technology is being ramped into high volume manufacturing.

V. Conclusions

A highly manufacturable technique for improving transistor performance through strain engineering is reported, which includes a novel PMOS transistor structure. World record drive currents at low off currents are reported. These transistors are incorporated in a 90 nm logic technology presently being ramped to high volume on high performance microprocessors. We believe this is the first time that strained Si transistors are being implemented in a manufacturing technology.

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References

[1]. S. Thompson et al., IEDM Tech Dig., pp. 61-64, (2002)
[2]. K. Rim et al., Symp. VLSI Tech Dig.., pp. 98-99, (2002)
[3]. K. Rim et al., IEDM Tech Dig., pp. 517-521, (1995)
[4]. S. Ito et al., IEDM Tech Dig., pp. 247-251, (2000)
[5]. A. Shimizu et al., IEDM Tech Dig., pp. 433-437, (2001)

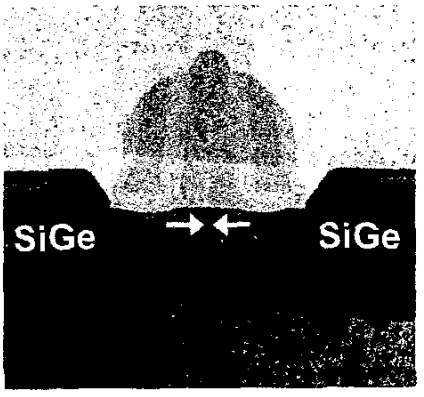

Fig. 1: TEM of PMOS Transistor. A strained epitaxial SiGe film is embedded into the source drain region to induce compressive strain in the channel region.

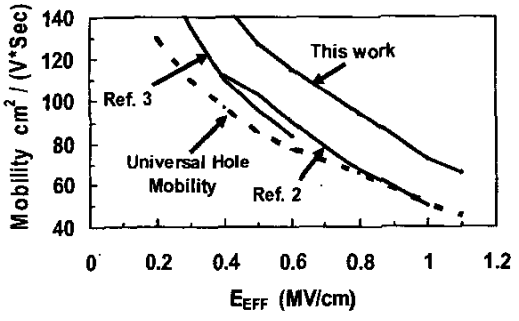

Fig. 3: Hole mobility as a function of vertical effective field for our uniaxially strained PMOS device [1] relative to conventional biaxially strained substrate techniques [2,3].

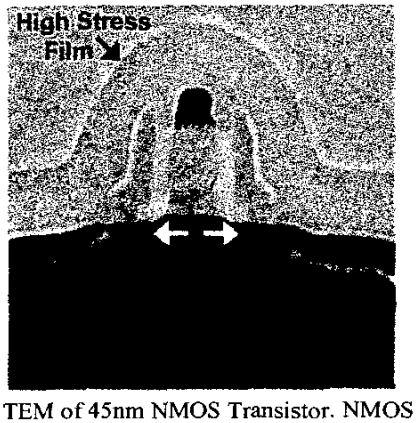

Fig. 5: TEM of 45nm NMOS Transistor. NMOS device is capped with a specially engineered high tensile stress silicon nitride layer to induce tensile channel strain.

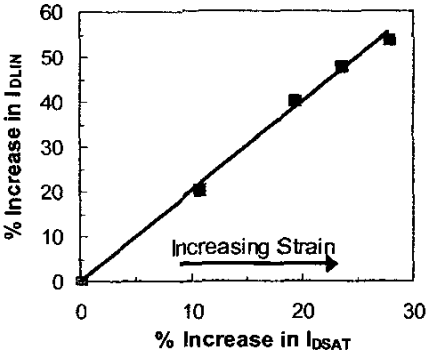

Fig. 2: Measured % improvement in PMOS linear drive (I_{DLIN}) vs. I_{DSAT} with increasing PMOS channel strain. I_{DLIN} gain is 2x I_{DSAT} gain due to larger sensitivity of I_{DLIN} on channel mobility.

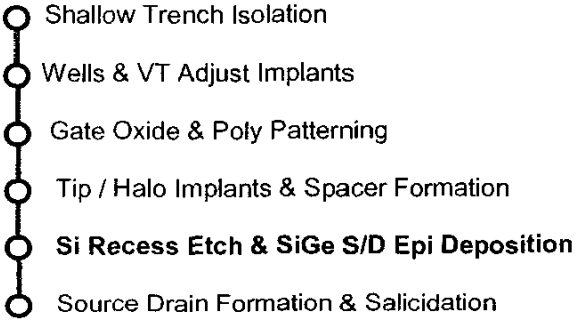

Fig. 4: Process flow sequence for our Strained SiGe source drain PMOS device structure. "Si recess Etch & SiGe S/D Epi Deposition" steps are added to the standard non-strained PMOS process to create strained PMOS devices.

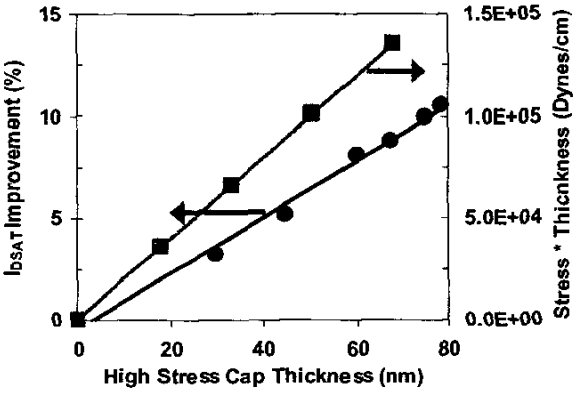

Fig. 6 Measured integrated film stress and the resultant NMOS I_{DSAT} improvement with increasing tensile film thickness for our devices. Tensile film thickness is selected to increase NMOS I_{DSAT} by 10% for our devices.

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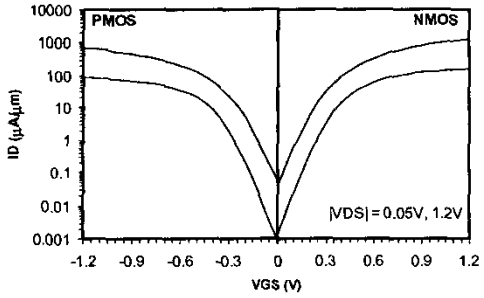


Fig. 7: NMOS and PMOS subthreshold curves.

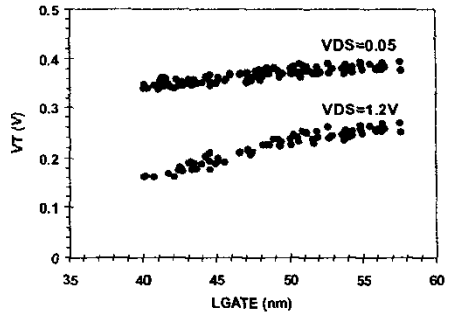


Fig. 8: V_T vs. gate length for NMOS at low and high V_{DS}

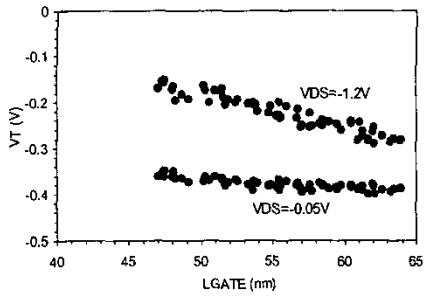


Fig. 9: V_T vs. gate length for PMOS at low and high V_{DS}

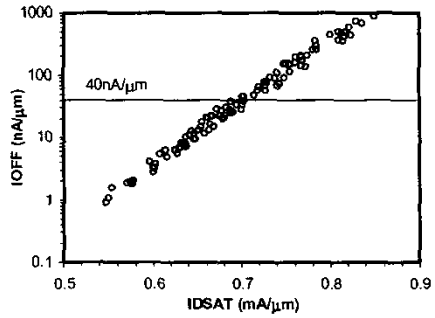


Fig. 10: PMOS I_{DSAT} vs. I_{OFF} at 1.2V

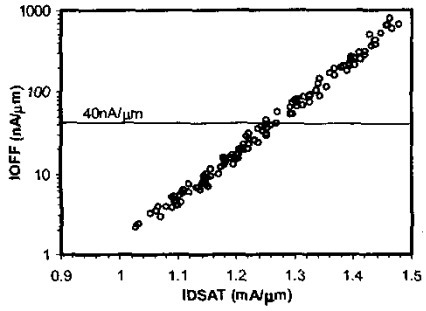
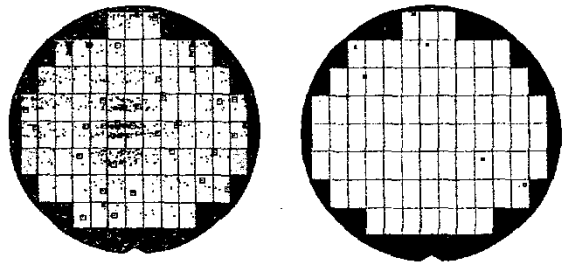


Fig. 11: NMOS I_{DSAT} vs. I_{OFF} at 1.2V



(a) (b)

Fig. 12: Wafer level plots of SiGe defect adders during selective SiGe deposition on 300mm product wafers. Fig. 12a shows SiGe defect adders during initial development phase while Fig. 12b shows a dramatic improvement in epi defects as a result of focused epi defect reduction effort.

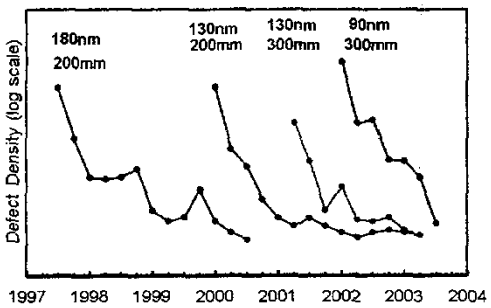


Fig. 13: Yield improvement trend for 90nm technology with strained silicon shows 2 year offset from 130nm.

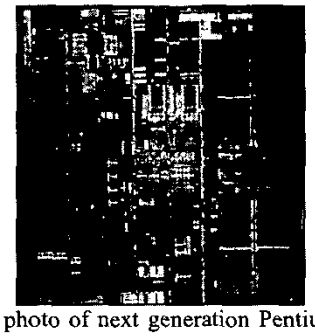


Fig. 14: Die photo of next generation Pentium® processor fabricated using 90nm logic technology and exercising strained transistors described in this work.

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