

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Taiwan Semiconductor Manufacturing Company Ltd.,
Petitioner

v.

Marlin Semiconductor Ltd.,
Patent Owner

Case No. – Not Yet Assigned
U.S. Patent No. 9,318,609

**DECLARATION OF DR. JACK LEE IN SUPPORT OF PETITION FOR
INTER PARTES REVIEW OF UNITED STATES PATENT NO. 9,318,609**

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I, Jack Lee, do hereby declare:

1. My name is Jack Lee. I am making this declaration at the request of Taiwan Semiconductor Manufacturing Company Limited (“TSMC”) in the matter of the *Inter Partes* Review of U.S. Patent No. 9,318,609 (“the ’609 Patent”).

2. I am being compensated for my work in this matter at my standard rate of \$680 per hour for such consulting services. My compensation in no way depends on the outcome of this proceeding.

3. I have been asked to provide my opinion on the technology covered by the ’609 Patent and the validity or invalidity of claims 1-9 of the ’609 Patent (“Challenged Claims”).

I. Qualifications

4. My qualifications generally are set forth in my *curriculum vitae*, which is submitted as Exhibit 1026.

5. I am an expert in the field of semiconductor design and process technology and have forty years of first-hand experience as a researcher, educator, and consultant in this field.

6. I received a B.S. degree in Electrical Engineering, with highest honors, in 1980, and an M.S. degree in Electrical Engineering in 1981, both from University of California, Los Angeles. I received a Ph.D. degree in Electrical Engineering in 1988 from University of California, Berkeley (“UC Berkeley”).

7. From 1979 to 1984, I was a Member of Technical Staff at the TRW Microelectronics Center, in the High-Speed Bipolar Device Program. I worked on bipolar device/circuit design, fabrication, and testing. I was promoted to Engineering Group Leader level in 1983.

8. I received several academic honors while at UC Berkeley. For example, I won the Best Paper Award from the Institute of Electrical and Electronics Engineers (“IEEE”) International Reliability Physics Symposium in 1988. I was also awarded a Lectureship with my own teaching assistant from UC Berkeley.

9. After receiving my Ph.D. in August 1988, I joined the faculty at The University of Texas at Austin (“UT Austin”). As a faculty member, I have taught numerous courses in semiconductor device fabrication and design, at both the undergraduate and graduate levels. I have supervised over 40 students who received their doctoral degrees under my guidance. Since September 2000, I have held the Cullen Trust for Higher Education Endowed Professor in Engineering in the Department of Electrical and Computer Engineering at UT Austin. In September 2023, I was promoted to the Professor Emeritus level.

10. My current research and teaching interests encompass semiconductor devices including 3D structures such as FinFETs or tri-gate MOSFETs, high-K gate dielectrics and gate electrodes, fabrication processes, electrical and material characterization, reliability and modeling, packaging technologies, dielectric and

passivation processes, display technologies, photovoltaic and solar cell technologies, semiconductor memory applications, and alternative channel materials.

11. I have been invited to give talks, teach short courses and participate in panel discussions at numerous conferences specifically on the topic of fabrication processes for nanoscale devices such as FinFETs and gate-all-around MOSFETs, high-K gate dielectrics, gate electrodes, and semiconductor memory devices. This includes prestigious conferences such as the Symposium on VLSI Technology, the IEEE International Electron Devices Meeting, and other global forums. My research group at The University of Texas at Austin is recognized as a pioneer in developing high-K gate dielectric metal-gate processes for nanoscale MOSFETs including FinFETs. I have extensive experience in this field, with numerous publications in journals and conference proceedings on the topics of nanoscale MOSFETs and FinFETs, fabrication processes, characterization, and device reliability.

12. My research has been partially supported by grants from the National Science Foundation, the Texas Advanced Research Program, the Semiconductor Research Corporation (SRC), SEMATECH, Texas Emerging Technology Funds, and others.

13. I have authored over 600 journal publications and conference proceeding papers and have coauthored 8 book and book chapters on semiconductor technologies.

I am a named inventor of 9 U.S. patents. I have also received numerous teaching and research awards, e.g. inventor recognition and best paper awards.

14. In 2002, I became an IEEE fellow for my “contributions to the understanding and development of ultra-thin dielectrics and their application to silicon devices.” I was also an IEEE Electron Devices Society Distinguished Lecturer from 2004 to 2016.

15. I have served in various technology consulting and business advisor roles. For example, I have been teaching short courses on semiconductor device physics and technologies at various semiconductor companies and consortiums (e.g., SEMATECH). I have also organized several international conferences and have given lectures at numerous conferences and symposia, including the International Symposium on VLSI Technologies, the IEEE Symposia on VLSI Technology, and the IEEE International Electron Devices Meeting. These conferences are some of the most prestigious in the field

16. Taken as a whole, my academic and practical experience have given me a substantial basis upon which to evaluate the technology that is in question in the claims of the '609 patent. Based on my experience and education, and the acceptance of my publications and professional recognition by peers in my field, I believe that I am qualified to opine as to the knowledge and level of skill of one of ordinary skill in the art at the time of the alleged invention of the '609 patent (which I further describe

below) and what such a person would have understood at that time, and the state of the art during that time.

II. Materials Reviewed

17. In forming the opinions expressed in this Declaration, I relied upon my education and experience in the relevant field, and have considered the viewpoint of a person having ordinary skill in the art (POSITA) at the time of the invention of the '609 Patent.

18. I understand that the prior art references and other documents that I discuss in this declaration will be filed with the Petition for *Inter Partes* Review in this matter ("Petition") and assigned exhibit numbers. I also understand that other exhibits, not referenced in this declaration may also be filed with the Petition.

19. In forming my opinions, I have reviewed and considered the following documents, identified by exhibit number:

Exhibit No.	Description
Exhibit 1001	U.S. Patent No. 9,318,609 ("'609 patent").
Exhibit 1002	Prosecution History of the '609 patent.
Exhibit 1004	U.S. Patent No. 9,166,022 B2 ("Xu").
Exhibit 1005	U.S. Patent No. 9,281,378 ("Ching").
Exhibit 1006	U.S. Patent No. 8,809,139 B2 ("Huang").
Exhibit 1007	T. Ghani et al, <i>A 90nm High Volume Manufacturing Logic Technology Featuring Novel 45 Nm Gate Length Strained Silicon CMOS Transistors</i> , IEEE International Electron Devices Meeting 2003, pp. 11.6.1-11.6.3, (2003).
Exhibit 1008	Excerpts from N. Collaert, <i>CMOS Nanoelectronics</i> (2012).
Exhibit 1009	Intentionally left blank
Exhibit 1010	Intentionally left blank

Exhibit 1011	Intentionally left blank
Exhibit 1012	Intentionally left blank
Exhibit 1013	D. Hisamoto et al., <i>Folded-channel MOSFET for deep-sub-tenth micron era</i> , International Electron Devices Meeting 1998 – Technical Digest, pp. 1032-1034, (1998).
Exhibit 1014	X. Huang et al., <i>Sub 50-nm FinFET: PMOS</i> , International Electron Devices Meeting 1999 – Technical Digest, pp. 67-70, (1999)
Exhibit 1015	D. Hisamoto et al., <i>FinFET – a self-aligned double-gate MOSFET scalable to 20 nm</i> , IEEE Transactions on Electron Devices, Vol. 47, No. 12, pp. 2320-2325 (2000)
Exhibit 1016	J. Markoff, <i>Intel Increases Transistor Speed by Building Upward</i> , New York Times (2011)
Exhibit 1017	Intel, <i>Intel's Revolutionary 22 nm Transistor Technology</i> (2011).
Exhibit 1018	A. Shimpi, <i>Intel Announces first 22nm 3D Tri-Gate Transistors, Shipping in 2H 2011</i> , AnandTech (2011) (archived May 18, 2011).
Exhibit 1019	K. Mistry et al., <i>A 45nm Logic Technology with High-k+ Metal Gate Transistors, Strained Silicon, 9 Cu Interconnect Layers, 193nm Dry Patterning, and 100% Pb-free Packaging</i> , 2007 IEEE International Electron Devices Meeting, pp. 247-250 (2007).
Exhibit 1020	Intentionally left blank
Exhibit 1021	S. Thompson et al., <i>Key Differences for Process-Induced Uniaxial vs. Substrate-Induced Biaxial Stressed Si and Ge Channel MOSFETs</i> , Technical Digest of the 2004 IEEE International Electron Devices Meeting (IEDM), pp. 221-224 (2004)
Exhibit 1022	C. Auth et al., <i>45nm High-k + Metal Gate Strain-Enhanced Transistors</i> , 2008 Symposium on VLSI Technology, pp. 128-129, (2008)
Exhibit 1023	S. Mayuzumi et al., <i>High-Performance Metal/High-k n- and p-MOSFETs With Top-Cut Dual Stress liners Using Gate-Last Damascene Process on (100) Substrates</i> , IEEE Transactions on Electron Devices, Vol. 56, No. 4, pp. 620-626, (2009)
Exhibit 1024	Intentionally left blank
Exhibit 1025	Excerpts from S. Wolf, <i>Microchip Manufacturing</i> (2004).

Exhibit 1026	Curriculum Vitae of Jack Lee, Ph.D
Exhibit 1027	MOSFET Scaling Presentation (2003)
Exhibit 1028	J. Steigerwald, <i>Chemical Mechanical Polish: The Enabling Technology</i> , 2008 IEEE International Electron Devices Meeting (2008)
Exhibit 1029	H. Wong et al., <i>Nanoscale CMOS</i> , IEEE, Vol. 87, No. 4, pp. 537-570 (1999)
Exhibit 1030	P. Zantye et al., <i>Chemical Mechanical Planarization for Microelectronics Applications</i> , Materials Science and Engineering R 45, pp. 89-220 (2004)
Exhibit 1031	Excerpts of S. Sze and K. Ng, <i>Physics of Semiconductor Devices (3d.)</i> (2007)

III. Relevant Legal Standards

20. I am an engineer by training and profession. The opinions I am expressing in this report involve the application of my knowledge and experience to the evaluation of certain prior art with respect to the '609 patent. My formal knowledge of patent law is no different than that of any lay person. Therefore, I have requested the attorneys from Jones Day, who represent TSMC, to provide me with guidance as to the applicable patent law in this matter. The paragraphs below express my understanding of how I must apply current principles related to patent validity to my analysis.

A. Claim Construction

21. I have been informed that that in determining whether a patent claim is obvious in view of the prior art, the Patent Office must apply the *Phillips* standard to construe the claim by giving the claim its plain and ordinary meaning as understood

by a POSITA at the time of the invention, in light of the specification and prosecution history.

22. For the '609 patent, I have been asked to consider the relevant time as just prior to June 9, 2013, the filing date of U.S. Patent No. 8,993,384, which is a parent to the '609 patent. For the purposes of this review, I have construed each claim term in accordance with its plain and ordinary meaning under the *Phillips* standard, unless otherwise indicated.

B. Obviousness

23. I have been informed that a claim is unpatentable under 35 U.S.C. § 103 if the claimed subject matter as a whole would have been obvious to a person of ordinary skill in the art at the time of the invention. As mentioned above with respect to claim construction, I have been asked to consider the relevant time as just prior to June 9, 2013, which is the filing date of U.S. Patent No. 8,993,384, a parent to the '609 patent. I understand that an obviousness analysis takes into account the scope and content of the prior art, the differences between the claimed subject matter and the prior art, and the level of ordinary skill in the art at the time of the invention.

24. In determining the scope and content of the prior art, it is my understanding that a reference is considered analogous prior art if it falls within the field of the inventor's endeavor. In addition, a reference is analogous prior art if it is reasonably pertinent to the particular problem with which the inventor was involved.

A reference is reasonably pertinent if it logically would have commended itself to an inventor's attention in considering his problem. If a reference relates to the same problem as the claimed invention, that supports use of the reference as prior art in an obviousness analysis.

25. To assess the differences between prior art and the claimed subject matter, it is my understanding that 35 U.S.C. § 103 requires the claimed invention to be considered as a whole. This "as a whole" assessment requires showing that one of ordinary skill in the art at the time of invention, confronted by the same problems as the inventor and with no knowledge of the claimed invention, would have selected the elements from the prior art and combined them in the claimed manner.

26. It is my further understanding that the Supreme Court has recognized several rationales for combining references or modifying a reference to show obviousness of claimed subject matter. Some of these rationales include:

- combining prior art elements according to known methods to yield predictable results;
- simple substitution of one known element for another to obtain predictable results;
- a predictable use of prior art elements according to their established functions; applying a known technique to a known device (method or product) ready for improvement to yield predictable results;

- choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success; and
- some teaching, suggestion, or motivation in the prior art that would have led one of ordinary skill in the art to modify the prior art reference or to combine prior art reference teachings to arrive at the claimed invention.

27. I have been told that a prior art reference may combined with one or more references and/or with the knowledge of a person of ordinary skill in the art to show obviousness. I have also been told that a person of ordinary skill in the is presumed to know all relevant prior art. I have also been told that the obviousness analysis may account for the inferences and creative steps that a person of ordinary skill in the art would have employed at the time of invention.

28. I understand that when combining prior art elements, the obviousness analysis requires determining whether a person of ordinary skill in the art would have had a “reasonable expectation of success” in arriving at the claimed invention by combining those elements. I have been told that a “reasonable expectation of success” does not require “absolute predictability.”

29. I have been told that the strongest rationale for combining references is a recognition, expressly or impliedly, in the prior art or drawn from a convincing line of reasoning based on established scientific principles or legal precedent, that some advantage or expected beneficial result would have been produced by their

combination. I have also been told that combining two embodiments disclosed adjacent to each other does not require a leap of inventiveness.

30. I have been told that, with respect to the obviousness of similar and overlapping ranges, where a claimed range overlaps or lies inside a range disclosed by the prior art, a prima facie case of obviousness exists. I have also been told that where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation. I have been told that obviousness in these cases may be rebut if the claimed range is critical or demonstrates new and unexpected results.

31. I have been told that a mere change in the timing or sequence of steps without any new or unexpected results is generally obvious.

IV. Person Of Ordinary Skill In The Art

32. It is my understanding that when interpreting the claims of the '609 Patent, I must do so based on the perspective of a POSITA as of the relevant priority date. My understanding is that the earliest claimed priority date of the '609 Patent is June 9, 2013.

33. In my opinion, a person of ordinary skill in the art for the '609 Patent would have been a person having at least a Master's degree in electrical engineering, physics, chemistry, materials science, or a related field, and three years of work experience in semiconductor manufacturing, such as, for example, in integrated circuit

device (or transistor) design and/or manufacturing, as of June 9, 2013. Additional relevant education could substitute for professional experience, and significant work experience or training could substitute for formal less education.

34. As described in detail above in the “Qualifications” section, my own training and experience exceeds that of one of ordinary skill in the art.

V. Background

A. Technology Background

35. The '609 patent relates to semiconductor devices. Semiconductor devices are generally manufactured on substrates that are employed as a building foundation and comprise billions of transistors.

36. Transistors are the fundamental building blocks for semiconductor chips. Each transistor operates as a switch that either allows or blocks the flow of electrical current. By combining thousands, or even billions of transistors together, circuit designers can implement electronic hardware like processors used in computers, mobile phones and other semiconductor devices.

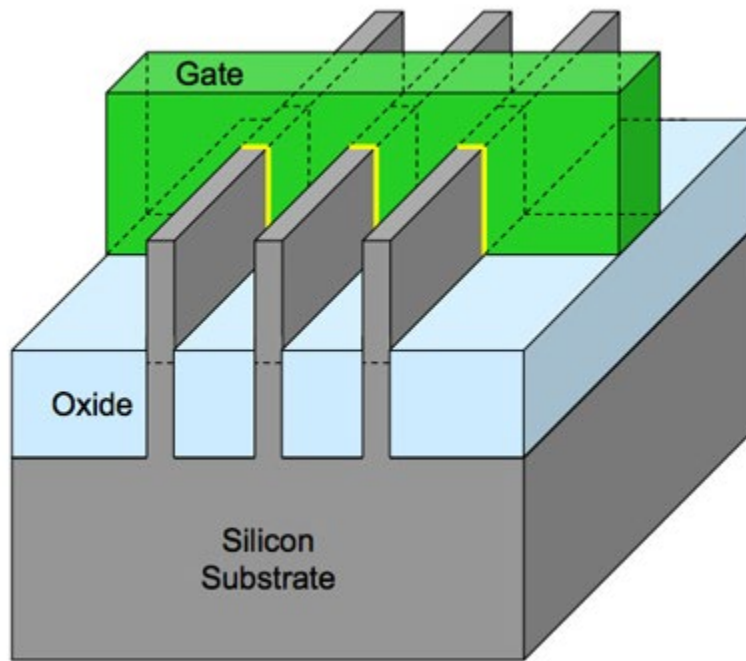
37. A typical transistor, known as a MOSFET (metal-oxide-semiconductor field-effect transistor) has three main components: a “source,” a “drain,” and a “gate.” When the transistor is “off,” no current flows between the source and drain. When a proper voltage is applied to the gate, the transistor is turned on, allowing current to flow through the “channel region” between the source and drain.

38. Transistors are classified as either “n-type” or “p-type.” In n-type MOSFET (or nMOS), current is carried by negatively charged electrons, and the source and drain regions doped with n-type impurities (e.g. arsenic or phosphorus), which contribute free electrons due to their higher valence electron count. In contrast, p-type MOSFET (or pMOS) conducts current via holes (positively charged carriers), and the source and drain regions are doped with p-type impurities (e.g., boron) which have fewer valence electrons and create a surplus of holes. In both cases, current flows through the channel when the transistor is in the on-state.

1. FinFETs

39. Around 1999, Chenming Hu, who later served as TSMC’s CTO, introduced a new type of transistor that he called “FinFETs.” *See* Exhibits 1013, 1014, 1015. FinFETs are so named because the transistor channel is formed in a thin vertical “fin” of silicon protruding from the substrate. The gate electrode wraps around multiple sides of this fin, typically the top and two sidewalls, offering improved electrostatic control over the channel compared to traditional planar MOSFETs. For this contribution, Dr. Hu was awarded the National Medal of Technology and Innovation for his invention of FinFETs.¹ A representative FinFET structure is shown below:

¹ *See* <https://www.chu.berkeley.edu/biography/>.



Ex. 1017 at 7. As shown above, the gate overlays multiple surfaces of the silicon fin, allowing for more effective control of the channel region between source and drain. FinFET transistors on the wafer are separated by dielectric materials, e.g. oxide, on the wafer. These devices are often referred to as tri-gate transistors, and later generations evolved into gate-all-around (GAA) structures, where the gate completely surrounds the channel. A POSITA would have understood “FinFET” to refer broadly to a class of non-planar transistors characterized by a raised semiconductor fin structure with tri-gate, double-gate, and gate-all-around configurations recognized as specific implementations with that broader FinFET architecture. The motivation for these non-planar geometries was to improve gate control over the channel, thereby reducing leakage current during the off-state. This translates into lower static

power dissipation and significantly enhanced battery life, making such transistors particularly attractive for mobile and low-power applications.

40. As described further below, by 2004, it was already known that transistor performance is improved by introducing strain into the transistor channel by using epitaxial techniques. For example, silicon germanium (or “SiGe”) was commonly used in the source and drain regions to induce compressive strain, particularly for pMOS devices, thereby improving carrier mobility and drive current. Ex. 1007 at 978-980 and Ex. 1019 at 247-250.

41. Thus, long before the priority date of the ’609 patent, FinFET transistors fabricated by forming fin structures, isolation structures, gate structures, and epitaxially formed source/drains were already well-known in the art. In fact, by 2013, the priority date of the ’609 patent, Intel had already commercialized FinFET-based products with this architecture. *See* Exs. 1016,² 1017,³ 1018.⁴ TSMC, likewise, had developed and held numerous patents on FinFET transistors featuring these same fabrication elements, as further discussed below in connection with the Xu and Lin prior art references.

² <https://www.nytimes.com/2011/05/05/science/05chip.html>.

³ https://download.intel.com/newsroom/kits/22nm/pdfs/22nm-Details_Presentation.pdf.

⁴ <https://web.archive.org/web/20110518133030/http://www.anandtech.com:80/print/4313/intel-announces-first-22nm-3d-trigate-transistors-shipping-in-2h-2011>.

2. Stressed/Strained Channels

42. The introduction of strained silicon channels in the early 2000s marked a major leap in CMOS technology by significantly enhancing carrier mobility. This innovation enabled higher transistor speeds and improved drive current without requiring aggressive reductions in gate length. A key technique for inducing strain involved recessing the source/drain (S/D) regions adjacent to the gate and then epitaxially regrowing them with lattice-mismatched materials. For example, silicon-germanium (SiGe) was widely adopted in pMOS transistors to apply compressive strain, while silicon carbon (SiC) or pure silicon was used in NMOS devices to induce tensile strain. *See* e.g., Ex. 1004 at 1:16-38; Ex. 1005 at ¶¶ [0002], [0035]. Strain engineering modifies the silicon crystal lattice in the channel region, which reduces carrier scattering and increases the speed at which electrons or holes can travel through the device, thereby lowering transistor delay and improving switching performance. *See* Ex. 1021 at 221-224.

43. This technique became mainstream in high-performance CMOS processes starting around the 90 nm node (~2003) and continues to be used in advanced nodes today. The process typically involves selective etching (i.e., recessing) of the S/D regions followed by selective epitaxial growth (SEG)—i.e., regrowing—using chemical vapor deposition (CVD), which deposits the desired stressor material only on exposed silicon surfaces. This induces localized stress in the

channel region without significantly altering the device geometry, and the substrate remains silicon throughout. Over time, this method became standard practice and is often combined with other strain-engineering techniques, such as stress liners and contact etch stop layers (CESLs). *See*, e.g. Ex. 1007 at 978-980. The combined effect led to substantial improvements in drive current, switching speed, and energy efficiency, supporting continued device scaling and increased integration density. These epitaxial strain techniques were specifically applied to FinFETs including in Exs. 1004, 1005, and 1006.

3. Replacement Metal Gates

44. The gate-first process was the standard approach in early CMOS technology, particularly through the 90 nm (~2003) and 65 nm (~2005) technology nodes. In this method, the gate electrode and dielectric are formed early, enabling self-aligned source and drain formation, which ensures precise alignment and helps minimize parasitic capacitance -- key to enhancing device performance. However, the gate-first approach became problematic with the introduction of high-K (high dielectric constant) materials and metal gates, which replaced traditional poly/SiO₂ stacks to address excessive gate leakage and degraded electrostatic control at smaller nodes.

45. By the 45 nm node (~2007) and beyond, it became clear that high-K/metal gate (HKMG) stacks are thermally sensitive, particularly to the junction

activation anneals and SiGe source/drain regrowth processes used to form low-resistance, strain-enhanced regions. These high-temperature steps can degrade the high-K dielectric and alter the metal gate's work function, leading to threshold voltage instability and reduced device reliability. To overcome this, the industry adopted the *gate-last*, or replacement metal gate (RMG), process. *See* e.g., Ex. 1004 at 4:13-17. In this approach, a sacrificial polysilicon "dummy" gate is patterned early to preserve self-alignment, while the final high-K dielectric and metal gate stack are introduced after all high-temperature processing is complete. *See* Ex. 1022; Ex. 1023.

46. The gate-last process typically involves depositing the dummy gate, forming sidewall spacers, creating source/drain regions through implantation and activation annealing — or by recessing and regrowing embedded S/D stressors — and then removing the dummy gate to expose the channel. A conformal high-K dielectric (e.g., HfO₂) and a metal gate stack are then deposited into the resulting trench. This method offers two major advantages: (1) enhanced work function tunability, since metals optimized for nMOS and pMOS can be selected post-anneal; and (2) preservation of gate stack integrity, as sensitive materials are never exposed to damaging thermal steps. Even at the most advanced nodes today, the gate-last process remains the industry standard for high-performance 3D nanoscale integrated-circuit devices.

4. Etch Processes And Depth Control

47. In advanced semiconductor fabrication, particularly in FinFET processing, precise etching techniques are essential for defining the geometry and depth of structures such as fins, trenches, and recesses for source/drain formation. Anisotropic dry etching techniques, such as reactive ion etching (RIE), allow for directional control and vertical sidewalls, while wet etching methods, though generally isotropic, are useful for certain selective removal steps. These etching processes can be tuned by adjusting gas chemistry, pressure, bias power, and time, enabling precise control over the depth and profile of etched features (Ex. 1025 at Ch. 21–22).

48. Etch depth control is typically achieved through techniques such as end-point detection, interferometry, or calibrated timed etching, allowing nanometer-scale precision. In FinFET process flows, it is common to partially recess isolation structures (such as shallow trench isolation, or STI) or fin structures to form three-dimensional profiles that support subsequent epitaxial growth, gate wrapping, or stress engineering. For example, a timed RIE step can be used to recess STI oxide to a depth that exposes the fin sidewalls for epitaxial growth or creates a height difference between the STI and the fin top. Similarly, the fin itself can be recessed using an etch chemistry selective to silicon, with a hardmask or spacer defining the lateral boundaries (*see* Ex. 1025 at pp. 383-388; 400-408).

49. Different etch chemistries and process steps can be selectively applied to silicon and dielectric materials to achieve vertical height differentials between adjacent regions. These techniques are commonly employed to facilitate void-free epitaxial growth, improve stress transfer into the channel, and enhance gate wrap coverage in FinFET structures.

B. The '609 Patent

50. The '609 patent is titled "Semiconductor Device with Epitaxial Structure." It describes FinFET transistors comprising "a fin structure, an isolation structure, a gate structure and an epitaxial structure." Ex. 1001 at Abst. The main feature of the '609 patent concerns the high-level structure of a FinFET.

51. Figures 1 through 3 of the '609 patent depict the fabrication of a conventional FinFET device, which was known by the priority date. As shown in Figure 3, the FinFET comprises a "a plurality of fin structures 12" (light blue), a "gate structure 30" (gold) formed over the fins, and "a spacer 40" (dark blue) formed "on the sidewalls of the gate structure 30." Ex. 1001 at 3:11-13, 4:62-66. Figure 3 also depicts "isolation structure 20" (magenta) formed on the substrate." *Id.* at 3:51-52.

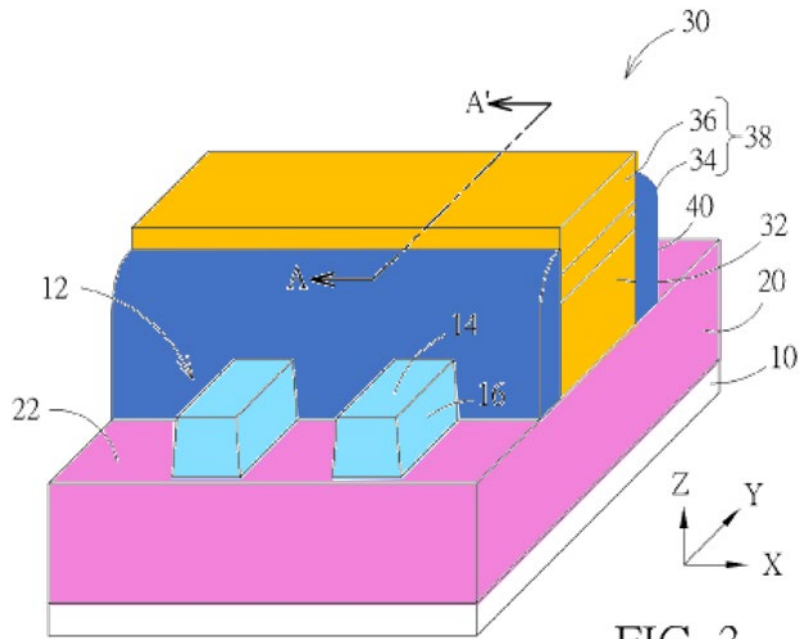


FIG. 3

52. Subsequently, “a first etching process 42, such as a wet etching or a dry etching process, may be carried out to selectively remove” the exposed portions of “isolation structure 20,” resulting in the structure shown in Figure 5. *Id.* at 5:17-28. As a result, “[t]here is a height difference H2 between the first top surface 22a [red] and the second top surface 22b [green]” of the isolation structure 20 (magenta) also depicted as a first depth “D1” in Figure 5. *Id.* at 5:22-39. References numbers 22a and 22b are depicted in Fig. 6 of the ’609 patent. *Id.* at Fig. 6.

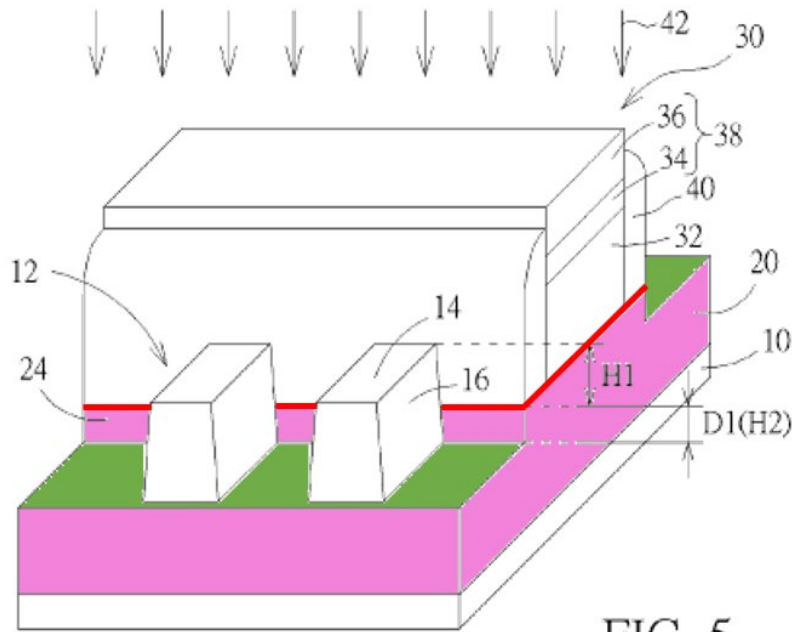


FIG. 5

53. Next, the fin structures are etched and “a recess 60 may be formed in each fin structure 12.” *Id.* at 5:47-51. An “epitaxial growth process” is then “carried out in order to grow an epitaxial structure 6[6] [*sic.*] in each corresponding recess 60.” *Id.* at 6:34-41. The recess is shown below in light blue (Figure 6) and the epitaxial structures are shown below in purple (Figure 9).

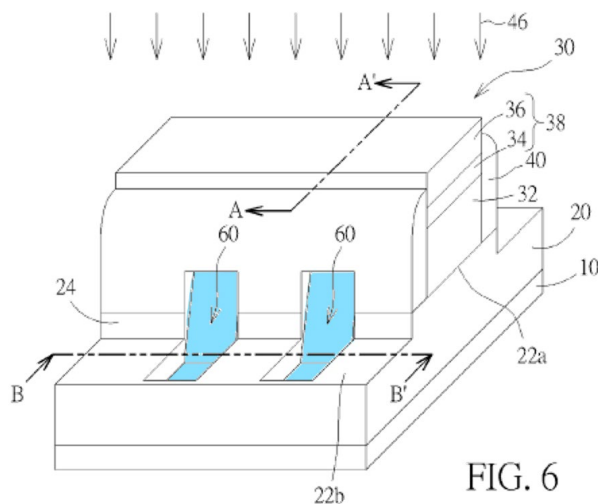


FIG. 6

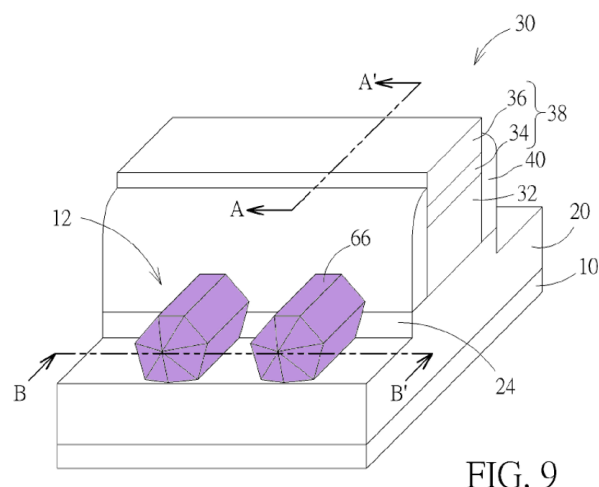
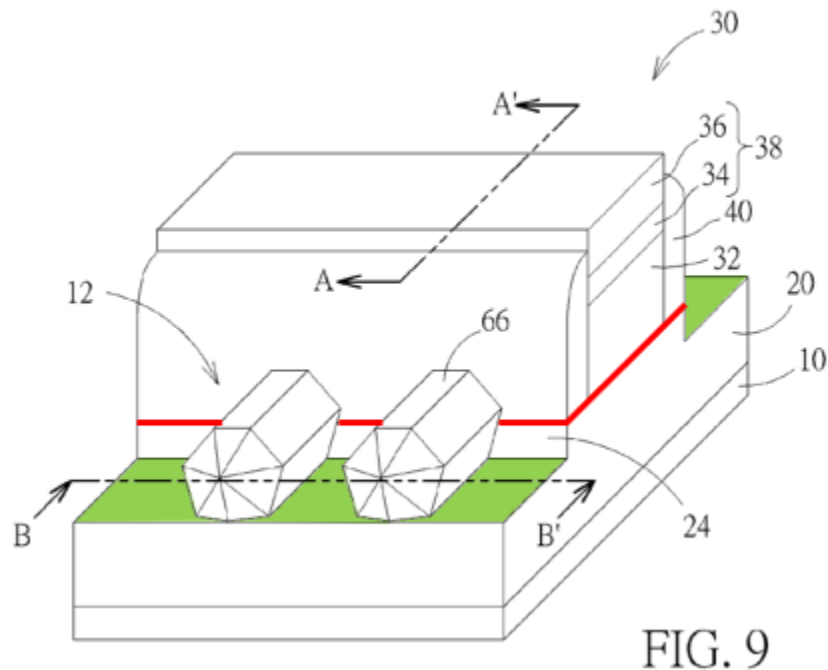


FIG. 9

54. The '609 patent tries to distinguish itself from the prior art by teaching that its “isolation structure” that “surrounds the fin structure” has a “first top surface” under the gate structure and a “second top surface” at the sides of the gate structure. *Id.* at Abst. According to the '609 patent, the “first top surface” (red, under the gate) is “higher” than the “second top surface” (green, on sides of the gate). *Id.* at Abst. This is shown in figure 9 of the '609 patent as annotated below, which depicts the completed FinFET.



C. Prosecution History

55. The Challenged Claims were allowed after one non-final rejection. Specifically, the Examiner rejected the pending claims based on U.S. Patent App. Pub. No. 2012/0193713 (“Kulkarni”). Ex. 1002 at 38. In response, the Applicant amended pending claim 1 (the only independent claim) to recite “an isolation structure,

disposed on the surface of the substrate and surrounding the fin structure.” *Id.* at 25.

The claims were subsequently allowed. *Id.* at 7. Notably, the Applicant conceded that the claims without the added limitation “disposed on the surface of the substrate” “may not sufficiently distinguish” the claimed structure from Kulkarni—effectively conceding that all other elements of the issued claims were already known in the art. *Id.* at 31.

VI. Overview Of The Prior Art

A. Overview of Xu

56. Xu was filed on November 2, 2010 by TSMC. *See* Ex. 1004. Xu qualifies as analogous art because it is in the same field (FinFET technology) and is reasonably pertinent to a problem the ’609 patent purports to address, namely, the structure and fabrication of FinFET devices. *See* Ex. 1001 at Abstr., 3:40-55; Ex. 1004 at Abstr. Xu describes “a FinFET device and method for fabricating a FinFET device.” *Id.* at Abst. “Figs. 2-6 provide various perspective views of a FinFET device 100, in portion or entirety, at various stages of fabrication according to the method 10 of FIG. 1.” *Id.* at 2:51-53. “The term FinFET device refers to any fin-based transistor.” *Id.* at 2:53-55.

57. Figure 2 of Xu depicts a “fin structure 115A and 115B [blue] that extends from the substrate 110.” *Id.* at 3:9-10. Figure 2 also shows “[i]solation features 130” that can be a “shallow trench isolation (STI) structure” (magenta) that “surround the

fin structure 115A and 115B.” *Id.* at 3:54-58. The FinFET device also includes a “gate structure 150” (gold). *Id.* at 3:66-4:3.

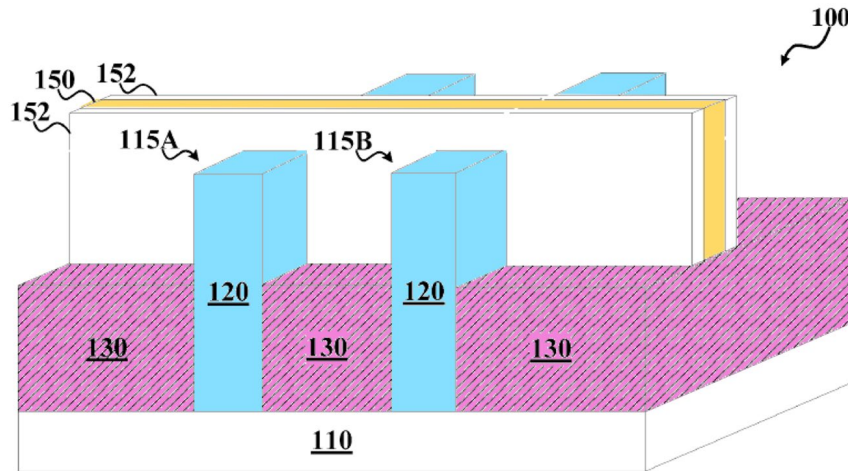


FIG. 2

58. After forming the gate structure, as shown in Figure 3, “a process is performed to recess the isolation features 130” using an “etching process.” *Id.* at 4:54-56. The “etching process selectively etches the isolation features 130.” *Id.* at 4:58-61. The process creates a height difference (or depth) between a top surface (red) under the gate and a top surface to the sides of the gate as shown below (green):

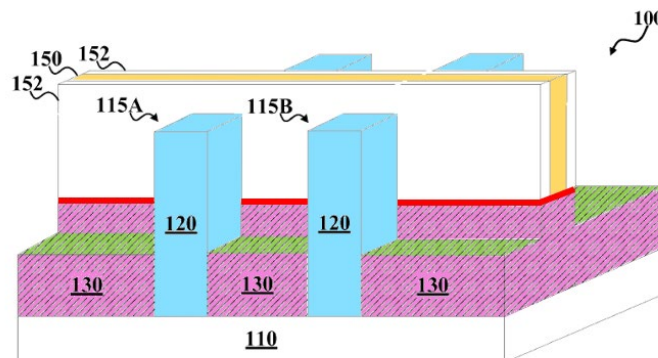


FIG. 3

59. Next, as shown in Figure 4, a “fin template 135” (purple) is formed to “merg[e] the fins 120 together” by “epitaxially (epi) growing a semiconductor material on exposed portions of the fins 120 in the source and drain regions of the fin structure 115A and 115B.” Ex. 1004 at 5:1-15.

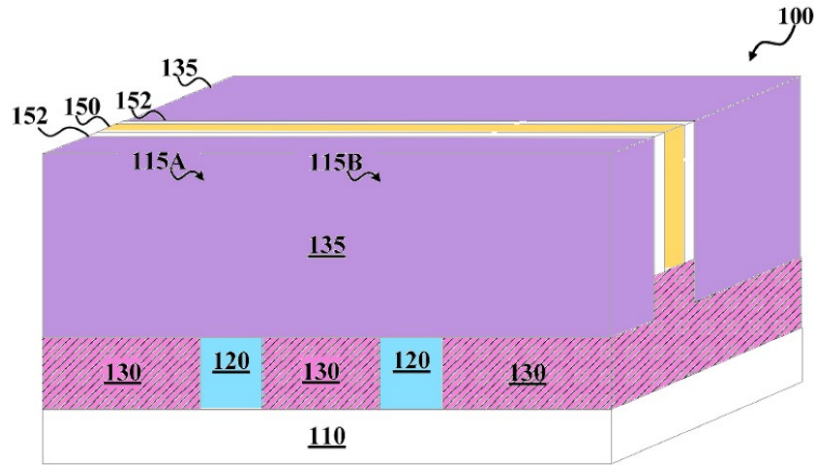


FIG. 4

60. The resulting fin template 135 (purple) and fins 120 (blue) are recessed in Figure 5 and, as shown in Figure 6, another “semiconductor material 160 [(checkered purple)] is epitaxially grown over the fin template 135,” which “generates channel strain.” *Id.* at 5:34-35, 5:49-55.

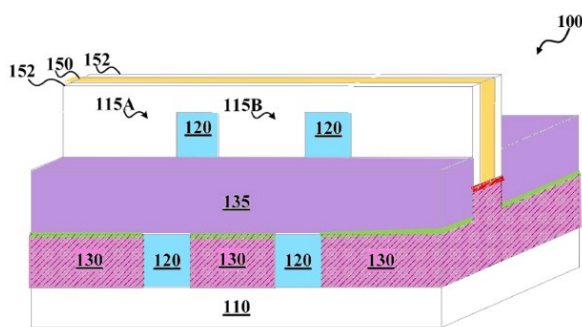


FIG. 5

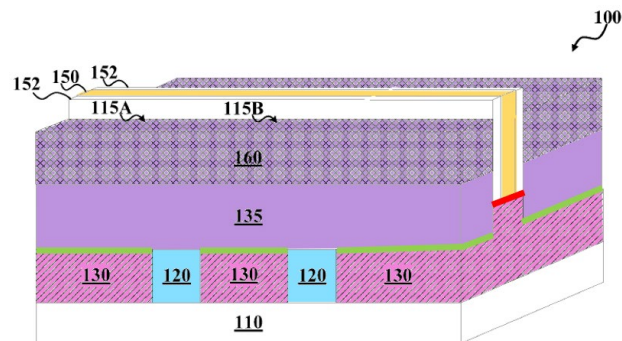


FIG. 6

61. Xu teaches that “[t]he semiconductor material 160 may be referred to as raised source and drain features of the source and drain regions of the fin structure 115A and 115B,” and that the “fin template 135 in the source and drain regions of the fin structures 115A and 115B may also be considered as part of the raised source and drain features.” *Id.* at 6:2-7. Notably, like the ’609 patent, Xu discloses a fin structure, an isolation structure, a gate structure, and an epitaxial structure, where the isolation structure has a first top surface that is higher than a second top surface.

62. Xu also discloses a second embodiment where “an etching process” removes portions “of the fin structures 215A and 215B,” resulting in recessed fins, as shown below. *Id.* at 7:58-61, 10:34-36; Fig. 7 (“[c]ompletely remove the second material portion [230] from the source and drain regions of the first and second fin structure”).

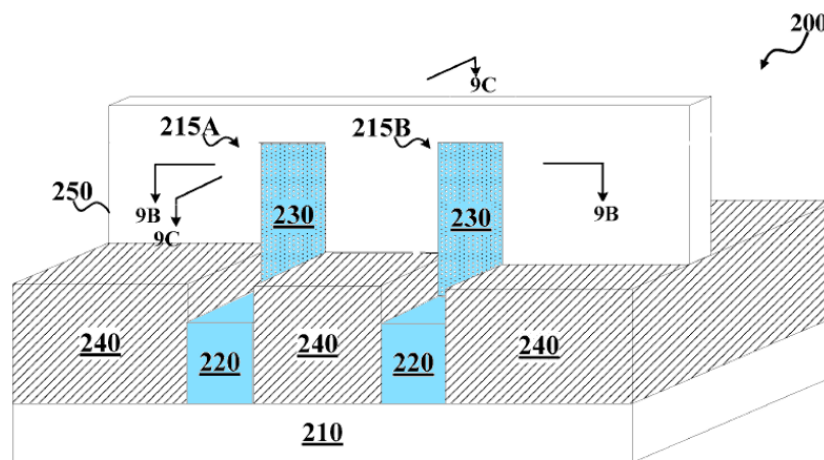


FIG. 9A

63. After that, the epitaxial materials (*i.e.*, the “fin template”) “may be formed by a process similar to that described above with reference to FIG. 5” (*i.e.*, the first embodiment discussed above) to fill the recesses. *Id.* at 11:2-4. Xu contemplates that a fabrication method can include both etching the isolation structure as well as recessing the fin structure. *See, e.g., id.* at 16:5-17:10 and claim 19

B. Overview of Ching

64. Ching was filed on November 9, 2012 by TSMC. Ex. 1005. Ching qualifies as analogous art because it is in the same field (FinFET technology) and is reasonably pertinent to a problem the ’609 patent purports to address, namely, the structure and fabrication of FinFET devices. *See* Ex. 1001 at Abstr., 3:40-55; Ex. 1005 at Abstr. Ching describes a “Fin Field-Effect Transistor (FinFET) and the methods of forming the same.” *Id.* at 1:53-55. “FIGS. 1 through 9D are cross-sectional views and perspective views of intermediate stages in the manufacturing of a FinFET in accordance with some exemplary embodiments.” *Id.* at 1:60-62.

65. Figure 1 shows an “initial structure” with a “substrate 20.” *Id.* at 1:63-67. Figure 1 also depicts “[i]solation regions such as Shallow Trench Isolation (STI) regions 22” (magenta) on the surface of substrate 20, as well as a “semiconductor strip 21” (light blue) protruding from the surface of the substrate which may be “the same material of substrate 20.” *Id.* at 2:1-13.

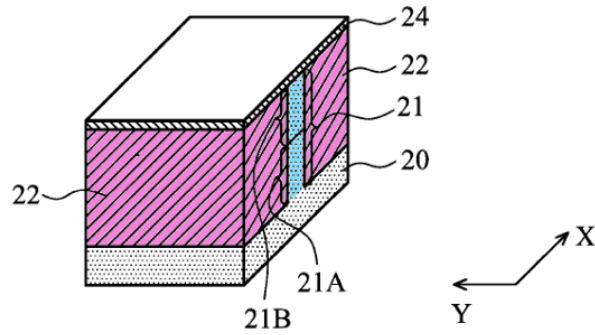


Fig. 1

66. Figure 2 shows that a “polysilicon layer 26” and “[h]ard mask layer 28” are then deposited over the “semiconductor strip.” *Id.* at 2:35-39.

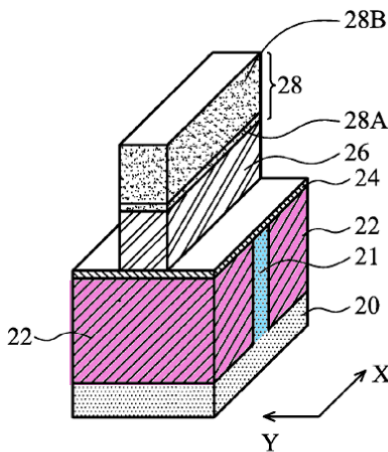


Fig. 2

67. Subsequently, as shown in Figure 3, “[a] first STI recessing may be performed” and “top surfaces 22A [green] of STI regions 22 are also recessed from the original top surface 22A’ [red line] of STI regions.” *Id.* at 2:59-67. “[G]ate spacers 30” (dark blue) are also formed as shown in Figure 3. *Id.* at 3:9-12.

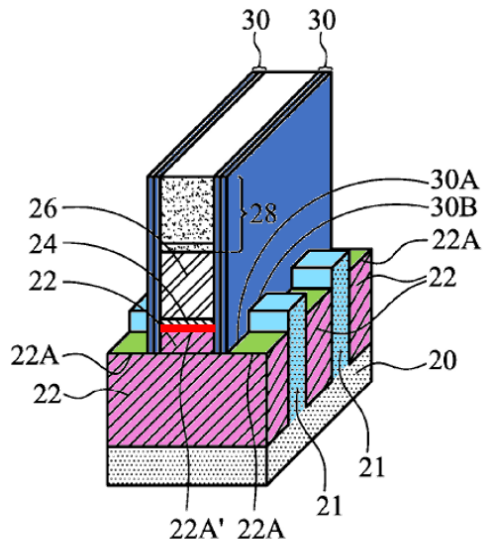


Fig. 3

68. Next, “exposed portions of semiconductor strip 21 [light blue] are recessed” (Figure 4) and “epitaxy regions 36” (purple) are formed “from recesses 32” (Figure 5). *Id.* at 3:20-22.

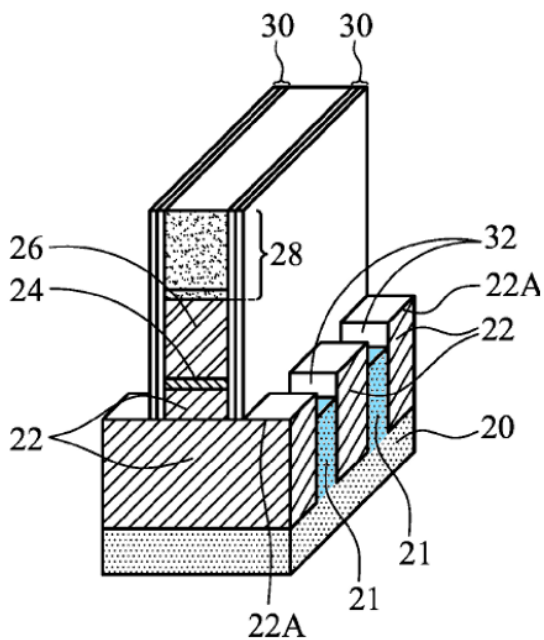


Fig. 4

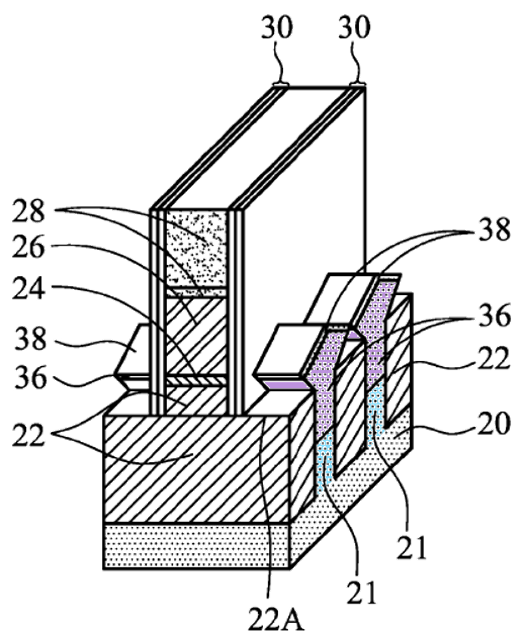


Fig. 5

69. Figure 8E illustrates a cross-sectional view of a device according to Ching at a later stage of fabrication. *Id.* at 4:22-25. Ching discloses that “top surfaces 22B [red line] are higher than top surfaces of 22A [green lines] of STI regions 22 [magenta].” *Id.* at 4:29-31. Further, “[i]n Fig. 8E, portions 22’ of STI regions 22 [magenta] are located between opposite gate spacers 30 [dark blue], and the sidewalls of portions 22’ are in contact with the sidewalls of gate spacers 30.” *Id.* at 4:31-34.

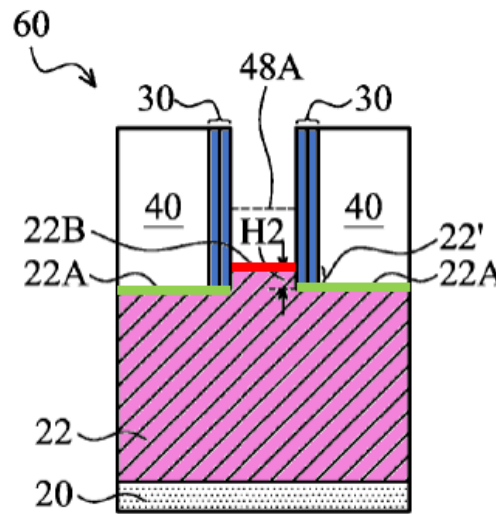


Fig. 8E

70. To complete formation of a FinFET, a “gate dielectric layer 50 and gate electrode 52” is formed. *Id.* at 4:39-40. Cross sectional views following this step are shown in modified Figures 9A and 9D below.

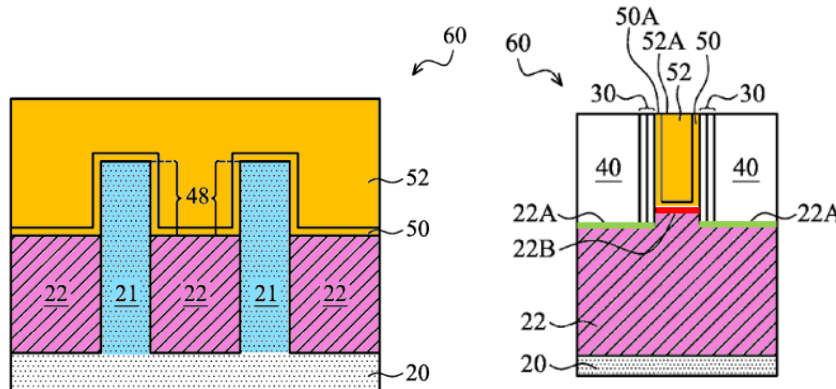


Fig. 9A

Fig. 9D

71. Ching concludes that “[i]t is observed that in the resulting FinFET 60, the portions of STI regions 22 that are on the opposite sides of a same gate electrode 52 (FIGS.9B, 9C, and 9D) have top surfaces 22A that are either higher than, level with, or lower than, top surface 22B that are underlying (and aligned to) gate electrode 52.” Ex. 1005 at 5:26-31.

C. Overview of Huang

72. Huang, filed on November 29, 2012 by TSMC, is a prior art under 102 and qualifies as analogous art to the ‘609 patent *See* Ex. 1006. Huang lies in the same technical field of FinFET technology and addresses problems directly relevant to those faced by the ‘609 patent, such as the formation and integration of FinFET structures. *See* Ex. 1001 at Abstr., 3:40-55; Ex. 1006 at Abstr. Huang expressly describes “a FinFET device and methods of forming a FinFET device.” *Id.* at Abst.

In particular, “FIGS 2A through 5B illustrate” various “stages in the manufacture of Fin-Last FinFET device.” *Id.* at 2:20-22.

73. Huang discloses forming “semiconductor strips 24 ... by patterning the semiconductor substrate 20.” *Id.* at 2:45-46. It explains that “the semiconductor substrate is etched to a specific depth, meaning the semiconductor strips 24 are formed to a height, the semiconductor strips may have a height from about 10 nm to about 500 nm.” *Id.* at 2:56-59. Huang further teaches that a “dielectric layer 22 may [be] blanket deposited on the FinFet device 100.” *Id.* at 3:7-8. Following deposition, “the dielectric layer 22 may be planarized” and this planarization process “may continue until the tops of the semiconductor strips 24 are exposed.” *Id.* at 3:17-27. As shown in modified Fig. 2B below, the resultant structure includes semiconductor strips (blue) positioned between dielectric regions (magenta):

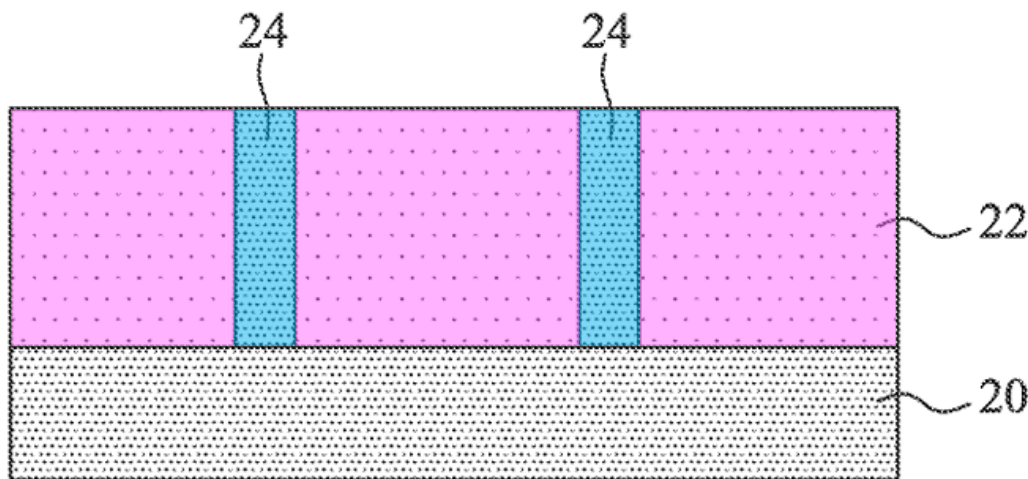


Fig. 2B

74. Next, Huang discloses “etching portions of the semiconductor strips 24 in a strained source drain (SSD) etch step to form recesses 26 in the semiconductor strips 24.” *Id.* at 4:10-12. The etch depth for these recesses may be “from about 5 nm to about 25 nm.” *Id.* at 4:15-16. This operation results in a structure, illustrated in modified Fig. 3B below, where recessed semiconductor strips (blue) remain between dielectric regions (magenta).

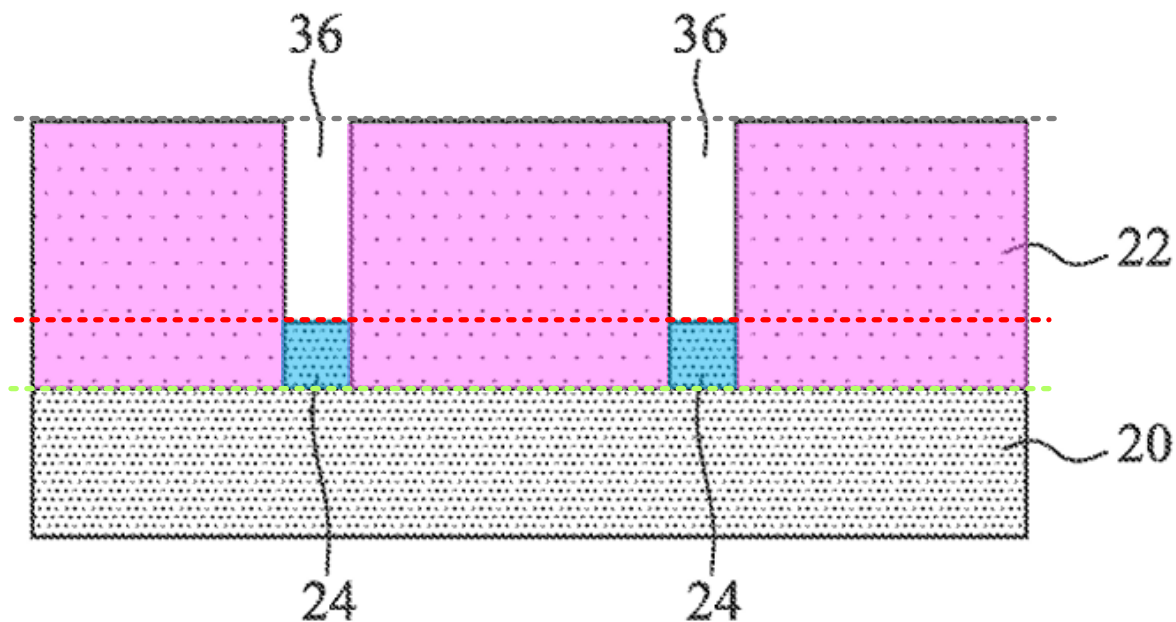


Fig. 3B

75. In Fig. 3B, the silver dashed line denotes the original height of the semiconductor strips, the red dashed line indicates the height after etching, and the green dashed line represents the bottom surface of both the dielectric regions and

semiconductor strips. Thus, the remaining fin height equals to the original fin height (H) minus the recess depth (D).

76. “After the recesses 36 are formed, the source 30 and drain regions 28 may be formed ... by epitaxially growing SiGe, Si, SiP, combinations thereof, or the like in the recesses 36.” *Id.* at 4:30-34. The resultant structure, shown in modified Fig. 4B, below, includes epitaxial structure (gold) grown atop the recessed semiconductor strips (blue), which remain surrounded by dielectric (magenta).

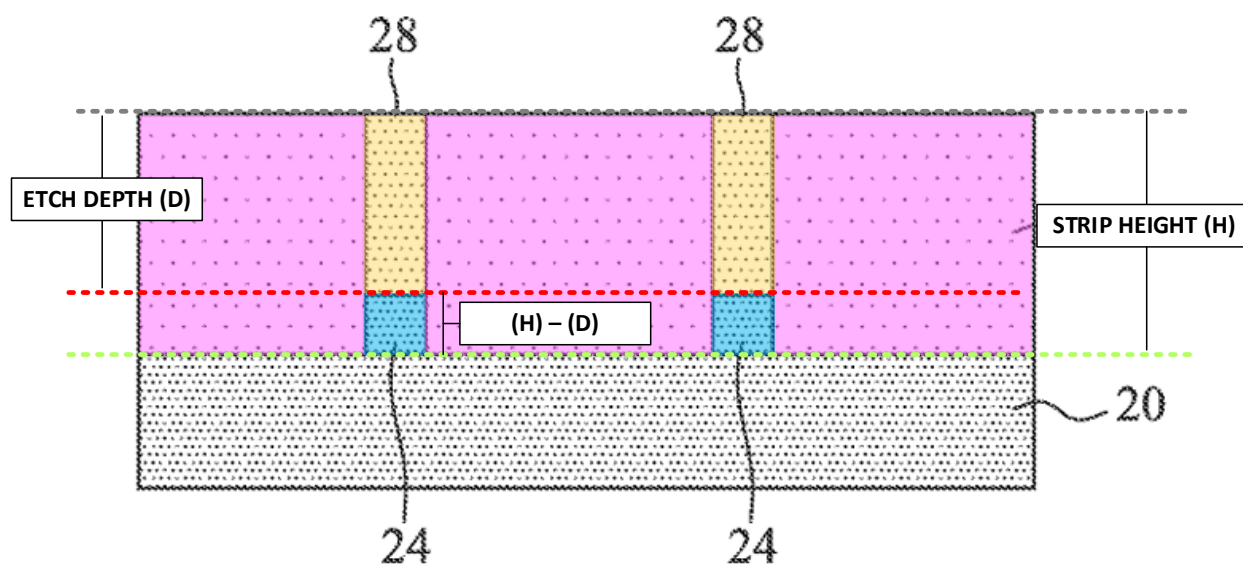
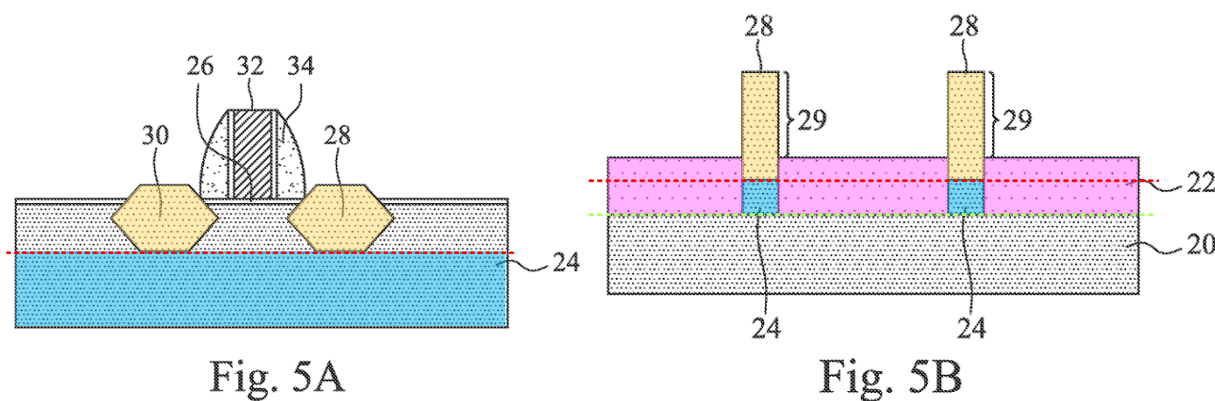


Fig. 4B

77. The bottom surface of the epitaxial structure (gold) aligns with the top of the recessed fins (red line). Thus, the vertical offset between this red line and the dielectric base (green line) corresponds to the difference $H - D$, where H is between 10–500 nm (*id.* at 2:59) and D is “between from about 10 nm to about 500 nm” (*id.* at

78. Once the epitaxial region is formed, Huang teaches forming fins 29 by “etching or recessing the dielectric layer 22 surrounding the semiconductor strips 24.” *Id.* at 4:62-64. The resulting fin structures are shown in modified Figs. 5A and 5B below, which illustrate the epitaxial source/drain atop a protruding fin body extending above the dielectric surface.



VII. Ground 1A: Claims 1-6 and 8-10 Are Anticipated And/Or Obvious Over Xu

79. In my opinion, claims 1-6 and 8-10 of the '609 Patent would have been obvious to a POSITA over the teachings of Xu in light of the knowledge of a POSITA.

A. Claim 1

1. 1[pre]: A semiconductor device, comprising:

80. Xu discloses and renders obvious a semiconductor device. For example, Xu discloses “[a] FinFET device and method for fabricating a FinFET device,” which

is a semiconductor device. *See, e.g.*, Ex. 1004 at Abst.; *id.* at 2:51-53 (“FIGS. 2-6 provide various perspective views of a FinFET device 100, in portion or entirety, at various stages of fabrication according to the method 10 of FIG.1.”).

2. 1[a]: a fin structure, protruding from a surface of a substrate, wherein the fin structure comprises a top surface and two side surfaces;

81. Xu discloses and renders obvious this limitation. For example, Xu discloses that “FinFET device 100 includes fin structure 115A and 115B that extend from the substrate 110.” Ex. 1004 at 3:9-10. The “fin structures 115A and 115B include fins 120.” *Id.* at 3:10-12. The “fins 120” are shown in Figure 3 (light blue) and comprise a top surface and two side surfaces. *Id.* at 2:63-3:8.

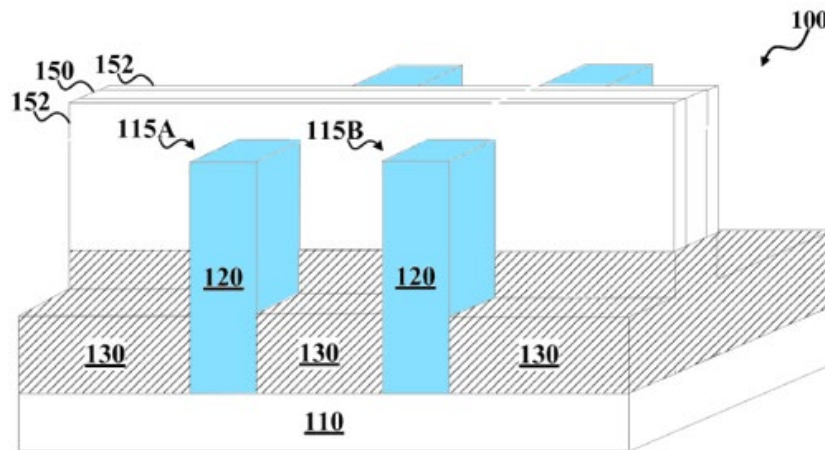


FIG. 3

82. The complete structure of the embodiment depicted by Figures 2 to 6 includes the “fins 120” (light blue) as shown in Figure 6 of Xu. *Id.* at Fig. 6 (note that

fins 120 retain their full original height in the section under the gate (not shown in Fig. 6)).

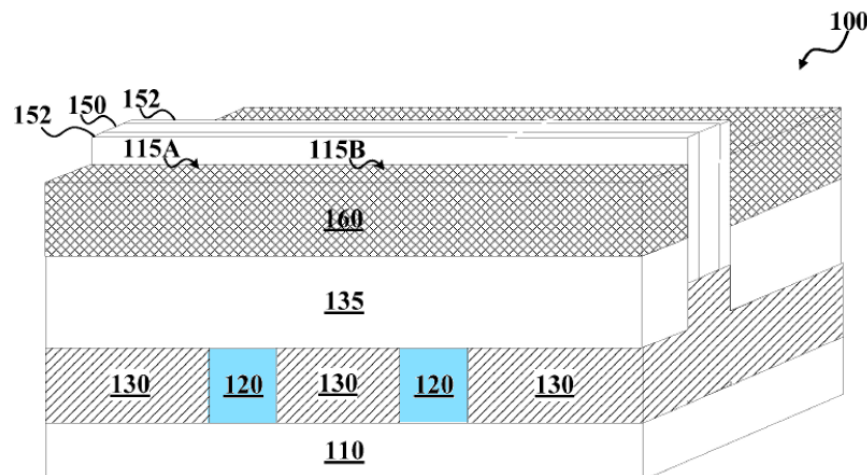


FIG. 6

3. 1[b]: an isolation structure, disposed on the surface of the substrate and surrounding the fin structure;

83. Xu discloses and renders obvious this limitation. For example, Xu discloses that “[i]solation features 130, such as shallow trench isolation (STI) structures, **surround the fin structures 115A and 115B** (in the depicted embodiment, the fins 120).” Ex. 1004 at 3:54-58. As shown in Fig. 3, the “isolation features 130” (magenta) are disposed on the surface of “substrate 110” and surround the fins 120 (light blue). *Id.* at 2:63-3:8

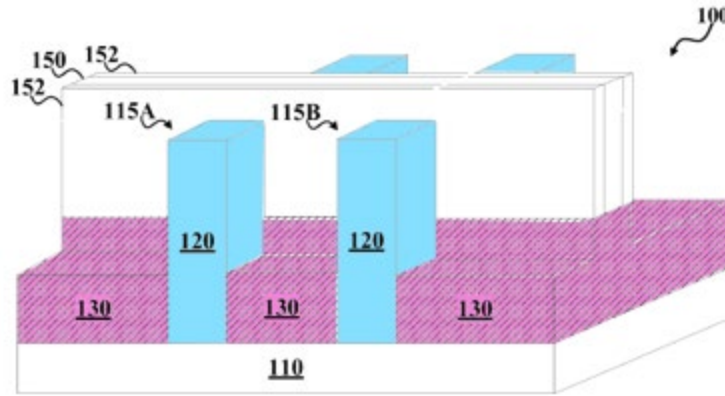


FIG. 3

84. The complete structure of the embodiment depicted by Figures 2 to 6 includes “isolation features 130” (magenta) as shown in Figure 6. *Id.* at Fig. 6.

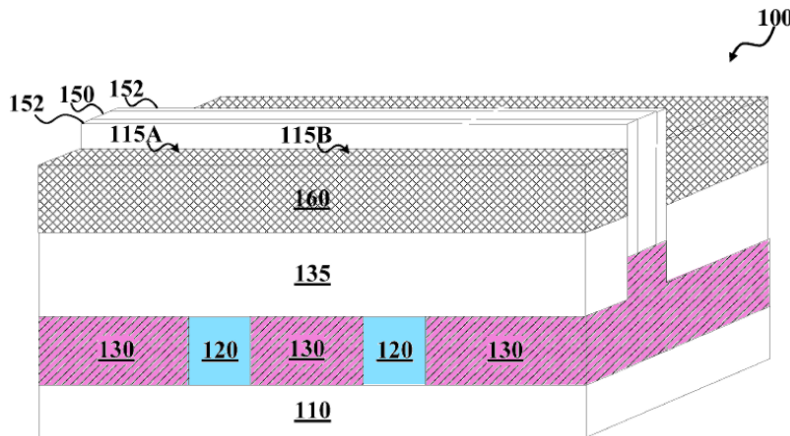


FIG. 6

4. **1[c(i)]: a gate structure, overlaying the top surface and the two side surfaces of a portion of the fin structure and covering a portion of the isolation structure;**

85. Xu discloses and renders obvious this limitation. For example, Xu discloses “a gate structure 150” that “traverses the fins 120, and in the depicted embodiment, is formed on a central portion of the fins 120.” Ex. 1004 at 3:66-4:1. As

shown in Figure 3, the “gate structure 150” (gold) overlays the top surface and two side surfaces of the “central portion of the fins 120” (light blue) and also covers a portion of the isolation structure 130 (magenta). *Id.*

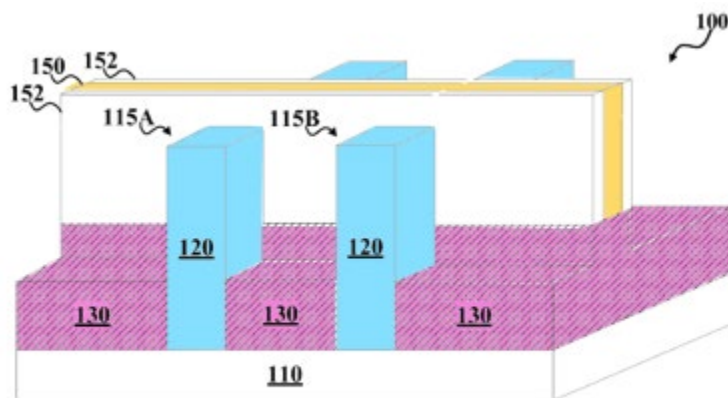


FIG. 3

86. The complete structure of the embodiment depicted by Figures 2 to 6 includes “gate structure 150” (gold) as shown in Figure 6. And, Figure 5, which shows the structure immediately preceding Figure 6, shows that the gate structure (gold) overlays the top surface and two side surfaces of a portion of the fins 120 (light blue), and also covers a portion of the isolation structure 130 (magenta). Ex. 1004 at Fig 5, Fig. 6.

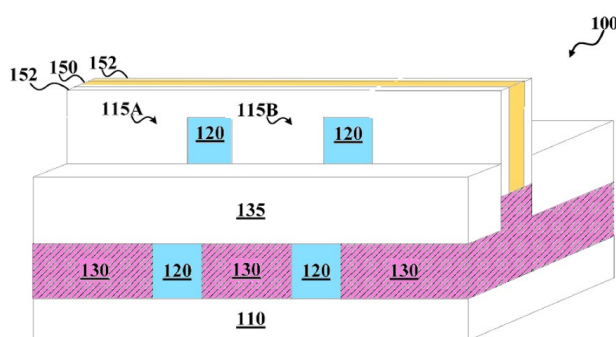


FIG. 5

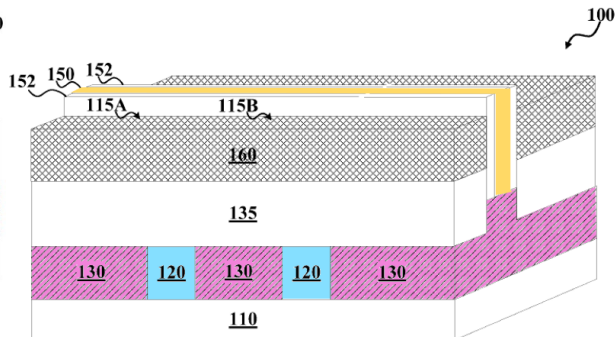


FIG. 6

5. 1[c(ii)]: wherein the isolation structure under the gate structure has a first top surface and the isolation structure at two sides of the gate structure has a second top surface, and the first top surface is higher than the second top surface; and

87. Xu discloses and renders obvious this limitation. For example, Xu discloses that “a process is performed to recess the isolation features 130” using an “etching process.” Ex. 1004 at 4:54-56. The “etching process selectively etches the isolation features 130” and “avoid[s] etching the silicon nitride spacers 152.” *Id.* at 4:58-61.

88. As shown in Fig. 3, this results in the “isolation features 130” (magenta) under the “gate structure 150” (gold) having a first top surface (red) and the “isolation features 130” (magenta) at the two sides of the “gate structure 150” (gold) having a “second top surface” (green). The first top surface (red) is higher than the second top surface (green).

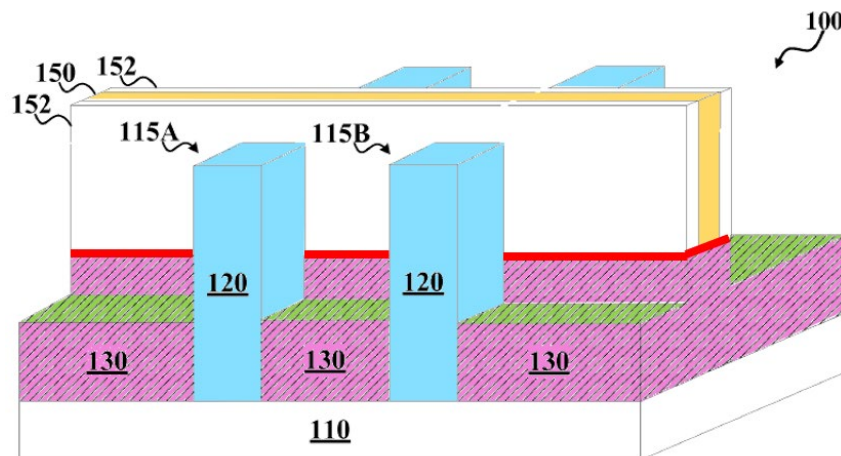


FIG. 3

89. The complete structure of the embodiment depicted by Figures 2 to 6 includes “isolation structure 130” (magenta) with the first and second top surfaces, where the first top surface (red line) is higher than the second top surface (green line) as shown in Figure 6.

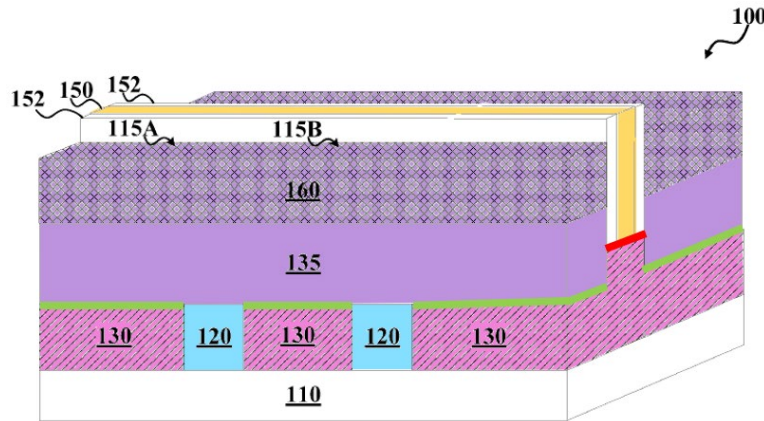


FIG. 6

6. 1[d]: an epitaxial layer, disposed at one side of the gate structure and in direct contact with the fin structure.

90. Xu discloses and renders obvious this limitation. As discussed below, the fin template 135 and the semiconductor material 160, both individually and together as a combined structure, meet limitation 1[d].

91. For example, Xu discloses a “fin template 135” is formed by “epitaxially (epi) growing a semiconductor material **on exposed portions of the fins 120** in the source and drain regions of the fin structure 115A and 115B.” Ex. 1004 at 5:1-15. The “fin template 135” is thus an epitaxial layer disposed at one side of the gate structure because the “source and drain regions” are located on either side of the “gate

structure 150.” As shown below, the “fin template 135” is also in direct contact with the “fins 120” (light blue). Ex. 1004 at Fig. 5.

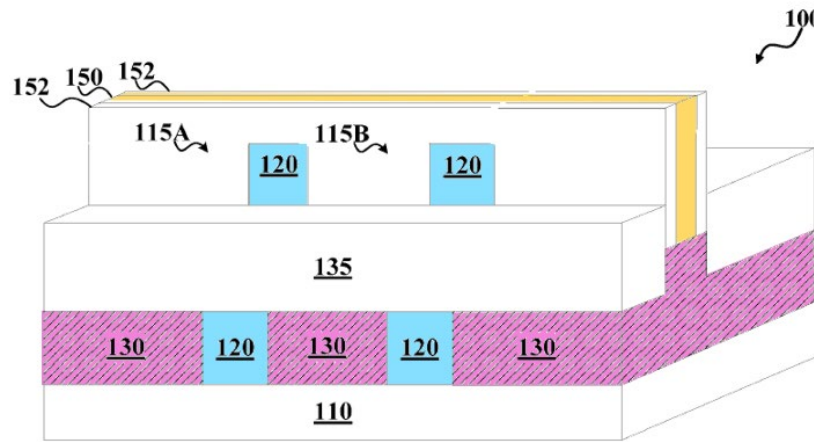


FIG. 5

92. As another example, Xu discloses that “a process is performed to recess the fin template 135” and “a semiconductor material 160 is epitaxially grown over the fin template 135.” *Id.* at 5:34-35, 5:49-50. The “semiconductor material is epi grown on the exposed fin template 135 **in the source and drain regions** of the fin structures 115A and 115B.” *Id.* at 5:50-55. Thus, “semiconductor material 160” is an “epitaxial layer” that is disposed at one side of the gate structure because the “source and drain regions” are located on either side of the “gate structure 150.” Further, portions of “fin structures 115A and 115B” are exposed prior to the formation of “semiconductor material 160 ... over the fin template 135” as shown in Figure 5 above. Ex. 1004 at Fig. 5. When “semiconductor material 160” is formed as shown in Figure 6, it will

therefore be in “direct contact with fin structure” 120 (light blue) as shown in Figure 6 below. *Id.* at Fig. 6.

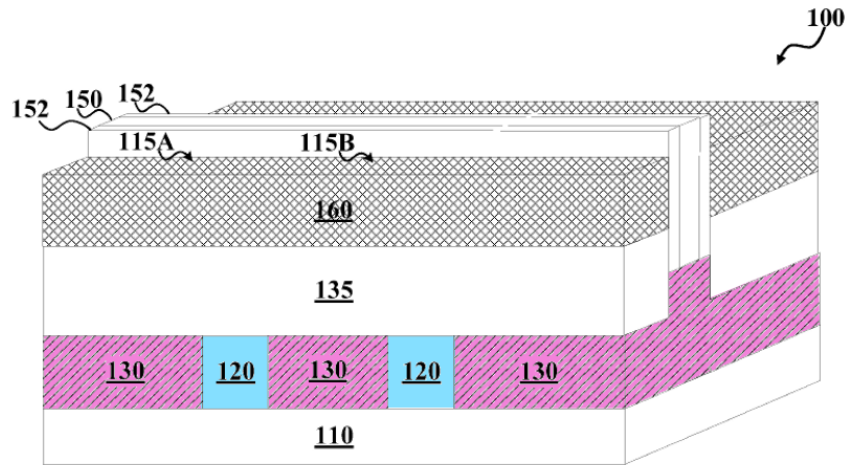


FIG. 6

93. Moreover, Xu teaches that the “epi grown semiconductor material 160 generates channel strain for the fin structures 115A and 115B.” Ex. 1004 at 5:50-55. This material 160 forms “raised source and drain features” that “can effectively introduce strain into the channels of the fin structures 115A and 115B.” Ex. 1004 at 5:45-48. A POSITA would have understood and found obvious that to accomplish this goal, the “semiconductor material 160” directly contacts the fins in order to physically expand or compress the crystal lattice of the channel and introduce strain.

94. In particular, a POSITA would have understood that channel strain is generated by using a semiconductor material in the source/drain regions that has a different lattice spacing than the material of the channel in between the source/drain regions. As is done in Xu, a common technique for introducing strain that was known

before 2013 is to recess the source/drain regions adjacent to the gate of a transistor and to then regrow the source/drain regions with lattice-mismatched materials. For example, a POSITA would have known that silicon germanium (SiGe) was widely adopted to apply compressive strain in pMOS devices, while silicon Carbon (SiC) was used to induce tensile strain in nMOS devices. *See, e.g.*, Ex. 1004 at 1:16-38. This structural difference alters the silicon crystal lattice in the channel region which reduces carrier scattering, thereby increasing carrier mobility. *See* Ex. 1021 at 221-224. Improved carrier mobility, in turn, lowers transistor delay and improves switching performance of the device. *Id.* A POSITA therefore would have understood and found obvious that to “effectively introduce strain into the channels of the fin structures 115A and 115B” (Ex. 1004 at 5:45-48), epi grown semiconductor material 160 would interface with the channel region in order to alter the lattice in the channel and achieve these benefits.

95. The complete structure of the embodiment depicted by Figures 2 to 6 includes both epitaxial “fin template 135” (purple) and epitaxial “semiconductor material 160” (checkered purple) disposed at one side of the “gate structure” (gold) and in contact with the “fins 120” as shown in Figure 6. *Id.*

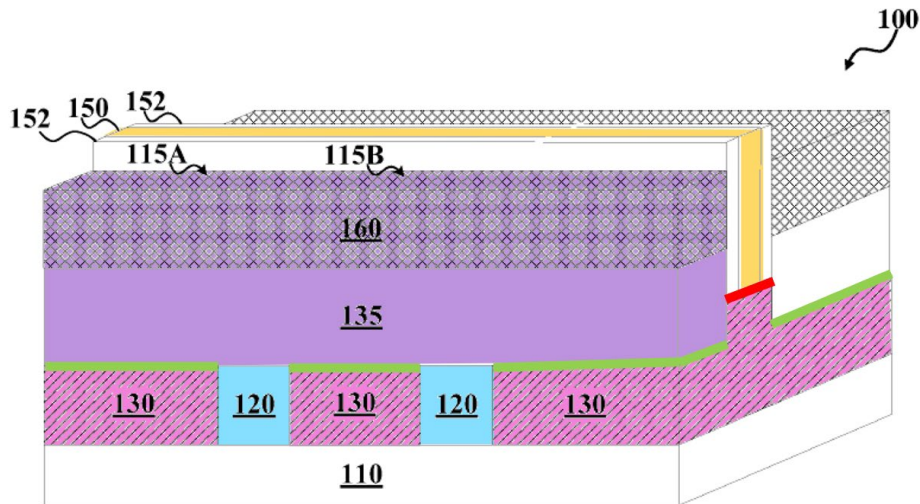


FIG. 6

96. As described above, each of epitaxially grown “fin template 135” and “epi grown semiconductor material 160” meet the requirements of element 1[d]. In addition to meeting the requirements of element 1[d] individually, the combination of “fin template 135” and “semiconductor material 160” is also “an epitaxial layer, disposed at one side of the gate structure and in direct contact with the fin structure” as claimed.

97. A POSITA would have understood that “an epitaxial layer” may comprise “one or more” epitaxial layers and therefore would have understood the combined layer of Xu to be “an epitaxial layer” as claimed. Further, Xu discloses that “fin template 135” and “semiconductor material 160” may be formed of the same materials, using the same deposition techniques and doping processes. *See* Ex. 1004 at 5:10-23; 5:55-67. This overlap in materials and deposition processes further

reinforces that a POSITA would have understood that the combined structure of “fin template 135” and “semiconductor material 160” collectively forms “an epitaxial layer” as claimed.

B. Claim 2: The semiconductor device according to claim 1, wherein there is a height difference between the first top surface and second top surface, and the height difference ranges from 100 Angstroms to 250 Angstroms.

98. As discussed above, Xu discloses and renders obvious a semiconductor device in accordance with claim 1.

99. Xu further discloses and renders obvious the additional limitations of claim 2. For example, as discussed above, Xu discloses a height difference between the first top surface and second top surface of the “isolation features 130” that results from the “etching process” that “selectively etches the isolation features 130.” *See* 1[c(ii)]; Ex. 1004 at 4:58-61. Xu further discloses that “in the depicted embodiment, the etching process uses a hydrofluoric acid (HF) etching solution of a suitable concentration (for example, 100:1)” and “the HF solution **recesses the isolation features 130 about 100 Å.**” *Id.* at 4:56-65 (emphasis added). Because the “etching process” recesses only the exposed “second top surface” (green)—and not the “first top surface” (red) under the “gate structure 150”—the complete structure of the embodiment depicted by Figures 2 to 6 discloses a height difference between the “first top surface and second top surface” of 100 Å.

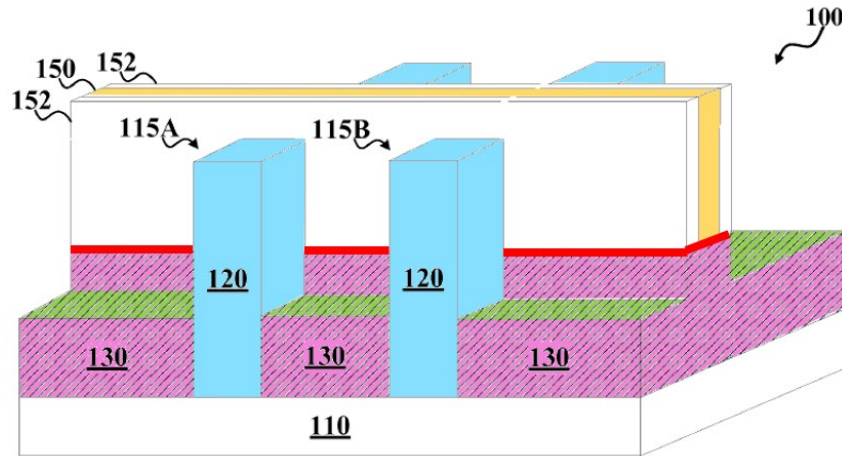
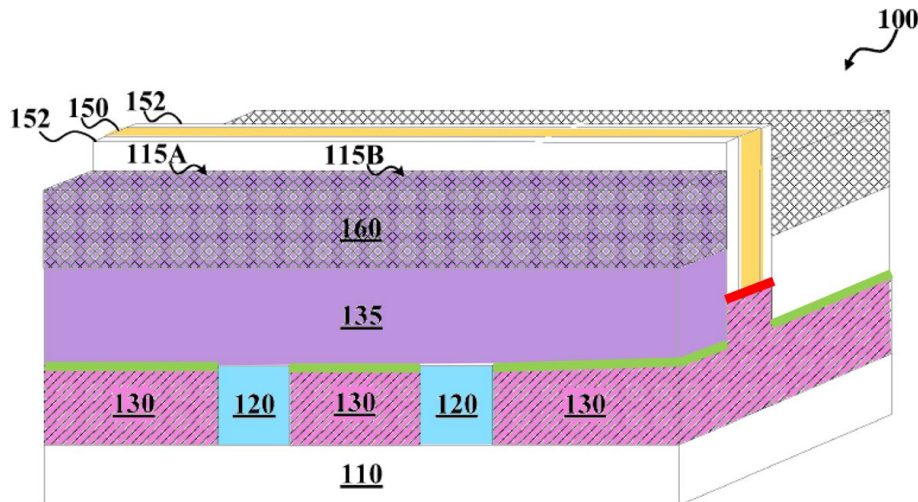


FIG. 3

100. Xu’s disclosure of recessing the second top surface (green) “about 100 Å” discloses the additional limitation of claim 2 because it lies inside the claimed range of “100 Angstroms to 250 Angstroms.”

101. The complete structure of the embodiment depicted by Figures 2 to 6 includes a height difference between the first top surface and second top surface, where the height difference ranges from 100 Angstroms to 250 Angstroms. The “isolation features 130” is not etched further in later steps at least in part because a “fin template 135” is subsequently “formed on exposed portions of the fins 120,” covering the first top surface (green), as shown in Figure 6. Ex. 1004 at 5:1-2.



C. Claim 3: The semiconductor device according to claim 1, wherein the gate structure is a metal gate structure.

102. As discussed above, Xu discloses and renders obvious a semiconductor device in accordance with claim 1.

103. Xu further discloses and renders obvious the additional limitation of claim 3. For example, Xu discloses that “[t]he gate structure 150 may include a gate dielectric layer and a gate electrode” and that “[t]he gate electrode includes ... a *metal* including Al, Cu, Ti, Ta, W, Mo, TaN, NiSi, CoSi, TiN, WN, TiAl, TiAlN, TaCN, TaC, TaSiN, other conductive materials, or combinations thereof.” Ex. 1004 at 4:2-3, 10-13.

104. A POSITA would have understood that “metal gate structure” refers to a gate structure comprising metal. For example, the ’609 Patent describes the “well-known” replacement metal gate process in which a dummy gate “composed of

polysilicon inside may be replaced with a metal gate structure.” Ex. 1001 at 7:12-24. Those skilled in the art would have appreciated that this was a common technique prior to the ’609 Patent that protects the final gate from high temperature processing that occurs earlier in the fabrication process, allows for greater control of the work function of the metal gate electrode, and can enhance channel stress in the transistor. Ex. 1008 at 16; Ex. 1022 at 128; Ex. 1023 at 620.

105. As the ’609 Patent and Xu both disclose, the “gate structure” may comprise a metal along with other associated layers. Ex. 1001 at 3:64-4:2, 7:10-25; Ex. 1004 at 4:2-3. By disclosing that the gate electrode may comprise metals (Ex. 1004 at 4:10-13), Xu discloses a metal gate structure.

D. Claim 4: The semiconductor device according to claim 1, wherein the isolation structure under the gate structure comprises a sidewall and the epitaxial structure⁵ is in direct contact with the sidewall.

106. As discussed above, Xu discloses and renders obvious a semiconductor device in accordance with claim 1.

⁵ Claims 4-8 and 10 use the term “epitaxial structure” as opposed to “epitaxial layer” as used in claim 1. I offer no opinion as to whether or not this language is definite, but interpret these instances of “epitaxial structure” as referring back to the “epitaxial layer” of claim 1.

107. Xu further discloses and renders obvious the additional limitations of claim 4. For example, “isolation features 130” undergo an “etching process” which results in the “isolation features 130” under the “gate structure 150” comprising a sidewall, as shown below in Figure 3 (yellow). Ex. 1004 at 4:54-61.

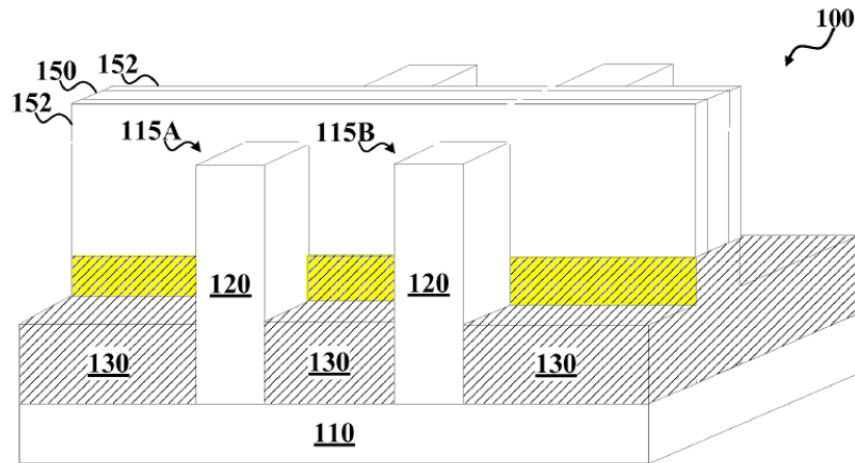


FIG. 3

108. In Xu, “fin template 135 is ... formed by a silicon epitaxial deposition process” or “by a silicon germanium epitaxial deposition process.” Ex. 1004 at 5:15-20. Then, in Xu’s device, the “fin template 135” (*i.e.*, the claimed “an epitaxial structure”) is in direct contact with the sidewall of the “isolation features 130” under the “gate structure 150,” as shown in annotated Figure 6 below. Ex. 1004 at Fig. 6.

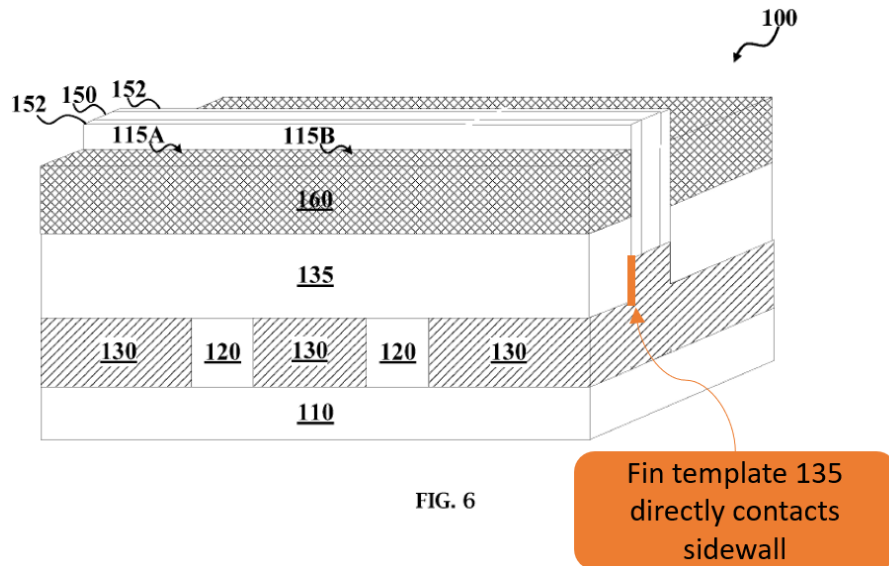


FIG. 6

109. As described above, “fin template 135” is, itself, the epitaxial layer as claimed and therefore the interface between “isolation features 130” under the gate structure and “fin template 135” represents the claimed direct contact between the isolation features and the epitaxial layer. Additionally, when “fin template 135” and “semiconductor material 160” (disclosed by Xu as being “epitaxially grown over the fin template 135”) are taken together as “the epitaxial structure,” this combined structure still meets the limitations of claim 4 through the contact between the sidewall of “fin template 135” and the “isolation features 130.”

E. Claim 5: The semiconductor device according to claim 1, further comprising a recess formed at one end of the fin structure, wherein the epitaxial structure fills up the recess.

110. As discussed above, Xu discloses and renders obvious a semiconductor device in accordance with claim 1.

111. Xu further discloses and renders obvious the additional limitations of claim 5. Specifically, Xu discloses a second embodiment of the FinFET device 200 where the “fin structures 215A and 215B” have two portions 220 and 230 (as shown in Figure 8A) and **“an etching process completely removes the fin portions 230 from the source and drain regions of the fin structures 215A and 215B, exposing the fin portions 220”** (as shown in Figure 9A). Ex. 1004 at 7:58-61, 10:34-36; Fig. 7 (“[c]ompletely remove the second material portion [230] from the source and drain regions of the first and second fin structure”).

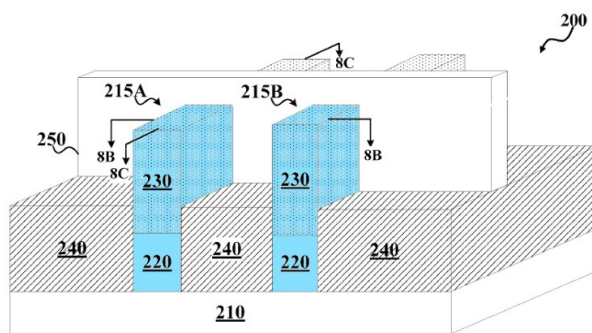


FIG. 8A

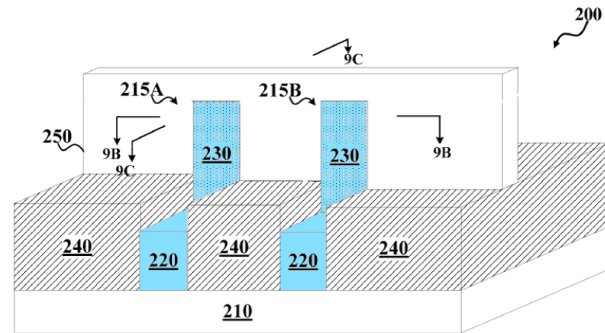


FIG. 9A

This etching process forms recesses in fin structure 215A, 215B at one end of the fin structure. *Id.* at Fig. 10

112. Xu further discloses that, in the second embodiment, “fin template 280” is “a semiconductor material [that] is epitaxially (epi) grown on the exposed fin portions 200” and fills up the recess formed by the prior etching process. Ex. 1004 at 11:2-8. This is depicted in annotated Fig. 10A below:

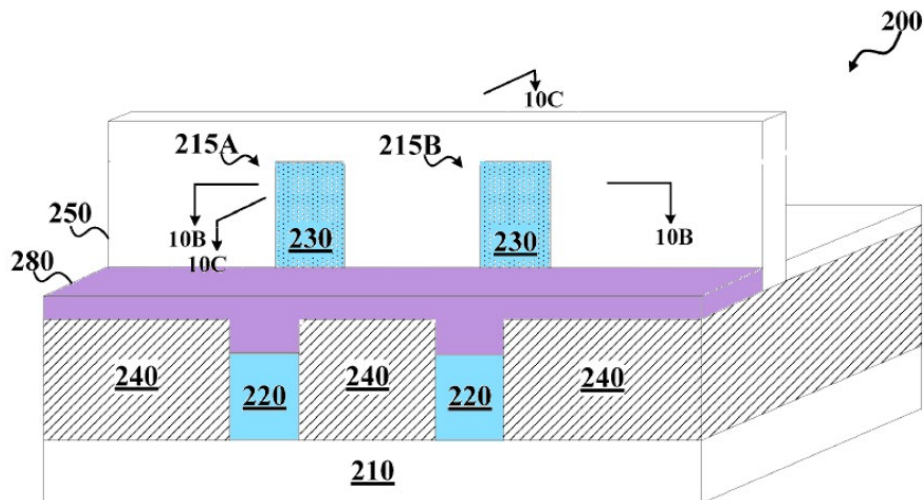


FIG. 10A

113. Specifically, Xu discloses that after the fins are recessed, fin template 280 “may be formed by a process similar to that described above with reference to FIG. 5” of Xu’s first embodiment.” Ex. 1004 at 11:2-4. In other words, Xu expressly discloses that the same epitaxial growth process of the first embodiment is used to fill the recess with the “fin template” (purple). *Id.* Accordingly, Xu’s second embodiment discloses a recess formed at one end of the fin structure, wherein the epitaxial structure fills up the recess.

114. It would have been obvious to a POSITA to combine the recess-and-fill of Xu’s second embodiment with Xu’s first embodiment such that the first embodiment includes an epitaxial structure filling the recess. First, this would have merely involved combining embodiments disclosed in the same reference, in close proximity to one another. In my opinion, it would have been readily apparent and obvious to a POSITA to combine the teachings of both embodiments from these

disclosures in a single reference. And, as described further below, Xu itself suggests combining these embodiments. Ex. 1004 at 16:5-17:10. The obviousness of this combination is especially apparent given that Xu itself suggests such a combination when summarizing the invention.

115. Additionally, Xu explains the benefits of using such recesses, noting that “by controlling source and drain trench depth”—which is dictated by the depth of the recess—“strain for both PMOS and NMOS FinFET devices can be achieved and optimized” and “different types of strain can be achieved.” Ex. 1004 at 15:56-66. “Accordingly, the trench depth can be tuned to independently optimize performance of each FinFET device in an integrated circuit device.” *Id.* at 15:67-16:2. Thus, the POSITA would have understood that recessing “fins 120” of Xu’s first embodiment will result in “achiev[ing] and optimiz[ing]” strain. *Id.* at 15:56-60, 15:67-16:2. Xu therefore expressly recognizes an advantage or expected beneficial result that would have motivated a POSITA to combine the recess-and-fill of the second embodiment with Xu’s first embodiment.

116. Further, a POSITA would have understood that nMOS devices benefit from tensile strain (*e.g.*, via SiC source/drain regions) and pMOS devices benefit from compressive strain (*e.g.*, via SiGe source/drain regions). *See, e.g.*, Ex. 1004 at 1:16–38; Ex. 1005 at ¶¶ [0002], [0035]. As discussed above, tensile strain enhances electron mobility by reducing effective mass and scattering in the conduction band, while

compressive strain improves hole mobility by modifying the valence band structure. Improved mobility directly translates into higher drive current, faster switching speed, and reduced delay, which are critical for achieving high-performance, low-power logic. A POSITA would also have known that strain must be carefully localized in the channel region to be effective, and that epitaxial regrowth of lattice-mismatched materials after selective S/D recessing was an established and effective technique to introduce such localized strain without disrupting overall device geometry or reliability. Tailoring strain for different transistor types (nMOS vs pMOS) using these epitaxial stressors was a well-understood and widely practiced technique, before the filing date of the '609 patent. *See, e.g.,* Ex. 1004 at 1:16–38; Ex. 1005 at [0002], [0035]. A POSITA therefore would have been familiar with the goal of imparting and optimizing strain sought by Xu's recessing process and would have found it obvious to apply this technique to Xu's first embodiment in order to further tailor the strain. In short, Xu's disclosure would have been viewed as compatible with, and motivated by, the well-known design objective of improving channel strain through source/drain engineering.

117. Moreover, starting from 16:5 through 17:10, Xu summarizes the invention in a way that suggests combining steps of Xu's first embodiment with steps of Xu's second embodiment in a single embodiment. Ex. 1004 at 16:5-44, 16:45-17:10. Xu explicitly states that the "disclosure provides for **many** different

embodiments.” Ex. 1004 at 16:5-6 (emphasis added). For example, Xu discloses a method (Ex. 1004 at 16:7-26) that can include “etching back the isolation structure” as taught in Xu’s first embodiment. Ex. 1004 at 16:17-19. Xu then presents alternative modifications to this method. *Id.* at 16:27-44. Specifically, Xu discloses “[t]he method may include completely removing the second material portion from the source and drain regions of the fins before forming the fin template.” *Id.* at 16:40-43. These techniques correspond to the fin recess-and-fill steps described in Xu’s second embodiment, as shown in Figures 7, 8A and 9A. Ex. 1004 at 16:45-17:10 (describing “another embodiment” that may include “etching back the isolation structure” and “removing a portion of the first and second fin structures before epitaxially growing the first semiconductor material” which may include “completely removing the second material portion”).

118. In my opinion, Xu’s express disclosure of using these steps together clearly suggests and renders obvious the combination of the first and second embodiments. A POSITA reading Xu’s disclosures of the first embodiment and second embodiment would not have had to consult other references, perform additional research or conduct further experimentation to arrive at this combined approach and to become appraised of all elements of the combination *and* an explanation of the potential advantages of including the fin recessing step. Rather, Xu’s own summary of the invention provides a direct rationale and support for

combining the disclosed etch-back and fin-recess steps into a unified process, rendering such a combination obvious. In my opinion, Xu's express disclosure of using these steps together suggests and renders obvious the combination of the first and second embodiments.

119. Additionally, it is my opinion that a POSITA would have had a reasonable expectation of success in making this combination. Xu discloses exemplary etch processes which can be used to perform the step of recessing the fin. Ex. 1004 at 10:36-61; 13:44-55. A POSITA would have understood these to be conventional, well-controlled etching techniques, readily applicable to the fin structures of Xu's first embodiment for precisely controlling the recess depth.

120. In particular, a POSITA would not view the etch-back of the STI in Xu's first embodiment as a technical barrier to implementing an optimized fin recess. These two steps, STI recessing and fin recessing, are independent and separable, and can be performed using known anisotropic etching techniques, including those explicitly disclosed in Xu, which teach etch selectivity and depth control. Ex. 1004 at 10:27-62.

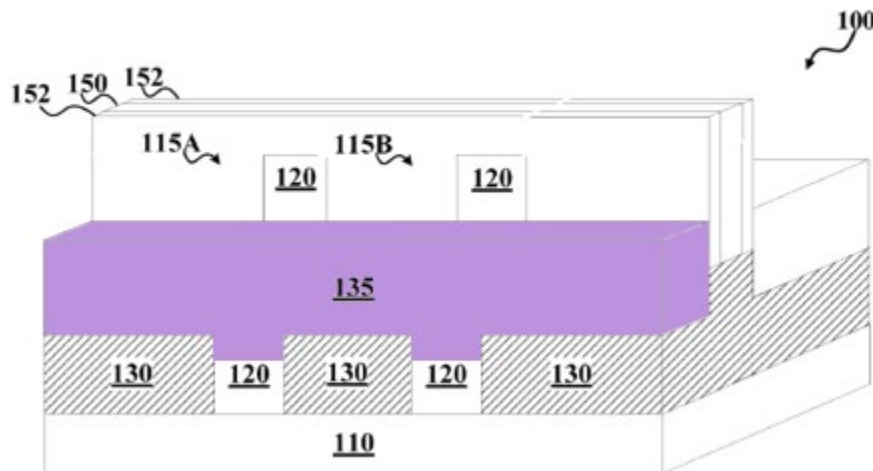
121. In my opinion, the combination of Xu's first and second embodiments is merely the application of a known technique to a known method that is ready for improvement. Specifically, Xu's first embodiment is a well-known conventional method for fabricating FinFET devices. The recessing of the fins of Xu's second

embodiment is also a known technique, and one that may be applied to the first embodiment. A POSITA would have recognized that applying the recessing of the fins to the first embodiment would have yielded predictable results in enhanced channel strain, consistent with Xu's own teaching of "provid[ing] different starting substrates for forming the fin templates, such that different types of strain can be achieved." Ex. 1004 at 15:64-16:2.

122. Finally, I note that Claim 19 of Xu further reinforces the obviousness of such a combination. Like the summary portions of the specification described above, Claim 19 sets forth a method that combines steps of the first embodiment with steps of the second embodiment. Specifically, claim 19 combines "completely removing the second material portion from the source and drain regions of the fins" (Ex. 1004 at 20:19-21) with "recessing the isolation structure by removing a portion of the isolation structure" (*id.* at 19:8-10, independent claim 11). Thus, Xu's claim 19 explicitly recites a fabrication method that combines the step of "recessing the isolation structure by removing a portion of the isolation structure"—as disclosed in the first embodiment—with the step of removing materials from the source and drain regions of the fins to form recesses in the fin structures—as described in the second embodiment. Ex. 1004 at Claim 19. That Xu claims these steps together demonstrates that a POSITA would have found it obvious to combine the first embodiment with the fin recess-and-fill of the second embodiment to arrive at the claimed semiconductor

device. A POSITA reading claim 19 could have easily contemplated such a combination and would have had a reasonable expectation of success in making it using conventional fabrication tools and known process flows.

123. When the recesses of the second embodiment are formed in the first embodiment, a POSITA would have understood and found it obvious that an epitaxial layer (purple) will “fill the recesses” because Xu teaches that, in both embodiments, the epitaxial layer is formed on the “exposed portions of the fins 120.” Ex. 1004 at 5:1-2 (first embodiment); 11:4-8 (second embodiment). This is shown in modified figure 5 below, which depicts the combination of the second embodiment’s recesses with the first embodiment:



F. Claim 6: The semiconductor device according to claim 5, wherein a bottom surface of the epitaxial structure is shallower than a bottom surface of the isolation structure.

124. As discussed above, Xu discloses a semiconductor device in accordance with claim 6.

125. Xu further discloses and renders obvious the additional limitations of claim 6. As discussed above, a POSITA would have been motivated to combine Xu's first embodiment with the technique for recessing the "fins 120" and filling the recesses with an epitaxial structure taught by Xu's second embodiment. *See supra* cl. 5. For example, as shown in Figure 10A, the bottom surface of epitaxial structure 280 is shallower than the bottom surface of the isolation structure 240 when the fin recess techniques of the second embodiment are applied. Ex. 1004 at Fig. 10A. This is because fin portion 220 is not completely removed during the etching process and forms a bottom surface (yellow) for epitaxial structure 280 (purple). The bottom surface of the epitaxial structure 280 is higher (and therefore shallower) than the bottom surface of isolation structure 240 (brown).

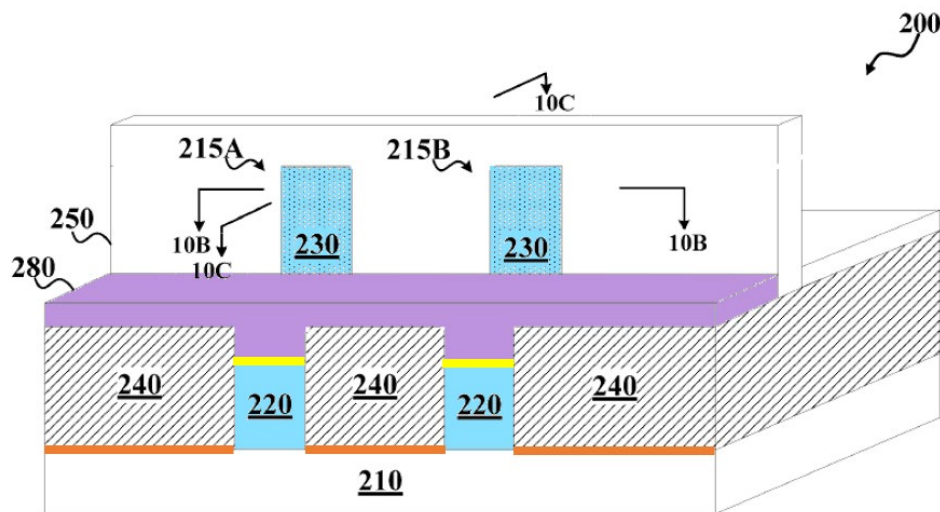
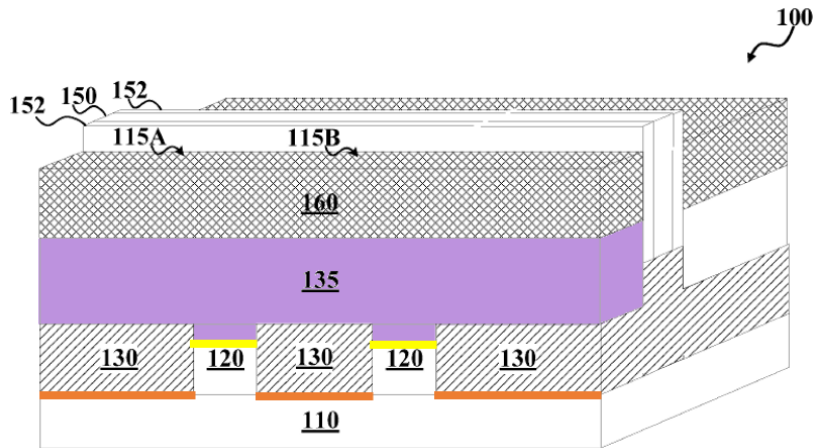


FIG. 10A

126. A POSITA would have understood “shallower” in this instance to refer to points closer to the top of the original fin. The ’609 Patent discloses the extent of the recess formed in each fin by a “depth D2.” Ex. 1001 at 5:59, Fig. 8. A POSITA would have understood that the etch process begins at the top surface of the original fin structure and etches downward to achieve this depth. Thus, elements that are closer to the bottom of the device (as measured in the orientation depicted in the figures) are “deeper” and elements closer to the top of the device are “shallower.” Xu similarly discloses, “removed fin portions 230 form trenches [(i.e., “recesses”)] in the source and drain regions of the fin structures 215A and 215B.” Ex. 1004 at 10:50-52. Xu therefore describes the extent of these trenches, or recesses, by a “depth” of the trenches. *Id.* at 10:55-57. Accordingly, the bottom surface of fin template 280 depicted in Fig. 10A is “shallower” than the bottom surface of the isolation structure 130.

127. The modified figure below shows the combination of Xu’s first and second embodiments. The fin template (epitaxial structure) will also have a bottom surface (yellow) that is shallower than the bottom surface of the isolation structure (brown) for the same reasons as the second embodiment in Figure 10A.



128. This is consistent with the disclosures of the first embodiment, where the “epitaxial structure 135” has a bottom surface (yellow) in contact with the top surface of the isolation structure 130, and is therefore shallower than the bottom surface (brown) of isolation structure 130 (which is in contact with substrate 110).

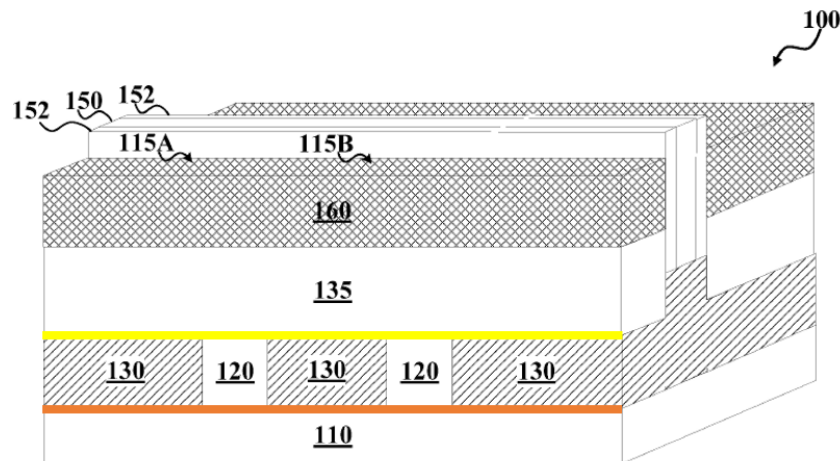


FIG. 6

G. Claim 8: The semiconductor device according to claim 1, wherein the epitaxial structure comprises silicon germanium, silicon phosphide or phosphor-doped silicon carbide.

129. As discussed above, Xu discloses and renders obvious a semiconductor device in accordance with claim 1.

130. Xu further discloses and renders obvious the additional limitations of claim 8. For example, Xu discloses that the “fin template 135,” which is an epitaxial structure as discussed above, *supra* 1[d], “could be silicon germanium (SiGe)” or silicon phosphide. Ex. 1004 at 5:18-20, 5:23-35 (“the epi silicon fin template 135 may be doped with phosphorous (to form a Si:P epi layer)”). As another example, Xu discloses that the “semiconductor material 160,” which is an epitaxial structure as discussed above, *supra* 1[d], “is silicon germanium (SiGe).” Ex. 1004 at 5:59-62. As both the fin template 135 and semiconductor material 160 may be SiGe, Xu also discloses and renders obvious this claim when the combination of fin template 135 and semiconductor material 160 are taken as the “epitaxial structure.”

H. Claim 9: The semiconductor device according to claim 1, further comprising a spacer disposed on a sidewall of the gate structure.

131. As discussed above, Xu discloses and renders obvious a semiconductor device in accordance with claim 1.

132. Xu further discloses and renders obvious the additional limitations of claim 9. For example, Xu discloses that “[s]pacers 152 are disposed on the sidewalls of the gate structure 150, such as along the gate electrode.” Ex. 1004 at 4:39-40. The

complete structure of the embodiment depicted by Figures 2 to 6 includes “spacers 152” (dark blue) disclosed on a sidewall of the “gate structure 150” as shown in Figure 6. *Id.* at Fig. 6.

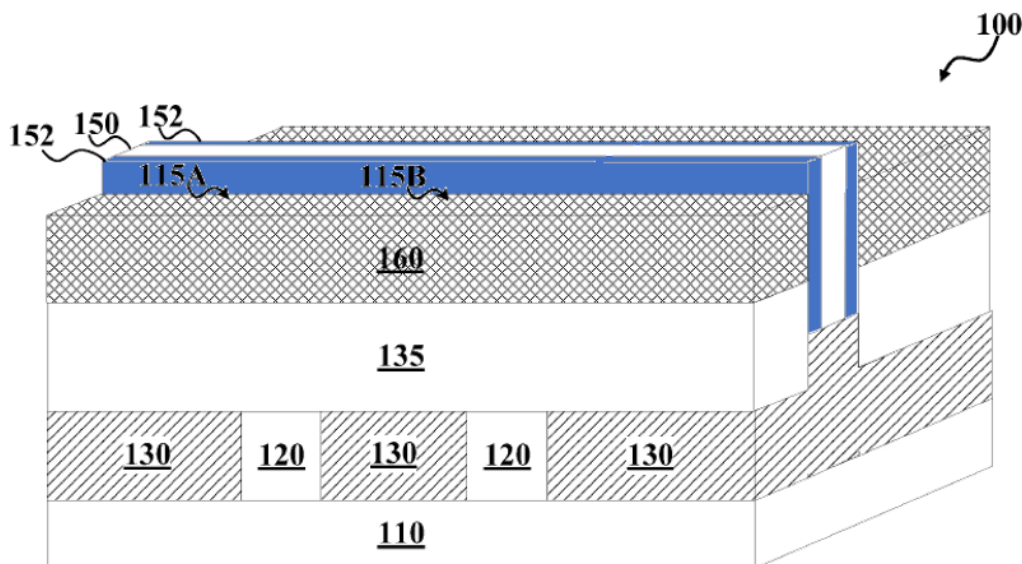


FIG. 6

I. Claim 10

1. **10[pre]: The semiconductor device according to claim 1, further comprising:**

133. As discussed above, Xu discloses and renders obvious a semiconductor device in accordance with claim 1.

2. **10[a]: another epitaxial structure, disposed at another side of the gate structure and in direct contact with the fin structure; and**

134. Xu discloses and renders obvious this limitation. For example, as explained above for limitation 1[d], Xu discloses a “fin template 135” and “semiconductor material 160” which are epitaxially grown, disposed on one side of

the “gate structure 150,” and in direct contact with “fins 120.” *See supra* 1[d]. As described above, the combination of “fin template 135” and “semiconductor material 160” is also “an epitaxial [structure]” as set forth in claim 1. *Id.*

135. Xu further discloses that both “fin template 135” and “semiconductor material 160” are epitaxially grown in the “**source and drain** regions of the fin structure 115A and 115B.” Ex. 1004 at 5:49-53 (emphasis added). Xu recognizes that source and drain regions are “separated by the gate structure.” *Id.* at 16:34-39. Indeed, a POSITA would have understood that the source and drain regions of a transistor are on opposite sides of the gate structure in a FinFET device. *See supra* III.A. Thus, “fin template 135” (purple) and “semiconductor material 160” (checkered purple) are disposed at “another side of the gate structure” and in direct contact with the fin structure for the same reason that these structures are in direct contact with the fin structure on the first side of the gate structure as shown in Figure 6 below. *See supra* 1[d].

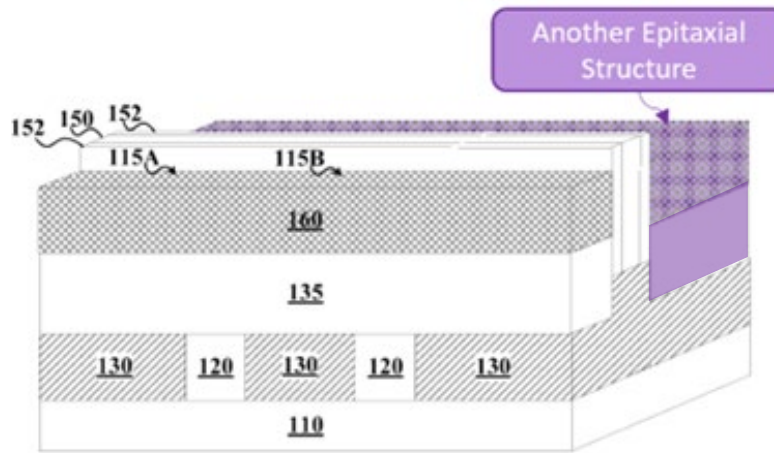


FIG. 6

3. **10[b]: a channel region, contiguous to the top surface and the side surfaces of the fin structure, and between the epitaxial structure and said another epitaxial structure;**

136. Xu discloses and renders obvious this limitation. For example, Xu discloses that the “fins 120 include a source region, a drain region, and a channel defined between the source and drain regions.” Ex. 1004 at 3:14-16. The channels can be seen in Figure 5 (light blue), as Xu discloses that when the “fin template 135 is etched back,” the “channels of the fin structures” are “expose[d].” *Id.* at 5:43-45. As shown below, the channel (light blue) is contiguous with the top surface and both side surfaces (orange) of the fin structure. *Id.* at Fig. 5. The channel is then covered by semiconductor material 160 (a portion of the source and drain epitaxial structure). *Id.* at Fig. 6. Xu thus discloses that the channel region is between the epitaxial structure (one of the source/drain) and said another epitaxial structure (the other of the source/drain).

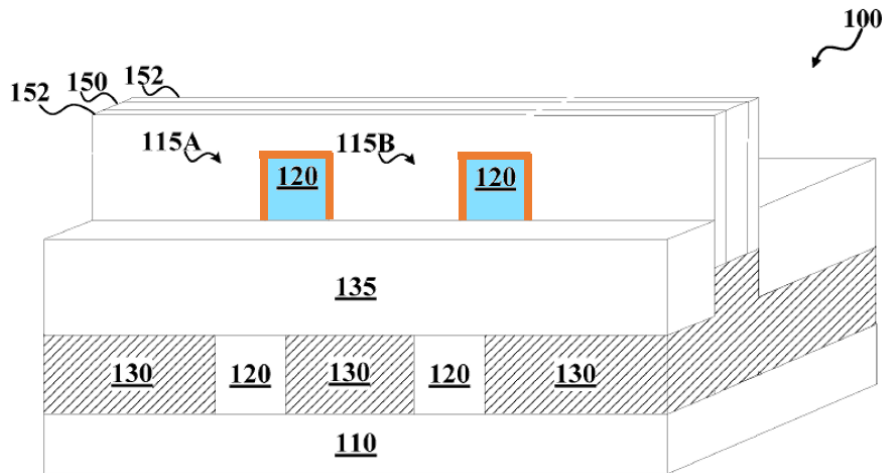


FIG. 5

137. As Xu recognizes, a “typical” FinFET device includes a “channel” that “is formed in the vertical fin” and “[a] gate is provided over (e.g., wrapping) the fin.” *Id.* at 1:22-26. Xu further teaches that “[i]t is beneficial to have a gate on both sides of the channel allowing gate control of the channel from both sides.” *Id.* at 1:26-28. A POSITA would have understood this arrangement to be a conventional **tri**-gate FinFET structure where the gate overlays the channel on **three** surfaces (top and two sides).

138. A POSITA would further understand the channel extends below the “gate structure 150” and is therefore positioned “between the epitaxial structure and said another epitaxial structure.” For example, Xu discloses that the “source and drain regions of each of the first and second fins **defines a channel therebetween.**” Ex. 1004 at 17:25-27 (emphasis added).

139. After the channel is exposed as shown in Figure 5 above, Xu's fabrication process deposits epitaxial "fin template 135" (purple) and epitaxial "semiconductor material 160" (checkered purple) on fin structures 120 on both sides of the gate—*i.e.*, in the source and drain regions. Ex. 1004 at 5:4-8, 5:49-55. Thus, as shown in Figure 6 below, the channel region (no longer exposed) is between the epitaxial structure 135 and/or 160 and the "another epitaxial structure" on the other side of the gate. *Id.* at Fig. 6.

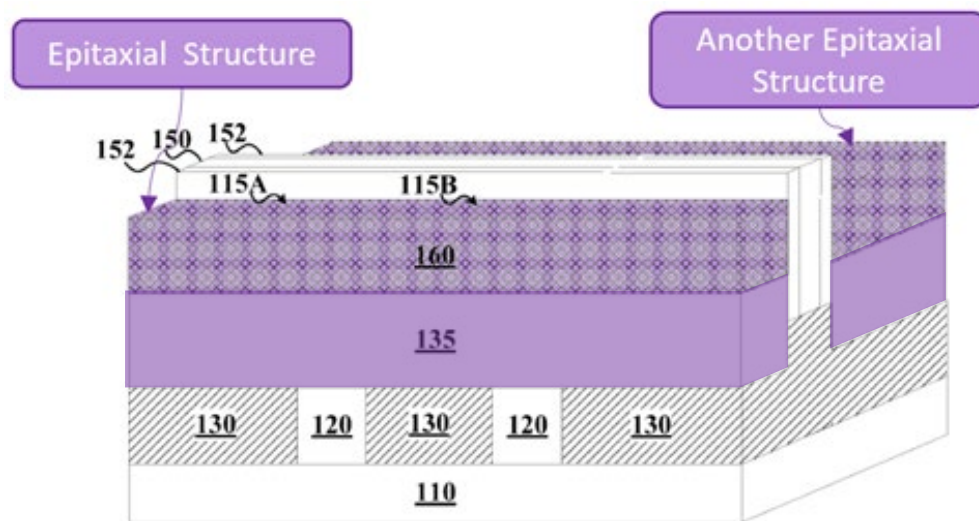


FIG. 6

140. This holds true whether the "fin template 135" alone, "semiconductor material 160" alone, or the combination of these elements is considered the "epitaxial structure."

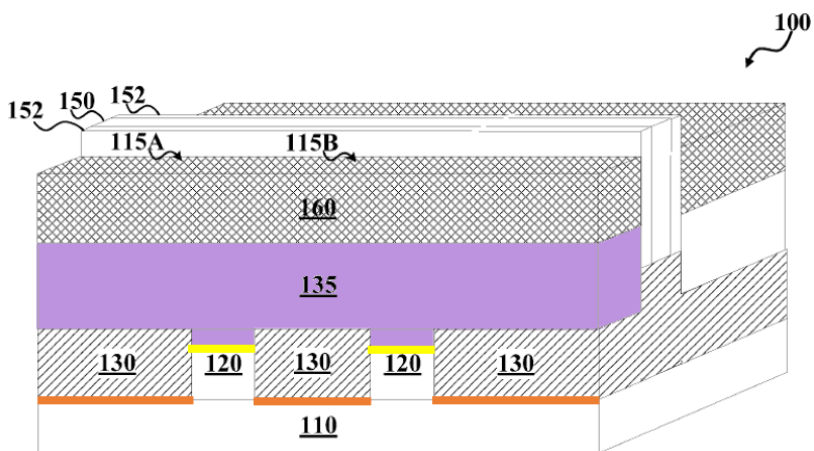
VIII. Ground 1B: Claim 7 Are Obvious Over Xu In View Of Huang

141. In my opinion, claim 7 would have been obvious to a POSITA over Xu in combination with Huang.

A. Claim 7: The semiconductor device according to claim 6, wherein there is a height difference between the bottom surface of the epitaxial structure and the bottom surface of the isolation structure, and the height difference ranges from 100 Angstroms to 250 Angstroms.

142. As discussed above, Xu discloses and renders obvious the fabrication method of claim 6. Xu in view of Huang renders obvious claim 7.

143. Specifically, as discussed above with respect to claims 5 and 6, the combination of Xu's first and second embodiments comprises an epitaxial structure formed within a recess in the fin structure such that the bottom surface of the epitaxial structure (yellow) is shallower than the bottom surface of the isolation structure (orange):



Ex. 1004 at Fig. 11A (modified).

144. Xu discloses that the recesses are formed to a controllable “depth (d_1)” (Ex. 1004 at 10:55-57) and that the “depth can be controlled” to yield different source/drain configurations and induce tailored channel strain for various FinFET devices (*id.* at 14:6-9). While the depth of these recesses is a controlled variable, Xu does not disclose example numerical values for the depth or for the dimensions of the nearby structures.

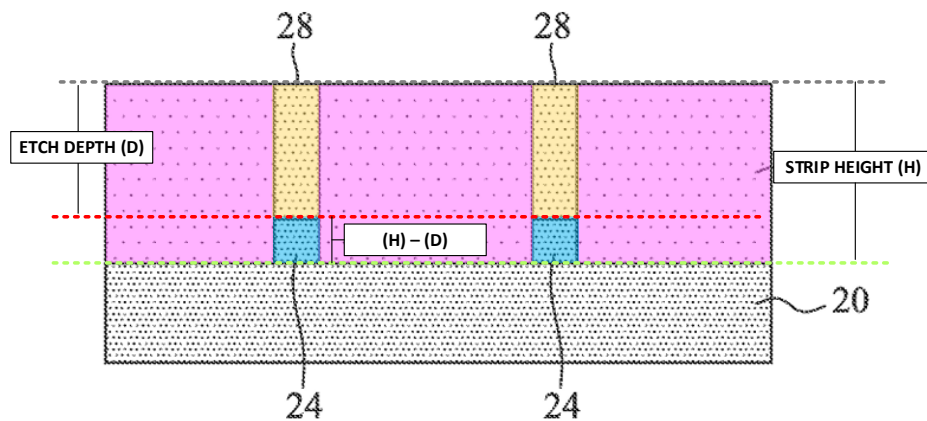
145. Xu therefore differs from claim 7 only in that Xu does not explicitly disclose the specifically claimed dimensions of the height difference between the bottom surface of the epitaxial structure and the bottom surface of the isolation structure. To fill this gap, a POSITA would have found it obvious to optimize the etch depth through routine experimentation to yield a desired strain.

146. In conducting such experimentation, a POSITA would have found it obvious to turn to additional prior art, such as Huang, for concrete dimensional guidance concerning the recess depth. In fact, Huang provides precisely the kind of dimensional specificity that Xu lacks. Like Xu, Huang discloses a method of fabricating a FinFET device including epitaxially growing source and drain regions in recesses formed within fin structures. Ex. 1006 at 4:30-36. Huang further expressly discloses specific dimensions for these features.

147. For example, Huang discloses forming “semiconductor strips 24” to “have a height from about 10 nm to about 500 nm.” *Id.* at 2:58-59. These

semiconductor strips are interspersed with “dielectric layer 22” which may be “blanket deposited on the FinFET device” and planarized “until the tops of the semiconductor strips are exposed.” *Id.* at 3:7-8, 26-27. Huang’s “dielectric layer 22” occupies the same space as the “isolation features 130” of Xu and may be formed of the same materials, such as silicon oxide or silicon nitride. Ex. 1004 at 3:58-62; Ex. 1006 at 3:8-13. A POSITA would have understood these materials as insulating materials that are well-known to provide electrical isolation. A POSITA therefore would have understood Huang’s dielectric layer to be both (1) analogous to Xu’s “isolation features”; and (2) the claimed “isolation structure.” Accordingly, Huang discloses an initial height of both the “semiconductor strips 24” and “dielectric layer 22” (*i.e.*, “isolation structure”) of 10 nm to about 500 nm.

148. Huang further discloses “etching of portions of the semiconductor strips 24 in a strained source drain (SSD) etch step to form recesses 36 in the semiconductor strips 24.” Ex. 1006 at 4:10-12. Again, Huang expressly provides dimensions for these recesses, disclosing that the etch depth may be “from about 5 nm to about 25 nm.” *Id.* at 4:15-16. The resultant structure, shown in modified Fig. 4B, below, includes epitaxial structure (gold) grown atop the recessed semiconductor strips (blue), which remain surrounded by dielectric (magenta):



149. The vertical offset between the bottom surface of the epitaxial structure (red line) and the bottom surface of the dielectric (green line) corresponds to the difference between the strip height H (*i.e.*, “from about 10 nm to about 500 nm”) and the etch depth D (*i.e.*, “from about 5 nm to about 25 nm”). Accordingly, the height difference between the bottom surface of the epitaxial region and the bottom surface of the dielectric layer (*i.e.*, “isolation structure”) is in the range from about 5 nm to about 475 nm. Huang thus discloses the general conditions for recess depths in FinFET processing.

150. It would have been obvious from the teachings of Xu and Huang to optimize the recess depth through routine experimentation and arrive at the claimed height difference. A POSITA would have understood that, in Xu, the claimed height difference is a direct result of the depth of the fin recess. That is, the isolation structures and the fin structures of Xu have a common bottom surface (*see* Ex. 1004 at Fig. 2, Fig. 8A) and, therefore, the difference in height between the bottom surface

of the isolation structure and the bottom surface of the epitaxial material corresponds to the amount of material removed when the fin is recessed.

151. Xu explicitly discloses that the depth of this fin recess “can be controlled to achieve various source and drain features for the fin structures, such that different kinds of channel strain can be achieved for different FinFET devices.” Ex. 1004 at 14:6-9. In fact, Xu explains that this depth “can be tuned to independently *optimize* performance of each FinFET device in an integrated circuit.” *Id.* at 15:67-16:2. Accordingly, a POSITA would have understood that the trench depth is a results-effective variable that Xu itself contemplates controlling in order to optimize performance. Moreover, Xu discloses particular etching techniques that may be used to create this recess (*id.* at 10:34-47), and a POSITA would have been familiar with ways to tune etch depths and etch profiles (*see, e.g.*, Ex. 1025 at Ch. 21–22; Ex. 1006 at 2:45-67; Ex. 1004 at 10:34-47).

152. While Xu does not disclose numerical values for the recess depth and the resulting height difference, Huang discloses the general conditions of these parameters, namely, a recess depth of between 5 nm and 25 nm and a resulting height difference of between 5 and 475 nm. Ex. 1006 at 2:59, 4:16. Further, in my opinion, the '609 Patent does not posit any criticality or unexpected results associated with the claimed range. Accordingly, from these general conditions and Xu's express desire to control the recess depth to achieve optimal performance, it would have been obvious

to a POSITA to optimize the recess depth and resulting height difference through routine experimentation and arrive at the claimed height difference.

153. Moreover, the '609 Patent's claimed range (100 Angstroms to 250 Angstroms) lies entirely within the range disclosed by Huang (5 nm to 475 nm, or 50 Angstroms to 4,750 Angstroms). A POSITA would have understood and found it obvious that the lower end of Huang's range would be more desirable in FinFET fabrication because smaller vertical dimensions accompany lateral scaling to maintain electrostatic integrity, improve packing density and simplify integration. Transistor scaling (*i.e.*, reducing both horizontal and vertical dimensions) is a well-established and fundamental goal of the semiconductor industry. *See* Ex. 1004 at 1:17-19, 34-38; Ex. 1005 at 1:15-18; Ex. 1006 at 1:7-15. At its core, scaling increases transistor packing density, enabling more devices per chip, which enhances circuit speed and overall computing performance. Shrinking in the horizontal dimensions increases integration density, reduces circuit delay and allows operation at lower supply voltages, improving energy efficiency. Ex. 1027 at 6, 14. A POSITA would have understood and found it obvious that when scaling to increase density, it is desirable to also scale in the vertical direction to maintain the relationships among critical dimensions of the device such as gate length, oxide thickness, source/drain junction depth, and the steepness of the source/drain doping profile. Ex. 1029 at 542. Corresponding scaling in the vertical dimensions helps to prevent undesirable short

channel effects (Ex. 1031 at 328) and maintains a proper aspect-ratio for process integration (Ex. 1028 at 2). High aspect-ratio features resulting from insufficient vertical scaling can cause process difficulties and undesirable outcomes such as non-uniform fills and poor step coverage. (Ex. 1028 at 2; Ex. 1030 at 94). A POSITA therefore would have been motivated to favor a smaller vertical offset, such as those at the lower end of Huang's range, as part of the well-established and predictable practice of scaling both horizontal and vertical dimensions to improve device performance and manufacturability.

154. Xu and Huang both recognize the industry-wide desire to scale down FinFET device size to permit more transistors to fit on the same sized chip. Ex. 1004 at 1:17-19, 34-38; Ex. 1006 at 7-15. A POSITA therefore would have been motivated to minimize the footprint of Xu to achieve higher density and performance. In doing so, the POSITA would have pursued the lower end of Huang's range, including from 100 Angstroms to 250 Angstroms. Height differences in this range are more applicable to smaller FinFETs with smaller overall footprints, when compared to the higher end of Huang's range, and a POSITA would have reasonably expected the resultant device to operate successfully.

155. A POSITA also would have been motivated to apply the teachings of Huang to the teachings of Xu and found it obvious to arrive at the claimed height difference due to the overlap of the claimed range and Huang's disclosed range. The

claim recites a range that lies completely within the range disclosed by Huang. While Huang discloses a larger range than that which is claimed, the difference is an order of nanometers, rather than a situation in which the prior art discloses an open-ended or potentially infinite range.

156. Plus, Xu explicitly motivates a POSITA to control the recess depth to achieve a desired strain (Ex. 1004 at 14:6-9) and both Huang and Xu explicitly motivate a POSITA to explore the lower end of Huang's range where the claimed range sits, as described above. That the claimed range lies within the portion of Huang's range exhibiting desirable features such as increased density further underscores the obviousness of this range. Additionally, a POSITA would have had a reasonable expectation of success in arriving at these desirable features using the exemplary etch processes disclosed by Huang to achieve the claimed height difference.

IX. Ground 2A: Claims 1, 3, 5-6, And 8-10 Are Anticipated And/Or Obvious Over Ching

157. In my opinion, claims 1-3, 5-6, and 8-10 would have been obvious to a POSITA over Ching in view of the knowledge of a POSITA.

1. 1[pre]: A semiconductor device, comprising:

158. Ching discloses and renders obvious a semiconductor device. For example, Ching discloses a "Fin Field-Effect Transistor (FinFET)," which is a

semiconductor device. Ex. 1005 at 1:53-55. Figures 1-9D illustrate “intermediate stages in the manufacturing of a FinFET.” Ex. 1005 at 1:60-62.

2. 1[a]: a fin structure, protruding from a surface of a substrate, wherein the fin structure comprises a top surface and two side surfaces;

159. Ching discloses and renders obvious this limitation. For example, Ching discloses “semiconductor strips 21” (blue) protruding from a surface of “substrate 20” (green) as shown in Figure 9A, below. Ex. 1005 at Fig. 9A. The “semiconductor strips 21” comprise a top surface and two side surfaces as shown below.

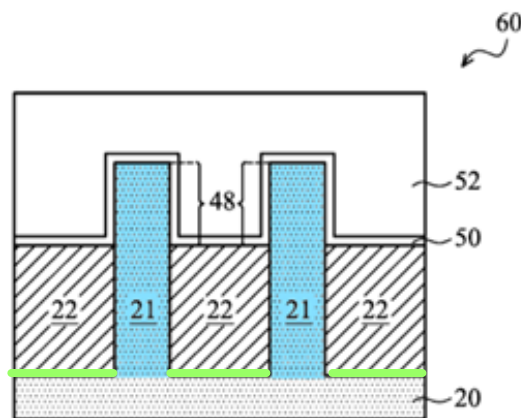


Fig. 9A

160. According to Ching “the portions of semiconductor strips 21 over top surface 22B form semiconductor fins 48,” confirming that semiconductor strips 21 are “fin structures.” *Id.* at 4:12-16.

161. This is consistent with the '609 Patent which uses the term “fin structure” to refer to the entirety of semiconductor material portions that protrude from the substrate after an etching process is performed to form such protrusions. *See* Ex. 1001

at 3:21-25 (“the fin structures 12 may be regarded as protruding from the surface 10a of the substrate and the compositions of the fin structures 12 and the substrate 10 may be the same.”).

3. 1[b]: an isolation structure, disposed on the surface of the substrate and surrounding the fin structure;

162. Ching discloses and renders obvious this limitation. For example, Ching discloses “Shallow Trench Isolation (STI) regions 22” (magenta) disposed on the surface of substrate 20 (green) and surrounding the “semiconductor strip 21” (blue) as shown in Figure 1. Ex. 1005 at Fig. 1. According to Ching, “semiconductor strip 21 [(blue)] is formed between, and contacting, neighboring STI regions 22 [(magenta)].” *Id.* at 2:5-6.

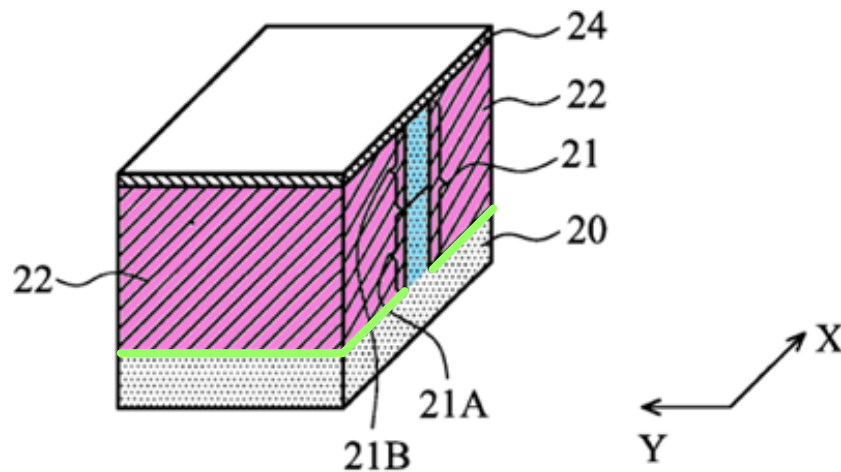
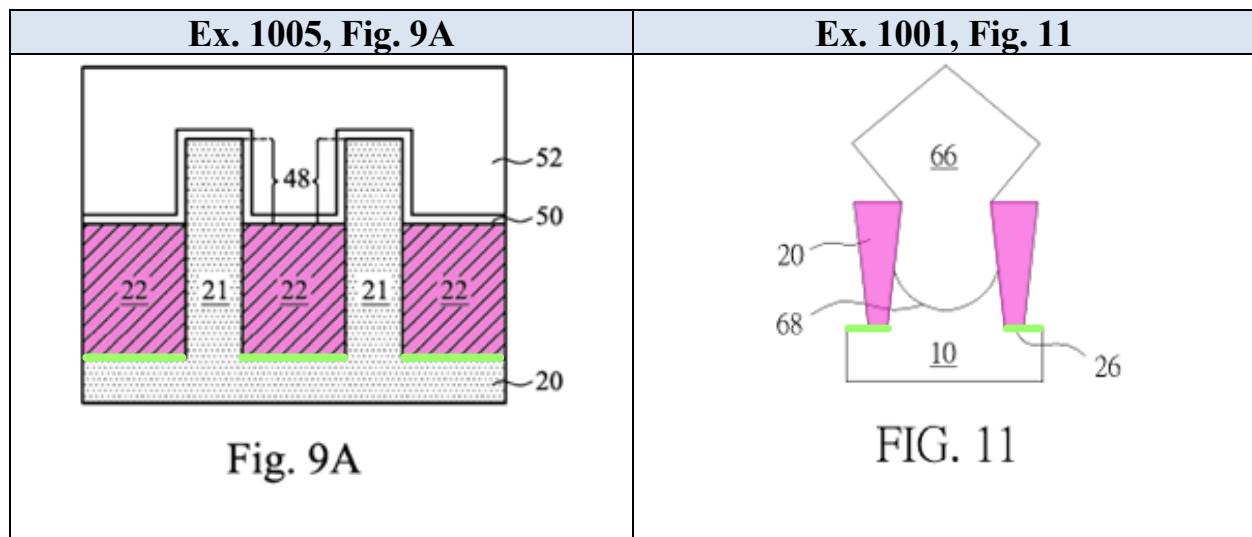


Fig. 1

163. While Ching discloses the STI regions are “formed in substrate 20 and extend from a top surface of substrate 20 into substrate 20” (Ex. 1005 at 2:2-4), a

POSITA would have understood this as referring to an initially formed substrate which is modified to accommodate STI regions 22 resulting in a substrate 20 having the surface indicated by the green lines above. For example, a POSITA would have understood that STI regions 22 could be formed by, for example, etching recesses into a bulk substrate and filling those recesses with STI (as is done in the '609 Patent), or through a thermal oxidation (e.g. LOCOS - Local Oxidation of Silicon), or similar process, that converts the substrate material into isolation regions (see Ex. 1025, Ch. 4). The result in Ching is a final device in which the STI regions 22 (magenta) are formed on the surface (green) of the remaining substrate from which the fin structures protrude. As depicted below, this is consistent with the positioning of the isolation structures of the '609 Patent:



Accordingly, a POSITA would have understood Ching as disclosing an isolation structure disposed on the surface of the substrate, as claimed. *See, e.g.*, Ex. 1005 at Fig. 1, Fig. 9A.

164. Ching further discloses the “STI regions 22” (*i.e.*, “isolation structure”) surrounding the “semiconductor strips 21” (*i.e.*, “fin structures.”). For example, a cross-section of the completed transistor⁶ in accordance with the 8E/9D embodiment is shown below, which shows “STI regions 22” (magenta) disposed on the surface of the substrate 20 and surrounding “semiconductor strips 21” on at least two sides. Ex. 1005 at Fig. 9A.

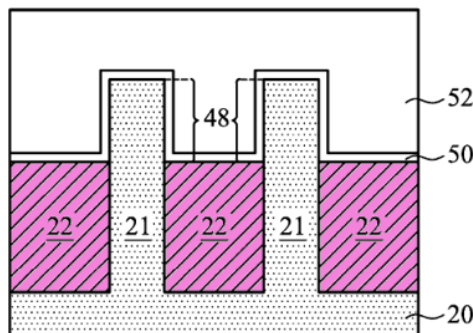


Fig. 9A

⁶ Ching discloses that the FinFET device is “finished” upon subsequent formation of ILD and contact plugs. Ex. 1005 at 5:12-17. These subsequent (and not shown) steps do not alter the structures depicted in Figs. 9A-9D and these figures therefore depict these structures as they are in the completed device.

165. To the extent the claim language requires the isolation structure to *fully* encircle the fin structures, Ching discloses and renders this obvious as well. A POSITA would have further understood that the shallow trench *isolation* regions (“STI regions 22”) isolate “semiconductor strips 21” from one another *and* isolate the transistors that will ultimately be formed from “semiconductor strips 21” from one another. Therefore, a POSITA would have understood that “STI regions 22” surround the semiconductor “semiconductor strips 21” in order for the resulting transistors to function properly.

4. 1[c(i)]: a gate structure, overlaying the top surface and the two side surfaces of a portion of the fin structure and covering a portion of the isolation structure;

166. Ching discloses and renders obvious this limitation. For example, Ching discloses a “gate dielectric layer 50 and gate electrode 52.” Ex. 1005 at 4:39-40. Ching discloses that the “gate dielectric layer 50 is formed . . . on the top surfaces and the sidewalls of semiconductor fins 48” and a “conductive material 52 is formed over gate dielectric layer 50.” *Id.* at 4:42-44, 4:56-57. Thus, the “gate structure” comprising the “gate dielectric layer 50 and gate electrode 52” overlays the top surface and two side surfaces of “semiconductor fins 48,” which is a portion of the fin structure (“semiconductor strip 21”), and covers a portion of the “STI regions 22.”

167. A cross-section of the completed transistor in accordance with the 8E/9D embodiment is shown below, which shows the “gate structure” (gold) overlaying the

top surface and two side surfaces of a portion of “semiconductor strip 21” (blue) and covering a portion of the isolation structure, “STI regions 22” (magenta). Ex. 1005 at Fig. 9A.

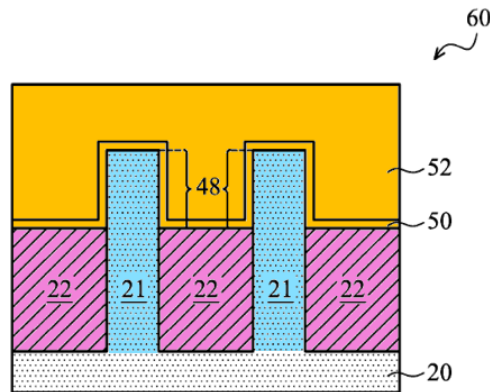


Fig. 9A

5. 1[c(ii)]: wherein the isolation structure under the gate structure has a first top surface and the isolation structure at two sides of the gate structure has a second top surface, and the first top surface is higher than the second top surface; and

168. Ching discloses and renders obvious this limitation. For example, Ching states:

It is observed that in the resulting FinFET 60, the portions of STI regions 22 that are on the opposite sides of a same gate electrode 52 (FIGS. 9B, 9C, and 9D) have top surfaces 22A that are either higher than, level with, or lower than, top surface 22B that are underlying (and aligned to) gate electrode 52.

Ex. 1005 at 5:26-31. As such, Ching discloses “top surface 22B that are underlying” the gate electrode (“a first top surface”) and “top surface 22A” on “the opposite sides of the same gate electrode” (“a second top surface”). *Id.* In one embodiment, top surface 22A (“the second top surface”) is “lower than” top surface 22B (“the first top

surface”). Ex. 1005 at 5:26-31. Conversely, that means “the first top surface is higher than the second top surface” as claimed. *Id.*

169. A cross-section of the completed transistor in accordance with the 8E/9D embodiment is shown below. The STI (magenta) under the gate structure (gold) has a “first top surface” 22B (red) and the STI (magenta) at two sides of the gate structure (gold) has a “second top surface” 22A (green), and the “first top surface” 22B (red) is higher than the “second top surface” 22A (green). *Id.* at Fig. 9D.

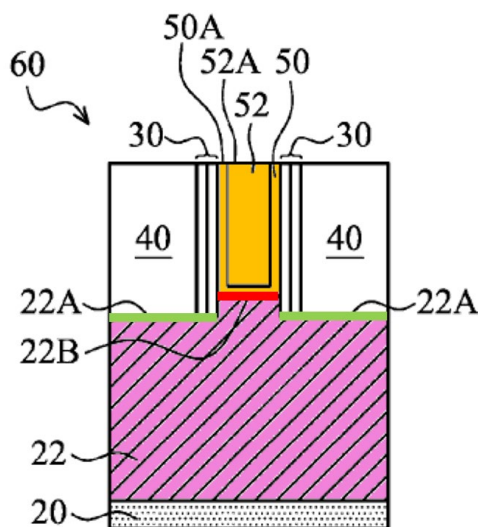


Fig. 9D

6. **1[d]: an epitaxial layer, disposed at one side of the gate structure and in direct contact with the fin structure.**

170. Ching discloses and renders obvious this limitation. During fabrication, portions of semiconductor strips 21 are recessed to form recesses 32, from which epitaxy regions 36 are selectively grown. Ex. 1005 at 3:20–32. These epitaxy regions

Figure 5. *Id.* at Fig. 5.

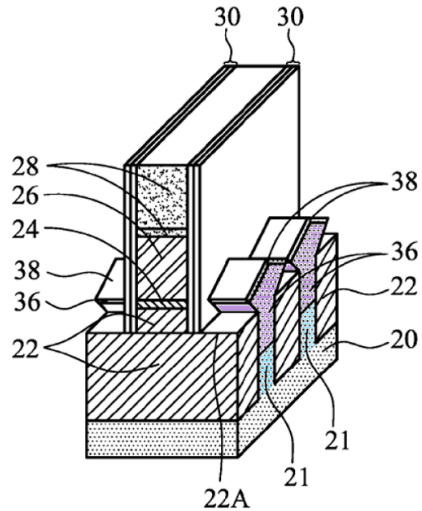


Fig. 5

171. As shown in Figure 5, epitaxy regions 36 are formed on both sides of the dummy gate and spacers. After gate replacement steps—removing the dummy gate and forming gate dielectric layer 50 and gate electrode 52 in recess 44 (id. at 4:42–57)—the epitaxy regions remain adjacent to the gate structure in the completed device, consistent with the claimed configuration. This is further evidenced by Ching’s description of the formation of contact plugs that couple to “silicide regions 38” which are formed on epitaxy regions 36, thereby disclosing the presence of these epitaxy regions in the completed device. *See* Ex. 1005 at 5:12-17.

B. Claim 3: The semiconductor device according to claim 1, wherein the gate structure is a metal gate structure

172. As discussed above, Ching discloses and renders obvious a semiconductor device in accordance with claim 1.

173. Ching further discloses and renders obvious the additional limitations of claim 3. For example, Ching discloses forming the gate via a “replacement-gate formation process.” Ex. 1005 at 5:10. This process involves first forming a “dummy polysilicon strip” that “is removed in an etching step, so that [a] recess is formed between opposite gate spacers 30.” *Id.* at 3:65-4:3.

174. The “dummy polysilicon strip” is then replaced by “conductive material 52” which “may comprise a metal-containing material such as TiN, TaN, TaC, Co, Ru, Al, combinations thereof, and multi-layers thereof.” *Id.* at 4:56-60. “Conductive material 52” forms part of “the replacement gate, which includes gate electrode 52 and [high-k] gate dielectric 50, respectively, of the resulting FinFET 60.” *Id.* at 4:65-5:3.

175. A POSITA therefore would have understood Ching as disclosing “a metal gate structure” as claimed at least because the “gate electrode 52” comprises “a metal-containing material” or even specifically enumerated metals (*i.e.*, Co, Ru, Al). Further, Ching’s disclosure of replacing “dummy polysilicon strip” with a “metal-containing material” for the gate electrode is consistent with the ’609 patent’s disclosure of “a high-k last replacement metal gate (RMG) process may be carried out

so that the gate structure composed of polysilicon inside may be replaced with a metal gate structure.” *Id.* at 7:12-15.

C. Claim 5: The semiconductor device according to claim 1, further comprising a recess formed at one end of the fin structure, wherein the epitaxial structure fills up the recess.

176. As discussed above, Ching discloses and renders obvious a semiconductor device in accordance with claim 1.

177. Ching further discloses and renders obvious the additional limitations of claim 5. For example, Ching discloses that “exposed portions of semiconductor strip 21 are recessed, for example, using anisotropic etching.” Ex. 1005 at 3:20-22. “The etching of semiconductor strips 21 may be continued until the top surfaces of semiconductor strips 21 are lower the top surfaces 22A of STI regions 22, forming recesses 32 in STI regions 22.” *Id.* at 3:24-27. As shown in Figure 4, “recesses 32” are formed at one end of “semiconductor strips 21,” which is a “fin structure” as discussed above. *Id.* at Fig. 4; *supra* 1[a].

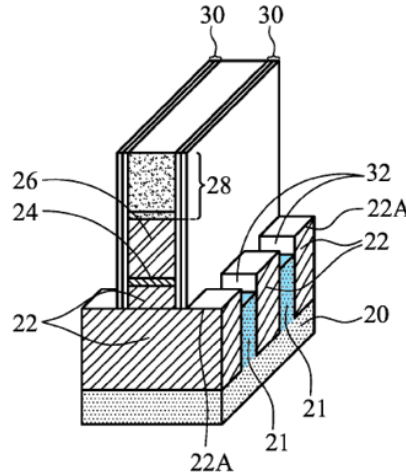


Fig. 4

178. For clarity, I note that Figure 4 contains an error where the spacers 30 are shown to extend down into the recesses 32. A POSITA would have understood that the etching of the fin structure 21 to form the recesses 32 would have exposed a side surface of fin structures 21 beneath the spacers 30. In fact, it is necessary to the operation of the device that fin structures 21 beneath the spacers and gate structure are exposed in order for carriers to be conducting across the channel between the source and drain regions. Ching confirms that subsequently grown epitaxy regions 36 (described further below) “form source and drain regions” (Ex. 1005 at 3:40-42) and therefore must interface with portions of the fin structures in the channel region. This error is not material to my opinions with respect to the Ching reference.

179. Next, “recesses 32” are filled by epitaxial structures. Ex. 1005 at 3:30-32. According to Ching, “epitaxy regions 36 are formed by selectively growing epitaxy regions 36 from recesses 32” and “recesses 32 are filled with epitaxy regions

the fin. Accordingly, and as shown in Figure 5 below, Ching discloses that the bottom surface (yellow line) of the epitaxial structure 36 is shallower than the bottom surface (red line) of the isolation structure 22. Ex. 1005 at Fig. 5.

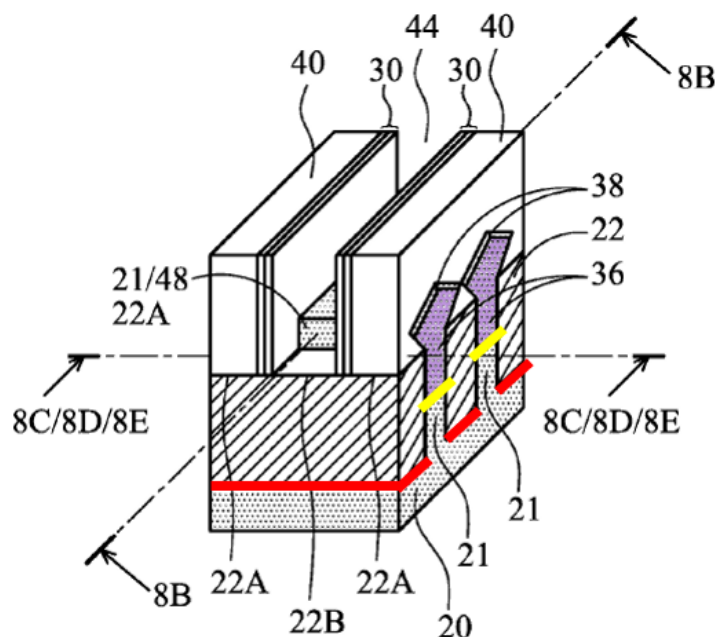


Fig. 8A

183. This is because, according to Ching, the bottom surface of the “Shallow Trench Isolation (STI) regions 22” extend “from a top surface of substrate 20.” *Id.* at 2:1-4. The bottom surfaces of the “epitaxy regions 36,” on the other hand, are formed “from recesses 32” at the top portions of “semiconductor strips 21,” above the “top surface of substrate 20.” *Id.* at 3:30-32.

E. Claim 8: The semiconductor device according to claim 1, wherein the epitaxial structure comprises silicon germanium, silicon phosphide or phosphor-doped silicon carbide.

184. As discussed above, Ching discloses and renders obvious a semiconductor device in accordance with claim 1.

185. Ching further discloses and renders obvious the additional limitations of claim 8. For example, Ching discloses that “[i]n some exemplary embodiments, epitaxy regions 36 comprise **silicon germanium** or silicon carbon.” Ex. 1005 at 3:32-33 (emphasis added).

F. Claim 9: The semiconductor device according to claim 1, further comprising a spacer disposed on a sidewall of the gate structure.

186. As discussed above, Ching discloses and renders obvious a semiconductor device in accordance with claim 1.

187. Ching further discloses and renders obvious the additional limitations of claim 9. For example, Ching discloses that “gate spacers 30 are formed on the sidewalls of hard mask strip 28 [and] polysilicon strip 26.” Ex. 1005 at 3:9-12. The “[g]ate spacers 30 are formed of dielectric materials.” Subsequently, “polysilicon strip 26 is removed in an etching step” and “hard mask layer 24 is removed,” resulting in “recess 44.” *Id.* at 3:65-4:9. As Ching recognizes, the “recess 44 is formed between opposite gate spacers 30,” as shown below in Figure 8A in dark blue. *Id.* at 3:65-67.

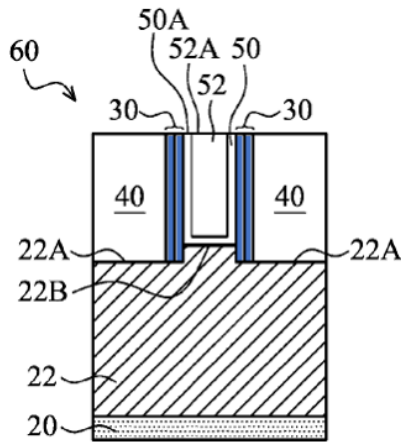


Fig. 9D

G. Claim 10

1. **10[pre]: The semiconductor device according to claim 1, further comprising:**

190. As discussed above, Ching discloses and renders obvious a semiconductor device in accordance with claim 1.

2. **10[a]: another epitaxial structure, disposed at another side of the gate structure and in direct contact with the fin structure; and**

191. Ching discloses and renders obvious this limitation.

192. Ching explicitly illustrates another epitaxial structure 36 (purple, below silicide 38) disposed at another side of the gate structure in Figure 5. Ex. 1005 at Fig. 5. A POSITA would have understood that the epitaxial structure 36 (purple) is also in “direct contact with” the “semiconductor strip 21” (a fin structure, as discussed above) because “epitaxy regions 36 are formed by selectively growing epitaxy regions

36 from recesses 32,” which are formed in the “semiconductor strip 21” on both sides of the gate structure. Ex. 1005 at 3:20-32:

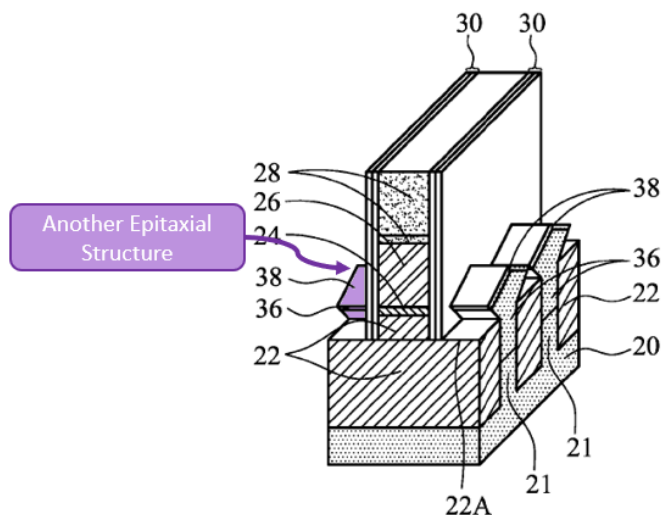


Fig. 5

Moreover, Ching’s “epitaxial structures 36” are “implanted to form source and drain regions.” Ex. 1005 at 3:40-42. A POSITA would have readily understood that the source and drain regions of a transistor are on opposite sides of the gate structure in a FinFET device. *See supra* V.A.

3. 10[b]: a channel region, contiguous to the top surface and the side surfaces of the fin structure, and between the epitaxial structure and said another epitaxial structure;

193. Ching discloses and renders obvious this limitation. As shown above for claim limitations 1[a] and 1[c(ii)], the gate structure overlays a top surface and two side surfaces of the fin structure. A POSITA would have understood this region of the fin structure to constitute a channel region. For example, Ching explicitly discloses that FinFETs have “increased channel widths” that are “achieved by forming channels

that include portions on the sidewalls of semiconductor fins and portions on the top surfaces of the semiconductor fins.” Ex. 1005 1:18-23. A POSITA would have therefore understood that the channel region of Ching is contiguous with the side surfaces and the top surface of the fins.

194. Further, as shown above for limitation [10a], the epitaxial structures 36 comprising the source and drain regions are on both sides of the gate. *See supra* 10[a]. Therefore, the channel region of the fins 21 beneath the gate is between the epitaxial structure (one of the source/drain) and said another epitaxial structure (the other of the source/drain). A POSITA would have understood that this configuration inherently establishes continuity between the fin channel and the epitaxially formed source and drain regions, because the epitaxial material is grown directly from the exposed fin surfaces following the formation of the recess. As such, there is no intervening layer or structural discontinuity that would prevent electrical connection — the source and drain are, by fabrication, extensions of the same semiconductor body as the fin.

195. Although the figures in Ching (e.g., Fig. 9D) show sidewall spacers adjacent to the gate, a POSITA would have understood that these spacers are dielectric and do not interrupt the electrical continuity between the source/drain regions and the underlying channel. Instead, the channel extends directly from the fin body beneath the gate into the fin portions in contact with the epitaxially grown source and drain. This continuity is essential for transistor operation, as carriers injected from the source

must traverse the channel to reach the drain. In fact, interrupting that continuity — for example, by inserting a barrier between the epitaxial region and the fin — would preclude normal device function. A POSITA would have immediately recognized that the spacers serve an isolation function only and are not positioned between the channel and the epitaxial regions along the transport path. Thus, even if not explicitly labeled in the figures, the fin region beneath the gate is electrically and structurally contiguous with the epitaxial source and drain regions on either side.

X. Ground 2B: Claims 2 And 4 Are Obvious Over Ching In View Of Xu

196. In my opinion, claims 2 and 4 would have been obvious to a POSITA over Ching in view of Xu.

A. Claim 2: The semiconductor device according to claim 1, wherein there is a height difference between the first top surface and second top surface, and the height difference ranges from 100 Angstroms to 250 Angstroms.

197. As discussed above, Ching discloses and renders obvious a semiconductor device in accordance with claim 1. Ching in view of Xu further renders obvious the additional limitations of claim 2.

198. For example, as discussed above with respect to claim element 1[c(ii)] and depicted in annotated Fig. 9D below, Ching discloses a vertical offset between the top surface of the isolation structure beneath the gate (red) and the top surface of isolation structure flanking the gate (green).

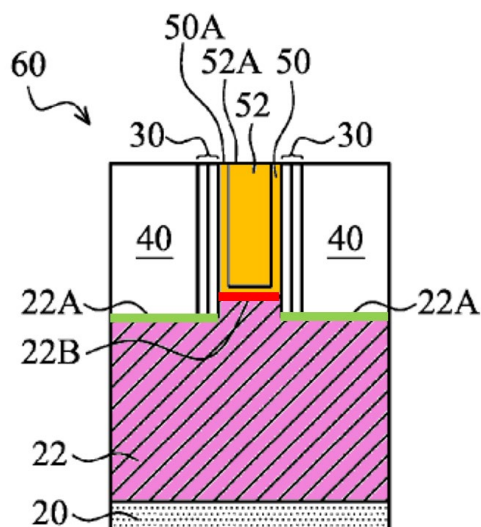


Fig. 9D

199.

200. Ching discloses that the vertical offset between the top surface of the isolation structure beneath the gate the isolation structure flanking the gate differentiates its FinFETs from conventional FinFETs. Ex. 1005 at 5:26-35. Ching differs from claim 2 only in that Ching does not explicitly disclose a numerical value for this vertical offset. Accordingly, a POSITA would have consulted additional prior art, including Xu, for dimensional guidance applicable to Ching's structure. Because both Ching and Xu employ selective etching of STI oxide to define fin height and improve gate wrapping, a POSITA would have found Xu's etch teachings directly relevant to controlling the same height difference described in Ching. Both Ching and Xu are directed to FinFET devices and fabrication methods (Ex. 1005 at 1:53-56; Ex. 1004 at 1:1-3) and are aimed at keeping up with the increasing down-scaling of integrated circuits and semiconductor devices (Ex. 1005 at 1:15-20; Ex. 1004 at 1:17-

22, 34-38). A POSITA would have been motivated to look to Xu and apply its dimensional guidance to the teachings of Ching based on these interrelated teachings, similar problems, and the known design demands in the industry.

201. Specifically, Xu discloses a height difference between the first top surface and second top surface of the “isolation features 130” that results from the “etching process” that “selectively etches the isolation features 130.” Ex. 1004 at 4:58-61. Xu further discloses that “in the depicted embodiment, the etching process uses a hydrofluoric acid (HF) etching solution of a suitable concentration (for example, 100:1)” and “the HF solution **recesses the isolation features 130 about 100 Å.**” *Id.* at 4:61-65 (emphases added).

202. The top surfaces of Ching’s etched isolation features 22 provide a surface for facets of the later-grown epitaxial structure. Ex. 1005 at 3:34-40. A POSITA would have understood that the etch-depth of the isolation features in combination with the depth of the fin-recess defines the starting substrate for epitaxial stressor growth. The recessed isolation surface thereby determines how effectively strain is transferred to the fin channel, which in turn impacts carrier mobility and drive current. As Xu discloses, the starting substrate, in turn, impacts the strain that can be achieved by the device. Ex. 1004 at 15:56-66. A POSITA therefore would have found it obvious to apply the isolation etch depth of Xu to the teachings of Ching in order to optimize

strain in the device, which enhances carrier mobility and improves device performance. Ex. 1004 at 15:56-66; 1:28-30.

203. Moreover, while Ching does not specify the numerical extent of the STI recess or the resulting height difference, Xu provides a concrete value for this parameter (*i.e.*, about 100 Angstroms), which overlaps the claimed range of between 100 Angstroms and 250 Angstroms. A POSITA would have understood that such a vertical offset in this range was well-known and routinely implemented in FinFET fabrication when recessing isolation structures surrounding fins. *See* Ex. 1006 at 4:62-5:1.

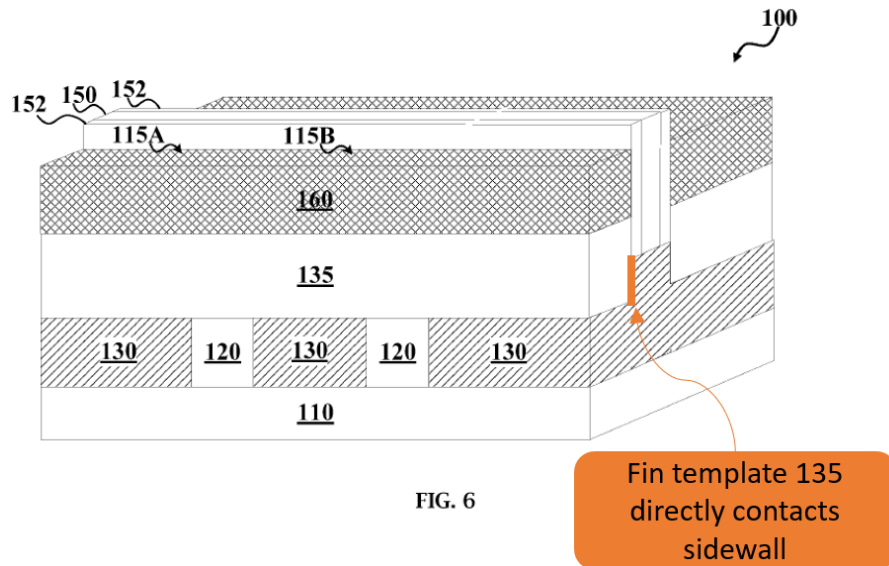
204. In my opinion, the '609 patent does not provide any evidence that the claimed range is critical or that it otherwise achieves unexpected results. A POSITA therefore would have been motivated to apply the teachings of Xu—which demonstrate that it was known in the prior art to incorporate a height difference overlapping the claimed range—to Ching and arrive at the claimed height difference with predictable results. Further, a POSITA would have had a reasonable expectation of success in doing so as Xu discloses an exemplary etch process that can be used to achieve the claimed height difference. Ex. 1004 at 4:61-65.

B. Claim 4: The semiconductor device according to claim 1, wherein the isolation structure under the gate structure comprises a sidewall and the epitaxial structure is in direct contact with the sidewall.

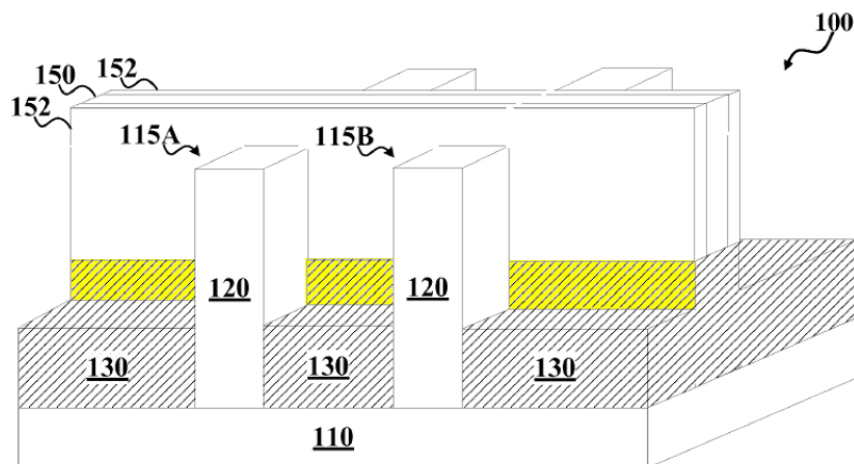
205. As discussed above for Ground 2A, Ching discloses and renders obvious the device of claim 1. Ching in view of Xu renders obvious claim 4.

206. Ching discloses the isolation structure under the gate structure comprises a sidewall. For example, as shown in Fig. 3, Ching's etching of the isolation structure recesses portions of STI regions 22 while leaving "un-recessed portions of STI regions 22" under the gate structure. Ex. 1005 at 3:9-12. Ching, however, does not teach a sidewall in direct contact with the epitaxial structure (because its gate spacers 30 are located between the relevant sidewall and the epitaxial structure). *Id.* at 2:59-3:19.

207. In contrast, Xu discloses the claimed direct contact. Specifically, Xu discloses the "fin template 135" (*i.e.*, the claimed "epitaxial structure") is in direct contact with the sidewall of the "isolation features 130" under the "gate structure 150," as shown in annotated Figure 6 below. Ex. 1004 at Fig. 6:



Xu achieves this result because it performs certain steps in a different order than Ching. Specifically, Xu applies “an etching process [] to recess isolation features 130” after gate spacers 152 are already formed. Ex. 1004 at 4:54-61. In doing so, the etching process exposes sidewalls of the isolation structure under the gate structure (yellow below) that directly abut the later-formed epitaxial structure:



208. It would have been obvious to a POSITA to apply the teachings of Xu to the teachings of Ching relative to the processing steps that result in the claimed direct contact. This is because, among other reasons, the processing steps applied in Xu provide advantages when forming the gate structure.

209. For example, a POSITA would have recognized that Ching's process of executing the STI recess etch before spacer formation exposes the sidewalls of the polysilicon strip 26 during etching. Ex. 1005 at 2:45-64. The POSITA would have understood that polysilicon strip is a "dummy polysilicon strip" used to preserve space for a later-formed gate electrode. Ex. 1005 at 3:65-4:3. Such "gate-last" schemes are advantageous because the "final metal gate is not exposed to the high activation anneal for the junctions." Ex. 1008 at 16. "As a result, a better controlled work function for nMOS and pMOS can be achieved." *Id.*

210. Accordingly, the POSITA would have found it obvious to modify Ching to perform gate spacer formation prior to etching the STI structure, as taught by Xu, in order to maintain the shape and alignment of the dummy gate for later replacement with a high-performance gate metal, thereby allowing for more reliable gate-last processing and its associated electrical advantages. *See* Ex. 1008 at 16.

211. As a result, the Ching-Xu combination would include portions of the STI of Ching exposed under the sidewall spacers, similar to the structure shown in Xu. Specifically, forming the sidewall spacers first ensures that the sidewalls do not extend

vertically below the original height of the STI. This principle is demonstrated in modified Fig. 2 of Xu, below:

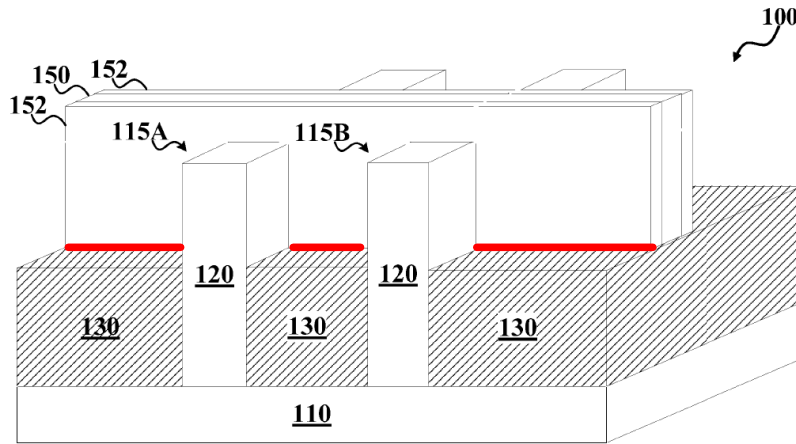


FIG. 2

When the etch occurs, portions of 130 directly underlying 152 are then exposed. Applying this feature to Ching would result in similar exposure of the portions of the STI underlying Ching's sidewall spacers. The modified figures below show the exposed isolation structure of Xu (yellow) and the corresponding exposed STI in the combination of Ching and Xu:

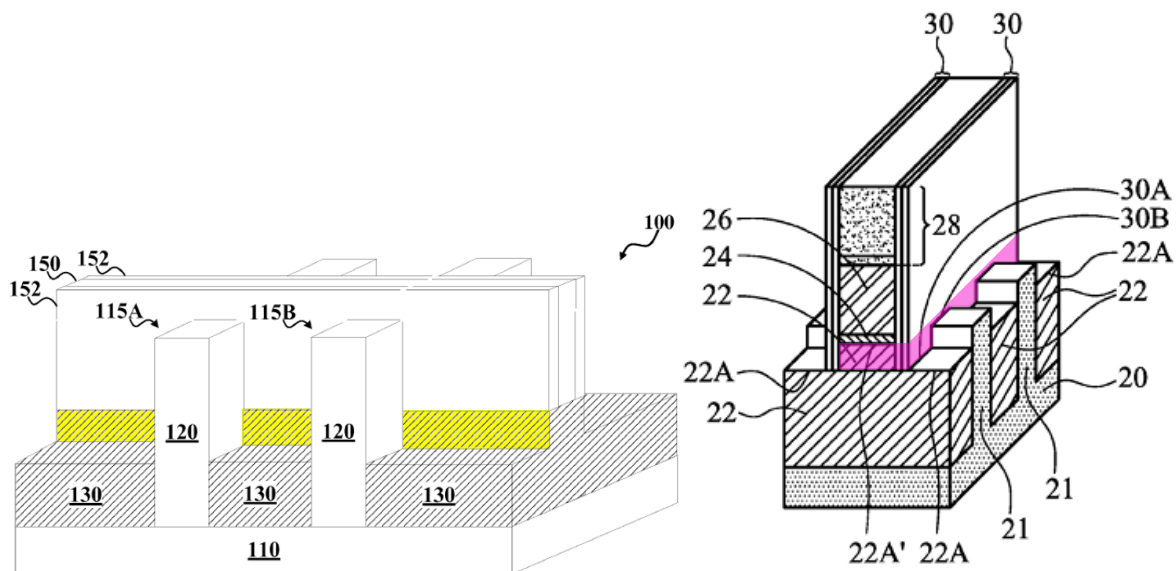


FIG. 3

Fig. 3

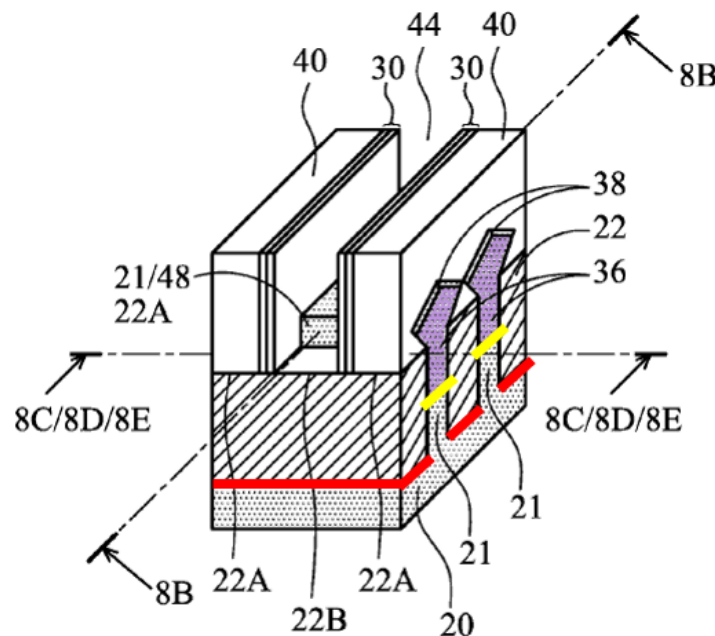
212. A POSITA would have understood that the Ching-Xu combination would then undergo the processing steps as taught by Ching, resulting in epitaxial structures 36 directly contacting the exposed sidewalls of the STI under the gate structure, as claimed. Moreover, a POSITA would have found it obvious to make this modification and had a reasonable expectation of success in doing so because the combination involves no more than changing the sequence of steps of Ching. Both the deposition of gate sidewall spacers and the isolation etch are well-known, conventional processes that a POSITA would have been able to perform in either order, and performing the sidewall deposition first does not achieve any unexpected results. Accordingly, reordering these steps would have been obvious to a POSITA.

213. In my opinion, claim 7 would have been obvious to a POSITA over Ching in view of Huang.

A. Claim 7: semiconductor device according to claim 6, wherein there is a height difference between the bottom surface of the epitaxial structure and the bottom surface of the isolation structure, and the height difference ranges from 100 Angstroms to 250 Angstroms.

214. As discussed above, Ching discloses and renders obvious the fabrication method of claim 1. Ching in view of Huang renders obvious claim 7.

215. As further discussed above with respect to claim 6, Ching discloses the bottom surface of the epitaxial structure (yellow) is shallower than the bottom surface of the isolation structure (red):



Ex. 1005 at Fig. 8A (modified).

216. Ching differs from claim 7 only in that Ching does not explicitly disclose specific numerical values for the depth of the recess or the dimensions of the surrounding features. A POSITA would have understood that this recess depth is a results-effective variable that can be used to tailor strain induced on the FinFET channel and optimize performance. *See* Ex. 1004 at 10:34-47, 15:67-16:4 (disclosing tuning the trench depth to optimize strain in the device). Moreover, Ching discloses an example etch technique that can be used to achieve this recess (Ex. 1005 at 3:20-29) and a POSITA would have been familiar with ways to tune etch depths and profiles. *See* Ex. 1025 at Chapters 21-22. A POSITA therefore would have found it obvious to optimize the etch depth through routine experimentation to yield a desired strain.

217. In doing so, a POSITA would have found it obvious to turn to additional prior art, such as Huang for guidance concerning the recess depth. Both Ching and Huang are directed to FinFET devices and methods (Ex. 1005 at 1:53-56; Ex. 1006 at 2:1-4) and are aimed at keeping up with the increasing down-scaling of integrated circuits and semiconductor devices (Ex. 1005 at 1:15-20; Ex. 1006 at 1:6-9). A POSITA would have been motivated to look to Huang and apply its dimensional guidance to the teachings of Ching based on these interrelated teachings, similar problems, and the known design demands in the industry.

218. As described above, Huang discloses dimensions for a height difference between the bottom surface Huang's dielectric layers and the bottom surface of an epitaxial structure formed over the remaining semiconductor strip. See Ex. 1006 at 2:55-59, 4:30-32, Fig. 4B; Section V.B., *supra*. In particular, Huang discloses a height difference of between 5 nm and 475 nm, which entirely encompasses the claimed range of from 100 Angstroms to 250 Angstroms. Ex. 1006 at 1:15-16. As described above in Section VIII.B., *supra*, and incorporated herein by reference, the '609 Patent provides no evidence of criticality of the claimed range. *Id.* Accordingly, it would have been obvious to a POSITA to optimize the height difference through routine experimentation and arrive at the claimed height difference. The POSITA would have had a reasonable expectation of success in doing so given the desirability of the lower range of Huang (*see* Ex. 1005 at 1:15-20; Ex. 1006 at 1:6-9) and Huang's disclosure of exemplary etch processes that can be used to achieve the claimed height difference (Ex. 1006 at 2:45-67, 4:10-29).

219. A POSITA also would have found it obvious and been motivated to apply the height difference of Huang to the teachings of Ching and arrive at the claimed height difference due to the overlap between the claimed range and the range disclosed by Huang. Huang's disclosure of a larger range than that which is claimed does not mitigate the obviousness of the claimed range for the same reasons set forth in Section VIII.B., *supra*. *See also* Ex. 1005 at 1:15-16 (describing "the increasing

down-scaling of integrated circuits). The POSITA would have been motivated and had a reasonable expectation of success in arriving at the claimed range because it lies within the lower end of Huang's disclosed range which is more desirable given its applicability to smaller-scale devices with increased density and because the prior art discloses etch processes that can be used to achieve that depth. Ex. 1006 at 2:45-67, 4:10-29.

XII. Conclusion

220. As set forth above, it is my opinion that the Challenged Claims of the '609 Patent are unpatentable because they are rendered obvious by the prior art.

221. In signing this declaration, I recognize that the declaration will be filed as evidence in a contested proceeding before the Patent Trial and Appeal Board of the United States Patent and Trademark Office. I also recognize that I may be subject to cross-examination in the proceeding and that cross-examination will take place within the United States. If cross-examination is required of me, I will appear for cross-examination within the United States during the time allotted for cross-examination.

222. I reserve the right to supplement my opinions in the future to respond to any arguments that Patent owner raises and to account for new information as it becomes available to me.

223. I declare that all statements made herein on my own knowledge are true and that all statements made on information and belief are believed to be true, and

further, that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Date: November 14, 2025

By: _____
Jack Lee, Ph. D.