UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/597,115	04/16/2019	10263108	2014-0937/24061.2998	8745

42717 7590 03/27/2019

HAYNES AND BOONE, LLP
IP Section
2323 Victory Avenue
Suite 700
Dallas, TX 75219

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Chun Hsiung Tsai, Hsinchu County, TAIWAN;
Taiwan Semiconductor Manufacturing Company, Ltd., Hsin-Chu, TAIWAN;
Yuan-Ko Hwang, Hsinchu City, TAIWAN;

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The USA offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to encourage and facilitate business investment. To learn more about why the USA is the best country in the world to develop technology, manufacture products, and grow your business, visit SelectUSA.gov.

In place of PTO-1449 Form	U. S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE			*Complete if Known*	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(use as many sheets as necessary)*				Application Number	14/597,115
				Filing Date	January 14, 2015
				First Inventor Name	Chun Hsiung TSAI
				Art Unit	2896
				Examiner Name	SPALLA, DAVID C
SHEET	1	OF	1	Attorney Docket Number	2014-0937/24061.2998

U. S. PATENTS				
Examiner's Initials	Cite No.	Document Number	Issue Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document
	A1	8853039	10-07-2014	Tsai et al.
	A2	9885123	02-06-2018	Halpin et al.

U. S. PATENT APPLICATION PUBLICATIONS				
Examiner's Initials	Cite No.	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document

FOREIGN PATENT DOCUMENTS					
Examiner's Initials	Cite No.	Foreign Patent Document (Country Code – Number – Kind)	Publication Date MM-DD-YYYY	Patentee or Applicant of Cited Document	Translation Y/N

NON-PATENT LITERATURE DOCUMENTS		
Examiner's Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article, title of the item, date, page(s), volume-issue number(s), publisher, city/country where published

Examiner Signature		Date Considered	

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include a copy of this form with next communication to applicant.

Electronic Acknowledgement Receipt

EFS ID:	35540590
Application Number:	14597115
International Application Number:	
Confirmation Number:	8745
Title of Invention:	Metal-Insensitive Epitaxy Formation
First Named Inventor/Applicant Name:	Chun Hsiung Tsai
Customer Number:	42717
Filer:	Michael Edward Ramon/Janie Martinez-Holm
Filer Authorized By:	Michael Edward Ramon
Attorney Docket Number:	2014-0937/24061.2998
Receipt Date:	27-MAR-2019
Filing Date:	14-JAN-2015
Time Stamp:	10:42:22
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal Letter	24061-2998_SupplementalIDS-4_Transmittal.pdf	34169 051ff1f53f5cf43d4fde42b027309d714536dbe9	no	2

Warnings:

Information:					
2	Information Disclosure Statement (IDS) Form (SB08)	24061-2998_SupplementalIDS-4_1449.pdf	24138 0d3171fe1508303acdf144766bc72142bceef7d9	no	1

Warnings:
Information:
This is not an USPTO supplied IDS fillable form

Total Files Size (in bytes):	58307

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	§	Dkt No.: 2014-0937 / 24061.2998
	§	
Chun Hsiung TSAI, *et al*	§	
	§	Group Art Unit: 2896
Application No.: 14/597,115	§	
	§	Examiner: Spalla, David C.
Filing Date: January 14, 2015	§	
	§	Confirmation No.: 8745
Entitled: Metal-Insensitive Epitaxy Formation	§	
	§	

INFORMATION DISCLOSURE STATEMENT

Via EFS-Web
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In compliance with the duty of disclosure under 37 CFR §1.56, and in accordance with the practice under 37 CFR §1.97 and §1.98, the Examiner's attention is directed to the documents listed on the enclosed modified Form PTO-1449.

No inference should be made that the cited references are in fact material, are in fact prior art, or that no better art exists. The cited patents are listed in numerical order and are not in any order based on their pertinence.

Pursuant to 37 CFR § 1.98(a)(2)(i), copies of the U.S. patent documents listed on the enclosed modified Form PTO-1449 are not attached.

This Information Disclosure Statement is being filed after the mailing date of a Notice of Allowance under §1.311 and after payment of the Issue Fee. The Applicants kindly request the attached documents be entered to the record.

The Commissioner is hereby authorized to charge any additional fees which may be required or credit any overpayment to Deposit Account No. 08-1394.

Respectfully submitted,

/Michael E. Ramon/

Michael E. Ramon
Registration No. 52,147

Dated: March 27, 2019

Haynes and Boone, LLP
2323 Victory Avenue, Suite 700
Dallas, Texas 75219
Telephone: 512.867.8528
Facsimile: 214.200.0853
ipdocketing@haynesboone.com

CERTIFICATE OF TRANSMISSION

I hereby certify that this correspondence is being transmitted to the United States Patent and Trademark Office, via EFS-Web, on the date indicated below:

on 3/27/19

/Janie Martinez-Holm/
Janie Martinez-Holm

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via EFS-Web.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

42717 7590 12/05/2018
HAYNES AND BOONE, LLP
IP Section
2323 Victory Avenue
Suite 700
Dallas, TX 75219

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission via EFS-Web

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via EFS-Web or by facsimile to (571) 273-2885, on the date below.

Krista Myrick	(Typed or printed name)
/Krista Myrick/	(Signature)
March 4, 2019	(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/597,115	01/14/2015	Chun Hsiung Tsai	2014-0937/24061.2998	8745

TITLE OF INVENTION: Metal-Insensitive Epitaxy Formation

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1000	$0.00	$0.00	$1000	03/05/2019

EXAMINER	ART UNIT	CLASS-SUBCLASS
SPALLA, DAVID C	2896	257-192000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-09 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 Haynes and Boone, LLP
2
3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: Taiwan Semiconductor Manufacturing Company, Ltd.

(B) RESIDENCE: (CITY and STATE OR COUNTRY): Hsin-Chu, Taiwan

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. Fees submitted: ☒ Issue Fee ☐ Publication Fee (if required) ☐ Advance Order - # of Copies _____

4b. Method of Payment: *(Please first reapply any previously paid fee shown above)*

☒ Electronic Payment via EFS-Web ☐ Enclosed check ☐ Non-electronic payment by credit card (Attach form PTO-2038)

☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. 08-1394

5. **Change in Entity Status** (from status indicated above)

☐ Applicant certifying micro entity status. See 37 CFR 1.29

☐ Applicant asserting small entity status. See 37 CFR 1.27

☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature /David M. O'Dell/ Date March 4, 2019

Typed or printed name David M. O'Dell Registration No. 42,044

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of: Chun Hsiung Tsai *et al.*	§	Docket No.: 2014-0937/24061.2998
	§	
Application No. 14/597,115	§	Art Unit: 2896
	§	
Filing Date: January 14, 2015	§	Examiner: Spalla, David C.
	§	
Entitled: METAL-INSENSITIVE EPITAXY FORMATION	§	Confirmation No.: 8745
	§	

COMMENTS ON STATEMENT OF REASONS FOR ALLOWANCE

In response to Examiner's Statement of Reasons for Allowance, Applicant agrees that the claims as allowed are patentably distinct over the cited art. Applicant further respectfully submits that it is the combination of all claim elements that comprehensively distinguish the claimed invention over the prior art.

Respectfully submitted,

/Michael E. Ramon/

Michael E. Ramon
Registration No. 52,147

Dated: March 4, 2019

Haynes and Boone, LLP
2323 Victory Avenue, Suite 700
Dallas, Texas 75219
Telephone: 512.867.8426
Facsimile: 214.200.0853

CERTIFICATE OF TRANSMISSION

I hereby certify that this correspondence and any attachments are being transmitted to the United States Patent and Trademark Office, via EFS-Web, on March 4, 2019.

/ Krista Myrick /

Krista Myrick

Electronic Patent Application Fee Transmittal

Application Number:	14597115
Filing Date:	14-Jan-2015
Title of Invention:	Metal-Insensitive Epitaxy Formation
First Named Inventor/Applicant Name:	Chun Hsiung Tsai
Filer:	David M. Odell/Krista Myrick
Attorney Docket Number:	2014-0937/24061.2998

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
UTILITY APPL ISSUE FEE	1501	1	1000	1000

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**1000**

Electronic Acknowledgement Receipt

EFS ID:	35316085
Application Number:	14597115
International Application Number:	
Confirmation Number:	8745
Title of Invention:	Metal-Insensitive Epitaxy Formation
First Named Inventor/Applicant Name:	Chun Hsiung Tsai
Customer Number:	42717
Filer:	David M. Odell/Krista Myrick
Filer Authorized By:	David M. Odell
Attorney Docket Number:	2014-0937/24061.2998
Receipt Date:	04-MAR-2019
Filing Date:	14-JAN-2015
Time Stamp:	15:56:40
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$1000
RAM confirmation Number	030519INTEFSW15572900
Deposit Account	
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	24061-2998_issuefee_signed.pdf	178113 e6541b548091b3db4db465be684fd4a6e9b7b7b8	no	1
Warnings:					
Information:					
2	Post Allowance Communication - Incoming	24061-2998_Comments.pdf	25964 de27fa60c9086015e7e916f16dc3bad7c99cd0c4	no	1
Warnings:					
Information:					
3	Fee Worksheet (SB06)	fee-info.pdf	30382 e20458087d9a851bb7b0ec56496858a482c712c5	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	234459		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

42717 7590 12/05/2018

HAYNES AND BOONE, LLP
IP Section
2323 Victory Avenue
Suite 700
Dallas, TX 75219

EXAMINER
SPALLA, DAVID C

ART UNIT	PAPER NUMBER
2896	

DATE MAILED: 12/05/2018

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/597,115	01/14/2015	Chun Hsiung Tsai	2014-0937/24061.2998	8745

TITLE OF INVENTION: Metal-Insensitive Epitaxy Formation

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1000	$0.00	$0.00	$1000	03/05/2019

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Maintenance fees are due in utility patents issuing on applications filed on or after Dec. 12, 1980. It is patentee's responsibility to ensure timely payment of maintenance fees when due. More information is available at www.uspto.gov/PatentMaintenanceFees.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via EFS-Web.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

42717 7590 12/05/2018

HAYNES AND BOONE, LLP
IP Section
2323 Victory Avenue
Suite 700
Dallas, TX 75219

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via EFS-Web or by facsimile to (571) 273-2885, on the date below.

(Typed or printed name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/597,115	01/14/2015	Chun Hsiung Tsai	2014-0937/24061.2998	8745

TITLE OF INVENTION: Metal-Insensitive Epitaxy Formation

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1000	$0.00	$0.00	$1000	03/05/2019

EXAMINER	ART UNIT	CLASS-SUBCLASS
SPALLA, DAVID C	2896	257-192000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-09 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____

2 _____

3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. Fees submitted: ❑ Issue Fee ❑ Publication Fee (if required) ❑ Advance Order - # of Copies _____

4b. Method of Payment: *(Please first reapply any previously paid fee shown above)*

❑ Electronic Payment via EFS-Web ❑ Enclosed check ❑ Non-electronic payment by credit card (Attach form PTO-2038)

❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. _____

5. **Change in Entity Status** (from status indicated above)

❑ Applicant certifying micro entity status. See 37 CFR 1.29

❑ Applicant asserting small entity status. See 37 CFR 1.27

❑ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/597,115	01/14/2015	Chun Hsiung Tsai	2014-0937/24061.2998	8745

42717 7590 12/05/2018

HAYNES AND BOONE, LLP
IP Section
2323 Victory Avenue
Suite 700
Dallas, TX 75219

EXAMINER	
SPALLA, DAVID C	

ART UNIT	PAPER NUMBER
2896	

DATE MAILED: 12/05/2018

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 14/597,115	Applicant(s) Tsai et al.	
	Examiner DAVID C SPALLA	Art Unit 2896	AIA Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☑ This communication is responsive to the AFCP filed on 11/13/2018.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☑ The allowed claim(s) is/are 1-10,12-20 and 27-36 . As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see **http://www.uspto.gov/patents/init_events/pph/index.jsp** or send an inquiry to **PPHfeedback@uspto.gov.**

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some *c) ☐ None of the:

   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____ .

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file areply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____ .

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____.
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material _____.
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date. _____.
5. ☐ Examiner's Amendment/Comment
6. ☑ Examiner's Statement of Reasons for Allowance
7. ☑ Other PTO-2323.

/DAVID C SPALLA/
Primary Examiner, Art Unit 2896

DETAILED ACTION

Allowable Subject Matter

Claims 1-10, 12-20 and 27-36 are allowed.

The following is an examiner's statement of reasons for allowance:

Claims 1, 15 and 27 disclose *inter alia* a method of epitaxially growing a second semiconductor material in source and drain regions for a FET, using a cyclic deposition and etching process having a first deposition step and a second deposition step, wherein the first deposition step and the second deposition step are performed at different temperatures.

US 2014/0264348 was relied on, in previous rejections, for showing a CDE process having different temperatures for deposition steps. However, Applicant has overcome the reference by establishing, in the remarks filed on 10/04/2017, that, not later than the effective filing date of the claimed invention, the subject matter disclosed and the claimed invention were either owned by the same person or subject to an obligation of assignment to the same person or subject to a joint research agreement. Thus, the reference is not available as art.

A search of relevant references in the art does not show Applicant's method to be obvious or anticipated. Claims 2-10, 12-14, 16-20 and 28-36 depend on one of Claims 1, 15 or 27 and are allowable for at least the reasons above.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DAVID C SPALLA whose telephone number is (303)297-4298. The examiner can normally be reached on Mon-Fri 10am-5pm MST.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steven Loke can be reached on (571) 272-1657. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/DAVID C SPALLA/
Primary Examiner, Art Unit 2896

AFCP 2.0 Decision

Application No.	Applicant(s)	
14/597,115	Tsai et al.	
Examiner	**Art Unit**	**AIA Status**
DAVID C SPALLA	2896	Yes

This is in response to the After Final Consideration Pilot request filed 13 November 2018.

1. **Improper Request** – The AFCP 2.0 request is improper for the following reason(s) and the after final amendment submitted with the request will be treated under pre-pilot procedure.

   ☐ An AFCP 2.0 request form PTO/SB/434 (or equivalent document) was not submitted.

   ☐ A non-broadening amendment to at least one independent claim was not submitted.

   ☐ A proper AFCP 2.0 request was submitted in response to the most recent final rejection.

   ☐ Other: _____

2. **Proper Request**

   A. After final amendment submitted with the request will not be treated under AFCP 2.0.
   The after final amendment cannot be reviewed and a search conducted within the guidelines of the pilot program.

   ☐ The after final amendment will be treated under pre-pilot procedure.

   B. Updated search and/or completed additional consideration.
   The examiner performed an updated search and/or completed additional consideration of the after final amendment within the time authorized for the pilot program. The result(s) of the updated search and/or completed additional consideration are:

   ☑ 1. All of the rejections in the most recent final Office action are overcome and a Notice of Allowance is issued herewith.

   ☐ 2. The after final amendment would not overcome all of the rejections in the most recent final Office action . See attached interview summary for further details.

   ☐ 3. The after final amendment was reviewed, and it raises a new issue(s). See attached interview summary for further details.

   ☐ 4. The after final amendment raises new issues, but would overcome all of the rejections in the most recent final Office action. A decision on determining allowability could not be made within the guidelines of the pilot. See attached interview summary for further details, including any newly discovered prior art.

   ☐ 5. Other: _____

   Examiner Note: Please attach an interview summary when necessary as described above.

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14/597,115	Tsai et al.
	Examiner	Art Unit
	DAVID C SPALLA	2896

CPC - Searched*		
Symbol	Date	Examiner
H01L 29/66636, 7848	06/23/2016	DCS
H01L 29/165, 167	12/11/2017	DCS
H01L 29/784, 66636, 66628	07/07/2018	DCS

CPC Combination Sets - Searched*		
Symbol	Date	Examiner

US Classification - Searched*			
Class	Subclass	Date	Examiner

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	Date	Examiner
Search of submitted IDS references	06/23/2016	DCS
See attached EAST search history	06/23/2016	DCS
See attached EAST updated search history	04/30/2017	DCS
See attached EAST updated search history	12/11/2017	DCS
Search of submitted IDS references	07/07/2018	DCS
See attached EAST updated search history	07/07/2018	DCS
Interference Search	11/30/2018	DCS
See attached EAST updated search history	11/30/2018	DCS

/DAVID C SPALLA/ Primary Examiner, Art Unit 2896	

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14/597,115	Tsai et al.
	Examiner	Art Unit
	DAVID C SPALLA	2896

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner
H01L 29	7848, 66636, 66628	11/30/2018	DCS

/DAVID C SPALLA/ Primary Examiner, Art Unit 2896	

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14/597,115	Tsai et al.
	Examiner	**Art Unit**
	DAVID C SPALLA	2896

CPC						
Symbol					**Type**	**Version**
H01L	/	29	/	7848	F	2013-01-01
H01L	/	29	/	165	I	2013-01-01
H01L	/	21	/	02447	I	2013-01-01
H01L	/	21	/	0245	I	2013-01-01
H01L	/	21	/	02529	I	2013-01-01
H01L	/	21	/	02532	I	2013-01-01
H01L	/	21	/	02576	I	2013-01-01
H01L	/	21	/	02579	I	2013-01-01
H01L	/	21	/	0262	I	2013-01-01
H01L	/	21	/	02639	I	2013-01-01
H01L	/	29	/	66545	I	2013-01-01
H01L	/	29	/	6659	I	2013-01-01
H01L	/	29	/	66636	I	2013-01-01
H01L	/	29	/	7833	I	2013-01-01
H01L	/	29	/	7834	A	2013-01-01

CPC Combination Sets								
Symbol					**Type**	**Set**	**Ranking**	**Version**
	/		/					

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	29	
/DAVID C SPALLA/ Primary Examiner, Art Unit 2896	30 November 2018	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	Fig. 5A

U.S. Patent and Trademark Office

Part of Paper No.: 20181130

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14/597,115	Tsai et al.
	Examiner	Art Unit
	DAVID C SPALLA	2896

INTERNATIONAL CLASSIFICATION				
CLAIMED				
H01L	/	29	/	78
H01L	/	21	/	02
H01L	/	21	/	04
H01L	/	21	/	3065
H01L	/	29	/	16
H01L	/	29	/	165

NON-CLAIMED				
	/		/	

US ORIGINAL CLASSIFICATION	
CLASS	SUBCLASS
438	498

CROSS REFERENCES(S)						
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)					
257	192					

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	29	
/DAVID C SPALLA/ Primary Examiner, Art Unit 2896	30 November 2018	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	Fig. 5A

U.S. Patent and Trademark Office

Part of Paper No.: 20181130

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14/597,115	Tsai et al.
	Examiner	**Art Unit**
	DAVID C SPALLA	2896

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIMS

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1	10	10	20	19	24	28								
2	2		11	21	20	25	29								
3	3	11	12		21	26	30								
4	4	12	13		22	27	31								
5	5	13	14		23	28	32								
6	6	16	15		24	14	33								
7	7	17	16		25	29	34								
8	8	18	17		26	15	35								
9	9	19	18	23	27	22	36								

NONE (Assistant Examiner)	(Date)	**Total Claims Allowed:** 29
/DAVID C SPALLA/ Primary Examiner, Art Unit 2896 (Primary Examiner)	30 November 2018 (Date)	O.G. Print Claim(s): 1 O.G. Print Figure: Fig. 5A

U.S. Patent and Trademark Office

Part of Paper No.: 20181130

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	27	(US-20030136985-$ or US-20150236157-$ or US-20130049101-$ or US-20080315254-$ or US-20140197455-$ or US-20140246710-$ or US-20140264348-$ or US-20060234504-$ or US-20120295427-$ or US-20090104739-$ or US-20060115933-$ or US-20070249168-$ or US-20100093147-$ or US-20140197493-$ or US-20140264636-$ or US-20120091469-$ or US-20130183814-$ or US-20150155386-$ or US-20070287272-$ or US-20080182075-$ or US-20150069466-$ or US-20120132957-$ or US-20100163939-$ or US-20110027955-$ or US-20140091308-$).did. or (US-8785285-$ or US-9064892-$).did.	US-PGPUB; USPAT	OR	OFF	2018/11/30 14:24
L2	1	"14597115"	US-PGPUB; USPAT; USOCR	OR	OFF	2018/11/30 14:24
S2	10680640	@ad<"20140822" @rlad<"20140822" @pt1d<"20140822"	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/13 10:07
S3	0	"14813556"	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/13 10:46
S4	1	"14597115"	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/13 13:33
S7	10680640	@ad<"20140822" @rlad<"20140822" @pt1d<"20140822"	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/13 13:36
S9	15	("7667271" | "8362575" | "8367498" | "8440517" | "8497528" | "8610240" | "8680576" | "8723272" | "8729634" | "8785285" | "8796759" | "8809139" | "8828823" | "8836016" | "8841701").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/13 13:41
S10	24	("20030052406" | "20060057859" | "20070059875" | "20070111439" | "20070128782" | "20070131969" | "20070145487" | "20080044960" | "20080251851" | "20090239344" | "20090280612" | "20100252816" | "20110147828" | "20120068193" |	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/13 13:44

		"20120104470" | "3909304" | "7112848" | "7132338" | "7518196" | "7910415" | "8110486" | "8338259").PN. OR ("8785285").URPN.				
S12	9538	fluorine adj3 (plasma treatment)	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/13 13:53
S14	10680640	@ad<"20140822" @rlad<"20140822" @pt1d<"20140822"	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/13 14:05
S15	4124	H01L29/66636.cpc.	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/13 14:05
S16	1731	S14 and S15 and ((silicon adj carbide) SiC) and ((silicon adj germanium) SiGe)	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/13 14:05
S17	31	S16 and (fluorine adj3 (plasma treat$4 clean$3))	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/13 14:12
S18	700	S14 and S15 and ((silicon adj carbide) SiC) and ((second upper) with ((silicon adj germanium) SiGe))	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/13 14:23
S19	260	S18 and (treat$3 clean$3)	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/13 14:27
S20	10686366	@ad<"20140822" @rlad<"20140822" @pt1d<"20140822"	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/15 15:31
S21	4131	H01L29/66636.cpc.	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/15 15:31
S22	103	S20 and S21 and (non-selective)	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/15 15:31
S23	2	S20 and S21 and ((non-selective) same precursor same (SiC (silicon adj2 carbide)))	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/15 15:39
S24	94	H01L29/66636.cpc. and (SiC same dop$3 same (prevent block$3 barrier diffusion))	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/17 17:53
S25	10690365	@ad<"20140822" @rlad<"20140822" @pt1d<"20140822"	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/17 18:16
S26	4134	H01L29/66636.cpc.	US-PGPUB; USPAT;	OR	ON	2016/06/17 18:16

			USOCR			
S27	5	S25 and S26 and ((non-selective) same cycle)	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/17 18:16
S28	9	S25 and S26 and ((non-selective) same (cyclic cycle))	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/17 18:18
S29	120	S25 and S26 and ((cyclic cycle) same (vary$3 chang$3 alter$3 rate factor))	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/17 18:19
S30	44	S25 and S26 and (((cyclic cycle) adj3 deposit$3) same (vary$3 chang$3 alter$3 rate factor))	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/17 18:20
S31	24	S25 and S26 and (((cyclic cycle) adj3 deposit$3) same (vary$3 chang$3 alter$3 rate factor)) and (degree celsius)	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/17 18:24
S32	0	S25 and S26 and (((cyclic cycle) adj3 deposit$3) same (vary$3 chang$3 alter$3 rate factor)) and ".degree."	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/17 18:30
S33	24	S25 and S26 and (((cyclic cycle) adj3 deposit$3) same (vary$3 chang$3 alter$3 rate factor)) and degree	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/17 18:31
S34	40	S25 and S26 and (((cyclic cycle) adj3 deposit$3) same (vary$3 chang$3 alter$3 rate factor)) and $4degree	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/17 18:31
S35	2	"20060234504"	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/21 15:48
S36	2	"20130328126"	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/21 15:55
S37	10698055	@ad<"20140822" @rlad<"20140822" @pt1d<"20140822"	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/23 16:27
S38	2137	S37 and (((cyclic cycle) adj3 deposit$3) same (vary$3 chang$3 alter$3 rate factor))	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/23 16:27
S39	3183	S37 and ((((cyclic cycle) adj3 deposit$3) CDE) same (vary$3 chang$3 alter$3 rate factor))	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/23 16:28
S40	661	S37 and ((((cyclic cycle) adj3 deposit$3) CDE) same (vary$3 chang$3 alter$3 rate factor)) and ((((cyclic cycle) adj3 deposit$3) CDE) same $4degree)	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/23 16:29
S42	335	S37 and ((((cyclic cycle) adj3 deposit$3)	US-	OR	ON	2016/06/23

		CDE) same (vary$3 chang$3 alter$3 rate factor)) and ((((cyclic cycle) adj3 deposit$3) CDE) same $4degree) and ((source drain source/drain s/d) with (deposit$3 epitax$5))	PGPUB; USPAT; USOCR			16:32
S43	9	S37 and (((cyclic cycle) adj3 deposit$3) CDE) with (non-selective (non adj selective)) with selective	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/23 16:51
S45	18	S37 and ((((cyclic cycle) adj3 deposit$3) CDE) same (non-selective (non adj selective)) same selective)	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/23 16:52
S46	98695	S37 and ((fluorine fluoride) with (treat$4 clean$3 process))	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/23 17:18
S47	4157	H01L29/66636.cpc.	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/23 17:19
S48	258	S37 and ((fluorine fluoride) with (treat$4 clean$3 process)) and S47	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/23 17:19
S49	86	S37 and ((fluorine fluoride) with (treat$4 clean$3 process) with plasma) and S47	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/23 17:20
S50	14	(US-20030136985-$ or US-20150236157-$ or US-20130049101-$ or US-20080315254-$ or US-20140197455-$ or US-20140246710-$ or US-20140264348-$ or US-20060234504-$ or US-20120295427-$ or US-20090104739-$ or US-20060115933-$ or US-20070249168-$).did. or (US-8785285-$ or US-9064892-$).did.	US-PGPUB; USPAT	OR	ON	2016/06/23 17:34
S51	95	S37 and ((fluorine fluoride) with (treat$4 clean$3 process) with plasma) and H01L29/7848.cpc.	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/23 17:34
S52	73	S37 and ((((cyclic cycle) adj3 deposit$3) CDE) same (vary$3 chang$3 alter$3 rate factor)) and ((((cyclic cycle) adj3 deposit$3) CDE) same $4degree) and ((source drain source/drain s/d) with (deposit$3 epitax$5)) and "cl.sub.2"	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/23 18:21
S53	58	S37 and ((((cyclic cycle) adj3 deposit$3) CDE) same (vary$3 chang$3 alter$3 rate factor)) and ((((cyclic cycle) adj3 deposit$3) CDE) same $4degree) and ((source drain source/drain s/d) with (deposit$3 epitax$5)) and ("cl.sub.2" same temperature)	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/23 18:23
S54	4698	H01L29/66636.cpc.	US-PGPUB; USPAT; USOCR	OR	ON	2017/04/30 18:23
S55	11016021	@ad<"20140822" @rlad<"20140822"	US-	OR	ON	2017/04/30

		@pt1d<"20140822"	PGPUB; USPAT; USOCR			18:23
S56	1111	(((silicon adj carbide) SiC) with (buffer passivation)) and ((silicon adj germanium) SiGe)	US-PGPUB; USPAT; USOCR	OR	ON	2017/04/30 18:24
S57	24	S54 and S55 and S56	US-PGPUB; USPAT; USOCR	OR	ON	2017/04/30 18:24
S58	2	"20060234504"	US-PGPUB; USPAT; USOCR	OR	ON	2017/04/30 18:54
S59	15	(US-20030136985-$ or US-20150236157-$ or US-20130049101-$ or US-20080315254-$ or US-20140197455-$ or US-20140246710-$ or US-20140264348-$ or US-20060234504-$ or US-20120295427-$ or US-20090104739-$ or US-20060115933-$ or US-20070249168-$ or US-20100093147-$).did. or (US-8785285-$ or US-9064892-$).did.	US-PGPUB; USPAT	OR	ON	2017/04/30 19:01
S60	1	S59 and (co-flow)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	ON	2017/04/30 19:01
S61	3	S54 and S55 and (varying adj2 etching)	US-PGPUB; USPAT; USOCR	OR	ON	2017/04/30 19:42
S62	4	S54 and S55 and ((SiC (silicon adj2 carbide)) same co-flow)	US-PGPUB; USPAT; USOCR	OR	ON	2017/04/30 19:47
S63	11	((SiC (silicon adj2 carbide)) same co-flow)	US-PGPUB; USPAT; USOCR	OR	ON	2017/04/30 19:48
S64	10	S55 and S63	US-PGPUB; USPAT; USOCR	OR	ON	2017/04/30 19:49
S65	2	(("etching/deposition" "E/D") adj2 factor)	US-PGPUB; USPAT; USOCR	OR	ON	2017/04/30 19:50
S66	92	(varying increasing decreasing) with ((cyclic adj2 deposition) CDE)	US-PGPUB; USPAT; USOCR	OR	ON	2017/04/30 19:51
S67	77	S55 and S66	US-PGPUB; USPAT; USOCR	OR	ON	2017/04/30 19:51

S68	0	S55 and S66 and co-flow	US-PGPUB; USPAT; USOCR	OR	ON	2017/04/30 19:52
S69	189	(("etching/deposition" "E/D") adj2 ratio)	US-PGPUB; USPAT; USOCR	OR	ON	2017/04/30 19:53
S70	0	S55 and S69 and co-flow	US-PGPUB; USPAT; USOCR	OR	ON	2017/04/30 19:55
S71	0	S55 and S69 and "co-flow"	US-PGPUB; USPAT; USOCR	OR	ON	2017/04/30 19:55
S72	9	S55 and ((cyclic adj2 deposition) CDE) and "co-flow"	US-PGPUB; USPAT; USOCR	OR	ON	2017/04/30 19:55
S73	11	((cyclic adj2 deposition) CDE) and "co-flow"	US-PGPUB; USPAT; USOCR	OR	ON	2017/04/30 19:58
S74	220	((etching with deposition) "E/D") adj2 (factor ratio)	US-PGPUB; USPAT; USOCR	OR	ON	2017/04/30 19:59
S75	0	S55 and S74 and co-flow	US-PGPUB; USPAT; USOCR	OR	ON	2017/04/30 20:00
S76	214	S55 and S74	US-PGPUB; USPAT; USOCR	OR	ON	2017/04/30 20:00
S77	12	((etching with deposition) "E/D") adj2 (factor ratio) same (CL HCL "CL.sub.2" CL2)	US-PGPUB; USPAT; USOCR	OR	ON	2017/04/30 20:01
S78	11	S55 and S77	US-PGPUB; USPAT; USOCR	OR	ON	2017/04/30 20:01
S79	46	S55 and ((cyclic adj2 deposition) CDE) with continuous	US-PGPUB; USPAT; USOCR	OR	ON	2017/04/30 20:15
S80	68	S55 and (((cyclic adj2 deposition) CDE) with constant)	US-PGPUB; USPAT; USOCR	OR	ON	2017/04/30 20:17
S81	109	(S79 S80)	US-PGPUB; USPAT; USOCR	OR	ON	2017/04/30 20:37
S82	18	(US-20030136985-$ or US-20150236157-$ or US-20130049101-$ or	US-PGPUB;	OR	ON	2017/12/11 10:30

		US-20080315254-$ or US-20140197455-$ or US-20140246710-$ or US-20140264348-$ or US-20060234504-$ or US-20120295427-$ or US-20090104739-$ or US-20060115933-$ or US-20070249168-$ or US-20100093147-$ or US-20140197493-$ or US-20140264636-$ or US-20120091469-$).did. or (US-8785285-$ or US-9064892-$).did.	USPAT			
S84	11200634	@ad<"20140822" @rlad<"20140822" @pt1d<"20140822"	US-PGPUB; USPAT; USOCR	OR	ON	2017/12/11 10:32
S85	10901	H01L29/66636,7848,165,167.cpc.	US-PGPUB; USPAT; USOCR	OR	ON	2017/12/11 10:32
S87	11200634	@ad<"20140822" @rlad<"20140822" @pt1d<"20140822"	US-PGPUB; USPAT; USOCR	OR	ON	2017/12/11 11:50
S88	10901	H01L29/66636,7848,165,167.cpc.	US-PGPUB; USPAT; USOCR	OR	ON	2017/12/11 11:50
S89	26	(coflow co-flow) and S87 and S88	US-PGPUB; USPAT; USOCR	OR	ON	2017/12/11 11:50
S90	18	"8598003"	US-PGPUB; USPAT; USOCR	OR	ON	2017/12/11 12:04
S91	45	(coflow$3 co-flow$3) and S87 and S88	US-PGPUB; USPAT; USOCR	OR	ON	2017/12/11 12:05
S92	2	"20150155386"	US-PGPUB; USPAT; USOCR	OR	ON	2017/12/11 12:43
S95	144	S87 and S88 and ("non-selective" with (deposit$4 growth))	US-PGPUB; USPAT; USOCR	OR	ON	2017/12/11 12:50
S96	22	(US-20030136985-$ or US-20150236157-$ or US-20130049101-$ or US-20080315254-$ or US-20140197455-$ or US-20140246710-$ or US-20140264348-$ or US-20060234504-$ or US-20120295427-$ or US-20090104739-$ or US-20060115933-$ or US-20070249168-$ or US-20100093147-$ or US-20140197493-$ or US-20140264636-$ or US-20120091469-$ or US-20130183814-$ or US-20150155386-$ or US-20070287272-$ or US-20080182075-$).did. or (US-8785285-$ or US-9064892-$).did.	US-PGPUB; USPAT	OR	ON	2017/12/11 13:01
S97	7	S96 and non-selective	US-	OR	ON	2017/12/11

			PGPUB; USPAT; USOCR; FPRS; EPO; JPO			13:01
S98	22	(US-20030136985-$ or US-20150236157-$ or US-20130049101-$ or US-20080315254-$ or US-20140197455-$ or US-20140246710-$ or US-20140264348-$ or US-20060234504-$ or US-20120295427-$ or US-20090104739-$ or US-20060115933-$ or US-20070249168-$ or US-20100093147-$ or US-20140197493-$ or US-20140264636-$ or US-20120091469-$ or US-20130183814-$ or US-20150155386-$ or US-20070287272-$ or US-20080182075-$).did. or (US-8785285-$ or US-9064892-$).did.	US-PGPUB; USPAT	OR	OFF	2018/07/07 14:38
S99	19	S98 and (temperature degree)	US-PGPUB; USPAT	OR	OFF	2018/07/07 14:59
S100	7	S98 and (temperature degree) and ((temperature degree) same2 (((cyclic cycle) adj3 deposit$3) CDE))	US-PGPUB; USPAT; USOCR	OR	OFF	2018/07/07 15:39
S101	11324631	@ad<"20140822" @rlad<"20140822" @pt1d<"20140822"	US-PGPUB; USPAT; USOCR	OR	ON	2018/07/07 15:48
S102	182	S101 and (H01L29/7848,66636,66628.cpc.) and (temperature degree) and ((temperature degree) same2 (((cyclic cycle) adj3 deposit$3) CDE))	US-PGPUB; USPAT; USOCR	OR	OFF	2018/07/07 15:48
S103	20	S98 and (temperature degree $4degree)	US-PGPUB; USPAT	OR	OFF	2018/07/07 15:53
S104	191	S101 and (H01L29/7848,66636,66628.cpc.) and ((temperature $4degree) same2 (((cyclic cycle) adj3 deposit$3) CDE))	US-PGPUB; USPAT; USOCR	OR	OFF	2018/07/07 16:02
S105	170	S101 and (H01L29/7848,66636,66628.cpc.) and ((fluorine with (doping doped)) flourine-doped flourine-doping f-doping f-doped)	US-PGPUB; USPAT; USOCR	OR	OFF	2018/07/07 16:57
S106	115	S101 and (H01L29/7848,66636,66628.cpc.) and (f with (doping doped))	US-PGPUB; USPAT; USOCR	OR	OFF	2018/07/07 18:10
S107	100	S106 not S105	US-PGPUB; USPAT; USOCR	OR	OFF	2018/07/07 18:10
S108	15	"8404546"	US-PGPUB; USPAT; USOCR	OR	OFF	2018/07/07 18:33
S109	25	(US-20030136985-$ or US-	US-	OR	OFF	2018/07/07

		20150236157-$ or US-20130049101-$ or US-20080315254-$ or US-20140197455-$ or US-20140246710-$ or US-20140264348-$ or US-20060234504-$ or US-20120295427-$ or US-20090104739-$ or US-20060115933-$ or US-20070249168-$ or US-20100093147-$ or US-20140197493-$ or US-20140264636-$ or US-20120091469-$ or US-20130183814-$ or US-20150155386-$ or US-20070287272-$ or US-20080182075-$ or US-20150069466-$ or US-20120132957-$ or US-20100163939-$).did. or (US-8785285-$ or US-9064892-$).did.	PGPUB; USPAT			18:37
S110	4	S109 and (boron with diffus$4)	US-PGPUB; USPAT; USOCR	OR	OFF	2018/07/07 18:37
S111	2	"20110027955"	US-PGPUB; USPAT; USOCR	OR	OFF	2018/07/07 18:46
S112	1	"14597115"	US-PGPUB; USPAT; USOCR	OR	OFF	2018/07/07 19:04
S113	1189	((doping doped) with fluorine) same (fluorine with plasma)	US-PGPUB; USPAT; USOCR	OR	OFF	2018/07/07 19:06
S114	5	S101 and (H01L29/7848,66636,66628.cpc.) and S113	US-PGPUB; USPAT; USOCR	OR	OFF	2018/07/07 19:06
S115	40	((doping doped) with fluorine) same (fluorine with plasma) same (drain source/drain s/d)	US-PGPUB; USPAT; USOCR	OR	OFF	2018/07/07 19:07
S116	38	S101 and S115	US-PGPUB; USPAT; USOCR	OR	OFF	2018/07/07 19:07
S117	2	"20100163939"	US-PGPUB; USPAT; USOCR	OR	OFF	2018/07/07 19:26
S118	2	"20140264348"	US-PGPUB; USPAT; USOCR	OR	OFF	2018/07/07 19:26

11/ 30/ 2018 2:44:09 PM
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PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 14/597,115	Filing Date 01/14/2015	☐ To be Mailed

ENTITY: ☑ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A		N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A		N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*		x $80 =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*		x $420 =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).				
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))					
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL	

APPLICATION AS AMENDED - PART II

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT	11/13/2018	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 29	Minus	** 29	= 0		x $100 =	0
	Independent (37 CFR 1.16(h))	* 3	Minus	*** 3	= 0		x $460 =	0
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	0

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=		x $0 =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=		x $0 =	
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.	LIE
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".	/Ramona D Wilson/
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".	
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.	

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Doc Code: A.NE.AFCP
Document Description: After Final Consideration Pilot Program Request

PTO/SB/434 (05-13)

CERTIFICATION AND REQUEST FOR CONSIDERATION UNDER THE AFTER FINAL CONSIDERATION PILOT PROGRAM 2.0

Practitioner Docket No.:	Application No.:	Filing Date:
2014-0937/24061.2998	14/597,115	01-14-2015
First Named Inventor:	**Title:**	
Chun Hsiung Tsai	Metal-Insensitive Epitaxy Formation	

APPLICANT HEREBY CERTIFIES THE FOLLOWING AND REQUESTS CONSIDERATION UNDER THE AFTER FINAL CONSIDERATION PILOT PROGRAM 2.0 (AFCP 2.0) OF THE ACCOMPANYING RESPONSE UNDER 37 CFR 1.116.

1. The above-identified application is (i) an original utility, plant, or design nonprovisional application filed under 35 U.S.C. 111(a) [a continuing application (*e.g.*, a continuation or divisional application) is filed under 35 U.S.C. 111(a) and is eligible under (i)], or (ii) an international application that has entered the national stage in compliance with 35 U.S.C. 371(c).
2. The above-identified application contains an outstanding final rejection.
3. Submitted herewith is a response under 37 CFR 1.116 to the outstanding final rejection. The response includes an amendment to at least one independent claim, and the amendment does not broaden the scope of the independent claim in any aspect.
4. This certification and request for consideration under AFCP 2.0 is the only AFCP 2.0 certification and request filed in response to the outstanding final rejection.
5. Applicant is willing and available to participate in any interview requested by the examiner concerning the present response.
6. This certification and request is being filed electronically using the Office's electronic filing system (EFS-Web).
7. Any fees that would be necessary consistent with current practice concerning responses after final rejection under 37 CFR 1.116, *e.g.*, extension of time fees, are being concurrently filed herewith. [There is no additional fee required to request consideration under AFCP 2.0.]
8. By filing this certification and request, applicant acknowledges the following:
    - Reissue applications and reexamination proceedings are not eligible to participate in AFCP 2.0.
    - The examiner will verify that the AFCP 2.0 submission is compliant, *i.e.*, that the requirements of the program have been met (see items 1 to 7 above). For compliant submissions:
        - The examiner will review the response under 37 CFR 1.116 to determine if additional search and/or consideration (i) is necessitated by the amendment and (ii) could be completed within the time allotted under AFCP 2.0. If additional search and/or consideration is required but cannot be completed within the allotted time, the examiner will process the submission consistent with current practice concerning responses after final rejection under 37 CFR 1.116, *e.g.*, by mailing an advisory action.
        - If the examiner determines that the amendment does not necessitate additional search and/or consideration, or if the examiner determines that additional search and/or consideration is required and could be completed within the allotted time, then the examiner will consider whether the amendment places the application in condition for allowance (after completing the additional search and/or consideration, if required). If the examiner determines that the amendment does not place the application in condition for allowance, then the examiner will contact the applicant and request an interview.
            - The interview will be conducted by the examiner, and if the examiner does not have negotiation authority, a primary examiner and/or supervisory patent examiner will also participate.
            - If the applicant declines the interview, or if the interview cannot be scheduled within ten (10) calendar days from the date that the examiner first contacts the applicant, then the examiner will proceed consistent with current practice concerning responses after final rejection under 37 CFR 1.116.

Signature	Date
/Michael E. Ramon/	November 13, 2018
Name (Print/Typed) Michael E. Ramon	**Practitioner Registration No.** 52147

***Note**: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4(d) for signature requirements and certifications. Submit multiple forms if more than one signature is required, see below*.*

☑ * Total of 1 forms are submitted.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

PTO/SB/22 (03-13)
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PETITION FOR EXTENSION OF TIME UNDER 37 CFR 1.136(a)

Docket Number (Optional): 2014-0937/24061.2998

Application Number: 14/597,115

Filed: 01-14-2015

For: Metal-Insensitive Epitaxy Formation

Art Unit: 2896

Examiner: SPALLA, DAVID C

This is a request under the provisions of 37 CFR 1.136(a) to extend the period for filing a reply in the above-identified application.

The requested extension and fee are as follows (check time period desired and enter the appropriate fee below):

		Fee	Small Entity Fee	Micro Entity Fee	
☑	One month (37 CFR 1.17(a)(1))	$200	$100	$50	$ 200.00
☐	Two months (37 CFR 1.17(a)(2))	$600	$300	$150	$
☐	Three months (37 CFR 1.17(a)(3))	$1,400	$700	$350	$
☐	Four months (37 CFR 1.17(a)(4))	$2,200	$1,100	$550	$
☐	Five months (37 CFR 1.17(a)(5))	$3,000	$1,500	$750	$

☐ Applicant asserts small entity status. See 37 CFR 1.27.

☐ Applicant certifies micro entity status. See 37 CFR 1.29.
Form PTO/SB/15A or B or equivalent must either be enclosed or have been submitted previously.

☐ A check in the amount of the fee is enclosed.

☑ Payment by credit card. ~~XXXXXXXXXXXXXXX~~ Form PTO-2038 is attached.

☐ The Director has already been authorized to charge fees in this application to a Deposit Account.

☑ The Director is hereby authorized to charge any fees which may be required, or credit any overpayment, to Deposit Account Number 08-1394.

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WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

I am the

☐ applicant/inventor.

☐ assignee of record of the entire interest. See 37 CFR 3.71. 37 CFR 3.73(b) statement is enclosed (Form PTO/SB/96).

☑ attorney or agent of record. Registration number 52,147.

☐ attorney or agent acting under 37 CFR 1.34. Registration number _____.

/Michael E. Ramon/ — Signature

November 13, 2018 — Date

Michael E. Ramon — Typed or printed name

512-867-8426 — Telephone Number

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. Submit multiple forms if more than one signature is required, see below*.

☑ * Total of 1 forms are submitted.

This collection of information is required by 37 CFR 1.136(a). The information is required to obtain or retain a benefit by the public, which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 6 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
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3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

REMARKS

Claims 1-10, 12-20 and 27-36 were previously pending, of which claim 27 has been amended. Reconsideration of presently pending claims 1-10, 12-20 and 27-36 is respectfully requested in light of the above amendments and the following remarks.

Disposition of Claims

In the Office Action Summary, the Office states that claims 1-20 and 27-36 are pending in the application. Applicant respectfully notes that in the Response filed March 15, 2018, claim 11 was cancelled, and claims 35 and 36 were added. Thus, claims 1-10, 12-20 and 27-36 are in fact pending in the application, as noted above.

Allowable Subject Matter

Claims 1-10, 12-20, 33, 35, and 36 are allowed. Applicant appreciates the indication of allowable subject matter.

Rejections Under 35 U.S.C. § 103

Claims 27, 29-32, and 34 were rejected under 35 U.S.C. §103 as being unpatentable over Park et al. (U.S. Patent Application Publication No. 2012/0091469, hereinafter referred to as "Park") in view of Bauer et al. (U.S. Patent Application Publication No. 2006/0234504, hereinafter referred to as "Bauer") and Woon et al. (U.S. Patent Application Publication No. 2011/0027955, hereinafter referred to as "Woon"). Claim 28 was rejected under 35 U.S.C. §103 as being unpatentable over Park, Bauer, and Woon as applied to claim 27, and further in view of Dasgupta et al. (U.S. Patent Application Publication No. 2014/0091308, hereinafter referred to as "Dasgupta"). With respect to the claims as herein amended, Applicants respectfully traverse these rejections.

Independent Claim 27

Amended claim 27 recites, in part:

> "epitaxially growing a second semiconductor material over the fluorine-doped passivation layer, thereby forming S/D features in the recesses, wherein the

first semiconductor material is different than the second semiconductor material, and wherein the epitaxially growing the second semiconductor material includes performing a cyclic deposition and etching (CDE) process having a first deposition step performed at a first temperature and a second deposition step performed at a second temperature different than the first temperature."

The amendment to claim 27 finds support at least at paragraphs [0046] and [0080] of the present application. While not acquiescing in the Examiner's interpretation of the applied references, Applicant provides the above amendment to claim 27 to clarify over the cited art.

In particular, claim 27 has been amended to include the limitation "wherein the epitaxially growing the second semiconductor material includes performing a cyclic deposition and etching (CDE) process having a first deposition step performed at a first temperature and a second deposition step performed at a second temperature different than the first temperature." Thus, similar to allowed claims 1 and 15, the cited references do not teach or suggest all of the limitations of claim 27, as amended. (*see* OA pages 5-6, 'Allowable Subject Matter').

Thus, factually supporting a *prima facie* case of obviousness has clearly not been met, and the rejection under 35 U.S.C. §103 of amended claim 27 should be withdrawn.

Claims 28-32 and 34 depend on and further limit claim 27 and therefore are deemed to be patentable over the prior art, for at least the same reasons set forth above in connection with independent claim 27. Accordingly, the rejection of claims 28-32 and 34 should be withdrawn.

Conclusion

An early formal notice of allowance of claims 1-20 and 27-36 is requested. A personal or telephonic interview is respectfully requested to discuss any remaining issues in an effort to expedite the allowance of this application.

Respectfully submitted,

/Michael E. Ramon/

Michael E. Ramon
Registration No. 52,147

Dated: November 13, 2018
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Certificate of Transmission

I hereby certify that this correspondence and any attachments are being filed with the U.S. Patent and Trademark Office via EFS-Web on:

11/13/2018

/Janie Martinez-Holm/

Janie Martinez-Holm

Listing of Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Previously Presented) A method of forming a field effect transistor (FET), the method comprising:

performing an etching process to a semiconductor substrate, thereby forming recesses in source and drain (S/D) regions of the semiconductor substrate;

forming, by a non-selective deposition process, a passivation material layer of a first semiconductor material in the recesses; and

epitaxially growing a second semiconductor material on the passivation material layer, thereby forming S/D features in the recesses, wherein the S/D features are separated from the semiconductor substrate by the passivation material layer, wherein the first semiconductor material is different than the second semiconductor material, wherein the epitaxially growing of the second semiconductor material includes performing a cyclic deposition and etching (CDE) process having a first deposition step and a second deposition step, and wherein the first deposition step and the second deposition step are performed at different temperatures.

2. (Previously Presented) The method of claim 1, wherein the forming of the passivation material layer includes performing the non-selective deposition process using a precursor free of chlorine.

3. (Previously Presented) The method of claim 2, wherein the forming of the passivation material layer includes epitaxially growing the passivation material layer of the first semiconductor material.

4. (Original) The method of claim 3, wherein the first semiconductor material includes silicon carbide and the second semiconductor material includes silicon germanium.

5. (Previously Presented) The method of claim 3, wherein the forming of the passivation material layer includes epitaxially growing the passivation material layer of the first semiconductor material that is free of dopant, using the precursor free of dopant-containing gas.

6. (Previously Presented) The method of claim 3, wherein the forming of the passivation material layer includes forming a silicon carbide layer having a carbon atomic percentage ranging from 1.8% to 3%.

7. (Previously Presented) The method of claim 1, wherein the forming of the passivation material layer includes forming the passivation material layer with a thickness ranging from 1 nm to 4 nm, effectively preventing interaction between chlorine and metal residuals under the passivation material layer.

8. (Original) The method of claim 1, further comprising performing a fluorine treatment to the passivation material layer before the epitaxially growing of the second semiconductor material.

9. (Previously Presented) The method of claim 8, wherein the performing of the fluorine treatment includes performing the fluorine treatment with a fluorine dose ranging from 1×10^{14} ions/cm^2 to 2×10^{15} ions/cm^2.

10. (Original) The method of claim 1, wherein the epitaxially growing of the second semiconductor material includes epitaxially growing the second semiconductor material with in-situ doping one of a n-type dopant and a p-type dopant.

11. (Cancelled)

12. (Previously Presented) The method of claim 1, wherein

the CDE process includes a first cycle for deposition and a second cycle for etching; and

the second cycle uses a chlorine-containing gas that includes at least one of HCl and Cl_2.

13. (Original) The method of claim 12, wherein the first cycle of the CDE process uses a precursor that includes PH_3, monomethylsilane (MMS), and at least one of SiH_4 and Si_2H_6.

14. (Original) The method of claim 12, wherein the first cycle of the CDE process uses a precursor that includes B_2H_6, GeH_4, and at least one of SiH_4 and Si_2H_6.

15. (Previously Presented) A method of forming a field effect transistor (FET), the method comprising:

performing an etching process to a semiconductor substrate, thereby forming recesses in source and drain (S/D) regions of the semiconductor substrate; and

epitaxially growing a semiconductor material by a deposition process with a varying etching/deposition (E/D) factor, thereby forming S/D features in the recesses, wherein the deposition process includes a co-flow epitaxy growth, wherein the deposition process includes a first deposition step performed at a first substrate temperature and a second deposition step performed after the first deposition step, and wherein the second deposition step is performed at a second substrate temperature different than the first substrate temperature.

16. (Previously Presented) The method of claim 15, wherein the first deposition step has a first etch/deposition (E/D) factor and the second deposition step has a second E/D factor greater than the first E/D factor.

17. (Previously Presented) The method of claim 15, wherein

the first deposition step is a non-selective deposition; and

the second deposition step is a selective deposition.

18. (Previously Presented) The method of claim 15, wherein

the first substrate temperature is less than 620 ^{0}C; and

the second substrate temperature is greater than 620 ^{0}C.

19. (Previously Presented) The method of claim 15, wherein the deposition process includes a combination of the co-flow epitaxy growth and a cyclic deposition and etching (CDE) process.

20. (Original) The method of claim 15, wherein the epitaxially growing of the semiconductor material includes varying the E/D factor by a mechanism selected from gas partial pressure, gas flow rate, substrate temperature, and a combination thereof.

21-26. (Canceled)

27. (***Currently Amended***) A method of forming a field effect transistor (FET), the method comprising:

performing an etching process to a semiconductor substrate, thereby forming recesses in source and drain (S/D) regions of the semiconductor substrate;

forming, by a non-selective deposition process, a passivation layer of a first semiconductor material in the recesses;

after forming the passivation layer of the first semiconductor material, doping the passivation layer with fluorine atoms to form a fluorine-doped passivation layer; and

epitaxially growing a second semiconductor material over the fluorine-doped passivation layer, thereby forming S/D features in the recesses, wherein the first semiconductor material is different than the second semiconductor material, and wherein the epitaxially growing the second semiconductor material includes performing a cyclic deposition and etching (CDE) process having a first deposition step performed at a first temperature and a second deposition step performed at a second temperature different than the first temperature.

28. (Previously Presented) The method of claim 27, wherein the doping is performed by a fluorine plasma treatment.

29. (Previously Presented) The method of claim 27, wherein the fluorine-doped passivation layer has a fluorine concentration per unit area ranging from 1×10^{14} cm^{-2} to 2×10^{15} cm^{-2}.

30. (Previously Presented) The method of claim 27, wherein the forming of the passivation layer includes performing the non-selective deposition process using a precursor free of chlorine; and the epitaxially growing of the second semiconductor material includes an etching process using a chlorine-containing gas.

31. (Previously Presented) The method of claim 27, wherein the forming of the passivation layer includes epitaxially growing the first semiconductor material that is free of dopant, using a precursor free of dopant-containing gas.

32. (Previously Presented) The method of claim 31, wherein the epitaxially growing of the second semiconductor material includes in-situ doping one of a n-type dopant and a p-type dopant to the second semiconductor material.

33. (Previously Presented) The method of claim 1, wherein the passivation material layer is formed by the non-selective deposition process using a precursor that includes monomethylsilane (MMS) and at least one of silane (SiH_4) and disilane (SiH_6).

34. (Previously Presented) The method of claim 27, wherein the passivation layer is formed by the non-selective deposition process using a precursor that includes monomethylsilane (MMS) and at least one of silane (SiH_4) and disilane (SiH_6).

35. (Previously Presented) The method of claim 1, further comprising:

prior to epitaxially growing the second semiconductor material, doping the passivation layer with fluorine atoms to form a fluorine-doped passivation layer; and

epitaxially growing a second semiconductor material on the fluorine-doped passivation material layer.

36. (Previously Presented) The method of claim 15, wherein the varying E/D factor includes a step-wise varying E/D factor.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of: Chun Hsiung Tsai *et al.*	§	Docket No.: 2014-0937/24061.2998
	§	
Application No. 14/597,115	§	Art Unit: 2896
	§	
Filing Date: January 14, 2015	§	Examiner: Spalla, David C.
	§	
Entitled: METAL-INSENSITIVE EPITAXY FORMATION	§	Confirmation No.: 8745
	§	

Mail Stop: AF
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE TO FINAL OFFICE ACTION DATED JULY 13, 2018

Applicants respectfully submit this paper in response to the Final Office Action mailed on July 13, 2018, setting a period for reply to expire on October 13, 2018. A petition for a one-month extension of time is attached, extending the period for reply to November 13, 2018. In light of the Amendments and/or Remarks herein, further consideration is requested.

Any fees required by this paper are being provided as directed in an electronic submission of this paper or in a transmittal letter accompanying this paper. However, the Commissioner is hereby authorized to charge any deficiency in fees required by this paper and any additional fees under 37 C.F.R. § 1.16 or 1.17 which may be required during the pendency of this application, and to similarly credit any overpayment, to Haynes and Boone, LLP's Deposit Account 08-1394.

Amendments to the Claims are reflected in the listing of claims which begins on page **2** of this paper.

Remarks/Arguments begin on page **7** of this paper.

Electronic Patent Application Fee Transmittal

Application Number:	14597115
Filing Date:	14-Jan-2015
Title of Invention:	Metal-Insensitive Epitaxy Formation
First Named Inventor/Applicant Name:	Chun Hsiung Tsai
Filer:	Michael Edward Ramon/Janie Martinez-Holm
Attorney Docket Number:	2014-0937/24061.2998

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension - 1 month with $0 paid	1251	1	200	200
Miscellaneous:				
			Total in USD ($)	**200**

Electronic Acknowledgement Receipt

EFS ID:	34296026
Application Number:	14597115
International Application Number:	
Confirmation Number:	8745
Title of Invention:	Metal-Insensitive Epitaxy Formation
First Named Inventor/Applicant Name:	Chun Hsiung Tsai
Customer Number:	42717
Filer:	Michael Edward Ramon/Janie Martinez-Holm
Filer Authorized By:	Michael Edward Ramon
Attorney Docket Number:	2014-0937/24061.2998
Receipt Date:	13-NOV-2018
Filing Date:	14-JAN-2015
Time Stamp:	15:53:14
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$200
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	After Final Consideration Program Request	24061-2998_AFCP_Form.pdf	226997 23b2a972dc830a98be507e25cc00d74c5c45e2a9	no	2
Warnings:					
Information:					
2	Extension of Time	24061-2998_EOT_1mo.pdf	182890 a1ceab782d2995114e045a86628d027a336ffc60	no	2
Warnings:					
Information:					
3		24061-2998_Response_07-13-18_FOA_2.pdf	161079 aacb64ff4ddbd70949a882ab55068e66cf4faacf	yes	9

Multipart Description/PDF files in .zip description

Document Description	Start	End
Applicant Arguments/Remarks Made in an Amendment	7	9
Claims	2	6
Response After Final Action	1	1

Warnings:					
Information:					
4	Fee Worksheet (SB06)	fee-info.pdf	30255 481fff1c5c8a7e8c371fc1f01675388977a27696	no	2
Warnings:					
Information:					
			Total Files Size (in bytes):	601221	

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/597,115	01/14/2015	Chun Hsiung Tsai	2014-0937/24061.2998	8745

42717 7590 07/13/2018

HAYNES AND BOONE, LLP
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2323 Victory Avenue
Suite 700
Dallas, TX 75219

EXAMINER	
SPALLA, DAVID C	

ART UNIT	PAPER NUMBER
2896	

NOTIFICATION DATE	DELIVERY MODE
07/13/2018	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ipdocketing@haynesboone.com

Office Action Summary	Application No. 14/597,115	Applicant(s) TSAI ET AL.	
	Examiner DAVID SPALLA	Art Unit 2896	AIA (First Inventor to File) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06/12/2018*.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) *1-20 and 27-36* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☒ Claim(s) *1-20,33,35 and 36* is/are allowed.

7)☒ Claim(s) *27-32 and 34* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☒ The drawing(s) filed on *01/14/2015* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☒ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

DETAILED ACTION

Information Disclosure Statement

The information disclosure statement (IDS) submitted on 06/12/2018 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103 which forms the basis for all obviousness rejections set forth in this Office action:

> A patent for a claimed invention may not be obtained, notwithstanding that the claimed invention is not identically disclosed as set forth in section 102, if the differences between the claimed invention and the prior art are such that the claimed invention as a whole would have been obvious before the effective filing date of the claimed invention to a person having ordinary skill in the art to which the claimed invention pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 27 and 29-32 are rejected under 35 U.S.C. 103 as being unpatentable over US PG Pub 2012/0091469 to Park et al. (hereinafter Park) in view of US PG Pub 2006/0234504 to Bauer et al. (hereinafter Bauer) and US PG Pub 2011/0027955 to Woon et al. (hereinafter Woon).

Regarding Claim 27, Park discloses a method of forming a field effect transistor (FET), the method comprising:

performing an etching process to a semiconductor substrate (Fig. 5, substrate 110), thereby forming recesses (111 a,111 b) in source and drain (S/D) regions of the semiconductor substrate;

forming a passivation material layer (131) of a first semiconductor material (SiC; [0035]) in the recess; and

epitaxially growing a second semiconductor material (SiGe; [0039]) over the passivation material layer, thereby forming S/D features in the recesses, wherein the first semiconductor material is different than the second semiconductor material (SiC for the first and SiGe for the second).

Park does not disclose the use of a non-selective deposition process for the formation of the passivation material layer.

Bauer discloses a method of forming SiC in S/D regions by performing a non-selective deposition process using a precursor free of chlorine [0100].

It would have been obvious to one of ordinary skill in the art, before the effective filing date of the invention, to have modified the method used by Park to use a non-selective deposition, free of chlorine as a precursor. As noted by Bauer in paragraph [0100], using a non-selective process with precursors such as trisilane and a carbon source would result in a carbon rich layer. Such a layer would have had benefits obvious to one of ordinary skill in the art such as preventing dopants from diffusing into the channel region or otherwise leaking from the S/D features, a desire Park notes in paragraph [0033].

Park does not disclose doping the passivation layer with fluorine atoms to form a fluorine-doped passivation layer.

Woon discloses a method including doping a recessed source/drain region (Fig. 2C) with fluorine atoms [0022].

It would have been obvious to one of ordinary skill in the art, before the invention was made, to have modified the method of Park to include the step of doping the passivation layer with fluorine atoms to form a fluorine-doped layer. Fluorine is a known inhibitor for boron atoms, preventing the diffusion of the atoms (Woon, [0024]). Including fluorine in the SiC buff layer of Park would have furthered the goal of the reference by enhancing the buffer layer, which is provided to prevent dopant diffusion, see Park para. [0034])

Regarding Claim 29, the combination of Park, Bauer and Woon makes obvious the method of Claim 27 wherein the fluorine-doped passivation layer has a fluorine concentration per unit area ranging from 1.times.10.sup.14 cm.sup.2 to 2.times.15.sup.2 (Woon, [0034]; 1.5 E14)

Regarding Claim 30, the combination of Park, Bauer and Woon makes obvious the method of Claim 27, wherein the forming of the passivation layer includes performing the non-selective process using a precursor free of chlorine (Park, [0062]) and the epitaxially growing of the second semiconductor material includes an etching process using a chlorine-containing gas (Park, [0065]).

Regarding Claim 31, the combination of Park, Bauer and Woon makes obvious the method of Claim 27, wherein the forming of the passivation material layer includes epitaxially growing the first semiconductor material that is free of dopant, using the precursor free of dopant-containing gas ([0062]; Park).

Regarding Claim 32, the combination of Park, Bauer and Woon makes obvious the method of Claim 31, wherein the epitaxially growing of the second semiconductor material includes in-situ doping one of a n-type dopant and a p-type dopant to the second semiconductor material (Park; [0066]&[0068]).

Regarding Claim 34, the combination of Park, Bauer and Woon makes obvious the method of Claim 37, wherein the passivation layer is formed by the non-selective deposition using a precursor that includes monomethylsilane (MMS) and at least one of silane (SiH.sub.4) and disilane (SiH.sub.6) (Bauer, [0085]&[0086]).

Claim 28 is rejected under 35 U.S.C. 103 as being unpatentable over the combination of Park, Bauer and Woon as applied to Claim 27 above, and further in view of US PG Pub 2014/0091308 to Dasgupta et al. (hereinafter Dasgupta).

Regarding Claim 28, the combination of Park, Bauer and Woon makes obvious the method of Claim 27 but does not disclose wherein the doping is perform by a fluorine plasma treatment.

Dasgupta discloses a method of doping a layer with fluorine using plasma-based fluorine doping.

It would have been obvious to one of ordinary skill in the art, before the invention was made, to have modified the method made obvious by Park and Woon such that the doping process is done by a plasma-based method. Numerous methods of doping are known in the art and Applicant has not noted any particular problem that is solved by using plasma doping over ion implantation. However, ion implantation is known to have problems such as crystallographic damage and could have selected plasma doping to avoid this.

Response to Arguments

Applicant's arguments with respect to Claim 27 have been considered but are moot because the arguments do not apply to the current rejection in view of Woon.

Allowable Subject Matter

Claims 1-10, 12-20, 22, 35 and 36 are allowed.

Claims 1 and 15 disclose *inter alia* a method of epitaxially growing a second semiconductor material, in source and drain regions for a FET, using a cyclic deposition and etching process having a first deposition step and a second deposition step, wherein the first deposition step and the second deposition step are performed at different temperatures.

US 2014/0264348 was relied on, in previous rejections, for showing a CDE process having different temperatures for deposition steps. However, Applicant has overcome the reference by establishing, in the remarks filed on 10/04/2017, that, not later than the effective filing date of the claimed invention, the subject matter disclosed and the claimed invention were either owned by the same person or subject to an obligation of assignment to the same person or subject to a joint research agreement. Thus, the reference is not available as art.

A search of relevant references in the art does not show Applicant's method to be obvious or anticipated. Claims 2-10, 12-14, 16-20, 35 and 36 depend on either Claim 1 or Claim 15 and are allowable for at least the reasons above.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DAVID SPALLA whose telephone number is (303)297-4298. The examiner can normally be reached on Mon-Fri 10am-5pm MST.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Loke Steven can be reached on (571) 272-1657. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/DAVID SPALLA/
Examiner, Art Unit 2896

Notice of References Cited	Application/Control No. 14/597,115	Applicant(s)/Patent Under Reexamination TSAI ET AL.	
	Examiner DAVID SPALLA	Art Unit 2896	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-2012/0091469 A1	04-2012	Park; Keum-Seok	H01L29/0847	257/77
*	B	US-2006/0234504 A1	10-2006	Bauer; Matthias	C23C16/04	438/674
*	C	US-2011/0027955 A1	02-2011	Woon; Wei-Yen	H01L21/26506	438/285
*	D	US-2014/0091308 A1	04-2014	DASGUPTA; Sansaptak	H01L29/7784	257/76
	E	US-				
	F	US-				
	G	US-				
	H	US-				
	I	US-				
	J	US-				
	K	US-				
	L	US-				
	M	US-				

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

In place of PTO-1449 Form	U. S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE			*Complete if Known*	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(use as many sheets as necessary)*				Application Number	14/597,115
				Filing Date	January 14, 2015
				First Inventor Name	Chun Hsiung Tsai et al.
				Art Unit	2896
				Examiner Name	SPALLA, DAVID C
SHEET	1	OF	1	Attorney Docket Number	2014-0937/24061.2998

U. S. PATENTS				
Examiner's Initials	Cite No.	Document Number	Issue Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document
	A1	8404546	03-26-2013	Woon et al.

U. S. PATENT APPLICATION PUBLICATIONS				
Examiner's Initials	Cite No.	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document

FOREIGN PATENT DOCUMENTS					
Examiner's Initials	Cite No.	Foreign Patent Document (Country Code – Number – Kind)	Publication Date MM-DD-YYYY	Patentee or Applicant of Cited Document	Translation Y/N
	B1				

NON-PATENT LITERATURE DOCUMENTS		
Examiner's Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article, title of the item, date, page(s), volume-issue number(s), publisher, city/country where published
	A1	
	A2	
	A3	
	A4	
	A5	

Examiner Signature	/DAVID C SPALLA/	Date Considered	07/07/2018

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include a copy of this form with next communication to applicant.

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14597115	TSAI ET AL.
	Examiner	Art Unit
	DAVID SPALLA	2896

CPC- SEARCHED		
Symbol	Date	Examiner
H01L 29/66636, 7848	06/23/2016	DCS
H01L 29/165, 167	12/11/2017	DCS
H01L 29/784, 66636, 66628	07/07/2018	DCS

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
45			

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

SEARCH NOTES		
Search Notes	Date	Examiner
Search of submitted IDS references	06/23/2016	DCS
See attached EAST search history	06/23/2016	DCS
See attached EAST updated search history	04/30/2017	DCS
See attached EAST updated search history	12/11/2017	DCS
Search of submitted IDS references	07/07/2018	DCS
See attached EAST updated search history	07/07/2018	DCS

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

/DAVID SPALLA/ Examiner.Art Unit 2896	

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L3	22	(US-20030136985-$ or US-20150236157-$ or US-20130049101-$ or US-20080315254-$ or US-20140197455-$ or US-20140246710-$ or US-20140264348-$ or US-20060234504-$ or US-20120295427-$ or US-20090104739-$ or US-20060115933-$ or US-20070249168-$ or US-20100093147-$ or US-20140197493-$ or US-20140264636-$ or US-20120091469-$ or US-20130183814-$ or US-20150155386-$ or US-20070287272-$ or US-20080182075-$).did. or (US-8785285-$ or US-9064892-$).did.	US-PGPUB; USPAT	OR	OFF	2018/07/07 14:38
L4	19	3 and (temperature degree)	US-PGPUB; USPAT	OR	OFF	2018/07/07 14:59
L7	7	3 and (temperature degree) and ((temperature degree) same2 (((cyclic cycle) adj3 deposit$3) CDE))	US-PGPUB; USPAT; USOCR	OR	OFF	2018/07/07 15:39
L8	11324631	@ad<"20140822" @rlad<"20140822" @pt1d<"20140822"	US-PGPUB; USPAT; USOCR	OR	ON	2018/07/07 15:48
L9	182	L8 and (H01L29/7848,66636,66628.cpc.) and (temperature degree) and ((temperature degree) same2 (((cyclic cycle) adj3 deposit$3) CDE))	US-PGPUB; USPAT; USOCR	OR	OFF	2018/07/07 15:48
L11	20	3 and (temperature degree $4degree)	US-PGPUB; USPAT	OR	OFF	2018/07/07 15:53
L13	191	L8 and (H01L29/7848,66636,66628.cpc.) and ((temperature $4degree) same2 (((cyclic cycle) adj3 deposit$3) CDE))	US-PGPUB; USPAT; USOCR	OR	OFF	2018/07/07 16:02
L14	170	L8 and (H01L29/7848,66636,66628.cpc.) and ((fluorine with (doping doped)) flourine-doped flourine-doping f-doping f-doped)	US-PGPUB; USPAT; USOCR	OR	OFF	2018/07/07 16:57
L15	115	L8 and (H01L29/7848,66636,66628.cpc.) and (f with (doping doped))	US-PGPUB; USPAT; USOCR	OR	OFF	2018/07/07 18:10
L16	100	15 not 14	US-PGPUB; USPAT; USOCR	OR	OFF	2018/07/07 18:10
L17	15	"8404546"	US-	OR	OFF	2018/07/07

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L18	25	(US-20030136985-$ or US-20150236157-$ or US-20130049101-$ or US-20080315254-$ or US-20140197455-$ or US-20140246710-$ or US-20140264348-$ or US-20060234504-$ or US-20120295427-$ or US-20090104739-$ or US-20060115933-$ or US-20070249168-$ or US-20100093147-$ or US-20140197493-$ or US-20140264636-$ or US-20120091469-$ or US-20130183814-$ or US-20150155386-$ or US-20070287272-$ or US-20080182075-$ or US-20150069466-$ or US-20120132957-$ or US-20100163939-$).did. or (US-8785285-$ or US-9064892-$).did.	US-PGPUB; USPAT	OR	OFF	2018/07/07 18:37
L19	4	18 and (boron with diffus$4)	US-PGPUB; USPAT; USOCR	OR	OFF	2018/07/07 18:37
L20	2	"20110027955"	US-PGPUB; USPAT; USOCR	OR	OFF	2018/07/07 18:46
L21	1	"14597115"	US-PGPUB; USPAT; USOCR	OR	OFF	2018/07/07 19:04
L22	1189	((doping doped) with fluorine) same (fluorine with plasma)	US-PGPUB; USPAT; USOCR	OR	OFF	2018/07/07 19:06
L23	5	L8 and (H01L29/7848,66636,66628.cpc.) and 22	US-PGPUB; USPAT; USOCR	OR	OFF	2018/07/07 19:06
L24	40	((doping doped) with fluorine) same (fluorine with plasma) same (drain source/drain s/d)	US-PGPUB; USPAT; USOCR	OR	OFF	2018/07/07 19:07
L25	38	8 and 24	US-PGPUB; USPAT; USOCR	OR	OFF	2018/07/07 19:07
L26	2	"20100163939"	US-PGPUB; USPAT; USOCR	OR	OFF	2018/07/07 19:26
L27	2	"20140264348"	US-PGPUB; USPAT; USOCR	OR	OFF	2018/07/07 19:26
S2	10680640	@ad<"20140822" @rlad<"20140822" @pt1d<"20140822"	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/13 10:07
S3	0	"14813556"	US-PGPUB;	OR	ON	2016/06/13 10:46

			USPAT; USOCR			
S4	1	"14597115"	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/13 13:33
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S9	15	("7667271" | "8362575" | "8367498" | "8440517" | "8497528" | "8610240" | "8680576" | "8723272" | "8729634" | "8785285" | "8796759" | "8809139" | "8828823" | "8836016" | "8841701").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/13 13:41
S10	24	("20030052406" | "20060057859" | "20070059875" | "20070111439" | "20070128782" | "20070131969" | "20070145487" | "20080044960" | "20080251851" | "20090239344" | "20090280612" | "20100252816" | "20110147828" | "20120068193" | "20120104470" | "3909304" | "7112848" | "7132338" | "7518196" | "7910415" | "8110486" | "8338259").PN. OR ("8785285").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/13 13:44
S12	9538	fluorine adj3 (plasma treatment)	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/13 13:53
S14	10680640	@ad<"20140822" @rlad<"20140822" @pt1d<"20140822"	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/13 14:05
S15	4124	H01L29/66636.cpc.	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/13 14:05
S16	1731	S14 and S15 and ((silicon adj carbide) SiC) and ((silicon adj germanium) SiGe)	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/13 14:05
S17	31	S16 and (fluorine adj3 (plasma treat$4 clean$3))	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/13 14:12
S18	700	S14 and S15 and ((silicon adj carbide) SiC) and ((second upper) with ((silicon adj germanium) SiGe))	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/13 14:23
S19	260	S18 and (treat$3 clean$3)	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/13 14:27
S20	10686366	@ad<"20140822" @rlad<"20140822" @pt1d<"20140822"	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/15 15:31
S21	4131	H01L29/66636.cpc.	US-	OR	ON	2016/06/15

			PGPUB; USPAT; USOCR			15:31
S22	103	S20 and S21 and (non-selective)	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/15 15:31
S23	2	S20 and S21 and ((non-selective) same precursor same (SiC (silicon adj2 carbide)))	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/15 15:39
S24	94	H01L29/66636.cpc. and (SiC same dop$3 same (prevent block$3 barrier diffusion))	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/17 17:53
S25	10690365	@ad<"20140822" @rlad<"20140822" @pt1d<"20140822"	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/17 18:16
S26	4134	H01L29/66636.cpc.	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/17 18:16
S27	5	S25 and S26 and ((non-selective) same cycle)	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/17 18:16
S28	9	S25 and S26 and ((non-selective) same (cyclic cycle))	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/17 18:18
S29	120	S25 and S26 and ((cyclic cycle) same (vary$3 chang$3 alter$3 rate factor))	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/17 18:19
S30	44	S25 and S26 and (((cyclic cycle) adj3 deposit$3) same (vary$3 chang$3 alter$3 rate factor))	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/17 18:20
S31	24	S25 and S26 and (((cyclic cycle) adj3 deposit$3) same (vary$3 chang$3 alter$3 rate factor)) and (degree celsius)	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/17 18:24
S32	0	S25 and S26 and (((cyclic cycle) adj3 deposit$3) same (vary$3 chang$3 alter$3 rate factor)) and ".degree."	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/17 18:30
S33	24	S25 and S26 and (((cyclic cycle) adj3 deposit$3) same (vary$3 chang$3 alter$3 rate factor)) and degree	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/17 18:31
S34	40	S25 and S26 and (((cyclic cycle) adj3 deposit$3) same (vary$3 chang$3 alter$3 rate factor)) and $4degree	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/17 18:31
S35	2	"20060234504"	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/21 15:48

S36	2	"20130328126"	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/21 15:55
S37	10698055	@ad<"20140822" @rlad<"20140822" @pt1d<"20140822"	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/23 16:27
S38	2137	S37 and (((cyclic cycle) adj3 deposit$3) same (vary$3 chang$3 alter$3 rate factor))	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/23 16:27
S39	3183	S37 and ((((cyclic cycle) adj3 deposit$3) CDE) same (vary$3 chang$3 alter$3 rate factor))	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/23 16:28
S40	661	S37 and ((((cyclic cycle) adj3 deposit$3) CDE) same (vary$3 chang$3 alter$3 rate factor)) and ((((cyclic cycle) adj3 deposit$3) CDE) same $4degree)	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/23 16:29
S42	335	S37 and ((((cyclic cycle) adj3 deposit$3) CDE) same (vary$3 chang$3 alter$3 rate factor)) and ((((cyclic cycle) adj3 deposit$3) CDE) same $4degree) and ((source drain source/drain s/d) with (deposit$3 epitax$5))	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/23 16:32
S43	9	S37 and (((cyclic cycle) adj3 deposit$3) CDE) with (non-selective (non adj selective)) with selective	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/23 16:51
S45	18	S37 and ((((cyclic cycle) adj3 deposit$3) CDE) same (non-selective (non adj selective)) same selective)	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/23 16:52
S46	98695	S37 and ((fluorine fluoride) with (treat$4 clean$3 process))	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/23 17:18
S47	4157	H01L29/66636.cpc.	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/23 17:19
S48	258	S37 and ((fluorine fluoride) with (treat$4 clean$3 process)) and S47	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/23 17:19
S49	86	S37 and ((fluorine fluoride) with (treat$4 clean$3 process) with plasma) and S47	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/23 17:20
S50	14	(US-20030136985-$ or US-20150236157-$ or US-20130049101-$ or US-20080315254-$ or US-20140197455-$ or US-20140246710-$ or US-20140264348-$ or US-20060234504-$ or US-20120295427-$ or US-20090104739-$ or US-20060115933-$ or US-20070249168-$).did. or (US-8785285-$ or US-9064892-$).did.	US-PGPUB; USPAT	OR	ON	2016/06/23 17:34

S51	95	S37 and ((fluorine fluoride) with (treat$4 clean$3 process) with plasma) and H01L29/7848.cpc.	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/23 17:34
S52	73	S37 and ((((cyclic cycle) adj3 deposit$3) CDE) same (vary$3 chang$3 alter$3 rate factor)) and ((((cyclic cycle) adj3 deposit$3) CDE) same $4degree) and ((source drain source/drain s/d) with (deposit$3 epitax$5)) and "cl.sub.2"	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/23 18:21
S53	58	S37 and ((((cyclic cycle) adj3 deposit$3) CDE) same (vary$3 chang$3 alter$3 rate factor)) and ((((cyclic cycle) adj3 deposit$3) CDE) same $4degree) and ((source drain source/drain s/d) with (deposit$3 epitax$5)) and ("cl.sub.2" same temperature)	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/23 18:23
S54	4698	H01L29/66636.cpc.	US-PGPUB; USPAT; USOCR	OR	ON	2017/04/30 18:23
S55	11016021	@ad<"20140822" @rlad<"20140822" @pt1d<"20140822"	US-PGPUB; USPAT; USOCR	OR	ON	2017/04/30 18:23
S56	1111	(((silicon adj carbide) SiC) with (buffer passivation)) and ((silicon adj germanium) SiGe)	US-PGPUB; USPAT; USOCR	OR	ON	2017/04/30 18:24
S57	24	S54 and S55 and S56	US-PGPUB; USPAT; USOCR	OR	ON	2017/04/30 18:24
S58	2	"20060234504"	US-PGPUB; USPAT; USOCR	OR	ON	2017/04/30 18:54
S59	15	(US-20030136985-$ or US-20150236157-$ or US-20130049101-$ or US-20080315254-$ or US-20140197455-$ or US-20140246710-$ or US-20140264348-$ or US-20060234504-$ or US-20120295427-$ or US-20090104739-$ or US-20060115933-$ or US-20070249168-$ or US-20100093147-$).did. or (US-8785285-$ or US-9064892-$).did.	US-PGPUB; USPAT	OR	ON	2017/04/30 19:01
S60	1	S59 and (co-flow)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	ON	2017/04/30 19:01
S61	3	S54 and S55 and (varying adj2 etching)	US-PGPUB; USPAT; USOCR	OR	ON	2017/04/30 19:42
S62	4	S54 and S55 and ((SiC (silicon adj2 carbide)) same co-flow)	US-PGPUB; USPAT;	OR	ON	2017/04/30 19:47

			USOCR			
S63	11	((SiC (silicon adj2 carbide)) same co-flow)	US-PGPUB; USPAT; USOCR	OR	ON	2017/04/30 19:48
S64	10	S55 and S63	US-PGPUB; USPAT; USOCR	OR	ON	2017/04/30 19:49
S65	2	(("etching/deposition" "E/D") adj2 factor)	US-PGPUB; USPAT; USOCR	OR	ON	2017/04/30 19:50
S66	92	(varying increasing decreasing) with ((cyclic adj2 deposition) CDE)	US-PGPUB; USPAT; USOCR	OR	ON	2017/04/30 19:51
S67	77	S55 and S66	US-PGPUB; USPAT; USOCR	OR	ON	2017/04/30 19:51
S68	0	S55 and S66 and co-flow	US-PGPUB; USPAT; USOCR	OR	ON	2017/04/30 19:52
S69	189	(("etching/deposition" "E/D") adj2 ratio)	US-PGPUB; USPAT; USOCR	OR	ON	2017/04/30 19:53
S70	0	S55 and S69 and co-flow	US-PGPUB; USPAT; USOCR	OR	ON	2017/04/30 19:55
S71	0	S55 and S69 and "co-flow"	US-PGPUB; USPAT; USOCR	OR	ON	2017/04/30 19:55
S72	9	S55 and ((cyclic adj2 deposition) CDE) and "co-flow"	US-PGPUB; USPAT; USOCR	OR	ON	2017/04/30 19:55
S73	11	((cyclic adj2 deposition) CDE) and "co-flow"	US-PGPUB; USPAT; USOCR	OR	ON	2017/04/30 19:58
S74	220	((etching with deposition) "E/D") adj2 (factor ratio)	US-PGPUB; USPAT; USOCR	OR	ON	2017/04/30 19:59
S75	0	S55 and S74 and co-flow	US-PGPUB; USPAT; USOCR	OR	ON	2017/04/30 20:00
S76	214	S55 and S74	US-PGPUB; USPAT; USOCR	OR	ON	2017/04/30 20:00
S77	12	((etching with deposition) "E/D") adj2	US-	OR	ON	2017/04/30

		(factor ratio) same (CL HCL "CL.sub.2" CL2)	PGPUB; USPAT; USOCR			20:01
S78	11	S55 and S77	US-PGPUB; USPAT; USOCR	OR	ON	2017/04/30 20:01
S79	46	S55 and ((cyclic adj2 deposition) CDE) with continuous	US-PGPUB; USPAT; USOCR	OR	ON	2017/04/30 20:15
S80	68	S55 and (((cyclic adj2 deposition) CDE) with constant)	US-PGPUB; USPAT; USOCR	OR	ON	2017/04/30 20:17
S81	109	(S79 S80)	US-PGPUB; USPAT; USOCR	OR	ON	2017/04/30 20:37
S82	18	(US-20030136985-$ or US-20150236157-$ or US-20130049101-$ or US-20080315254-$ or US-20140197455-$ or US-20140246710-$ or US-20140264348-$ or US-20060234504-$ or US-20120295427-$ or US-20090104739-$ or US-20060115933-$ or US-20070249168-$ or US-20100093147-$ or US-20140197493-$ or US-20140264636-$ or US-20120091469-$).did. or (US-8785285-$ or US-9064892-$).did.	US-PGPUB; USPAT	OR	ON	2017/12/11 10:30
S84	11200634	@ad<"20140822" @rlad<"20140822" @pt1d<"20140822"	US-PGPUB; USPAT; USOCR	OR	ON	2017/12/11 10:32
S85	10901	H01L29/66636,7848,165,167.cpc.	US-PGPUB; USPAT; USOCR	OR	ON	2017/12/11 10:32
S87	11200634	@ad<"20140822" @rlad<"20140822" @pt1d<"20140822"	US-PGPUB; USPAT; USOCR	OR	ON	2017/12/11 11:50
S88	10901	H01L29/66636,7848,165,167.cpc.	US-PGPUB; USPAT; USOCR	OR	ON	2017/12/11 11:50
S89	26	(coflow co-flow) and S87 and S88	US-PGPUB; USPAT; USOCR	OR	ON	2017/12/11 11:50
S90	18	"8598003"	US-PGPUB; USPAT; USOCR	OR	ON	2017/12/11 12:04
S91	45	(coflow$3 co-flow$3) and S87 and S88	US-PGPUB; USPAT; USOCR	OR	ON	2017/12/11 12:05
S92	2	"20150155386"	US-	OR	ON	2017/12/11

			PGPUB; USPAT; USOCR			12:43
S95	144	S87 and S88 and ("non-selective" with (deposit$4 growth))	US-PGPUB; USPAT; USOCR	OR	ON	2017/12/11 12:50
S96	22	(US-20030136985-$ or US-20150236157-$ or US-20130049101-$ or US-20080315254-$ or US-20140197455-$ or US-20140246710-$ or US-20140264348-$ or US-20060234504-$ or US-20120295427-$ or US-20090104739-$ or US-20060115933-$ or US-20070249168-$ or US-20100093147-$ or US-20140197493-$ or US-20140264636-$ or US-20120091469-$ or US-20130183814-$ or US-20150155386-$ or US-20070287272-$ or US-20080182075-$).did. or (US-8785285-$ or US-9064892-$).did.	US-PGPUB; USPAT	OR	ON	2017/12/11 13:01
S97	7	S96 and non-selective	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	ON	2017/12/11 13:01

7/ 7/ 2018 7:37:39 PM
C:\ Users\ dspalla\ Documents\ EAST\ Workspaces\ 14597115.wsp

In place of PTO-1449 Form	U. S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE			*Complete if Known*	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(use as many sheets as necessary)*				Application Number	14/597,115
				Filing Date	January 14, 2015
				First Inventor Name	Chun Hsiung Tsai et al.
				Art Unit	2896
				Examiner Name	SPALLA, DAVID C
SHEET	1	OF	1	Attorney Docket Number	2014-0937/24061.2998

U. S. PATENTS				
Examiner's Initials	Cite No.	Document Number	Issue Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document
	A1	8404546	03-26-2013	Woon et al.

U. S. PATENT APPLICATION PUBLICATIONS				
Examiner's Initials	Cite No.	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document

FOREIGN PATENT DOCUMENTS					
Examiner's Initials	Cite No.	Foreign Patent Document (Country Code – Number – Kind)	Publication Date MM-DD-YYYY	Patentee or Applicant of Cited Document	Translation Y/N
	B1				

NON-PATENT LITERATURE DOCUMENTS		
Examiner's Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article, title of the item, date, page(s), volume-issue number(s), publisher, city/country where published
	A1	
	A2	
	A3	
	A4	
	A5	

Examiner Signature		Date Considered	

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include a copy of this form with next communication to applicant.

Electronic Acknowledgement Receipt

EFS ID:	32878213
Application Number:	14597115
International Application Number:	
Confirmation Number:	8745
Title of Invention:	Metal-Insensitive Epitaxy Formation
First Named Inventor/Applicant Name:	Chun Hsiung Tsai
Customer Number:	42717
Filer:	Michael Edward Ramon/Janie Martinez-Holm
Filer Authorized By:	Michael Edward Ramon
Attorney Docket Number:	2014-0937/24061.2998
Receipt Date:	12-JUN-2018
Filing Date:	14-JAN-2015
Time Stamp:	17:36:29
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal Letter	24061-2998_SuppIDS-3_Transmittal.pdf	106545 2c9a3669d0609ad406e60f6c373edea84e0c305d	no	1

Warnings:

Information:					
2	Information Disclosure Statement (IDS) Form (SB08)	24061-2998_SuppIDS-3_1449.pdf	89550 9a71ed2855cc6dd6b5b1bccc82e2878686b64d3f	no	1
Warnings:					
Information:					
This is not an USPTO supplied IDS fillable form					
			Total Files Size (in bytes):	196095	

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Chun Hsiung Tsai *et al.*	§	Confirmation No.: 8745
Application No. 14/597,115	§	Group Art Unit: 2896
Filed: January 14, 2015	§	Examiner: Spalla, David C.
For: Metal-Insensitive Epitaxy Formation	§	Attorney Docket No. 2014-0937/24061.2998

INFORMATION DISCLOSURE STATEMENT

Via EFS-Web
Commissioner For Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In compliance with the duty of disclosure under 37 CFR §1.56, and in accordance with the practice under 37 CFR §1.97 and §1.98, the Examiner's attention is directed to the documents listed on the enclosed modified Form PTO-1449. No inference should be made that the cited references are in fact material, are in fact prior art, or that no better art exists. The references are not in any order based on their pertinence.

It is hereby certified that each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. (37 CFR §1.97 (e)(1)). Therefore, Applicants believes that no fee is due.

The Commissioner is hereby authorized to charge any additional fees which may be required or credit any overpayment to Deposit Account No. 08-1394.

It is respectfully requested that the above information be considered by the Examiner and that a copy of the enclosed modified Form PTO-1449 be returned indicating that such information has been considered.

Respectfully submitted,

/Michael E. Ramon/

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Date: June 12, 2018
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CERTIFICATE OF TRANSMISSION

I hereby certify that this correspondence and any attachments are being transmitted via the Electronic Filing System (EFS) Web with the United States Patent and Trademark Office on 6/12/2018.

/Janie Martinez-Holm/
Janie Martinez-Holm

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of: Chun Hsiung Tsai *et al.*	§	Docket No.: 2014-0937/24061.2998
	§	
Application No. 14/597,115	§	Art Unit: 2896
	§	
Filing Date: January 14, 2015	§	Examiner: Spalla, David C.
	§	
Entitled: METAL-INSENSITIVE EPITAXY FORMATION	§	Confirmation No.: 8745
	§	

Mail Stop: Amendment
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE TO OFFICE ACTION DATED DECEMBER 18, 2017

Applicants respectfully submit this paper in response to the Office Action mailed on December 18, 2017, setting a period for reply to expire on March 18, 2018. Entry of the following amendments and comments into the record of the above-identified application is respectfully requested.

Any fees required by this paper are being provided as directed in an electronic submission of this paper or in a transmittal letter accompanying this paper. However, the Commissioner is hereby authorized to charge any deficiency in fees required by this paper and any additional fees under 37 C.F.R. § 1.16 or 1.17 which may be required during the pendency of this application, and to similarly credit any overpayment, to Haynes and Boone, LLP's Deposit Account 08-1394.

Amendments to the Claims are reflected in the listing of claims which begins on page **2** of this paper.

Remarks/Arguments begin on page **7** of this paper.

Listing of Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (***Currently Amended***) A method of forming a field effect transistor (FET), the method comprising:

performing an etching process to a semiconductor substrate, thereby forming recesses in source and drain (S/D) regions of the semiconductor substrate;

forming, by a non-selective deposition process, a passivation material layer of a first semiconductor material in the recesses; and

epitaxially growing a second semiconductor material on the passivation material layer, thereby forming S/D features in the recesses, wherein the S/D features are separated from the semiconductor substrate by the passivation material layer, [[and]] wherein the first semiconductor material is different than the second semiconductor material, wherein the epitaxially growing of the second semiconductor material includes performing a cyclic deposition and etching (CDE) process having a first deposition step and a second deposition step, and wherein the first deposition step and the second deposition step are performed at different temperatures.

2. (Previously Presented) The method of claim 1, wherein the forming of the passivation material layer includes performing the non-selective deposition process using a precursor free of chlorine.

3. (Previously Presented) The method of claim 2, wherein the forming of the passivation material layer includes epitaxially growing the passivation material layer of the first semiconductor material.

4. (Original) The method of claim 3, wherein the first semiconductor material includes silicon carbide and the second semiconductor material includes silicon germanium.

5. (Previously Presented) The method of claim 3, wherein the forming of the passivation material layer includes epitaxially growing the passivation material layer of the first semiconductor material that is free of dopant, using the precursor free of dopant-containing gas.

6. (Previously Presented) The method of claim 3, wherein the forming of the passivation material layer includes forming a silicon carbide layer having a carbon atomic percentage ranging from 1.8% to 3%.

7. (Previously Presented) The method of claim 1, wherein the forming of the passivation material layer includes forming the passivation material layer with a thickness ranging from 1 nm to 4 nm, effectively preventing interaction between chlorine and metal residuals under the passivation material layer.

8. (Original) The method of claim 1, further comprising performing a fluorine treatment to the passivation material layer before the epitaxially growing of the second semiconductor material.

9. (Previously Presented) The method of claim 8, wherein the performing of the fluorine treatment includes performing the fluorine treatment with a fluorine dose ranging from 1×10^{14} ions/cm^2 to 2×10^{15} ions/cm^2.

10. (Original) The method of claim 1, wherein the epitaxially growing of the second semiconductor material includes epitaxially growing the second semiconductor material with in-situ doping one of a n-type dopant and a p-type dopant.

11. (***Cancelled)***

12. (***Currently Amended***) The method of claim [[11]]1, wherein

the CDE process includes a first cycle for deposition and a second cycle for etching; and

the second cycle uses a chlorine-containing gas that includes at least one of HCl and Cl_2.

13. (Original) The method of claim 12, wherein the first cycle of the CDE process uses a precursor that includes PH_3, monomethylsilane (MMS), and at least one of SiH_4 and Si_2H_6.

14. (Original) The method of claim 12, wherein the first cycle of the CDE process uses a precursor that includes B_2H_6, GeH_4, and at least one of SiH_4 and Si_2H_6.

15. (***Currently Amended***) A method of forming a field effect transistor (FET), the method comprising:

performing an etching process to a semiconductor substrate, thereby forming recesses in source and drain (S/D) regions of the semiconductor substrate; and

epitaxially growing a semiconductor material by a deposition process with a varying etching/deposition (E/D) factor, thereby forming S/D features in the recesses, wherein the deposition process includes a co-flow epitaxy growth, wherein the deposition process includes a first deposition step performed at a first substrate temperature and a second deposition step performed after the first deposition step, and wherein the second deposition step is performed at a second substrate temperature different than the first substrate temperature.

16. (***Currently Amended***) The method of claim 15, wherein the ~~deposition process incudes a~~ first deposition step ~~having~~ has a first etch/deposition (E/D) factor and ~~thereafter a~~ the second deposition step ~~having~~ has a second E/D factor greater than the first E/D factor.

17. (***Currently Amended***) The method of claim [[16]]15, wherein

the first deposition step is a non-selective deposition; and

the second deposition step is a selective deposition.

18. (***Currently Amended***) The method of claim [[16]]15, wherein

the ~~first deposition step has a~~ first substrate temperature is less than 620 ^{0}C; and

the ~~second deposition step has a~~ second substrate temperature is greater than 620 ^{0}C.

19. (Previously Presented) The method of claim 15, wherein the deposition process includes a combination of the co-flow epitaxy growth and a cyclic deposition and etching (CDE) process.

20. (Original) The method of claim 15, wherein the epitaxially growing of the semiconductor material includes varying the E/D factor by a mechanism selected from gas partial pressure, gas flow rate, substrate temperature, and a combination thereof.

21-26. (Canceled)

27. (***Currently Amended***) A method of forming a field effect transistor (FET), the method comprising:

performing an etching process to a semiconductor substrate, thereby forming recesses in source and drain (S/D) regions of the semiconductor substrate;

forming, by a non-selective deposition process, a passivation layer of a first semiconductor material in the recesses;

after forming the passivation layer of the first semiconductor material, ~~performing a fluorine treatment to~~ doping the passivation layer with fluorine atoms to form a fluorine-doped passivation layer; and

epitaxially growing a second semiconductor material over the fluorine-doped passivation layer, thereby forming S/D features in the recesses, wherein the first semiconductor material is different than the second semiconductor material.

28. (***Currently Amended***) The method of claim 27, wherein the ~~fluorine treatment~~ doping is performed by a fluorine plasma treatment.

29. (***Currently Amended***) The method of claim 27, wherein the fluorine-doped passivation layer ~~treatment uses~~ has a fluorine [[dose]]concentration per unit area ranging from 1×10^{14} cm^{-2}~~ions/cm^{-2}~~ to 2×10^{15} cm^{-2}~~ions/cm^{-2}~~.

30. (Previously Presented) The method of claim 27, wherein the forming of the passivation layer includes performing the non-selective deposition process using a precursor free of chlorine; and the epitaxially growing of the second semiconductor material includes an etching process using a chlorine-containing gas.

31. (Previously Presented) The method of claim 27, wherein the forming of the passivation layer includes epitaxially growing the first semiconductor material that is free of dopant, using a precursor free of dopant-containing gas.

32. (Previously Presented) The method of claim 31, wherein the epitaxially growing of the second semiconductor material includes in-situ doping one of a n-type dopant and a p-type dopant to the second semiconductor material.

33. (Previously Presented) The method of claim 1, wherein the passivation material layer is formed by the non-selective deposition process using a precursor that includes monomethylsilane (MMS) and at least one of silane (SiH_4) and disilane (SiH_6).

34. (Previously Presented) The method of claim 27, wherein the passivation layer is formed by the non-selective deposition process using a precursor that includes monomethylsilane (MMS) and at least one of silane (SiH_4) and disilane (SiH_6).

35. (***New***) The method of claim 1, further comprising:

prior to epitaxially growing the second semiconductor material, doping the passivation layer with fluorine atoms to form a fluorine-doped passivation layer; and

epitaxially growing a second semiconductor material on the fluorine-doped passivation material layer.

36. (***New***) The method of claim 15, wherein the varying E/D factor includes a step-wise varying E/D factor.

REMARKS

Claims 1-20 and 27-34 were previously pending, of which claims 1, 12, 15-18, and 27-29 have been amended, claim 11 has been cancelled, and claims 35 and 36 have been added. Reconsideration of presently pending claims 1-10, 12-20 and 27-36 is respectfully requested in light of the above amendments and the following remarks.

Allowable Subject Matter

Claim 18 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all the limitations of the base claim and any intervening claims. In view of the deficiencies of the cited references, as discussed below, Applicants believe it would be premature to rewrite claim 18 in independent form, as suggested by the Office. Applicants also respectfully note that claim 18 depends on and further limits claim 15 and is allowable for at least the reasons set forth in connection with independent claim 15.

Rejections Under 35 U.S.C. § 103

Claim 1-7, 10, and 33 were rejected under 35 U.S.C. §103 as being unpatentable over Park et al. (U.S. Patent Application Publication No. 2012/0091469, hereinafter referred to as "Park") in view of Bauer et al. (U.S. Patent Application Publication No. 2006/0234504, hereinafter referred to as "Bauer"). Claims 8 and 9 were rejected under 35 U.S.C. §103 as being unpatentable over Park and Bauer as applied to claim 1, and in further view of Rotondaro et al. (U.S. Patent Application Publication No. 2007/0249168, hereinafter referred to as "Rotondaro"). Claims 11-14 were rejected under 35 U.S.C. §103 as being unpatentable over Park and Bauer as applied to claim 1, and in further view of Bauer (U.S. Patent Application Publication No. 2012/0295427, hereinafter referred to as "Bauer '427"). Claims 15, 16, 19, and 20 were rejected under 35 U.S.C. §103 as being unpatentable over Hung et al. (U.S. Patent Application Publication No. 2015/0155386, hereinafter referred to as "Hung"). Claim 17 was rejected under 35 U.S.C. §103 as being unpatentable over Hung as applied to claim 16, and in further view of Bauer '427. Claims 27-29, 30, 31, 32, and 34 were rejected under 35 U.S.C. §103 as being unpatentable over Park in view of Bauer and Rotondaro. With respect to the claims as herein amended, Applicants respectfully traverse these rejections.

Independent Claim 1

Amended claim 1 recites, in part:

"epitaxially growing a second semiconductor material on the passivation material layer, thereby forming S/D features in the recesses, wherein the S/D features are separated from the semiconductor substrate by the passivation material layer, wherein the first semiconductor material is different than the second semiconductor material, wherein the epitaxially growing of the second semiconductor material includes performing a cyclic deposition and etching (CDE) process having a first deposition step and a second deposition step, and wherein the first deposition step and the second deposition step are performed at different temperatures."

The amendment to claim 1 finds support at least at cancelled claim 11, claim 18, and paragraphs [0046] and [0080] of the present application. In the rejection of claim 1, the Examiner relies on Park's silicon buffer layer 131 as allegedly disclosing the claimed "passivation material layer" and admits that "Park does not disclose the use of a non-selective deposition process for the formation of the passivation material layer". OA at page 3.

Thus, the Examiner cites to Bauer as allegedly disclosing "performing a non-selective deposition process". Even assuming *arguendo* the Office's interpretation of Bauer, which Applicants do not admit, neither Bauer nor Park teach or suggest a CDE process "having a first deposition step and a second deposition step, and wherein the first deposition step and the second deposition step are performed at different temperatures.", as required by amended claim 1. In fact, at page 12 of the present Action, the Examiner states that "the references of record **do not**…note a temperature differences between CDE steps."

Thus, factually supporting a *prima facie* case of obviousness has clearly not been met, and the rejection under 35 U.S.C. §103 of amended claim 1 should be withdrawn.

Dependent Claims 2-14

Claim 11 has been cancelled, rendering the rejection of this claim moot. Claims 2-10, 12-14, and 33 depend on and further limit independent claim 1 and therefore are deemed to be patentable over the prior art, for at least the same reasons set forth above in connection with

independent claim 1. Accordingly, the rejection of claims 2-10, 12-14, and 33 should be withdrawn. Claim 12 was amended in view of the cancellation of claim 11.

Independent Claim 15

Amended claim 15 recites, in part, "wherein the deposition process includes a first deposition step performed at a first substrate temperature and a second deposition step performed after the first deposition step, and wherein the second deposition step is performed at a second substrate temperature different than the first substrate temperature" The amendment to claim 15 finds support at least at claims 16 and 18, and at paragraph [0080] of the present application. Hung, relied upon for the rejection of claim 15, does not disclose first and second deposition steps "wherein the second deposition step is performed at a second substrate temperature different than the first substrate temperature". In fact, as noted above, the Examiner states at page 12 of the present Action that "the references of record **do not**…note a temperature differences between CDE steps."

Thus, factually supporting a *prima facie* case of obviousness has clearly not been met, and the rejection under 35 U.S.C. §103 of amended claim 15 should be withdrawn.

Dependent Claims 16-20

Claims 16-20 depend on and further limit independent claim 15 and therefore are deemed to be patentable over the prior art, for at least the same reasons set forth above in connection with independent claim 15. Accordingly, the rejection of claims 16-20 should be withdrawn. Claims 16-18 were amended in view of the amendment to claim 15.

Independent Claim 27

Amended claim 27 recites, in part:

> "performing an etching process to a semiconductor substrate, thereby forming recesses in source and drain (S/D) regions of the semiconductor substrate;
> forming, by a non-selective deposition process, a passivation layer of a first semiconductor material in the recesses;
> after forming the passivation layer of the first semiconductor material, doping the passivation layer with fluorine atoms to form a fluorine-doped passivation layer; and

epitaxially growing a second semiconductor material over the fluorine-doped passivation layer…"

The amendment to claim 27 finds support at least at paragraph [0041] and [0076] of the present application. In the rejection of claim 27, the Examiner admits that "Park does not disclose performing a fluorine treatment to the passivation layer", and then cites to Rotondaro as allegedly disclosing this feature. OA at pages 9 and 10. In particular, the Office cites to Rotondaro's paragraph [0040] which recites "fluorine cleaning plasmas".

Even assuming *arguendo* the Office's interpretation of Rotondaro, which Applicants do not admit, Rotondaro's "fluorine cleaning plasmas" **do not**, and are not intended to, perform doping of a passivation layer. For example, with reference to Rotondaro's FIG. 4 (reproduced below) and related paragraphs [0039] and [0040], Rotondaro describes that contaminants can be deposited in the recessed-region 115 and that "the contaminants are deposited on surfaces 415 of the recessed-region 115 that are created by dry-etch plasma proceses. The presence of contaminant on roughened surfaces 415, in turn, necessitates…cleaning processes (e.g., one or more of oxygen and fluorine cleaning plasmas…) **before** the recessed-region 115 can be filled." (emphasis added). Thus, Rotondaro's fluorine cleaning plasma is *at best* used immediately after recess formation, and before deposition of any subsequent layers, to remove contaminants deposited on surfaces 415 of the recessed-region 115. In contrast, Applicants' amended claim 27 requires "forming recesses" followed by "forming a passivation layer…in the recesses", "after forming the passivation layer…, doping the passivation layer with fluorine atoms to form a fluorine-doped passivation layer" and "growing a second semiconductor material over the fluorine-doped passivation layer…"

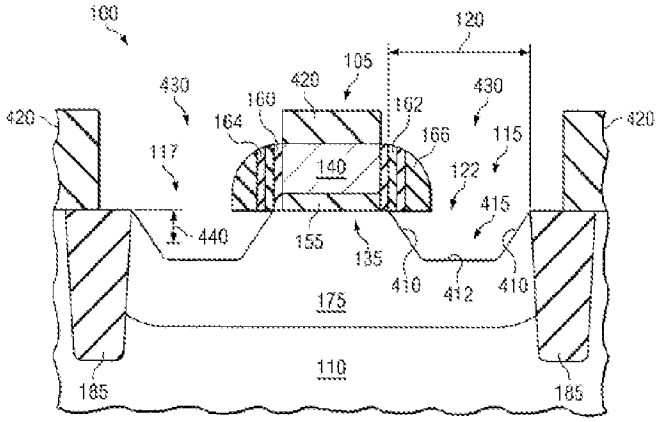


FIG. 4

Thus, Park, Bauer, and Rotondaro do not teach or suggest "after forming the passivation layer of the first semiconductor material, doping the passivation layer with fluorine atoms to form a fluorine-doped passivation layer; and epitaxially growing a second semiconductor material over the fluorine-doped passivation layer…", as required by amended claim 27.

Thus, factually supporting a *prima facie* case of obviousness has clearly not been met, and the rejection under 35 U.S.C. §103 of amended claim 27 should be withdrawn.

Dependent Claims 28-32 and 34

Claims 28-32 and 34 depend on and further limit claim 27 and therefore are deemed to be patentable over the prior art, for at least the same reasons set forth above in connection with independent claim 27. Accordingly, the rejection of claims 28-32 and 34 should be withdrawn. Claims 28 and 29 were amended in view of the amendment to claim 27.

New Claims

Claims 35 and 36, which depend on and further limit claims 1 and 15, respectively, have been added and are deemed to be patentable over the cited art, for at least the same reasons set forth above in connection with independent claims 1 and 15.

Conclusion

An early formal notice of allowance of claims 1-20 and 27-36 is requested. A personal or telephonic interview is respectfully requested to discuss any remaining issues in an effort to expedite the allowance of this application.

Respectfully submitted,

/Michael E. Ramon/

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Registration No. 52,147

Dated: March 15, 2018

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3/15/2018

/Janie Martinez-Holm/

Janie Martinez-Holm

Electronic Acknowledgement Receipt

EFS ID:	32061816
Application Number:	14597115
International Application Number:	
Confirmation Number:	8745
Title of Invention:	Metal-Insensitive Epitaxy Formation
First Named Inventor/Applicant Name:	Chun Hsiung Tsai
Customer Number:	42717
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Application Type:	Utility under 35 USC 111(a)

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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		24061-2998_Response_12-18-17_NFOA_2.pdf	173554 49e13573a4d23e38c3a003b51ab34e447a4ed196	yes	12

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Amendment/Req. Reconsideration-After Non-Final Reject	1	1
	Claims	2	6
	Applicant Arguments/Remarks Made in an Amendment	7	12
Warnings:			
Information:			
	Total Files Size (in bytes):	173554	

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 14/597,115	Filing Date 01/14/2015	☐ To be Mailed

ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT **03/15/2018**

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	* 29	Minus	** 29	= 0	X $100 =	0
Independent (37 CFR 1.16(h))	* 3	Minus	***3	= 0	X $460 =	0
☐ Application Size Fee (37 CFR 1.16(s))						
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
					TOTAL ADD'L FEE	0

AMENDMENT

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =	
☐ Application Size Fee (37 CFR 1.16(s))						
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
					TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
MELINDA L. OLIVER

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**
If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/597,115	01/14/2015	Chun Hsiung Tsai	2014-0937/24061.2998	8745

42717 7590 12/18/2017

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Dallas, TX 75219

EXAMINER	
SPALLA, DAVID C	

ART UNIT	PAPER NUMBER
2896	

NOTIFICATION DATE	DELIVERY MODE
12/18/2017	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ipdocketing@haynesboone.com

Office Action Summary	Application No. 14/597,115	Applicant(s) TSAI ET AL.	
	Examiner DAVID SPALLA	Art Unit 2896	AIA (First Inventor to File) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10/04/2017*.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) *1-20 and 27-34* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *1-17,19,20 and 27-34* is/are rejected.

8)☒ Claim(s) *18* is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☒ The drawing(s) filed on *01/14/2015* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☒ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 10/04/2017 has been entered.

Information Disclosure Statement

The information disclosure statement (IDS) submitted on 06/21/2017 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103 which forms the basis for all obviousness rejections set forth in this Office action:

> A patent for a claimed invention may not be obtained, notwithstanding that the claimed invention is not identically disclosed as set forth in section 102, if the differences between the claimed invention and the prior art are such that the claimed invention as a whole would have been obvious before the effective filing date of the claimed invention to a person having ordinary skill in the art to which the claimed invention pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-7, 10 and 33 are rejected under 35 U.S.C. 103 as being unpatentable over US PG Pub 2012/0091469 to Park et al. (hereinafter Park) in view of US PG Pub 2006/0234504 to Bauer et al. (hereinafter Bauer).

Regarding Claim 1, Park discloses a method of forming a field effect transistor (FET), the method comprising:

performing an etching process to a semiconductor substrate (Fig. 5, substrate 110), thereby forming recesses (111a,111b) in source and drain (S/D) regions of the semiconductor substrate;

forming a passivation material layer (131) of a first semiconductor material (SiC; [0035]) in the recess; and

epitaxially growing a second semiconductor material (SiGe; [0039]) on the passivation material layer, thereby forming S/D features in the recesses, wherein the S/D features are separated from the semiconductor substrate by the passivation material layer (Fig. 7), and wherein the first semiconductor material is different than the second semiconductor material (SiC for the first and SiGe for the second).

Park does not disclose the use of a non-selective deposition process for the formation of the passivation material layer.

Bauer discloses a method of forming SiC in S.D regions by performing a non-selective deposition process using a precursor free of chlorine [0100].

It would have been obvious to one of ordinary skill in the art, before the effective filing date of the invention, to have modified the method used by Park to use a non-selective deposition, free of chlorine as a precursor. As noted by Bauer in paragraph [0100], using a non-selective process with precursors such as trisilane and a carbon source would result in a carbon rich layer. Such a layer would have had benefits obvious to one of ordinary skill in the art such as preventing dopants from diffusing into the channel region or otherwise leaking from the S/D features, a desire Park notes in paragraph [0033].

Regarding Claim 2, the combination of Park and Bauer makes obvious the method of Claim 1, wherein the forming of the passivation material layer includes performing the non-selective deposition process using a precursor free of chlorine (Park, [0062]).

Regarding Claim 3, the combination of Park and Bauer makes obvious the method of Claim 2, wherein the forming of the passivation material layer includes epitaxially growing the passivation material layer of the first semiconductor material (Park, [0035]).

Regarding Claim 4, the combination of Park and Bauer makes obvious the method of Claim 3, wherein the first semiconductor material includes silicon carbide (Park; [0035]) and the second semiconductor material includes silicon germanium (Park; [0039]).

Regarding Claim 5, the combination of Park and Bauer makes obvious the method of Claim 3, wherein the forming of the passivation material layer includes epitaxially growing the passivation material layer of the first semiconductor material that is free of dopant, using the precursor free of dopant-containing gas ([0062]; Park leaves the passivation material layer free of dopants to block the diffusion of dopants from the second semiconductor material [0033]).

Regarding Claim 6, the combination of Park and Bauer makes obvious the method of Claim 3, wherein the forming of the passivation material layer includes forming a silicon carbide layer having a carbon atomic percentage ranging from 1.8% to 3% (Bauer, [0100]; 1-3.5% atomic percentage).

Regarding Claim 7, the combination of Park and Bauer makes obvious the method of Claim 1, wherein the forming of the passivation material layer includes forming the passivation material layer with a thickness ranging from 1 nm to 4 nm [0035], effectively preventing interaction between chlorine and metal residuals under the passivation material layer.

Regarding Claim 10, the combination of Park and Bauer makes obvious the method of Claim 1, wherein the epitaxially growing of the second semiconductor material includes epitaxially growing the second semiconductor material with in-situ doping one of a n-type dopant and a p-type dopant ([0066]&[0068]).

Regarding Claim 33, the combination of Park, Bauer and Rotondaro makes obvious the method of Claim 1, wherein the passivation layer is formed by the non-selective deposition using a precursor that includes monomethylsilane (MMS) and at least one of silane (SiH.sub.4) and disilane (SiH.sub.6) (Bauer, [0085]&[0086]).

Claims 8 and 9 are rejected under 35 U.S.C. 103 as being unpatentable over the combination of Park and Bauer as applied to Claim 1 above and in view of US PG Pub 2007/0249168 to Rotondaro et al. (hereinafter Rotondaro).

Regarding Claim 8, the combination of Park and Bauer makes obvious the method of Claim 1 but does not disclose a fluorine treatment.

Rotondaro discloses a method for forming S/D freatures involving a fluorine treatment before growing a semiconductor material [0040].

It would have been obvious to one of ordinary skill in the art, before the effective filing date of the invention, to have modified the method of Park to include a fluorine treatment step. In the art, it is known that a clean surface is preferential for growing a semiconductor material to avoid defects. While Rotondaro performs the cleaning process on the substrate, the principle would apply to silicon containing layers including the passivation layer of Park. Absent any unexpected results, it would have been obvious to one of general skill in the art to perform a cleaning process before growing additional layers to ensure a defect free source/drain feature.

Regarding Claim 9, the combination of Park, Bauer and Rotondaro makes obvious the method of Claim 8 but does not explicitly disclose the fluorine dose range.

However, absent any unexpected results, it would have been obvious to one of ordinary skill in the art, before the invention was made, so select a range of dosing between 1x10.sup.14 to 2x10.sup.15 ions/cm .sup.2 since it has been held that where the general conditions of a claim are disclosed in the prior art (ie, fluorine plasma cleaning of silicon surfaces) discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233. Applicant has not noted that the specified range solves any particular problem or is otherwise critical in developing the source/drain features. The specific range of dosing would depend on obvious factors such as temperature and/or duration for the fluorine treatment. Absent any unexpected results, it would have been obvious to one of general skill in the art to perform a cleaning process at a range suitable to ensure a defect free source/drain feature.

Claims 11-14 are rejected under 35 U.S.C. 103 as being unpatentable over the combination of Park and Bauer as applied to Claim 1 above and in further view of US PG Pub 2012/0295427 to Bauer (hereinafter Bauer‘427).

Regarding Claim 11, the combination of Park and Bauer discloses the method of Claim 1 but does not disclose the use of a CDE process.

Bauer’437 discloses a process for epitaxially depositing stressor material for a source/drain feature wherein the epitaxially growing of the material includes performing a cyclic deposition and etching (CDE) process [0046].

It would have been obvious to one of ordinary skill in the art, before the effective filing date of the invention, to have modified the method of Park to comprise a CDE process. As would have been known at the time of the invention, a CDE process allows for a high quality semiconductor layer to be formed by removing poorly formed portions throughout the process. A cyclic deposition process would provide the high quality layers for stressing the channel while also providing the flexibility for adding dopants in subsequent cycles.

Regarding Claim 12, the combination of Park, Bauer and Bauer'427 makes obvious the method of Claim 11, wherein the CDE process includes a first cycle for deposition and a second cycle for etching; and the second cycle uses a chlorine-containing gas that includes at least one of HCl and Cl.sub.2 (Bauer'427, [0029]).

Regarding Claim 13, the combination of Park, Bauer and Bauer'427 makes obvious the method of Claim 12, wherein the first cycle of the CDE process uses a precursor that includes PH.sub.3, monomethylsilane (MMS), and at least one of SiH.sub.4 and Si.sub.2H.sub.6 (Bauer'427, [0039]&[0041]).

Regarding Claim 14, the combination of Park, Bauer and Bauer'427 makes obvious the method of Claim 12, wherein the first cycle of the CDE process uses a precursor that includes B.sub.2H.sub.6, GeH.sub.4, and at least one of SiH.sub.4 and Si.sub.2H.sub.6 (Bauer'427, [0039]&[0042]),

Claims 15, 16 and 20 are rejected under 35 U.S.C. 103 as being unpatentable over US PG Pub 2015/0155386 to Hung et al. (hereinafter Hung).

Regarding Claim 15, Hung discloses a method of forming a field effect transistor (FET), the method comprising:

performing an etching process to a semiconductor substrate, thereby forming recesses in source and drain (S/D) regions of the semiconductor substrate (Figs. 5, 6); and

epitaxially growing a semiconductor material by a deposition process with a varying etching/deposition (E/D) factor, thereby forming S/D features in the recesses, wherein the deposition process includes a co-flow epitaxy growth (Fig. 9, [0038]).

Regarding Claim 16, Hung discloses the method of Claim 15, wherein the deposition process incudes a first deposition step having a first etch/deposition (E/D) factor and thereafter a second

deposition step having a second E/D factor greater than the first E/D factor (*i.e. an increase in the Ge source gas*).

Regarding Claim 19, Hung discloses the method of claim 15, wherein the deposition process includes a combination of the co-flow epitaxy growth and a cyclic deposition and etching (CDE) process [0038].

Regarding Claim 20, Hung discloses the method of Claim 15, wherein the epitaxially growing of the semiconductor material includes varying the E/D factor by a mechanism selected from gas partial pressure, gas flow rate, substrate temperature, and a combination thereof (*an increase in the Ge source gas*).

Claims 17 is rejected under 35 U.S.C. 103 as being unpatentable over Hung as applied to Claim 16 above and in further view of Bauer'427

Regarding Claim 17, Hung discloses the method of Claim 16, wherein he second deposition step is a selective deposition (cyclic selective epitaxial deposition).

Hung does not disclose the first deposition step as a non-selective deposition.

Bauer'427 discloses the use of a combination of non-selective deposition and selective deposition (blanket deposition followed by selective cyclical processes) [0078]-[0079].

It would have been obvious to one of ordinary skill in the art, before the effective filing date of the invention, to have modified the method of Hung to include a non-selective deposition for the first deposition step. Forming a blanket deposit, or non-selective, initial step would have provided obvious benefits known in the art for non-selective deposition such as avoiding defects while the following deposition steps could selective as the process achieves a higher throughput over blanket deposition (Bauer'427,[0079]).

Claims 27-29, 31 and 32 are rejected under 35 U.S.C. 103 as being unpatentable over Park in view of Bauer and Rotondaro.

Regarding Claim 27, Park discloses a method of forming a field effect transistor (FET), the method comprising:

performing an etching process to a semiconductor substrate (Fig. 5, substrate 110), thereby forming recesses (111 a,111 b) in source and drain (S/D) regions of the semiconductor substrate;

forming a passivation material layer (131) of a first semiconductor material (SiC; [0035]) in the recess; and

epitaxially growing a second semiconductor material (SiGe; [0039]) over the passivation material layer, thereby forming S/D features in the recesses, wherein the first semiconductor material is different than the second semiconductor material (SiC for the first and SiGe for the second).

Park does not disclose the use of a non-selective deposition process for the formation of the passivation material layer.

Bauer discloses a method of forming SiC in S.D regions by performing a non-selective deposition process using a precursor free of chlorine [0100].

It would have been obvious to one of ordinary skill in the art, before the effective filing date of the invention, to have modified the method used by Park to use a non-selective deposition, free of chlorine as a precursor. As noted by Bauer in paragraph [0100], using a non-selective process with precursors such as trisilane and a carbon source would result in a carbon rich layer. Such a layer would have had benefits obvious to one of ordinary skill in the art such as preventing dopants from diffusing into the channel region or otherwise leaking from the S/D features, a desire Park notes in paragraph [0033].

Park does not disclose performing a fluorine treatment to the passivation layer.

Rotondaro discloses a method for forming S/D freatures involving a fluorine treatment before growing a semiconductor material [0040].

It would have been obvious to one of ordinary skill in the art, before the invention was made, to have modified the method of Park to include a fluorine treatment step. In the art, it is known that a clean surface is preferential for growing a semiconductor material to avoid defects. While Rotondaro performs the cleaning process on the substrate, the principle would apply to silicon containing layers including the passivation layer of Park. Absent any unexpected results, it would have been obvious to one of general skill in the art to perform a cleaning process before growing additional layers to ensure a defect free source/drain feature.

Regarding Claim 28, the combination of Park, Bauer and Rotondaro makes obvious the method of Claim 27, wherein the fluorine treatment is a fluorine plasma treatment [0042],

Regarding Claim 29, the combination of Park, Bauer and Rotondaro makes obvious the method of Claim 27 but does not disclose the fluorine dose range.

However, absent any unexpected results, it would have been obvious to one of ordinary skill in the art, before the invention was made, so select a range of dosing between 1x10.sup.14 to 2x10.sup.15 since it has been held that where the general conditions of a claim are disclosed in the prior art (ie, fluorine plasma cleaning of silicon surfaces) discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233. Applicant has not noted that the specified range solves any particular problem or is otherwise critical in developing the source/drain features. The specific range of dosing would depend on obvious factors such as temperature and/or duration for the fluorine treatment. Absent any unexpected results, it would have been obvious to one of general skill in the art to perform a cleaning process at a range suitable to ensure a defect free source/drain feature.

Regarding Claim 30, the combination of Park, Bauer and Rotondaro makes obvious the method of Claim 27, wherein the forming of the passivation layer includes performing the non-selective process using a precursor free of chlorine (Park, [0062]) and the epitaxially growing of the second semiconductor material includes an etching process using a chlorine-containing gas (Park, [0065]).

Regarding Claim 31, the combination of Park, Bauer and Rotondaro makes obvious the method of Claim 27, wherein the forming of the passivation material layer includes epitaxially growing the first semiconductor material that is free of dopant, using the precursor free of dopant-containing gas ([0062]; Park leaves the passivation material layer free of dopants to block the diffusion of dopants from the second semiconductor material [0033]).

Regarding Claim 32, the combination of Park, Bauer and Rotondaro makes obvious the method of Claim 31, wherein the epitaxially growing of the second semiconductor material includes in-situ doping one of a n-type dopant and a p-type dopant to the second semiconductor material (Park; [0066]&[0068]).

Regarding Claim 34, the combination of Park, Bauer and Rotondaro makes obvious the method of Claim 37, wherein the passivation layer is formed by the non-selective deposition using a precursor that includes monomethylsilane (MMS) and at least one of silane (SiH.sub.4) and disilane (SiH.sub.6) (Bauer, [0085]&[0086]).

Allowable Subject Matter

Claim 18 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 18 discloses the method of Claim 16, wherein the first deposition step has a first substrate temperature less than 620.degree.C; and the second deposition step has a second substrate temperature greater than 620.degree.C. A search of relevant references in the art does not show this to be anticipated

or obvious. While it's known in the art that some methods such as the selection of Cl.sub.2 as an etchant can lower the processing temperature (US PG Pub 2006/0115934. [0027]), the references of record do not single out Cl.sub.2 as a preferred chlorine based etchant, nor do they note a temperature differences between CDE steps.

Response to Arguments

Applicant's arguments with respect to Claim 15 have been considered but are moot because the arguments do not apply to the current rejection.

Applicant's arguments filed 10/04/2017, with respect to Claims 1 and 27 have been fully considered but they are not persuasive.

Applicant's arguments with regards to Liao and Park are not pertinent as the rejection is in view of Bauer.

With regards to Bauer, Applicant argues that a combination of Bauer and Park would change or destroy the functionality of Park's upper layers 132 and 133 since they are used to provide stress on the channel but layer 131, if formed using the method disclosed by Bauer, would already be imparting stress on the channel. However, layer 131 is grown in Park to apply tensile stress to a channel region [0035]. Given this, it appears that Bauer's SiC layer imparting stress on the channel region seems to be compatible with the SiC layer of Park. It is not apparent, from Applicant's arguments, why the method of Bauer would alter the stress that Park is already seeking to achieve in such a manner that changes or destroys the functionality of the source/drain regions 132/133. Therefore, Examiner does not find the arguments to be persuasive.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DAVID SPALLA whose telephone number is (303)297-4298. The examiner can normally be reached on Mon-Fri 10am-5pm MST.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Such can be reached on (571) 272-8895. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/DAVID SPALLA/
Examiner, Art Unit 2896

Notice of References Cited	Application/Control No. 14/597,115	Applicant(s)/Patent Under Reexamination TSAI ET AL.	
	Examiner DAVID SPALLA	Art Unit 2896	Page 1 of 1

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*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-2012/0091469 A1	04-2012	Park; Keum-Seok	H01L29/0847	257/77
*	B	US-2006/0234504 A1	10-2006	Bauer; Matthias	C23C16/04	438/674
*	C	US-2012/0295427 A1	11-2012	Bauer; Matthias	H01L21/02532	438/494
*	D	US-2007/0249168 A1	10-2007	Rotondaro; Antonio Luis Pacheco	H01L21/30608	438/700
*	E	US-2015/0155386 A1	06-2015	Hung; Yu-Hsiang	H01L29/7848	257/401
	F	US-				
	G	US-				
	H	US-				
	I	US-				
	J	US-				
	K	US-				
	L	US-				
	M	US-				

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14597115	TSAI ET AL.
	Examiner	Art Unit
	DAVID SPALLA	2896

CPC- SEARCHED		
Symbol	Date	Examiner
H01L 29/66636, 7848	06/23/2016	DCS
H01L 29/165, 167	12/11/2017	DCS

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
45			

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

SEARCH NOTES		
Search Notes	Date	Examiner
Search of submitted IDS references	06/23/2016	DCS
See attached EAST search history	06/23/2016	DCS
See attached EAST updated search history	04/30/2017	DCS
See attached EAST updated search history	12/11/2017	DCS

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

/DAVID SPALLA/ Examiner.Art Unit 2896	

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	11200634	@ad<"20140822" @rlad<"20140822" @pt1d<"20140822"	US-PGPUB; USPAT; USOCR	OR	ON	2017/12/11 11:50
L2	10901	H01L29/66636,7848,165,167.cpc.	US-PGPUB; USPAT; USOCR	OR	ON	2017/12/11 11:50
L3	26	(coflow co-flow) and L1 and L2	US-PGPUB; USPAT; USOCR	OR	ON	2017/12/11 11:50
L5	18	"8598003"	US-PGPUB; USPAT; USOCR	OR	ON	2017/12/11 12:04
L6	45	(coflow$3 co-flow$3) and L1 and L2	US-PGPUB; USPAT; USOCR	OR	ON	2017/12/11 12:05
L7	2	"20150155386"	US-PGPUB; USPAT; USOCR	OR	ON	2017/12/11 12:43
L10	144	l1 and 2 and ("non-selective" with (deposit$4 growth))	US-PGPUB; USPAT; USOCR	OR	ON	2017/12/11 12:50
L12	22	(US-20030136985-$ or US-20150236157-$ or US-20130049101-$ or US-20080315254-$ or US-20140197455-$ or US-20140246710-$ or US-20140264348-$ or US-20060234504-$ or US-20120295427-$ or US-20090104739-$ or US-20060115933-$ or US-20070249168-$ or US-20100093147-$ or US-20140197493-$ or US-20140264636-$ or US-20120091469-$ or US-20130183814-$ or US-20150155386-$ or US-20070287272-$ or US-20080182075-$).did. or (US-8785285-$ or US-9064892-$).did.	US-PGPUB; USPAT	OR	ON	2017/12/11 13:01
L13	7	12 and non-selective	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	ON	2017/12/11 13:01
S2	10680640	@ad<"20140822" @rlad<"20140822"	US-	OR	ON	2016/06/13

		@pt1d<"20140822"	PGPUB; USPAT; USOCR			10:07
S3	0	"14813556"	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/13 10:46
S4	1	"14597115"	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/13 13:33
S7	10680640	@ad<"20140822" @rlad<"20140822" @pt1d<"20140822"	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/13 13:36
S9	15	("7667271" | "8362575" | "8367498" | "8440517" | "8497528" | "8610240" | "8680576" | "8723272" | "8729634" | "8785285" | "8796759" | "8809139" | "8828823" | "8836016" | "8841701").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/13 13:41
S10	24	("20030052406" | "20060057859" | "20070059875" | "20070111439" | "20070128782" | "20070131969" | "20070145487" | "20080044960" | "20080251851" | "20090239344" | "20090280612" | "20100252816" | "20110147828" | "20120068193" | "20120104470" | "3909304" | "7112848" | "7132338" | "7518196" | "7910415" | "8110486" | "8338259").PN. OR ("8785285").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/13 13:44
S12	9538	fluorine adj3 (plasma treatment)	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/13 13:53
S14	10680640	@ad<"20140822" @rlad<"20140822" @pt1d<"20140822"	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/13 14:05
S15	4124	H01L29/66636.cpc.	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/13 14:05
S16	1731	S14 and S15 and ((silicon adj carbide) SiC) and ((silicon adj germanium) SiGe)	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/13 14:05
S17	31	S16 and (fluorine adj3 (plasma treat$4 clean$3))	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/13 14:12
S18	700	S14 and S15 and ((silicon adj carbide) SiC) and ((second upper) with ((silicon adj germanium) SiGe))	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/13 14:23
S19	260	S18 and (treat$3 clean$3)	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/13 14:27

S20	10686366	@ad<"20140822" @rlad<"20140822" @pt1d<"20140822"	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/15 15:31
S21	4131	H01L29/66636.cpc.	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/15 15:31
S22	103	S20 and S21 and (non-selective)	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/15 15:31
S23	2	S20 and S21 and ((non-selective) same precursor same (SiC (silicon adj2 carbide)))	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/15 15:39
S24	94	H01L29/66636.cpc. and (SiC same dop$3 same (prevent block$3 barrier diffusion))	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/17 17:53
S25	10690365	@ad<"20140822" @rlad<"20140822" @pt1d<"20140822"	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/17 18:16
S26	4134	H01L29/66636.cpc.	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/17 18:16
S27	5	S25 and S26 and ((non-selective) same cycle)	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/17 18:16
S28	9	S25 and S26 and ((non-selective) same (cyclic cycle))	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/17 18:18
S29	120	S25 and S26 and ((cyclic cycle) same (vary$3 chang$3 alter$3 rate factor))	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/17 18:19
S30	44	S25 and S26 and (((cyclic cycle) adj3 deposit$3) same (vary$3 chang$3 alter$3 rate factor))	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/17 18:20
S31	24	S25 and S26 and (((cyclic cycle) adj3 deposit$3) same (vary$3 chang$3 alter$3 rate factor)) and (degree celsius)	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/17 18:24
S32	0	S25 and S26 and (((cyclic cycle) adj3 deposit$3) same (vary$3 chang$3 alter$3 rate factor)) and ".degree."	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/17 18:30
S33	24	S25 and S26 and (((cyclic cycle) adj3 deposit$3) same (vary$3 chang$3 alter$3 rate factor)) and degree	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/17 18:31
S34	40	S25 and S26 and (((cyclic cycle) adj3 deposit$3) same (vary$3 chang$3 alter$3 rate factor)) and $4degree	US-PGPUB; USPAT;	OR	ON	2016/06/17 18:31

			USOCR			
S35	2	"20060234504"	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/21 15:48
S36	2	"20130328126"	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/21 15:55
S37	10698055	@ad<"20140822" @rlad<"20140822" @pt1d<"20140822"	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/23 16:27
S38	2137	S37 and (((cyclic cycle) adj3 deposit$3) same (vary$3 chang$3 alter$3 rate factor))	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/23 16:27
S39	3183	S37 and ((((cyclic cycle) adj3 deposit$3) CDE) same (vary$3 chang$3 alter$3 rate factor))	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/23 16:28
S40	661	S37 and ((((cyclic cycle) adj3 deposit$3) CDE) same (vary$3 chang$3 alter$3 rate factor)) and ((((cyclic cycle) adj3 deposit$3) CDE) same $4degree)	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/23 16:29
S42	335	S37 and ((((cyclic cycle) adj3 deposit$3) CDE) same (vary$3 chang$3 alter$3 rate factor)) and ((((cyclic cycle) adj3 deposit$3) CDE) same $4degree) and ((source drain source/drain s/d) with (deposit$3 epitax$5))	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/23 16:32
S43	9	S37 and (((cyclic cycle) adj3 deposit$3) CDE) with (non-selective (non adj selective)) with selective	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/23 16:51
S45	18	S37 and ((((cyclic cycle) adj3 deposit$3) CDE) same (non-selective (non adj selective)) same selective)	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/23 16:52
S46	98695	S37 and ((fluorine fluoride) with (treat$4 clean$3 process))	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/23 17:18
S47	4157	H01L29/66636.cpc.	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/23 17:19
S48	258	S37 and ((fluorine fluoride) with (treat$4 clean$3 process)) and S47	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/23 17:19
S49	86	S37 and ((fluorine fluoride) with (treat$4 clean$3 process) with plasma) and S47	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/23 17:20
S50	14	(US-20030136985-$ or US-20150236157-$ or US-20130049101-$ or US-20080315254-$ or US-20140197455-$ or US-20140246710-$ or US-20140264348-$	US-PGPUB; USPAT	OR	ON	2016/06/23 17:34

		or US-20060234504-$ or US-20120295427-$ or US-20090104739-$ or US-20060115933-$ or US-20070249168-$).did. or (US-8785285-$ or US-9064892-$).did.				
S51	95	S37 and ((fluorine fluoride) with (treat$4 clean$3 process) with plasma) and H01L29/7848.cpc.	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/23 17:34
S52	73	S37 and ((((cyclic cycle) adj3 deposit$3) CDE) same (vary$3 chang$3 alter$3 rate factor)) and ((((cyclic cycle) adj3 deposit$3) CDE) same $4degree) and ((source drain source/drain s/d) with (deposit$3 epitax$5)) and "cl.sub.2"	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/23 18:21
S53	58	S37 and ((((cyclic cycle) adj3 deposit$3) CDE) same (vary$3 chang$3 alter$3 rate factor)) and ((((cyclic cycle) adj3 deposit$3) CDE) same $4degree) and ((source drain source/drain s/d) with (deposit$3 epitax$5)) and ("cl.sub.2" same temperature)	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/23 18:23
S54	4698	H01L29/66636.cpc.	US-PGPUB; USPAT; USOCR	OR	ON	2017/04/30 18:23
S55	11016021	@ad<"20140822" @rlad<"20140822" @pt1d<"20140822"	US-PGPUB; USPAT; USOCR	OR	ON	2017/04/30 18:23
S56	1111	(((silicon adj carbide) SiC) with (buffer passivation)) and ((silicon adj germanium) SiGe)	US-PGPUB; USPAT; USOCR	OR	ON	2017/04/30 18:24
S57	24	S54 and S55 and S56	US-PGPUB; USPAT; USOCR	OR	ON	2017/04/30 18:24
S58	2	"20060234504"	US-PGPUB; USPAT; USOCR	OR	ON	2017/04/30 18:54
S59	15	(US-20030136985-$ or US-20150236157-$ or US-20130049101-$ or US-20080315254-$ or US-20140197455-$ or US-20140246710-$ or US-20140264348-$ or US-20060234504-$ or US-20120295427-$ or US-20090104739-$ or US-20060115933-$ or US-20070249168-$ or US-20100093147-$).did. or (US-8785285-$ or US-9064892-$).did.	US-PGPUB; USPAT	OR	ON	2017/04/30 19:01
S60	1	S59 and (co-flow)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	ON	2017/04/30 19:01
S61	3	S54 and S55 and (varying adj2 etching)	US-PGPUB;	OR	ON	2017/04/30 19:42

			USPAT; USOCR			
S62	4	S54 and S55 and ((SiC (silicon adj2 carbide)) same co-flow)	US-PGPUB; USPAT; USOCR	OR	ON	2017/04/30 19:47
S63	11	((SiC (silicon adj2 carbide)) same co-flow)	US-PGPUB; USPAT; USOCR	OR	ON	2017/04/30 19:48
S64	10	S55 and S63	US-PGPUB; USPAT; USOCR	OR	ON	2017/04/30 19:49
S65	2	(("etching/deposition" "E/D") adj2 factor)	US-PGPUB; USPAT; USOCR	OR	ON	2017/04/30 19:50
S66	92	(varying increasing decreasing) with ((cyclic adj2 deposition) CDE)	US-PGPUB; USPAT; USOCR	OR	ON	2017/04/30 19:51
S67	77	S55 and S66	US-PGPUB; USPAT; USOCR	OR	ON	2017/04/30 19:51
S68	0	S55 and S66 and co-flow	US-PGPUB; USPAT; USOCR	OR	ON	2017/04/30 19:52
S69	189	(("etching/deposition" "E/D") adj2 ratio)	US-PGPUB; USPAT; USOCR	OR	ON	2017/04/30 19:53
S70	0	S55 and S69 and co-flow	US-PGPUB; USPAT; USOCR	OR	ON	2017/04/30 19:55
S71	0	S55 and S69 and "co-flow"	US-PGPUB; USPAT; USOCR	OR	ON	2017/04/30 19:55
S72	9	S55 and ((cyclic adj2 deposition) CDE) and "co-flow"	US-PGPUB; USPAT; USOCR	OR	ON	2017/04/30 19:55
S73	11	((cyclic adj2 deposition) CDE) and "co-flow"	US-PGPUB; USPAT; USOCR	OR	ON	2017/04/30 19:58
S74	220	((etching with deposition) "E/D") adj2 (factor ratio)	US-PGPUB; USPAT; USOCR	OR	ON	2017/04/30 19:59
S75	0	S55 and S74 and co-flow	US-PGPUB; USPAT; USOCR	OR	ON	2017/04/30 20:00

S76	214	S55 and S74	US-PGPUB; USPAT; USOCR	OR	ON	2017/04/30 20:00
S77	12	((etching with deposition) "E/D") adj2 (factor ratio) same (CL HCL "CL.sub.2" CL2)	US-PGPUB; USPAT; USOCR	OR	ON	2017/04/30 20:01
S78	11	S55 and S77	US-PGPUB; USPAT; USOCR	OR	ON	2017/04/30 20:01
S79	46	S55 and ((cyclic adj2 deposition) CDE) with continuous	US-PGPUB; USPAT; USOCR	OR	ON	2017/04/30 20:15
S80	68	S55 and (((cyclic adj2 deposition) CDE) with constant)	US-PGPUB; USPAT; USOCR	OR	ON	2017/04/30 20:17
S81	109	(S79 S80)	US-PGPUB; USPAT; USOCR	OR	ON	2017/04/30 20:37
S82	18	(US-20030136985-$ or US-20150236157-$ or US-20130049101-$ or US-20080315254-$ or US-20140197455-$ or US-20140246710-$ or US-20140264348-$ or US-20060234504-$ or US-20120295427-$ or US-20090104739-$ or US-20060115933-$ or US-20070249168-$ or US-20100093147-$ or US-20140197493-$ or US-20140264636-$ or US-20120091469-$).did. or (US-8785285-$ or US-9064892-$).did.	US-PGPUB; USPAT	OR	ON	2017/12/11 10:30
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S85	10901	H01L29/66636,7848,165,167.cpc.	US-PGPUB; USPAT; USOCR	OR	ON	2017/12/11 10:32

EAST Search History (Interference)

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12/11/2017 1:40:29 PM
C:\Users\dspalla\Documents\EAST\Workspaces\14597115.wsp

In place of PTO-1449 Form	U. S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE			*Complete if Known*	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(use as many sheets as necessary)*				Application Number	14/597,115
				Filing Date	January 14, 2015
				First Inventor Name	Chun Hsiung Tsai et al.
				Art Unit	2896
				Examiner Name	SPALLA, DAVID C
SHEET	1	OF	1	Attorney Docket Number	2014-0937/24061.2998

U. S. PATENTS

Examiner's Initials	Cite No.	Document Number	Issue Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document
	A1	8598003	12-03-2013	Murthy et al.

U. S. PATENT APPLICATION PUBLICATIONS

Examiner's Initials	Cite No.	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document

FOREIGN PATENT DOCUMENTS

Examiner's Initials	Cite No.	Foreign Patent Document (Country Code – Number – Kind)	Publication Date MM-DD-YYYY	Patentee or Applicant of Cited Document	Translation Y/N
	B1	KR 10-2012-0086369	08-02-2012	INTEL CORP.	Y, Corresponding U.S. Pat. 8598003

NON-PATENT LITERATURE DOCUMENTS

Examiner's Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article, title of the item, date, page(s), volume-issue number(s), publisher, city/country where published
	A1	
	A2	
	A3	
	A4	
	A5	

Examiner Signature	/DAVID C SPALLA/	Date Considered	12/11/2017

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include a copy of this form with next communication to applicant.

Doc code: RCEX
Doc description: Request for Continued Examination (RCE)

PTO/SB/30EFS (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
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REQUEST FOR CONTINUED EXAMINATION(RCE)TRANSMITTAL
(Submitted Only via EFS-Web)

Application Number	14597115	Filing Date	2015-01-14	Docket Number (if applicable)	20140937/24061.2998	Art Unit	2896
First Named Inventor	Chun Hsiung Tsai			Examiner Name	Spalla, David C.		

This is a Request for Continued Examination (RCE) under 37 CFR 1.114 of the above-identified application.
Request for Continued Examination (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, or to any design application. The Instruction Sheet for this form is located at WWW.USPTO.GOV

SUBMISSION REQUIRED UNDER 37 CFR 1.114

Note: If the RCE is proper, any previously filed unentered amendments and amendments enclosed with the RCE will be entered in the order in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).

☐ Previously submitted. If a final Office action is outstanding, any amendments filed after the final Office action may be considered as a submission even if this box is not checked.

☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____

☐ Other _____

☒ Enclosed

☒ Amendment/Reply

☐ Information Disclosure Statement (IDS)

☐ Affidavit(s)/ Declaration(s)

☒ Other Extension of Time (2mo.)

MISCELLANEOUS

☐ Suspension of action on the above-identified application is requested under 37 CFR 1.103(c) for a period of months _____ (Period of suspension shall not exceed 3 months; Fee under 37 CFR 1.17(i) required)

☐ Other _____

FEES

☒ **The RCE fee under 37 CFR 1.17(e) is required by 37 CFR 1.114 when the RCE is filed.**
The Director is hereby authorized to charge any underpayment of fees, or credit any overpayments, to Deposit Account No 081394

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

X Patent Practitioner Signature

Applicant Signature

PTO/SB/30EFS (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
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Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Signature of Registered U.S. Patent Practitioner			
Signature	/Michael E. Ramon/	Date (YYYY-MM-DD)	2017-10-04
Name	Michael E. Ramon	Registration Number	52147

This collection of information is required by 37 CFR 1.114. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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The information provided by you in this form will be subject to the following routine uses:

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5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of: Chun Hsiung Tsai *et al.*	§	Docket No.: 2014-0937/24061.2998
Application No. 14/597,115	§	Art Unit: 2896
Filing Date: January 14, 2015	§	Examiner: Spalla, David C.
Entitled: METAL-INSENSITIVE EPITAXY FORMATION	§	Confirmation No.: 8745

Mail Stop: Amendment
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE TO FINAL OFFICE ACTION DATED MAY 8, 2017

Applicants respectfully submit this paper in response to the Final Office Action mailed on May 8, 2017, setting a period for reply to expire on August 8, 2017. A petition for a two-month extension of time is attached, extending the period for reply to October 8, 2017. Entry of the following amendments and comments into the record of the above-identified application is respectfully requested.

Any fees required by this paper are being provided as directed in an electronic submission of this paper or in a transmittal letter accompanying this paper. However, the Commissioner is hereby authorized to charge any deficiency in fees required by this paper and any additional fees under 37 C.F.R. § 1.16 or 1.17 which may be required during the pendency of this application, and to similarly credit any overpayment, to Haynes and Boone, LLP's Deposit Account 08-1394.

Amendments to the Claims are reflected in the listing of claims which begins on page **2** of this paper.

Remarks/Arguments begin on page **7** of this paper.

Listing of Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (***Currently Amended***) A method of forming a field effect transistor (FET), the method comprising:

performing an etching process to a semiconductor substrate, thereby forming recesses in source and drain (S/D) regions of the semiconductor substrate;

forming, by a non-selective deposition process, a passivation material layer of a first semiconductor material in the recesses; and

epitaxially growing a second semiconductor material on the passivation material layer, thereby forming S/D features in the recesses, wherein the S/D features are separated from the semiconductor substrate by the passivation material layer, and wherein the first semiconductor material is different than the second semiconductor material.

2. (***Currently Amended***) The method of claim 1, wherein the forming of the passivation material layer includes performing [[a]]the non-selective deposition process using a precursor free of chlorine.

3. (Previously Presented) The method of claim 2, wherein the forming of the passivation material layer includes epitaxially growing the passivation material layer of the first semiconductor material.

4. (Original) The method of claim 3, wherein the first semiconductor material includes silicon carbide and the second semiconductor material includes silicon germanium.

5. (Previously Presented) The method of claim 3, wherein the forming of the passivation material layer includes epitaxially growing the passivation material layer of the first semiconductor material that is free of dopant, using the precursor free of dopant-containing gas.

6. (Previously Presented) The method of claim 3, wherein the forming of the passivation material layer includes forming a silicon carbide layer having a carbon atomic percentage ranging from 1.8% to 3%.

7. (Previously Presented) The method of claim 1, wherein the forming of the passivation material layer includes forming the passivation material layer with a thickness ranging from 1 nm to 4 nm, effectively preventing interaction between chlorine and metal residuals under the passivation material layer.

8. (Original) The method of claim 1, further comprising performing a fluorine treatment to the passivation material layer before the epitaxially growing of the second semiconductor material.

9. (Previously Presented) The method of claim 8, wherein the performing of the fluorine treatment includes performing the fluorine treatment with a fluorine dose ranging from 1×10^{14} ions/cm^2 to 2×10^{15} ions/cm^2.

10. (Original) The method of claim 1, wherein the epitaxially growing of the second semiconductor material includes epitaxially growing the second semiconductor material with in-situ doping one of a n-type dopant and a p-type dopant.

11. (Original) The method of claim 1, wherein the epitaxially growing of the second semiconductor material includes performing a cyclic deposition and etching (CDE) process.

12. (Original) The method of claim 11, wherein

the CDE process includes a first cycle for deposition and a second cycle for etching; and

the second cycle uses a chlorine-containing gas that includes at least one of HCl and Cl_2.

13. (Original) The method of claim 12, wherein the first cycle of the CDE process uses a precursor that includes PH_3, monomethylsilane (MMS), and at least one of SiH_4 and Si_2H_6.

14. (Original) The method of claim 12, wherein the first cycle of the CDE process uses a precursor that includes B_2H_6, GeH_4, and at least one of SiH_4 and Si_2H_6.

15. (Previously Presented) A method of forming a field effect transistor (FET), the method comprising:

performing an etching process to a semiconductor substrate, thereby forming recesses in source and drain (S/D) regions of the semiconductor substrate; and

epitaxially growing a semiconductor material by a deposition process with a varying etching/deposition (E/D) factor, thereby forming S/D features in the recesses, wherein the deposition process includes a co-flow epitaxy growth.

16. (Original) The method of claim 15, wherein the deposition process incudes a first deposition step having a first etch/deposition (E/D) factor and thereafter a second deposition step having a second E/D factor greater than the first E/D factor.

17. (Previously Presented) The method of claim 16, wherein

the first deposition step is a non-selective deposition; and

the second deposition step is a selective deposition.

18. (Previously Presented) The method of claim 16, wherein

the first deposition step has a first substrate temperature less than 620 ^{0}C; and

the second deposition step has a second substrate temperature greater than 620 ^{0}C.

19. (Previously Presented) The method of claim 15, wherein the deposition process includes a combination of the co-flow epitaxy growth and a cyclic deposition and etching (CDE) process.

20. (Original) The method of claim 15, wherein the epitaxially growing of the semiconductor material includes varying the E/D factor by a mechanism selected from gas partial pressure, gas flow rate, substrate temperature, and a combination thereof.

21-26. (Canceled)

27. (***Currently Amended***) A method of forming a field effect transistor (FET), the method comprising:

performing an etching process to a semiconductor substrate, thereby forming recesses in source and drain (S/D) regions of the semiconductor substrate;

forming, by a non-selective deposition process, a passivation layer of a first semiconductor material in the recesses;

performing a fluorine treatment to the passivation layer; and

epitaxially growing a second semiconductor material over the passivation layer, thereby forming S/D features in the recesses, wherein the first semiconductor material is different than the second semiconductor material.

28. (Previously Presented) The method of claim 27, wherein the fluorine treatment is a fluorine plasma treatment.

29. (Previously Presented) The method of claim 27, wherein the fluorine treatment uses a fluorine dose ranging from 1×10^{14} ions/cm^2 to 2×10^{15} ions/cm^2.

30. (***Currently Amended***) The method of claim 27, wherein the forming of the passivation layer includes performing [[a]]the non-selective deposition process using a precursor free of chlorine; and the epitaxially growing of the second semiconductor material includes an etching process using a chlorine-containing gas.

31. (Previously Presented) The method of claim 27, wherein the forming of the passivation layer includes epitaxially growing the first semiconductor material that is free of dopant, using a precursor free of dopant-containing gas.

32. (Previously Presented) The method of claim 31, wherein the epitaxially growing of the second semiconductor material includes in-situ doping one of a n-type dopant and a p-type dopant to the second semiconductor material.

33. (***New***) The method of claim 1, wherein the passivation material layer is formed by the non-selective deposition process using a precursor that includes monomethylsilane (MMS) and at least one of silane (SiH_4) and disilane (SiH_6).

34. (***New***) The method of claim 27, wherein the passivation layer is formed by the non-selective deposition process using a precursor that includes monomethylsilane (MMS) and at least one of silane (SiH_4) and disilane (SiH_6).

REMARKS

Claims 1-20 and 27-32 were previously pending, of which claims 1, 2, 27, and 30 have been amended, and claims 33 and 34 have been added. Reconsideration of presently pending claims 1-20 and 27-34 is respectfully requested in light of the above amendments and the following remarks.

Allowable Subject Matter

Claim 18 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all the limitations of the base claim and any intervening claims. In view of the deficiencies of the cited references, as discussed below, Applicants believe it would be premature to rewrite claim 18 in independent form, as suggested by the Office. Applicant also respectfully notes that claim 18 depends on and further limits claim 15 and is allowable for at least the reasons set forth in connection with independent claim 15.

Rejections Under 35 U.S.C. § 102(a)(1)

Claim 1 was rejected under 35 U.S.C. §102(a)(1) as being anticipated by Liao et al. (U.S. Patent Application Publication No. 2010/0093147, hereinafter referred to as "Liao"). Claims 1, 7, and 10 were rejected under 35 U.S.C. §102(a)(1) as being anticipated by Park et al. (U.S. Patent Application Publication No. 2012/0091469, hereinafter referred to as "Park"). With respect to the claims as herein amended, Applicants respectfully traverse these rejections.

Independent Claim 1

Amended claim 1 recites, in part:

> "forming, by a non-selective deposition process, a passivation material layer of a first semiconductor material in the recesses;."

The amendment to claim 1 finds support at least at paragraph [0065] of the present application. In the rejection of claim 1, the Examiner relies on Liao's first epitaxial layer 220 as allegedly disclosing the claimed "passivation material layer". OA at page 2. Amended claim 1 requires "forming, by a non-selective deposition process, a passivation material layer of a first

semiconductor material in the recesses…" Liao at paragraph [0020] states that "a first SEG process is performed to form a first epitaxial layer 220…" Thus, even assuming *arguendo* the Office's interpretation of Liao's first epitaxial layer 220, Liao does not teach or suggest "forming, by a non-selective deposition process, a passivation material layer of a first semiconductor material in the recesses", as positively recited in Applicants' amended claim 1. Thus, the Office has not shown how the relied upon portion of Liao discloses the Applicants' claimed method.

Therefore, the rejection of claim 1 is not supported by the Liao reference and should be withdrawn.

Additionally, in the rejection of claim 1, the Examiner relies on Park's silicon buffer layer 131 as allegedly disclosing the claimed "passivation material layer". OA at page 3. Park at paragraph [0035] states that "The silicon buffer layer 131 may be made of a material containing silicon carbide (SiC) prepared by selective epitaxial growth." Further, Park at paragraph [0042] states that "after the silicon buffer layer 131 is formed by selective epitaxial growth…" Thus, even assuming *arguendo* the Office's interpretation of Park's silicon buffer layer 131, Park does not teach or suggest "forming, by a non-selective deposition process, a passivation material layer of a first semiconductor material in the recesses", as positively recited in Applicants' amended claim 1. Thus, the Office has not shown how the relied upon portion of Park discloses the Applicants' claimed method.

Therefore, the rejection of claim 1 is not supported by the Park reference and should be withdrawn.

For avoidance of doubt, Bauer et al. (U.S. Patent Application Publication No. 2006/0234504, hereinafter referred to as "Bauer") is relied on in the rejection of claim 2 for disclosure of performing a non-selective deposition process. However, as previously argued in Applicants' response dated January 5, 2017, Bauer's Si-containing epitaxial layer 30 (e.g., SiC) is intended to exert strain on the channel region 22 (Bauer, paragraph [0067]). Bauer at paragraph [0103] states the "the SiC layer is selectively formed in recessed source/drain regions 20, and is preferably deposited under conditions (thickness, temperature) *that maintain stress*." (Emphasis added). On the contrary, Applicants' passivation layer is not used for, or intended to be used for, inducing strain. For instance, Applicants' paragraph [0037] states "The SiC layer… is *not suitable for strain effect*..." (Emphasis added).

In addition, combining Bauer's strain-exerting SiC layer with Liao's first epitaxial layer 220 and second epitaxial layer 222 could change or destroy the functionality of Liao's second epitaxial layer 222, which is used to provide channel stress. For example, Liao at paragraph [0025] states that "by forming the second epitaxial layer 222 near the channel region, proper stress is provided due to the higher Ge or C concentration of the second material…" Thus, as both Liao's second epitaxial layer 222 and Bauer's SiC layer are intended to exert strain (e.g., on a channel), the stress-inducing efficacy of each film is likely to be altered upon interaction with one another.

Therefore, even if the teachings of Bauer are exactly as the Office suggests, which Applicants do not admit, Bauer and Liao do not teach or suggest the limitations of Applicants' claim 1.

Similarly, combining Bauer's strain-exerting SiC layer with Park's silicon buffer layer 131, source region 132, and drain region 133 could change or destroy the functionality of Park's source and drain regions 132, 133, which are used to provide channel stress. For example, in discussing the source and drain regions 132, 133, Park at paragraph [0039] states that "the silicon germanium (SiGe) layer applies compressive stress to a channel…" Thus, as both Park's source and drain regions 132, 133 and Bauer's SiC layer are intended to exert strain (e.g., on a channel), the stress-inducing efficacy of each film is likely to be altered upon interaction with one another.

Therefore, even if the teachings of Bauer are exactly as the Office suggests, which Applicants do not admit, Bauer and Park do not teach or suggest the limitations of Applicants' claim 1.

Dependent Claims 2-14

Claims 2-14 depend on and further limit independent claim 1 and therefore are deemed to be patentable over the prior art, for at least the same reasons set forth above in connection with independent claim 1. Accordingly, the rejection of claims 2-14 should be withdrawn. Claim 2 was amended in view of the amendment to claim 1.

Rejections Under 35 U.S.C. §103

Claims 2-6 were rejected under 35 U.S.C. §103 as being unpatentable over Park as applied to claim 1, and in further view of Bauer. Claims 8 and 9 were rejected under 35 U.S.C. §103 as being unpatentable over Park as applied to claim 1, and in further view of Rotondaro et al. (U.S. Patent Application Publication No. 2007/0249168, hereinafter referred to as "Rotondaro"). Claims 11-14 were rejected under 35 U.S.C. §103 as being unpatentable over Park as applied to claim 1, and in further view of Bauer (U.S. Patent Application Publication No. 2012/0295427, hereinafter referred to as "Bauer '427"). Claims 15-17 and 19 were rejected under 35 U.S.C. §103 as being unpatentable over Tsai et al. (U.S. Patent Application Publication No. 2014/0264636, hereinafter referred to as "Tsai") in view of Tsai et al. (U.S. Patent Application Publication No. 2014/0264348, hereinafter referred to as "Tsai '348"). Claims 27-29, 31, and 32 were rejected under 35 U.S.C. §103 as being unpatentable over Park in view of Rotondaro. Claim 30 was rejected as being unpatentable over the combination of Park and Rotondaro as applied to claim 27, and in further view of Bauer.

With respect to the claims as herein amended, Applicants respectfully traverse these rejections on the grounds that the references are defective in establishing a *prima facie* case of obviousness.

Dependent Claims 2-6, 8, 9, and 11-14

As noted above, claims 2-6, 8, 9, and 11-14 depend on and further limit independent claim 1 and therefore are deemed to be patentable over the prior art, for at least the same reasons set forth above in connection with independent claim 1. Accordingly, the rejection of claims 2-6, 8, 9, and 11-14 should be withdrawn.

Independent Claim 15

The cited Tsai and Tsai '348 references are 35 USC 102(a)(2) art, and subject to 102(b)(2)(C)

The Examiner relies on the Tsai reference, discussed above, which as evidenced from the face of the publication, was effectively filed May 23, 2013 and published September 18, 2014. The present application claims priority from Provisional Application No. 62/040,880 and thus

was effectively filed August 22, 2014, after the filing date of the Tsai reference. The Examiner also relies on the Tsai '348 reference, discussed above, which as evidenced from the face of the publication, was effectively filed April 30, 2013 and published September 18, 2014. The present application claims priority from Provisional Application No. 62/040,880 and thus was effectively filed August 22, 2014, after the filing date of the Tsai '348 reference. Thus, as stated at page 7 of the present Action, it is apparent that the Examiner is using the Tsai reference and the Tsai '348 reference as prior art under 35 USC §102(a)(2), which is subject to 35 USC §102(b)(2)(C). 35 USC §102(b)(2)(C) states:

> A disclosure shall not be prior art to a claimed invention under subsection (a)(2) if the subject matter disclosed and the claimed invention, not later than the effective filing date of the claimed invention, were owned by the same person or subject to an obligation of assignment to the same person.

The Tsai reference and the present application, not later than the effective filing date of the claimed invention, were both subject to assignment to Taiwan Semiconductor Manufacturing Company, Ltd. as evidenced by the front page of the Tsai reference and associated assignment recorded in the Tsai reference (reel 030478, frame 0471), and the assignment recorded in the present application (reel 034716, frame 0071). Thus, the cited Tsai reference is not available art.

In addition, the Tsai '348 reference and the present application, not later than the effective filing date of the claimed invention, were both subject to assignment to Taiwan Semiconductor Manufacturing Company, Ltd. as evidenced by the front page of the Tsai '348 reference and associated assignment recorded in the Tsai '348 reference (reel 030314, frame 0062), and the assignment recorded in the present application (reel 034716, frame 0071). Thus, the cited Tsai '348 reference is not available art.

The Applicants note that the Tsai reference and the Tsai '348 reference have a different inventive entity than the present application. By stating that the Examiner has used the Tsai reference and the Tsai '348 under 102(a)(2), the Applicants are not admitting that any given claim or the cited Tsai reference and the Tsai '348 reference are indeed "by another."

While the Applicants do not agree with the characterizations of the Examiner of the references, or the rejection, these deficiencies are not required to be detailed herein as the Tsai reference and the Tsai '348 reference are not properly available prior art. Thus, the rejection of claim 15 based on the Tsai reference and the Tsai '348 reference should be withdrawn.

In addition, claims 16-20, which depend on and further limit claim 15, are allowable.

Dependent Claims 16, 17, 19, and 20

Claims 16, 17, 19, and 20 depend on and further limit independent claim 15 and therefore are deemed to be patentable over the prior art, for at least the same reasons set forth above in connection with independent claim 15. Accordingly, the rejection of claims 16, 17, 19, and 20 should be withdrawn.

Independent Claim 27

Amended claim 27 recites, in part, "forming, by a non-selective deposition process, a passivation layer of a first semiconductor material in the recesses…" The amendment to claim 27 finds support at least at paragraph [0065] of the present application. The rationale offered in the Office Action for the rejection of this claim is effectively the same rationale that is offered for the rejection of independent claim 1. Therefore, for reasons similar to those discussed above in association with independent claim 1, it is respectfully submitted that Park and Rotondaro do not teach or suggest the limitations of Applicants' amended claim 27. For avoidance of doubt, the Rotondaro reference is relied upon merely for a teaching of performing a fluorine treatment. Thus, even if the teachings of Rotondaro are exactly as the Office suggests, which Applicants do not admit, Park and Rotondaro do not teach or suggest "forming, by a non-selective deposition process, a passivation layer of a first semiconductor material in the recesses…", as positively recited in Applicants' amended claim 27.

Accordingly, independent claim 27 is allowable, and notice to that effect is respectfully requested.

Dependent Claims 28-32

Claims 28-32 depend on and further limit claim 27 and therefore are deemed to be patentable over the prior art, for at least the same reasons set forth above in connection with independent claim 27. Accordingly, the rejection of claims 28-32 should be withdrawn.

New Claims

Claims 33 and 34, which depend on and further limit claims 1 and 27, respectively, have been added and are deemed to be patentable over the cited art, for at least the same reasons set forth above in connection with independent claims 1 and 27.

Conclusion

An early formal notice of allowance of claims 1-20 and 27-34 is requested. A personal or telephonic interview is respectfully requested to discuss any remaining issues in an effort to expedite the allowance of this application.

Respectfully submitted,

/Michael E. Ramon/

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10/4/2017

/Janie Martinez-Holm/
Janie Martinez-Holm

Electronic Patent Application Fee Transmittal

Application Number:	14597115
Filing Date:	14-Jan-2015
Title of Invention:	Metal-Insensitive Epitaxy Formation
First Named Inventor/Applicant Name:	Chun Hsiung Tsai
Filer:	Michael Edward Ramon/Janie Martinez-Holm
Attorney Docket Number:	2014-0937/24061.2998

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension - 2 months with $0 paid	1252	1	600	600
Miscellaneous:				
RCE- 1st Request	1801	1	1200	1200
		Total in USD ($)		**1800**

Electronic Acknowledgement Receipt

EFS ID:	30563469
Application Number:	14597115
International Application Number:	
Confirmation Number:	8745
Title of Invention:	Metal-Insensitive Epitaxy Formation
First Named Inventor/Applicant Name:	Chun Hsiung Tsai
Customer Number:	42717
Filer:	Michael Edward Ramon/Janie Martinez-Holm
Filer Authorized By:	Michael Edward Ramon
Attorney Docket Number:	2014-0937/24061.2998
Receipt Date:	04-OCT-2017
Filing Date:	14-JAN-2015
Time Stamp:	14:50:37
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$1800
RAM confirmation Number	100517INTEFSW14520300
Deposit Account	
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Extension of Time	24061-2998_EOT_2MO.pdf	178510 3f8569530a44a80fb4d52304abe4e21016ff6576	no	2
Warnings:					
Information:					
2	Request for Continued Examination (RCE)	24061-2998_RCE_Transmittal_1st.pdf	697648 5e6aa310e978e9279b7d1db05c86972ca46dfe29	no	3
Warnings:					
Information:					
3		24061-2998_RCE_Amendment.pdf	196534 05a41b145a5b662c2c31b6489a7a5b397b6b89ef	yes	13

Multipart Description/PDF files in .zip description

Document Description	Start	End
Amendment Submitted/Entered with Filing of CPA/RCE	1	1
Claims	2	6
Applicant Arguments/Remarks Made in an Amendment	7	13

Warnings:					
Information:					
4	Fee Worksheet (SB06)	fee-info.pdf	31976 23037cbb84934e955880474abc080f24b0f26db2	no	2
Warnings:					
Information:					
			Total Files Size (in bytes):	1104668	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/22 (03-13)
Approved for use through 3/31/2013. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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PETITION FOR EXTENSION OF TIME UNDER 37 CFR 1.136(a)

Docket Number (Optional): 20140937 / 24061.2998

Application Number: 14/597,115

Filed: 01-14-2015

For: Metal-Insensitive Epitaxy Formation

Art Unit: 2896

Examiner: Spalla, David C.

This is a request under the provisions of 37 CFR 1.136(a) to extend the period for filing a reply in the above-identified application.

The requested extension and fee are as follows (check time period desired and enter the appropriate fee below):

	Fee	Small Entity Fee	Micro Entity Fee	
☐ One month (37 CFR 1.17(a)(1))	$200	$100	$50	$
☑ Two months (37 CFR 1.17(a)(2))	$600	$300	$150	$ 600.00
☐ Three months (37 CFR 1.17(a)(3))	$1,400	$700	$350	$
☐ Four months (37 CFR 1.17(a)(4))	$2,200	$1,100	$550	$
☐ Five months (37 CFR 1.17(a)(5))	$3,000	$1,500	$750	$

☐ Applicant asserts small entity status. See 37 CFR 1.27.

☐ Applicant certifies micro entity status. See 37 CFR 1.29.
Form PTO/SB/15A or B or equivalent must either be enclosed or have been submitted previously.

☐ A check in the amount of the fee is enclosed.

☑ Payment by credit card. ~~XXXXXXXXXXXXXX~~ Form PTO-2038 is attached.

☐ The Director has already been authorized to charge fees in this application to a Deposit Account.

☑ The Director is hereby authorized to charge any fees which may be required, or credit any overpayment, to Deposit Account Number 08-1394.

☑ Payment made via EFS-Web.

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

I am the

☐ applicant/inventor.

☐ assignee of record of the entire interest. See 37 CFR 3.71. 37 CFR 3.73(b) statement is enclosed (Form PTO/SB/96).

☑ attorney or agent of record. Registration number 52,147.

☐ attorney or agent acting under 37 CFR 1.34. Registration number _____.

/Michael E. Ramon/ — Signature

October 4, 2017 — Date

Michael E. Ramon — Typed or printed name

512-867-8426 — Telephone Number

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. Submit multiple forms if more than one signature is required, see below*.

☑ * Total of 1 forms are submitted.

This collection of information is required by 37 CFR 1.136(a). The information is required to obtain or retain a benefit by the public, which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 6 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 14/597,115	Filing Date 01/14/2015	☐ To be Mailed

ENTITY: ☑ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A		N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A		N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*		x $80 =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*		x $420 =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).				
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))					
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL	

APPLICATION AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
AMENDMENT	10/04/2017							
	Total (37 CFR 1.16(i))	* 28	Minus	** 26	= 2		x $80 =	160
	Independent (37 CFR 1.16(h))	* 3	Minus	*** 3	= 0		x $420 =	0
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	160

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
AMENDMENT								
	Total (37 CFR 1.16(i))	*	Minus	**	=		x $0 =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=		x $0 =	
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.	LIE
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".	theresa D dawkins
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".	
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.	

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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United States Patent and Trademark Office
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In place of PTO-1449 Form	U. S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE			*Complete if Known*	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(use as many sheets as necessary)*				Application Number	14/597,115
				Filing Date	January 14, 2015
				First Inventor Name	Chun Hsiung Tsai et al.
				Art Unit	2896
				Examiner Name	SPALLA, DAVID C
SHEET	1	OF	1	Attorney Docket Number	2014-0937/24061.2998

U. S. PATENTS				
Examiner's Initials	Cite No.	Document Number	Issue Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document
	A1	8598003	12-03-2013	Murthy et al.

U. S. PATENT APPLICATION PUBLICATIONS				
Examiner's Initials	Cite No.	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document

FOREIGN PATENT DOCUMENTS					
Examiner's Initials	Cite No.	Foreign Patent Document (Country Code – Number – Kind)	Publication Date MM-DD-YYYY	Patentee or Applicant of Cited Document	Translation Y/N
	B1	KR 10-2012-0086369	08-02-2012	INTEL CORP.	Y, Corresponding U.S. Pat. 8598003

NON-PATENT LITERATURE DOCUMENTS		
Examiner's Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article, title of the item, date, page(s), volume-issue number(s), publisher, city/country where published
	A1	
	A2	
	A3	
	A4	
	A5	

Examiner Signature		Date Considered	

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include a copy of this form with next communication to applicant.

(19) 대한민국특허청(KR)
(12) 공개특허공보(A)

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(뒷면에 계속)
(74) 대리인
제일특허법인

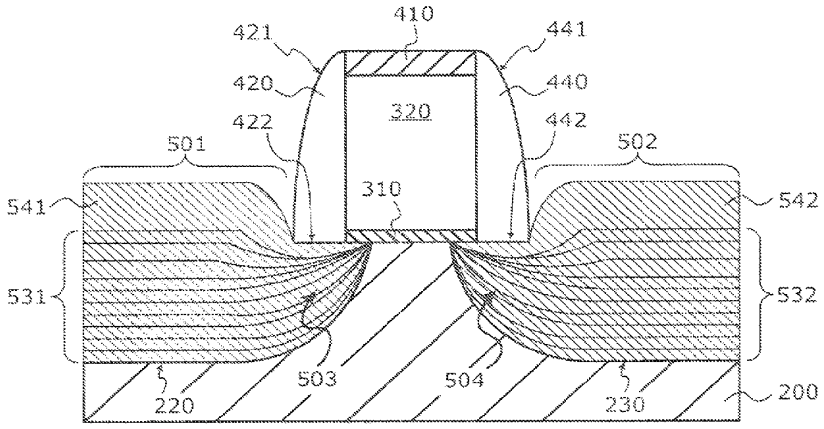
전체 청구항 수 : 총 42 항

(54) 발명의 명칭 **도핑된 에피택셜 영역을 가진 반도체 디바이스 및 그 제조 방법**

(57) 요 약

본 발명은 반도체 디바이스 상의 에피택셜 영역을 설명한다. 일 실시예에서 에피택셜 영역은 주기적 증착-에칭 공정을 통해 기판 상에 증착된다. 주기적 증착-에칭 공정 중에 스페이서 바로 밑에 생성되는 중공들이 에피택셜 캡 층에 의해 채워진다. 에피택셜 영역 및 에피택셜 캡 층은 채널 영역에서 전자 이동성을 개선하며, 단채널 효과를 낮추며 기생 저항을 줄인다.

대 표 도



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Page 143 of 351

(72) 발명자

가니 타히르

미국 오레곤주 97229 포틀랜드 노스웨스트 안달루시안 웨이 15523

페테 아브히짓 자이얀트

미국 오레곤주 97124 힐스보로 노스웨스트 모다 웨이 2848

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특허청구의 범위

청구항 1

반도체 디바이스를 형성하는 방법으로서,

게이트 전극을 갖는 기판 및 상기 게이트 전극의 측벽 상에 형성된 스페이서를 제공하는 단계와,

오목한(recessed) 계면을 형성하기 위해 상기 기판을 에칭하는 단계와,

상기 기판을 제 1 전구체(precursor) 및 제 2 전구체에 교대로 노출시킴으로써 상기 오목한 계면 위에 에피택셜 영역(epitaxial region)을 형성하는 단계와,

상기 에피택셜 영역 위에 캡 층을 선택적으로 증착하는 단계를 포함하는

방법.

청구항 2

제 1 항에 있어서,

상기 기판을 상기 제 1 전구체 및 상기 제 2 전구체에 교대로 노출시키는 단계는

상기 오목한 계면 위에 에피택셜 막을 증착하며, 상기 스페이서의 측벽 및 저면(bottom surface) 상에 비결정질 층을 증착하기 위해 상기 기판을 상기 제 1 전구체에 노출하는 단계와,

상기 스페이서의 상기 측벽 및 저면으로부터 상기 비결정질 층을 제거하기 위해 상기 기판을 상기 제 2 전구체에 노출시키는 단계를 포함하는

방법.

청구항 3

제 1 항에 있어서,

상기 제 1 전구체는

실란(silane)을 포함하는 실리콘 함유 화합물과,

유기실란을 포함하는 탄소 함유 화합물과,

인을 포함하는 도펀트를 포함하는

방법.

청구항 4

제 3 항에 있어서,

상기 에피택셜 영역은 인으로 도핑된 실리콘 및 탄소를 포함하는

방법.

청구항 5

제 1 항에 있어서,

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상기 제 2 전구체는 에천트(etchant) 가스인

방법.

청구항 6

제 1 항에 있어서,

상기 오목한 계면 위에 상기 에피택셜 영역을 형성하는 단계는 상기 에피택셜 영역과 상기 스페이서의 저면 사이에 보이드(void)를 발생시키며,

상기 캡 층은 상기 보이드를 다시 메우는

방법.

청구항 7

제 1 항에 있어서,

상기 캡 층은 상기 기판을 제 3 전구체에 노출시킴으로써 상기 에피택셜 영역 위에 선택적으로 증착되며,

상기 제 3 전구체는

실란을 포함하는 실리콘 함유 화합물과,

인을 포함하는 도펀트와,

에천트 가스를 포함하는

방법.

청구항 8

제 7 항에 있어서,

상기 캡 층은 인으로 도핑된 실리콘을 포함하는

방법.

청구항 9

제 1 항에 있어서,

상기 기판을 제 1 전구체 및 제 2 전구체에 교대로 노출시키는 단계 전에, 상기 기판 상에서 수소 베이킹 처리를 수행하는 단계를 더 포함하는

방법.

청구항 10

제 1 항에 있어서,

오목한 계면을 형성하기 위해 상기 기판을 에칭하는 단계는

상기 기판의 {111} 결정면 내에 {111} 면을 형성하기 위해 습식 에칭을 수행하는 단계를 포함하는

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방법.

청구항 11

제 10 항에 있어서,

상기 습식 에칭은 상기 기판의 {010} 결정면 내에 {010} 면을 형성하는

방법.

청구항 12

제 10 항에 있어서,

상기 습식 에칭은 수산화 칼륨(KOH), 수산화 나트륨(NaOH), 암모니아 기반 에천트 또는 아민 기반 에천트로 이루어진 그룹으로부터 선택된 에천트 화학제를 사용하는

방법.

청구항 13

반도체 디바이스를 형성하는 방법으로서,

게이트 전극을 갖는 기판, 및 상기 게이트 전극의 마주보는 측벽 상에 형성된 제 1 스페이서 및 제 2 스페이서를 제공하는 단계와,

오목한 소스 계면 및 오목한 드레인 계면을 형성하기 위해 상기 기판을 에칭하는 단계와,

상기 기판을 에천트 가스를 포함하는 전구체에 노출시킴으로써, 상기 오목한 소스 계면 위에 제 1 에피택셜 층 및 상기 오목한 드레인 계면 위에 제 2 에피택셜 층을 선택적으로 증착하는 단계를 포함하는

방법.

청구항 14

제 13 항에 있어서,

상기 전구체는

실란을 포함하는 실리콘 함유 화합물과,

인을 포함하는 도펀트를 포함하는

방법.

청구항 15

제 14 항에 있어서,

상기 제 1 에피택셜 층 및 제 2 에피택셜 층의 양쪽은 인으로 도핑된 실리콘을 포함하는

방법.

청구항 16

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제 13 항에 있어서,

오목한 소스 계면 및 오목한 드레인 계면을 형성하기 위해 상기 기판을 에칭하는 단계는

상기 오목한 소스 계면 및 상기 오목한 드레인 계면에서 상기 기판의 {111} 결정면 내에 {111} 면을 형성하기 위해 습식 에칭을 수행하는 단계를 포함하는

방법.

청구항 17

제 16 항에 있어서,

상기 습식 에칭은 상기 오목한 소스 계면 및 상기 오목한 드레인 계면에서 상기 기판의 {010} 결정면 내에 {010} 면을 형성하는

방법.

청구항 18

제 16 항에 있어서,

상기 습식 에칭은 수산화 칼륨(KOH), 수산화 나트륨(NaOH), 암모니아 기반 에천트 또는 아민 기반 에천트로 이루어진 그룹으로부터 선택된 에천트 화학제를 사용하는

방법.

청구항 19

반도체 디바이스를 형성하는 방법으로서,

상부에 절연층을 갖는 기판, 및 상기 절연층을 통해 상기 기판으로부터 연장된 반도체 바디(body)를 제공하는 단계와,

상기 반도체 바디의 일부 위에 게이트 전극을 형성하여 상기 반도체 바디의 노출 부분을 한정하는 단계와,

상기 게이트 전극의 측벽 상에 게이트 스페이서를 증착하는 단계와,

상기 절연층의 상면 아래에 오목한 제 1 표면, 및 상기 게이트 스페이서와 동일 평면인 제 2 표면을 형성하기 위해 상기 반도체 바디의 노출 부분을 에칭하는 단계와,

상기 기판을 제 1 전구체 및 제 2 전구체에 교대로 노출시킴으로써 상기 제 1 표면 및 제 2 표면 상에 에피택셜 영역을 형성하는 단계와,

상기 에피택셜 영역 위에 캡 층을 선택적으로 증착하는 단계를 포함하는

방법.

청구항 20

제 19 항에 있어서,

상기 게이트 전극의 측벽 상에 상기 게이트 스페이서를 증착하는 단계는

상기 반도체 바디의 노출 부분의 측벽 상에 바디 스페이서(body spacers)를 증착하는 단계를 포함하는

방법.

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청구항 21

제 20 항에 있어서,

상기 반도체 바디의 노출 부분을 에칭하는 단계 전에, 상기 반도체 바디의 노출 부분의 측벽으로부터 상기 바디 스페이서를 제거하는 단계를 더 포함하는

방법.

청구항 22

제 19 항에 있어서,

상기 제 2 표면이 상기 게이트 스페이서 내에서 오목하게 되도록 상기 제 2 표면을 에칭하는 단계를 더 포함하는

방법.

청구항 23

제 19 항에 있어서,

상기 제 1 표면 및 제 2 표면 상에 에피택셜 영역을 형성하는 단계는 상기 에피택셜 영역과 상기 절연층 사이에 보이드를 발생시키며,

상기 캡 층은 상기 보이드를 다시 메우는

방법.

청구항 24

제 19 항에 있어서,

상기 기판을 상기 제 1 전구체 및 상기 제 2 전구체에 교대로 노출시키는 단계는

상기 제 1 표면 및 제 2 표면 위에 에피택셜 막을 증착하며, 상기 절연층 및 상기 게이트 스페이서 상에 비결정질 층을 증착하기 위해 상기 기판을 상기 제 1 전구체에 노출시키는 단계와,

상기 절연층 및 상기 게이트 스페이서로부터 상기 비결정질 층을 제거하기 위해 상기 기판을 상기 제 2 전구체에 노출시키는 단계를 포함하는

방법.

청구항 25

제 19 항에 있어서,

상기 제 1 전구체는

실란을 포함하는 실리콘 함유 화합물과,

유기실란을 포함하는 탄소 함유 화합물과,

인을 포함하는 도펀트를 포함하는

방법.

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청구항 26

제 25 항에 있어서,

상기 에피택셜 영역은 인으로 도핑된 실리콘 및 탄소를 포함하는

방법.

청구항 27

제 19 항에 있어서,

상기 제 2 전구체는 에천트 가스인

방법.

청구항 28

제 19 항에 있어서,

상기 캡 층은 상기 기판을 제 3 전구체에 노출시킴으로써 상기 에피택셜 영역 위에 선택적으로 증착되며,

상기 제 3 전구체는

실란을 포함하는 실리콘 함유 화합물과,

인을 포함하는 도펀트와,

에천트 가스를 포함하는

방법.

청구항 29

제 28 항에 있어서,

상기 캡 층은 인으로 도핑된 실리콘을 포함하는

방법.

청구항 30

반도체 디바이스로서,

기판 - 상기 기판은 상기 기판의 채널 영역 위에 형성되는 게이트 전극과, 상기 게이트 전극의 마주보는 쪽에서 상기 기판 상에 형성된 오목한 소스 계면 및 오목한 드레인 계면을 포함함 - 과,

상기 게이트 전극의 마주보는 측벽 상에 형성되는 제 1 스페이서 및 제 2 스페이서 - 상기 오목한 소스 계면의 일부는 상기 제 1 스페이서의 저면 아래에서 횡방향으로 연장되며, 상기 오목한 드레인 계면의 일부는 상기 제 2 스페이서의 저면 아래에서 횡방향으로 연장됨 - 와,

상기 오목한 소스 계면 위에 형성되는 제 1 에피택셜 영역과, 상기 제 1 에피택셜 영역 위에 형성되는 제 1 캡 층을 포함하는 소스 영역 - 상기 제 1 캡 층의 일부는 상기 제 1 에피택셜 영역과 상기 제 1 스페이서의 저면 사이에 형성됨 - 과,

상기 오목한 드레인 계면 위에 형성되는 제 2 에피택셜 영역과, 상기 제 2 에피택셜 영역 위에 형성되는 제 2 캡 층을 포함하는 드레인 영역 - 상기 제 2 캡 층의 일부는 상기 제 2 에피택셜 영역과 상기 제 2 스페이서의 저면 사이에 형성됨 - 을 포함하는

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반도체 디바이스.

청구항 31

제 30 항에 있어서,

상기 제 1 에피택셜 영역 및 제 2 에피택셜 영역은 각각 인으로 도핑된 실리콘 및 탄소를 포함하는

반도체 디바이스.

청구항 32

제 31 항에 있어서,

상기 제 1 에피택셜 영역 및 제 2 에피택셜 영역은 각각

0.5 원자% 내지 4 원자% 범위 안의 탄소 농도와,

$9E19cm^{-3}$ 내지 $3E21cm^{-3}$ 범위 안의 인 농도를 갖는 실리콘을 포함하는

반도체 디바이스.

청구항 33

제 31 항에 있어서,

상기 제 1 캡 층 및 제 2 캡 층은 각각 인으로 도핑된 실리콘을 포함하는

반도체 디바이스.

청구항 34

제 33 항에 있어서,

상기 제 1 캡 층 및 제 2 캡 층은 각각 $8E19cm^{-3}$ 내지 $3E21cm^{-3}$ 범위 내의 인 농도를 갖는 실리콘을 포함하는

반도체 디바이스.

청구항 35

반도체 디바이스로서,

상부에 절연층이 형성된 기판과,

상기 절연층을 통해 상기 기판으로부터 연장되는 반도체 바디 - 상기 반도체 바디는 상기 절연층 위에 노출되는 상면, 전면 및 후면과, 상기 상면으로부터 소스 계면까지 연장된 제 1 측벽과, 상기 제 1 측벽 반대 편에 있으며 상기 상면으로부터 드레인 계면까지 연장되는 제 2 측벽을 포함함 - 와,

상기 반도체 바디의 상기 상면, 상기 전면 및 상기 후면 위에 형성되는 게이트 전극과,

상기 게이트 전극의 마주보는 측벽 상에 형성되는 제 1 스페이서 및 제 2 스페이서와,

상기 제 1 측벽 및 상기 소스 계면 상에 형성되는 제 1 에피택셜 영역 및 상기 제 1 에피택셜 영역 위에 형성되는 제 1 캡 층을 포함하는 소스 영역 - 상기 제 1 캡 층의 일부는 상기 제 1 에피택셜 영역과 상기 절연층 사이에 형성됨 - 과,

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상기 제 2 측벽 및 상기 드레인 계면 위에 형성되는 제 2 에피택셜 영역 및 상기 제 2 에피택셜 영역 위에 형성되는 제 2 캡 층을 포함하는 드레인 영역 - 상기 제 2 캡 층의 일부는 상기 제 2 에피택셜 영역과 상기 절연층 사이에 형성됨 - 을 포함하는

반도체 디바이스.

청구항 36

제 35 항에 있어서,

상기 제 1 측벽은 상기 제 1 스페이서와 실질적으로 동일 평면이며, 상기 제 2 측벽은 상기 제 2 스페이서와 동일 평면인

반도체 디바이스.

청구항 37

제 35 항에 있어서,

상기 제 1 측벽은 상기 제 1 스페이서 안에서 오목하며, 상기 제 2 측벽은 상기 제 2 스페이서 안에서 오목한

반도체 디바이스.

청구항 38

제 35 항에 있어서,

상기 소스 계면 및 상기 드레인 계면는 상기 절연층의 상기 상면 아래에서 오목한

반도체 디바이스.

청구항 39

제 35 항에 있어서,

상기 제 1 에피택셜 영역 및 제 2 에피택셜 영역은 각각 인으로 도핑된 실리콘 및 탄소를 포함하는

반도체 디바이스.

청구항 40

제 39 항에 있어서,

상기 제 1 에피택셜 영역 및 제 2 에피택셜 영역은 각각

0.5 원자% 내지 4 원자% 범위 안의 탄소 농도, 및

$9E19cm^{-3}$ 내지 $3E21cm^{-3}$ 범위 안의 인 농도를 갖는 실리콘을 포함하는

반도체 디바이스.

청구항 41

제 35 항에 있어서,

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상기 제 1 캡 층 및 제 2 캡 층은 각각 인으로 도핑된 실리콘을 포함하는

반도체 디바이스.

청구항 42

제 41 항에 있어서,

상기 제 1 캡 층 및 제 2 캡 층은 각각 $8E19cm^{-3}$ 내지 $3E21cm^{-3}$ 범위 내의 인 농도를 갖는 실리콘을 포함하는

반도체 디바이스.

명 세 서

기 술 분 야

[0001] 본 발명은 반도체 공정 분야에 관한 것으로서, 특히 도핑된 에피택셜 영역들을 가진 반도체 디바이스 및 그 제조 방법에 관한 것이다.

배 경 기 술

[0002] 반도체 디바이스, 특히 트랜지스터들의 성능을 높이는 것이 반도체 산업분야에서는 항상 주요한 고려사항이 되어 왔다. 예를 들어, 산화 금속 반도체 전계 효과 트랜지스터(MOSFET(metal oxide semiconductor field effect transistor))의 설계 및 제조 중에 소자 성능을 개선하기 위해 채널 영역의 전자 이동성을 높이며 기생 저항을 줄이는 것이 항상 공통적인 목표였다.

[0003] 소자 성능을 개선하는 다른 방법들은 예컨대 소스/드레인 영역들 및 채널 영역 사이의 영역을 도핑함으로써 MOSFET의 전체적 저항을 줄이는 것을 포함하며, 이 사이의 영역은 MOSFET의 '팁(tip)' 또는 소스/드레인 확장 영역이라 칭한다. 예를 들어, 도펀트(dopant)가 소스/드레인 영역 내에 주입되며 어닐링(annealing) 단계가 그 도펀트를 채널 영역을 향해 확산시킨다. 그러나, 도펀트 농도와 위치를 제어함에 있어 한계가 존재한다. 게다가, 주입 및 확산 방법은 팁 영여들에서의 측면 언더컷(lateral undercut)이나 기생 저항 문제를 처리하지 못한다.

도면의 간단한 설명

[0004] 도 1은 본 발명의 일 실시예에 따른 반도체 디바이스를 예시한 단면도이다.

도 2는 본 발명의 다른 실시예에 따른 반도체 디바이스를 예시한 단면도이다.

도 3은 본 발명의 다른 실시예에 따른 반도체 디바이스를 예시한 단면도이다.

도 4는 본 발명의 다른 실시예에 따른 반도체 디바이스를 예시한 사시도이다.

도 5a-5f는 도 1에 도시된 반도체 디바이스 제조 방법을 예시한 단면도들이다.

도 6a-5e는 도 2에 도시된 반도체 디바이스 제조 방법을 예시한 단면도들이다.

도 7a-7c는 도 3에 도시된 반도체 디바이스 제조 방법을 예시한 단면도들이다.

도 8a-8i는 도 4에 도시된 반도체 디바이스 제조 방법을 예시한 사시도들이다.

도 9-15는 도 8e-8i에 도시된 반도체 디바이스의 단면도들이다.

도 8ee는 도 8e에 도시된 반도체 디바이스의 대안적 실시예를 예시한 사시도이다.

도 9a는 도 9에 도시된 반도체 디바이스의 대안적 실시예를 예시한 사시도이다.

발명을 실시하기 위한 구체적인 내용

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[0005] 도핑된 에피택셜 영역을 가지는 반도체 디바이스 및 그 제조 방법이 설명된다. 이하의 설명에서, 본 발명에 대한 철저한 이해를 제공하기 위해 수많은 특정 세부사항들이 언급된다. 다른 경우, 본 발명을 불필요하게 모호하게 하지 않도록 잘 알려진 반도체 공정 기법들 및 특징들은 설명되지 않았다.

[0006] 본 발명의 실시예들은 반도체 디바이스 상의 에피택셜 영역 형성 방법을 설명한다. 일 실시예에서 에피택셜 영역은 주기적 증착-에칭 공정을 통해 증착된 인시투(in-situ) 탄소 및 인 도핑된 실리콘($Si_y(C,P)_{1-y}$) 영역이다. 주기적 증착-에칭 공정 중에 스페이서 바로 밑에 생성되는 중공들이 매우 높게 인 도핑된 실리콘(Si_yP_{1-y}) 에피택셜 캡 층에 의해 채워진다. 자가 정렬 에피 팁((Self-aligned Epi Tip:SET) 구조 내 에피택셜 영역 및 캡 층의 스택이 채널 영역에서 증가된 전자 이동성 이득, 감소된 단채널 효과(탄소 억제 인 확산에 기인함), 및 (Si_yP_{1-y}) 에피택셜 캡 층 내 매우 높은 인 도핑에 의해 제공되는 감소된 기생 저항의 결합된 효과들로 인해 놀라운 드랜지스터 성능 이득을 제공한다.

[0007] 도 1은 본 발명의 일 실시예에 따른 반도체 디바이스의 단면도를 예시한다. 반도체 디바이스는 비한정적인 것으로서 단결정 실리콘과 같은 반도체 물질로 이뤄지는 기판(200)을 포함한다. 일 실시예에서, 기판(200)은 절연체 상의 실리콘(SOI, silicon on insulator) 기판의 실리콘막이거나, 실리콘, 실리콘 게르마늄, 게르마늄, III-V 화합물 반도체들을 포함하는 다층 구조의 기판이다.

[0008] 게이트 유전체(310)가 기판(200)의 채널 영역 위에 형성된다. 일 실시예에서 유전체 층(310)은 비한정적인 것으로서 산화 실리콘(e.g., SiO_2)과 같은 어떤 잘 알려진 절연 물질로 이루어진다. 다른 실시예에서, 유전체 층(310)은 이산화 실리콘보다 실질적으로 높은 유전 상수(즉, k>3.9)를 가진 높은 k의 유전 물질로 이루어진다. 높은 k의 유전 물질들의 예들로는 산화 탄탈륨(Ta_2O_5), 산화 티타늄(TiO_2) 및 산화 하프늄(HfO_2)이 포함되나 이에 국한되지 않는다.

[0009] 게이트 전극(320)이 게이트 유전체(310) 위에 형성된다. 일 실시예에서 게이트 전극(320)은 비한정적인 것으로서 폴리실리콘(polysilicon)과 같은 어떤 잘 알려진 절연 물질로 이루어진다. 다른 실시예들에서 게이트 전극(320)은 비한정적인 것으로서 백금, 텅스텐 또는 티타늄과 같은 금속이나 금속 합금 물질로 이루어진다.

[0010] 일 실시예에서, 하드 마스크(410)가 게이트 전극(320) 상부에 형성된다. 일 실시예에서 하드 마스크(410)는 비한정적인 것으로서 질화 실리콘이나 산질화 실리콘과 같은 물질로 이루어진다. 스페이서들(420, 440)이 게이트 전극(320)의 양 측벽들 상에 형성된다. 일 실시예에서, 스페이서들(420, 440)은 게이트 전극(320)의 전체 측벽 너비를 따라 형성된다. 스페이서들(420, 440)은 측벽들(421, 441) 및 저면들(422, 442)을 포함한다. 일 실시예에서 스페이서들(420, 440)은 비한정적인 것으로서 질화 실리콘, 이산화 실리콘, 또는 산질화 실리콘과 같은 물질로 이루어진다.

[0011] 본 발명의 일 실시예에서, 오목한(recessed) 소스 계면(220) 및 오목한 드레인 계면(230)이 게이트 전극(320)의 양측에서 기판(200) 상에 형성된다. 일 실시예에서 오목한 소스 계면(220)의 일부는 스페이서(420)의 저면(422) 밑과 게이트 전극(320)의 일부 밑에서 옆으로 연장된다. 마찬가지로, 오목한 드레인 계면(230)의 일부는 스페이서(440)의 저면(442) 밑과 게이트 전극(320)의 일부 밑에서 옆으로 연장된다.

[0012] 소스 영역(501)이 소스 계면(220) 위에 형성된다. 본 발명의 일 실시예에서, 소스 영역(501)은 오목한 소스 계면(220) 위에 형성된 에피택셜 영역(531)을 포함한다. 캡 층(541)이 에피택셜 영역(531) 위에 형성된다. 소스 영역(501)은 스페이서(420) 및 게이트 유전체(310) 바로 밑에 형성된 에피택셜 영역(531) 및 캡 층(541)의 일부를 포함하는 소스 에피 팁(epi-tip) 영역(503)을 포함한다.

[0013] 드레인 영역(502)이 드레인 계면(230) 위에 형성된다. 일 실시예에서, 드레인 영역(502)은 오목한 드레인 계면(230) 위에 형성된 에피택셜 영역(532)을 포함한다. 캡 층(542)이 에피택셜 영역(532) 위에 형성된다. 드레인 영역(502)은 스페이서(440) 및 게이트 유전체(310) 바로 밑에 형성된 에피택셜 영역(532) 및 캡 층(542)의 일부를 포함하는 드레인 에피 팁(epi-tip) 영역(504)을 포함한다. 소스 및 드레인 에피 팁 영역들(503, 504)을 채널 영역에 상대적으로 근접하여 형성함으로써, 채널 영역에 보다 큰 등방 응력(hydrostatic stress)이 유도되고, 그 결과 보다 높은 전자 이동성 및 증가된 구동 전류를 파생한다.

[0014] 본 발명의 일 실시예에서 에피택셜 영역들(531, 532)은 인으로 도핑된 실리콘 및 탄소를 포함한다. 이 경우, 도 1에 도시된 반도체 디바이스는 자가 정렬 에피 팁(SET) 구조를 가진 NMOS 플라나(planar) 또는 트리게이트(trigate) 트랜지스터이다. 일 실시예에서, 에피택셜 영역들(531, 532)은 약 0.5 원자% 내지 4 원자% 의 탄소

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농도 및 약 9E19cm^{-3}내지 3E21cm^{-3}의 인 농도를 가지는 실리콘을 포함한다. 특정 실시예에서, 에피택셜 영역들(531, 532)은 2.2 원자% 의 탄소 농도 및 2E20 cm^{-3}의 인 농도를 가지는 실리콘을 포함한다. 소스 및 드레인 영역들(501, 502)의 에피택셜 영역들(531, 532) 내 치환 탄소(2 원자% 를 넘음)가 등방 응력을 채널 영역 상에 전달하고, 이러한 것이 전자 이동성을 향상시킨다. 게다가 치환 탄소는 어느 이어지는 열처리(thermal anneals) 중에 어떤 인 확산을 억제함으로써 단채널 효과를 감소시킨다.

[0015] 본 발명의 일 실시예에서 캡 층들(541, 542)은 인으로 도핑된 실리콘을 포함하는 에피택셜 층들이다. 일 실시예에서 캡 층들(541, 542)은 약 8E19cm^{-3} 내지 3E21cm^{-3}의 인 농도를 가지는 실리콘을 포함한다. 특정 실시예에서,캡 층들(541, 542)은 2E21cm^{-3}의 인 농도를 가지는 실리콘을 포함한다. 캡 층들(541, 542) 내에서의 높은 인 농도 레벨이 기생 저항, 특히 실리콘 화합물 및 소스/드레인 영역들(501, 502) 사이의 접촉 저항을 낮춘다.

[0016] 도 2는 도 1과 유사한 반도체 디바이스의 단면도를 예시한다. 기판(200)은 {001} 실리콘으로 이루어지고, {001} 실리콘 기판(200)의 {111} 결정면 안에 {1 11} 면(241)을 가지는 오목한(recessed) 소스 계면(240) 및 {001} 실리콘 기판(200)의 {111} 결정면 안에 {111} 면(251)을 가지는 오목한 드레인 계면(250)을 포함한다. {111} 면들(241, 251)은 감소되는 볼륨과 그에 상응하여 개선되는 단채널 효과의 제어를 제공한다. 일 실시예에서, 오목한 소스 및 드레인 계면들(240, 250) 각각은 {001} 실리콘 기판(200)의 {010} 결정면 내에 {010} 면(242, 252)을 더 포함하며, 그 {010} 면들(242, 252)은 게이트 전극(320) 바로 아래로 연장된다. {010} 면들(242, 252)은 반도체 디바이스의 금속학적 채널 길이를 보다 확실하게 한정하고 단채널 효과를 감소시키는 데 기여한다.

[0017] 도 1과 유사하게, 도 2에 도시된 반도체 디바이스는 소스 영역(501) 및 드레인 영역(502)를 포함하며, 그 각각의 영역은 에피택셜 영역(531, 532) 및 캡 층(541, 542)을 가진다. 에피택셜 영역들(531, 532) 및 캡 층들(541, 542)은 각자의 {111} 면들(241, 251) 및 {010} 면들(242, 252)을 포함하는 오목한 소스 및 드레인 계면들(240, 250) 위에 형성된다. 소스 영역(501)은 스페이서(420), 게이트 유전체(310), 및 {111}, {010} 면들(241, 242)에 의해 둘러싸인 에피택셜 영역(531) 및 캡 층(541)의 일부를 포함하는 소스 에피 팁(epi-tip) 영역(505)을 포함한다. 드레인 영역(502)은 스페이서(440), 게이트 유전체(310), 및 {111}, {010} 면들(251, 252)에 의해 둘러싸인 에피택셜 영역(532) 및 캡 층(542)의 일부를 포함하는 드레인 에피 팁(epi-tip) 영역(506)을 포함한다. 소스 및 드레인 에피 팁 영역들(505, 506)을 채널 영역에 상대적으로 근접하여 형성하는 것은 채널 영역에 보다 큰 등방 응력(hydrostatic stress)을 유도하고, 그에 따라 전자 이동성이 증가되며 그것이 보다 높은 구동 전류를 파생한다.

[0018] 도 3은 도 2과 유사한 반도체 디바이스의 단면도를 예시한다. 일 실시예에서, 소스 및 드레인 영역들(501, 502) 각각은 각자의 {111} 면들(241, 251) 및 {010} 면들(242, 252)을 포함하는 오목한 소스 및 드레인 계면들(240, 250) 위에 형성된 에피택셜 층(610, 620)을 포함한다.

[0019] 소스 영역(501)은 스페이서(420), 게이트 유전체(310), 및 {111}, {010} 면들(241, 242)에 의해 둘러싸인 에피택셜 층(610)의 일부를 포함하는 소스 에피 팁(epi-tip) 영역(611)을 포함한다. 드레인 영역은 스페이서(440), 게이트 유전체(310), 및 {111}, {010} 면들(251, 252)에 의해 둘러싸인 에피택셜 층(620)의 일부를 포함하는 드레인 에피 팁(epi-tip) 영역(621)을 포함한다. 소스 및 드레인 에피 팁 영역들(611, 621)을 채널 영역에 상대적으로 근접하여 형성하는 것은 채널 영역에 보다 큰 등방 응력(hydrostatic stress)을 유도하고, 그에 따라 전자 이동성이 증가되며 그것이 보다 높은 구동 전류를 파생한다.

[0020] 본 발명의 일 실시예에서 에피택셜 층(610, 620)은 인으로 도핑된 실리콘을 포함한다. 일 실시예에서 에피택셜 층들(610, 620)은 약 8E19cm^{-3} 내지 3E21cm^{-3}의 인 농도를 가지는 실리콘을 포함한다. 특정 실시예에서, 에피택셜 층들(610, 620)은 2E21cm^{-3}의 인 농도를 가지는 실리콘을 포함한다. 에피택셜 층들(610, 620) 내에서의 높은 인 농도 레벨이 기생 저항, 특히 실리콘 화합물 및 소스/드레인 영역들(501, 502) 사이의 접촉 저항을 낮춘다.

[0021] 도 1, 2 및 3은 채널 영역에서 전자 이동성을 개선하거나 소스/드레인 영역들에서 접촉 저항을 줄이기 위한 플라나(planar) 트랜지스터들 내 에피택셜 영역들의 응용법을 예시한다. 에피택셜 영역들이 플라나 트랜지스터들에 국한되는 것이 아니라 비한정적인 것으로서 트리게이트(trigate) 트랜지스터와 같은 다른 소자들 상에서 제조될 수 있다는 것을 예상할 수 있을 것이다. 도 4는 반도체 바디(body)나 핀(fin)(260)(점선으로 나타냄)을 가진 기판(200)을 포함하는 트리게이트 소자의 사시도를 예시한다. 3 개의 게이트들을 형성하기 위해 핀(260)

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의 3 개 표면들 위에 게이트 전극(340)이 형성된다. 하드 마스크(410)가 게이트 전극(340) 상부에 형성된다. 게이트 스페이서들(460, 470)이 게이트 전극(340)의 양 측벽들에서 형성된다. 소스 영역은 오목한 소스 계면(266) 및 핀(260) 측벽 상에 형성되는 에피택셜 영역(531)을 포함한다. 캡 층(541)이 에피택셜 영역(531) 위에 증착된다.

[0022] 도 5a-5f는 도 1과 관련하여 논의된 바와 같은 반도체 디바이스를 형성하는 방법을 예시한다. 반도체 디바이스의 제조는 도 5a에 도시된 것과 같이 기판(200)을 제공하는 것에서 시작된다. 게이트 유전체(310)가 기판(200)의 원하는 채널 영역 위에 형성된다. 일 실시예에서, 게이트 유전체(310)는 비한정적인 것으로서 물리적 증기 증착법(PVD(physical vapor deposition)), 화학적 증기 증착법(CVD(chemical vapor deposition)), 또는 원자 층 증착법(ALD(atomic layer deposition))과 같은 어떤 잘 알려진 방법들에 의해 형성된다.

[0023] 게이트 전극(320)이 게이트 유전체(310) 위에 형성된다. 본 발명의 일 실시예에서, 게이트 전극(320)은 나중에 교체 게이트 공정 시 실제 게이트 전극으로 교체되는 희생 게이트 전극이다. 하드 마스크(410)가 게이트 전극(320) 상부에 형성된다. 본 발명의 일 실시예에서, 게이트 전극(320) 및 하드 마스크(410)는 PVD나 CVD를 사용하여 증착되고, 그런 다음 잘 알려진 광석판술 및 에칭 기법들을 이용해 패턴화된다.

[0024] 스페이서들(420, 440)이 이제 게이트 전극(320)의 양 측벽들 상에 형성된다. 스페이서들(420, 440)은 측벽들(421, 441) 및, 기판(200)의 상면 위에 형성되는 저면들(422, 442)을 포함한다. 일 실시예에서 스페이서들(420, 440)은 게이트 전극(320)을 포함하는 전체 기판(200) 위에 스페이서 물질 층을 증착하고 그런 다음 게이트 전극(320)의 측벽들 상에 스페이서들(420, 440)을 형성하기 위해 스페이서 물질 층을 비등방성으로 에칭하는 것과 같은 잘 알려진 기법을 이용함으로써 형성된다.

[0025] 다음으로, 소스 영역 및 드레인 영역이 기판(200) 상에 형성된다. 본 발명의 일 실시예에서, 소스 및 드레인 영역들의 제조는 비한정적인 것으로서 건조 에칭 또는 습식 에칭과 같은 잘 알려진 에칭 기법들을 이용하여 기판(200)의 일부를 오목하게 함으로써 시작된다. 본 발명의 일 실시예에서, 기판(200)에 대해 실질적으로 선택성이 있는 에천트 화학제를 포함하는 습식 에칭이 기판(200)을 오목하게 하는데 사용되어, 도 5b에 도시된 것과 같은 오목한 소스 계면(220) 및 오목한 드레인 계면(230)을 형성하도록 한다.

[0026] 일 실시예에서 습식 에칭은 스페이서들(420, 440) 밑을 잘라내어 스페이서(420)의 저면(422)과 오목한 소스 계면(220) 사이에 소스 에피 팁 중공(271)을 형성하고, 스페이서(440)의 저면과 오목한 드레인 계면(230) 사이에 드레인 에피 팁 중공(272)을 형성한다. 그 결과, 소스 에피 팁 중공(271) 및 드레인 에피 팁 중공(272)이 스페이서들(420, 440)의 저면들(422, 442)을 노출시킨다. 일 실시예에서, 소스 에피 팁 중공(271) 및 드레인 에피 팁 중공(272)은 게이트 유전체(310)의 일부를 또한 노출시킨다. 그 결과, 오목한 소스 계면(220)의 일부는 스페이서(420) 바로 밑과 게이트 전극(320)의 일부 바로 밑에서 옆으로 연장된다. 마찬가지로, 오목한 드레인 계면(230)의 일부는 스페이서(440)의 바로 밑과 게이트 전극(320)의 일부 바로 밑에서 옆으로 연장된다.

[0027] 습식 에칭은 소스 및 드레인 에피 팁 중공들(271, 272)이 게이트 유전체(310)를 노출하지 않도록 조절될 수 있다(가령, 에칭 지속 기간을 조정함으로써 조절됨)는 것을 예상할 수 있다. 예를 들어, 오목한 소스 계면(220)은 단지 스페이서(420) 바로 밑에서 옆으로 연장되며, 오목한 드레인 계면(230)은 단지 스페이서(440) 바로 밑에서 옆으로 연장된다.

[0028] 본 발명의 일 실시예에서, 오목한 소스 및 드레인 계면들(220, 230)이 반도체 디바이스의 채널 영역을 규정한다. 채널 영역은 게이트 유전체(310) 바로 밑과 오목한 소스 및 드레인 계면들(220, 230) 사이에 자리하는 기판(200)의 일부를 의미한다.

[0029] 다음으로, 기판(200)을 제 1 전구체(precursor) 및 제 2 전구체로 교대로 노출시킴으로써 오목한 소스 및 드레인 계면들(220, 230) 각각 위에 에피택셜 영역이 증착된다. 에피택셜 영역의 제조는 도 5c에서, 오목한 소스 및 드레인 계면들(220, 230) 상에 에피택셜 막들(511, 512)을 증착하기 위해 전체 기판(200)을 제 1 전구체에 노출시킴으로써 시작된다. 기판(200)이 단결정 실리콘으로 이루어지는 경우, 오목한 소스 및 드레인 계면들(220, 230)은 그 위에서 에피택셜 막들(511, 512)의 에피택셜 성장을 가능하게 하는 단결정 표면들이다. 한편, 하드 마스크(410), 스페이서들(420, 440), 및 게이트 유전체(310)는 비결정 표면들이다. 그 결과, 하드 마스크(410)의 상면 위와, 스페이서들(420, 440)의 측벽들(421, 441) 및 저면들(422, 442) 위과 게이트 유전체(310)의 저면의 일부 위에 비결정질 층(513)이 증착된다.

[0030] 본 발명의 일 실시예에서, 제 1 전구체는 실리콘 함유 화합물, 탄소 함유 화합물, 및 도펀트를 포함한다. 일 실시예에서, 실리콘 함유 화합물은 비한정적인 것으로서 실란(silanes) 및 할로겐화 실란을 포함한다. 그러한

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실리콘 함유 화합물은 실란(SiH_4), 디실란(Si_2H_6), 트리실란(Si_3H_8), 디클로로실란(SiH_2Cl_2), 및 펜타 클로로 실란을 포함한다.

[0031] 일 실시예에서, 탄소 함유 화합물은 비한정적인 것으로서 유기실란(organosilanes)을 포함한다. 예를 들어, 탄소 함유 화합물은 모노메칠실란(CH_3-SiH_3)을 포함한다. 일 실시예에서 탄소 함유 화합물은 수소(H_2)나 아르곤과 혼합된다. 예를 들어 모노메칠실란(CH_3-SiH_3)은 수소(H_2)나 아르곤과 혼합되고, 이때 CH_3-SiH_3 농도는 0.5% 내지 20%의 범위 내에 있다.

[0032] 본 발명의 일 실시예에서, 도펀트는 비한정적인 것으로서 인이나 비소와 같은 n-타입 도펀트이다. 일 실시예에서, 인 도펀트는 N_2나 Ar과 같은 불활성 기체나수소로의 어떠한 희석도 없이 인화수소(PH_3)를 사용하여 에피택셜 막에 포함된다. 다른 실시예에서, 예컨대 수소(H_2) 내 3%의 인화수소 혼합물과 같이 인화수소 가스가 수소와 혼합된다.

[0033] 일 실시예에서 제 1 전구체가 캐리어 가스를 이용해 기판(200) 상으로 전달되거나 방출된다. 일 실시예에서 캐리어 가스는 비한정적인 것으로서 수소(H_2), 또는 질소(N_2), 아르곤 및 헬륨, 그리고 이들의 어떤 조합과 같은 어떤 비활성 가스를 포함한다.

[0034] 본 발명의 일 실시예에서, 기판(200)은 섭씨 약 500도 내지 700도의 온도, 약 5 내지 300 토르(torr)의 기압, 및 약 3 내지 60초의 지속시간으로 제 1 전구체에 노출된다. 특정 일 실시예에서, 기판(200)은 섭씨 600도의 온도에서 30 토르(torr)의 기압으로 15초의 지속시간 동안 제 1 전구체에 노출된다.

[0035] 일 실시예에서 에피택셜 막들(511, 512)은 약 6 내지 100 옹스트롬(Angstroms)의 두께를 가지도록 성장된다. 일 실시예에서 에피택셜 막들(511, 512)은 50 옹스트롬의 두께를 가지도록 성장된다. 제 1 전구체가 인 도펀트를 사용하는 경우, 증착된 에피택셜 막들(511, 512)은 인으로 도핑된 실리콘 및 탄소를 포함하는 결정 막들(즉, 인시투(in-situ) 탄소 및 인 도핑된 실리콘 층)이다. 비결정질 층(513)은 인으로 도핑된 실리콘 및 탄소를 포함한다.

[0036] 에피택셜 성장을 촉진시키고 표면 결함을 줄이기 위해 기판을 제 1 전구체에 노출시키기 전에 옵션 표면 전처리가 기판(200) 상에서 수행될 수 있다. 본 발명의 일 실시예에서, 표면 전처리는 오목한 소스 및 드레인 계면들(220, 230)을 세정하기 위해 기판(200)(도 5b) 위에서 수행되는 수소 베이킹 처리(hydrogen bake treatment)를 포함한다. 수소 베이킹 처리는 산소를 제거하고, 에피택셜 막들(511, 512)이 결함을 만들지 않으면서 쉽게 응집할 수 있도록 표면 복구를 행한다. 일 실시예에서 수소 베이킹 처리는 섭씨 약 700 내지 1050도에서 약 10 내지 120초의 지속 시간 동안 수행된다. 본 발명의 일 실시예에서 염화수소(HCl)가 수소 베이킹 처리에 더해진다. 염화수소(HCl)는 오목한 소스 및 드레인 계면들(220, 230)이 산소, 탄화수소 및 어떤 다른 오염물질에서 자유롭도록 오목한 소스 및 드레인 계면들(220, 230)의 약 1 개 내지 3 개의 단층들의 제거를 행한다. 일 실시예에서 염화수소(HCl)를 이용한 수소 베이킹 처리는 섭씨 약 700 내지 900도의 보다 낮은 온도에서 약 10 내지 120초의 지속 시간 동안 수행된다. 다른 대안으로서, 염소(Cl_2), 저메인(GcH_4) 또는 인화수소(PH_3)가 염화 수소(HCl)에 대한 추가 혹은 대안적인 화학적 화합물로서 사용될 수 있다.

[0037] 대안적 실시예에서, 표면 전처리는 오목한 소스 및 드레인 계면들(220, 230)을 세정하기 위해 에칭 단계를 이용한다. 일 실시예에서 에칭 단계는 비한정적인 것으로서 수소(H_2), 무수 염산(HCL), 또는 저메인(GeH_4) 및 수소(H_2)의 혼합물과 같은 에천트 가스를 사용한다. 다른 실시예에서, 표면 전처리는 에칭 단계 및 수소 베이킹 처리의 조합을 이용한다.

[0038] 기판(200)을 제 2 전구체에 노출하기 전에, 기판(200)으로부터 제 1 전구체 및 다른 부산물들을 제거하기 위해 정화(purging) 공정이 수행될 수 있다. 일 실시예에서, 정화 공정은 어떤 비반응 제 1 전구체나 부산물들을 제거하기 위해 비한정적인 것으로서 질소(N_2), 헬륨 또는 아르곤과 같은 비활성 가스를 주입한다.

[0039] 다음으로, 도 5d에서, 스페이서들(420, 440)의 측벽들(421, 441) 및 저면들(422, 442)로부터 비결정질 층(513)을 제거하기 위해 전체 기판(200)이 제 2 전구체로 노출된다. 게다가 제 2 전구체는 하드 마스크(410) 상과 게이트 유전체(310) 밑에서 형성되는 어떤 비결정질 층(513) 역시 제거한다. 일 실시예에서, 제 2 전구체(900)는 에피택셜 막들(511, 512)보다 빠르게 비결정질 층(513)을 에칭하는 에천트 화학제를 이용한다. 일 실시예에서 제 2 전구체(900)는 비한정적인 것으로서 수소(H_2), 무수 염산(HCL), 및 저메인(GeH_4) 및 수소(H_2)의 혼합

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불과 같은 에천트 가스이다. 저메인(GeH_4)은 촉매작용을 통해 에칭을 행함으로써, 낮은 온도들에서 높은 에칭 속도(etch rate)를 제공할 수 있다.

[0040] 일 실시예에서, 기판(200)은 약 30 내지 300 토르(torr)의 기압에서 약 5 내지 60초의 지속시간 동안 제 2 전구체에 노출된다. 특정 일 실시예에서, 기판(200)은 80 도르(torr)의 기압에서 20초의 지속시간 동안 제 2 전구체에 노출된다. 일 실시예에서, 기판(200)을 제 1 전구체 및 제 2 전구체 둘 모두에 노출할 때 온도는 실질적으로 동일한 레벨로 유지된다.

[0041] 비결정질 층(513)과 하드 마스크(410), 스페이서들(420, 440) 및 게이트 유전체(310) 사이의 약한 화학적 결합으로 인해, 제 2 전구체는 그 위에 증착된 비결정질 층(513)을 쉽게 제거한다. 제 2 전구체는 비결정질 층(513)과 반응하여 그것을 부산물로 바꿈으로써, 비결정질 층(513)을 하드 마스크(410), 스페이서들(420, 440) 및 게이트 유전체(310)로부터 제거한다.

[0042] 한편, 에피택셜 막들(511, 512)은 오목한 소스 및 드레인 계면들(220, 230)과 강한 화학적 결합을 가진다. 강한 화학적 결합으로 인해, 에피택셜 막들(511, 512)의 작은 일부 만이 제 2 전구체에 의해 제거된다. 일 실시예에서, 도 5c 도중이나, 도 5d에서 기판(200)에 제 2 전구체를 노출하는 지속시간 동안 증착된 에피택셜 막들(511, 512)의 두께는 그 에피택셜 막들(511, 512)에 대한 충분한 두께를 유지하면서 비결정질 층(513)을 효과적으로 제거하도록 조정될 수 있다.

[0043] 도 5c 및 5d는 오목한 소스 및 드레인 계면들(220, 230) 위에 에피택셜 막들(511, 512)을 형성하는 한 번의 증착-에칭 주기를 예시한다. 일 실시예에서, 증착-에칭 주기는 같은 타입의 제 1 및 제 2 전구체들을 사용하여, 원하는 수의 에피택셜 막들이 증착될 때까지 반복된다. 예를 들어, 도 5e는 각기 10 개의 에피택셜 막들을 포함하는 에피택셜 영역들(531, 532)을 도시한다.

[0044] 에피택셜 영역들(531, 532)은 단지 각각 10 개 층의 에피택셜 막들에 국한되지 않는다는 것을 예상할 수 있다. 일 실시예에서 에피택셜 영역들(531, 532)을 형성하기 위해 약 3 내지 100 회의 증착-에칭 주기들이 수행된다. 특정 실시예에서, 약 30 나노미터의 두께를 가지는 에피택셜 영역들(531, 532)을 형성하기 위해 30 회의 증착-에칭 주기들이 수행된다.

[0045] 본 발명의 일 실시예에서 에피택셜 영역들(531, 532)은 탄소나 인의 등급별(graded) 농도를 이용하여 증착된다. 각각의 에피택셜 막 증착의 탄소 및 인 농도는 최적의 선택성 및 부결함 에피택셜를 제공하기 위해 최적화될 수 있다. 게다가 등급별 탄소나 인 농도는 증착-에칭 주기들 중에 비결정 물질의 제거를 촉진한다. 일 실시예에서 에피택셜 영역들(531, 532)(도 5e에 도시됨)의 등급별 탄소 농도는 최저 에피택셜 막에 대해 약 0.5 원자%로 시작하고 최상위 에피택셜 막에서 약 2 원자% 의 원하는 수준까지 점진적으로 증가된다. 다른 실시예에서 에피택셜 영역들(531, 532)의 등급별 인 농도는 최저 에피택셜 막에 대해 약 $8E19cm^{-3}$로 시작하고 최상위 에피택셜 막에서 약 $2E21cm^{-3}$의 원하는 레벨까지 점진적으로 증가된다. 일 실시예에서 에피택셜 영역들(531, 532)은 등급별 탄소 농도(0.5-2 원자%) 및 등급별 인 농도($8E19 - 2E21cm^{-3}$)의 조합을 이용하여 증착된다.

[0046] 에피택셜 영역들(531, 532)은 도 5e에 도시된 것과 같이 오목한 소스 및 드레인 계면들(220, 230) 위에 선택적으로 형성된다. 그러나, 각각의 증착-에칭 주기 도중 비결정질 층(513)의 제거는 스페이서들(420, 440)의 서면들(422, 442) 및 에피택셜 영역들(531, 532)의 상위 면들 사이에 형성되는 보이드나 중공들(281, 282)을 파생한다. 일 실시예에서, 중공들(281, 282)은 또한 게이트 유전체(310)의 일부분 및 에피택셜 영역들(531, 532) 사이에 연장되어 있다. 중공들(281, 282)은 트랜지스터 성능에 해로운 효과를 일으킬 수 있으므로 제거되어야 한다. 본 발명의 일 실시예에서, 중공들(281, 282)은 도 5f에 도시된 것과 같이 에피택셜 영역들(531, 532) 위에 선택적으로 증착된 캡 층들(541, 542)에 의해 실질적으로 메워진다.

[0047] 본 발명의 일 실시예에서 캡 층들(541, 542)은 기판(200)을 제 3 전구체에 노출시킴으로써 단일 증착 공정에서 에피택셜 영역들(531, 532) 위에 선택적으로 증착된다. 일 실시예에서, 제 3 전구체는 제 1 전구체의 동일한 실리콘 함유 화합물 및 도펀트, 그리고 제 2 전구체의 동일한 에천트 가스를 포함한다.

[0048] 에피택셜 영역들(531, 532)이 인으로 도핑된 실리콘 및 탄소를 가진 결정 막들인 경우, 제 3 전구체는 동일한 인 도펀트를 사용하여 캡 층들(541, 542)을 형성한다. 에피택셜 층들(531, 532)의 결정질 표면들은 그 위에서 캡 층들(541, 542)의 에피택셜 성장을 가능하게 하며, 그 결과 캡 층들(541, 542)은 인으로 도핑된 실리콘을 포함하는 에피택셜 층들이 된다. 중공들을 메우는 것과 별도로, 인 도핑된 실리콘 캡 층들(541, 542)은 채널 영

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역 상에 인장 응력을 유발하는 이점을 제공하고, 그로써 전자 이동성을 높이고 소자 성능을 개선한다.

[0049] 일 실시예에서 기판(200)을 실리콘 함유 화합물, 도펀트, 및 에천트 가스에 동시에 노출시키기 위해 병류(co-flown) 증착 기법이 사용된다. 일 실시예에서, 에천트 가스는 저메인(GeH_4)을 포함하지 않는다. 증착 중에, 에천드 가스가 하드 마스크(410) 및 스페이서들(420, 440) 상에 약하게 결합된 어떤 실리콘 및 인 함유 화합물을 쉽게 제거함으로써 캡 층들(541, 542)이 에피택셜 영역들(531, 532) 위에 증착되지만 하드 마스크(410)나 스페이서들(420, 440) 상에는 증착되지 않도록 한다.

[0050] 본 발명의 일 실시예에서, 기판(200)은 섭씨 약 550도 내지 800도의 온도에서, 약 10 토르 내지 대기압까지의 기압으로 약 30 내지 900초의 지속시간 동안 제 3 전구체에 노출된다. 특정 일 실시예에서, 기판(200)은 섭씨 635도의 온도에서, 600 토르(torr)의 기압으로 180초의 지속시간 동안 제 1 전구체에 노출된다.

[0051] 일 실시예에서 캡 층들(541, 542)은 약 50 내지 500 옹스트롬(Angstroms)의 두께를 가지도록 성장된다. 일 실시예에서 캡 층들(541, 542)은 300 옹스트롬의 두께를 가지도록 성장된다.

[0052] 스페이서(420) 및 게이트 유전체(310) 바로 아래의 캡 층(541) 및 에피택셜 영역들(531)의 일부들이 소스 에피-탭 영역(503)을 형성한다. 마찬가지로, 스페이서(440) 및 게이트 유전체(310) 바로 아래의 캡 층(542) 및 에피택셜 영역들(532)의 일부들이 드레인 에피-탭 영역(504)을 형성한다. 소스 및 드레인 에피 팁 영역들(503, 504)을 채널 영역에 상대적으로 근접하여 형성함으로써, 채널 영역에 보다 큰 등방 응력(hydrostatic stress)이 유도되고, 그 결과 보다 높은 전자 이동성 및 증가된 구동 전류를 파생한다. 응력은 에피택셜 영역들(531, 532)의 제조 중에 소스 및 드레인 에피-탭 영역들(503, 504)의 탄소 농도를 증가시킴으로써 더 증폭될 수 있다. 게다가, 소스 및 드레인 에피 팁 영역들(503, 504)의 탄소 농도는 또한 후속 열처리 중에 어떤 인 확산의 억제를 돕는다.

[0053] 본 발명의 일 실시예에서, 게이트 전극(320)은 나중에 교체 게이트 공정 시 실제 게이트 전극으로 교체되는 희생 게이트 전극이다. 일 실시예에서, 교체 게이트 공정은 캡 층들(541, 542) 위에 마스크를 증착하고, 그런 다음 하드 마스크(400)(미도시)와 동일 평면(coplanar)이 되도록 마스크를 평탄화하는 것에서 시작된다. 이어서, 잘 알려진 에칭 기법들을 이용하여 하드 마스크(410) 및 게이트 전극(320)이 제거된다. 하드 마스크(410) 및 게이트 전극(320)을 제거한 후, 이제 실제 게이트 전극이 게이트 유전체(310) 상에 증착된다. 일 실시예들에서 실제 게이트 전극(320)은 비한정적인 것으로서 백금, 텅스텐 또는 티타늄과 같은 물질들을 포함하는 금속 게이트 전극이다. 이것이 도 1에 도시된 반도체 디바이스의 제조를 마무리한다.

[0054] 도 6a-6f는 도 2와 관련하여 논의된 바와 같은 반도체 디바이스를 형성하는 방법을 예시한다. 반도체 디바이스의 제조는 도 6a에 도시된 것과 같이 기판(200)을 제공하는 것에서 시작된다. 도 6a에 도시된 반도체 디바이스는 도 5a와 동일하므로 상세히 논의되지는 않을 것이다. 간단히 말하면, 반도체 디바이스는 기판(200)의 원하는 채널 영역 위에 형성되는 게이트 유전체(310)를 포함한다. 게이트 전극(320)이 게이트 유전체(310) 위에 형성된다. 본 발명의 일 실시예에서, 게이트 전극(320)은 나중에 교체 게이트 공정 시 실제 게이트 전극으로 교체되는 희생 게이트 전극이다. 하드 마스크(410)는 게이트 전극 상부에 형성되고, 스페이서들(420, 440)은 게이트 전극(320)의 측벽들에서 형성된다.

[0055] 다음으로, 소스 영역 및 드레인 영역이 기판(200) 상에 형성된다. 본 발명의 일 실시예에서, 소스 및 드레인 영역들의 제조는 비한정적인 것으로서 건조 에칭 또는 습식 에칭과 같은 잘 알려진 에칭 기법들을 이용하여 기판(200)의 일부를 오목하게 함으로써 시작된다. 본 발명의 일 실시예에서, 기판(200)에 대해 실질적으로 선택성이 있는 습식 에칭이 기판(200)을 오목하게 하는데 사용되어, 도 6b에 도시된 것과 같은 오목한 소스 계면(240) 및 오목한 드레인 계면(250)을 형성하도록 한다.

[0056] 본 발명의 일 실시예에서, 기판(200)은 {001} 실리콘으로 이루어진다. 습식 에칭은 결정학적 방향에 기초하여 {001} 실리콘 기판(200)을 에칭하는 에천트 화학제를 이용하고, 특히 {001} 실리콘 기판(200)을 그 {111} 결정면을 따라 훨씬 더 느리게 에칭하여 {111} 면들(241, 251)을 형성하는데, 이는 에칭이 다른 결정학적 방향들로 훨씬 더 빠르게 진행하기 때문이다. 결국, 소스 에피 팁 중공(271)이 스페이서(420)의 저면(422)과 {111} 면(241) 사이에 형성된다. 드레인 에피 팁 중공(272)이 스페이서(440)의 저면과 {111} 면(251) 사이에 형성된다.

[0057] 습식 에칭 화학제는 암모니아 기반 혹은 아민 기반 에천트를 포함하나 그에 국한되지 않는다. 암모니아 기반 에천트들의 예들이 수산화 암모늄(NH4OH), 수산화 테트라메칠암모늄(TMAH) 및 수산화 벤질트리메칠암모늄(BTMH)이다. 습식 에칭 화학제는 수산화 칼륨(KOH) 및 수산화 나트륨(NaOH)과 같은 다른 타입의 에천트들을 포함한

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다.

[0058] 일 실시예에서 습식 에칭은 {001} 실리콘 기판(200)의 채널 영역 내에 {010} 면들(242, 252)을 더 생성한다. {010} 면들(242, 252)은 게이트 유전체(310) 바로 아래에서 연장되어 있다. 특정 실시예에서, {010} 면들(242, 252)은 게이트 유전체(310)로부터 약 3 나노미터의 길이까지 형성된다.

[0059] 다음으로, 기판(200)을 제 1 전구체(precursor) 및 제 2 전구체로 교대로 노출시킴으로써 오목한 소스 및 드레인 계면들(240, 250) 각각 위에 에피택셜 영역이 증착된다. 도 6c, 6d 및 6e에 예시된 바와 같이, 에피택셜 영역을 제조하는 방법은 도 5c, 5d 및 5e에 논의된 제조 방법들과 유사하다. 기판(200)을 제 1 전구체에 노출시키기 전에, 에피택셜 성장을 촉진하고 표면 결함들을 줄이기 위해 표면 전처리 옵션이 기판(200) 상에서 수행될 수 있다. 일 실시예에서 표면 전처리는 오목한 소스 및 드레인 계면들(240, 250)을 세정하기 위해 도 5c에 앞서 논의된 바와 같이 수소 베이킹 처리 및/또는 에칭 단계를 포함한다.

[0060] 도 6c로부터 시작할 때, 오목한 소스 및 드레인 계면들(240, 250) 상에 에피택셜 막들(511, 512)을 증착하기 위해 전체 기판(200)이 제 1 전구체로 노출된다. 각자의 {111} 면들(241, 251) 및 {010} 면들(242, 252)을 포함하는 오목한 소스 및 드레인 계면들(240, 250)은 그 위에 에피택셜 막들(511, 512)의 에피택셜 성장을 가능하게 하는 단결정 표면이다. 한편, 하드 마스크(410), 스페이서들(420, 440), 및 게이트 유전체(310)는 비결정 표면들이고, 따라서 비결정질 층(513)이 그 위에 증착된다. 도 5c와 관련하여 논의된 바와 같이 동일한 제 1 전구체 및 공정 조건들이 여기에 적용될 수 있으므로 더 논의하지 않을 것이다.

[0061] 다음으로, 도 6d에서, 스페이서들(420, 440)의 측벽들(421, 441) 및 저면들(422, 442)로부터 비결정질 층(513)을 제거하기 위해 전체 기판(200)이 마찬가지로 제 2 전구체로 노출된다. 게다가 제 2 전구체는 하드 마스크(410) 상과 게이트 유전체(310) 밑에서 형성되는 어떤 비결정질 층(513) 역시 제거한다. 도 5d와 관련하여 논의된 바와 같이 동일한 제 2 전구체 및 공정 조건들이 여기에 적용될 수 있으므로 더 논의하지 않을 것이다.

[0062] 도 6c 및 6d는 각자의 {111} 면들(241, 251) 및 {010} 면들(242, 252)을 포함하는 오목한 소스 및 드레인 계면들(240, 250) 위에 에피택셜 막들(511, 512)을 형성하는 일 회의 증착-에칭 주기를 예시한다. 이 증착-에칭 주기는 원하는 개수의 에피택셜 막들이 증착될 때까지 반복된다. 예시의 목적으로, 도 6e는 각기 10 개의 에피택셜 막들을 포함하는 에피택셜 영역들(531, 532)을 도시한다. 본 발명의 일 실시예에서 에피택셜 영역들(531, 532)은 앞서 도 5e에 기술된 바와 같이, 탄소나 인의 등급별(graded) 농도를 이용하여 증착된다. 예를 들어, 에피택셜 영역들(531, 532)(도 6e에 도시됨)은 최저 에피택셜 막에 대해 0.5 원자% 의 등급별 탄소 농도로 증착되고, 최상의 에피택셜 막에 대해 원하는 수준의 약 2 원자% 까지 점진적으로 증가된다. 다른 대안으로서, 에피택셜 영역들(531, 532)은 최저 에피택셜 막에 대해 약 8E19cm^{-3}의 등급별 인 농도 수준을 이용하여 증착되고 최상위 에피택셜 막에 대해 약 2E21cm^{-3}의 원하는 수준까지 점진적으로 증가된다. 일 실시예에서 에피택셜 영역들(531, 532)은 등급별 탄소 농도(0.5-2 원자%) 및 등급별 인 농도(8E19 - 2E21cm^{-3})의 조합을 이용하여 증착된다.

[0063] 각각의 증착-에칭 주기 도중 비결정질 층(513)의 제거는 마찬가지로, 스페이서들(420, 440)의 저면들(422, 442) 및 에피택셜 영역들(531, 532)의 상위 면들 사이에 형성되는 보이드나 중공들(281, 282)을 파생한다. 중공들(281, 282)은 도 6f에 도시된 것과 같이 에피택셜 영역들(531, 532) 위에 선택적으로 증착된 캡 층들(541, 542)에 의해 실질적으로 메워진다.

[0064] 일 실시예에서 캡 층들(541, 542)은 기판(200)을 제 3 전구체에 노출시킴으로써 단일 증착 공정에서 에피택셜 영역들(531, 532) 위에 선택적으로 증착된다. 도 5f와 관련하여 논의된 바와 같이 동일한 제 2 전구체 및 공정 조건들이 여기에 적용될 수 있으므로 더 논의하지 않을 것이다. 에피택셜 영역들(531, 532)이 인으로 도핑된 실리콘 및 탄소를 가진 결정 막들인 경우, 제 3 전구체는 동일한 인 도펀트를 사용하여 캡 층들(541, 542)을 형성한다. 에피택셜 영역들(531, 532)의 결정질 표면들은 그 위에서 캡 층들(541, 542)의 에피택셜 성장을 가능하게 하며, 그 결과 캡 층들(541, 542)은 인으로 도핑된 실리콘을 포함하는 에피택셜 층들이 된다. 이것이 도 2에 도시된 반도체 디바이스의 제조를 마무리한다.

[0065] 도 7a-7c는 도 3과 관련하여 논의된 바와 같은 반도체 디바이스를 형성하는 방법을 예시한다. 도 7a로부터 시작할 때, 반도체 디바이스의 제조가 기판(200)을 제공함으로써 시작된다. 도 7a에 도시된 반도체 디바이스는 도 5a와 동일하므로 상세히 논의되지는 않을 것이다.

[0066] 다음으로, 소스 영역 및 드레인 영역이 기판(200) 상에 형성된다. 본 발명의 일 실시예에서, 소스 및 드레인

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영역들의 제조는 비한정적인 것으로서 건조 에칭 또는 습식 에칭과 같은 잘 알려진 에칭 기법들을 이용하여 기판(200)의 일부를 오목하게 함으로써 시작된다. 일 실시예에서, 기판(200)을 오목하게 하기 위해 도 6b에서 사용된 습식 에칭이 여기에 적용되어 도 7b에 도시된 것과 같은 오목한 소스 계면(240) 및 오목한 드레인 계면(250)을 형성하도록 한다. 습식 에칭은 도 6b와 관련하여 기술된 것과 동일한 에천트 화학제를 이용하여 {001} 실리콘 기판(200)의 {111} 결정면 내에 {111} 면들(241, 251)을 형성한다. 일 실시예에서 습식 에칭은 {001} 실리콘 기판(200)의 채널 영역 내에 {010} 면들(242, 252)을 더 생성한다.

[0067] 이어서, 에피택셜 층들(610, 620)이 도 7c에 도시된 것과 같이 오목한 소스 및 드레인 계면들(240, 250) 위에 선택적으로 증착된다. 본 발명의 일 실시예에서 기판(200)을 에천트 가스를 포함하는 전구체에 노출시킴으로써 에피택셜 층들(610, 620)이 단일 증착 공정 안에서 선택적으로 증착된다.

[0068] 일 실시예에서 전구체는 도 5c에 유사하게 기술된 실리콘 함유 화합물 및 도펀트를 포함한다. 일 실시예에서, 실리콘 함유 화합물은 비한정적인 것으로서 실란(silanes) 및 할로겐화 실란을 포함한다. 그러한 실리콘 함유 화합물은 실란(SiH4), 디실란(Si2H6), 트리실란(Si3H8), 디클로로실란(S1H2C12), 및 펜타 클로로 실란을 포함한다. 본 발명의 일 실시예에서, 도펀트는 비한정적인 것으로서 인이나 비소와 같은 n-타입 도펀트이다. 일 실시예에서, 인 도펀트는 N_2나 Ar과 같은 불활성 기체나 수소로의 어떠한 희석도 없이 인화수소(PH_3)를 사용하여 에피택셜 층들 안으로 도입된다. 다른 실시예에서, 예컨대 수소(H_2) 내 3%의 인화수소(PH_3) 혼합물과 같이, 인화수소 가스가 수소와 혼합된다. 일 실시예에서 전구체의 에천트 가스는 비한정적인 것으로서 수소(H_2) 및 무수 염산(HCl)을 포함한다.

[0069] 일 실시예에서 에천트 가스를 포함하는 전구체를 기판(200)으로 동시에 전달하기 위해 병류(co-flown) 증착 기법이 사용된다. 일 실시예에서, 기판(200)은 섭씨 약 550도 내지 800도의 온도에서, 약 10 토르 내지 대기압까지의 기압으로 약 30 내지 2000초의 지속시간 동안 전구체에 노출된다. 특정 실시예에서, 기판(200)은 섭씨 635도의 온도에서, 600 토르(torr)의 기압으로 800초의 지속시간 동안 제 1 전구체에 노출된다.

[0070] 일 실시예에서 에피택셜 층들(610, 620)은 약 30 내지 2000 옹스트롬(Angstroms)의 두께를 가지도록 성장된다. 특정 실시예에서 에피택셜 층들(610, 620)은 750 옹스트롬의 두께를 가지도록 성장된다. 인 도펀트가 사용되는 경우, 에피택셜 계층들(610, 620)은 인으로 도핑된 실리콘을 포함한다.

[0071] 기판(200)이 단결정 실리콘으로 이루어지는 경우, 각자의 {111} 면들(241, 251) 및 {010} 면들(242, 252)을 포함하는 오목한 소스 및 드레인 계면들(242, 252)은 그 위에서 에피택셜 막들(610, 620)의 에피택셜 성장을 가능하게 하는 단결정 표면들이다. 하드 마스크(410) 및 스페이서들(420, 440)이 비결정 표면들을 가지기 때문에, 증착 중에 에천트 가스가 하드 마스크(410) 및 스페이서들(420, 440) 상에 약하게 결합된 어떤 실리콘 및 인 함유 화합물을 쉽게 제거함으로써 에피택셜 층들(610, 620)은 오목한 소스 및 드레인 계면들(240, 250) 위에 증착되지만 하드 마스크(410)나 스페이서들(420, 440) 상에는 증착되지 않는다.

[0072] 스페이서(420) 및 {111}, {010} 면들(241, 242) 사이에 증착된 에피택셜 층(610)의 일부가 소스 에피 팁 영역(611)을 형성한다. 마찬가지로, 스페이서(440) 및 {111}, {010} 면들(251, 252) 사이에 증착된 에피택셜 층(620)의 일부가 드레인 에피 팁 영역(621)을 형성한다. 소스 및 드레인 에피 팁 영역들(611, 621)을 채널 영역에 상대적으로 근접하여 형성함으로써, 채널 영역에 보다 큰 등방 응력(hydrostatic stress)이 유도되고, 그 결과 보다 높은 전자 이동성을 낳게 된다. 게다가, 인 도핑된 실리콘 에피택셜 층들(610, 620)은 채널 영역 상에 인장 응력을 포함하고, 그로써 전자 이동성을 높이고 소자 성능을 개선한다. 이것이 도 3에 도시된 반도체 디바이스의 제조를 마무리한다.

[0073] 또한, 에피택셜 성장을 촉진시키고 표면 결함을 줄이기 위해 기판을 전구체에 노출시키기 전에 옵션 표면 전처리가 기판(200) 상에서 수행될 수 있다. 예를 들어, 각자의 {111} 면들(241, 251) 및 {010} 면들(242, 252)을 포함하는 오목한 소스 및 드레인 계면들(240, 250)을 세정하기 위해, 도 5c와 관련하여 기술된 것과 유사한 수소 베이킹 처리가 기판(200)(도 7b) 상에서 수행된다.

[0074] 도 8a-8i는 도 4와 관련하여 논의된 바와 같은 트리게이트(tri-gate) 소자를 형성하는 방법을 예시한다. 트리게이트 소자의 제조는 도 8a에 도시된 것과 같이 기판(200)을 제공하는 것에서 시작된다. 기판(200)은 기판(200)으로부터 절연 영역들(710, 720)을 통과해 연장된 반도체 바디 또는 핀(260)을 포함한다. 일 실시예에서 절연 영역들(710, 720)은 트렌치들을 형성하기 위해 기판(200)을 에칭하고 그런 다음 그 트렌치들 상에 산화 물질을 증착하여 얕은 트렌치 절연(STI(shallow trench isolation)) 영역들을 형성하는 것과 같은 전형적 기법들

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에 의해 형성되는 STI 영역들이다. 절연 영역들(710, 720)은 비한정적인 것으로서 산화 실리콘(e.g., SiO_2)과 같은 어떤 잘 알려진 절연 물질로 이루어진다.

[0075] 일 실시예에서, 핀(260)은 절연 영역들(700) 위의 상면(261)을 포함한다. 핀(260)은 절연 영역(710) 위에 노출되는 전면(262) 및 절연 영역(720) 위에 노출되는 후면(263)을 더 포함한다. 일 실시예에서, 핀(260)은 기판(200)과 동일한 반도체 물질들로 이루어진다.

[0076] 이어서, 도 8b에서 게이트 유전체(330)가 상면(261), 전면(262) 및 후면(263)의 일부 위에 형성된다. 일 실시예에서, 게이트 유전체(330)는 비한정적인 것으로서 물리적 증기 증착법(PVD(physical vapor deposition)), 화학적 증기 증착법(CVD(chemical vapor deposition)), 또는 원자 층 증착법(ALD(atomic layer deposition))과 같은 어떤 잘 알려진 방법들에 의해 형성된다.

[0077] 그런 다음, 게이트 전극(340)이 게이트 유전체(330) 및 게이트 전극(340)의 양측에 있는 핀(260)의 노출 부분들(264) 위에 형성된다. 일 실시예에서 게이트 전극(340)은 비한정적인 것으로서 폴리실리콘(polysilicon)과 같은 어떤 잘 알려진 절연 물질로 이루어진다. 상면(261), 전면(262) 및 후면(263) 위에 형성되는 게이트 전극(340)은 트리게이트 소자의 세 개의 게이트들을 생성한다. 그런 다음 하드 마스크(410)가 게이트 전극(320)의 상부에 형성된다.

[0078] 이어서, 도 8c에 도시된 것과 같이 게이트 스페이서들(460, 470)이 게이트 전극(340)의 양편 측벽들 상에 증착된다. 일 실시예에서 스페이서들(460, 470)은 게이트 전극(320)을 포함하는 전체 기판(200) 위에 스페이서 물질 층을 증착하고 그런 다음 게이트 전극(340)의 측벽들 상에 스페이서들(460, 470)을 형성하기 위해 스페이서 물질 층을 비등방성으로 에칭하는 것과 같은 잘 알려진 기법을 이용함으로써 형성된다. 동시에, 핀 스페이서들(480, 490)이 핀(260)의 노출 부분들(264, 265)의 측벽들 상에 형성된다. 일 실시예에서 게이트 스페이서들(460, 470) 및 핀 스페이서들(480, 490)은 비한정적인 것으로서 질화 실리콘, 이산화 실리콘, 또는 산질화 실리콘과 같은 물질로 이루어진다.

[0079] 다음으로, 소스 영역 및 드레인 영역이 기판(200) 상에 형성된다. 본 발명의 일 실시예에서, 소스 및 드레인 영역들의 제조는 도 8d에서, 핀(260)의 노출 부분들(264, 265)의 측벽들로부터 핀 스페이서들(480, 490)을 제거함으로써 시작된다. 핀 스페이서들(480, 490)은 비한정적인 것으로서 건식 에칭이나 습식 에칭과 같은 잘 알려진 에칭 기법들에 의해 제거된다.

[0080] 일 실시예에서, 핀(260)의 노출 부분들(264, 265)로부터 핀 스페이서들(480, 490)을 완벽하게 제거하기 위해 비등방성 습식 에칭이 사용된다. 동시에 그 비등방성 습식 에칭은 게이트 스페이서들(460, 470)의 일부를 또한 제거하고, 그로써 하드 마스크(410) 측벽들의 일부를 노출시킨다. 게이트 스페이서들(460, 470)이 핀 스페이서들(480, 490) 보다 더 큰 높이 및 두께를 가지기 때문에, 비등방성 습식 에칭은 게이트 스페이서들(460, 470)보다 빠르게 핀 스페이서들(480, 490)을 제거한다. 비등방성 습식 에칭은 핀 스페이서들(480, 490)을 완벽하게 제거하지만 게이트 전극(340) 측벽들이 노출되지 않도록 게이트 전극(340) 상에 충분한 두께의 게이트 스페이서들(460, 470)을 남겨두도록 조절될 수 있다.

[0081] 이어서, 핀(260)의 노출 부분들(264, 265)을 오목하게 하기 위한 에칭이 기판(200) 상에서 수행된다. 일 실시예에서 그 에칭은 노출 부분(264)을 오목하게 하기 위해 핀(260)에 대해 실질적으로 선택적인 에천트 화학제를 이용하여, 도 8e에 도시된 것과 같이 절연 영역들(710, 720)의 상면 아래에 오목한 소스 계면(266)을 형성하고 핀 측벽(267)을 형성하도록 한다. 게이트 전극(340)의 다른 측면 상에서, 노출 부분(264)이 오목하게 되어 오목한 드레인 계면(268) 및 핀 측벽(269)을 형성한다. 일 실시예에서 오목한 소스 및 드레인 계면들(266, 268)은 절연 영역들(710, 720)의 상면 아래에서 약 100 내지 400 옹스트롬이 된다.

[0082] 도 9는 상면(261)으로부터 오목한 소스 계면(266)까지 연장된 핀 측벽(267) 및 상면(261)으로부터 오목한 드레인 계면(268)까지 연장된 핀 측벽(269)을 도시한 트리게이트 소자의 단면도를 예시한다. 본 발명의 일 실시예에서 핀 측벽들(267, 269)은 게이트 스페이서들(460, 470)의 측벽들(461, 471)과 실질적으로 동일 평면이거나 동일 면이다. 일 실시예에서 핀 측벽들(267, 269)은 기판(200)의 {110} 결정면 내 {110} 면들이고, 오목한 소스 및 드레인 계면들(266, 268)은 기판(200)의 {100} 결정면 내 {100} 면들이다.

[0083] 다른 대안적 실시예에서는 게이트 스페이서들(460, 470) 안에서 오목한 핀 측벽들(267, 269)을 형성하기 위해 등방성 에칭이 사용된다. 도 8ee는 게이트 스페이서(470) 안에 오목한 핀 측벽(267)을 보여주는 트리게이트 소자의 사시도이다. 도 9a는 게이트 스페이서(460, 470) 아래에서 오목한 두 핀 측벽들(267, 269)을 도시한 단면도이다. 일 실시예에서 핀 측벽들(267, 269)은 게이트 스페이서 측벽들(461, 471)로부터 약 25 내지 200 옹스

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트롬까지 오목하다.

[0084] 도 8e부터 계속하여, 기판(200)을 제 1 전구체 및 제 2 전구체로 교대로 노출시킴으로써 오목한 소스 및 드레인 계면들(266, 268) 각각 위에 이제 에피택셜 영역이 증착된다. 도 8f, 8g 및 8h에 예시된 바와 같이, 에피택셜 영역을 제조하는 방법은 도 5c, 5d 및 5e에 논의된 제조 방법들과 유사하다.

[0085] 도 8f로부터 시작할 때, 오목한 소스 계면(266) 및 핀 측벽(267) 상에 에피택셜 막(511)을 증착하기 위해 전체 기판(200)이 제 1 전구체로 노출된다. 동시에, 도 10의 단면도에 도시된 바와 같이 오목한 드레인 계면(268) 및 핀 측벽(269) 상에 에피택셜 막(512)이 증착된다. 오목한 소스 및 드레인 계면들(266, 268), 및 핀 측벽들(267, 269)은 그 위에 에피택셜 막들(511, 512)의 에피택셜 성장을 가능하게 하는 단결정 표면들이다. 한편, 하드 마스크(410), 게이트 스페이서들(460, 470), 및 절연 영역들(710, 720)은 비결정 표면들이고, 따라서 비결정질 층(513)이 그 위에 형성된다. 도 5c와 관련하여 논의된 바와 같이 동일한 제 1 전구체 및 공정 조건들이 여기에 적용될 수 있으므로 더 논의하지 않을 것이다.

[0086] 다음으로, 도 8g에서, 게이트 스페이서들(460, 470) 및 절연 영역들(710, 720)로부터 비결정질 층(513)을 제거하기 위해 전체 기판(200)이 마찬가지로 제 2 전구체로 노출된다. 게다가 제 2 전구체는 하드 마스크(410) 상에 형성된 어떤 비결정질 층(513)을 또한 제거한다. 도 11은 비결정질 층(513)이 제거된 뒤 트리게이트 소자의 난년도를 도시한다. 도 5d와 관련하여 논의된 바와 같이 동일한 제 2 전구체 및 공정 조건들이 여기에 적용될 수 있으므로 더 논의하지 않을 것이다.

[0087] 도 8f-8g 및 eh 10-11은 오목한 소스 및 드레인 계면들(267, 268) 및 핀 측벽들(267, 269) 위에 에피택셜 막들(511, 512)을 형성하는 한 번의 증착-에칭 주기를 예시한다. 이 증착-에칭 주기는 원하는 개수의 에피택셜 막들이 증착될 때까지 반복된다. 일 실시예에서, 마지막 에피택셜 영역들(531, 532)은 도 12에 도시된 것과 같이 다섯 개의 에피택셜 막들을 포함한다. 본 발명의 일 실시예에서 에피택셜 영역들(531, 532)은 앞서 도 5e에 기술된 바와 같이, 탄소나 인의 등급별(graded) 농도를 이용하여 증착된다. 예를 들어, 에피택셜 영역들(531, 532)(도 12에 도시됨)은 최저 에피택셜 막에 대해 0.5 원자% 의 등급별 탄소 농도로 증착되고, 최상의 에피택셜 막에 대해 원하는 수준의 약 2 원자% 까지 점진적으로 증가된다. 다른 대안으로서, 에피택셜 영역들(531, 532)은 최저 에피택셜 막에 대해 약 8E19cm^{-3}의 등급별 인 농도 수준을 이용하여 증착되고 최상위 에피택셜 막에 대해 약 2E21cm^{-3}의 원하는 수준까지 점진적으로 증가된다. 일 실시예에서 에피택셜 영역들(531, 532)은 등급별 탄소 농도(0.5-2 원자%) 및 등급별 인 농도(8E19 - 2E21cm^{-3})의 조합을 이용하여 증착된다.

[0088] 핀 측벽들(267, 269)이 게이트 스페이서들(460, 470) 안에서 오목하게 되는 다른 대안적 실시예에서, 에피택셜 영역들(531, 532)은 트리게이트 소자의 채널 영역에 인접하여 형성되고, 그에 따라 채널 영역 상에서 보다 높은 응력량을 유발한다.

[0089] 각각의 증착-에칭 주기 도중 비결정질 층(513)의 제거는 도 8h 및 13에 도시된 바와 같이 에피택셜 영역들(531, 532) 및 절연 영역들(710, 720) 사이에 형성되는 보이드들이나 중공들(281, 282)을 마찬가지로 파생시킨다. 중공들(281, 282)은 도 8, 14 및 15에 도시된 것과 같이 에피택셜 영역들(531, 532) 위에 선택적으로 증착된 캡 층들(541, 542)에 의해 실질적으로 메워진다.

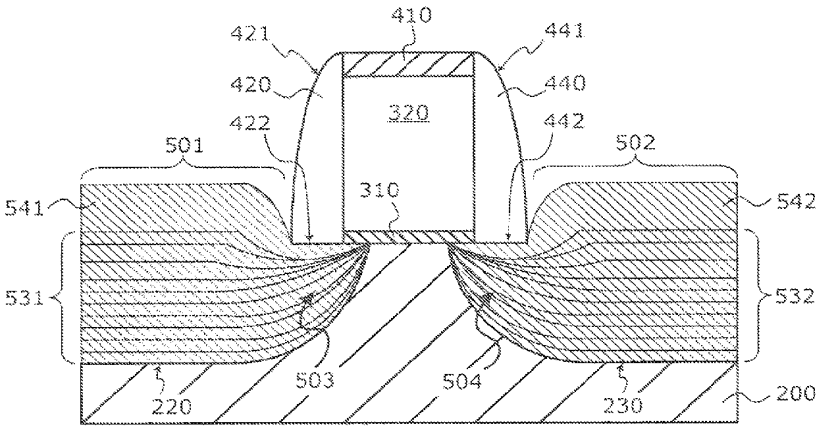
[0090] 일 실시예에서 캡 층들(541, 542)은 기판(200)을 제 3 전구체에 노출시킴으로써 단일 증착 공정에서 에피택셜 영역들(531, 532) 위에 선택적으로 증착된다. 도 5f와 관련하여 논의된 바와 같이 동일한 제 2 전구체 및 공정 조건들이 여기에 적용될 수 있으므로 더 논의하지 않을 것이다. 에피택셜 영역들(531, 532)이 인으로 도핑된 실리콘 및 탄소를 가진 결정 막들인 경우, 제 3 전구체는 동일한 인 도펀트를 사용하여 캡 층들(541, 542)을 형성한다. 에피택셜 영역들(531, 532)의 결정질 표면들은 그 위에서 캡 층들(541, 542)의 에피택셜 성장을 가능하게 하며, 그 결과 캡 층들(541, 542)은 인으로 도핑된 실리콘을 포함하는 에피택셜 층들이 된다. 인 도핑된 실리콘 캡 층들(541, 542)은 반도체 핀(260)의 채널 영역에 인장 응력을 유발하는 이점을 제공하고, 이는 전자 이동성을 높이며 소자 성능을 개선시킨다. 이것이 도 4에 도시된 반도체 디바이스의 제조를 마무리한다.

[0091] 본 발명의 여러 실시예들이 앞에서와 같이 설명되었다. 그러나, 이 분야의 당업자는 본 발명의 기술된 실시예들에 국한되지 않으며 뒤따르는 첨부된 청구범위의 사상 및 범위 안에서 수정과 변형을 하여 실시될 수 있다는 것을 인식할 수 있을 것이다.

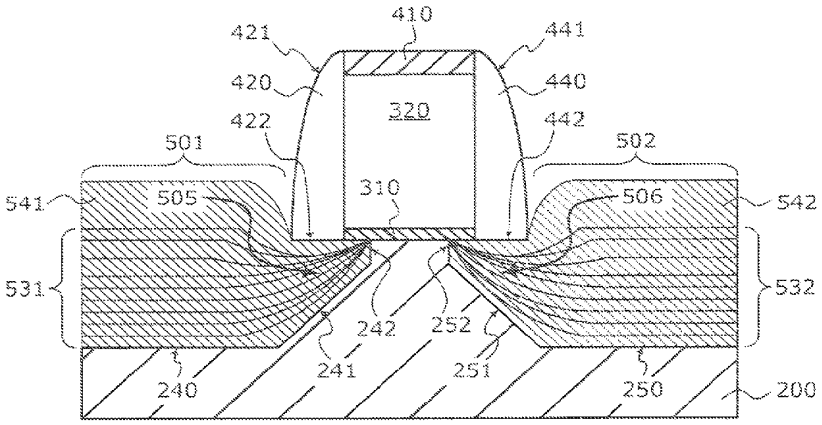
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도면

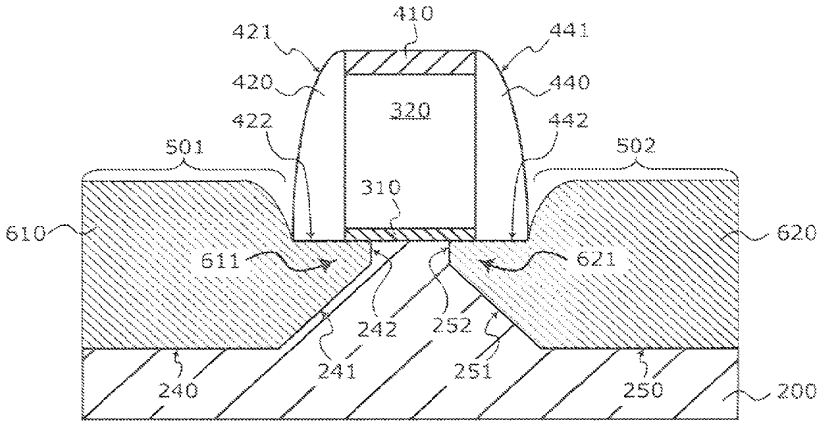
도면1



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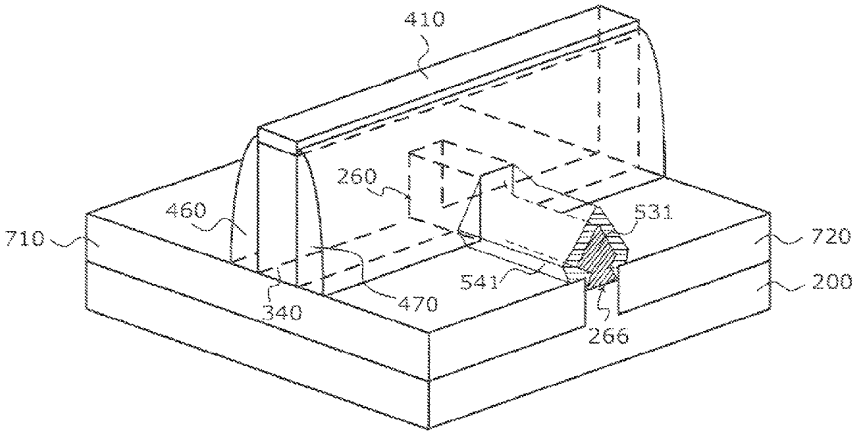


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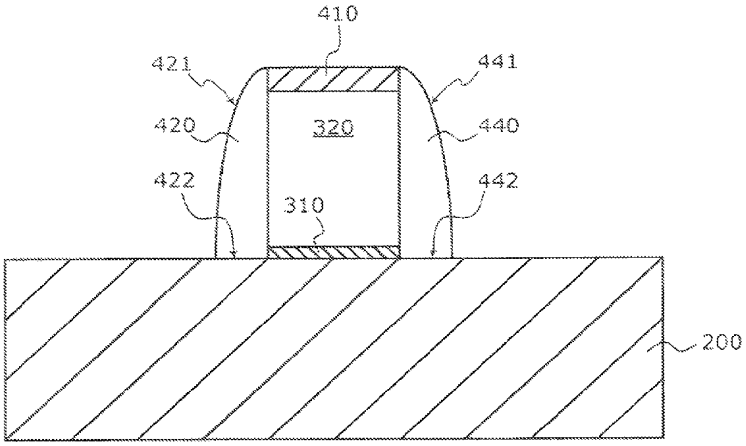


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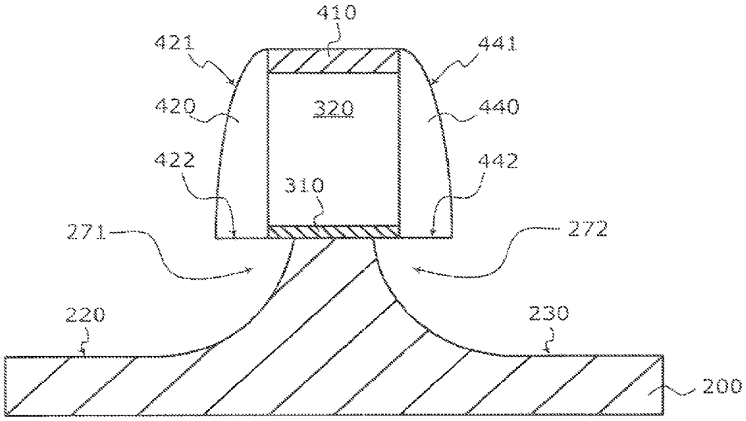
도면4



도면5a

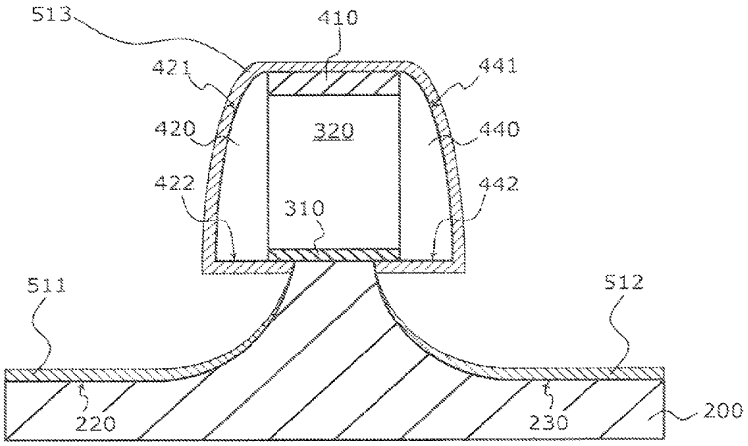


도면5b

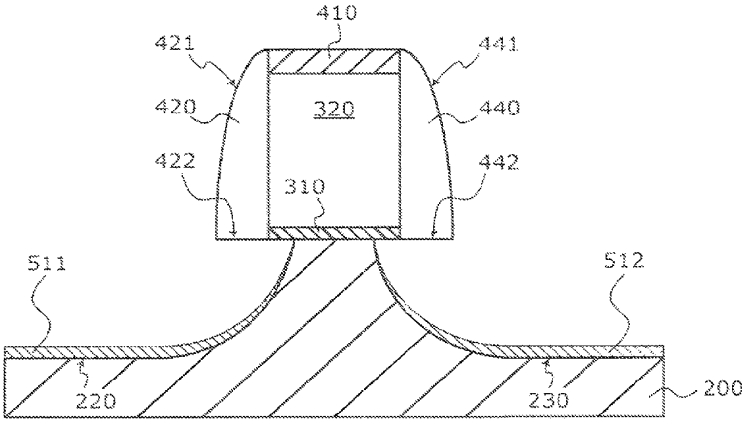


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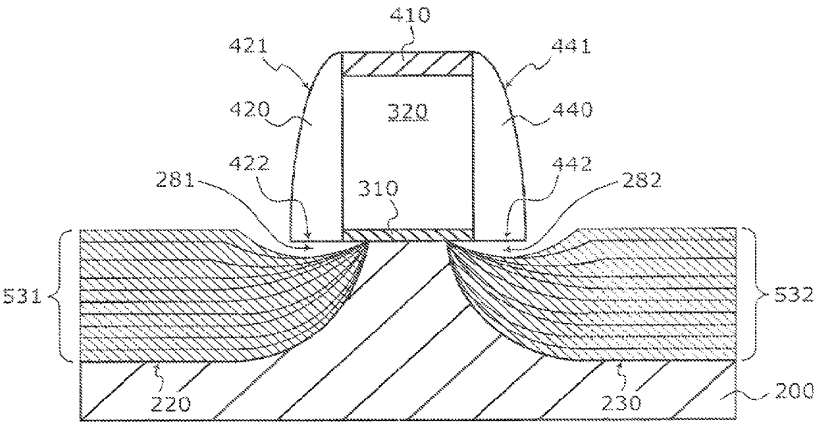
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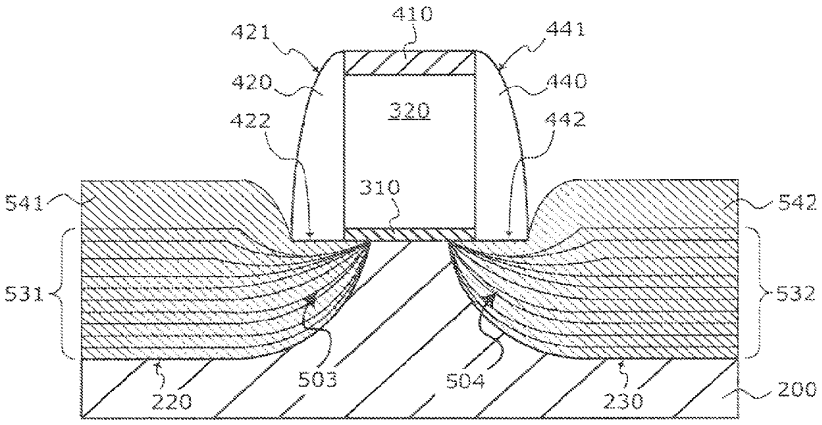
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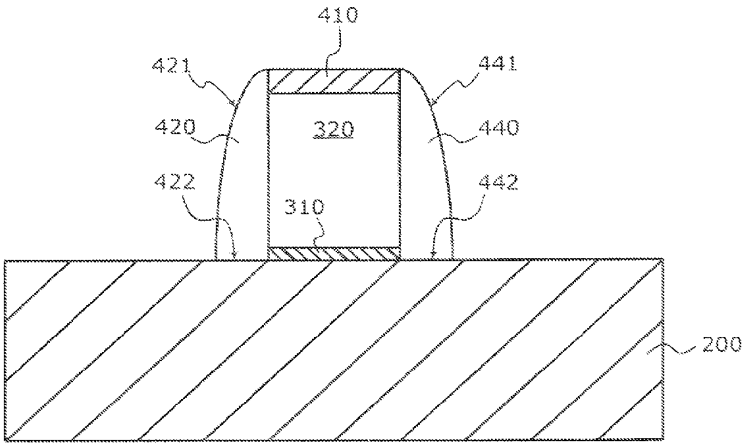
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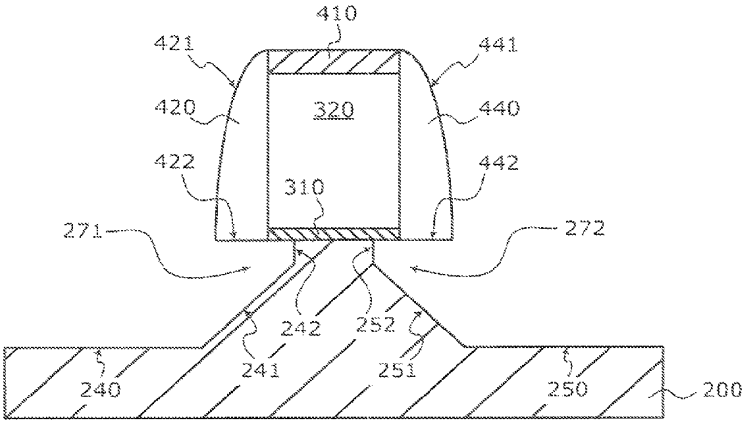
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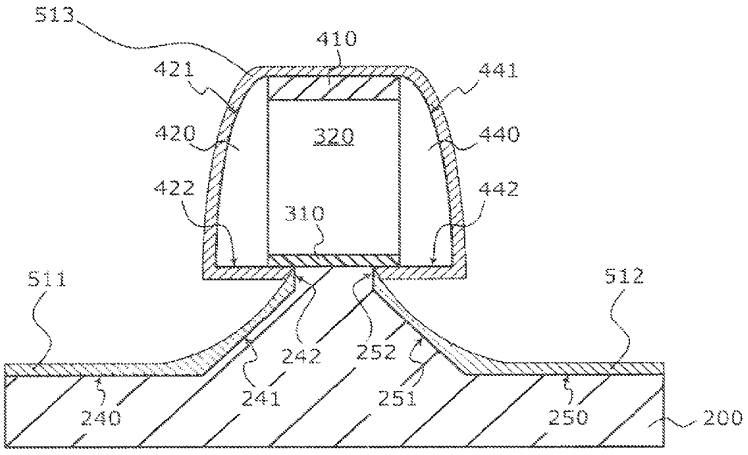
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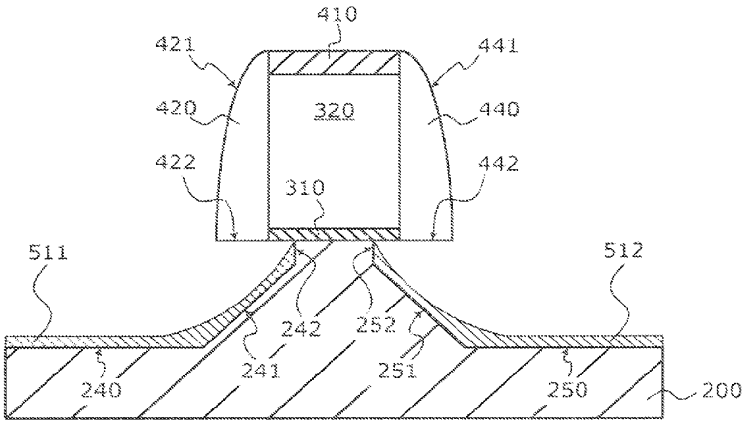
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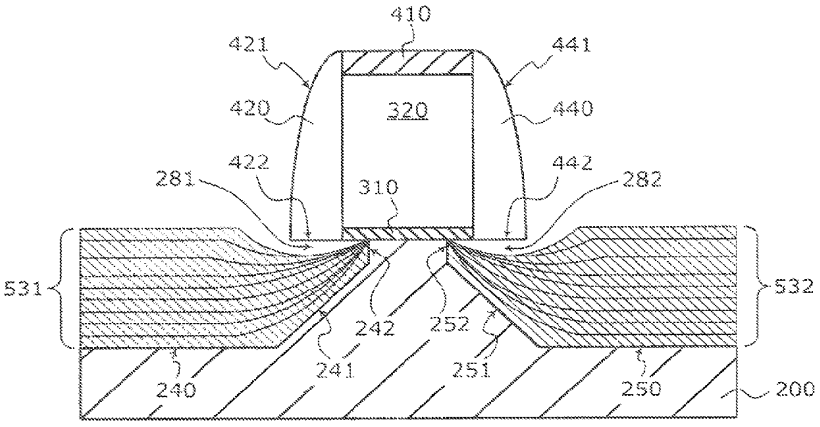
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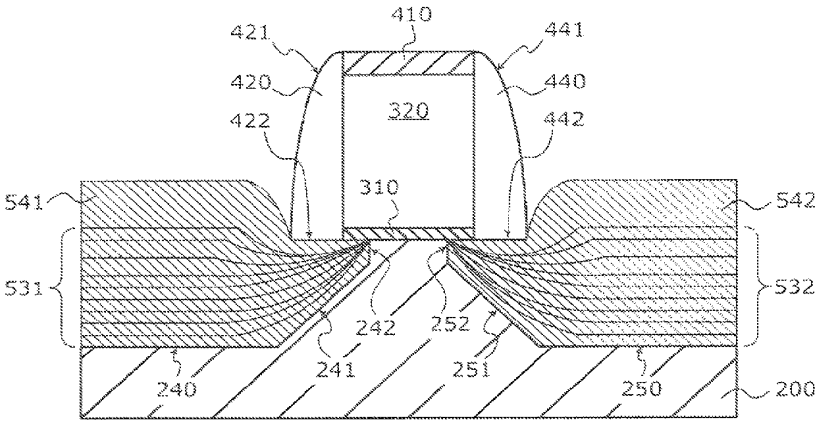
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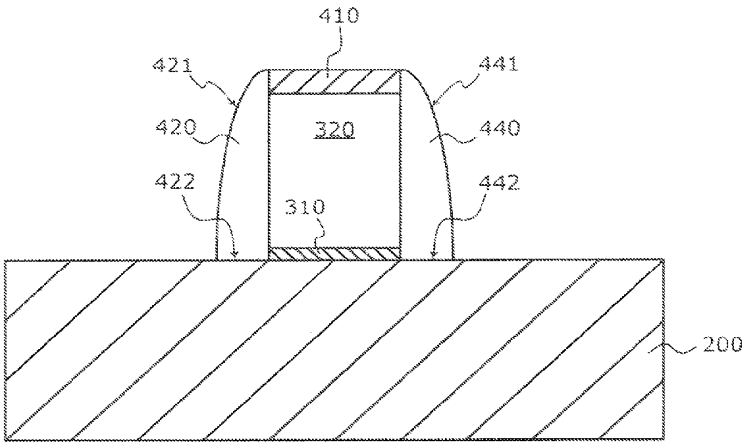
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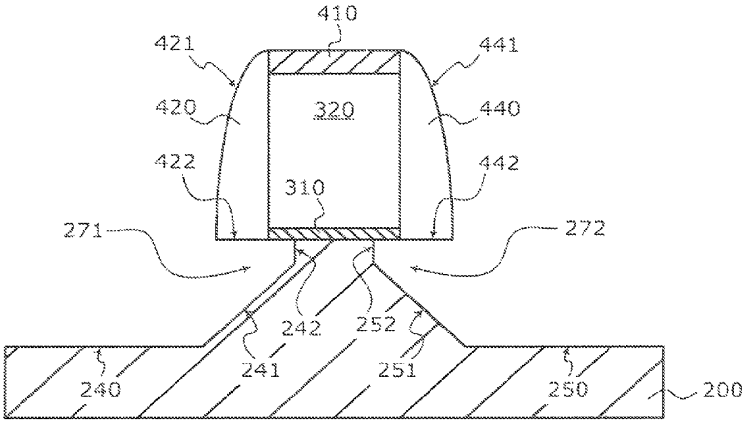
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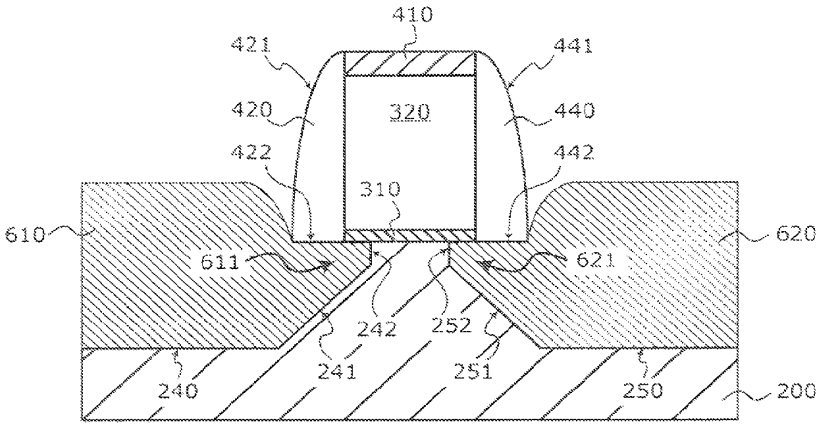
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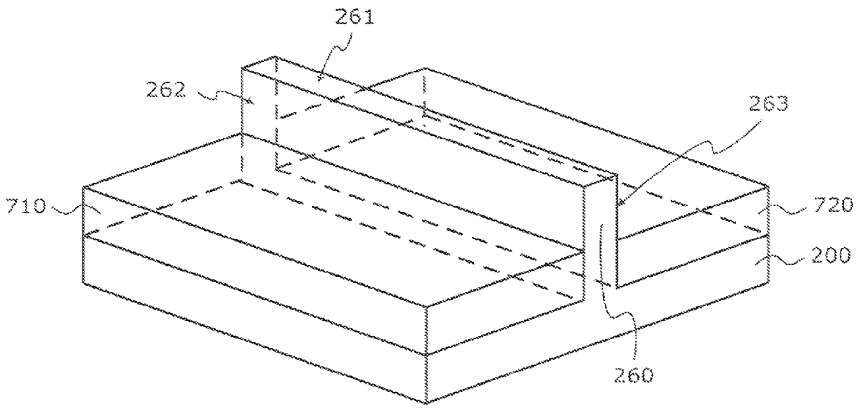
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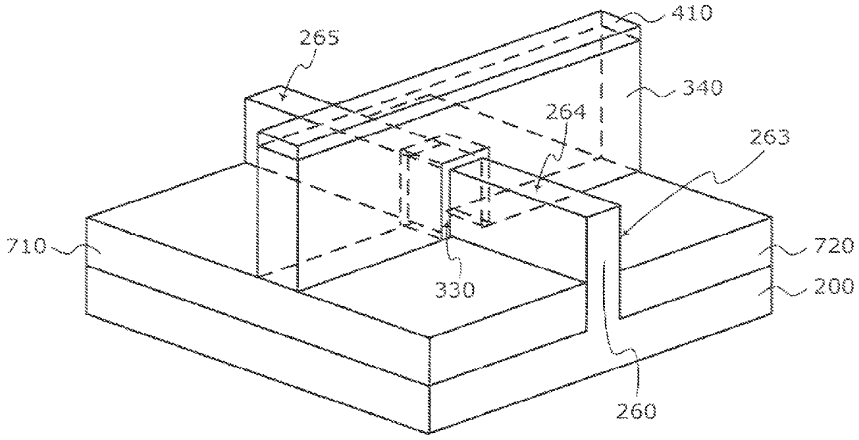
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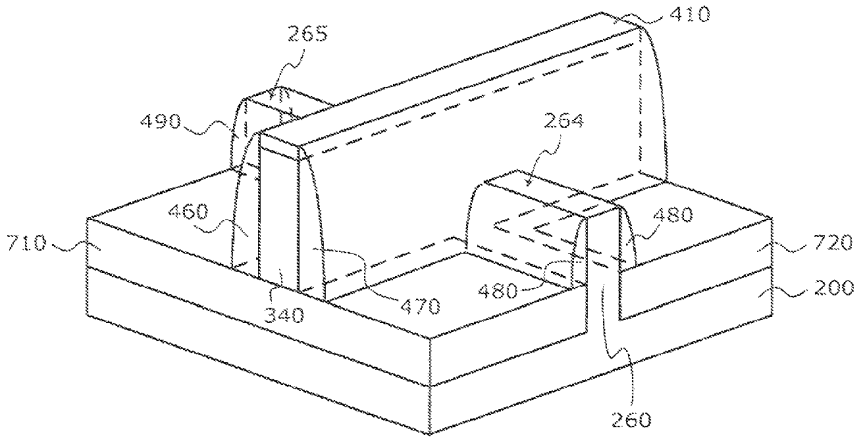
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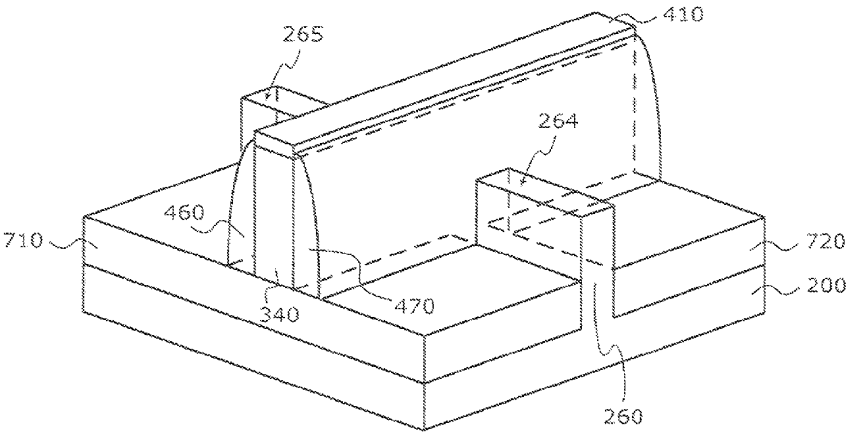
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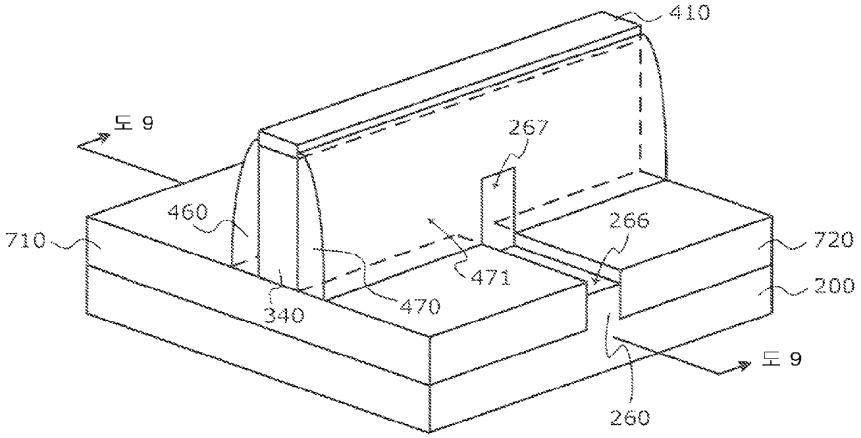
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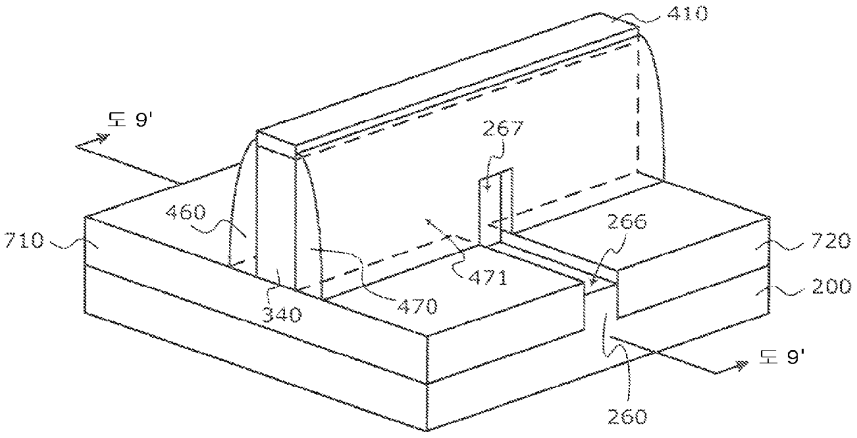
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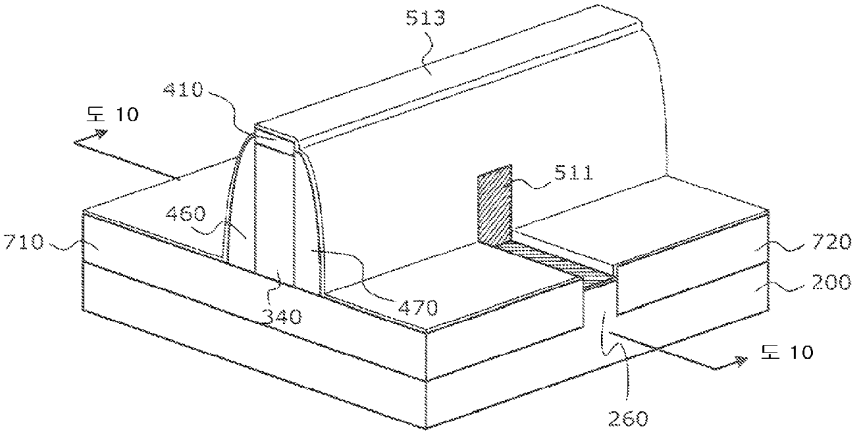
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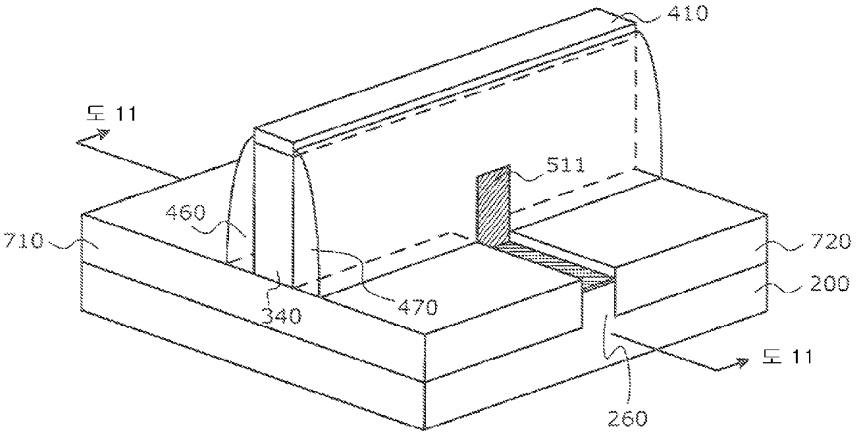
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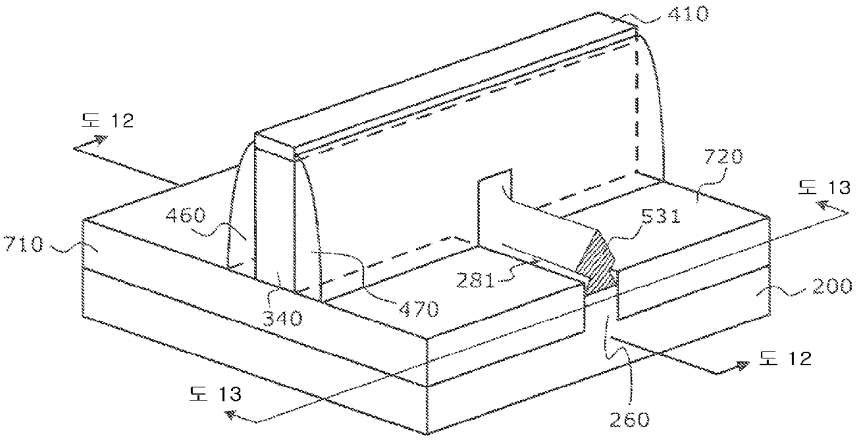
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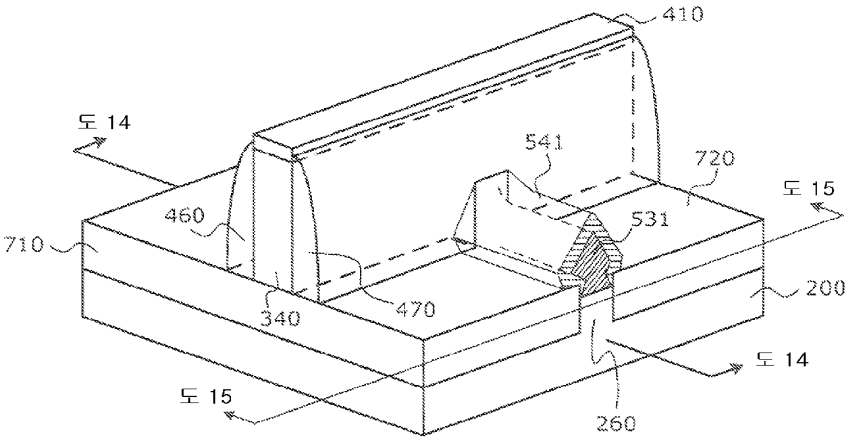
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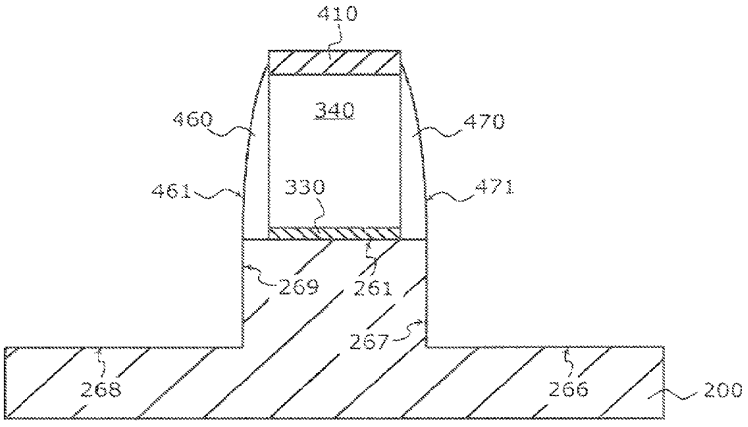
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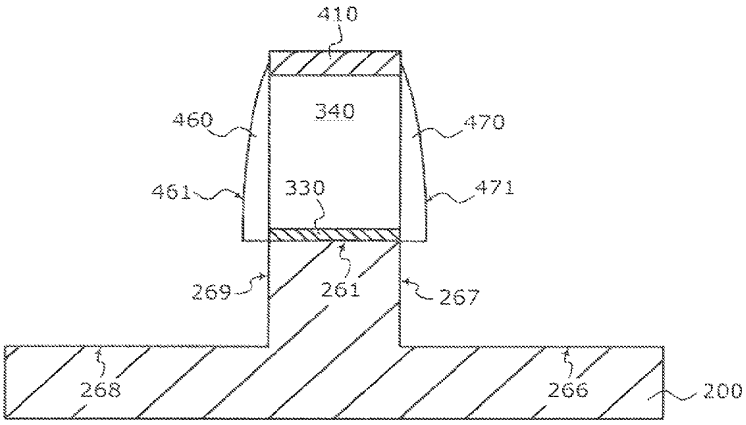
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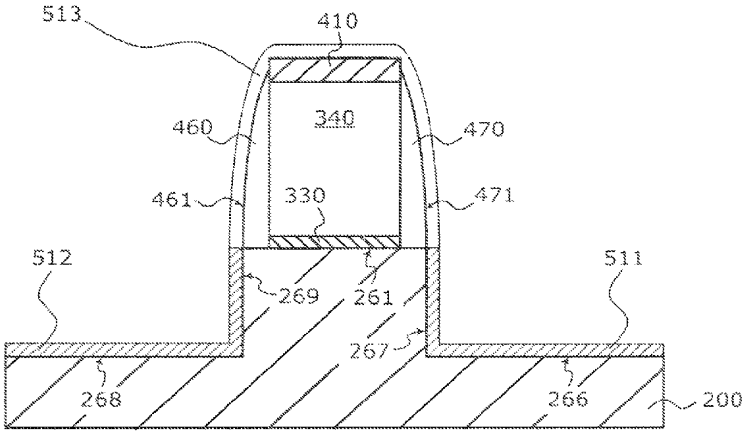
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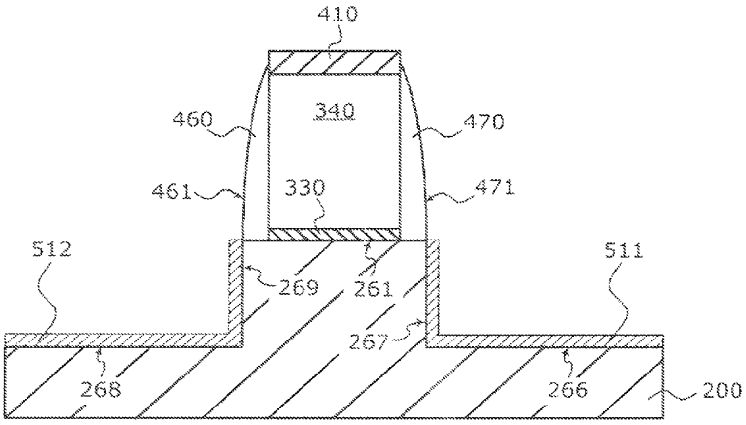
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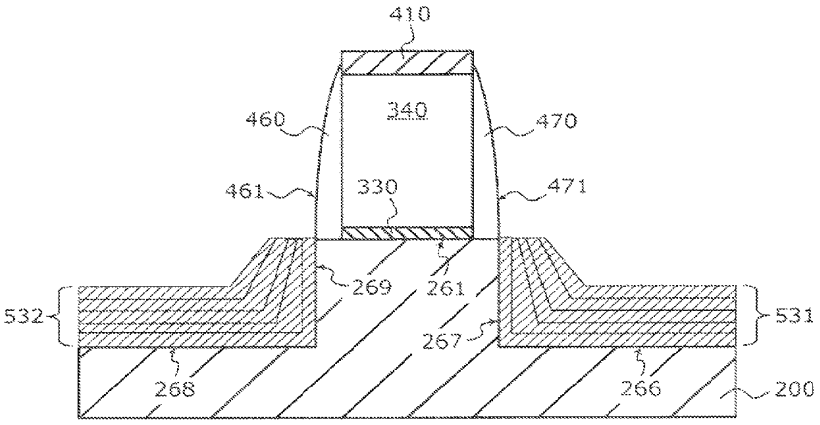


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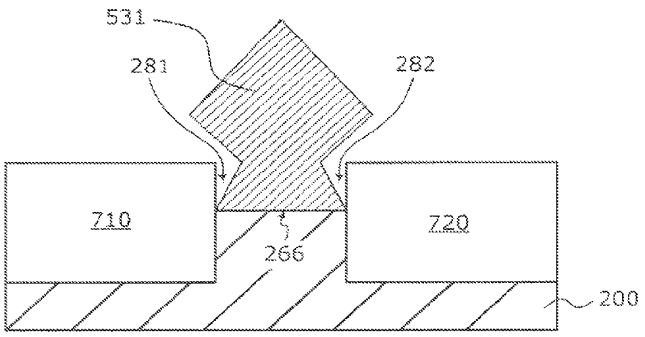


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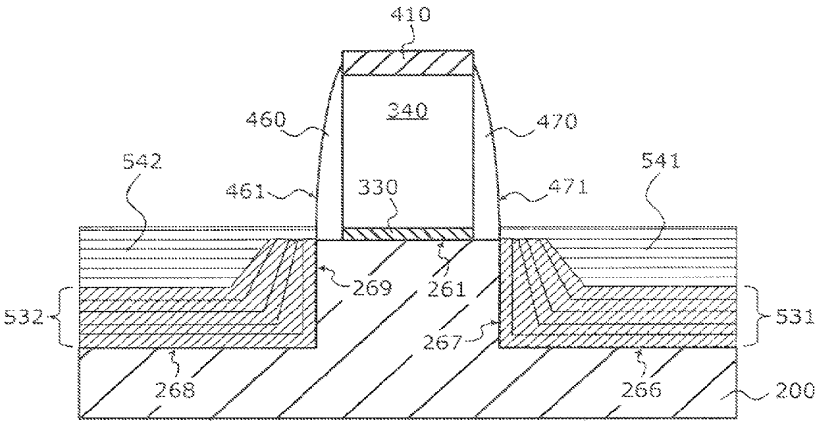
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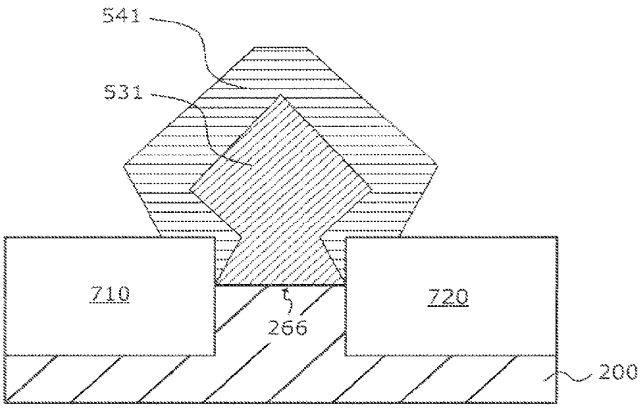
도면13



도면14



도면15



Electronic Acknowledgement Receipt

EFS ID:	29568719
Application Number:	14597115
International Application Number:	
Confirmation Number:	8745
Title of Invention:	Metal-Insensitive Epitaxy Formation
First Named Inventor/Applicant Name:	Chun Hsiung Tsai
Customer Number:	42717
Filer:	Michael Edward Ramon/Jo El Mercer
Filer Authorized By:	Michael Edward Ramon
Attorney Docket Number:	2014-0937/24061.2998
Receipt Date:	21-JUN-2017
Filing Date:	14-JAN-2015
Time Stamp:	17:16:32
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal Letter	24061-2998_SuppIDS-2_Transmittal.pdf	106192 61d8c878be6fc35bf4bab89a31bfac770ba3b091	no	1

Warnings:

Information:					
2	Information Disclosure Statement (IDS) Form (SB08)	24061-2998_SuppIDS-2_1449.pdf	70166 c4dcae959647295904fac178bdb4d18480b7e5aa	no	1
Warnings:					
Information:					
This is not an USPTO supplied IDS fillable form					
3	Foreign Reference	24061-2998_B1-KR20120086369A.pdf	1602979 6f230d6215bfc071ed45bb13d2476ece38f918eb	no	34
Warnings:					
Information:					
			Total Files Size (in bytes):	1779337	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Chun Hsiung Tsai *et al.*	§	Confirmation No.: 8745
Application No. 14/597,115	§	Group Art Unit: 2896
Filed: January 14, 2015	§	Examiner: Spalla, David C.
For: Metal-Insensitive Epitaxy Formation	§	Attorney Docket No. 2014-0937/24061.2998

INFORMATION DISCLOSURE STATEMENT

Via EFS-Web
Commissioner For Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In compliance with the duty of disclosure under 37 CFR §1.56, and in accordance with the practice under 37 CFR §1.97 and §1.98, the Examiner's attention is directed to the documents listed on the enclosed modified Form PTO-1449. No inference should be made that the cited references are in fact material, are in fact prior art, or that no better art exists. The references are not in any order based on their pertinence.

This Information Disclosure Statement is being filed more than three months after the United States filing date and after the mailing date of the first Office Action on the merits, but before the mailing date of any of a Final Action under § 1.113, a Notice of Allowance under § 1.311, or an action that otherwise closes prosecution in the application under §1.311 (37 CFR §1.97(c)).

Accompanying this transmittal is the $180.00 fee set forth in 37 CFR §1.17(p) for submission of an Information Disclosure Statement under §1.97(c). The Commissioner is hereby authorized to charge any additional fees which may be required or credit any overpayment to Deposit Account No. 08-1394.

It is respectfully requested that the above information be considered by the Examiner and that a copy of the enclosed modified Form PTO-1449 be returned indicating that such information has been considered.

Respectfully submitted,

/Michael E. Ramon/

Michael E. Ramon
Registration No. 52,147

Date: June 21, 2017

HAYNES AND BOONE, LLP
IP Section
2323 Victory Avenue, Suite 700
Dallas, Texas 75219
Direct Telephone: 512-867-8426
IP Facsimile: 214-200-0853
ipdocketing@haynesboone.com

CERTIFICATE OF TRANSMISSION

I hereby certify that this correspondence and any attachments are being transmitted via the Electronic Filing System (EFS) Web with the United States Patent and Trademark Office on 6/21/2017.

/Janie Martinez-Holm/
Janie Martinez-Holm

UNITED STATES PATENT AND TRADEMARK OFFICE

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/597,115	01/14/2015	Chun Hsiung Tsai	2014-0937/24061.2998	8745

42717 7590 05/08/2017

HAYNES AND BOONE, LLP
IP Section
2323 Victory Avenue
Suite 700
Dallas, TX 75219

EXAMINER
SPALLA, DAVID C

ART UNIT	PAPER NUMBER
2896	

NOTIFICATION DATE	DELIVERY MODE
05/08/2017	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ipdocketing@haynesboone.com

Office Action Summary	Application No. 14/597,115	Applicant(s) TSAI ET AL.	
	Examiner DAVID SPALLA	Art Unit 2896	AIA (First Inventor to File) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01/05/2017*.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) *1-20 and 27-32* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *1-17,19,20 and 27-32* is/are rejected.

8)☒ Claim(s) *18* is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☒ The drawing(s) filed on *01/14/2015* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a)(1) the claimed invention was patented, described in a printed publication, or in public use, on sale or otherwise available to the public before the effective filing date of the claimed invention.

Claim 1 is rejected under 35 U.S.C. 102(a)(1) as being anticipated by US PG Pub 2010/0093147 to Liao et al. (hereinafter Liao).

Regarding Claim 1, Liao discloses a method of forming a field effect transistor (FET), the method comprising:

performing an etching process to a semiconductor substrate (Fig. 5, substrate 200), thereby forming recesses (216) in source and drain (S/D) regions of the semiconductor substrate;

forming a passivation material layer (220) of a first semiconductor material (SiC; [0021]&[0025]) in the recess; and

epitaxially growing a second semiconductor material (SiGe; **[0023]** "second material is not limited to being similar or different from the first material") on the passivation material layer, thereby forming S/D features in the recesses, wherein the S/D features are separated from the semiconductor substrate by the passivation material layer (Fig. 3), and wherein the first semiconductor material is different than the second semiconductor material (SiC for the first and SiGe for the second).

Claims 1, 7 and 10 are rejected under 35 U.S.C. 102(a)(1) as being anticipated by US PG Pub 2012/0091469 to Park et al. (hereinafter Park).

Regarding Claim 1, Park discloses a method of forming a field effect transistor (FET), the method comprising:

performing an etching process to a semiconductor substrate (Fig. 5, substrate 110), thereby forming recesses (111a,111b) in source and drain (S/D) regions of the semiconductor substrate;

forming a passivation material layer (131) of a first semiconductor material (SiC; [0035]) in the recess; and

epitaxially growing a second semiconductor material (SiGe; [0039]) on the passivation material layer, thereby forming S/D features in the recesses, wherein the S/D features are separated from the semiconductor substrate by the passivation material layer (Fig. 7), and wherein the first semiconductor material is different than the second semiconductor material (SiC for the first and SiGe for the second).

Regarding Claim 7, Park discloses the method of Claim 1, wherein the forming of the passivation material layer includes forming the passivation material layer with a thickness ranging from 1 nm to 4 nm [0035], effectively preventing interaction between chlorine and metal residuals under the passivation material layer.

Regarding Claim 10, Park discloses the method of Claim 1, wherein the epitaxially growing of the second semiconductor material includes epitaxially growing the second semiconductor material with in-situ doping one of a n-type dopant and a p-type dopant ([0066]&[0068]).

Claims 2-6 are rejected under 35 U.S.C. 103 as being unpatentable over Park as applied to Claim 1 above and in view of US PG Pub 2006/0234504 to Bauer et al. (hereinafter Bauer).

Regarding Claim 2, Park discloses the method of Claim 1, wherein the forming of the passivation material layer uses a precursor free of chlorine [0062].

Park does not disclose the use of a non-selective deposition process.

Bauer discloses a method of forming SiC in S.D regions by performing a non-selective deposition process using a precursor free of chlorine [0100].

It would have been obvious to one of ordinary skill in the art, before the invention was made, to have modified the method used by Park to use a non-selective deposition, free of chlorine as a precursor. As noted by Bauer in paragraph [0100], using a non-selective process with precursors such as trisilane and a carbon source would result in a carbon rich layer. Such a layer would have had benefits obvious to one of ordinary skill in the art such as preventing dopants from diffusing into the channel region or otherwise leaking from the S/D features, a desire Park notes in paragraph [0033].

Regarding Claim 3, the combination of Park and Bauer makes obvious the method of Claim 2, wherein the forming of the passivation material layer includes epitaxially growing the passivation material layer of the first semiconductor material (Park, [0035]).

Regarding Claim 4, the combination of Park and Bauer makes obvious the method of Claim 3, wherein the first semiconductor material includes silicon carbide (Park; [0035]) and the second semiconductor material includes silicon germanium (Park; [0039]).

Regarding Claim 5, the combination of Park and Bauer makes obvious the method of Claim 3, wherein the forming of the passivation material layer includes epitaxially growing the passivation material layer of the first semiconductor material that is free of dopant, using the precursor free of dopant-containing gas ([0062]; Park leaves the passivation material layer free of dopants to block the diffusion of dopants from the second semiconductor material [0033]).

Regarding Claim 6, the combination of Park and Bauer makes obvious the method of Claim 3, wherein the forming of the passivation material layer includes forming a silicon carbide layer having a carbon atomic percentage ranging from 1.8% to 3% (Bauer, [0100]; 1-3.5% atomic percentage).

Claims 8 and 9 are rejected under 35 U.S.C. 103 as being unpatentable over Park as applied to Claim 1 above and in view of US PG Pub 2007/0249168 to Rotondaro et al. (hereinafter Rotondaro).

Regarding Claim 8, Park discloses the method of Claim 1 but does not disclose a fluorine treatment.

Rotondaro discloses a method for forming S/D freatures involving a fluorine treatment before growing a semiconductor material [0040].

It would have been obvious to one of ordinary skill in the art, before the invention was made, to have modified the method of Park to include a fluorine treatment step. In the art, it is known that a clean surface is preferential for growing a semiconductor material to avoid defects. While Rotondaro performs the cleaning process on the substrate, the principle would apply to silicon containing layers including the passivation layer of Park. Absent any unexpected results, it would have been obvious to one of general skill in the art to perform a cleaning process before growing additional layers to ensure a defect free source/drain feature.

Regarding Claim 9, the combination of Park and Rotondaro makes obvious the method of Claim 8 but does not disclose the fluorine dose range.

However, absent any unexpected results, it would have been obvious to one of ordinary skill in the art, before the invention was made, so select a range of dosing between 1x10.sup.14 to 2x10.sup.15 ions/cm.sup.2 since it has been held that where the general conditions of a claim are disclosed in the

prior art (ie, fluorine plasma cleaning of silicon surfaces) discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233. Applicant has not noted that the specified range solves any particular problem or is otherwise critical in developing the source/drain features.

Claims 11-14 are rejected under 35 U.S.C. 103 as being unpatentable over Park as applied to Claim 1 above and in further view of US PG Pub 2012/0295427 to Bauer (hereinafter Bauer'427).

Regarding Claim 11, Park discloses the method of Claim 1 but does not disclose the use of a CDE process.

Bauer'437 discloses a process for epitaxially depositing stressor material for a source/drain feature wherein the epitaxially growing of the material includes performing a cyclic deposition and etching (CDE) process [0046].

It would have been obvious to one of ordinary skill in the art, before the invention was made, to have modified the method of Park to comprise a CDE process. As would have been known at the time of the invention, a CDE process allows for a high quality semiconductor layer to be formed by removing poorly formed portions throughout the process. A cyclic deposition process would provide the high quality layers for stressing the channel while also providing the flexibility for adding dopants in subsequent cycles.

Regarding Claim 12, the combination of Park and Bauer'427 makes obvious the method of Claim 11, wherein the CDE process includes a first cycle for deposition and a second cycle for etching; and

the second cycle uses a chlorine-containing gas that includes at least one of HCl and Cl.sub.2 (Bauer'427, [0029]).

Regarding Claim 13, the combination of Park and Bauer'427 makes obvious the method of Claim 12, wherein the first cycle of the CDE process uses a precursor that includes PH.sub.3, monomethylsilane (MMS), and at least one of SiH.sub.4 and Si.sub.2H.sub.6 (Bauer'427, [0039]&[0041]).

Regarding Claim 14, the combination of Park and Bauer'427 makes obvious the method of Claim 12, wherein the first cycle of the CDE process uses a precursor that includes B.sub.2H.sub.6, GeH.sub.4, and at least one of SiH.sub.4 and Si.sub.2H.sub.6 (Bauer'427, [0039]&[0042]),

Claims 15-17 and 19 are rejected under 35 U.S.C. 103 as being unpatentable over US PG Pub 2014/0264636 to Tsai et al. (hereinafter Tsai) in view of US PG Pub 2014/0264348 to Tsai et al. (hereinafter Tsai'348).

The applied reference has a common inventor with the instant application. Based upon the earlier effectively filed date of the reference, it constitutes prior art under 35 U.S.C. 102(a)(2).

This rejection under 35 U.S.C. 103 might be overcome by: (1) a showing under 37 CFR 1.130(a) that the subject matter disclosed in the reference was obtained directly or indirectly from the inventor or a joint inventor of this application and is thus not prior art in accordance with 35 U.S.C.102(b)(2)(A); (2) a showing under 37 CFR 1.130(b) of a prior public disclosure under 35 U.S.C. 102(b)(2)(B); or (3) a statement pursuant to 35 U.S.C. 102(b)(2)(C) establishing that, not later than the effective filing date of the claimed invention, the subject matter disclosed and the claimed invention were either owned by the same person or subject to an obligation of assignment to the same person or subject to a joint research agreement. See generally MPEP § 717.02.

Regarding Claim 15, Tsai discloses a method of forming a field effect transistor (FET), the method comprising:

performing an etching process to a semiconductor substrate (Step 120, Fig. 1), thereby forming recesses in source and drain (S/D) regions of the semiconductor substrate; and

epitaxially growing a semiconductor material by a deposition process with a varying etching/deposition (E/D) factor, thereby forming S/D features in the recesses (Portion 216 of the S/D region is formed using a higher E/D ratio [0064] and SEG process compared to the CDE process for portion 215).

Tsai does not disclose a co-flow epitaxy process.

Tsai'348 discloses a CDE process involving a continuous flow of the etchant during pulses of the deposition precursor [0009].

It would have been obvious to one of ordinary skill in the art, before the invention was made, to have used a co-flow CDE process for the formation of layer 215 in Tsai. By exposing the substrate to a continuous flow of etchant vapor, amorphous portions of the deposited epitaxial layer can be removed, leaving crystalline portions intact and creating a more desirable material for the S/D regions.

Regarding Claim 16, the combination of Tsai and Tsai'348 makes obvious the method of Claim 15, wherein the deposition process incudes a first deposition step having a first etch/deposition (E/D) factor and thereafter a second deposition step having a second E/D factor greater than the first E/D factor (Tsai, [0064], the SEG process uses a higher E/D ratio to reduce particles).

Regarding Claim 17, the combination of Tsai and Tsai'348 makes obvious the method of Claim 16, wherein the first deposition step is a non-selective deposition (Tsai; [0035]); and the second deposition step is a selective deposition (Tsai, [0042]).

Regarding Claim 19, the combination of Tsai and Tsai'348 makes obvious the method of Claim 15, wherein the deposition process includes a combination of the co-flow epitaxy growth and a cyclic deposition and etching (CDE) process as Tsai'348 notes that the etchant has a continuous flow resulting in a co-flowing of deposition and etching precursors during pulses of the silicon based precursor.

Regarding Claim 20, the combination of Tsai and Tsai'348 makes obvious the method of claim 15, wherein the epitaxially growing of the semiconductor material includes varying the E/D factor by a mechanism selected from gas partial pressure, **gas flow rate**, substrate temperature, and a combination thereof (Tsai'348, [0064]).

Claims 27-29, 31 and 32 are rejected under 35 U.S.C. 103 as being unpatentable over Park in view of Rotondaro.

Regarding Claim 27, Park discloses a method of forming a field effect transistor (FET), the method comprising:

performing an etching process to a semiconductor substrate (Fig. 5, substrate 110), thereby forming recesses (111a,111b) in source and drain (S/D) regions of the semiconductor substrate;

forming a passivation material layer (131) of a first semiconductor material (SiC; [0035]) in the recess; and

epitaxially growing a second semiconductor material (SiGe; [0039]) over the passivation material layer, thereby forming S/D features in the recesses, wherein the first semiconductor material is different than the second semiconductor material (SiC for the first and SiGe for the second).

Park does not disclose performing a fluorine treatment to the passivation layer.

Rotondaro discloses a method for forming S/D freatures involving a fluorine treatment before growing a semiconductor material [0040].

It would have been obvious to one of ordinary skill in the art, before the invention was made, to have modified the method of Park to include a fluorine treatment step. In the art, it is known that a clean surface is preferential for growing a semiconductor material to avoid defects. While Rotondaro performs the cleaning process on the substrate, the principle would apply to silicon containing layers including the

passivation layer of Park. Absent any unexpected results, it would have been obvious to one of general skill in the art to perform a cleaning process before growing additional layers to ensure a defect free source/drain feature.

Regarding Claim 28, the combination of Hsiao and Rotondaro makes obvious the method of Claim 27, wherein the fluorine treatment is a fluorine plasma treatment [0042],

Regarding Claim 29, the combination of Hsiao and Rotondaro makes obvious the method of Claim 27 but does not disclose the fluorine dose range.

However, absent any unexpected results, it would have been obvious to one of ordinary skill in the art, before the invention was made, so select a range of dosing between 1 xl 0A14 to 2X10A15 since it has been held that where the general conditions of a claim are disclosed in the prior art (ie, fluorine plasma cleaning of silicon surfaces) discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233. Applicant has not noted that the specified range solves any particular problem or is otherwise critical in developing the source/drain features.

Regarding Claim 31, the combination of Park and Rotondaro makes obvious the method of Claim 27, wherein the forming of the passivation material layer includes epitaxially growing the first semiconductor material that is free of dopant, using the precursor free of dopant-containing gas ([0062]; Park leaves the passivation material layer free of dopants to block the diffusion of dopants from the second semiconductor material [0033]).

Regarding Claim 32, the combination of Park and Rotondaro makes obvious the method of Claim 31, wherein the epitaxially growing of the second semiconductor material includes in-situ doping one of a n-type dopant and a p-type dopant to the second semiconductor material (Park; [0066]&[0068]).

Claim 30 is rejected under 35 U.S.C. 103 as being unpatentable over the combination of Park and Rotondaro as applied to Claim 27 above and in further view of Bauer.

Regarding Claim 30, the combination of Hsiao and Rotondaro makes obvious the method of Claim 27, where the epitaxially growing of the second semiconductor material includes an etching process using a chlorine-containing gas (Park, [0065]) but does not disclose wherein the forming of the passivation layer includes performing a non-selective deposition process using a precursor free of chlorine.

Bauer discloses a method of forming SiC in S/D regions by performing a non-selective deposition process using a precursor free of chlorine [0100].

It would have been obvious to one of ordinary skill in the art, before the invention was made, to have modified the method used by Park to use a non-selective deposition, free of chlorine as a precursor. As noted by Bauer in paragraph [0100], using a non-selective process with precursors such as trisilane and a carbon source would result in a carbon rich layer. Such a layer would have benefits obvious to one of ordinary skill in the art such as preventing dopants from diffusing into the channel region or otherwise leaking from the S/D features.

Response to Arguments

Applicant's arguments with respect to Claims 1, 15 and 27 have been considered but are moot because the arguments do not apply to the current rejection.

Allowable Subject Matter

Claim 18 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 18 discloses the method of Claim 16, wherein the first deposition step has a first substrate temperature less than 620.degree.C; and the second deposition step has a second substrate temperature greater than 620.degree.C. A search of relevant references in the art does not show this to be anticipated or obvious. While it's known in the art that some methods such as the selection of Cl.sub.2 as an etchant can lower the processing temperature (US PG Pub 2006/0115934. [0027]), the references of record do not single out Cl.sub.2 as a preferred chlorine based etchant, nor do they note a temperature differences between CDE steps.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DAVID SPALLA whose telephone number is (303)297-4298. The examiner can normally be reached on Mon-Fri 10am-5pm MST.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Such can be reached on (571) 272-8895. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/D. S./
Examiner, Art Unit 2896

/JEROME JACKSON JR/
Primary Examiner, Art Unit 2815

Notice of References Cited	Application/Control No. 14/597,115	Applicant(s)/Patent Under Reexamination TSAI ET AL.	
	Examiner DAVID SPALLA	Art Unit 2896	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-2010/0093147 A1	04-2010	Liao; Chin-I	H01L21/28123	438/300
*	B	US-2012/0091469 A1	04-2012	Park; Keum-Seok	H01L29/0847	257/77
*	C	US-2006/0234504 A1	10-2006	Bauer; Matthias	C23C16/04	438/674
*	D	US-2012/0295427 A1	11-2012	Bauer; Matthias	H01L21/02532	438/494
*	E	US-2007/0249168 A1	10-2007	Rotondaro; Antonio Luis Pacheco	H01L21/30608	438/700
*	F	US-2014/0264348 A1	09-2014	Tsai; Chun Hsiung	C30B25/165	257/57
*	G	US-2014/0264636 A1	09-2014	Tsai; Chun Hsiung	H01L29/66636	257/408
	H	US-				
	I	US-				
	J	US-				
	K	US-				
	L	US-				
	M	US-				

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L6	4698	H01L29/66636.cpc.	US-PGPUB; USPAT; USOCR	OR	ON	2017/04/30 18:23
L7	11016021	@ad<"20140822" @rlad<"20140822" @pt1d<"20140822"	US-PGPUB; USPAT; USOCR	OR	ON	2017/04/30 18:23
L8	1111	(((silicon adj carbide) SiC) with (buffer passivation)) and ((silicon adj germanium) SiGe)	US-PGPUB; USPAT; USOCR	OR	ON	2017/04/30 18:24
L9	24	6 and 7 and 8	US-PGPUB; USPAT; USOCR	OR	ON	2017/04/30 18:24
L13	2	"20060234504"	US-PGPUB; USPAT; USOCR	OR	ON	2017/04/30 18:54
L14	15	(US-20030136985-$ or US-20150236157-$ or US-20130049101-$ or US-20080315254-$ or US-20140197455-$ or US-20140246710-$ or US-20140264348-$ or US-20060234504-$ or US-20120295427-$ or US-20090104739-$ or US-20060115933-$ or US-20070249168-$ or US-20100093147-$).did. or (US-8785285-$ or US-9064892-$).did.	US-PGPUB; USPAT	OR	ON	2017/04/30 19:01
L15	1	14 and (co-flow)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	ON	2017/04/30 19:01
L16	3	6 and 7 and (varying adj2 etching)	US-PGPUB; USPAT; USOCR	OR	ON	2017/04/30 19:42
L17	4	6 and 7 and ((SiC (silicon adj2 carbide)) same co-flow)	US-PGPUB; USPAT; USOCR	OR	ON	2017/04/30 19:47
L18	11	((SiC (silicon adj2 carbide)) same co-flow)	US-PGPUB; USPAT; USOCR	OR	ON	2017/04/30 19:48
L19	10	7 and 18	US-	OR	ON	2017/04/30

			PGPUB; USPAT; USOCR			19:49
L20	2	(("etching/deposition" "E/D") adj2 factor)	US-PGPUB; USPAT; USOCR	OR	ON	2017/04/30 19:50
L21	92	(varying increasing decreasing) with ((cyclic adj2 deposition) CDE)	US-PGPUB; USPAT; USOCR	OR	ON	2017/04/30 19:51
L22	77	7 and 21	US-PGPUB; USPAT; USOCR	OR	ON	2017/04/30 19:51
L23	0	7 and 21 and co-flow	US-PGPUB; USPAT; USOCR	OR	ON	2017/04/30 19:52
L24	189	(("etching/deposition" "E/D") adj2 ratio)	US-PGPUB; USPAT; USOCR	OR	ON	2017/04/30 19:53
L25	0	7 and 24 and co-flow	US-PGPUB; USPAT; USOCR	OR	ON	2017/04/30 19:55
L26	0	7 and 24 and "co-flow"	US-PGPUB; USPAT; USOCR	OR	ON	2017/04/30 19:55
L27	9	7 and ((cyclic adj2 deposition) CDE) and "co-flow"	US-PGPUB; USPAT; USOCR	OR	ON	2017/04/30 19:55
L28	11	((cyclic adj2 deposition) CDE) and "co-flow"	US-PGPUB; USPAT; USOCR	OR	ON	2017/04/30 19:58
L29	220	((etching with deposition) "E/D") adj2 (factor ratio)	US-PGPUB; USPAT; USOCR	OR	ON	2017/04/30 19:59
L30	0	7 and 29 and co-flow	US-PGPUB; USPAT; USOCR	OR	ON	2017/04/30 20:00
L31	214	7 and 29	US-PGPUB; USPAT; USOCR	OR	ON	2017/04/30 20:00
L32	12	((etching with deposition) "E/D") adj2 (factor ratio) same (CL HCL "CL.sub.2" CL2)	US-PGPUB; USPAT; USOCR	OR	ON	2017/04/30 20:01
L33	11	7 and 32	US-PGPUB; USPAT; USOCR	OR	ON	2017/04/30 20:01

L34	46	7 and ((cyclic adj2 deposition) CDE) with continuous	US-PGPUB; USPAT; USOCR	OR	ON	2017/04/30 20:15
L35	68	7 and (((cyclic adj2 deposition) CDE) with constant)	US-PGPUB; USPAT; USOCR	OR	ON	2017/04/30 20:17
L36	109	(34 35)	US-PGPUB; USPAT; USOCR	OR	ON	2017/04/30 20:37
S2	10680640	@ad<"20140822" @rlad<"20140822" @pt1d<"20140822"	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/13 10:07
S3	0	"14813556"	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/13 10:46
S4	1	"14597115"	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/13 13:33
S7	10680640	@ad<"20140822" @rlad<"20140822" @pt1d<"20140822"	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/13 13:36
S9	15	("7667271" | "8362575" | "8367498" | "8440517" | "8497528" | "8610240" | "8680576" | "8723272" | "8729634" | "8785285" | "8796759" | "8809139" | "8828823" | "8836016" | "8841701").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/13 13:41
S10	24	("20030052406" | "20060057859" | "20070059875" | "20070111439" | "20070128782" | "20070131969" | "20070145487" | "20080044960" | "20080251851" | "20090239344" | "20090280612" | "20100252816" | "20110147828" | "20120068193" | "20120104470" | "3909304" | "7112848" | "7132338" | "7518196" | "7910415" | "8110486" | "8338259").PN. OR ("8785285").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/13 13:44
S12	9538	fluorine adj3 (plasma treatment)	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/13 13:53
S14	10680640	@ad<"20140822" @rlad<"20140822" @pt1d<"20140822"	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/13 14:05
S15	4124	H01L29/66636.cpc.	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/13 14:05
S16	1731	S14 and S15 and ((silicon adj carbide) SiC) and ((silicon adj germanium) SiGe)	US-PGPUB; USPAT;	OR	ON	2016/06/13 14:05

			USOCR			
S17	31	S16 and (fluorine adj3 (plasma treat$4 clean$3))	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/13 14:12
S18	700	S14 and S15 and ((silicon adj carbide) SiC) and ((second upper) with ((silicon adj germanium) SiGe))	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/13 14:23
S19	260	S18 and (treat$3 clean$3)	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/13 14:27
S20	10686366	@ad<"20140822" @rlad<"20140822" @pt1d<"20140822"	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/15 15:31
S21	4131	H01L29/66636.cpc.	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/15 15:31
S22	103	S20 and S21 and (non-selective)	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/15 15:31
S23	2	S20 and S21 and ((non-selective) same precursor same (SiC (silicon adj2 carbide)))	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/15 15:39
S24	94	H01L29/66636.cpc. and (SiC same dop$3 same (prevent block$3 barrier diffusion))	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/17 17:53
S25	10690365	@ad<"20140822" @rlad<"20140822" @pt1d<"20140822"	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/17 18:16
S26	4134	H01L29/66636.cpc.	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/17 18:16
S27	5	S25 and S26 and ((non-selective) same cycle)	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/17 18:16
S28	9	S25 and S26 and ((non-selective) same (cyclic cycle))	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/17 18:18
S29	120	S25 and S26 and ((cyclic cycle) same (vary$3 chang$3 alter$3 rate factor))	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/17 18:19
S30	44	S25 and S26 and (((cyclic cycle) adj3 deposit$3) same (vary$3 chang$3 alter$3 rate factor))	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/17 18:20
S31	24	S25 and S26 and (((cyclic cycle) adj3	US-	OR	ON	2016/06/17

		deposit$3) same (vary$3 chang$3 alter$3 rate factor)) and (degree celsius)	PGPUB; USPAT; USOCR			18:24
S32	0	S25 and S26 and (((cyclic cycle) adj3 deposit$3) same (vary$3 chang$3 alter$3 rate factor)) and ".degree."	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/17 18:30
S33	24	S25 and S26 and (((cyclic cycle) adj3 deposit$3) same (vary$3 chang$3 alter$3 rate factor)) and degree	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/17 18:31
S34	40	S25 and S26 and (((cyclic cycle) adj3 deposit$3) same (vary$3 chang$3 alter$3 rate factor)) and $4degree	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/17 18:31
S35	2	"20060234504"	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/21 15:48
S36	2	"20130328126"	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/21 15:55
S37	10698055	@ad<"20140822" @rlad<"20140822" @pt1d<"20140822"	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/23 16:27
S38	2137	S37 and (((cyclic cycle) adj3 deposit$3) same (vary$3 chang$3 alter$3 rate factor))	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/23 16:27
S39	3183	S37 and ((((cyclic cycle) adj3 deposit$3) CDE) same (vary$3 chang$3 alter$3 rate factor))	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/23 16:28
S40	661	S37 and ((((cyclic cycle) adj3 deposit$3) CDE) same (vary$3 chang$3 alter$3 rate factor)) and ((((cyclic cycle) adj3 deposit$3) CDE) same $4degree)	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/23 16:29
S42	335	S37 and ((((cyclic cycle) adj3 deposit$3) CDE) same (vary$3 chang$3 alter$3 rate factor)) and ((((cyclic cycle) adj3 deposit$3) CDE) same $4degree) and ((source drain source/drain s/d) with (deposit$3 epitax$5))	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/23 16:32
S43	9	S37 and (((cyclic cycle) adj3 deposit$3) CDE) with (non-selective (non adj selective)) with selective	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/23 16:51
S45	18	S37 and ((((cyclic cycle) adj3 deposit$3) CDE) same (non-selective (non adj selective)) same selective)	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/23 16:52
S46	98695	S37 and ((fluorine fluoride) with (treat$4 clean$3 process))	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/23 17:18
S47	4157	H01L29/66636.cpc.	US-PGPUB;	OR	ON	2016/06/23 17:19

			USPAT; USOCR			
S48	258	S37 and ((fluorine fluoride) with (treat$4 clean$3 process)) and S47	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/23 17:19
S49	86	S37 and ((fluorine fluoride) with (treat$4 clean$3 process) with plasma) and S47	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/23 17:20
S50	14	(US-20030136985-$ or US-20150236157-$ or US-20130049101-$ or US-20080315254-$ or US-20140197455-$ or US-20140246710-$ or US-20140264348-$ or US-20060234504-$ or US-20120295427-$ or US-20090104739-$ or US-20060115933-$ or US-20070249168-$).did. or (US-8785285-$ or US-9064892-$).did.	US-PGPUB; USPAT	OR	ON	2016/06/23 17:34
S51	95	S37 and ((fluorine fluoride) with (treat$4 clean$3 process) with plasma) and H01L29/7848.cpc.	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/23 17:34
S52	73	S37 and ((((cyclic cycle) adj3 deposit$3) CDE) same (vary$3 chang$3 alter$3 rate factor)) and ((((cyclic cycle) adj3 deposit$3) CDE) same $4degree) and ((source drain source/drain s/d) with (deposit$3 epitax$5)) and "cl.sub.2"	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/23 18:21
S53	58	S37 and ((((cyclic cycle) adj3 deposit$3) CDE) same (vary$3 chang$3 alter$3 rate factor)) and ((((cyclic cycle) adj3 deposit$3) CDE) same $4degree) and ((source drain source/drain s/d) with (deposit$3 epitax$5)) and ("cl.sub.2" same temperature)	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/23 18:23

EAST Search History (Interference)

<This search history is empty>

4/30/2017 8:59:54 PM
C:\Users\dspalla\Documents\EAST\Workspaces\14597115.wsp

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14597115	TSAI ET AL.
	Examiner	Art Unit
	DAVID SPALLA	2896

CPC- SEARCHED		
Symbol	Date	Examiner
H01L 29/66636, 7848	06/23/2016	DCS

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
45			

SEARCH NOTES		
Search Notes	Date	Examiner
Search of submitted IDS references	06/23/2016	DCS
See attached EAST search history	06/23/2016	DCS
See attached EAST updated search history	04/30/2017	DCS

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

/DAVID SPALLA/ Examiner.Art Unit 2896	

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of: Chun Hsiung Tsai *et al.*	§	Docket No.: 2014-0937/24061.2998
Application No. 14/597,115	§	Art Unit: 2896
Filing Date: January 14, 2015	§	Examiner: Spalla, David C.
Entitled: METAL-INSENSITIVE EPITAXY FORMATION	§	Confirmation No.: 8745

Mail Stop: Amendment
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE TO OFFICE ACTION DATED JULY 8, 2016

Applicants respectfully submit this paper in response to the Office Action mailed on July 8, 2016, setting a period for reply to expire on October 8, 2016. A petition for a three-month extension of time is attached, extending the period for reply to January 8, 2017. Entry of the following amendments and comments into the record of the above-identified application is respectfully requested.

Any fees required by this paper are being provided as directed in an electronic submission of this paper or in a transmittal letter accompanying this paper. However, the Commissioner is hereby authorized to charge any deficiency in fees required by this paper and any additional fees under 37 C.F.R. § 1.16 or 1.17 which may be required during the pendency of this application, and to similarly credit any overpayment, to Haynes and Boone, LLP's Deposit Account 08-1394.

Amendments to the Claims are reflected in the listing of claims which begins on page **2** of this paper.

Remarks/Arguments begin on page **6** of this paper.

Listing of Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (***Currently Amended***) A method of forming a field effect transistor (FET), the method comprising:

performing an etching process to a semiconductor substrate, thereby forming recesses in source and drain (S/D) regions of the semiconductor substrate;

forming a passivation material layer of a first semiconductor material in the recesses; and

epitaxially growing a second semiconductor material on the passivation material layer, thereby forming S/D features in the recesses, wherein the S/D features are separated from the semiconductor substrate by the passivation material layer, and wherein the first semiconductor material is different than the second semiconductor material.

2. (Original) The method of claim 1, wherein the forming of the passivation material layer includes performing a non-selective deposition process using a precursor free of chlorine.

3. (***Currently Amended***) The method of claim 2, wherein the forming of the passivation material layer includes epitaxially growing the passivation material layer of the first semiconductor material~~, the first semiconductor material being different from the second semiconductor material~~.

4. (Original) The method of claim 3, wherein the first semiconductor material includes silicon carbide and the second semiconductor material includes silicon germanium.

5. (***Currently Amended***) The method of claim 3, wherein the forming of the passivation material layer includes epitaxially growing the passivation material layer of the first semiconductor material that is free of dopant, using the precursor free of dopant-containing gas.

6. (Previously Presented) The method of claim 3, wherein the forming of the passivation material layer includes forming a silicon carbide layer having a carbon atomic percentage ranging from 1.8% to 3%.

7. (Previously Presented) The method of claim 1, wherein the forming of the passivation material layer includes forming the passivation material layer with a thickness ranging from 1 nm to 4 nm, effectively preventing interaction between chlorine and metal residuals under the passivation material layer.

8. (Original) The method of claim 1, further comprising performing a fluorine treatment to the passivation material layer before the epitaxially growing of the second semiconductor material.

9. (Previously Presented) The method of claim 8, wherein the performing of the fluorine treatment includes performing the fluorine treatment with a fluorine dose ranging from 1×10^{14} ions/cm^2 to 2×10^{15} ions/cm^2.

10. (Original) The method of claim 1, wherein the epitaxially growing of the second semiconductor material includes epitaxially growing the second semiconductor material with in-situ doping one of a n-type dopant and a p-type dopant.

11. (Original) The method of claim 1, wherein the epitaxially growing of the second semiconductor material includes performing a cyclic deposition and etching (CDE) process.

12. (Original) The method of claim 11, wherein

the CDE process includes a first cycle for deposition and a second cycle for etching; and

the second cycle uses a chlorine-containing gas that includes at least one of HCl and Cl_2.

13. (Original) The method of claim 12, wherein the first cycle of the CDE process uses a precursor that includes PH_3, monomethylsilane (MMS), and at least one of SiH_4 and Si_2H_6.

14. (Original) The method of claim 12, wherein the first cycle of the CDE process uses a precursor that includes B_2H_6, GeH_4, and at least one of SiH_4 and Si_2H_6.

15. (***Currently Amended***) A method of forming a field effect transistor (FET), the method comprising:

performing an etching process to a semiconductor substrate, thereby forming recesses in source and drain (S/D) regions of the semiconductor substrate; and

epitaxially growing a semiconductor material by a deposition process with a varying etching/deposition (E/D) factor, thereby forming S/D features in the recesses, wherein the deposition process includes a co-flow epitaxy growth.

16. (Original) The method of claim 15, wherein the deposition process incudes a first deposition step having a first etch/deposition (E/D) factor and thereafter a second deposition step having a second E/D factor greater than the first E/D factor.

17. (***Currently Amended***) The method of claim [[15]] 16, wherein

the first deposition step is a non-selective deposition; and

the second deposition step is a selective deposition.

18. (***Currently Amended***) The method of claim [[15]] 16, wherein

the first deposition step has a first substrate temperature less than 620 ^{0}C; and

the second deposition step has a second substrate temperature greater than 620 ^{0}C.

19. (***Currently Amended***) The method of claim 15, wherein the deposition process includes [[one]]a combination of the co-flow epitaxy growth and a cyclic deposition and etching (CDE) process~~; a co-flow epitaxy growth; and a combination thereof~~.

20. (Original) The method of claim 15, wherein the epitaxially growing of the semiconductor material includes varying the E/D factor by a mechanism selected from gas partial pressure, gas flow rate, substrate temperature, and a combination thereof.

21-26. (Canceled)

27. (***Currently Amended***) A method of forming a field effect transistor (FET), the method comprising:

performing an etching process to a semiconductor substrate, thereby forming recesses in source and drain (S/D) regions of the semiconductor substrate;

forming a passivation layer of a first semiconductor material in the recesses;

performing a fluorine treatment to the passivation layer; and

epitaxially growing a second semiconductor material over the passivation layer, thereby forming S/D features in the recesses, wherein the first semiconductor material is different than the second semiconductor material.

28. (Previously Presented) The method of claim 27, wherein the fluorine treatment is a fluorine plasma treatment.

29. (Previously Presented) The method of claim 27, wherein the fluorine treatment uses a fluorine dose ranging from 1×10^{14} ions/cm^2 to 2×10^{15} ions/cm^2.

30. (Previously Presented) The method of claim 27, wherein the forming of the passivation layer includes performing a non-selective deposition process using a precursor free of chlorine; and the epitaxially growing of the second semiconductor material includes an etching process using a chlorine-containing gas.

31. (Previously Presented) The method of claim 27, wherein the forming of the passivation layer includes epitaxially growing the first semiconductor material that is free of dopant, using a precursor free of dopant-containing gas.

32. (Previously Presented) The method of claim 31, wherein the epitaxially growing of the second semiconductor material includes in-situ doping one of a n-type dopant and a p-type dopant to the second semiconductor material.

REMARKS

Claims 1-20 and 27-32 were previously pending, of which claims 1, 3, 5, 15, 17-19, and 27 were amended. Reconsideration of presently pending claims 1-20 and 27-32 is respectfully requested in light of the above amendments and the following remarks.

Allowable Subject Matter

Claim 18 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all the limitations of the base claim and any intervening claims, and if the corrections required for the removal of the rejection under 112 are met. With this paper, Applicants provide an amendment to claim 18 to address the Office's concerns with respect to the rejection under 112. Further, in view of the deficiencies of the cited references, as discussed below, Applicants believe it would be premature to rewrite claim 18 in independent form, as suggested by the Office. Applicant also respectfully notes that claim 18 depends on and further limits claim 15 and is allowable for at least the reasons set forth in connection with independent claim 15.

Rejections under 35 U.S.C. § 112

Claims 17 and 18 were rejected under 35 U.S.C. §112(b) or 35 U.S.C. §112 (pre-AIA), second paragraph, as being indefinite for failing to point out and distinctly claim the subject matter which the inventor or a joint inventor, or for pre-AIA the applicant regards as the invention. With this paper, Applicants provide amendments to make claims 17 and 18 dependent on claim 16, thereby providing antecedent basis for the limitations "the first deposition step" and "the second deposition step".

Thus, Applicants respectfully request that the rejection of claims 17 and 18 under 35 U.S.C. §112 be withdrawn.

Rejections Under 35 U.S.C. § 102(a)(1)

Claims 1 and 10 were rejected under 35 U.S.C. §102(a)(1) as being anticipated by Hsiao et al (U.S. Patent Application Publication No. 2013/0049101, hereinafter referred to as "Hsiao"). Claims 1 and 7 were rejected under 35 U.S.C. §102(a)(1) as being anticipated by Fukuda et al

(U.S. Patent Application Publication No. 2008/0315254, hereinafter referred to as "Fukuda"). With respect to the claims as herein amended, Applicants respectfully traverse these rejections.

Independent Claim 1

Amended claim 1 recites:

"A method of forming a field effect transistor (FET), the method comprising:

performing an etching process to a semiconductor substrate, thereby forming recesses in source and drain (S/D) regions of the semiconductor substrate;

forming a passivation material layer of a first semiconductor material in the recesses; and

epitaxially growing a second semiconductor material on the passivation material layer, thereby forming S/D features in the recesses, wherein the S/D features are separated from the semiconductor substrate by the passivation material layer, and wherein the first semiconductor material is different than the second semiconductor material."

The amendment to claim 1 finds support at least at paragraphs [0036] and [0042] of the present application. In the rejection of claim 1, the Examiner relies on Hsiao's lower film portion 26 and intermediate film portion 30 as allegedly disclosing the claimed "passivation material layer" and "second semiconductor material", respectively. OA at page 3. Amended claim 1 requires "forming a passivation material layer of a first semiconductor material in the recesses; and epitaxially growing a second semiconductor material on the passivation material layer…wherein the first semiconductor material is different than the second semiconductor material." Hsiao at paragraph [0013] states that "Intermediate film portion 30 may be formed of *the same stressor material*, i.e., SiGe, as lower film portion 26 but intermediate film portion 30 will additionally include the first dopant impurity therein." (Emphasis added). Thus, even assuming *arguendo* the Office's interpretation of Hsiao's lower film portion 26 and intermediate film portion 30, Hsiao does not teach or suggest "forming a passivation material layer of a first semiconductor material in the recesses; and epitaxially growing a second semiconductor material on the passivation material layer…wherein the first semiconductor material is different than the

second semiconductor material", as positively recited in Applicants' amended claim 1. Thus, the Office has not shown how the relied upon portion of Hsiao discloses the Applicants' claimed method.

Therefore, the rejection of claim 1 is not supported by the Hsiao reference and should be withdrawn.

Additionally, in the rejection of claim 1, the Examiner relies on Fukuda's lower layer portion 7a and upper layer portion 7b as allegedly disclosing the claimed "passivation material layer" and "second semiconductor material", respectively. OA at page 4. With reference to Fukuda's FIG. 7 'sequence d' (reproduced below, annotated) and related paragraph [0045], Fukuda teaches that the lower layer portion 7a and the upper layer portion 7b are both SiGe, thus *the lower layer portion 7a and the upper layer portion 7b are the same semiconductor material*. At best, Fukuda teaches a SiGe layer where the lower layer portion 7a has a thickness 'X' and a first HCl gas content, and the upper layer portion 7b has a thickness 'Y-X' and a second HCl gas content. Thus, even assuming *arguendo* the Office's interpretation of Fukuda's lower layer portion 7a and upper layer portion 7b, Fukuda does not teach or suggest "forming a passivation material layer of a first semiconductor material in the recesses; and epitaxially growing a second semiconductor material on the passivation material layer…wherein the first semiconductor material is different than the second semiconductor material", as positively recited in Applicants' amended claim 1. Thus, the Office has not shown how the relied upon portion of Fukuda discloses the Applicants' claimed method.

Therefore, the rejection of claim 1 is not supported by the Fukuda reference and should be withdrawn.

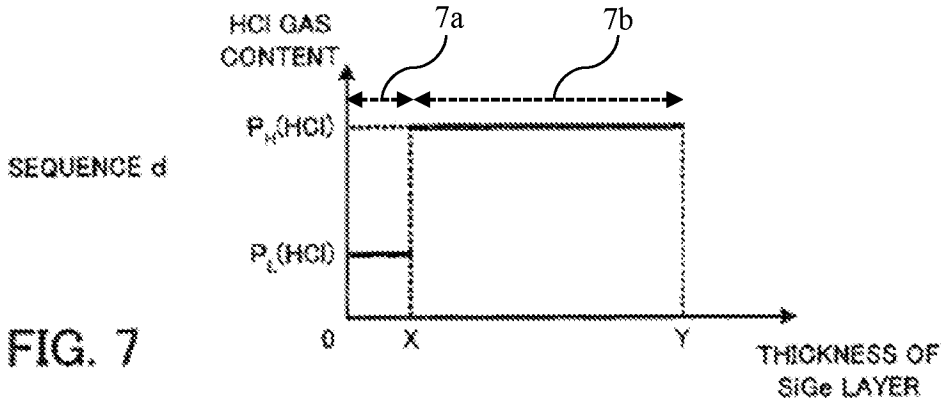


FIG. 7

Dependent Claims 2-14

Claims 2-14 depend on and further limit independent claim 1 and therefore are deemed to be patentable over the prior art, for at least the same reasons set forth above in connection with independent claim 1. Accordingly, the rejection of claims 2-14 should be withdrawn. Claim 3 was amended to correct a typographical error and in view of the amendment to claim 1. Claim 5 was amended merely to correct a typographical error.

Rejections Under 35 U.S.C. §103

Claims 2-6 were rejected under 35 U.S.C. §103 as being unpatentable over Hsiao as applied to claim 1, and in further view of Bauer et al. (U.S. Patent Application Publication No. 2006/0234504, hereinafter referred to as "Bauer"). Claims 11-16, 19, and 20 were rejected under 35 U.S.C. §103 as being unpatentable over Hsiao as applied to claim 1, and in further view of Bauer (U.S. Patent Application Publication No. 2012/0295427, hereinafter referred to as "Bauer '427"). To be sure, it appears that the rejections of claims 15, 16, 19, and 20 are presented as 102 anticipation rejections in view of Bauer '427 (OA at page 7). Claims 27-29, 31, and 32 were rejected under 35 U.S.C. §103 as being unpatentable over Hsiao in view of Rotondaro et al. (U.S. Patent Application Publication No. 2007/0249168, hereinafter referred to as "Rotondaro"). Claim 30 was rejected as being unpatentable over the combination of Hsiao and Rotondaro as applied to claim 27, and in further view of Bauer and Bauer '427. Claims 8 and 9 were rejected under 35 U.S.C. §103 as being unpatentable over Hsiao as applied to claim 1, and in further view of Rotondaro. Claim 17 was rejected under 35 U.S.C. §103 as being unpatentable over Bauer '427 as applied to claim 16, and in further view of Tsai et al. (U.S. Patent Application Publication No. 2014/0264348, hereinafter referred to as "Tsai").

With respect to the claims as herein amended, Applicants respectfully traverse these rejections on the grounds that the references are defective in establishing a *prima facie* case of obviousness.

Dependent Claims 2-6, 8, and 9

As noted above, claims 2-6, 8, and 9 depend on and further limit independent claim 1 and therefore are deemed to be patentable over the prior art, for at least the same reasons set forth above in connection with independent claim 1. Accordingly, the rejection of claims 2-6, 8, and 9 should be withdrawn.

For avoidance of doubt, the Bauer reference is relied on for disclosure of a Si-containing epitaxial layer 30 (e.g., SiC) grown in S/D regions 20. In particular, the Examiner relies on Bauer's SiC layer as allegedly disclosing the claimed "passivation material layer". OA at pages 5-6, Bauer paragraph [0100]. At page 5 of the present Action, the Office argues that it would have been obvious to combine the method of Bauer with Hsiao because "using a non-selective process with precursors such as trisilane and a carbon source would result in a *carbon rich layer*." (Emphasis added). It is noted that Bauer's Si-containing epitaxial layer 30 (e.g., SiC) is intended to exert strain on the channel region 22 (Bauer, paragraph [0067]). In fact, paragraph [0103] of Bauer states the "the SiC layer is selectively formed in recessed source/drain regions 20, and is preferably deposited under conditions (thickness, temperature) *that maintain stress*." (Emphasis added). On the contrary, Applicants' passivation layer is not used for, or intended to be used for, inducing strain. For instance, Applicants' paragraph [0037] states "The SiC layer with such low carbon concentration is *not suitable for strain effect* but is more effective as the passivation layer for isolating and preventing diffusion." (Emphasis added).

In addition, using Bauer's strain-exerting SiC layer with Hsiao's three portion stressor film (e.g., lower film portion 26, intermediate film portion 30, and upper film portion 34) could change or destroy the functionality of Hsiao's stressor film. As one example, Hsiao's lower film portion 26 is intended to be "completely void of any other dopant impurities" (Hsiao, paragraph [0012]), while Bauer's SiC layer is taught as being formed with dopant source gases such as "arsine, phosphine or diborane" (Bauer, paragraphs [0067]-[0068]). Thus, the composition of Hsiao's lower film portion 26 could be unintentionally altered. Furthermore, as both Hsiao's stressor film and Bauer's SiC layer are intended to exert strain (e.g., on a channel), the stress-inducing efficacy of each film is likely to be altered upon interaction with one another.

Therefore, even if the teachings of Bauer are exactly as the Office suggests, which Applicants do not admit, Bauer and Hsiao do not teach or suggest the limitations of Applicants' claims 2-6, for at least the same reasons set forth above in connection with claim 1.

In addition, and for avoidance of doubt, the Rotondaro reference is relied upon merely for a teaching of performing a fluorine treatment. Thus, even if the teachings of Rotondaro are exactly as the Office suggests, which Applicants do not admit, Hsiao and Rotondaro do not teach or suggest the limitations of Applicants' claims 8 and 9.

Dependent Claims 11-14

As noted above, claims 11-14 depend on and further limit independent claim 1 and therefore are deemed to be patentable over the prior art, for at least the same reasons set forth above in connection with independent claim 1.

Independent Claim 15

MPEP 2143.03 states that "[a]ll words in a claim must be considered in judging the patentability of that claim against the prior art." Quoting *In re Wilson*, 424 F.2d 1382, 1385 (CCPA 1970).

Amended claim 15 recites, in part, "wherein the deposition process includes a co-flow epitaxy growth". The amendment to claim 15 finds support at least at paragraphs [0050], [0051], [0073], [0078], [0080], [0081], and [0083]-[0087] of the specification. While claims 15, 16, 19, and 20 were rejected under 35 U.S.C. §103 as being unpatentable over Hsiao as applied to claim 1, and in further view of Bauer '427 (OA at page 6), it appears that the rejections of claims 15, 16, 19, and 20 are presented as 102 anticipation rejections in view of Bauer '427 (OA at page 7). In particular, in the rejection of claim 15, the Examiner apparently relies on Bauer '427's recesses 114 of FIG. 2A as allegedly disclosing the claimed "recesses", and Bauer '427's process shown in FIGS. 2B-2F as allegedly disclosing the claimed "deposition process with a varying etching/deposition (E/D) factor". OA at page 7. Amended claim 15 requires "wherein the deposition process includes a co-flow epitaxy growth." At best, Bauer '427 discloses a cyclic deposition and etching (CDE) process, for example, at paragraph [0046] and FIG. 1. Therefore, even if the teachings of Bauer '427 are exactly as the Office suggests, which Applicants do not admit, Hsiao and Bauer '427 do not teach or suggest "wherein the deposition process includes a co-flow epitaxy growth", as positively recited in Applicants' amended claim 15.

Accordingly, independent claim 15 is allowable, and notice to that effect is respectfully requested.

TSMC Exhibit 1065
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Dependent Claims 16, 17, 19, and 20

Claims 16, 17, 19, and 20 depend on and further limit independent claim 15 and therefore are deemed to be patentable over the prior art, for at least the same reasons set forth above in connection with independent claim 15. Accordingly, the rejection of claims 16, 17, 19, and 20 should be withdrawn. Claims 17 was amended to address the Office's concerns with respect to the rejection under 112. Claim 19 was amended in view of the amendment to independent claim 15.

Independent Claim 27

Amended claim 27 recites, in part, "wherein the first semiconductor material is different than the second semiconductor material". The amendment to claim 27 finds support at least at paragraphs [0036] and [0042] of the present application. The rationale offered in the Office Action for the rejection of this claim is effectively the same rationale that is offered for the rejection of independent claim 1. Therefore, for reasons similar to those discussed above in association with independent claim 1, it is respectfully submitted that Hsiao and Rotondaro do not teach or suggest the limitations of Applicants' claim 27. For avoidance of doubt, the Rotondaro reference is relied upon merely for a teaching of performing a fluorine treatment. Thus, even if the teachings of Rotondaro are exactly as the Office suggests, which Applicants do not admit, Hsiao and Rotondaro do not teach or suggest "wherein the first semiconductor material is different than the second semiconductor material", as positively recited in Applicants' amended claim 27.

Accordingly, independent claim 27 is allowable, and notice to that effect is respectfully requested.

Dependent Claims 28-32

Claims 28-32 depend on and further limit claim 27 and therefore are deemed to be patentable over the prior art, for at least the same reasons set forth above in connection with independent claim 27. Accordingly, the rejection of claims 28-32 should be withdrawn.

Conclusion

An early formal notice of allowance of claims 1-20 and 27-32 is requested. A personal or telephonic interview is respectfully requested to discuss any remaining issues in an effort to expedite the allowance of this application.

Respectfully submitted,

/Michael E. Ramon/

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1/5/2017

/Janie Martinez-Holm/
Janie Martinez-Holm

Electronic Patent Application Fee Transmittal

Application Number:	14597115
Filing Date:	14-Jan-2015
Title of Invention:	Metal-Insensitive Epitaxy Formation
First Named Inventor/Applicant Name:	Chun Hsiung Tsai
Filer:	Michael Edward Ramon/Janie Martinez-Holm
Attorney Docket Number:	2014-0937/24061.2998

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension - 3 months with $0 paid	1253	1	1400	1400
Miscellaneous:				
			Total in USD ($)	**1400**

Electronic Acknowledgement Receipt

EFS ID:	27985287
Application Number:	14597115
International Application Number:	
Confirmation Number:	8745
Title of Invention:	Metal-Insensitive Epitaxy Formation
First Named Inventor/Applicant Name:	Chun Hsiung Tsai
Customer Number:	42717
Filer:	Michael Edward Ramon/Janie Martinez-Holm
Filer Authorized By:	Michael Edward Ramon
Attorney Docket Number:	2014-0937/24061.2998
Receipt Date:	05-JAN-2017
Filing Date:	14-JAN-2015
Time Stamp:	17:51:10
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$1400
RAM confirmation Number	010617INTEFSW17542300
Deposit Account	
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Extension of Time	24061-2998_EOT_3mo.pdf	188722 5f5cdaaaa73995db393b7dfaf4942fa93825e030	no	2
Warnings:					
Information:					
2		24061-2998_Response_07-08-16_1st_OA.pdf	183786 05b970c114d45b8d32f9bc3304335ecd88ae6b5a	yes	13

Multipart Description/PDF files in .zip description

Document Description	Start	End
Amendment/Req. Reconsideration-After Non-Final Reject	1	1
Claims	2	5
Applicant Arguments/Remarks Made in an Amendment	6	13

Warnings:					
Information:					
3	Fee Worksheet (SB06)	fee-info.pdf	30254 605d83f79d458d6831820b4305460b9039a07b49	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	402762		

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/22 (03-13)
Approved for use through 3/31/2013. OMB 0651-0031
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PETITION FOR EXTENSION OF TIME UNDER 37 CFR 1.136(a)

Docket Number (Optional): 2014-0937/24061.2998

Application Number	Filed
14/597,115	01-14-2015

For: Metal-Insensitive Epitaxy Formation

Art Unit	Examiner
2896	SPALLA, DAVID C

This is a request under the provisions of 37 CFR 1.136(a) to extend the period for filing a reply in the above-identified application.

The requested extension and fee are as follows (check time period desired and enter the appropriate fee below):

	Fee	Small Entity Fee	Micro Entity Fee	
☐ One month (37 CFR 1.17(a)(1))	$200	$100	$50	$
☐ Two months (37 CFR 1.17(a)(2))	$600	$300	$150	$
☑ Three months (37 CFR 1.17(a)(3))	$1,400	$700	$350	$ 1400.00
☐ Four months (37 CFR 1.17(a)(4))	$2,200	$1,100	$550	$
☐ Five months (37 CFR 1.17(a)(5))	$3,000	$1,500	$750	$

☐ Applicant asserts small entity status. See 37 CFR 1.27.

☐ Applicant certifies micro entity status. See 37 CFR 1.29.
Form PTO/SB/15A or B or equivalent must either be enclosed or have been submitted previously.

☐ A check in the amount of the fee is enclosed.

☐ Payment by credit card. Form PTO-2038 is attached.

☐ The Director has already been authorized to charge fees in this application to a Deposit Account.

☑ The Director is hereby authorized to charge any fees which may be required, or credit any overpayment, to Deposit Account Number 08-1394.

☑ Payment made via EFS-Web.

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

I am the

☐ applicant/inventor.

☐ assignee of record of the entire interest. See 37 CFR 3.71. 37 CFR 3.73(b) statement is enclosed (Form PTO/SB/96).

☑ attorney or agent of record. Registration number 52,147.

☐ attorney or agent acting under 37 CFR 1.34. Registration number _____.

/Michael E. Ramon/ — Signature

January 5, 2017 — Date

Michael E. Ramon — Typed or printed name

512-867-8426 — Telephone Number

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. Submit multiple forms if more than one signature is required, see below*.

☑ * Total of 1 forms are submitted.

This collection of information is required by 37 CFR 1.136(a). The information is required to obtain or retain a benefit by the public, which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 6 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 14/597,115	Filing Date 01/14/2015	☐ To be Mailed

ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT	01/05/2017	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 26	Minus	** 26	= 0	X $80 =	0
	Independent (37 CFR 1.16(h))	* 3	Minus	***3	= 0	X $420 =	0
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	0

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
TONI HAKIM

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/597,115	01/14/2015	Chun Hsiung Tsai	2014-0937/24061.2998	8745

42717 7590 07/08/2016

HAYNES AND BOONE, LLP
IP Section
2323 Victory Avenue
Suite 700
Dallas, TX 75219

EXAMINER	
SPALLA, DAVID C	

ART UNIT	PAPER NUMBER
2896	

NOTIFICATION DATE	DELIVERY MODE
07/08/2016	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ipdocketing@haynesboone.com

Office Action Summary	Application No. 14/597,115	Applicant(s) TSAI ET AL.	
	Examiner DAVID SPALLA	Art Unit 2896	AIA (First Inventor to File) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03/14/2016*.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) *1-20 and 27-32* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *1-17,19,20 and 27-32* is/are rejected.

8)☒ Claim(s) *18* is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☒ The drawing(s) filed on *01/14/2015* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☒ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

DETAILED ACTION

Election/Restrictions

Applicant's election without traverse of Invention I in the reply filed on 03/14/2016 is acknowledged.

Claims 21-26 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 03/14/2016.

Information Disclosure Statement

The information disclosure statement (IDS) submitted on 01/14/2015 and 06/01/2015 are in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Claim Rejections - 35 USC § 112

> The following is a quotation of 35 U.S.C. 112(b):
> (b) CONCLUSION.—The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the inventor or a joint inventor regards as the invention.
>
> The following is a quotation of 35 U.S.C. 112 (pre-AIA), second paragraph:
> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 17 and 18 are rejected under 35 U.S.C. 112(b) or 35 U.S.C. 112 (pre-AIA), second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the inventor or a joint inventor, or for pre-AIA the applicant regards as the invention.

Claims 17 and 18 recite the limitations "first deposition step" and "second deposition steps". There is insufficient antecedent basis for this limitation in the claim since Claim 15 makes no mention of a first and second deposition step. For purposes of examination, these claims are being treated as dependents of Claim 16. Correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a)(1) the claimed invention was patented, described in a printed publication, or in public use, on sale or otherwise available to the public before the effective filing date of the claimed invention.

Claims 1 and 10 are rejected under 35 U.S.C. 102(a)(1) as being anticipated by US PG Pub 2013/0049101 to HSIAO et al. (hereinafter Hsiao).

Regarding Claim 1, Hsiao discloses a method of forming a field effect transistor (FET), the method comprising:

performing an etching process to a semiconductor substrate (Fig. 1, substrate 2), thereby forming recesses (14) in source and drain (S/D) regions of the semiconductor substrate;

forming a passivation material layer (26) of a first semiconductor in the recesses; and

epitaxially growing a second semiconductor material (30; [0013]), thereby forming S/D features in the recesses, wherein the S/D features are separated from the semiconductor substrate by the passivation material layer (Fig. 3).

Regarding Claim 10, Hsiao discloses the method of Claim 1, wherein the epitaxially growing of the second semiconductor material includes epitaxially growing the second semiconductor material with in- situ doping one of a n-type dopant and a p-type dopant [0013].

Claims 1 and 7 are rejected under 35 U.S.C. 102(a)(1) as being anticipated by US PG Pub 2008/0315254 to Fukuda et al. (hereinafter Fukuda).

Regarding Claim 1, Fukuda discloses a method of forming a field effect transistor (FET), the method comprising:

performing an etching process to a semiconductor substrate (Fig. 4, substrate 1), thereby forming recesses (6) in source and drain (S/D) regions of the semiconductor substrate;

forming a passivation material layer (7a) of a first semiconductor in the recesses; and

epitaxially growing a second semiconductor material (7b, [0034]), thereby forming S/D features in the recesses, wherein the S/D features are separated from the semiconductor substrate by the passivation material layer (Fig. 6).

Regarding Claim 7, Fukuda discloses the method of Claim 1, wherein the forming of the passivation material layer includes forming the passivation material layer with a thickness ranging from 1nm to 4nm, effectively preventing interaction between chlorine and metal residuals under the passivation material layer [0037].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103 which forms the basis for all obviousness rejections set forth in this Office action:

> A patent for a claimed invention may not be obtained, notwithstanding that the claimed invention is not identically disclosed as set forth in section 102 of this title, if the differences between the claimed invention and the prior art are such that the claimed invention as a whole would have been obvious before the effective filing date of the claimed invention to a person having ordinary skill in the art to which the claimed invention pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims are rejected under 35 U.S.C. 103 as being unpatentable over Hsiao as applied to Claim 1 above and in further view of US PG Pub 2006/0234504 to Bauer et al. (hereinafter Bauer).

Regarding Claim 2, Hsiao discloses the method of Claim 1 but does not explicitly disclose the precursors used.

Bauer discloses a method of forming SiC in S/D regions by performing a non-selective deposition process using a precursor free of chlorine [0100].

It would have been obvious to one of ordinary skill in the art, before the invention was made, to have modified the method used by Hsiao to use a non-selective deposition, free of chlorine as a precursor. As noted by Bauer in paragraph [0100], using a non-selective process with precursors such as trisilane and a carbon source would result in a carbon rich layer. Such a layer would have benefits obvious to one of ordinary skill in the art such as preventing dopants from diffusing into the channel region or otherwise leaking from the S/D features.

Regarding Claim 3, the combination of Hsiao and Bauer makes obvious the method of Claim 2, wherein the forming of the passivation material layer includes epitaxially growing the passivation layer of the first semiconductor material, the first semiconductor material being different from the second semiconductor material substrate (the first semiconductor material is SiC and the second is SiGe).

Regarding Claim 4, the combination of Hsiao and Bauer makes obvious the method of Claim 3, wherein the first semiconductor material includes silicon carbide and the second semiconductor material includes silicon germanium (Hsiao; [0012]-[0013]).

Regarding Claim 5, the combination of Hsiao and Bauer makes obvious the method of claim 3, wherein the forming of the passivation material layer includes epitaxially growing the passivation layer of the first semiconductor material that is free of dopant, using the precursor free of dopant-containing gas (Hsiao; [0012]).

Regarding Claim 6, the combination of Hsiao and Bauer makes obvious the method of Claim 3, wherein the forming of the passivation material layer includes forming a silicon carbide layer having a carbon atomic percentage ranging from 1.8% to 3% (Bauer, [0100]; 1-3.5% atomic %).

Claims 11-16, 19 and 20 are rejected under 35 U.S.C. 103 as being unpatentable over Hsiao as applied to Claim 1 above and in further view of US PG Pub 2012/0295427 to Bauer (hereinafter Bauer '427).

Regarding Claim 11, Hsiao discloses the method of Claim 1 but does not disclose the use of a CDE process.

Bauer '427 discloses a process for epitaxially depositing stressor material for a source/drain feature wherein the epitaxially growing of the material includes performing a cyclic deposition and etching (CDE) process [0046].

It would have been obvious to one of ordinary skill in the art, before the invention was made, to have modified the method of Hsiao to comprise a CDE process. As would have been known at the time of the invention, a CDE process allows for a high quality semiconductor layer to be formed by removing poorly formed portions throughout the process. A cyclic deposition process would provide the high quality layers for stressing the channel while also providing the flexibility for adding dopants in subsequent cycles.

Regarding Claim 12, the combination of Hsiao and Bauer '427 makes obvious the method of Claim 11, wherein the CDE process includes a first cycle for deposition and a second cycle for etching; and

the second cycle uses a chlorine-containing gas that includes at least one of HCl and Cl_2 [0029].

Regarding Claim 13, the combination of Hsiao and Bauer '427 makes obvious the method of Claim 12, wherein the first cycle of the CDE process uses a precursor that includes PH_3, monomethylsilane (MMS), and at least one of SiH4 and Si_2H_6 [0039]&[0041].

Regarding Claim 14, the combination of Hsiao and Bauer '427 makes obvious the method of Claim 12, wherein the first cycle of the CDE process uses a precursor that includes B_2H_6, GeH_4, and at least one of SiH_4 and Si_2H_6 [0039]&[0042].

Regarding Claim 15, Bauer '427 discloses a method of forming a field effect transistor (FET), the method comprising:

performing an etching process to a semiconductor substrate (Fig. 2A), thereby forming recesses in source and drain (S/D) regions of the semiconductor substrate; and

epitaxially growing a semiconductor material by a deposition process with a varying etching/deposition (E/D) factor, thereby forming S/D features in the recesses (Figs. 2B-2F; [0045]).

Regarding Claim 16, Bauer '427 discloses the method of Claim 15, wherein the deposition process incudes a first deposition step having a first etch/deposition (E/D) factor and thereafter a second deposition step having a second E/D factor greater than the first E/D factor [0036] (carrier gas flow rate is varied to achieve higher etch rates for subsequent CDE steps).

Regarding Claim 19, Bauer '427 discloses the method of Claim 15, wherein the deposition process includes one of a **cyclic deposition and etching (CDE) process**; a co-flow epitaxy growth; and a combination thereof.

Regarding Claim 20, Bauer '427 discloses the method of claim 15, wherein the epitaxially growing of the semiconductor material includes varying the E/D factor by a mechanism selected from gas partial pressure, **gas flow rate**, substrate temperature, and a combination thereof [0036].

Claims 27-29, 31 and 32 are rejected under 35 U.S.C. 103 as being unpatentable over Hsiao in view of US PG Pub 2007/0249168 to Rotondaro et al. (hereinafter Rotondaro).

Regarding Claim 27, Hsiao discloses a method of forming a field effect transistor (FET), the method comprising:

performing an etching process to a semiconductor substrate (Fig. 1), thereby forming recesses in source and drain (S/D) regions of the semiconductor substrate;

forming a passivation layer (26, Fig. 1) of a first semiconductor material in the recesses; and

epitaxially growing a second semiconductor material (30, Fig. 2) over the passivation layer, thereby forming S/D features in the recesses.

Hsiao does not disclose performing a fluorine treatment to the passivation layer.

Rotondaro discloses a method for forming S/D freatures involving a fluorine treatment before growing a semiconductor material [0040].

It would have been obvious to one of ordinary skill in the art, before the invention was made, to have modified the method of Hsiao to include a fluorine treatment step. In the art, it is known that a clean surface is preferential for growing a semiconductor material to avoid defects. While Rotondaro performs the cleaning process on the substrate, the principle would apply to silicon containing layers including the passivation layer of Hsiao. Absent any unexpected results, it would have been obvious to one of general skill in the art to perform a cleaning process before growing additional layers to ensure a defect free source/drain feature.

Regarding Claim 28, the combination of Hsiao and Rotondaro makes obvious the method of Claim 27, wherein the fluorine treatment is a fluorine plasma treatment [0042].

Regarding Claim 29, the combination of Hsiao and Rotondaro makes obvious the method of Claim 27 but does not disclose the fluorine dose range.

However, absent any unexpected results, it would have been obvious to one of ordinary skill in the art, before the invention was made, so select a range of dosing between 1x10^14 to 2X10^15 since it has been held that where the general conditions of a claim are disclosed in the prior art (ie, fluorine plasma cleaning of silicon surfaces) discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233. Applicant has not noted that the specified range solves any particular problem or is otherwise critical in developing the source/drain features.

Regarding Claim 31, the combination of Hsiao and Rotondaro makes obvious the method of Claim 27, wherein the forming of the passivation layer includes epitaxially growing the first semiconductor material that is free of dopant, using a precursor free of dopant-containing gas (Hsiao, [0012]).

Regarding Claim 32, the combination of Hsiao and Rotondaro makes obvious the method of Claim 31, wherein the epitaxially growing of the second semiconductor material includes in-situ doping one of a n-type dopant and a p-type dopant to the second semiconductor material (Hsiao, [0013]).

Claim 30 is rejected under 35 U.S.C. 103 as being unpatentable over the combination of Hsiao and Rotondaro as applied to Claim 27 above and in further view of Bauer and Bauer '427.

Regarding Claim 30, the combination of Hsiao and Rotondaro makes obvious the method of Claim 27, but does not disclose (1) wherein the forming of the passivation layer includes performing a non-selective deposition process using a precursor free of chlorine; and (2) the epitaxially growing of the second semiconductor material includes an etching process using a chlorine-containing gas.

With regards to (1), Bauer discloses a method of forming SiC in S/D regions by performing a non-selective deposition process using a precursor free of chlorine [0100].

It would have been obvious to one of ordinary skill in the art, before the invention was made, to have modified the method used by Hsiao to use a non-selective deposition, free of chlorine as a precursor. As noted by Bauer in paragraph [0100], using a non-selective process with precursors such as trisilane and a carbon source would result in a carbon rich layer. Such a layer would have benefits obvious to one of ordinary skill in the art such as preventing dopants from diffusing into the channel region or otherwise leaking from the S/D features.

With regards to (2), Bauer '427 discloses a method of growing SiGe [0042] using a chlorine based etchant [0043].

It would have been obvious to one of ordinary skill in the art, before the invention was made, to have modified the method used by Hsiao to use a chlorine based etchant on the second semiconductor material. As noted above, the precursors lacking chlorine are used to make a carbon rich layer. As the SiGe layer of Hsiao lacks carbon, more common methods may be used. HCl and CL.sub.2 are commonly used in the art as they can selective remove silicon containing layers.

Claims 8 and 9 are rejected under 35 U.S.C. 103 as being unpatentable over Hsiao as applied to Claim 1 above and in view of Rotondaro.

Regarding Claim 8, Hsiao discloses the method of Claim 1 but does not disclose a fluorine treatment.

Rotondaro discloses a method for forming S/D freatures involving a fluorine treatment before growing a semiconductor material [0040].

It would have been obvious to one of ordinary skill in the art, before the invention was made, to have modified the method of Hsiao to include a fluorine treatment step. In the art, it is known that a clean surface is preferential for growing a semiconductor material to avoid defects. While Rotondaro performs

the cleaning process on the substrate, the principle would apply to silicon containing layers including the passivation layer of Hsiao. Absent any unexpected results, it would have been obvious to one of general skill in the art to perform a cleaning process before growing additional layers to ensure a defect free source/drain feature.

Regarding Claim 9, the combination of Hsiao and Rotondaro makes obvious the method of Claim 8 but does not disclose the fluorine dose range.

However, absent any unexpected results, it would have been obvious to one of ordinary skill in the art, before the invention was made, so select a range of dosing between 1x10^14 to 2X10^15 since it has been held that where the general conditions of a claim are disclosed in the prior art (ie, fluorine plasma cleaning of silicon surfaces) discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233. Applicant has not noted that the specified range solves any particular problem or is otherwise critical in developing the source/drain features.

Claim 17 is rejected under 35 U.S.C. 103 as being unpatentable over Bauer '427 as applied to Claim 16 above and in further view of US PG Pub 2014/0264348 to Tsai et al. (hereinafter Tsai).

Regarding Claim 17, Bauer '427 discloses the method of Claim 16 but does not explicitly disclose the first deposition step to be non-selective and the second to be selective.

Lee discloses a method of forming source/drain features which includes a CDE method of growing the semiconductor material wherein the first deposition includes a non-selective method and the second [0030].

It would have been obvious to one of ordinary skill in the art, before the invention was made, to have modified the method of forming the stressor material to include both non-selective and selective deposition. Bauer '427 discloses the process for a blanket deposition (non-selective), Example 1, and a process for selective deposition, Example 3. Using a combination of these methods would have been

obvious so as to form high-quality layers at the boundary with the channel and then to fill the source/drain features quickly with faster deposition techniques.

Allowable Subject Matter

Claim 18 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims and if the corrections required for the removal of the rejection under 112 are met.

Claim 18 discloses the method of Claim 16, wherein the first deposition step has a first substrate temperature less than 620 ℃; and the second deposition step has a second substrate temperature greater than 620 ℃. A search of relevant references in the art does not show this to be anticipated or obvious. While it's known in the art that some methods such as the selection of Cl.sub.2 as an etchant can lower the processing temperature (US PG Pub 2006/0115934. [0027]), the references of record do not single out Cl.sub.2 as a preferred chlorine based etchant, nor do they note a temperature differences between CDE steps.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DAVID SPALLA whose telephone number is (303)297-4298. The examiner can normally be reached on Mon-Fri 10am-5pm MST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Such can be reached on (571) 272-8895. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/D. S./
Examiner, Art Unit 2896

/JEROME JACKSON JR/

Primary Examiner, Art Unit 2815

Notice of References Cited	Application/Control No. 14/597,115	Applicant(s)/Patent Under Reexamination TSAI ET AL.	
	Examiner DAVID SPALLA	Art Unit 2896	Page 1 of 1

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*	B	US-2008/0315254 A1	12-2008	Fukuda; Masahiro	H01L21/02532	257/190
*	C	US-2014/0197455 A1	07-2014	LEE; Wei-Yang	H01L29/78	257/192
*	D	US-2006/0234504 A1	10-2006	Bauer; Matthias	C23C16/04	438/674
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*	F	US-2007/0249168 A1	10-2007	Rotondaro; Antonio Luis Pacheco	H01L21/30608	438/700
	G	US-				
	H	US-				
	I	US-				
	J	US-				
	K	US-				
	L	US-				
	M	US-				

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	N					
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	S					
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NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
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	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
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CONFIRMATION NO. 8745

SERIAL NUMBER	FILING or 371(c) DATE RULE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
14/597,115	01/14/2015	257	2896	2014-0937/24061.2998

APPLICANTS
Taiwan Semiconductor Manufacturing Company, Ltd., Hsin-Chu, TAIWAN;

INVENTORS
Chun Hsiung Tsai, Hsinchu County, TAIWAN;
Yuan-Ko Hwang, Hsinchu City, TAIWAN;

DCS

**** CONTINUING DATA ***************************
This appln claims benefit of 62/040,880 08/22/2014

DCS

**** FOREIGN APPLICATIONS ***************************
NONE

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**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ****
01/29/2015

Foreign Priority claimed ☐ Yes ☑ No 35 USC 119(a-d) conditions met ☐ Yes ☑ No Verified and Acknowledged /DAVID C SPALLA/ Examiner's Signature	☐ Met after Allowance Initials	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
		TAIWAN	23	26	3

ADDRESS
HAYNES AND BOONE, LLP
IP Section
2323 Victory Avenue
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Dallas, TX 75219
UNITED STATES

TITLE
Metal-Insensitive Epitaxy Formation

FILING FEE RECEIVED		
2080	FEES: Authority has been given in Paper No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

In place of PTO-1449 Form	U. S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE			Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(use as many sheets as necessary)*				Application Number	TBD
				Filing Date	Herewith
				First Inventor Name	Chun Hsiung Tsai
				Art Unit	TBD
				Examiner Name	TBD
SHEET	1	OF	1	Attorney Docket Number	2014-0937/24061.2998

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Examiner's Initials	Cite No.	Document Number	Issue Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document
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		8,367,498	02/05/2013	Chang et al.
		8,440,517	05/14/2013	Lin et al.
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		8,610,240	12/17/2013	Lee et al.
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		8,723,272	05/13/2014	Liu et al.
		8,729,627	05/20/2014	Cheng et al.
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		8,853,025	10/07/2014	Zhang et al.

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Examiner's Initials	Cite No.	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document
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		2013/0011983	01/10/2013	Tsai Ji-Yin et al.
		2013/0328126	12/12/2013	Tsai et al.
		2014/0252412	09/11/2014	Tsai Chun Hsiang et al.

FOREIGN PATENT DOCUMENTS					
Examiner's Initials	Cite No.	Foreign Patent Document (Country Code – Number – Kind)	Publication Date MM-DD-YYYY	Patentee or Applicant of Cited Document	Translation Y/N

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Examiner's Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article, title of the item, date, page(s), volume-issue number(s), publisher, city/country where published

Examiner Signature	/David Spalla/	Date Considered	06/13/2016

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EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L9	10698055	@ad<"20140822" @rlad<"20140822" @pt1d<"20140822"	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/23 16:27
L10	2137	L9 and (((cyclic cycle) adj3 deposit$3) same (vary$3 chang$3 alter$3 rate factor))	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/23 16:27
L11	3183	L9 and ((((cyclic cycle) adj3 deposit$3) CDE) same (vary$3 chang$3 alter$3 rate factor))	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/23 16:28
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L15	9	L9 and (((cyclic cycle) adj3 deposit$3) CDE) with (non-selective (non adj selective)) with selective	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/23 16:51
L17	18	L9 and ((((cyclic cycle) adj3 deposit$3) CDE) same (non-selective (non adj selective)) same selective)	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/23 16:52
L18	98695	L9 and ((fluorine fluoride) with (treat$4 clean$3 process))	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/23 17:18
L19	4157	H01L29/66636.cpc.	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/23 17:19
L20	258	L9 and ((fluorine fluoride) with (treat$4 clean$3 process)) and L19	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/23 17:19
L21	86	L9 and ((fluorine fluoride) with (treat$4 clean$3 process) with plasma) and L19	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/23 17:20
L23	14	(US-20030136985-$ or US-20150236157-$ or US-20130049101-$ or US-20080315254-$ or US-20140197455-$ or	US-PGPUB; USPAT	OR	ON	2016/06/23 17:34

		US-20140246710-$ or US-20140264348-$ or US-20060234504-$ or US-20120295427-$ or US-20090104739-$ or US-20060115933-$ or US-20070249168-$).did. or (US-8785285-$ or US-9064892-$).did.				
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S4	1	"14597115"	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/13 13:33
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S10	24	("20030052406" | "20060057859" | "20070059875" | "20070111439" | "20070128782" | "20070131969" | "20070145487" | "20080044960" | "20080251851" | "20090239344" | "20090280612" | "20100252816" | "20110147828" | "20120068193" | "20120104470" | "3909304" | "7112848" | "7132338" | "7518196" | "7910415" | "8110486" | "8338259").PN. OR ("8785285").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/13 13:44
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S16	1731	S14 and S15 and ((silicon adj carbide) SiC) and ((silicon adj germanium) SiGe)	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/13 14:05
S17	31	S16 and (fluorine adj3 (plasma treat$4 clean$3))	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/13 14:12
S18	700	S14 and S15 and ((silicon adj carbide) SiC) and ((second upper) with ((silicon adj germanium) SiGe))	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/13 14:23
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S21	4131	H01L29/66636.cpc.	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/15 15:31
S22	103	S20 and S21 and (non-selective)	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/15 15:31
S23	2	S20 and S21 and ((non-selective) same precursor same (SiC (silicon adj2 carbide)))	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/15 15:39
S24	94	H01L29/66636.cpc. and (SiC same dop$3 same (prevent block$3 barrier diffusion))	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/17 17:53
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S26	4134	H01L29/66636.cpc.	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/17 18:16
S27	5	S25 and S26 and ((non-selective) same cycle)	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/17 18:16

S28	9	S25 and S26 and ((non-selective) same (cyclic cycle))	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/17 18:18
S29	120	S25 and S26 and ((cyclic cycle) same (vary$3 chang$3 alter$3 rate factor))	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/17 18:19
S30	44	S25 and S26 and (((cyclic cycle) adj3 deposit$3) same (vary$3 chang$3 alter$3 rate factor))	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/17 18:20
S31	24	S25 and S26 and (((cyclic cycle) adj3 deposit$3) same (vary$3 chang$3 alter$3 rate factor)) and (degree celsius)	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/17 18:24
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S34	40	S25 and S26 and (((cyclic cycle) adj3 deposit$3) same (vary$3 chang$3 alter$3 rate factor)) and $4degree	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/17 18:31
S35	2	"20060234504"	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/21 15:48
S36	2	"20130328126"	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/21 15:55

EAST Search History (Interference)

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Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14597115	TSAI ET AL.
	Examiner	Art Unit
	DAVID SPALLA	2896

CPC- SEARCHED		
Symbol	Date	Examiner
H01L 29/66636, 7848	06/23/2016	DCS

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES		
Search Notes	Date	Examiner
Search of submitted IDS references	06/23/2016	DCS
See attached EAST search history	06/23/2016	DCS

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

/DAVID SPALLA/ Examiner.Art Unit 2896	

In place of PTO-1449 Form	U. S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE			Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(use as many sheets as necessary)*				Application Number	14/597,115
				Filing Date	January 14, 2015
				First Inventor Name	Chun Hsiung Tsai et al.
				Art Unit	2811
				Examiner Name	unknown
SHEET	1	OF	1	Attorney Docket Number	2014-0937/24061.2998

U. S. PATENTS

Examiner's Initials	Cite No.	Document Number	Issue Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document

U. S. PATENT APPLICATION PUBLICATIONS

Examiner's Initials	Cite No.	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document

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NON-PATENT LITERATURE DOCUMENTS

Examiner's Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article, title of the item, date, page(s), volume-issue number(s), publisher, city/country where published
	A1	Y. BOGUMILOWICZ *et al.*, "Chemical vapour etching of Si, SiGe and Ge with HC1; applications to the formation of thin relaxed SiGe buffers and to the revelation of threading dislocations," Institute of Physics Publishing, December 17, 2004, pages 127-134, Semicond. Sci. Technol. 20 (2005), France.
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	A3	V. DESTEFANIS *et al.*, Low-thermal surface preparation, HC1 etch and Si/SiGe selective epitaxy on (1 1 0) silicon surfaces," Semiconductor Science and Technology, September 16, 2008, pages 9, Semicond. Sci. Technol. 23 (2008), France.
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Examiner Signature	/David Spalla/	Date Considered	06/13/2016

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include a copy of this form with next communication to applicant.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /D.S/
TSMC Exhibit 1065
Page 245 of 351

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of: Chun Hsiung Tsai *et al.*	§	Docket No.: 2014-0937/24061.2998
Application No. 14/597,115	§	Art Unit: 2896
Filing Date: January 14, 2015	§	Examiner: Spalla, David C.
Entitled: Metal-Insensitive Epitaxy Formation	§	Confirmation No.: 8745

RESPONSE TO RESTRICTION REQUIREMENT

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Alexandria, VA 22313-1450

Dear Commissioner:

The present paper is being submitted in response to the Restriction Requirement - Office Action mailed January 12, 2016.

No fees are expected due at this time. However, if any fees, including extension of time fees are necessary, the extension of time is hereby requested, and the Commissioner is hereby authorized to charge any fees, including those for the extension of time, to Haynes and Boone, LLP's Deposit Account No. 08-1394.

Listing of Claims begins on page **2** of this paper.
Remarks/Arguments begin on page **6** of this paper.

Listing of Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Original) A method of forming a field effect transistor (FET), the method comprising:

performing an etching process to a semiconductor substrate, thereby forming recesses in source and drain (S/D) regions of the semiconductor substrate;

forming a passivation material layer of a first semiconductor in the recesses; and

epitaxially growing a second semiconductor material, thereby forming S/D features in the recesses, wherein the S/D features are separated from the semiconductor substrate by the passivation material layer.

2. (Original) The method of claim 1, wherein the forming of the passivation material layer includes performing a non-selective deposition process using a precursor free of chlorine.

3. (Currently amended) The method of claim 2, wherein the forming of the passivation material layer includes epitaxially growing the passivation layer of the first semiconductor material, the first semiconductor material being different from the second semiconductor material ~~substrate~~.

4. (Original) The method of claim 3, wherein the first semiconductor material includes silicon carbide and the second semiconductor material includes silicon germanium.

5. (Original) The method of claim 3, wherein the forming of the passivation material layer includes epitaxially growing the passivation layer of the first semiconductor material that is free of dopant, using the precursor free of dopant-containing gas.

6. (Currently amended) The method of claim 3, wherein the forming of the passivation material layer includes forming a silicon carbide layer having a carbon atomic percentage ranging from ~~about~~ 1.8% to ~~about~~ 3%.

7. (Currently amended) The method of claim 1, wherein the forming of the passivation material layer includes forming the passivation material layer with a thickness ranging from ~~about~~ 1 nm to ~~about~~ 4 nm, effectively preventing interaction between chlorine and metal residuals under the passivation material layer.

8. (Original) The method of claim 1, further comprising performing a fluorine treatment to the passivation material layer before the epitaxially growing of the second semiconductor material.

9. (Currently amended) The method of claim 8, wherein the performing of the fluorine treatment includes performing the fluorine treatment with a fluorine dose ranging from ~~about~~ 1×10^{14} ions/cm^2 to ~~about~~ 2×10^{15} ions/cm^2.

10. (Original) The method of claim 1, wherein the epitaxially growing of the second semiconductor material includes epitaxially growing the second semiconductor material with in-situ doping one of a n-type dopant and a p-type dopant.

11. (Original) The method of claim 1, wherein the epitaxially growing of the second semiconductor material includes performing a cyclic deposition and etching (CDE) process.

12. (Original) The method of claim 11, wherein

the CDE process includes a first cycle for deposition and a second cycle for etching; and

the second cycle uses a chlorine-containing gas that includes at least one of HCl and Cl_2.

13. (Original) The method of claim 12, wherein the first cycle of the CDE process uses a precursor that includes PH_3, monomethylsilane (MMS), and at least one of SiH_4 and Si_2H_6.

14. (Original) The method of claim 12, wherein the first cycle of the CDE process uses a precursor that includes B_2H_6, GeH_4, and at least one of SiH_4 and Si_2H_6.

15. (Original) A method of forming a field effect transistor (FET), the method comprising:

performing an etching process to a semiconductor substrate, thereby forming recesses in source and drain (S/D) regions of the semiconductor substrate; and

epitaxially growing a semiconductor material by a deposition process with a varying etching/deposition (E/D) factor, thereby forming S/D features in the recesses.

16. (Original) The method of claim 15, wherein the deposition process incudes a first deposition step having a first etch/deposition (E/D) factor and thereafter a second deposition step having a second E/D factor greater than the first E/D factor.

17. (Original) The method of claim 15, wherein

the first deposition step is a non-selective deposition; and

the second deposition step is a selective deposition.

18. (Original) The method of claim 15, wherein

the first deposition step has a first substrate temperature less than 620 ^{0}C; and

the second deposition step has a second substrate temperature greater than 620 ^{0}C.

19. (Original) The method of claim 15, wherein the deposition process includes one of a cyclic deposition and etching (CDE) process; a co-flow epitaxy growth; and a combination thereof.

20. (Original) The method of claim 15, wherein the epitaxially growing of the semiconductor material includes varying the E/D factor by a mechanism selected from gas partial pressure, gas flow rate, substrate temperature, and a combination thereof.

21-26. (Canceled)

27. (New) A method of forming a field effect transistor (FET), the method comprising:

performing an etching process to a semiconductor substrate, thereby forming recesses in source and drain (S/D) regions of the semiconductor substrate;

forming a passivation layer of a first semiconductor material in the recesses;

performing a fluorine treatment to the passivation layer; and

epitaxially growing a second semiconductor material over the passivation layer, thereby forming S/D features in the recesses.

28. (New) The method of claim 27, wherein the fluorine treatment is a fluorine plasma treatment.

29. (New) The method of claim 27, wherein the fluorine treatment uses a fluorine dose ranging from 1×10^{14} ions/cm^2 to 2×10^{15} ions/cm^2.

30. (New) The method of claim 27, wherein the forming of the passivation layer includes performing a non-selective deposition process using a precursor free of chlorine; and the epitaxially growing of the second semiconductor material includes an etching process using a chlorine-containing gas.

31. (New) The method of claim 27, wherein the forming of the passivation layer includes epitaxially growing the first semiconductor material that is free of dopant, using a precursor free of dopant-containing gas.

32. (New) The method of claim 31, wherein the epitaxially growing of the second semiconductor material includes in-situ doping one of a n-type dopant and a p-type dopant to the second semiconductor material.

Remarks

Claims 1-26 were originally filed in the present application, of which claims 21-26 have been canceled, claims 3, 6, 7, and 9 have been amended, and claims 27-32 have been added. Consideration and allowance of pending claims 1-20 and 27-32 is respectfully requested.

The Examiner has identified two groups for restriction:

Group I: claims 1-20; and

Group II: claims 21-26.

Applicants elect, without traverse, Group I. Claims directed to the unelected groups have been canceled. Applicants further submit that new claims 27-32 are directed to the elected group.

The Examiner is invited to telephone the undersigned as needed.

Respectfully submitted,

/David M. O'Dell/

David M. O'Dell
Registration No. 42,044

Date: March 14, 2016

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2323 Victory Avenue, Suite 700
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15624862_1

Certificate of Service

I hereby certify that this correspondence is being filed with the U.S. Patent and Trademark Office via EFS-Web on March 14, 2016.

/Linda Ingram/

Linda Ingram

Electronic Acknowledgement Receipt

EFS ID:	25190385
Application Number:	14597115
International Application Number:	
Confirmation Number:	8745
Title of Invention:	Metal-Insensitive Epitaxy Formation
First Named Inventor/Applicant Name:	Chun Hsiung Tsai
Customer Number:	42717
Filer:	David M. Odell/Linda Ingram
Filer Authorized By:	David M. Odell
Attorney Docket Number:	2014-0937/24061.2998
Receipt Date:	14-MAR-2016
Filing Date:	14-JAN-2015
Time Stamp:	16:55:51
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		2998_Response_Restriction.pdf	36081 1ecda9dde8a61042bd1ec9c891f4cefc44252 48d	yes	6

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Response to Election / Restriction Filed	1	1
	Claims	2	5
	Applicant Arguments/Remarks Made in an Amendment	6	6
Warnings:			
Information:			
	Total Files Size (in bytes):	36081	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 14/597,115	Filing Date 01/14/2015	☐ To be Mailed

ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT **03/14/2016**

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	* 26	Minus	** 26	= 0	X $80 =	0
Independent (37 CFR 1.16(h))	* 3	Minus	***3	= 0	X $420 =	0
☐ Application Size Fee (37 CFR 1.16(s))						
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
					TOTAL ADD'L FEE	0

AMENDMENT

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =	
☐ Application Size Fee (37 CFR 1.16(s))						
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
					TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
/SONYA HILLIARD/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
14/597,115	01/14/2015	Chun Hsiung Tsai	2014-0937/24061.2998

CONFIRMATION NO. 8745

PUBLICATION NOTICE

42717
HAYNES AND BOONE, LLP
IP Section
2323 Victory Avenue
Suite 700
Dallas, TX 75219

OC000000080914795

Title: Metal-Insensitive Epitaxy Formation

Publication No.US-2016-0056290-A1
Publication Date:02/25/2016

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently http://www.uspto.gov/patft/.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Office of Public Records. The Office of Public Records can be reached by telephone at (703) 308-9726 or (800) 972-6382, by facsimile at (703) 305-8759, by mail addressed to the United States Patent and Trademark Office, Office of Public Records, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently http://pair.uspto.gov/. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 1-866-217-9197.

Office of Data Managment, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/597,115	01/14/2015	Chun Hsiung Tsai	2014-0937/24061.2998	8745

42717 7590 01/12/2016

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EXAMINER	
SPALLA, DAVID C	

ART UNIT	PAPER NUMBER
2896	

MAIL DATE	DELIVERY MODE
01/12/2016	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 14/597,115	Applicant(s) TSAI ET AL.	
	Examiner DAVID SPALLA	Art Unit 2896	AIA (First Inventor to File) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 2 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01/14/2015*.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) *1-26* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☐ Claim(s) _____ is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☒ Claim(s) *1-26* are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

DETAILED ACTION

Election/Restrictions

Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-20, drawn to a process, classified in H01L 21/823418+.

II. Claims 21-26, drawn to a product, classified in H01L 29/7848+.

The inventions are distinct, each from the other because of the following reasons:

Inventions I and II are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make another and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f)). In the instant case, the product could be made by a materially different process such as forming a dummy gate or mask, etching S/D regions, forming a passivation and semiconductor material in the recess, removing the dummy gate or mask and forming the final gate.

Restriction for examination purposes as indicated is proper because all these inventions listed in this action are independent or distinct for the reasons given above and there would be a serious search and/or examination burden if restriction were not required because one or more of the following reasons apply:

A thorough search of the product, as claimed, would not cover the scope of examination needed for the process. Numerous methods of etching and deposition are known in the art, a number of which might arrive at the claimed product. A thorough search of the process, as claimed, would not cover the scope of examination needed for the product. The first process lacks structural requirements of the product such as a second transistor to form a CMOS device. The second process lacks structural requirements such as a passivation layer.

Applicant is advised that the reply to this requirement to be complete must include (i) an election of an invention to be examined even though the requirement may be traversed (37 CFR 1.143) **and (ii) identification of the claims encompassing the elected invention**.

The election of an invention may be made with or without traverse. To reserve a right to petition, the election must be made with traverse. If the reply does not distinctly and specifically point out supposed errors in the restriction requirement, the election shall be treated as an election without traverse. Traversal must be presented at the time of election in order to be considered timely. Failure to timely traverse the requirement will result in the loss of right to petition under 37 CFR 1.144. If claims are added after the election, applicant must indicate which of these claims are readable upon the elected invention.

Should applicant traverse on the ground that the inventions are not patentably distinct, applicant should submit evidence or identify such evidence now of record showing the inventions to be obvious variants or clearly admit on the record that this is the case. In either instance, if the examiner finds one of the inventions unpatentable over the prior art, the evidence or admission may be used in a rejection under 35 U.S.C. 103 or pre-AIA 35 U.S.C. 103(a) of the other invention.

Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be corrected in compliance with 37 CFR 1.48(a) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. A request to correct inventorship under 37 CFR 1.48(a) must be accompanied by an application data sheet in accordance with 37 CFR 1.76 that identifies each inventor by his or her legal name and by the processing fee required under 37 CFR 1.17(i).

The examiner has required restriction between product or apparatus claims and process claims. Where applicant elects claims directed to the product/apparatus, and all product/apparatus claims are subsequently found allowable, withdrawn process claims that include all the limitations of the allowable product/apparatus claims should be considered for rejoinder. All claims directed to a nonelected process invention must include all the limitations of an allowable product/apparatus claim for that process invention to be rejoined.

In the event of rejoinder, the requirement for restriction between the product/apparatus claims and the rejoined process claims will be withdrawn, and the rejoined process claims will be fully examined for patentability in accordance with 37 CFR 1.104. Thus, to be allowable, the rejoined claims must meet all criteria for patentability including the requirements of 35 U.S.C. 101, 102, 103 and 112. Until all claims to the elected product/apparatus are found allowable, an otherwise proper restriction requirement between product/apparatus claims and process claims may be maintained. Withdrawn process claims that are not commensurate in scope with an allowable product/apparatus claim will not be rejoined. See MPEP § 821.04. Additionally, in order for rejoinder to occur, applicant is advised that the process claims should be amended during prosecution to require the limitations of the product/apparatus claims. **Failure to do so may result in no rejoinder.** Further, note that the prohibition against double patenting rejections of 35 U.S.C. 121 does not apply where the restriction requirement is withdrawn by the examiner before the patent issues. See MPEP § 804.01.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DAVID SPALLA whose telephone number is (303)297-4298. The examiner can normally be reached on Mon-Fri 10am-5pm MST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Such can be reached on (571) 272-8895. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/DAVID SPALLA/
Examiner, Art Unit 2896

In place of PTO-1449 Form	U. S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE			*Complete if Known*	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(use as many sheets as necessary)*				Application Number	14/597,115
				Filing Date	January 14, 2015
				First Inventor Name	Chun Hsiung Tsai et al.
				Art Unit	2811
				Examiner Name	unknown
SHEET	1	OF	1	Attorney Docket Number	2014-0937/24061.2998

U. S. PATENTS				
Examiner's Initials	Cite No.	Document Number	Issue Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document

U. S. PATENT APPLICATION PUBLICATIONS				
Examiner's Initials	Cite No.	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document

FOREIGN PATENT DOCUMENTS					
Examiner's Initials	Cite No.	Foreign Patent Document (Country Code – Number – Kind)	Publication Date MM-DD-YYYY	Patentee or Applicant of Cited Document	Translation Y/N

NON-PATENT LITERATURE DOCUMENTS		
Examiner's Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article, title of the item, date, page(s), volume-issue number(s), publisher, city/country where published
	A1	Y. BOGUMILOWICZ *et al.*, "Chemical vapour etching of Si, SiGe and Ge with HC1; applications to the formation of thin relaxed SiGe buffers and to the revelation of threading dislocations," Institute of Physics Publishing, December 17, 2004, pages 127-134, Semicond. Sci. Technol. 20 (2005), France.
	A2	V. DESTEFANIS *et al.*, "High pressure *in situ* HC1 etching of $Si_{1-x}Ge_x$ versus Si for advanced devices," Semiconductor Science and Technology, September 16, 2008, pages 9, Semicond. Sci. Technol. 23 (2008), France.
	A3	V. DESTEFANIS *et al.*, Low-thermal surface preparation, HC1 etch and Si/SiGe selective epitaxy on (1 1 0) silicon surfaces," Semiconductor Science and Technology, September 16, 2008, pages 9, Semicond. Sci. Technol. 23 (2008), France.
	A4	Y. BOGUMILOWICZ *et al.*, "Selective chemical vapour etching of $Si_{1-x}Ge_x$ versus Si with gaseous HC1," Semiconductor Science and Technology, October 18, 2006, pages 1668-1674, Semicond. Sci. Technol. 21 (2006), France.
	A5	J. M. HARTMANN *et al.*, "Tensile-strained Si layers grown on $Si_{0.6}Ge_{0.4}$ and $Si_{0.5}Ge_{0.5}$ virtual substrates: I. Film thickness and morphology, Semiconductor Science and Technology, March 7, 2007, pages 354-361, Semicond. Sci. Technol. 22 (2007), France.

Examiner Signature		Date Considered	

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include a copy of this form with next communication to applicant.

Electronic Acknowledgement Receipt

EFS ID:	22500998
Application Number:	14597115
International Application Number:	
Confirmation Number:	8745
Title of Invention:	Metal-Insensitive Epitaxy Formation
First Named Inventor/Applicant Name:	Chun Hsiung Tsai
Customer Number:	42717
Filer:	David M. Odell/Linda Ingram
Filer Authorized By:	David M. Odell
Attorney Docket Number:	2014-0937/24061.2998
Receipt Date:	01-JUN-2015
Filing Date:	14-JAN-2015
Time Stamp:	16:58:12
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		2998_IDS.pdf	114865 dfe7bcd805bc6a705fa78e297cf8d903778a3363	yes	2

	Multipart Description/PDF files in .zip description				
	Document Description		**Start**	**End**	
	Transmittal Letter		1	1	
	Information Disclosure Statement (IDS) Form (SB08)		2	2	
Warnings:					
Information:					
2	Non Patent Literature	2998_NPL1_chemicalvapouretching.pdf	1012758 6a337c48d456874aea0c95caa2f5e6d218785aca	no	8
Warnings:					
Information:					
3	Non Patent Literature	2998_NPL2_selectivechemicalvapour.pdf	687575 36e9b483269e2b64f1ee0a8ddfaf0359cc153227	no	7
Warnings:					
Information:					
4	Non Patent Literature	2998_NPL3_highpressureinsitu.pdf	914792 5229fd41786f187afb035e3a8a217eb806c7c84f	no	9
Warnings:					
Information:					
5	Non Patent Literature	2998_NPL4_tensilestrainedsi.pdf	1776069 9dc8fda0dc7b5bdcfe63e656ea2f6c3795301371	no	8
Warnings:					
Information:					
6	Non Patent Literature	2998_NPL5_lowthermalsurfacepreparation.pdf	732764 b3935e3fafeee4d22b3f1e76c8f1b63e9c88f88c	no	9
Warnings:					
Information:					
		Total Files Size (in bytes):	5238823		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Chun Hsiung Tsai *et al.*	§	Confirmation No.: 8745
Application No. 14/597,115	§	Group Art Unit: 2811
Filed: January 14, 2015	§	Examiner: unknown
For: Metal-Insensitive Epitaxy Formation	§	Attorney Docket No. 2014-0937/24061.2998

INFORMATION DISCLOSURE STATEMENT

Mail Stop Amendment
Commissioner For Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

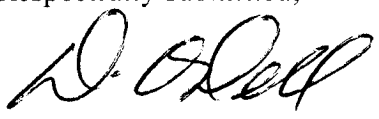
In compliance with the duty of disclosure under 37 CFR §1.56, and in accordance with the practice under 37 CFR §1.97 and §1.98, the Examiner's attention is directed to the documents listed on the enclosed modified Form PTO-1449. No inference should be made that the cited references are in fact material, are in fact prior art, or that no better art exists. The references are not in any order based on their pertinence.

This Information Disclosure Statement is being filed within three months of the United States filing date or before the mailing date of a first Office Action on the merits. No certification or fee is required (37 CFR §1.97(b)).

The Commissioner is hereby authorized to charge any additional fees which may be required or credit any overpayment to Deposit Account No. 08-1394.

It is respectfully requested that the above information be considered by the Examiner and that a copy of the enclosed modified Form PTO-1449 be returned indicating that such information has been considered.

Respectfully submitted,



Date: June 1, 2015

David M. O'Dell
Registration No. 42,044

HAYNES AND BOONE, LLP
IP Section
2323 Victory Avenue, Suite 700
Dallas, Texas 75219
Direct Telephone: 972-739-8635
IP Facsimile: 214-200-0853

CERTIFICATE OF TRANSMISSION

I hereby certify that this correspondence and any attachments are being transmitted via the Electronic Filing System (EFS) Web with the United States Patent and Trademark Office on June 1, 2015.

Linda Ingram

Linda Ingram

15055958_1

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 14/597,115

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	280
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	600
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	720
TOTAL CLAIMS (37 CFR 1.16(i))	26 minus 20 =	* 6			OR	x 80 =	480
INDEPENDENT CLAIMS (37 CFR 1.16(h))	3 minus 3 =	*				x 420 =	0.00
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	2080

APPLICATION AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE($)	ADDITIONAL FEE($)		RATE($)	ADDITIONAL FEE($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
14/597,115	01/14/2015	2811	2080	2014-0937/24061.2998	26	3

CONFIRMATION NO. 8745

42717
HAYNES AND BOONE, LLP
IP Section
2323 Victory Avenue
Suite 700
Dallas, TX 75219

FILING RECEIPT

OC000000073113666

Date Mailed: 01/29/2015

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

Chun Hsiung Tsai, Hsinchu County, TAIWAN;
Yuan-Ko Hwang, Hsinchu City, TAIWAN;

Applicant(s)

Taiwan Semiconductor Manufacturing Company, Ltd., Hsin-Chu, TAIWAN

Power of Attorney: The patent practitioners associated with Customer Number 42717

Domestic Priority data as claimed by applicant

This appln claims benefit of 62/040,880 08/22/2014

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.
Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access - A proper **Authorization to Permit Access to Application by Participating Offices** (PTO/SB/39 or its equivalent) has been received by the USPTO.

If Required, Foreign Filing License Granted: 01/29/2015

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 14/597,115**

Projected Publication Date: 02/25/2016

Non-Publication Request: No

Early Publication Request: No

Title

Metal-Insensitive Epitaxy Formation

Preliminary Class

257

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

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This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

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Doc Code: PD.TO.AUTH
Document Description: Authorization to access Appl. by Trilateral Office

PTO/SB/39 (07-09)
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AUTHORIZATION TO PERMIT ACCESS TO APPLICATION BY PARTICIPATING OFFICES

Send completed form to: Commissioner for Patents
P.O. Box 1450, Alexandria, VA 22313-1450

COMPLETE IF KNOWN	
Application Number	Unassigned
Filing Date	Herewith
First Named Inventor	Chun Hsiung Tsai et al.
Attorney Docket Number	2014-0937/24061.2998
Title (Required)	Metal-Insensitive Epitaxy Formation

The undersigned hereby grants the USPTO authority to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the World Intellectual Property Office (WIPO), and any other intellectual property offices in which a foreign application claiming priority to the above-identified patent application is filed access to the above-identified patent application. See 37 CFR 1.14(c) and (h).

In accordance with 37 CFR 1.14(h)(3), access will be provided to a copy of the above-identified application with respect to: 1) the above-identified patent application-as-filed; 2) any foreign application to which the above-identified patent application claims priority under 35 U.S.C. 119(a)-(d) if a copy of the foreign application that satisfies the certified copy requirement of 37 CFR 1.55 has been filed in the above-identified patent application; and 3) any U.S. application-as-filed from which benefit is sought in the above-identified patent application.

In accordance with 37 CFR 1.14(c), access may be provided to information concerning the date of filing the Authorization to Permit Access to Application by Participating Offices.

This written authorization should be submitted prior to the filing of a subsequent foreign application, in which priority is claimed to the above-identified patent application, with any intellectual property office (e.g., the EPO, JPO, KIPO, or DAS Accessing Office). However, if applicant does not wish the EPO, JPO, KIPO, WIPO, or other intellectual property office in which a foreign application claiming priority to the above-identified patent application is filed to have access to the above-identified patent application, this written authorization should not be filed.

No fee will be charged under 37 CFR 1.19(b)(1) for providing a participating intellectual property office with an electronic copy of the above-identified patent application.

This form must be signed by an authorized party in accordance with 37 CFR 1.14(c).

/David M. O'Dell/	January 14, 2015
Signature	Date
David M. O'Dell	972-739-8635
Printed or Typed Name	Telephone Number
Attorney of Record	42,044
Title	Registration Number, if applicable

This collection of information is required by 37 CFR 1.14(h). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process an application). Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 6 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

steady 2014/09/12 09:38:12

Docket No.: 2014-0937/24061.2998
Customer No.: 42717

INVENTORS' DECLARATION FOR PATENT APPLICATION

As below named inventor, I hereby declare that:

The below-mentioned application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the below-mentioned application.

METAL-INSENSITIVE EPITAXY FORMATION

the specification of which (check one):

__X__ is attached hereto.

_____ was filed on _____
under Attorney's Docket Number 2014-0937/24061.2998
as Application Serial No. _____
and was amended on_____ (if applicable).

I hereby authorize the attorney of record to update this document to include Patent Office information as deemed necessary (i.e., filing date, serial number, etc.).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to patentability of this application in accordance with 37 CFR 1.56, material information which became available between the filing date of the application and issuance thereof, including any continuation, divisional and/or continuation-in-part.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

FULL NAME OF INVENTOR: YUAN-KO HWANG

INVENTOR'S SIGNATURE: _____ DATED: 09/17/2014

chcealy 2014/09/12 09:38:12

Docket No.: 2014-0937/24061.2998
Customer No.: 42717

INVENTORS' DECLARATION FOR PATENT APPLICATION

As below named inventor, I hereby declare that:

The below-mentioned application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the below-mentioned application.

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the specification of which (check one):

__X__ is attached hereto.

_____ was filed on _____
under Attorney's Docket Number 2014-0937/24061.2998
as Application Serial No. _____
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I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

FULL NAME OF INVENTOR: CHUN HSIUNG TSAI

INVENTOR'S SIGNATURE: Chun Hsiung Tsai DATED: 09/12/2014

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Chun Hsiung Tsai et al.	§	Confirmation No.: Unknown
Application No. Unknown	§	Group Art Unit: Unknown
Filed: Herewith	§	Customer No.: 42717
For: Metal-Insensitive Epitaxy Formation	§	Docket No.: 2014-0937/24061.2998

INFORMATION DISCLOSURE STATEMENT

Mail Stop Amendment
Commissioner For Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In compliance with the duty of disclosure under 37 CFR §1.56, and in accordance with the practice under 37 CFR §1.97 and §1.98, the Examiner's attention is directed to the documents listed on the enclosed modified Form PTO-1449. No inference should be made that the cited references are in fact material, are in fact prior art, or that no better art exists. The cited patents are listed in numerical order and are not in any order based on their pertinence.

Pursuant to 37 CFR § 1.98(a)(2)(i), copies of the U.S. patent documents listed on the enclosed modified Form PTO-1449 are not attached.

This Information Disclosure Statement is being filed within three months of the United States filing date or before the mailing date of a first Office Action on the merits. No certification or fee is required (37 CFR §1.97(b)).

The Commissioner is hereby authorized to charge any additional fees which may be required or credit any overpayment to Deposit Account No. 08-1394.

It is respectfully requested that the above information be considered by the Examiner and that a copy of the enclosed modified Form PTO-1449 be returned indicating that such information has been considered.

Respectfully submitted,

David M. O'Dell
Registration No. 42,044

Date: 1-14-15
HAYNES AND BOONE, LLP
IP Section
Direct Telephone: 972-739-8635
IP Facsimile: 214-200-0853
R-392084_1

CERTIFICATE OF TRANSMISSION

I hereby certify that this correspondence and any attachments are being transmitted via the Electronic Filing System (EFS) Web with the United States Patent and Trademark Office on January 14, 2015

Linda Ingram

In place of PTO-1449 Form	U. S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE			*Complete if Known*	
				Application Number	TBD
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(use as many sheets as necessary)*				Filing Date	Herewith
				First Inventor Name	Chun Hsiung Tsai
				Art Unit	TBD
				Examiner Name	TBD
SHEET	1	OF	1	Attorney Docket Number	2014-0937/24061.2998

U. S. PATENTS				
Examiner's Initials	Cite No.	Document Number	Issue Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document
		7,667,271	02/23/2010	Yu et al.
		8,362,575	01/29/2013	Kwok et al.
		8,367,498	02/05/2013	Chang et al.
		8,440,517	05/14/2013	Lin et al.
		8,497,528	07/30/2013	Lee et al.
		8,610,240	12/17/2013	Lee et al.
		8,680,576	03/25/2014	Ching et al.
		8,723,272	05/13/2014	Liu et al.
		8,729,627	05/20/2014	Cheng et al.
		8,729,634	05/20/2014	Shen et al.
		8,785,285	07/22/2014	Tsai et al.
		8,796,759	08/05/2014	Perng et al.
		8,809,139	08/19/2014	Huang et al.
		8,828,823	09/09/2014	Liu et al.
		8,836,016	09/16/2014	Wu et al.
		8,841,701	09/23/2014	Lin et al.
		8,847,293	09/30/2014	Lee et al.
		8,853,025	10/07/2014	Zhang et al.

U. S. PATENT APPLICATION PUBLICATIONS				
Examiner's Initials	Cite No.	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document
		2011/0068407	03/24/2011	Yeh Chih Chieh et al.
		2013/0011983	01/10/2013	Tsai Ji-Yin et al.
		2013/0328126	12/12/2013	Tsai et al.
		2014/0252412	09/11/2014	Tsai Chun Hsiang et al.

FOREIGN PATENT DOCUMENTS					
Examiner's Initials	Cite No.	Foreign Patent Document (Country Code – Number – Kind)	Publication Date MM-DD-YYYY	Patentee or Applicant of Cited Document	Translation Y/N

NON-PATENT LITERATURE DOCUMENTS		
Examiner's Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article, title of the item, date, page(s), volume-issue number(s), publisher, city/country where published

Examiner Signature		Date Considered	

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include a copy of this form with next communication to applicant.

Doc Code: PA..
Document Description: Power of Attorney

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TRANSMITTAL FOR POWER OF ATTORNEY TO ONE OR MORE REGISTERED PRACTITIONERS

NOTE: This form is to be submitted with the Power of Attorney by Applicant form (PTO/AIA/82B) to identify the application to which the Power of Attorney is directed, in accordance with 37 CFR 1.5, unless the application number and filing date are identified in the Power of Attorney by Applicant form. If neither form PTO/AIA/82A nor form PTO/AIA82B identifies the application to which the Power of Attorney is directed, the Power of Attorney will not be recognized in the application.

Application Number	TBD
Filing Date	January 14, 2015
First Named Inventor	Chun Hsiung Tsai
Title	Metal-Insensitive Epitaxy Formation
Art Unit	TBD
Examiner Name	TBD
Attorney Docket Number	2014-0937/24061.2998

SIGNATURE of Applicant or Patent Practitioner

Signature	/David M. O'Dell/	Date (Optional)	January 14, 2015
Name	David M. O'Dell	Registration Number	42044
Title (if Applicant is a juristic entity)	Attorney of Record		
Applicant Name (if Applicant is a juristic entity)	Taiwan Semiconductor Manufacturing Company, Ltd.		

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4(d) for signature requirements and certifications. If more than one applicant, use multiple forms.

☑ *Total of 1 forms are submitted.

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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POWER OF ATTORNEY BY APPLICANT

I hereby revoke all previous powers of attorney given in the application identified in either the attached transmittal letter or the boxes below.

Application Number	Filing Date

(Note: The boxes above may be left blank if information is provided on form PTO/AIA/82A.)

☑ I hereby appoint the Patent Practitioner(s) associated with the following Customer Number as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above: 42717

OR

☐ I hereby appoint Practitioner(s) named in the attached list (form PTO/AIA/82C) as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the patent application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above. (Note: Complete form PTO/AIA/82C.)

Please recognize or change the correspondence address for the application identified in the attached transmittal letter or the boxes above to:

☑ The address associated with the above-mentioned Customer Number

OR

☐ The address associated with Customer Number:

OR

Firm or Individual Name	Haynes and Boone, LLP				
Address	2323 Victory Avenue, Suite 700				
City	Dallas	State	TX	Zip	75219
Country	USA				
Telephone	214-651-5000	Email	ipdocketing@haynesboone.com		

I am the Applicant (if the Applicant is a juristic entity, list the Applicant name in the box):

Taiwan Semiconductor Manufacturing Company, Ltd.

☐ Inventor or Joint Inventor (title not required below)

☐ Legal Representative of a Deceased or Legally Incapacitated Inventor (title not required below)

☑ Assignee or Person to Whom the Inventor is Under an Obligation to Assign (provide signer's title if applicant is a juristic entity)

☐ Person Who Otherwise Shows Sufficient Proprietary Interest (e.g., a petition under 37 CFR 1.46(b)(2) was granted in the application or is concurrently being filed with this document) (provide signer's title if applicant is a juristic entity)

SIGNATURE of Applicant for Patent

The undersigned (whose title is supplied below) is authorized to act on behalf of the applicant (e.g., where the applicant is a juristic entity).

Signature ✓		Date (Optional)	
Name	Billie Chen		
Title	Director of Intellectual Property Division, Taiwan Semiconductor Manufacturing Company, Ltd.		

NOTE: Signature - This form must be signed by the applicant in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. If more than one applicant, use multiple forms.

☐ Total of forms are submitted.

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: **Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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STATEMENT UNDER 37 CFR 3.73(c)

Applicant/Patent Owner: Chun Hsiung Tsai et al.

Application No./Patent No.: TBD Filed/Issue Date: January 14, 2015

Titled: Metal-Insensitive Epitaxy Formation

Taiwan Semiconductor Manufacturing Company, Ltd., a corporation

(Name of Assignee) (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that, for the patent application/patent identified above, it is (choose **one** of options 1, 2, 3 or 4 below):

1. ☑ The assignee of the entire right, title, and interest.

2. ☐ An assignee of less than the entire right, title, and interest (check applicable box):

   ☐ The extent (by percentage) of its ownership interest is _____%. Additional Statement(s) by the owners holding the balance of the interest must be submitted to account for 100% of the ownership interest.

   ☐ There are unspecified percentages of ownership. The other parties, including inventors, who together own the entire right, title and interest are:

   Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

3. ☐ The assignee of an undivided interest in the entirety (a complete assignment from one of the joint inventors was made). The other parties, including inventors, who together own the entire right, title, and interest are:

   Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

4. ☐ The recipient, via a court proceeding or the like (*e.g.*, bankruptcy, probate), of an undivided interest in the entirety (a complete transfer of ownership interest was made). The certified document(s) showing the transfer is attached.

The interest identified in option 1, 2 or 3 above (not option 4) is evidenced by either (choose **one** of options A or B below):

A. ☑ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel _____, Frame _____, or for which a copy thereof is attached.

B. ☐ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: _____ To: _____

   The document was recorded in the United States Patent and Trademark Office at

   Reel _____, Frame _____, or for which a copy thereof is attached.

2. From: _____ To: _____

   The document was recorded in the United States Patent and Trademark Office at

   Reel _____, Frame _____, or for which a copy thereof is attached.

This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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STATEMENT UNDER 37 CFR 3.73(c)

3. From: _____ To: _____

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The document was recorded in the United States Patent and Trademark Office at

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The document was recorded in the United States Patent and Trademark Office at

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6. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

☐ Additional documents in the chain of title are listed on a supplemental sheet(s).

☐ As required by 37 CFR 3.73(c)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

/David M. O'Dell/	January 14, 2015
Signature	Date
David M. O'Dell	42,044
Printed or Typed Name	Title or Registration Number

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

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Docket No.: 2014-0937/24061.2998
Customer No.: 42717

ASSIGNMENT

WHEREAS, we,

(1)	Chun Hsiung Tsai	of	No. 7, Daxiang Road, Xinpu Township Hsinchu County 305, Taiwan, R.O.C.
(2)	Yuan-Ko Hwang	of	No. 66, Zhiping Road, Hsinchu City 300 Taiwan, R.O.C.

have invented certain improvements in

METAL-INSENSITIVE EPITAXY FORMATION

for which we have executed an application for Letters Patent of the United States of America,

__X__ of even date filed herewith; and
_____ filed on _____ and assigned application number _____; and

WHEREAS, we authorize the attorney of record to update this document to include Patent Office information as deemed necessary (i.e., filing date, serial number, etc.);

WHEREAS, Taiwan Semiconductor Manufacturing Company, Ltd., ("TSMC"), No. 8, Li-Hsin Rd. 6, Science-Based Industrial Park Hsin-Chu, Taiwan 300-77, Republic of China. is desirous of obtaining the entire right, title, and interest in, to and under the said invention and the said application in the United States of America and in any and all countries foreign thereto;

NOW, THEREFORE, for good and valuable consideration, the receipt and sufficiency of which is hereby acknowledged, and other good and valuable consideration, we have sold, assigned, transferred and set over, and by these presents do hereby sell, assign, transfer and set over, unto the said TSMC, its successors, legal representatives, and assigns, the entire right, title, and interest in, to and under the said invention, and the said application, and all divisional, renewal, substitutional, and continuing applications thereof, and all Letters Patent of the United States of America which may be granted thereon and all reissues and extensions thereof, and all applications for Letters Patent which may be filed for said invention in any country or countries foreign to the United States of America, and all extensions, renewals, and reissues thereof, and all prior patents and patent applications from which a filing priority of the above-described patent application may be obtained, including the right to collect past damages; and we hereby authorize and request the Commissioner of Patents of the United States of America, and any official of any country or countries foreign to the United States of America, whose duty it is to issue patents on applications as aforesaid, to issue all Letters Patent for said invention to the said TSMC, its successors, legal representatives and assigns, in accordance with the terms of this instrument.

AND WE HEREBY covenant that we have full right to convey the entire interest herein assigned, and that we have not executed, and will not execute, any agreement in conflict herewith.

AND WE HEREBY further covenant and agree that we will communicate to said TSMC, its successors, legal representatives and assigns, any facts known to us respecting said invention, and testify in any legal proceedings, sign all lawful papers, execute all divisional, renewal, substitutional, continuing, and reissue applications, make all rightful declarations and/or oaths and generally do everything possible to aid the

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said TSMC, its successors, legal representatives and assigns, to obtain and enforce proper patent protection for said invention in all countries.

Inventor Name: Chun Hsiung Tsai

Residence Address: No. 7, Daxiang Road, Xinpu Township
Hsinchu County 305, Taiwan, R.O.C.

Dated: 09/12/2014 Chun Hsiung Tsai
Inventor Signature

Inventor Name: Yuan-Ko Hwang

Residence Address: No. 66, Zhiping Road, Hsinchu City 300, Taiwan, R.O.C.

Dated: 09/17/2014 Yuan-Ko Hwang
Inventor Signature

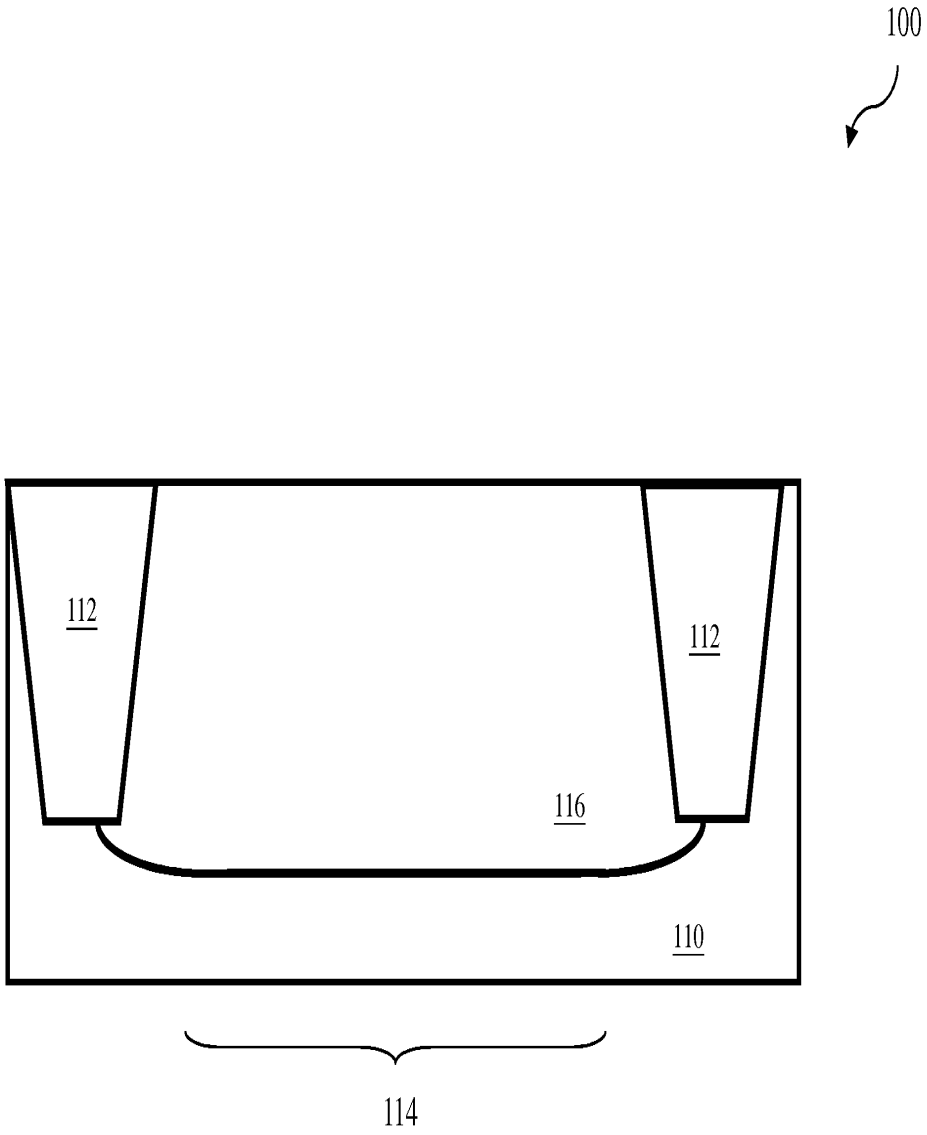


Fig. 1A

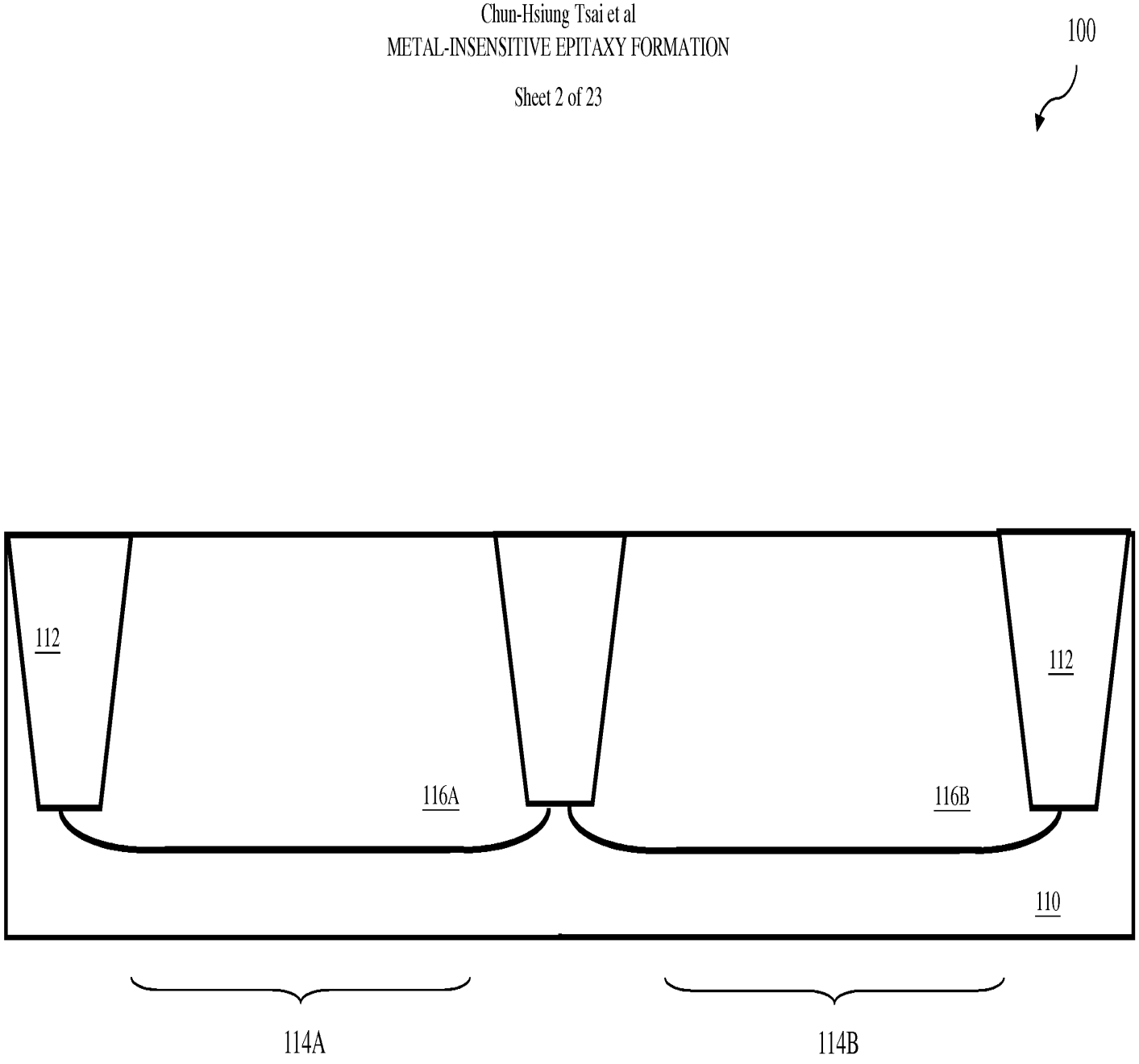


Fig. 1B

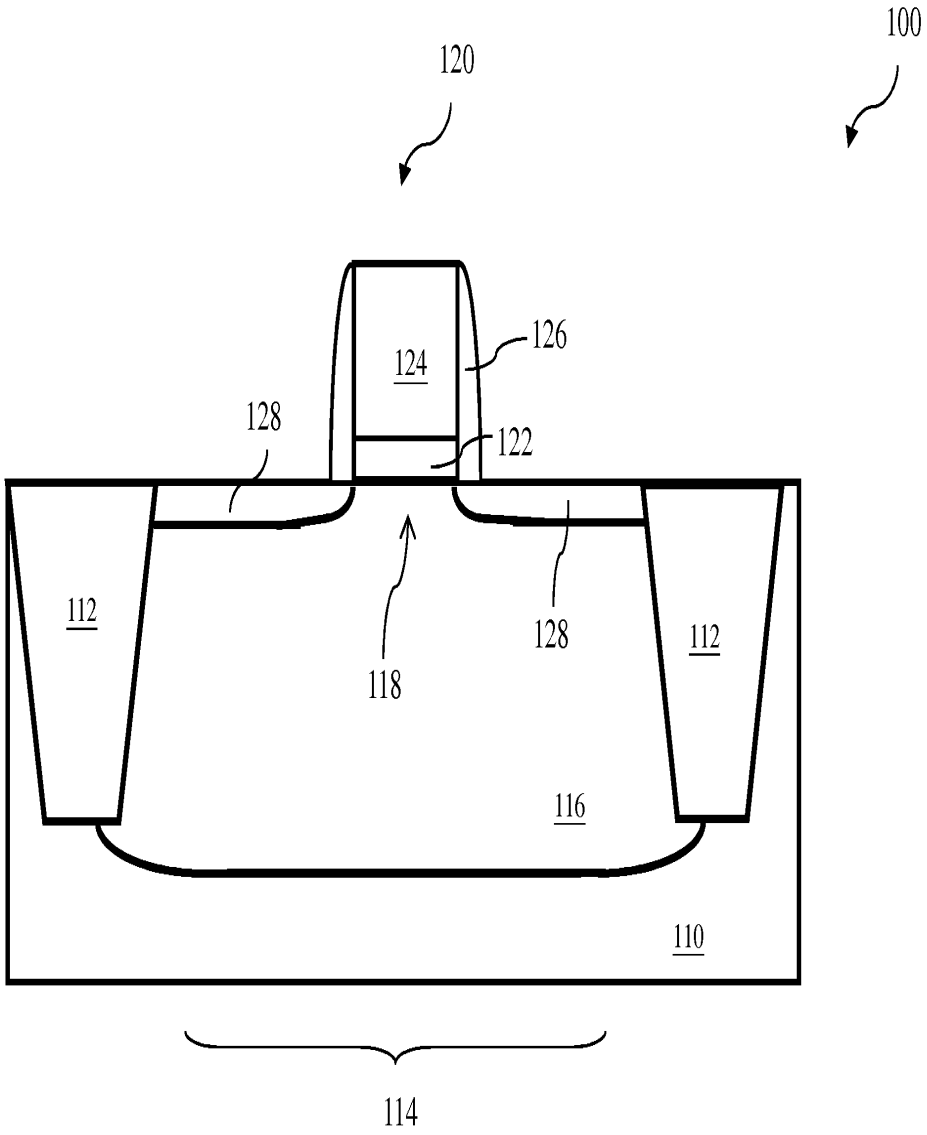


Fig. 2

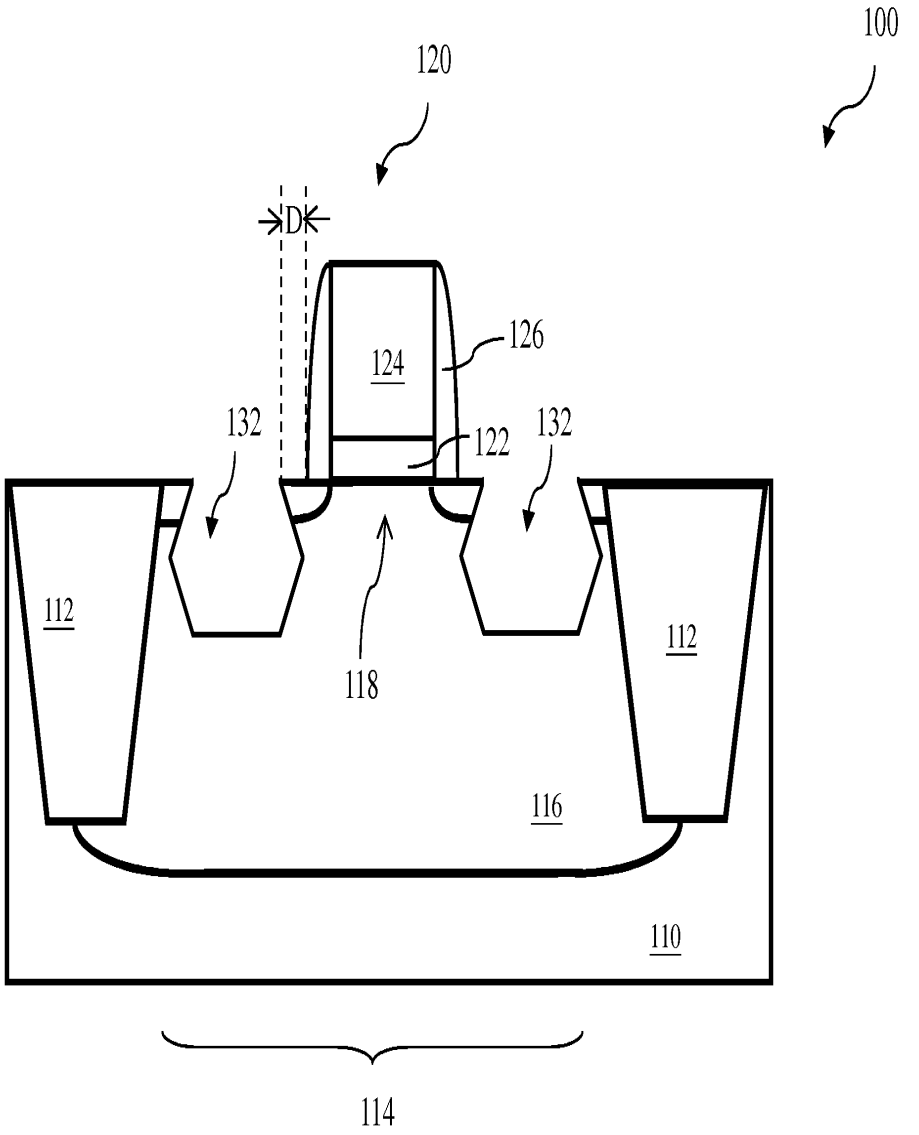


Fig. 3

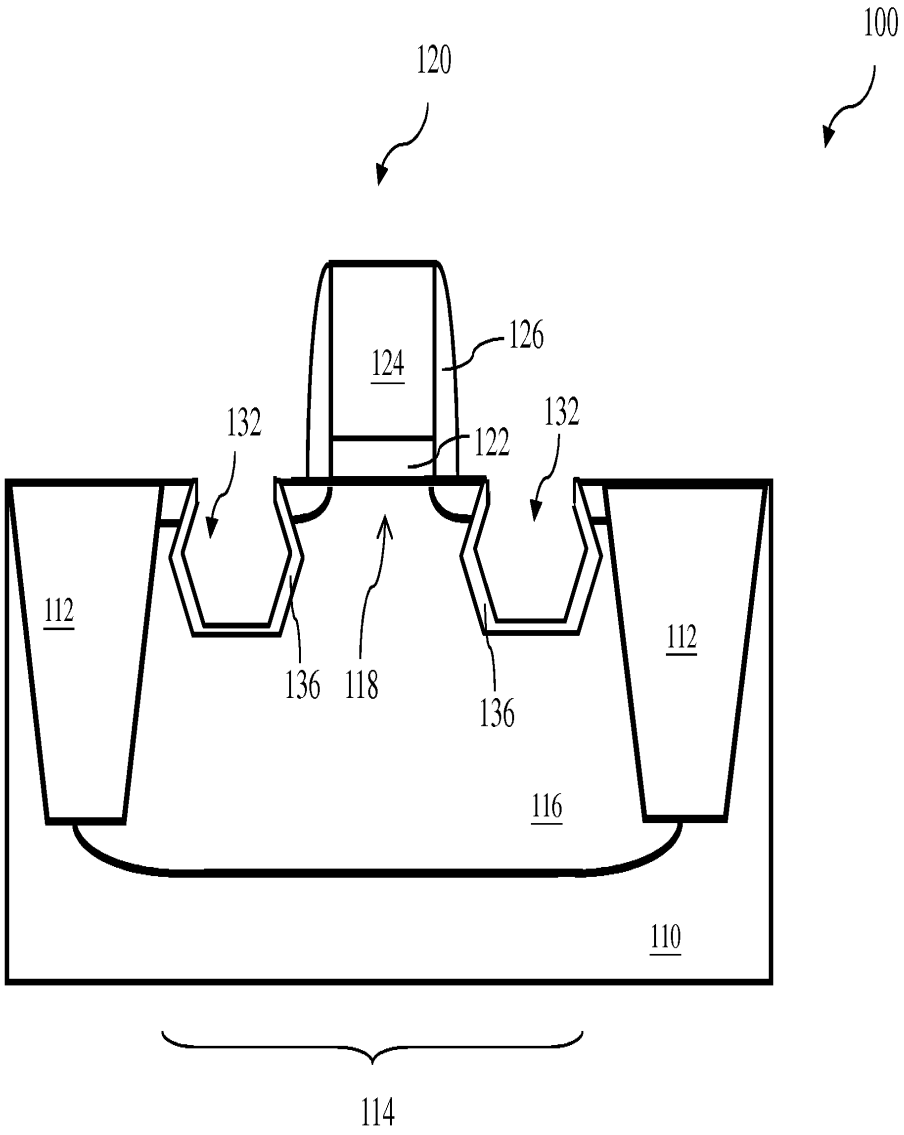


Fig. 4A

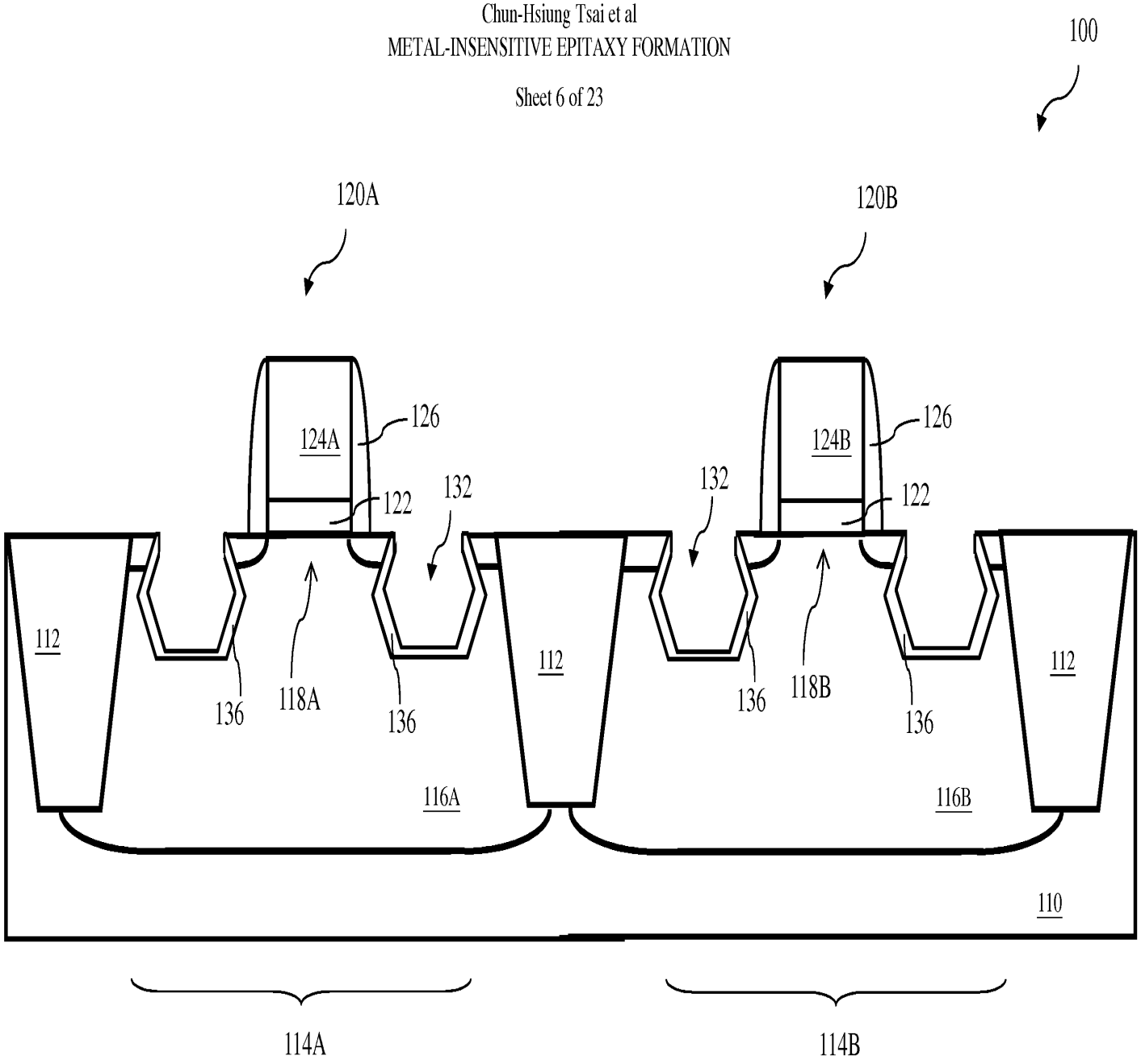

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Fig. 4B

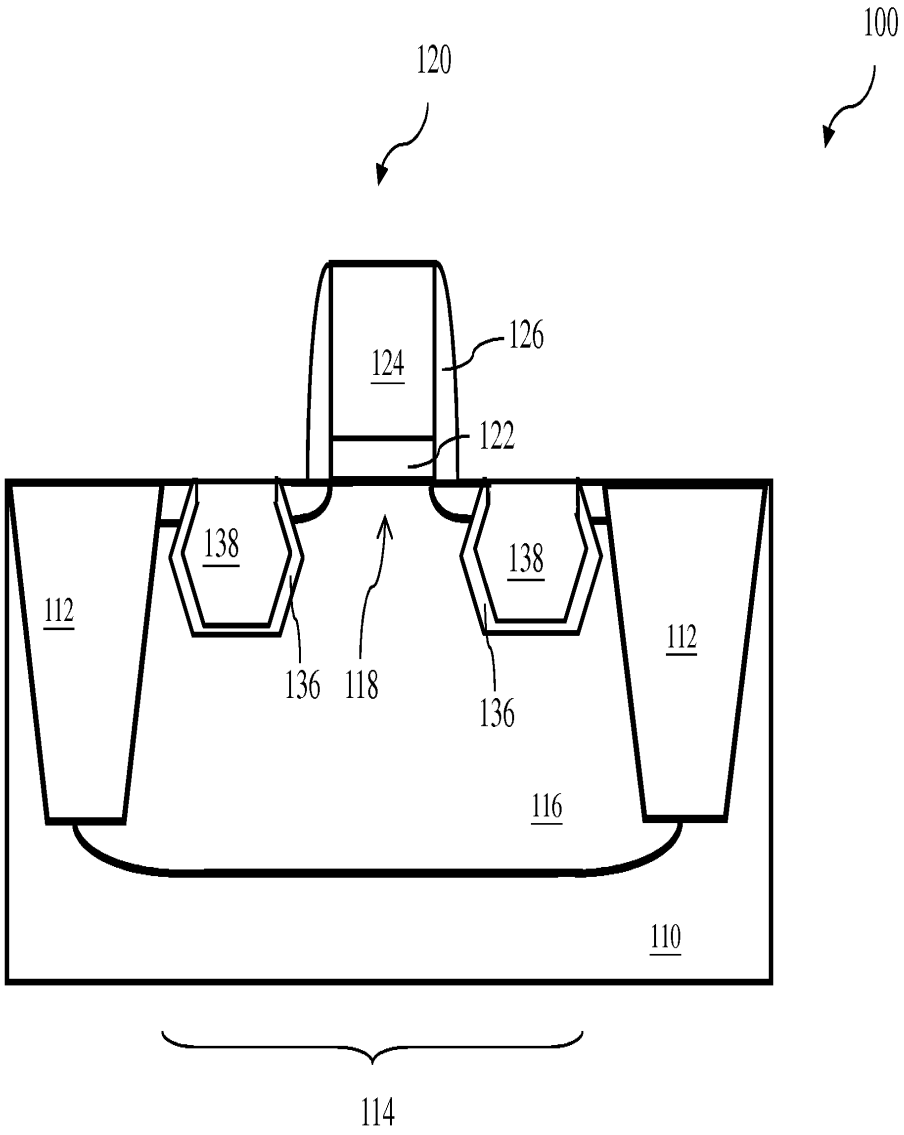


Fig. 5A

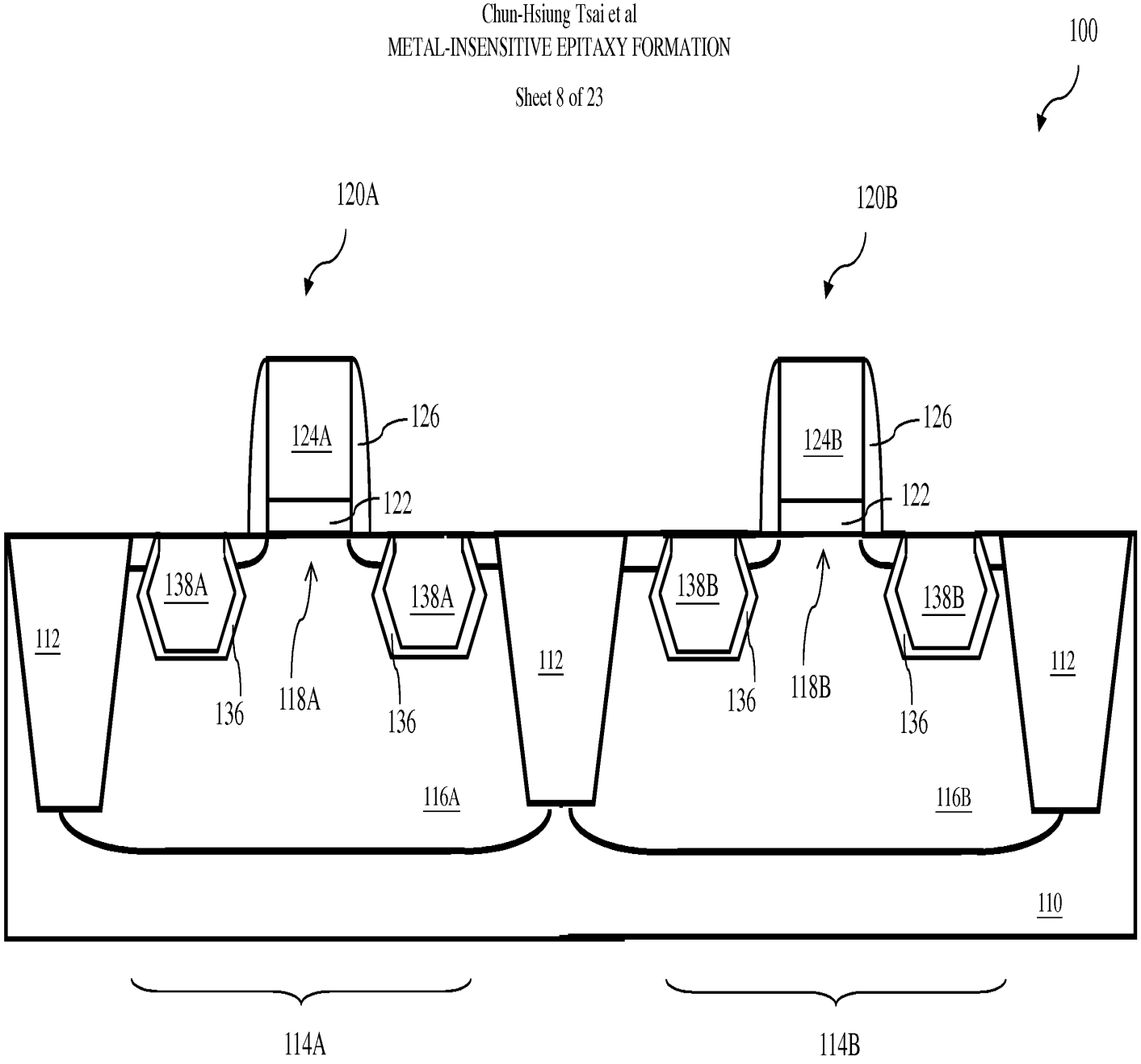

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Fig. 5B

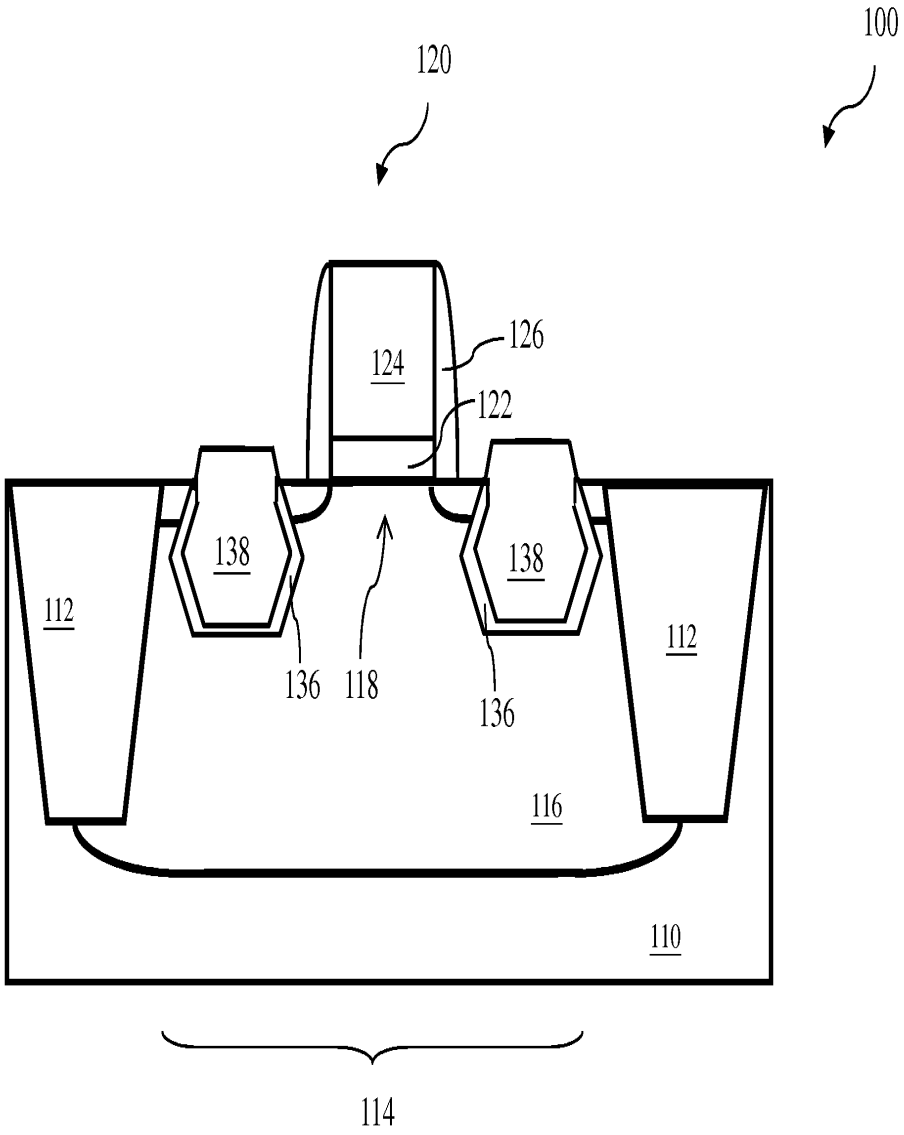


Fig. 6

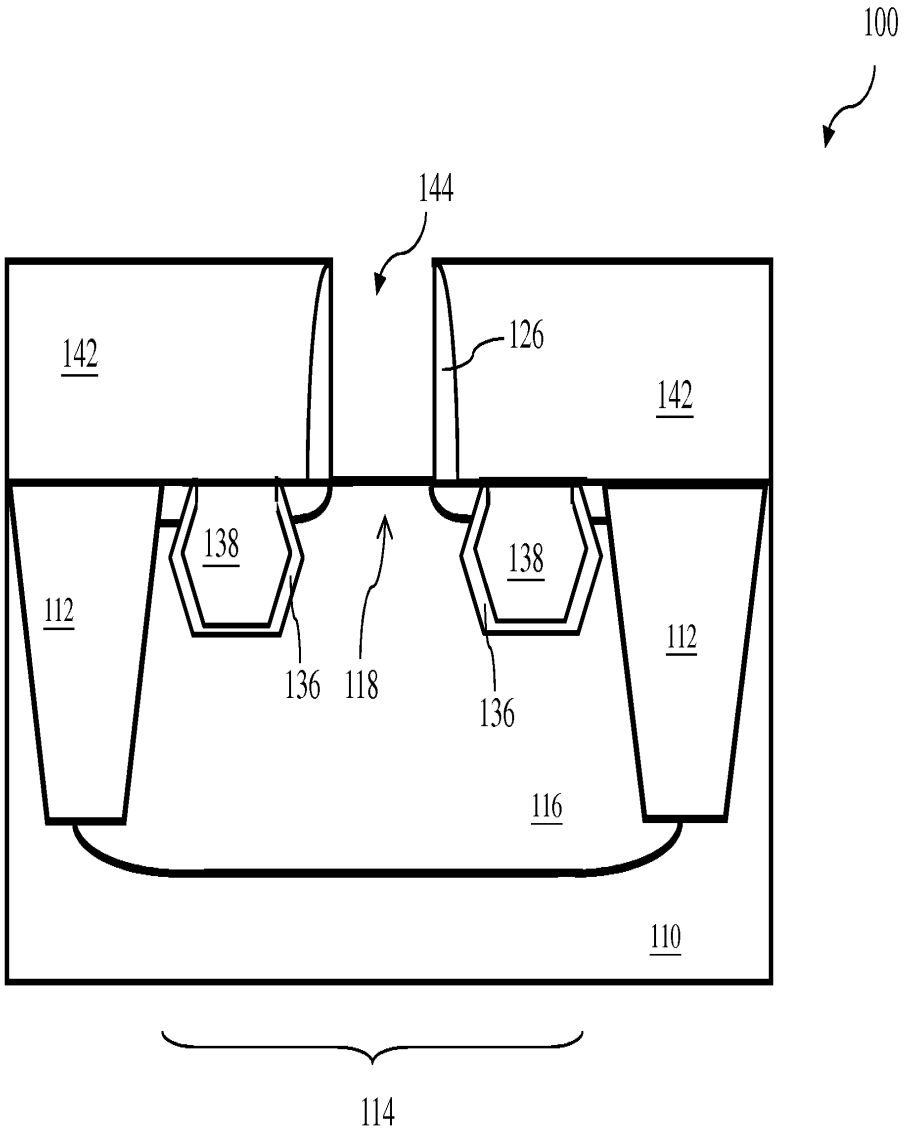


Fig. 7

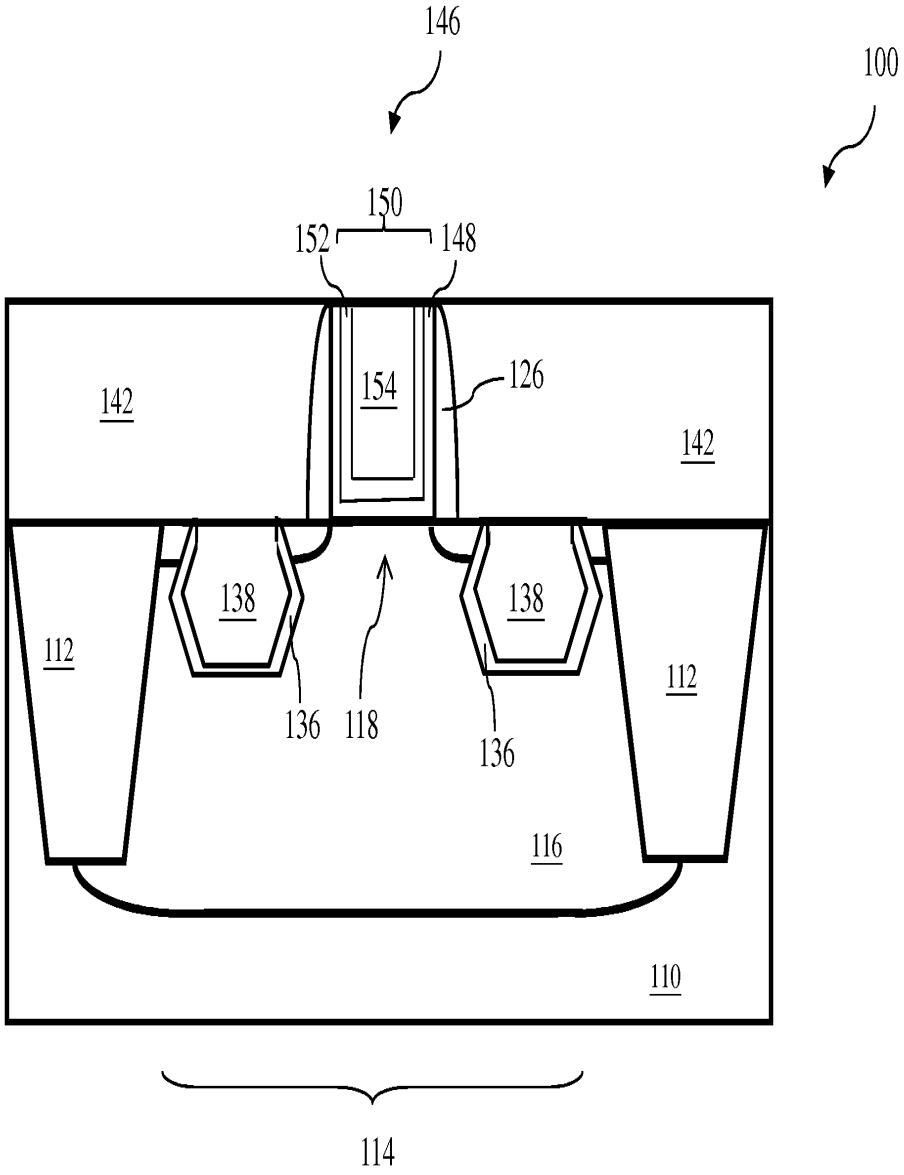

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Fig. 8A

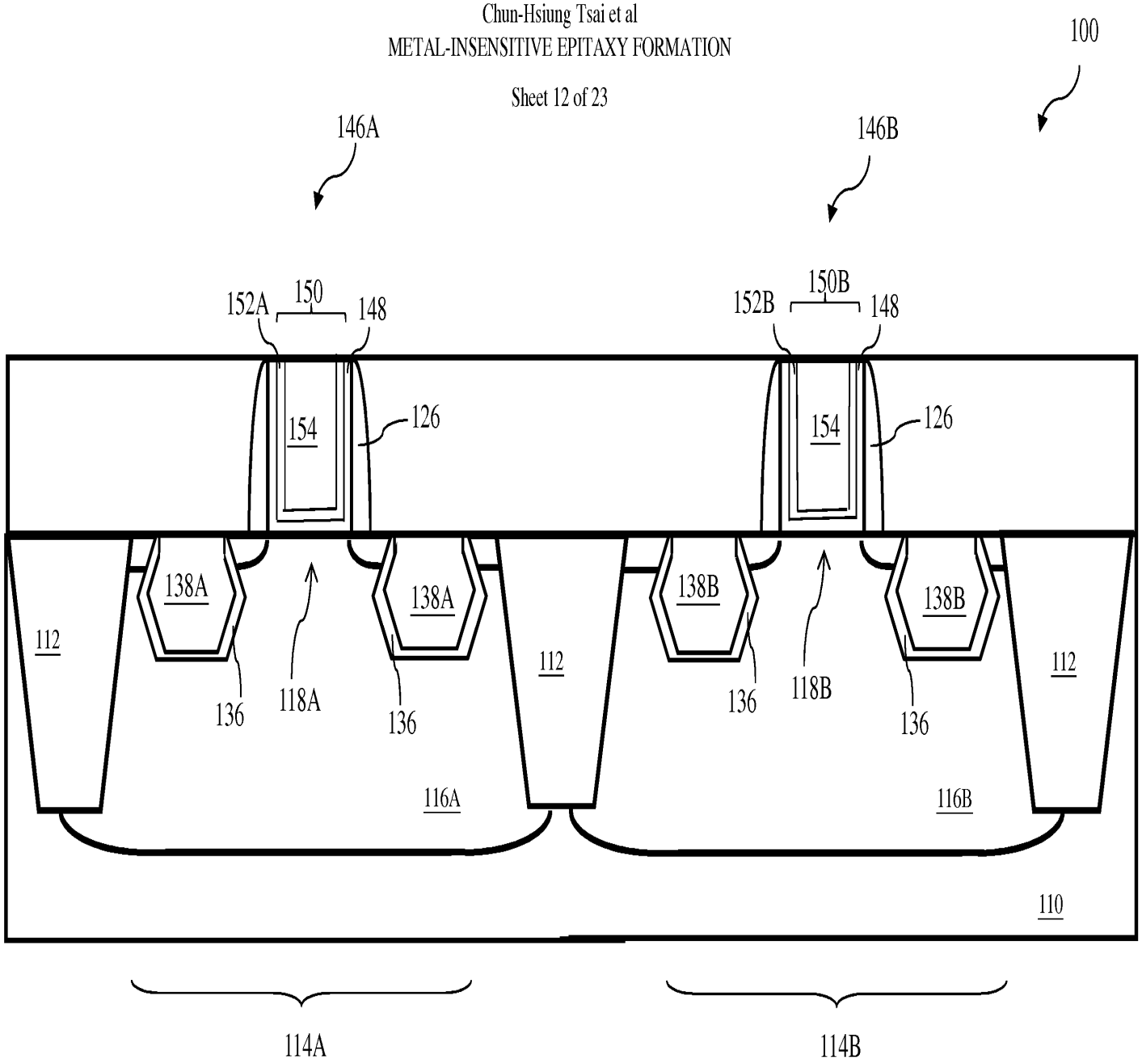

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Fig. 8B

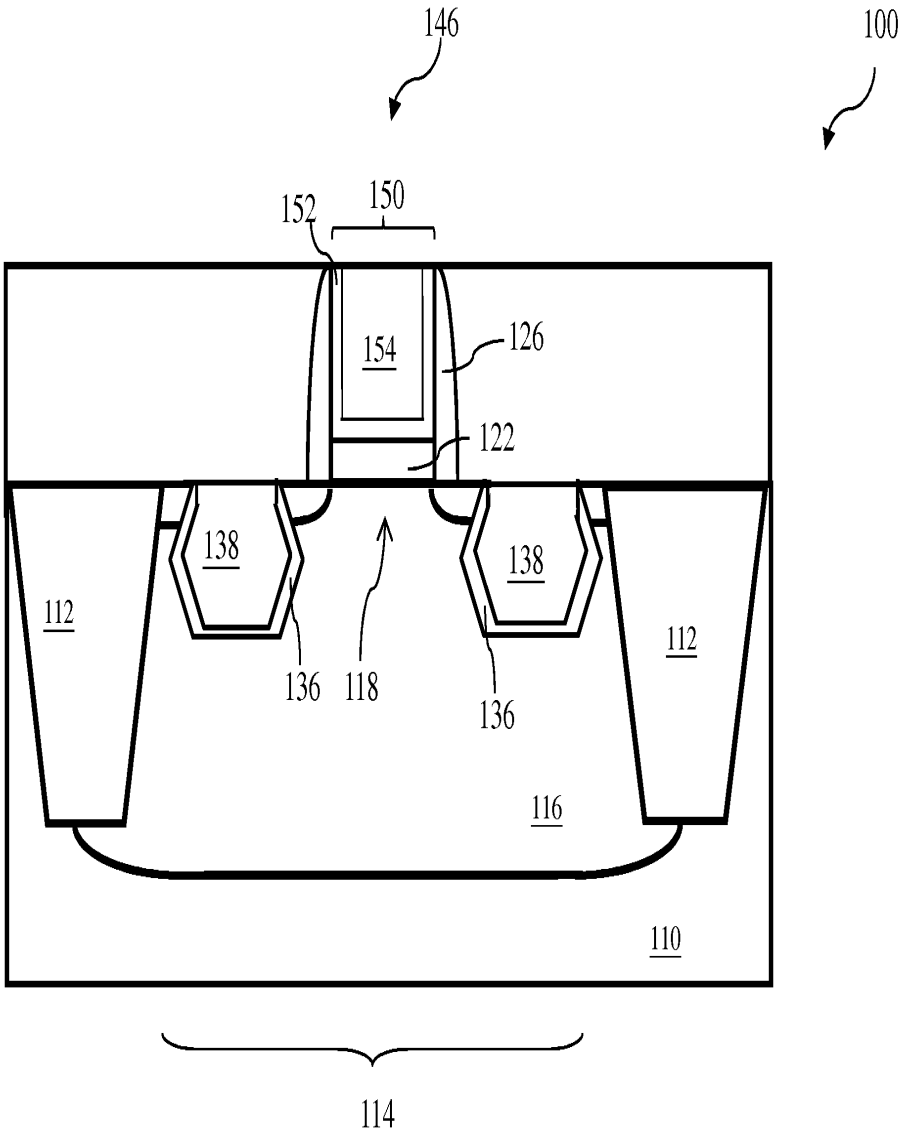

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Fig. 9

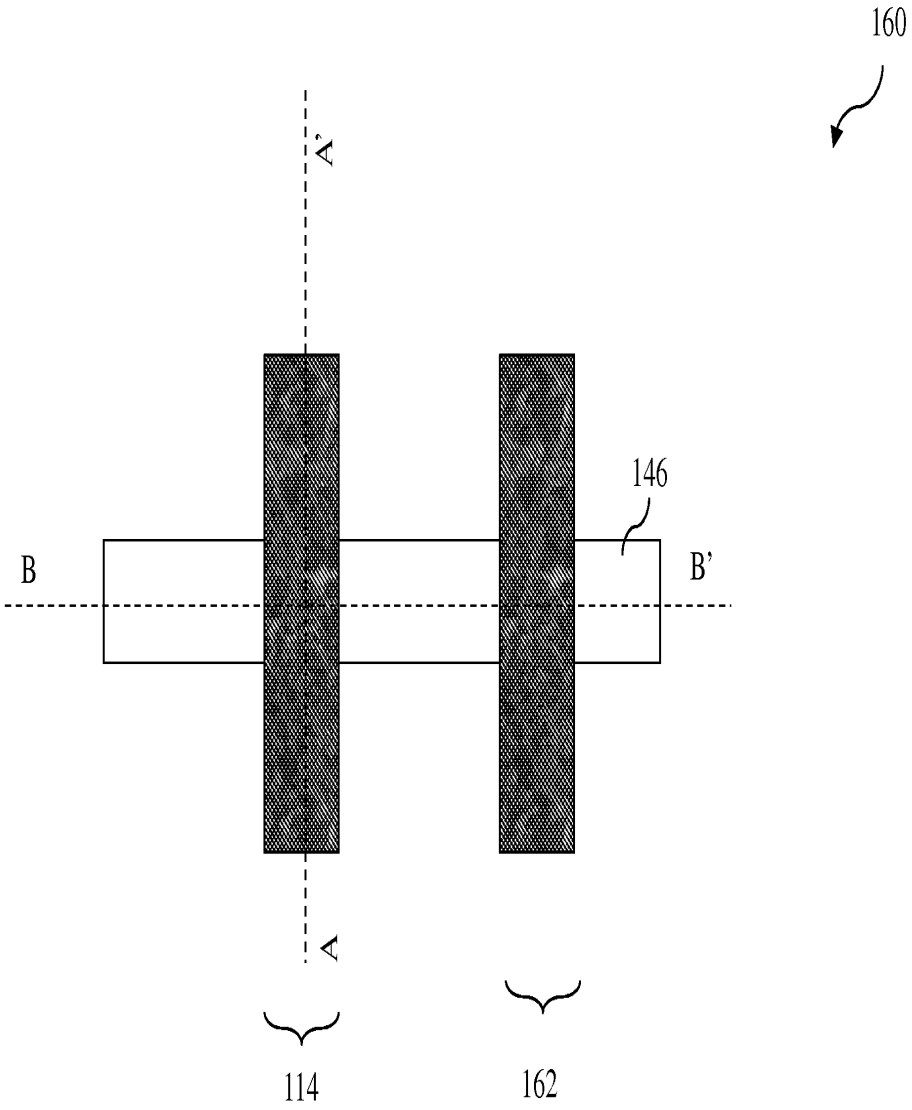


Fig. 10

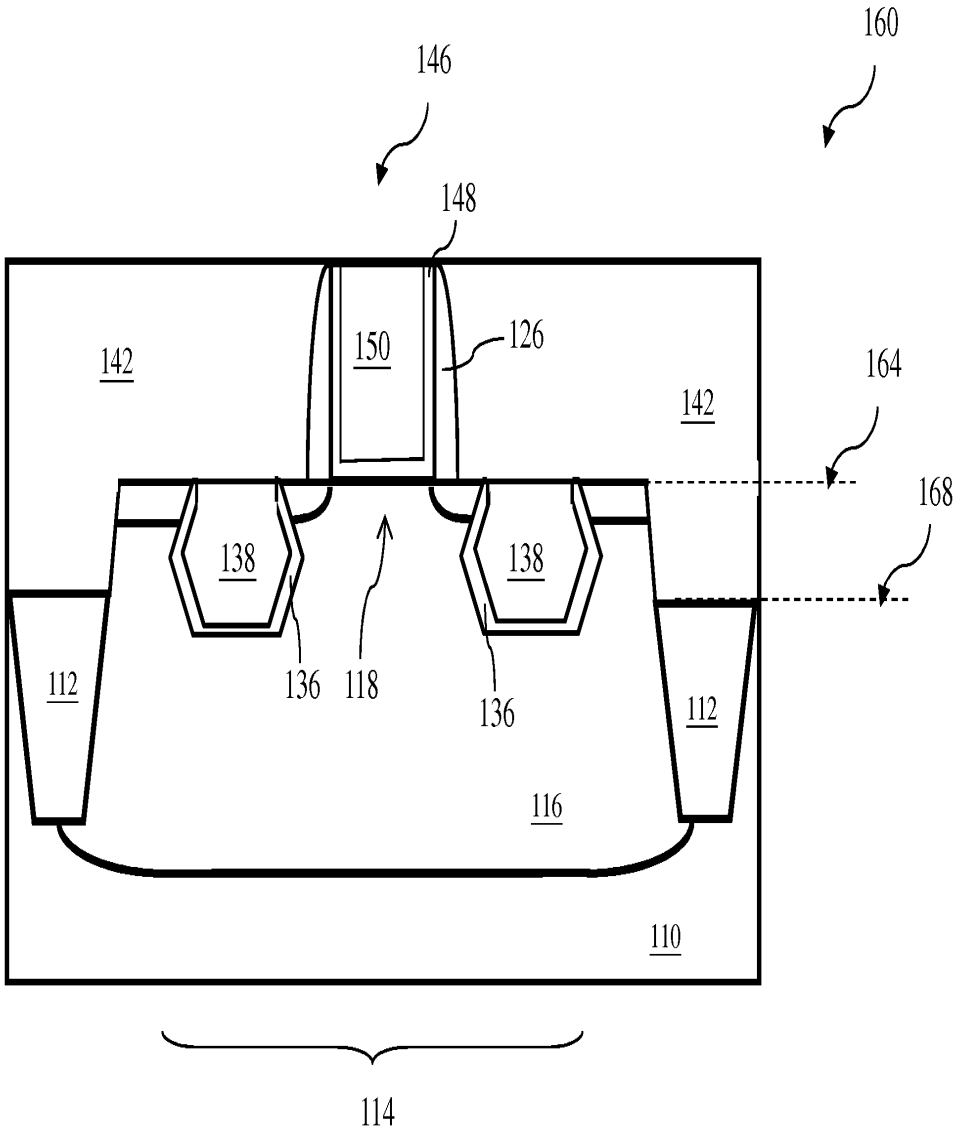

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Fig. 11

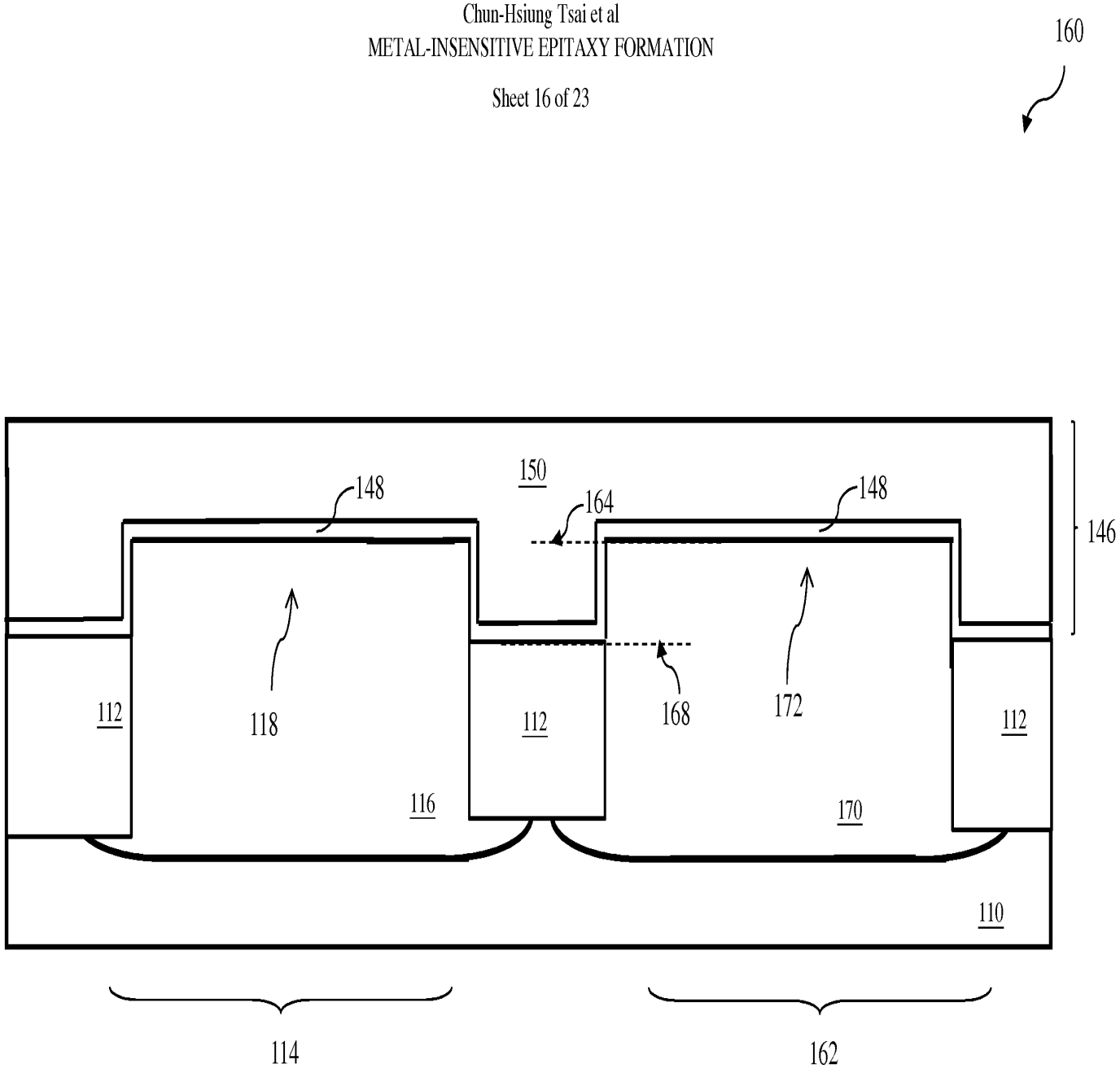

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Fig. 12

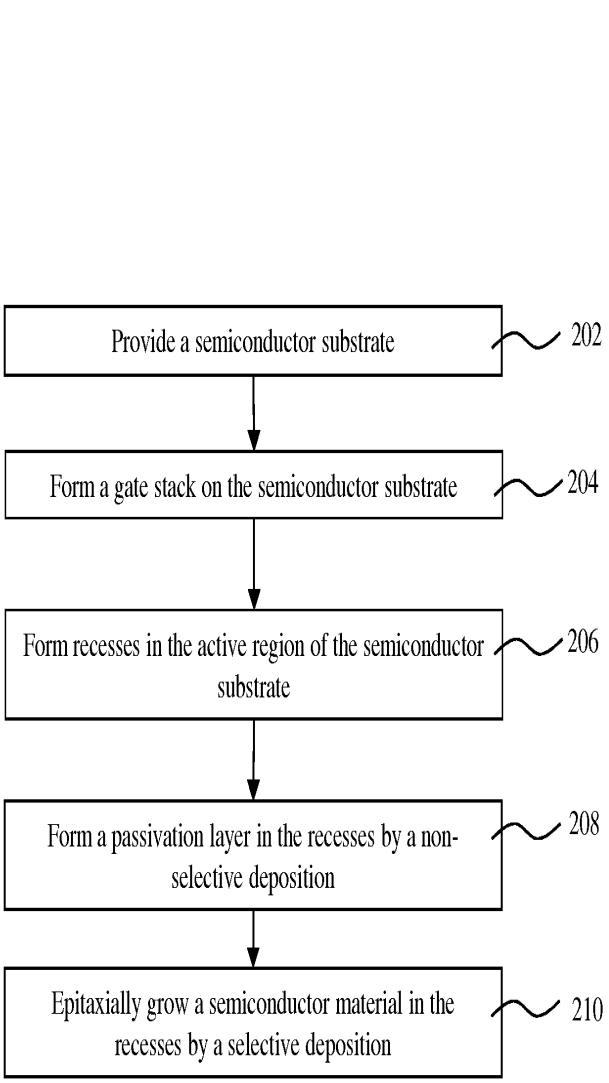

200
Provide a semiconductor substrate
202
Form a gate stack on the semiconductor substrate
204
Form recesses in the active region of the semiconductor substrate
206
Form a passivation layer in the recesses by a non-selective deposition
208
Epitaxially grow a semiconductor material in the recesses by a selective deposition
210

Fig. 13

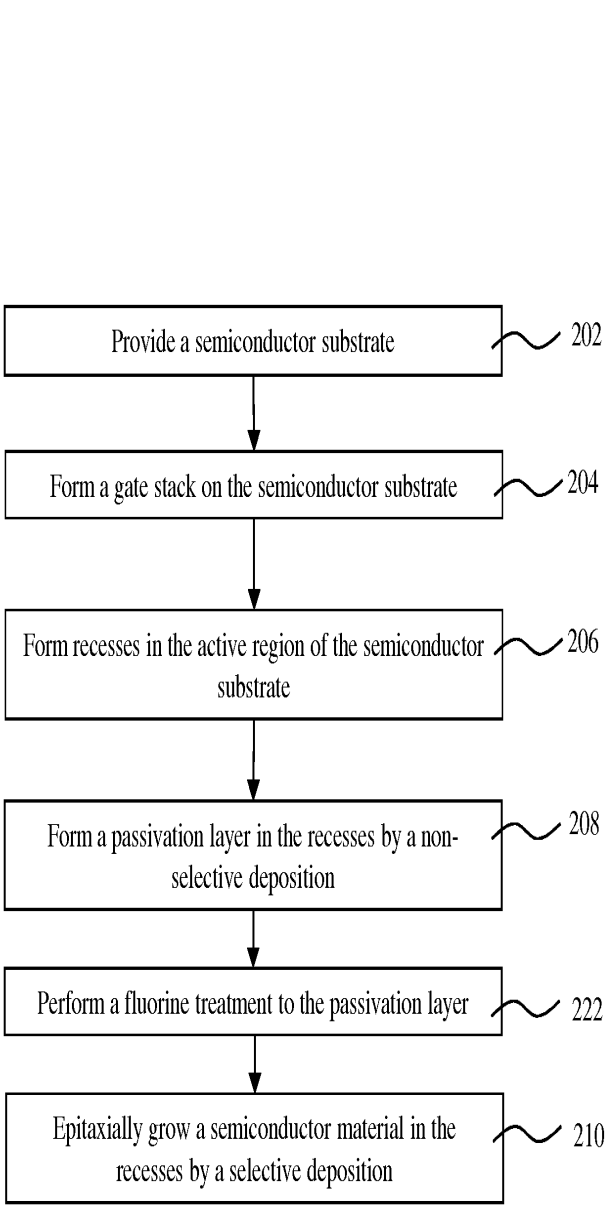

220
Provide a semiconductor substrate
202
Form a gate stack on the semiconductor substrate
204
Form recesses in the active region of the semiconductor substrate
206
Form a passivation layer in the recesses by a non-selective deposition
208
Perform a fluorine treatment to the passivation layer
222
Epitaxially grow a semiconductor material in the recesses by a selective deposition
210

Fig. 14

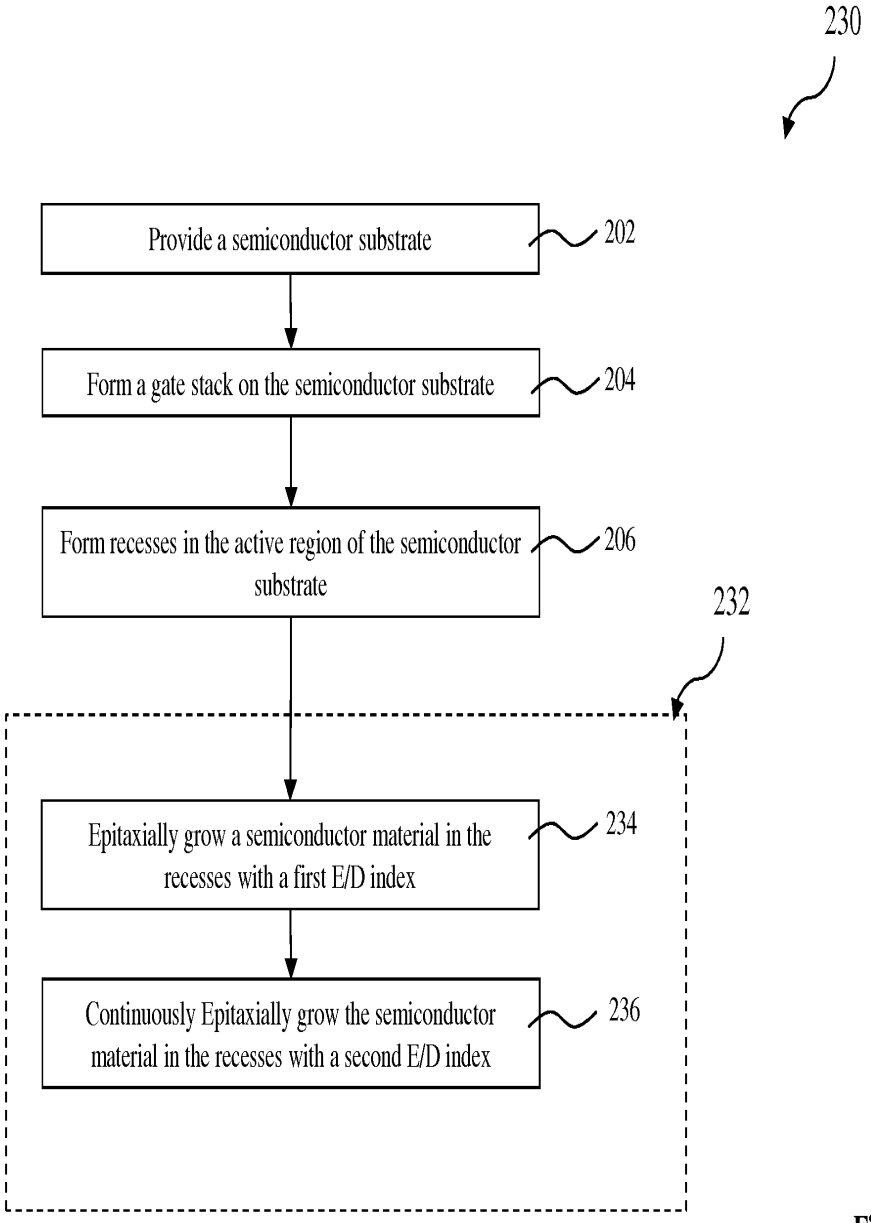

230
Provide a semiconductor substrate
202
Form a gate stack on the semiconductor substrate
204
Form recesses in the active region of the semiconductor substrate
206
232
Epitaxially grow a semiconductor material in the recesses with a first E/D index
234
Continuously Epitaxially grow the semiconductor material in the recesses with a second E/D index
236

Fig. 15

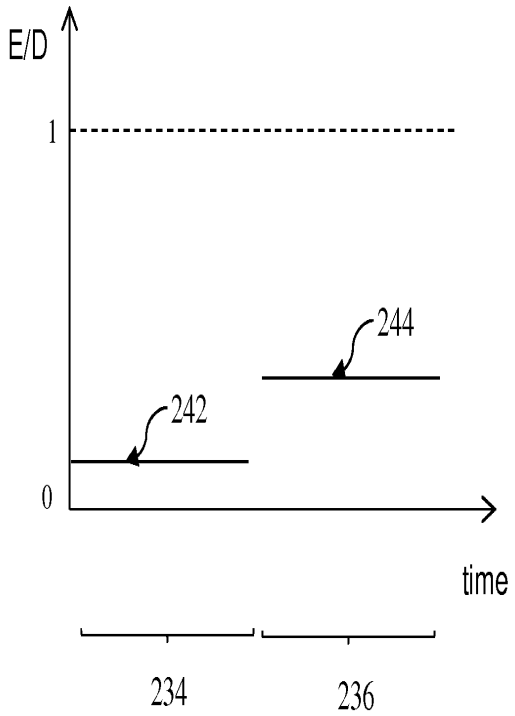


Fig. 16

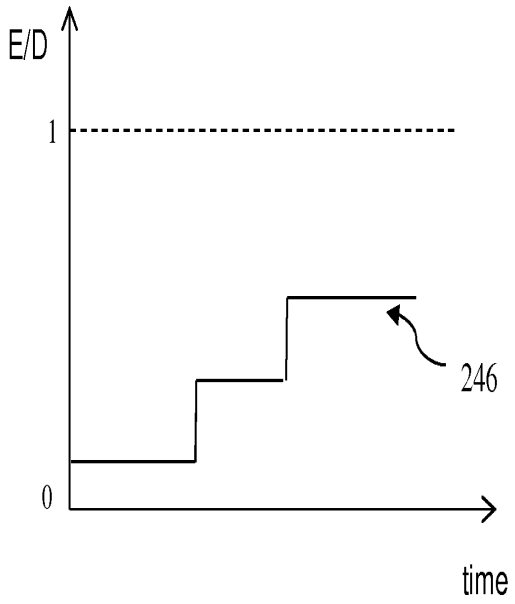


Fig. 17

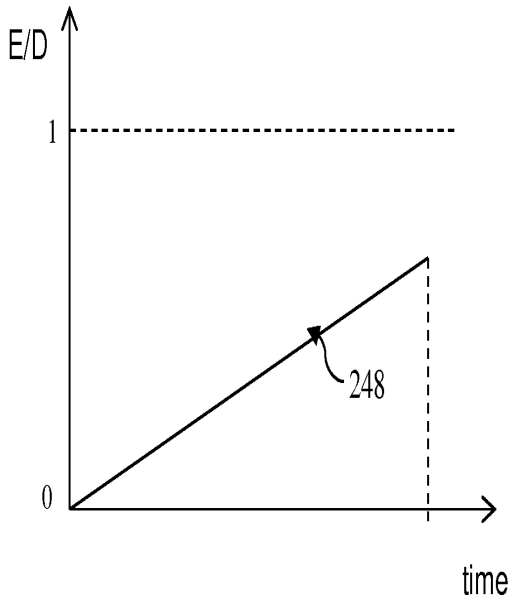


Fig. 18

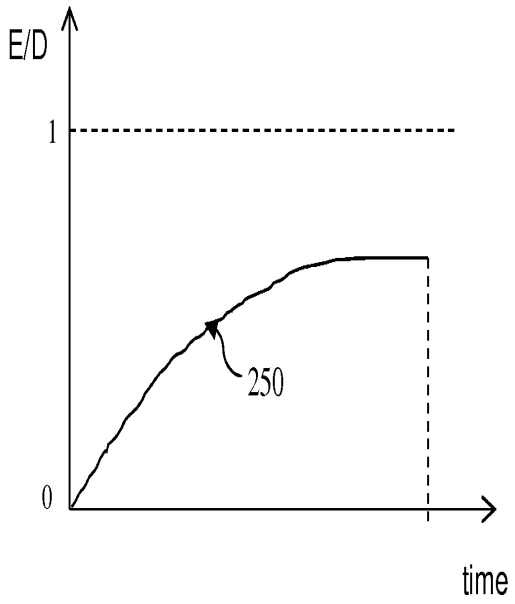


Fig. 19

Electronic Patent Application Fee Transmittal

Application Number:	
Filing Date:	
Title of Invention:	Metal-Insensitive Epitaxy Formation
First Named Inventor/Applicant Name:	Chun Hsiung Tsai
Filer:	David M. Odell/Linda Ingram
Attorney Docket Number:	2014-0937/24061.2998

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Utility application filing	1011	1	280	280
Utility Search Fee	1111	1	600	600
Utility Examination Fee	1311	1	720	720
Pages:				
Claims:				
Claims in Excess of 20	1202	6	80	480
Miscellaneous-Filing:				
Petition:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**2080**

Electronic Acknowledgement Receipt

EFS ID:	21213160
Application Number:	14597115
International Application Number:	
Confirmation Number:	8745
Title of Invention:	Metal-Insensitive Epitaxy Formation
First Named Inventor/Applicant Name:	Chun Hsiung Tsai
Customer Number:	42717
Filer:	David M. Odell/Linda Ingram
Filer Authorized By:	David M. Odell
Attorney Docket Number:	2014-0937/24061.2998
Receipt Date:	14-JAN-2015
Filing Date:	
Time Stamp:	19:25:18
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	$2080
RAM confirmation Number	5356
Deposit Account	081394
Authorized User	O'DELL, DAVID M.

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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		2998_Specification.pdf	171733 77d45e65753a116712d08e7d50fe293a9414ea21	yes	33

Multipart Description/PDF files in .zip description		
Document Description	**Start**	**End**
Specification	1	28
Claims	29	32
Abstract	33	33

Warnings:

Information:

2	Application Data Sheet	2998_ADS.pdf	1286116 9ad4e087be97f0faa674688c14fd36bc7dda6add	no	7

Warnings:

Information:

3	Authorization to access Appl. by Trilateral Office	2998_SB39.pdf	90113 70673e206cf97619d18a72ac04b34f1e37f4b97f	no	1

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Information:

4		2998_Declaration.pdf	55287 3cc5e0acc2796f20a0a881cf9459cde368b275d5	yes	2

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Oath or Declaration filed	1	1
Oath or Declaration filed	2	2

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Information:

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Document Description	**Start**	**End**
Transmittal Letter	1	1
Information Disclosure Statement (IDS) Form (SB08)	2	2

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Information:

6		2998_POA.pdf	371163 615484781de5d5dd0ab9fe9176919c23ce398cf7	yes	7

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Power of Attorney	1	2
Assignee showing of ownership per 37 CFR 3.73.	3	7

Warnings:

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7	Drawings-only black and white line drawings	2998_Drawings.pdf	207492 c84ff717818ffdbf545286929b77b03670098b89	no	23

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Information:

8	Fee Worksheet (SB06)	fee-info.pdf	36428 221f6f71b6a2ecc7442736eefc62fc1cbf811fd2	no	2

Warnings:

Information:

Total Files Size (in bytes):	2323742

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National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

METAL-INSENSITIVE EPITAXY FORMATION

BACKGROUND

[0001] This application claims the benefit of U.S. Provisional Application 62/040,880 entitled "METAL-INSENSITIVE EPITAXY FORMATION," filed August 22, 2014, herein incorporated by reference in its entirety.

[0002] The semiconductor industry has progressed into nanometer technology process nodes in pursuit of higher device density, higher performance, and lower cost. In the course of IC evolution, functional density (i.e., the number of interconnected devices per chip area) has generally increased while geometry size (i.e., the smallest component (or line) that can be created using a fabrication process) has decreased. This scaling down process generally provides benefits by increasing production efficiency and lowering associated costs. Despite groundbreaking advances in materials and fabrication, scaling planar device such as the conventional MOSFET has proven challenging. For example, such scaling-down also produces a relatively high power dissipation value. To overcome these challenges, IC industries look to novel structures and fabrication to deliver improved performance. One avenue of inquiry is the development of strained field effect transistor (FET) with enhanced mobility. However, the existing structure and fabrication method present issues associated with the metal contamination, which introduces device defects and other performance concerns.

[0003] Therefore, there is a need for a structure and method for a FET device to address these concerns for enhanced performance and reduced defects.

BRIEF DESCRIPTION OF THE DRAWINGS

[0004] Aspects of the present disclosure are best understood from the following detailed description when read with the accompanying figures. It is emphasized that, in accordance with the standard practice in the industry, various features are not drawn to scale. In fact, the dimensions of the various features may be arbitrarily increased or reduced for clarity of discussion.

[0005] Figs. 1A, 2, 3, 4A, 5A, 7 and 8A are sectional views of a semiconductor structure at various fabrication stages constructed in accordance with some embodiments.

[0006] Figs. 1B, 4B, 5B and 8B are sectional views of a semiconductor structure at various fabrication stages constructed in accordance with some other embodiments.

[0007] Fig. 6 is a sectional view of a semiconductor structure constructed according to other embodiments.

[0008] Fig. 9 is a sectional view of a semiconductor structure constructed according to other embodiments.

[0009] Fig. 10 is a top view of a semiconductor structure constructed in accordance with some embodiments.

[0010] Figs. 11-12 are sectional views of the semiconductor structure of Fig. 10 constructed in accordance with some embodiments.

[0011] Fig. 13 is a flowchart of a method making a semiconductor structure constructed according to various aspects of the present disclosure in some embodiments.

[0012] Fig. 14 is a flowchart of a method making a semiconductor structure constructed according to various aspects of the present disclosure in some other embodiments.

[0013] Fig. 15 is a flowchart of a method making a semiconductor structure constructed according to various aspects of the present disclosure in some other embodiments.

[0014] Fig. 16 illustrates a deposition process in the method of Fig. 15 and the corresponding E/D factor in accordance with some embodiments.

[0015] Fig. 17 illustrates a deposition process in the method of Fig. 15 and the corresponding E/D factor in accordance with some other embodiments.

[0016] Fig. 18 illustrates a deposition process in the method of Fig. 15 and the corresponding E/D factor in accordance with some other embodiments.

[0017] Fig. 19 illustrates a deposition process in the method of Fig. 15 and the corresponding E/D factor in accordance with some other embodiments.

DETAILED DESCRIPTION

[0018] It is to be understood that the following disclosure provides many different embodiments, or examples, for implementing different features of various embodiments. Specific examples of components and arrangements are described below to simplify the present disclosure. These are, of course, merely examples and are not intended to be limiting. In addition, the present disclosure may repeat reference numerals and/or letters in the various examples. This repetition is for the purpose of simplicity and clarity and does not in itself dictate a relationship between the various embodiments and/or configurations discussed. Moreover, the formation of a first feature over or on a second feature in the description that follows may include embodiments in which the first and second features are formed in direct contact, and may also include embodiments in which additional features may be formed interposing the first and second features, such that the first and second features may not be in direct contact.

[0019] Figs. 1A, 2, 3, 4A, 5A, 7 and 8A are sectional views of a semiconductor structure 100 at various fabrication stages constructed in accordance with some embodiments. Figs. 1B, 4B, 5B and 8A are sectional views of the semiconductor structure at various fabrication stages constructed in accordance with some other embodiments. The semiconductor structure 100 and the method making the same are collectively described in accordance with some embodiments. In one embodiment, the semiconductor structure 100 includes one or more field effect transistor (FET).

[0020] Referring to Fig. 1A, the semiconductor structure 100 includes a semiconductor substrate 110. The semiconductor substrate 110 includes silicon. Alternatively, the substrate includes germanium, silicon germanium or other proper semiconductor materials. In another embodiment, the semiconductor substrate 110 may include a buried dielectric material layer for isolation formed by a proper technology, such as a technology referred to as separation by implanted oxygen (SIMOX). In some embodiments, the substrate 110 may be a semiconductor on insulator, such as silicon on insulator (SOI).

[0021] As various examples for illustration, the semiconductor structure 100 includes other components or features. In some embodiments, isolation features, such as various shallow trench isolation (STI) features 112, are formed in the semiconductor substrate 110 and define various semiconductor regions (or active regions) 114. The semiconductor regions 114 are separated and isolated from each other by the STI features 112. In one example, the top surface of the semiconductor substrate 110 and the top surfaces of the STI features 112 may be coplanar, resulting in a common top surface. In another example, the top surface of the semiconductor substrate 110 and the top surfaces of the STI features 112 are not coplanar, resulting in a three-dimensional structure, such as a fin FET (FinFET) structure.

[0022] In some embodiments, the formation of the STI features 112 includes, forming a hard mask with openings that define the regions for STI features; etching the semiconductor substrate 110 through the openings of the hard mask to form trenches in the semiconductor substrate; depositing one or more dielectric material to fill in the trenches; and performing a chemical mechanical polishing (CMP) process. As one embodiment for illustration, the depth of the STI features 112 ranges between about 50 nm and about 500 nm. In one example, the formation of the hard mask includes depositing a hard mask layer; a lithography process to form a patterned resist layer on the hard mask layer; and etching the hard mask layer using the patterned resist layer as an etch mask. In some examples, the deposition of the dielectric material further includes thermal oxidation of the trenches and then filling in the trenches by the dielectric material, such as silicon oxide, by CVD. In one example, the CVD process to fill in the trenches includes high density plasma CVD (HDPCVD). In some embodiments, the formation of the STI features 112 further includes removing the hard mask after CMP. In another embodiment, the hard mask includes a silicon oxide layer by thermal oxidation and a silicon nitride on the silicon oxide layer by chemical vapor deposition (CVD).

[0023] In Fig. 1A, the active region 114 is designed to form a FET, such as a p-type FET (pFET) or an n-type FET (nFET). In some embodiments, a doped well 116 may be formed in one or more active region 114. In some examples, the doped well 116 includes an n-type dopant, such as phosphorous (P), distributed in an active region where a pFET is to be formed. The n-type dopant may be introduced to the n-well 116 through an opening of the mask layer by a suitable doping process, such as one or more ion implantation. In some other examples, the doped well 116 includes a p-type dopant, such as boron (B), distributed in an active region where

an nFET is to be formed. The p-type dopant may be introduced to the p-well 116 through an opening of the mask layer by a suitable doping process, such as one or more ion implantation. The STI features 112 further functions to define the dopants to the desired active regions. In the present example for illustration, the n-well 116 is formed in the semiconductor region 114. In one example, the doped well 116 may have a corresponding doping concentration ranging between about 10^{16} and 10^{18} cm^{-3}. In another example, the doped well 116 may have a depth ranging between about 0.5 micrometers and 2 micrometers. A channel region 118 is defined in the active region 114 and serves as a conductive path when the corresponding FET is turned on during operations.

[0024] The semiconductor structure 100 may include more active regions. As illustrated in Fig. 1B, the semiconductor structure 100 includes a first active region 114A and a second active region 114B, which are separated by one STI feature 112 in some examples. The first active region 114A is designed for an nFET to be formed thereon and the second active region 114B is designed for a pFET to be formed thereon. In this case, a p-type doped well 116A is formed in the first active region 114A for the nFET and an n-type doped well 116B is formed in the second active region 114B for the pFET by a suitable procedure. In some examples, the procedure may include covering the first active region with a first mask (hard mask or soft mask patterned by lithography process); performing a first ion implantation to the second active region with an n-type dopant using the first mask as implantation mask; covering the second active region with a second mask (hard mask or soft mask patterned by lithography process); and performing a second ion implantation to the first active region with a p-type dopant using the second mask as implantation mask. In the following description, one exemplary active region and one FET are usually present for simplicity. However, two exemplary active regions and two FETs are present in some figures, in order to describe different embodiments, such as a nFET and a pFET that are different in terms of composition, configuration and/or formation.

[0025] Referring to Fig. 2, a gate stack 120 is formed on the active region 114 and a channel region 118 is defined in the active region 114. The gate stack 120 is overlying the channel region 118 and is vertically aligned with the channel region 118. The gate stack 120 includes a gate dielectric feature 122 disposed on the semiconductor substrate 110 and a gate electrode 124 disposed on the gate dielectric feature 122. The semiconductor structure 100 may further include gate spacers 126 disposed on sidewalls of the gate stack 120.

[0026] The gate dielectric feature 122 includes a gate dielectric material, such as silicon oxide or a suitable dielectric material having a higher dielectric constant (high-k dielectric material). In the present embodiment, the gate dielectric feature 122 includes more than one dielectric material layers. For example, the gate dielectric feature 122 includes an interfacial dielectric layer, such as silicon oxide, and a high-k dielectric material layer on the interfacial layer.

[0027] The gate electrode 124 includes a conductive material layer, such as doped polysilicon, metal, metal alloy, metal silicide, or a combination thereof. In some embodiments, the gate electrode 124 includes more than one conductive material layers. For example, the gate electrode 124 includes a first conductive layer having a suitable work function on the gate dielectric feature 122 and a second conductive layer on the first conductive layer. In one example, the first conductive layer includes tantalum nitride or titanium nitride. In another example, the second conductive layer includes aluminum, tungsten, copper, doped polysilicon or a combination thereof.

[0028] The gate stack 120 is formed by a procedure that includes various deposition processes and patterning. The formation of the gate stack 120 is further described in accordance with some embodiments. In one embodiment, an interfacial layer is formed on the semiconductor substrate 110. The interfacial layer may include silicon oxide formed by a proper technique, such as an atomic layer deposition (ALD), thermal oxidation or UV-Ozone Oxidation. The interfacial layer may have a thickness less than 10 angstrom. A high k dielectric material layer is formed on the interfacial layer. The high-k dielectric layer includes a dielectric material having the dielectric constant higher than that of thermal silicon oxide, about 3.9. The high k dielectric material layer is formed by a suitable process such as ALD or other suitable technique. Other methods to form the high k dielectric material layer include metal organic chemical vapor deposition (MOCVD), physical vapor deposition (PVD), UV-Ozone Oxidation or molecular beam epitaxy (MBE). In one embodiment, the high k dielectric material includes HfO2. Alternatively, the high k dielectric material layer includes metal nitrides, metal silicates or other metal oxides. The interfacial layer and the high k dielectric material layer constitute the gate dielectric layer.

[0029] In some embodiments, the gate electrode 124 includes polysilicon. A polysilicon layer is formed on the gate dielectric layer by a proper technique, such as CVD. In one example, a

capping layer may be further formed between the high k dielectric material layer and the polysilicon layer by a proper technique, such as PVD. The capping layer may include titanium nitride (TiN), tantalum nitride (TaN) or a combination thereof in some examples. The capping layer may serve one or more functions, such as diffusion barrier, etch stop, and/or protection.

[0030] After the depositions, the gate material layers are patterned to form the gate stack 120 (or a plurality of gate stacks). The patterning of the gate stack 120 includes a lithography process and etching. A lithography process forms a patterned resist layer. In one example, the lithography process includes resist coating, soft baking, exposing, post-exposure baking (PEB), developing, and hard baking. The gate stack material layers are thereafter patterned by etching using the patterned resist layer as an etching mask. The etching process may include one or more etching steps. For example, multiple etching steps with different etchants may be applied to etch respective gate stack material layers.

[0031] In other embodiments, the patterning of the gate stack material layers may alternatively use a hard mask as an etching mask. The hard mask may include silicon nitride, silicon orynitride, silicon oxide, other suitable material, or a combination thereof. A hard mask layer is deposited on the gate stack material layers. A patterned resist layer is formed on the hard mask layer by a lithography process. Then, the hard mask is etched through the opening of the patterned resist layer, thereby forming a patterned hard mask. The patterned resist layer may be removed thereafter using a suitable process, such as wet stripping or plasma ashing.

[0032] The gate spacers 126 include a dielectric material and may have one or more films. In some embodiments, the fate spacers 126 include silicon oxide, silicon nitride, silicon oxynitride, other suitable dielectric material, or a combination thereof. The gate spacers 126 are formed by deposition and anisotropic etch (such as dry etch).

[0033] In some embodiments, the semiconductor structure 100 may include light-doped drain (LDD) features 128 formed in the active region 114 by a suitable process, such as ion implantation. The LDD features 128 have a doping type opposite to that of the doped well 116. For example for a pFET, the doped well 116 is n-type and the LDD features 128 are p-type. In another example for a nFET, the doped well 116 is p-type and the LDD features 128 are n-type. The LDD features 128, the dummy gate stack and gate spacers 126 may be formed in a collective

procedure. For examples, the gate stack material layers are deposited and patterned to form the dummy gate stack; the LDD features are formed by ion implantation using the dummy gate stack (and STI features) to constrain the LDD features; and then the spacers are formed. In other embodiments, the LDD features 128 are optional and may be eliminated from the semiconductor structure 100.

[0034] Referring to Fig. 3, recesses 132 are formed in the semiconductor substrate within the active region 114 by an operation that includes etching. In some embodiments, the recesses 132 may be formed using, such as a wet (and/or dry) etch process, selectively etch the material of the substrate 110. In furtherance of the embodiments, the gate stack 120, the gate spacers 126, and the STI 112 collectively function as an etching hard mask, thereby forming the recesses 132 in the source and drain regions. In some examples, an etchant such as carbon tetrafluoride (CF4), tetramethylammonium hydroxide (THMA), other suitable etchant, or a combination thereof is used to form the recesses 132. In some embodiments, the recesses 132 are formed with a width ranging from 50 Å and about 400 Å. A cleaning process may follow the etching process using a suitable chemical. The recesses 132 are substantially aligned with the gate structure, particularly aligned with outer edges of the gate spacers 126. As labeled in Fig. 3, the horizontal distance "D" is substantially zero in some examples. In some other examples, the distance "D" is greater than zero due to directionality of the etching process and/or the shadowing effect of the gate stacks 120 during the etching process. In some other examples when a wet etchant is used, lateral etch may additionally undercut the spacers 126. In this case, the distance "D" may be less than zero or negative, which means undercut. The recesses 132 may have different geometries, such as hexagonal, depending on design and tuning of the etching process. For example, a wet etching process is substantially non-directional isotropic but the etch rate is related to the crystal orientation of a substrate surface to be etched.

[0035] In experiments, it is found that the metal residuals, such as noble metals, may present in the recesses 132. The metal residuals may be introduced to the recesses during the operation to form the recesses 132, such as wet etch, dry etch, and/or cleaning process. The metal residuals are identified, through our experiments and failure mode analysis, to be the root cause of defects formed in the substrate 110 during subsequent operations to fill the recesses 132. In the present embodiments, the defects are formed through a mechanism of metal-assisted silicon etching.

When chlorine is involved in the subsequent operations for filling the recesses, the metal residuals function as catalyst during chlorine-containing etching. Particularly, the silicon beneath the noble metal is etched much faster than the silicon without noble metal coverage. As a result, the noble metal sinks into the silicon substrate, generating pores or rough profile in the substrate. This will introduce defects, such as micro-porous structures to the substrate. The present disclosed method and structure are designed to address the issues.

[0036] Referring to Fig. 4A, a passivation layer 136 is formed on the recesses 132 to cover the surfaces of the recesses 132. The passivation layer 136 is designed with composition and thickness to effectively isolate the metal residuals from the chlorine chemical during the subsequent operations. The passivation layer 136 effectively eliminates (or substantially reduces) the metal assisted silicon etching, and accordingly eliminates the formation of the associated defects. In some embodiments, the passivation layer 136 includes carbon, germanium, silicon carbide or silicon germanium. The passivation layer 136 is epitaxially grown on the surfaces of the recesses 132 and so is in crystalline structure. Thus, the subsequent operations can epitaxially grow on the passivation layer 136 and fill the recesses 132 with a semiconductor material in crystalline structure. During the formation of the passivation layer 136, the precursor is free of chlorine (Cl) to avoid direct reaction between chlorine and the metal residuals. Since the precursor is free of chlorine, the formation of the passivation layer 136 does not involve etching and is nonselective. The passivation layer 136 may also be formed on other regions, such as on the gate stack and STI features. Those unexpected portions of the passivation layer in other regions will be removed by subsequent operations, such as deposition and etching process to fill the recesses. In some examples, the passivation layer 136 includes silicon or silicon carbide formed by a deposition with a precursor free of Cl. In some embodiments, the passivation layer 136 has a thickness ranging from about 1 nm to about 4 nm.

[0037] In one embodiment, the passivation layer 136 is a silicon carbide layer formed by a suitable process, such as CVD process, that epitaxially grows a silicon carbide layer using a precursor free of Cl. In furtherance of the embodiment, the precursor includes monomethylsilane (CH_3SiH_3 or MMS) and silane (SiH_4). The silicon-containing chemical in the precursor may alternatively include disilane (SiH_6), trisilane (Si_3H_8), other suitable silicon-containing chemical or a combination thereof. In some examples, the precursor is free of chlorine. In the present

example, the precursor is further free of dopant-containing chemical (free of phosphorous or other n-type dopant) as well. The passivation layer 136 is designed to be effective for diffusion prevention and inertness to etching. As an example for illustration, phosphorous isanother issue in addition to the metal-assistant silicon etching. The phosphorous diffusion leads to the leakage and further leads to the degradation of device performance. The dopant-free precursor and corresponding dopant-free passivation layer 136 formed thereby address the above issues. In another examples, the precursor is provided with proper gas flows and partial pressures such that the epitaxially grown passivation layer 136 of SiC has a carbon concentration ranging from about 1.8% to about 3% (atomic percentage). The SiC layer with such low carbon concentration is not suitable for strain effect but is more effective as the passivation layer for isolating and preventing diffusion. In yet some examples, the passivation layer 136 is formed in both the recesses for nFET S/D regions and the recesses for pFET S/D regions, such as illustrated in Fig. 4B. In Fig. 4B, the first active region 114A is for an nFET and the second active region 114B is for a pFET. In some examples, the passivation layer 136 is dopant-free; has a carbon concentration ranging from about 1.8% to about 3% (atomic percentage); and is formed in formed in both the recesses for nFET S/D regions and the recesses for pFET S/D regions.

[0038] In some embodiment, the passivation layer 136 is a silicon carbide layer formed by a suitable process, such as CVD process. The SiC passivation layer 136 includes phosphorous (P) dopant with a low P doping concentration less than $1\times10^{20}/cm^3$, or $0 \sim 1\times10^{20}/cm^3$. The P dopant may be introduced by in-situ doping. During the epitaxial growth of the passivation layer 136, the precursor further includes phosphorous-containing chemical, such as phosphine (PH_3). The P concentration in the SiC passivation layer 136 may be not enough for S/D features. S/D features of a nFET may have a P dopant concentration greater than $1\times10^{20}/cm^3$. The P concentration of the SiC passivation layer 136 is so tuned such that to provide a grading P concentration with smooth transition from the substrate to the S/D features and the P concentration is not too high to cause leakage concerns.

[0039] In some embodiments, the passivation layer 136 is a silicon layer formed by epitaxially growing a silicon layer using a precursor free of Cl. In furtherance of the embodiment, the precursor includes SiH_4 or other silicon-containing chemical. In the present embodiment, the precursor has no dopant (free of phosphorous and boron-containing chemical)

to prevent dopant diffusion. Accordingly, the corresponding silicon passivation layer 136 is dopant-free. In some examples, the precursor during the epitaxy growth has a low partial pressure ranging from about 1 Torr to about 10 Torr.

[0040] In some embodiments, the passivation layer 136 is a silicon germanium (SiGe) layer formed by epitaxially growing a silicon germanium layer using a precursor free of Cl. In furtherance of the embodiment, the precursor includes a silicon-containing chemical (such as SiH_4) and a germanium-containing chemical (GeH_4). In the present embodiment, the precursor has no dopant (free of phosphorous and boron-containing chemical) to prevent dopant diffusion. Accordingly, the corresponding SiGe passivation layer 136 is dopant-free (free of boron or other p-type dopant). In some examples, the SiGe passivation layer 136 has a Ge concentration ranging from about 10% to about 40% for enhanced effectiveness of the passivation layer 136. In yet some examples, the SiGe passivation layer 136 is formed in both the recesses for nFET S/D regions and the recesses for pFET S/D regions, such as illustrated in Fig. 4B. In Fig. 4B, the first active region 114A is for an nFET and the second active region 114B is for a pFET. In some examples, the SiGe passivation layer 136 is dopant-free; has a germanium concentration ranging from about 10% to about 40% (atomic percentage); and is formed in formed in both the recesses for nFET S/D regions and the recesses for pFET S/D regions. In some examples, the precursor during the epitaxy growth has a low partial pressure ranging from about 1 Torr to about 10 Torr.

[0041] In some embodiments, a fluorine (F) treatment is further applied to the passivation layer 136. Fluorine has strong interaction with silicon of the passivation layer 136 by forming F-Si bonds), thereby reducing dangling bonds. As the passivation layer is thus enhanced and certain damage to the active regions is also reduced. In some examples, the F treatment is a fluorine plasma treatment. Particularly, fluorine plasma is generated and is introduced to the passivation layer 136 in a plasma chamber. In further examples, the fluorine dose of the fluorine treatment ranges from about 1×10^{14} to about 2×10^{15} ions/cm^2. Accordingly, thus formed passivation layer 136 a semiconductor layer (such as Si, SiC or SiGe as described above in various embodiments) has a fluorine concentration ranging from about 1×10^{14} to about 2×10^{15} cm^{-2}. Note that the F concentration is defined as a number of fluorine atoms per unit area in the present example. In other examples, the F treatment includes applies a bias voltage ranging from

0.5 keV to about 5 keV. In some examples, the F treatment is executed in the same apparatus used to form the passivation layer 136.

[0042] Referring to Fig. 5A, the recesses 132 are filled with a semiconductor material by a selective deposition process, thereby epitaxially growing source and drain (S/D) features 138 in crystalline structure. The deposition process to form the S/D features 138 involves chlorine for etching effect and makes the deposition selective. The selective deposition process is designed and tuned to epitaxially grow such that the S/D features 138 formed in the recesses 132 include the semiconductor material in a crystalline structure. The semiconductor material is different from that of the substrate 110. For example, the semiconductor material includes silicon carbide or silicon germanium while the substrate 110 is a silicon substrate. In some embodiments, the semiconductor material is chosen for proper strained effect in the channel region 118 such that the corresponding carrier mobility is increased. In one example, the active region 114 is for a pFET, the semiconductor material is silicon germanium doped with boron for S/D features 138 while the substrate 110 is a silicon substrate. In another example, the active region 114 is for an nFET, the semiconductor material is silicon carbide doped with phosphorous for S/D features 138 while the substrate 110 is a silicon substrate.

[0043] This is further illustrated in Fig. 5B in accordance with some embodiments. The semiconductor structure 100 includes the first active regions 114A for a nFET and the second active region 114B for a pFET. The semiconductor structure 100 further includes the p-type doped well 116A in the first active region 114A and the n-type doped well 116B in the second active region 114B for the pFET. The semiconductor structure 100 further includes the first gate stack 120A and the second gate stack 120B, disposed within the first and second active regions, respectively. Particularly, the S/D features 138A are silicon carbide doped with phosphorous (SiC-P), providing tensile stress to the channel region 118A of the nFET, according to one embodiment. In another embodiment, the S/D features 138B are silicon germanium doped with boron (SiGe-B), providing compressive stress to the channel region 118B of the pFET. In some other embodiments, the S/D features 138A of SiC-P and the S/D features 138B of SiGe-P are both present in the semiconductor structure 100 and are formed respectively by a suitable procedure. In one example, the procedure includes covering the first active region 114A using a first mask while epitaxially growing SiGe-B in the recesses of the second active region 114B and

covering the second active region 114B using a second mask while epitaxially growing SiC-P in the recesses of the first active region 114A. The first and second masks may be patterned resist layers formed by lithography or alternatively hard masks formed by deposition and lithohraphy patterning. In yet other embodiments, the S/D features 138A are SiC-P while the S/D features 138B are silicon doped with boron (Si-B) or the S/D features 138A are silicon doped with phosphorous (Si-P) while the S/D features 138B are SiGe-B.

[0044] Still referring to Fig. 5B, while the S/D features 138A and 138B are different as described above, the passivation layer 136 is same to both active regions 114A and 114B in terms of composition and formation, in accordance with some embodiments, such as those in Fig. 4B. In one example, the passivation layer 136 includes a phosphorous-free SiC layer with a carbon concentration ranging from about 1.8% to about 3%. In furtherance of the example, the S/D features 138A include SiC-P (or Si-P) while the S/D features 138B may include SiGe-B (or Si-B). In another example, the passivation layer 136 includes a SiC-P layer with a phosphorous concentration less than $10^{-20}/cm^3$ and the S/D features 138A include SiC-P with a phosphorous concentration greater than $10^{-20}/cm^3$. In yet another example, the passivation layer 136 is a SiGe layer free of boron or other p-type dopant.

[0045] Still referring to Fig. 5B, the first gate electrode 124A and the second gate electrode 124B may be same in composition (such as polysilicon) or alternatively different (such as the first gate electrode 124A includes a n-type work function metal layer and the second gate electrode 124B includes a p-type work function metal layer), such as in a gate-first process to form metal gates.

[0046] The operation to form the S/D features is further described according to various embodiments. In some embodiments, the selective deposition process to form the S/D features 138 in the recesses 132 is a cyclic deposition and etching (CDE) process. The semiconductor material is epitaxially grown in the recesses 132. In the present embodiment, the S/D features 138 are in-situ doped during the CDE process with precursor that includes dopant-containing chemical. The CDE process is a two-cycle operation with a precursor having chlorine for deposition/etching effects so that the semiconductor material is selectively deposited in the recesses 132. In the first cycle (deposition cycle), the various chemicals are used as precursor to epitaxially grow the semiconductor material. In the second cycle (etching cycle), chlorine-

containing gas (such as HCl, Cl2 or both) is used for etching. The CDE process repeats the two cycles until the recesses 132 are filled or alternatively overgrowing beyond the top surface of the substrate 110.

[0047] In some embodiments when an nFET is formed in the active region 114 in Fig. 5A (or 114A in Fig. 5B), the semiconductor material is silicon carbide with phosphorous (P) dopant. In furtherance of the embodiments, the precursor used in the first cycle (deposition cycle) of the CDE process includes SiH_4 (and/or Si_2H_6), PH_3, and MMS. The second cycle (etching cycle) includes HCl or Cl_2. In one example, the HCl is provided with a processing chamber pressure ranging from about 200 Torr to about 250 Torr.

[0048] In some other embodiments when a pFET is formed in the active region 114 in Fig. 5 (or 114B in Fig. 5B), the semiconductor material is silicon germanium with boron (B) dopant. In furtherance of the embodiments, the precursor used in the first cycle (deposition cycle) of the CDE process includes SiH_4 (and/or Si_2H_6), B_2H_6, and GeH_4. The second cycle (etching cycle) includes HCl or Cl_2. In one example, the HCl is provided with a processing chamber pressure ranging from about 200 Torr to about 250 Torr.

[0049] In some embodiments, the precursor used in the deposition cycle may alterantively includes other silicon-containing chemical, such as silane (SiH_4), disilane ($Si2H_6$), trisilane (Si_3H_8), dichlorosilane (SiH_2Cl_2), another silicon-containing precursor, or a combination thereof.

[0050] In some embodiments, the operation to form the S/D features 138 may alternatively use other deposition technique, such as a deposition process that the deposition gas (chemicals for deposition) and etching gas (chlorine-containing gas, such as Cl2 or HCl) are simultaneously flown to the processing chamber. Instead of two cycles, the operation is a continuous deposition/etching process that epitaxially grows the semiconductor material selectively in the recesses 132. Thus, the disclosed deposition of the semiconductor material to the recesses 132 is insensitive to the metal residuals, eliminating the metal assisted silicon etching issue and the associated defects. The deposition process is referred to as selective epitaxy growth (SEG) with co-flow deposition & etches chemicals, or simply referred to as co-flow epitaxy growth (or co-flow epitaxy deposition).

[0051] In some embodiments, the S/D features may be formed by a combination of CDE and co-flow epitaxy growth. The S/D features 138A may include SiC-P with graded phosphorous concentration formed by two or more steps of CDE and co-flow eptaxy growth. For example, the the S/D features 138A incudes first SiC-P layer; a second SiC-P layer on the first SiC-P layer; and a third SiC-P layer on the second SiC-P layer with respective dopant concentrations. In a particular example, the S/D features 138A include the first SiC-P layer with a first phosphorous concentration ranging from about $10^{20}/cm^3$ to about $4\times10^{20}/cm^3$ formed by a CDE process with in-situ doping; the second SiC-P layer with a second phosphorous concentration ranging from about $4\times10^{20}/cm^3$ to about $10^{21}/cm^3$ formed by a co-flow epitaxy growth with in-situ doping; and the third SiC-P layer with a third phosphorous concentration ranging from about $10^{21}/cm^3$ to about $3\times10^{21}/cm^3$ formed by another co-flow epitaxy growth with in-situ doping. In furtherance of the example, the first, second and third SiC-P layers have thicknesses 10 nm ~ 20 nm; 10 nm ~ 20 nm; and 5 nm ~ 15 nm, respectively.

[0052] In some embodiments, the S/D features 138 are formed in the recesses 132 such that the recesses 132 are substantially filled with a top surface substantially coplanar to the substrate 110 (particularly, coplanar with the top surface of the channel region 118, such as illustrated in Fig. 5A or Fig. 5B. The S/D features 138 may have other alternatives in terms of composition, geometry and formation. As illustrated in Fig. 6, the S/D features 138 are over grown in the recesses 132 beyond the top surface of the channel region 118.

[0053] The semiconductor structure 100 may include other features formed by corresponding operations. In one embodiment, an interlayer dielectric (ILD) layer is formed by a deposition technique, such as chemical vapor deposition CVD and CMP. In another embodiment, an interconnect structure is formed and include various conductive features (such as metal lines, contact features and via features) configured to couple various devices to form a functional circuit.

[0054] In other embodiments, the gate stack 120 is a dummy gate and is replaced by a gate stack having metal electrode and high-k dielectric in a gate replacement procedure, such as a gate-last process or a high-k last process. In a gate-last process, an interlayer dielectric (ILD) material layer is formed on the substrate and surrounding the gate stack 120, by deposition and

polishing (e.g., CMP). The gate electrode in the dummy gate is removed by selective etching, resulting in a gate trench in the ILD. Thereafter, a final gate stack is formed in the gate trench of the ILD by a suitable procedure, such as deposition and CMP. A high-k-last process is similar to the gate-last process but the gate dielectric of the dummy gate is treated differently. In the high-k-last process, the dummy gate stack (including both gate dielectric and gate electrode) is removed after the ILD formation. Thereafter, a final gate stack is formed in the gate trench of the ILD.

[0055] One embodiment of the gate replacement is provided in Figs. 7 and 8A for illustration. An ILD layer 142 is formed on the substrate 110 and surrounding the dummy gate stack 120, by deposition and polishing (e.g., CMP). The ILD material layer 142 includes one or more dielectric m materials, such as silicon oxide, fluorinated silica glass (FSG), low-k dielectric material or other suitable dielectric material. The deposition may include CVD or plasma-enhanced CVD or other suitable deposition technique. The dummy gate stack 120 is removed by selective etching, resulting in a gate trench 144 in the ILD material layer 142. Thereafter, a gate stack 146 of high k dielectric and metal electrode is formed in the gate trench 144 by a suitable procedure that includes deposition and CMP. Thus formed gate 146 includes gate dielectric 148 and metal gate electrode 150. In a particular example, the gate dielectric 148 includes an interfacial layer of silicon oxide and a high-k dielectric layer on the interfacial layer.

[0056] The metal gate electrode 150 includes a metal layer 152 has a proper work function (a metal with a work function less than about 4.2 eV for nFET or greater than about 5.2 eV for pFET), such as tantalum for nFET and titanium nitride for pFET. The metal layer 152 is also referred to as work function (WF) layer, or particularly n-type WF layer or p-type WF layer. The gate electrode 150 may include multiple conductive layers. For example, the gate electrode 150 includes the WF layer 152 on the gate dielectric feature 148 and a conductive layer 154 on the WF layer 152. In one example, the WF layer 152 includes tantalum or titanium nitride. In another example, the conductive layer 154 includes aluminum, tungsten, copper, doped polysilicon or a combination thereof. When the gate stack 146 is formed by a high-k last process, the gate dielectric layer 148 is formed on bottom and sidewalls of the gate trench 144, or is U-shaped in other words.

[0057] Thus formed semiconductor structure 100 includes a gate stack, epiaxially grown S/D features of a semiconductor material different from that of the substrate; and a passivation layer disposed surrounding the S/D features and separating the S/D features from the substrate. The passivation layer effectively prevents the metal residual from direct contact with the Cl-containing chemical during the operations to form the S/D features, thereby eliminating the defects associated with the interaction between Cl and the metal residuals.

[0058] Fig. 8B illustrates a sectional view of the semiconductor structure 100 that includes a first FET of a first conductivity and a second FET of second conductivity opposite to the first conductivity. The first conductivity is one of a n-type conductivity and a p-type conductivity and the second conductivity is another one. For example, the first and second FETs are nFET and pFET, respectively. The semiconductor structure 100 in Fig. 8B includes a first metal gate stack 146A disposed on the first active region 114A for nFET and a second metal gate stack 146B disposed on the second active region 114B for pFET. The first metal gate stack 146A and the second metal gate stack 146B are both metal gate stacks formed by high-k last process. In the present embodiment, the first metal gate stack 146A and the second metal gate stack 146B are different from each other in composition. Particularly, the first metal gate stack 146A includes a n-type WF layer 152A having a work function less than about 4.2 eV (such tantalum) and a p-type WF layer 152B having a work function greater than about 5.2 eV (such as tantalum nitride). In one example of a procedure to form the metal gate stacks, the first gate stack 146A is formed within the first active region 114A while the second active region 114B is covered by a mask (such as a patterned resist layer or a patterned hard mask layer), and the second gate stack 146B is formed within the second active region 114B while the first active region 114A is covered by another mask.

[0059] Fig. 9 illustrates a sectional view of the semiconductor structure 100 in accordance with other embodiments. The semiconductor structure 100 in Fig. 9 is similar to that in Fig. 8A except for that the metal gate stack 146 is formed by a gate last process. Particularly, the gate dielectric layer 120 is formed before the formation of the ILD layer 142 and therefore is not formed on the sidewalls of the gate trench 144.

[0060] As noted above, the described semiconductor structure 100 may be formed on a planar substrate or alternatively on a non-planar substrate, such as a substrate having fin-like active region(s). Figs. 10-12 illustrate the semiconductor structure 160 having fin-like active regions, constructed according to various aspects of the present disclosure in some embodiments. Fig. 10 is a top view of the semiconductor structure 160. Fig. 11 is a sectional view of the semiconductor structure 160 along the dashed line AA' and Fig. 12 is a sectional view of the semiconductor structure 160 along the dashed line BB'. The semiconductor structure 160 includes a first fin-like active region 114 and a second fin-like active region 162 separated isolation features 112, such as STI features. The semiconductor structure 160 further includes a gate stack 146 formed over the first and second fin-like active regions.

[0061] For a fin-like active region, the top surface 164 of the semiconductor substrate 110 (specifically the top surface of the channel region 118) and the top surfaces 168 of the STI features 112 are not coplanar, resulting in a three-dimensional structure. A FET formed on a fin-like active region is also referred to as a fin FET (FinFET). As illustrated in Fig. 11, the active region 114 is extruded above the top surface 168 of the STI features 112. The fin-like active regions are formed by a suitable technique, such as etching or epitaxy growth. In one example, after the formation of STI features 112, an etching process, such as wet etching, is applied to selectively etch the STI such that the STI features 112 are recessed. In another example, after the formation of STI features 112, a selective epitaxy growth process is applied to epitaxially grow a semiconductor material on the semiconductor substrate 110 such that the active region 114 is extended vertically above the top surface of the STI features 112. The semiconductor material of the fin active regions may be same to that of the semiconductor substrate, such as silicon, or alternatively different from that of the semiconductor substrate, such as silicon germanium. As illustrated in Fig. 12, the second fin active region 162 includes a doped well 170 and a channel region 172 formed in the doped well channel region. The gate stack 146 includes gate dielectric 148 and a gate electrode 150 formed by any proper procedure, such as gate-last process or high-k last process. Even though the fin-like active regions are illustrated in Figs. 10-12, various embodiments of the semiconductor structure 100 illustrated in Fig. 1A through 9 may also embrace a fin structure having fin-like active region(s) and FinFET(s).

[0062] Fig.13 is a flowchart of a method 200 to form a semiconductor structure (such as 100 or 160) constructed according to various aspects of the present disclosure in some embodiments. The method 200 is described with reference to Fig. 8 and other figures. However, the semiconductor structure 100 is provided as an example and is not intended to limit the scope of the method. The method 200 includes a block 202 by providing a semiconductor substrate 110, such as a silicon wafer. The semiconductor substrate 110 may further include other features/components, such as doped well 116 and STI 112.

[0063] The method 200 also includes an operation 204 to form gate stack 120. The formation of the gate stack includes various depositions and patterning. Other features, such as gate spacers 126 and LDD features 128 may be further formed.

[0064] The method 200 includes an operation 206 by forming recesses 132. The recesses 132 are formed in the semiconductor substrate within the active region 114 by an operation that includes etching. In some embodiments, the recesses 132 may be formed using, such as a wet (and/or dry) etch process selective to the material of the substrate 110. A cleaning process may follow the etching process using a suitable chemical. The etching and/or cleaning processes may introduce metal residuals to the recesses 132.

[0065] The method 200 includes an operation 208 by forming a passivation layer 136. The passivation material layer 136 is formed to cover the substrate 110 and is designed with composition and thickness to effectively isolate the metal residuals from the chlorine chemical during the subsequent operations, thereby eliminating the metal assisted silicon etching and eliminating the formation of the associated defects. In some embodiments, the passivation layer 136 includes carbon, germanium, silicon carbide or silicon germanium, such as those described in Fig. 4A. The passivation layer 136 is epitaxially grown on the substrate 110 and is formed by a non-selective epitaxy growth using a chlorine-free precursor. Note that the passivation layer 136 may be formed on other regions (such as on STI features and/or on gate stack) with non-crystalline structure but those portions of the passivation layer 136 will eventually be removed, such as during the next operation 210. Thus, the passivation layer 136 within the recesses 132 is in crystalline structure so that the subsequent operations can epitaxially grow and fill the recesses 132 to from S/D features in crystalline structure. During the formation of the passivation layer 136, the precursor is free of chlorine (Cl) to avoid direct reaction between Cl and the metal residuals. Since the precursor is free of Cl, the deposition is nonselective and may also be formed

on other regions, such as on the gate stack and STI features. In some examples, the passivation layer 136 includes silicon or silicon carbide formed by a deposition with precursor free of Cl. In some embodiments, the passivation layer 136 has a thickness ranging from about 1 nm to about 4 nm.

[0066] In one embodiment, the passivation layer 136 is a silicon carbide layer formed by epitaxially growing a silicon carbide layer using a precursor free of Cl. In furtherance of the embodiment, the precursor includes monomethylsilane (CH_3SiH_3 or MMS) and SiH4. The passivation layer 136 may include a mono layer or multiple layers. In the present example, the precursor is further free of dopant (such as free of phosphorous) to prevent dopant diffusion. In this case, the passivation layer 136 is free of chlorine and dopant. In some embodiments, the precursor is tuned (by controlling gas flows for examples) to form a SiC layer.

[0067] In alternative embodiment, the passivation layer 136 is a silicon layer formed by epitaxially growing a silicon layer using a precursor free of Cl. In furtherance of the embodiment, the precursor includes SiH_4. The passivation layer may include a mono layer or multiple layers. In the present embodiment, the precursor includes no dopant (such as phosphorous or boron-containing chemical) to prevent dopant diffusion. In some other embodiments, the passivation layer 136 may include is a germanium layer or a silicon germanium layer.

[0068] The method 200 includes an operation 210 to form S/D feature 138 by epitaxial growing in the recesses 132 with a semiconductor material different from that of the substrate 110 for strain effect. The operation 210 involves chlorine for etching effect and therefore is selective. The deposition occurs on the substrate 110 and also on other regions (such as STI and gate stacks) with different deposition rates and structures. The chlorine-containing gas provides etching effect such that the semiconductor material deposited on the other regions (such as on STI features and/or gate stack) is completely removed, making the operation 210 a selective deposition. The semiconductor material deposited in the recesses 132 is crystalline since the passivation layer 136 is crystalline and serves as a seed layer for epitaxy growth.

[0069] In some embodiments, the operation 210 includes a CDE process. The recesses 132 are filled with the semiconductor material by a CDE process, thereby forming S/D features 138. The semiconductor material is different from that of the substrate 110. For example, the semiconductor material includes silicon carbide or silicon germanium while the substrate 110 is

a silicon substrate. In the present embodiment, the source and drain features 138 are in-situ doped during the CDE process during the CDE process with precursor that includes dopant-containing chemical. The CDE process is a two cycle operation. In the first cycle for deposition, various chemicals are used as precursor to epitaxially grow the semiconductor material. In the second cycle, a chlorine-containing gas (such as HCl, Cl_2 or both) is used for etching. The CDE process repeats the two cycles until the recesses 132 are filled or alternatively overgrowing beyond the top surface of the substrate 110.

[0070] In some embodiments when an nFET is formed in the active region 114, the semiconductor material is silicon carbide with phosphorous (P) dopant. In furtherance of the embodiments, the precursor used in the first cycle (deposition cycle) of the CDE process includes SiH_4 (and/or Si_2H_6), PH_3, and MMS. The second cycle (etching cycle) includes HCl or Cl_2. In one example, the HCl is provided with a processing chamber pressure ranging from about 200 Torr to about 250 Torr.

[0071] In some other embodiments when a pFET is formed in the active region 114, the semiconductor material is silicon germanium with boron (B) dopant. In furtherance of the embodiments, the precursor used in the first cycle (deposition cycle) of the CDE process includes SiH_4 (and/or Si_2H_6), B_2H_6, and GeH_4. The second cycle (etching cycle) includes HCl or Cl_2. In one example, the HCl is provided with a processing chamber pressure ranging from about 200 Torr to about 250 Torr.

[0072] In some embodiments, the precursor used in the deposition cycle includes silane, disilane, trisilane, Dichlorosilane ($SiH2Cl_2$), another silicon-containing precursor, and/or any combinations thereof.

[0073] In some embodiments, the operation 210 may use a co-low deposition process. In the co-flow epitaxy growth, the chemicals for deposition and chlorine-containing gas are simultaneously flown to the processing chamber for continuous and simultaneous deposition/etching effect. The chemicals for deposition and the chlorine-containing gas are similar to those used in the CDE process.

[0074] Other fabrication steps may be implemented before, during and after the operations of the method. In one embodiment, an inter-level dielectric (ILD) layer is formed on the semiconductor substrate. The ILD layer includes silicon oxide, low k dielectric material, other suitable dielectric materials, or combinations thereof. The ILD layer is formed by a suitable

technique, such as CVD. For example, high density plasma CVD may be implemented to form the ILD layer.

[0075] In another embodiment, the method further includes a procedure to form various interconnection features designed to couple various devices to form a functional circuit. The interconnection features include vertical interconnects, such as contacts and vias, and horizontal interconnects, such as metal lines. The various interconnection features may use various conductive materials including copper, tungsten and silicide. In one example, a damascene process is used to form copper-based multilayer interconnection structure. In another embodiment, tungsten is used to form tungsten plug in the contact holes. In another example, silicide is used to form various contact on source and drain regions for reduced contact resistance.

[0076] Fig. 14 is a flowchart of a method 220 to form a semiconductor structure constructed according to various aspects of the present disclosure in some other embodiments. The method 220 is similar to the method 200. However, the method 220 further includes an operation 222 implemented between the operations 208 and 210. The operation 222 includes applying a fluorine treatment process to the passivation layer 136. In some embodiments, the F treatment is a fluorine plasma treatment. Particularly, fluorine plasma is generated in a plasma chamber and is introduced to the passivation layer 136. In further examples, the fluorine dose of the fluorine treatment ranges from about 1×10^{14} to 2×10^{15} ions/cm^2. Accordingly, thus formed passivation layer 136 a semiconductor layer (such as Si, SiC or SiGe as described above in various embodiments) has a fluorine concentration ranging from about 1×10^{14} to 2×10^{15} cm^{-2}. In other examples, the F treatment includes applies a bias voltage ranging from 0.5 keV to about 5 keV. In some examples, the F treatment is executed in the same apparatus used to form the passivation layer 136. Fluorine has a strong interaction with silicon and forms F-Si bonds, reduces the dangling bonds, and therefore reducing/eliminating subsequent damages to the substrate, particularly the portions underlying the passivation layer 136. After the F treatment to the passivation layer 136, the method 220 proceeds to the operation 210 by epitaxially growing a semiconductor material in the recesses 132.

[0077] Fig. 15 is a flowchart of a method 230 to form a semiconductor structure constructed according to various aspects of the present disclosure in some other embodiments. The method 230 is designed to form epitaxy grown S/D features while the metal assisted silicon etching

effect and the associated defects are eliminated or substantially reduced. The method 230 includes blocks 202-206 similar to those of the method 200.

[0078] After the formation of the recesses 132 in the substrate 110 by the operation 206, the method 230 proceeds to an operation 232 to form the S/D features 138 in the recesses 132. The operation 232 includes an epitaxy deposition with a varying etching/deposition factor. Particularly, the operation 232 epitaxially grows a semiconductor material in the recesses 132 with both deposition and etching effects. During the operation 232, a chlorine-containing gas (such as Cl2 or HCl) is introduced into the processing chamber for etching effect, thus making the epitaxy deposition selective (selectively growing on a substrate 110). In various embodiments, the operation 232 includes a CDE process, a co-flow epitaxy growth, or a combination thereof. Various aspects of the CDE and co-flow epitaxy growth are described above and are not repeated here. An etching/deposition (E/D) factor is introduced and defined to characterize the epitaxy deposition 232. The E/D factor is defined as a ratio of the etch amount over the deposition amount to the semiconductor substrate during a certain process time. The E/D factor ranges from 0 to a value less than 1. The epitaxy deposition 232 is implemented in a way such that the E/D factor varies over the epitaxy deposition process, particularly increases over the process. The epitaxy deposition 232 and the E/D factor are further described below in accordance with some embodiments.

[0079] As described above with the method 200, a CDE process includes a deposition cycle (or D cycle) and an etching cycle (or E cycle) repeated multiple times. The E/D factor is variable by varying one or more parameters, such as processing temperature, gas flow, gas partial pressure, E cycle duration, D cycle duration, a ratio of E cycles over D cycles, or a combination thereof. In one embodiment, the duration of D cycle and the duration of E cycles (or a ratio of D duration over E duration) are tuned to vary the E/D factor. As an example for illustration, a CDE process may have 15 second deposition and then 10 second etching for one E/D factor, or have 10 second deposition and then 6 second etching for another E/D factor. In another embodiment, the number of E cycles and the number D cycles (or a ratio of E cycles over D cycles) are tuned to vary the E/F factor. As an example for illustration, a CDE process may have 2 deposition cycles and 1 etching cycle for one E/D factor, or have 1 deposition cycle and 1 etching cycle for another E/D factor. In another embodiment, the substrate temperature is varied to vary the E/D factor. In an example for illustration, during an etching cycle of the CDE process, the substrate

temperature is decreased to reduce the etching effect, therefore decreasing the E/D factor. In another embodiment, the E/D factor is tuned by reducing the deposition gas pressure (or deposition gas flow rate) to increase the E/D factor. In yet another embodiment, the E/D factor is tuned by reducing the etching gas pressure (or etching gas flow rate) to decrease the E/D factor.

[0080] In a co-flow epitaxy growth, the E/D factor is varied similarly. In one embodiment, the substrate temperature is varied to vary the E/D factor. For example, the etching effect is apparent only when the substrate temperature is at or greater than 620 C. When the substrate temperature is increased to above 620 C, thereby increasing the etching effect, therefore increasing the E/D factor. In another embodiment, the E/D factor is tuned by reducing the deposition gas partial pressure (or deposition gas flow rate) to increase the E/D factor. In yet another embodiment, the E/D factor is tuned by reducing the etching gas partial pressure (or etching gas flow rate) to decrease the E/D factor.

[0081] In the operation 210 of the method 200, the E/D factor in the corresponding CDE process or co-flow epitaxy growth is a constant over the process. In the operation 232, the E/D factor is a varying parameter that increases over the process. Initially, the E/D factor is less enough such that the metal assisted silicon etching is eliminated or substantially reduced. Then, the E/D factor is increased over the process time, thereby making the epitaxy process 232 selective.

[0082] In some embodiments, the epitaxy deposition process in the operation 232 includes a first deposition step 234 having a first E/D factor and a second deposition step 236 having a second E/D factor. It is further illustrated in Fig. 15. At the first deposition step 234, the epitaxy deposition process is controlled to have the first E/D factor 242 that is chosen to substantially reduce the chlorine and reduces the interaction between the chlorine and the metal residuals. The first E/D factor 242 ranges from zero to about 0.2 in some examples. The first deposition step 234 is not selective. At the second deposition step 236, the second E/D factor 244 is tuned such that the epitaxy deposition process selectively deposits on the substrate 110. The second E/D factor 244 is greater than the first E/D factor 242. The second E/D factor 244 ranges from about 0.2 to about 0.5 in some examples. Note the deposition at the first deposition step 234 is not selective or has no enough selectivity. Any unexpected deposition to other regions (such as STI

features and gate stack) during the first deposition step will be removed during the second deposition step due to the increased etching effect.

[0083] In the operation 232, the corresponding deposition technique may be a CDE process, co-flow epitaxy growth or a combination. In some other embodiments, as long as the two deposition steps are tuned to address the metal related defects and deposition selectivity, the deposition gas (not etching gas) may include chlorinated chemical. For example, the SiH_2Cl_2 may be used as a silicon-containing gas in the operation 232.

[0084] In some examples, the epitaxy deposition process 232 is a CDE process. The first deposition step 234 has a HCl (or Cl_2) partial pressure less than 100 Torr for the etch cycle(s) while the second deposition step 236 has a HCl (or Cl_2) partial pressure greater than 100 Torr for the etch cycle(s). In some other examples, the epitaxy deposition process 232 is a co-flow epitaxy epitaxy growth. The first deposition step 234 has a HCl (or Cl_2) partial pressure less than 3 Torr while the second deposition step 236 has a HCl (or Cl_2) partial pressure greater than 3 Torr.

[0085] In some other examples, the epitaxy deposition process 232 is a co-flow epitaxy growth (or a CDE process). The E/D factor is tuned by the substrate temperature. As noted above, the etch effect is apparent when the substrate temperature is greater than 620 C. The first deposition step 234 has a first substrate temperature less than about 620 C and the second deposition step 236 has a second substrate temperature greater than 620 C.

[0086] In some other embodiments, the operation 232 uses a co-flow epitaxy growth that with two steps: a first deposition step 234 with a first E/D factor and a second deposition step 236 with a second E/D factor greater than the first E/D factor. During the co-flow epitaxy growth, the deposition gas and etching gas are dynamically controlled, such as by controlling gas flow rates, to dynamically change the E/D factor with considerations similar to those described with the CDE process. For example, the etching gas flow rate is initially zero or lower. Then the etch gas flow rate increases over processing time. At the first deposition step 234, the chlorine (e.g., HCl) gas partial pressure in the processing chamber is low, such as ranging from about 1 Torr to about 10 Torr in some examples. At the second deposition step 236, the chlorine gas partial pressure in the processing chamber is greater than that of the first deposition step 225, such as ranging from about 200 Torr to about 250 Torr in some examples.

[0087] In some other embodiments, the epitaxy deposition process 232 is designed such that the E/D factor has a step-wise variation over the process. As illustrated in Fig. 17, the E/D factor 246 is step-wise over the process time. Again, the variation of the E/D factor may be implemented through one or more mechanisms, such as gas flow, gas partial pressure, and substrate temperature. The deposition mechanism may be CDE, co-flow epiatxy growth or a combination.

[0088] In some embodiments, the operation 232 is designed such that the E/D factor varies continuously over the process. The E/D factor varies in a range from 0 to 1. During the operation 232, the E/D factor dynamically changes for various considerations that include the deposition selectivity, the metal assisted silicon etching issues and/or deposition quality. Initially, the metal assisted silicon etching issues is the prime concern, so the E/D factor is chosen to be lower. At the later stage of the operation 232, the deposition selectivity is a dominant while the metal assisted silicon etching issue is subordinate. Therefore, the E/D factor is increased. The E/D factor may be is a proper function of the process time, such as a linear function or a non-linear function. Illustrated in Fig. 18 is an example that the E/D factor 248 is a linear function of the process time. Illustrated in Fig. 19 is another example that the E/D factor 250 is a non-linear function of the process time. It may be tuned and optimized for better fabrication result in consideration of various factors, such as the semiconductor material to be deposited, processing throughput, and device tolerance range to the defects associated with the metal assisted silicon etching effect.

[0089] Other fabrication steps may be implemented before, during and after the operations of the method. In one embodiment, an inter-level dielectric (ILD) layer is formed on the semiconductor substrate. The ILD layer includes silicon oxide, low k dielectric material, other suitable dielectric materials, or combinations thereof. The ILD layer is formed by a suitable technique, such as CVD. For example, high density plasma CVD may be implemented to form the ILD layer. In another embodiment, a gate replacement procedure may be implemented to form a final gate stack having high k dielectric and metal gate electrode. In another embodiment, the method further includes a procedure to form various interconnection features designed to couple various devices to form a functional circuit.

[0090] The present disclosure provides a method and structure of a FET that addressing the defect issue associated with the metal residuals and chlorine. The method includes forming a

passivation layer in the recesses of the semiconductor substrate before expitaxially growing a semiconductor material to form S/D features in the recesses. The passivation layer is designed with composition, thickness and configuration to effectively prevent the interaction between Cl-containing chemical and the metal residual in the recesses. In other embodiments, a fluorine treatment is further applied to the passivation layer to enhance its effectiveness. In other embodiments, the method implements a deposition method to epitaxially growing S/D features with a varying E/D factor. The E/D factor varies over the processing time to address the defect issue associated with the metal residuals and chlorine. The E/D factor is chosen to be lower initially to address the defect issue, and then is increased over time to enhance the deposition selectivity.

[0091] The semiconductor structure 100 may be used in various applications, such as logic circuit, dynamic random access memory (DRAM), static random access memory (SRAM) cells, flash memory, or imaging sensor. The semiconductor structure is a planar FET structure or alternatively a FinFET structure. In other embodiments, the disclosed method to selectively deposit a semiconductor material layer may be used to form other epitaxy features with substantially reduced metal sensitivity during the process. In one example for a FET with epitaxy grown channel region, the method is described below: the dummy gate is removed to form a gate trench; the substrate is recessed within the gate trench; epitaxially growing a semiconductor material in the recessed region by the disclosed deposition method.

[0092] The present disclosure provides a method forming a field effect transistor (FET) in accordance with some embodiments. The method includes performing an etching process to a semiconductor substrate, thereby forming recesses in source and drain (S/D) regions of the semiconductor substrate; forming a passivation material layer of a first semiconductor in the recesses; and epitaxially growing a second semiconductor material, thereby forming S/D features in the recesses, wherein the S/D features are separated from the semiconductor substrate by the passivation material layer.

[0093] The present disclosure provides a method forming a field effect transistor (FET) in accordance with some other embodiments. The method includes performing an etching process to a semiconductor substrate, thereby forming recesses in source and drain (S/D) regions of the semiconductor substrate; and epitaxially growing a semiconductor material by a deposition

process with a varying etching/deposition (E/D) factor, thereby forming S/D features in the recesses.

[0094] The present disclosure provides an integrated circuit structure in accordance with some embodiments. The integrated circuit structure includes a semiconductor substrate of a first semiconductor material and having first recesses; a first gate stack formed on the semiconductor substrate and being adjacent the first recesses; a passivation material layer of a second semiconductor material and formed in the first recesses; and first source and drain (S/D) features of a third semiconductor material and formed in the first recesses and being separated from the semiconductor substrate by the passivation material layer, wherein the passivation material layer is free of chlorine.

[0095] The foregoing has outlined features of several embodiments. Those skilled in the art should appreciate that they may readily use the present disclosure as a basis for designing or modifying other processes and structures for carrying out the same purposes and/or achieving the same advantages of the embodiments introduced herein. Those skilled in the art should also realize that such equivalent constructions do not depart from the spirit and scope of the present disclosure, and that they may make various changes, substitutions and alterations herein without departing from the spirit and scope of the present disclosure.

WHAT IS CLAIMED IS:

1. A method of forming a field effect transistor (FET), the method comprising:

performing an etching process to a semiconductor substrate, thereby forming recesses in source and drain (S/D) regions of the semiconductor substrate;

forming a passivation material layer of a first semiconductor in the recesses; and

epitaxially growing a second semiconductor material, thereby forming S/D features in the recesses, wherein the S/D features are separated from the semiconductor substrate by the passivation material layer.

2. The method of claim 1, wherein the forming of the passivation material layer includes performing a non-selective deposition process using a precursor free of chlorine.

3. The method of claim 2, wherein the forming of the passivation material layer includes epitaxially growing the passivation layer of the first semiconductor material, the first semiconductor material being different from the second semiconductor substrate.

4. The method of claim 3, wherein the first semiconductor material includes silicon carbide and the second semiconductor material includes silicon germanium.

5. The method of claim 3, wherein the forming of the passivation material layer includes epitaxially growing the passivation layer of the first semiconductor material that is free of dopant, using the precursor free of dopant-containing gas.

6. The method of claim 3, wherein the forming of the passivation material layer includes forming a silicon carbide layer having a carbon atomic percentage ranging from about 1.8% to about 3%.

7. The method of claim 1, wherein the forming of the passivation material layer includes forming the passivation material layer with a thickness ranging from about 1 nm to about 4 nm, effectively preventing interaction between chlorine and metal residuals.

8. The method of claim 1, further comprising performing a fluorine treatment to the passivation material layer before the epitaxially growing of the second semiconductor material.

9. The method of claim 8, wherein the performing of the fluorine treatment includes performing the fluorine treatment with a fluorine dose ranging from about 1×10^{14} ions/cm^2 to about 2×10^{15} ions/cm^2.

10. The method of claim 1, wherein the epitaxially growing of the second semiconductor material includes epitaxially growing the second semiconductor material with in-situ doping one of a n-type dopant and a p-type dopant.

11. The method of claim 1, wherein the epitaxially growing of the second semiconductor material includes performing a cyclic deposition and etching (CDE) process.

12. The method of claim 11, wherein

the CDE process includes a first cycle for deposition and a second cycle for etching; and

the second cycle uses a chlorine-containing gas that includes at least one of HCl and Cl_2.

13. The method of claim 12, wherein the first cycle of the CDE process uses a precursor that includes PH_3, monomethylsilane (MMS), and at least one of SiH_4 and Si_2H_6.

14. The method of claim 12, wherein the first cycle of the CDE process uses a precursor that includes B_2H_6, GeH_4, and at least one of SiH_4 and Si_2H_6.

15. A method of forming a field effect transistor (FET), the method comprising:

performing an etching process to a semiconductor substrate, thereby forming recesses in source and drain (S/D) regions of the semiconductor substrate; and

epitaxially growing a semiconductor material by a deposition process with a varying etching/deposition (E/D) factor, thereby forming S/D features in the recesses.

16. The method of claim 15, wherein the deposition process incudes a first deposition step having a first etch/deposition (E/D) factor and thereafter a second deposition step having a second E/D factor greater than the first E/D factor.

17. The method of claim 15, wherein

the first deposition step is a non-selective deposition; and

the second deposition step is a selective deposition.

18. The method of claim 15, wherein

the first deposition step has a first substrate temperature less than 620 ^{0}C; and

the second deposition step has a second substrate temperature greater than 620 ^{0}C.

19. The method of claim 15, wherein the deposition process includes one of a cyclic deposition and etching (CDE) process; a co-flow epitaxy growth; and a combination thereof.

20. The method of claim 15, wherein the epitaxially growing of the semiconductor material includes varying the E/D factor by a mechanism selected from gas partial pressure, gas flow rate, substrate temperature, and a combination thereof.

21. An integrated circuit structure, comprising:

a semiconductor substrate of a first semiconductor material and having first recesses;

a first gate stack formed on the semiconductor substrate and being adjacent the first recesses;

a passivation material layer of a second semiconductor material and formed in the first recesses; and

first source and drain (S/D) features of a third semiconductor material and formed in the first recesses and being separated from the semiconductor substrate by the passivation material layer, wherein the passivation material layer is free of chlorine.

22. The integrated circuit structure of claim 21, wherein

the first S/D features are doped with a dopant selected from the group consisting of a n-type dopant and a p-type dopant; and

the passivation material layer is free of the dopant.

23. The integrated circuit structure of claim 21, wherein

the first semiconductor material is silicon; and

the second semiconductor material is different from the third semiconductor material.

24. The integrated circuit structure of claim 23, wherein the passivation material layer further includes fluorine.

25. The integrated circuit structure of claim 24, wherein the passivation material layer includes fluorine with a fluorine concentration ranging from about 1×10^{14} to about 2×10^{15} cm^{-2}.

26. The integrate circuit structure of claim 23, further comprising

second recesses in the semiconductor substrate;

a second gate stack formed on the semiconductor substrate and being adjacent the second recesses;

the passivation material layer of the second semiconductor material in the second recesses; and

second S/D features of the second semiconductor material and formed in the second recesses and being separated from the semiconductor substrate by the passivation material layer, wherein

the first gate stack and the first S/D features are configured to form a first field effect transistor of a first conductivity, and

the second gate stack and the second S/D features are configured to form a second field effect transistor of a second conductivity opposite to the first conductivity.

ABSTRACT

The present disclosure provides a method forming a field effect transistor (FET) in accordance with some embodiments. The method includes performing an etching process to a semiconductor substrate, thereby forming recesses in source and drain (S/D) regions of the semiconductor substrate; forming a passivation material layer of a first semiconductor in the recesses; and epitaxially growing a second semiconductor material, thereby forming S/D features in the recesses, wherein the S/D features are separated from the semiconductor substrate by the passivation material layer.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	2014-0937/24061.2998
	Application Number	
Title of Invention	Metal-Insensitive Epitaxy Formation	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
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Title of the Invention	Metal-Insensitive Epitaxy Formation		
Attorney Docket Number	2014-0937/24061.2998	**Small Entity Status Claimed**	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	23	**Suggested Figure for Publication (if any)**	8B

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For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country

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Title of Invention	Metal-Insensitive Epitaxy Formation	

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Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
	Claims benefit of provisional	62/040880	2014-08-22

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Application Number	Country [i]	Filing Date (YYYY-MM-DD)	Access Code [j] (if applicable)

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Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.
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Name of the Deceased or Legally Incapacitated Inventor :	

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Organization Name	Taiwan Semiconductor Manufacturing Company, Ltd.

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Title of Invention	Metal-Insensitive Epitaxy Formation	

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First Name	David M.	Last Name	O'Dell	Registration Number	42044

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3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.