

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY LTD.,
Petitioner,

v.

MARLIN SEMICONDUCTOR LIMITED,
Patent Owner.

Case No. IPR2026-00130
U.S. Patent No. 9,318,609 B2

PATENT OWNER'S RESPONSE

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TABLE OF EXHIBITS

Exhibit	Description
2001	Declaration of Joseph C. McAlexander III
2002	Peter Van Zant, <i>Microchip Fabrication, A Practical Guide to Semiconductor Processing</i> , (4 th ed. 2000)
2003	<i>Curriculum Vitae</i> of Joseph C. McAlexander III
2004	Merriam-Webster Definition of “surround” (https://www.merriam-webster.com/dictionary/surround)
2005	Second Declaration of Joseph C. McAlexander III
2101	Website: Foundries to Grow Faster than Integrated Circuits in 2016 (https://marketrealist.com/2015/12/foundries-grow-faster-integrated-circuits-2016/)
2102	Website: Ranked: Semiconductor Foundries by Revenue Share (www.visualcapitalist.com/ranked-semiconductor-foundries-by-revenue-share/)
2103	Website: US Patent No. 9,318,609 B2 – Semiconductor Device with Epitaxial Structure – Google Patents https://patents.google.com/patent/US9318609B2/en?q=9%2c318%2c609+
2104	Declaration of Paul Ahern Regarding Patent Owner’s Request for Discretionary Denial of Institution

I. INTRODUCTION

None of Petitioner's presented grounds anticipates or renders obvious claims 1-10 of U.S. Patent No. 9,318,609 ("the '609 Patent"). As explained below, and in more detail throughout this Patent Owner Response ("Response") and in the accompanying second declaration of Joseph McAlexander (EX2005), Petitioner's presented grounds fail for multiple reasons.

First, as explained in Patent Owner's Preliminary Response (Paper 8) and below, all grounds also fail to disclose or render obvious an isolation structure surrounding a fin structure. Neither of the Petition's primary references (Xu for Grounds 1A and 1B, Ching for Grounds 2A-C) describes such an isolation structure. An important feature of the '609 patent's claimed semiconductor device is that the isolation structure surrounds the fin structure on all four sides, thereby completely isolating the fin structure. That the isolation structure surrounds the fin structures is confirmed by the '609 patent's specification, which explains that "a lower portion of each fin structure is **embedded** in the isolation structure 20," indicating that the isolation structure covers all four sides of each fin structure. EX1001 at 3:52-53 (emphasis added). This is further confirmed by the '609 patent's figures, which consistently illustrate the isolation structure 20 covering all four sides of the fin structures 12:

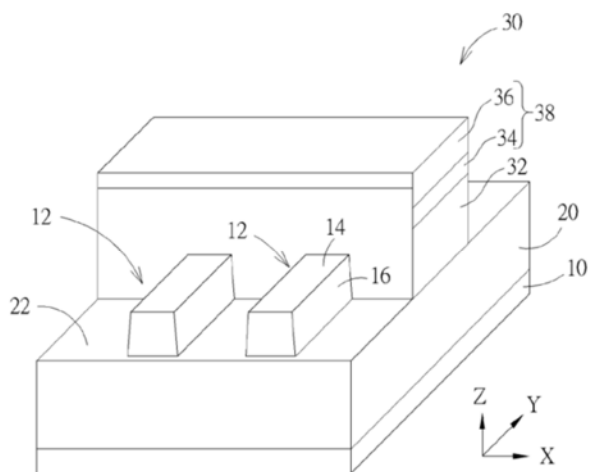


FIG. 2

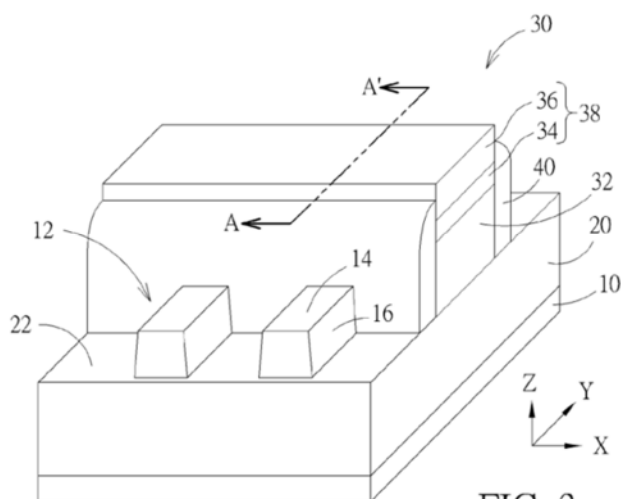


FIG. 3

EX1001 at Figs. 2 and 3; *see also id.* at Fig. 5.

In contrast, in Xu, “isolation features 130” do not surround the fin structures on all four sides of the fins 120, but rather only cover two sides of the fins 120:

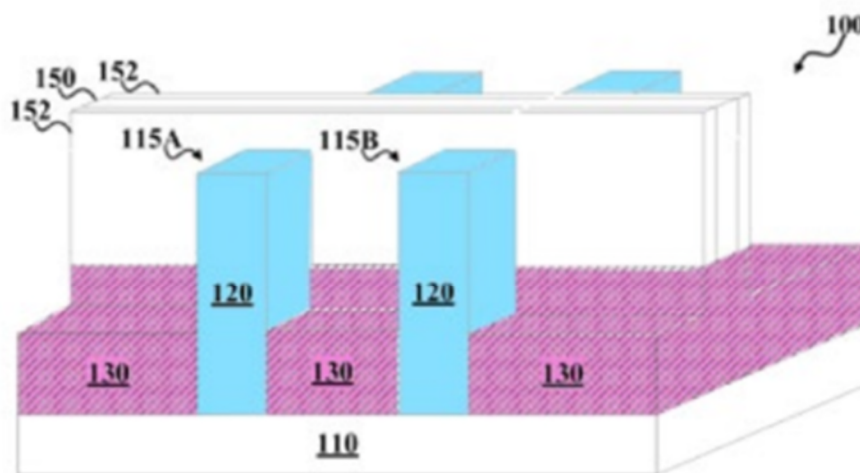


FIG. 3

Pet., 16 (showing annotated EX1004-Xu, Fig. 3). Although Xu states that “[i]solation features 130 . . . surround the fin structures 115A and 115B” (EX1004-Xu at 3:54-56), a POSITA would have understood that Xu’s usage of the term “surround” is inconsistent with that term as required by the claimed semiconductor device. Moreover, even if Xu’s isolation features 130 are interpreted as “surrounding” fins 120, Xu’s isolation features nevertheless do not surround Xu’s “fin structure” because, unlike the ’609 patent’s claimed semiconductor device, Xu’s device merges its fins together into a single, merged “fin structure.” Xu explains that a “fin template 135 is formed by merging together the fins 120 of the FinFET device 100.” EX1004-Xu at 5:2-4. A “semiconductor material is epitaxially grown by an epi process until the fins 120 of the fin structures 115A and 115B are merged together to form the fin template 135.” *Id.* at 5:8-10. Xu’s Figure 4 illustrates the merging together of fins 120 to form fin template 135:

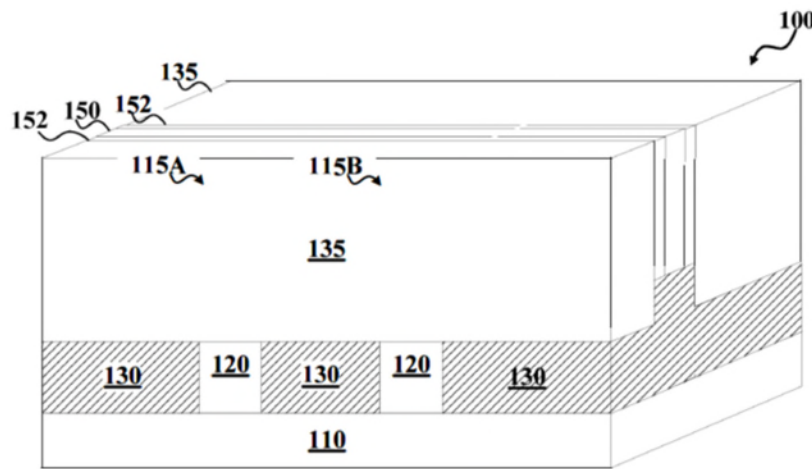


FIG. 4

Id. at Fig. 4. 58. As shown in Figure 4 above, Xu's fin template 135 is disposed on top of isolation features 130. As such, Xu's "isolation features 130" do not surround its fin structure because it does not enclose any side of the merged fin structure, e.g., the part made up of fin template 135.

Similarly, in Ching, the alleged isolation structure (STI regions 22) does not surround the alleged fin structure (semiconductor strip 21) on all four sides, but rather only covers two sides of semiconductor strip 21:

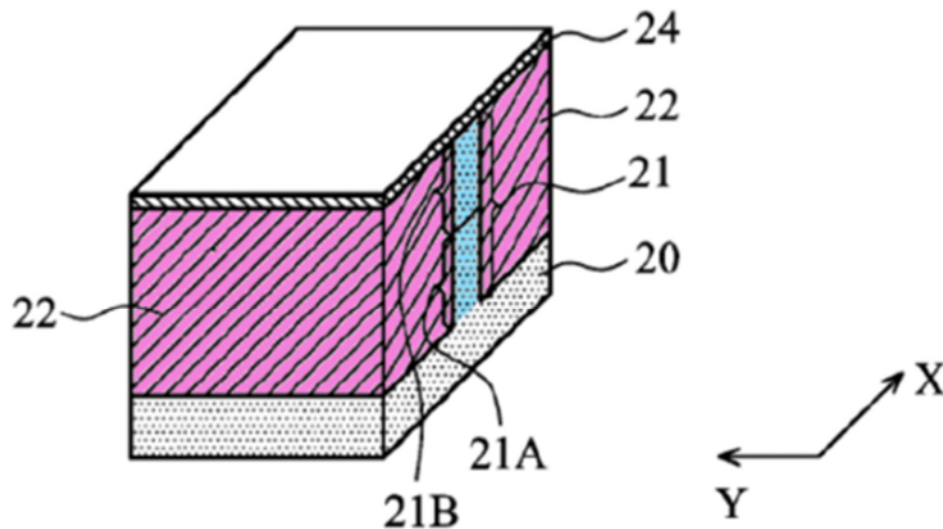
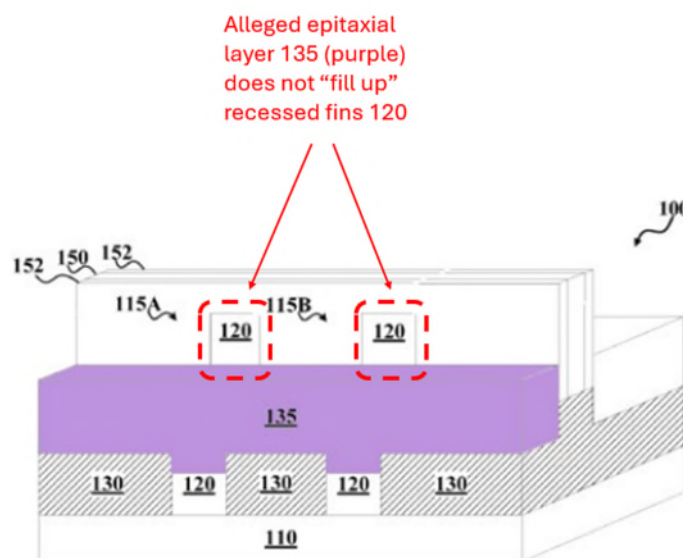


Fig. 1

Pet. at 57 (showing annotated EX1005-Ching, Fig. 1). The Petition argues that “[t]o the extent the claim language requires the isolation structure to *fully* circle the fin structures . . . [a] POSITA would have further understood that, in Ching, the shallow trench isolation regions (‘STI regions 22’) isolate ‘semiconductor strips 21’ from one another *and* isolate the transistors that will ultimately be formed from ‘semiconductor strips 21’ from one another.” Pet. at 59. But this argument is conclusory and contradicted by Ching’s own disclosure, which states that “semiconductor strip 21 is formed **between, and contacting, neighboring** STI regions 22.” EX1005-Ching at 2:5-6 (emphasis added). That Ching’s semiconductor strips are formed between neighboring STI regions demonstrates that

the STI regions do not surround the semiconductor strips, because the STI regions would need to merge in order to enclose the semiconductor strips on all four sides.

Second, Grounds 1A and 1B fail to disclose or render obvious claim 5’s requirement of “a recess formed at one end of the fin structure, wherein the epitaxial structure fills up the recess.” The Petition improperly combines two separate and incompatible embodiments of Xu—one in which strain is achieved by etching the isolation structure and fin template (Figures 1-6), and another in which strain is achieved by forming a recess in the fin (Figures 7-11A)—without any valid rationale for doing so, as each embodiment provides a different and self-contained method of controlling source and drain depth. Moreover, even in the Petition’s proposed modification, Xu’s “fin template” does not fill up the alleged recess, as the fin template does not extend to the top of the recess as required by claim 5.



Third, Grounds 1B and 2C fail to render obvious claim 7’s recited height-difference range of 100 to 250 Angstroms. The Petition relies on Huang to supply the dimensional specificity that Xu and Ching lack, but a POSITA would not have been motivated to combine either Xu or Ching with Huang because Huang employs a fundamentally different “Fin-Last” process architecture—in which epitaxial growth occurs before the fins are even defined—that produces entirely different device geometries and dimensional relationships than the “Fin-First” architectures of Xu and Ching. Furthermore, Huang does not disclose the claimed range; the Petition merely derives a computed range of approximately 50 to 4,750 Angstroms by subtracting two independently disclosed, unrelated parameters—a range so broad that it spans nearly two orders of magnitude and provides no meaningful guidance toward the narrow 100-250 Angstrom window of claim 7.

II. SEMICONDUCTOR TRANSISTOR TECHNOLOGY PRIMER

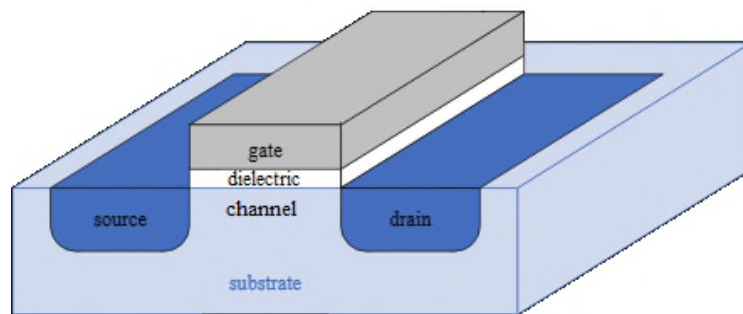
The following is a brief primer of semiconductor transistors to establish a foundation of common terms and concepts that can be used in addressing the defects in the Petition. These terms and concepts focus on: (1) the basic components of transistors; (2) the difference between planar and three-dimensional (*e.g.*, fin) transistors; and (3) common process steps for creating transistors. EX2005-McAlexander-Decl, ¶21.

A. Basic Transistor Components

Today's semiconductor devices trace their lineage back to the first computers of the 1940s, which used vacuum tubes to perform two key electrical functions: switching (*i.e.*, turning access to electrical current on and off) and amplification (*i.e.*, increasing the amplitude of a signal while retaining its electrical characteristics). EX2002 at 1-2; EX2005-McAlexander-Decl, ¶22. Where earlier tube devices used a vacuum tube to control the flow of electrons (turning electrical current on and off), today's semiconductor devices use transistors. EX2002 at 3; EX2005-McAlexander-Decl, ¶22.

One type of transistor typically used in an integrated circuit (or "chip") is a "field effect transistor," or FET. EX2005-McAlexander-Decl, ¶23. Materials used to build such transistors are divided into three categories based on their ability to conduct electrical current: conductors, dielectrics, and semiconductors. EX2002 at 29-34; EX2005-McAlexander-Decl, ¶23. In a conductor (*e.g.*, a metal), electric current can flow freely. EX2002 at 29; EX2005-McAlexander-Decl, ¶23. A dielectric (*e.g.*, silicon dioxide) is an insulative material at the opposite end of the conductivity spectrum and has a high resistance to the flow of current. EX2002 at 30; EX2005-McAlexander-Decl, ¶23. Semiconductors (*e.g.*, silicon) fall between conductors and dielectrics and have some conducting and some resisting ability. EX2002 at 31-34; EX2005-McAlexander-Decl, ¶23.

The simplified FET below illustrates how these materials may be used to create a semiconductor transistor device. EX2005-McAlexander-Decl, ¶24. As shown, the transistor is built on a semiconductor substrate and comprises a source, a drain, a gate, and a channel. *See, e.g.*, EX2002 at 510-511. The source, drain and channel comprise semiconductor material, the gate comprises a conductor, and the gate and channel are separated by a thin dielectric layer.

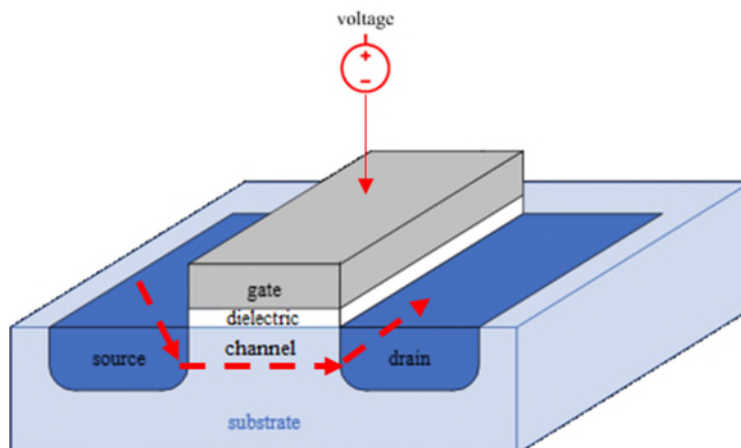


See, e.g., EX2002 at 510-511; EX2005-McAlexander-Decl, ¶24.

The source and drain are regions in the semiconductor substrate that are either rich in electrons (a negative, or n-type, region) or rich in holes (a positive, or p-type, region). EX2002 at 26-28, 427-28; EX2005-McAlexander-Decl, ¶25. The channel is a region under the gate and between the source and drain, and is of the opposite type to that of the source and drain. In other words, if the source and drain are n-type regions, then the channel will be a p-type region (and vice versa). EX2002 at 510-511; EX2005-McAlexander-Decl, ¶25.

The gate is a conductor (or semiconductor) located above the channel. EX2005-McAlexander-Decl, ¶26. In this simplified version of a FET, there is a dielectric between the channel and the gate. EX2002 at 510-511; EX2005-McAlexander-Decl, ¶26. When a voltage is applied to the gate, the dielectric prevents the “flow of charge” (current) between the gate and the channel, but the applied voltage results in the creation of a “field effect” in the channel. EX2002 at 510-511; EX2005-McAlexander-Decl, ¶26. This “field effect” either builds up or depletes the charges in the channel (depending on whether it is a p- or n-type channel). EX2002 at 510-511; EX2005-McAlexander-Decl, ¶26.

As illustrated below, this field effect allows charge to flow from the source, through the channel, to the drain. EX2005-McAlexander-Decl, ¶27. Thus, selectively applying voltage to the gate switches the transistor on and off, starting and stopping drain-to-source or source-to-drain current. EX2005-McAlexander-Decl, ¶27.

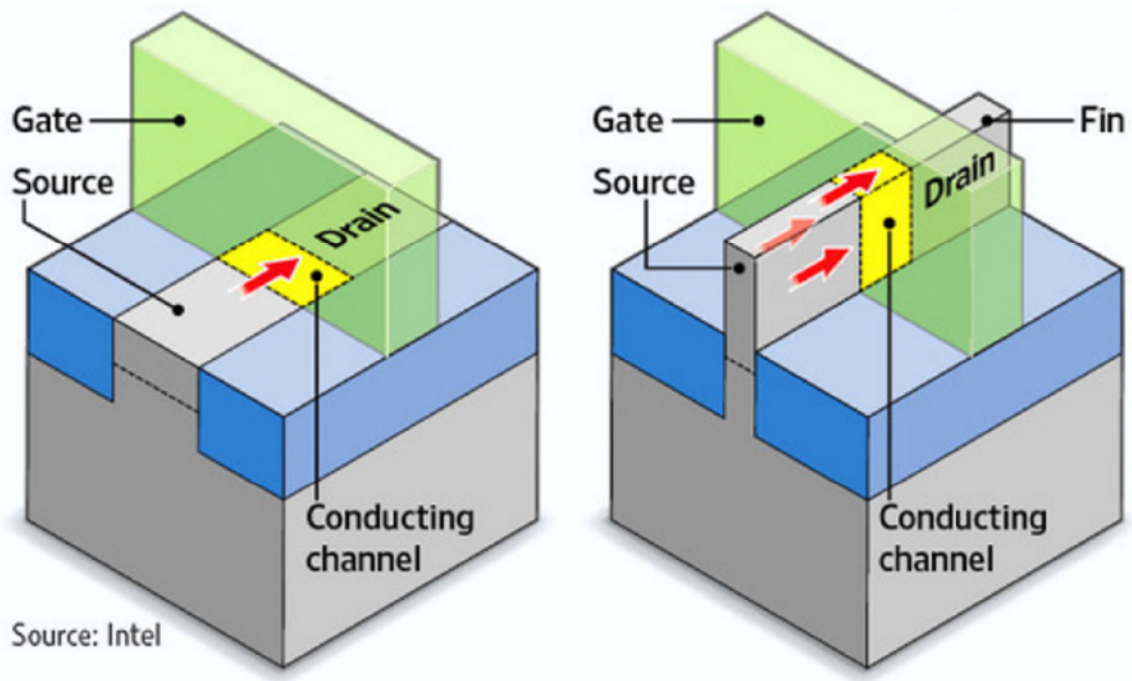


B. Planar vs. Three-Dimensional Transistors

Integrated circuit chips in modern computer systems are typically composed of millions and even billions of transistors. EX2005-McAlexander-Decl, ¶28. The first transistor prototypes in 1947 were several inches in size, and implementing even the simplest early computers required tens of thousands of gates or transistors. *Id.* Given those numbers, and the correlation between an increased number of transistors and increased computing power, the desire to shrink transistor sizes to fit more transistors on a chip has been consistent and widespread in industry. *Id.* This desire led to the development of a new type of transistor, a “FinFET.” EX2005-McAlexander-Decl, ¶28.

The simplified illustrative FET transistors illustrated in the previous section all feature a gate structure built on a flat semiconductor substrate; in other words, a “planar” FET. EX2005-McAlexander-Decl, ¶29. In the early 2010s, however, commercial gates evolved from such two-dimensional (2D) planar transistors to three-dimensional (3D) FinFET transistors. EX2005-McAlexander-Decl, ¶29.

In the below image, the figure on the left illustrates a 2D planar transistor built on a flat silicon substrate. EX2005-McAlexander-Decl, ¶30. In this traditional 2D planar transistor, the transistor forms a conducting channel in the silicon region under the gate.



EX2005-McAlexander-Decl, ¶30.

In contrast, as illustrated above in the right figure, an exemplary 3D fin transistor design features a vertical semiconductor fin structure above the substrate that acts as a channel between the source and drain regions. EX2005-McAlexander-Decl, ¶31. In the resulting fin field effect transistor (“FinFET”), the source and drain regions are formed at opposing regions of the fin, and the gate is wrapped over the fin overlaying the fin on the top and two sides. *Id.*

Thus, where a planar gate has only a horizontal dimension, the FinFET gate has both horizontal and vertical dimensions, thereby allowing a FinFET transistor to take up less surface area than a planar transistor. EX2005-McAlexander-Decl, ¶32. This alone means that more FinFET transistors may fit on an integrated circuit chip

compared to that of the planar transistor. *Id.* In addition, because FinFETs typically leak less current than planar FET transistors, FinFETs may be more tightly packed on an integrated circuit chip. *Id.* This, too, increases the number of FinFET transistors that may fit onto a single chip. *Id.*

C. Processes For Manufacturing Integrated Circuits And Transistors

1. The Four Stages Of Fabricating Integrated Circuits

The intricate, complex manufacturing process developed over the years for achieving such highly-dense integrated circuits can be divided into four distinct stages: (1) material preparation; (2) wafer preparation; (3) wafer fabrication; and (4) packaging. EX2005-McAlexander-Decl, ¶33.

In the first stage, the semiconductor material itself is created. EX2002 at 13. For a silicon semiconductor, the raw starting material is sand, which is converted to pure silicon with a polysilicon structure. EX2002 at 13; EX2005-McAlexander-Decl, ¶34.

In the second stage, the semiconductor material is first formed into a silicon crystal with specific electrical and structural parameters, and it is then sliced into thin disks called “wafers.” EX2002 at 13-14; EX2005-McAlexander-Decl, ¶35. A wafer acts as a semiconductor substrate on and in which transistors may be formed. EX2005-McAlexander-Decl, ¶35.

The third stage is wafer fabrication, during which individual integrated circuits are formed in and on the wafer semiconductor substrate. EX2002 at 14; EX2005-McAlexander-Decl, ¶36. Thousands of integrated circuits can be formed on the substrate of a single wafer. EX2002 at 14; EX2005-McAlexander-Decl, ¶36.

In the packaging stage, the wafer is separated into individual chips. EX2002 at 14-15; EX2005-McAlexander-Decl, ¶37.

2. The Wafer Fabrication Stage

The third manufacturing stage, wafer fabrication, is the one most relevant here, and it can take several thousand steps, during which transistors and other devices are formed in and on the wafer's substrate. EX2002 at 14; EX2005-McAlexander-Decl, ¶38. These steps are generally performed using three categories of materials (conductors, semiconductors, and dielectrics) in four basic operations (layering, patterning, doping, and heat treatments). See EX2002 at 29-31, 71; EX2005-McAlexander-Decl, ¶38. For purposes of understanding the Petition and its deficiencies, the two most important basic operations are layering and patterning. EX2005-McAlexander-Decl, ¶38.

Layering is the operation used to add thin layers to the semiconductor substrate. EX2002 at 72; EX2005-McAlexander-Decl, ¶39. The layers may be conductors, semiconductors, or dielectrics; and they can have a variety of functions and be made in a variety of ways. EX2002 at 72; EX2005-McAlexander-Decl, ¶39.

For example, one way of adding a layer of material is to deposit that material onto the semiconductor substrate. EX2005-McAlexander-Decl, ¶40. Another way of adding a layer of material is to grow the material on the semiconductor substrate. *Id.* After an initial layer is added to the semiconductor substrate, additional layers may be added to the earlier layers using similar growth or deposition processes. *Id.* To illustrate, the transistor structure shown below shows a number of layers that have been added to the wafer's semiconductor substrate, some deposited, some grown. EX2002 at 72; EX2005-McAlexander-Decl, ¶40.

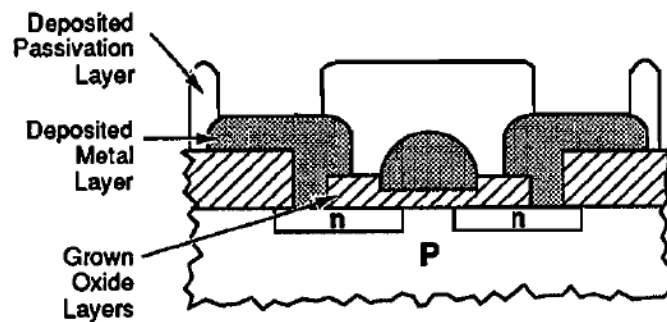


Figure 4.4 Cross section of completed metal gate MOS transistor with grown and deposited layers.

Patterning is the series of steps to remove (etch away) selected portions of the semiconductor substrate or one or more layers of materials that were added during one or more prior layering operations. EX2002 at 72-73; EX2005-McAlexander-Decl, ¶41. This creates a pattern on the wafer surface. EX2002 at 72-73; EX2005-McAlexander-Decl, ¶41.

The patterning may result in one or more holes in the layered material or one or more remaining islands of material. EX2002 at 72-73; EX2005-McAlexander-Decl, ¶42. For example, the following figures illustrate the use of patterning to make (1) a hole in a previously formed layer: and (2) an island from a previously formed layer:



Figure 4.7 Patterning.

EX2005-McAlexander-Decl, ¶42.

The repeated combination of layering and patterning in different sequences and variations is critical to the formation of transistors in and on the semiconductor wafer:

These parts are created one layer at a time by the combination of putting a layer on the surface and removing a portion, with a patterning process, to leave a specific shape. The goal of the patterning operations is to create the desired shapes in the exact dimensions (feature size) required by the circuit design, and to locate them in their proper location on the wafer surface and in relation to the other parts.

EX2002 at 73; EX2005-McAlexander-Decl, ¶43.

III. THE INVENTION OF THE '609 PATENT

The '609 patent “provide[s] a semiconductor device with an epitaxial layer so that stress imposed on the channel region can be increased.” EX1001 at 1:54-56.

According to a preferred embodiment of the invention:

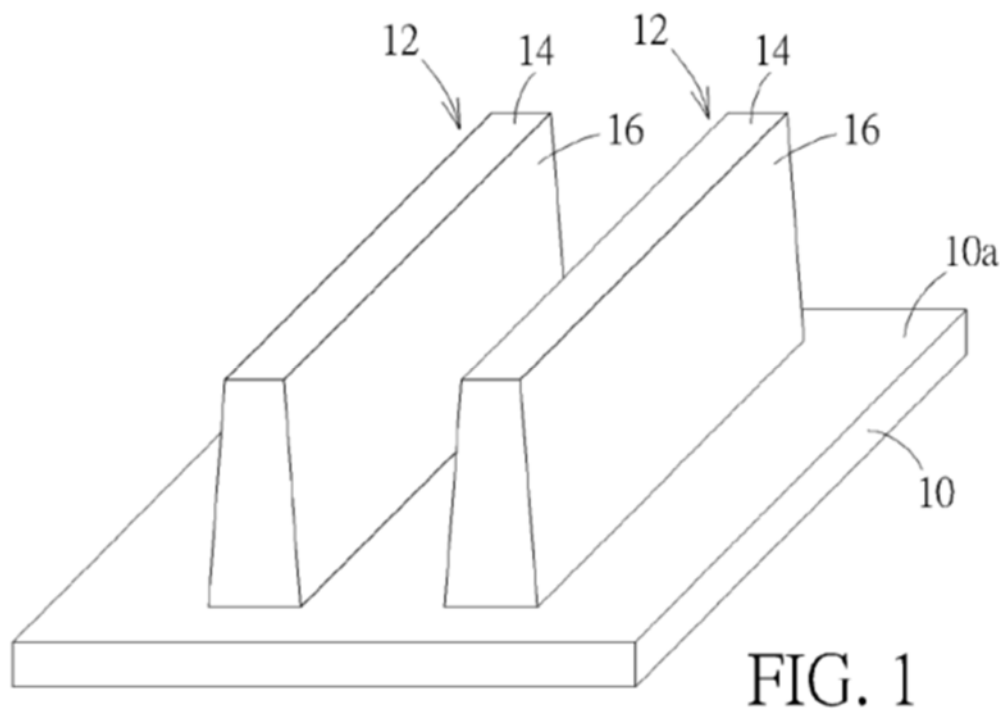
The semiconductor device includes a fin structure, an isolation structure, a gate structure and an epitaxial structure. The fin structure protrudes from the surface of the substrate and includes a top surface and two sidewalls. The isolation structure surrounds the fin structure. The gate structure overlays the top surface and the two sidewalls of a portion of the fin structure, and covers a portion of the isolation structure. The isolation structure under the gate structure has a first top surface and the isolation structure at two sides of the gate structure has a second top surface, wherein the first top surface is higher than the second top surface. The epitaxial layer is disposed at one side of the gate structure and is in [] direct contact with the fin structure.

Id. at 1:57-2:3.

The invention of the '609 patent provided benefits over prior-art semiconductor devices. For example, “[s]ince the process for etching the isolation structure is optionally carried out prior to and/or after the formation of the recess, the height of the isolation structure at two sides of the gate structure may be reduced.

In this way, the epitaxial layer may be filled into the corresponding recess easily during the epitaxial growth process.” *Id.* at 2:6-12. “Furthermore, since the epitaxial structure is not sealed during the epitaxial growth process, the void defects may be also avoided as a result.” *Id.* at 2:12-15.

Figures 1 to 11 of the '609 patent illustrate “a fabrication method of a semiconductor device according to a preferred embodiment of the present invention.” *Id.* at 2:24-26. “FIG. 1 is a schematic perspective view showing the semiconductor device of at the beginning of the fabrication process.” *Id.* at 3:4-6.



Id. at Fig. 1. At the beginning of the fabrication process, the device includes a substrate 10 with fin structures 12 protruding from the substrate. EX2005-

McAlexander-Decl, ¶47. Notably, as shown, the fin structures 12 do not extend to the edge of the substrate 10. *Id.*

Next, “FIG. 2 is a schematic perspective diagram showing the semiconductor device after the formation of a dummy gate structure.” EX1001 at 3:46-47.

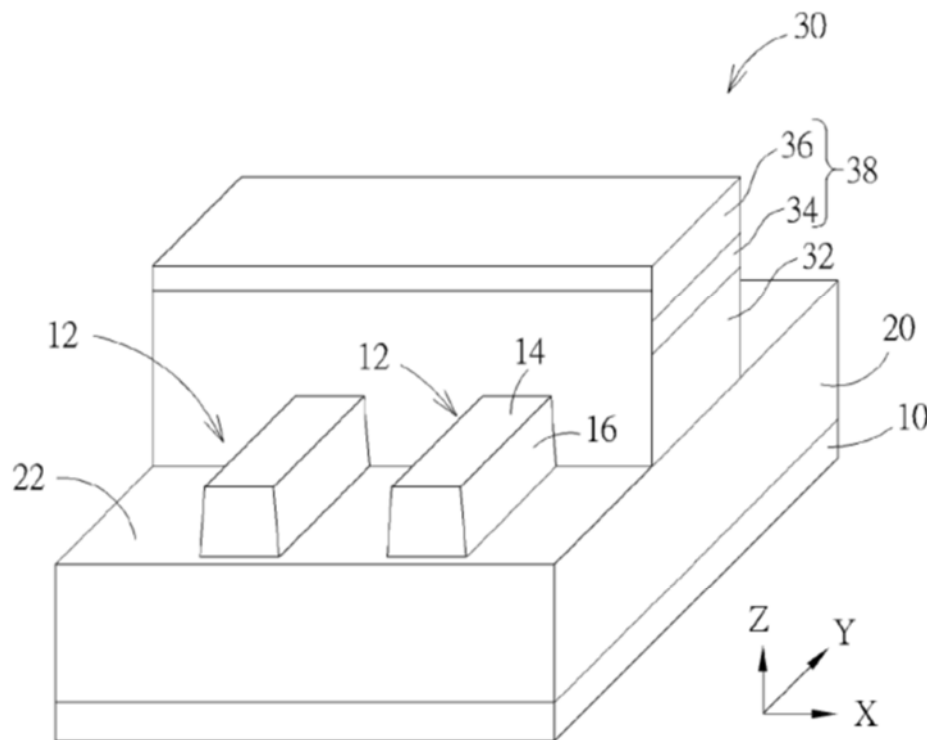


FIG. 2

Id. at Fig. 2. As shown, “[a]t this stage, a lower portion of each fin structure 12 is **embedded** in the isolation structure 20.” *Id.* at 3:52-53 (emphasis added). That is, as clearly shown in Fig. 2, the isolation structure encloses each side of the lower portion of each fin structure. EX2005-McAlexander-Decl, ¶49. Forming the isolation structure to surround the fin structures in this manner is important in order

to fully isolate each fin structure, preventing unwanted contact and electrical interaction and thereby ensuring that each fin structure operates independently without interference. *Id.* Figure 2 also illustrates the formation of a gate structure 30 which “may cover a top surface 14 and two side surfaces 16 of portions of each fin structure 12, and may cover a top surface 22 of portions of the isolation structure 20.” EX1001 at 4:4-7.

“FIG. 5 is a schematic perspective view showing the semiconductor device after etching the isolation structure.” *Id.* at 5:17-19.

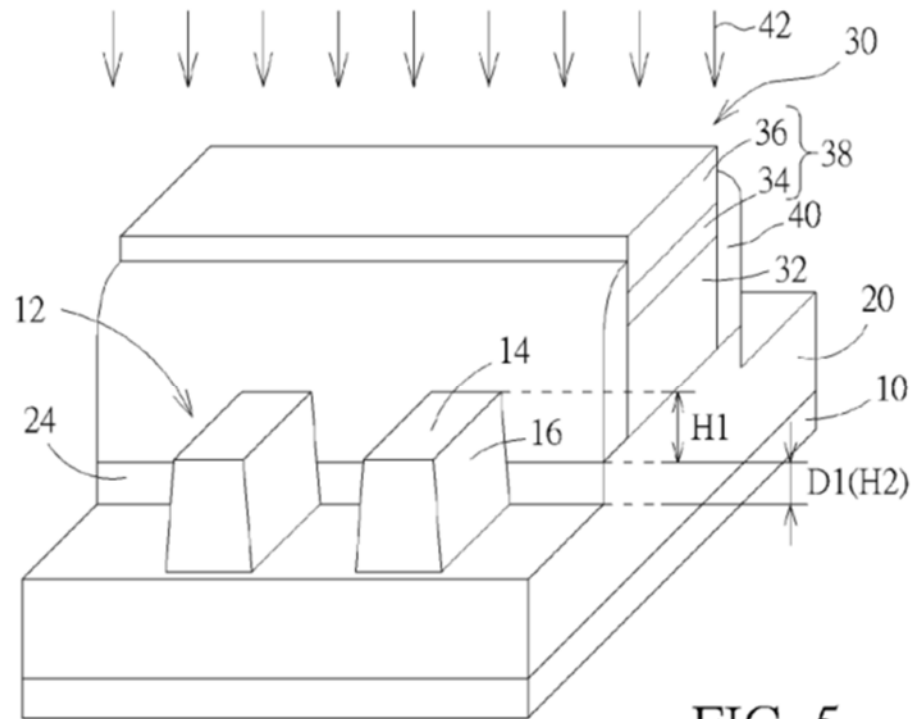
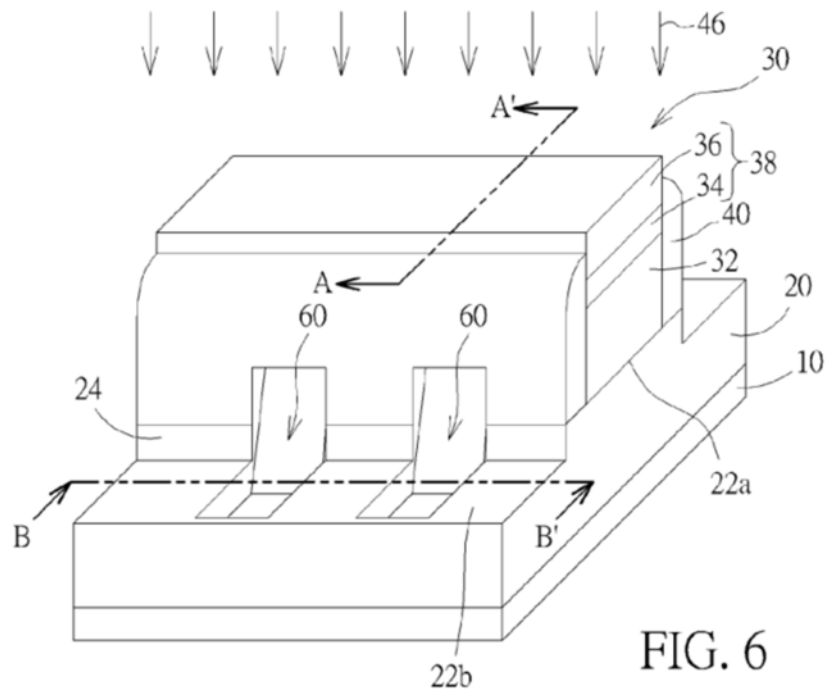


FIG. 5

Id. at Fig. 5. “After the formation of the spacers 40, the isolation structure 20 exposed from the gate structure 30 and the spacers 40 may be further etched by a

suitable etching process. In this way, a top surface 22 of portions of the isolation structure 20 may be etched down to a predetermined depth.” *Id.* at 5:19-24. “At this time, the isolation structure 20 under the gate structure 30 and the spacers 40 may have a relatively high first top surface 22a, while the isolation structure 20 exposed from the gate structure 30 may have a relatively low second top surface 22b.” *Id.* at 5:33-37.

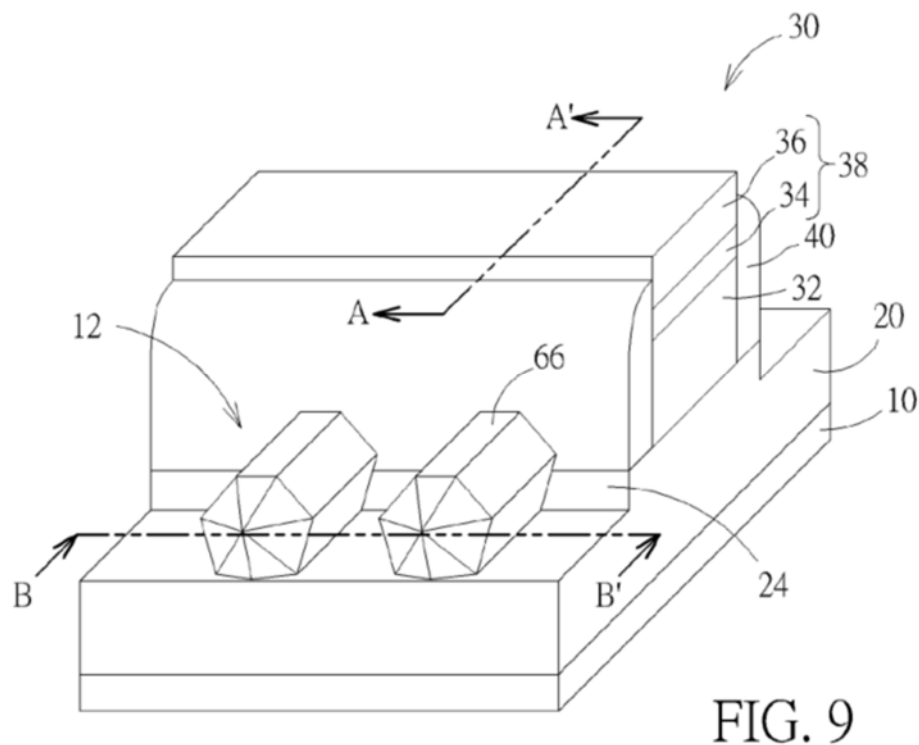
“FIG. 6 is a schematic perspective view showing the semiconductor device after etching fin structures.” *Id.* at 5:42-44.



Id. at Fig. 6. “As shown in FIG. 6 . . . a second etching process 46 is carried out to etch the fin structures 12 under the gate structure 30 and the spacers 40. After the etching process, a recess 60 may be formed in each fin structure at at least one side

of the gate structure 30.” *Id.* at 5:47-51. Because the isolation structure 20 encloses the fin structures on all four sides, when the fin structures are etched down to form recesses 60, the isolation structure 20 surrounds the recesses 60, as can be seen in Fig. 6 above. EX2005-McAlexander-Decl, ¶53.

Finally, “FIG. 9 is a schematic perspective view showing the semiconductor device after the formation of an epitaxial layer.” EX1001 at 6:29-31. Figure 9 illustrates an embodiment of the claimed semiconductor device:



Id. at Fig. 9. “As shown in FIG. 9 . . . an epitaxial growth process . . . maybe carried out in order to grow an epitaxial structure [66] in each corresponding recess 60.” *Id.* at 6:34-39. “[E]ach epitaxial structure 66 may completely cover the bottom surface

68 and sidewalls 70 of the corresponding recess 60.” *Id.* at 6:39-41. Because the isolation structure 20 surrounds the recesses 60 on all four sides, when the epitaxial structures 66 are formed in the recesses 60, the isolation structure 20 also surrounds the epitaxial structures 66, as can be seen in Fig. 9 above. EX2005-McAlexander-Decl, ¶55. This beneficially ensures that the epitaxial structures are structurally separate and isolated, preventing unwanted contact and electrical interaction and thereby ensuring that each fin structure operates independently without interference. *Id.* Moreover, “through etching the isolation structure 20 at two sides of the gate structure 30, the epitaxial structure 66 may be formed with a desired height (also called depth) and without any void defects.” EX1001 at 7:3-7. Thus, the ’609 patent’s isolation structure provides an improvement over prior-art semiconductor devices by mitigating defects associated with epitaxial structures. EX2005-McAlexander-Decl, ¶55.

The above-described innovative aspects of the invention are embodied in all challenged claims via independent claim 1, which recites:

1. A semiconductor device, comprising:

[1.a] a fin structure, protruding from a surface of a substrate, wherein the fin structure comprises a top surface and two side surfaces;

[1.b] *an isolation structure, disposed on the surface of the substrate and surrounding the fin structure;*

[1.c(i)] a gate structure, overlaying the top surface and the two side surfaces of a portion of the fin structure and covering a portion of the isolation structure,

[1.c(ii)] wherein the isolation structure under the gate structure has a first top surface and the isolation structure at two sides of the gate structure has a second top surface, and the first top surface is higher than the second top surface; and

[1.d] an epitaxial layer, disposed at one side of the gate structure and in direct contact with the fin structure.

EX1001, claim 1 (annotated to identify claim elements).

IV. THE PETITION GROUNDS FAIL TO DISCLOSE OR RENDER OBVIOUS THE CHALLENGED CLAIMS

The Petition asserts five grounds challenging various claims of the '609 patent:

Ground	Claim(s) Challenged	35 U.S.C. §	References
1A	1-6, 8-10	102/103	Xu
1B	7	103	Xu in view Huang
2A	1, 3, 5, 6, 8-10	102/103	Ching
2B	2, 4	103	Ching in view of Xu
2C	7	103	Ching in view of Huang

Pet., 4. As explained below, all of the Petition grounds fail to disclose or render obvious any of the challenged claims. Accordingly, all claims should be found patentable.

A. All Asserted Grounds Fail To Disclose Or Render Obvious “An Isolation Structure, Disposed On The Surface Of The Substrate And Surrounding The Fin Structure” (Element [1.b])

1. Grounds 1A and 1B: Xu Fails To Disclose Or Render Obvious “An Isolation Structure, Disposed On The Surface Of The Substrate And Surrounding The Fin Structure”

a. Xu’s Alleged Isolation Structure Does Not Surround A Fin

The Petition alleges that Xu’s “isolation features 130” (the alleged isolation structure) surround the “fins 120.” Pet., 16. However, as shown in the figure below (annotated in the Petition), Xu’s “isolation features 130” do not surround the fin structures on all four sides of the fins 120, but rather only cover two sides of the fins 120:

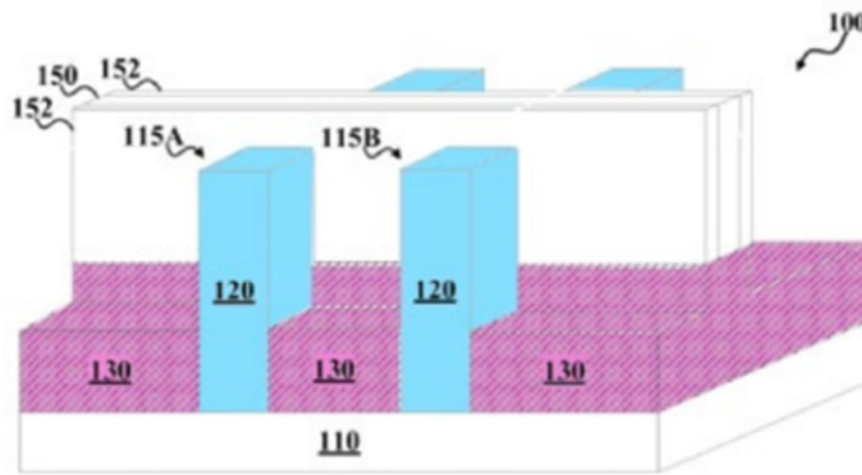


FIG. 3

Pet., 16 (showing annotated EX1004-Xu, Fig. 3).

This is in contrast with the challenged claims, which require that the “isolation structure . . . **surrounding** the fin structure.” As explained above in Section III, an important feature of the ’609 patent’s claimed semiconductor device is that the isolation structure surrounds the fin structure on all four sides, thereby completely isolating the fin structures and the epitaxial structures formed on the fin structures. EX2005-McAlexander-Decl, ¶60. That the isolation structure surrounds the fin structures is confirmed by the ’609 patent’s specification, which explains that “a lower portion of each fin structure is **embedded** in the isolation structure 20,” indicating that the isolation structure covers all four sides of each fin structure. EX1001 at 3:52-53 (emphasis added); EX2005-McAlexander-Decl, ¶60. This is further confirmed by the ’609 patent’s figures, which consistently illustrate the

isolation structure 20 covering all four sides of the fin structures 12, not merely two of the sides as in Xu:

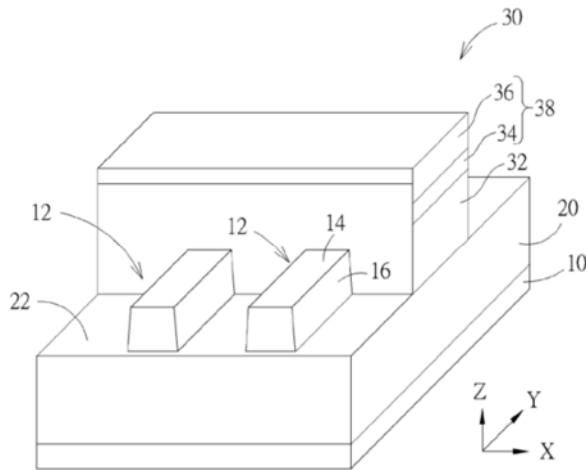


FIG. 2

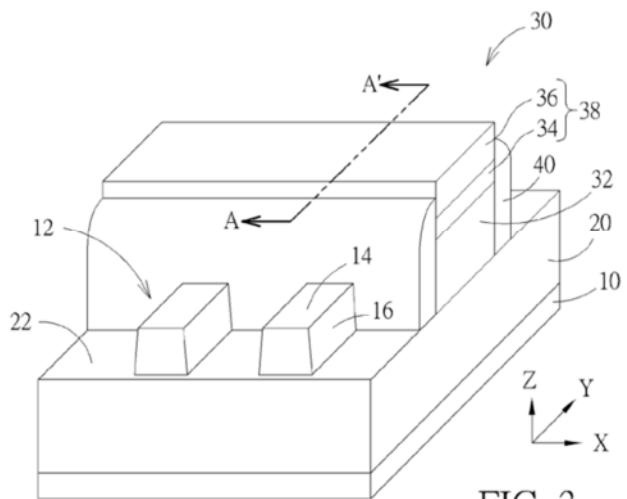


FIG. 3

EX1001 at Figs. 2 and 3; *see also id.* at Fig. 5. Moreover, the figures also illustrate that the isolation structure 20 surrounds all four sides of the etched down fin structures (recesses 60) and the epitaxial structures 66 formed over the etched down fin structures:

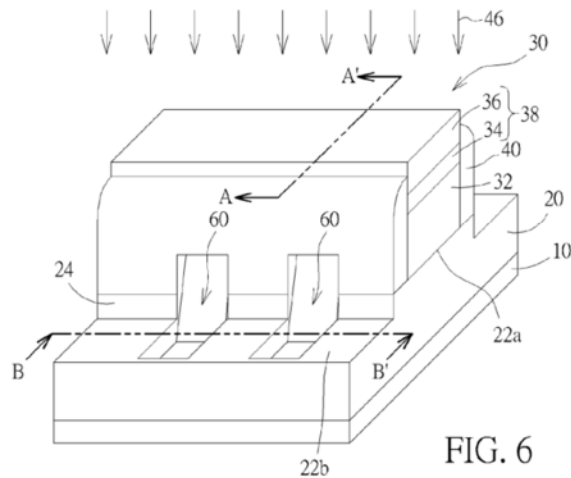


FIG. 6

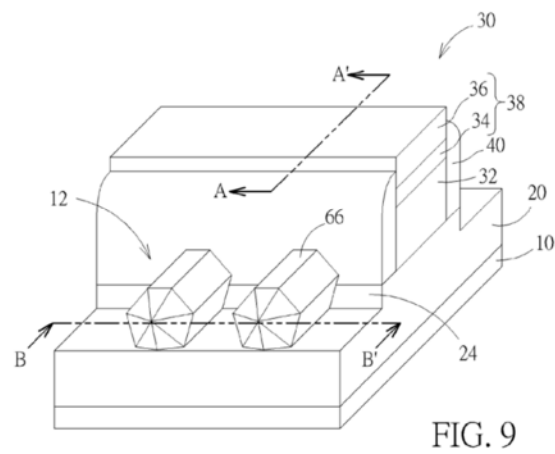


FIG. 9

EX1001 at Figs. 6 and 9. Thus, a POSITA would have understood that in the claimed semiconductor device, the isolation structure surrounds the fin structure on all four sides. EX2005-McAlexander-Decl, ¶62; *see also* EX2004 (“surround” means “to enclose on all sides”).

In contrast, Xu’s “isolation features 130” do not surround the fin structures as required by the challenged claims. *Id.* Although Xu states that “[i]solation features 130 . . . surround the fin structures 115A and 115B,” (EX1004-Xu at 3:54-56) a POSITA would have understood that Xu’s usage of the term “surround” is inconsistent with the claimed semiconductor device. EX2005-McAlexander-Decl, ¶63. That passage in Xu describes Xu’s Figure 2, which shows that isolation features 130 do not, in fact, surround the fin structures but rather only cover two sides of each fin:

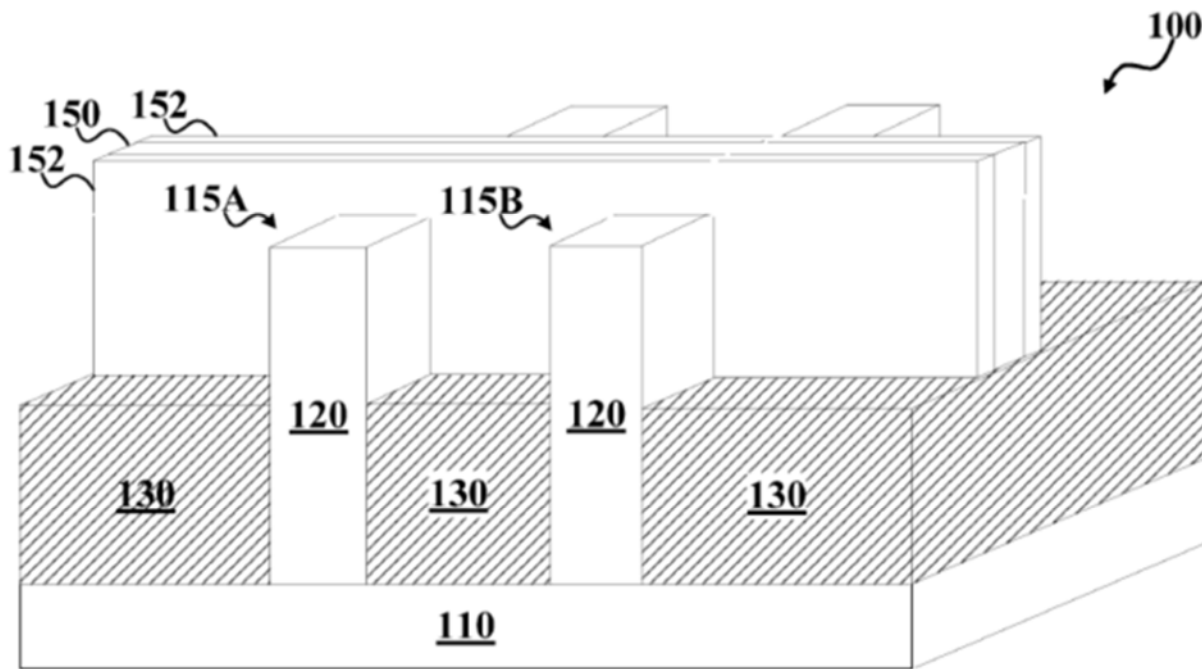


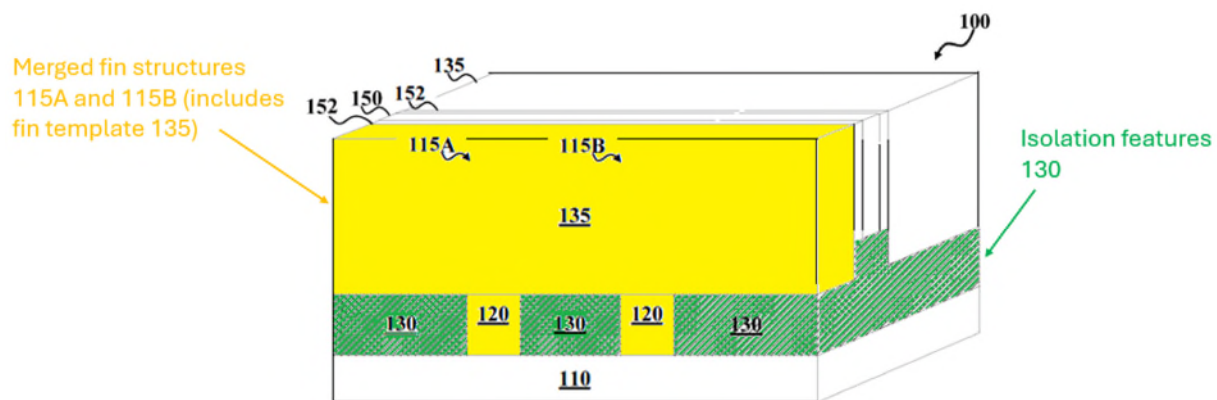
FIG. 2

EX1004-Xu at Fig. 2. In contrast to the '609 patent's figures, which all illustrate the isolation structure surrounding the fin structures, all of Xu's figures consistently illustrate "isolation features 130" as covering only two sides of the fins 120. EX1004-Xu at Figs. 2-6, 8A-C, 9A-C, 10A, 11A, 13A, 14A, 15A, 16A.

b. Xu's Alleged Isolation Structure Does Not Surround Xu's Merged Fin Structure

Moreover, Xu fails to disclose or render obvious this limitation for an additional reason. Even if Xu's isolation features 130 are interpreted as "surrounding" fins 120, Xu's isolation features nevertheless do not surround Xu's

“fin structure” because unlike the ’609 patent’s claimed semiconductor device, Xu’s device merges its fins together into a single, merged “fin structure.” EX2005-McAlexander-Decl, ¶65. For example, Xu explains that a “fin template 135 is formed by merging together the fins 120 of the FinFET device 100.” EX1004-Xu at 5:2-4. A “semiconductor material is epitaxially grown by an epi process until the fins 120 of the fin structures 115A and 115B are merged together to form the fin template 135.” *Id.* at 5:8-10. Xu’s Figure 4 illustrates the merging together of fins 120 to form fin template 135:



Id., Fig. 4 (annotated); EX2005-McAlexander-Decl, ¶65. Xu explains that “[t]hough the fins 120 and fin template 135 are depicted separately, it is understood that ‘fin template’ can refer to the newly grown epi semiconductor material alone (depicted as fin template) or the newly grown epi semi-conductor material combined with the initial fins (depicted as fins 120). EX1004-Xu, 5:28-33. Thus, a POSITA would

have understood that Xu's device's "fin structure" includes both fins 120 and fin template 135, which merges adjacent fin structures 115A and 115B. EX2005-McAlexander-Decl, ¶66.

As shown in Figure 4 above, Xu's fin template 135 is disposed on top of isolation features 130. As such, Xu's "isolation features 130" do not surround its fin structure because it does not enclose *any* side of the merged fin structure, *e.g.*, the part made up of fin template 135. EX2005-McAlexander-Decl, ¶67.

Accordingly, Xu does not disclose "an isolation structure . . . surrounding the fin structure, as required by all challenged claims." The Petition also alleges that Xu renders obvious this limitation but does not provide any explanation or analysis on this point. Pet. at 16-17. Thus, Grounds 1A and 1B fail.

**2. Grounds 2A-C: Ching Fails To Disclose Or Render Obvious
"An Isolation Structure, Disposed On The Surface Of The
Substrate And Surrounding The Fin Structure"**

The Petition alleges that "Ching discloses 'STI regions 22' (magenta) disposed on the surface of substrate 20 (green) and surrounding the 'semiconductor strip 21' (blue) as shown in Figure 1." Pet. at 56.

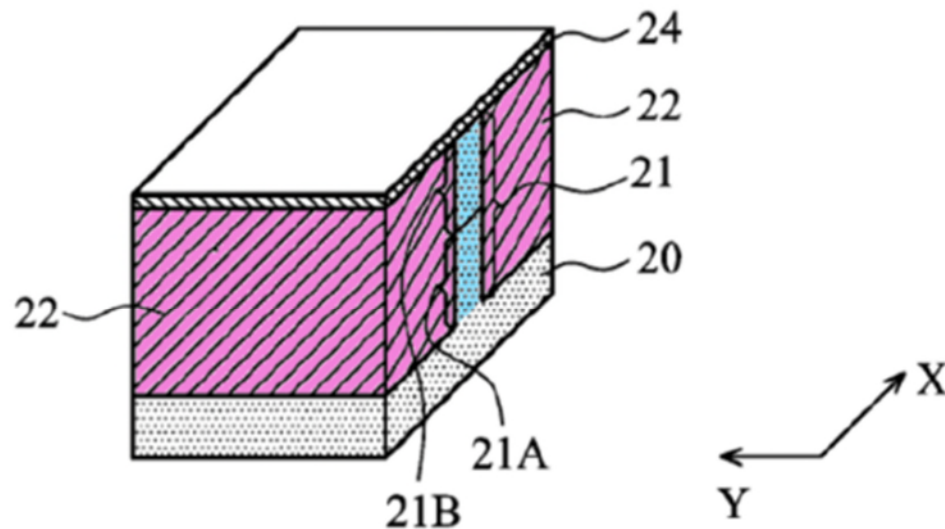


Fig. 1

Pet. at 57 (showing annotated EX1005-Ching, Fig. 1). However, as shown in Figure 1 above, Ching's STI regions 22 do not surround the alleged fin structure (semiconductor strip 21) on all four sides, but rather only cover two sides of semiconductor strip 21.

As explained above with respect to Xu, a POSITA would have understood that in the '609 patent's claimed semiconductor device, the isolation structure surrounds the fin structure on all four sides. EX2005-McAlexander-Decl, ¶71; *see also* EX2004. In contrast, in Ching, STI regions 22 only cover two sides of the alleged fin structure. This is apparent from Ching's description of the STI regions, which explains that "semiconductor strip 21 may be formed by etching a portion of

the original substrate 20 **between** STI regions 22, and epitaxially growing semiconductor strip 21 between STI regions 22.” EX1005-Ching at 2:23-27 (emphasis added). That is, as illustrated in Ching’s Fig. 1, “STI regions 22” are two distinct regions that do not merge, and semiconductor strip 21 is etched between the two regions, such that STI regions 22 only cover two sides of the semiconductor strip 21. *Id*; EX2005-McAlexander-Decl, ¶71. This is different from the ’609 patent’s device, in which “a lower portion of each fin structure 12 is **embedded** in the isolation structure 20.” EX1001 at 3:52-53 (emphasis added). Thus, Ching does not disclose “an isolation structure, disposed on the surface of the substrate and surrounding the fin structure,” as required by the challenged claims.

The Petition argues that “[t]o the extent the claim language requires the isolation structure to *fully* circle the fin structures . . . Ching discloses and renders this obvious as well.” Pet. at 59. The Petition argues that “[a] POSITA would have further understood that, in Ching, the shallow trench isolation regions (‘STI regions 22’) isolate ‘semiconductor strips 21’ from one another *and* isolate the transistors that will ultimately be formed from ‘semiconductor strips 21’ from one another.” *Id*. But this argument is circular and conclusory. A POSITA would have understood that Ching’s STI regions would only “isolate the transistors that will ultimately be formed from semiconductor strips 21 from one another”—as the Petition argues—if

they surround the semiconductor strips (on all four sides). EX2005-McAlexander-Decl, ¶72. The Petition’s argument thus merely states the conclusion that a POSITA would have understood that STI regions surround the semiconductor strips. But this conclusion is wholly unsupported by Ching’s disclosure. Indeed, Ching actually ***contradicts*** the Petition’s argument, stating that “semiconductor strip 21 is formed ***between, and contacting, neighboring STI regions*** 22.” EX1005-Ching at 2:5-6 (emphasis added). As explained above, that Ching’s semiconductor strips are formed between neighboring STI regions demonstrates that the STI regions do not surround the semiconductor strips, because the STI regions would need to merge in order to enclose the semiconductor strips on all four sides. EX2005-McAlexander-Decl, ¶72. Tellingly, the Petition does not cite to any part of Ching in making its obviousness argument, instead citing only its expert’s declaration. Pet. at 59 (citing EX1003 at ¶165). But the expert provides no analysis to support the Petition’s conclusion, instead simply stating the same conclusory argument as the Petition. EX1003 at ¶165. Such “conclusory expert testimony is inadequate to support an obviousness determination.” *TQ Delta, LLC v. CISCO Sys., Inc.*, 942 F.3d 1352, 1359 (Fed. Cir. 2019).

Accordingly, Ching does not disclose or render obvious “an isolation structure . . . surrounding the fin structure, as required by all challenged claims.” Thus, Ground 2A fails.

Ground 2B adds Xu to address additional limitations of dependent claims 2 and 4, which depend from independent claim 1. Pet. at 73-82. Ground 2B does not provide any further analysis regarding claim 1. *Id.* Similarly, Ground 2C adds Huang to address additional limitations of dependent claim 7, which depends from independent claim 1. Pet., 82-85. Ground 2C does not provide any further analysis regarding claim 1. *Id.* Thus, Grounds 2B and 2C fail for the same reasons as Ground 2A.

B. Grounds 1A and 1B Fail To Disclose Or Render Obvious “A Recess Formed At One End Of The Fin Structure, Wherein The Epitaxial Structure Fills Up The Recess” (Claim 5)

1. The Petition Relies On Two Separate And Incompatible Embodiments In Xu For “Wherein the Isolation Structure Under The Gate Structure Has A First Top Surface And The Isolation Structure At Two Sides Of The Gate Structure Has A Second Top Surface” (Claim 1) And ““A Recess Formed At One End Of The Fin Structure” (Claim 5)

Challenged claim 5 recites: “The semiconductor device according to claim 1, further comprising a recess formed at one end of the fin structure, wherein the epitaxial structure fills up the recess.” Thus, the device of claim 5 must comprise all elements of claim 1 and “a recess formed at one end of the fin structure.” As the

Petition concedes, Xu does not disclose an embodiment satisfying both “wherein the isolation structure under the gate structure has a first top surface and the isolation structure at two sides of the gate structure has a second top surface”—as recited in claim 1—and “a recess formed at one end of the fin structure.” Pet., 31. The Petition acknowledges that Figures 1-6 constitute a first embodiment in which an isolation structure is etched, and that Figures 7-11A constitute a second embodiment in which a recess in the fin structure is formed. Pet., 31. Xu itself refers to these two embodiments as distinct approaches and different methods. EX1004-Xu, 1:49-58 (“FIG. 1 is a flow chart of **a method** for fabricating a fin-like field effect transistor (FinFET) device according to aspects of the present disclosure”; “FIG. 7 is a flow chart of **another method** for fabricating a FinFET device according to aspects of the present disclosure.”).

The Petition argues that “[i]t would have been obvious to a POSITA to combine the recess-and-fill of Xu’s second embodiment with Xu’s first embodiment such that the first embodiment includes an epitaxial structure filling the recess.” Pet., 31. The Petition’s rationale for such a combination is that it would “result in achieving and optimizing strain.” Pet. 31-32 (cleaned up). The Petition’s argument is that in the second embodiment, “by controlling source and drain trench depth—which is dictated by the depth of the recess—strain for both PMOS and NMOS

FinFET devices can be achieved and optimized and different types of strain can be achieved.” Pet., 31 (citing EX1004-Xu, 15:56-66) (internal quotations omitted). However, this method for achieving strain is incompatible with the first embodiment, which has no fin trench. EX2005-McAlexander-Decl, ¶77. Indeed, the first embodiment, Figures 1-6, describes a different and incompatible method of achieving strain from that of the second embodiment that the Petitioner seeks to add to the first embodiment. *Id.* In the first embodiment, starting with Figure 2, the isolation structure is etched to arrive at Figure 3:

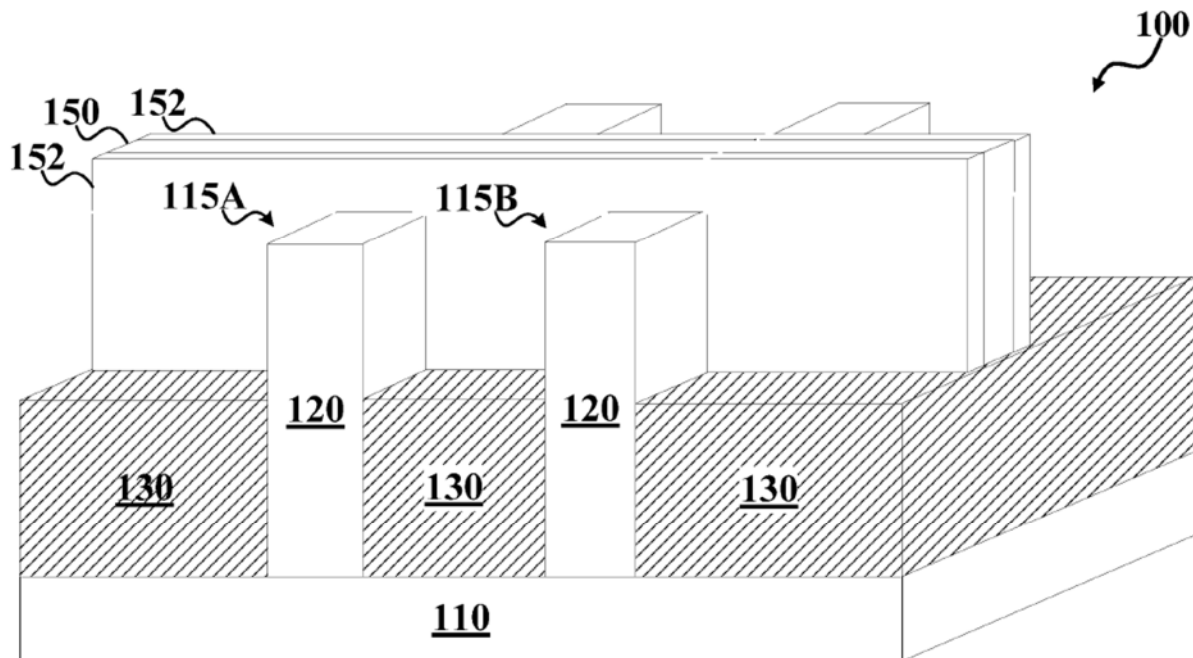


FIG. 2

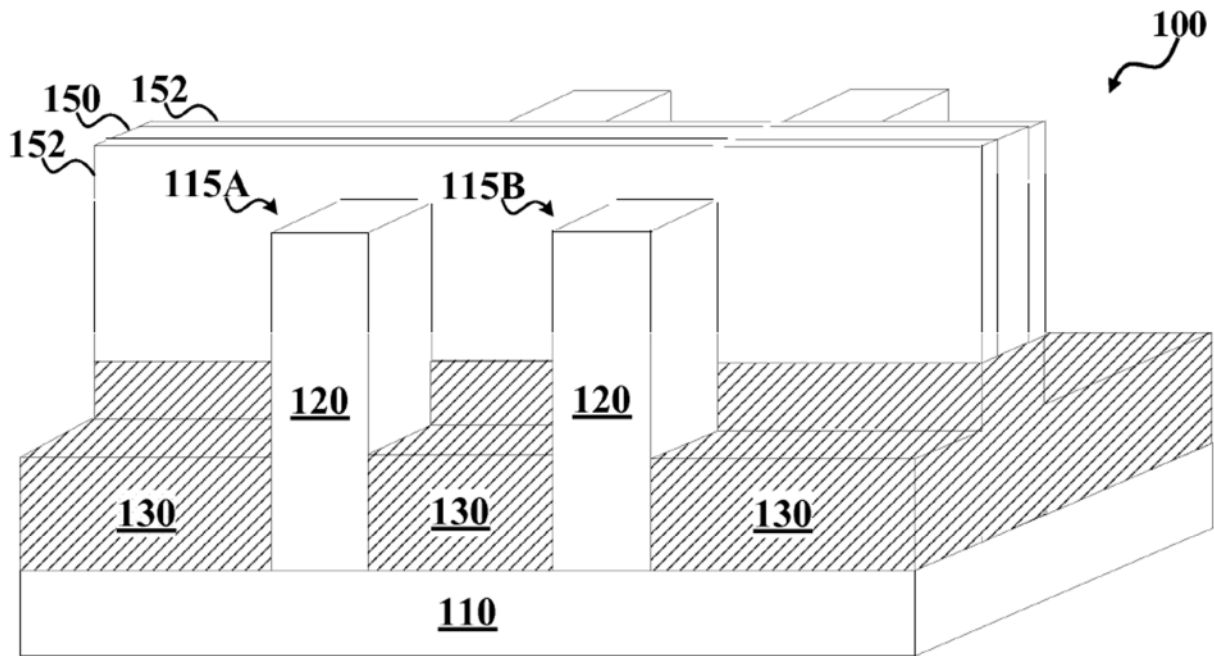


FIG. 3

EX1004-Xu, Figs. 2 and 3; EX2005-McAlexander-Decl, ¶77. Then, “a fin template 135 is formed on exposed portions of the fins 120.” EX1004-Xu, 5:1-2.

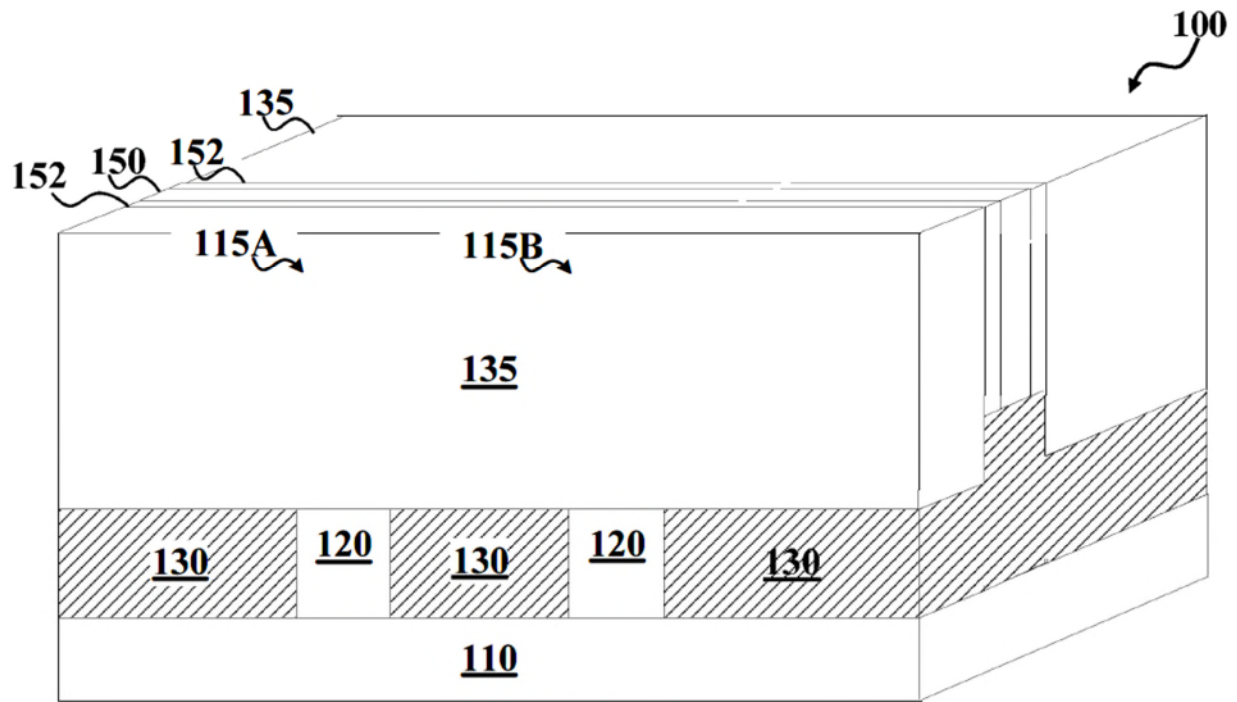


FIG. 4

Id., Fig. 4; EX2005-McAlexander-Decl, ¶78. Then, in Figure 5, “a process is performed to recess the fin template 135” from what is shown in Figure 4:

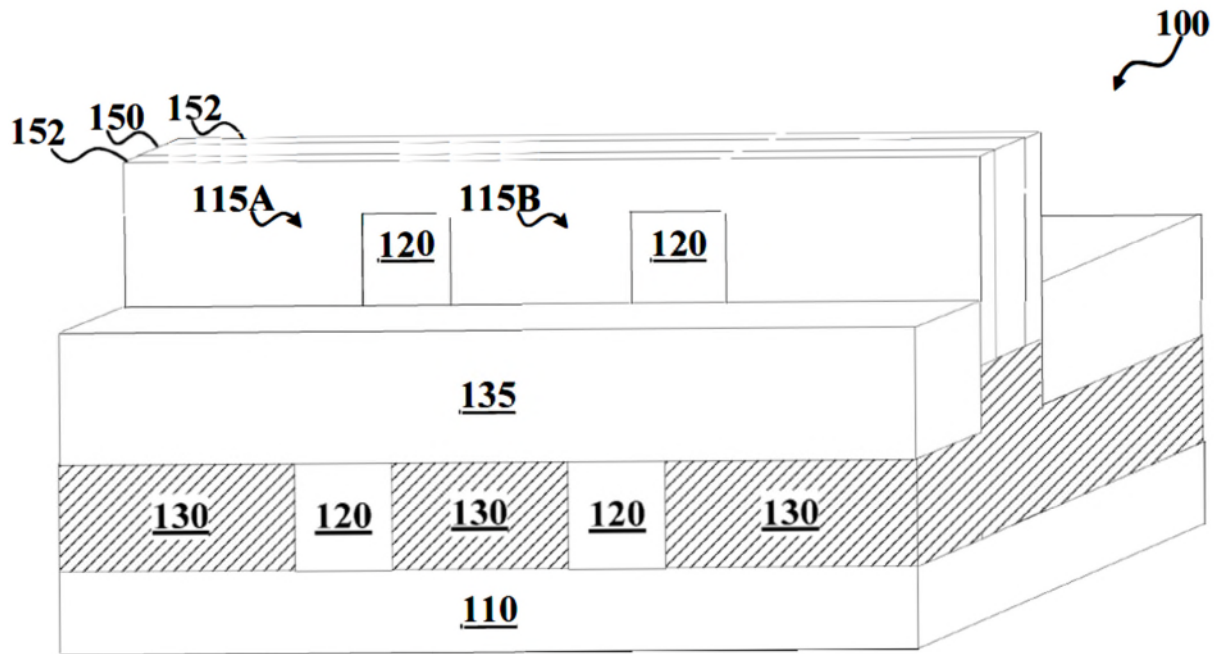


FIG. 5

EX1004-Xu, 5:34-35, Fig. 5; EX2005-McAlexander-Decl, ¶79. Specifically, “[t]he fin template 135 is etched back sufficiently to expose the channels of the fin structures 115A and 115B,” as illustrated in FIG. 5. *Id.*, 5:43-45; Fig. 5. As Xu states, “[t]his ensures that later-formed raised source and drain features (semiconductor material 160) **can effectively introduce strain** into the channels of the fin structures 115A and 115B.” *Id.*, 5:45-47.

This process, as shown above, removes part of the fin structure, but notably, as the Petition concedes, it does not meet the claim requirement to “form[] a recess in the fin structure at a side of the gate structure.” Pet. 20-26; EX2005-McAlexander-Decl, ¶81.

Then, in Figure 6, “a semiconductor material 160 is epitaxially grown over the fin template 135. In the depicted embodiment, a semiconductor material is epi grown on the exposed fin template 135 in the source and drain regions of the fin structures 115A and 115B”:

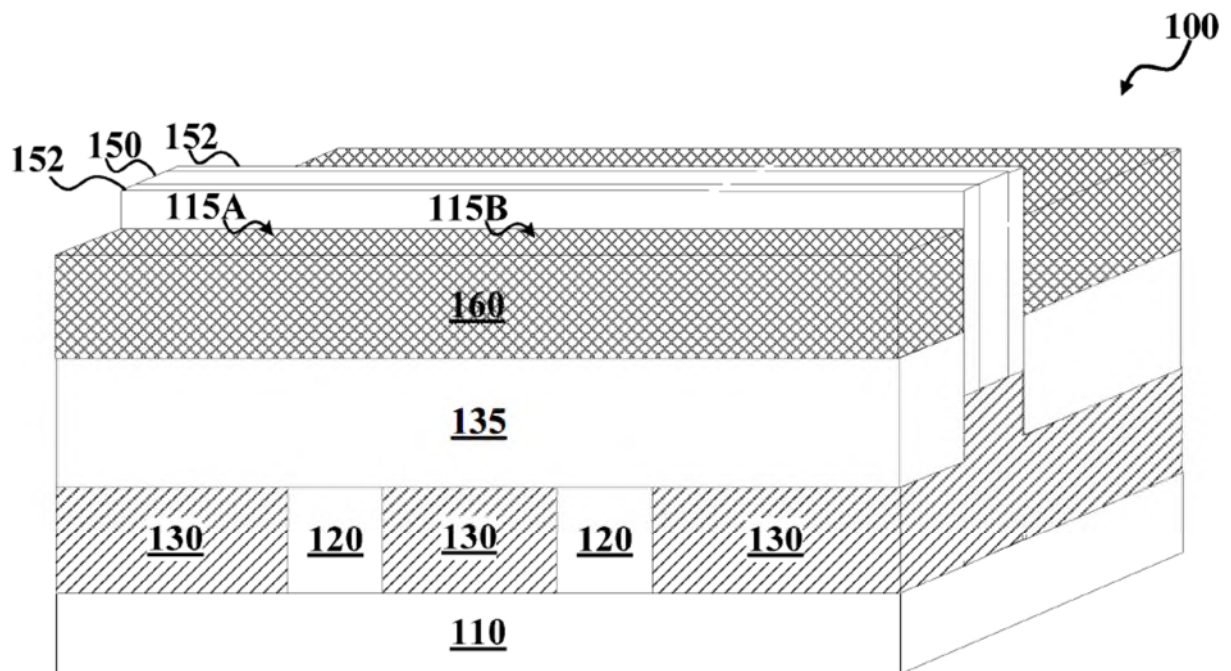


FIG. 6

EX1004-Xu, 5:49-53; Fig. 6. Xu explains that “[t]he epi grown semiconductor material 160 **generates channel strain** for the fin structures 115A and 115B.” *Id.*, 5:53-55 (emphasis added); EX2005-McAlexander-Decl, ¶83. As Xu therefore states, the semiconductor material 160 generates channel strain, not the depth of the trench, which does not exist in the first embodiment. *Id.*

Thus, in the first embodiment, the source and drain depth is controlled by etching the isolation structure and fin template to a certain depth, which allows for effective introduction of channel strain. In contrast, in the second embodiment, the source and drain depth is controlled by forming a recess in the fins. EX1004-Xu, 15:56-16:2. A POSITA would therefore have no reason to combine the two embodiments, as each embodiment provides different methods to control the source and drain depth to achieve effective channel strain. EX2005-McAlexander-Decl, ¶84. Petitioner's assertion to the contrary is merely a post-hoc rationalization to justify combining two distinct embodiments of Xu.

2. Xu Does Not Disclose Or Render Obvious “Wherein The Epitaxial Structure Fills Up The Recess”

The Petition alleges that Xu's “fin template” (the alleged epitaxial layer) fills up the recess. Pet., 30-31. As with other elements, the Petition improperly combines different aspects of different embodiments. However, even in the alleged modification, Xu's “fin template” does not “fill[] up the recess,” as required by claim 5. The Petition alleges that Xu discloses an “etching process [which] forms recesses in fin structure 215A, 215B, at one end of the fin structure”:

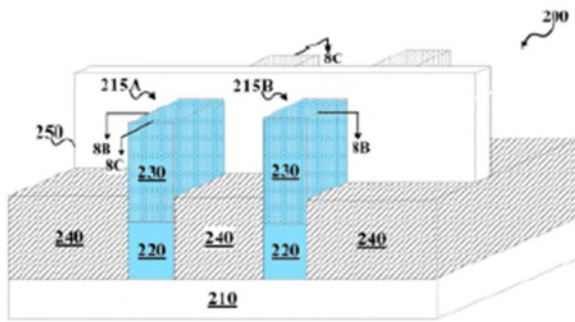


FIG. 8A

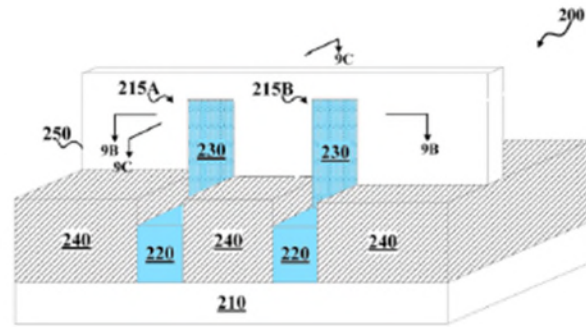
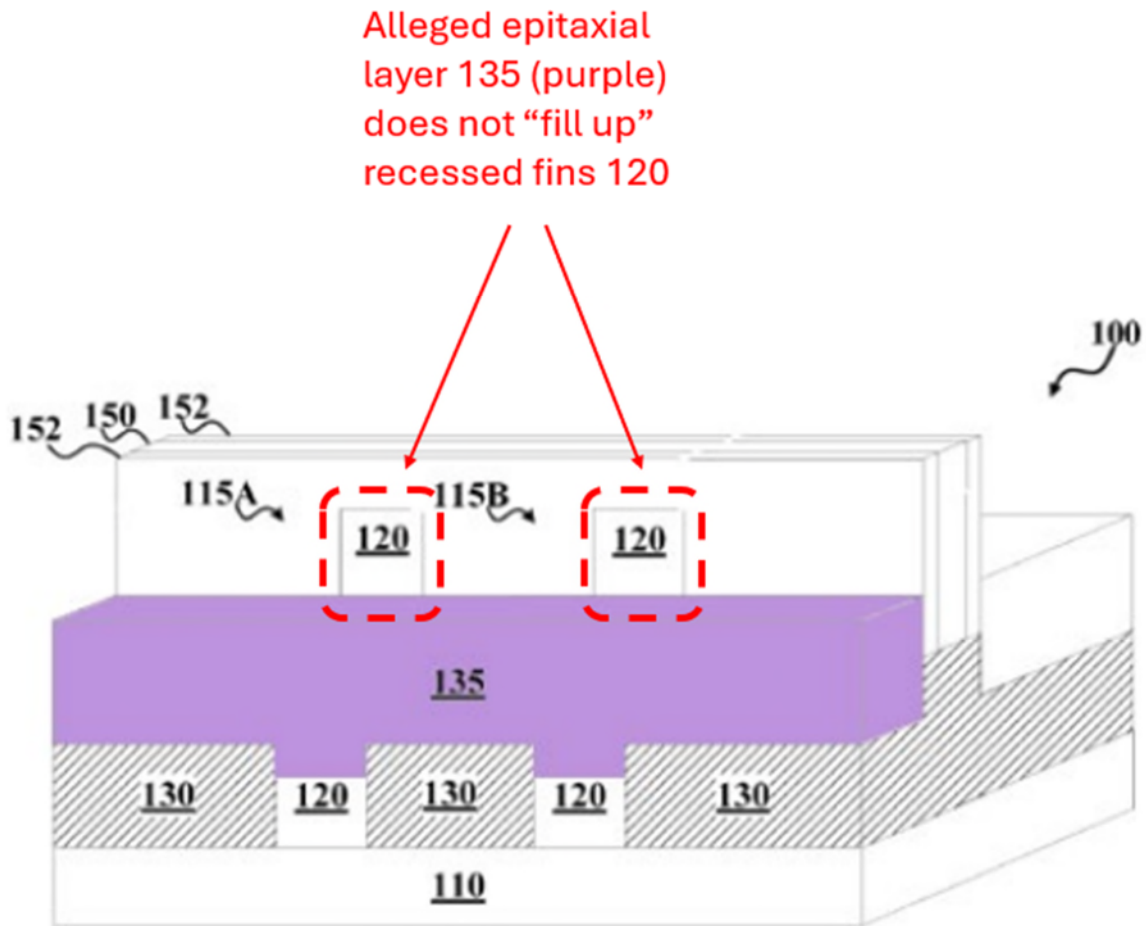


FIG. 9A

Pet., 30 (annotated EX1004-Xu, Figs. 8A and 9A). As shown, the Petition's alleged recess (colored in blue above) includes the exposed portions of the fin under the gate structure. *Id.* However, as shown in the figure below (annotated and modified in the Petition), Xu's "fin template" does not fill up the recesses, as the fin template does not extend to the top of the alleged recess:

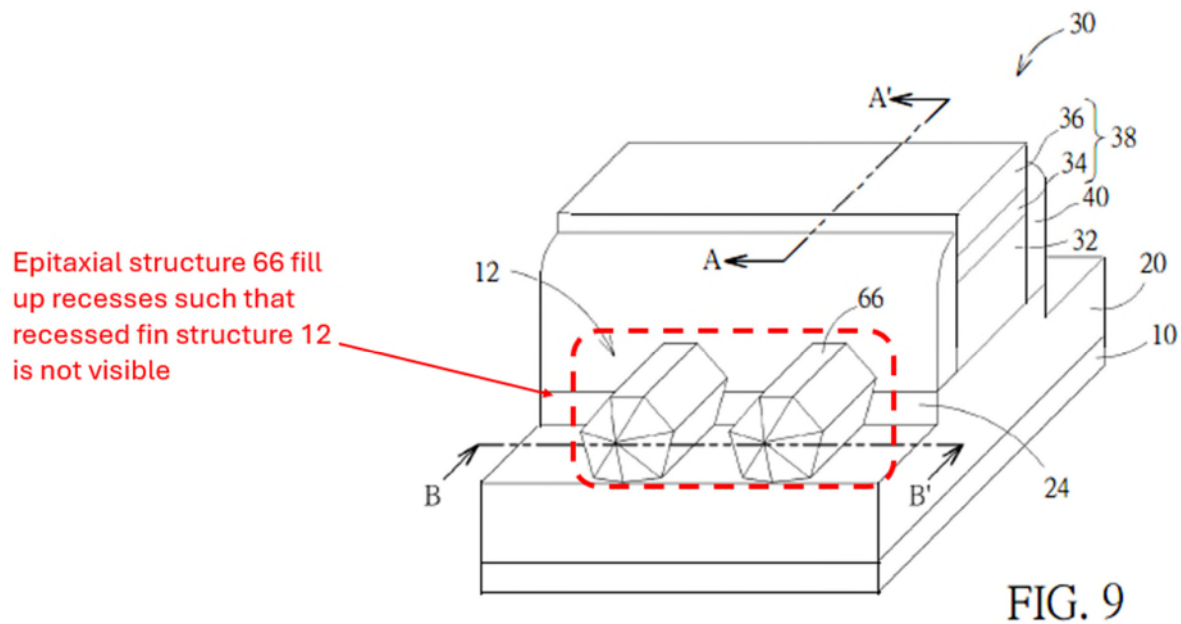


Pet., 35 (showing annotated and modified figure, further annotated here). As shown, the alleged epitaxial layer does not extend vertically to the top of the recess, as evidenced by the fact that the tops of the fins 120 are visible over the top of the fin template 135.

This is in contrast with challenged claim 5, which requires that “the structure fills up the recess.” The ’609 patent specification explains that “[m]ore precisely, each epitaxial structure 66 may *completely cover the bottom surface 68 and*

sidewalls 70 of the corresponding recess 60.” EX1001, 6:39-41 (emphasis added).

As shown in Figures 9 and 10 below, this means that epitaxial structures 66 completely fill up the recess 60, such that the unrecessed portions of the fins are covered by the epitaxial structure:



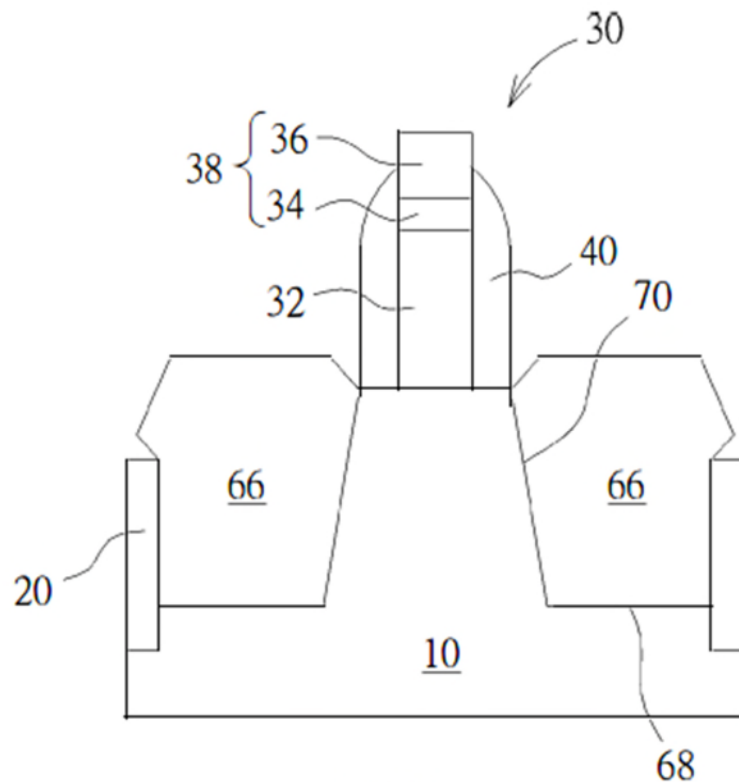


FIG. 10

Id., Figs. 9 (annotated) and 10; *see also* EX2005-McAlexander-Decl, ¶88.

Accordingly, Ground 1A fails to disclose or render obvious claim 5, as well as claim 6, which depends from claim 5. Similarly, Ground 1B fails to disclose or render obvious claim 7 for the same reasons, because claim 7 depends from claim 6.

C. Grounds 1B and 2C Fail Because A POSITA Would Not Have Been Motivated To Combine Either Xu Or Ching With Huang To Render Obvious Claim 7's Recited Range

1. A POSITA Would Not Have Been Motivated To Combine Either Xu Or Ching With Huang Because Huang Uses An Entirely Different Process Architecture

The Petition's Grounds 1B and 2C rely on Huang to supply the dimensional specificity that Xu and Ching respectively lack for claim 7's height-difference limitation of 100 to 250 Angstroms. Pet., 43-50, 82-85. But Huang employs a “Fin-Last” process architecture that is structurally and sequentially distinct from the “Fin-First” architectures of both Xu and Ching. A POSITA would have recognized that this difference is technically significant and therefore would not have even considered—much less been motivated—to look to Huang to modify either Xu or Ching, because the architectures of Xu and Ching are not compatible with that of Huang. EX2005-McAlexander-Decl, ¶90.

a. Huang's Fin-Last Fabrication Process Differs From the Fin-First Sequences Of Xu And Ching

Huang expressly describes “various stages in the manufacture of a **Fin-Last** FinFET device.” EX1006-Huang, 2:20-22 (emphasis added); EX1003, ¶72. In Huang's Fin-Last process, the fabrication sequence proceeds as follows: (1) semiconductor strips 24 are formed by patterning the substrate to a height of “about 10 nm to about 500 nm” (EX1006-Huang at 2:45-46, 2:56-59); (2) a dielectric layer

22 is blanket-deposited and planarized “until the tops of the semiconductor strips are exposed” (*id.* at 3:7-8, 3:17-27); (3) recesses 36 are etched in the semiconductor strips to a depth of “about 5 nm to about 25 nm” in a “strained source drain (SSD) etch step” (*id.* at 4:10-16); (4) epitaxial source and drain regions are grown in those recesses (*id.* at 4:30-34); and then—critically—(5) the fins are defined after the epitaxial growth by “etching or recessing the dielectric layer 22 surrounding the semiconductor strips 24” to form fins 29 (*id.* at 4:62-64). To illustrate, Huang’s Fig. 2B illustrates the device after semiconductor strips 24 are formed and the dielectric layer 22 is planarized:

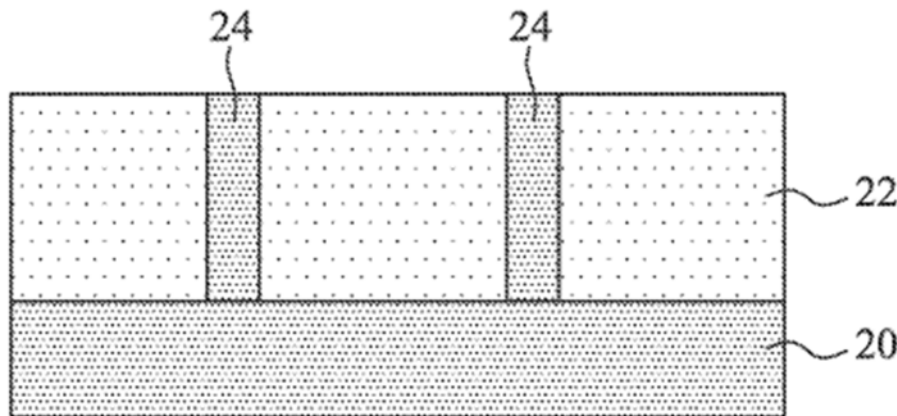


Fig. 2B

EX1006-Huang, Fig. 2B; EX2005-McAlexander-Decl, ¶91. Then, as shown in Fig. 3B, the semiconductor strips 24 are etched to form recesses 36:

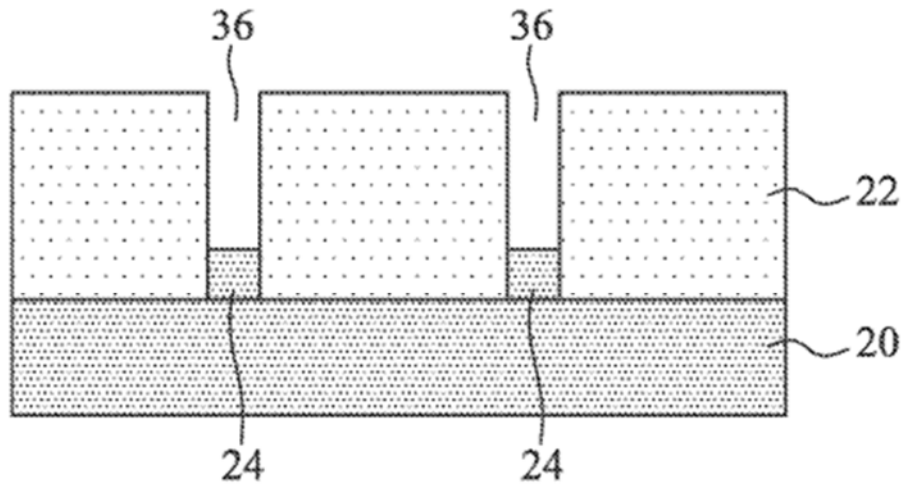


Fig. 3B

EX1006-Huang, Fig. 3B; EX2005-McAlexander-Decl, ¶92. Then, as shown in Fig. 4B, source and drain regions 28 are epitaxially grown in the recesses:

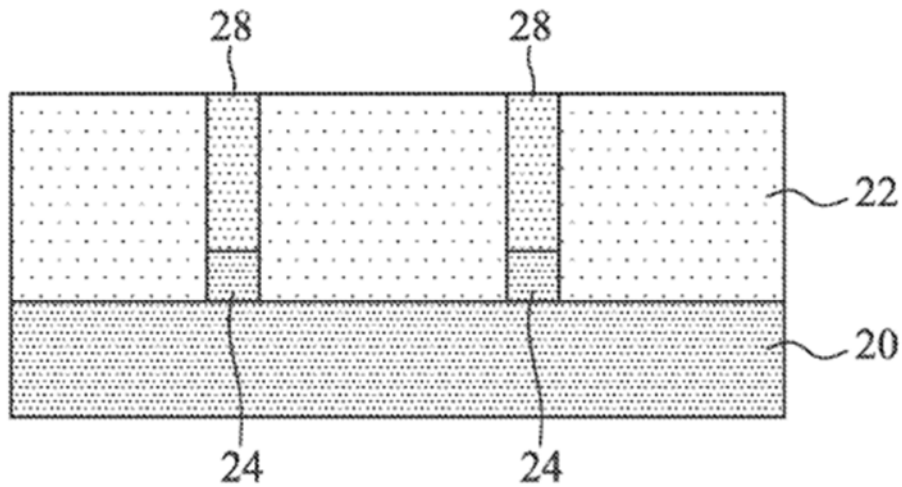


Fig. 4B

EX1006-Huang, Fig. 3B; EX2005-McAlexander-Decl, ¶93. Thus, as shown by the figures above, in Huang's device, at the time the epitaxial source/drain regions are formed, the dielectric layer 22 remains at the full, planarized height. EX2005-McAlexander-Decl, ¶94.

In contrast, both Xu and Ching employ Fin-First architectures in which the fins are defined before the source/drain epitaxial growth occurs. EX2005-McAlexander-Decl, ¶95. For example, in Ching, semiconductor strip 21 is formed in substrate 20 between STI regions 22, a dummy gate (polysilicon layer 26 and hard mask 28) is deposited, an STI recess is performed, and only thereafter are the semiconductor strips recessed and epitaxy regions 36 grown from recesses 32. EX1005-Ching at 2:1-13, 2:35-39, 2:59-67, 3:20-32. To illustrate, Ching's Figures 2 and 3 show that STI regions 22 (the alleged isolation structure) are etched to define protruding fins (semiconductor strips 21) before formation of a recess:

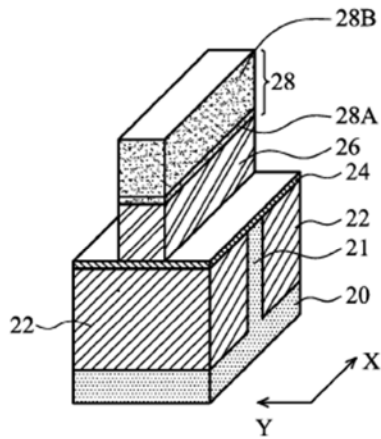


Fig. 2

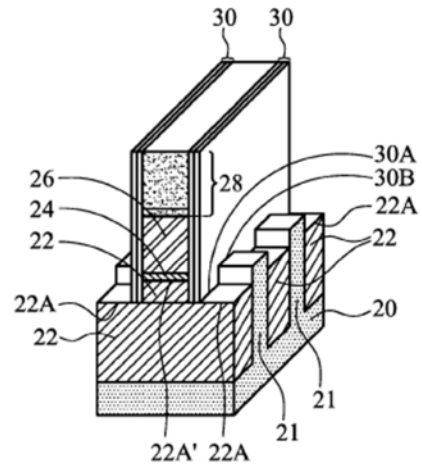


Fig. 3

EX1005-Ching, Figs. 2 and 3; EX2005-McAlexander-Decl, ¶95. Then, as shown in Figures 4 and 5, recesses 32 are formed and epitaxy regions 36 are formed in the recesses:

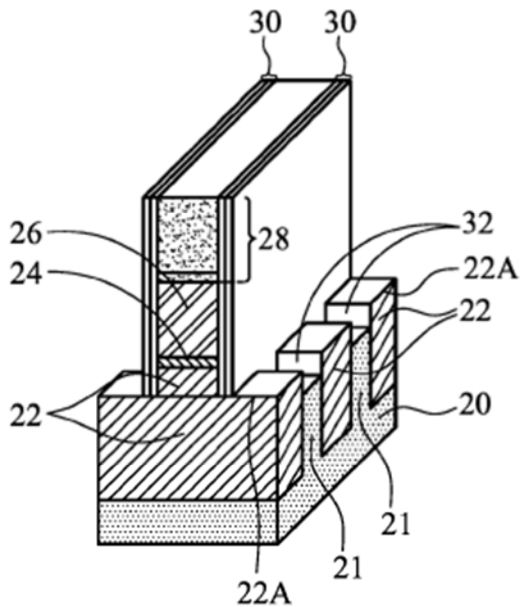


Fig. 4

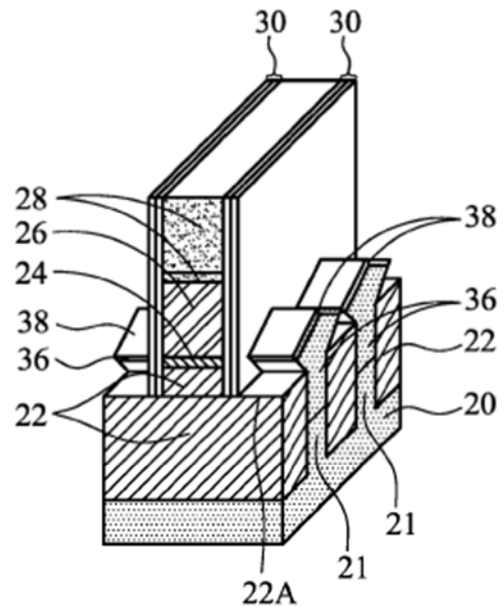


Fig. 5

EX1005-Ching, Figs. 2 and 3; EX2005-McAlexander-Decl, ¶96. Similarly, in Xu, fin structures 115A and 115B are first formed from the substrate, then isolation features 130 are deposited, a gate structure 150 is formed over the fins, and the isolation features are etched. EX1004-Xu at 3:9-10, 3:54-58, 3:66-4:1, 4:54-56. Only then does Xu perform the epitaxial growth steps. *Id.* at 5:1-15, 5:49-55.

Thus, the fundamental sequencing difference is clear: in the Xu and Ching, epitaxial growth occurs in a recess formed within an already-defined fin, and below the already-etched isolation regions. EX2005-McAlexander-Decl, ¶98. In Huang, epitaxial growth occurs in a recess at the top of a semiconductor strip that is still fully encased in dielectric up to the strip's top surface. *Id.*

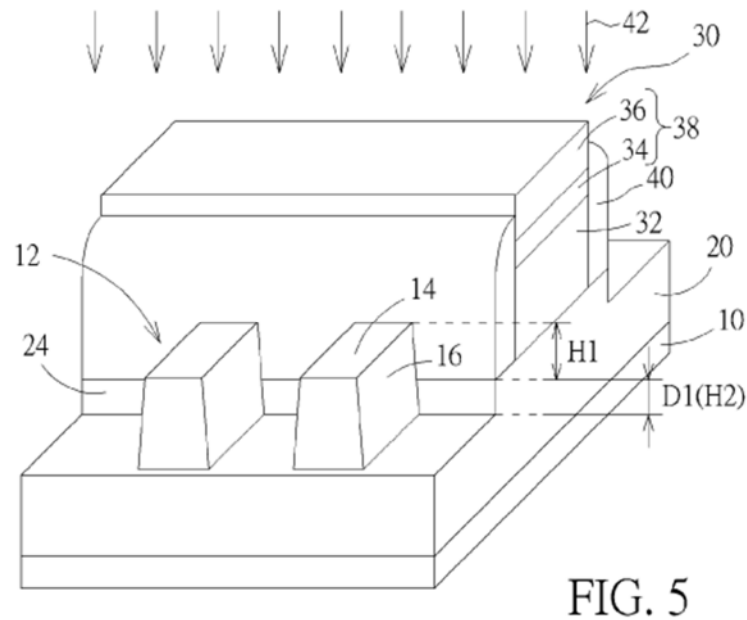
b. A POSITA Would Have Recognized These Differences As Technically Significant

The Fin-Last versus Fin-First distinction is not a mere labeling difference. Rather, it results in fundamental differences in device geometry that render dimensional parameters from one architecture inapplicable to the other. EX2005-McAlexander-Decl, ¶99. A POSITA would have understood that the structural context in which the epitaxial recess depth operates differs materially between the two architectures. *Id.* For example, in Xu and Ching's Fin-First processes, the recess depth determines the height difference between the bottom of the epitaxial structure and the bottom of an isolation structure that has already been etched to a lower level

outside the gate region. EX2005-McAlexander-Decl, ¶99. The isolation structure's top surface has been etched before the epitaxial growth occurs. See EX1004-Xu at 4:54-61; EX1005-Ching at 2:59–67. In this configuration, the recess depth interacts with the already-recessed isolation structure to define the aspect ratio of the epitaxial growth cavity. EX2005-McAlexander-Decl, ¶99. As noted in the '609 Patent, this aspect ratio is a parameter that is directly relevant to whether void defects will occur during epitaxial filling, because “the aspect ratio of the epitaxial layer [] get[ting] higher . . . often incur[s] unwanted defects, such as void defects in the epitaxial layer.” EX1001 at 2:6-15.

In contrast, in Huang's Fin-Last process, the dielectric layer remains at its full planarized height at the time of epitaxial growth. EX1006-Huang at 3:17-27, 4:10-34. The semiconductor strips are recessed only a shallow depth (5-25 nm) while the surrounding dielectric extends to the full strip height (10-500 nm). *Id.* at 2:56-59, 4:15-16. The epitaxial material therefore grows within a relatively open, unconstrained geometry—the dielectric still extends well above the bottom of the recess on both sides. EX2005-McAlexander-Decl, ¶100. The aspect ratio of the growth cavity is thus entirely different from that in Fin-First devices, where the isolation has already been partially etched down. *Id.*

To illustrate, in the '609 Patent, which also uses a Fin-First process, Figure 5 shows the isolation structure 20 etched before the recesses are formed:



EX1001, Fig. 5; EX2005-McAlexander-Decl, ¶101. Then, as shown in Figure 6, recesses 60 are formed:

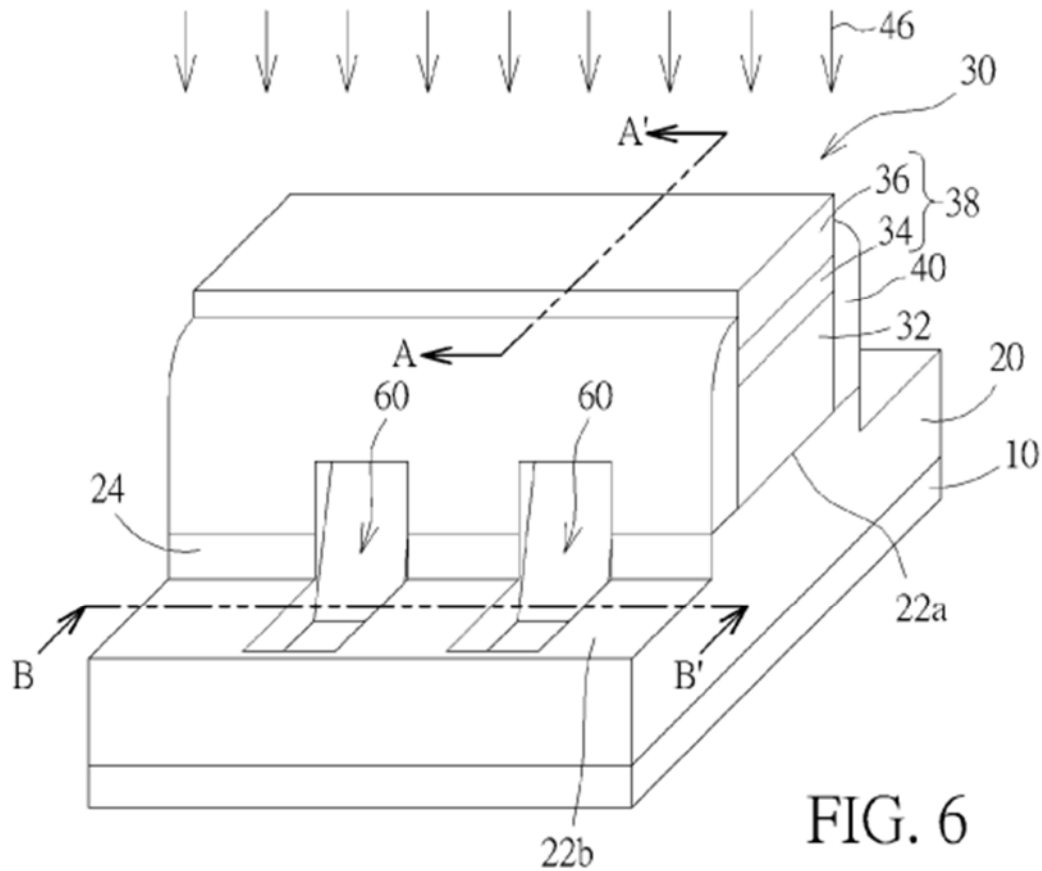


FIG. 6

EX1001, Fig. 6; EX2005-McAlexander-Decl, ¶102. Because the isolation structure 20 was already etched prior to forming the recesses, the aspect ratio of the recesses is relatively shallow. EX2005-McAlexander-Decl, ¶103.

On the other hand, in Huang, the aspect ratio of the epitaxial growth cavity is relatively higher because dielectric layer 22 has not been etched before formation of the recesses 36:

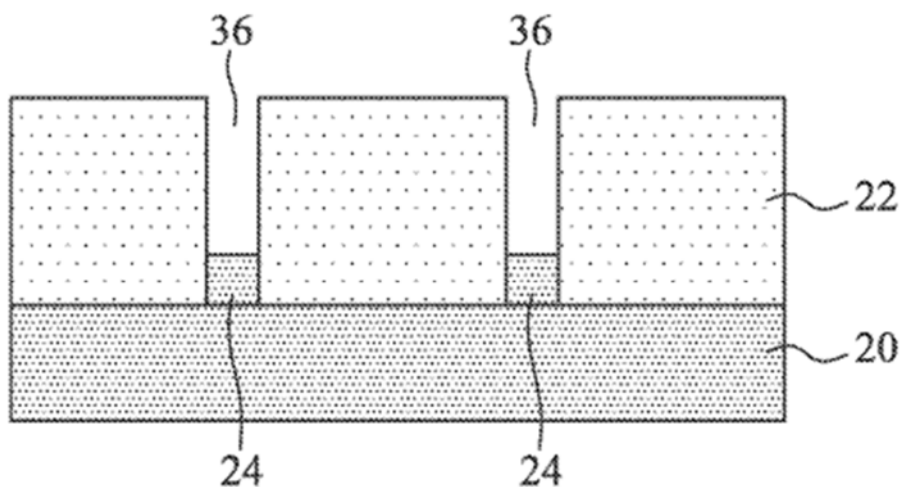


Fig. 3B

EX1006-Huang, Fig. 3B; EX2005-McAlexander-Decl, ¶104. Then, source and drain regions 28 are epitaxially grown in the recesses 36:

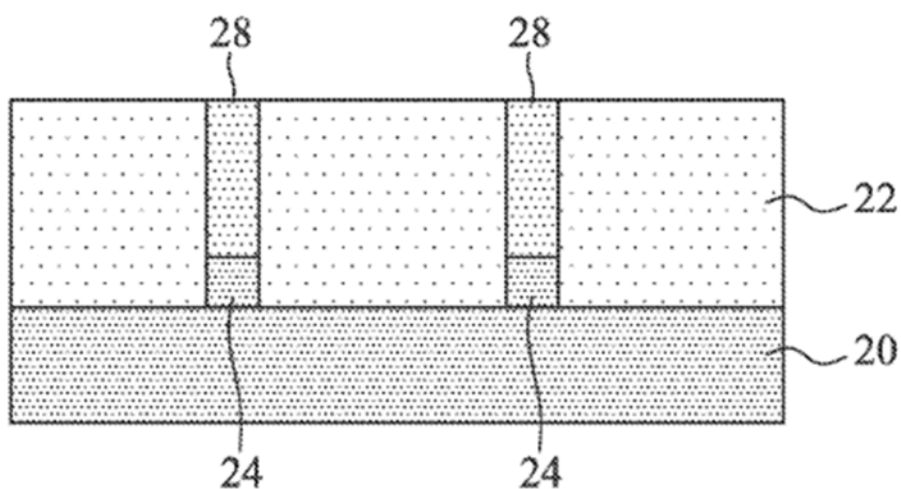


Fig. 4B

EX1006-Huang, Fig. 4B; EX2005-McAlexander-Decl, ¶105. Only then is the dielectric layer 22 etched down to reveal the fins:

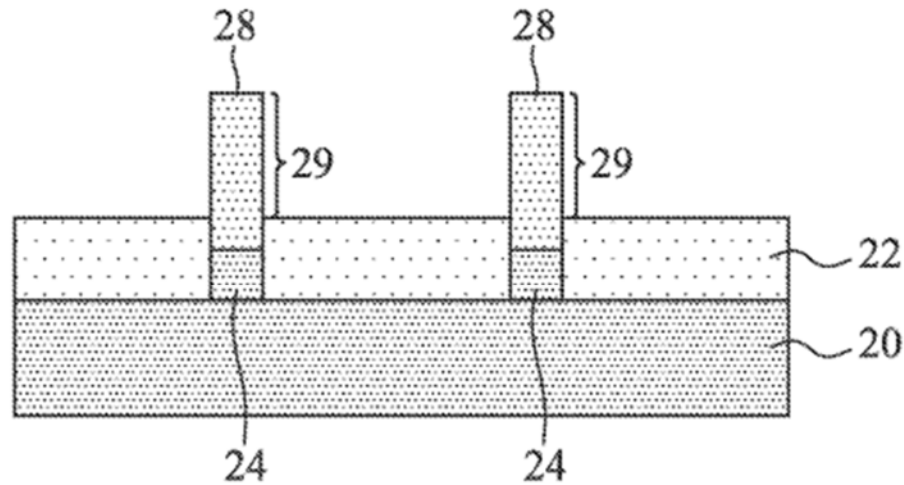
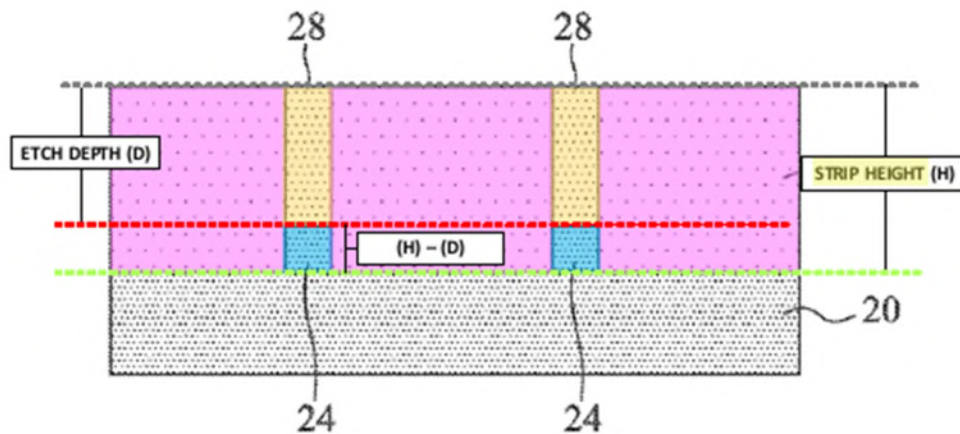


Fig. 5B

EX1006-Huang, Fig. 5B; EX2005-McAlexander-Decl, ¶106. Because Huang's fins are revealed (by etching the dielectric layer) only after the epitaxial growth, the height difference between the epitaxial bottom surface and the dielectric bottom surface ($H - D$, per the Petition at 46-47) reflects a geometry that does not exist in the Fin-First architecture:



Pet., 46 (showing annotated EX1006-Huang, Fig. 4B). In contrast, in Xu and Ching, the height difference between the bottom of the epitaxial structure and the bottom of the isolation structure (which is the height difference described in challenged claim 7) is measured **after** the alleged isolation structure has undergone multiple etching steps. EX2005-McAlexander-Decl, ¶108. In contrast, in Huang, the measurement is taken at an intermediate fabrication stage before the fin is even formed—the dielectric is subsequently recessed to form fins 29 (EX1006-Huang at 4:62–64), which alters the very dimensional relationships from which the Petition seeks to draw guidance.

A POSITA would have understood that the epitaxial growth conditions—including susceptibility to void defects—are governed by the geometry at the time of the epitaxial growth, not by post-growth processing (such as Huang’s subsequent etching of the dielectric layer). EX2005-McAlexander-Decl, ¶109. A POSITA would have further understood that because the epitaxial grown cavity geometry

differs between Fin-First and Fin-Last architectures at the moment of epitaxial deposition, a recess depth that produces void-free growth in one architecture does not necessarily produce the same result in the other. *Id.*

c. These Architectural Differences Defeat The Petition's Asserted Motivation To Combine

Because Huang's Fin-Last architecture produces fundamentally different structural relationships than the Fin-First architectures of Xu and Ching, the Petition fails to establish the required motivation to combine. The Petition's only articulated motivation is that “both [Xu/Ching] and Huang are directed to FinFET devices and methods” and “are aimed at keeping up with the increasing down-scaling of integrated circuits and semiconductor devices.” Pet. at 50, 84; EX1003 at ¶¶146, 217. This is legally insufficient.

The Supreme Court has held that an “identifiable reason” is required for a POSITA to combine references, not merely that references exist in the same general field. *KSR International Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2007). An obviousness analysis based solely on subject-matter overlap—such as the Petition’s argument that both references are “FinFET” patents—would permit combining any two FinFET references. That is precisely the kind of unfocused, hindsight-based reasoning that the motivation-to-combine requirement is designed to prevent. See *id.* at 421 (cautioning against “the distortion caused by hindsight bias”).

Here, the Petition offers no specific, articulable reason why a POSITA working with Xu's or Ching's Fin-First device architecture would have looked to a Fin-Last reference for dimensional guidance. A POSITA seeking to optimize the recess depth in a Fin-First device—where the epitaxial structure must grow within a confined cavity adjacent to a gate structure and between partially-etched isolation sidewalls—would naturally look to other Fin-First references for dimensional guidance, or would calibrate the etch depth based on the specific geometry of the primary reference's own device. EX2005-McAlexander-Decl, ¶112. A POSITA would not have imported parameters from a Fin-Last reference such as Huang, in which the dimensional context is different. *Id.*

The Petition's reliance on *In re Aller*, 220 F.2d 454, 456 (CCPA 1955), is equally unavailing. Pet., 45, 48, 84. *In re Aller* applies “where the general conditions of a claim are disclosed in the prior art.” *In re Aller*, 220 F.2d at 456. But Huang does not disclose the “general conditions” of the claimed device—it discloses a different device with a different process sequence, different cavity geometry at the time of epitaxial growth, and different dimensional relationships in the completed structure. Thus, contrary to the Petition’s allegations, borrowing a dimension from Huang and inserting it into the fundamentally different structural context of Xu or Ching is not “routine experimentation.” Pet., 45, 48, 84. Rather, it

is an attempt to transplant a parameter across architectural boundaries without any showing that the parameter retains its significance or produces predictable results in the different context.

Indeed, even Petitioner's own expert implicitly acknowledges this defect. Dr. Lee's declaration does not identify any teaching in Huang that would direct a POSITA to apply Huang's 5-25 nm recess depth to a Fin-First device's recess. Instead, Dr. Lee merely asserts that a POSITA “would have found it obvious to turn to additional prior art, such as Huang, for concrete dimensional guidance.” EX1003-Lee-Decl, ¶¶146, 217. This is precisely the kind of “conclusory expert testimony” that is “inadequate to support an obviousness determination.” *TQ Delta, LLC v. CISCO Sys., Inc.*, 942 F.3d 1352, 1359 (Fed. Cir. 2019). Dr. Lee provides no analysis of why Huang's Fin-Last dimensions would be applicable to a Fin-First structure, no discussion of how the different cavity geometries affect the transferability of etch-depth parameters, and no explanation of how a POSITA would account for the fact that Huang's height difference is measured at an intermediate fabrication stage that does not correspond to the final device structure of Xu or Ching.

Accordingly, the Petition fails to articulate a sufficient motivation to combine Huang with either Xu or Ching in the manner contemplated by the Petition. Thus, Grounds 1B and 2C fail and claim 7 should be upheld.

2. A POSITA Would Not Have Been Motivated To Combine Either Xu Or Ching With Huang To Satisfy Claim 7's Recited Range

a. Huang Does Not Disclose The Claimed Range

Even setting aside the architectural incompatibility discussed above, Huang does not explicitly disclose the height difference of 100 to 250 Angstroms recited in claim 7. The Petition's alleged derivation of this dimension from Huang merely involves subtracting two independently disclosed ranges and then assuming, without any basis in Huang's text, that those ranges interact in the manner the Petition posits. *See* Pet., 46-47.

Specifically, Huang separately discloses two separate parameters: (1) that the semiconductor strips 24 “may have a height from about 10 nm to about 500 nm” (EX1006-Huang at 2:56–59); and (2) that the strained source drain etch depth “may be from about 5 nm to about 25 nm” (*id.* at 4:15–16). These two disclosed ranges are not linked or correlated within the reference. Rather, these disclosures appear in completely different sections of Huang, describe different process steps, and are not presented as interdependent variables. Huang does not state or suggest that a

particular strip height should be paired with a particular etch depth to achieve a target height difference, nor does Huang identify any functional reason why the difference of these values should be controlled to any specific value or range. A POSITA reading Huang would therefore have no basis to combine these two independent ranges into a derived dimensional parameter, much less to conclude that the resulting height difference should fall within the narrow 100–250 Angstrom window required by claim 7. EX2005-McAlexander-Decl, ¶118. The Petition's mathematical derivation is an exercise in hindsight reconstruction—impermissibly selecting two ranges from different portions of a reference and performing arithmetic to reverse-engineer a range that encompasses the claimed limitation—rather than a genuine teaching of Huang. *Id.*

For example, the Petition's calculation simply subtracts the lowest etch depth (5 nm) from the lowest strip height (10 nm) and the highest etch depth (25 nm) from the highest strip height (500 nm) to arrive at a computed “height difference” of 5 nm to 475 nm. Pet., 47; EX1003, ¶149. But Huang nowhere states that such a subtraction yields the relevant height difference, nor does Huang disclose the resulting range of 5-475 nm as a parameter of its device. This computed range is a construct of the Petition, not a teaching of the reference. Huang does not identify any relationship between these two independent parameters and does not teach a

POSITA that the height difference between the bottom surface of the epitaxial structure and the bottom surface of the isolation structure should fall within any particular range, let alone the specific 100-250 Angstrom range recited in claim 7.

The Petition does not identify any particular strip height or etch depth value that a POSITA would select from Huang's disclosed ranges that would make sense to import into the structures of Xu or Ching. Indeed, even taking the Petition's arguments at face value that Huang discloses any combination of the two independent dimensional ranges, Huang would actually disclose a range that includes ***negative values***, such that the etched recess is deeper than the bottom surface of the dielectric layer (e.g., semiconductor strip height of 5 nm and etch depth of 25 nm). This highlights the oversimplified and hand-wavy nature of the Petition's analysis.

As such, the Petition fails to identify any particular disclosure in Huang that would result in the claimed height difference range of claim 7. Nor does it provide any rationale that a POSITA would select any particular combination of Huang's strip height and etch depth ranges that would: (1) be functionally beneficial, (2) make sense for the structures of Xu or Ching, and (3) result in a height difference within the range recited in challenged claim 7. Accordingly, Grounds 1B and 2C fail and claim 7 should be upheld.

b. Even If Huang Discloses The Entire Range Alleged In the Petition, That Range Is Too Broad To Render Obvious Claim 7's Recited Range

Even if the Petition's calculation of Huang's height-difference range were accepted at face value, the resulting range of approximately 50 Angstroms to 4,750 Angstroms is so broad as to be uninformative with respect to the specific 100–250 Angstrom range recited in claim 7. The Petition's calculated range spans nearly two orders of magnitude—from dimensions characteristic of a few atomic layers to dimensions exceeding the height of an entire modern FinFET device. EX2005-McAlexander-Decl, ¶122. A range this expansive effectively encompasses any height difference that could conceivably appear in a FinFET structure, and therefore provides no meaningful guidance toward any particular sub-range within it. *Id.*

The Petition's reliance on *In re Peterson*, 315 F.3d 1325, 1329–30 (Fed. Cir. 2003), for the proposition that "even a slight overlap in range establishes a prima facie case" (Pet. at 49) is misplaced. The presumption in *Peterson* operates where the prior art directs the skilled artisan toward the claimed range or where the range is narrow enough that selecting the claimed value would be predictable. Here, the prior art "range" is not a range that Huang itself discloses as a design parameter—rather, it is a computed envelope derived from two unrelated dimensional disclosures. Huang provides no teaching whatsoever that any particular value within this enormous computed span is preferable, functionally significant, or even relevant

to the height difference between the bottom of an epitaxial structure and the bottom of an isolation structure. See *In re Jones*, 958 F.2d 347, 350 (Fed.Cir.1992) (rejecting argument that “regardless [] how broad, a disclosure of a chemical genus renders obvious any species that happens to fall within it”). Indeed, Petitioner’s own cited case, *In re Peterson*, recognizes that “a disclosed range of such breadth might present a situation analogous to our cases involving the failure of a very broad disclosed genus of substances to render prima facie obvious specific substance within its scope.” *In re Peterson*, 315 F.3d at 1330, n.1 (citing *In re Baird*, 16 F.3d 380, 382 (Fed. Cir. 1994); *In re Jones*). Here, the claimed 100–250 Angstrom range occupies barely 4% of the Petition’s calculated range; without any teaching directing a POSITA to that narrow window, the overlap is meaningless. EX2005-McAlexander-Decl, ¶123.

Critically, the Petition identifies no teaching in Huang—or anywhere else in the prior art—associating the 100–250 Angstrom height-difference range with any functional advantage. The Petition argues that “general scaling demands” would motivate a POSITA toward the lower end of Huang’s enormous range (50 Å to 4,750 Å), because “smaller vertical dimensions accompany lateral scaling.” Pet., 48-49. But if generic scaling demands were sufficient motivation to select any small dimension from any FinFET reference, then every dimensional claim in every

FinFET patent would be obvious over any other FinFET reference that discloses any dimensional range. The law does not permit such a generic, all-encompassing motivation. *ActiveVideo Networks, Inc. v. Verizon Commc'ns, Inc.*, 694 F.3d 1312, 1328 (Fed. Cir. 2012) (rejecting motivation-to-combine testimony that is “generic” and “fails to explain why a person of ordinary skill in the art would have combined elements from specific references *in the way the claimed invention does.*”) (emphasis in original). The Petition’s scaling argument provides no reason to arrive at the specific 100-250 Å range, does not account for the functional significance of that range in the context of the '609 patent's Fin-First architecture (namely, void-free epitaxial growth), and does not address why Huang's Fin-Last dimensions—derived from an entirely different structural context—would produce predictable and beneficial results when applied to Xu's or Ching's devices.

Moreover, the '609 patent does not claim its specific range because of scaling; rather, it claims this range because it solves a specific technical problem. The specification teaches that by controlling the height of the isolation structure at two sides of the gate structure, “the epitaxial layer may be filled into the corresponding recess easily during the epitaxial growth process” and “the void defects may be also avoided as a result.” EX1001 at 2:6–15; EX2005-McAlexander-Decl, ¶125. The specification further discloses a preferred height difference H2 of 150 Angstroms—

squarely within the claimed range—and ties this value to enabling void-free epitaxial growth without sealing the growth cavity. EX1001 at 5:33–39. Neither Huang nor the Petition identifies void-defect avoidance as a reason to select any particular recess depth or height difference. The disconnect between the Petition's stated motivation (generic scaling) and the patent's actual technical contribution (void-free epitaxial filling within a specific dimensional window) confirms that the selection of the claimed range was not obvious from Huang's teachings but rather reflects the '609 Patent's recognition of a specific structure-function relationship that the prior art did not appreciate.

Accordingly, Grounds 1B and 2C fail and claim 7 should be upheld.

V. CONCLUSION

For at least the reasons discussed above, the challenged claims of the '609 patent should be found patentable.

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Respectfully submitted,

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The undersigned certifies that the portions of the above-captioned PATENT OWNER'S RESPONSE specified in 37 C.F.R. § 42.24 have 9,983 words, in compliance with the 14,000 word limit set forth in 37 C.F.R. § 42.24(b)(1). This word count was prepared by the word-processing program used to prepare this paper (Microsoft Word).

Dated: July 15, 2026

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CERTIFICATE OF SERVICE

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