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THIN FILM TRANSISTOR TECHNOLOGIES (TFTT VII)



Edited by
Y. Kuo

PV 2004-15

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THIN FILM TRANSISTOR TECHNOLOGIES (TFTT VII)

Proceedings of the International Symposium

Editor

Y. Kuo
Texas A&M University
College Station, Texas, USA



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Proceedings Volume 2004-15



THE ELECTROCHEMICAL SOCIETY, INC.
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PREFACE

This proceedings volume contains papers presented at the Seventh Symposium on Thin Film Transistor Technologies (TFTT VII), held in Honolulu, Hawaii, USA, October 4-6, 2004. This symposium was sponsored by the Electronics and Dielectric Science and Technologies Divisions of The Electrochemical Society.

This symposium was organized into 9 sections: Poly-Si TFTs from Laser Crystallization, Poly-Si TFTs from Metal-and Non-Metal-Induced Crystallization, TFT Gate Dielectrics, Doping, Structures, etc., Devices and Modeling, Circuits and Systems, Materials and Substrates, Organic TFTs, New and Novel Applications, and Posters. Totally, 39 papers contributed from 13 countries or regions, i.e., Brazil, Canada, China, France, Germany, Greece, Hong Kong, Japan, Korea, Netherlands, Spain, Taiwan, UK and USA, are included in this proceedings volume. Authors are from industry/institutes (Advanced LCD Technologies Development Center Co., Corning, DuPont, FlexICs, Fujitsu, Hitachi, IBM, Japan Science & Technology Agency, NEC, Optoelectronic Industry and Technology Development Assoc., Philips, Samsung, Seiko Epson, and Sharp) and universities (Aristotle University of Thessaloniki, Cambridge University, Delft University of Technology, Hanyang University, Hong Kong University of Science and Technology, Kyung Hee University, Lehigh University, Nankai University, National and Kapodistrian University of Athens, National Chiao-Tung University, Norwegian University of Science and Technology, Pennsylvania State University, Rennes I University, Rensselaer Polytechnic Institute, Sejong University, Shimane University, Seoul National University, Simon Fraser University, Sungkyunkwan University, Surrey University, Technische Universitat Dresden, Texas A&M University, Tokyo University, Tokyo Institute of Technology, Tokyo Polytechnic University, and Universitat Rovira i Virgili).

In order to present all papers in a coherent manner, this proceedings volume is edited into 8 sections. All papers are published as their original forms without alteration of their technical contents except for the format.

The editor wishes to express his sincere appreciation to the following people for their involvement in organizing and conducting the symposium:

- co-organizers for their contributions in planning and coordinating the program.
- authors and presenters of papers for their participation.
- section chairs and co-chairs for their conducting the meeting.
- B. Bachetti for his assistance in preparing and editing the volume.
- staffs of The Electrochemical Society for their administrative assistance in organizing the symposium and in publishing this volume.

Yue Kuo
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Facts about ECS

The Electrochemical Society (ECS) is an international, nonprofit, scientific, educational organization founded for the advancement of the theory and practice of electrochemistry, electrothermics, electronics, and allied subjects. The Society was founded in Philadelphia in 1902 and incorporated in 1930. There are currently over 7,000 scientists and engineers from more than 70 countries who hold individual membership; the Society is also supported by more than 100 corporations through Contributing Memberships.

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CW LASER LATERAL CRYSTALLIZATION (CLC)

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ABSTRACT

The low-temperature poly-Si TFT performances have become comparable to those of the single-crystalline Si MOSFET's by using CLC. The quality of CLC film and the electrical characteristics of CLC-TFTs have been investigated. High performance of the CLC circuits have been confirmed by the fabrication of test circuits: a 100 ps propagation delay ring oscillator at 4V, a 270 MHz shift register at 5V, a 1K bit SRAM, an oscillators, and a power supply, etc. The throughput of CLC is dramatically improved by the selective and simultaneous irradiation of divided laser beams.

INTRODUCTION

The CW laser Lateral Crystallization (CLC) of amorphous Si by a 532nm diode-pumped solid-state (DPSS) laser has been developed for low temperature poly-Si TFTs on glass substrate [1]. With the CLC, both the poly-Si grain size and the field-effect-mobility of poly-Si TFTs have been remarkably enhanced even on glass substrates [1-2], compared to those of conventional TFTs by pulse laser crystallization such as excimer laser crystallization (ELC) and its modifications[3-5]

The mobilities of CLC TFTs are greater than those of the ELC by a factor of 2-3. The CLC is a technology to realize a sheet computer, where many kinds of intelligent and high performance circuits are integrated in the same glass or plastic substrate with the pixel array of LCD or EL displays, as shown in Fig.1. Although various circuits have been already fabricated as well as display drivers with LCD pixel array on a glass substrate with TFTs by pulse laser crystallization [6-8], these TFT performances must be still improved..

CLC PROCESS

In the CLC process, molten region moves laterally with the scanning CW laser spots and the crystal growth is induced laterally and continuously, resulting in extended large grains having nearly parallel grain boundaries, as shown in Fig.2. The trace of a single scanning of the amorphous Si consists of three regions: lateral grain crystal at the center, polygonal grain crystal, and micro grain crystal at the edges, as shown in Fig.3. Raman scattering data in the polygonal region are scattered and agree with that of the ELC crystals, and Raman scattering data in the lateral crystal gather round a region and these line widths resemble that of the Si single crystal, as shown in Fig4 [9,10].

The single crystalline grain size of the lateral crystal exceeds that of ELC by a factor of 10 to 100, as shown in Fig.5. The laser power is 2-10 W, the scanning speed 40-200 cm/s, the amorphous silicon film thickness 40-250 nm, the buffer SiO2 layer 400nm between the amorphous Si and glass, and the obtained width of lateral crystal region 20-

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350 um by a single scanning. Cross sectional TEM of the CLC film verifies that the surface of the CLC film is flat and no damage is induced in the underlying glass, as shown in Fig.6..

The CLC poly-Si film is qualitatively same kind of film as that was obtained by unseeded CW Ar+ laser crystallization on Si-wafer to make 3-D integrations [11-13]. Fig.7 shows the first 3-D integration. An NMOS FET is fabricated in a laser recrystallized SOI film directly above another bulk PMOS FET with insulating film in between. But the used scanning speed of the present CLC film on glass substrate is much faster, the obtained molten width wider, and the crystallized film thickness thinner than those on Si-wafer. Main problems of 3-D integrations were process reproducibility and throughput. They are now conquered by the stable DPSS laser instead of the Ar+ laser and the existence of the non-scalable display area in the sheet computers.

CLC-TFT CHARACTERISTICS

The obtained mobilities of CLC poly-Si TFTs are 570 and 200 cm2/Vs for n- and p-channel TFTs, respectively, as shown in Figs 8 and 9. These values of the CLC poly-Si TFTs are comparable to those of the CLC single-Si TFTs [2] and the bulk single-Si MOSFETs. In the CLC crystal, grain boundaries, if they are present, are almost parallel to the scanning direction, and this grain boundary slightly affect the carrier flow if the source-to-drain is formed parallel to the scanning direction.

The large value and small deviation in mobility of CLC-TFTs are both realized, as shown in Fig.10. The small threshold voltage variation is also fulfilled, as shown in Fig.11. If the laser scanning is carried out perpendicular to the source-to-drain direction, the mobility becomes lower than that of parallel scanning, as shown in Fig.12. The smaller effect of grain boundary in the parallel scanning is also revealed in the variation of the activation energy of the temperature dependence of mobility, as shown in Fig.13.

The hot-carrier reliability of CLC-TFTs is superior to that of pulse ELC-TFTs, as shown in Fig.14 [14,15]. The drain current degradation coefficient ΔId / Id(initial) after hot-carrier stress is normalized by the total charge flowed from source to drain during the stress.

LATERAL CRYSTAL GROWTH CONDITION

There is an irradiation condition to obtain a lateral grain crystal film in CLC process, as shown in Fig.15. Higher power or lower scanning speed condition results in agglomeration of Si film. Lower power or higher scanning speed condition results in the polygonal crystals. Further lowered power or increased speed surely results in non melted surface. The change from lateral to polygonal with decreasing power or increasing speed is explained by the change of gradient of the liquid-solid interface. When the laser power becomes low or the scanning speed becomes large, the liquid-solid interface declines, as shown in Fig.16. Then the lateral crystal growth changes to the vertical crystal growth to the underlying substrate, resulting in the change from the lateral grain crystal to polygonal grain crystal because the crystal growth occurs perpendicular to the liquid-solid interface.

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EFFECT OF Si FILM THICKNESS

The obtained mobility of TFTs increases with the Si film thickness, as shown in Fig.17. This is explained by that the distance of single-crystal region between parallel grain boundaries becomes large and the (100) texture also becomes dominant with Si film thickness.

Fig.18 shows effect of optical illumination on the drain current v.s. gate voltage characteristics. The leakage current is induced during OFF state. But no effect is observed during ON state. This is also revealed by the no change in mobility between illuminated and non-illuminated devices, as shown in Fig.19. The photo-induced leakage current in the OFF state does not increase abruptly, but increases proportionally with Si film thickness, as shown in Fig.20.

OVERLAPPED SCANNING

In the peripheral region, many kinds of TFTs are densely packed, and it is difficult to crystallize each TFT region selectively. All the peripheral regions including TFT active regions and field regions are crystallized by the same overlapped scanning. The overlapped crystallization does not affect the mobility or S-values, but it induces a slight decrease in threshold voltage about 0.1V, as shown in Fig.21 [16]. This slight decrease is due to the Si film thickness decrease by the overlapped scanning; 50nm decrease in Si film is observed. The threshold voltage variation will be prevented by the partially-depleted structure of TFTs even if the Si film thickness changes .

SCALED TFTs

Scaled TFTs is necessary to decrease the area of peripheral region into acceptable level as well as to improve the circuit performance. A laser direct writing technology has been developed for fine lithography on a large glass substrate to make scaled devices in the peripheral[17]. Fig. 22 shows the resist pattern for gate electrodes just after development; 0.4 um width line is formed on aluminum film. Fig.23 shows a cross sectional TEM image of the 0.5 um CLC-TFTs. The direct writing fine-patterning is useful for the narrow and small area of peripheral; the major area of pixel array with a large design-rule is patterned by the conventional steppers.

CLC-TFT CIRCUITS

The high performance of CLC-TFT circuits on glass have been confirmed by fabricating LCD panels and various TFT circuits such as 100 ps propagation-delay ring oscillators at 1 um design rule and 4V, as shown in Fig.24, 270 MHz clock shift registers at 1.5um design rule and 5V, as shown in Fig.25, and 1 k bit SRAMs at 3.0um design rule, as shown in Fig.26, level-shifters, oscillators[18], power supply circuits, etc.

THROUGHPUT OF CLC

Fig.27 shows image of a sheet computer. Major part is formed by pixel array. Integrated circuits are formed in the narrow region about 2 mm wide in the peripheral of the pixel array. It is important to improve the throughput of the crystallization in the pixel

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area to improve the overall throughput. High throughput of the CLC is obtained by the simultaneous and selective irradiation of the divided and multiplexed laser beams to each TFT active area in pixel, as shown in Fig.28. The selective crystallization can be done at higher speed up to 2m/s, because newly designed focusing optics reveals a high quality lateral crystal even at high scanning speed of 2m/s, as shown in Fig.29. At the scanning speed decreases, irradiation power is limited by the agglomeration and the width of lateral crystal becomes small.

The net crystallization throughput becomes larger than that of ELC, as shown in Fig.30. The peripheral region is crystallized by 8-beam simultaneous irradiation at 300um lateral crystal width and 50um overlapping for each beam at 50cm/s scanning speed. The pixel area is simultaneously crystallized by 32 divided sub-beams at a 30 um lateral crystal width and a 2m/s scanning speed.

CLC is also suitable to a large size TV as well as a mobile sheet computer because the throughput increases with the pixel pitch due to the selective crystallization. The CLC scanning system is scalable and the substrate can be easily extended to the 7th generation size.

CONCLUSION

The CW laser Lateral Crystallization (CLC) of amorphous Si by a 532nm diode-pumped solid-state (DPSS) laser has been developed for low temperature poly-Si TFTs on glass substrate The low-temperature poly-Si TFT performances have become comparable to those of the single-crystalline Si MOSFET's. The quality of CLC film and the electrical characteristics of CLC-TFTs have been investigated. The effect of parallel and vertical scanning is discussed. The hot carrier reliability is superior to that of ELC devices. The condition to obtain the lateral grain crystal is also discussed. High performance of the CLC circuits have been confirmed by the fabrication of test circuits: a 100 ps propagation delay ring oscillator at 4V, a 270 MHz shift register at 5V, a 1K bit SRAM, a oscillators, and a power supply, etc. The throughput of CLC is dramatically improved by the selective and simultaneous irradiation of divided laser beams.

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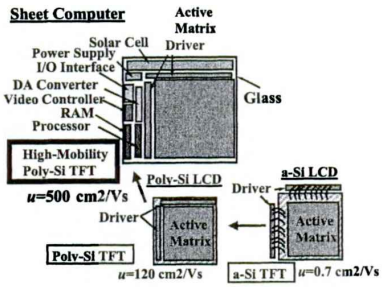


Fig.1. Evolution from LCD panels to Sheet Computers.

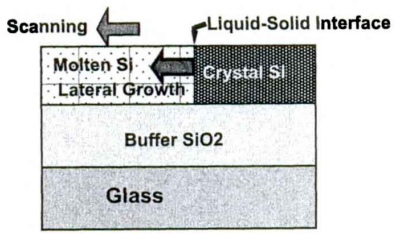


Fig.2. Principle of CLC. Beam spot from a 532nm DPSS laser is scanned laterally.

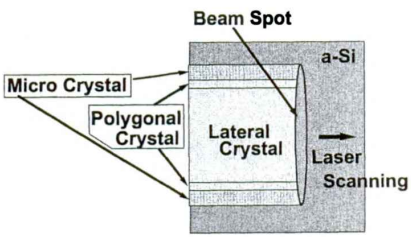


Fig.3. Trace of a single scanning. Lateral crystal is formed at the central region of the scanning trace. Polygonal crystal like a ELC poly-Si and miro crystal are formed at the edges of the scanning.

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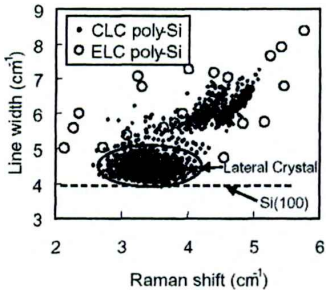


Fig. 4. Raman scattering of the single beam trace of CLC in comparison with ELC.

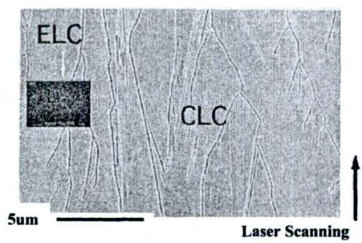


Fig.5. SEM grain boundary patterns of CLC and ELC after delineation etching.

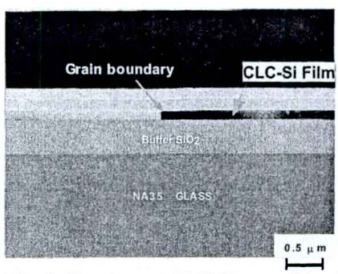


Fig. 6. Cross sectonal TEM image of the CLC region.

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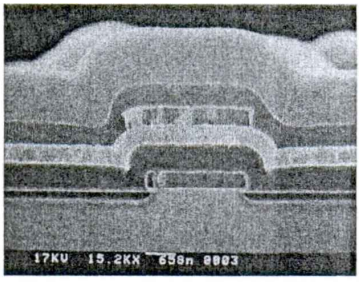


Fig.7. Cross sectional SEM image of the first 3-D integration device. An NMOS SOI MOSFET is stacked over a PMOS bulk Si MOSFET, forming an inverter of a ring oscillator.

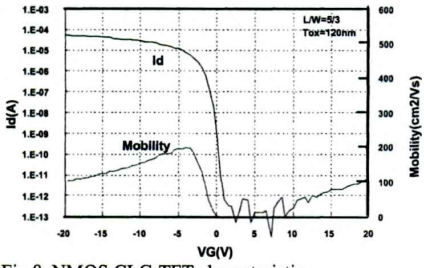
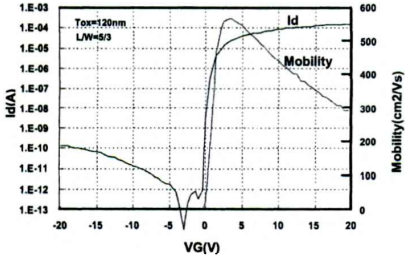


Fig.8. NMOS CLC-TFT characteristic.



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Fig.9. PMOS CLC-TFT characteristic.

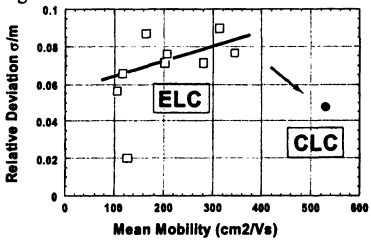


Fig.10. Relative deviation of CLC mobility distribution as a function of mean value.

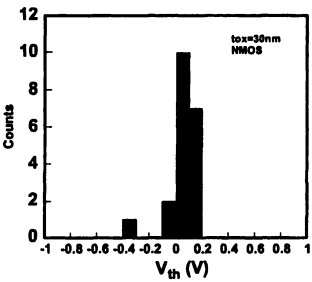


Fig.11. Threshold voltage distribution of NMOS CLC-TFTs. Gate oxide thickness *tox* is 30nm

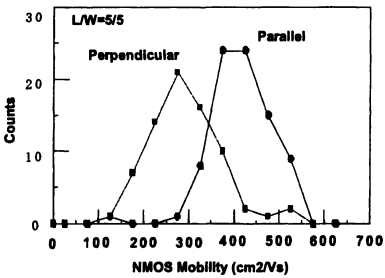


Fig.12. Comparison of NMOS CLC-TFT mobility distribution between parallel and perpendicular scanning.

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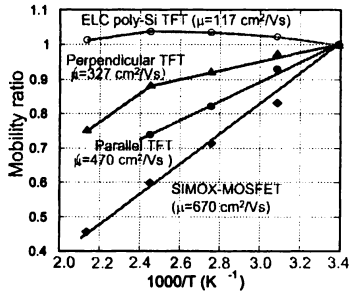


Fig.13. Temperature dependence of mobility between various NMOS devices: ELC-TFTs, perpendicular scanned CLC-TFTs, parallel scanned CLC-TFTs, and SIMOX-MOSFETs.

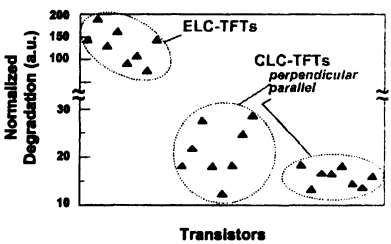


Fig. 14. Hot carrier induced reliability.

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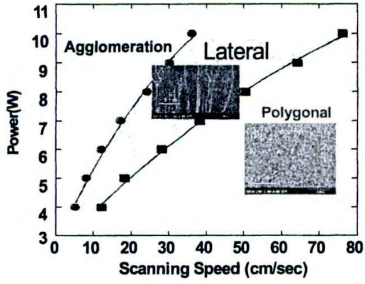


Fig.15. The lateral gowth condition area is shown as a function of iraddiated power and the scanning speed at a beam spot.

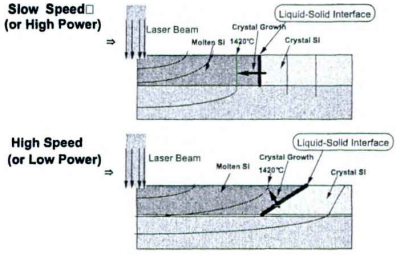


Fig.16. Temperature distribution in the Si film during CLC process.

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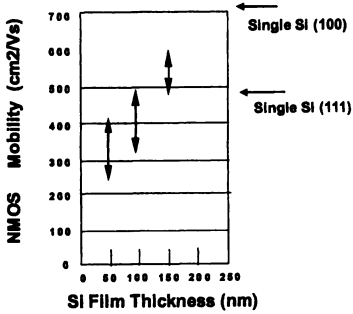


Fig. 17. CLC TFT mobility as a function of Si film thickness.

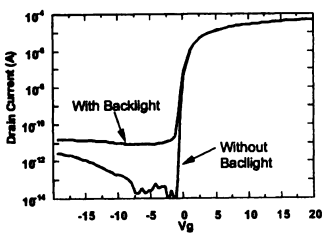


Fig.18. Effect of optical illumination on the Id-Vg characteristics of CLC-TFTs.

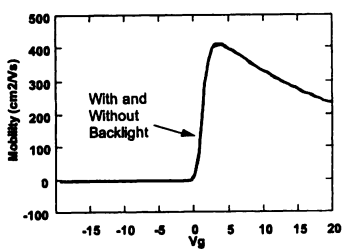


Fig. 19. Effect of optical illumination on the mobility of CLC-TFTs.

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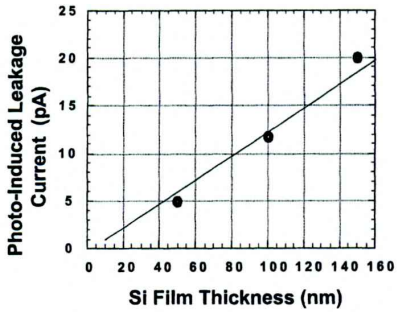


Fig.20. Photo-induced leakage current of CLC-TFTs as a function of Si film thickness.

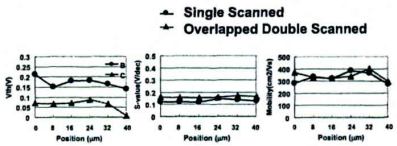


Fig.21. Effect of overlapped scanning on Vth, S value, and mobility. Cirlce: single scanning. Triangle : overlapped sanning.

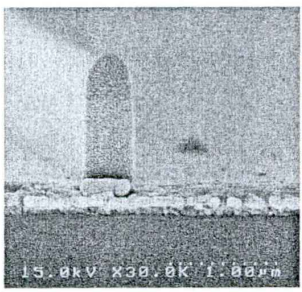


Fig. 22. SEM picture of a resit pattern for the gate electrode formed by the laser direct writing.

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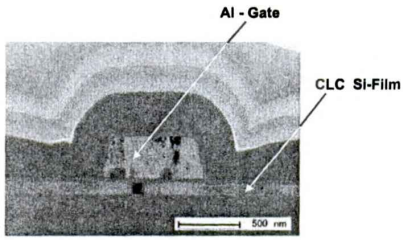


Fig.23. Cross sectional TEM image of the 0.5um CLC-TFT.

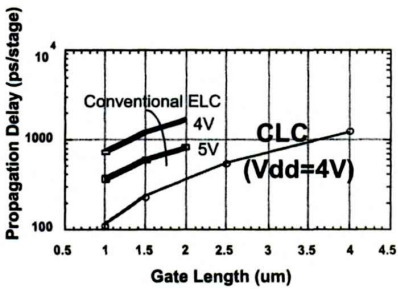


Fig. 24. Propagation delay of ring oscillators as a function of gate length. In the CLC devices, 100ps delay time is achieved at 1um gate length and 4V power supply.

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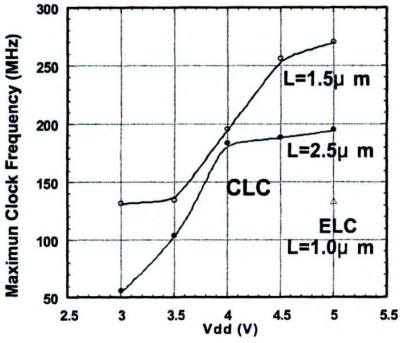


Fig. 25. Maximum clock frequency of shift registes as a function of power supply voltage Vdd.

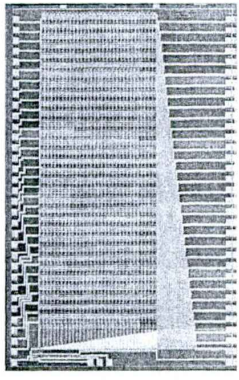


Fig.26. Fabricated 1 kbit CLC CMOS-SRAM.
Chip size is 7 x 9.8mm2. Design rule is 3 um.

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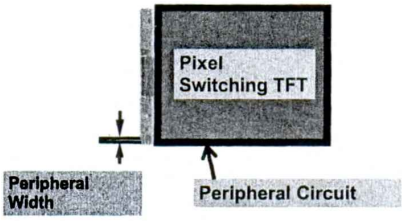


Fig. 27. Image of a sheet computer. Major part is formed by pixel array. Integrated circuits are formed in the narrow region in the peripheral of the pixel array.

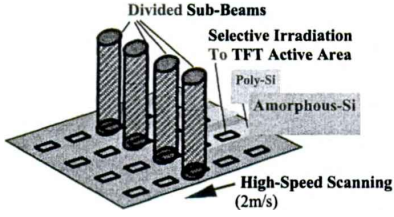


Fig. 28. CLC selective irradiation by the divided laser beams in the pixel area.

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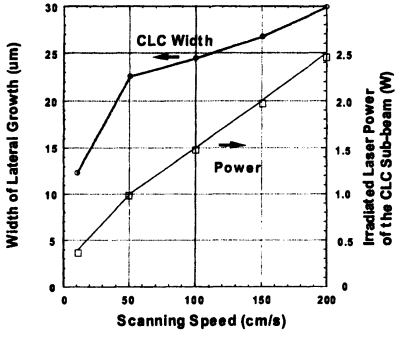


Fig. 29. Width of the lateral crystal growth in CLC as a function of the scanning speed for the selective crystallization of the switching TFTs in the pixel array.. Newly designed focusing optics reveals a high quality lateral crystal even at a high scanning speed of 2m/s. The irradiation power is limited by the agglomeration.

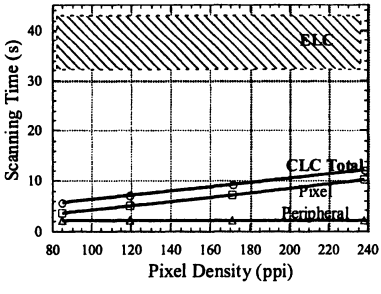


Fig. 30. Comparison of the calculated net scanning time between CLC and ELC for each 15 inch panel. The width of peripheral region is 2 mm. The peripheral region is crystallized by 8-beam simultaneous irradiation at a 50cm/s scanning speed. The pixel area is by 32 divided sub-beams at a 200cm/s scanning speed.

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NOVEL PHASE-MODULATOR FOR ELA-BASED LATERAL GROWTH OF SI

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Phase-modulated excimer laser annealing (PMELA) is an advanced excimer-laser crystallization (ELC) method characterized by the intensity modulation of irradiated light by a phase modulator. In this method, a temperature gradient is formed in melted Si and large crystal grains are laterally grown at predetermined positions. In order to form grains with a high packing efficiency, a periodic "V-shaped" form of the light intensity distribution is desired. In the present study, a novel "duty phase modulator" is developed for projection-type PMELA. The light intensity distribution on the sample surface can be freely controlled and its design method is simple. We confirmed that a V-shaped light intensity distribution could be achieved by preparing a prototype duty phase modulator. In addition, crystallization was carried out with this duty phase modulator and 5-μm long crystal grains with a high packing efficiency were successfully grown.

INTRODUCTION

ELC is a key technology for polycrystalline Si thin-film transistors (poly-Si TFTs) designed for "system-on-glass" devices and has been the subject of numerous studies. PMELA, which we have been investigating, is an advanced ELC method featuring the intensity modulation of irradiated light on a-Si using a phase modulator (Figure 1). In this method, a temperature gradient is formed in melted Si and large crystal grains grow laterally at predetermined positions. In this way, a TFT channel section can be prepared from a single crystal grain. TFTs of higher performance can be prepared from these large crystal grains than from conventional poly-Si.

In order to form a whole circuit, it is necessary to grow large crystal grains with a high packing efficiency. For this purpose, the distribution of the light intensity is determined based on the following characteristics of the lateral growth.

1) Lateral growth starts at a certain "lateral growth starting intensity". At a lower light intensity, Si does not melt or it remains in the form of fine grains.

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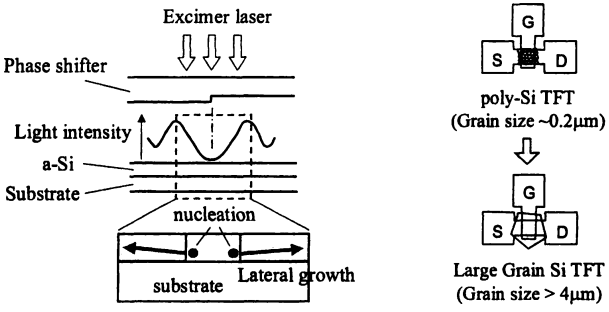


Fig.1 Schematic of phase modulated eximer laser crystallization.

2) Lateral growth takes place along the direction of the temperature gradient, namely, the direction of the light intensity gradient. If this gradient is small, the lateral growth will stop halfway.

Based on these characteristics, we have identified the optimum distribution to have a periodic "V-shaped" form to grow crystal grains with a high packing efficiency. As shown in Figure 2, crystal nuclei are born at the bottom of the V-shaped irradiating light intensity distribution. Subsequently, lateral growth can take place along the gradient of the V-shape to peak intensity points. In this way, it is possible to grow large crystal grains with a high packing efficiency. It is important that the light intensity at the bottom of the V-shape is just the lateral growth starting intensity. If the intensity at the bottom of the V-shape is too low, large grains cannot be formed in those regions. If the intensity at the bottom of the V-shape is too high, random nucleation, resulting in small grains, takes place in the bottom.

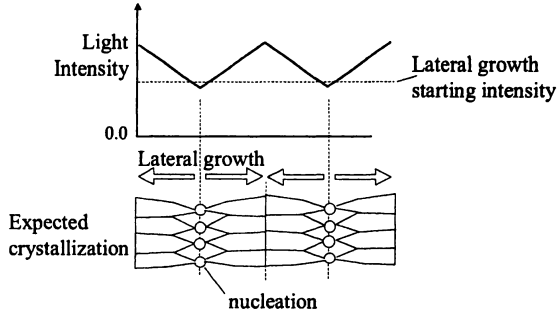


Fig.2 Target of light intensity distribution.

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In a previous report, 3-μm long crystal grains were formed using a line-and-space (L&S) type phase modulator (1). By this method, however, the desired V-shaped light intensity distribution could not be achieved even when the optical system was carefully adjusted. A concave distribution was obtained, but it was localized and control of the light intensity at the bottom of the distribution was difficult. Therefore, crystallization with a high packing efficiency could not be achieved.

In order to improve on this method, a new duty phase modulator has been developed (2). In this report, the principle, design method, and advantages of this duty phase modulator are explained and the results of a crystallization experiment using the duty phase modulator are reported.

ADVANCED OPTICAL SYSTEM FOR PMELA

Optical systems for PMELA

With reference to Figure 3, in this section we explain the newly developed method (advanced projection PMELA system) in comparison with the conventional method (basic PMELA system).

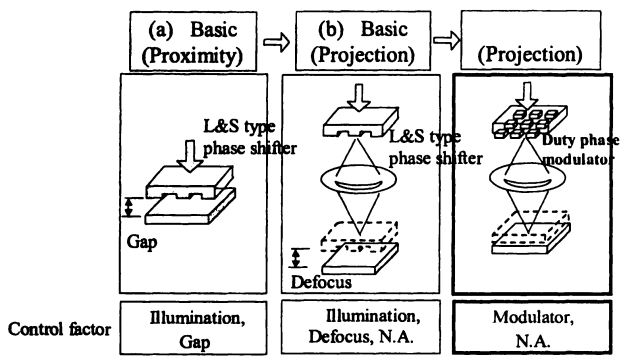


Fig.3 Optical systems for PMELA.

The proximity exposure method and the projection exposure method are used in basic optical systems. An L&S type phase shifter is used in both methods. In the proximity exposure method (a), irradiation is performed keeping a fixed gap between the phase shifter and the substrate. The light intensity distribution is controlled by a Fresnel

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diffraction pattern generated by the gap. In the projection exposure method (b), an image of the phase shifter is formed by the optical imaging system and the substrate is placed away from the image at a defocused position. Thus, the light intensity distribution is controlled by a Fresnel diffraction pattern generated by the defocusing. The control factors of the light intensity distribution in the proximity exposure method are the illumination conditions of the phase shifter and the width of the gap. In the projection exposure method, the control factors are the illumination conditions of the phase shifter, the defocus value, which corresponds to the gap width, and the numerical aperture (N.A.) of the optical imaging system. The last factor concerns the amplitude point spread function (ASF) of the optical imaging system. It is worthy to notice that light intensity distribution on this sample surface is more deformed in (b) than (a), since N.A. filters highly diffracted light.

In the advanced PMELA system, the abovementioned effect of N.A. is applied in a positive manner. The phase shifter is imaged on the sample surface deformed by ASF. In other words, an optical imaging system is used, but defocus is not used. The light intensity distribution is controlled with a fine concavo-convex plane pattern prepared on the shifter surface. The concavo-convex plane pattern can be freely created and thus controllability of the light intensity distribution can be drastically improved. As a result, it is possible to create an ideal V-shaped distribution.

Principle of advanced optical system

In this section we explain the principle of light intensity control in the advanced PMELA system by looking at the function of the pupil of the imaging system (Figure 4).

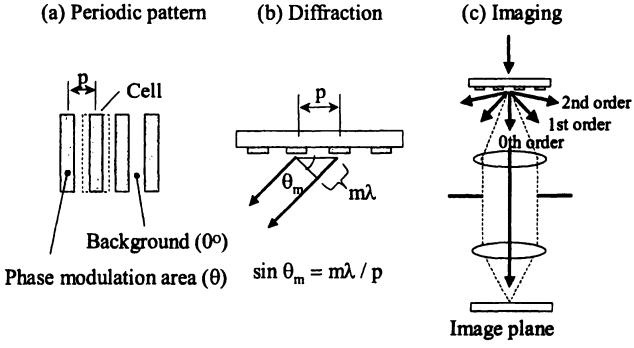


Fig.4 Control of light intensity.

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A duty phase modulator is a set of fine phase modulation units called "cell". The phase of the background is set at 0° and the phase of a phase modulation area with respect to the phase of the background is designated by θ. The percentage of the phase modulation area on a cell is called the "duty".

For the time being, we assume that the duty is constant, that is, the pattern is perfectly periodic. In addition, the cells are considered to have a one-dimensional arrangement as shown in Figure 4(a). Then, since the duty phase modulator can be considered a kind of diffraction grating, the transmitted light is discretely diffracted and the diffraction angle θ can be expressed by the following equation, based on Figure 4(b).

$$\sin \theta_m = m\lambda / p$$

where p is the cell pitch, m is the diffraction order, and λ is the wavelength of laser light.

As shown in Figure 4(c), if p is set to be less than a certain critical value, diffracted light other than 0th order escapes outside the pupil of the optical imaging system. As a result, only the 0th order light reaches the image plane. An image is formed only by the interference on the image plane of higher order light diffracted from the object. Accordingly, fine patterns do not appear under these conditions and the image takes a uniform intensity distribution. In this case, the normalized light intensity, I, is equal to the light intensity of the 0th order diffraction and can be expressed by the following equation.

$$I = | U |^2 = | 1/p \int_0^p e^{i\varphi(x)} dx |^2 \qquad [1]$$

where U is the complex amplitude of light and φ(x) is the phase distribution of the duty phase modulator. Thus, the light intensity can be adjusted by changing φ(x), namely, the geometry of the phase modulation area in the cell.

The above concept is true for the case in which cells take a two-dimensional arrangement as shown in Figure 5. Although the diffraction is two-directional, an equation similar to equation [1] can be devised by using two-dimensional integration.

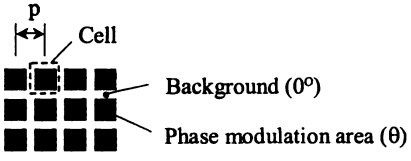


Fig.5 Two-dimensional cells.

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Formulation of light intensity by amplitude point spread function

In this section, we formulate an expression for the light intensity function on the image plane using the concept of the amplitude point spread function. Image formation with optical imaging systems is classified into coherent imaging, in which the image is formed by illumination from a point light source, incoherent imaging, in which the image is formed by illumination from a sufficiently large and perfectly incoherent light source, and partial coherent imaging, which is intermediate between the two. For a partial coherent imaging, which a real optical system is applied to, the light intensity distribution can be obtained from the equation derived by H. H. Hopkins (3). However, it seems difficult to derive a simple expression from this equation for this case. Therefore, we consider here the case of an approximation to coherent imaging.

The amplitude distribution U(x, y) on the image plane by coherent imaging can be obtained from Fourier imaging theory by the convolution shown in equation [2] (4).

$$U(x, y) = \iint T(\xi, \eta)\, ASF(x - \xi, y - \eta)\, d\xi d\eta \qquad [2]$$

where T(x, y) is the complex amplitude transmittance of the object (duty phase modulator) and ASF(ξ, η) is the amplitude point spread function (complex amplitude distribution formed by a point object) of an optical imaging system.

The amplitude point spread function can be obtained by the Fourier transformation of the pupil function of the optical imaging system. The amplitude point spread function ASF(ξ, η) can be expressed by the following equation.

$$ASF(\xi, \eta) = \frac{2 J_1(2\pi NA\, r / \lambda)}{2\pi NA\, r / \lambda} \qquad [3]$$

$$r = \sqrt{\xi^2 + \eta^2}$$

where λ is the wavelength of the light, NA is the numerical aperture of the optical imaging system, and J_1 is the 1st order Bessel function.

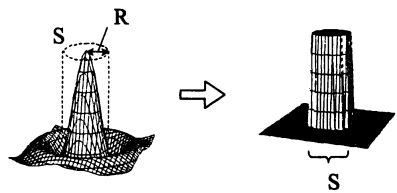


Fig.6 Approximation of amplitude point spread function.

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Since it is difficult to evaluate equation [2] using equation [3] in this form, equation [3] is approximated by a cylindrical function of radius R as shown in Figure 6. That is,

$$ASF(\xi, \eta) = \begin{cases} 1 & r < R \\ 0 & r > R \end{cases}$$

$$R = 0.61\lambda / NA, \qquad [4]$$

where R is the minimum value of r that makes the right side of equation [3] zero. The circular area with radius R is called the "point spread area" and it is represented by the symbol S. Equation [2] can then be simplified to an integral of the complex amplitude transmittance $T(\xi, \eta)$ in S, which has a center at (x, y). Since phase modulator changes phase of light but no its amplitude, the complex amplitude transmittance $T(\xi, \eta)$ can also be expressed as a function of the phase distribution $\varphi(\xi, \eta)$ in the same way as equation [1]. Thus, a general equation that gives the amplitude due to a duty phase modulator is obtained.

$$U(x, y) = \int_S e^{i\varphi(\xi - x, \eta - y)} d\xi d\eta \qquad [5]$$

This equation is similar to equation [1] described above. Equation [1] has the condition that the phase distribution pattern $\varphi(x)$ must be periodic. However, equation [5] has no restriction and $\varphi(\xi, \eta)$ may take a non-periodic pattern.

As described later, when p is smaller than R, U(x, y) does not locally depend on the position coordinates.

NOVEL DUTY-PHASE MODULATOR

Binary phase modulation

A more specific equation can be devised under the condition that the phase modulation is binary, that is, the phase values in the phase modulation area are of one kind. Here, we denote the phase value of the phase modulation area by θ and the duty by D and we set the phase value of the background to be 0° and its duty to be 1 – D. In addition, we assume that there are enough cells within S. The percentage of the phase modulation area in the point spread area is approximately the same as D and it is not expected to depend upon the location of the center of the point spread area. As a result, equation [5] can be simplified. Hereinafter, the functions containing position coordinates will be abbreviated.

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$$U = D\,e^{i\theta} + (1-D)\,e^{i0} \qquad [6]$$

Since the light intensity, I, is the square of the absolute value of the amplitude, U, the following equation is obtained.

$$I = |U|^2 = (2-2\cos\theta)\,D^2 - (2-2\cos\theta)\,D + 1 \qquad [7]$$

Equation [7] gives the light intensity on the image plane when the phase modulation is binary. Figure 7 shows Equation [7] graphically. The light intensity, I, becomes a minimum at a duty of 50%. This minimum can be arbitrarily set in the range [0–1] by changing θ, as

$$I_{min} = (1 + \cos\theta\,) / 2 \qquad [8]$$

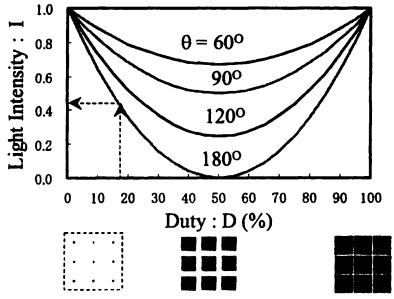


Fig.7 D-I Relation.

Desirable cell pitch

p was assumed to be sufficiently small compared with R of the point spread area. When p is large, this approximation does not hold and the light intensity distribution is not uniform. Thus, an irregularity in the light intensity is expected to appear.

An optical simulation based on scalar diffraction theory was conducted to determine the necessary cell pitch that does not cause light intensity irregularity. The light intensity irregularity on the image plane was examined by changing the value of p with respect to R. A square-shaped phase modulation area with a phase value of 180° and duty 14.6% was used as a duty phase modulator. In this case, the light intensity is expected to be 0.5 from equation [7]. In addition, an optical imaging system with

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wavelength 248 nm and numerical aperture 0.13 was assumed. In this case, R of the point spread area is 1.16 μm from equation [4]. For the optical simulation, the lithography simulation software SOLID-C™ was used.

The distribution of the light intensity with respect to p/R is shown in Figure 8(a). When p/R is less than 1.2, the distribution is uniform. When p/R is more than 1.4, an irregularity in the light intensity appears. The distribution of the light intensity at p/R=1.6 is shown in Figure 8(b). It was found that irregularity disappears completely when p/R<1 for any case.

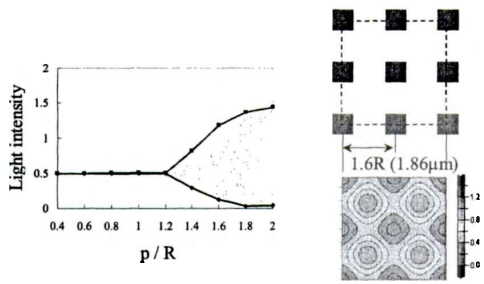


Fig.8 Influence of cell pitch.

Light intensity distribution

We want to form a light intensity distribution that changes within a plane using the duty phase modulator. It can be seen from equation [5] that the intensity is determined only by the pattern in the point spread area. Therefore, even when the duty changes within a plane, it is expected that equation [7] holds as long as the change is mild compared with the size of the point spread area.

In order to confirm this prediction, an accurate distribution of light intensity was determined by an optical simulation. We designed a duty phase modulator based on equation [7] with the objective of obtaining a V-shaped distribution with a bottom intensity of zero. The cell pitch was set at 1.0 μm and the phase was set at 180°. The results of the optical simulation are shown in Figure 9. An optical system with wavelength 248 nm, coherence factor 0.5, and numerical aperture 0.13 was assumed. The value of p/R was 0.86 in this case and this value is in the range where intensity irregularity does not occur, as shown in Figure 8.

As shown in Figure 9(c), the required distribution could be achieved. Thus, it is

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confirmed that equation [7] is a good design guideline even for the intensity distribution, which changes within a plane. This can also confirm the validity of the three approximations used: the approximation of a coherent imaging system, the approximation of the point spread function shown in Figure 6, and the approximation used in the derivation of equation [5].

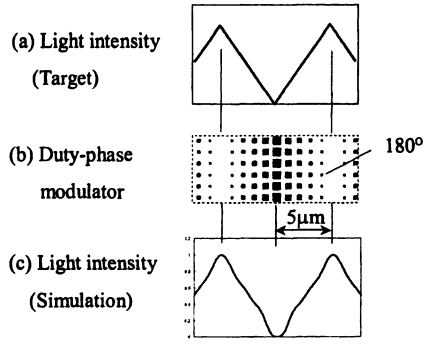


Fig.9 Light intensity by simulation.

EXPERIMENT

A duty phase modulator was prepared and the distribution of the generated light intensity was measured.

A projection optical system with wavelength 248 nm, numerical aperture 0.13, and coherence factor 0.5 was used. Cells with a size equivalent to a 1 μm square on the image plane were adopted for the duty phase modulator. The phase modulation areas were arranged with duties of 0%, 5%, 11%, 18%, 28%, and 50% in respective cells. The phase modulation areas were prepared on a quartz substrate by forming steps 244 nm deep, which corresponds to a phase difference of 180°.

An image of the prepared duty phase modulator observed with an optical microscope, the light intensity distribution predicted by the simulation, and the measured light intensity distribution are shown in Figure 10. It was confirmed that the measurement and the simulation are in good agreement. In addition, it was confirmed that a V-shaped distribution could be achieved.

Subsequently, crystallization was experimented with the duty phase modulator. The conditions and results are shown in Figure 11. A duty phase modulator was prepared with

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a phase 60° to set the bottom of the V-shaped distribution to the lateral growth starting intensity. Crystallization of amorphous Si film was conducted with the projection optical system shown in Figure 11. As a result, 5-μm long Si crystal grains with a high packing efficiency were successfully grown.

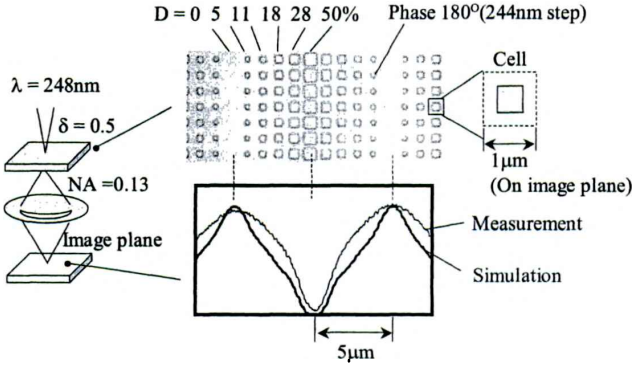


Fig.10 Measurement result of light intensity

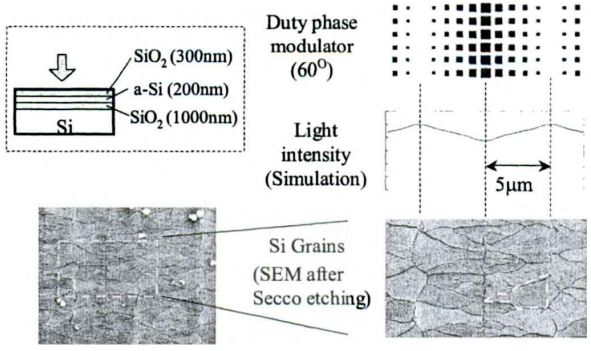


Fig.11 Crystallization

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CONCLUSION

A duty phase modulator was devised for advanced PMELA method. The principle, design method, and advantages of this duty phase modulator were described. This device can freely control the light intensity distribution and can be easily designed. A perfect V-shaped distribution was achieved and 5-μm long Si crystal grains with a high packing efficiency were successfully grown using this modulator.

ACKNOWLEDGMENTS

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AN ADVANCED SAMPLE STRUCTURE FOR LARGE GRAIN GROWTH BY EXCIMER LASER CRYSTALLIZATION

- Enlargement of the lateral growth length by using photosensitive capping layer-

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ABSTRACT

More than 10-μm-long grains were grown laterally in a 50-nm-thick Si layer by PMELA. Photosensitive SiOx capping layer enables this longer lateral growth with lower irradiated intensity of a laser light compared to those with the conventional SiO_2 capping layer.

INTRODUCTION

Low-temperature polycrystalline Si (poly-Si) films are very attractive for active-matrix liquid-crystal displays because poly-Si thin-film-transistors (TFTs) enable to form pixel arrays and peripheral circuits at a time. To add new or higher functions to these peripheral circuits monolithically toward to system-on-glass (SOG), better performance is strongly requested for TFTs. Ultra-high performance TFT, the key device for the SOG, could not be fabricated without using lateral growth methods for Si grains, and phase-modulated excimer-laser annealing (PMELA) method is the most promising method among them since only this method optimize a light intensity profile for long growth [1-5]. We have reported [6,7] that the optimum thickness of the SiO_2 capping layer is about 200 nm for a 200 nm-thick Si/SiO_2 structure under the condition of the irradiated laser intensity of 820 mJ/cm^2. The thermal diffusion effects make the whole SiO_2 capping layer to act as a heat capacitor and multi-reflection effects of the capping layer reduces the net light reflection from the sample. The growth length was about 6.6 μm, sufficiently long for 1-μm-long channel TFTs.

The requests from the mass production are to reduce the thickness of the Si for reducing the tact-time for CVD process and to decrease the laser light intensity to work out an ELA process for a high throughput. Thus, we have investigated an advanced

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structure, which can reduce the average light intensity drastically and which can enlarge the growth length of Si. In this paper, the $SiOx/SiO_2$ double layers structure is newly introduced for the capping layer for KrF and XeCl laser lights.

PROPOSED SAMPLE STRUCTURE FOR THE PMELA METOHD

Growth duration, which is closely related to the growth length, is determined mainly by the critical time for the super-cooled melt to cool down to the critical temperature for spontaneous nucleation. The sample structure plays also an important role since it determines solidification characteristics under fixed light intensity conditions. Suppose the sample is of a stacked SiO_2/a-Si/SiO_2 layer on a substrate, the factors to determine the growth duration may be heat stored near the molten Si and thermal conductance of molten Si.

Thick Si film is effective for increasing the amount of heat stored, but enhances the lateral heat loss along the highly conductive molten Si. Thus, combination of thin Si layer and thick photosensitive (and thermally low conductive) capping layer that can compensate the decrease of heat stored in Si is one of the solutions for longer grain growth [8]. There is another feature for the photosensitive capping layer, that it decreases the reflection of the incident laser light. This is because a large amount of light reflected at the capping layer/molten Si interfaces is absorbed in this capping layer during its return and cannot reach at the sample surface.

Reduction of the incident light intensity

The sample structure for numerical simulation of transient temperature is explained with an example shown in Fig.1. It is a stacked structure, with a 200-nm-thick SiO_2 capping layer, a 200-nm-thick Si layer and a thermal SiO_2 layer on a Si substrate. The method of this calculation was referred to the prior report [6] and was found to be useful for determine the layer structure. Flattop intensity was assumed for the incident light pulse (at the time t=20 nsec on the assumption of using a KrF laser). Initial and ambient temperatures were assumed to be 0°C. The solidification duration was defined as a difference between the time at which the temperature of the Si layer reduced to 1000°C and the time that the irradiation ended i.e. 20 nsec for KrF case.

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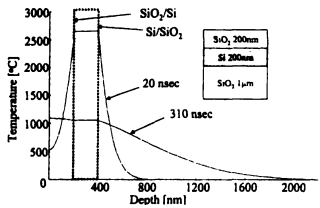


Fig.1. One-dimensional time-dependent temperature distribution normal to the sample surface.

Figure 2 shows the result of the time-dependent temperature distributions for the two samples. The samples had the same 200-nm-thick Si layers on SiO_2 films but with the 200-nm-thick SiO_2 capping layer (a) and with 250-nm-thick photosensitive capping layer with the same thermal characteristics as SiO_2 (b), respectively. This figure shows that the light intensity was reduced with photosensitivity at the capping layer. The reason of this reduction may be the decrease of the net reflection of light by using the photosensitive capping layer.

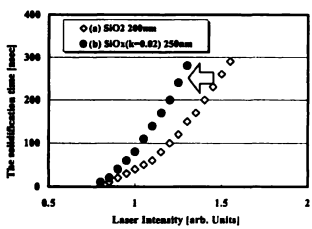


Figure 2. The comparison of the solidification time (calculation) at various laser intensity between the samples with transparent and photosensitive capping layer.

Enlarging the growth length with thin Si layer

Figure 3 shows the result of the time-dependent temperature distributions for the two samples. The structures of the samples were the same 50-nm-thick Si layers on the

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SiO_2 films with the SiO_2 capping layer and with the photosensitive capping layer, with various thicknesses respectively. The value of the flattop intensity during the light irradiation (30 nsec on the assumption of using a XeCl laser) was adjusted such that both the Si layer could withstand a peak temperature as high as 3000°C and that the capping layer as high as 1700°C. The other configuration was the same for both samples. This figure shows that the solidification time of Si with photosensitive layer is longer than that with transparent capping layer. The desirable intensity for the sample with the photosensitive capping layer is a little more than that for the transparent capping layer, but the heated capping layer with photosensitivity may bring a longer solidification duration. The thick capping layer play a role of the heat capacitance for the lateral growth of Si so that there may be the amount of the effective heat capacitor during the laser irradiation more than that with the transparent capping layer, even there are the same thicknesses. It is expected that the length of the lateral growth may be longer compared to that at using the transparent capping layer.

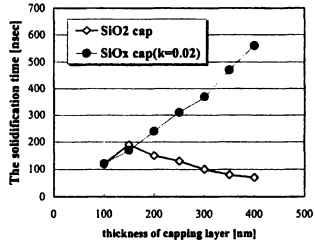


Figure 3. The comparison of the solidification time (calculation) at various thicknesses of the capping layer between the samples with transparent and photosensitive capping layer.

EXPERIMENTAL

SiOx was applied as the capping layer since it has a suitable light absorption coefficient against the KrF laser light (248 nm) and XeCl laser light (308nm), respectively, and since it has an ease to be made using a conventional mass production process of poly-Si TFT-LCDs. The detailed sample structure is shown in Fig.4. 30-nm-thick SiO_2 layers were inserted at the both surfaces of the Si layer for passivation. The combinations of the thicknesses of the layers are shown in Table 1. The stacked structures by Si, SiO_2 and SiOx films were made by advanced PECVD

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apparatus without braking vacuum [9]. The extinction coefficient of the SiOx layer changed with changing the SiH_4/N_2O flow rate ratio as shown in Fig.5. The SiOx films with κ=0.02 are satisfied at the ratio ranging for 24 to 27%. For excimer laser lights, the samples were irradiated by a single shot of the light pulse after dehydrogenation. Details of the ELA apparatus were reported elsewhere [5]. The micro-structural analyses of the crystallized Si films were performed by means of a SEM after Secco-etching.

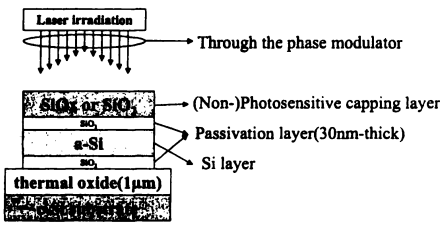


Fig.4 Schematics of the sample structure.

Table 1. Combinations of the thicknesses of the samples [nm]

No.	Objective	Cap SiOx	Cap SiO_2	Si
1a	Reduction of the	250	-----	200
1r	fluence	-----	170	200
2a	Elongating the growth	350	-----	50
2r	length	-----	100	50

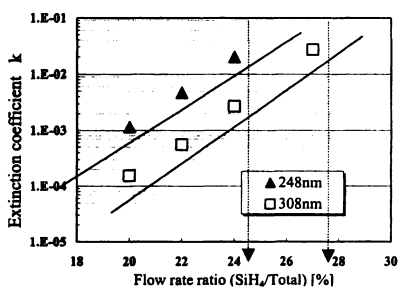


Fig.5 Extinction coefficient as a function of flow rate ratio SiH_4/Total

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RESULTS AND DISCUSSION

Figure 6 shows SEM images of Secco-etched films. 5-μm-long lateral growths were obtained at the KrF light intensity of 480 mJ/cm^2 for #1a sample and 680 mJ/cm^2 for #1r sample. The length is the same for #1a sample and #1r samples but the actual light intensity to #1a reduced to 70% of that of the #1r sample and became very near the typical value of the conventional ELA in spite of that the Si thickness was about 4 times as much as the conventional substrate structure.

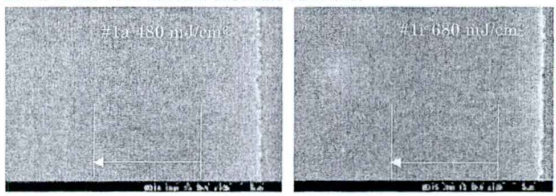


Fig.6 SEM images after Secco-etching of the samples with 200-nm-thick Si

Figure 7 shows the lateral growth length of Si as a function of the irradiated intensity. This figure shows that the 30% reduction of the irradiated light intensity was achieved using the photosensitive capping layer for the lateral growth length of 3 μm to 5 μm. These curves are the same dependency as Fig.2 so that a qualitative discussion about the lateral growth length may be allowed with using the "solidification duration" we proposed in this report.

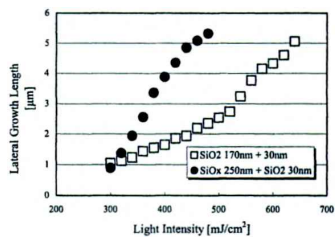


Fig. 7. The lateral growth length as a function of an irradiating light intensity

Figure 8 shows SEM images of Secco-etched films. 10-μm-long lateral growth was obtained at the XeCl light intensity of 540 mJ/cm^2 for #2a sample while 4-μm-long

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lateral growth for #2r sample [6]. #2r sample might work out the maximum lateral growth length under the condition of the Si thickness of 50 nm since the layers structure such as the thickness of the capping layer and the slope of the intensity profile were optimized [6]. The length for #2a was twice of that for #2r but with lower light intensity. These results suggest that the photosensitive capping layer is very attractive to obtain the longer lateral growth with lower irradiating laser light intensity.

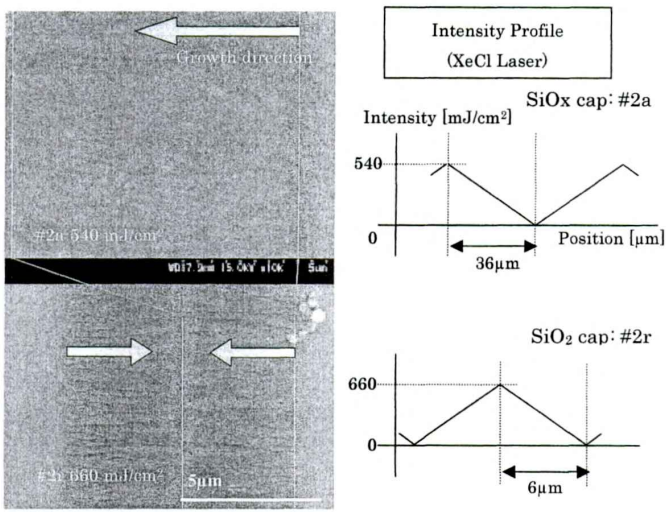


Fig. 8. SEM images after Secco-etching of the samples with 50-nm-thick Si and schematics of the irradiated light intensity.

CONCLUSION

The SiOx capping layer has demonstrated the long lateral growth of more than 5 μm with lower light intensity and thinner Si film. SiOx is suitable material for capping layer because of its compatibility with Si process. This light intensity and this thickness of Si are at the same level as that using in the mass production so that the advanced layer structure for our PMELA method could easily apply for commercial production.

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ACKNOWLEDGEMENTS

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THE ELECTRICAL CHARACTERISTICS OF THE POLY-SI TFTs FABRICATED BY 2-DIMENSIONAL GRAIN GROWING ELA METHOD

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We report the high performance poly-Si TFTs fabricated by 2-dimensional grain growing ELA method. The poly-Si TFTs have high field effect mobility and low threshold voltage due to high quality grain structure in the channel region. Dual-gate structure is used for precluding the perpendicular grain boundary in the channel region so that the poy- Si TFT has better electrical characteristics than single-gate poly-Si TFT with one perpendicular grain boundary in the channel region. Dual-gate poly-Si TFTs also has good characteristics of reliability due to the high quality grain structure near the drain junction. The driving current capability of each channel is similar so that the field-effect mobility and threshold voltage of poly-Si TFTs with different channel number are similar. High gain inverter is also successfully fabricated employing 2-dimensional grain growing ELA method.

INTRODUCTION

Polysilicon thin-film technology is becoming increasingly attractive for active-matrix liquid-crystal displays (AMLCD's) and other large-area electronic devices (1). To achieve system on glass (SOG), high performance Si devices on a large glass substrate are necessary. The electrical characteristics of poly-Si TFT such as field-effect mobility and threshold voltage are dependent on the grain size and grain microstructure (2). However, the grain size of poly-Si film recrystallized by conventional ELA may not be large enough for suitable device and circuit applications (3). Various efforts such as sequential lateral solidification (SLS), optical phase shift mask and pre-patterned laser beam mask have been reported to control grain size as well as grain boundary location.

The purpose of our work is to report the electrical characteristics employing a new ELA method, which can produce large lateral grains and control grain boundary location. We have already reported ELA method with floating active structure which produces the large lateral grain and controls the location of grain boundary (4). However, grain boundaries parallel to the current flow may disturb the carrier drift motion during operation of poly-Si TFT. A new ELA process decreases the number of grain boundaries parallel to current flow by employing the effect of pre-patterning. Dual gate structure annihilates the grain boundary perpendicular to current path. The poly-Si TFT that exhibits very high mobility is fabricated by single laser irradiation on selectively fabricated by single laser irradiation on selectively floating a-Si layer with multi-channel structure and dual gate structure. We have investigated the reliability of the poly-Si TFTs under the high current stress. In order to investigate the driving current capability of each cannel, we have fabricated the poly-Si TFTs with various channel numbers. High gain

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CMOS inverter is also successfully fabricated by 2-dimensional grain growing ELA method.

EXPERIMENTAL

The process of poly-Si fabrication is as follows. 50nm-thick sacrificial metal layer was deposited on oxidized Si substrate. After patterning of 13μm-wide rectangular metal layer, 100nm-thick bottom oxide, 100nm-thick a-Si and thin capping oxide were sequentially deposited. After definition of active island across the sacrificial metal pattern, the sacrificial metal under the a-Si active layer was completely removed by wet etch. The selectively floating structure was irradiated with single-pulse XeCl excimer laser (λ=308nm). A 100nm-thick TEOS (Tetra-Ethyl-Ortho-Silicate) based silicon dioxide as gate insulator was deposited by PECVD (Plasma Enhanced Chemical Vapor Deposition) after the upper capping oxide was stripped. A 500nm-thick Al electrode was deposited by sputtering. Ion implantation was carried out and impurities were activated by laser irradiation. A top-gate self-aligned device was fabricated without offset or LDD (lightly doped drain) structure. Post annealing such as hydrogenation was not carried out. It should be noted that the proposed TFT consists of two high-quality 6μm-long lateral grains and the Al gate electrode is defined inside the floating Si region, so that source/drain junction exists in the large lateral grain. In order to preclude grain boundary perpendicular to current path, dual gate structure is adapted with highly doped region between two 5μm effective channel regions.

RESULTS AND DISCUSSION

The proposed ELA method is illustrated in Fig. 1. It is well known that lateral temperature gradient in a melted Si film would induce the lateral grain growth (5). In our proposed ELA method employing floating active structure and multi channel structure, temperature gradient is induced in two directions (x-axis, y-axis) so that 2-dimensional grain growth occurs. Along the x-axis, an air-gap, of which thermal conductivity is very low, blocks the heat conduction to the substrate so that the lateral temperature gradient is successfully induced. In the Si region adherent to the substrate (region A), the heat absorbed in the molten Si film is conducted through the underlying substrate so that the melted Si cools off rapidly and begins solidification. However, the vertical cooling rate in the selectively floating Si region (region B) is remarkably reduced due to low thermal conductivity of the air-gap. The heat stored in the floating Si region would conduct laterally through the neighboring Si region adherent to the substrate, so that the significant lateral temperature gradient is occurred between the region A and B. Along the y-axis, temperature gradient also occurs because of surface tension effect (6) so that the number of parallel grain boundary is significantly reduced due to pre-pattern effect.

Fig. 2(a) is schematic diagram of the dual-gate poly-Si TFTs and Fig. 2(b) shows the transfer characteristics of the dual-gate structure poly-Si TFT which has no perpendicular grain boundary in the channel. Field effect mobility of n-channel TFTs and p-channel TFTs are 571cm^2/Vs and 292 cm^2/Vs, respectively. The high mobility value of the proposed TFT is due to the reduction of grain boundaries. Fig. 3 shows the schematic diagram and transfer characteristics of the single gate poly-Si TFT with one

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perpendicular grain boundary in the channel. Field effect mobility of single-gate poly-Si TFT is 367 cm^2/Vs on n-type TFT and 211 cm^2/Vs on p-type TFT.

To investigate reliability of the proposed poly-Si TFTs, the current source is biased at 1.2mA with grounded gate and drain electrode during 1000 seconds. Fig 3 shows the electrical characteristics change during the stress time. In spite of high current exceeding 1mA, the proposed poly-Si TFTs is scarcely degraded due to the high quality grain structure near the drain junction.

We have fabricated the poly-Si TFT with different channel number in order to investigate the driving current capability of each channel. Fig. 4 shows schematic diagram and transfer characteristics of the poly-Si TFT with different channel numbers. The width of each channel is 2μm. The filed effect mobility of 4channels, 2 channels and 1 channel are 526 cm^2/Vs, 514 cm^2/Vs and 517 cm^2/Vs, respectively. This results shows that the driving current capability of each channel is similar. We have also fabricated CMOS inverter. Fig. 5 shows the electrical characteristics of CMOS inverter fabricated by 2-dimensional grain growing ELA method. A small signal gain within the transition region is very high due to high field effect mobility of the proposed poly-Si TFTs.

CONCLUSION

We have fabricated high performance poly-Si TFTs by 2-dimensional grain growing ELA method. Dual gate structure has better electrical characteristics due to no perpendicular grain boundary in the channel region. We have investigated that each channel of multi-channel structure has similar capability of current driving. Under the high current stress exceeding 1mA, the proposed poly-Si TFTs are scarcely degraded due to the high quality grain structure near the drain junction. We have also fabricated CMOS inverter with high voltage gain.

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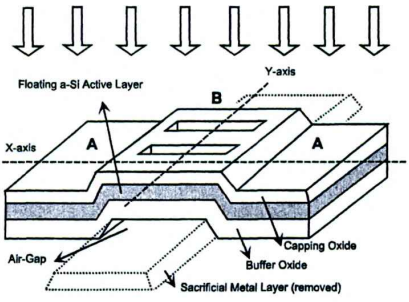
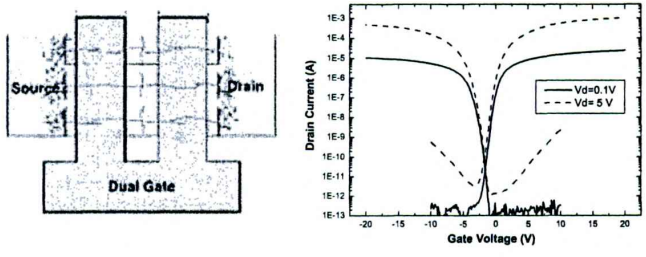
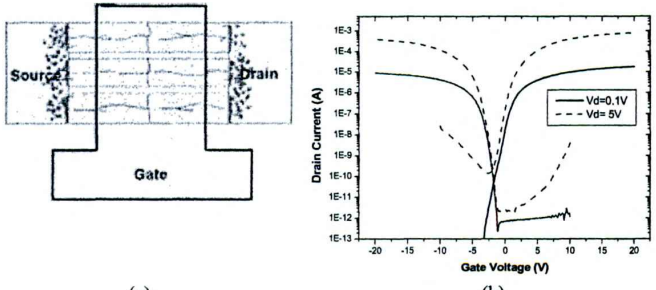


Fig. 1. Schematic diagram of the proposed ELA method.



(a) (b)

Fig. 2. The Schematic diagram and the transfer characteristics of the dual-gate poly-Si TFT without perpendicular grain boundary in the channel.



(a) (b)

Fig. 3. The Schematic diagram and the transfer characteristics of the singlel-gate poly-Si TFT with one perpendicular grain boundary in the channel.

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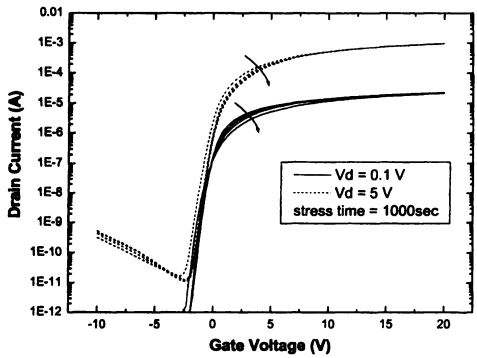


Fig. 3. The electrical characteristics change during the high current stress bias. Each sample is measured at 0s, 10s, 100s and 1000s.

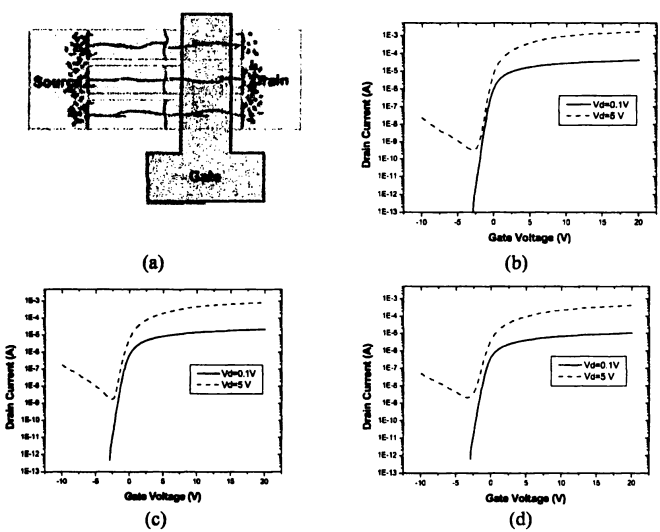


Fig. 4. The Schematic diagram and the transfer characteristics of the poly-Si TFT with different channel number: (a) schematic diagram (b) number of channels = 4 (c)) number of channels = 2 (d)) number of channels = 1

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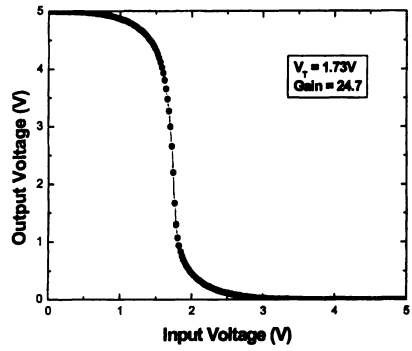


Fig. 5. Transfer characteristics of CMOS inverters with high voltage gain

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A NEW DUAL L-GATE STRUCTURE OF POLY-SI TFT FOR THE REDUCTION OF THE KINK EFFECT IN SLS/CW LASER METHOD

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ABSTRACT

A new device structure was proposed for the reduction of the kink effect in poly-Si TFTs which are crystallized by SLS or CW laser method. It was already reported in our previous work that the asymmetric dual gate structure of sub-TFTs could help to reduce the kink current of poly-Si TFT. In the proposed TFT, L-shape dual gate structure was employed for the asymmetry between sub TFTs. The one of sub-TFT was located in a parallel direction of grain growth and the other of sub-TFT was located vertically. It was verified by simulation and experimental results that the proposed dual L-gate TFT reduced the kink current of poly-Si TFT which had a fixed direction of grains in channel such as TFTs fabricated by SLS or CW laser method.

INTRODUCTION

Polycrystalline silicon thin film transistors (poly-Si TFTs) have attracted much attention for driving circuits in AMLCD and AMOLED due to high mobility and driving capability [1,2]. Recently, new laser crystallization methods such as sequential lateral solidification (SLS) and CW laser method have been reported in order to improve the mobility of poly-Si TFTs [3,4]. However, undesirable effects such as kink effect have not been settled yet. In this paper, we propose a new device structure for suppressing the kink effect in SLS and CW laser method, which have a fixed grain growth direction.

Many efforts to eliminate the kink effect have been reported such as lateral body terminal TFT and asymmetrical dual gate TFT [6,7]. In three terminal devices, asymmetrical dual gate TFT is an effective structure to reduce the kink effect. In the asymmetrical dual gate TFT, the ratio of the channel lengths between sub-TFTs should be high but this is limited by design rule.

We propose a new L-gate structure for the reduction of the kink effect of poly-Si TFTs fabricated by SLS or CW laser method. In the SLS or CW laser method, the silicon grain grows in a fixed direction by scanning of laser beam [3,4,5]. It was also reported that the TFT, which has the parallel direction of silicon grain with the direction of current, has superior characteristics to the TFT which has the vertical direction of silicon grain with the direction of current. So the difference of channel structure was used in the proposed device instead of asymmetric gate length.

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DEVICE STRUCTURE

Figure 1 (a) shows the reported asymmetrical dual gate structure and figure 1 (b) shows the proposed dual L-gate structure. In the proposed device structure, we employed the difference of the number of grain boundaries in the channel as an asymmetric structure instead of the difference of gate length in the asymmetric dual gate structure. The proposed structure may be useful when the gate length is limited by design rule. And there is no short channel sub-TFT, so that reliability of the proposed device would be improved better than that of the asymmetric dual gate TFT.

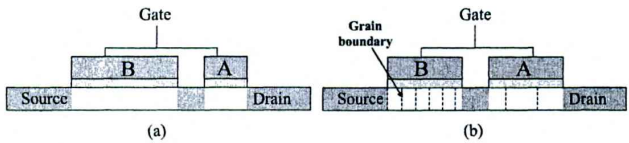


Figure 1 The device structures for suppressing the kink effect; (a) reported asymmetric dual gate TFT, (b) proposed dual L-gate TFT

Figure 2 shows the plane view of the proposed device. In the SLS method, which is widely used for the crystallization of amorphous silicon film, poly-Si grains are grown toward an identical direction as shown Figure 2 [7]. Therefore, the grain boundaries of the sub-TFT A is less than that of the sub-TFT B. This asymmetric structure affects the device characteristics similarly with asymmetric dual gate structure.

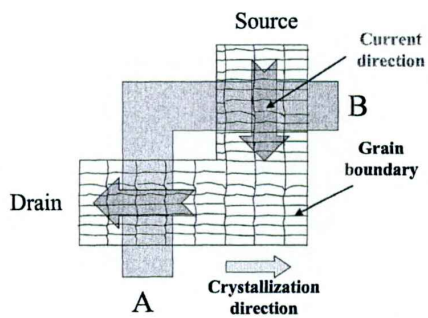


Figure 2 The plane view of proposed dual L-gate poly Si TFT

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SIMULATION AND EXPERIMENT

Figure 3 shows the output characteristics of conventional p-type TFTs which were used in simulation. The W/L ratio of sub-TFT was 10 μm/ 8 μm in the simulation. The grain direction of sub-TFT A is parallel to the current direction and that of sub-TFT B is vertical to the current direction. The mobility of sub-TFT A was about double of that of sub-TFT B. However, the kink current was observed similarly in both TFT.

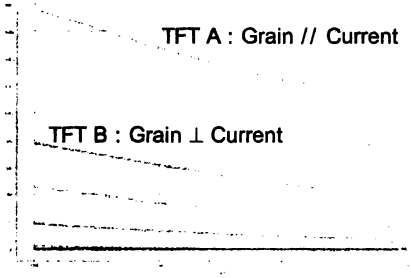


Figure 3 The output characteristics of sub-TFTs along the direction of grain and current

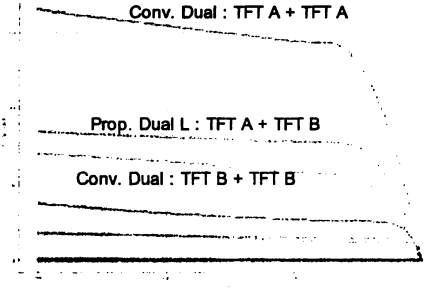


Figure 4 Simulation; the output characteristics of a conventional dual gate TFT and the proposed dual L-gate TFT (p-type)

Figure 4 shows the simulation results of conventional dual gate TFT and the proposed TFT. The conventional dual gate TFTs were composed of 2 sub-TFT A or 2 sub-TFT B respectively and the proposed TFT consisted of sub-TFT A (drain side)

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and sub-TFT B (source side). In the output curve of the proposed TFT, the total current was decreased compared with conventional dual gate TFT, which consists of two sub-TFT A, due to the increase of channel resistance. However, the kink effect was much suppressed as shown in Figure 4. The current of the proposed TFT was higher than that of conventional dual gate TFT, which consists of two sub-TFT B, and the saturation characteristic of the proposed TFT was also better than that of conventional dual gate TFT. So it could be verified that the kink current of poly-Si TFT was reduced by the proposed device structure.

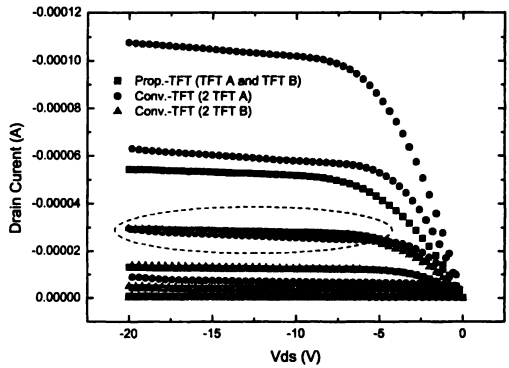


Figure 5 Measurement; the output characteristics of a conventional dual gate TFT and the proposed dual L-gate TFT

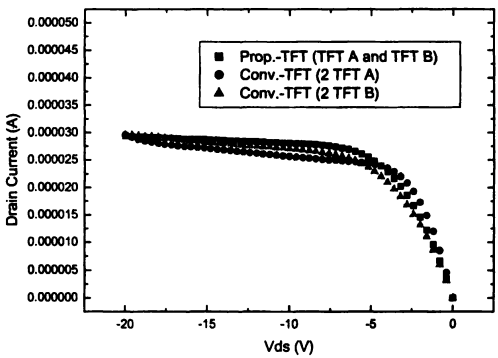


Figure 6 Measurement; the output characteristics in similar saturation current level

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Figure 5 and 6 are the experimental results of the fabricated poly-Si TFTs. The W/L ratio of sub-TFT was 10 μm/ 5 μm in the experiment and SLS was employed for the crystallization of amorphous silicon layer. Figure 5 shows the measured output characteristics of conventional dual gate TFTs and the proposed dual L-gate TFT. The experimental results showed similar tendency with simulation. The current of the proposed TFT was lower than that of conventional dual gate TFT (2 TFT A) and higher than that of conventional dual gate TFT (2 TFT B). However, the kink current of the proposed TFT was reduced compared with conventional TFTs. Figure 6 is the enlarged figure of the dashed ellipse in Figure 5. In the similar current level (about 30 μA), the proposed dual L-gate TFT exhibits the best saturated characteristic among three TFTs. It was verified by this result that the proposed dual L-gate structure could help to reduce the kink current of poly-Si TFT fabricated by SLS method as asymmetric dual gate structure.

CONCLUSION

We have proposed the new asymmetric dual gate poly-Si TFT, which could suppress the kink current successfully. The proposed device adopted dual L-gate structure for the asymmetry of sub-TFTs which has same gate length. And the proposed structure could reduce the kink current in the poly-Si TFTs which had a fixed direction of grains in channel such as TFTs fabricated by SLS or CW laser method without a gate length modulation.

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RELIABILITY STUDY OF MILC POLY-SI TFTs ON PLASTIC SUBSTRATES USING POSTFLEX TRANSFER PROCESS

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INTRODUCTION

Transfer approaches for fabricating poly-Si TFTs on plastics can avoid the problems caused by the use of these substrates, such as temperature limitations and mechanical instability during processing. Some prototype displays using transfer processes have already been demonstrated. Transfer approaches include surface free technology by laser annealing (SUTLA) from Seiko/Epson [1, 2], total mother substrate etching by Sony [3, 4], and PostFlex transfer technology from Penn State University/NanoHorizons [5-7]. PostFlex transfer technology using wet chemical etching of a sacrificial layer can reliably release a poly-Si TFTs/polymer substrate structure from the mother substrate quickly and the poly-Si formation can be by laser or solid phase crystallization.

Here we report on the reliability of PostFlex high performance poly-Si TFTs on plastic made by the metal induced lateral crystallization (MILC) solid phase crystallization approach. These p-type poly-Si TFTs typically had a linear field effect hole mobility of ~170 $cm^2/V{\cdot}s$, on/off current ratio of 10^8 at V_{ds}= -0.1V, and sub-V_t swing of 200mV/dec which remained the same before and after separation and transfer [5, 6, 7].

In actual applications, thin film transistors on polymer substrates will be unavoidably exposed to different environmental conditions. The resulting temperature, light, and mechanical stressing will all affect the performance of the devices. Consequently, the characterization of the devices under various stresses is very important for overall system design. In this study, electrical characterization results of PostFlex process prepared MILC poly-Si TFTs on BCB/parylene substrates under various temperature, light intensity, and mechanical strain conditions are presented and discussed.

EXPERIMENT

The PostFlex transfer scheme is illustrated in Fig. 1. In the last step of the TFT fabrication shown in step (a), the contact windows are opened in the gate, drain, and source areas. Part of the windows extends through the SiO_2 capping layer and the contact metal fills all these windows in step (b). In step (c), trenches are etched around the TFTs down to the column/void nano-Si sacrificial layer and the trenches are filled with channel forming (stress release) metal sacrificial materials (e.g., Ni, Cu, or other easily removable materials) by lift-off. In step (d), an adhesion-enhancing, planarizing BCB layer is coated. This is followed by surface roughening plasma treatment on the BCB and the coating of 40μm parylene in step (e). In step (f), through holes for sacrificial layer removal are defined and dry-etched using Al as hard mask down to the channel forming metal sacrificial material. Next the metal sacrificial material is removed and the channel surrounding the TFT islands is formed in step (g). In step (h), final release using KOH is

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performed and the TFTs are now on the polymer substrate. For the tests of this study, an additional step was needed to electrically access the individual TFTs. This entailed dry etching the Si_3N_4 capping layer (See step (i)) allowing the contact pads to be exposed for electrical characterization. Fig. 2 shows the actual transferred MILC poly-Si TFTs on BCB/parylene substrate.

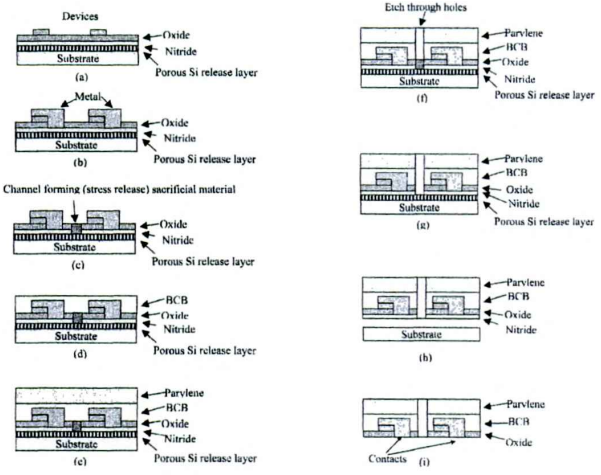


Figure 1 Two-step PostFlex transfer scheme.

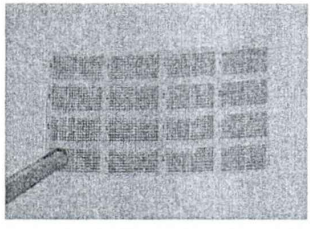


Figure 2 Transferred MILC poly-Si TFTs on BCB/parylene substrate.

Electrical characterization of the MILC poly-Si thin film transistors was performed using a computerized HP4145B Semiconductor Parameter Analyzer. The probes and the sample stage are enclosed in a dark metal Faraday shielding box to isolate the devices from interference. All the test cables are low noise 50Ω triax cable. A silicone oil heated thermal chuck was used to measure the devices at various temperatures. A 200W halogen lamp was used to obtain the light intensity to test the effect of illumination on the devices. The light intensity was calibrated using a Lux-meter (Cen-tech FX101). A test set with radiuses ranging from 16.7mm to 92mm was used to subject the separated TFTs on plastic to different bending statuses. This latter measurement was done with two types

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of bending as shown in Fig. 3: (a) compressive and (b) tensile strain. In all cases the bending was arranged to be parallel to the drain-source current direction.

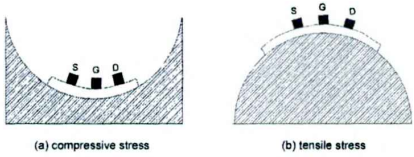


Figure 3 Sample configuration for the measurement of TFT characteristics with substrate bending. (a) TFT under compressive strain and (b) TFT under tensile strain.

RESULTS AND DISCUSSION

Fig. 4 presents the transfer characteristics of a typical MILC poly-Si p-channel TFT of this study while on the mother substrate before separation and on a polymer substrate after separation. It shows that the separation leads to a slight increase of the off-current while the rest of the curve is essentially the same. After the separation, the whole assembly has a structure of 40μm of parylene substrate / 3μm of BCB adhesion layer / poly-Si TFTs / 300nm of silicon dioxide (silicon nitride was etched to expose the metal contact pads). These separated samples are flat, which indicates that there is no overall stress after the separation. We now examine the effects of temperature, bending, and finally light on these separated transistors.

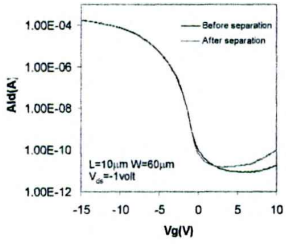


Figure 4 The transfer characteristics of a MILC poly-Si TFT before and after separation.

Fig 5. shows the extracted behavior of the threshold, off-current, and field effect hole mobility vs. temperature for separated transistors on plastic. Here the threshold voltage and field effect mobility are normalized to the values at 20°C and the off-current is taken at V_g = 1V. It can be seen that, in the studied temperature range, the poly-Si TFTs show an exponentially increased leakage current with an activation energy of 0.41eV, smaller field effect mobility, and slowly decreasing threshold voltage with increasing temperature.

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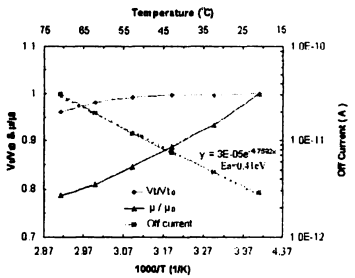


Figure 5 The effect of temperature on MILC poly-Si TFTs on polymer substrates.

The leakage current in poly-Si TFTs, in general, has contributions from thermionic emission, thermionic field emission, and field emission and each of these can dominate under different TFT working conditions [8] Thermal emission is expected to dominate under low gate voltage and low drain-source voltage conditions. Pure field emission dominates under high gate voltage and high drain-source voltage conditions. Under intermediate gate voltages and source-drain voltages thermionic field emission is expected to be the major factor in leakage current. It is also important to note that, in addition to V_g and V_{ds}, the distribution of trap states is also a factor that can decide when each of these three factors dominates [8]. The test results shown in Fig. 5 were done at low source-drain voltage (V_{ds}= -1V) and intermediate gate voltages (V_g = -8V to 8V). Consequently, thermionic emission and thermionic field emission are expected to be the main contributors to the off-current. At V_g = 1V and V_{ds}= -1V, thermal emission should be the major factor. This thermal emission current should have the same trend as that of carrier concentration of the undoped poly-Si inside the channel, which has an exponentially increasing relation with one over temperature and the activation energy should have, and does have, the same value of 0.41eV. The carrier mobility in a poly-Si channel in the on-state has two contributions [9]. One is from the scattering in the grains. The other is from the free carrier emission over the barriers at the grain boundaries. The first is characterized by a mobility μ_G in the grains similar to the mobility in single crystal MOS device and the second is represented by a mobility μ_{GB} which is thermally activated by the grain boundary barriers [10]. This leads to an overall effective mobility μ given by

$$\frac{1}{\mu} = \frac{1}{\mu_G} + \frac{1}{\mu_{GB}}$$

where $\mu_{GB} = \mu_0 \exp(\frac{-E_B}{KT})$. Here E_B is the grain boundary energy barrier. As seen from the above equations, μ_{GB} increases with an increase of temperature. The respective importance of both contributions depends on the value of the barrier E_B. Fig 5 shows that, for the temperatures studied for our MILC poly-Si TFTs, the transport in the channel in the saturation region is controlled by μ_G which, as expected, decreases due to the thermal (phonon) scattering when temperature increases. This demonstrates that our MILC process results in a channel region that contains few grain boundaries across the channel due to the lateral crystallization. This leads to the observed reduction of the overall hole

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field effect mobility with the increase of temperature. It has been reported that the field effect mobility of some poly-Si TFTs showed an opposite trend. In that case, the TFTs have a large E_B and the behavior of μ_{GB} dominates [9, 11].

The threshold voltage shift with temperature follows the trend seen in single crystal MOSFET devices [11, 12]. However, in single crystal MOSFETs, the threshold voltage variation with temperature is mainly due to the variation of the Fermi level ϕ_F

$$\phi_F = \frac{KT}{q}\ln\frac{N_B}{n_i} = \frac{KT}{q}\ln\frac{N_B}{\sqrt{N_c N_v}} + \frac{E_g}{2q}$$

where N_B, n_i, N_c, N_v, and E_g are the channel doping density, the intrinsic carrier density, effective density of states in the conduction band, effective density of states in the valence band, and band gap, respectively. With this picture, a change in temperature leads to a change in ϕ_F and V_T [11, 12]. While in intrinsic channel poly-Si TFTs, the possible reason for threshold voltage reduction with the increase of temperature is attributed to the reduction of the unfilled grain boundary trap states and the reduction of the grain boundary barrier E_B [9]. Grain boundary states can act as sinks for carriers thereby reducing the free carrier population. This filling of grain boundary states can also change E_B. Both of these contributions then affect the threshold voltage in poly-Si TFTs.

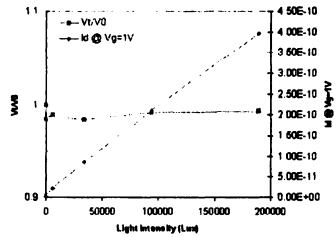


Figure 6 The effect of light illumination on MILC poly-Si TFTs on polymer substrates.

Fig. 6 examines the effect of light on separated TFTs. The data here are the threshold voltage and off-current data extracted from the transfer characteristics plot. It can been seen that the light illumination as high as 189,000 Lux only affects the leakage current of the MILC poly-Si TFT and the increase of off-current has a linear relation with the light intensity. It is also found in this study that the light illumination only influences the leakage current in the region corresponding to the thermionic emission regions in the temperature study. This reveals that the off-current enhancement due to the light illumination has a similar mechanism as that due to temperature's effect. Thermal excitation and the resulting thermionic emission is the major factor that enhances the off-current in the low off-state gate voltage region. As seen, even though poly-Si thin films normally have a much lower light adsorption coefficient than a-Si thin films, the adsorbed photon energy can also assist in exciting carries and in allowing them to be emitted over the barrier E_B thereby leading to a higher off-current (photocurrent). However, it is important to note that compared to an optimized a-Si TFT, the studied

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separated MILC poly-Si TFTs on a parylene substrate have much smaller off-current photosensitivity [13].

We now report on the bending stress studies of these separated transistors. The sequence of tests was: flat → tensile at radius 92mm → tensile at radius 64mm → tensile at radius 50mm → tensile at radius 35mm → tensile at radius 16.5mm → compressive at radius 92mm → compressive at radius 64mm → compressive at radius 50mm → compressive at radius 35mm → compressive at radius 16.5mm → flat.

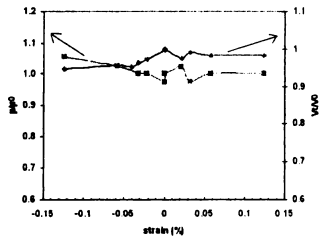


Figure 7 The effect of mechanical stress on MILC poly-Si TFTs on polymer substrates.

Fig. 7 shows the relative field effect mobility and threshold voltage of our separated MILC poly-Si TFTs under compressive and tensile strain. All the values are relative to the values at initial flat conditions. In this study, since the Young's moduli of BCB and parylene are both around 3GPa and the silicon/silicon oxide Young's moduli are around 180GPa, the whole separated assembly can be equated to a two-layer structure: the device layer with a thickness of 0.7μm (0.3μm of capping oxide, 0.1μm of active layer, and 0.3μm of poly-Si gate) and polymer substrate with a thickness of 43μm (40μm of Parylene and 3μm of BCB). According to Suo et al. [14], smallest bending radius at 16.5mm just causes a very small strain of 0.13% since the polymer substrate is very thin. As may be seen from Fig. 7, both the threshold voltage and linear field effect mobility had no substantial change for the whole bending range. The threshold voltages under strain are slightly lower than when the devices are strain free. Under compressive strain, the field effect mobility is higher while under tensile strain, the field effect mobility on average is lower. This trend agrees with the results reported by Asano et al. [4] in their laser crystallized low temperature p-channel poly-Si TFTs (LTPS).

There are very few reports discussing the mechanism of the effects of mechanical strain on the performance of silicon thin film transistors. Most are focused on a-Si TFTs. Won et al.[15] did tests on the performance of a-Si TFTs under various strain conditions. They found that under compressive strain the field effect mobility decreases and in tensile strain the field effect mobility increases and attributed these changes to the changes of Urbach of a-Si:H. Mechanical compressive strain increases the disorder of the material; hence, increases the Urbach energy and the conduction band tail width. As a result, the electron mobility decreases. On the other hand, they found that tensile strain had opposite effect on the mobility. The threshold voltage increased notably in both strain conditions. Glekova et al. [16] observed the same trend in field effect mobility change under strains in their a-Si TFTs, but the threshold voltage hardly changed under all strain

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conditions. They found it difficult to clearly correlate the changes in the current-voltage characteristics to their physical origin due to TFTs' complex multi-layer structure and proposed the following factors may cause the changes: the piezo-resistive effect in undoped and n-type doped a-Si:H that affects the contact resistance; strain-induced change in the band gap that affects the slope of the conduction-band tail; or changes in the dangling bond density of the a-Si:H channel materials. The above results from a-Si TFTs are in agreement with the results obtained for poly-Si n-channel laser crystallized LTPS TFTs and opposite to those seen for p-channel LTPS TFTs as reported by Asano et al. [4]. Compared with a-Si TFTs, our MILC poly-Si TFTs have an even more complex structure. This structural complexity mainly lies in the silicon of channel area. Unlike an a-Si film, a poly-Si film is not a uniform material. The band gap parameters have spatial variations due to the existence of the grain boundaries and the random location of the grain boundaries. The mechanical strain should have an effect on grain boundary properties and, therefore, this makes the understanding of the mechanism of strain effects on poly-Si TFTs even harder. Clearly materials with randomly oriented grains would be expected to have a different response to strain than a material such as our MILC Si with its oriented grains.

SUMMARY

A novel two-step separation technology for transferring high temperature fabricated TFTs onto flexible plastic substrates was developed. This PostFlex technology can transfer poly-Si TFTs onto plastic substrates with high yield. The effects of separation, temperature, light illumination, and mechanical strain on these MILC TFTs after separation were studied. The study shows that all the above factors have some influence on the performance of transferred MILC poly-Si TFTs. Compensation may be needed in system design to compensate for this.

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REDUCTION OF THE LEAKAGE CURRENT OF THIN-FILM TRANSISTOR ON METAL-INDUCED LATERALLY CRYSTALLIZED POLYCRYSTALLINE SILICON

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ABSTRACT

Leakage current was found to be reduced when metal-induced lateral crystallization was performed prior to transistor island formation. The reduction was found to be higher for shorter channel width. An explanation based on residual nickel concentration is proposed.

INTRODUCTION

Low temperature crystallization of amorphous silicon (a-Si) thin film has been attracting considerable attention because of its wide applications in large area electronics, such as flat-panel display and image sensor[1-5]. Metal-induced laterally crystallized (MILC) polycrystalline silicon (poly-Si) is a promising material for fabricating thin-film transistor (TFT) based active matrix on glass substrate[6,7]. TFTs built on MILC poly-Si have been shown to exhibit high carrier mobility, good device uniformity and simple fabrication process.

Since flat-panel displays (FPDs) require active pixel TFTs with on-off current ratio more than 10^6 and leakage current lower than 10pA, the leakage current of MILC poly-Si TFT is one of the key factors in determining if MILC poly-Si TFT technology can be practically utilized in active-matrix FPDs. Besides grain boundaries, residual nickel in an MILC poly-Si TFT active island may also have an undesirable influence on TFT leakage current.

Reported methods for reducing leakage current in an MILC poly-Si TFT are (1) metal-induced unilaterally crystallization (MIUC) [8-9], (2) nickel gettering, (3) post-crystallization laser annealing [10] and (4) employing lightly-doped drain structure to decrease junction electric field[11]. The penalty of using the last three techniques is increased process complexity and cost. It is desirable to develop alternative techniques of reducing leakage current without increase in process complexity.

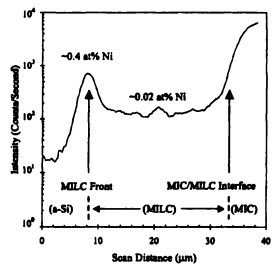


Figure 1. Distribution of nickel concentrations in different regions of MILC poly-Si thin film.

From the nickel distribution shown in Figure 1, it is clear that nickel concentration is the highest

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within the MIC region and the lowest within the MILC region. The nickel concentration at the MILC front is much higher than that within the MILC region. This implies that MILC poly-Si resulting from non-patterned a-Si thin film will have different states of crystallization and different distribution of nickel concentration, when compared to that resulting from patterned a-Si island with edge confinement. The effects of switching the order of island patterning and lateral crystallization were studied. TFTs were fabricated and transistor characteristics are compared in this report.

MIUC TFT DEVICE FABRICATION

Two types of TFTs were fabricated in the same process, one (Type A) with active islands formed before MILC and the other (Type B) with active islands formed after MILC. The detailed fabrication process steps are summarized in Figure 2.

500nm thick low-temperature oxide (LTO) diffusion barrier layer was formed using low-pressure chemical vapor deposition (LPCVD) on Corning 1737 glass substrates. 100nm thick LPCVD a-Si thin film was next formed on the LTO at 550℃. This would become the TFT active layer. Islands for Type A TFTs were patterned. 200 nm LTO was deposited as the nickel masking layer. After the opening of the crystallization-inducing holes, 5nm nickel was deposited using electron-beam evaporation. MILC was then performed in nitrogen atmosphere at 550°C for 10 hours. The rate of crystallization was ~4μm/hour.

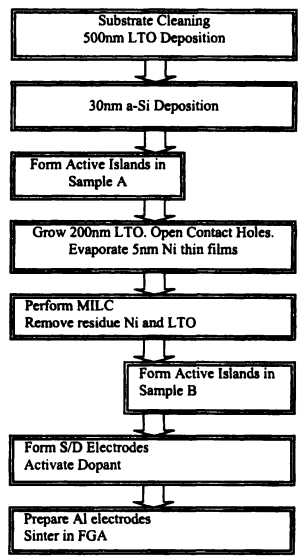


Figure 2. Process flow of Types A and B MILC poly-Si TFTs.

After the removal of Ni in 120 °C heated sulfuric acid and hydrogen peroxide solution and the LTO masking layer, the active islands for Type B TFTs were formed. All processes for Types A and B TFTs were identical from this point on. 100nm LTO was deposited as the gate oxide and a-Si formed using metal-induced crystallization (MIC) was used as the gate electrode. The gate, source and drain regions were then implanted with boron at an energy of 40KeV and at a dose of $4 \times 10^{15} cm^{-2}$. The implanted dopants were thermally activated for 8 hour at 550°C before contact holes were opened and aluminum metal electrodes were formed. The TFTs were tested after final sintering in forming gas for 30mins at 380°C.

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EXPERIMENT RESULTS

A photograph of two of the active islands of Type A TFT is shown in Figure 3. The stripes on the left hand sides of the active islands are the MIC regions, located within the crystallization-inducing holes. The MILC fronts with high nickel concentration moved right with the crystallization and stopped at the right most edges of the active islands.

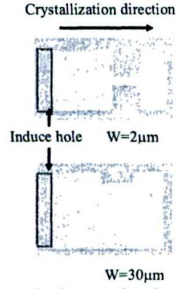


Figure 3. Photographs of active islands patterned before MILC.

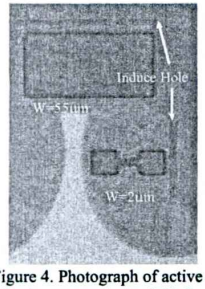


Figure 4. Photograph of active islands patterned after MILC.

A photograph of Type B TFT immediately after active island patterning is shown in Figure 4. The dark green regions are covered with photoresist. Removed from the active islands are the MILC/MIC interface and all MILC fronts with high residual nickel concentration. It can be readily seen in Figure 4 that the direction of MILC is not necessarily parallel to the channel conduction direction.

The transfer characteristics of Types A and B TFTs are shown in Figure 5. Both types of TFTs exhibit high mobility of ~100cm^2/Vs, steep sub-threshold slope of ~ 0.5V/decade and low threshold voltage of <5V. However, the leakage current behavior was quite different.

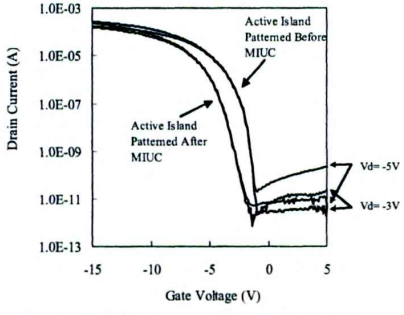


Figure 5. Transfer characteristics of p type MILC poly-Si TFTs with active island patterned before and after MILC at different drain bias voltage V_d.

For Type A TFTs with active islands patterned before MILC, the minimum leakage current for a TFT with channel width/length of 12μm/5μm is about 24.5pA at a drain voltage (V_d) of -5V. The transfer characteristics also reveal that Type A TFTs have high gate-induced leakage current. The leakage current is as high as 212pA at a gate bias (V_g) of 5V and a V_d of -5V. For Type B TFTs with active islands patterned after MILC, the minimum leakage current for a TFT with the same channel width/length ratio is 5.25pA at V_d= -5V. A reduced dependence gate bias is

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also evident. The leakage current is about 10.8pA at V_g= 5V and V_d=-5V.

Shown in Figure 6 is the dependence of the average minimum leakage current per unit channel width at V_d=-5V and the average leakage current per unit channel width at V_d=-5V and V_g=5V on the channel width.

It can be seen that the average leakage current per unit channel width of Type B TFT is much lower than that of Type A TFT. This is particularly true for TFTs with small channel width of 2 and 3μm. The difference between the leakage current per unit channel width can be almost 2 orders of magnitude.

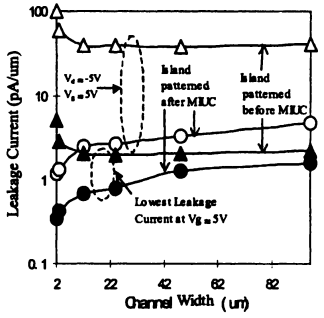


Figure 6. Dependence of the leakage current per unit channel width on the channel width of Types A and B TFTs.

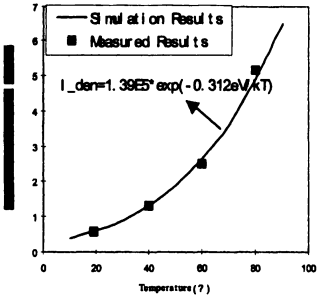


Figure 7. Measured variation of the leakage current with device temperature for p-type MIUC TFT with active island patterned after MILC. An analytical fit is also shown.

Show in Figure 7 is the dependence of the leakage current per unit width of Type B TFTs on device temperature. A good fit to this dependence is

$$I_{den} = 1.39 \times 10^5 \times e^{\left(-0.312eV/kT\right)}$$

with an activation energy of ~0.312eV. The leakage current per unit width is about 5pA at 80 °C, which is still acceptable for active-matrix FPDs.

DISCUSSION

It is presently suggested that the difference in leakage current behavior of the two types of TFTs is caused by the different residual nickel concentrations in the active channels.

For Type A TFT, the MILC front with high nickel concentration moves with the crystallization front and stops at the edge of an active island. Although the TFT channel is located within the MILC region, nickel residing on the left and right side of the active island diffuses back into the TFT channel during subsequent thermal treatments, such as dopant activation. Moreover, the lateral edges of the channel also function as MILC front stopping edges, where the nickel concentration should be higher than that within the TFT channel. The higher nickel concentration causes higher leakage current.

Furthermore, convergent flux of nickel into the channel occurs when the channel width is

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smaller than that of the crystallization-inducing window (Fig. 8). Consequently, nickel concentration within the channel increases with decreasing channel width, resulting in an increase of the average leakage current per unit channel width.

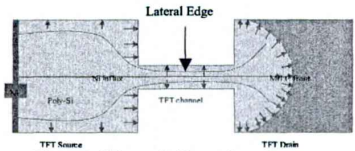


Figure 8. Schematic illustration of convergent flux of nickel into narrow TFT channel in a Type A TFT.

For Type B TFTs, the movement of an MILC front is not constrained by any edge of an a-Si island. Consequently, an MILC front moves freely, unless it collides with another MILC front. By confining TFT active islands within a high quality MILC region, MILC/MIC interface and all MILC fronts with high residual nickel concentration are eliminated. Hence, nickel concentration in the channels of Type B TFTs is believed to be lower than that of Type A TFTs.

However, if the channel width is larger than the length of the crystallization-inducing hole, MILC will take place along directions not entirely parallel to the direction of channel conduction. This might be the reason for the increase of average leakage current per unit channel width as the channel width is increased.

CONCLUSIONS

MILC Poly-Si TFTs with active islands patterned before and after MILC have been investigated. Both types of TFTs exhibit high carrier mobility. However, the leakage current is reduced for TFTs with active islands patterned after MILC. The reduction becomes more obvious as the channel width was narrowed to 2 and 3μm. The leakage current per unit channel width of TFT with active island patterned after MILC was smaller than 1pA at room temperature and remained small even up to 80 °C.

ACKNOWLEDGMENT

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LOW-TEMPERATURE MICROWAVE PLASMA OXIDATION FOR GATE DIELECTRICS OF Poly-Si TFTs USING HIGH-DENSITY SURFACE WAVE PLASMA

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ABSTRACT

Low temperature oxidation for gate dielectrics is a key technology for Poly-Si TFTs. Our purpose is to obtain an excellent SiO_2/Si interface properties under low-temperature process. We have proposed a stacked gate insulator with a PE-CVD film on an low-temperature oxidation layer in order to strike a balance between interface quality and process throughput at a low temperature. An atomically flat SiO_2/Si interface was obtained by oxygen radical oxidation even at a process temperature of 300°C. Surface-wave plasma is one of the most promising methods for radical oxidation. It reduces bulk plasma heating and lowers electron temperature, which is suitable for a low-damage process for forming the gate insulator. Neither oxidation rate nor interface states density was affected by the surface orientation of the crystalline Si substrate on which an oxide layer of several-nanometers-thick was prepared by the surface-wave plasma method. The TFT characteristics showed good mobility property. An extension to the application of microwave PE-CVD is also discussed.

INTRODUCTION

System on glass (SOG) is an innovative technology for making user-friendly displays. Low-temperature poly-silicon thin-film transistors (LTPS-TFTs) can be used to integrate the numerous circuits needed for SOG technology, and forming gate dielectrics at low temperatures is a key technology for making LTPS-TFTs. Of the low-temperature oxidation methods that have been reported [1]-[6], those using microwave plasma, especially surface-wave plasma (SWP) are the ones most likely to provide high electron density and low ion energy needed for improving the characteristics of the SiO_2/Si

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interface [4]. We have developed a process for making LTPS-TFTs that combines low-temperature SWP oxidation and plasma-enhanced chemical vapor deposition (PECVD) and that yields good interfaces and oxide layers of practical thicknesses [7][8]. Ito et al. from Toshiba reported that radical oxidation at temperatures between 700°C and 900°C produced atomically flat SiO_2/Si interfaces [9]. We have confirmed the effectiveness of radical oxidation even in a low–temperature process and have evaluated the properties of the interfaces produced using low-temperature SWPs.

This paper first reviews the features of SWP we generate and then, describes the electrical and the structural properties of the oxide prepared by using this plasma. It also discusses the characteristics of a TFT made using the low-temperature oxidation for the gate insulator and an extension to the use of microwave PE-CVD for the fabrication of stacked layers.

EXPERIMENTAL

Figure I shows a schematic diagram of the plasma oxidation system using SWP. 2.45-GHz microwaves were introduced into a 300-mm-square chamber through a quartz window. The SWP produced using pure O_2 gas or a Kr/O_2 gas mixture was generated at an average power of 1200 W. The total pressure was fixed at 80 Pa. Before the P-type single-crystal silicon (100)-oriented or (111)-oriented substrates were oxidized, they were treated with 0.5 % HF for 2 minutes and rinsed in deionized water. The substrate was placed 54 mm from the quartz window (Z = 54 mm), and the substrate temperature was kept at 300°C during the oxidation. The electron density and the electron temperature

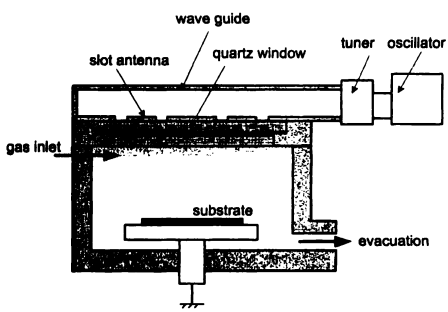


Fig. 1. Schematic diagram of microwave (2.45 GHz) plasma oxidation system.

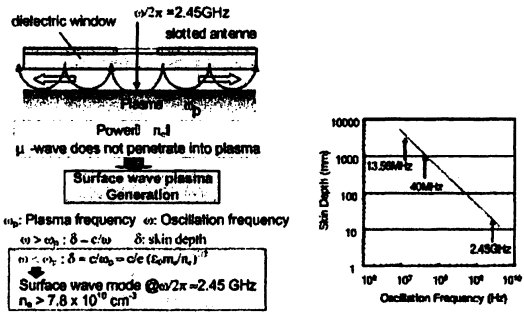
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were measured using the Langmuir probe method, and the oxygen atom density was measured using actinometry [10]. The Si 2p X-ray photoelectron spectra and O 1s photoelectron energy loss spectra were measured at soft-X-ray undulator beam line (BL27SU) of the Super Photon Ring 8 GeV (SPring-8) [11]. Both VHF (40 MHz) PE-CVD and microwave PE-CVD were used to prepare the SiO_2. VHF was applied to a conventional parallel electrode. The microwave PE-CVD was carried out in the same reactor shown in Fig. 1, but the gas inlet was modified into two parts: one near the quartz window for discharge gas, the other near the substrate for source gas. Tetraethoxysilane (TEOS) was used as Si source gas. The fixed charge density properties of the MOS device were calculated from the C-V measurements made using evaporated aluminum electrodes.

RESULTS AND DISCUSSION

1. Surface-wave plasma generation

High-electron-density plasma could be obtained by increasing either the applied power or the oscillation frequency. Increasing the applied power increases the amount of electrons generated, whereas increasing the frequency increases the efficiency of the generation. When the electron density n_e continues increasing and results in the oscillation frequency ω < plasma frequency ω_p, the surface-wave plasma condition is expected. As shown in figure 2(a), the n_e should be more than 7.8×10^{10} cm^{-3} to maintain



(a) Condition of surface-wave plasma (b) Skin depth vs. oscillation frequency.

Fig. 2. Generation of surface wave plasma and the relation between skin depth and oscillation frequency.

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the surface-wave mode when the oscillation frequency is 2.45 GHz. Skin depth is also an important parameter that has to be taken into account in order to avoid plasma damage, and skin depth is shown in Figure 2(b) as a function of the n_e. We can see there that damage can be avoided by keeping the substrate at least 20 mm away from the microwave plasma.

2. Radical oxidation

The oxide thickness obtained on Si(100) and Si(111) substrates when the Kr/O_2 ratio was 97/3 is shown as a function of plasma oxidation time in Figure 3, where we can see that the surface orientation did not affect to the oxidation rate. The initial plasma oxidation rate was very fast, and an oxide layer about 1-nm-thick was obtained within 5 seconds. Then the plasma oxide grew under diffusion-limited conditions as the thickness increased linearly with the square root of time.

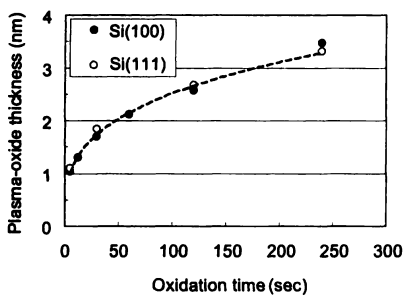


Fig. 3. Time dependence of plasma-oxide thickness on Si(100) and (111) substrates.

The dependence of interface states density on the substrate orientation was investigated by using Kr/O_2 surface-wave plasma to oxidize Si(100) and Si(111) substrates to thicknesses from zero to 3 nm and then using $TEOS/O_2$ gas to produce a 30-nm thickness of SiO_2 by VHF (40 MHz) PE-CVD. Figure 4, the interface states density varied widely when there was no plasma oxide, and the insertion of the plasma oxide was effective in improving the interface property. Almost no difference was found between the case of Si(100) and (111) substrates.

The thickness of the plasma-oxide film at an oxidation time of 4 minutes (○) and the square root of the calculated oxygen atom density (●) are shown in Figure 5 as functions of the Kr dilution ratio. The thickness of the plasma-oxide film is proportional to the square root of the oxygen atom density in the diffusion-limited condition of oxidation.

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The oxidation rate was primarily determined by the oxygen atom concentration. At the Kr dilution ratio of about 99%, both the oxidation rate and the atom density increased.

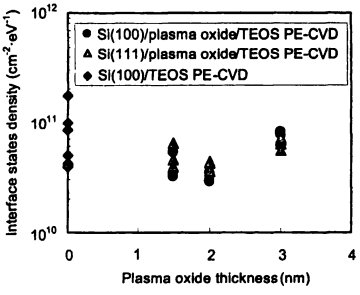


Fig. 4 Interface states density as a function of plasma-oxide thickness on Si (100) and (111) substrates.

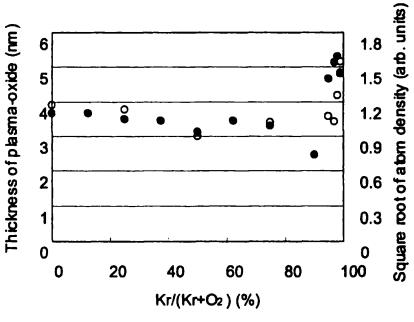


Fig. 5. Plasma-oxide thickness (○) and square root of calculated oxygen atom density (●) as functions of the Kr dilution ratio.

Parabolic rate constants of oxidation were also plotted against oxidation temperature for cases with and without Kr dilution, but no significant difference could be found between the parabolic rate constant and the activation energy [12].

The SiO_2/Si interface structures were evaluated by using the soft X-ray undulation beam line of the SPring-8. Si 2p photoelectron spectra were measured with an incident energy of 1050 eV. The spectrum was decomposed into the Si $2p_{1/2}$ and Si $2p_{3/2}$ spin-orbit partner lines. The amount of Si^{n+}, which is expressed in one monolayer (ML) of 6.8×10^{14} cm^{-2}, are listed in Table 1. Here it is considered that the normalized intensity

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(NSi $^{n+}$/NS) for the Si 2p $_{3/2}$ spectrum originated in the Si $^{n+}$ can be approximated as $N_n/(n_s\Lambda_s \cdot \sin\theta)$, where NS, N_n, n_s, Λ_s, and θ represent the Si 2p $_{3/2}$ spectral intensity arising from the Si substrate, the areal density of Si^{n+}, the density of Si atoms in a Si substrate, the escape depth of Si 2p photoelectrons in Si, and the photoelectron take-off angle, respectively [13]. In these analysis, 5×10^{28} m^{-3} was used for n_s, and 1.59 nm for Λ_s. In all cases the total amount of suboxides was approximately one ML. This indicates that the steepness of the structural transition area is almost the same in these three oxides.

Table 1 Amount of Si^{n+} and total amount of suboxides

	Amount of suboxide (ML)			
	Si^{1+}	Si^{2+}	Si^{3+}	total
Kr/O_2 Plasma oxide	0.33	0.26	0.36	0.95
O_2 Plasma oxide	0.27	0.27	0.42	0.96
Thermal oxide	0.26	0.26	0.27	0.79

The effect of Kr dilution appeared in the O 1s photoelectron energy loss spectra shown in figure 6. In addition to the energy loss at a threshold energy of about 9 eV [14][15], an energy loss at a threshold energy of 3.5 eV was observed for all oxide films. The amount of energy loss at a threshold energy of 3.5 eV were ranked in the following order:

Kr/O_2 plasma oxide < thermal oxide < pure O_2 plasma oxide

A value of 3.5 eV corresponds to the minimum energy required for direct interband transition at the Γ point in the energy band structure of Si [16]. The O 1s photoelectrons lose their energy in Si substrate by exciting the direct interband transition when O 1s photoelectrons penetrate into Si substrate before escaping into vacuum. The O 1s photoelectrons also lose their energy in oxide by exciting the direct interband transition between the electronic states penetrated from Si substrate into oxide [17]. In both cases, the number of O 1s photoelectrons escaping into vacuum without inelastic scattering in oxide film decreased as the uniformity of silicon oxide film increased. Therefore, uniformity resulted in the following order:

Kr/O_2 plasma oxide > thermal oxide > pure O_2 plasma oxide

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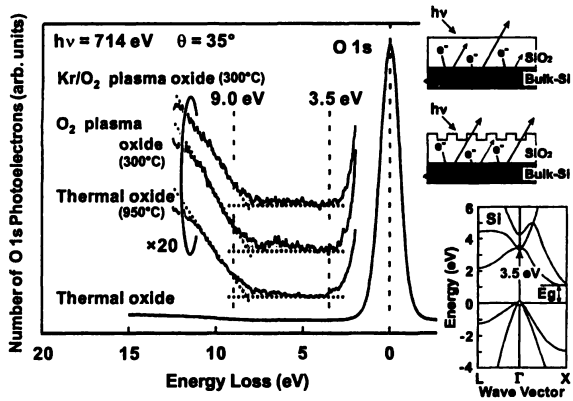


Fig. 6. O 1s photoelectron energy loss spectra.

Thus, Kr dilution may enhance the surface reaction and improve the SiO_2 homogeneity. However, we also observed disadvantages of the Kr dilution. Figure 7 shows the interface states density as a function of the oxide thickness. For the thicknesses

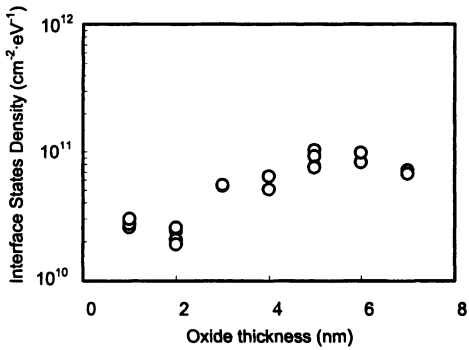


Fig. 7 Interface states density as a function of the oxide thickness.

not more than 2 nm, the states density was low, but it increased with the increase in the oxide thickness. The oxidation time for 2 nm, 3 nm and 4 nm in thickness corresponded to 47 s, 160 s and 340 s respectively. Longer exposure to the Kr diluted plasma caused

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damage to the interface.

The relation between the O_2^+ ion energy and the Kr dilution ratio was investigated by using quadropole mass spectroscopy [18]. The amount of O_2^+ ion increased drastically when the Kr dilution ratio was more than 95%. The O_2^+ ion energy itself also increased to about 4 eV when the dilution ratio was 99%. The moderate O_2^+ ion bombardment may improve the homogeneity of the oxide mentioned above. Meanwhile, if the tail of the O_2^+ ion energy distribution exceeds 4 eV, there may cause the damage onto the interface because the Si-O bonding energy was reported to be 3.68 eV [19].

Figure 8 shows HR-TEM pictures of SiO_2/Si interfaces prepared by conventional dry oxidation at 950°C and by atomic oxygen radical oxidation from Kr/O_2 gas at 300°C. A previous report [9] compared the oxygen radical oxidation and the conventional thermal oxidation at the same temperature (950°C) and concluded that the oxygen radical oxidation formed an atomically flat interface. According to this figure, an atomically flat interface was also formed even at 300°C.

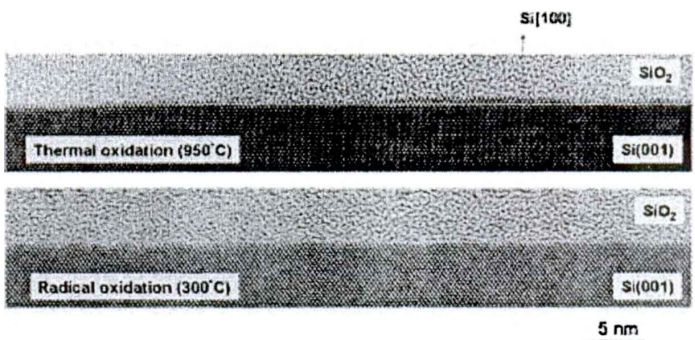


Fig. 8. HR-TEM pictures of SiO_2/Si interfaces formed by dry oxidation at 950°C (upper image), by radical oxidation at 300°C(lower image).

The characteristics of a TFT in which the gate insulator was formed by using VHF (40 MHz) PE-CVD at 300°C to grow SiO_2 on a microwave-plasma oxide were evaluated. SOI wafer was used as the substrate. The results are listed in Table 2.

The good mobility properties imply that the interface could be flat and have a low defect density.

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Table 2 TFT characteristics

	NMOS	PMOS
μ_{max} ($cm^2/V \cdot s$)	659	199
S (V/dec)	0.072	0.072

3. Extension to the microwave PE-CVD SiO_2 application

Thus far, the feature of surface-wave plasma oxidation was discussed. Microwave plasma was suitable for low-damage processing. The VHF PE-CVD layers of stacked structures should be replaced by microwave PE-CVD layer because there are many advantages to using microwave PE-CVD. The decomposition reaction of the source gas is more controllable because the discharge gas can be introduced separately from the source gas. And the substrate also can be separated from the plasma, which lessens ion damages to the surface. We modified the oxidation reactor, equipping it with two separated gas inlets. One was for discharge gas, the other was for source gas. Surface-wave plasma CVD was carried out with the modified reactor. Figure 9 shows the electron temperature and the electron density as functions of the applied microwave power. At powers greater

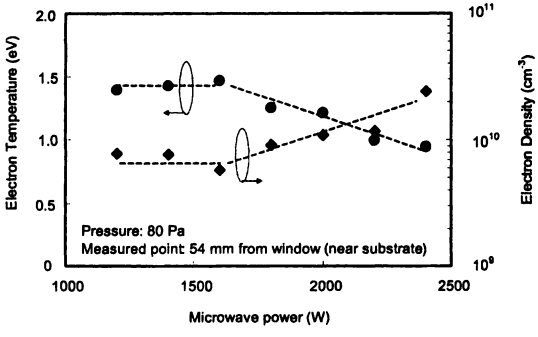


Fig. 9. The electron temperature and the electron density as functions of the applied microwave power.

than 1700 W, the electron temperature decreased and the electron density increased. The fixed charge density measured in the same microwave power region is plotted against microwave power in figure 10, which shows that the fixed charge density decreased monotonously as the microwave power increased. When the power was increased beyond

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1700 W, the electron temperature gradually decreased. This tendency is consistent with the data shown in Fig. 9, but the monotonous decrease of the fixed charge density at powers below 1700 W cannot be explained by the tendency of electron temperature in shown in Fig. 9. When the applied power is low, there might not be enough oxygen radicals for the three-dimensional SiO_2 networking reaction of TEOS intermediates.

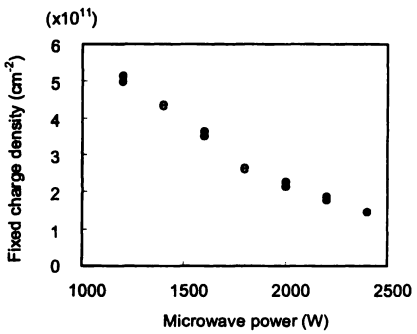


Fig. 10 Fixed charge density as a function of the applied microwave power.

CONCLUSIONS

Low-temperature surface-wave plasma oxidation was studied using microwaves. Surface-wave plasma is one of the most promising methods for radical oxidation. It reduces bulk plasma heating and lowers the electron temperature, which is suitable for a low-damage process for forming the gate insulator. The orientation of the substrate does not affect the oxidation rate, homogeneity, or the interface states density. An atomically flat SiO_2/Si interface was obtained by oxygen radical oxidation even at a process temperature of 300°C. According to the X-ray photoelectron spectroscopy studies, the SiO_2/Si interface was very steep, the structural transition layer was estimated to be about one-monolayer thick. O1s energy loss spectroscopy results indicate the effect of Kr dilution, which may connect to the moderate O_2^+ ion bombardment. Meanwhile, the Si-O bonding energy was 3.68 eV and the distribution of the O_2^+ ion energy larger than 4 eV could cause the damage onto the interface in the Kr dominant plasma conditions.

Microwave plasma CVD was also investigated using TEOS and O_2 mixtures. Fixed charge density could be lowered by controlling the electron temperature.

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ACKNOWLEDGEMENTS

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FABRICATION AND CHARACTERIZATION OF N- AND P- CHANNEL POLY-Si TFTS BY SPUTTERING OF ULTRA THIN GATE SiO_2 FILMS

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N- and p- channel polycrystalline silicon thin film transistors (poly-Si TFTs) with sputter-deposited ultra thin gate SiO_2 films have been fabricated and characterized. Measurements clarified that (1) thinning gate SiO_2 films suppresses punch-through effect and improves subthreshold properties for n- and p- channel poly-Si TFTs, (2) high speed operation of C-MOS poly-Si TFT ring-oscillators was confirmed, and (3) high reliability was confirmed compared with conventional thermal CVD oxide. Then, ultra thin gate SiO_2 film by sputter-deposition is very promising for future poly-Si TFTs.

INTRODUCTION

As the promising material for future displays, such as system on panel, low temperature polycrystalline silicon thin film transistors (poly-Si TFTs) have been widely studied. In order to improve the drivability of poly-Si TFTs, deposition of high quality thin gate oxide is one of the key issues (1,2,3). However, studies of poly-Si TFTs including C-MOS circuits have not been reported. In this study, we have fabricated the n- and p-channel poly-Si TFTs with ultra thin gate SiO_2 film down to 9 nm thick and characterized the poly-Si TFTs.

POLY-SI TFT FABRICATION AND GATE SiO_2 FILM DEPOSITION

Co-planar structure, n- and p- channel poly-Si TFTs and ring-oscillator circuits were fabricated by C-MOS poly-Si TFT fabrication process (4). Crystallized poly-Si film was prepared by solid phase annealing at 600℃ for 10 hrs. Thin gate SiO_2 films of 9.5 to 100 nm thickness were deposited by radio-frequency planar-magnetron sputtering at 200℃ substrate temperature. The target and sputtering gas used were high quality quartz (99.999%) and 30% oxygen-70% argon mixture. Hydrogenation was performed at 400 ℃ for 20 minutes in forming gases after aluminum metallization.

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RESULTS AND DISCUSSION

Figure 1 shows characteristics of drain current vs. gate voltage for 25 and 9.5 nm thick gates SiO_2 film, n- and p-channel poly-Si TFTs. The transfer curves were plotted for channel lengths of 3,7,10, and 20 μm. For gate SiO_2 film of 25 nm thick, both n- and p-channel poly-Si TFTs show that drain current increases with decreasing of channel length. However, punch-through effect clearly appears in poly-Si TFTs with short channel of 3 μm poly-Si TFTs, resulting in being unable to control the drain currents by gate voltage. The punch-through effect is suppressed by thinning gate SiO_2 film to 9.5 nm for both n- and p-channel poly-Si TFTs. Threshold voltage (Vt) of TFT with various gate oxide thicknesses was investigated as shown in Fig.2. Improvement of the Vt was clearly observed by decreasing gate oxide thickness for both n- and p-channel TFT.

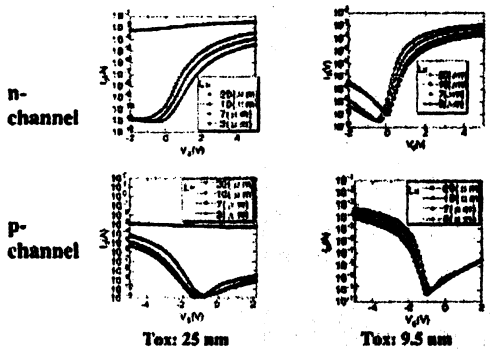


Fig.1: Characteristics of drain current vs. gate voltage characteristics for 25 and 9.5 nm gate SiO_2, n- and p channel poly-Si TFTs for various channel lengths.

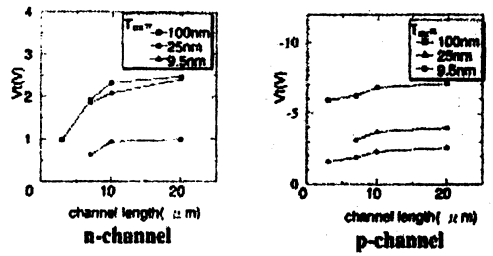


Fig.2: Changes of threshold voltage by channel length in n- and p channel poly-Si TFTs.

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Figure 3 shows dependences of subthreshold slope on channel length for 100, 25 and 9.5 nm thick gate SiO_2 films in n- and p- channel poly-Si TFTs. Subthreshold slopes are improved with decreasing channel length. Moreover, subthreshold slopes for 9.5 nm thick gates SiO_2 film are superior to those for 25 nm thick film in both n- and p- channel poly-Si TFTs. As shown in Figs.1, 2 and 3, subthreshold characteristics are improved remarkably by decreasing gate SiO_2 film thickness in addition to increasing of drain current.

Figure 4 shows output characteristics of drain current vs. drain voltage for 25 and 9.5 nm thick gate SiO_2 poly-Si TFTs with channel length of 3 and 7 μ m. The curves are

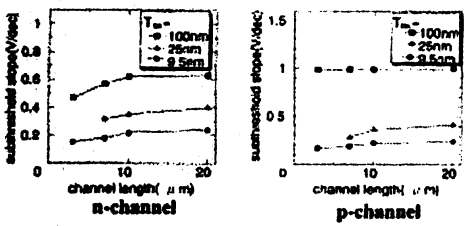


Fig.3: Changes of subthreshold slope by channel length in n- and p channel poly-Si TFTs.

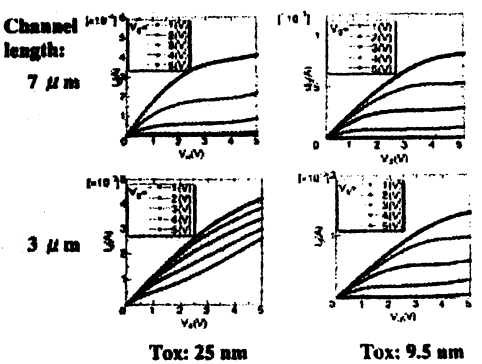


Fig.4: Characteristics of drain current vs. drain voltage for 25 and 9.5 nm gate SiO_2, n-channel poly-Si TFTs with 7 and 3 μ channel length.

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plotted as a parameter of gate voltage. For gate SiO_2 film of 25 nm thickness, the 3 μ m channel length poly-Si TFT indicates high current even at low gate voltage of 1 V due to punch-through effect. However, the punch-through effect is effectively suppressed by thinning gate SiO_2 film to 9.5 nm, resulting in ideal shapes as shown in Fig.4.

C-MOS ring-oscillator circuits consisted of poly-Si TFTs with thin gate SiO_2 were fabricated as shown in Fig.5. Figure 6 shows characteristics of the circuits for 25 and 9.5 nm thick gate SiO_2 films. Clear oscillations for both gate SiO_2 are observed at supply voltage as low as 5 V. Oscillation frequency for 9.5 nm thick gate SiO_2 film is as high as 3.5 MHz, which is higher than that for 25 nm thick film by about 1.5 times.

Photoemission from C-MOS ring-oscillator circuits during the real operation was observed for the first time using emission microscope as shown in Fig.7. Sensitivity range of the wavelength was from 400 to 1000nm. Clear emission was observed in all

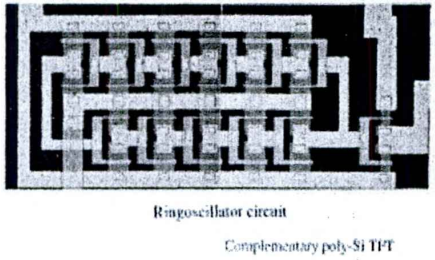


Fig.5: Photograph of C-MOS ring-oscillator circuit with 11 stages.

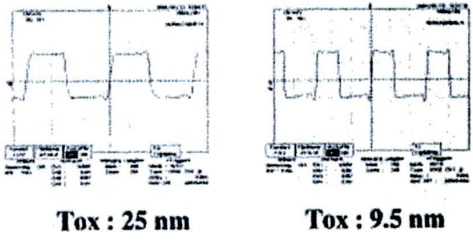


Fig.6: Characteristics of C-MOS ring-oscillators with 25 and 9.5 nm thick gate SiO_2 films.

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circuits with thin gate oxide down to 9.5nm. The observation indicated that all TFTs consisting ring oscillator actively and uniformly operated accompanied by the hot carrier generation.

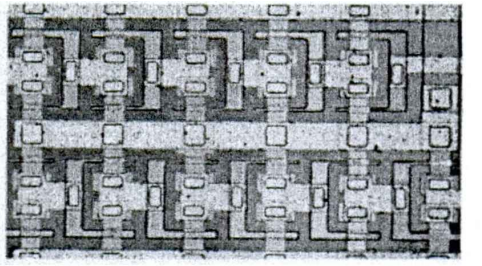


Fig.7: Photoemission from C-MOS ring-oscillator circuit with 9.5 nm gate SiO_2 film.

Finally we have evaluated the reliability of n-channel TFT with an oxide thickness of 100 nm against the DC stress. As the stress condition, stress gate voltage was fixed to threshold voltage and fixed 15V was applied to drain. Degradation of drain current and mobility was measured as shown in Fig.8. As the reference, TFT with thermal CVD gate oxide was compared. Much higher reliability was confirmed for the TFT with sputtered oxide, compared with thermal CVD oxide. Although hot carrier generation was clearly confirmed in Fig.7, it was confirmed that sputtered oxides receive very little damage.

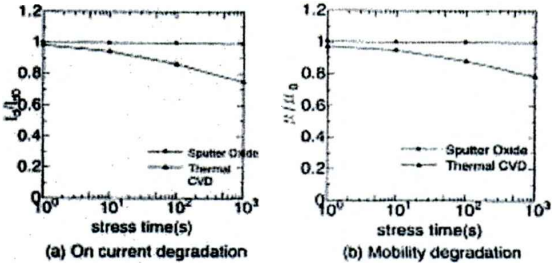


Fig.8: Degradations of drain current (a) and mobility (b) by DC stress for sputtered and thermal CVD SiO_2 poly-Si TFTs.

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As shown in Figs. 1, 4, and 6, gate voltages as high as 5V were successfully applied even for 9.5 nm thick gate SiO_2 film without suffering from breakdown failure. This indicates that sputtered SiO_2 films have excellent properties of breakdown electrical field higher than 5 MV/cm and low leakage current.

CONCLUSION

High performance n- and p-channel poly-Si TFTs were obtained using sputter-deposition of ultra thin gate SiO_2 films. Moreover, high frequency C-MOS ring oscillator circuits operation was confirmed. Also, superior properties of the SiO_2 film were achieved at low deposition temperature. Much higher reliability was confirmed for the poly-Si TFT with sputtered oxide, compared with thermal CVD oxide. Then, ultra thin gate SiO_2 films deposited by sputtering technique is very promising to fabricate poly-Si TFTs with high performance for the development of future displays.

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ION SHOWER DOPING OF POLYSILICON FILMS ON PLASTIC SUBSTRATES FOR FLEXIBLE TFT ARRAYS

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ABSTRACT

An ion shower doping technique was performed to form source-drain contacts for polysilicon TFTs on polyethersulfone (PES) substrates. The doped layer was subsequently annealed with an excimer laser to activate the dopant atoms electrically. The polysilicon films on the PES substrate showed much higher sheet resistance than those on a glass substrate when the two substrates were processed at the identical doping and activation conditions. Also, the plastic substrates heated up and caused film failure under prolonged exposure to the ion shower. The doping time and the resulting ion dose could be increased by reducing the RF power and allowing intervals for relaxation. A sheet resistance value as low as 300 ohms/sq. were obtained, which was low enough for a good ohmic contact.

INTRODUCTION

Thin Film Transistors (TFTs), having a poly-crystalline silicon film as a channel layer, are used for driving active matrix organic light-emitting display (AM-OLED) devices.(1,2) The AM-OLED is a good candidate for flexible displays due to its self-illuminating capability and very wide viewing angle.(3) Also, since both the driving electronics and the illuminating layers are integrated on a single substrate, the gap control is not necessary. Therefore, construction of poly-silicon TFTs on plastic substrates is a critical process to develop a flexible AM-OLED.

Performance of the TFT is greatly affected by the contact resistance at source-drain electrodes.(4) The silicon layer underneath the source-drain electrodes need to be doped heavily to ensure good ohmic contact characteristics. Sheet resistance values that are lower than 10^3 ohms/sq. are often desired. Also, the entire doping process must be completed at a temperature that is considerably lower than the glass transition temperature of the plastic substrate, so as not to damage the substrate.

Ion shower doping technique is widely used to control the contact resistance of the polysilicon TFTs because of its large area capability.(5) Unlike on glass substrates, ion shower doping on plastic substrates has certain technical limitations, such as poor activation efficiency and susceptibility to thermal damage.

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In this paper, ion shower doping was performed on polysilicon films on PES substrates to make source-drain contacts. Various process parameters that influence the ultimate sheet resistance of the polysilicon film were investigated, and a proper doping process was proposed to obtain sufficiently low resistance.

EXPERIMENTAL PROCEDURE

A thin (1000Å) layer of polycrystalline silicon was grown on polyethersulfone (PES) substrates by sputtering and was crystallized by an excimer laser annealing (ELA) technique. Phosphorus doping was performed to form source-drain contacts of a TFT, by using an ion shower doping system located at Seoul National University. Fig. 1 shows a schematic diagram of the ion shower system. Active dopant ion radicals were generated from a mixture of PH_3 and H_2 gas by a 13.56 MHz RF source. The radicals were then accelerated on to the substrate by a DC bias of 15 kV. The RF power and the doping time were varied to investigate the effect of bombarding ions on the plastic substrates.

The doped layer was subsequently annealed with an excimer laser to activate the dopant atoms electrically. The laser energy density and the number of laser shots were varied and their effects on the sheet resistance were studied.

RESULTS AND DISCUSSION

The polysilicon films on plastic substrates usually exhibited lower values of sheet resistance than those on glass substrates. Ion shower doping for 30 seconds on plastic substrates resulted in sheet resistance values that were much higher than 10^3 ohms/sq., while a sheet resistance of 400 ohms/sq. could be achieved on glass substrates.

We attempted a long term thermal annealing at a temperature of 180°C which is slightly lower than the glass transition temperature of the PES substrate. The change in the sheet resistance after thermal annealing is plotted in Fig. 2. As shown in the plot, the sheet resistance decreased with the annealing time up to 12 hours. This result implies that, in the polysilicon film deposited on plastic substrates, there exist certain micro-structural defects associated with the dopant atoms, which can be annealed out with relatively low activation energy.

Park *et al.* reported that the micro-structural damage in the polysilicon films on glass substrate, which was caused by ion implantation, was responsible for the increase in the sheet resistance at high ion dose.(6) The recovery of the structural damage is a much slower process than the dopant activation. Therefore, a sufficient thermal budget would be required for effective activation annealing. However, in this experiment, the polysilicon films on plastic substrates seemed to behave in a different manner from the foregoing argument.

We compared the degree of crystallinity by using a UV reflectance spectroscopy technique after the samples were annealed with an excimer laser for dopant activation. Fig. 3 shows the UV reflectance spectra for films doped with various ion dose. White circle, triangle, and square symbols stand for the UV reflectance spectra of the laser-activated films following ion shower doping for 3 minutes, 7 minutes, and 15 minutes,

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respectively. As a reference, a UV spectrum of a film that was doped but not activated was also included, and is represented by black square symbols.

For activated films, the spectra show characteristic peaks at the wavenumbers of approximately 280 nm and 370 nm. The peak intensity increases with increase in the doping time. However, no noticeable peaks appear for the un-activated film. The degree of crystallinity was estimated by integrating the area under the characteristic peaks and by comparing them with the peaks of a silicon wafer. The peak areas of the samples doped for 3 minutes, 7 minutes, and 15 minutes were calculated to be 54%, 73%, and 86%, respectively, of the single crystal silicon.

The laser energy density used for dopant activation was only 70% of what was used for initial crystallization of the as-deposited silicon films. The UV reflectance data show that the laser activation not only activated the dopant atoms but also lead to significant recrystallization of the amorphized film, even at this level of laser energy. This result suggests that the dopant ions may assist recrystallization and grain growth, and the slow damage recovery of the crystalline structure is not responsible for the relatively high sheet resistance on the plastic substrate. Although the acceleration voltage was the same as that used in Park *et al.*'s experiment, the polysilicon films on PES substrates are in the dose-controlled regime and not in the defect-controlled regime.(6) Therefore, the decrease in the sheet resistance after the long term annealing at 180°C is thought to be associated with some localized defects other than incomplete crystallization, or with local strain caused by the relatively high compliance of the plastic substrate.

Although the thermal annealing decreased the sheet resistance, the annealing time beyond 12 hours did not lead to a sufficiently low sheet resistance value to obtain good contact resistance. Also, such a long term annealing is not very practical in fabricating the TFT arrays for display devices. Therefore, a very high doping density is usually required, and consequently the doping time must be extended to obtain sufficiently low resistivity values. However, we found that, during the ion shower process, the plastic substrates often suffered structural damage. As shown in Fig. 4, the doped film blistered, cracked, and finally delaminated. This damage is believed to be due to the self-heating caused by the ion bombardment.

At an RF power of 150W which was a standard value for doping on glass substrates, the temperature of the film surface rose to a temperature that was as high as 210°C after 30 seconds from the onset of the ion shower. Ion shower doping was performed at a reduced RF power to verify that the film damage was a consequence of the ion bombardment. Fig. 5 shows the sheet resistance values at two different levels of RF power, 100W and 150W, respectively. Doping for 2 minutes at 100W resulted in the sheet resistance values comparable to those doped for 30 seconds at 150W. At the RF power of 100W, the substrate could last much longer inside the doping chamber than at 150W. After 2 minutes of doping, the temperature of the film surface increased only to 150°C. However, the doping time must be extended to obtain the equivalent sheet resistance at the reduced RF power.

From the above result, the RF power was set to 100W and the ion shower doping process was divided into cycles consisting of 1 minute doping and 2 minute relaxation. The doping time was controlled by repeating the cycles by required number of times. Fig.

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6 shows the sheet resistance values for 3 different values of the doping time. As the doping time increased, the average ion dose and the final sheet resistance decreased linearly. A sheet resistance that was as low as 300 ohms/sq. was accomplished. One thing to note is that, as the ion dose increased, the sheet resistance, R_S, changed linearly with a negative slope, and was not inversely proportional as expected by the relation:

$$R_S = \frac{1}{D_n q \mu}$$

where D_n is the ion dose, q is the electron charge, and μ is the electron mobility. In other words, the decrease in the sheet resistance is more pronounced than the increase in the number of ions incorporated. As discussed previously with the UV reflectance spectra, the relatively large grain size which appeared in the heavily doped samples might lower the overall resistivity,

SUMMARY

Ion shower doping for polysilicon TFTs was studied for the source-drain contact of TFTs on PES substrates. The polysilicon films on the PES substrate showed much higher sheet resistance. Thermal annealing at 180°C for an extended period up to 12 hours decreased the sheet resistance by a factor of 1/2 ~ 1/3, but was not sufficient to obtain what was required for a good source-drain contact. A relatively high ion dose was required for sheet resistance values below 10^3 ohms/sq., but, the plastic substrates heated up and caused film failure under prolonged exposure to the ion shower. The doping time and the resulting ion dose could be increased by reducing the RF power and allowing intervals for relaxation. A sheet resistance value as low as 300 ohms/sq. were obtained, which was low enough for a good ohmic contact. The higher the ion dose, the larger the grain size of the polysilicon film after activated and annealed by an excimer laser.

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ACKNOWLEDGEMENT

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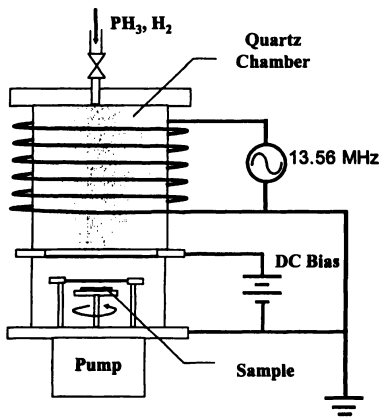


Fig. 1 Schematic diagram of the ion shower doping system

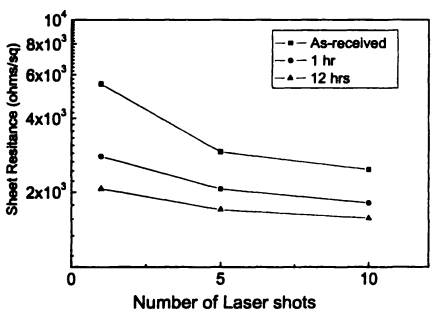


Fig. 2 Change in sheet resistance with additional thermal annealing at 180°C after the laser activation

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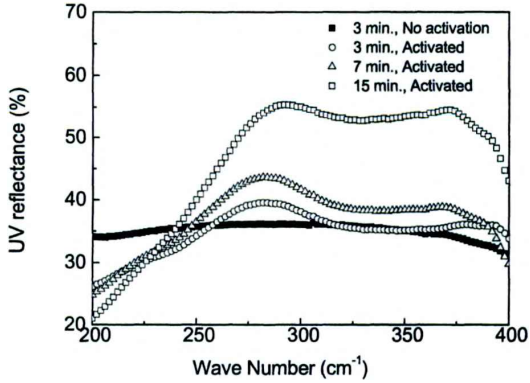


Fig. 3 UV reflectance spectra of the polysilicon films doped by ion shower and activated by subsequent excimer laser annealing. White circle, triangle, and square symbols stand for the laser-activated films following ion shower doping for 3 minutes, 7 minutes, and 15 minutes, respectively. Black square symbols are included as a reference and represent the film that was doped for 3 minutes, but not activated with a laser.

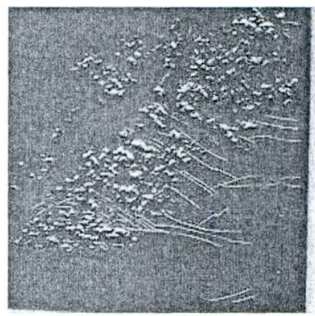


Fig. 4 Optical micrograph showing a polysilicon layer damaged during the ion shower doping.

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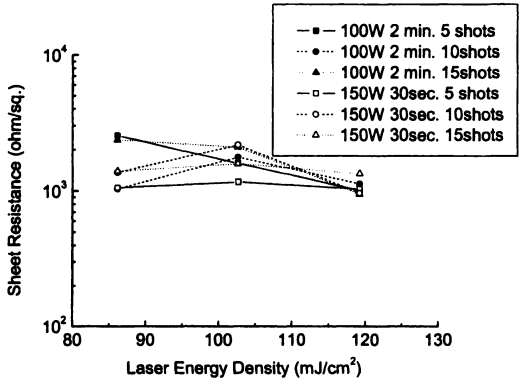


Fig. 5. Change in sheet resistance at two different levels of RF power for generating dopant ions.

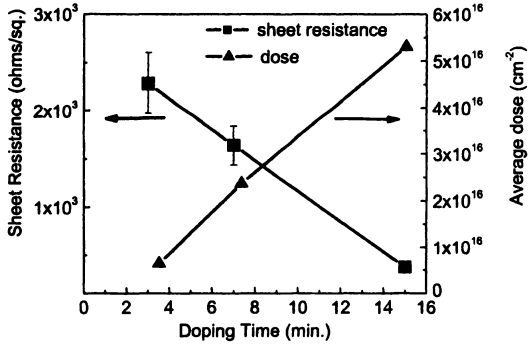


Fig. 6. Change in the sheet resistance and the average ion dose with increase in the doping time

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A SIMPLE CMOS SELF-ALIGNED DOUBLE-GATE POLY-SI TFT TECHNOLOGY

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In this paper, a new CMOS self-aligned double-gate thin-film transistor (SA-DG TFT) technology is proposed and demonstrated. The self-alignment between the top-gate and the bottom-gate is realized by a back-light exposure step. The structure has an ultra-thin channel region (300Å) and a thick source/drain region. Experimental results show that this technology provides excellent current saturation due to a combination of the effective reduction in the drain field and the fully-depletion of the ultra-thin channel. Moreover, for n-channel devices, the SADG TFT has 4.2 times higher on-current at high gate biases (V_{gs}=20 V). For p-channel devices, the SADG TFT has 3.6 times higher on-current at high gate biases (V_{gs}=-20 V).

INTRODUCTION

Poly-Si TFT technology is the most promising candidate for the ultimate goal of building fully-integrated flat panel display system on glass (SOG) [1]. It has been experimental demonstrated that double-gate structure is capable to provide a significant improvement in current drive, better saturation characteristics and a steeper subthreshold slope [2]. Thus, it is very attractive for both analog and digital applications. However, this structure is not a self-aligned structure. It results in significant performance variation and poor scalability. A few self-aligned double-gate TFTs have been demonstrated [3, 4], but all of them are complicated and require the use of critical process such as chemo-mechanically polishing (CMP).

In this paper, a simple CMOS self-aligned double-gate (SADG) poly-Si TFT technology is reported. Experimental results show that this technology provides excellent saturation characteristics, high current drive, and low leakage current. The device fabrication process is described, and the typical device characteristics are reported.

DEVICE FABRICATION

The self-aligned double-gate TFT devices were fabricated using a low temperature process (≤ 600 °C). Fig. 1 shows the schematic cross-sections of the major fabrication

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steps. Glass wafers with 3000Å low temperature oxide (LTO) were used as starting substrates. First, a 2000Å poly-Si film was deposited, implanted with phosphorus, and patterned using wet etch. Following this, a 1000Å LTO was deposited as gate oxide, and a 300Å a-Si was then deposited as the channel layer (Fig. 1(a)). After that a thick layer of LTO was deposited and coated with positive photo-resist. Back-light exposure was used to define the protected region, and the exposed LTO was removed (Fig. 1 (b)). This technique was used before to obtain self-aligned single gate ultra-thin channel TFT devices [5]. After that, a photolithography step was used to define the active area, and wet etch was used to remove the rest of the LTO and the ultra-thin a-Si layer. Following this, a 3000Å thick layer of a-Si was deposited as thick source/drain regions. After that, source/drain regions of the N- and P-channel devices were implanted with phosphorous and boron, respectively. A photolithography step was followed to define the active area. Then, the thick a-Si film was left behind (Fig. 1 (c)). Then the isolation LTO was removed, and a 1000Å LTO was deposited as top gate oxide. And a 3000Å a-Si film was deposited, implanted with phosphorus, and patterned as top gate (Fig. 1 (d)). After that a layer of 3500Å of LTO was deposited, and contact holes to the gate, source, and drain were defined. Metal Induced Lateral Crystallization (MILC) was used to recrystallize the a-Si film. The glass wafers were then sintered at 400 °C for 30 mins after metallization and patterning. For comparison, conventional self-aligned single-gate (SG) TFTs were also fabricated in the same run.

CHARACTERIZATION AND DISCUSSION

The measured I_d-V_d of the SADG TFT shows that the kink effect is suppressed significantly even at high drain bias (e.g. at V_{ds}=20 V), and good saturation characteristics are obtained. The good current saturation characteristics are attributed to a combination of the effective reduction in the drain field and the fully-depletion of the ultra-thin channel [5]. Fig. 2 shows the gate transfer characteristics of the SADG TFT and the conventional single gate TFT. The SADG TFT has much higher on-state current than that of the single gate TFT. For n-channel devices, the SADG TFT has 4.2 times higher on-current at high gate biases (V_{gs}=20 V). For p-channel devices, the SADG TFT has 3.6 times higher on-current at high gate biases (V_{gs}=-20 V). The higher than two times of on-current is due to the enhancement in mobility.

CONCLUSION

In summary, a novel self-aligned double-gate Poly-Si TFT was fabricated. The experimental results show that excellent current saturation characteristics, high current drive, and low off-current are obtained. The SADG TFT is very promising for fully-integrated flat panel display system on glass applications.

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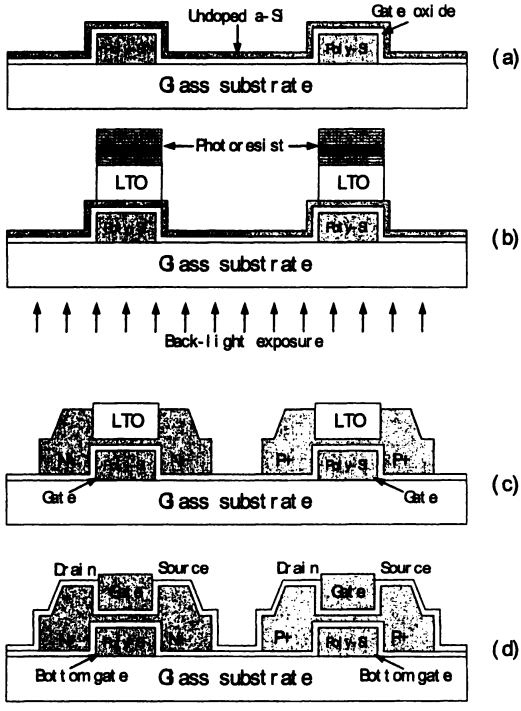


Fig. 1. Major fabrication steps of the SA-DG poly-Si TFT technology with complementary devices.
(a) Poly-gate, gate oxide, and a-Si deposition.
(b) Self-aligned of gate and active channel through back-light exposure.
(c) a-Si deposition, source/drain implants and definition.
(d) LTO remove, top gate oxide deposition, and top gate deposition and pattern.

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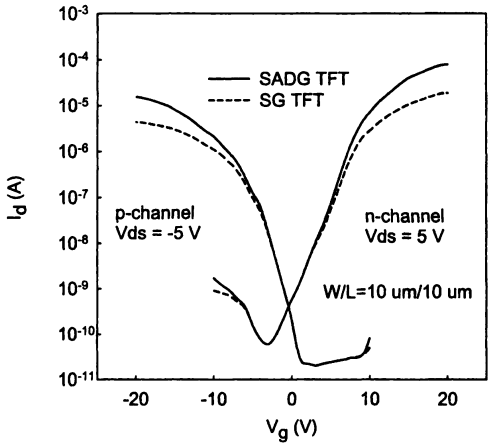


Fig. 2. Comparison of the I_d-V_g characteristics of the SA-DG TFT and conventional SG TFT.

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INFLUENCE OF CHANNEL POSITION ON CHARCATERISTICS OF P-CHANNEL c-Si TFT INISDE A LOCATION-CONTROLLED GRAIN

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ABSTRACT

To obtain a high performance of the p-channel single crystalline Si TFTs, a study of TFT's channel position inside a location-controlled grain was done. The location of grain is precisely controlled by μ-Czochralski process with excimer-laser. The subthreshold characteristics of p-channel c-Si TFTs was not change by avoiding the grain-filter. Nevertheless the field-effect hole mobility increases when the current flow direction aligns with the direction of radial grown defects from the grain-filter. The field-effect hole mobility of 250 cm^2/Vs and subthreshold slope of 0.16 V/dec. for the p-channel c-Si TFTs was obtained successfully.

INTRODUCTION

Excimer-laser crystallization of a-Si is an attractive technique for realizing the low temperature (<350 °C) poly-Si TFTs on glass (1). The field-effect electron mobility μ_{FEe} of the poly-Si TFTs fabricated by conventional excimer-laser crystallization is around 100 cm^2/Vs, which excludes the use of TFTs for other circuitries, such as DAC and pixel memory. The μ_{FEe} of poly-Si is lower than that of MOS transistor since the electrically active grain boundaries form the potential barrier that hinders the motion of carriers in poly-Si TFTs (2.3). TFTs fabricated inside a grain, i.e., single-crystalline Si (c-Si) TFTs will improve the poor characteristics (4). For producing the c-Si TFTs on glass, it is essential to control the position of large grain at desired position on substrate, i.e., 2D location control. Precise location-controlled grain allows us to eliminate the grain boundaries from active area of thin-film transistor. We have controlled the position of grain by modifying the substrate with conventional photolithography. The μ-Czochralski (grain-filter) process provides a precise way to control position of grain in excimer-laser crystallization (5). The n-channel c-Si TFTs fabricated inside a location-controlled grain by μ-Czochralski (grain-filter) process showed a field-effect electron mobility (μ_{FEe}) of ~ 600 cm^2/Vs on average (6). The rather high subthreshold slope S (0.45 V/dec.) was improved to 0.20 V/dec. by positioning the current flow direction parallel to the direction of radial defects, which are mainly coherent twin boundaries. P-channel c-Si TFTs fabricated by μ-Czochralski (grain-filter) process showed a field-effect hole mobility (μ_{FEh}) of ~ 250 cm^2/Vs and S of 0.29 V/dec. with the channel area on the top of the grain

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filter and gate SiO_2 thickness of 120 nm (7). This higher electrical performance of c-Si TFTs will allow us to integrate system circuits as well as driver circuits with display, i.e., system on glass.

In this article, first of all, effect of the position of p-channel c-Si TFTs inside a grain was investigated. The characteristics like n-channel c-Si TFTs inside the grain, might be limited by defects at /near the bottom of the grain filter. The location-controlled grain has planer defects inside, which are mainly coherent twin boundaries although they are radially distributed from the grain filter. It was suggested that in n-channel case the defects transversing to current flow direction impede ON-current (8). In this study, we have fabricated TFTs with and without the grain filter and with various current flow directions. Moreover, the effect of silicon thickness and vacuum annealing has been investigated.

EXPERIMENT

The TFTs used in this experiment were fabricated with μ-Czochralski process (5) with excimer-laser. The schematic diagram of c-Si TFT is shown in Fig. 1.

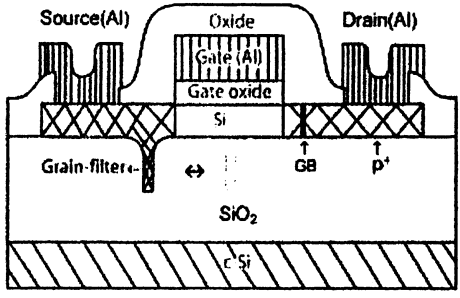


Figure 1. Cross-section of p-channel c-Si TFT

Thermally oxidized c-Si wafers were patterned into the grid of 0.75 μm deep cavity with the diameter of 1.0 μm by plasma etching. Subsequently, a silicon dioxide was deposited by plasma-enhanced chemical vapor deposition (PECVD) using tetraethylorthosilicate (TEOS) and oxygen at 350 °C. The diameter of the larger cavity was decreased to a final value of below 100nm. Next, 100 or 250 nm thick a-Si was deposited by LPCVD using silane at 545 °C. Subsequently, boron ions were implanted to control the threshold voltage. The samples having 250 nm a-Si, were crystallized with XeCl excimer-laser (λ = 308nm, pulse duration = 56ns) with various energy densities at an elevated temperature of 450 °C. The samples having 100 nm a-Si were crystallized with a longer pulse XeCl excimer-laser (9) (pulse duration = 200ns) with various energy densities at an elevated temperature 400 °C. In both cases samples are irradiated with one shot of excimer-laser. After the formation of location-controlled grain, oxygen plasma treatment was carried out to passivate the trap states. Subsequently, the crystallized Si film was patterned into

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islands by reactive ion etching. The channel of the transistor is designed such that channel position with respect to grain-filter, changes in different directions as shown in fig. 2.

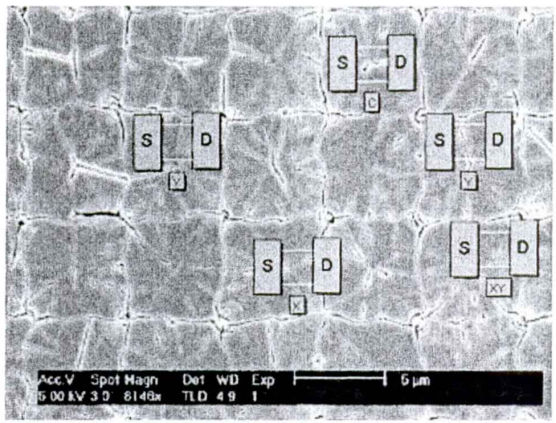


Figure 2. SEM image of the grid of grain fabricated by μ-Czochralski process.

Then, a 80 nm thick ECR-PECVD SiO_2 was deposited as a gate insulator at room temperature and annealed in water vapor at 333 °C. The gate electrode was then formed with sputtered Al at room temperature. The channel length and width, measured by SEM was 2.03 and 1.87 μm respectively. The source and drain were doped of boron by ion shower using Al gate pattern as a mask, and subsequently annealed at 300 °C for four hours in nitrogen ambient. Afterwards, passivation oxide, source and drain electrode were formed. No hydrogenation was carried out later.

RESULTS AND DISCUSSION

The position of TFT channel, was shifted in X, Y or the combination (XY) with respect to the center of the grain-filter (C), while the current flow direction was kept in the X direction. The amount of the channel shift with respect to the center of the grain filter is 1.5 μm. Figure 3 shows the transfer characteristics of the p-channel c-Si TFTs having 80 nm thick ECR-PECVD SiO_2 as a gate insulator fabricated with various channel positions. The energy density of the excimer-laser pulse was 1.025 J/cm^2. By shifting the channel position from the top of the grain-filter (C), there is no change in subthreshold characteristics. This suggests the fact that the defects near the bottom of the grain-filter do not affect the subthreshold characteristics, which is different than the n-channel counterparts. There is however improvement in the ON current by shifting to X direction. Table 1 shows μ_{FEh}, S value, off-current (I_{OFF}) and threshold voltage (V_{TH}) for c-Si TFTs. It is evident from table 1 that c-Si TFTs at the X position give the highest μ_{FEe}, since the carrier of motion is not impeded by the defects generated radially from the grain-filter

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(C).

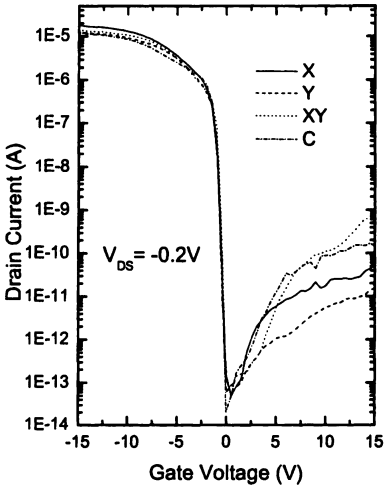


Figure 3. I_D –V_G characteristics of p-channel c-Si TFTs for the different position w.r.t grain filter

Table 1. Characteristics value of p-channel c-Si TFTs for different positions

Channel Position	Mobility (cm^2/Vs)	S (V/dec).	I_{OFF} (A) 1E-14	V_{th}(V)
X	250±21 (11%)	0.16± 0.04 (23%)	7.6 ± 2.8 (36%)	-2.7± 0.7(25%)
Y	197±12 (8%)	0.14±0.01 (7%)	5.6± 1.3 (22%)	-2.9±0.3 (15%)
XY	224± 21 (8%)	0.16± 0.0 34 (20%)	1.4± 5.7 (43%)	-2.9±0.5 (16%)
C	210±38 (7%)	0.15±0.04 (26%)	3.5±1.3 (37%)	-2.9±0.4 (15%)

Figure 4 shows the $\mu_{FEh,}$ as a function of energy density for the p-channel c-Si TFTs for different positions, it is quite clear that at moderate energy density, X shift c-Si TFTs gives highest $\mu_{FEh,}$ and that there is a slightly degradation in the μ_{FEh} for higher energy density, since higher energy density produces some planar defects in the silicon (6).

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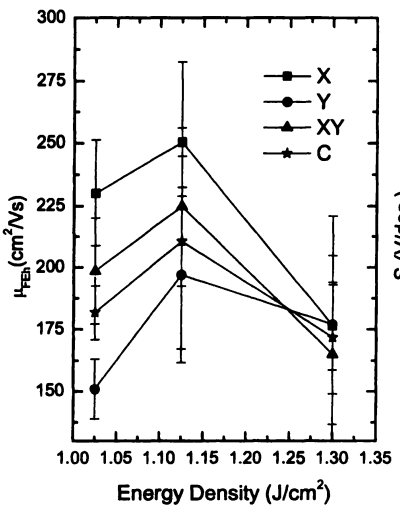


Figure 4. Variation of μ_{FEh} with crystallization energy density for various channel position w.r.t. grain-filter.

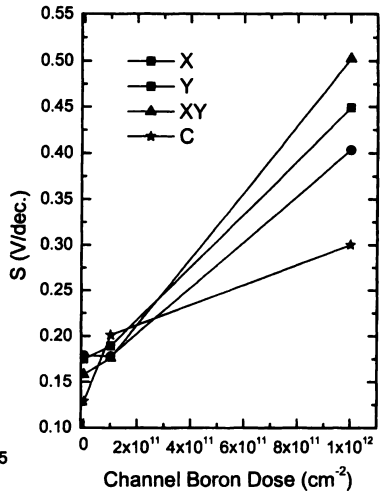


Figure 5. Variation of S with boron channel dose for various position w.r.t grain-filter.

Figure 5 shows the S as a function of boron channel doping for p-channel c-Si TFTs for various positions with respect to the grain-filter (C). As channel boron dose increases, the S value was degraded. The degradation of S is attributed to fact that some field lines originating from gate terminate at the acceptor ions and hence reduce the accumulated hole at the interface (10). Figure 6 shows the effect of silicon thickness on S and μ_{FEh} for p-channel c-Si TFTs. As silicon thickness decreases, S and μ_{FEh} both degrade. It is caused by more defects that are created during crystallization of the thinner silicon (11).

Annealing Effect

We performed a post vacuum annealing for one hour in N_2 ambient at 350 °C for the same p-channel c-Si TFTs. Figure 7 shows the effect of vacuum annealing on μ_{FEh}. It is evident that the μ_{FEh} improves after annealing. This would be attributed to the reduction of series resistance. Figure 8 shows the effects of annealing on S. there is slightly an improvement in subthreshold characteristics of p-channel c-Si TFTs. This suggests that the interface between Si and SiO_2 improves along with the bulk. The vacuum annealing helps to rearrange the weak bonds between Si and SiO_2.

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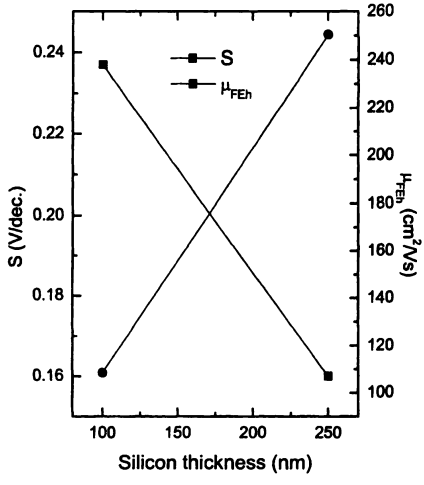


Figure 6. Effect of silicon thickness on the S and μ_{FEh}.

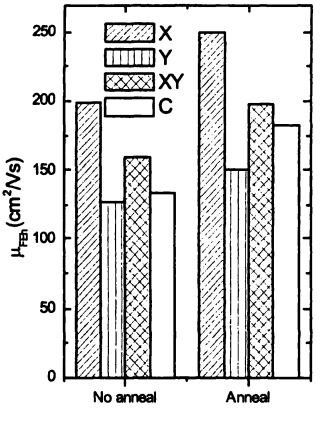


Figure 7. Effect of vacuum annealing on μ_{FEh}.

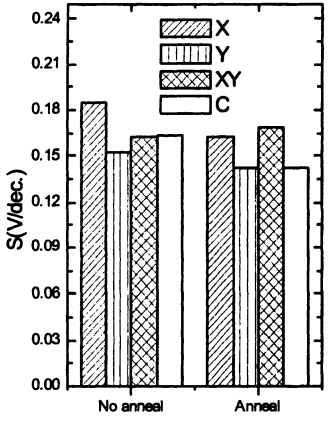


Figure 8. Effect of vacuum annealing on S

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CONCLUSION

Dependence of channel position inside a location-controlled grain on the p-channel c-Si TFT characteristics was investigated. By eliminating the grain-filter from the channel region, the μ_{FEh} improves especially with aligning the direction of carrier motion with the radially grown twin defects. However, there is no change in the subthreshold characteristics by the elimination of grain-filter. This suggests that in subthreshold region the carriers are not affected by the defects in the grain-filter. The c-Si TFT, shifted in the current flow direction with respect to the center of grain-filter gave the high mobility of 250 cm^2/Vs and subthreshold slope of 0.16V/dec. successfully. This high performance of p-channel TFTs suggests that the c-Si TFTs is attractive for an application to future system CMOS circuit integration in AMLCD and also 3D integration of ICs.

ACKNOWLEDGEMENT

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HIGH PERFORMANCE P-CHANNEL SCHOTTKY BARRIER THIN-FILM TRANSISTORS WITH PTSI SOURCE/DRAIN

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ABSTRACT

In this work, PtSi which has low valence-band barrier height is employed as the source/drain (S/D) material in p-channel Schottky barrier poly-Si thin-film transistors (SBTFTs) with field-induced drain (FID). This results in 5 times improvement in device's on-current as compared to the counterpart with $CoSi_2$ S/D. In the meantime, the inherent high off-state leakage current observed in conventional SBTFTs is successfully suppressed by the implementation of electrical junctions induced by a sub-gate, further improving the on/off current ratio.

INTRODUCTION

In our previous work, we have proposed and demonstrated a novel Schottky barrier (SB) poly-Si TFT with field-induced-drain (FID) extension (1)-(5). With proper sub-gate bias polarity, the transistor can be operated in ether n- or p-channel mode. In these studies, $CoSi_2$ was employed as the source/drain (S/D) of the fabricated devices that is capable of ambipolar operation since the $CoSi_2$ material possesses a near-mid-gap work function. However, the $CoSi_2$ S/D device also suffers from low current drive because of the large barrier height. To improve the device characteristics, low barrier silicide materials, such as PtSi for p-channel (6) and $ErSi_2$ for n-channel (7), is needed. In this work, we fabricated and characterized FID-SBTFTs featuring PtSi S/D. As compared with the $CoSi_2$ S/D counterpart, significant improvement in p-channel performance is achieved.

DEVICE STRUCTURE AND OPERATION

The cross-sectional view of a fabricated SB device with FID structure is shown in Fig. 1. X_D and X_S are drain and source offset, respectively. Figure 2 shows the detailed process flow. Briefly, after a 500nm substrate oxide was formed by thermal oxidation, a 50nm-thick amorphous silicon layer was deposited using low-pressure chemical vapor deposition (LPCVD), followed by a solid-phase crystallization (SPC) step to transform the layer into poly-Si. The SPC was performed at 600 °C in a furnace for 24 hours. After patterning of the channel islands, a 15nm LPCVD-TEOS was then deposited serving as the gate oxide, followed by the formation of n^+ poly-Si gate electrode. The sub-dielectric was subsequently deposited by LPCVD and patterned to define the source and drain offsets with lengths of X_S and X_D, respectively.

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Next, wafers receive either Pt or Co self-aligned silicidation (SALICIDE) treatment to form the metallic source/drain of the SB TFTs. Dual E-gun was used for Pt deposition, followed by furnace annealing to form the PtSi junctions. The formation of $CoSi_2$ could be found in our previous reports (1)(5). Finally, a 80nm passivation oxide was deposited by plasma enhanced CVD (PECVD), followed by aluminum deposition and metal pad formation. The sub-gate structure (metal field-plate) was formed simultaneously during the final step.

The unique sub-gate design allows ambipolar device operation to be realized in the fabricated devices. Electrical source/drain extensions could be induced in the channel offset regions underneath the channel offset regions by applying a high voltage on the sub-gate. Depending on the polarity of bias applied on the field-plate, the device could be set for either n- or p-channel operation.

RESULTS AND DISCUSSION

Figure 3 shows typical p-channel subthreshold characteristics for the devices with either $CoSi_2$ or PtSi S/D. It can be seen that the use of PtSi results in significant performance improvements including steeper subthreshold slope, larger on-current, and higher on/off current ratio. The increased on-current is ascribed to the lower barrier height for holes in p-channel operation, while the lower off-state leakage current is ascribed to a larger barrier height for the thermionic emission of electrons, which dominates the off-state conduction of the p-channel operation (3). Figures 4 and 5 show the output characteristics of devices with PtSi and $CoSi_2$ S/D, respectively. With the bias conditions at V_G= -5V and V_D= -2V, the on-current for the device with PtSi S/D is about 3uA, which is nearly five times larger than that with $CoSi_2$ S/D.

It should be noted that the improvement is not observed in n-channel operation. Actually, the performance of n-channel operation for the PtSi S/D device is worse as compared to that with $CoSi_2$ S/D, as shown in Figs. 6 and 7. This is not surprising since the barrier height for electrons in PtSi/Si junction is quite high (> 0.8 eV) which results in lower on-current in n-channel operation. In contrast to this, the device with $CoSi_2$ S/D exhibits nearly symmetrical ambipolar subthreshold characteristics, owing to the mid-band-gap work function of the $CoSi_2$/Si junctions.

Figure 8 shows the effects of the sub-gate bias and the length of the drain electrical junctions (X_D). A higher sub-gate bias can help reduce the parasitic resistance of the channel offset regions, and leads to a higher on-current. The impact is more significant for devices with $CoSi_2$ S/D. On the other hand, a increase in X_D decreases the on-current significantly. As can be seen in the figure that the benefit for using of PtSi as the S/D becomes non-significant when X_D is increased to 5 m.

CONCLUSIONS

FID-SBTFT devices with SPC poly-Si channel and PtSi S/D were fabricated and characterized. As compared with the counterpart with $CoSi_2$ S/D, the new PtSi S/D devices exhibit significant improvements in performance in case that the length of the electrical extensions is not long. These improvements are mainly ascribed to the low valence-band barrier height at the PtSi/Si junctions.

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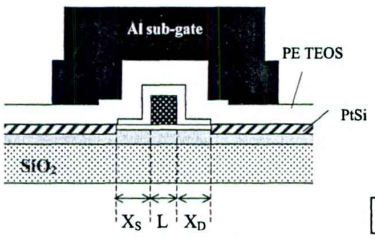


Fig.1 Cross-sectional view of FID-SBTFT.

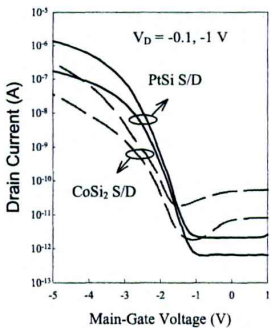


Fig.3 P-channel subthreshold characteristics of FID-SBTFT with $CoSi_2$ and PtSi S/D. (L/W = 0.8/20 μm/ μm, X_S=X_D = 0.2 μm, and sub-gate bias = 4.5 V.)

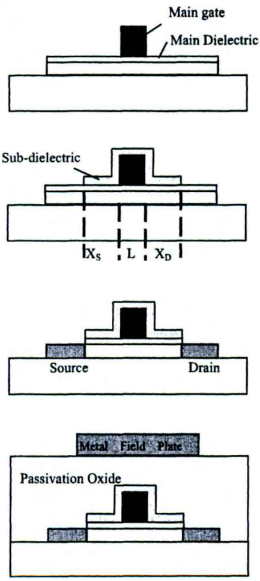


Fig.2 Detail Process flow of FID-SBTFT

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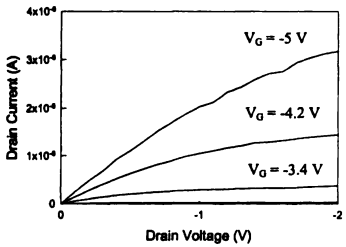


Fig.4 Output characteristics of FID-SBTFT with PtSi S/D. (L/W = 0.8/20 μm/ μm, X_S=X_D = 0.2 μm, and sub-gate bias = -4.5 V.)

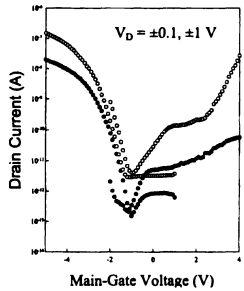


Fig.6 Ambipolar subthreshold characteristics of FID-SBTFT with PtSi S/D. (L/W = 5/20 μm/ μm, X_S= X_D = 1 μm, and sub-gate bias = ± 4.5 V.)

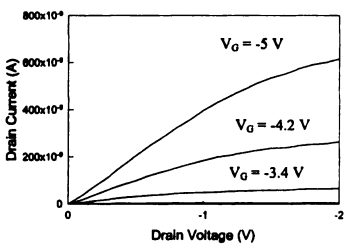


Fig.5 Output characteristics of FID-SBTFT with $CoSi_2$ S/D. (L/W = 0.8/20 μm/ μm, X_S=X_D = 0.2 μm, and sub-gate bias = -4.5 V.)

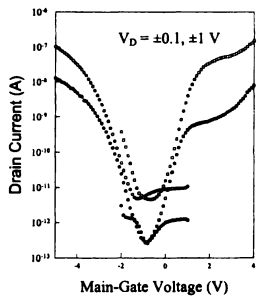


Fig.7 Ambipolar subthreshold characteristics of FID-SBTFT with $CoSi_2$ S/D. (L/W = 5/20 μm/ μm, X_S= X_D = 1 μm, sub-gate bias = ± 4.5 V.)

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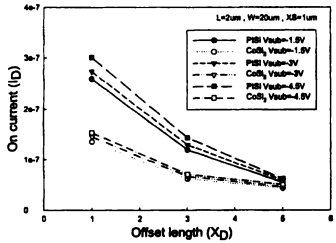


Fig.8 On-current versus offset length (X_D) with different sub-gate bias conditions. (L/W = 2/20 μm/ μm, X_S= 1 μm.)

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HOT-CARRIER INSTABILITY IN N- AND P-CHANNEL POLY-SI TFTS

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ABSTRACT

The degradation mechanism for low-temperature n- and p-channel poly-Si TFTs is discussed on the basis of both measured substrate and gate currents, and a power-time dependence law of threshold voltage shift. In n-channel TFTs, degradation under strong current saturation stress is ascribable to acceptor-type interface state generation at the poly-Si/gate oxide interface and in the grain boundaries near the drain. While under weak current saturation stress, the degradation increases with stress time, which is presumably due to acceptor-type interface state generation. In p-channel TFTs, degradation under strong saturation stress is dominantly due to trapping of hot-electrons injected into SiO2 near the drain giving rise to short-channel effect, whereas under weak saturation stress, the degradation is ascribable to trapping of hot-holes injected into SiO2 at the poly-Si/SiO2 interface in the entire channel region. The degradation increases for deeper stress gate voltage with stress time, which is presumably due to donor-type interface state generation.

INTRODUCTION

Low-temperature poly-Si thin-film transistors (TFTs) are of great interest regarding the integration of the circuitry in active-matrix liquid-crystal displays (AMLCDs), system on glass (SOG), and also driving circuitry in active-matrix organic light emitting displays (AM-OLED). However, from the viewpoint of realizing devices of high reliability, hot-carrier-induced degradation under stress voltage is an important issue. Although studies on hot-carrier degradation for low-temperature poly-Si TFTs have been reported (1), a systematic study of the hot-carrier instability in n- and p- channel poly-Si TFTs has not been reported (2-5). In this paper, we report the degradation of threshold voltage (Vt) and transconductance (Gm) of n- and p-channel TFTs under systematic stress bias condition and study the hot-carrier degradation mechanism by analyzing these device parameters.

EXPERIMENTAL

Low-temperature process of below 600℃ was used to fabricate n- and p-channel poly-Si TFTs. A-Si (amorphous-silicon) film was deposited using plasma-CVD on glass substrate and recrystallized by XeCl laser annealing. Poly-Si film thickness was 50nm and plasma-CVD gate oxide was 140nm thick. For n-channel devices, lightly doped n^- regions for LDD TFTs and heavily doped n^+ regions for single drain (SD) TFTs were self-aligned to metal gate electrode. For p-channel devices, heavily doped n+ regions

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were self-aligned to the metal gate electrode. Channel length and width of the devices (W/L) mainly used, were 9 μ m and 4.5 μ m, respectively.

Gate current (Ig), substrate current (Isub) and drain current (Id) were measured. Changes of threshold voltage (Vt) and transconductance (Gm) due to hot-carrier-induced degradation were systematically measured under strong current saturation stress condition and weak current saturation stress using HP4156B semiconductor parameter analyzer.

RESULTS AND DISCUSSION

GATE CURRENT AND SUBSTRATE CURRENT

Ig was measured using wide width device with L/W=4.5 μ m/300 μ m to detect the gate current. Isub and Id were measured for a four-terminal poly-Si TFT with substrate contact for device of W/L=9 μ m/4.5 μ m. Fig.1 shows Isub, Ig and Id divided channel width against effective gate voltage (Vg-Vtl) for n-channel poly-Si LDD TFTs, where Vtl (threshold voltage) is defined as an extrapolated gate voltage in linear region of Vg-Id curve. Vtls of these devices were 2.1V to 2.5V, respectively.

Bell-shaped substrate and gate current characteristics similar to those reported for bulk-Si n-channel MOSFETs can be observed (6). The current flow polarity indicates that Isub is hole current and the maximum was observed at a gate voltage of around Vg-Vtl=1V due to impact ionization in the high field region near the drain. Ig is thought to be electron current injected into gate oxide due to hot-carrier generated in the channel.

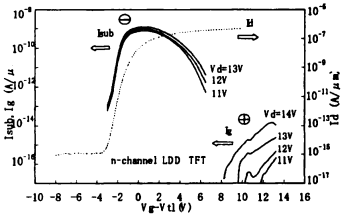


Fig.1. Vg-Vtl dependence of Isub, Ig and Id for n-channel LDD TFTs.

Fig. 2 shows Isub, Ig and Id divided channel width for p-channel TFTs as a function of gate voltage (Vg-Vtl). Devices whose feature size is similar to that in the n-channel device case are used to measure these currents. Vtls of these devices are around -3V.

Bell-shaped electron substrate current curves similar to the case of bulk-Si p-channel devices can also be observed (7). The maximum substrate current was observed at gate voltage of around Vg-Vtl=-1V due to impact ionization in the high field region near the drain. The maximum substrate current is two orders lower than that of n-channel devices due to the ionization rate of hole being lower than that of electron (6). Gate current in shallow gate voltage also exhibited bell-shaped curves and the maximum gate current was observed at a gate voltage of around Vg-Vtl=1V, which is considered to be due to the electrons injected into the gate oxide as a consequence of the drain avalanche

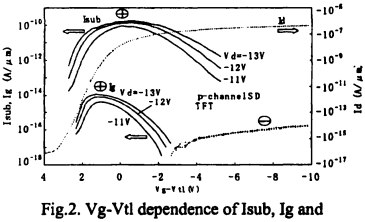


Fig.2. Vg-Vtl dependence of Isub, Ig and Id for p-channel TFTs.

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hot-carrier (DAHC) generation near the drain (7). For more negative gate voltage, opposite polarity gate current is observed, which is thought to be hole current injected into gate oxide due to high field normal to channel.

CHANGES OF DEVICE CHARACTERISTICS AFTER STRESS

In bulk-Si MOSFETs, Δ Vt or Δ Gm has been found to follow a power-time dependent law as follows:

$$\Delta Vt \text{ (or } \Delta Gm) = At^n \qquad [1]$$

where exponent n=0.2-0.7 and A is a constant related fabrication process parameter. It has been shown that the exponent n of 0.2-0.3 is due to carrier trapping in the gate oxide. The exponent n of 0.4-0.7 corresponds to interface state generation at the gate oxide/Si interface, which is related to the trapping of holes followed by electron capture induced by drain avalanche hot-carrier injection into the gate oxide (6,8). In poly-Si TFTs, it has been supposed that the degradation of field effect mobility depends on the interface state generation at the gate oxide/Si interface and band-tail state generation in the grain boundaries near the drain (1).

In our hot-carrier-degradation experiment, threshold voltage (Vt) is defined as a deeper gate voltage at which |Id| is 1.8μA at |Vd|=0.1V (0.2μA/μm of channel width) for n- and p-channel devices. In this bias condition, the band bend is deeper and threshold voltage shifts after stress (ΔVt) would be affected by both the trapped charge and generated interface state charge if these charges were created (6,8). ΔVt against stress time was measured for varying stress gate voltage Vsg at fixed stress drain voltage of |Vsd|=12V. ΔVt is defined as follows:

$$\Delta Vt = (Vta - Vti) \qquad [2]$$

where Vta and Vti are after stress and initial Vt, respectively.

N-CHANNEL TFTS. Fig.4(a) shows ΔVt under strong saturation stress as a parameter of Vsg for n-channel LDD and SD TFTs. It is found from this figure that ΔVt is 120mV and ~8V for LDD and SD TFTs after stress time of 100sec under the stress of Vsg=3V, respectively. It can be observed that the power-time dependence of Vt degradation is of the form At^n. The exponent n takes values of 0.4-0.5 for various Vsg in n-channel TFTs in the shorter stage of stress time. The degradation has a tendency to saturate with the increase of stress time as observed ΔGmmax (3). This is because the ΔVt and ΔGmmax at a stress time are almost linearly related to each other. This result plotted in

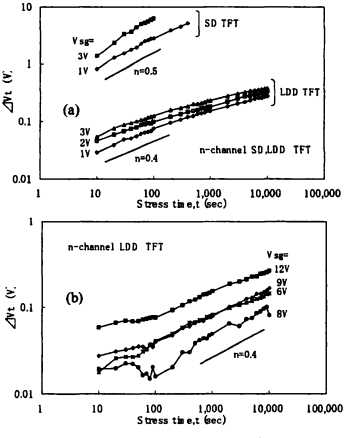


Fig.4. Stress time dependence of ΔVt for n-channel TFTs. (a) strong, and (b) weak saturation stress.

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Fig.4 (a) indicates that the degradation in the case of the shorter stage is caused by negative charges induced by hot-carrier stress, which are possibly due to the interface state generation at the gate oxide/poly-Si interface and in the grain boundaries in poly-Si near the drain. Saturation mechanisms in Gm (and Vt) with the stress time have been reported for bulk-Si devices (8). It is supposed that the saturation of ΔGmmax is due to the combination of an increase in barrier height, an increase in drain-side parasitic series resistance, and a reduction in carrier mobility induced by Coulomb scattering owing to the negative charges generated near the drain. The effect of parasitic resistance could depend on the donor concentration at the drain-side, affecting the parasitic series resistance of LDD TFTs even more.

Fig. 4(b) shows ΔVt under weak saturation stress for LDD TFTs. ΔVt tends to saturate in shorter stress time of 100sec and to increase after the stress of 100sec, showing n-value of 0.4 indicating two-step degradation. The increase of ΔVt after long stress time is observed in SOI MOS (9) and bulk MOS devices (10). The mechanism of Vt change in short stress time is due to the electron trapping injected into gate oxide because of gate electron current dominantly observed (Fig.1). With the increase of the number of trapped electrons, potential barrier for electron increases, resulting in the saturation of ΔVt. In the longer stress time, as the potential barrier for holes decreases, holes are also injected. It is supposed that n-value of 0.4 under this stress condition is due to the generation of interface state at the interface and in the grain boundaries in whole channel region.

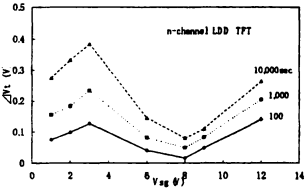


Fig.5.Stress gate voltage Vsg dependence of Δ Vt for n-channelLDD TFTs.

Fig. 5 shows ΔVt as a function of Vsg for n-channel LDD TFTs after stress time of 100, 1,000 and 10,000 sec. It is noticed that, under the strong current saturation stress, Δ Vt shows a maximum at around Vsg=3V corresponding to the low gate voltage of Vg-Vtl=1V showing the largest substrate current (Fig.1), whereas under weak current saturation stress, Δ Vt increases with the increase of Vsg for deeper Vsg of Vsg$\geqq$10V.

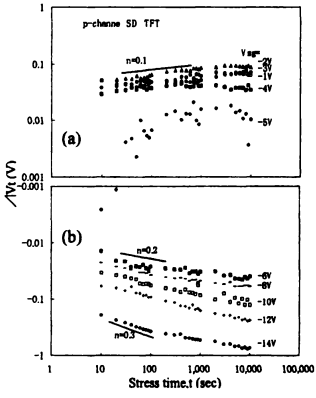


Fig.6. Stress time dependence of Δ Vt for p-channel TFTs. (a) strong, and (b) weak saturation stress.

P-CHANNEL TFTS. Figs. 6 (a) and (b) show the Δ Vt against stress time under the strong current saturation (-1$\geqq$Vsg$\geqq$-5V) and weak current saturation stress condition (-6V$\geqq$Vsg $\geqq$ -14V), respectively, varying stress gate voltage Vsg at fixed stress drain voltage of Vsd=-12V. It is observed that the threshold voltage shifted to positive direction under the strong saturation stress (Fig. 6(a)), where Gm enhancement was observed. On the other

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hand, under the weak saturation stress (Fig. 6(b)), threshold voltage shifted to negative direction corresponding to the decrease of Gm. Vt shifts to positive direction and the exponent n takes values of around n=0.1 under the strong saturation stress in the shorter stage of stress time. These results indicate that the degradation is caused dominantly by the generation of negative charges near the drain region induced by hot-carrier stress, which are possibly due to electron trapping at the gate oxide/poly-Si interface and in the grain boundaries in poly-Si caused by the generated hot electrons near the drain. Consequently, the effective channel length is shortened, thereby giving rise to Gm enhancement as reported in the case of bulk-Si p-channel MOS FETs (7). The degradation has a tendency to saturate with the increase of stress time. On the other hand, in the case of weak saturation stress of $-6 \geqq Vsg \geqq -8V$, Vt changes to negative direction and the exponent n shows the values of around n=0.2 in the shorter stage of stress time. Vt changes are caused by positive charge generation at the interface in channel region from source to drain. The degradation in this case is presumably due to the trapped holes injected into the gate oxide owing to the high field in the channel normal to the interface as is observed in Fig.2. For deeper Vsg such as −10V and −14V, n-value tends to increase to n=0.3 or more. This result for deeper Vsg suggests that hot holes are trapped and also the interface states with positive charges (donor-type interface states) are generated at the interface and in the grain boundaries in poly-Si near the interface.

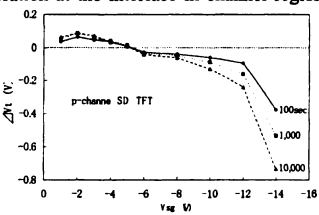


Fig.7.Stress gate voltage Vsg dependence of Δ Vt for p-channel TFTs.

Fig.7 shows Δ Vt as a function of stress gate voltage for stress times of 100, 1,000, and 10,000 sec. It is noticed that, under the strong saturation stress, Δ Vt shows the maximum at around Vsg=-2V corresponding to the low gate voltage of Vg-Vtl=1V (Vtl=-3V) showing the largest gate current (Fig.2) and tends to saturate in the case of the longer stress time, whereas under weak current saturation stress, $|\Delta Vt|$ continues to increase with the increase of stress time, such increase being especially marked for deeper Vsg such as -10V∼-14V.

DEGRADED REGION IN THE CHANNEL AFTER STRESS

In order to investigate the hot-carrier-degraded region in n- and p-channel TFTs, changes of both forward and reverse mode drain current (Δ Id) were measured at various drain voltages (Vd). Reverse mode drain currents are those when source and drain terminals were interchanged. Δ Id (%) is defined as follows:

$$\Delta Id(\%) = ((Id(i)-Id(10,000))/Id(i)) \times 100 \quad [3]$$

where Id(i) and Id(10,000) are drain current for initial and after stress of 10,000sec at measured gate voltage of $|Vg|=6V$, respectively. Fig.8 shows the Δ Id against measured Vd as a parameter of stress gate voltage Vsg for n-channel device. Solid and dotted lines are forward and reverse mode Δ Id, respectively. Δ Id shows positive values resulting in negative charge generation at SiO2/poly-Si interface or in the grain boundaries in poly-Si. In strong saturation stress (Vsg=1, 2, 3V), forward mode Δ Id markedly decreased with

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the increase of Vd in the range of 0.25V to 6V. This implies that the hot-carrier-degraded region is localized near the drain edge, since the degraded region near the drain is shielded by drain depletion layer extended from the drain edge. The increase of Δ Id in deep Vd region (Vd > 6V) is thought to be due to the suppression of kink current after stress. While, in weak saturation stress (Vsg ≧ 8V), the difference of Δ Id between the forward and reverse modes was small compared with that in strong saturation stress. This suggests that, in the weak saturation stress, the degraded region due to generated negative charges is distributed in a wide range from drain and source.

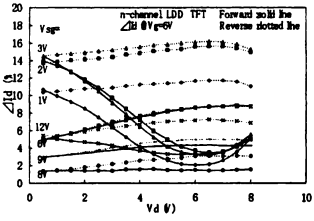


Fig.8. Measured Vd dependence of Drain current change Δ Id for n-channel LDD TFT.

Fig.9 shows Δ Id as a function of Vd for p-channel device. In strong saturation stress (Vsg=-2,-4V), both forward and reverse mode Δ Id are negative, indicating electron trapping near the drain. The decrease of | Δ Id| in deep Vd region (Vd < -6V) is due to the suppression of kink current after stress. While, in weak current saturation stress (Vsg=-8V,-10V,-12V), Δ Id was positive and the difference of Δ Id was small between forward and reverse modes. These results indicate that positive charges are generated at the interface in whole channel region [8].

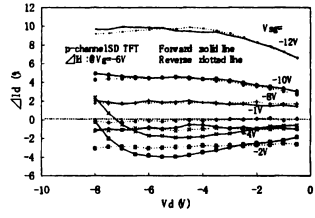


Fig. 9. Measured Vd dependence of drain current change Δ Id for p-channel TFT.

NUMERICAL SIMULATION OF FIELD IN THE CHANNEL

In order to investigate lateral and vertical field distribution in the channel, 2-D numerical simulations using the ATLAS device simulation software were performed. A density of states (DOS) in poly-Si, which is mainly located at the grain boundaries, has been modeled by a spatially homogeneous density of states (four exponential tails, two of which are located in the upper half of band gap (acceptor-like) and two in the lower half of band gap (donor-like)(11). Lateral doping profile near the drain edge greatly influences the field distribution near drain (12). Ion-implanted lateral and vertical impurity profiles in source and drain regions were simulated by using 2-D process simulation, and the lateral impurity profiles in poly-Si were fitted to Gaussian doping profile by choosing the lateral spread defined as the standard deviation of the Gaussian for ATLAS device simulation software. Activation rate of implanted impurities used was 30%.

Fig. 10 shows simulated lateral and vertical field distribution at the gate oxide/poly-Si interface along the channel of n-channel LDD TFT for various gate voltages at Vd=12V. It can be seen that the maximum lateral field along the channel is located near the edge of n^- LDD region under gate oxide, where the hot-carrier-degradation due to DAHC is supposed to occur at this region.

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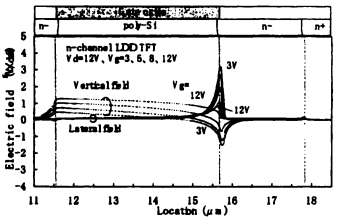


Fig.10. Simulated field distribution along the channel for n-channel TFT.

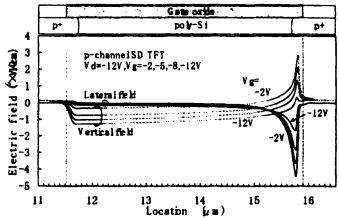


Fig.11. Simulated field distribution along the channel for p-channel TFT.

Fig. 11 shows the field distribution at the gate oxide/poly-Si interface in the case of p-channel TFTs at Vd=-12V. For drain current saturation bias (Vg≧-5V)the maximum lateral high field locates near the drain junction, whereas, for weak saturation bias (Vg ≦-8V), vertical field normal to channel is distributed in almost the entire channel region, which is thought to cause the hole gate current.

SUMMARY

Hot-carrier degradation in low-temperature n- and p- channel poly-Si TFTs has been studied under the stress of strong and weak drain current saturation region on the basis of both substrate and gate currents, and a power-time dependence law.

1. In n-channel TFTs, under strong saturation stress, the degradation is worst at the gate voltage corresponding to the largest substrate hole current caused by DAHC. ΔVt in short stress time has exhibited a power-time dependence with an exponent n of 0.4～0.5, which could be due to the acceptor-type interface state generation at poly-Si/gate oxide interface and in the grain boundaries in high field region near the drain. It is supposed that saturation of ΔVt with the increase of stress time is due to the combination of an increase in barrier height, an increase in series resistance and a reduction in carrier mobility owing to the state generation near the drain.

   Whereas, under weak saturation stress, ΔVt tends to saturate in shorter stress time and to increase after the longer stress with the n-value of 0.4, showing tow-step degradation. Vt change in short stress time is due to the electron trapping injected into gate oxide. As a number of trapped electrons increases, potential barrier for electron increases resulting the saturation of ΔVt. In the longer stress time as the potential barrier for holes decreases, holes are also injected. It is supposed that the n-value of 0.4 under this stress condition is thought to be due to the generation of acceptor-type interface states at the interface and in the grain boundaries. Degradation will occur in wide range from drain and source edges.
2. In p-channel TFTs, under strong saturation stress, Vt changes to positive direction, and ΔVt peaks at the gate voltage corresponding to the largest gate current and tends to saturate with the stress time. The degradation of threshold voltage is dominantly due to the trapping of generated hot electrons caused by DAHC near the drain at the gate oxide/poly-Si interface and in the grain boundaries, giving rise to

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short-channel effect.

On the other hand, under the weak current saturation stress, Vt shifts to negative direction possibly due to trapping of holes at the interface caused by high field normal to interface in the channel. For deeper stress gate voltage, n-value increases to 0.3 or more, which is presumably due to the trapping of channel hot-holes (CHH) and also the generation of donor-type interface states at the interface and in the grain boundaries in the whole channel region from source to drain. $|\Delta Vt|$ continues to increase with the stress time under this stress condition. As a result, in the case of longer term stress, the degradation in weak saturation stress could be more serious than that in the case of strong saturation stress.

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SWITCH-ON UNDERSHOOT CURRENT OBSERVED IN THIN FILM TRANSISTORS

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The transient drain current of the single grain silicon TFTs with ECR-PECVD gate oxide has been measured by applying a square signal on the gate and a constant low voltage between source and drain. Switch-on undershoot current has been observed, which can be attributed to the motion of space charge in gate oxide. Assuming there are some mobile ions in the gate oxide, we find the drift kinetics of the ions is quite similar to the mobile protons in SiO_2, as reported in the literature.

INTRODUCTION

The technology of low-temperature polycrystalline Silicon Thin Film Transistors (poly-Si TFT), fabricated by excimer laser recrystallization on a glass or plastic substrate, is being pursued to achieve the so-called system-on-panel (1,2). A new development in TFT technology is the fabrication of location controlled Single Grain Silicon TFTs (SG-TFT) by the method referred to as Micro-Czochralski or grain filter process (3-5). Much higher electron mobilities than for standard laser-crystallized poly-Si TFT are obtained with SG-TFTs (450 cm^2/Vs). By exploiting the capability of this technology to take on many functions traditionally reserved for single-crystal devices, it is expected that a complete computer system will be fabricated on glass or plastic substrate. In view of these applications, characterization of the transient behaviour of SG-TFTs is of paramount importance for the optimum design of electronic circuits.

To improve the performance of the SG-TFTs, two different fabrication processes for the gate oxide have been used, i.e. Low-pressure Chemical Vapour Deposition (LPCVD) and Electron Cyclotron Resonance Plasma Enhanced Chemical Vapour Deposition (ECR-PECVD). We found that the devices with ECR-PECVD oxide have better Si/SiO_2 interface and higher field effect mobility (5). The transient properties of these devices have been studied carefully. We have reported before that SG-TFT with LPCVD oxide exhibit a switch-on overshoot that is the transient drain current after switch-on higher than the static value. The effect has been attributed to trapping in the bulk or in the interface (6-8). By contrast in devices with ECR-PECVD oxide, a different transient effect has been observed. The transient drain current after switch-on is lower than the static value. We refer to this effect as "undershoot". The purpose of this work is to understand the physical origin of the "undershoot".

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EXPERIMENTAL

The n-channel SG-TFTs were fabricated inside location-controlled grains by the Micro-Czochralski process (3). After formation of the location controlled grains, the Si film was patterned into islands by dry etching. A 137nm thick SiO_2 film was deposited by the ECR-PECVD at room temperature to serve as the gate dielectric. Microwaves with a frequency of 2.45GHz, parallel to the magnetic field lines, were introduced to the chamber via a quartz window. SiH_4 and O_2 were used as source gasses and the pressure was kept at 1 mTorr. The SiO_2 was successively annealed at 333°C in H_2O/N_2 ambient. The gate electrode was Al. The channel length and width were measured to be 3.21 μm and 2.88 μm, respectively. Control devices with ECR-PECVD gate oxide were fabricated on undoped {100} oriented Silicon-on-Insulator (SOI) with the rest of the process being identical to that of the SG-TFTs.

The transient measurement setup has been reported before (6,7). As shown in fig.1, a train of pulses was applied to the gate by an Agilent 33250A waveform generator. The source was grounded and a constant voltage (V_{DS}=0.1V) was applied to the drain by a Keithley 230 voltage source. The transient current was amplified by a Keithley 428 current voltage converter and detected by a LC584AL digital oscilloscope. The output signal was averaged over 1000 periods to reduce the noise. The pulse rise time was set to 20ns, chosen to be comparable with those typically used in TFT digital circuitry. All of the measurements were controlled through Labview. The transient measurements were carried out on SG-TFTs with a typical field effect mobility of 400cm^2/Vs A square waveform ($V_{GS\text{-}max}$ $-V_{off}$) was applied to the gate. V_{off} = 0 and $V_{GS\text{-}max}$ was varied between 1.5V and 9.0V. The on time and off time were 0.5s.

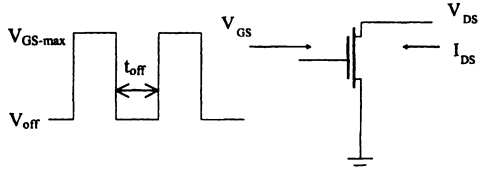


Fig.1 , Waveform used in the transient measurements.

RESULTS AND DISCUSSIONS

As shown in fig.2, the drain current after switch-on increases with time until it reaches the static value (undershoot). The transient current can be fitted to the following expressions.

$$I_{DS}(t) = I_{static} - \Delta I_1 \exp(-t/\tau_1) - \Delta I_2 \exp(-t/\tau_2) \qquad [1]$$

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where, I_{static} is the static value, ΔI_1 and ΔI_2 are the undershoot values for the two relaxation times τ_1 and τ_2. τ_1 corresponds to the faster relaxation process, which is tens of milliseconds long and τ_2 corresponds to a slower process lasting hundreds of milliseconds. Fig.3 shows the undershoot current measured at V_{GS}=8.5V fitted to the equation above. Fig.4 shows that the relaxation time τ_2 decreases with the increase of $V_{GS\text{-}max}$.

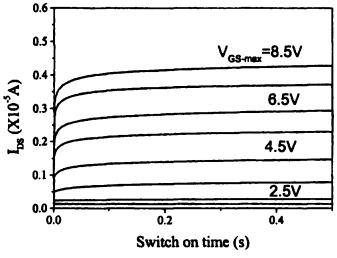


Fig.2 Undershoot current observed in a 3.2μm×2.9μm n-channel SG-TFT. V_{DS}=0.1V. From top to bottom, $V_{GS\text{-}max}$ varies from 8.5V to 1.5V. V_{off}=0V.

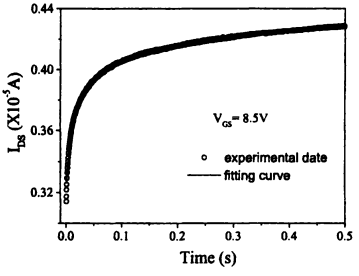


Fig.3 Fitting of the undershoot current to equ. [1]- (see text).

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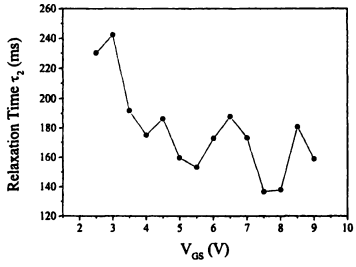


Fig.4 The relaxation time τ_2 (see taxt) as a function of $V_{GS\text{-}max}$.

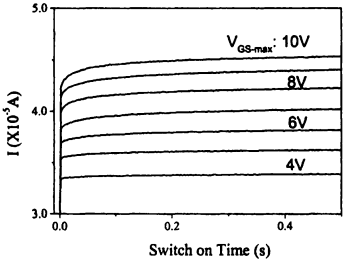


Fig.5, Undershoot current observed in a 1.8μm×2.0μm n-channel SOI MOSFET. V_{DS}=0.1V, V_{off} =3V.

As shown in fig.5, the undershoot current of SOI TFTs exhibit a similar relaxation time constant τ_2 of about 300 ms. This is a strong indication that the undershoot is due to the ECR-PECVD gate oxide.

The undershoot implies that the number of electrons in the channel increases with time after switch-on. If we assume that there are mobile space charges in the gate oxide, the effect on the channel electron density is described by the equ. 2:

$$V_{GS} = \frac{1}{\varepsilon_r \varepsilon_0}\{Q_c|d - |Q_+|c_+ + |Q_-|c_-\} + \Psi_s \qquad [2]$$

where, ε_r is the relative dielectric constant of the gate oxide, Q_c is the channel charge density per unit area, Q_+ and Q. are the positive and negative charge density per unit area in the oxide film, c_+ and c. are the distances of the centroids of positive and negative

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charge from the metal gate/insulator interface, d is the thickness of the gate oxide and ψ_s is the surface potential. Equ.2 indicates that the change of space charge density or the motion of space charge in the oxide can influence the electron density in the channel. The first case corresponds to space charge injection from the gate metal or the channel. The second case can be regarded as dielectric relaxation of the oxide film. In the case of space charge injection, two types of processes may occur with positive V_{GS}: electron injection from the channel, which would result in a lower channel electron density and hole injection from the gate metal that would give rise to higher channel electron density and consequently higher drain current. Hence the undershoot could be due to hole injection from the gate. But hole injection from the metal gate due to Schottky emission or Poole-Frenkel emission is expected to yield a nonlinear relationship between the injection current and the applied electric field. By contrast, as shown in Fig.6, the undershoot value depends linearly on the applied gate voltage. We consider next the motion of space charge in the oxide. When a positive gate voltage is applied, positive charges move away from the gate and/or negative charges move toward gate, therefore c_+ increases and/or c_- decreases. According to equ.2 this results in an increase of electron density in the channel and the undershoot.

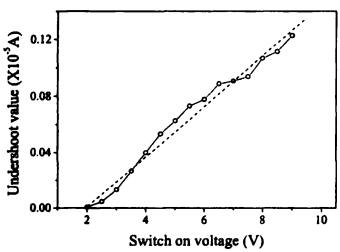


Fig.6, The overshoot value $|I_{DS}(t=20ns) - I_{DS}(t=0.5s)|$ for a single grain silicon TFT for different $V_{GS\text{-}max}$. V_{DS}=0.1V.

To confirm this mechanism we have fabricated metal oxide semiconductor (MOS) devices with ECR-PECVD oxide and LPCVD oxide on p-type Si wafer with $N_A = 10^{16}$ cm^{-3}. The oxide layers were fabricated with the same process as SG-TFTs. The thicknesses of ECR-PECVD and LPCVD oxide films are 126.2nm and 131.5nm, respectively. The C-V curves of these devices have been measured at different frequencies. The devices with ECR-PECVD oxide show unstable flatband voltage, whereas the LPCVD oxide ones show a very stable flatband. So we conclude that the space charge motion in the ECR-PECVD oxide film is responsible for the variation of the flatband voltage.

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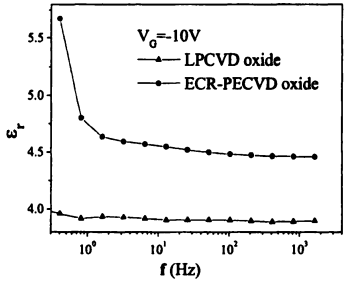


Fig.7, The dielectric constant of ECR-PECVD and LPCVD oxides in MOS devices deduced from capacitance measurements vs frequency at V_G=-10V. The top electrode is Al.

Fig.7 shows the calculated dielectric constants of the two films as a function of frequency extracted from the capacitance measured at V_G=-10V (accumulation condition). The ECR-PECVD oxide has much higher dielectric constant and a large frequency dispersion, which is due to the space charge relaxation in the oxide (9, 10). Therefore, the MOS C-V measurements versus frequency are consistent with the transient measurements in the SG-TFTs.

It is difficult to decide the nature of the space charge in our ECR-PECVD oxide films from the measurements described above. Since the undershoot value is proportional to the applied voltage, the effect can be due to the relaxation of dipoles formed by impurity ions in the oxide film (10) or the drift of ions/localized charges. A similar drain current relaxation lasting hundreds of milliseconds has been observed in SOI MOSFET by K. Vanheusden, et al (11). This relaxation has been attributed to the drift of protons in the gate dielectric. We expect that protons can be easily introduced in our SiO_2 films during deposition or annealing. Thus the undershoot current we observed in SG-TFTs could be due to the drift of protons in the gate oxide.

ACKNOWLEDGEMENTS

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MODELLING OF SOURCE-GATED TRANSISTORS IN AMORPHOUS SILICON

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The most important advantage of a source-gated transistor compared with an FET is its low saturation voltage and high output impedance. Here we model a reverse biased gated Schottky barrier source in hydrogenated amorphous silicon and show good qualitative agreement between the calculated effect of source geometry and measurements. Furthermore, calculations of electron concentration profiles in the source show why the source-gated transistor in hydrogenated amorphous silicon is more stable than an equivalent FET.

INTRODUCTION

A new form of thin film transistors (TFT) was introduced recently named the Source Gated Transistor (SGT) (1). The basic principle of operation is different from a conventional field effect transistor (FET) where the electrical field induced by the gate modulates the channel conductance and current saturates when the semiconductor region at the drain end is depleted.
In the SGT the electric field induced by a gate located directly below the source is used to change the current through a reverse biased source barrier and current saturates when the semiconductor underneath the source barrier is depleted by the reverse biased barrier. Fig.1 shows a schematic drawing of the SGT transistor. The electron current flows from the source barrier to the semiconductor-insulator interface and then laterally to the drain contact.

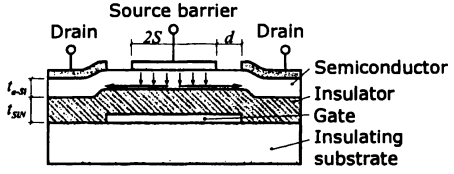


Fig.1. Schematic drawing of SGT transistor. The gap between source and drain contacts is defined as the source-drain separation (d).

The SGT has many advantages over a conventional FET such as excellent output characteristics with low saturation voltage and very high output impedance (2). An example is shown in Fig.2. Moreover the SGT in hydrogenated amorphous silicon (a-Si:H) shows good device stability at low currents (3), which allows us to consider these devices for analog circuits. Short channel effects are also reduced in the SGT (4). Furthermore it has been shown that a useful dynamic range can be achieved by increasing the capacitance of the gate dielectric (5).

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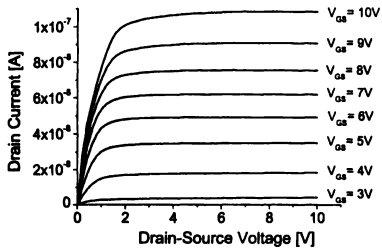


Fig.2. Experimental SGT transistor characteristics. The width of the device and source-drain separation was 12um and 2um respectively (t_{SiN} = 300nm and $t_{a\text{-}Si}$ = 100nm).

SGT's have been made in a-Si:H using a Schottky barrier source and ion implantation technology to control the effective source barrier height and passivate the region between the source and drain contacts (d Fig.1). The gate insulator was silicon nitride. The gate was extended under the region *d* to form a parasitic FET in series with the source barrier. This is necessary in a-Si:H otherwise its high resistivity would introduce an unacceptably high parasitic drain resistance in the on-state. In this configuration the on-state is controlled by the gated source barrier while the off-state is controlled by the parasitic FET.

The gated source barrier is a vital part of the SGT concept since it controls the on-state. A full understanding of the behavior of the source barrier is necessary, therefore, in order to characterize these devices. Here we are reporting on the source modeling of the SGT in a-Si:H, in particular how the barrier height and geometry of the source influence device performance. These issues are related to the validity of the dielectric model (2) for the saturation voltage and the stability of the SGT.

COMPARISON OF MODELLING WITH EXPERIMENT

Modelling of the SGT was done using the developer version of the ATLAS Silvaco (v.5.7.28.C) programme with the latest implementation of the model for the barrier tunneling and lowering mechanism.

Simulation of the saturation voltage and its dependence on the source-drain separation (*d*) of the parasitic FET is shown in Fig.3(a). It is seen that for small *d* when there is no constriction of the current the slope of the curve is given very well by dielectric model where the semiconductor is assumed to be depleted of charge at saturation and the slope dV_{SAT} / dV_G is C_G/C_S+C_G where C_S and C_G are the semiconductor and insulator capacitances per unit area. For the structure shown in Fig.3 this calculated value is 0.16. As *d* increases the saturation voltage increases because voltage is dropped across the parasitic FET. It is seen that the change of saturation voltage with gate voltage can be ten times lower than a conventional FET (V_G-V_T). Similar trends are seen in the experimental

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results shown in Fig.3(b) and shows that the Atlas model is able to predict the saturation voltage for a given geometry.

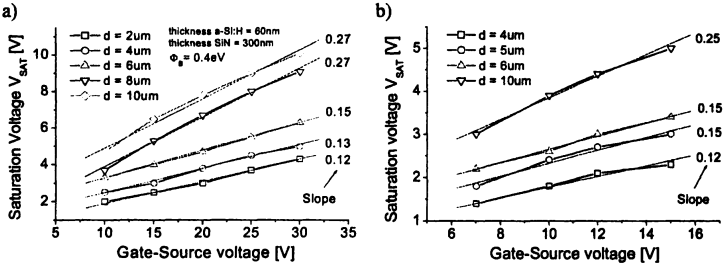


Fig.3 Dependence of saturation voltage on gate source voltage for various source-drain separation d a) modelled and b) measured.

The current (I_D) through the SGT is determined by a reverse biased source barrier i.e. it mainly depends on $_B$, the tunneling constant and area of the source. It has been shown that I_D scales linearly with the source width but is independent of source-drain separation d (4). In case of source length S (Fig.1) the I_D increases linearly with S for high $_B$ however for lower $_B$ the current has a tendency to saturate with increasing source length S (Fig.4(a)).

The dependence of current on source length S calculated using SILVACO Atlas is shown in Fig.4(b). It is seen that the change of the current with source length is in reasonable agreement with experiment (Fig.4(a)). With low barriers and high currents the source current tends to saturate with increasing source length.

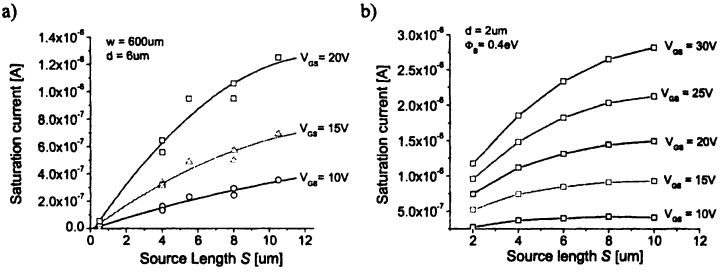


Fig.4 a) experimental and b) simulated dependence of the saturation current on source length S

The reason why the current tends to saturate can be seen with reference to Fig.5 where the current density normal to the Shottky barrier interface is calculated. It is seen that for higher current passing across the interface (Fig. 5(a)) the current density is not uniform

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and is more concentrated towards the edge of the source opposite the drain contact. As the current through the source increases there is a lateral voltage drop under the source barrier (Fig. 6(a)) and a large electric field gradient away from the edge of source and as the source length is increased a smaller fraction of current per unit source length is added to the source current. With low currents, however, the lateral voltage drop is much smaller and there is a fairly uniform current density along the source giving a linear dependence between source current and source length S (Fig. 5(b)).

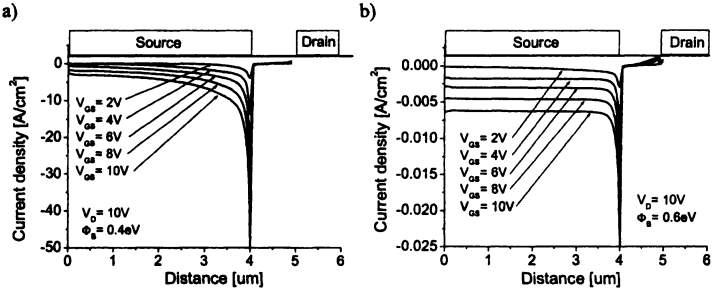


Fig.5 The calculated current density distribution along the source normal to the interface for two different barrier heights a) 0.4eV and b) 0.6eV.

The feature of current crowding towards the edge of source at high currents is further emphasised from the potential and electron concentration profiles along the semiconductor-insulator interface shown in Fig.6. Here we also include the parasitic FET with channel length of 1 micron.

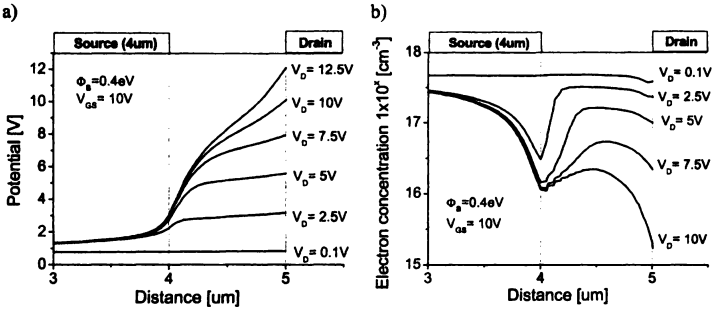


Fig.6.a) potential and b) electron concentration distribution along the semiconductor-insulator interface under the source

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The potential profile shows the lateral potential gradient under the source. When V_D is above the saturation voltage (~2V) the source depletion layer extends into the channel of the parasitic FET. At low drain voltages the potential drop across the FET is negligible while the source potential of the FET floats upwards to a value relative to the drain potential such that it just carries the saturation current supplied by the source barrier. When $V_D > V_G - V_T$, which is around 7V in this case, the device pinches off at the drain and the parasitic FET also operates in saturation and becomes depleted. This situation at large biased drain biases leads to further improvements to the output impedance.

For an FET biased into the on-state the electron quasi-Fermi level moves towards the conduction band in the channel region. This is consequently accompanied by a rise in the electron concentration and there is an increase in the generation of defect states (i.e. silicon dangling bonds) that trap electrons and cause a threshold voltage shift and current instability of the FET. However in a low current SGT the region underneath the source barrier is depleted after current saturation so the quasi-Fermi level is closer to the thermal equilibrium state. Therefore fewer states are generated in the a-Si:H and the device is much more stable (3).

Interestingly for high current devices when the depletion under the source barrier is very non-uniform, most of the current flows in the region where the electron concentration is lowest and the device most stable. In Fig.6 for example the peak current density occurs where the electron concentration at the interface is ~ $1x10^{16}$ cm^{-3}. This compares with a concentration of ~ $3x10^{17}$ cm^{-3} 1micron from the source edge. The amount of depletion is illustrated further in Fig.7 where electron concentration profiles across the a-Si:H from the source barrier to the semiconductor-insulator interface are plotted and compared with an FET having the same layers. Clearly the electron concentration increases with the lower barrier and higher current device but it is still much lower than that in the FET. Therefore as shown by experiment the SGT is more stable than an FET. However this stability improvement is less at higher current levels (i.e. lower barrier heights) (3).

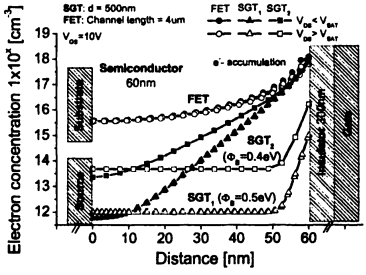


Fig.7. Electron concentration underneath the edge of the source barrier of an SGT with $_B$ = 0.5eV and 0.4eV. Also shown is the electron concentration 100nm from the source region of an FET.

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CONCLUSIONS

It has been shown that there is good qualitative agreement between experimental results and simulations using the SILVACO Atlas programme. In particular the dependence of the saturation voltage, saturation current and device stability of an SGT on the barrier height and geometry of the source has been clarified.

ACKNOWLEDGEMENTS

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AN INVESTIGATION OF THE ELECTRICALLY ACTIVE DEFECTS IN POLY-SI THIN FILM TRANSISTORS

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Reliability assessment of thin film transistors (TFTs) fabricated by excimer laser sequential lateral solidification (ELA SLS) process is presented. The devices were subjected to static hot carrier stress (DC HCS), with the bias levels appropriately selected to fulfill worst ageing conditions. The electrically active defects introduced by the static degradation were monitored by deep level transient spectroscopy (DLTS) technique. In order to further investigate the material quality, DLTS experiments were carried out both under dark and illumination conditions. The results stemmed from the DLTS analysis, manifested a continuous contribution of generation/recombination centers within the Si-film, indicative of high quality material.

1. Introduction

Polysilicon thin-film-transistors (TFT) are key building blocks for active-matrix-driven flat panel displays. The quality of a poly-Si film can be described as a function of the grain size, the defect density within the grain and at the grain boundary and the uniformity of the microstructure over a large area. These characteristic parameters are strongly affected by the crystallization process. Despite the necessary compromise among material quality, uniformity and process throughput, laser crystallization is the only technology that can produce polycrystalline films of high quality standards. Recently, polycrystalline silicon films have been obtained by means of an advanced crystallization method [1]. This method allowed the formation of large and directional (practically continuous) grains, leading to high quality material. Transistors with channel orientation parallel to the grains exhibited carrier mobility of about 300cm^2/Vsec. In this work, we took a step forward by investigating TFTs performance in the electrical characterization domain. Since DC stress tests constitute a standard practice on wafer-level and package-device reliability basis, we examined the impact of DC hot carrier degradation on MOSFET performance. The extracted results were assessed by implementing DLTS technique, under dark (i.e. no illumination) and under white illumination conditions.

2. Experimental

Polysilicon TFTs were fabricated in films formed by crystallization of amorphous silicon. The initial hydrogenated a-Si films (a-Si:H) were deposited at 320°C by plasma enhanced chemical vapor deposition (PECVD) on quartz substrates. The film

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thickness was 100nm. After deposition, the a-Si:H films were subjected to a dehydrogenation annealing step, at 500°C for 2h in nitrogen ambient, to remove the excess hydrogen. The resulting a-Si films were transformed to polysilicon ones by excimer laser annealing (ELA), using the sequential lateral solidification process (SLS). This process results in a polysilicon film composed of long crystal domains (grains), separated by roughly parallel grain boundaries [2]. All the devices were floating body (FB), n-channel MOSFETs, fabricated using a non-self-aligned top metal gate structure. The devices were aligned so that the grains would be parallel to the direction of the drain-current conduction. The gate dielectric was a 100nm thick PECVD SiO_2 film. The intrinsic active region of all TFTs (W x L) was 200μm x 8μm.

The static characteristics of the transistors were extracted using a Keithley 236 SMU in order to monitor the drain current, and a Keithley 6487 pico-ammeter/voltage source, which provided the gate bias and measured the gate current. The I_{DS}-V_{GS} transfer characteristics were recorded at 300K with V_{DS}=50mV and V_{GS} swept from -5V to +5V. The slope of a line fitted to the I_{DS}-V_{GS} curve at the point of maximum transconductance, and the intercept of that line on the V_{GS} axis, yielded the extrapolated threshold voltage. The subthreshold slope was extracted from the maximum slope of the I_{DS}-V_{GS} characteristic, drawn in semilog scale. The subthreshold swing was used to calculate the deep trap states density in the vicinity of the intrinsic Fermi level.

The HCS degradation characteristics were obtained at the worst ageing conditions regime, corresponding to V_G=V_D/2 and V_D=14V. The symbols V_G and V_D stand for gate and drain bias, respectively. The static stress duration was of the order of 10^5sec.

The DLTS assessment was based on recording drain current spectra $\Delta I_D(T)$ immediately after the device transition from ON- (accumulation) to OFF- (strong inversion) state, under dark and under white illumination conditions. The duration of the OFF-state was kept constant at 100msec. All measurements were carried out in the linear region of MOSFET operation (V_{DS}=50mV), in order to prevent further ageing of the devices. The DLTS experimental setup consisted of an SR570 current amplifier, which also provided the drain bias, and a DAQ card, which digitized the drain signal. The drain current was sampled in the 0-256ms time interval with a 1ms sampling rate. All the DLTS measurements were performed with the devices placed in a liquid nitrogen cryostat, which controlled the measurement temperature in the range of 200K to 400K. The switch-on transients were recorded and stored under thermal equilibrium conditions at every 1K step.

3. Results and discussion

3.1 HCS results

Typical transfer characteristics I_{DS}-V_{GS}, are shown in Figure 1. It is obvious that the degradation process shifts the threshold voltage towards more positive values, indicative of electron trapping into the gate oxide. This shift is presented against stressing time in logarithmic scale in Figure 2.

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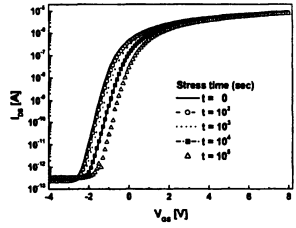


Figure 1. I_{DS}-V_{GS} characteristic curves of SLS ELA TFTs.

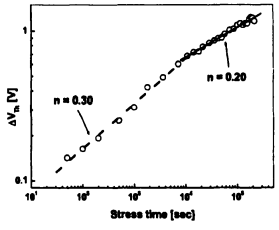


Figure 2. Threshold voltage shift due to DC HCS.

It is remarkable that threshold voltage variation against stress duration, reflects a complex degradation mechanism consisting of two distinguished components that obey the same empirical law $\Delta V_{Th}=At^n$. The degradation component with the power index value of n=0.2 is ascribed to the electron trapping into the gate oxide [3]. As for the other component, the power index value of n=0.3 is indicative of the maximum interface-state formation due to the maximum carrier injection towards the $Si-SiO_2$ interface [4]. The latter is consistent with the degradation condition $V_G=V_D/2$ that favors the injection of both types of carriers into the gate oxide. This behavior exhibits many similarities to the response of PD (partial depletion) SOI MOSFETs under the initial stages of DC HCS regime [5,6]. Figure 3 shows the drain current degradation versus stressing time. Actually, the reduced drain current is depicted so that any impact of mobility dependence is ruled out. Drain current degradation is relatively small; its variation reaches almost 10% for stressing times up to $2x10^5$sec. Accordingly to the threshold voltage degradation, the drain current degradation follows an analogous power law dependence $\Delta I_D/I_D=At^n$ for stressing times longer than 10^2 sec.

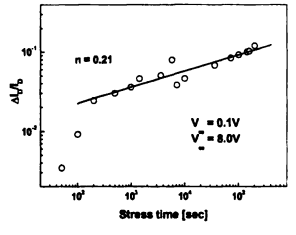


Figure 3. Reduced drain current versus stress duration.

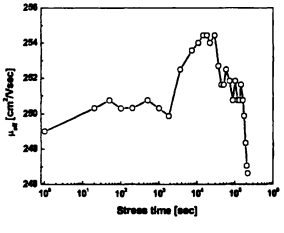


Figure 4. Effective mobility versus stress duration.

In this case, the respective value of power index n is 0.21. This fact verifies that the origin of degradation mechanism is associated to electron trapping towards the gate oxide. In Figure 4 the effective mobility versus stressing time is presented. The respective degradation is insignificant since its variation is estimated to be less than 3% for stress duration up to $2x10^5$ sec. The main factors that cause effective mobility

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degradation are: a) the existence of the interface traps located at the gate channel interface, and b) the potential barrier height introduced by the grain boundaries along the channel direction.

3.2 DLTS results

The drain current spectra under dark and illumination conditions of unstressed TFTs are presented in Figure 5. The spectrum under dark is continuous indicating a contribution from a continuous distribution of carrier interactions [7]. The latter affects mainly traps located in the vicinity of the channel, rather than deeper in the Si-film. During the ON-state, hole emission emerges, as soon as the channel is formed. The activation energy of such process is estimated approximately at 0.26eV. When the device is in the OFF-state holes are captured. On the condition that the Si-film is intrinsic, holes before being captured in the OFF-state should have followed a preceding thermal generation process from deep states [8]. Furthermore, since carrier emission rate decreases with decreasing temperature [9], the drain current magnitude levels off below 250K, suggestive of a freeze-out mechanism.

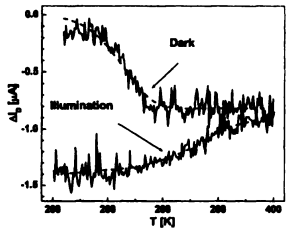


Figure 5. DLTS spectra of unstressed SLS ELA TFTs.

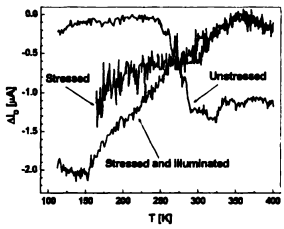


Figure 6. The impact of DC HCS on DLTS spectra.

Under illumination electron-hole pair generation occurs. The Fermi level beneath grain boundaries, splits into electron and hole quasi-Fermi levels. This quasi-Fermi shift encompasses much more localized states than at steady state, and hence more traps, especially those near the midgap, act as efficient recombination centers [10]. Thus, the increasing recombination current via grain boundary recombination centers, causes the drain current magnitude to obtain larger values.

There is remarkable difference of the DLTS spectra under the impact of DC HCS at dark, as it is exhibited in Figure 6. The shape of the spectra is totally different compared to the unstressed case, indicating that other mechanisms come into play. In particular, the contribution of hole traps is compensated by other traps, negatively charged, most likely stemming from hot-electron generation. The latter is in accord with the threshold voltage shift to more positive values.

Although DLTS spectra after HCS process, under both dark and white illumination conditions, are similar for temperatures larger than 250K, the impact of light differentiates the magnitude of the spectra below 250K. This may be interpreted by assuming an introduction of a large concentration of recombination centers. Such

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centers can decrease significantly the carrier lifetime, hence decreasing the concentration of excess carriers produced under white-light illumination. We note that temperature is equivalent to energy, in terms of eV, which can be also interpreted as location within the Si bandgap, with reference to the interacting band. The interacting band in our case is the valence band. Hence, the larger values of the spectra under stress and simultaneous illumination, leads us to the conclusion that HCS introduces relatively shallow traps.

4. Conclusions

The impact of DC HCS on SLS ELA TFTs was studied. The assessment was conducted by DLTS technique under dark and white-light illumination conditions. The DLTS spectra of unstressed devices revealed that thermally generated holes are captured in the OFF-state, and emitted in the ON-state. The impact of light, through photo-induced pair generation, compensates the freeze-out phenomena at low temperatures. The difference in the DLTS spectra due to HCS, under dark conditions, suggests that hot carrier generation compensates hole capture-emission mechanisms derived from hole-trap contribution. When illuminated, the stressed devices below 250K exhibit partially altered DLTS spectra. The latter is indicative of the existence of relatively shallow traps.

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SIMULATION OF TWIN BOUNDARY EFFECT ON TFT CHARACTERISTICS

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The influence of twin boundary on the characteristics of single grain TFT has been analysed by ISE 3-D simulator. It has been found that the orientation and the position of the twin boundary could affect the field effect mobility, the leakage current and the kink effect of the device. The field effect mobility increases with the decrease of the angle between the twin boundary and the channel direction, which is consistent with the experiment results. The twin boundary in contact with the drain leads to higher leakage current because electron-hole generation is enhanced by the trap states in the twin boundary. The simulation indicates that the local electric field near a twin boundary is very high, thus inducing strong impact ionization. The smaller the distance between the twin boundary and the drain the higher the kink effect.

INTRODUCTION

Recently, thanks to a new technique referred to as Micro-Czochralski or grain-filter process (1-3), Thin Film Transistors (TFTs) can be fabricated on a location controlled silicon single grain. Much higher mobilities (400 cm^2/Vs) than those of standard laser-crystallized polycrystalline silicon TFTs (poly-Si TFT) are obtained in such Single Grain TFT (SG-TFT). However, device to device non-uniformities are sometimes observed and attributed to the presence of twin boundaries (4). We report here for the first time 3-D simulation of TFTs and use it to investigate the effect of a twin boundary in the devices, including its influence on effective mobility, off current and kink effect.

SIMULATION METHOD AND MODELS

ISE - Integrated Systems Engineering commercial package version 9.0 has been used for the 3-D simulation. The geometry of the device, doping density and mesh for the simulation were generated by the 3D device editor: DEVISE and the electric behaviour of the device was simulated by DESSIS.

In the simulation, there are three governing equations for charge transport in semiconductor devices: Poisson equation and two electron and hole continuity equations. The Poisson equation is stated as:

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$$\nabla\varepsilon.\nabla\psi = -q(p - n + N_{D+} - N_{A-}), \quad [1]$$

where, N_{D+} and N_{A-} are the number of ionized donors and acceptors, respectively, n and p are the electron and hole density. The electron and hole continuity equations are written as follows:

$$\nabla \bullet \overrightarrow{J_n} = qR + q\frac{\partial n}{\partial t} \quad [2]$$

$$\nabla \bullet \overrightarrow{J_p} = qR + q\frac{\partial p}{\partial t} \quad [3]$$

where R is the net electron-hole recombination rate and J_n and J_p are the electron and hole current density. In this simulation, the Shockley-Read-Hall recombination model has been applied.

In high electric field, free carriers gain a very high energy, thus the carrier temperature is higher than the lattice temperature, which is especially important for the simulation on kink effect. Therefore the hydrodynamic model has been adopted(5). In this model the current densities are defined as follows:

$$\overrightarrow{J_n} = \mu_n(n\nabla E_C + kT_n\nabla n + f_n^{td}kn\nabla T_n - 1.5nkT_n\nabla \ln m_e) \quad [4]$$

$$\overrightarrow{J_p} = \mu_p(p\nabla E_V - kT_p\nabla p - f_p^{td}kp\nabla T_p - 1.5pkT_p\nabla \ln m_h) \quad [5]$$

where, E_C and E_V are the conduction and valence band energies, respectively, $T_n$and T_p are the temperature of electrons and holes, respectively. m_e and m_h are effective masses. f_n^{td} and f_p^{td} are parameters for electrons and holes.

RESULTS AND DISCUSSIONS

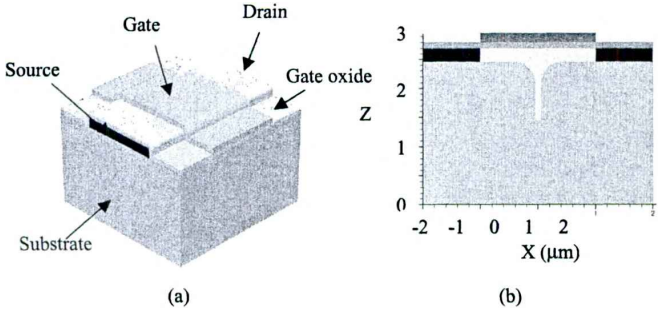


Fig.1, (a) Three-dimensional view of the SG-TFT device structure used for simulation. (b) Cross-sectional view of the device.

Fig.1 shows the n-channel SG-TFT structure used in the simulation. The thickness of gate oxide is 100nm, and the gate size is 2μm/2μm. The active thickness of Si film is 250μm, which is identical to that of the fabricated devices. The diameter of the central

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hole (grain filter) is 100nm. In the simulation, the trap states density and the capture cross section need to be set with reasonable values. We model the twin boundary as a planar defect with a density of gap states (6). The Density of States (DOS) is given by:

$$N(E) = N_{at}e^{(E-E_C)/E_{at}} + N_{ad}e^{(E-E_C)/E_{ad}} + N_{dt}e^{(E_V-E)/E_{dt}} + N_{dd}e^{(E_V-E)/E_{dd}} \quad [6]$$

where, the subscripts *a* and *d* refer to acceptor- and donor-like states, respectively, the subscripts *t* and *d* refer to tail and deep states. Fig.2 shows the DOS in the twin boundary we used for the simulation, which was generated with the data below:

$N_{at} = 5\times10^{15}cm^{-2}eV^{-1}$, $E_{at} = 0.05eV$

$N_{ad} = 2\times10^{12}cm^{-2}eV^{-1}$, $E_{ad} = 0.33eV$

$N_{dt} = 5\times10^{15}cm^{-2}eV^{-1}$, $E_{dt} = 0.05eV$

$N_{dd} = 4.5\times10^{12}cm^{-2}eV^{-1}$, $E_{dd} = 0.33eV$

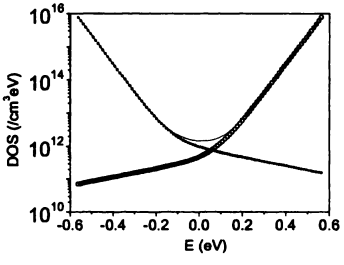


Fig.2 Density of trap states (DOS) in the twin boundary used in the simulation

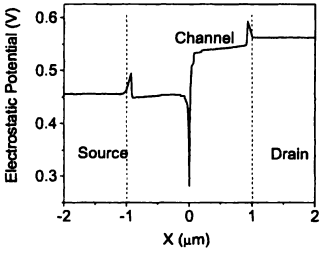


Fig.3 Surface potential of the SG-TFT with a twin boundary perpendicular to the channel direction and located in the middle of the channel. V_{DS}=0.1V and V_{GS}=10.0V

To accurately simulate the off current, the Shorkley-Read-Hall generation-recombination model has been adopted in the simulation. The capture cross sections of trap states are: $\sigma_{nd}=10^{-13}cm^2$, $\sigma_{na}=10^{-15}cm^2$, $\sigma_{pd}=10^{-15}cm^2$ and $\sigma_{pa}=10^{-13}cm^2$. $\sigma_{n(p)d(a)}$ is the electron(hole) capture cross section of donor (acceptor) states.

A. Effect of twin boundary orientation on transfer characteristics

It has been reported that the orientation of twin boundary had pronounced influence on the field effect mobility in SG-TFTs. To show this effect, we have simulated five n-channel devices with the same geometry and with a single twin boundary in the channel. The devices differ in the angle between the twin boundary and the channel

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direction: 90° (orthogonal to channel direction), 60°, 45°, 30° and 0° (parallel to channel).

Fig.3 shows the channel surface potential for the device with 90° twin boundary at V_{gs}=10.0V and V_{ds}=0.1V. There is a potential barrier associated with the twin boundary, ~0.17eV high, which is much bigger than kT at room temperature. So the current across the barrier is limited by thermionic emission. As shown in Fig.4, we find that the effective electron mobility decreases for increasing angle between the twin boundary and the channel direction, which is consistent with the experiment results. Because the current is controlled by the twin boundary, it is approximately proportional to the boundary length if the latter crosses the entire channel width. Therefore, it is reasonable to conclude that the orientation effect can be explained in terms of the boundary length effect.

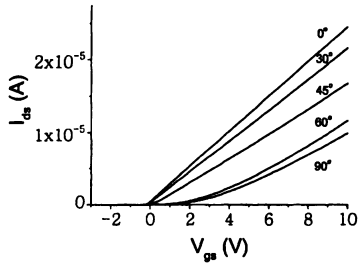


Fig.4 The simulated transfer characteristics of the SG-TFTs with one twin boundary in the middle of the channel. V_{ds}=0.1V. The angle between the twin boundary and the source-drain direction varies from 0° to 90°.

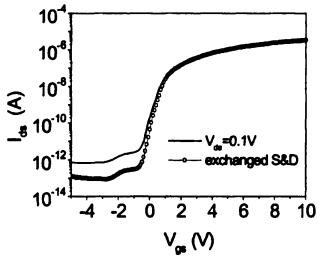


Fig.5 Experimental transfer characteristics of the SG-TFT (W/L=3.2μm/2.9μm) for source and drain exchange.

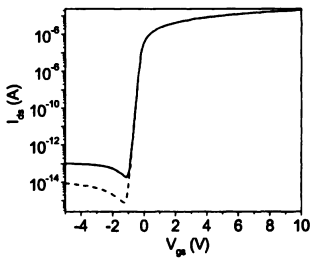


Fig.6 Simulation of the transfer characteristics of a SG-TFT device with a twin boundary in contact with the drain (solid line) or the source (dashed line). V_{ds}=0.1V.

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B. Effect of twin boundary on off-current

Another important TFT parameter is the off current. As shown in fig. 5, some n-channel SG-TFTs show asymmetrical off current when source and drain are exchanged. This phenomenon is not present in small grain poly-Si TFTs. We have simulated the effect of the twin boundary on the off current and found that the latter is much higher if the twin boundary is in contact with the drain (Fig.6). This is due to the fact that the off-current is controlled by carrier generation near the drain (6). So, if the twin boundary is in contact with the drain but not with the source, an asymmetry in the off current for source-drain swapping will result. In our simulation, we have found the main contribution of the electron-hole generation comes from the midgap states, thus DOS in the midgap and the capture cross section of these states are important for the off current, which is consistent with the theory for off current reported before (7).

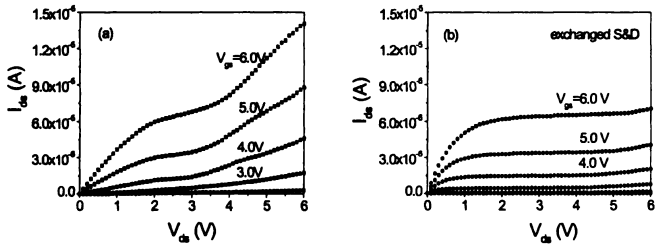


Fig.7 (a) Experimental output characteristics of a SG-TFT (W/L=3.2μm/2.9μm) showing the kink effect. (b) Output characteristics of the same device with the source and drain exchanged: no kink effect is present.

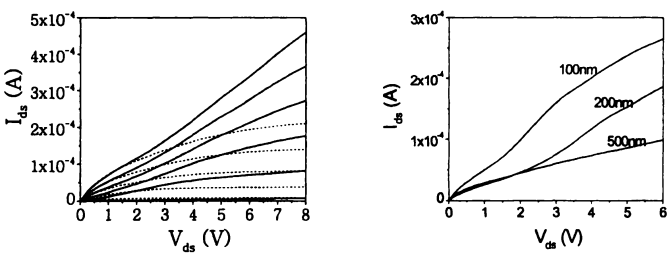


Fig.8, Simulated output curves of the SG-TFTs with a twin boundary near the drain (solid line) or near the source (dash line). From top to bottom, V_{gs} =10V, 8V, 6V, 4V, 2V, and 0V, respectively.

Fig.9. Simulated output curves of the SG-TFTs with different distance between the twin boundary and the drain. V_{gs}=6V.

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C. Simulation on kink effect

The kink effect has been observed in some SG-TFTs. Fig.7 shows the experimental output characteristics of a n-channel SG TFT. However, the kink effect (Fig.7a), disappears when source and drain are exchanged (Fig.7b). This effect can be reproduced in simulation (Fig.8). In this simulation, the twin boundary is orthogonal to the source-drain direction. We found that the position of the twin boundary is very important for the kink effect. A big kink effect can be observed when the boundary is close to the drain (100nm between the twin boundary and the drain) whereas no kink is observed when it is close to the source. Hence the asymmetry for source-drain swapping results. According to the simulation results, the effect is due to the enhancement of the electric field and the associated impact ionization at the twin boundary. Such enhancement is strongly dependent on the density of traps at the boundary.

We have simulated the devices with different distances between the twin boundary and the drain. As shown in fig. 9, the output current becomes smaller with the increase of the distance. Simulation shows that this is due to the fact that the local electric field and impact ionization at the twin boundary decreases for increasing distance between the latter and the drain.

ACKNOWLEDGEMENTS

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THIN FILM TRANSISTOR MODELS FOR CIRCUIT SIMULATION

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We review recent physics-based TFT models suitable for implementation in circuit simulators, such as SPICE, with emphasis on modeling non-ideal effects, including gate voltage dependent field effect mobility, and non-linear gate voltage dependent series resistances. The models accurately reproduce the characteristics of TFTs of different types for a broad range of channel lengths.

INTRODUCTION

Modeling of Thin Film Transistors (TFTs) presents unique challenges related to a rich variety of observed TFT characteristics and many non-ideal features affecting their performance [1]. These non-ideal characteristics are related to the gate voltage dependent field effect mobility, the distributive nature of gate-to-channel capacitance, gate voltage dependent series source and drain resistances, non-ohmic contacts, gate and drain bias voltage stress effects, and short channel effects that are very pronounced even in relatively long channel devices. Localized states play an important role in all TFTs as illustrated in Fig. 1 that compares the distributions of localized states in a-Si and poly-Si with the absence of such states in crystalline silicon. Amorphous silicon and polysilicon TFT models are better established than models for nanocrystalline silicon (nc-Si) TFTs and Organic TFTs (OTFTs). The unique properties of nc-Si have been reported very recently. OTFT characteristics strongly depend on the organic compound used and on the device design; for example, on the location of the source and drain contacts in so-called top contact and bottom contact TFTs. Modeling of TFTs on flexible substrates, such as metal or plastic foils, presents additional challenges.

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This paper will review physics-based TFT models suitable for implementation in circuit simulators, such as SPICE, with emphasis on modeling non-ideal effects, including modeling stress effects and non-linear gate voltage dependent series resistances. Comparison with measured data shows that these models adequately reproduce experimental data and are suitable for simulation of electronic circuits containing TFTs. We will also discuss low frequency noise in TFTs and link the device physics to the observed noise behavior. (The low frequency noise in TFTs is primarily 1/f noise and is several orders of magnitude higher than in their crystalline counterparts.)

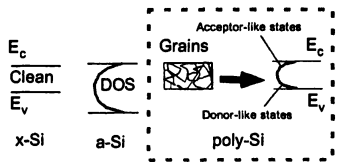


Fig. 1. Energy band diagrams for crystalline silicon, amorphous silicon, and poly-Si[TF1].

RESULTS AND DISCUSSION

1. Poly-Si TFT Modeling

To[TF2] develop poly-Si TFT models suitable for circuit simulation, we consider the non-uniform polysilicon film with grain boundaries as some uniform effective medium with effective material properties (the "effective medium" approach [1-5]).

We previously developed a complete poly-Si TFT model, implemented as MOSFET Level 16 in AIM-Spice [1-4], which was proven to be valid for channel lengths down to 6 μm. In the subthreshold regime, the current, I_{sub}, is dominated by diffusion and is given by:

$$I_{sub} = \mu_s C_{ox} \frac{W}{L} (\eta V_{th})^2 \exp\left(\frac{V_{gs} - V_T}{\eta V_{th}}\right)\left[1 - \exp\left(\frac{-V_{ds}}{\eta V_{th}}\right)\right] \quad (1)$$

where C_{ox} is the oxide capacitance, V_T is the threshold voltage, η is the subthreshold ideality factor, V_{gs} and V_{ds} are gate-to-source and drain-to-source voltages, respectively, and μ_s is the effective subthreshold mobility.

An additional term is added to the drain current to account for the leakage well below threshold, which is mostly caused by thermionic field emission (TFE) through the grain-boundary trap states [4].

Above threshold, the transport of carriers is determined by a combination of two mechanisms: drift in the grains and thermionic emission in the grain boundaries. To the first order, the drain current I_a is given by an expression similar to that used for crystalline MOSFETs:

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$$I_a = \mu_{FET} C_{ox} \frac{W}{L}\left(V_{gt} - \frac{V_{dse}}{2\alpha_{sat}}\right)V_{dse}. \qquad (2)$$

Here μ_{FET} is the gate voltage dependent field-effect mobility that includes the effects of the trap states in the grain boundaries, α_{sat} is the body constant, $V_{gt}=V_{gs}-V_T$, and V_{dse} is a smoothening function which represents the effective drain-source voltage.

At high drain voltage (i.e., high longitudinal fields), impact ionization happens near the drain and electron-hole pairs are generated. In an *n*-channel device, the generated electrons (holes in p-channel devices) move to the drain and the generated holes (electrons in *p*-channel devices) are injected into the film, lowering the source-film potential barrier and, as a result, increasing the above threshold drain current. This increase of the drain current is modeled by adding an additional term to the current [1-4]:

$$I_D = I_d + \Delta I_{kink} = I_d(1+M) \qquad (3)$$

where $I_{d,sat}$ is the drain current in saturation and

$$M = \left(\frac{L_{kink}}{L}\right)^{m_{kink}}\left(\frac{V_{ds}-V_{dse}}{V_{kink}}\right)\exp\left(\frac{-V_{kink}}{V_{ds}-V_{dse}}\right) \qquad (4)$$

Here, V_{kink}, L_{kink} and m_{kink} are the kink model parameters.

A unified model for the drain current I_d, is obtained by combining the subthreshold and above-threshold currents as: $\frac{1}{I_d} = \frac{1}{I_{sub}} + \frac{1}{I_a}$.

We have observed that in transistors with channel lengths smaller than 6.0 μm, short-channel effects become more pronounced, and, consequently, additional improvements become necessary. For this purpose, we developed a new poly-Si TFT model [1-3,5] more appropriate for shorter devices and based on the principles of the unified FET modeling concept. [1,6]

The channel current is written according to the following unified and universal expression:

$$I_d = \frac{g_{ch} V_{ds}\left(1+\lambda V_{ds}\right)}{\left[1+\left(g_{ch} V_{ds}/I_{sat}\right)^m\right]^{1/m}}, \qquad (5)$$

where λ is the channel length modulation parameter, m is a shape parameter that controls the transition from linear regime to saturation, and g_{ch} is the extrinsic linear channel conductance given by

$$g_{ch} = \frac{g_{chi}}{1+g_{chi}\left(R_s+R_d\right)}. \qquad (6)$$

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Here R_s and R_d are the source and drain parasitic series resistances, respectively, and $g_{chi} = qn_s\mu_{eff}\frac{W}{L}$ [TF3] is the intrinsic channel conductance, n_s being a unified expression of the sheet carrier density at the source end of the channel.

The unified saturation current I_{sat} entering into Eq. (5) is derived by using an adequate velocity-field relationship [1-3,5].

The increase of drain current in saturation caused by impact ionization is modeled using (3) and (4). The new model also accounts for the observed decrease of the subthreshold ideality factor with increasing drain voltage due to floating body and impact ionization effects [1-3,5].

This short-channel model was validated for transistors of channel lengths down to 2 μm (see Fig. 2.) Good agreement between the model predictions and experiments is observed throughout all operating regimes.

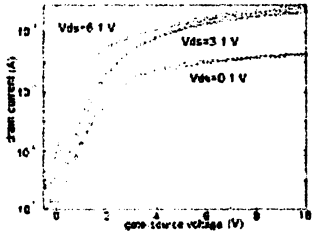


Fig. 2. Comparisons between measured (symbols) and modeled (solid curves) I-V characteristics of an n-channel poly-Si TFT with W = 10 μm and L = 2 μm [5]

2. Amorphous silicon TFT Modeling

Our long-channel compact a-Si TFT model was proven to fit quite accurately the characteristics of long channel devices [1]. However, in short-channel devices, two additional effects become relevant; the self-heating and the kink effect [1,2,7,8]. The self-heating effect is caused by an increase of the carrier temperature in the a-Si film as the channel current (and, hence, the power dissipation) increases. The result is an enhancement of the drain current, because the effective carrier mobility increases with increasing temperature (due to a larger density of free carriers) [1,8]. The kink effect is caused by the lowering of the source-film potential barrier due to the injection of holes generated at high drain voltages. In a-Si TFTs, these holes are generated by tunneling from traps near the drain at high longitudinal fields.

A short-channel a-Si TFT model was formulated by adapting our long-channel model to include self-heating and kink effects. We start by considering the intrinsic expression for the drain current in the above-threshold regime [1,2,7]:

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$$I_a = \mu_{FET} C_{ox} \frac{W}{L} \left(V_{gs} - V_{T0} - \alpha_{SAT} V_{dse}\right) V_{dse} \quad (7)$$

The field-effect mobility in a-Si TFTs can be expressed as:

$$\mu_{FET} = \mu_n \left(\frac{V_{gs} - V_{T0}}{V_{AA}} \right)^{\gamma} \quad (8)$$

where V_{AA} is a characteristic voltage, and γ is a model parameter related to the density of localized states.

In the subthreshold regime, the drain current is modeled as a power function of V_{gs} - V_{FB}, where V_{FB} is the flat-band voltage [1,7]. Well below threshold, the dominant current mechanism is a hole-induced drain leakage current caused by thermionic diffusion at the contacts, which is accounted for as suggested in [7].

In order to derive an analytical equation for the self-heating effect, we first find the temperature dependencies of the three device parameters that are most sensitive to the temperature (threshold voltage, field-effect mobility, and the saturation parameter). Using a first-order expansion in temperature, the expression of the drain current accounting for self-heating is derived.

To account for the kink effect, we assume that the generated holes decrease the threshold voltage with this decrease being proportional to the tunneling current.

We finally obtain the following expression for the drain current [1,2,8]:

$$I_D = \frac{I_{Do}}{1 - \frac{I_{Do} V_{ds}}{R_{total} T_{tot}}} + \Gamma V_{gs} \left(V_{ds} - V_{dse}\right) \exp\left(\frac{-V_K}{V_{ds} - V_{dse}} \right) \quad (9)$$

where Γ and V_K are the adjustable model parameters, R_{total} is the thermal resistance and T_{tot} is the effective device temperature, which is a function of the bias.

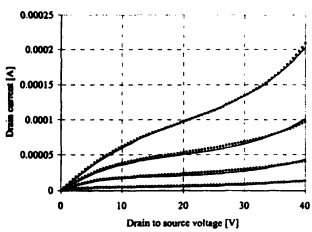


Fig.3. Measured (dots) and modeled (solid lines) characteristics of an a-Si TFT with L = 4 μm [8]

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In Fig. 3, we show that by accounting for both self-heating and kink effect, the model fits very well the characteristics of short-channel TFTs.

3. Nanocrystalline silicon TFT modeling

When we tried to fit the experimental *nc*-Si TFT characteristics using the *a*-Si:H TFT model presented in [3,9], we observed that that model cannot reproduce a substantial increase of the drain current and transconductance for V_{gs} above a certain, and not very high, value (about 17 V). Therefore, we had to develop a separate model for *nc*-Si TFT model based on the a-Si TFT model.

In a-Si:H TFTs, the field effect mobility μ_{FET} is proportional to $n_{free}/(n_{free}+n_{trapped})$, where n_{free} is the free electron concentration and $n_{trapped}$ is the concentration of the electrons trapped in defect states [3,9]. For gate voltages within the normal operation range, $n_{free} < n_{trapped}$. Both n_{free} and $n_{trapped}$ increase with increasing gate voltage, but the factors $n_{free}/(n_{free}+n_{trapped})$ and μ_{FET} well above threshold (but in the regime when the tail states are not completely filled) are weak functions of the gate voltage [8].

For gate voltages higher than a certain transition voltage, V_{tr}, the tail states are almost completely filled and as a consequence, $n_{trapped}$ remains constant, whereas n_{free} increases linearly with increasing V_{gs} similarly to that in crystalline MOSFETs. Therefore, the field effect mobility becomes linearly dependent on V_{gs}, leading to the quadratic dependence of the channel current on V_{gs}. A lower density of the tail states eases the transition to the crystalline-like regime at lower gate voltages. This is why, in *nc*-Si:H TFTs (which has lower DOS than a-Si TFTs), SSS[TF4] the transition to crystalline-like regime occurs at significantly lower gate voltages than in a-Si TFTs.

Consequently, we have modified the existing a-Si:H TFT AIM-Spice model to describe the quadratic-dependent current component at high V_{gs}. We use an expression for the current that is added to the current given by the a-Si TFT model [9]:

$$I_{tr} = \frac{1}{2}\mu_n C_i \frac{W}{L} V_{dse}(1+\lambda V_{DS}) \cdot M \cdot V_{gtre}^{2+D} \qquad (10_{[TF5]})$$

$$\text{where } V_{gtre} = V_{th} \cdot \left[1+\frac{V_{gtr}}{2V_{th}}+\sqrt{\delta^2+\left(\frac{V_{gtr}}{2V_{th}}-1\right)^2}\right] \qquad (11)$$

To make the model compact and continuous over all operation regimes, we use the following unified expression of the channel current, which smoothly tends to the desired expression in each regime:

$$I_{ds} = I_{leak} + \left(\frac{1}{I_{sub}} + \frac{1}{I_{abv}+I_{tr}}\right)^{-1} \qquad (12)$$

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where I_{leak} and I_{sub} are, respectively the expressions of the leakage and subthreshold channel current given in [9], and I_{abv} is the linear above threshold contribution given by (7).

A new procedure was developed to determine model parameters for nanocrystalline TFTs [10]. The method is partly based on the so-called integral function method. The method allows the extraction of the model parameters for the three regions observed for nanocrystalline devices, that is, for the subthreshold region and for the two above-threshold regions. These parameters are extracted in a simple and direct way from the experimental measurements, with no need of assigning predetermined values to any other model parameter or using optimization methods.

In Fig. 4 we see that the modeled transconductance characteristic agrees very well with the experimental data both below and above threshold.

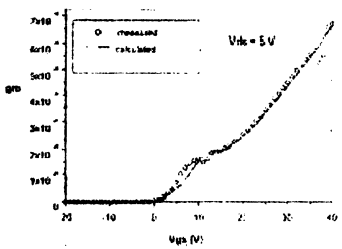


Fig 4. Experimental and modeled transconductance using the new nc-Si:H model [9].

4. Organic TFT modeling

The physics of organic TFTs is very complex, but there are some similarities with a-Si TFTs [11]. In pentacene organic TFTs operating above-threshold, most of the charge induced by the gate-source voltage is trapped with only a small fraction of the carriers participating in the current conduction. We developed a model that accounts for the effect of the charge trapping via a gate-voltage dependent field-effect mobility, using an expression similar to (8). The model also takes into account the parasitic series drain and source resistances.

The two main designs of pentacene OTFTs are top (TC) and bottom (BC) source and drain contact (TC) TFTs.

Fig.5 shows the output characteristics of the gold (Au) and palladium (Pd) TC TFTs and the Pd BC TFT (L=60μm) at V_{GS} =60 V. The Pd TC and BC TFT have a pronounced non-linearity of the output characteristic at low V_{DS} ($|V_{DS}|$ <2 V), in contrast to the Au TC TFT characteristic.

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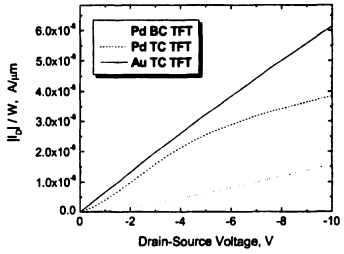


Fig. 5. Top contact and bottom contact pentacene TFT (gate length) output characteristics (V_{GS} =-60V) [12]

Because of the linearity of its low v_{ds} output characteristic, the au tc tft contact resistance can be modeled as a total contact resistance in series with the channel resistance. The tc tft contact resistance is comparable to or exceeds the channel resistance for channels shorter than approximately 10 μm. The extracted au tc tft contact resistance depends on v_{gs}, but shows no dependence on the drain bias [12].

The contact resistance of bc tfts depends both on gate and drain bias. We proposed a circuit to simulate the bc tft contact resistance and we extracted and compared the tft channel resistances at different drain voltages [12]. The equivalent bc tft circuit consists of the tft with linear source and drain access resistances, and a pair of anti-parallel leaky schottky diodes connected to each access resistor in series [11, 12]. Two diodes in parallel are needed to obtain a symmetric current-voltage characteristic.

We proved that our model provides fair agreement between the modeled and measured characteristics for both TC (Fig. 6) and BC OTFTs from subthreshold to above threshold.

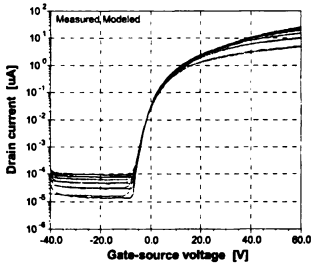


Fig. 6. Modeling of Au TC pentacene TFT transfer characteristics [11]

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We studied the low-frequency noise in pentacene organic thin film transistors of different designs [13]. Our studies showed that the TFT design affects the noise level and the noise dependence on the gate- and drain-source biases. The measured low-frequency noise is 1/f noise in the 100 Hz-3.5 KHz range for both TC and BC TFTs (Fig. 7). The measured noise level was the lowest for the TFTs with a top source and drain contacts design. For these devices, the noise dependence at low drain current values resembled that for *n*-type crystalline Si metal–oxide–semiconductor field-effect transistors.

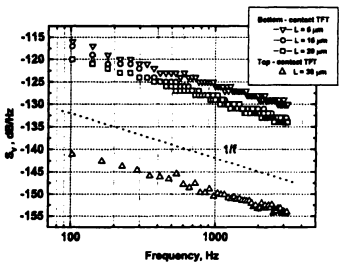


Fig. 7. Typical spectral density of the voltage fluctuations S_V versus frequency for pentacene TFTs. 1/f line is shown for reference [13].

The extracted Hooge parameter, which allows comparing the noise level in different devices and materials, was 0.045 for the top-contact TFTs. This parameter value is several orders of magnitude lower than that for conducting polymers[TF7] and only several times higher than that for hydrogenated amorphous Si (a-Si:H) TFTs. The bottom source and drain contacts TFTs had a much higher noise level with a noise dependence on the terminal voltages that differed from the noise voltage dependence for the top-contact TFTs. The Hooge parameter values were in the range of 5–20 for the bottom-contact TFTs. We estimated that the contact noise could be comparable to the channel noise for both TC and BC TFTs.

CONCLUSIONS

We have reviewed recent physics-based TFT models adequate for implementation in circuit simulators, such as SPICE. For an accurate modeling, a number of non-ideal effects should be considered, such as gate voltage dependent field effect mobility and non-linear gate voltage dependent series resistances. Our models accurately reproduce the characteristics of TFTs of different types (poly-Si, *a*-Si, *nc*-Si and organic TFTs) through all operating regimes and for a broad range of channel lengths.

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TFT MOBILITY REQUIREMENT FOR AMOLED HDTVS

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ABSTRACT

This paper thoroughly investigates the performance requirements of TFTs for 30-inch and 40-inch diagonal full-specification (1920×1080) AMOLED HDTV. We tried to find the minimum required mobility of TFTs to meet the pixel charging capability as well as the OLED driving current for two kinds of voltage programmable pixel structures and one current programmable pixel structure. One of voltage programming pixels is a basic 2TFT-and-1Capacitor (2T1C) pixel, and the other one is a 5TFT-and-1Capacitor (5T1C) pixel proposed for compensating the V_{TH} variations. We choose the current programmable 4TFT-and-2Capacitor (4T2C) pixel structure with voltage boosting function for better current programmability. For this purpose, we found the pixel circuit design methods for minimizing the required mobility with various design parameters, and carefully constitute the panel modeling. Through SPICE simulations reveal that the minimum TFT mobility for 30-inch and 40-inch HDTV with voltage programming pixel structures is 1.19cm^2/V-s and 1.00cm^2/V-s, respectively, for the 2T1C pixel with V_{TH} = 3V and ΔV_P = 200mV, and 0.57cm^2/V-s and 0.73cm^2/V-s for the 5T1C pixel with V_{TH} = 3V, respectively. And the minimum TFT mobility of 30~40inch HDTV with the current programmable pixel structure for driving TFT sizes of 30μm/10μm with V_{TH} = 2V and 30μm/10μm with V_{TH} = 3V is 19cm^2/V-s and 21cm^2/V-s, respectively.

INTRODUCTION

Organic light emitting diodes (OLEDs) have been expected to be one of the most promising candidates for the next generation flat panel displays (FPDs), because they have many advantages over their competitors including liquid crystal displays (LCDs) and plasma display panels (PDPs); wide viewing angle, fast response time, slimness, low cost, and low power consumption [1].

However, OLEDs remain mainly small-size display devices for digital camera view finders or mobile phone displays[2-3]. To penetrate into the medium- or large-size display territory, active matrix OLEDs (AMOLEDs) are inevitable. Passive matrix OLEDs (PMOLEDs) have to perform such a high degree of multiplexing for high-resolution display that impracticably high level currents are required.

Similarly to the case of LCDs, thin film transistors (TFTs) based on amorphous silicon (α-Si) and low temperature poly silicon (LTPS) are the technologies of choice for the large-size OLED displays. OLEDs are basically current-driven devices, so each pixel circuit has to provide a significant current to OLED material to get the agreeable

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brightness. The LTPS technologies are preferable in this respect, because they generally show some two orders higher mobility than their α-Si counterparts. On the other hand, the fabrication cost and the proven maturity for large-size displays make α-Si technologies very attractive.

Among a variety of technical challenges for AMOLEDs to be employed for large-size displays, this paper focuses on the TFT performance requirements. We considered various design parameters and specifications of the pixel circuits to find the minimum required mobility of TFTs to support the full-specification HDTV (1920×1080) of 30 and 40 inches on the diagonal. First, we found out the minimum required mobility of a basic pixel circuit consisting of 2 TFTs and 1 capacitor, and then, moved to the threshold voltage (V_{TH})-compensated voltage programmable pixel circuit structure. And finally, we investigated the minimum required mobility of the current programmable pixel structure with voltage pre-charging and voltage boosting functions for better current programmability.

SPECIFICATIONS AND ASSUMPTIONS

International Display Technology already demonstrated the 20-inch diagonal α-Si TFT-OLED with the WXGA(1280×768) format[4]. To expand the applications to the full-specification HDTV, we deal with 30-inch and 40-inch diagonal AMOLEDs with the 1920×1080 format, and in order to get the competitive edge over the reported LCD TV brightness of 500 cd/m^2[5], the target brightness is chosen to be 600 cd/m^2. With the given OLED current efficiencies, the required currents can be calculated using the pixel size determined by the number of pixels and the panel size. The current requirements for both 30-inch and 40-inch HDTV are summarized in Table 1.

		R	G	B
Brightness [cd/m^2]		600		
Panel Brightness [cd/m^2]		536.0	874.9	389.0
OLED Brightness [cd/m^2]		1340.1	2183.3	97.6
Current Efficiency [cd/A]		8.4	22.0	5.6
Pixel Size [μm^2]	30-inch	115.3×345.9		
	40-inch	153.7×461.2		
Current [μA]	30-inch	6.348	3.965	6.927
	40-inch	11.284	7.048	12.312

Table 1. Current requirements for AMOLED HDTV

In addition, there are some transient characteristics we should consider. That is, within the given scanning period, a data voltage should be loaded to the pixel electrode. In our case, the scanning period is some 15.4μs at the frame frequency of 60Hz. The available

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charging time, however, is significantly reduced due to the RC delay of the column and row lines. Accordingly, transient requirements closely relate to the parasitic resistance and capacitance of the column and row lines. We obtained parasitic resistance and capacitance of those lines using the RC extraction simulator RAPHAEL [6] assuming the line width is 10μm each.

The voltage drop on the power supply (VDD) line is another consideration for voltage programmable pixel structures. Suppression of this IR drop on the VDD line needs a sufficient width. From the currents given in Table 1, we determined the VDD line widths to be 30μm and 85μm for 30-inch and 40-inch HDTV panels, respectively, to suppress the voltage drop under 2V and the vertically split VDD lines. This configuration reduces the IR drop to a fourth, since the resistance and the current on each power line are reduced to half, respectively. In the pixels with p-channel TFTs in Figure 1(a), 2V-drop on the VDD line severely degrades the brightness, because the voltage applied between the gate and the source (V_{GS}) of driving TFTs is reduced, which translates to the OLED current reduction. On the contrary, it hardly influences on the n-channel TFT pixel, because the V_{GS} is independent of the VDD line as shown in Figure 2(b), if the VDD level is set to be high enough.

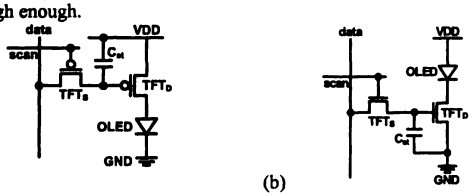


Figure 1. Basic 2-TFT-and-1Capacitor OLED pixel (a) p-channel pixel (b) n-channel pixel.

To get the minimum required mobility, we should take the maximum TFT width available in the pixel area. So, we assume the top emission type OLEDs to fully make use of the pixel area without concern about the aperture ratio. This assumption can admit the quite large VDD line widths in Table 2, where the panel parameters and parasitic resistance and capacitance are given.

Panel Diagonal Size		30-inch	40-inch
Emission Type		Top Emission	
Column Line	Width [μm]	10.48	13.97
	Resistance [kΩ]	10.074	10.074
	Capacitance [pF]	23.34	33.7
Row Line	Width [μm]	12	13
	Resistance [kΩ]	5.213	6.416
	Capacitance [pF]	164.26	248.7
VDD Line Width [μm]		31	44
Max. IR Drop [V]		1.5	1.5

Table 2. Panel parameters of AMOLED HDTV and parasitic resistance and capacitance

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BASIC 2TFT-AND-1CAPACITOR PIXEL: 2T1C PIXEL

Pixel Design

The goal of this section is to determine the minimum required mobility of the TFTs used in the basic 2T1C OLED pixel. Because the OLED is basically a current-driven device, the previous literature has focused on the driving current requirements of the driving TFT, TFT_D in Figure 1(b) [4]. However, the current capability of the switching TFT, TFT_S, is also important to adequately load the data to the pixel electrode. Therefore, we should find the minimum required mobility to meet the requirements of both TFTs, the charging ratio and the driving current.

As expressed in the current equation (1) in the saturation region, the current of a TFT is a function of many parameters. So, for a given current the required mobility can vary so much depending on the other parameters.

$$I_{TFT_D} = \frac{1}{2}\mu C_{OX}\frac{W}{L}(V_{GS} - V_{TH})^2 \qquad (1)$$

In order to obtain the minimum required mobility, we assign the whole available area of a pixel to the TFTs except the column, row and VDD lines area. The storage capacitor is formed under the VDD line. This is allowed without the aperture ratio issue, because we assume the top emission type.

When we design the width of TFT_S, we should consider two points: the charging ratio and the switching error coined ΔV_P. Although the width should be large enough to charge the pixel electrode, the large width leads to the large switching error. So, we should find the right width range to meet the both requirements. Anyhow, because the perfect elimination of the switching error is impossible, we sized the width of TFT_S with the parameter of ΔV_P. The remaining area is fully assigned for TFT_D.

The nominal row line time is given 15.4μs for the full-specification HDTV at the frame rate of 60Hz, but the practical row line time is significantly reduced by the RC delay due to the parasitic resistance and capacitance. The same sort of delay occurs on the column line, too. In addition, the data loading on the column line is also limited by the slew-rate of the column driver circuit. When we check the charging characteristics, all of these factors should be considered. Figure 2 illustrates the panel modeling, where we employ the π-3 model for the column and the row lines.

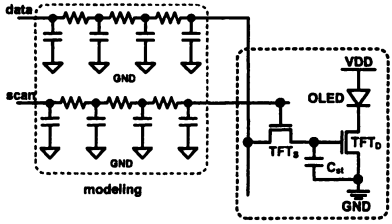


Figure 2. Panel modeling including parasitic resistance and capacitance.

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The widths of TFTs are determined above, but the current is still a function of V_{GS} and V_{TH}. The higher V_{GS} we can apply to the TFT_D, the lower mobility is required for the given current in Table 1. But, the applicable V_{GS} is limited by the VDD level and the OLED characteristics. In Figure 3, suppose that the drain voltage of TFT_D is V_{DS}, its drain current is I_{DS} and the V_{EL} is applied to the OLED. Because the OLED acts as a load for TFT_D, the V_{DS}-I_{DS} curves can be drawn with the OLED I_D-V_{EL} curve as a load line. In order to get the stable current irrespective of the drain voltage, TFT_D should operate in the saturation region. Because the V_{GS} higher than V_{DS} plus V_{TH} puts TFT_D into the triode region, the V_{GS} should be limited under the level. The V_{DS} is determined using the given VDD level and the V_{EL}, and we use the V_{TH} as a simulation parameter.

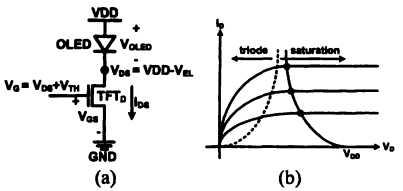


Figure 3. (a) Pixel circuit consisting of driving TFT and OLED (b) TFT I_{DS}-V_{DS} curves with the load line.

Simulation Conditions

Table 3 summarizes the electrical parameters we assume for these simulations. Although a higher Von voltage for a selected row enhances the charging characteristics of TFT_S, it also induces a higher switching error. So, raising the Von for enhancing the charging characteristics is not a good choice. The VDD and the slew-rate of the column are assumed to have typical values. The parasitic capacitors and resistance given in Table 2 might cause longer RC delays than the values in Table 2, but the simulated RC delay is quite reduced due to the distributed nature.

Von of row line [V]		20
VDD [V]		15
Slew-rate of column driver [V/μs]		2.5
Charging ratio [%]		99
Storage capacitor [pF]	30-inch	1.5
	40-inch	2.5

Table 3. Electrical parameters of 30-inch and 40-inch AMOLED panel.

Simulation Results and Discussions

Figure 4 plots the required mobility for TFT_D and TFT_S respectively for the 30-inch HDTV as a function of V_{GS}. The V_{GS} is the gate voltage of TFT_D for the maximum

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current, that is, blue pixel current for the target brightness in Table 1. In Figure 3, the VDD is 15V, the maximum OLED voltage is 6V in our case, and the IR drop on the VDD line is 1.5V in Table 2. So, the maximum permitted drain voltage of TFT_D is set to be 7V with some margin. Since the gate voltage is allowed to $V_{DS} + V_{TH}$, the V_{GS} is 8V here. As expected, the required mobility for TFT_D is dramatically reduced with the V_{GS}. On the contrary, the required mobility for TFT_S increases with the V_{GS}, because the V_{GS} of TFT_S gets smaller as the V_{GS} of TFT_D increases. Another point is that if we can tolerate a larger switching error, we can enlarge the W_S. This means the required mobility for TFT_S can be relaxed. In Figure 4, when the switching error of 100mV is tolerable, the mobility to meet the requirements of both TFTs is found at about 1.65cm^2/V-s that is determined by the switching TFT requirement, and it drops to about 1.22cm^2/V-s and about 0.96cm^2/V-s, as the switching error moves up to 150mV and 200mV. From Figure 4 (b) and (c), it is found that the required mobility gets higher with the V_{TH}. It is chiefly because the current capability of TFT_S is lowered at the same gate voltage. For TFT_D, the V_{TH} has little influence on the required mobility, since the higher V_{GS} is allowed as the V_{TH} increases so that the $V_{GS} - V_{TH}$ is maintained. Figure 4(d) shows the required mobility of 30-in panel when $V_{TH} = 9V$ for long term stressed α-Si TFT pixel structures.

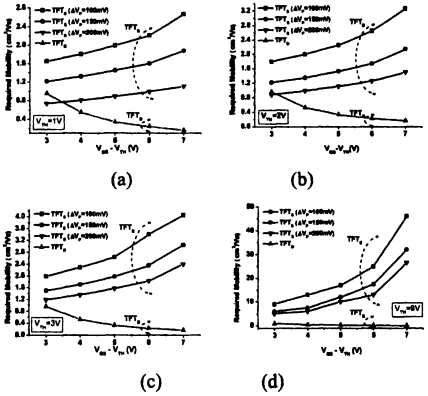


Figure 4. Required mobility of TFT_D and TFT_S of 2T1C pixel as a function of V_{GS} for 30-inch AMOLED HDTV (a) $V_{TH} = 1V$, (b) $V_{TH} = 2V$, (c) $V_{TH} = 3V$ and (d) $V_{TH} = 9V$.

Figure 5 plots the required mobility for TFT_D and TFT_S respectively for the 40-inch HDTV as a function of V_{GS}. If the switching error of 100mV is tolerable, the mobility to meet the requirements of both TFTs is found at about 1.35cm^2/V-s that is determined by the switching TFT requirement, and it drops to about 0.80cm^2/V-s and about 0.65cm^2/V-s, as the switching error moves up to 150mV and 200mV. Note that the required mobility for 40-inch panel is lower than that of 30-inch panel. This is because for the 40-inch panel, storage capacitor size is larger than that of 30-inch panel. Thus, the size of switching TFT of 40-inch panel is larger than that of 30-inch panel, this cause the phenomenon. As shown in Figure 4 and 5, the required mobility is limited by the

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switching TFT because of charging time and ΔV_P limitation. If we compensate the ΔV_P in the video data signal processing, the required mobility can be reduced in the 2T1C pixel structure.

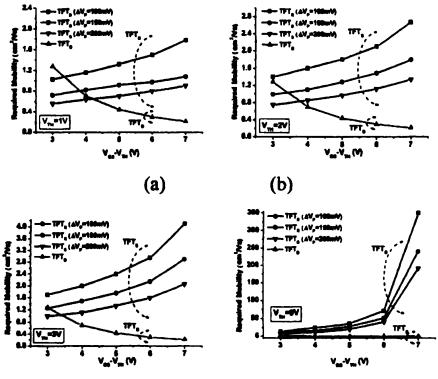


Figure 5. Required mobility of TFT_D and TFT_S of 2T1C pixel as a function of V_{GS} for 40-inch AMOLED HDTV (a) V_{TH} = 1V, (b) V_{TH} = 2V, (c) V_{TH} = 3V and (d) V_{TH} = 9V.

As we can be seen equation (1), the pixel current is very sensitive to V_{TH} variations, which results in the non-uniformity of the picture throughout the panel. To resolve this problem, pixel circuit-level V_{TH} compensation approaches have been tried [7-10]. Section 4 will determine the required mobility for an example pixel circuit.

V_{TH} -COMPENSATED PIXEL

To resolve the non-uniformity problem mainly due to the V_{TH} variations, various pixel circuits have been proposed [7-10] Most of those pixel circuits are composed of 4 or 5 TFTs and 1 or 2 capacitors, so that the circuit is more complicated than the 2T1C pixel, and each TFT size has to be smaller. This means the required mobility necessarily gets higher. Among various pixel circuits, we choose the pixel circuit shown in Figure 6 as an example and determine the required mobility.

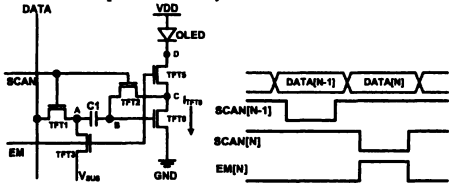


Figure 6. Pixel circuit composed of 5 TFTs and 1 capacitor and timing diagram for compensating the V_{TH} variations.

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Operation Principle

When a row is scanned, TFT1 and TFT2 are turned on, and TFT3 and TFT5 are turned off. Through TFT1, node A is charged to a data voltage V_{DATA}, and the voltage of node B is set to V_{TH} of TFT0. At the end of the row line time TFT1 and TFT2 are turned off, and TFT3 and TFT5 are turned on, when node A voltage is changed to V-S_{US}, and node B voltage is also changed, because node B is floating at the moment. If the voltage level of V-S_{US} is equal to VDD, and the ratio of capacitor C1 and the gate capacitance of TFT0 is 5:1, the voltage of node B, V_B, is expressed in equation (2)

$$V_B = V_{TH} + \frac{5}{6}(VDD - V_{DATA}). \qquad (2)$$

Consequently, if TFT0 operates in the saturation region, the pixel current I_{TFT0} is obtained by equation (3)

$$\begin{aligned} I_{TFT0} &= \frac{1}{2}\mu C_{OX}\frac{W}{L}(V_B - V_{TH})^2 \\ &= \frac{1}{2}\mu C_{OX}\frac{W}{L}(V_{TH} + \frac{5}{6}(VDD - V_{DATA}) - V_{TH})^2 \\ &= \frac{25}{72}\mu C_{OX}\frac{W}{L}(VDD - V_{DATA})^2 \end{aligned} \qquad (3)$$

Note that there is no V_{TH} term in the current equation (3), which means that the pixel current is determined independently of the V_{TH} variations. Also, VDD in equation (3) is just the voltage level, not the power supply voltage, so the pixel current is not influenced by the IR drop on the power supply line, either.

Pixel Design

Node A in Figure 6 never gets floating, because the node is always biased by V_{DATA} or V-S_{US} through TFT2 or TFT3. Therefore, we can adequately size TFT2 and TFT3 for the charging capability without concern about the switching error. This feature of the pixel circuit allows the capacitor C1 to be reduced compared to the 2T1C pixel circuit. In addition, TFT2 need not charge the gate capacitance of TFT0 unlike the 2T1C pixel circuit. Both of these facts enhance the charging characteristics for node A. So, the mobility requirement does not appear to be determined by both of the switching TFT and the driving TFT, but comes from the driving TFT only.

The V_{TH} compensation of this pixel circuit can be achieved only when TFT0 operate in the saturation region. To make sure to put TFT0 into the saturation region, TFT0 and TFT5 are carefully sized and biased. Because TFT5 is used as a switch, it operates in the triode region, so the current I_{TFT5} can be expressed in equation (4)

$$\begin{aligned} I_{TFT5} &= \mu C_{OX}(\frac{W}{L})_5\{(V_{GS5} - V_{TH})V_{DS5} - \frac{1}{2}V^2_{DS5}\} \\ &= \mu C_{OX}(\frac{W}{L})_5\{(V_{EM} - V_C - V_{TH})(V_D - V_C) - \frac{1}{2}(V_D - V_C)^2\} \end{aligned} \qquad (4)$$

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where V_{EM} is the EM signal voltage in Figure 6, V_C and V_D are the voltages of node C and node D, respectively. In our case, the OLED voltage is 6V, VDD is 15V, V_{EM} is 20V and V_{TH} is assumed to be 1V, so that the equation (4) can be rewritten in equation (5) as a function of only the TFT size and Vc.

$$I_{TFT5} = \mu C_{ox}(\frac{W}{L})_5\{(19-V_C)(9-V_C)-\frac{1}{2}(9-V_C)^2\}. \quad (5)$$

On the other hand, the current of TFT0 is expressed in equation (6)

$$I_{TFT0} = \frac{1}{2}\mu C_{ox}(\frac{W}{L})_0(V_{GS0}-V_{TH})^2 \quad (6)$$

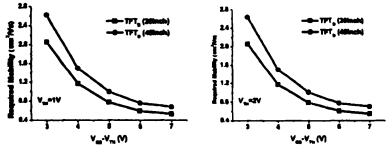
To make sure that TFT0 operates in the saturation region, the gate voltage of TFT0 can be biased up to $V_C + V_{TH}$. Substituting $V_C + V_{TH}$ into V_{GS0} in equation (6), the current is rewritten in equation (7) as a function of only the size and Vc.

$$I_{TFT0} = \frac{1}{2}\mu C_{ox}(\frac{W}{L})_0 V_C^2 \quad (7)$$

By equating equations (5) and (7), we can size TFT0 and TFT5 as a function of V_C. For example, if we intend to apply 8V to the gate of TFT0, V_C should be 7V or higher (assuming V_{TH} =1V), and $(W/L)_5/(W/L)_0$ should be 22/24.5 or larger. Of course, the actual current equation has some deviations from equations (4) and (6), the right sizes should be found by SPICE simulations [11].

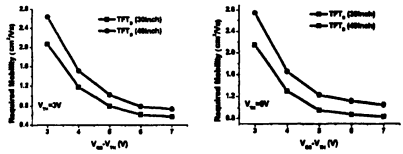
Simulation Results and Discussions

The operating conditions of the 5T1C pixel circuit are different from those of the 2T1C pixel. As explained in Section 4.2, the widths of TFT5 and TFT0 should vary according to V_C. The example in Section 4.2 is the case where V_{DS} of TFT5 is 2V. If we increase V_{DS} of TFT5, the width of TFT5 can be smaller, because the larger V_{DS} and V_{DS} are given to TFT5 for the current (recall that TFT5 operates in the triode region), and the larger width is allowed for TFT0 by the amount TFT5 width gets smaller. Note that the gate voltage of TFT5 should be lowered to operate in the saturation region as V_C is lowered. In brief, the gate voltage of TFT5 should be lowered by V_{DS} of TFT5.



(a) (b)

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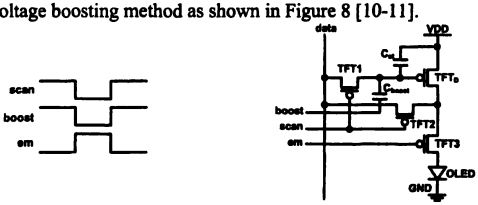
(c) (d)

Figure 7. Required mobility of 5T1C pixel as a function of V_{GS} for 30-inch and 40-inch AMOLED HDTV (a) V_{TH} = 1V, (b) V_{TH} = 2V, (c) V_{TH} = 3V and (d) V_{TH} = 9V.

Figure 7 plots the required mobility for 30-inch and 40-inch diagonal HDTV. Surprisingly, when the TFT V_{TH} = 3V, the minimum required mobility of 30-inch and 40-inch panels is just 0.57cm^2/V-s and 0.73cm^2/V-s, respectively, which are lower than those of 2T1C pixel. Although the threshold voltage of pixel TFTs increases up to 9V, the minimum mobility is quite low as shown in Figure 7(d). We expected the 5T1C pixel circuit is more complicated, so the driving TFT width can take smaller area, resulting in higher mobility. However, in reality, the minimum required mobility of the 2T1C pixel does not stem from the driving TFT, but from the switching TFT. Whereas the width of the switching TFT of the 2T1C pixel is limited, being afraid of the switching error, the 5T1C pixel is free from the switching error as explained in Section 4.2. So, we can adequately size the switching TFT for the pixel charging, and the mobility requirement only comes form the driving TFT. We can find in Figure 4 and Figure 5, the required mobility for the driving TFT is quite low even in the 2T1C pixel.

CURRENT PROGRAMMING PIXEL

To solve the non-uniformity problem of panel caused by caused by non-uniformities of TFT and supply voltage, current programming pixel structure can be considered. But the major problem of current programming pixel structures for large size panel is that programming time is much longer than line time. In order to solve this problem, current programming pixel structure with voltage pre-charging method is proposed [10-11]. The use of voltage pre-charging method in current programming pixel structures is not enough to program within line time for large size panel using reasonable program current level. In this paper, we chose the current programming pixel structure with voltage pre-charging and voltage boosting method as shown in Figure 8 [10-11].



(a) (b)

Figure 8(a) current programmable pixel circuit composed of 4 TFTs and 2 capacitors and (b) timing diagram.

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Operation Principle

The gate voltage, which compensates non-uniformity of of TFT_D, is programmed at Cst by the data current. After the charging the parasitic capacitance of data lines during row line time, a large amount of current of TFT_D is scaled down by the coupling effect of C_{boost}. The major drawback of this pixel circuit is that there is the non-uniformity problem caused by the difference of mobility and threshold voltage of TFT_D during current scaling time [10-11]. Because the parasitic capacitance of data line is getting larger as the size of panel is getting larger, a large amount of data current is required for current programming method without voltage pre-charging. This increases the power consumption and make hard to use this structure at large size panel. As the result, pre-charging of data line by voltage is used in this paper because reasonably small amount of current is required after the pre-charging.

Pixel Design and Simulation Results

Poly-Si TFT devices are used for pixel circuits because the minimum mobility should be higher than $1cm^2/V\text{-}s$. The simulation conditions are summarized in Table 4. Several assumptions are required to find the minimum required mobility and reasonable pixel design. Bottom emission type pixel is assumed and the aperture ratio of pixel is greater than 35%. The amount of minimum current for charging the storage capacitance after the pre-charging of data line is assumed 1μA. As shown Table 4, we assumed that the data and scan line widths are assumed 10μm. So the parasitic capacitance of data lines for 30-inch and 40-inch is same because the parasitic capacitance is mainly caused by overlap capacitance between the data line and scan lines. The case of 20μm and 10μm of channel length of both TFT_D and TFT2, which are located at the programming current path, and the case of 2V and 3V of threshold voltage are simulated. The minimum required mobility to charge the remaining amount of voltage after the pre-charging is the function of the width of TFT_D and TFT2.

		30-inch	40-inch
Emission Type		Bottom Emission	
Column Line	Width [μm]	10	10
	Resistance [KΩ]	10.557	14.076
	Capacitance [pF]	55.69	55.69
Row Line	Width [μm]	10	10
	Resistance [KΩ]	6.256	8.342
	Capacitance [pF]	99	132
Supply Voltage [V]		18	19.5
VDD Line Width [μm]		20	30
Max. IR Drop [V]		2.6	4.1

Table 4. Electrical parameters of 30-inch and 40-inch AMOLED panel.

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Figure 9 shows the simulation result, while the V_{SG} of TFT_D is greater than threshold voltage and this size TFT_D supply the current of 1LSB to OLED. As the result of simulation, the minimum required mobility is 19cm^2/V-s and 21cm^2/V-s at the case of 2V and 3V of V_{TH}, respectively, while the size of TFT_D and TFT2 is 30μm/10μm.

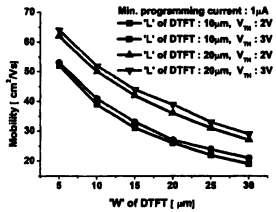


Figure 9. Required mobility of 4T2C pixel as a function of W_{TFTD} for 30-inch and 40-inch AMOLED HDTV

CONCLUSIONS

We investigated the TFT mobility requirements of three kinds of pixels for 30-inch and 40-inch diagonal full-specification (1920×1080) AMOLED HDTV with a basic 2TFT-and-1Capacitor (2T1C) pixel, a 5TFT-and -1Capacitor (5T1C) voltage programmable pixel proposed for compensating the V_{TH} variations and a 4TFT-and-2Capacitor (4T2C) current programmable pixel with voltage pre-charging and voltage boosting. For the 2T1C pixel, the required mobility gets higher due to the switching TFT, because the width of the switching TFT is limited with concern about the switching error. However, because the 5T1C pixel has the switching error-free structure, the mobility requirement is only attributed to the driving TFT, so that the required mobility is lower than that of the 2T1C. Through SPICE simulations reveal that the TFT mobility for 30-inch and 40-inch HDTV is 1.65cm^2/V-s and 1.35cm^2/V-s respectively for the 2T1C pixel with V_{TH} = 3V. The 40-inch AMOLED HDTV has the lower mobility requirement, because it has to use larger switching TFT. For the 5T1C pixel, the required mobility is 0.57cm^2/V-s and 0.73cm^2/V-s for 30-inch and 40-inch AMOLED HDTV panels with V_{TH} = 3V, respectively. Although the threshold voltage of pixel TFTs increases up to 9V, the minimum mobility is 0.83cm^2/V-s and 1.00cm^2/V-s for 30-inch and 40-inch AMOLED HDTV panels, respectively. Therefore, 30-inch and 40-inch AMOLED HDTV panel with 5T1C voltage programmable pixel structure can be implemented using α-Si TFT technology.

The minimum TFT mobility of 30~40inch HDTV with the current programmable pixel structure for driving TFT sizes of 30μm/10μm with V_{TH} = 2V and 30μm/10μm with V_{TH} = 3V is 19cm^2/V-s and 21cm^2/V-s, respectively. These minimum mobility may be the minimum mobility requirements for 30-inch and 40-inch HDTV panels with current programmable pixel structures for the case of driving TFT's threshold voltage variation of within 0.5V.

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SYSTEM DISPLAYS, TFT DEVICE AND PROCESS TECHNOLOGIES

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The evolution of wireless networks has stimulated advances in personal mobile information interfaces. The need for system displays that incorporate sophisticated human-friendly interfaces is widely recognized. The system display of the future will be a combination of a pixel array and an integrated system on the substrate. To provide platform for such systems, advances to be made in MACRO cell libraries and sub-micrometer TFT process technology are essential. Similar advances in device and process technologies are also important stepping stones.

SYSTEM DISPLAY

The system display is an innovative concept for next-generation, human-friendly displays where information-processing functions will be integrated within a glass substrate together with pixel arrays. Data processing capabilities, such as decoding and DA conversion, have already been integrated within the panel to enable very high resolution and area-effective displays. Such system displays are now widely used in color cellular phones and PDAs. Further integration is expected to accelerate over the next several years. Figures 1 and 2, respectively, show the trends in information network evolution and the technical path toward fully integrated system displays.

Application domains for system displays will be enormously wide and diverse. For example, an ultra-thin card-type viewer having wireless communication, image processing, and biometric identification functions, as well as very high resolution, will appear as an advanced replacement for credit cards.

SYSTEM DESIGN AND CELL LIBRARY

The wide variety of system functions needed for such applications means that functions integrated on the panel will have to be designed more systematically using higher level system description language. For this purpose, a library of standard cells to perform element logic functions (such as NOR, NAND, D-Flip-Flop, and SRAM functions) will have to be developed. Each cell can be described as a set of information regarding, for example, logical behavior, speed, dissipation power, mask layout, or process conditions (Fig. 3).

TFTs and MACRO cells are formed in position-controlled crystallized semiconductor areas on a substrate. The crystallized areas are formed as an array and are located periodically at a predetermined position. TFTs are formed after a series of lithography and etching steps, which include isolation, contact, and metallization. Patterning is carried out in alignment with the crystallized areas (Fig. 4). Periodic placement of the

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crystallized areas ensures precise alignment so that the channel region is formed of single-crystal Si. This leads to high mobility for high current drivability, reduced V_{th} scattering, and low p-n junction leakage for a long retention time.

Figure 5 shows how the R&D related to the system display should be carried out.

TFT AND KEY PROCESS

TFTs fabricated on a glass substrate are key components of system displays. TFTs with submicron feature sizes and high mobility of about 500 cm^2/Vs are fast and have a high drivability sufficient for clock frequencies above 100 MHz. The development of TFT technology is closely linked to advances in materials science and technology integration.

Crystallization

TFTs are fabricated with a crystallized Si layer on the panel. The size of the crystallized area has to be large enough to accommodate several submicron CMOS devices within it. To form large crystallized areas at any predetermined position, phase-modulated excimer laser annealing (PMELA) appears to be the only currently available technology. The PMELA system is composed of an excimer laser, illumination optics including homogenizer and condenser lenses, a phase modulator, projection optics, and a substrate stage. The system has three principal parameters, the coherent factor σ, the phase difference θ, and the point spread function of the projection optics. Position-controlled array growth is achieved with a pair of phase modulators. The modulator pair produces a combined light profile containing a steadily varying slope profile and a narrow dip line profile. The cross point of the two profiles is the minimal point of the light intensity, which is the nucleation point from which lateral growth starts. By placing the modulator pair precisely with respect to the projection optics, we can fix the position of the crystallized areas relative to the light axis of the projection optics. Thus, two-dimensionally controlled crystallization takes place (Fig.6).

This technology is explained in further detail elsewhere at this conference.

Gate Insulator

With the TFT gate length reduced to the submicron range, we need a gate insulator layer as thin as 30 nm with a low interface state density. We have developed a stacked gate insulator as a thin gate dielectric (about 30 nm thick) to get high current drivability for the TFTs. The stacked insulator is composed of oxidized silicon and deposited silicon dioxide. A low interface state density is enabled by the clean semiconductor-dielectric interface formed between the Si and oxidized SiO_2. High-resolution TEM has shown that the interface, formed by radical oxidation using microwave-enhanced oxygen plasma, has atomic level flatness. The leakage current characteristics of the stacked gate, formed at a 300°C substrate temperature, are as good as those of a thermally grown oxide. Microwave-plasma-enhanced CVD makes it possible to form a high quality

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insulator, while keeping the maximum process temperature no higher than 300°C.

ACKNOWLEDGEMENTS

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FIGURES

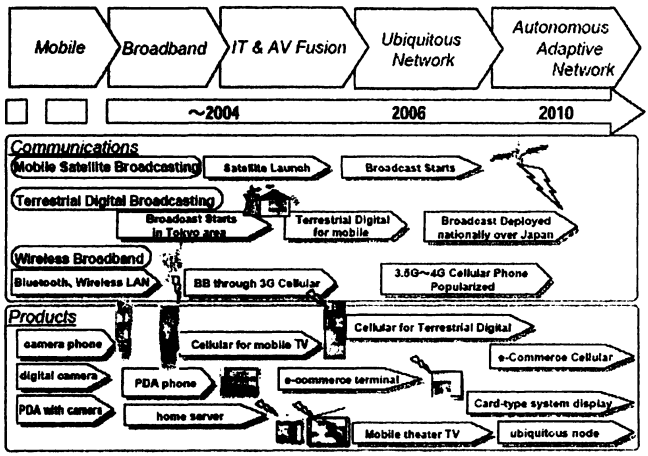


Fig.1 Information Network Evolution

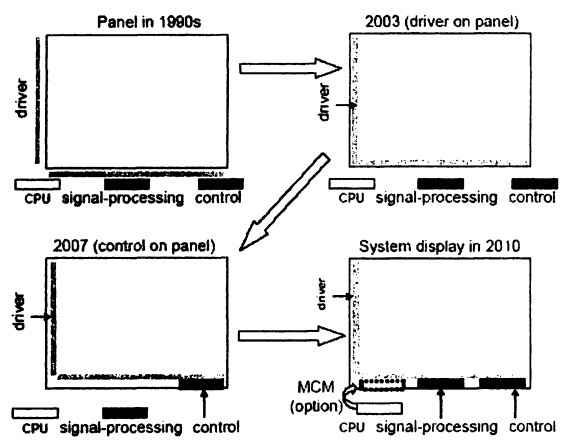


Fig.2 From Image Panel to System Display

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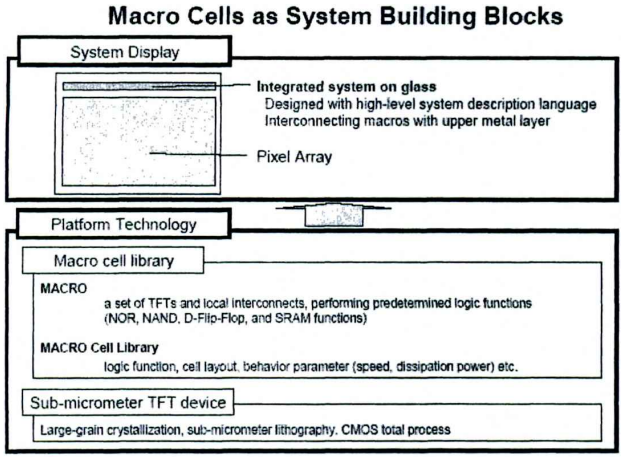


Fig.3 Macro Cells as System Building Block

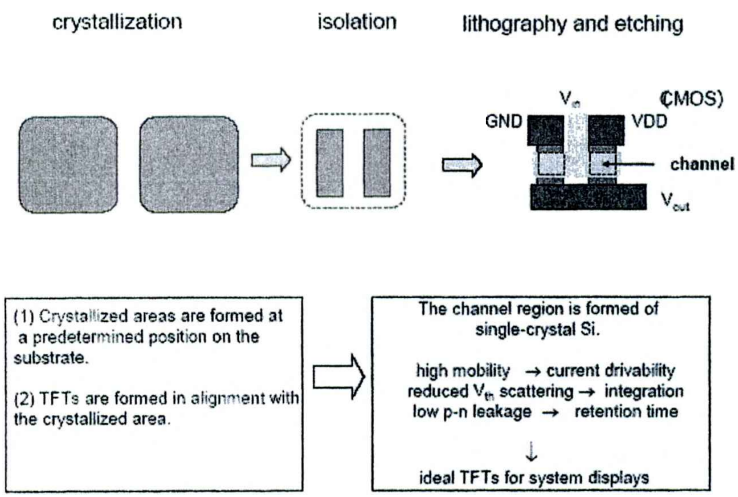


Fig.4 Position-controlled crystallization and lithography

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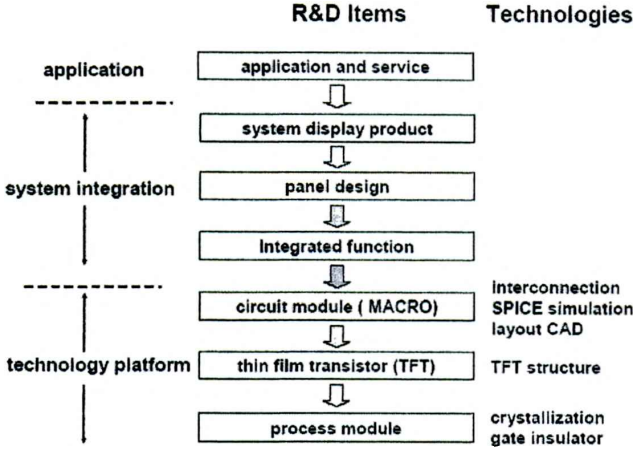
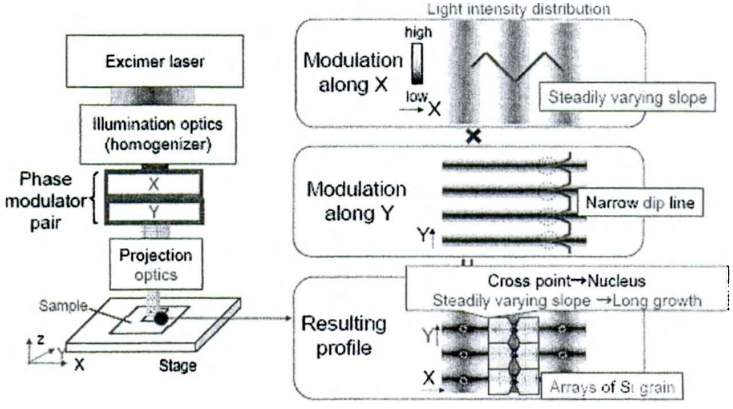


Fig.5 R&D on System Displays



By using a modulator pair, a nearly ideal light intensity is obtained.

Fig.6 Position-controlled array growth using a phase modulator pair

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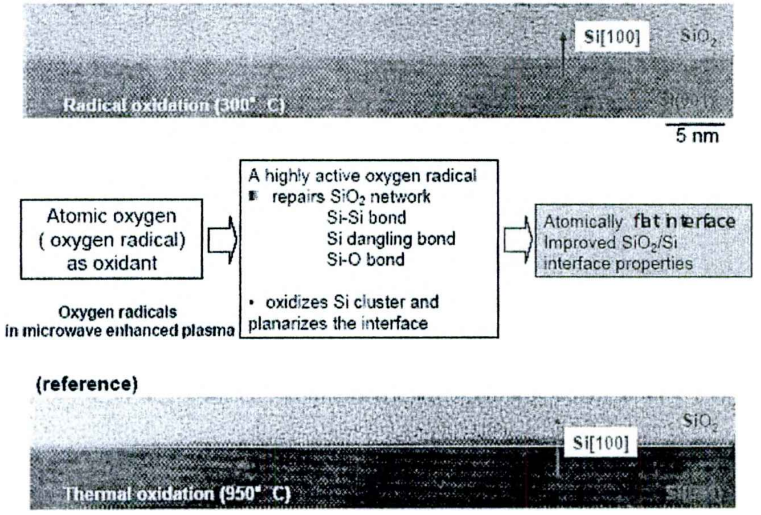


Fig.7 HR-TEM image of a Si/SiO_2 interface

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HIGH PERFORMANCE TFT CIRCUITS FOR ALL-INTEGRATED SYSTEMS ON STAINLESS STEEL FOILS

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ABSTRACT

In an attempt to fabricate all inclusive systems we are presenting a study on several elements that would be used as building blocks for all-on-board integrated applications on stainless steel foils. These systems would include in the same substrate all or many of the components of a modern day electronic device such as PDA or cellular phone. We are reporting results on both digital and analog circuits on stainless steel foils. An extensive study on shift registers running at speeds greater than 1.0MHz is shown as well as oscillators operating at over 40 Mhz. Pixel circuits for driving organic light emitting diodes are presented as well as experimental OLED's on the same steel material substrate. The device technology of choice is that based on poly-silicon TFT technology as it has the potential of producing circuits with good performance and considerable cost savings over the established processes on quartz or glass substrates (amorphous Silicon a-Si:H or silicon on Insulator SOI).

1. INTRODUCTION

During the past decade, there has been an increased research and development effort towards the realization of highly integrated large area electronics, on flexible substrates. The main application targeted is displays and other matrix-based electronics, with focus on a systems-based approach. The appeal of flexible electronics lies in their capacity to realize novel circuits whose space / layout and mechanical restrictions do not permit the use of a rigid printed circuit board, and to utilize a roll-to-roll manufacturing process similar to a rolling photolithographic printing process, which can produce this type of circuits with a throughput 10-100 times higher than normal semiconductor processing.
Displays are the preferred flexible electronic application because of the mechanical (robust, lightweight) and space saving advantages a conformal or foldable display has, and also because the specifications for pixel electronics such as thin film transistor (TFT) switches and current sources are relatively relaxed, compared to other high speed digital / analog electronics. However, a larger degree of system integration requires the incorporation of high performance digital and analog circuits for display driving and signal processing. A higher integration scale is highly desirable, because it is shown to increase system yield, since external connections - which are a substantial source of failure - are greatly reduced, and substantially decrease manufacturing costs.

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The fabrication of highly integrated large area systems on flexible substrates with reasonable performance characteristics is - at this time - possible only with polysilicon. The high carrier mobility values that can be obtained with this approach, and the prospect of realizing highly efficient, low power CMOS circuitry are the two strongest assets of polysilicon TFT technology.

In order to realize monolithic flexible circuits, where all components are fabricated with the same process sequence on the substrate material, two distinct substrate materials can be used: *(a)* plastics and *(b)* thin metal foils. Other substrates, such as thin glass sheets, although flexible are still brittle and thus not suitable with the possible exception of use in specialized applications. The use of plastic substrates involves some serious issues, primarily spurring from the severely reduced thermal budged that can be tolerated. In this case, processing temperature should not be higher than about 200°C, and an ongoing effort is made to limit it in the 100°C - 150°C range. This is considerably lower than the approximate 400°C limit observed in low temperature polysilicon processing (LTPS) on glass substrates (such as Corning® 1737). An impact in device and circuit performance is usually observed from lowering temperatures in critical steps such as gate dielectric formation and contact anneal.

Good quality polysilicon TFTs have been fabricated on plastic substrates from the mid-1990s on [1]. This has been made possible in part by the continuous optimization of excimer laser crystallization equipment, which is the most suitable way of obtaining high mobility TFTs on plastics, where the thermal budget is severely constrained. Keeping processing temperatures at a maximum of 150°C, polysilicon TFTs with effective mobility values in the region of 60cm^2/Vs have been fabricated on polyester substrates [2]. Higher quality devices (effective pmos mobility values around 170cm^2/Vs and I_{ON}/I_{OFF} ratios of 10^8) have been realized utilizing novel transfer processes from high temperature compatible, temporary substrates to permanent flexible ones [3,4].

Metal foils are largely immune to the problems affecting plastic substrates; stainless steel foils –for example– can tolerate temperatures above 1000°C, offering at the same time excellent resistance to corrosion and chemical attack and no water or oxygen absorption. During the late 1990s, excimer laser crystallization was used to produce high mobility (>100cm^2/Vs) thin film transistors on steel foils for the first time [5]. Other crystallization approaches such as furnace annealing have also been utilized, but with significantly lower returns in device performance [6,7]. Progress has continued in the field, resulting in devices with mobility values higher than 200cm^2/Vs and the fabrication of functional digital circuits for the first time on metal foils [8,9]. From the application viewpoint, thin metal foils have been recently utilized in the fabrication of active-matrix, a-Si TFT digital ink displays [10].

On this paper, we are presenting high-speed polycrystalline silicon thin film transistor digital circuits as well as all the elements needed for the fabrication of a display, representing some of the building blocks for such integrated systems. Both n-channel and p-channel excimer laser re-crystallized poly-silicon devices with effective mobility values in the region of 250cm2/Vs and 100cm2/Vs respectively, and ON vs. OFF current ratios at least seven orders of magnitude have been fabricated, and their characteristics are presented. Ring oscillators running at frequencies above 40MHz are described, along with static and dynamic shift registers, with maximum clock frequency exceeding 1.0MHz. The presented results indicate the potential of these circuits for possible row and column driving for displays or memory addressing. This paper outlines the fabrication and the performance of the above mentioned circuits first, followed by pixels circuits next, and finally the Organic Light Emitting Diodes (OLED's).

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2. HIGH PERFORMANCE CIRCUITS

2.1 Circuit Fabrication

Type-304 Stainless steel foils, 100μm thick, were manually and chemically polished and cut to 100mm diameter wafer size substrates. The manual and chemical polishing step was developed and used in order to reduce the surface roughness of the untreated foils, which approached 1500Å. After polishing, an RMS value of surface roughness approaching 100Å was obtained.

After cleaning, the substrates were coated with an isolation layer of PECVD SiO_2, 750nm thick. The active amorphous Si film was PECVD deposited, crystallized with an Excimer Laser and patterned to form the TFT islands, 1000Å thick. The gate dielectric was PECVD silicon dioxide 1000Å thick, followed by a PECVD a-Si layer for the gate electrode. After these depositions, the gate electrode was n+ ion implanted and patterned, followed by the patterning of the gate dielectric and the drain / source region formation through p+ (BF_2) or n+ (P) ion implantation.

The drain and source TFT regions and poly-Si inter-connects were silicided using sputtered Ni and an in situ anneal at 400°C. A passivation oxide layer 3000Å thick was PECVD deposited and followed by the patterning of contact holes. In order to avoid aluminum hillocks that can lead to circuit failure, AlNi was selected as the most suitable metalization layer for this purpose. Aluminum and nickel were sputtered to a total thickness of 3000Å, then annealed in situ to form the alloy. After patterning the metal, the devices and circuits were measured.

2.2 Circuit Performance

Stand alone devices of various geometries were fabricated and tested, and their electrical characteristics are presented below. The minimum fabricated channel length was 2μm (minimum feature size). Figure 1 shows the I_{DS}/V_{GS} characteristics of two devices, taken at $|V_{DS}| = 0.1V$ and 1.1V. Stand alone p- and n-type devices were measured, and their basic characteristics were recorded. Table 1 shows the average values of mobility, threshold voltage, inverse sub-threshold slope and off current for both types of gate oxide TFTs. For all devices, there is a difference between Id(ON) and Id(OFF) at least six orders of magnitude, which is one of the highest compared with previously published results.

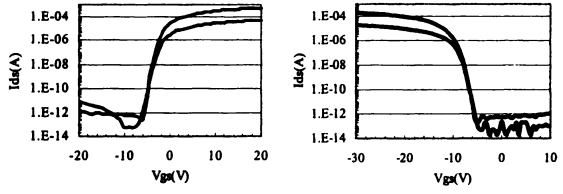


Fig. 1: Typical characteristics of PECVD oxide NMOS and PMOS devices at Vds=0.iV and 1.1V (W/L=20/4)

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Gate Oxide	Device (W/L=20/4)	Mobility (cm^2/Vs)	Vt (V)	SS (V/dec)	Ioff (A)
PECVD	NMOS	200	+1.4	1.4	1 pA
	PMOS	87	-9.8	2.4	0.1 pA

Table 1: Average values of PMOS and NMOS TFTs

A basic circuit for the evaluation of digital circuit performance is a ring oscillator (RO). The oscillators we have fabricated are composed of 19 CMOS inverter stages, and have buffered outputs. Both NMOS and PMOS devices have the same geometry 20μm/4μm. Figure 2 shows the RO frequency as a function of supply voltage. Powered with a supply voltage of 15V, its free running frequency was measured to be approximately 40.4MHz. This results in an average delay time of 1.302ns per inverter stage.

Architecture	f_{min} (kHz)	f_{max} (MHz)
Static	<10Hz	2.50
Dynamic	500Hz	1.50

Table 2: Min. and max. speeds of SR's on steel vs. supply voltage

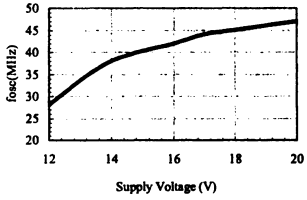


Fig. 2: Free-running frequency of RO

One of the most important memory and display driver circuits (for both active- and passive-matrix displays) is a shift register. Assuming the simplest driving scheme, the rows and the columns of the display matrix are activated one at a time, which is accomplished by the active shift register output (which can be high or a low signal) being shifted to the next bit, and eventually cycled to the register's input again.
Two types of shift registers have been designed and evaluated: a static, D-type latch-based design and a dynamic pass-gate gate design. Both are 10-bit, serial input, parallel output designs. Both are based on the clocked CMOS (C^2MOS) logic architecture, which uses a non-overlapping pseudo two-phase clock signal for shift timing. The circuit schematics are shown in Figure 3; labels indicate the W/L ratios of the TFTs.

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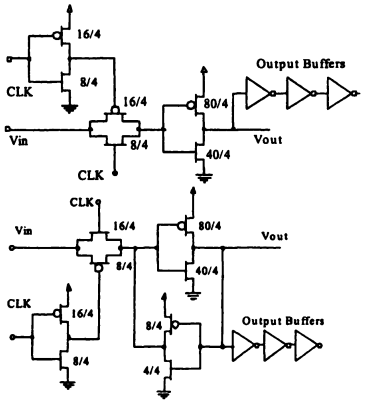


Fig. 3: One-half bit stage schematics of the fabricated dynamic (left) and static (right) shift registers.

The maximum clock frequency of a shift register (defined as the maximum frequency for bit error-free operation) depends on the register's propagation delay and, as such, is a function of device characteristics (effective mobility, threshold voltage), device geometry (primarily channel length) and operation conditions (supply voltage, clock signal levels) [11]. In order to design a register circuit for maximum performance, the effect of the parasitic capacitance to the conductive substrate should also be taken into account; we have shown that this parasitic capacitance is detrimental to circuit performance if the electrical isolation dielectric deposited on the substrate is not thick enough [12].

As a simple design rule, we consider a simple CMOS inverter, with device geometries W_p and W_n (PMOS and NMOS, respectively), channel length L and oxide capacitance C_{ox}. The propagation delay of the inverter can be approximated to a first degree as an RC product, where the capacitive term is the sum of the inverter's output capacitance, plus any load capacitance seen at the output. Assuming that an identical inverter is driven by the first one, we can express the capacitive term of the delay as follows:

$$C \approx \tfrac{1}{2}LC_{ox}(W_p + W_n) + \tfrac{3}{2}LC_{ox}(W_p + W_n) + C_p \qquad (1)$$

where the first and the second terms of the sum represent the output capacitance of the first inverter and the input capacitance of the inverter it drives, respectively. C_p is the parasitic capacitance to the substrate, seen at the output of the first inverter. In order to figure out a suitable isolation dielectric thickness, we require that the parasitic term be negligible compared to the inherent capacitive terms, i.e.

$$C_p = \frac{\varepsilon_0 \varepsilon_d}{t_d} A << 6W_n LC_{ox} \Rightarrow$$
$$t_d >> \frac{\varepsilon_0 \varepsilon_d}{6W_n LC_{ox}} A \qquad (2)$$

where ε_d and t_d are the relative permittivity and the thickness of the isolation dielectric

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layer, respectively, and A is the area of the conductive interconnects (metal / polysilicon) from the first to the second inverter. It is assumed that scaled inverters are used (i.e. $W_p = 2W_n$). It should be noted that C_p depends on the surface roughness, too, and it may deviate significantly form the parallel-plate capacitor formula of (2) for rough substrates. Table 2 shows the maximum and minimum operational frequency of the fabricated dynamic and static shift registers, measured at a supply voltage of 14V. Note that both of these designs could be successfully used for both column and row driver realizations in low to medium resolution active matrix array. The dc power consumption at the maximum frequency was approximately 52mW for the dynamic, and 70mW for the static design. Figure 4 shows the typical output waveforms of five consecutive shift register stages. The clock and input signals are also shown. The traces, from top to bottom, are: $V_{OUT}(1)$, $V_{OUT}(2)$, $V_{OUT}(3)$, $V_{OUT}(4)$, $V_{OUT}(5)$, CLK, V_{INPUT} . Figure 5 shows two completed shift registers, a dynamic and a static one. Note that most part of the circuit area is occupied by the output buffer structures.

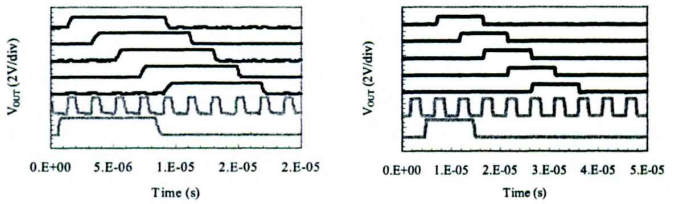


Fig. 4: Output waveforms of dynamic (top) and static (bottom) shift registers, at 500 and 200kHz, respectively.

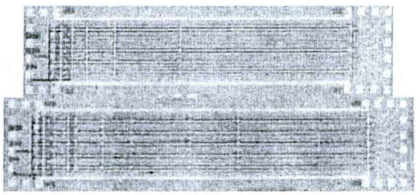


Fig. 5: Dynamic (left) and static (right) 10-stage shift registers on stainless steel foil.

3. OLED DISPLAY CIRCUITS

3.1 Pixel architectures

Two different circuit architectures have been implemented. The first one is the standard 2- TFT design [13]. In this circuit, M1 behaves as a voltage controlled current source, and M2 is the control switch. This means that there are three lines going into each pixel (Vdata, Vadd and Vdd). This circuit works as follows: an analog voltage is programmed

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in the data line during addressing time (when M2 is turned ON by the address line.) This voltage activates M1 allowing a controlled current to flow through it. When the addressing period is over, M2 is turned OFF and C stores the data voltage. This allows M1 to keep supplying the correct current during the non-addressing time. This pixel architecture was implemented with two topologies: an all PMOS design, and a CMOS design with the driving transistor being NMOS and the switch being PMOS.

This circuit does not compensate for TFT device parameter variations such as mobility or threshold voltage. Several pixel designs have been proposed to compensate for such variations. One approach that has attracted a great deal of interest in the last few years is the current addressing technique [14]. When directly addressing with a current, turn-ON voltages and mobility variations do not affect the LED current. This is done by programming the current source with a reference current instead of a voltage, so the current provided by that source is not a function of the voltage on the transistor's gate (instead, the voltage on the gate is a function of the current.)

The 4 TFT current copy circuit is perhaps a good compromise between performance and complexity. This circuit works as follows: during addressing time, a reference current is sinked through Idata. Since M1 is diode connected, a corresponding voltage is established on its gate to allow that current to flow. When M2 and M3 are turned OFF and M4 is turned ON, C holds the programmed voltage on the gate of M1 allowing that current to now flow through the diode. (Figure 6 shows all three pixel circuits)

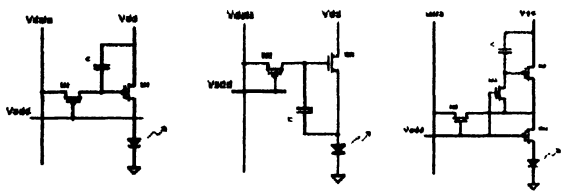


Fig. 6: 2 TFT pixel PMOS (left) CMOS (center), 4 TFT pixel (right).

Both architectures were implemented with two different layouts. The more traditional layout requires a power supply line. However, when using metal foil substrates the high conductivity of stainless steel can be used to bring in power to each pixel creating a less resistive power distribution. The main motive for developing this approach was to increase the light emitting area of the display, since the common power supply line can be omitted. An extra contact layer is required to create contacts between the pixels and the substrate. These contacts are formed after the patterning the first metal contact holes during the fabrication of electric circuits. A second PECVD passivation oxide follows, and then vias that make contact between the AlNi layer and the Indium Tin Oxide film that follows are patterned and opened. After the patterning of the ITO film, the organic electroluminescent material is deposited, followed by the OLED cathode deposition and final display encapsulation.

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Fig. 1: The AM-OLED pixel structure on steel and cross section (vertical dimensions not to scale)

3.2 Pixel Performance

The overall functionality of both pixel designs and both layout implementations were proven at different load impedances 10K, 50K and 100K to account for possible variations in OLED performances. Also the 2-TFT pixel was demonstrated with three pitch sizes: 250 x 250 um and 110 x 105 um for the PMOS implementation, and 125 x 125 um for the CMOS implementation.

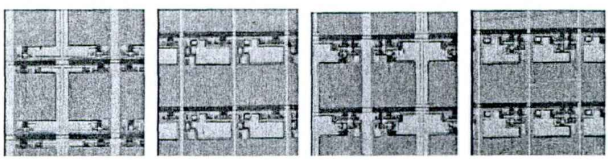


Fig. 7: 2 TFT pixels (left) and 4 TFT pixels (right); all 250 um pitch

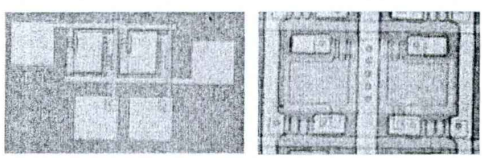


Fig. 8: 2 TFT pixels 125 um x 125 um (left) and 2 TFT pixels 110um x 105 um (right)

Figure 9 shows the average current measured through different pixels over a range of data values and its normalized variation as a function of data voltage, in the 2 TFT pixels. This normalized variation curve was extrapolated to obtain percentage variation of threshold voltage and mobility of the measured devices. We can obtain the theoretical variation by solving the difference equations for mobility (3) and threshold voltage (4) at different gate bias. (First level approximation done with TFT's working on saturation.)

(3) $$\partial I = \partial\mu \cdot k \cdot (Vgs - Vt)^2$$

(4) $$\partial I = \partial Vt \cdot 2 \cdot k \cdot \mu \cdot (Vgs - Vt)$$

If we normalize for the absolute value of current and notice that $\partial\mu = \overline{\mu} \cdot \xi_\mu$ and $\partial Vt = \overline{Vt} \cdot \xi_{Vt}$ (where $\overline{\mu}$, ξ_μ and $\overline{Vt}$, ξ_{Vt} are the average and the percentage mobility and threshold voltage variations respectively), we obtain:

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(5) $$\frac{\partial I}{I} = \xi_{\mu}$$ for mobility changes of ξ_{μ} percent , and

(6) $$\frac{\partial I}{I} = 2 \cdot \frac{\overline{Vt} \cdot \xi_{Vt}}{\overline{Vgs} - \overline{Vt}}$$ for threshold voltage changes of ξ_{Vt} percent.

The extrapolated numbers from figure 9 were 4% for mobility and 9% for threshold voltage which approximate the actual variations seen when obtaining Table 1.
Figure 10 shows the output current versus the programming current in the 4 TFT pixels. The nonlinearity at low current levels can be explained by assuming non-saturation behavior of the driving TFT's. Furthermore, the line impedance that the driving TFT sees when programming is different from the OLED's impedance. As a consequence, the finite output impedance for these devices also explains the loss of linearity between programming current and operating current. [14]

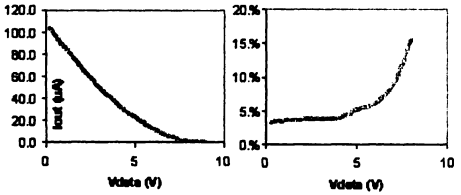


Fig. 9: Typical output current versus input data for 2 TFT pixels and normalized deviations

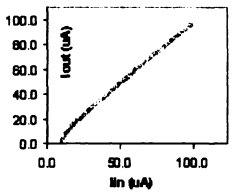


Fig. 10: Output current vs. programming current in 4 TFT pixels

4. DISPLAY OLED

4.1 OLED Fabrication

Liquid Crystal Displays have now been in the market for a number of years; however recent enhancements on Organic Light Emitting Devices (OLED's) offer a new alternative to the Flat Panel Display industry. OLED's offer improved luminous efficiency, high brightness, and excellent viewing angle. In addition, OLED displays have thinner profiles, weigh less, and consume less power than LCD's. Due to their emissive nature, OLED displays do not require a backlight which makes this technology a lower cost and more suitable alternative to flexible display applications.
Their structure consist of a series of thin films that usually include electron and hole injection layers, electron and hole transport layers, and an emissive layer. (In general, polymer OLED's only require a hole transport layer and an emissive layer.) The anode (metal that makes contact with the hole injection layer) is usually made of a high work function metal such as transparent Indium-Tin Oxide (ITO) while the cathode is made by a low work function metal. When the holes and electrons recombine in the emissive layer light is produced.
The PLED's presented in this paper are formed with an anode layer of Al/Ni/ITO (1000A/500A/500A.) PEDOT and PPV are spun on top of the anode sequentially, after etching the insulating layer, SiO_2. By following each spin-casting of the polymers, a

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drying process has to be performed in order to evaporate the solvent. The drying process can be done either on a hot plate or in a vacuum oven. In the current process, solvent drying is done on the hot plate. The thickness of PEDOT and MEH-PPV adopted are 800A and 600A respectively. Thicker films relate to a higher threshold voltage, however, a thicker PEDOT film has more capability of compensating the anode surface resulting in improved yield. A thinner PPV film facilitates the electron and hole recombination, but the thinner film cannot withstand high electric fields. For a top-emitting OLED device, the semi-transparent or transparent cathode is required. Usually, this cathode consists of two different metals. One is the low work function metal (Al, Ca, Ba, Cs, Ag, Li, Mg.....etc.), which is in contact with the light-emitting layer and enhances the electron injection, PPV. Mostly, this metal film is very thin, such as 50A; the other metal plays a role of carrying the current, and ITO or IZO is almost the one and only choice. Ideally, both of these two metals have to be evaporated, rather than being sputtered, in order to reduce the ion bombardment upon the surface of PPV.

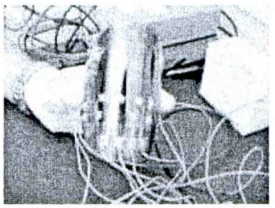


Fig. 11: Flexible passive matrix OLED

4.2 OLED Performance

When using an Al/Ni anode, it essentially becomes $AlNiO_2$ because of the O_2 plasma treatment before the spin-casting of polymers [15]. Some documentation has proved that NiO_2 has the work function of 5.0eV as high as ITO does [16]. This reproducible result has also been found on our device, which was PLEDs on flexible steel. The NiO_2 surface is capable of forming the well-performed holes-injecting interface with PEDOT. One more advantage is that Al/NiO_2 surface can reflect more light than Al/Ni/ITO, presuming that Ni catalyzes the formation of Tin Oxide (SnO_2). That results in the darkness on the surface of Al/Ni/ITO. In our system, Al was sputtered as the low work function metal first, using a low RF power of 50W. Another sample with e-beam evaporated Al was prepared on the thin steel substrate, and it showed a better performance than with sputtered Al (Figure 12). ITO was sputtered in both cases and the thickness was around 900A. Characteristics of electroluminescence and photoluminescence were measured (Fig. 13 and 14) as well as the spectrum of the flexible PLED taken at different voltages. The measurements at 10 V and 11 V were taken twice. In between, there was some degradation of the PLED due to high current during the elapsed time. The degradation of the PLED was measured with two scans taken a half hour apart (Fig. 15). In the interim, the PLED was fed a 9 V signal. The % Change is slightly more for off-peak wavelengths than for the peak wavelength.

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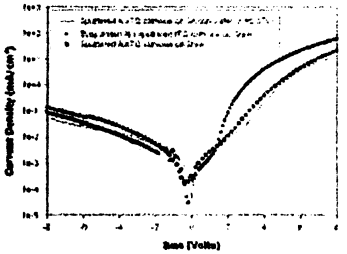


Fig. 12: I-V Curve for OLED

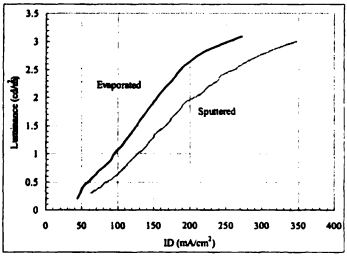


Fig. 13: Luminance of OLED

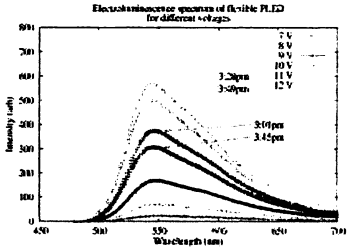


Fig. 14: Electroluminescence of PLED degradation

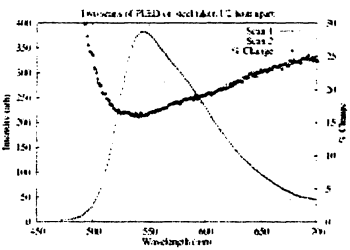


Fig. 15: Electroluminescence

5. CONCLUSION

This paper discussed fabrication issues and measurement results of excimer laser annealed polysilicon TFT devices, circuits and display elements on flexible, type-304 stainless steel foil substrates. We have demonstrated this is possible with a high temperature, CMOS compatible poly-Si TFT fabrication process. This process has resulted in devices adequate not only for active matrix displays implementations, but for integrated display driver circuits too, further enhancing the cost savings realizable with

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this approach. The functionality of several pixels has been proven and stand alone PLED structures have been demonstrated on stainless steel substrates.
These results justify the fabrication of high performance digital circuits for display driver and other medium to high-speed applications on flexible metal foils, and underscore the substantial practical advantages of this type of substrate for high volume, low cost highly integrated flexible electronics.

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OXIDE SEMICONDUCTORS FOR FLEXIBLE ELECTRONICS

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ABSTRACT

We have synthesized thin film transistors with oxide semiconductors of ZnO, In_2O_3, and SnO_2 by rf magnetron sputtering on unheated substrates. ZnO transistors deposited on a high quality HfO_2 dielectric, grown by atomic layer deposition, had mobility exceeding 10 $cm^2/V\text{-}s$ with a high on-off ratio ($> 10^7$), low threshold voltage (< 3 V), and a relatively low sub-threshold slope of ~ 0.5 v/decade. In contrast ZnO transistors had much higher threshold voltage, ~ 30 V, with lower mobility (0.3 $cm^2/V\text{-}s$), when they were on a thermally grown SiO_2 dielectric. The In_2O_3 transistors also had higher mobility (~ 6 $cm^2/V\text{-}s$) on an evaporated Al_2O_3 dielectric than on SiO_2. Because these oxide semiconductors can be processed at low temperature, they are compatible with inexpensive plastic substrate, and we demonstrated fabrication of a ZnO transistor on a polyimide substrate.

The attraction of flexible electronics on plastic substrates is the potential for lower manufacturing cost and a package that is thinner, lighter, more robust, portable and formable. Applications targeted include LCD, OLED, and electrophoretic displays, RFID tags, and inexpensive electronics generally. However, the challenge for flexible electronics is either to develop a plastic substrate to accommodate existing high-temperature processing or find new materials or processes that are compatible with available low cost, more temperature-sensitive plastic substrates. In fact the properties needed for a high-temperature plastic substrate are formidable: dimensional stability (low shrinkage), low thermal expansion, high optical clarity (displays), high use-temperature (e.g., ~ 300° C for processing a-Si TFTs), and chemical durability. Further, because plastic substrates are highly permeable to air and water vapor, they will also need barrier and encapsulation technology. Even if such a substrate technology existed today, it would only be compatible with low temperature Si (amorphous and nanocrystalline) and organic semiconductors. But their lower mobility (< 1 $cm^2/V\text{-}s$) is typically inadequate to achieve high current in OLED displays or the high frequency response needed for RFID tags. Both higher performance for new applications and the goal of enabling flexible electronics on inexpensive plastic substrates have motivated us to search for alternative semiconductors. In particular we have focused on oxide semiconductors.

Oxide semiconductors typified by ZnO, In_2O_3, and SnO_2 are ubiquitous in electronics as transparent conducting electrodes [1]. Electrical conduction in un- doped films of these oxides occurs because of intrinsic defects, such as interstitial metal ions or oxygen vacancies, which can donate free electrons. These oxide semiconductors are normally n-type or electron conductors, and oxide semiconducting films can be made with electron carrier concentrations more than 10^{20} cm^{-3} and a mobility greater than 50 $cm^2/V\text{-}s$ [2], even though their structure is nanocrystalline or amorphous! However, the earliest attempts to demonstrate field effect TFTs in thin film SnO_2 or single crystal ZnO

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gave somewhat disappointing results [3,4] (μ ~1 cm^2/V-s), especially compared to CdS TFTs[5], which were prominently studied at that time. Subsequently, with advances in Si-technology, research activity on oxide TFTs essentially stopped, that is, until recently.

Some of the renewed interest in oxide TFTs, especially ZnO [6,7], has been motivated by its optical transparency. Transparent electronics, with as yet unspecified applications, is alluring. Transparency could, however, prove to be a practical advantage in active matrix schemes to drive displays, because the TFT is both light sensitive, requiring shielding from ambient light, and reduces the pixel "aperture", in proportion to the fractional area the TFT occupies. For this reason a transparent ZnO TFT could increase the effective aperture and would be less sensitive to visible light. This could be important for driving OLEDs, where the pixel design requires multiple TFTs for stable current operation [8]. Principally, our interest in these oxides is their compatibility with plastic substrates and their potential for superior performance with lower temperature processing.

EXPERIMENTAL

Although a number of different synthesis methods for oxide semiconductors are possible, we chose rf magnetron sputtering because of its excellent control, reproducibility, and ease of scale-up for manufacturing. The targets were 6.5 inch diameter, dense ZnO, In_2O_3, or SnO_2 (SCM, Tallman, NY). Sputtering was in a stainless steel chamber (MRC8667) with a substrate-to-target distance of 76 mm. Prior to deposition the chamber was cryo-pumped to ~$2x10^{-7}$ Torr. Typical substrates included DuPont Kapton® polyimide film (50 μm thick), Corning 7059 glass, thin Si, and patterned Si for device fabrication, all placed on a water-cooled substrate table directly beneath the sputtering target. Sputtering was in Ar with a metered partial pressure of O_2. Generally we sputtered at low power (100 W) and low cathode voltage (- 100 V) to mitigate potentially damaging bombardment of the growing film by energetic negative oxygen ions[9], which can cause high stress.

We characterized film crystallographic structure by X-ray diffraction, surface microstructure by atomic force microscopy (Digital Instruments xxx), and optical properties with an n&k Model 1280 Analyzer. Electrical resistivity and Hall mobility were measured using the van der Pauw method[10] on thin film samples about 1 cm^2 square with air-dried Ag paint or In-solder contacts to the film at the four corners. The Hall measurements were made in a magnetic field between 0.5-1.0 T.

Frequently we fabricated TFTs on heavily doped n-type Si substrates with a thermal oxide layer 100-200 nm thick on one side. Ti-Au source and drain electrodes (10 nm Ti followed by 100 nm Au), were deposited and patterned directly on the thermal silicon oxide layer by traditional photolithography. Ti-Au was also deposited on the back of the Si as a common gate electrode. The oxide semiconductor, typically 50 nm thick, was then sputtered between source and drain electrodes using a shadow mask. A few devices were fabricated on flexible, Kapton® polyimide substrates, 50 μm thick. In those instances device patterning was done with a laminated photopolymer resist (Riston®) and metal shadow masks, as discussed specifically in the text. Device properties were evaluated either with an Agilent 4155C Semiconductor Analyzer or with laboratory electronics--- a Keithley Model 236 Source-Measure unit for measuring source-drain current, while sweeping or fixing the source-drain voltage; gate voltages were from a Keithley Model 230 Programmable Voltage Source. Contact to the source,

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drain, and gate conducting pads were with tungsten wire probes connected to these instruments with miniature coaxial cables.

RESULTS AND DISCUSSION

ZnO thin film transistors

ZnO is a wide bandgap (3.37 eV), stable, n-type semiconductor possessing hexagonal wurtzite structure and a high melting temperature (1975 C). Thin films of ZnO that we rf magnetron sputtered on unheated substrates were polycrystalline with c-axis texture, as exemplified by the X-ray diffraction pattern in Fig. 1. From surface imaging with atomic force microscopy, we found that films sputtered at 20 mTorr and pO_2=1x10^{-5} Torr possessed granular morphology with average grain size in the range 32-38 nm and an average surface roughness of ~1.9 nm, as shown in Figure 2. Changing the oxygen partial pressure during sputtering in the range 10^{-6} Torr to 10^{-3} Torr, had little influence on structural properties of ZnO. Also, somewhat independent of pO_2, ZnO films were transparent in the visible with a measured optical transmission typically above 80% for an optical wavelength > 400 nm, as shown in Fig. 3.

In contrast, the electrical resistivity of ZnO films does depend strongly on pO_2 during sputtering[7]. Figure 4 shows that the resistivity undergoes an abrupt transition from semiconducting (ρ~0.03 ohm cm) at low oxygen partial pressure to semi-insulating (ρ =10^6-10^8 ohm cm) at higher pO_2. For films with a resistivity less than 1 ohm-cm, we measured Hall mobility in the range 12-25 cm^2/V-s (n-type). For comparison, the mobility of single crystalline ZnO is ~ 200 cm^2/V-s[11]. In order to achieve a low leakage or off-state current in a ZnO TFT, high resistivity ZnO is preferred, corresponding to high pO_2 during sputtering. However, the electron mobility in these polycrystalline films depends inversely on pO_2, so that synthesis conditions need to be adjusted for optimum device performance[12].

Fig. 5 shows typical output and transfer characteristics for a ZnO TFT on a 200 nm thick thermal oxide of silicon. The calculated (saturation) mobility for this device was 0.3 cm^2/V-s with a threshold voltage of 28.4 V and an on/off ratio~ 10^6. The sub-threshold slope, determined between 10V and 20 V, was 4.1 V/decade. The measurable hysteresis in the transfer curve and large subthreshold slope are evidence for charge trapping. Previously we estimated a surface trap density[7] for ZnO on thermal oxide to be between 1.5x10^{12} cm^{-2} and 3.0x10^{12} cm^{-2}. Although the mobility for this particular device is a little lower than has been common ($\geq$ 1 cm^2/V-s) in our experience, the high threshold voltage, we now recognize, is a signature property of ZnO grown on the thermal oxide of silicon. While a high threshold voltage limits applications, e.g., liquid crystal displays operate at voltages ~10 V, nonetheless the relatively high mobility, high on/off ratio, and low leakage current (~ pA) of ZnO TFTs on thermal oxide are impressive, considering that the ZnO semiconductor was grown without intentionally heating the substrate.

A direct approach to improve the properties of a ZnO TFT is to try other dielectrics. Nomura et al.[13] found a nearly fifty-fold increase in mobility for crystalline indium-gallium-zinc oxide semiconductor with a HfO_2 dielectric compared to Al_2O_3, while other groups have reported improvements in ZnO TFT performance by inserting a dielectric buffer layer[14] between a SiO_2 dielectric and the ZnO semiconductor. We investigated ZnO TFT properties for a HfO_2 dielectric layer, 25 nm thick. The starting for device fabrication was a conducting Si wafer on which 25 nm of HfO_2 was grown by

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atomic layer deposition[15] at Aviza Technologies. Ti/Au source and drain electrodes were then photolithographically patterned on this dielectric and the ZnO semiconductor subsequently sputtered through a metal shadow mask. Figure 6 shows ZnO transistor output and transfer characteristics on HfO_2 for a device with channel length 20 μm x 200 μm wide. Compared to the device on SiO_2 dielectric, the mobility increased 40-fold to 12.2 cm^2/V-s, the threshold was reduced to 2.55 volts with a sub-threshold slope of about 0.5 V/decade, and the on/off ratio was ~10^7, although the leakage current was higher. The high output current (~mA) at less than 10 V for this device is particularly attractive for driving an OLED. Clearly the choice of dielectric can substantially improve the device properties of ZnO TFTs beyond that attributable only to the higher dielectric constant of HfO_2 (ε_r=25) and its correspondingly higher gate capacitance (0.89 μF/cm^2). Further, ZnO TFTs exhibit very small hysteresis. We measured only about 50 mV from the transfer characteristic.

Ultimately our goal for ZnO TFTs is to create a plastic or flexible electronics technology using low temperature processing. As an example of a ZnO TFT on a flexible substrate we built transistors starting with DuPont Pyralux® (Cu-coated polyimide), that we patterned source and drain by photolithography. ZnO was then sputtered through a liftoff mask. This was followed by lamination of a fluoropolymer dielectric (~ 2 μm thick) over the transistor active region. Finally, Al gates were thermally evaporated using a metal shadow mask. Figure 7 illustrates the performance characteristics of these flexible transistors, which had μ ~ 0.4 cm^2/V-s and on/off ratios larger than 10^4. While this performance is respectable, we have achieved higher performance with alternative dielectrics grown by physical vapor deposition without substrate heating.

In_2O_3 thin film transistors

Indium-oxide (IO) doped with Sn (ITO) is well known in electronics and displays as a transparent thin film electrode[1], while non-stoichiometric InOx films are reported to be effective gas sensors[16]. Both ITO and IO can be deposited at room temperature with high conductivity (~ $3x10^3$ ohm^{-1} cm^{-1}) and Hall mobility (~ 50 cm^2/V-s)[2]. They are n-type conductors in which ionized oxygen vacancies donate free electrons for conduction: ideally, $O_O \rightarrow V_O + 2\ e^- + 1/2\ O_2$ (g), where V_O is a vacancy at an oxygen site. We have published that the conductivity of IO films made by sputtering can be varied from semi-insulating to highly conducting by controlling the oxygen partial pressure (pO_2) during sputtering[2]. High pO_2 promotes formation of more insulating, stoichiometric In2O3, while films sputtered in low pO_2 become more electrically conducting because of lattice oxygen deficiency. As for ZnO, a thin film transistor requires both the low off-state current of the insulating phase and the higher mobility of electrically conducting IO, and synthesis conditions that balance these properties.

IO semiconductor films, which gave good TFT properties, were less than ~50 nm thick and sputtered at 4 mTorr total pressure with pO_2 between 0.1 mTorr and 1.0 mTorr. We found IO films had better TFT performance when their sheet resistance was > 500 M ohm/square, corresponding to a conductivity less than about 10^{-4} ohm^{-1} cm^{-1}. From X-ray diffraction we determined that films were polycrystalline with the c-type rare-earth structure (bixbyite) and (222)-texture. The surface microstructure from atomic force microscopy was granular with very small feature size ~ 30 nm. These structural details are similar to those we already reported[2] for conducting IO films sputtered at 12 mTorr with pO2 < 0.1 mTorr, although increasing pO2 and reducing the total sputtering pressure, as in these experiments, enhanced film crystallinity, which we concluded from sharper and more intense X-ray diffraction peaks.

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Figures 8 and 9 summarize the output and transfer characteristics of typical IO thin film transistors sputtered on a thermal oxide of SiO_2 and on evaporated Al_2O_3. On SiO_2 dielectric, we measured an initial saturation mobility, μ_{sat}= 0.028 cm^2/V-s, and an on/off ratio ~10^4 with a threshold voltage V_{th}=8.2 V. When this same device was remeasured, after storing in the laboratory ambient for 16 days, the mobility increased to μ_{sat}= 0.36 cm^2/V-s, V_{th} decreased to 1.6 V, and the on/off ratio increased to ~10^5. IO TFTs grown on Al_2O_3 had a higher mobility, in this case μ= 5.6 cm_2/V-s, a threshold voltage V_{th}=8.1 V, and an on/off ~ 5x10^3. After storage for several months in an ambient environment, without light shielding, indium oxide devices on both dielectrics continued to change. At this time we do not fully understand the origin of these changes in indium oxide devices, but work is underway to find a means to stabilize them.

SnO_2 thin film transistors

Work on SnO2 TFTs in our laboratory is only preliminary, but initial experiments confirm that devices can be made with this oxide semiconductor. Fig. 10 shows the transistor output characteristic for a sputtered SnO_2 device. It was fabricated on a Si wafer with 100nm thick thermal oxide on one side and a Ti/Au common gate electrode on the back side. Al source drain electrodes with channel length 100 μm x 1mm width were deposited through a metal shadow mask, followed by sputtering of the SnO_2 semiconductor, 87.5 nm thick, also through a shadow mask. The SnO_2 was sputtered in 10 mTorr Ar and O_2 (5%). SnO_2 films sputtered at these conditions were transparent in the visible with > 80% transmission above a wavelength of 375 nm and a high index of refraction, n=1.86 (at 633 nm). However, the sheet resistance of this film was only ~ 6 MΩ/ square, corresponding to a relatively low, film resistivity --50 Ω-cm. This was likely responsible for the high off-state (Vg=0) current of ~ 10^{-7} A. From a plot of $I_d^{1/2}$ versus V_g near saturation, we deduced a mobility μ=0.015 cm^2/V-s, an on/off ratio ~ 300, and a threshold voltage of −11.4 V. Although these properties are not as good as for In_2O_3 or ZnO, there is wide latitude for optimizing SnO_2 semiconductor properties.

CONCLUSIONS

In this work we demonstrated that thin film transistors can be fabricated with a sputtered semiconductor of ZnO, In_2O_3, or SnO_2. Since all of these oxides were synthesized on unheated substrates, they are compatible with processing on inexpensive plastic substrates or even paper. In one specific example a ZnO device formed on a polyimde substrate, with lamination at low temperature to a fluoropolymer dielectric, had mobility ~0.4 cm^2/V-s with on/off > 10^4. We further showed that oxide TFTs, grown on a high quality dielectric, such as by atomic layer deposition, can have mobility exceeding 10 cm^2/V-s, making them attractive for high performance applications, e.g., high frequency RFID tags or a drive transistor for an OLED.

ACKNOWLEDGMENTS

The authors would like to thank Dr. Yoshi Sensaki and his team at AVIZA Technology for expertly depositing by atomic layer deposition a high quality HfO_2 dielectric for this study on oxide semiconductors.

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FIGURES

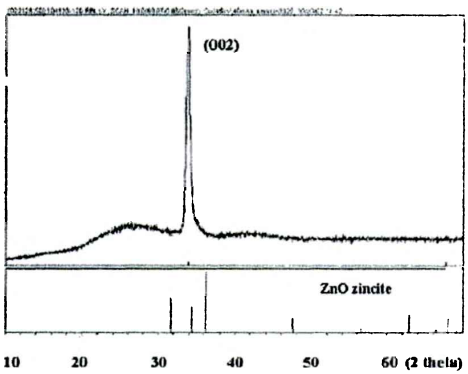


Fig. 1 X-ray diffraction pattern of ZnO thin film with (002)-texture and reference line pattern for ZnO zincite.

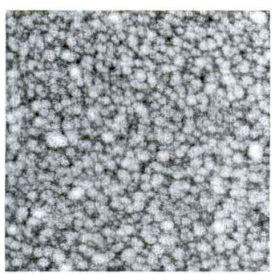


Figure 2. Atomic force microscope image of ZnO surface topography for sputtering conditions of 20 mTorr ($Ar+O_2$) and $pO_2=10^{-5}$ Torr. The ZnO film thickness was 108 nm. The image height or z-range is 30 nm and the scan size is 1 μm x 1 μm.

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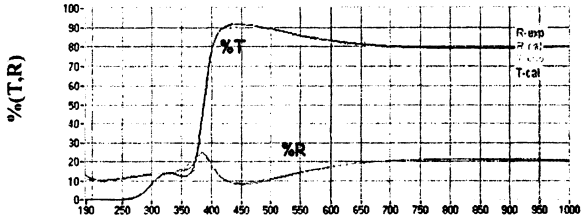


Fig. 3 Optical transmission and reflectance for ~100 nm thick ZnO thin film rf magnetron sputtered at 20 mTorr (Ar) with pO_2=1x10^{-5} Torr. Substrate is Corning 7059 glass.

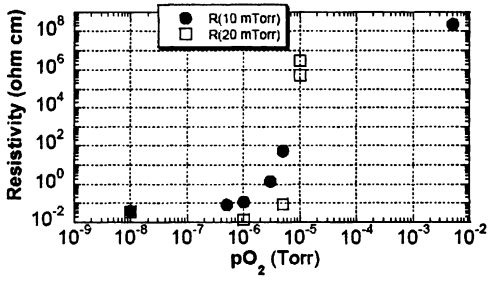


Figure 4. Dependence of electrical resistivity of magnetron sputtered ZnO thin films on partial pressure of oxygen (pO_2) used in sputtering at total Ar–O_2 pressure of 10 mTorr (•) and 20 mTorr (❑).

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Figure 5. Transfer (a) and output (b) curves for ZnO thin film transistors on 200 nm thick, thermally grown SiO_2 dielectric.

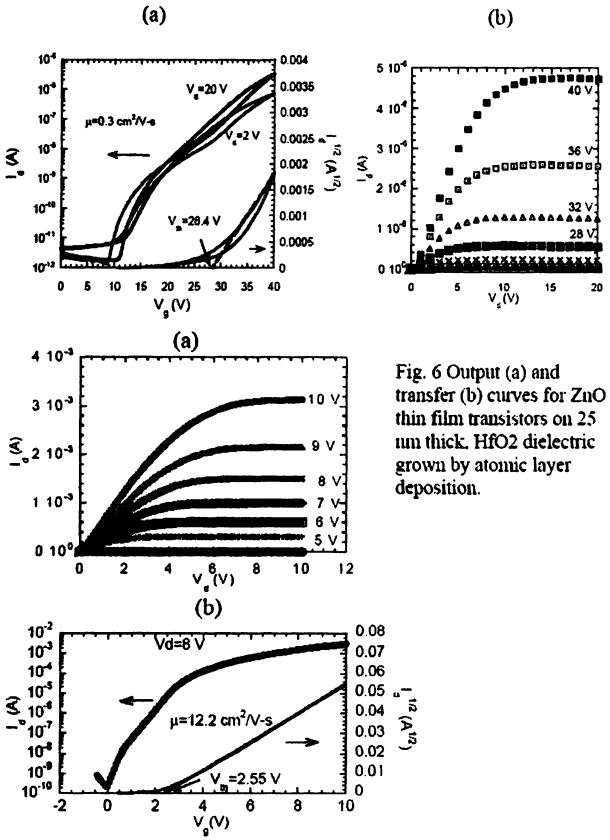


Fig. 6 Output (a) and transfer (b) curves for ZnO thin film transistors on 25 nm thick. HfO2 dielectric grown by atomic layer deposition.

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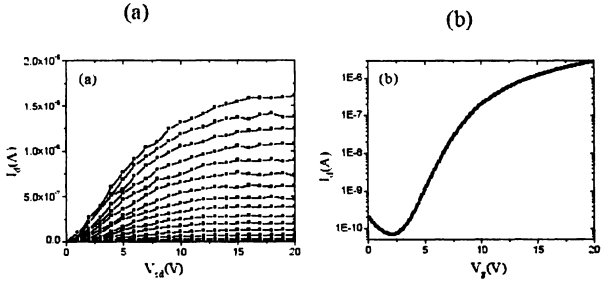


Figure 7: (a) Id-vs-Vsd at Vg varying from 0V to 20V in steps of 1V. (b) Id-vs-Vg at Vsd = 20V. W = 400 μm. L = 40 μm

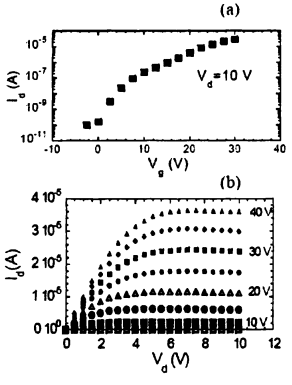


Fig. 8 Transfer (a) and output (b) curves for In_2O_3 thin film transistors on 200 nm thick, thermally grown SiO_2 dielectric.

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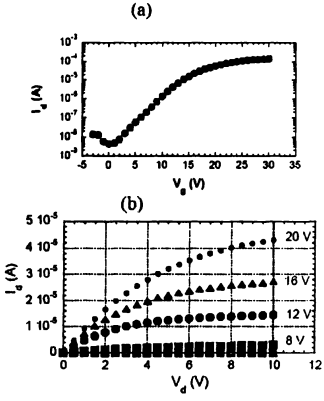
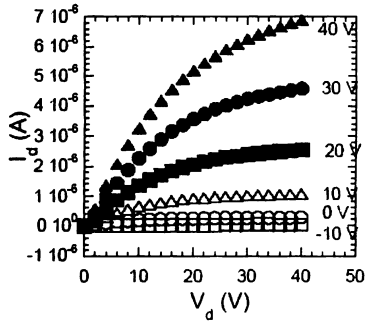


Fig. 9 Transfer (a) and output (b) curves for In_2O_3 thin film transistors on 500 nm thick. e-beam evaporated Al_2O_3 dielectric.

Fig. 10 Output characteristic for sputtered SnO2 thin film transistors on 200 nm thick, thermally grown SiO_2 dielectric.



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THIN-FILM TRANSISTORS BASED ON SPIN-COATED CHALCOGENIDE SEMICONDUCTOR CHANNELS

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The production of high-performance solution-processed semiconductor films represents an important materials challenge, with achievement of field-effect mobilities >10 cm^2/V-sec being particularly desirable for high-speed low-cost microelectronic applications. While most soluble semiconductor research has focused on organic systems, this review addresses a hydrazinium precursor approach for solution-processing high-quality inorganic films. Ultrathin $SnSe_{2-x}S_x$ channel layers, spin coated from a hydrazine solution of chalcogenides, yield field-effect mobilities and on-off ratios as high as 12 cm^2/V-s and 10^6, respectively. Analogous devices have also been prepared from water-hydrazine solvent mixtures (20% hydrazine by volume), thereby reducing the concentration of highly toxic hydrazine during spin-coating. Additionally, In_2Se_3 channel layers have been demonstrated, spin coated without the use of hydrazine as solvent, yielding μ_{sat}=16.5 cm^2/V-s, μ_{lin} = 4.9 cm^2/V-s, $I_{on}/I_{off}=10^6$, with a subthreshold swing as low as S = 450 mV/decade. The operating voltages in these latter devices have been reduced to 8V through the use of a relatively thin (250 Å) SiO_x gate insulator. Reductions in the use of hydrazine and in the TFT operating voltage improve fabrication and operational compatibility of the devices with respect to electronics industry standards.

INTRODUCTION

Low-cost solution-based fabrication of thin-film field-effect transistors (TFTs) has become a key goal among the materials science community, primarily as a result of applications potentially enabled by the new technologies (e.g., flexible displays, electronic newspapers, smart cards / fabric) (1-10). Paramount to this search is the need to identify thin-film deposition processes that simultaneously offer high-throughput deposition (e.g., spin coating, printing, stamping), as well as continuous and uniform films. As circuit device components are scaled to smaller dimensions and reduced operational parameters, control of film thickness to ultrathin dimensionality also represents an important aspect to any proposed film-deposition process (11,12).

Among the various TFT components to be deposited from solution, the semiconducting channel provides a significant challenge. The challenge arises because of a strong dependence of the device properties on the film quality (as well as substrate-film interface) and the desire to deposit high-mobility semiconductors, which are generally covalently bonded solids and not very soluble. Most work on solution-

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processed TFTs has focused on organic-based channel layers (1-4), with highest demonstrated mobilities in the range of 1 cm^2/V-s (same order of magnitude as amorphous silicon) (3). Organic-inorganic hybrids have also been demonstrated as an approach for targeting higher mobility solution-processed films (5,6), with the potential of combining the templating / self-assembly characteristics of organic molecules with the higher mobility from an extended inorganic framework. Spin coated tin(II)-iodide-based hybrid channels currently yield mobilities of order 1 cm^2/V-s (5,6). While thin-film carrier mobilities of ~1 cm^2/V-s are appropriate for lower-end applications (e.g., TFTs to address moderate size/resolution LCD displays), high-throughput solution-processed films with a mobilities >10 cm^2/V-s would provide opportunities for new technologies, including low-cost logic for applications requiring higher levels of integration and speed than currently afforded by the present generation of solution-processed organic and hybrid semiconductors (or amorphous silicon).

Here, we discuss two related approaches for spin coating crystalline inorganic channel layers, each based on the low-temperature decomposition of highly-soluble hydrazinium (or related) precursors of main group metal (e.g., Ge, Sn, In, Sb) chalcogenides (8-10). Resulting metal chalcogenide films are only a few unit cells thick, with remarkably large field-effect mobilities – up to an order of magnitude better than previous studies involving high-throughput solution-based deposition.

EXPERIMENTAL

TFTs have been prepared (Figure 1), based on spin-coated chalcogenide channel layers fabricated using one of the approaches described below. The heavily doped silicon substrate acts both as the substrate and gate. Thermal oxides, with thickness ranging from 250 – 2100 Å, have been employed as the gate insulator.

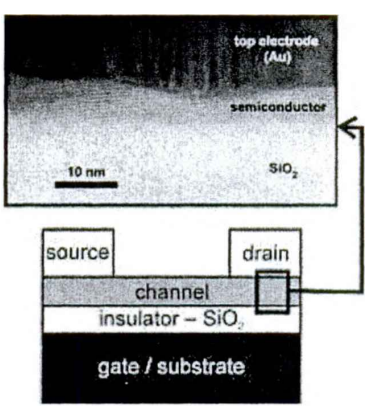


Figure 1. The TFT device consists of a heavily *n*-doped silicon wafer as the substrate/gate, a thermally grown SiO_2 gate dielectric, a spin-coated chalcogenide channel layer, and patterned evaporated metal source and drain electrodes. The magnified region shows a transmission electron microscope (TEM) cross-sectional image of a device based on a spin-coated $SnS_{1.4(1)}Se_{0.5(1)}$ film (8).

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Approach 1: Metal Chalcogenide Solution in Hydrazine and Excess Chalcogen (8)

Tin(IV) chalcogenide ($SnSe_{2-x}S_x$) channel layers are spin coated onto thermally oxidized silicon substrates (heavily doped n-type, 2100 Å SiO_x), cleaned using a 'piranha' process (hydrogen peroxide:sulphuric acid in 1:4 volume ratio), from a solution prepared from 14 mg SnS_2, 8 mg $SnSe_2$ and 6 mg S (excess chalcogen) in 1.9 ml freshly-distilled hydrazine. The solid reactants completely dissolve after stirring at room temperature in a nitrogen-filled vial for 2 h. Spin coating is performed in air by flooding the substrate surface with the clear yellow solution (passed through a 0.2-μm filter) and spinning at 3500 r.p.m. for 45 s. The hydrazinium precursor films are then immediately dried in air for 5 min at 120 °C on a preheated hot plate, followed by a final 20 min anneal at 270 °C in a nitrogen-filled dry box with oxygen and water levels maintained below 1 p.p.m. The chemical composition and average film thickness of the final films, as determined by medium energy ion scattering (MEIS), are $SnS_{1.4(1)}Se_{0.5(1)}$ and 42(5) Å, respectively (8). Transmission electron microscope (TEM) images of a film cross section (Figure 1) demonstrate the ultrathin, crystalline nature of the films, with average film thicknesses of ~50 Å (consistent with the MEIS results) – i.e., only ~ 8-10 unit cells thick. Substantial preferred orientation is visible within the films, with the $SnSe_{2-x}S_x$ layers oriented nominally parallel to the substrate surface (corresponding to the fringes observed in the TEM images). The average interlayer (fringe) separation is 6(1) Å, consistent with the (0 0 1) layer separation of the $SnS_{2-x}Se_x$ structures (13). Electron-beam-evaporated gold is used for the source/drain electrodes on top of these films. The gold deposition is patterned through a silicon membrane mask.

Given the toxic nature of hydrazine, it is desirable to reduce the amount of this solvent used in the spinning process. To this end, in addition to the films described above, we have also recently demonstrated (9) high quality tin chalcogenide films and devices spun using a mixed water / hydrazine solution. In one experiment, 14 mg SnS_2, 8 mg $SnSe_2$, and 8 mg S were dissolved in 0.4 ml hydrazine (by stirring approximately 2 hours under a nitrogen atmosphere). After dissolution, 1.6 ml of water was added and the resulting solution was spun in air (3500 rpm) as for the devices prepared from pure hydrazine (final anneal / decomposition treatment for this film was at 260 °C for 20 minutes). The films deposited from the 20 % (by volume) hydrazine / water mixture exhibited similar device characteristics to those deposited from pure hydrazine (8,9). For devices based on these films, lower work function tin source/drain contacts (e-beam-evaporated) were employed.

Approach 2: Hydrazinium Precursor in Non-Hydrazine-Based Solvent (10)

To further demonstrate departure from the use of hydrazine as a solvent during spin coating, indium selenide channel layers have been prepared using isolated hydrazinium precursors and a mixed solvent (ethanolamine / dimethylsulfoxide (DMSO)) system (10). For the preparation of the hydrazinium precursor, a transparent pale yellow viscous solution was formed by dissolving, in a nitrogen atmosphere, 466.5 mg In_2Se_3 (1 mmol) and 79.0 mg Se (1 mmol) in 3 ml of freshly distilled hydrazine. Upon evaporating the solvent overnight under nitrogen flow, 687 mg of a yellow glassy material was formed, with approximate composition $(N_2H_4)_2(N_2H_5)_2In_2Se_4$ (10). Based on the $(N_2H_4)_2(N_2H_5)_2In_2Se_4$ stoichiometry, the yield was approximately 100% relative to the initial In_2Se_3 and Se starting charge.

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Indium selenide films were spin coated onto thermally oxidized silicon substrates (heavily doped n-type, 250 Å SiO_2), cleaned as for the Approach 1 substrates, from a solution consisting of 55 mg hydrazinium precursor in 0.6 ml ethanolamine (Fluka, ≥99.0 %; distilled before use) and 1.0 ml DMSO (Aldrich, 99.9+ %, anhydrous; distilled before use). The mixture was stirred in a closed vial (maintained in a nitrogen-filled glovebox) at room temperature for 15 hr and at approximately 160 °C for 1 h. Little solubility was noted until the mixture was heated, at which point the precursor rapidly dissolved to form a clear orange-brown solution. The material stayed in solution upon cooling to room temperature. Spin coating was performed in air by flooding the substrate with the solution (passed through a 0.2-μm filter) and spinning at 3500 rpm for 50 sec. The films were immediately dried in air for 3 min at 100 °C on a preheated hot plate, followed by a final anneal for 20 min at 350 °C in a nitrogen-filled drybox with oxygen and water levels maintained below 1 ppm. The resulting composition and thickness for the films are $In_2Se_{2.8(1)}$ and 47(5) Å, respectively, as determined by MEIS (10). The MEIS results yield a composition within 2σ of the ideal 3:2 In:Se ratio (perhaps, however, suggesting a slight chalcogen deficiency). Composite indium/gold (i.e., ~1:1 atomic ratio) source and drain contacts for TFT device fabrication were co-deposited by two-source e-beam evaporation (rotating substrate stage to ensure uniform film composition).

Characterization

Thermogravimetric analysis (TGA) scans of the hydrazinium precursors were performed using a TA Instruments TGA-2950 to examine thermal decomposition. The TGA was run using a 2°C/min ramp rate and a flowing nitrogen atmosphere. MEIS analysis was performed with 200 keV protons using an electrostatic energy analyzer at a scattering angle of 120°. The large scattering angle was chosen to minimize overlap between the metal and chalcogen peaks. The system was calibrated to better than 5% accuracy using a SiO_2 film of known thickness. TFT devices were tested using a Hewlett-Packard 4145B semiconductor analyzer. Devices were maintained and TFT measurements were performed in a nitrogen-filled drybox with oxygen and water levels maintained below 1 p.p.m. Extensive exposure to the ambient atmosphere generally led to an increase in the off-current and therefore a reduction in current modulation.

RESULTS AND DISCUSSION

Channel Layer Deposition Process

The hydrazinium precursor process (8) employs excess chalcogen (S or Se) to directly improve the solubility and film formation properties of main group metal chalcogenides (generally fairly insoluble) in hydrazine and related solvents. The resulting solutions of the hydrazinium precursors are spin coated onto substrates, leaving behind a hydrazinium precursor film that can be cleanly decomposed to the targeted metal chalcogenide semiconductor at moderately low temperature (200 - 350 °C). Note that the relatively low temperatures employed during fabrication are already compatible with selected flexible plastic substrates (e.g., Kapton), while lower-temperature plastics might also be

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compatible if pulsed-laser annealing were employed for the final heating step, as has been previously demonstrated for the preparation of polysilicon films (14).

For the tin chalcogenides, dissolution in hydrazine and excess chalcogen is expected to primarily occur through the overall reaction (8):

$$5N_2H_4 + 2X + 2SnX_2 \rightarrow N_2\,(gas) + 4N_2H_5^+ + Sn_2X_6^{4-}\ (X = S, Se) \qquad [1]$$

Evaporation of the pale yellow solution over a 24 hour period yields $(N_2H_5)_4Sn_2S_6$ (X = S) or $(N_2H_4)_3(N_2H_5)_4Sn_2Se_6$ (X = Se) crystals, which consist of anionic dimers of edge-sharing SnX_4 tetrahedra ($Sn_2X_6^{4-}$) alternating with hydrazinium cations (Figure 2, inset) and, for X = Se, neutral hydrazine molecules (8,9). The observed crystal structures are similar to that found (15) in $K_4Sn_2Se_6$ with, however, the replacement of the alkali metal cation with a small volatile hydrazinium species, which can be decomposed from the material using a low temperature anneal. Polycrystalline films (rather than single crystals) of the precursor can also be achieved by spin-coating the hydrazine-based solution onto a substrate. For $(N_2H_5)_4Sn_2S_6$, decomposition to the microcrystalline metal chalcogenide semiconductor upon heating is essentially complete by approximately 200 °C (Figure 2), highlighting the low-temperature nature of this deposition process (8). The observed weight loss during decomposition (34.6% at 300 °C) agrees with the expected value for the formation of SnS_2 (as also confirmed by x-ray diffraction of the product). For the analogous selenide compound, the transistion to crystalline $SnSe_2$ is also completed by approximately 200 °C, although higher temperatures (~350 °C) are required to dissociate excess Se from the film, which remains in the sample after the precursor decomposition (16). A similar dissolution process to that presented in equation [1] has also been observed for $GeSe_2$ (16) and In_2Se_3.

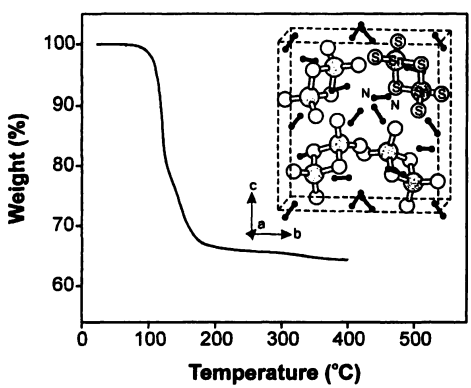


Figure 2. Thermogravimetric analysis (TGA) scan for the bulk $(N_2H_5)_4Sn_2S_6$ precursor (2 °C/min ramp rate) (8). **Inset:** $(N_2H_5)_4Sn_2S_6$ crystal structure determined using single crystal X-ray diffraction (8). Hydrogen atoms have been removed for clarity. Unit cell (outlined by dashed lines): Orthorhombic ($P\,2_1\,2_1\,2_1$), a = 8.5220(5) Å, b = 13.6991(8) Å, c = 14.4102(9) Å, V = 1682.301 Å^3, and Z = 4.

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Despite the promising characteristics of the resulting spin-coated films (see below), several materials and device issues limit the prospective application of the new approach for commercial device fabrication (8-10,17). Primary among these issues is the use during spin coating of the solvent hydrazine – a highly toxic and explosive material. In the above discussion, the metal chalcogenides are directly dissolved and solution-processed into thin film form from a hydrazine solution (corresponding to Approach 1 in the experimental section). Mixtures of water and hydrazine, with relatively small levels of hydrazine (20% by volume) can also be used to spin coat high quality metal chalcogenide films (9), thereby reducing the concentration of hydrazine in the precursor solution. Significantly, we have also recently explored the use of non-hydrazine-based solvents (and mixtures) during the spin-coating process. Approach 2 (see Experimental section) describes a process in which the steps of forming the hydrazinium precursor and spin-coating a film are separated (10), thereby enabling the use of a non-hydrazine based solvent during the spin-coating process (assuming the identification of a suitable alternative solvent). In the example discussed, an ethanolamine / DMSO mixture is used as an effective solvent for an indium(III)-selenide-based hydrazinium percursor and high quality γ-In_2Se_3 films are thereby deposited by spin coating. The attractiveness of this approach for large-scale device fabrication is that use of hydrazine can be limited to the step of precursor synthesis (presumably to be carrier out by a chemical manufacturer), while the device fabrication facility can be free of hydrazine solvent.

In a more general sense, the described deposition processes (Approaches 1 and 2) rely on the formation of a precursor that: 1) has the extended metal chalcogenide framework broken up into smaller inorganic anions (enhancing solubility), and 2) a counter cation that is volatile and small enough for low-temperature removal from the film with minimal disruption (thereby enabling convenient recovery of the extended semiconducting framework after spin-coating). Given this understanding, it seems likely that the hydrazinium precursor approach will be extendable to other chalcogenides (besides the $SnS_{2-x}Se_x$, $GeSe_2$ and In_2Se_3 systems already considered), as well as to a range of solvent systems. The resulting high-quality metal chalcogenide films have proven useful as TFT channel layers.

Device Results

TFTs based on the spin coated chalcogenide films have been fabricated with the architecture shown in Figure 1. A representative plot of drain current, I_D, versus drain voltage, V_D, as a function of the applied gate voltage, V_G, is shown in Figure 3A for a TFT with a $SnS_{1.4(1)}Se_{0.5(1)}$ channel formed from a hydrazine-based solution (Approach 1). The device operates as an n-channel transistor (accumulation mode upon application of a positive gate bias). At low V_D, the TFT shows typical transistor behavior as I_D increases linearly with V_D. Current saturation, with a small ohmic component, is observed at high V_D as the accumulation layer is pinched off near the drain electrode. Current modulation (I_{ON}/I_{OFF}) and saturation regime field-effect mobility (μ_{sat}) are calculated (18) from the plot of I_D and $I_D^{1/2}$ versus V_G (Figure 3B), yielding $I_{ON}/I_{OFF} > 10^6$ and $\mu_{sat} = 12.0$ cm^2/V-s, respectively, for a -60 to 85 V gate sweep and $V_D = 85$ V. The linear regime mobility derived from the plot in Figure 3A, $\mu_{lin} = 2.4$ cm^2/V-s, is lower than the saturation regime value, as also typically observed for organic and organic-inorganic hybrid semiconductors (5,6). While substantial variability exists among device results in these early devices produced using the hydrazinium precursor approach, these

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mobility values are representative of the devices measured and are approximately an order of magnitude higher than previous results for spin-coated films. In one run that involved two substrates and a total of 17 devices measured (biased to 85 V), μ_{sat} ranged from 6.4 to 13.3 cm^2/V-s (only 3 devices, with the largest channel lengths examined, had a mobility lower than 9 cm^2/V-s).

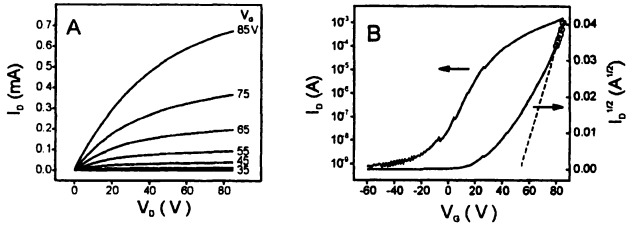


Figure 3. Device characteristics for a $SnS_{1.4}Se_{0.5}$ film spun from a hydrazine-based solution (as described in the text). The source/drain contacts are evaporated gold. The gate dielectric consists of 2100 Å of thermally grown oxide and channel length and width are L = 14 μm and W = 250 μm, respectively: (A) Drain current, I_D, versus drain voltage, V_D, as a function of gate voltage, V_G. (B) Plots of I_D and $I_D^{1/2}$ versus V_G at constant V_D = 85 V (8).

In an effort to reduce the operating voltage of the $SnSe_{2-x}S_x$-based devices, a thinner gate dielectric was employed (400 Å versus 2100 Å). Additionally, the channel length in the devices was scaled down to 4.4 μm (from 14 μm). Film processing was exactly as for the previously described devices (see Experimental section under Approach 1), with the exception that 1.6 ml of hydrazine was used as solvent rather than 1.9 ml. Device characteristics are shown in Figure 4, yielding mobilities that are very similar to those obtained from the film spin coated on a thicker oxide (μ_{sat} = 11.4 cm^2/V-s; μ_{lin} = 3.5 cm^2/V-s). The on-off ratio is somewhat smaller than for the previous device (10^5), presumably because of the short channel length, which makes it more difficult to shut the device off. Note that the threshold voltage has been proportionally decreased with the oxide thickness ($V_T \approx 10$V rather than ≈55V for the 400 Å and 2100 Å gate oxide devices, respectively). In addition, note that only a small change in the shape of I_D versus V_G curve is noted in progressing from the 10th cycle of operation through the 500th cycle, with essentially no change in the overall current modulation. The device characteristics for the 500th and 1000th cycle for the device fall virtually on top of each other, demonstrating the relative stability of the device with respect to cycling (in an inert atmosphere). Further testing is required to learn how the devices fatigue with further cycling and what aspects of the devices lead to device degradation and failure (e.g., gate dielectric-semiconductor interface, metal contact-semiconductor interface).

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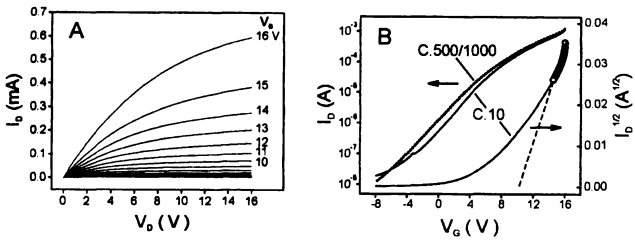


Figure 4. Device characteristics for a tin chalcogenide film spun from a hydrazine solution (as described in the text). The source/drain contacts are gold. The gate dielectric consists of 400 Å of thermally grown oxide and channel length and width are L = 4.4 μm and W = 250 μm, respectively: (A) Drain current, I_D, versus drain voltage, V_D, as a function of gate voltage, V_G, for an as-made device. (B) Plots of I_D and $I_D^{1/2}$ versus V_G at constant V_D = 16 V, for a device cycled 10 times (C.10), 500 times (C.500) and 1000 times (C.1000). Note that the C500 and C1000 curves essentially overlap.

Devices based on $SnSe_{2-x}S_x$ have also been fabricated (see Experimental section) by spin coating the channel from water/hydrazine mixtures (to reduce the toxicity and explosive nature of the solvent), with typical device characteristics shown in Figure 5 (9). The mobilities for this device are similar to those obtained from the film spin coated from undiluted hydrazine (μ_{sat} = 7.0 cm^2/V-s; μ_{lin} = 4.3 cm^2/V-s). As for the previous two sets of devices, the threshold voltage (~20V) scales appropriately with the gate oxide thickness.

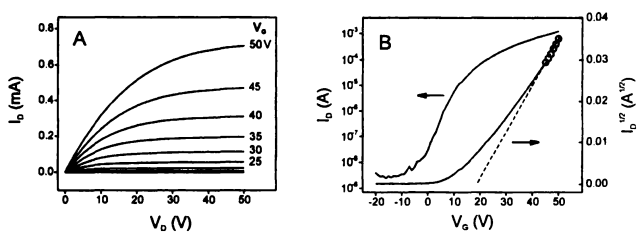


Figure 5. Device characteristics for a tin chalcogenide film spun from a mixed water / hydrazine solution (as described in the text). The source/drain contacts are tin, rather than gold. The gate dielectric consists of 1000 Å of thermally grown oxide and channel length and width are L = 95 μm and W = 1000 μm, respectively: (A) Drain current, I_D, versus drain voltage, V_D, as a function of gate voltage, V_G. (B) Plots of I_D and $I_D^{1/2}$ versus V_G at constant V_D = 50 V (9).

TFTs based on indium(III) selenide channel layers have also recently been demonstrated (10), with the spin coating performed using a non-hydrazine-based solution (Approach 2). The In_2Se_3 channel layers are deposited by spin-coating of an indium

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selenide hydrazinium precursor from a solvent mixture of ethanolamine and DMSO. Figure 6A displays a plot of drain current, I_D, versus drain voltage, V_D, as function of the applied gate voltage, V_G, for an n-channel indium-selenide-based TFT. Current modulation (I_{ON}/I_{OFF}), saturation regime field-effect mobility (μ_{sat}), linear-regime mobility (μ_{lin}) and subthreshold swing (S) are calculated using standard equations (18) from the data in Figures 6A and 6B, yielding $I_{ON}/I_{OFF} = 2 \times 10^6$, $\mu_{sat} = 16.5$ cm^2/V-s, $\mu_{lin} =$ 4.9 cm^2/V-s, and S = 450 mV/decade (Figure 6C). Operating voltages ($\leq$ 8V) are signficantly lower than those for previous devices based on spin-coated tin(IV) chalcogenides (8), primarily as a result of the thinner (250 Å) gate insulator (19). The observed subthreshold swing can be compared with the theoretical lower limit of ~ 60 mV/decade at room temperature (18) and is similar in magnitude to that found in high-performance amorphous-silicon-based devices (20). While the characteristics presented in Figure 6 are among the best achieved during our studies, several other devices exhibited essentially identical characteristics. The primary factor limiting yield and device performance in the indium selenide channel study was gate leakage / breakdown through the relatively thin SiO_x insulator, which either led to devices with inferior performance or to source/drain-gate electrical shorts.

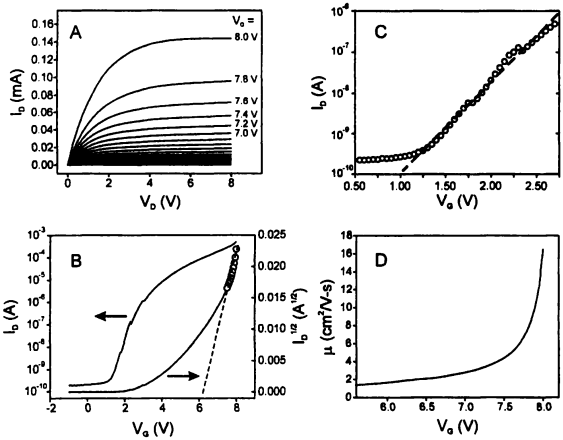


Figure 6. (A) Drain current, I_D, versus source-drain voltage, V_D, as a function of gate voltage, V_G, for the spin-coated indium selenide channel, having a channel length and width, L = 13 μm and W = 1500 μm, respectively (10). Source and drain contacts were patterned using mixed indium-gold evaporation. (B) Plots of I_D and $I_D^{1/2}$ versus V_G at constant V_D = 8 V, used to calculate current modulation, I_{on}/I_{off}, saturation regime mobility, μ_{sat}, and subthreshold swing, S, for the same device. The dashed line indicates the slope used to calculate mobility. (C) Zoomed in plot of I_D versus V_G in the subthreshold region. The dashed line shows the approximately logarithmic V_G dependence of I_D over several orders of I_D. (D) Gate voltage dependence of mobility, with the mobility progressively calculated in the saturation regime (using the data from Figure 6B) at various maximum values of V_G (19).

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Field-effect mobilities (μ_{sat}, μ_{lin}) have been calculated employing a standard approximation (18), which neglects gate-voltage dependence of mobility. In fact, as is also observed in polycrystalline organic and hybrid semiconductors (5,19), carrier mobilities are significantly V_G dependent (Figure 6D), presumably as a result of trap states in the In_2Se_3 film (e.g., arising from grain boundaries). Increasing V_G raises the number of accumulated charges available in the channel to fill localized traps. As the traps become filled, additional charges may transport with the intrinsic mobility of the delocalized semiconductor bands. Mobility saturation, which might be anticipated after the trap states become filled (19), is not observed for $V_G \leq 8V$ in the spin-coated In_2Se_3 channel layers and the calculated mobilities ($V_G \approx 8V$) are consistent with the lower end of the $20 \leq \mu \leq 60$ $cm^2/V\text{-}s$ Hall mobility range previously established in vacuum-evaporated polycrystalline In_2Se_3 films (21). These factors suggest that higher mobility values might be possible with application of higher dielectric constant gate insulators and/or by gaining better control over film grain structure and current injection from the source/drain contacts.

CONCLUSION

Ultimately, any technology developed to solution deposit thin films with mobility in the > 10 $cm^2/V\text{-}sec$ range needs to satisfy several criteria to be of practical importance for TFT applications (9). First, the technique must yield uniform and continuous films with ability to control film thickness. Second, the processing should be cheaper than polycrystalline silicon technology (the entrenched technology) for comparable mobility. The technology should also enable new niche technologies for pervasive computing, not readily achievable with traditional poly- or single-crystal silicon technology (e.g., low-cost solution-based deposition on cheap, flexible plastic substrates). Finally, improvement in mobility should not come at the expense of other important device parameters (e.g., on-off ratio, threshold voltage, subthreshold swing).

In this study, two related approaches have been highlighted to address solubility and film formation of inorganic semiconductors. In one approach, based on the low-temperature thermal decomposition of highly soluble hydrazinium-based precursors of metal chalcogenide semiconductors, the films are directly deposited from a hydrazine-based solution. In the second related approach, the steps of forming the hydrazinium precursor and spin coating are separated, enabling a wider choice of solvents for the hydrazinium precursor and the development of a process that is more compatible with a device fabrication standards. In each case, high quality thin film deposition has been demonstrated, along with application of these films for TFT channel layers. Despite the early stage of development, these spin-coated chalcogenide films have already yielded mobilities > 10 $cm^2/V\text{-}sec$, demonstrating the feasibility of achieving relatively high mobility films using a low-cost, high-throughput process. As for the organic semiconductors, which have undergone tremendous progress over the last 15 years, it is expected that the relatively young and highly promising field of solution-processed inorganic semiconductor will likewise yield many further exciting developments, enabling the solution deposition of films and device structures with outstanding characteristics.

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HYDROGEN-INDUCED DEFECTS IN POLY-SILICON THIN FILMS OBSERVED BY RAMAN SPECTROSCOPY

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ABSTRACT

Effects of hydrogenation on excimer-laser annealed polycrystalline silicon (poly-Si) for thin film transistors were investigated by using Hall effect and Raman spectroscopy. Down-stream plasma was used for hydrogenation. It was shown that the termination of dangling bonds at grain boundaries was almost completed in short time (1 min in this work) leading to the improvement of mobility and appearance of 2000 cm^{-1} band in Raman spectra. It was also shown that excess hydrogenation generates defects in grains resulting in the degradation of mobility and monotonous increase in 2100 cm^{-1} band intensity. Light exposure during hydrogenation enhances the 2100 cm^{-1} band intensity due to attacking of weak Si-Si bonds leading to the defects generation.

INTRODUCTION

Polycrystalline silicon (poly-Si) films have been extensively developed as a material of thin film transistors (TFT) on liquid crystal display panels. Excimer-laser annealed (ELA) poly-Si is especially useful owing to allowance of crystallization on glass substrates. Poly-Si films contain large density of defects at grain boundaries and in grains. It is known that hydrogenation terminates dangling bounds at defects leading to an improvement of TFT performance such as field-effect mobility and sub-threshold voltage (1). Beside intentional hydrogenation, there are several opportunities for exposure to hydrogen; those are plasma-enhanced chemical-vapor deposition (PE-CVD) of amorphous Si (a-Si) using H_2-diluted SiH_4, ion doping using PH_3 or B_2H_6, and in some case diffusion from under layer made from SiN_x.

Hydrogen atoms in Si act not only as the termination of defects but also as generation of defects. In the case of solar cell made from a-Si, several models are given for hydrogen-related defects, those are the weak-bond-dangling-bond conversion under thermal equilibrium (2) and light induced defects (3). In both cases, hydrogen atoms in a-Si break weak bonds leading to an increase in dangling bonds. For crystalline Si, it is

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reported that hydrogen-ion implantation generates vacancies with various structures (4) and hydrogen plasma generates hydrogen-stabilized platelets or micro-cracks (5). In the case of poly-Si thin films, however, effects of hydrogen are complicated and vary with crystallization conditions. So more detailed studies on hydrogen-induced defects are required.

We have investigated defects in poly-Si using Raman spectroscopy (6), (7). The width of the optical modes at ~520 cm^{-1} has been conventionally used to characterize defects. We also used local vibration modes (LVM) appearing after hydrogenation. For ELA poly-Si films, two bands were frequently detected at 2000 and 2100 cm^{-1}, which corresponds to bond-stretching mode of Si-H and is available for the analysis of different defects.

In this paper, hydrogen-induced defects in poly-Si thin films are investigated. The relationship between mobility and defects is shown. Defects are observed by Raman spectroscopy. Hydrogen and light induced defects are examined to compare the weak-bond model for a-Si:H.

EXPERIMENTAL

As a starting material of poly-Si, a-Si films (50 nm thick) were deposited on glass or quartz substrates by PE-CVD followed by dehydrogenation and annealing with KrF or XeCl excimer laser. Down-stream plasma was used for hydrogenation. The merit of this technique is low damage owing to no electrical acceleration of ions and electrons. Hydrogenation was performed at substrate temperature of 350°C under the hydrogen pressure of ~1 Torr. Light exposure during hydrogenation was performed by using a 150 W-Xe lamp with a fused silica window. Electrical properties were characterized by Hall effect measurement using van der Pauw method. To obtain a conductivity required for the measurement, P-ions were doped to poly-Si with a dose of 5×10^{13} cm^{-2} followed by activation at 600°C for 2 min in N_2. Raman spectroscopy was performed with back scattering geometry using Ar ion laser (514.5 nm) for excitation. Unintentional doped films were also used for Raman spectroscopy. Typical spectra for the optical mode and local-vibration modes obtained for poly-Si were shown in elsewhere (7).

RESULTS AND DISCUSSION

Mobility and Width of the Optical Mode

Figures 1 and 2 show variation of mobility and width of the optical mode with hydrogenation time, respectively. The carried density of hydrogenated films was n=2-3×

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10^{18} cm^{-3}. The mobility was remarkably improved by hydrogenation for so short as 1 min. Then the mobility was gradually degraded by longer time hydrogenation. Such variation of mobility was also obtained for the previous examination (8). The width of the optical mode is once decreased at 1 min and gradually increased by longer time hydrogenation. Therefore, it is expected that there are two factors. One is decrease in defects appearing as the narrowing of the peak width, which leads to the improvement of mobility. The other is increase in defect density appearing as broadening of the peak. Those defects act as scattering centers causing the degradation of mobility.

It is known that hydrogen atoms in a-Si increase structural order leading to narrowing of the transverse-optical (TO) mode peak (9). The slight reduction of the peak width by short time hydrogenation in Fig. 2 suggests that the structure ordering by hydrogen is caused also in poly-Si.

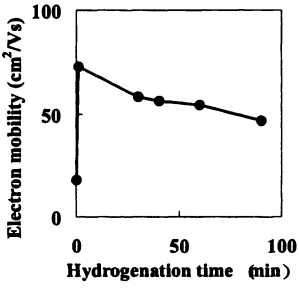


Fig. 1 Variation of electron mobility with hydrogenation time.

Defects and Local-Vibration Modes

Relationship between LVM intensity and hydrogenation time is shown in Fig. 3. The 2000 cm^{-1} band intensity, I_{2000}, nearly saturates at a short time, which corresponds to finish of the termination of dangling bonds in as-crystallized films. The variation of I_{2000} with excimer-laser energy density, E_L, is shown in Fig. 4, where grain size is also plotted in this figure. I_{2000} decreases with increase in E_L while little variation with hydrogenation time was found. On the other hand, the grain size increases with increase in E_L. Thus, it is expected that this band is associated with grain boundary density. Results for several other experiments are consistent with this expectation (6), (7). Therefore, it is deduced that both the improvement of mobility and the appearance of the 2000

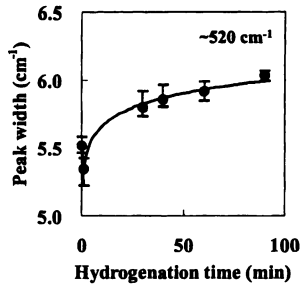


Fig. 2 Variation of the optical mode width with hydrogenation time.

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cm^{-1} band is due to the termination of dangling bonds at grain boundaries.

The correlation with E_L and grain size has been also demonstrated for spin density in ELA poly-Si by electron spin resonance (10), where it was mentioned that the spin density decreases with hydrogenation. Therefore, it is deduced that dangling bonds at grain boundaries before and after the termination with hydrogen are detected as spin density and 2000 cm^{-1} band, respectively.

The behaviors of the 2100 cm^{-1} band are relatively complex. The 2100 cm^{-1} band intensity, I_{2100}, monotonously increases with time as shown in Fig. 3. So, this band is related to defects generated by hydrogenation. Figure 5 shows the variation of I_{2100} with E_L. At the high energy density, I_{2100} increases with the hydrogenation time as well as in Fig. 3. On the contrary at the lowest energy density, I_{2100} is large even for short time hydrogenation and exhibits little time dependence. In this case, this band is related to termination of defects existing in as-crystallized film. Thus two origins are given for the 2100 cm^{-1} band. Viewing the plots for long time hydrogenation in Fig. 5, variation of I_{2100} with E_L is little. Thus, it is deduced that the 2100 cm^{-1}-related defects exist rather in grains than at grain boundaries.

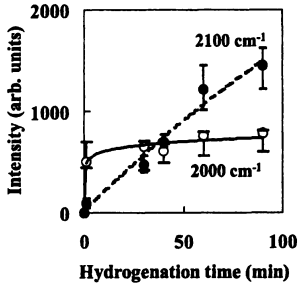


Fig. 3 Variation of the local-vibration mode intensity with hydrogenation time.

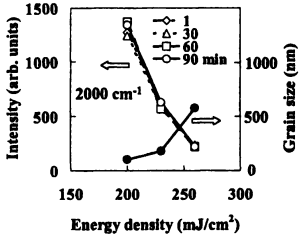


Fig. 4 Relationship between 2000 cm^{-1} band intensity and excimer laser energy density. Grain size for individual energy densities is also plotted. Hydrogenation was performed with four different times.

The 2100 cm^{-1} band in a-Si and crystalline Si has been assigned to defects with some structures; those are Si-H bonds at relatively large voids (11) and crystallographic planes (5), respectively. For poly-Si films, we have related the 2100 cm^{-1} band to atomic vacancies left by rapid cooling after excimer-laser irradiation (7). It is because this band was not observed in films crystallized by furnace anneal under various conditions. Taking those works and present results into consideration, it is supposed that the excess hydrogenation attacks vacancies in as-crystallized films and generates defects with

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some crystallographic structure in grains.

Hydrogen and Light Induced Defects

The generation of defects associated with hydrogen has been known for a-Si:H. It was reported that long exposure to light decreases both the photoconductivity and dark conductivity of a-Si:H (3) and the light-induced defects are created through a breaking of weak Si-Si bonds in the region containing clustered hydrides (12). Assuming that the hydrogen-induced defects in poly-Si is also due to the break of weak bonds in grains, it is expected that light exposure enhances the generation of hydrogen-induced defects in the same manner as a-Si:H. Thus, hydrogenation with and without light exposure was examined for poly-Si films cut from the same specimen.

Typical spectra of LVM were shown in Fig. 6. The 2000 cm^{-1} band is dominant in the film hydrogenated without light exposure. On the contrary, the 2100 cm^{-1} band becomes to be dominant with light exposure. Figure 7 shows the variation of I_{2000} and I_{2100} with light exposure, where mean values of three positions on individual films are shown. While the

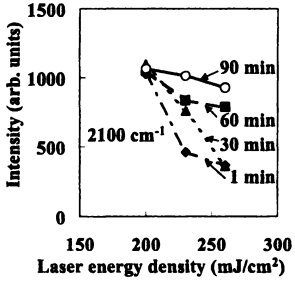


Fig. 5 Relationship between 2100 cm^{-1} band intensity and excimer laser energy density.

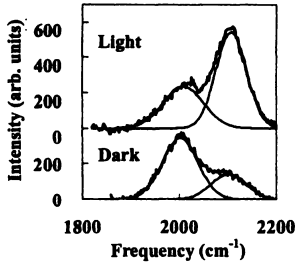


Fig. 6 Spectra of local-vibration modes for ELA poly-Si hydrogenated with and without light exposure during hydrogenation.

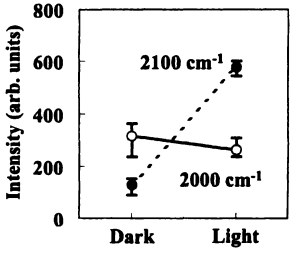


Fig. 7 Variation of intensity of 2000 and 2100 cm^{-1} bands with light exposure during hydrogenation.

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variation of I_{2000} is little, I_{2100} is obviously increased by light exposure. Therefore it is deduced that light exposure during hydrogenation enhances the attacking of weak Si-Si bonds in the vicinity of vacancies leading to increase in the 2100 cm^{-1} band-related defects.

CONCLUSIONS

The hydrogenation-induced defects in ELA poly-Si were investigated by Hall effect and Raman spectroscopy. Suitable hydrogenation, that is 1 min in present work, causes improvement of mobility, narrowing the optical mode and appearance of 2000 cm^{-1} band. Those are attributed to the termination of dangling bonds at grain boundaries with hydrogen atoms. Excess hydrogenation causes degradation of mobility, broadening of the optical mode and enhancement of I_{2100}. Those are attributed to the generation of hydrogen-induced defects in grains. On the basis of the light exposure effects during hydrogenation, it was deduced that the generation of defects is attributed to the attack of weak Si-Si bonds in the vicinity of vacancies by hydrogen atoms in the same manner as in a-Si:H.

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ANALYSIS OF TRASFER MECHANISM IN SURFACE FREE TECHNOLOGY BY LASER ANNEALING / ABLATION (SUFTLA™)

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ABSTRACT

We developed a new technology which we have named SUFTLA™. This technology enables the transfer of thin film devices from an original substrate to another substrate. An a-Si film exfoliation layer is deposited on an original substrate, upon which thin film devices consisting of low-temperature processed polycrystalline-silicon thin film transistors (poly-Si TFTs) are subsequently fabricated. After the completion of thin film devices, an XeCl excimer laser irradiates the exfoliation layer from the back side of the original substrate, causing the exfoliation layer to melt and release hydrogen. The evaporation pressure reduces the adhesion between the exfoliation layer and substrate. In addition, the number of dangling bonds is increased and a large number of voids are generated in the exfoliation layer. This phenomenon also reduces the adhesive force and adhesive area. As a result, the transfer of thin film devices can be accomplished from an original substrate to another substrate.

INTRODUCTION

The progress of digital information technology requires high performance flat panel displays in order to supply more information and precise images. TFT liquid crystal display (TFT-LCD) technology is the dominant technology for such displays. Two types of TFT-LCD are currently in practical production. One is an amorphous silicon TFT (a-Si TFT) panel and the other is a poly-Si TFT panel. Poly-Si TFTs are further classified into two types: high temperature processed poly-Si TFTs and low temperature

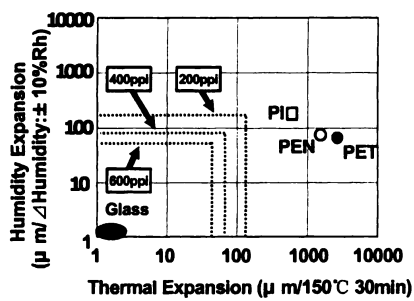


Fig. 1. Expansion of 300 mm x 300 mm plastic films. The horizontal axis is the thermal expansion and the vertical axis is humidity expansion. Types of plastic films are PI, PEN and PET.

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processed poly-Si TFTs. The advantage of poly-Si TFTs is their high performance. In general, electron mobility is approximately 100 $cm^2V^{-1}s^{-1}$ or more, and CMOS configuration is also applicable. These characteristics enable the integration of driver circuits in the panels. In the case of low temperature processed poly-Si TFTs, the maximum process temperature is below 600°C. Therefore, TFT-LCDs with integrated drivers can be fabricated on conventional glass substrates. We succeeded in developing the world's first TFT-LCDs with integrated drivers using low temperature processed poly-Si TFTs (1).

Current research is focused on new applications using low temperature processed poly-Si TFTs (2)-(3). If we can fabricate TFTs on flexible substrates such as plastic films, thin electronic devices that are lightweight, robust, and flexible can be envisaged. Researchers around the world have been investigating technologies for manufacturing poly-Si TFTs on plastic films. The main approach has been to fabricate TFTs directly on plastic films (4)-(5) by reducing the maximum process temperature to below 200°C. However, it is difficult to form high quality films for gate insulators and channel silicon layers at low temperatures, which result in reduced TFT performance. In addition, the expansion and flexibility of plastic films cause a serious problem. Figure 1 shows the expansion of plastic films measuring 300 mm x 300 mm. The horizontal axis is the thermal expansion and the vertical axis is humidity expansion. The plastic films are made of PI, PEN and PET. In all cases, the expansion values are larger than the pixel size of the 200 ppi display. That means it is impossible to realize large, high-resolution displays when TFTs are directly fabricated on plastic films.

In 1996, T. Sameshima reported that aluminum thin film can be peeled from a glass substrate by laser irradiation and predicted that TFTs could be transferred from a glass substrate to another substrate (6). We have investigated new technology that enables TFTs and TFT devices to be transferred from the original substrate to any secondary substrate (7)-(8). This technology, which was termed SUFTLA™ (surface free technology by laser annealing/ablation), has enabled us to successfully transfer TFTs and TFT circuits. We were able to use this technology to fabricate the world's first all-plastic substrate TFT-LCDs (9)-(11) and TFT light-emitting polymer displays (TFT-LEPDs) (12)-(13). Since TFTs can be fabricated on glass or quartz substrates, we do not have to reduce the maximum process temperature or find the best plan for the expansion of substrates. In this paper we discuss the transfer mechanism and the optimum laser energy density in SUFTLA™ technology (14)-(15).

SUFTLA™ PROCESS

First Transfer Process

Figure 2 shows the SUFTLA™ process sequence. First, a 100-nm a-Si film is deposited as an exfoliation layer by chemical vapor deposition (CVD) on a glass substrate. This glass substrate is the "original substrate." After that, the CMOS poly-Si TFTs are fabricated on the exfoliation layer by using a low-temperature process. The maximum temperature is less than 425°C (16). The original substrate with the CMOS poly-Si TFTs is glued onto a second glass substrate using a temporary adhesive. The second glass substrate is called the "first transfer substrate," and the adhesive is

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water-soluble and stiffened in UV light. Next, the original substrate is irradiated from the back side with an XeCl excimer laser, causing the exfoliation layer to melt and release hydrogen, since a-Si film deposited by CVD contains hydrogen in several %. This phenomenon reduces the adhesion between the exfoliation layer and the original substrate, enabling TFTs to be detached from the original substrate [Figure 2(a)]. The transfer mechanism is discussed in detail later.

The wavelength of the XeCl excimer laser is 308 nm, and the light absorption coefficient of silicon film at 308 nm is 1.8×10^{-1} nm^{-1}. Thus the XeCl excimer laser beam is almost completely absorbed into a silicon film of 5.6 nm, and the TFTs are not damaged by laser irradiation in the SUFTLA™ process.

Second Transfer Process

The first transfer substrate to which the TFTs were transferred is glued onto a second transfer substrate using a permanent adhesive. This adhesive is non-water-soluble and also stiffens in UV light. We used plastic film for the second transfer substrate [Figure 2(b)]. The bonded first transfer substrate and second transfer substrate are then cut and soaked in water. Since the water-soluble adhesive dissolves in water, the TFTs are peeled from the first transfer substrate while remaining on the second substrate [Figure 2(c)]. In this way, TFTs and TFT-devices can be transferred from the glass substrate to plastic film.

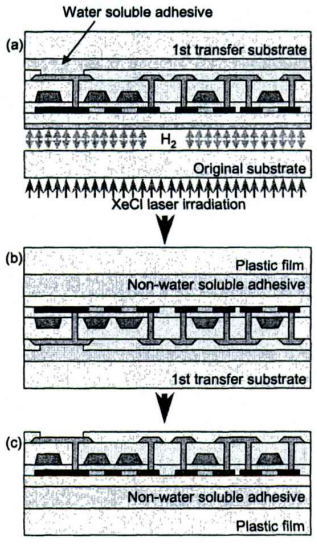


Fig. 2. SUFTLA™ process sequence.

Poly-Si TFT backplanes for LEPD with integrated drivers were successfully transferred from glass substrates to plastic film. Figure 3 shows a photograph of a TFT backplane after the transfer (12). These results indicate that SUFTLA™ technology has the potential to realize new electronic devices manufactured on plastic film.

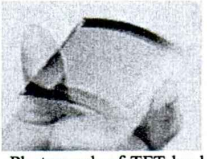


Fig. 3. Photograph of TFT backplane for LEPD with integrated drivers after the transfer. The display measures 5.3 cm diagonally and has 200 x 150 pixels.

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RESULTS AND DISCUSSION

Transfer Mechanism of SUFTLA™ Process

Next, we investigated the transfer mechanism in the SUFTLA™ process and made the following samples. A 100 nm electron cyclotron resonance CVD (ECR-CVD) SiO_2 film (bottom SiO_2 layer), a 100 nm plasma enhanced CVD (PE-CVD) a-Si film (an exfoliation layer) and a 500 nm ECR-CVD SiO_2 film (upper SiO_2 layer) were deposited on quartz substrates in a sequential manner. The films were then annealed at 450°C for 2 hours, and an XeCl excimer laser irradiated the back side of the substrates. The properties of a-Si film were evaluated before and after the laser irradiation. Since it is difficult to evaluate the property of exfoliation layer after ablation, the irradiated laser energy density was just below the laser energy density that causes ablation. Therefore, the a-Si layer was sometimes changed into a poly-Si layer due to laser irradiation.

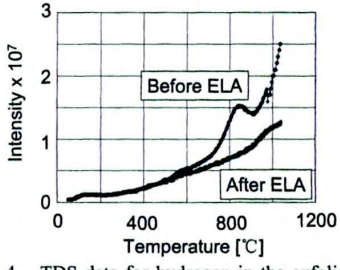


Fig. 4. TDS data for hydrogen in the exfoliation layer before and after the laser irradiation. Prior to TDS analysis, the upper SiO_2 layer was removed.

Concentrations of hydrogen in the exfoliation layer before and after the laser irradiation were measured by means of thermal desorption spectroscopy (TDS). Prior to TDS analysis, the upper SiO_2 layer was removed. As shown in Figure 4, a peak of intensity for hydrogen is observed at about 850°C before laser irradiation. On the other hand, this peak disappears after laser irradiation. It can be assumed that hydrogen is released from the silicon layer due to the laser irradiation. In the range below 500°C, hydrogen intensities are nearly the same before and after the laser irradiation. It is thought that hydrogen is released during the 450°C annealing, so laser irradiation causes no significant change.



Fig. 5. ESR data on the exfoliation layers before and after the laser irradiation. The upper SiO_2 layer was also removed as same as the case of TDS analysis.

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The exfoliation layers were also analyzed by ESR (electron spin resonance) after the upper SiO_2 layer was removed, as in the case of TDS analysis. The result is shown in Figure 5. The spin densities are 1.39 x 10^{18} cm^{-3} before laser irradiation, and 2.34 x 10^{18} cm^{-3} after laser irradiation. That is, the spin density increased twofold due to the laser irradiation. The g values were nearly 2.005 (2.0046 before laser irradiation and 2.0044 after laser irradiation), which corresponds to the value for dangling bonds of silicon. These results indicate that hydrogen bonded with silicon is released due to the laser irradiation and the dangling bonds are increased in the exfoliation layer.

Figure 6(a) and Figure 6(b) show cross-sectional TEM (transmission electron microscopy) images of the exfoliation layers before and after the laser irradiation, respectively. Uniform interfaces can be observed between the exfoliation layer and SiO_2 layers before laser irradiation. Conversely, numerous voids are observed in

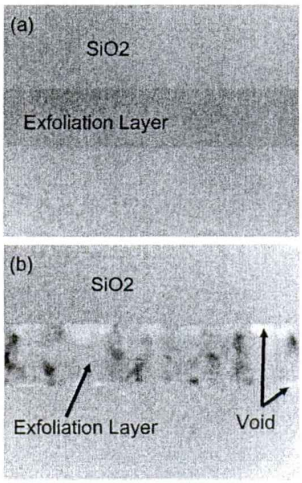


Fig. 6. Cross sectional TEM image of the exfoliation layers.
(a) before laser irradiation.
(b) after laser irradiation.
Numerous voids are observed in the exfoliation layer and at the interfaces between the exfoliation layer and SiO_2 layers after laser irradiation.

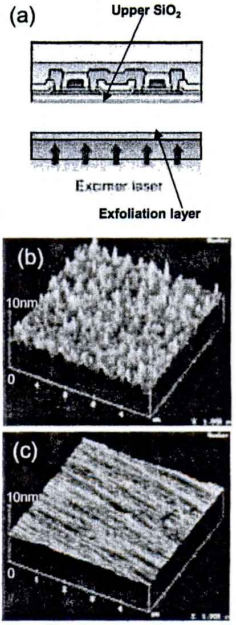


Fig. 7. Surface roughness of the exfoliation interface after the first transfer process, as measured by AFM.
(a) Structure of the sample. Detachment occurred at the interface between the exfoliation layer and upper SiO_2 layer.
(b) Roughness of the top surface in exfoliation layer (Ra = 0.56 nm).
(c) Roughness of the back surface in upper SiO_2 layer (Ra = 0.27 nm).

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the exfoliation layer and at the interfaces between the exfoliation layer and SiO_2 layers after the laser irradiation. This phenomenon can be considered as follows. Irradiating the exfoliation layer with the laser causes it to melt and release hydrogen, inducing bubbles in the exfoliation layer. Since crystallization occurs very rapidly (in several tens of nanoseconds), voids are generated in the exfoliation layer and at the interfaces between the exfoliation layer and SiO_2 layers.

We fabricated CMOS TFT circuits on the exfoliation layer and measured the surface roughness of the exfoliation interface after the first transfer process by using atomic force microscope (AFM). Figure 7(a) shows the structure of the sample. The detachment occurred at the interface between the exfoliation layer and the upper SiO_2 layer. Figure 7(b) shows the roughness of the top surface in the exfoliation layer, and Figure 7(c) shows the roughness of the back surface in the upper SiO_2 layer. It was confirmed that the surface of the exfoliation layer is rough (Ra = 0.56 nm). On the contrary, the surface of the SiO_2 layer remains smooth (Ra = 0.27 nm). This result corresponds to the data of TEM images shown in Figure 6(a) and Figure 6(b).

These data enable us to conclude that the transfer mechanism is as follows. The laser irradiation causes the exfoliation layer to melt and release hydrogen. The evaporation pressure at this time reduces the adhesion between the exfoliation layer and substrate. In addition, the number of silicon dangling bonds is increased, and a large number of voids are generated in the exfoliation layer and at the interfaces between the exfoliation layer and SiO_2 layers due to the laser irradiation. These phenomena also reduce the adhesive force and adhesive area between the exfoliation layer and substrate. Thanks to this mechanism, the detachment of TFTs and TFT devices are accomplished.

Optimum Laser Energy Density in the SUFTLA™ Process

The minimum laser energy density required for exfoliation layer ablation is a vital value in terms of optimizing the laser energy density in the SUFTLA™ process. The transfer is accomplished by ablating the exfoliation layer, and there is a strong correlation between the optimized laser energy density in the SUFTLA™ process and the minimum laser energy density required for exfoliation layer ablation.

It was empirically confirmed that there was a relationship between the minimum laser energy density for ablation and the hydrogen concentration in the exfoliation layer. For example, the

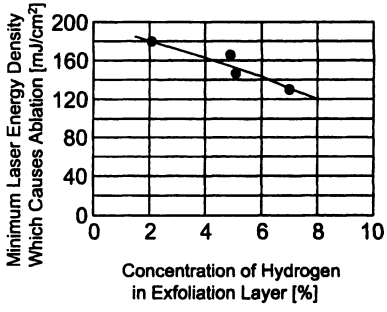


Fig. 8. Relationship between hydrogen concentration in the exfoliation layer and the minimum laser energy density which causes the ablation. When hydrogen concentration is 2.1%, the minimum laser energy density is about 180 mJ/cm^2. The minimum laser energy density declines as the hydrogen concentration rises, reaching 130 mJ/cm^2 at a hydrogen concentration of 7%.

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optimum laser energy density for the a-Si exfoliation layer deposited by PE-CVD is lower than that for the a-Si exfoliation layer deposited by low pressure CVD (LP-CVD). In general, the hydrogen concentration of the a-Si exfoliation layer deposited by PE-CVD is higher than that of the a-Si exfoliation layer deposited by LP-CVD.

We investigated the relationship between the hydrogen concentration in the exfoliation layer and the minimum laser energy density required for ablation by conducting the experiments described below. The 100-nm a-Si films were deposited on quartz substrates by PE-CVD. Some of the samples were then annealed for 2 hours at temperatures ranging from 300°C to 450°C. The concentrations of hydrogen were measured by TDS following annealing. We found that the as-deposited a-Si film contained hydrogen of 3.49×10^{21} molecules per cubic centimeter; that is, a hydrogen concentration of about 7%. The hydrogen concentration declined as the annealing temperature increased, and the number of molecules of hydrogen in a cubic centimeter decreased to 1.05×10^{20} – or about 2.1% – in the case of a-Si film annealed at 450°C.

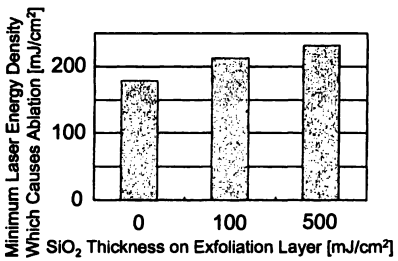


Fig. 9. Relationship between SiO_2 thickness on the exfoliation layer and the minimum laser energy density which causes the ablation.

Next, an XeCl excimer laser was used to irradiate these a-Si films from the back side of the substrate, and each sample was evaluated to determine the lowest laser energy density that would cause ablation. Figure 8 shows the relationship between hydrogen concentration in the exfoliation layer and the minimum laser energy density for ablation. When the hydrogen concentration is 2.1%, the minimum laser energy density is about 180 mJ/cm^2. The minimum laser energy density declines as the hydrogen concentration rises, reaching 130 mJ/cm^2 at a hydrogen concentration of 7%.

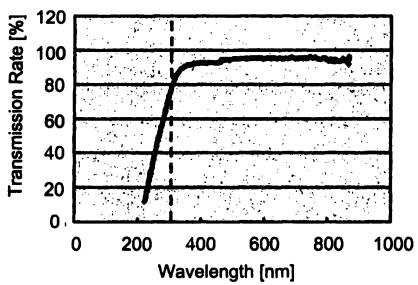


Fig. 10. Light transmission rate of a glass substrate that we usually use. The light transmission rate is about 80% at a wavelength of 308 nm.

We also found that the optimum laser energy density in the SUFTLA™ process changed with the thickness of the SiO_2 layer on the exfoliation layer. This phenomenon was also investigated due to the following experiment. The 100-nm a-Si films were

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deposited on quartz substrates by PE-CVD, and the films were annealed at 450°C for 2 hours. Following this, some samples were produced by depositing 100 nm SiO_2 films and 500 nm SiO_2 films in a sequential manner on the a-Si films. ECR-CVD was used to deposit SiO_2 films. After the samples were completed, an XeCl excimer laser was used to irradiate the a-Si films from the back side of the substrate, and the minimum laser energy densities required for ablation were evaluated. We confirmed as a result that the minimum laser energy density increased along with the thickness of the SiO_2 on the a-Si film, as shown in Figure 9. The minimum laser energy density is about 180 mJ/cm^2 when there is no SiO_2 film on the a-Si film. On the other hand, it increases to 230 mJ/cm^2 when a 500 nm SiO_2 is present on the a-Si film.

Finally, the optimum laser energy density is also dependent on the type of substrate, as each type of substrate has a different light transmission rate. A quartz substrate has a light transmission rate of about 90%. Glass substrates, on the other hand, have different light transmission rates. Figure 10 shows the light transmission rate of the type of glass substrate that we usually use. In this case, the light transmission rate is about 80% at a wavelength of 308 nm.

These data enable us to conclude that the optimum laser energy density in the SUFTLA™ process is strongly dependent on the hydrogen concentration in the exfoliation layer, on the conditions of layers that are formed on the exfoliation layer, and on the type of substrate used. The laser energy density in the SUFTLA™ process is usually determined so as to be several tens mJ/cm^2 higher than the minimum laser energy density required for ablation in the exfoliation.

CONCLUSION

We have discussed the transfer mechanism and the optimum laser energy density in SUFTLA™ technology. There is a strong relationship between the transfer mechanism and the hydrogen contained in the exfoliation layer. The laser irradiation causes the exfoliation layer to melt and release hydrogen. The evaporation pressure at that time reduces the adhesion between the exfoliation layer and substrate. In addition, the number of silicon dangling bonds is increased, which reduces the adhesive force between the exfoliation layer and substrate. Furthermore, a large number of voids are generated in the exfoliation layer and at the interfaces between the exfoliation layer and SiO_2 layers due to the laser irradiation. Therefore, the adhesive area between the exfoliation layer and substrate is reduced, resulting in reduced adhesive force. In this way, TFTs and TFT devices can be detached from the original substrate and transferred to another substrate. It was also verified that the optimum laser energy density in the SUFTLA™ process was influenced by the concentration of hydrogen in the exfoliation layer, by the conditions of layers on the exfoliation layer, and by the type of substrate used.

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HIGH MOBILITY TOP-GATE MICRO-CRYSTALLINE SILICON TFTs PROCESSED at LOW TEMPERATURE (<200°C)

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ABSTRACT

N type top gate microcrystalline silicon thin film transistors (TFTs) are fabricated on glass substrates at a maximum temperature of 200°C. The active layer is an undoped μc-Si film, 200 nm thick, deposited by PECVD. The drain and source regions are highly phosphorus (N-type TFTs) doped μc-films deposited also by PECVD. The gate insulator is a silicon dioxide film deposited by RF sputtering. Al-SiO_2- N type c-Si structures using this insulator present low flat-band voltage, -0.2V, and low density of states at the interface D_{it}=6,4 x 10^{10} $eV^{-1}cm^{-2}$. High electron field effect mobility, 40 $cm^2/V.s$, is obtained. The sub-threshold slope is as low as 0.4 V/dec.

INTRODUCTION

High quality electronic devices processed at low temperature on foreign substrates becomes now a real challenge. The field effect transistor, that is the basic element in electronics, is extensively studied to validate different low temperature technological process. Intrinsically hydrogenated amorphous silicon (a-Si:H) is the most appropriate candidate as active material to built these electronic devices. It can be deposited at very low temperature compatible with the use of plastics substrates. a-Si:H based thin film transistor (TFT), fabricated on glass substrate, is studied since about 20 years. Practically, it is used in a large extent to switch the pixels of Liquid Crystal Displays that are used in different applications, from cellular phones to TV. However, its use in other applications is more problematic. In fact it suffers from 2 drawbacks. The very low hole mobility avoids any CMOS possibility and the large shift of its characteristics under functioning eliminates any application where the parameters have to be well controlled.

To overcome these drawbacks, the use of microcrystalline silicon (μc-Si) can be considered as a serious alternative. It is deposited in the same temperature range as a-Si:H. It is much more stable under functioning. The electron mobility is much higher. The hole mobility passed beyond 1 $cm^2/V.s$ [1] very lastly and can be improved more in near future.

Here, the electron mobility of n-type μc-Si TFTs is addressed to improve it more. To improve the characteristics of a field effect transistor, we have to keep in mind that the performance of an electronic device depends on the quality of the materials and the interfaces. For example, the parameters of a field effect transistor depend on the quality of the active material, the gate insulator, the conductivity of the

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doped regions and more important the interface between the active material and the gate insulator where the channel forms.

In this paper, undoped μc-Si that it is used as active layer and N-type doped μc-Si that constitutes the source and drain regions are deposited by PECVD at 165°C. Silicon dioxide film, that acts as gate insulator, is deposited by RF sputtering and then submitted to a plasma post-treatment without heating the substrate holder. Aluminium / RF sputtered SiO_2 / single crystalline silicon wafer MIS structures are used to check the insulator quality of the SiO_2 film.

EXPERIMENTAL

To have some chance to succeed in the goal to fabricate high performance TFTs, we have to optimize the deposition conditions at low temperature of the gate insulator, silicon dioxide, the undoped μc-Si active layer, the doped μc-Si source and drain regions.

SiO_2 films are first deposited by RF sputtering of SiO_2 target using an Ar/O_2 mixture and without heating the substrate holder, so the temperature reached by the film during deposition is about 80°C. Capacitance measurements of aluminum / RF sputtered SiO_2 / single crystalline silicon wafer MIS structures are used to optimize the deposition and post-treatment conditions.

Then, N type top gate TFTs have been processed using 200 nm-thick microcrystalline silicon (μc-Si:H) film as active layer. The deposition is performed by PECVD. 2x2 square inch glass covered with 200 nm Atmospheric Pressure CVD (APCVD) deposited SiO_2 are used as substrate.

The configuration of the TFTs is presented in Fig. 1. The process [2] begins by the deposition of a stack of undoped and n-type doped silicon films. Then, the doped film is plasma etched to form the source and drain regions. The next step is the deposition of 100 nm-thick SiO_2 layer by RF sputtering in the conditions previously optimized. Source and drain contacts are opened through gate insulator and finally aluminum is thermally evaporated and patterned to form the source, drain and gate electrodes. Post-metallization annealing is performed at 200°C in an atmosphere of forming gas. The maximum temperature reached during the process is 200°C that is compatible with the use of many plastics substrates as Kapton E polyimide.

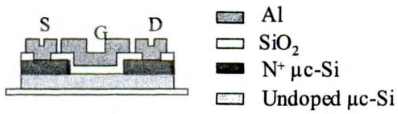


Fig. 1: Cross-section of the *in-situ* doped micro-crystalline silicon (μc-Si) TFT's

Before the TFT fabrication, the deposition conditions of undoped as well as doped μc-Si films are optimized to get the highest crystalline fraction that insures the electrical quality of the undoped films and the efficiency of the doping for the doped layer. During this optimization, the temperature of the substrate was kept at 165°C that is low enough to be compatible with the use of plastics substrates. Raman spectroscopy is used to determine the crystalline fraction. The data are taken at room temperature using the 514.5 nm line of an argon laser. A very low laser power, 20 mW, is used to avoid any structural change during the irradiation.

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In the optimized conditions; the undoped film is deposited at a power of 20 W, a pressure of 0.9 mbar, a silane flow of 1.5 sccm, an hydrogen flow of 50 sccm and an argon flow of 100 sccm. When the film thickness reaches 200 nm, the doping arsine gas is introduced with a flow of 10 sccm without stopping the deposition. Then the doped layer grows starting from the crystallized undoped layer. The deposition is stopped when the thickness of the doped layer reaches 200 nm.

RESULTS

Optimization of the SiO_2 deposition and post-treatment.

SiO_2 films are deposited by RF sputtering of SiO_2 target using an Ar/O_2 mixture and without heating the substrate holder. Then, the main deposition parameters are : the RF power and the O_2 dilution. To check the effect of these 2 parameters, aluminum / RF sputtered SiO_2 / N-type single crystalline silicon wafer (Al-SiO_2-Si) MIS structures are fabricated. These structures are submitted to a forming-gas annealing at 200°C during 1 hour. The characteristics capacitance-bias (C-V) is measured at high frequency (1MHz), HF-CV, and in the quasi-static regime QS-CV. High quality silicon dioxide can be characterized qualitatively by :

- clear saturation of the quasi-static capacitance
- same insulator capacitance in both the accumulation and the inversion regimes
- HF-CV and QS-CV identical in the depletion and accumulation regimes
- deep minimum of the QS C-V curve
- low flat-band voltage V_{FB}

Taking into account these criteria, both high RF power and O_2 dilution have beneficial effect. However they are not sufficient. H_2+O_2 plasma post-treatment is needed to improve really the C-V characteristics and then the quality of the insulator. Fig. 2 shows the final C-V characteristics at 1MHz and in the quasi-static regime at the end of the optimization. The fifth criteria can be considered as fulfilled.

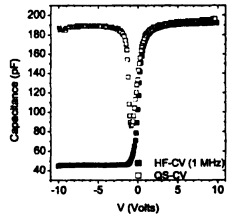


Fig. 2 : Optimized C-V characteristics at 1MHz and in the quasi-static regime. The figure highlights the saturation of the QS curve, the same capacitance in both the accumulation and the inversion regimes, the fit between HF-CV and QS-CV curves in the depletion and accumulation regimes, the deep minimum of the QS curve and finally the low flat-band voltage V_{FB}. The thickness of the insulator is 67 nm in this case.

The optimized deposition and post-treatment parameters are : 200W RF power, 30% O_2 dilution, and H_2+O_2 plasma post-treatment during 15 minutes. In these conditions the flat-band voltage V_{FB} is -0.2V. The calculated density of states D_{it} at

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the interface is 6,4 x 10^{10} $eV^{-1}cm^{-2}$.All the C-V characteristics, the low flat-band voltage and the low density of states highlights the very high quality of the present sputtered silicon dioxide fabricated at a temperature maximum of 200°C that is reached during the final annealing. The temperature is fully compatible with the goal to make electronics on plastics substrates.

Optimization of the crystalline quality of the undoped µc-Si layer

The transverse optic (TO) mode peak of the optimized undoped film is shown in Fig. 2. It has an asymmetric shape with a slight absorption in the low energy part. As usual, it can be fitted by 3 Gaussian peaks that corresponds to the crystalline band at 520 cm^{-1} , the amorphous band at 480 cm^{-1} and an intermediate peak that is attributed usually to low sized crystallites. The crystalline fraction, X_C, is taken as the ratio of the sum of the areas of the two crystalline phase peaks to the total area of the TO peak. X_C is found to be 73%. Here, we do not take into account the ratio of the cross section of the crystalline phase to that of the amorphous phase. Its value is subjected to caution as it can vary from 0.9 to 0.7 depending on the crystallite size [3]. Then the value of X_C, given in this work, is under-estimated.

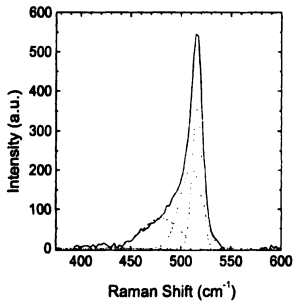


Fig 2. : Raman TO peak of undoped µc-Si film deposited in the optimized conditions.

Optimization of the conductivity of the arsenic doped µc-Si layer

The deposition conditions are optimized to insure the lowest resistive arsenic doped µc-Si layer that acts as source and drain contacts. In this optimized conditions, the sheet resistance reaches 2355 Ω/□ for a 200 nm thick layer. Then the resistivity is 4.7 10^{-2} Ω cm.

Thin Film Transistors Characteristics

Using all the previous optimizations, TFTs are then fabricated and characterized at 300K using a HP4155A semiconductor parameter analyzer. The threshold voltage V_T, the transconductance g_m and the subthreshold slope S are determined from the measured transfer characteristics. V_T is determined in the linear mode by a linear extrapolation on the V_G-axis of the drain current I_D versus gate voltage V_G curve. µ is determined from the maximum slope of this curve that is g_m. S is the minimum reverse slope of the transfer characteristic ($\partial V_{GS}/\partial \log I_{DS}$) measured in the switching region.

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Figure 3 shows transfer characteristics of the N-type μc-Si TFTs measured at 1V drain voltage. The minimum off-current is under the low limit of the measurement. Excellent swing is highlighted by the steep increase of the current. The electrical parameters calculated from these characteristics are given in Table 1.

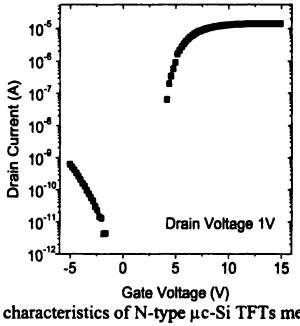


Figure 3 : Transfer characteristics of N-type μc-Si TFTs measured at 1V drain voltage.

on to off current ratio	Subthreshold slope	Threshold voltage	Electron mobility
$>> 10^7$	0.3 V/dec	4.9 V	40 $cm^2/V.s$

Table 1 : Electrical parameters of the N-type μc-Si TFT deduced from the transfer characteristics of Figure 3.

The electron mobility is definitively high for μc-Si TFTs. It highlights the quality of the present process that it was improved through the quality of the silicon films, the silicon dioxide, the interface between these two layers, and the technological steps.

CONCLUSION

Full N-type microcrystalline silicon TFT's process was presented. It uses undoped and doped microcrystalline silicon films deposited by PECVD at 165°C. The temperature were chosen to be compatible with plastics substrates.

Silicon dioxide acting as gate insulator was deposited by RF sputtering without heating the substrate. The deposition process was optimized through the parameters of Al/sputtered SiO_2/N-type single crystalline structures.

Very high field effect mobility, 37 $cm^2/V.s$, low subthreshold slope and threshold voltage were obtained. These excellent results are due to the quality of the silicon films, the silicon dioxide, the interface between these two layers, and to the technological steps. Particularly the quality of the interface μc-Si/ sputtered SiO_2 has to be precisely characterized to better understand the previous improvements.

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POLYSILICON TFTS ON PLASTIC

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This paper describes an innovative ultra-low temperature poly-silicon TFT process on plastic substrates. Key technologies includes near room-temperature silicon and oxide deposition steps, laser crystallization and dopant activation. Manufacturing issues related to plastic material compatibility in a TFT process are reviewed. Lamination and de-lamination of plastic wafers to glass carrier wafers for manufacturability is discussed. An active matrix TFT backplane will be fabricated with an OLED (Organic Light Emitting Diode) display to demonstrate this technology.

INTRODUCTION

Currently, amorphous silicon thin film transistors (TFT's) on glass are predominantly used in the flat panel display industry for notebook computers, mobile phones, PDA's (Personal Digital Assistant), and other handheld devices. Today, flat panels made by amorphous TFT technology are replacing desktop computer CRT (Cathode Ray Tube) monitors at an ever-increasing rate. Amorphous TFT technology applications are limited due to its inherently low electron mobility. Applications that require integration of display drivers such as hand-held camcorder and cell phone displays are using poly-silicon based TFT's for cost and space savings. This eliminates the need for costly assembly of conventional silicon chips onto the amorphous TFT display panels. Advances in polysilicon technology have expanded TFT technology to high-speed electronics applications such as Smart Cards, RFID tags and other integrated circuit functions.

FlexICs has developed an ultra low-temperature polysilicon TFT technology on both glass and plastic substrates. The plastic substrates are thinner, lighter, shatterproof, flexible, rollable and foldable, making silicon-on-plastic an enabling technology for new applications/products. Some of the possibilities are roll-up/down displays, lightweight, thin wall-mounted TVs, electronic newspapers, and wearable display/computing devices. Moreover, plastic substrates offer the potential of roll-to-roll (R2R) manufacturing which can reduce manufacturing cost substantially compared to conventional plate-to-plate (P2P) methods. Other possibilities include smart cards, RFID tags, and portable imaging devices, photovoltaic devices and solid-state lighting.

The challenge of silicon-on-plastic technology is to overcome the fact that plastic melts at the temperature required to build transistors in conventional TFT processes. FlexICs has developed an ultra low-temperature process that is compatible with plastic substrates and offers good TFT performance. Technological innovations have been made to accommodate silicon processing at low temperatures. FlexICs has developed an integrated manufacturing process for active-matrix TFT backplanes.

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1) Low temperature (< 100° C) gate oxide deposition:

FlexICs has developed a proprietary deposition machine and a compatible process to deposit high quality TFT gate oxides at sub-100° C temperatures. It is a special PECVD (Plasma-Enhanced Chemical Vapor Deposition) system with an added plasma source configuration akin to ECR (Electron Cyclotron Resonance) to generate high-density plasma at low temperature.

The process is optimized to provide high-density plasma for silicon dioxide deposition using SiH_4 and O_2. The gate oxide film at 100 nm thickness has a breakdown voltage of more than 70V, while the gate leakage current density is less than 60 nA/cm2 at 20-V bias. As-deposited gate oxide shows good C-V characteristics as exhibited in Figure 1. A small amount of hysteresis is observed before annealing takes place. A pre-oxidation plasma treatment step using a mixture of H_2 and O_2 to grow a very thin oxide at the interface between the deposited silicon and the gate oxide with acceptable interface states was added to the process flow. Sufficiently high-density plasma must be generated in order to grow oxide with any significant thickness. The chuck is cooled to 20° C to keep the plastic temperature below 100° C during the entire pre-oxidation and deposition process. The cleanliness of the Si surface is critical prior to the oxidation process.

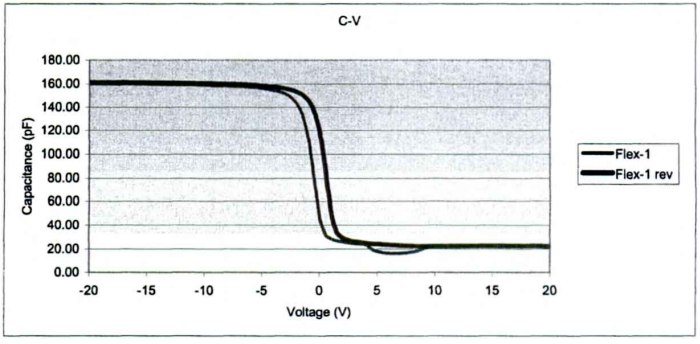


Fig. 1 C -V characteristics of FlexICs' as-deposited low-temperature gate oxide

The result shown in Figure 2 exhibits the difference between gate oxides with and without pre-oxidation. With pre-oxidation, we obtain an oxide C-V curve very close to the one calculated theoretically.

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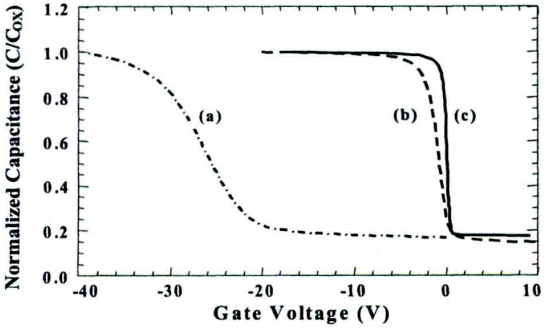


Fig. 2 C-V curves for gate oxide made (a) without pre-oxidation, (b) with pre-oxidation plasma treatment in comparison with (c) theoretical calculation.

2) Poly-silicon laser processing:

A Xe-Cl excimer laser is used to crystallize sputtered silicon on plastic, thereby forming large polysilicon grains for TFT's with much higher mobility than its amorphous counterpart. The extremely short laser pulses provide sufficient energy to melt the deposited Si, while the subsequent cooling forms a polycrystalline structure. This crystallization technique is similar to polysilicon formation on glass.

The challenge with plastic substrates is to melt the deposited silicon while preserving the structural quality of the underlying base material. Fig. 3 shows the temperature profiles in the plastic substrate covered with Si and SiO_2. The SiO_2 layer is sandwiched between the plastic substrate and Si to act as a heat sink preventing the plastic substrate from melting.

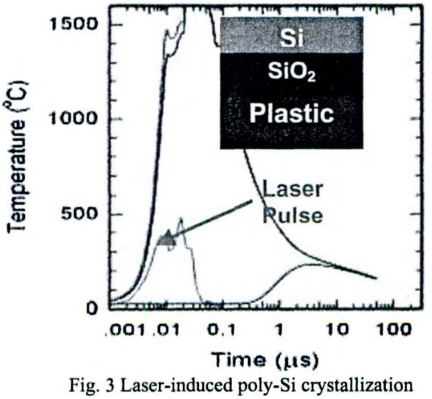


Fig. 3 Laser-induced poly-Si crystallization

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- Excimer Laser Annealing converts amorphous-Si to polysilicon film
  - 30ns Xe-Cl (308nm) pulse
  - Produces large grains for high performance TFT's
- SiO_2 layer traps heat in silicon layer
  - Plastic substrate is not damaged or deformed
  - Heat insulation allows full melt of silicon without damaging the plastic substrate

Fig. 4 reflects polysilicon grain size engineering. At first, the grain size increases with laser fluence due to the increase of melt depth. Once the full melt threshold (FMT) is reached, all Si seeds are melted, the film crystallizes by homogeneous nucleation of super-cooled molten Si, resulting in a uniform fine grain structure. The peak of the FMT is apparent in the figure. To maintain reasonable uniformity in grain sizes and operate the laser reproducibly, the laser fluence is selected to grow grains slightly above half-micron diameter.

The same laser system is used to perform dopant activation and annealing after source/drain ion implantation. Again, it provides nearly full S/D dopant activation without damaging the plastic underneath the Si layer.

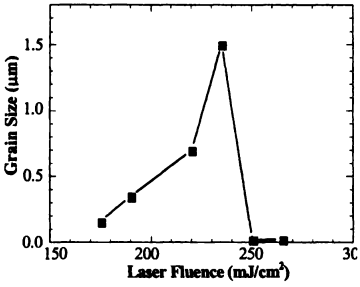


Fig. 4. Effect of laser fluence on the grain size in the Poly-Si film.

3) Plastic handling: Lamination and delamination processes

In order to use standard automated semiconductor manufacturing tools, FlexICs has developed a lamination/de-lamination process to handle the flexible substrates. The plastic sheets are cut into 6-inch wafer formats and laminated onto carrier wafers made of glass. This allows for processing the full TFT or active-matrix back plane using standard tools with plastic laminated glass wafers. The wafers are delaminated at the completion of the wafer processing. The schematic of process sequence is illustrated in Fig. 5.

Both sides of the plastic wafer are coated with a proprietary hard-coat material that increases resistance to scratches and chemicals. Additionally, the hard coat helps planarize the plastic surface, which is typically rougher than a standard display-grade glass. The plastic wafers are then processed through a heat-stabilization cycle, referenced to the plastic material's glass transition temperature (T_g). This cycle helps relieve internal stresses and reduces plastic deformation in subsequent processing steps.

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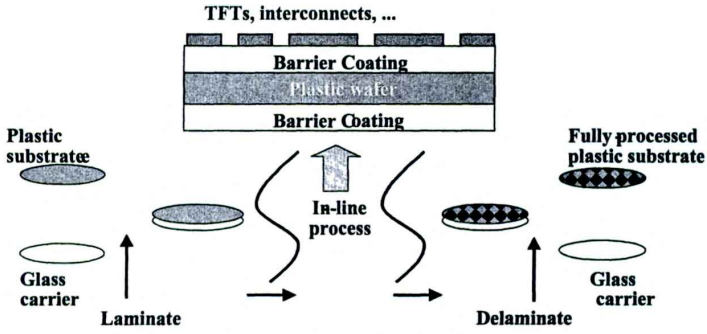


Fig. 5. Lamination, in-line processing and delamination of plastic wafers.

In addition, the lamination process has to satisfy several stringent requirements. The total flatness of the resulting sandwich needs to be tightly controlled to avoid issues in the photolithographic steps that follow. The laminate material thickness has to be optimized to minimize peak-to-valley variations. Fig. 6 shows that a thicker laminate layer brings larger peak-to-valley non-uniformity.

The lamination process cannot trap air bubbles between the laminated films. It also needs to withstand wet processing (solvents in particular) and to be "clean" and "dry" to meet deposition chamber requirements, such as minimum moisture and solvent out-gassing. The laminated wafer needs to be processed so that the plastic wafers can be delaminated safely and easily from the glass carrier wafers after the TFT manufacturing process is completed. This must be accomplished without inducing structural damage or adversely affecting the electrical properties of the TFT devices. FlexICs uses the same TFT process for its laminated plastic wafers as for its glass wafers. Fig. 7a shows the robot of an automated photoresist coater tool handling a laminated plastic wafer. This lamination technique enables the full use of automated processing tools. After completing the process and delamination, the plastic wafers retain their original flexibility, as shown in Fig. 7b.

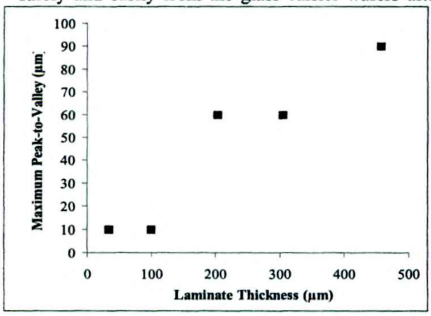


Fig. 6. Final thickness non-uniformity, measured by the maximum peak-to-valley variation.

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Another important consideration is the maximum temperature tolerated by the laminated wafer during the process. This depends on both the type of plastic and on the type of laminate chosen. At present, polyimide films are used for the plastic substrate, and the process temperature is limited by the stability of the laminate to about 110°C. The ultra low temperature poly-silicon TFT process used ensures adhesion of the laminate throughout the process and minimizes issues in subsequent lithography layer-to-layer registrations. Once the full process has been completed and the flexible substrate is detached, it can be post-annealed at a higher temperature, as allowed by the chosen plastic type. Table 1 summarizes important properties of different plastic substrates with high glass transition temperatures (T_g).

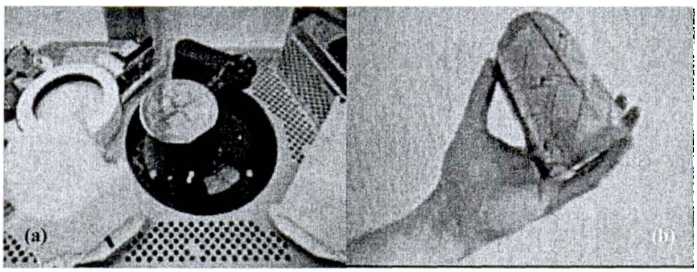


Fig. 7. (a). Photoresist coater robot handling a 6-inch laminated plastic wafer. (b) Flexible plastic wafer after process completion and delamination.

Table 1 Plastic Substrates with $T_g > 300$ °

Properties	Unit	Kapton	New PI	Arylite A1000HC	Appear 3000
Base		Polyimide	Polyimide	Polyarylate	Cyclic olefin
Thickness	μm	100	75	100	100
Physical					
Young's modulus	GPa	2.5	6.9	2.9	1.9
Tensile Strength	MPa	231	362	100	50
Water absorption	%	1.8	1.5	0.4	0.03
Thermal					
Decomposition Temperature at 5 wt% loss	°C	>500	>500	480	360
Tg	°C	>360	>360	325	330
CTE	ppm/°C	20	20	53	74
Optical					
% Transparent				90.4	91.6
Refractive Index		1.7		1.64	1.52
Color		Amber	Amber	Clear	Clear
Chemical Resistance		Excellent	Excellent	Poor	Poor

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Because of the critical requirement on alignment accuracy at lithographic steps, the most important process parameter is dimensional stability during the entire fabrication process. Fig. 8 shows the run-out measured as dimensional changes at different radial locations of the 6-inch wafers between two successive photolithography steps. Using a proprietary heat stabilization treatment prior to wafer processing, it is possible to reduce the run-out to meet the requirements of current design rules (~4 μm).

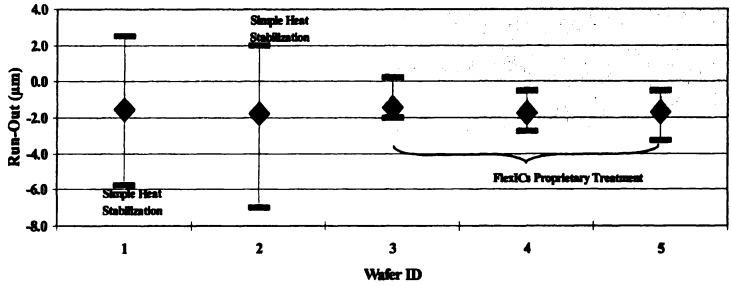


Fig. 8 Dimensional instability induced run-out and its reduction by heat stabilization treatments

4) Integration Issues and TFT performance:

In order to make an integrated circuit using TFT's, all process modules including the ones mentioned above must be fully integrated. The process sequence shown to the left of Fig. 9 represents a simple 4-mask TFT process. The cross-sectional view of a finished TFT device is shown on the right. It is a "top-gate" device structure with source/drain regions self-aligned to the aluminum (Al) gate.

- Barrier coating deposited on plastic
- Laminate plastic to glass carrier
- Deposit a-Si and crystallize
- Pattern device island (MASK 1)
- Deposit gate dielectric & metal
- Pattern gate stack (MASK 2)
- Dope source/drain. Laser activation.
- Contact ILD deposition
- Pattern contact holes (MASK 3)
- Deposit 1st level metal
- Pattern metal (MASK 4)
- Delamination/annealing

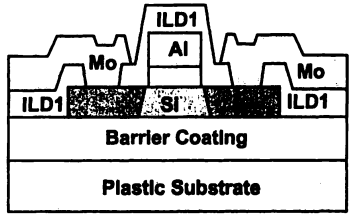


Fig. 9 Process sequence and the corresponding finished TFT device

A refractory metal, molybdenum (Mo), is used as first level of metal, but it is known to have a high level of film stress. However, it is also possible to use Al and/or an Al/Mo composite metallization scheme to reduce stress caused by Mo. This is a unique

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integration issue associated with plastic substrates due to their sensitivity to film stress. This causes too much dimensional instability and run-out problems. Fig. 10 shows improvement in run-out when using the Al/Mo composite metallization instead of a pure Mo film.

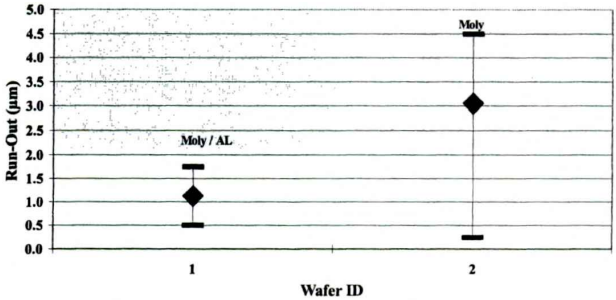


Fig. 10 Improvement in run-out with a Al/Mo composite metallization

In a display, a storage capacitor is included to mitigate a small amount of off current (or leakage current) from the TFT. One or two additional masks are needed to make the capacitor. Depending on the type of display materials (electro-optical materials) used, extra processes steps are needed. For example, if a bottom-emitting OLED is used, it is necessary to add a transparent conducting layer, normally ITO (Indium Tin Oxide), and a second contact level, often called Via. This requires two additional masks. However, these masks are not needed if a top-emitting OLED device is used. The subsequent deposition of the OLED film and another layer of a cathode material completes the display. Fig.11 (a) and (b) shows the cross-sectional views for both cases.

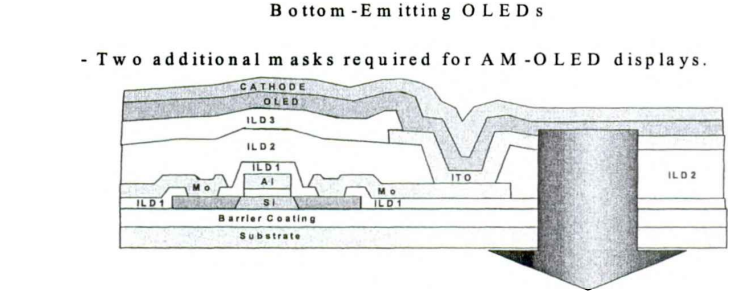
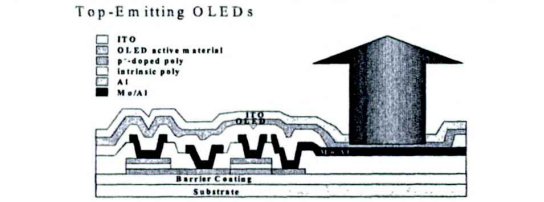


Fig. 11 (a)

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•The same back-plane process can also be used for different display types, such as LCD, Electrophoretic

Fig. 11 (b)

As described earlier, plastic substrate integrity is maintained during laser recrystallization since most laser energy is absorbed in the deposited amorphous film with a relative thick SiO_2 layer underneath. However, during source/drain implant activation when Si islands have already been formed, laser damage can occur in the area where the plastic substrate is no longer covered by a blanket silicon layer. To resolve this issue, FlexICs has embedded a Bragger reflector layer in between the plastic substrate and the Si layer. By using alternating oxide/nitride layers plastic damage is avoided.

Another important integration issue is plastic substrate control during gate oxide deposition. To avoid excessive run-out, cooling is needed for the plastic substrate, however excessive cooling leads to poor oxide quality due to lack of mean free path during SiO_2 nucleation. Fig 12 illustrates this issue and the solution obtained at FlexICs.

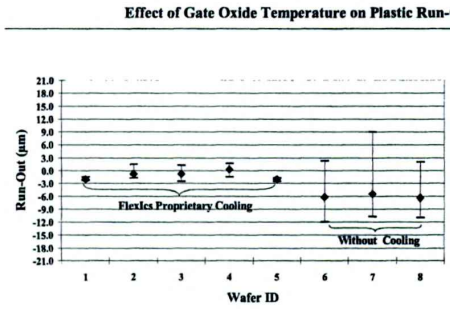


Fig 12: Gate Oxide Deposition and cooling

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A typical finished TFT device is shown in Fig. 13. After the plastic sheet is de-laminated, low off current is achieved using a 300°C hydrogen plasma anneal process.

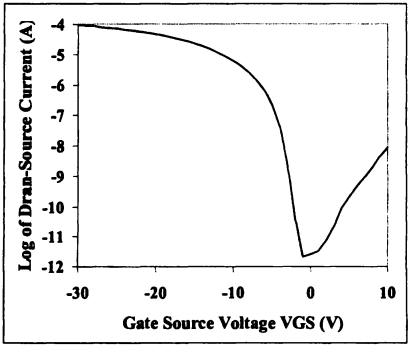


Fig. 13. Current-Voltage curve for a 4/20 *W/L* n-channel TFT fabricated on plastic

All relevant device parameters are summarized in Table 2. The electrical TFT device characteristics on glass substrates are similar to these TFT's made on plastic substrates.

Parameter	Median Value	Standard Deviation
Hole field-effect mobility (cm^2/Vs)	71	9
Threshold voltage (V)	-4.8	0.25
Sub-threshold slope (V/decade)	0.59	0.09
Drain-Source leakage current (pA)	2.7	1.2
Gate Leakage current (pA)	Below 0.1 pA (instrument sensitivity limited)	

Table 2: Device parameters of TFT's made on plastic substrate

The ultra low-temperature polysilicon TFT described above has been used to fabricate active matrix backplanes on glass and plastic substrates. The backplanes were then used to make display demos with OLED. Fig. 14 shows the display demo made on glass using bottom-emitting OLED material deposited by our partner. To reduce defects, attention is focused on cleanliness and handling of the TFT samples prior to the OLED deposition. Back-planes on plastic substrate are shipped to partners for OLED film deposition.

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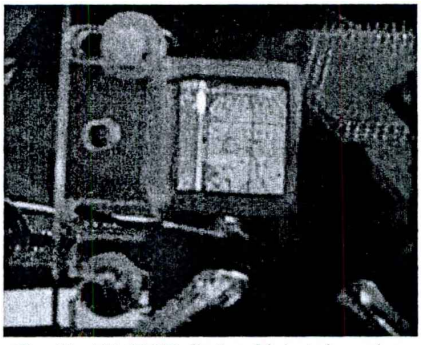


Fig. 14. AM-OLED display fabricated on glass using "plastic compatible" process. Jeff Spindler at Kodak is acknowledged.

All above-mentioned data are obtained from Polyimide plastic substrate which is amber color, not transparent. Consequently, bottom-emitting OLED can not be used. Recently, we have been working on Polyarylate plastic (see Table 1) which is a transparent (clear) plastic and can tolerate 300 ° C anneal which is needed to reduce off current. The material does not have good chemical resistance; however we have modified our TFT process and de-lamination method to accommodate it. We also use our own proprietary coating to protect and flatten the surface. Preliminary result is encouraging as shown on Fig. 15. At 310 ° C anneal, TFTs on the transparent plastic perform the same as their counter parts made on glass substrate. For the glass substrate, higher temperature anneal (328 ° C anneal) further reduces the off current. However, the clear plastic didn't survive the 328 ° C anneal. Work is in progress to optimize the TFT performance on the clear plastic substrate.

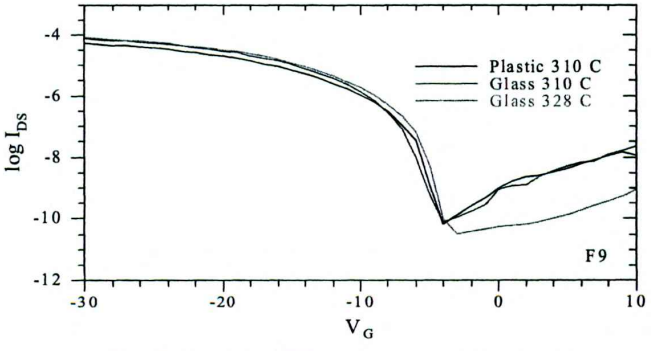


Fig. 15 I-V curves of TFTs made on clear plastic substrate as compared to TFTs made on glass.

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VHF PECVD MICRO-CRYSTALLINE SILICON BOTTOM GATE TFT WITH THIN INCUBATION LAYER

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ABSTRACT

Microcrystalline Si thin film transistor (μc-Si TFT) generally requires that the active layer should have not only high crystallization volume fraction but also thin incubation layer, especially for bottom gate TFT. It was found that decreasing the ratio of $SiH_4/[H_2+SiH_4]$ (Sc) is an effective way to decrease the incubation layer thickness of μc-Si directly deposited by VHF PECVD without any further thermal and laser treatment. Based on the μc-Si with thin incubation layer, the bottom gate thin film transistor (BG-TFT) with Al/SiNx/μc-Si/n^+-μc-Si/Al structure was fabricated.

INTRODUCTION

With the development of new panel display technology, such as AMOLED, thin film transistors with good performance and low cost are required. Recently, intrinsic μc-Si (microcrystalline silicon) without any further treatment by thermal or laser annealing is extremely appealing due to its higher mobility and better stability than amorphous silicon (a-Si) TFT and lower cost than polycrystalline (poly-Si) TFT[1-2]. Compared with the mature a-Si TFT technology, μc-Si TFT could be used in higher-resolution displays, or it would allow the use of smaller size TFT to increase optical aperture. Furthermore, the fabrication process of bottom-gate (BG) μc-Si TFTs is almost compatible with that of the a-Si TFTs, that is to say, the same product line which today produce a-Si TFT could easily be switched to BG μc-Si TFT production. However, for the μc-Si film, difficulty arises from the fact that a kind of incubation layer with amorphous structure clings on top of the substrate though the rest of the film may exhibit a high crystallinity [3-5]. The thin incubation layer may affect the TFT performance obviously, especially in BG μc-Si TFT. In this paper, the studies on incubation layer are presented and the performance of BG μc-Si TFT with a thin

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incubation layer is shown.

EXPERIMENTAL DETAILS

Series of μc-Si thin films were deposited by VHF-PECVD with the active frequency of 60M Hz, the silicon concentration diluted by hydrogen ($SC=SiH_4/(SiH_4+H_2)$) was varied from 0.67% to 8%, film thickness changed from 10nm to 1000nm, the pressure and the substrate temperature was fixed at 120Pa and 220 ℃, respectively. The same excited power, 25W, was applied for all samples. The crystallinity of μc-Si is measured by Raman spectra using 632.8nm He-Ne laser. Here, the crystalline volume fraction (*Xc*) was used to describe the crystalline degree of the films. As well known, the *Xc* of the sample can be deduced from its Raman scattering spectra by the ratio of $Xc=Ic/(Ic+Ia)=(I_{520}+I_{510})/(I_{520}+I_{510}+I_{480})$. Where Ic is the crystalline intensity peak at 520 and 510, but Ia is the amorphous intensity at 480cm^{-1}. Conduction activation energy (*Ea*) was measured utilizing the equipment designed by our-self.

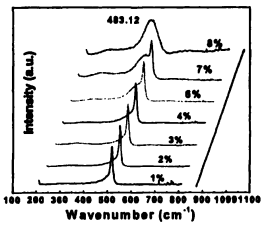


Fig.1 Raman spectra of the 1000nm

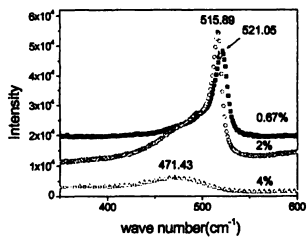


Fig.2 Raman spectra of the 160nm μc-Si film with variable SC

For the BG μc-Si TFT fabrication, a four-mask process with specially designed layout was used. First, we thermally evaporated Al, and patterned it using reactive ion etching to form the gate electrode, then, deposited 200 nm SiN_x as gate insulator. Next, 160 nm of intrinsic μc-Si as the channel layer and 50-100 nm of n^+ μc-Si as the contact layer were grown on the SiN_x substrate orderly without breaking vacuum. Afterwards the channel was defined by photolithography and wet etching. Then, Al was thermally evaporated and patterned by wet etching to form the source and drain electrodes. The active channel was configurated by conventional back-channel etching. Finally, we opened the contact holes to TFT gate electrode.

RESULTS AND DISCUSSIONS

Incubation layer

To achieve a good μc-Si TFT, crystallinity of the μc-Si film is an essential factor.

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Fig.1 shows the Raman spectra of the 1000nm thick μc-Si film with increasing hydrogen dilution under other identical deposition conditions. It can be observed that the Raman spectra peak changes from amorphous band at 480 cm^{-1} to the crystal band at 520 cm^{-1} gradually above a certain threshold dilution ratio around the Sc of 6%. However, it is different in the case of a thinner (<0.2 μm) μc-Si used as the TFT channel as shown in Fig.2.

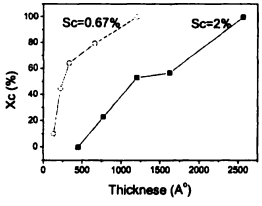


Fig.4 Variation of Xc with the thickness of μc-Si thin film at different silicon concentration

As Fig.2 shows for the thinner μc-Si film, the phase transition point is around Sc of 4%. This could be attributed to the effect of the initial amorphous layer that is called incubation layer, existing between the substrate and the crystalline layer. Apparently, the thinner the μc-Si film, the more obvious effect of the incubation-layer, which will make the μc-Si TFT, especially the bottom gate TFT, shows characteristics of a-Si TFT instead of the advantages of μc-Si TFT. According to our experiments results, we have found that decreasing SC is an effective way to thin the incubation-layer. When SC=4%, the thickness of the incubation-layer is above 200 nm which is thicker than the channel thickness of μc-Si TFT, while, it is down to 60~70 nm for SC=2% and becomes more thinner (about 20 nm) for SC=0.67% as shown in Fig.3 (a) and (b), respectively. From Fig.4, it is important to note that for μc-Si film deposited at SC=0.67%, the Xc of its 20nm incubation-layer is nearly 50%, which can be seen in Fig. 5. Increasing the film thickness, Xc tends to rise slower.

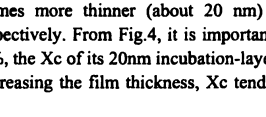


Fig.5 Analysis of Raman for 220Å at SC=0.67%

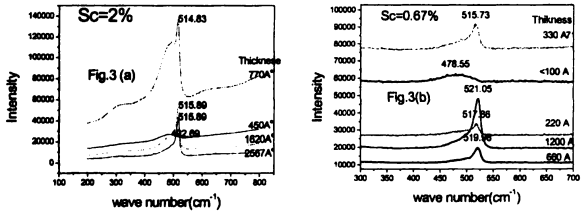


Fig.3 Raman spectra for μc-Si film deposited at SC=2% (a), 0.67% (b) with variable film thickness

While, Xc of the μc-Si film deposited at SC=2% with 60nm incubation-layer is

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nearly 20% and shows the same tend.

Thus far, we have effectively thinned the initial amorphous incubation layer in μc-Si film by using high H dilution of SiH_4 simply. However, the drawback of too high H dilution is that it results in a lower deposition rate and lower activation energy (E_a). The deposition rate of μc-Si film deposited at SC=0.67%, 25W, and 120Pa is only 0.68Å/s and the E_a is about 0.1ev. The drastic decreasing of E_a may be caused by the oxygen contamination. For the growth of μc-Si, atomic hydrogen reaching the film-growing surface breaks weak Si - Si bonds in the amorphous network structure, leading to a removal of Si atoms weakly bonded to another Si. This site is replaced with a new film precursor SiH3, creating rigid and strong Si - Si bond, giving rise to an ordered structure[5]. Under too high H dilution condition, the role of the atomic hydrogen etching is too great, which leads to much void in μc-Si film between the columnar grains, then, oxygen penetration into it[6]. Strong oxygen contamination makes the threshold voltage of TFT negative and gives rise to large leakage current as well as the deterioration of gate modulation effect. In addition, R.E.I. Schropp has found that oxygen incorporation increases linearly with decreasing deposition rate[7]. Therefore, from the view of oxygen contamination point, the Sc should not be too low.

Considering the incubation layer thickness and the oxygen contamination, we try to choose the SC for the μc-Si film used as the TFT channel as 2%. In this case, its E_a is 0.45eV and the thickness of incubation layer is about 60nm (Xc of the incubation layer is about 30%), which may be relatively suitable for the BG μc-Si TFT. The optimum structure has to be studied more later.

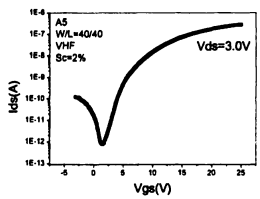


Fig. 6 Transfer Characteristics of μc-Si TFT

BG μc-Si TFT

Bottom gate TFTs were fabricated with the μc-Si deposited at SC of 2%. The almost same fabrication processes as those for making a-Si TFT were employed to fabricate μc-Si TFT. The transfer characteristic curve of the resulted TFT without any other treatment and LDD structure is shown in Fig.6. The ratio of on state current to the off state current (I_{on}/I_{off}) is up to 10^6, the mobility is around 0.7cm^2/V-sec, and the threshold voltage is about 5V. The TFT characteristics are comparable to that of the μc-Si TFT reported by other research groups. Further optimization, such as the μc-Si grain size, the film density and interface treatment, is still required to make the BG μc-Si TFT show more obvious advantages to a-Si TFT.

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CONCLUSIONS

Decreasing the silicon concentration is an effective way to achieve a μc-Si film with ultra-thin (<20 nm) incubation-layer or much less by VHF-PECVD. However, too high H dilution leads to too low deposition rate and serious oxygen contamination. From the view of the above two points, μc-Si film deposited at SC of 2% is suitable for the application of the bottom gate TFT and this TFT without any other treatment and LDD structure shows relatively good performances. Nevertheless, further optimization of μc-Si film is still required to achieve a better bottom gate μc-Si TFT. This work is under our study.

ACKNOWLEDGMENT

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SEMICONDUCTING PROPERTIES OF PENTACENE THIN FILMS STUDIED BY COMPLEX IMPEDANCE, SURFACE MOBILTY AND PHOTO-INDUCED EFFECTS

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ABSTRACT

This paper discusses semiconducting properties of pentacene thin films focusing on complex impedance analysis, accurate carrier mobility determination, and carrier generation/annihilation processes, all of which are fundamental characteristics for any semiconductors. Although pentacene is considered to be a promising material for organic field effect transistors (FETs), there have not been many reports on basic properties as a semiconductor. For actual application and device modeling, quantitative analysis on the basis of experiments will be necessarily required. A carrier response in the semiconductor after majority carrier injection or generation in the film is a target to discuss, since it should affect a single device performance as well as circuit performance.

1. INTRODUCTION

Pentacene has attracted much attention from its high mobility viewpoint as an active material for organic field-effect transistors[1),2)]. Also, possible applications achieved by using pentacene transistors have been already proposed[3)]. One knows that there have been tremendous amount of efforts on continuous development of the current inorganic semiconductor devices from the viewpoints of science as well as technology. On the other hand, organic materials have been studied mainly by chemistry viewpoints, and not so many electronics engineers have been involved in this community. In fact, semiconducting properties of pentacene have not been fully understood yet, but in order to obtain high performance and highly reliable organic FETs, detailed understanding of material properties and electronic states of thin pentacene films should be strongly required. This paper reports basic material properties of pentacene films in terms of C-V characteristics, dielectric properties, interface carrier mobility and photo-induced effects. It is pointed out that the capacitive component inherent to the pentacene film has a significant role for device characterization. Furthermore, the carrier annihilation process with a very long time constant is experimentally demonstrated.

2. EXPERIMENTAL PROCEDURE

2.1 Sample Fabrication

Four types of pentacene device structures were fabricated for studying complex impedance, FET mobility and majority carrier response in the films. MOS and MIM capacitors (a), (b) and (c), and FET structure device (d) employed in this work are schematically shown in **Fig. 1**. The pentacene film was grown by the thermal evaporation at room temperature at 0.05 nm/sec deposition rate in a vacuum camber with a base pressure of 10^{-5} Pa. Au for the electrical contacts to pentacene and Al

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for the back contact to silicon substrate were also thermally evaporated in a different vacuum chamber. Pentacene thickness was varied from 260 to 400 nm.

2.2 Measurement Methods

A top view of the bottom source/drain pentacene FET measured by SEM is shown in **Fig. 2**. The grain size is typically 0.2 μm on Au electrode, while that on SiO_2 is

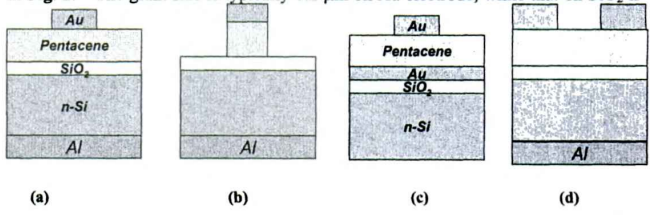


Fig.1. Schematic cross section of devices used in this work. (a) and (b) are MOS capacitor type devices, where n-Si, SiO_2 and pentacene are gate electrode, gate insulator and semiconductor, respectively. (c) is a MIM capacitor, where I is pentacene dielectric film, and (d) is a top source/drain pentacene TFT used commonly as a test vehicle.

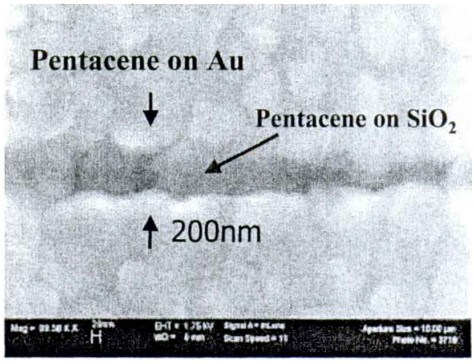


Fig. 2. Top view of pentacene film measured by SEM. The pentacene film in this case is deposited both on SiO_2 and Au for bottom source/drain FET with a small channel length.

limited by the channel window between source and drain Au electrodes in this case.The XRD pattern of the evaporated films only show the thin film phase. Electrical characteristics were measured at 25 °C in the air on the electrical probing station MOS capacitors and in the vacuum for FETs.. The impedance measurement

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and mobility analysis were performed by using the precision LCR meter and the semiconductor parameter analyzer. The spectroscopic ellipsometry was used for obtaining the photo-absorption spectrum of the film. A fluorescent light of microscope equipped on the electrical characterization probe station was used for investigating the photo-induced effects on the electrical conductance.

3. EXPERIMENTAL RESULTS

3.1 Capacitance-Voltage Characteristics

The MOS capacitor type devices with structures of (a) and (b) in Fig.1, where 30 nm-thick thermally grown SiO_2 and n-Si were used for gate insulator and gate electrode, respectively, were used for measuring capacitance-voltage characteristics. Note that "S" of "MOS" denotes the semiconducting pentacene film. **Fig. 3 (a)** and **(b)** show a comparison of C-V characteristics between devices (a) and (b) [4]. It is reported that pentacene is a p-type semiconductor, so overall characteristics are roughly reasonable. However, note that the frequency dependence of capacitance is quite different from each other. In particular, the low frequency capacitance is quite large in the case of type (a) device. At 50 Hz, approximately one order of difference in a unit-area capacitance between them is observed. A device structure difference between them is just a pentacene area under Au electrodes. In terms of MOS C-V characteristics, the type (b) behavior seems quite normal. This significant difference of C-V characteristics is understandable by considering the fact that pentacene is a dielectric film and its effective capacitor area depends on the frequency, as schematically shown in **Fig. 4**.

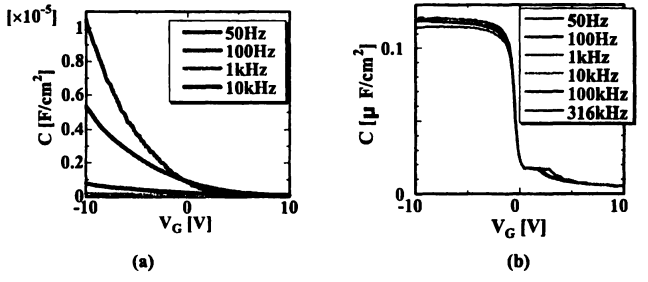
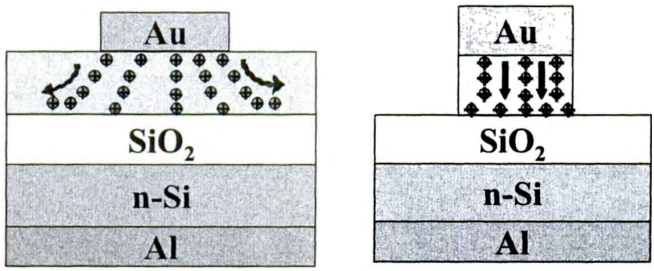


Fig.3. Capacitance-gate voltage characteristics **(a)** for type (a) and **(b)** for type (b) devices. A distinct difference between (a) and (b) is observed, though the pentacene area and alignment with regard to gate electrode is different.

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(a) (b)

Fig. 4. Schematic description for explaining the difference of C-V characteristics observed in Fig. 3. At a low frequency region, majority carriers can spread out over a wide area of accumulation channel. The pattern alignment accuracy is quite important for quantitative C-V characterization.

At a lower frequency region, injected carriers are easily spread out over a wider area at SiO_2/pentacene interface. This fact should be generally taken into consideration for the semiconducting organic film capacitor characterization. On the other hand, Fig. 3(b) shows that the interface quality at the pentacene/SiO_2 seems quite good from the shape of C-V curve, though the interface states density, Dit, has not been determined. Thus, to investigate C-V characteristics quantitatively, an accurate pattern alignment is needed as shown in the device (b) in Fig. 1. From those results, it is likely that the pentacene film behaves as a simple inorganic semiconductor. However, as shown in the case of Fig. 3(a), it should be considered that pentacene itself is a dielectric film with high resistivity. This behavior is due to intrinsic properties of majority carrier response in the film, though it can be seen in inorganic semiconductors at much higher frequency region.

3.2 Complex Impedance Measurement and Dielectric Properties

It is important to investigate the pentacene film as a passive layer as well as an active layer for actual applications. The frequency dependent C-V characteristics at a high frequency region observed in Fig.2 (b) include the dielectric properties of pentacene films rather than the structure dependent capacitance. To analyze dielectric properties of the film more quantitatively, the device with type (c) structure as *metal/pentacene/metal* (MPM) was utilized for studying the complex impedance characteristics, where pentacene dielectric properties can be simply characterized by applying a small ac amplitude signal[5]. Actual experiments were performed with 100 mV ac signal in the frequency range from 20 Hz to 1 MHz. **Fig. 5** shows the measured impedance plots in the complex plane for MPM devices with two kinds of electrode areas. Two semicircular arcs which can be described by a simple RC parallel circuit shown in Fig. 5 are observed. Indeed we assumed the three-elements model, but found that the two-elements model was accurate enough for the analysis from the fact that the extrapolation of the two arcs passed the origin. This result means that the contact resistance at Au/pentacene is negligibly small in these samples.

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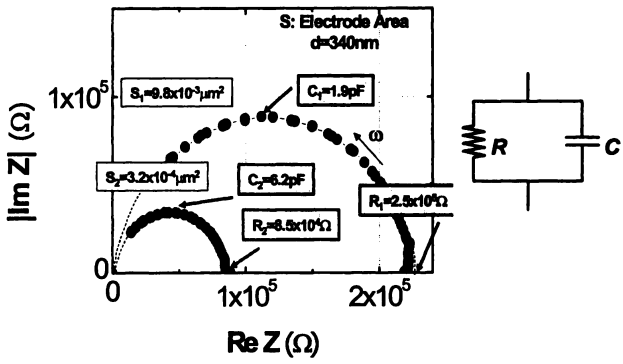


Fig. 5. Impedance plots in the complex plane for the device (c) in Fig.1. Two kinds of electrode area cases are shown. Two semicircular arcs are clearly observed. From the fitting to parallel RC model, both R and C can be evaluated.

Note that $\sigma_{\perp}$ determined by R_P normalized by the electrode area and the film thickness, and the unit area capacitance are almost the same for two devices. This fact clearly assures the validity of the present analysis that a complex RC network in the film is basically expressed by a simple RC parallel circuit.

The pentacene thickness dependence of the unit area capacitance is shown in **Fig. 6**. Since the pentacene thickness has a little bit ambiguity in the determination of the film thickness due to the surface roughness, the dielectric constant ε_{pen} of the pentacene was evaluated from the slope of the linear relationship in Fig. 6, with the result that ε_{pen} is about 6. The microscopic origin of the capacitance in the film is not clear now, and the grain size or crystal phase dependence of ε_{pen} would be interesting to study for future.

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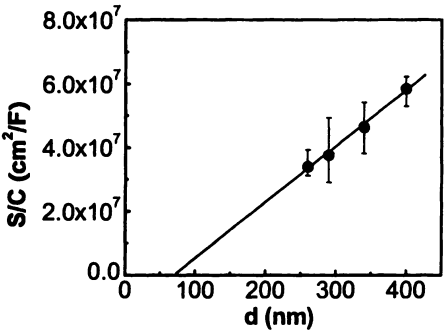


Fig. 6. Relationship between S/C (the inverse of unit area capacitance) and d (film thickness). From the slope of this line, the pentacene dielectric constant, ε_{pen}, can be evaluated to be about 6.

3.3 Channel Mobility Extraction by a Coupled Method of C-V with I-V Measurements

The channel mobility is usually determined by the analytical formula of saturated FET characteristics as follows.

$$I_{DS} = \frac{WC_{OX}}{2L}\mu_{FE}(V_{GS} - V_{TH})^2 \qquad (1)$$

, where L, W, C_{OX}, V_{TH} are the channel length, channel width, oxide capacitance per unit area, and threshold voltage of FET, respectively. However, it is not sure whether $C_{OX}(V_{GS}-V_{TH})$ simply describes the carrier density in the drain current expression based on the gradual channel approximation. In particular, the mobility is hard to determine accurately near V_{TH}. For the mobility analysis of inorganic MISFETs such as Si-MOSFETs, the carrier mobility is evaluated by experimentally separating drain current from carrier number, since the conductive mobility is basically defined by a ratio of the drain current to the carrier number in the linear region as below.

$$\begin{aligned} I_{DS} &= W\mu_{FE}\cdot n_{ch}e\cdot E \\ &= W\mu_{FE}\frac{Q_{ch}}{LW}\frac{V_{DS}}{L} \\ &= \frac{1}{L^2}\mu_{FE}\cdot Q_{ch}\cdot V_{DS} \end{aligned} \qquad (2)$$

Here, Q_{ch} is the total charges in the channel. This mobility determination method is called as the split C-V technique in the Si-MOSFET mobility analysis. We also employed this method to evaluate the carrier mobility of pentacene FET, though it is not the split C-V method in a rigid sense (not discussed here). **Fig. 7** shows a basic idea

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to directly measure the channel carrier number injected from source and drain by using the conventional LCR meter. As mentioned in the 2.2, it should be paid attention to the fact that the effective channel area depends on the measurement frequency in the impedance measurement. Furthermore, the measurement frequency should be low enough for majority carriers to form the stable accumulation layer. Thus, the low frequency measurement is absolutely required for accuracy.

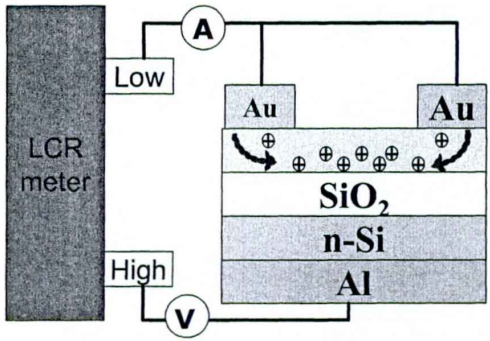


Fig. 7. Schematic description for the direct measurement system of channel carriers. Actual injected carriers are counted by LCR meter. Low frequency measurement is a key to achieve an accurate analysis.

In addition, it is important that the capacitance contribution from *metal/pentacene/SiO_2/Si/metal structure* just below source and drain electrodes should be subtracted from the experimentally obtained capacitance to estimate the channel carrier number. By measuring the capacitances of two devices with different channel length, and same electrode areas, only the channel area capacitance contribution was evaluated as follows.

$$C_{total} = C_{Source} + C_{Drain} + C_{Channel}(L). \qquad (3)$$

Then, the channel charges per unit area, $q_{Channel}$, can be calculated by integrating the channel area C-V characteristics.

$$q_{Channel} = \frac{Q_{total}(L_1) - Q_{total}(L_2)}{(L_1 - L_2)W}. \qquad (4)$$

Q_{ch} in Eq. (2) is the total carrier number in the channel area. Thus, for a devices with a given L and W, Q_{ch} is described as follows.

$$Q_{ch} = \frac{Q_{total}(L_1) - Q_{total}(L_2)}{(L_1 - L_2) \cdot W} \cdot LW. \qquad (5)$$

As a result, the carrier mobility can be determined according to the definition of Eq. (2). This technique enables to produce a wide range of carrier density dependence of the mobility. **Fig. 8** shows the gate voltage dependence of the mobility obtained by

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the present analysis. The result clearly shows that the mobility increases with the carrier number increase[2]. For comparison, the mobility determined by the conventional method is also shown in Fig. 8. Note that the mobility value obtained by the present method is smaller than that in the conventional one due to the underestimation of the carrier number in the conventional method.

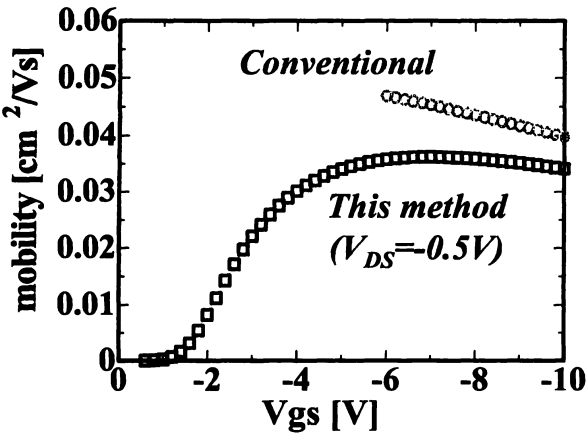


Fig. 8. Channel mobility obtained by both the present and conventional characterization methods. The present analysis provides mobility values in a wide range of gate voltage (carrier density). Note that a smaller mobility value comparing with the conventional method in the linear region is obtained.

3.4 Mobility Behavior in a Low Carrier Density Region

Fig. 9 shows a relationship between mobility and carrier density as a function of gate voltage near V_{TH}. Note that the mobility is quite low at low V_{GS} (low carrier density region). It means that near V_{TH}, even though carriers are injected into the film, they do not contribute to the actual DC channel current. It is inferred that the injected carriers are not mobile but localized at the interface due to a relatively large potential fluctuation. This effect can be reduced by applying the higher drain voltage thanks to the effective barrier lowering in the channel direction. In addition, it is worth while mentioning that the conductance properties at low carrier density region are quite interesting in terms of localized state transport, which seems to be generally observed in organic devices.

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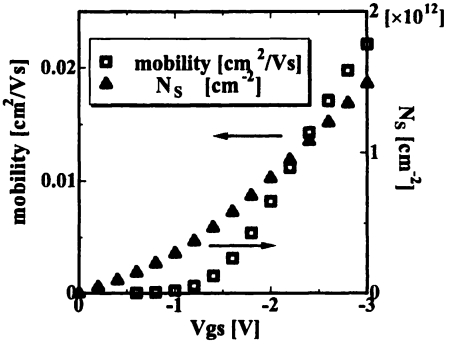


Fig. 9. Both mobility and carrier density are plotted as a function of gate voltage. Note that near V_{TH} region, though carrier number is finite, mobility is almost zero in the linear region (V_{DS}= -0.5 V).

3.5 Photo-induced Effects

In inorganic semiconductors, the carrier excitation experiment by irradiating the light with an energy over the band gap is commonly performed for studying the carrier response properties. To do the same experiment in the pentacene film, it is necessary to estimate the band gap energy beforehand. The photon absorption (wavelength dependence of extinction coefficient k) was measured by using the spectroscopic ellipsometry. As reported[6], a strong absorption peak is observed at $h\nu$=1.8 eV with a couple of shoulder peaks at higher energies, as shown in **Fig. 10.**

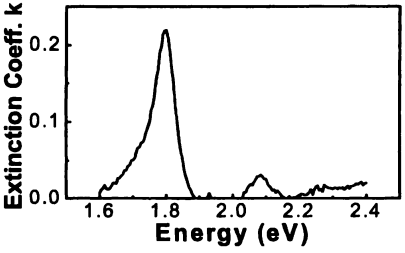


Fig. 10. Optical absorption spectrum of pentacene film measured by the spectroscopic ellipsometry. There is a peak absorption at $h\nu$=1.8 eV and several shoulders at higher energies. It is considered that the peak absorption energy corresponds to the main energy gap of pentacene as a semiconductor.

We consider that this main peak corresponds to the pentacene "energy gap", though the joint density of states is very narrow. This fact implies that the visible light energy seems high enough to excite excess carriers in the pentacene films over

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the intrinsic gap. Thus, a fluorescent light was irradiated to *metal/pentacene/metal* device (type (C) structure) with the semi-transparent electrode (thin Au) so as to investigate the photo conductivity. **Fig. 11** shows that the resistivity increases with the time after the light was off and becomes flat after 1000 sec [5]. This fact indicates that the light induces more free excess carriers in the film, and that by switching off the light, the resistivity increases with the time. So, the time dependence of the resistance change after the light off implies that a very slow relaxation process of excited carriers in the film is involved just after the transient resistivity increase. We have not understood what type of relaxation mechanism is microscopically involved in the pentacene film, but it is quite interesting to replot the resistivity as a function of *log(t)* as shown in **Fig. 12.** Two types of relaxation processes of majority carriers seem to exist in the film.

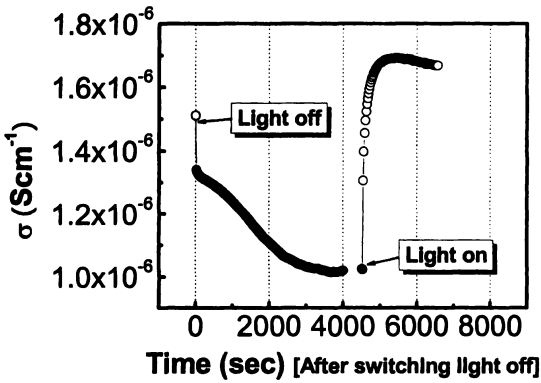


Fig. 11. Time dependence of conductivity change after the light off and on. The decay time constant is very long (typically thousand seconds), which implies that there is a rare recombination event in the film.

4. DISCUSSION

In all of the experiments performed in this work, it is a key to understand the carrier response behavior in the film. There is a clear difference of the time constants between the impedance analysis and the photo-excited carrier decay process. In the impedance analysis, the time constant is effectively expressed by the *RC* network formed inside the pentacene film, where C might originate in the intrinsic capacitance of the pentacene molecule. On the other hand, in the case of the photo-excitation experiment, it looks like the persistent photo current with a long time constant. If the mobility of excited minority carriers is very low or localized, and a very rare recombination process is assumed, the majority carrier number is high enough to maintain the high conductance with a long time constant. In fact, the mi-

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nority carrier, electron in this case, is considered to be trapped at defects instantaneously, and it is inferred that the decay time constant of conductance is controlled by a very small recombination rate in the film, as shown schematically shown in **Fig. 13.** These processes limit the dynamic performance of pentacene FETs and circuits, and it will become more important for actual application to understand physics of the carrier response behavior.

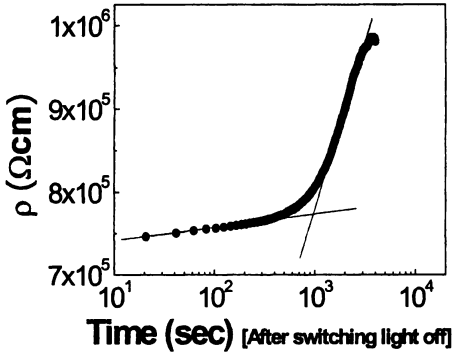


Fig. 12. Time dependence of resistivity increase after the light is switched off. Two kinds of recombination processes seem to be involved with the resistivity change.

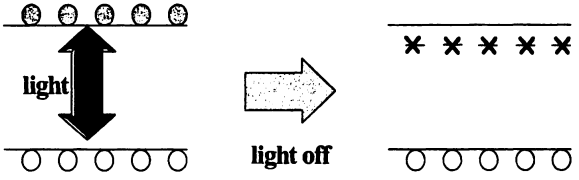


Fig. 13. Schematic view for both majority and minority carrier responses after the light is switched off. It is inferred that generated minority carriers are localized at defect sites just after the light is off, and the recombination rate is significantly reduced, but further study is obviously needed for microscopic understanding of the results.

5. CONCLUSION

The complex impedance as a function of measurement frequency, the FET mo-

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bility determination by using the combined technique of C-V with I-V measurements, and the relaxation process of photo-induced carriers have been investigated for pentacene thin films. All of the results clearly show that the pentacene is well described as a highly resistive inorganic semiconductor with a rather long life time of generated carriers. The dynamic properties of majority carriers in pentacene films should affect TFT circuit performance as well as a single device performance. Furthermore, the carrier dependence of the mobility in the vicinity of V_{TH} has been shown for the first time. Those properties described in this work will play important roles for improving and modeling the organic device performance.

ACKNOWLEDGEMENT

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BOTTOM CONTACT ORGANIC THIN-FILM TRANSISTORS WITH THIOL-BASED SAM TREATMENT

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ABSTRACT

We report on a thiol-based self-assembled monolayer treatment of the source/drain electrodes to improve the characteristics of an organic thin-film transistor with a bottom-contact configuration. With the treatment of immersing the substrate in octadecanethiol solution for 1 minute, the field effect mobility increases by 25% and the off current decreases about one order of magnitude compared to that without the treatment. It has been confirmed that thiol molecules absorbs in lying-down phase on the source/drain electrodes. A self-assembled monolayer in lying-down phase between the electrodes and a semiconductor plays an important role to reduce resistance at the interface without increase of the Schottky and tunneling barrier height.

Organic thin-film transistors (TFTs) have received interest due to their simple and low cost process. Among TFT structures, the bottom contact configuration, with organic semiconductor deposited onto the prefabricated source/drain electrodes, is suitable for printing process, but it usually has the field-effect mobility lower than that of the top contact configuration. This is caused by high contact resistance, R_c, between the source/drain electrodes and a semiconductor, becoming a substantial part of the total TFT resistance [1]. A self-assembled monolayer (SAM) on the electrode surface is reported to reduce R_c [2], but details of the treatment condition and mechanism for reducing R_c are still unclear.

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In this paper, SAM treatment condition should be optimized to reduce R_c directly extracted from the transfer characteristics of the bottom contact TFTs with different channel lengths. Causes for reducing R_c will be discussed in terms of the grain growth of a semiconductor film at the electrode edge and energy barrier height for the carrier injection.

A schematic cross section of a TFT sample is shown in Fig. 1 Heavily doped silicon was used as the substrate and the gate electrode together with thermally grown 300-nm-thick silicon dioxide as the gate-dielectric layer. 50-nm/1-nm thick Au/Cr was deposited by evaporation and patterned using photolithography with a lift-off method to make the source/drain electrodes. The kinetics and adhesion mechanism of octadecanethiol (ODT) on Au are well characterized [3], and it was used as a dip-coating to form a SAM on the electrode surface. The samples were dipped in a 0.1-mM octane solution for periods ranging from 1 minute to 4 days. After the SAM was formed, the Au surface was rinsed with octane and chloroform. Finally, a 50-nm thick pentacene film was deposited by thermal evaporation at a rate of 0.1 nm/s in an atmosphere of 2×10^{-6} Torr without heating the substrate.

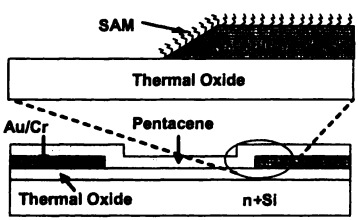


Fig. 1 Schematic cross section of organic TFT.

To estimate the value of the contact resistance, R_c, TFTs with various channel lengths from 5 to 400μm and a constant channel width of 2000 μm were prepared. The values of the R_c were obtained from the intercept on the y-axis of the relationship between the total resistance and channel length [1], [4]. Surface morphologies of pentacene were observed by using atomic force microscopy (AFM). The ionization energy of the pentacene and the change in the work function of the Au surface was measured using an ultra-violet photoemission counter operated in atmosphere (AC-2: Riken Keiki).

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The transfer characteristics of TFTs with ODT treatment time are shown in Fig. 2. With ODT treatment for 1 minute, the field-effect mobility increases by 25%, and the off current decreases by about one order of magnitude compared to that without the

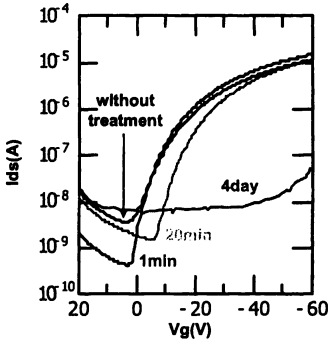


Fig. 2 Transfer characteristics. The channel length L is 2000 mm and the channel width W is 400 mm (Vds=-20V). The field effect mobility of TFT with ODT treatment for 1 min is 0.24cm²/Vs.

treatment. However, excessive treatment results in a decrease in mobility, accompanied by a shift in the threshold voltage. With the 4-day treatment, the current decreases to less than 10^{-8} A and the switching behavior completely disappears.

The changes in TFT characteristics with the treatment correspond to changes in the R_c. The value of the R_c is shown in Fig. 3 as a function of the time that the substrates are immersed in the ODT. With the 1-minute treatment, the R_c decreases to almost half the value of that without the treatment. However, with a longer treatment time, the R_c increases steeply. Finally, the R_c increases threefold compared to without the treatment.

From the observation of surface morphologies of pentacene film shown in Fig. 4, it is confirmed that grain boundaries that have dense trap states are not reduced by the treatment at the immediate neighborhood of source/drain electrodes as reported [2]. This result indicates that there is another factor that improves the efficiency of the charge carrier injection.

The work function and on the Au surface and Schottky barrier height ϕ_B as a function of the treatment time are shown in Fig. 5. The work function of the Au surface without treatment is 4.8 eV, which is almost the same as the ionization energy of the pentacene. This means that the contact between the semiconductor and electrode is

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almost ohmic and the Schottky barrier height, ϕ_B, which is the difference in energy between the work function of metal and the ionization energy of a semiconductor, is nearly equal to zero. With a longer treatment time, ϕ_B increases about 0.4 eV with a reduction in the work function of the Au surface. Excessive treatment adversely affects

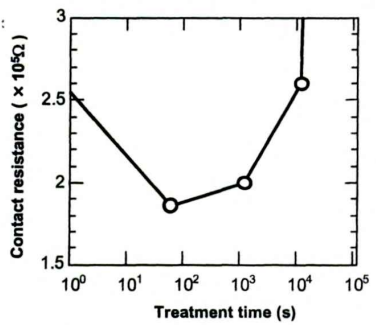


Fig. 3 SAM treatment time dependence of the contact resistance

the transfer characteristics of the organic TFT with an increase in the ϕ_B, which is a factor in the energy barrier at the interface.

The contact angles of pure water and a model for the adsorption of ODT

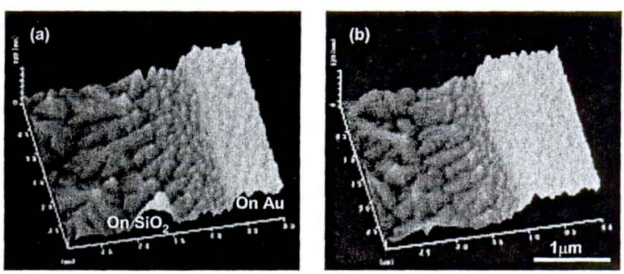


Fig. 4 3.0× 3.0 μm² AFM images of pentacene films on SiO_2 and Au electrode: (a) without treatment, (b) with treatment for 1 min.

molecules on the surface of the Au electrodes are shown in Fig. 6. The contact angle changes from 88 to 96 degrees. This result indicates that with a short treatment time, the ODT molecules adsorb sparsely on the Au surface in a lying-down phase on the electrode surface. As the treatment time increases, the ODT molecules gradually stand up the

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electrode surface. This means that the thickness of the intervening layer of ODT

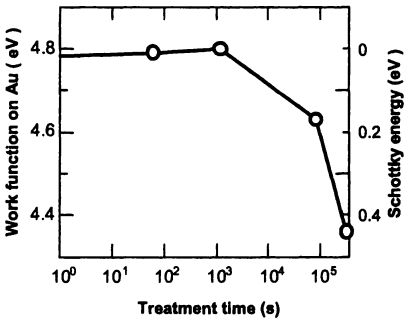


Fig. 5 Change of work function on Au and Schottky energy at the interface

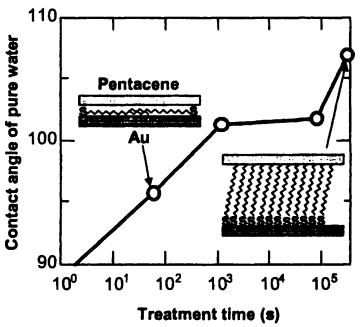


Fig. 6 Contact angles of pure water and a model for the adsorption of ODT molecules on the surface of the Au electrodes

molecules between the source/drain electrodes and the semiconductor increases. Finally, the ODT molecules orient to the electrode surface at 60 degrees and the thickness of the ODT monolayer becomes 2.3 nm [3].

When taking into account the results so far, R_c decreases with the condition of ODT molecule lying-down phase. The energy potential at the interface to account for the model of charge carriers injection is shown Fig. 7. When a semiconductor is directly formed on the electrodes, the states in the semiconductor where charge carriers are injected from the electrode are placed too close to the electrode and image potential is too

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large. In this case, charge carriers easily recombine and do not efficiently inject into semiconductor. On the other hand, when the SAM exists at the interface, charge carriers are captured in the states at a distance from the electrode

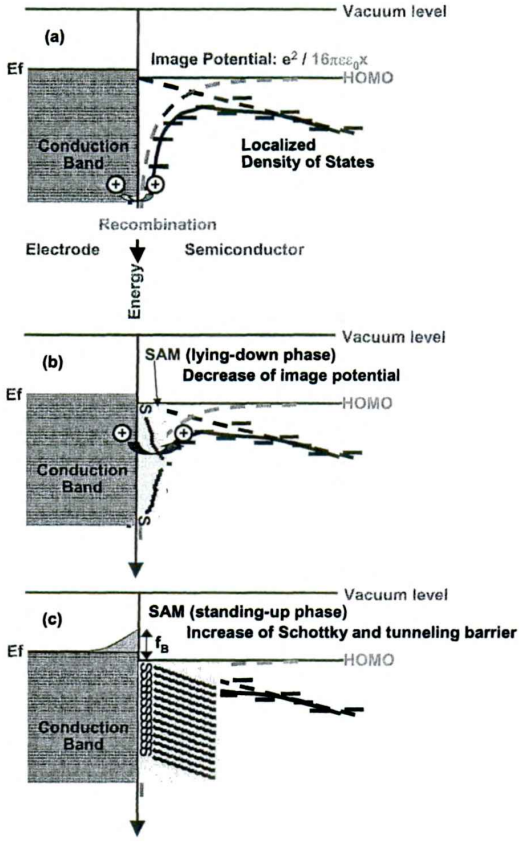


Fig.7 Energy potential at the interface to account for the model of charge carriers injection: (a) without SAM, (b) with SAM lying-down phase, (c) with SAM standing-down phase

which is nearly equal to the thickness of the SAM where the image potential is relatively small. It is considered the SAM of which thickness is moderate relieves the influence of

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the image potential and reduces R_c. However, when ODT molecules become standing on the electrode and increase the thickness of the SAM, the tunneling energy exponentially increases. This should be another factor other than the increased Schottky barrier for

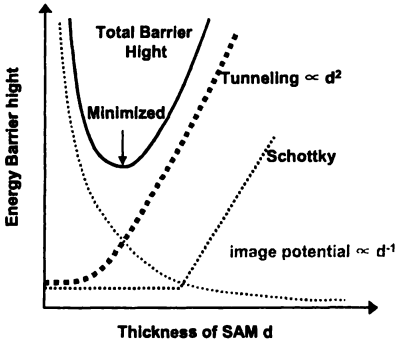


Fig. 8 Model of energy barrier at the interface between the electrode and semiconductor.

increasing R_c with an excessive treatment. It is considered the total energy barrier height at the interface ends up with the sum of Schottky, the image force and the tunnelig barrier height and it is minimized at a thickness of SAM in lying-down phase shown in Fig. 8.

In conclusion, the field-effect mobility of organic TFTs with a bottom-contact configuration is improved by a SAM with a long alkyl chain in the lying-down phase. In this phase, the SAM results in charge carriers being injected from the electrode to a state in the semiconductor where the influence of the image potential is small. Conversely, excessive treatment adversely affects the characteristics of the organic TFT with an increase in the Schottky barrier height and tunneling energy. Thus, optimizing the configuration of the SAM is important in controlling the height of the energy barrier at the interface between the electrode and the semiconductor.

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FLEXIBLE QVGA ACTIVE MATRIX DISPLAYS BASED ON ORGANIC ELECTRONICS

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Highly flexible QVGA active-matrix backplanes and integrated circuits are made on 25μm thin polymer substrates. This is realized in a process using only 4 mask steps, and applying 2 of the 4 structured layers from solution. Displays are made by combining these backplanes with an electrophoretic display effect from either E Ink Corporation or SiPix, resulting in 100μm thin electronic paper displays. These are the world's thinnest active matrix displays.

INTRODUCTION

Due to the roll-out of wireless networks and the ever increasing digitalization of information there is a growing demand for mobile displays. A disadvantage of the currently used glass-based mobile displays is that they are prone to damage, relatively heavy and, due to their inflexibility, often determine the size of the device they are used in. If one could make rollable displays, one could store a large display in a small device. In this way the size of the display would be decoupled from the size of the device it is used for.

For a flexible display one needs a display effect that tolerates bending and a flexible backplane. For the first, electrophoretic ink is a good candidate, since it has got no viewing angle dependence (contrary to LC displays), has a paper like appearance, is low power due to its bi-stability and can be applied to highly flexible polymer substrates[1, 2]. Using organic electronics, *i.e.* using an organic material as semi-conductor, with its maximum processing temperature of only 170°C, opens up the possibility to use highly flexible polymer substrates for the backplane. Although flexible active matrix backplanes have been made on steel foil[3], from the point of view of matching material properties of front and backplane, it is more convenient to use polymer substrates for the backplane as well. The use of solution processable organic materials instead of the more conventional inorganic materials leads to a simplification of the display manufacturing process (spin-coating of organic materials versus chemical vapor phase deposition of inorganic materials).

The first active-matrix displays using organic electronics, still made on glass, were reported in 2000[4]. One year later the first active matrix displays on polymer substrates using organic semi-conductors were shown[5].

Here we demonstrate the use of an organic semi-conductor and an organic insulator, both applied from solution, in highly flexible active-matrix QVGA backplanes, as well as

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the realization of logic functions in integrated circuits. Combining the backplanes with SiPix Microcup® electrophoretic film and E Ink® Imaging Film gives 130μm and 100μm thin bi-stable reflective QVGA displays, respectively.

ORGANIC TFT TECHNOLOGY

Bottom gate thin-film transistors (TFT), of which the layout is shown in Figure 1, are used. The geometry is comparable to the inverted staggered electrode structure as is

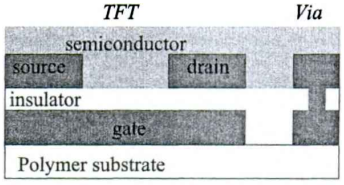


Figure 1 Cross section of a TFT and a vertical interconnect (via).

commonly used for amorphous silicon TFTs. A 25μm thin freestanding foil, as used as a substrate material for our backplanes, is too flexible to be processed directly. So, the first process step is to laminate the foil onto a rigid support. This enables the use of standard silicon processes, like spin coating, photolithography, etc. After processing the support is removed without influencing the properties of the backplane and can be reused. The demand on the registration of the different layers with respect to each other determines the choice of substrate material. The design used is based on a registration of the different layers with respect to each other of better than 5μm. So, between all the consecutive process steps, the foil should return within 5μm to its original dimensions. Polyethylene naphthalate has been found very suitable. The material is very well resistant against the chemicals used, and can be obtained in a highly crystalline form with a melting point of 265°C. This high crystallinity makes that the material can withstand our highest process of 170°C whilst its glass transition temperature is only 121°C[6]. Using this material a registration better than 2.5μm over a 150mm wafer for a 4-mask process is typically achieved. Given the specifications of sheet conductivity of the column and row lines in the display metallic electrodes are used. Gate electrodes and first level interconnects are made by patterning gold using photolithographic techniques, the advantage being that this gives the possibility to fully exploit the mature production equipment used in the established IC and AMLCD industry. The gate dielectric is a 350nm thick photo-structurable polymer (polyvinylphenol), which is applied by spin coating and is subsequently exposed to UV light to define contact holes. The source-drain electrodes, pixel pad and second level interconnects are defined in the second gold layer. On top of this stack, the semi conductor is applied by spin coating a 100nm thick precursor pentacene[7] layer. Shortly heating this layer to 170°C converts the precursor material to pentacene. The pentacene is structured using a subtractive photolithographic process.

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Backplane

The QVGA display contains 240 rows and 320 columns. The pixel size is 300x300μm² resulting in a display diagonal of 4.7 inch. The pixel layout is given in Figure 2. The TFT channel length (L) and width (W) are 5μm and 140μm respectively. The display has an optical aperture of 79%. Table 1 gives a summary of the specifications of the QVGA backplane.

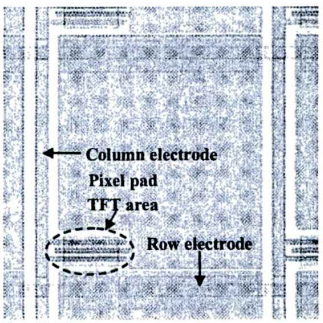


Figure 2 Pixel layout of the display.

Table 1 Summary of the QVGA backplane specification.

Backplane size	**4.7inch (72mm x 96mm)**
Resolution	**320x240 (85ppi)**
Number of pixels	**76800**
Pixel size	**300 m x 300 m**
Aperture ratio	**79%**
Backplane thickness	**25 m**
Backplane weight	**0.39grams**
TFT channel length	**5 m**
TFT channel width	**140 m**
Mobility	**0.01cm²/Vs**
Current modulation	**10^6**

Transistor characteristics

Devices made using the technology mentioned above have an average field effect mobility of 0.01cm²/Vs at a gate bias of –20V. Transfer characteristic of an organic TFT are given in Figure 3a. An impression of the uniformity of the mobility as measured on

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an active-matrix backplane is given in Figure 3b. The current modulation, measured between a gate bias of 10V and –20V, exceeds 10^5.

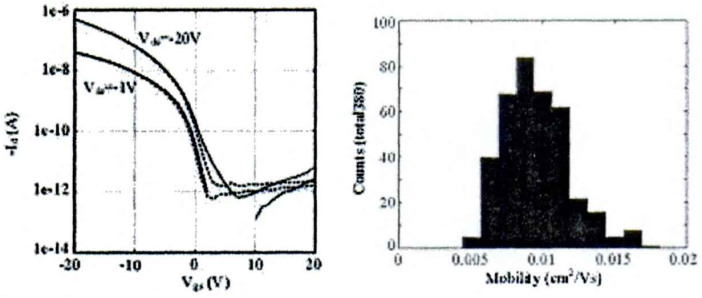


Figure 3 (a): Transfer characteristics of a pixel TFT with a typical mobility of 0.01cm²/Vs. (b): Distribution of the linear mobility on a QVGA active-matrix backplane based on measurements of 380 pixel TFTs, extracted from the transfer characteristics for V_{GS}=-20V and V_{DS}=-1V.

Functional displays

The QVGA active-matrix backplanes are combined with two different kinds of electrophoretic display effects, SiPix and E Ink. SiPix uses "microcups" containing positively charged white sub-micron particles and a colored ink[8]. Contrast is obtained by moving the particles either to the viewer's side of the cup generating a white state, or to the opposite side generating a color given by the ink, in this case blue. The Microcup® electrophoretic foil is laminated onto the active-matrix backplane, resulting in a 130µm thin display. Figure 4 shows a Sipix display. A pixel voltage of 15V is used, resulting in a switching time of 1s. The display shows an image containing 4 gray levels, while rolled into a 1cm diameter stick.

E Ink uses for their electrophoretic display effect micro capsules filled with a transparent fluid containing black and white sub-micron particles[1]. These particles have opposite charge. Using an electric field the particles can be moved. The particles closest to the viewer, determine whether a white, scattering state, or a black, absorbing state is observed. Figure 5 shows a 100µm thin display obtained by laminating E Ink® Imaging Film onto a backplane. Using a pixel voltage of 15V a switching time of 0.5s is obtained. The optical contrast is 12.

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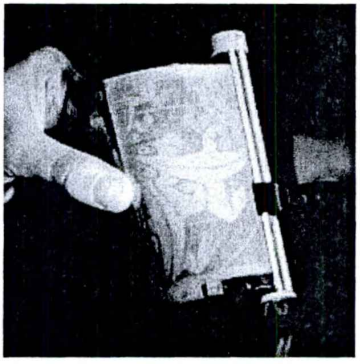


Figure 4 A picture of a rollable QVGA active-matrix display using organic TFT's combined with SiPix's Microcup® electrophoretic film.

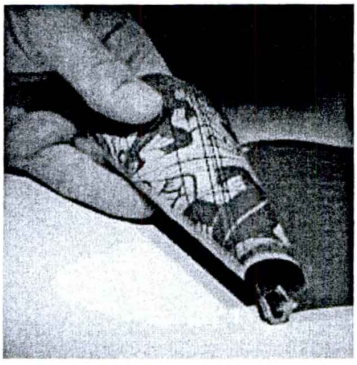


Figure 5 A picture of a rollable QVGA active-matrix display using organic TFT's combined with E Ink's ® electronic ink electrophoretic film.

Shift registers

In the current backplane design every row has an individual external connection. This leads to a total of almost 600 connections (320 columns + 240 rows). Using a line-by-line addressing scheme for the display, the row connections can be replaced by a shift register. In the shift register, the row selection pulse is shifted from one stage to the next

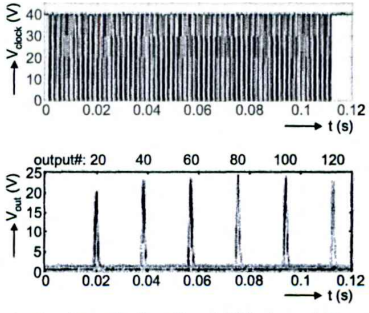


Figure 6 Clock and output pulses of a functional 120-stage shift register operating at a clockfrequency of 1kHz.

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at every clock pulse. Stand-alone shift registers with up to 120 stages have been made using the same technology as used for the backplanes. Figure 6 shows the measurementresults of a 120-stage shift register. Both the clock pulses as well as the output pulses for every 20th stage are shown. The shift register contains over 2000 transistors, the highest integration level to date for organic electronics.

CONCLUSIONS

A technology based on organic electronics is presented which is used to make highly flexible, even rollable, displays. Integration of the row drivers on the flexible backplane may well be possible as evidenced by the manufacturing of stand-alone shift registers in the same technology.

ACKNOWLEDGEMENT

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STUDY OF ORGANIC FIELD-EFFECT TRANSISTORS FROM POLY-3-OCTYLTHIOPHENE SOLUTIONS ON DIFFERENT GATE DIELECTRICS

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ABSTRACT

We compared several gate dielectrics useful for organic thin film transistors (OFET) on flexible substrates: spun on benzocylobutene and polyimide, anodically grown Al_2O_3, reactively sputtered Ta_2O_5 and mixed Ta_2O_5/SiO_2; for comparison we included thermally grown SiO_2. Commercially available P3OT and P3HT have been applied as organic semiconductors, mainly via spin coating, additionally we tested ink-jet printing. Although organic dielectrics revealed good coverage, they failed at very thin films. With respect to electrical behavior as gate dielectrics Ta_2O_5/SiO_2-films turned out to be best, because of its high permittivity accompanied by excellent insulation characteristics. Nevertheless, it introduces problems with mechanical stresses and susceptibility to cracking. Anodically grown Al_2O_3 might be a good candidate from an overall point of view, but we ended up with a strong dependency of breakdown behavior on area due to defects that prevented successful OFET preparation. We built up OFETs on Ta_2O_5, Ta_2O_5/SiO_2, and BCB with the Ta_2O_5 ones exhibiting very low gate voltages of 3 V for full operation with a I_{on}/I_{off}-ratio of about 300.

INTRODUCTION

One promising field of application of organic transistors is electronics on flexible substrates [1, 2]. In order to achieve this, the thermal SiO_2 dielectrics often used for research purposes has to be replaced by a gate dielectric that can be deposited at low temperatures. Several dielectrics have been tested for this purpose by other researchers already, this covers mainly spun on common photoresist [3], photo-acryl [4], polymethylmethacrylate [5, 6], polyimide [6, 7, 8], and polyhydroxystyrene [2, 9], different self-assembled organic monolayers [10], evaporated parylene [6, 7], sputtered SiO_2 [11], and Si_3N_4 [12], and anodically grown Al_2O_3 [13, 14] and Ta_2O_5 [15].

On one hand side, this dielectrics should be processable from solution in order to ease the process, to enable printing technologies, and to end up with a fully organic low-cost transistor. On the other side the gate capacitance should be as high as possible in order to allow low gate voltages for current control. This calls for thin dielectrics with high permittivity. Unfortunately, common soluble polymer dielectrics do not show high permittivities, and common anorganic thin film dielectrics have to be vacuum deposited to keep their good electrical properties.

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We compared spin-coated commercially available polyimide (Brewer Science) and benzocyclobutene (Dow), anodically grown Al_2O_3, and reactively sputtered Ta_2O_5 and mixed Ta_2O_5/SiO_2 for that purpose.

In order to obtain a high transconductance of the transistor, i.e. to control the transistor with a low gate voltage, the gate dielectrics has to have a high permittivity and a low thickness while maintaining good insulation. This can be summarized with the maximum gate charge Q/A_{max} density as a figure of merit for the comparison of gate dielectrics:

$$Q/A_{max} = \varepsilon_r \cdot \varepsilon_0 \cdot E_{bd} \quad (1)$$

with ε_r, ε_0 - the relative and absolute permittivity, and E_{bd} - the break-down field strength.

EXPERIMENTAL

At first we studied the insulating and dielectric behavior of blanket dielectric films within metal-insulator-metal- (MIM) -structures on rigid Si substrates, independently on transistor design (see fig. 1). Sputtered AlSi1-films have been used as blanket ground electrode.

Benzocylobutene (BCB XU, Dow) and polyimide (PI T-1001, Brewer Science) were spun on from precursor solution with thicknesses of 250 - 900 nm and 150 nm, respectively, and baked according to the manufacturer's recipes [16].

Al_2O_3-films were anodically grown on the aluminum underlayers up to 100 nm thicknesses from both organic (ethyleneglycole) and aqueous electrolyte solutions of tartaric acid. [17]. With this method the final Al_2O_3-thickness can be controlled via the maximum anodization voltage: Making use of a compact flow cell we obtained a very homogeneous deposition with a thickness variation of less than 4% across a whole 4"-wafer and a roughness below 1 nm.

Ta_2O_5-films and mixed films of Ta_2O_5/SiO_2 (125 - 200 nm) were reactively sputtered with a Ar-O-plasma of a rf-magnetron source from a Ta and Ta_5Si_3-target, respectively. Controlling the deposition conditions, namely argon and oxygen flow, we obtained nearly stoichiometric Ta_2O_5- and Ta_2O_5/SiO_2-films with a slight excess in oxygen [18]. Because those films were intentionally developed as encapsulation layer for solar cells, they exhibit large compressive stresses. Having the target of flexible electronics in mind, we were able to decrease the mechanical stresses to below 200 MPa by varying the Ar-pressure.

Finally, we introduced as reference samples thermally grown SiO_2 (140 nm) for comparison.

Top electrodes of Al were deposited using evaporation via shadow masks. Alternatively we attached evaporated Ti/Au electrodes using lift-off patterning with the same preparation as used for OFETs.

Organic thin film transistors were prepared on rigid substrates of Si/SiO_2/AlSi1 and AlSi1/doped Si, respectively, with the gate dielectrics mentioned above. Because of their similar structure with bottom gate, bottom contact design, the same preparation sequences were applied to obtain the initial test vehicles (see fig. 2). Source-/drain-electrodes of 25 nm Ti and 125 nm Au were evaporated and lift-off patterned for devices of 20 - 50 µm channel length and 1 - 3 mm channel width.

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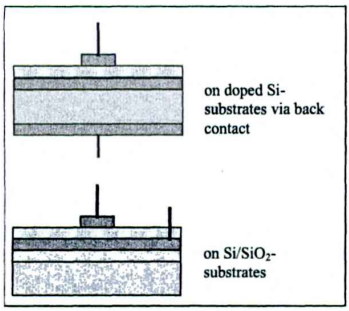


Fig. 1: MIM design for insulator characterization

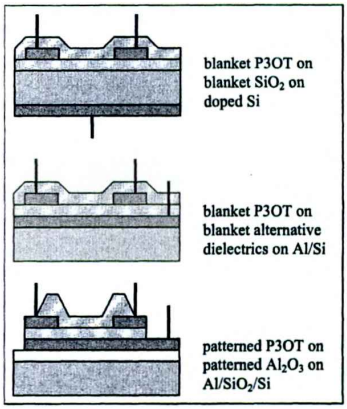


Fig. 2: Transistor design and tips

Poly-3-octylthiophene (P3OT) and poly-3-hexylthiophene (P3HT), both from Aldrich, were chosen as organic semiconductors. They were deposited onto the test vehicles using spin coating from chloroforme solution under nitrogen atmosphere.

In order to avoid excessive gate leakage accompanied with blanket semiconductor films, and to take account of patterned gate dielectrics in certain cases, we additionally introduced ink-jet printing of lines of the organic semiconductors. This was performed from chlorobenzene and xylene solution of the semiconductor using a pipetting tool with a technology described elsewhere [19].

RESULTS AND DISCUSSION

At first we measured the capacitances and break-down voltages under applied voltage-ramps at the MIM-structures with different dielectric films, and calculated the geometry independent parameters. Table I summarizes the mean data for midrange electrode areas of 10,000 - 100,000 μm^2.

Table I: Electrical insulator properties

dielectric	relative permittivity ε_r	break-down field strength E_{bd} [MV/cm]	maximum gate charge (avg.) Q'_{max} [10^{-6} As/cm^2]
thermal SiO_2	3.9	6 - 7.5	2.3
BCB	3.0 - 3.3	1 - 3	0.6
PI	~ 3	.. 2	0.5
anodic Al_2O_3 (from aqueous	6.5 - 9.5	2.3 - 3.5	2.1

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solution)			
Ta_2O_5	26 - 28	1.3 - 3.3	5.6
Ta_2O_5/SiO_2	12.5 - 14.5	5.5 - 8	7.8

PVD mixed Ta_2O_5/SiO_2-films clearly turn out to work best as a gate dielectric for our purposes. They exceed thermal SiO_2-performance by a factor larger than 3. This is mainly engendered by the combination of both comparatively high permittivity, and excellent ultimate field strength. Unfortunately, pure Ta_2O_5-films with the highest permittivities obtained here, were falling behind due to earlier break-down. Obviously, the additional SiO_2 within the mixed films strongly enhances an amorphous structure of the films, that suppresses early current paths. Although we managed the reduction of the mechanical stresses within those film down to values appropriate to flexible electronics, the Ta-based dielectric films are still susceptible to cracking on polymeric substrates.

The commercially available insulator materials for spinning-on of very thin films in electronic devices were developed as low-*k*-dielectrics in line-stacks, consequently they do not allow high gate charges. One advantage of polymeric films should be good coverage of the underlying relief. This proved right for PI, but it did not for thin BCB films. As a result, the rather improper performance of BCB is further decreased by the fact, that we did not succeed in keeping the moderate break-down field strength at films thinner than approx. 500 nm, whereas the other insulators were introduced with about 100 - 200 nm in thickness.

Anodically grown Al_2O_3-films present themselves with moderate electrical properties at a level of conventional thermal SiO_2. One advantage of those films is, that they can be grown into holes of photoresist masks, and by this additively patterned already during deposition (fig. 3). This enables an easier integration of several transistors to organic electronics, although the non-independence of patterning establishes some further problems. In order to allow this, we had to switch to aqueous electrolytes with a bit diminished insulator properties, because we had to avoid electrolyte and mask interaction that was present at the organic electrolyte. Fig. 4 displays a 3-layer patterned test-vehicle for OFET preparation on anodic Al_2O_3, unfortunately, electric break-down happened earlier at those devieces due to the action of the developper for S/D-lift-off.

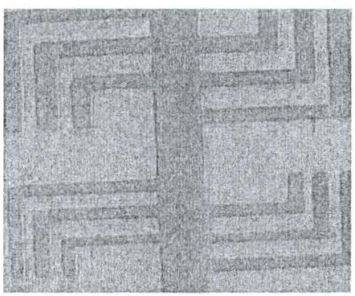


Fig. 3: Additively patterned anodic Al_2O_3

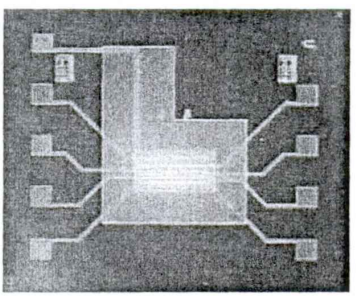


Fig. 4: 3-layer (Al-gate, anodic Al_2O_3-gate dielectric, Au-S/D) patterned test-vehicle on Si for OFET preparation

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Quite noteworthy, the values given here do not represent an intrinsic limit of the materials themselves, but the actual mean of a spready defect induced distribution. This implies on one hand side, that further increase in performance should be available, but on the other hand, that the data strongly depend on geometry. This is one reason, that we did not succeed in the preparation of OFETs on Al_2O_3: at the higher electrode areas accompanied with that patterns the dielectric failed still earlier.

The semiconductor solutions wet the non-conventional dielectrics much better than SiO_2 surfaces after chloroforme pretreatment for hydrophobization. This might, in future, lead to better interface properties, and by this, to higher charge carrier mobilities in the semiconductor. Though, until now we ended up with mobilities of up to $3 \cdot 10^{-4}$ Vs/cm² on Ta_2O_5 and Ta_2O_5/SiO_2 and $1 \cdot 10^{-4}$ Vs/cm² on BCB in comparison to up to $2 \cdot 10^{-3}$ cm²/Vs on thermal SiO_2 with the same structures (see below and fig. 5, 6).

In spite of the fact, that we obtained OFETs with blanket PAT and substituted oligothiophene semiconductor films on Si/SiO_2 samples with moderate properties [16, 17, 20, 21], the problems with gate leakage increased on the non-conventional gate dielectrics under investigation. Over that, early gate break-down occurred. Therefore, most results were obtained with ink-jet patterned semiconductors. Figs. 5 and 6 display the out-put characteristics of two transistors with ink-jetted semiconductors on BCB and Ta_2O_5/SiO_2, respectively. Although the semiconductor performance is still moderate (see above), the advantage of the high-*k*-dielectrics, the control of the transistors with lower gate voltages becomes clear. Ta_2O_5 works still better in this direction, we obtained a switch-on gate voltage step of only 3 V with ink-jetted P3HT on 190 nm Ta_2O_5, even though the carrier mobility was $1 \cdot 10^{-4}$ Vs/cm² only.

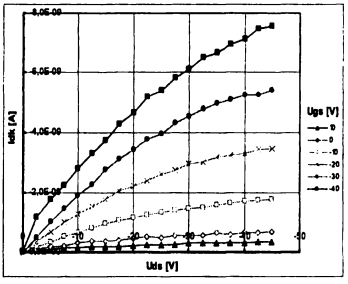


Fig. 5: Out-put characteristics of ink-jetted P3OT-oFET on 850 nm BCB (35x1000 µm² channel)

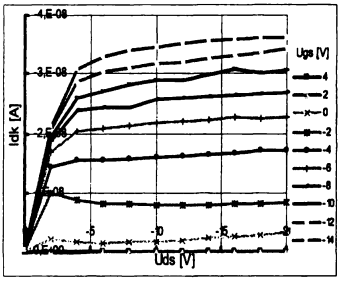


Fig. 6: Out-put characteristics of ink-jetted P3HT-oFET on 100 nm Ta_2O_5/SiO_2 (15x3000 µm² channel)

CONCLUSIONS

Mixed Ta_2O_5/SiO_2-films from reactive rf-sputtering were working best among our candidates for gate dielectrics because of highest possible gate charges, and excellent insulation behavior even at higher electrode areas. Nevertheless, because of the suscep-

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tibility to cracking of Ta-based dielectrics on flexible substrates, we suggest anodic Al_2O_3 to be considered for further application because ease of patterning.

The reduction of the semiconductor area via patterning turned out to be a key issue for OFETs on non-conventional gate dielectrics because of the strong defect induced area dependence of the electric break-down of those films. Therefore, ink-jet printing reveals to operate as work-horse for device and materials development.

We obtained OFETs on Ta_2O_5 and Ta_2O_5/SiO_2 dielectrics with $1 \cdot 10^{-4}$ Vs/cm² and $3 \cdot 10^{-4}$ Vs/cm², respectively. The much better wetting behavior of the semiconductor solutions on those films compared to SiO_2 yielded more homogenous films which might lead to better semiconductor-dielectric interfaces in the near future.

ACKNOWLEDGMENTS

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A NOVEL TFT-DRIVEN MICROCHANNEL ELECTROPHORESIS DEVICE FOR PROTEINS SEPARATION AND IDENTIFICATION

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ABSTRACT

A new protein separation and detection device that uses an amorphous silicon (a-Si:H) thin film transistor (TFT) to drive a microchannel electrophoresis has been fabricated and investigated. Three model proteins in a mixture were separated and identified from the current vs. time curve, which could be used to calculate individual protein's mobility. This *in-situ* method needs no complicated protein labeling and optical scanning procedures. One of the critical issues of the microchannel electrophoresis device is the current perturbation at the early stage of the operation, which can affect the overall signal identification. When a TFT is connected to the microchannel device, it functions as a current regulator diminishing the perturbation phenomenon. Therefore, proteins can be easily identified in a short period of time. This device can be a potentially important for identifying various biomolecules.

INTRODUCTION

Recently, microcapillary or microchip electrophoresis devices have been extensively developed for DNA or protein electrophoresis [1,2]. Protein or DNA could be separated, with or without the presence of polyacrylamide gel in the capillary or channel, using a high electric field of 100-600V/cm [1,2]. Some advantages of these devices include a small sample volume, short analysis time, and ease of operation. However, there are several disadvantages associated with them. Protein or DNA has to be labeled with fluorescent chemicals, which is a time consuming procedure and requires a massive optical equipment to detect the laser induced fluorescence (LIF) signals.

Kuo and Lee recently reported a new type of microchannel device that separated and detected protein *in situ* [3,4]. A drastic increase of the contact resistance at the detection electrode surface during the adsorption of protein molecules was used to detect the separated proteins. The adsorption shows up as a peak in the current change rate (dI/dt) vs. operation time (t) curve. The principle of the microchannel electrophoresis is similar to, but slightly different from, that of a conventional slab-type electrophoresis. In the slab-gel system, proteins are separated into different bands inside of the gel. They are then stained for easy detection. However, in this new microchannel system, all separated proteins pass through the gel into the detection reservoir. After reaching the detection reservoir, the protein is quickly migrated and adsorbed onto the surface of the detection electrode. Since different proteins arrive at the electrode at a different velocity, there are several sharp drops in the current *vs.* time (I-t) curve. The time of a sharp current drop corresponds to the arrival of a specific protein. However, at the early electrophoresis stage, the current (I) fluctuates drastically [2,4]. In this case, differentiation of the

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fluctuation peak from the protein detection peak will be a complicated procedure. Therefore, this kind of device suffers from high signal noise at the beginning.

Since amorphous silicon (a-Si:H) thin film transistors (TFT) have a stable drain current (I_d) under normal operation conditions, they can be used as a current stabilizer when connected to the microchannel electrophoresis device.

EXPERIMENTAL

Masks for the inverted staggered TFTs and the microchannel devices were designed using an integrated circuit (IC) mask design tool, L-Edit Pro (Ver 9.2, Tanner EDA Inc., Pasadena, CA). Only two photomasks were required for the complete TFT. The TFT fabrication process is described as follows. First, molybdenum (Mo, 1200 Å) was deposited by DC sputtering on the Corning 7059 glass and patterned into the gate electrode using the first mask. Second, the tri-layer structure of SiN_x (3000 Å)/ a-Si (500 Å)/ SiN_x (2000 Å) was deposited with PECVD (Applied Materials, AMP 3300 I, Santa Clara, CA) with the one-pump-down process at 250°C. The plasma was driven by a 50 kHz rf power supply. The a-Si:H layer was deposited under the condition of 70 sccm SiH_4, 250 mTorr, and 250 W. The top SiN_x channel protection layer was then defined by backlight exposure using the gate as the self-aligned mask [5,6]. A chromium (Cr) layer was sputter deposited and defined into the source and drain electrodes with the second mask. The feed and detection electrodes of the microchannel electrophoresis device were completed at the same time. The n^+ layer was reactive ion etched (Plasma-Therm, model 700D, St. Petersburg, FL) using a gas mixture of CF_4 (2 sccm) and Cl_2 (8 sccm) at 100 mTorr and 250 W.

A thick layer (30 μm) of negative photoresist (NANO SU-8, MicroChem Corp., Newton, MA) was spin-coated and patterned into the channel and reservoirs of the electrophoresis device using a third mask. The channel has a dimension of 495 μm wide, 29 μm deep, and 5 mm long.

The top of the channel region was covered and sealed with a cellulose tape. A small amount of 15 % polyacrylamide gel (PAGel) solution was fed at the feed reservoir, which automatically filled the channel region due to the capillary effect. The gel was polymerized inside the channel within 5 min at room temperature. The gel solution was consisted of 15% acrylamide/bis-acrylamide (29:1), 0.75% ammonium persulfate, 0.2% SDS, and 0.3% tetramethyl-ethylenediamine (TEMED) in 0.045 M tris-borate and 0.001 M EDTA solution at pH 8.2 (0.5× TBE) containing 0.2% SDS.

In this experiment, the detection electrode (2.8 mm^2) was connected to the source electrode of the TFT. The electrophoresis process was done by applying 10 V (V_d=10 V) between the drain electrode and feed electrode of the TFT. Three proteins mixture, *i.e.*, ovalbumin (45 kDa), carbonic anhydrase (29 kDa), and α-lactalbumin (14.2 kDa), were prepared by dissolving lyophilized powders in a 0.5× TBE solution. The solution was heated to 98°C for 3 minutes to denature the protein. A 1 μl of protein (1000 μg/ml) solution was loaded into the feed reservoir. The electrical current (I) vs. time (t) was measured with an Agilent 4155C semiconductor parameter analyzer.

RESULTS AND DISCUSSIONS

Figure 1 shows electrical characteristics of a completed TFT: (a) output

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characteristics and (b) transfer characteristics of I_{ds}-V_{ds} curves of an a-Si:H TFT made of SiN_x ($SiH_4/NH_3/N_2$ 30/120/720 sccm) and a-Si:H (SiH_4 70 sccm). In Fig. 1(a), the curves show no severe crowding phenomena, which means the n^+ layer to intrinsic a-Si:H contacts are ohmic [5,6]. In Fig. 1(b), the measurements were done after a 1 hour annealing at 250°C in atmosphere. The calculated field effect mobility is 0.127 cm^2/Vs and the threshold voltage is 5.9 V with a channel width 39 μm and a channel length 88 μm.

Reactive Ion Etching (RIE) was also critical to the device performance because it has been shown that the plasma radiation from RIE can increase the TFT threshold voltage and leakage current by damaging the gate dielectric film and the top and bottom interfaces [5,6]. After the annealing, no V_{th} shift and anomalous high leakage current due to RIE process were detected.

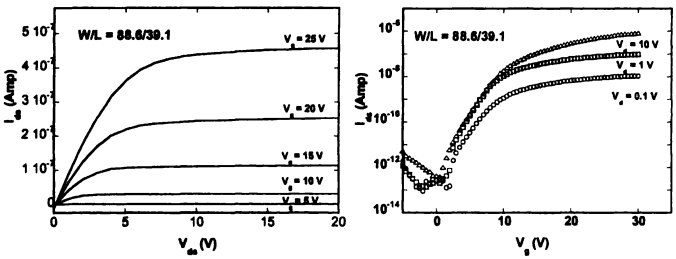


Figure 1. Electric characteristics of an a-Si:H TFT; (a) output characteristics and (b) transfer characteristics.

Figure 2 shows the general relationship between the reflective index (RI) of gate SiN_x and corresponding TFT threshold voltage (V_{th}). The two curves are from different PECVD systems with different electrode configurations and design. The top curve was from a 50 kHz rf (low frequency) power supply and the bottom curve was from a 13.56 MHz rf (high frequency) power supply (6). In addition to thin film deposition conditions, TFTs in the two curves have different configurations (W/L = 88/39 μm vs. W/L = 100/16 μm). However, both curves show the same trend, i.e., the lowest values of V_{th} occurs in a small range of gate SiN_x reflective indices, *i.e.*, 1.85 - 1.90. The low frequency condition has a higher overall V_{th} (4.7 – 7.6 V) than the high frequency V_{th} (2.0 – 4.5 V). This is probably because plasma damages from the low frequency power source to the gate dielectric interface and the gate dielectric are more serious than those from the high frequency power source.

The feed gas composition also affects the V_{th} value. For example, for the 50 kHz power source, the lowest V_{th} occurs at the gate SiN_x feed of $SiH_4/NH_3/N_2$ 30/120/720 and 40/160/720; for the 13.56 MHz power source, it occurs at $SiH_4/NH_3/N_2$ 10/80/500 and 20/80/500. Since Si-H and N-H are usually hole and electron trapping centers, the film with the lowest threshold voltage probably contains an optimized NH/SiH area ratio [7]. Bi- or multi-layer a-Si:H TFTs are often reported to have a higher mobility than a single-layer TFT of the same a-Si:H thickness. Therefore, TFT characteristics in Fig. 2 can be further improved by optimizing the a-Si:H deposition condition.

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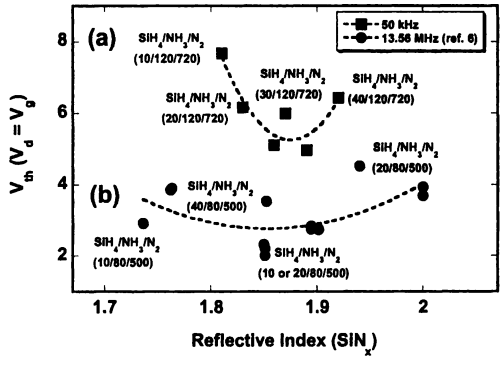


Figure 2. Threshold voltage of a-Si:H TFT depending on reflective index of dielectric SiN_x film.

The electrical current vs. time curve (I-t) for the microchannel electrophoresis was transformed into the dI/dt-t curve optimized with the Savitsky-Golay method with an order of 3 and 9 data points [8]. In order to improve PAGel affinity to the SU-8 channel surface, the microchannel device was treated with O_2 plasma. After the plasma treatment, no interfacial bubble between PAGel and SU-8 microchannel sidewall was observed. Electrical properties of the TFT, such as the output and transfer characteristics, were not influenced by the O_2 plasma exposure process.

Figure 3 shows (a) a microscopic image and (b) a simplified description of the TFT-driven microchannel device.

In order to investigate the stability of the system, a TFT and a TFT connected to gel-filled microchannel without the existence of proteins were stressed under a constant V_g (30 or 40 V) and V_d (10 V) for 2400 sec. The result showed that the I_d decreased with the operation time. The current decrease with the stress time, which is due to the deterioration of the interface and the bulk a-Si:H layer, follows the exponential relationship [9,10]. Therefore, the I_d curves of the TFT and the TFT plus gel-filled microchannel were linearly dependent on the logarithmic time scale. After the 4800 sec stress on the TFT-electrophoresis unit, the TFT had a large V_{th} shift of 14.8 V.

When a TFT was connected to a gel-filled microchannel with proteins loaded, the I_d–t curve showed small fluctuations for the entire operation period. A drastic drop of the curve when each separated protein arrived the detection electrode was observed, too. In addition, the total resistance of the system increased with the incorporation of gel to the channel region and loading of proteins in the feed reservoir. The total current value decreased significantly.

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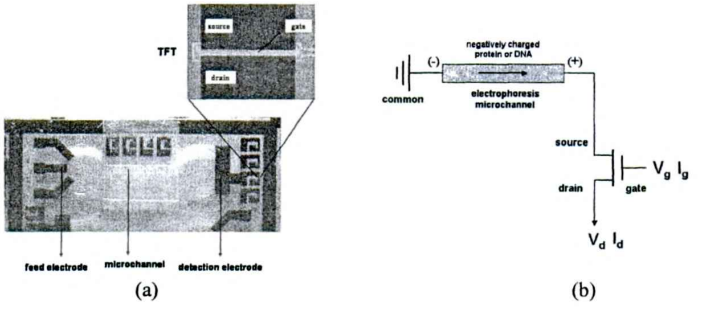


Figure 3. (a) Microscopic image and (b) schematic diagram of the TFT-microchannel electrophoresis system.

Previously, authors observed that the current of a microchannel electrophoresis fluctuated severely at the beginning of the operation [3,4]. There are many possible causes for this perturbation of the current readings. For example, the system was not equilibrated when the voltage was initially applied. In addition, part of the solution might have been evaporated due to the sudden rise of temperature when the current was applied [2,4]. The current fluctuation needs to be suppressed in order to make it easy to identify the protein peaks.

Figure 4 shows the dI/dt vs. t curves of (a) a gel-filled microchannel device of which the channel was made from KOH solution etched silicon coated with a thin sputtered SiO_2 layer, (b) a gel-filled microchannel device of which the channel was made from the spin coated SU-8 film after O_2 plasma treatment, and (c) Fig. 4(b) microchannel device connected to an a-Si:H TFT. Fig. 4(a) is re-plotted from the data of ref. 4. The effective migration speed (channel length divided by the peak time) of the protein decreases with the increase of its molecular weight in all graphs. These results are consistent with those of conventional electrophoresis [11]. The peak intensity of the TFT-connected system (Fig. 4(c)) is more than one order of magnitude lower than that without TFT connected (Fig. 4(b)). When the electrophoresis was operated without a TFT connected, the current was higher than that with the TFT connected. This is because the later is limited by the magnitude of the on-current of the TFT, which is lower than that of the microchannel device.

Figure 4 clearly shows that the incorporation of a TFT removed the severe initial current perturbation. Since the same kind of protein sample and same type of microchannel material were used in the test, the peak time for each protein in Fig. 4(b) and (c) is almost the same. In Fig. 4(c), the migration velocities of α-lactalbumin (14.2 kDa), carbonic anhydrase (29 kDa), and ovalbumin (45 kDa) are estimated to be 5.5, 3.8, and 1.9 cm/hour, separately, under 10 V/cm. The corresponding velocities in Fig. 4(a) are 5.4, 3.85, and 2.22 cm/hour, separately, under 11.8 V/cm. Therefore, the protein migration speed is little influenced by the channel material.

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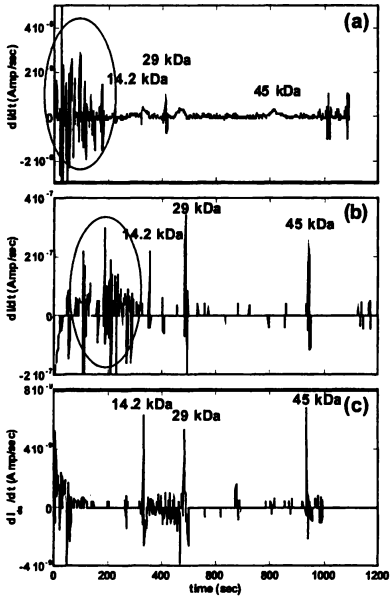


Figure 4. The dI/dt vs. t curves of (a) a gel-filled Si microchannel device (b) a filled-filled SU-8 microchannel device, and (c) a gel-filled SU-8 microchannel device connected to an a-Si:H TFT.

For each protein, the mobility values of the two Si-based and SU-8 based systems are almost same because there are no significant differences in the microchannel's geometrical factors, *i.e.*, depth, width, and length [4]. The SU-8 microchannel without a TFT connection in Fig. 4(b) is less noisy than the KOH etched Si microchannel in Fig. 4(a). The difference is related to the channel wall material. The Si microchannel has a SiO_2 coating. The SU-8 channel contains the SU-8 sidewall and PECVD SiN_x bottom layer both of which were oxidized with O_2 plasma. The Fig. 4(b) or (c) channel surface has a higher affinity for the DNA solution than the Fig. 4(a) surface does [12].

The mobility can be calculated by dividing the velocity by the electric field, *i.e.*, 10 V/cm in this experiment. Compared to the mobility of a conventional slab-type SDS-PAGE, the mobility of the TFT connected microchannel is higher than that of the typical slab-type electrophoresis [9]. This difference may be due to factors such as the geometry of the channel cross-sectional area and the chemical properties of the channel wall.

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CONCLUSIONS

In conclusion, the authors reported a new type of TFT-driven microchannel for protein separation and identification. The a-Si:H TFT was fabricated using the 2-photomask process and the PECVD deposition method. Multiple distinct proteins were separated and identified with the new TFT-connected microchannel device. The connection of the a-Si:H TFT removed the undesirable current perturbation phenomenon in the early operation stage, which makes it easy to identify proteins. The TFT connected to the microchannel acted as a current regulator to suppress the signal noise. The mobility of the protein does not change with the connection of the TFT to the microchannel device. It is also independent of the channel material.

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HYDROGENATED AMORPHOUS SILICON BIPOLAR JUNCTION THIN FILM TRANSISTORS (a-Si:H B-TFTs)

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ABSTRACT

A bipolar junction transistors made of a-Si:H thin films has the potential advantages of a conventional bipolar junction transistors, such as large current driving ability and high switching speed, and low thin film deposition temperatures, which supplies a very thin base layer and may result in the device's low power consumption. In this study, authors fabricated n-p-n bipolar junction transistors from a-Si:H thin films (B-TFT). A stacked structure of $n^+/i/p/i/n^+$ of a-Si:H thin films was used to form emitter/base/collector layers. All a-Si:H layers and the SiN_x passivation film were deposited by PECVD at 250°C. The complete transistor was fabricated using five masks. The proper film thicknesses for good junction behaviors were obtained from studying the a-Si:H p-i-n diode characteristics, separately. The B-TFT showed a current gain of 3~6 and a current of ~50 μA both of which are larger than the literature values. The current noise might be contributed by the high defect densities at junction interfaces, especially the interface between the base and the emitter. The "OFF" current of a few micro-amps and the right shift of the knees in the I-V curves are attributed to the parasitic p-n diodes formed between the base and the collector outside of the emitter active region. The high series resistance of the base layer in the extrinsic region needs to be solved to improve the transistor characteristics.

INTRODUCTION

The conventional single crystalline silicon-based bipolar junction transistor (BJT) has a larger current driving ability and a faster switching speed than the field effect transistor (FET). But, it also has larger power consumption. The conventional a-Si:H TFT can be fabricated on a large substrate using low temperature plasma enhanced chemical vapor deposition (PECVD) films. However, the a-Si:H TFT suffers from a low "ON" current and a slow switching speed because of high defect densities in the bulk a-Si:H film and at the a-Si:H/gate dielectrics interface. If bipolar transistors can be fabricated using low temperature PECVD a-Si:H films, limits on current driving and switching speed could be solved. In addition, since the a-Si:H film can be prepared very thin, the power consumption can be low. Also, since the a-Si:H film is amorphous, it will not form pipes between the emitter and the collector, which is a yield-killing factor for the epi-based bipolar process.

In spite the promising prediction, there are many technical challenges in fabricating a-Si:H B-TFT, such as the lower charge carrier mobility, the very short minority carrier diffusion length, and the very large lateral resistance of thin a-Si:H films [1]. So far, there is only one report on the a-Si:H B-TFT with limited information on device characteristics

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and the fabricated process [2]. In this research, we fabricated the n-p-n a-Si:H B-TFT structure by means of conventional TFT processes and materials, which is applicable to the low-temperature substrates. Device characterizations were done on the complete B-TFT. Influences of the process on the device characteristics were also investigated.

EXPERIMENTAL

A-Si:H diodes, which are major components of a-Si:H B-TFTs, were investigated in order to find the optimized film thickness for each a-Si:H layer in the transistor. The diode was made from a film stack of Cr/Mo/n^+/i/p/p^+/Mo, where Cr was used for the bottom electrode, Mo was the contact metal, n^+ was the heavily phosphorus-doped a-Si:H layer, i was the intrinsic a-Si:H layer, p was the lightly boron-doped a-Si:H layer, and p^+ was the heavily boron-doped a-Si:H layer. The fabrication process includes: 1) sputter deposition of Cr/Mo, 2) PECVD of stacked a-Si:H layers in one pump-down at 250°C, 3) sputter deposition of top Mo, 4) photoresist spin coating and patterning with a mask, 5) wet etching of top Mo film, 6) dry etching of the stacked a-Si:H n^+/i/p/p^+ layers, 7) photoresist striping, and 8) device annealing at 240°C in atmosphere for 1 hour. The thickness ranges of each layer in the n^+/i/p/p^+ stack were about 18-30 nm/20-200 nm/15-30 nm/15-30 nm. The PECVD p and p^+ processes were developed previously.

The cross-sectional and top views of the B-TFT in this study are shown in Figures 1 and 2. The collector is at the bottom and the base and emitter are on the top. A contact aligner was used to define all of the patterns, which were then etched with either a plasma process or a wet solution. To fabricate the B-TFT, five masks were used, i.e., for device active islands (mask 1), emitter contacts (mask 2), emitter electrodes (mask 3), base contacts (mask 4), and base electrodes (mask 5), respectively. As shown in Fig. 1, the stack from emitter to collector was Mo-n^+_2-i_2-p-i_1-n^+_1-Mo-Cr. The thickness range of i_1 layer was 60-200 nm, and that of the i_2 layer was 20-80 nm. A thin i_2 layer was used to shorten the electron diffusion distance from emitter to base. The n^+_1/i_1/p stack was deposited in one pump-down and then defined by the first mask. The i_2/n^+_2 stack was also deposited in one pump-down and defined with Mo using the third mask. The SiN_x layer was used as the dielectric material as in a conventional field-effect TFT. Contact windows were etched with the combined RIE and wet processes in order to achieve a high selectivity and minimum undercuts. The above process is fully compatible with conventional TFT process, and does not need sophisticated processes such as lifting-off.

An Agilent 4155C semiconductor parameter analyzer and a 4140B pico-ampere meter were used to characterize the diodes and B-TFTs. Electron Spectroscopy for Chemical Analysis (ESCA) was used to analyze the PECVD films. The film thickness was determined by deposition rate and time.

RESULTS AND DISCUSSION

Junction behaviors of a-Si:H diodes Figure 3 shows junction behaviors of various diodes. As the i-layer became thinner, both the forward-biased current and the leakage current increased. The forward-biased behavior degraded with the increase of the i-layer thickness. The stacked p^+/i/n^+ diode was also investigated and showed better

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characteristics than the above $n^+/i/p/p^+$ diode. In addition, after annealing at 240°C in the air for 1 hour, the diode leakage currents decreased slightly. This indicated that the RIE-induced device defects could be repaired like the FET-type a-Si:H TFT [4].

Figure 4 presents J-V curves of diodes, which had a similar structure of the B-C or B-E junction in the B-TFT. Each curve followed the $J \propto e^{qV/nkT}$ relationship for V = 0.2~0.5 V. This equation was originally derived for a single crystal silicon device [5]. Compared to the two straight lines of $e^{qV/kT}$ and $e^{qV/2kT}$, the n value of the a-Si:H diodes decreased from 2 to 1 as the i-layer thickness decreased from 200 nm to 20 nm. The $e^{qV/kT}$ relationship is attributed to electron diffusion through the internal barrier. The $e^{qV/2kT}$ relationship can be explained by the recombination of injected carriers in the depletion region [6,7]. Therefore, when the i-layer is thick, the depletion region extends to such a wide range that most of the injected carriers are diminished by recombination. To optimize the B-E junction of a B-TFT, the i-layer should be as thin as possible while still thick enough to prevent current tunneling or punching through [8].

Junction behaviors of a-Si:H B-TFTs Although authors observed good B-C junctions in some B-TFTs [9], they also detected poor performance junctions in some transistors. Figure 5 shows that the B-C characteristics of an a-Si:H B-TFT, which has worse junction behavior than that of the individual diode in Fig. 4. The magnitude difference between the forward-biased current and reverse-biased leakage current through the B-C junction is much smaller than that of the individual diode, which can decrease the current gain of the B-TFT. The inferior base contact properties could be the cause. In the individual diode fabrication case, all a-Si:H layers were deposited in one pump-down. There was no contamination at the interface between the p and p^+ layers. However, in the B-TFT fabrication process, there was an air-exposure step before the p^+ layer deposition, which deteriorated the interface quality although the sample was dipped in a dilute HF solution before the p^+ layer deposition.

Figure 5 also shows that the B-E junction behavior of the B-TFT is worse than that of an individually prepared diode. The forward-biased current density of the former is lowered than that of the latter by three orders of magnitude. In addition, the leakage current in Fig. 5 is lower than the forward biased current by one three orders of magnitude while that in Fig. 4 is larger than five orders of magnitude. In an individually prepared diode, the direction of the current flow between the two electrodes is vertical to the junction interface. In the B-TFT, the emitter-to-base current flows parallel to the junction interface, i.e., in a lateral direction. Therefore, the resistance between the two electrodes is very large. In this paper, the designed distance between the base contact and emitter contact was larger than 12 micrometers. For a vertical junction structure, the distance between the two electrodes is much less than 1 micron.

As shown above, the p-n junction characteristics of the B-TFTs were worse than those of the individually prepared diodes. The poor interface formed in the B-TFT fabrication process might result in a poor interior p-i quality, which could make the p-i interface a current limiting factor for the device [6]. The curves, especially J_{BE}, contain serious noise in the range of V = -0.4~0.2 V. This is consistent with the noise detected in the output characteristics, i.e., I_C-V_{CE}, of the B-TFT. Figure 5 also shows the $J \propto e^{qV/2kT}$ relationship in the region of V = 0.2~0.4 V. The air-exposed p-i interface might have a rather high defect density, which could not be eliminated by the HF dipping procedure.

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Therefore, to develop an effective method to preserve the high quality interface is imperative for the improvement of the performance of B-TFT.

Output characteristics of B-TFT Figure 6 shows the common-emitter output characteristics of an a-Si:H B-TFT, i.e., I_C vs. V_{CE}. The current began to saturate at V_{CE} ~ 3 V, which was not shown in the previous report [2]. This B-TFT has a high I_C of 52 μA at V_{CE} = 4 V while the ref. 2 transistor has a lower I_C of around 10 μA [2]. Therefore, the B-TFT in this paper has a better current driving capability than the ref. 2 transistor. The ac current gain at V_{CE} = 3.5 ~ 6 V is around 3~6, which is also higher than the literature report of 2~3 [2].

The large noise in Fig. 6 curves is probably contributed to the high defect density at the p-i and p-p^+ interfaces, especially the former that is the interface between the base and the emitter. A high "OFF" current, i.e., a few micro-amps measure at V_{CE} = 0 V, is also observed, which results in a low "ON/OFF" ratio. All curves also significant shift to the positive V_{CE} direction. Both phenomena could be attributed to the parasitic p-n diode formed between the base and collector outside of the emitter via region. The high lateral series resistance of the base layer is a major factor to degradation of the output characteristics.

CONCLUSIONS

The a-Si:H B-TFTs were successfully fabricated with conventional IC materials and processes. Compared with the result reported in the literature [3], the B-TFT is this paper showed a higher current driving capability and a larger current gain. The fabrication process is fully compatible with the conventional TFT technology. Although the feasibility of this kind of device has been demonstrated, there are some structure, process, and material issues that need to be resolved. Authors are investigating methods to improve the interface quality and to lower the lateral resistance of the base layer.

ACKNOWLEDGMENTS

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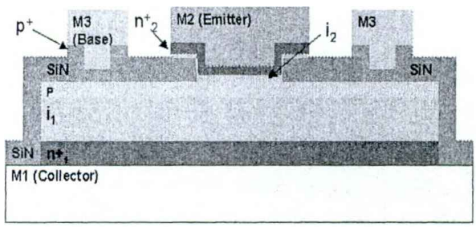


Fig. 1. Cross-section profile of a B-TFT.

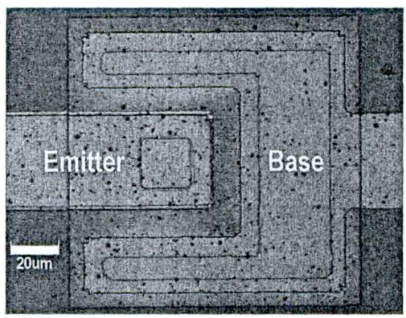


Fig. 2. Top view of a completed B-TFT device (Emitter 20×20 μm^2, Base 120×120 μm^2).

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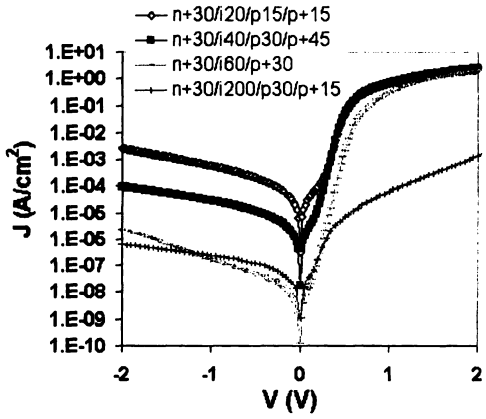


Fig. 3. Current density-voltage characteristics of a-Si:H diodes (thickness in nm unit).

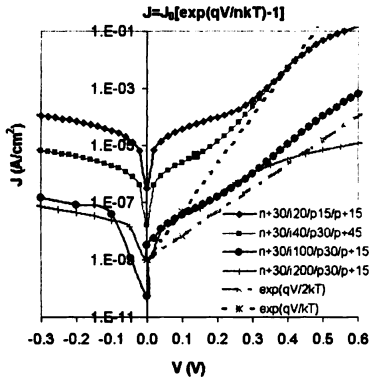


Fig. 4. Exponential region of diode J-V characteristics (the unit of thickness is nm).

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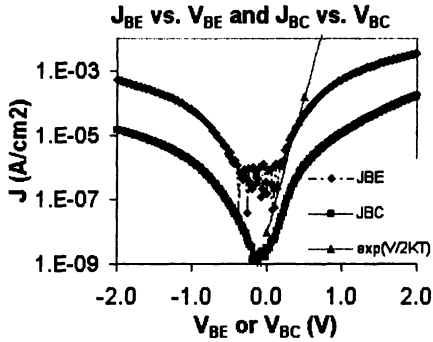


Fig. 5. BE and BC junction behaviors of a B-TFT.

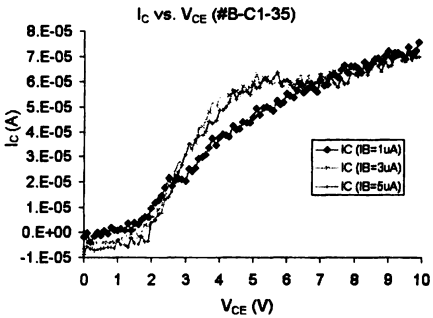


Fig. 6. Common-emitter output characteristics (I_C vs. V_{CE}) of a B-TFT device with emitter area of 20×20 μm^2. (The thickness of each film is 15nm / 20nm / 30nm / 60nm / 30nm in the order of n^+_2 / i_2 / p / i_1 / n^+_1 from Emitter to Base.)

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HIGHLY pH SENSITIVE SUSPENDED-GATE SILICON THIN FILM TRANSISTOR (ISTFT)

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ABSTRACT

This paper presents a new architecture of an Ion Sensitive Field Effect Transistor (ISFET). It is based on a suspended gate polysilicon thin film transistor, with the gate-bridge formed by a stack of three silicon nitride, polysilicon and silicon nitride layers deposited by Low Pressure Chemical Vapor Deposition (LPCVD). This new structure is called "Ion Sensitive Thin Film Transistor" (ISTFT). Very high sensitivity, greater than 200 mV/pH, is found by using this structure. It is much higher than the usual Nernstian sensitivity of ISFETs. It is due to the high field effect induced by the small distance between the gate and the channel of the transistor.

INTRODUCTION

Field Effect ion – sensitive structure is the well-known Bergveld's Ion Sensitive Field Effect Transistor (ISFET) [1] that is a gateless FET with a sensitive film covering the channel insulator and with a reference electrode diving in the solution and fixing the gate bias. The sensitivity of ISFET is explained from the shift of the threshold voltage induced by the variation of the flat-band voltage, V_{FB}, in presence of charges distributed in the solution, and more especially the H^+ ion concentration that governs the pH of the water solution. Particularly, the surface potential at the insulator-solution interface, which is included in the V_{FB} expression, linearly varies with the value of the pH solution. In this case, the maximum sensitivity, which is the Nernstian sensitivity, is 59 mV/pH at 20°C [2]. So, the sensitivity of all the present ISFET is lower than or close to this maximum.

In this usual ISFET structure, the reference electrode only fixes the potential of the solution, which is homogeneous with a homogeneous distribution of the H^+ ions.

Here, the air-gap TFT structure, for which we published previously the technological process [3] (Figure 1), is used with some improving modifications to measure the pH value in a solution. This new structure is called "Ion Sensitive Thin Film Transistor" (ISTFT). It is fabricated using surface micro machining technology

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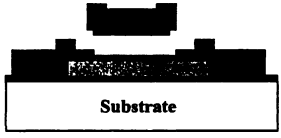


Figure 1: Air-gap structure [3]

EXPERIMENTAL

Materials

Silicon thin films used in the electronic as well as mechanical parts of air-gap TFTs are amorphously deposited at a temperature of 550°C and a pressure of 90 Pa using a hot wall Low Pressure Chemical Vapor Deposition (LPCVD) reactor. Phosphorous or boron *in situ* doped silicon films are deposited with same conditions using a mixture of silane, and phosphine or diborane as doping gas. Doped as well as undoped layers are solid phase crystallized in the deposition reactor only by increasing the furnace temperature still 600°C,without breaking the vacuum.

Polycrystalline germanium films deposited by LPCVD in another similar reactor are used as sacrificial layer. Thanks to its great etch selectivity against silicon oxide, silicon nitride, polysilicon. due to the unstable germanium oxide, the etch rate is very high in H_2O_2 (1,2 µm/min) at low temperature 90°C [4]

Silicon oxide that is used as first gate insulator is deposited in a Atmospheric Pressure CVD (APCVD) at 400°C using a mixture of silane and oxygen.

Silicon Nitride is used as passivation layer. It is deposited also by LPCVD technique at 600 °C, 400 µbar, and NH_3/SiH_4 flow ratio of 1 [5].

Aluminum is deposited in a Joule effect system.

Micro-bridge

The gate of the p-type air-gap TFTs is a highly boron doped polycrystalline silicon bridge. Boron doped polysilicon has a high positive mechanical stress. Then it is hard to succeed in the fabrication of boron doped polysilicon bridge usually. Here, the boron doped polysilicon film is embedded between two silicon nitride layers that ensure the mechanical maintain of the bridge thanks to the negative stress of Si_3N_4 layers. In the same time, silicon nitride layers insure the electrical passivation of the bridge.

Five hundred nanometers thick poly-Ge, to be used as sacrificial layer, is deposited on 2 inches single-crystalline silicon wafer. Ge sacrificial layer is then patterned using standard photolithography techniques. The anchor windows of the bridge were opened on germanium by plasma etching using SF_6 reactive gas. Then, the structural film is formed by a stack of three layers of silicon nitride, boron doped polysilicon and silicon nitride, successively deposited. Fig. 2: shows an example of these free standing micro bridges.

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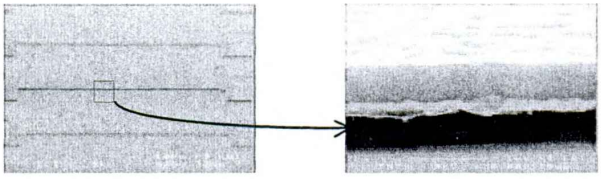


Figure 2: SEM image of a micro bridge and a zoomed-in view of the central zone.

ISTFT process

Eight masks were designed for the fabrication of this new structure. The fabrication process is summarized as follows. First, the substrate is covered with 500nm thick silicon nitride that acts as diffusion and contamination barrier. Then 350 nm thick single layer of silicon is deposited. The first 200 nm of this layer is deposited undoped by using only pure silane gas and successively without breaking the vacuum, just by switching on the diborane opening valve, the last p-type doped 150 nm are deposited. This structure is *in situ* crystallized at 600°C. The doped up-layer is plasma etched to define source and drain regions. Then 70 nm thick silicon dioxide and 45 nm thick silicon nitride films are successively deposited in order to passivate the channel. There after, 500 nm thick germanium sacrificial layer is deposited and patterned to form the regions of the drain and source contacts and the bridge anchors. Next, 45 nm thick silicon nitride film is deposited. This layer and the previous silicon dioxide / silicon nitride stack of layers are patterned simultaneously to open the drain and source windows. Then, 500 nm thick boron doped polysilicon and 45 nm thick silicon nitride films are successively deposited and patterned to form the gate (bridge). Afterwards, 500 nm thick aluminum film is deposited and patterned to form the source, drain, and gate pads. The contacts wires are insulated using a resine. Then the sacrificial germanium layer is easily etched using H_2O_2 only. A scheme of the cross-section of the final ISTFT structure is shown in figure 3. Figure 4 is a Scanning Electron Microscope up-view of the structure.

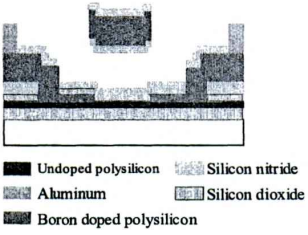


Figure 3 : cross-section of the final ISTFT structure

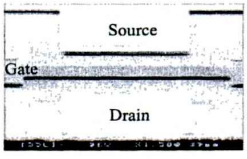


Figure 4 : Scanning Electron Microscope up-view of the structure

Electrical testing in pH buffer solutions

The same procedure to check the sensitivity of the ISTFT characteristics to the solution pH is used in all our experiments. The ISTFT is dived into a buffer solution for which the pH was fixed before between 3 and 10. Then, the transfer characteristics

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drain-source current I_{DS} versus the gate voltage V_{GS} is measured using a HP4155A semiconductor parameter analyzer. The drain-source voltage V_{DS} is kept constant at -2 V during this measurement. The ISTFT under testing is rinsed using de-ionized water between 2 measurements in buffer solution with different pH value.

RESULTS

In the present paper, the pH sensitivity is defined as the gate voltage variation per pH unit when the drain-source current I_{DS} is fixed to -100 µA. Figure 5 shows the transfer characteristics I_{DS}-V_{GS} of the same ISTFT dived in buffer solution with different pH values at ambient temperature. The threshold voltage decreases for higher pH values. In the same time, the drain current at fixed V_{GS}, increases.

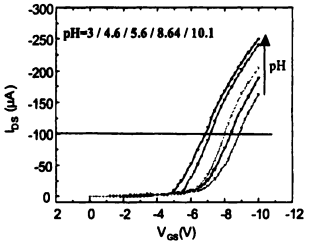


Figure 5 : Transfer characteristics of the same ISTFT dived into solution with different increasing pH values at ambient temperature. At fixed V_{GS}, the drain current increases with the pH value.

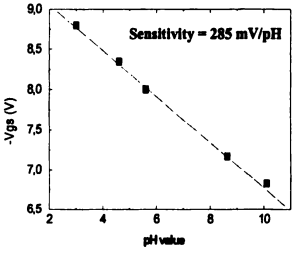


Figure 6 : Plot of the V_{GS} values versus pH when the drain-source current is fixed to −100 µA at ambient temperature. The sensitivity of the present ISTFT is the slope of the straight line.

To check the sensitivity, the V_{GS} value at I_{DS}= −100 µA is plotted as a function of the pH in figure 6. The variation of V_{GS} with pH is perfectly linear. The slope of the straight line gives a sensitivity of 285 mV/pH. This sensitivity is 5 times higher than the usual value given by the commercially available ISFET. It is due to the low height of the gap under the gate-bridge. The H^+ concentration becomes non-uniform due to the high field effect present in the gap. The solution close to the nitride surface seems to be characterized by a higher pH value. Then the V_{GS} variation is large. The effect of the low height gap is highlighted by the lower sensitivity obtained when the gap is larger.

CONCLUSION

New architecture of an ISFET was presented in this contribution. It is based on polysilicon thin film technology that becomes mature now. The new structure is called Ion Sensitive Thin Film Transistor (ISTFT). The pH sensitivity of this ISTFT is 285 mV/pH that exceeds five times the Nernstian limit.

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HIGH DYNAMIC RANGE PIXEL AMPLIFIER ARCHITECTURE IN AMORPHOUS SILICON TECHNOLOGY FOR DIAGNOSTIC X-RAY IMAGING APPLICATIONS

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On-pixel amplifiers offer an approach to increase the pixel signal-to-noise ratio (SNR) in low-exposure, real-time digital fluoroscopy using amorphous silicon (a-Si) technology. Experiments reveal a reduction in readout noise and indicate that the a-Si pixel amplifiers can meet the stringent requirements for digital X-ray fluoroscopy. However, larger input voltages cause the output of these pixel amplifiers to become non-linear thus reducing the pixel dynamic range. In this research, we investigate a hybrid amplified pixel that exhibits large signal linearity and consequently higher dynamic range. Gain, linearity, noise, and metastability simulations along with area estimations for the hybrid pixel pixel indicate its applicability towards large-area medical X-ray imaging applications that require switching between low-exposure, real-time fluoroscopy and high-exposure chest radiography modes at a region of interest.

INTRODUCTION

Digital imagers based on amorphous silicon (a-Si) technology are increasingly being used for large-area medical imaging (Figure 1) (1), because they offer the benefits of uniform deposition, low capital cost, and tolerance to X-ray radiation. While image intensifier based fluoroscopy offers real-time imaging (2), flat panel detectors based on amorphous silicon (a-Si) thin film transistor (TFT) technology are becoming more prevalent due to their many advantages such as tele-diagnosis, immediate viewing of the radiograph, convenient computer storage, and portability due to compactness of the imager. Fluoroscopy is a real-time X-ray image of the patient body and is used in many types of examinations and procedures, such as barium X-rays, cardiac catheterization, and placement of intravenous catheters that require the insertion of hollow tubes into veins or arteries. In digital fluoroscopy, a catheter is guided through an artery while the patient is continuously exposed to radiation which necessitates low doses and consequently, reduces the X-ray input signal to the imaging electronics.

Using industry standard, a-Si switch based pixels (2), the signal-to-noise ratio (SNR) at the low fluoroscopic exposure levels can result in blurred images. In contrast, current-mediated a-Si pixel amplifiers have been reported (3,4) to give an improved SNR for real-time low dose imaging. However, for imaging modalities that require larger doses to the patient, and consequently result in large X-ray input signals, the pixel amplifier output becomes non-linear, thus limiting the upper end of the pixel dynamic range. An application that has generated considerable interest recently is a digital X-ray imaging flat

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panel that can be configured to dynamically switch between fluoroscopic and radiographic acquisition modes (2). To enable such a dual mode X-ray imager, we investigate an a-Si hybrid amplified pixel architecture that exhibits large signal linearity and thus, can perform higher dynamic range X-ray imaging.

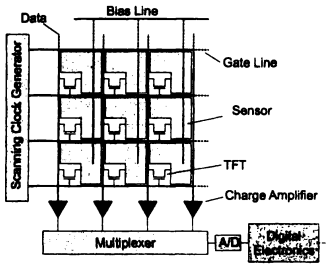


Figure 1. Amorphous silicon active matrix flat panel imager (AMFPI)

X-RAY IMAGING REQUIREMENTS

The pixel, forming the fundamental unit of the active matrix, consists of a detector and a readout circuit, whose configuration in practice differs with the detection scheme. Two schemes (5) are prevalent in literature: the first is direct-detection which uses an X-ray photoconductor as the detector (for example, amorphous selenium (a-Se)) and the second is an indirect detection scheme, which employs a CsI phosphor coupled with an a-Si:H p-i-n photodiode sensor. Regardless of the detection scheme, the detector needs to be coupled to an appropriate on-pixel readout circuit to efficiently transfer the collected electrons to external off-panel electronics for data processing. The requirements on X-ray spectrum and exposure for a direct detection imager using a-Se are shown in Table I for diagnostic fluoroscopy and chest radiography, where the primary differences between the two modalities lie in the real-time nature of fluoroscopy and that different amounts of charge collected per pixel area.

Table I. Requirements on a digital, diagnostic X-ray flat panel imager (6)

	Chest Radiography	Fluoroscopy
Imager size (cm)	35 x 43	25 x 25
Pixel area (μm^2)	200 x 200	250 x 250
Pixel count	1750 x 2150	1000 x 1000
Image readout time (s)	< 5	0.033/frame
X-ray spectrum (kVp)	120	80
Exposure range (mR)	0.03 – 3	0.0001 – 0.01
X-ray fluence (photons/mm^2/mR)	2.30×10^5	1.98×10^5
Image charge per pixel (in pC)	0.016 – 1.6	0.00016 – 0.008

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As evident, more than two orders of magnitude of charge can accumulate on a pixel during a chest radiography exposure as compared to during fluoroscopic mode. In the following sections, we will discuss the dynamic range limitations of the industry standard, switch based, amorphous silicon passive pixel sensor (PPS) and the recently reported active pixel sensor (APS) architecture. Then, as a potential solution to achieve a higher pixel dynamic range, we will introduce the hybrid APS pixel architecture.

PIXEL ARCHITECTURES

Passive Pixel Sensor (PPS)

The PPS is the workhorse of the imaging industry and consists of a sensor element (e.g. p-i-n photodiode) and an integrated readout TFT. A sample array of a-Si imaging PPS pixels is illustrated in Figure 1. A gate driver sequentially addresses every row in the array. Pixel outputs are connected to charge amplifiers and the columns are read out in parallel when a row of TFTs is enabled. The amplifier outputs are then multiplexed to an analog-to-digital (A/D) converter, which sends the digital output to a computer for image signal processing. There are three modes of operation for the PPS in Figure 2:

- Integration Mode: Signal charge accumulates on C_{PIX} (sum of sensor and parasitic capacitances at node V_G) proportional to the amount of X-ray radiation.
- Readout/Reset Mode: Following integration, the READ TFT is turned ON thereby transferring the signal charge accumulated on C_{PIX} during integration to the feedback capacitance, C_{FB}, of the column charge amplifier. The readout step has the effect of simultaneously causing pixel reset since the charge transfer is a destructive process. Also, since readout is essentially a charge transfer process, the gain of the PPS is limited to being ≤ 1 and the operation is inherently linear.

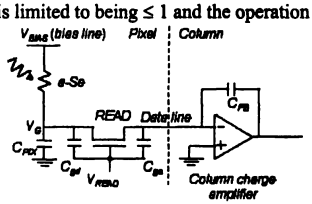


Figure 2. Schematic of a PPS using an a-Se photodetector. C_{gs} and C_{gd} are the parasitic gate-source capacitances of the READ TFT switch.

While the PPS architecture has the advantage of being compact and amenable to high-resolution imaging, previous studies (5) have shown that external column charge amplifiers in the PPS array add a large electronic noise component to the pixel (~ 1500 electrons referred to the detector input). The PPS electronic noise component presents a challenge to the development of a fluoroscopic X-ray imager which would ideally, be only X-ray quantum noise limited. For commercialized indirect and direct X-ray detectors such as CsI coupled to a-Si p-i-n photodiodes or a-Se, the quantum noise limit

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requirement for fluoroscopy requires the input referred electronic noise to be less than 1000 electrons.

Current-mediated Active Pixel Sensor (C-APS)

To achieve quantum noise limited X-ray imagers for fluoroscopy, signal amplification can be incorporated at either the X-ray detector or at the pixel readout circuit. The former alternative requires the use of high gain X-ray detectors such as HgI_2, PbO or CdZnTe, all of which are still in their experimental stages (2). The second alternative of using a-Si on-pixel amplifiers to improve the fluoroscopic SNR is promising (3,7) because it does not require a departure from either the well-established X-ray detector technologies or the mature a-Si thin film transistor (TFT) technology.

An amplifed pixel architecture reported for fluoroscopy is the current-mediated active pixel sensor (C-APS) that is derived from highly popular APS image sensor research in crystalline silicon CMOS technology (8). Central to the C-APS illustrated in Figure 3 is a source follower circuit which produces a current output to drive an external charge integrating amplifier. Here, the readout of the APS array is column parallel, i.e. one charge amplifier is provided per column so that an entire row is read out simultaneously. The C-APS operates in three modes (7):

- Reset mode: The RESET TFT switch is pulsed ON and the pixel capacitance, C_{PIX} charges up to Q_P through the TFT's on resistance. C_{PIX} is usually defined by an on-pixel storage capacitor since the a-Se photoconductor capacitance is very small (due to thick layers for good X-ray absorption at diagnostic X-ray energies).
- Integration mode: After reset, the RESET and READ TFT switches are turned OFF. During the integration, T_{INT}, the input signal, $h\nu$, generates photo-carriers discharging C_{PIX} by ΔQ_P and decreases the potential on C_{PIX} by a small signal voltage, ΔV_G.
- Readout mode: After integration, the READ TFT switch is turned ON for a sampling time T_S, which connects the APS pixel to the charge amplifier and an output voltage, V_{OUT}, is developed across C_{FB} proportional to T_S.

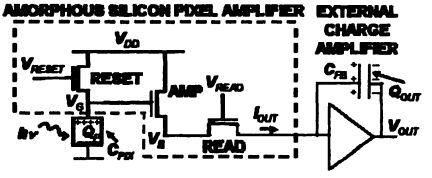


Figure 3. Current mode active pixel schematic (7)

Current-mediated a-Si pixel amplifiers have been reported to give a good SNR for fluoroscopy at low X-ray inputs (3,4). However, since the drain current of the AMP TFT (denoted as I_{OUT} in Figure 3) has a quadratic relationship with the voltage at the gate of the AMP TFT (i.e. V_G), the charge amplifier output, V_{OUT}, changes non-linearly with changes in V_G. This nature of the quadratic relationship can be determined by examining

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the behavior of ΔI_{OUT} with respect to ΔV_G. Here, we note that the AMP TFT is operating in the saturation region while the READ TFT is in the linear operation region during pixel readout. Taking into account the non-idealities of a-Si, where $(W/L)_{AMP}$ is the aspect ratio of the AMP TFT, μ is the electron band mobility, C_I is the insulator capacitance per area, K_t is a temperature constant, x_S is the channel length modulation, and V_{T0} is the threshold voltage, the I_{DS}-V_{DS} relationship of AMP TFT is given as (9),

$$(I_{DS})_{AMP} = (W/L)_{AMP}\mu C_I (V_G - V_B - (V_{T0})_{AMP})^{2/K_t} x_S \quad , \qquad [1]$$

$$\text{where } x_S = [1 - {}^{V_{DS}}\!/_{\lambda}]^{-1} V_{DS}^{(2-2/K_t)}/2 \text{, and } K_{AMP} = \left({}^{W}\!/_{L}\right)_{AMP} \mu C_I x_S . \qquad [2]$$

Based on a nominal channel temperature of T = 300°C and setting $(I_{DS})_{AMP}$ to I_{OUT}, equation [1] can be simplified as (9),

$$I_{OUT} = K_{AMP}(V_G - (R_{ON})_{READ} I_{OUT} - (V_{T0})_{AMP})^2 \qquad [3]$$

To determine the impact of the pixel's quadratic transfer function on the C-APS gain, we examine the charge gain, G_i, relationship which is defined as the ratio of the charge collected on the external amplifier feedback capacitor and the charge collected on C_{PIX} during to the X-ray input signal. Thus,

$$G_i = |\Delta Q_{OUT}/\Delta Q_P| = (\Delta I_{OUT}.T_S)/\Delta V_G C_{PIX} = g_m T_S / C_{PIX} , \qquad [4]$$

$$\text{where, } \frac{\Delta I_{out}}{\Delta V_G} = g_m . \qquad [5]$$

Rearranging I_{OUT} in equation [3],

$$I_{OUT} = \frac{1 + 2(R_{ON})_{READ} K_{AMP}(V_G - (V_{T0})_{AMP}) - \sqrt{1 + 4(R_{ON})_{READ} K_{AMP}(V_G - (V_{T0})_{AMP}}}{2(R_{ON})_{READ}^2 K_{AMP}} \qquad [6]$$

the transconductance, g_m, of the AMP and READ TFT circuit is found to be,

$$g_m = \frac{dI_{OUT}}{dV_G} = \frac{1}{(R_{ON})_{READ}}\left[1 - \frac{1}{\sqrt{1 + 4(R_{ON})_{READ} K_{AMP}(V_G - (V_{T0})_{AMP})}}\right] \qquad [7]$$

where $(R_{ON})_{READ}$ is the ON resistance of the READ TFT,

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$$(R_{ON})_{READ} = \frac{1}{\mu C_I (W/L)_{READ}(V_{READ}(V_{t0})_{READ})} \quad [8]$$

In order to extract g_m as a function of V_G only, the voltage at the node common to the READ and AMP TFT, V_B, is determined using $V_B = (R_{ON})_{READ} I_{OUT}$, equation [6] and equation [8] which yields,

$$V_B = \frac{1}{2}\left[\frac{\left[K_{READ}(V_{READ} - (V_{T0})_{READ}) + 2K_{AMP}(V_G - (V_{T0})_{AMP}) - \left[\left(4K_{AMP}K_{READ}(V_{T0})_{AMP}((V_{T0})_{READ} - V_{READ}) + 4K_{AMP}V_G K_{READ}(V_{READ} - (V_{T0})_{READ})\right) + K_{READ}^2(V_{READ}^2 + (V_{T0})_{READ}^2) - 2K_{READ}^2 V_{READ}(V_{T0})_{READ}\right]^{1/2}\right]}{(K_{AMP})}\right] \quad [9]$$

Figure 4a shows the quadratic relationship of I_{OUT} with increasing V_G while Figure 4b shows the correspondingly decrease in g_m for increasing V_G. Note that the change in g_m is linear for small changes in V_G only.

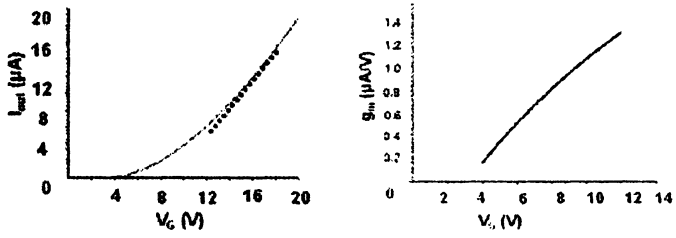


Figure 4. (a) I_{OUT} versus V_G, and (b) g_m versus V_G for the C-APS pixel circuit. Here, $V_{DD} = V_G$, $V_{READ} = 20$V, $(V_{T0})_{AMP} = (V_{T0})_{READ} = 3.2$V, $C_I = 250$ μF/m^2, $\mu = 0.8$ cm^2/V.s, $(W/L)_{AMP} = 280/30$, $(W/L)_{READ} = 200/10$, $x_S = 450$, $C_{FB} = 10$ pF, and $C_{PIX} = 1$ pF.

Figure 5 illustrates the linearity of G_i with increasing input X-ray signal charge ΔQ_P. based on circuit simulations for $C_{PIX} = 1$pF, $C_{FB} = 10$pF. For the quantities listed in Table I, ΔQ_P ranges from 0.00016 to 0.008 pC for the fluoroscopic input signal which is well within the linear region of operation where $G_i = 27$ is a constant value. However, for chest radiography X-ray inputs where ΔQ_P ranges from 0.016 to 1.6 pC, the large signal performance of the C-APS pixel amplifier becomes important as G_i will range from 27 at lower X-ray input signals to about 13 for larger X-ray inputs.

There are a couple of alternatives to overcome the inherent non-linearity in the C-APS readout circuit at higher X-ray input levels. The primary consequence of a non-linear pixel transfer function is that standard correlated double sampling mechanisms cannot be implemented in hardware as is typically done with active matrix imaging arrays. Double sampling (10) is required to correct for the effect of process non-uniformities (in the form of offsets) and in the case of a-Si technology, transistor instability (11) on pixel circuit performance.

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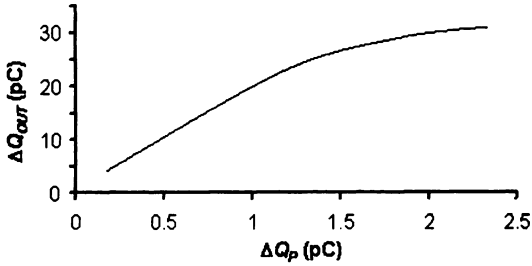


Figure 5. Simulation results for the linearity of the C-APS charge gain, G_l. Here, the circuit in Figure 3 was simulated using $V_{DD} = V_G$, $V_{READ} = 20V$, $(V_{T0})_{AMP} = (V_{T0})_{READ} = 3.2V$, $C_l = 250\mu F/m^2$, $\mu = 0.8cm^2/V.s$, $(W/L)_{AMP} = 280/30$, $(W/L)_{READ} = 200/10$, $x_S = 450$, $C_{FB} = 10pF$, and $C_{PIX} = 1pF$. The TFT model was implemented in Verilog-A and was based on the static and dynamic behavior reported in (9).

A possible solution to the non-linearity issue is to implement a frame memory in software to store each C-APS pixel's transfer characteristic curve so that the x-ray input could be extracted by interpolation. This is not however, an attractive option because longer frame times are required to process the imager output than if the basic non-uniformity correction was primarily implemented in hardware. In addition, the instability of a-Si transistors in the C-APS pixel will cause the pixel transfer characteristics to shift (11). Unstable pixel transfer characteristics would require repeated characterization of the pixel transfer functions at regular intervals which would further slow down the imager readout making it challenging to switch instantaneously from fluoroscopic to radiographic mode. X-ray imagers targeting chest radiography can have up to 4 million pixels per imager which would make rapid readout times with a software frame memory challenging. In the following section, we present a hybrid pixel architecture based on the PPS and C-APS architectures that offers a pixel-level solution to achieve a high dynamic range imager.

HIGH DYNAMIC RANGE PIXEL ARCHITECTURE

Hybrid Active Pixel Sensor (H-APS)

An alternative to achieving large signal linearity, amplification, and real-time readout simultaneously is to use a combination of PPS and C-APS circuits. Combining the PPS architecture for radiographic mode with the C-APS for low-noise fluoroscopy can give a high dynamic range flat panel imager. A circuit schematic of a hybrid active pixel sensor (H-APS) architecture is shown in Figure 6. Here, the RDC transistor is operated while the RDP TFT (i.e. the PPS switch) is kept OFF during fluoroscopic mode, and the circuit would essentially behave as the C-APS circuit shown in Figure 3. For C-APS operation, the pixels send their outputs out on column (**n**). For radiographic operation, the RDP pixel transistor is operated while the RDC and RESET transistors are OFF and the circuit operates as a PPS sending its output on column (**n-1**) shown in Figure 2.

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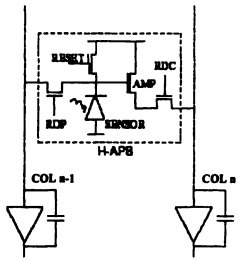


Figure 6. Hybrid APS (H-APS) pixel schematic (1)

Linearity and Gain

Since the H-APS contains both the C-APS and PPS architectures, the pixel will yield a linear output for both fluoroscopy and chest radiography level signals as long as the appropriate mode is chosen. However, there is a difference between the G_i for the C-APS and H-APS pixel due to the C_{gs} parasitic capacitance (and hence a larger C_{PIX}) and the additional line capacitance due to the metal line overlap added by the extra RDP TFT. Based on equation [4], increasing C_{PIX} will reduce G_i, while reset noise, the largest noise component in the C-APS circuit, becomes larger with increasing pixel capacitance (3). However, the increase in C_{PIX} due to RDP TFT can be minimized by appropriate choice of the RDP TFT aspect ratio, and layout. For example, using a $(W/L)_{RDP}$ = 50/10 is adequate to achieve a PPS readout time of < 3 μs for a C_{PIX} = 1 pF, V_{READ} = 20 V, $(V_{T0})_{RDP}$ = 3.2 V, C_i = 250 μF/m^2, and μ = 0.8 cm^2/V.s. The additional parasitic capacitance due to the RDP TFT with $(W/L)_{RDP}$ = 50/10 is about 20 fF, the impact of which is discussed in the following sections.

Transient behavior

Charge injection and feed-through from the additional RDP TFT can affect the steady-state voltage at the signal integration node for the H-APS pixel. When transistors turn OFF, charge injection occurs by two mechanisms. The first is due to the channel charge, which must flow out from the channel region of the transistor to the drain and source regions. It can be estimated using (12),

$$\Delta V_G = (1/2)\frac{(V_{ON} - V_T)C_{OX}WL}{C_{PIX}} \qquad [10]$$

The second error which is typically smaller than the feedthrough error, is due to the overlap capacitances between the gate and the source/drain junction and can be ignored unless the gate voltage is very small or TFT dimensions are small. This error can be estimated as (12),

$$\Delta V_G = \frac{(C_{gs})}{(C_{gs}) + C_{PIX}}(V_{ON} - V_{OFF}) \qquad [11]$$

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The feedthrough and charge injection errors are only significant when the RESET TFT turns OFF (since the error voltage will determine the V_G on the AMP TFT during the next readout cycle) and when the RDP TFT turns ON (since the error voltage is now included in the PPS readout). The transient error voltages are summarized in Table II and it should be noted that since these voltages are deterministic and repeatable, standard doubling sampling mechanisms (10) can mitigate their effect.

Table II. Transient voltages at V_G. Here, $(W/L)_{RESET} = (W/L)_{RDP} = 50/10$, $(W/L)_{AMP} = 280/30$, $(W/L)_{RDC} = 200/10$. $V_{RESET} = 20$ V, $V_T = 3.2$ V, $(C_{OL})_{RESET} = (C_{OL})_{RDP} = 0.02$ pF, $(C_{OL})_{AMP} = 0.1$ pF, $(C_{OL})_{RDC} = 0.08$ pF, $C_I = 250$ μF/m^2, $C_{PIX} = 1$ pF.

Type of Error	Value
Feedthrough error when RESET TFT turns OFF	1.05V
Overlap error for RESET TFT turn OFF	0.38V
Overlap error at V_G (When RDP turns ON)	0.38V

Metastability

There are four TFTs in the H-APS pixel (RDP, RESET, AMP, and RDC) that are affected by the bias-induced shift in TFT threshold voltage (11). In diagnostic medical imaging applications, a factor aiding the metastability concerns is the significantly reduced TFT duty cycle. For example, in a 1000 x 1000 pixel real-time fluoroscopic imager, the TFTs are clocked 33 μs every 33 ms (i.e. a duty cycle of 0.1%). Experiments on TFT V_T shift, ΔV_T, (13) and on the AMP and READ TFTs in the C-APS pixel (14) to extract the X-ray imager lifetime at various duty cycles yielded a model (14) that estimated a change in g_m (and thus G_i) of less than 2% over 10,000 hours of operation as shown in Figure 7 (3).

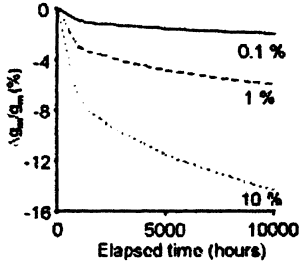


Figure 7. % change in the g_m of the C-APS readout circuit for different duty cycles (8)

The ΔV_T for the RESET and RDP TFTs affects pixel reset time (T_{RESET}) and the PPS pixel readout time, respectively, since both TFTs behave as switches. Typical voltages at the gate of these TFTs (with respect to the TFT drain and source) would range from $V_{GS} = -5$V or -10 V in the OFF state to minimize leakage and $V_{GS} = +15$ V in the ON state to minimize TFT ON resistance (R_{ON}) and hence reset or readout time. Consequently, ΔV_T

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would affect the switch ON-resistance thus affecting the reset/readout time. Based on models developed in (13), ΔV_T and reset times (T_{RESET}) for the RESET TFT are shown in Figure 8 (15) where it is seen that the V_T changes by a much larger amount than T_{RESET}. The main reason for the difference between ΔV_T and ΔT_{RESET} is that T_{RESET} is a function of R_{ON} (= $1/G_{ON}$) and its sensitivity to V_T depends on the applied V_{RESET} bias in the ON state. The normalized sensitivity of TFT on-conductance, G_{ON} with respect to V_T is,

$$\frac{dG_{ON}}{dV_T}\frac{V_T}{G_{ON}} = -\frac{V_T}{(V_{RESET} - V_T)}, \qquad [12]$$

where $G_{ON} = dI_{DS}/dV_{DS} = K_{RESET}(V_{GS} - V_T)$ for $V_{DS} \sim 0$. So if a large V_{RESET} (+15 V in the figure below) is chosen, the T_{RESET} becomes relatively insensitive to ΔV_T. A similar argument applied to the RDP TFT.

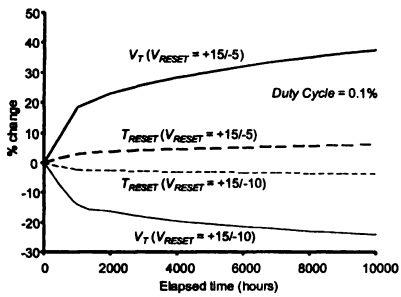


Figure 8. % change in V_T and reset time (T_{RESET}) over a 10,000 hour lifetime for TFTs. Here, two RESET pulses of magnitude +15/-5 and +15/-10 are applied at a pulse frequency of 30 Hz and a duty cycle of 0.1% ($V_{DS} \sim 0$ V).

Noise performance and pixel area considerations

Low frequency thermal and flicker noise for the READ and AMP TFTs, reset noise for the RESET TFT and the amplifier noise have been characterized in the past for the C-APS circuit (16). The RDP TFT causes low frequency thermal and flicker noise during PPS operation which is expected during the normal operation of a PPS pixel. Based on models developed for the different noise sources in the C-APS pixel (16), Table III lists the input referred noise equivalent electrons (NEQ) for the C-APS pixel and the H-APS pixel operating in C-APS mode.

The primary difference between the two pixel circuits is the additional parasitic capacitance added by the RDP TFT to C_{PIX} in the H-APS pixel and to C_{LINE}. Here, based on the TFT parameters listed in Table III, a nominal 20 fF gate-drain parasitic capacitance is estimated to add to C_{PIX}. Also, based on a 1750 x 2150 pixel chest radiography X-ray imager and a nominal metal overlap capacitance of 10 fF for a state-of-the-art a-Si TFT process, the increase in column line capacitance, C_{LINE}, is expected to be ~ 20 pF. As shown in Table III, the additional capacitance increases the reset noise,

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decreases the charge gain and due to the relationship of double sampling to uncorrelated random noise sources, increases the impact of the thermal and flicker noise components of the H-APS pixel. However, the net increase in noise is small and the H-APS pixel can be theoretically designed to give less than 1000 input referred noise electrons which is less than the quantum noise limit for digital fluoroscopy systems. To obtain the gain and noise performance shown in Table III, the various TFTs in the H-APS pixel are estimated to need a 170 x 170 μm pixel area using a state-of-the-art a-Si TFT process with a minimum dimension of 10 μm.

Table III. Input referred noise of the C-APS compared to the H-APS operating in C-APS mode. Here, $(W/L)_{RESET} = (W/L)_{RDP}$ = 50/10, $(W/L)_{AMP}$ = 280/30, $(W/L)_{RDC}$ = 200/10. V_{RESET} = 20 V, V_T = 3.2 V, $(C_{OL})_{RESET} = (C_{OL})_{RDP}$ = 0.02 pF, $(C_{OL})_{AMP}$ = 0.1 pF, $(C_{OL})_{RDC}$ = 0.08 pF, C_l = 250 μF/m^2, g_m = 0.89 (μA/V), μ = 0.8 cm^2/V.s, T_s = 30 μs and a nominal value of 1500 electrons is assumed for the external charge integrator noise.

	NEQ (electrons) C-APS (C_{PIX} = 0.98pF, C_{LINE} = 76pF)	**NEQ H-APS (C_{PIX} = 1.0pF, C_{LINE} = 96pF)**	**Difference (%)**
Charge Gain	27.2	26.7	1.8
Thermal	171	195	14.0
Flicker	698	751	7.6
Reset	562	568	1.1
Total Noise	913	962	5.3

CONCLUSION

A novel high dynamic range, amplified pixel architecture (H-APS) is presented that is capable of providing both, a charge gain to noise vulnerable input signals for improved SNR and large signal linearity with unity gain for larger input signals. Based on an amplified pixel architecture, the H-APS is suitable for integration with on-panel multiplexers, which can further reduce off-panel circuit complexity. The H-APS has one additional TFT in contrast to the previously reported C-APS amplified pixel. However, the H-APS circuit can be designed to yield a quantum noise limited fluoroscopic pixel array that can operate in real-time. The impact of the additional transistors on pixel area can be minimized if vertically stacked pixel architectures are used where the TFTs are embedded underneath the sensor. The H-APS pixel architecture presented in this paper is of particular relevance to the development of advanced X-ray imagers that can switch instantly between low exposure, fluoroscopic imaging and higher exposure radiographic imaging modes that will ultimately yield higher X-ray image quality as well as lower patient X-ray dosage and therefore better patient care.

ACKNOWLEDGEMENTS

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A NEW PIXEL CIRCUIT TO RECOVER THRESHOLD VOLTAGE SHIFT IN AMORPHOUS SILICON TFT FOR ACTIVE MATRIX OLEDS

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ABSTRACT

A new pixel circuit of a-Si:H thin film transistor (TFT) employing negative bias annealing for active matrix organic light emitting diode (AMOLED) is proposed. This circuit consists of two driving TFTs, two storage capacitors and two inverter blocks. The new driving scheme adopting negative bias annealing entitled polarity balanced driving (PBD) successfully suppresses the degradation of V_{TH} in a-Si:H TFT. The proposed pixel circuit was also verified by spice simulation with device parameters extracted from experimental data.

INTRODUCTION

Active matrix organic light emitting diode (AM-OLED) has potential to provide superior properties such as wide viewing angle, fast response time and simple process [1], [2]. Poly-Si thin film transistors (TFT) are mostly used for the AM-OLED display due to high field-effect mobility and stability. However, poly-Si TFT suffers from the inherent grain boundaries which cause the pixel to pixel non-uniformity of threshold voltage and mobility variation.

a-Si:H (Hydrogenated amorphous silicon) TFT used as a switching device in AM-LCD can be fabricated at low cost and with uniform material property [1]. In this reason, a-Si:H TFT has been employed as a current source as well as a switching transistor for AM-OLED applications. Nevertheless, a-Si:H TFT has a severe problem such as the degradation of threshold voltage due to the gate electrical bias. Since the luminance of OLED is dependent on the injected current provided by the driving TFT, the driving current must be accurately controlled. For this reason, several pixel designs have been proposed to compensate this degradation of a-Si:H TFT as well as non-uniform characteristics of poly-Si [2], [4]. These conventional schemes memorizing V_{TH} are not to reduce the degradation of a-Si:H TFT by electrical bias but to supply data voltage taken into account the shifted threshold voltage as storage capacitor memorizes the value of the threshold voltage of the degraded TFT before providing data [1], [2], [4], [5].

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In this paper, to minimize the shift of the threshold voltage caused the display deterioration, we propose a new pixel circuit employing a-Si:H TFT for AM-OLEDs. The new method applied pixel circuit can considerably reduce the degradation of threshold voltage.

EXPERIMENTS AND DISCUSSIONS

Background of Bias Annealing

The instability of a-Si:H TFTs has been investigated under the gate bias for a long time. It is well known that the threshold voltage in a-Si:H TFT increases with time under the electrical bias. This phenomenon of degradation is explained by two mechanisms. One of these is called the charge trapping in slow states in the silicon nitride (SiNx), and the other is the creation of defect states in the channel (a-Si:H) [6]. Powell reported that the charges are trapped by positive bias stress in silicon nitride may be emitted by following the negative bias and the defect states in the band gap are also reduced [6], [7], [8], [9].

Measurement System and Fabrication Process

As mentioned above, in order to examine to the effectiveness of negative bias, a series of experiments were conducted under both the direct current (DC) and the alternating current (AC) biasing conditions, using semiconductor parameter analyzer (HP4156B) and pulse generator unit. We have fabricated the testing TFT devices using the inverted staggered structure. The thickness of three layers on the gate metal, silicon nitride, a-Si:H and n+ a-Si:H layers are 450, 200 and 50nm, respectively. After masking the source/drain electrode, the n+ a-Si:H layer between the source and drain was etch-off by reactive ion etching (RIE). The passivating layer of silicon nitride (300nm thickness) was deposited over the undoped a-Si:H.

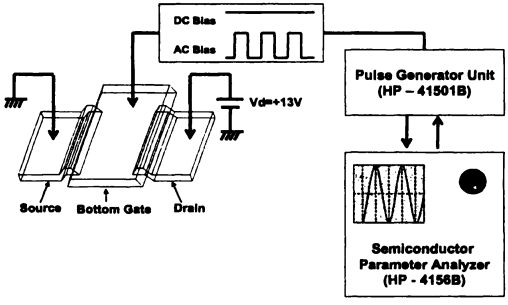


Figure 1. System of measurement and bias stress for a-Si:H TFT.

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I-V Characteristics of a-Si:H TFT before and after Bias stress

Fig. 2 and 3 show the transfer characteristics of the a-Si:H TFT. As the bias voltage was set to a voltage higher than the operation bias voltage for OLED, we conducted experiments under the accelerated conditions.

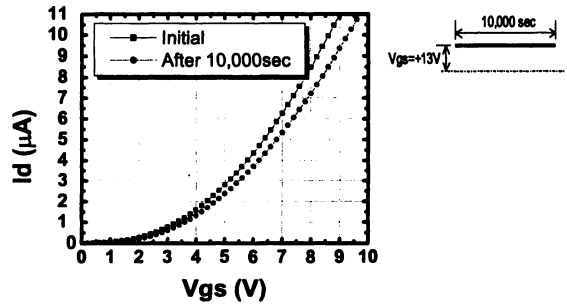


Figure 2. Measured data of transfer characteristics in a-Si:H TFT before and after DC bias stress. The stress conditions were as follows: V_{GS}=+13V, V_{DS}=+13V, stress time 10,000sec.

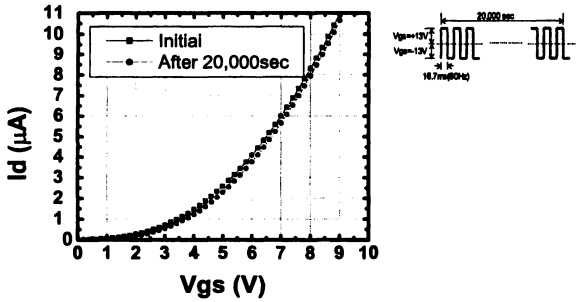


Figure 3. Measured data of transfer characteristics in a-Si:H TFT before and after DC bias stress. The stress conditions were as follows: V_{GS}=+13V or -13V with 50% duty, V_{DS}=+13V, stress time 20,000secs; effective positive stress time 10,000sec.

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When V_{GS} =+13V, V_{DS}=+13V and the stressed time is 10,000 seconds, the degradation of drain current and threshold voltage before and after DC biasing stress are shown in box symbol line and round symbol line of Fig. 2. The box symbol line denoting the transfer characteristic after the applied bias stress indicates that the DC biasing stress seriously reduced the drain current as the threshold voltage is positively shifted. On the other hand, we maintained equally effective positive stress time by setting the gate voltage to either +13V or -13V with 50% duty cycle for 20,000 seconds. The lines in Fig. 3 also show that the difference of drain current before and after PBD biasing stress is considerably less than that of DC biasing. When V_{GS} is 10V, the drain current of the driving TFT dropped from the initial value by 14.9% after the application of the DC biasing stress but by less than 5% after the PBD biasing. This result indicated that this new driving method considerably reduced the level of threshold voltage shifting before and after stress application.

PROPOSED NEW PIXEL CIRCUIT

Composition of proposed pixel circuit

Fig. 4(a) and (b) show the a-Si:H TFT pixel circuit and timing diagram of the proposed pixel circuit. The circuit suppresses threshold voltage fluctuation by adopting the method of negative bias annealing entitled PBD (Polarity Balanced Driving) [10].

This schematic circuit exhibits that driving TFTs, storage capacitors, and inverter block are in symmetrical structures. The main driving circuit consists of two driving transistors that alternately operate and two storage capacitor that maintain the renewed data voltage during one frame. Each inverter block is composed of four TFTs.

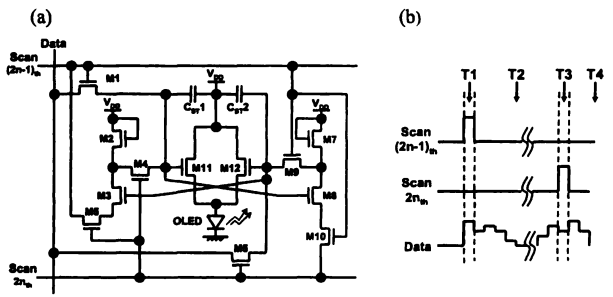


Figure 4. (a) Equivalent pixel circuit and (b) timing diagram for proposed new pixel circuit.

Operation of pixel circuit

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In the odd frame, when the scan $(2N-1)^{th}$ line is supplied with high scan signal, switching TFTs M1, M9 and M10 are turned on. As M1 is turned on, storage capacitor $C_{ST}1$ connected to the drain and gate of the driving TFT M11 is charged and this maintains positive data "$+V_{DATA}$" throughout one frame time. Simultaneously, As M10 is turned on, it activates the inverter block 2 and M9 will charge the storage capacitor $C_{ST}2$ in the opposite side with negative data "$-V_{DATA}$", as it is indicated by Fig. 5(a). As a result, $C_{ST}1$ and $C_{ST}2$ will be charged with "$+V_{DATA}$" and "$-V_{DATA}$", respectively. During the next time frame T2, when the scan signal is low, the charged $C_{ST}1$ and C_{ST} will supply "$+V_{DATA}$" and "$-V_{DATA}$" to driving TFT M11 and M12, respectively. Then M11 results in the emission of OLED, and M12 will result in annealing by the negative biasing during the time frame T2 as shown in Fig. 5(b).

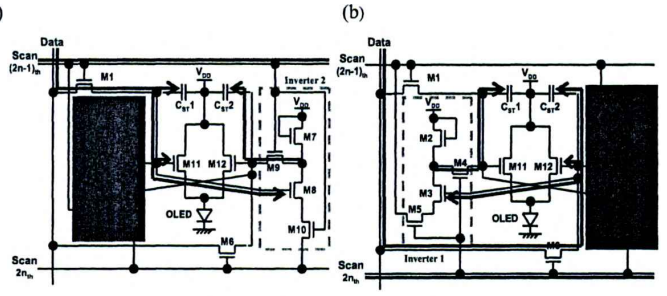


Figure 5. The T1 (a) and T2 (b) operation of proposed new pixel circuit

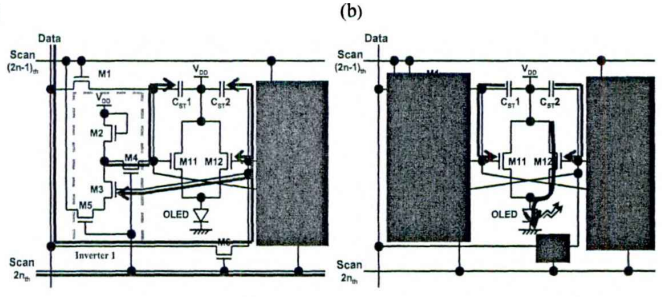


Figure 6. The T3 (a) and T4 (b) operation of proposed new pixel circuit

In the next frame $2N^{th}$ (meaning the even frame), this circuit may repeat odd frame operation, however, with reversed polarity of the charged voltage in storage capacitors $C_{ST}1$ and $C_{ST}2$. As shown in Fig. 6(a), the right hand side inverter block 2 is deactivated, and the other side inverter block is activated to provide negative bias voltage. At this time

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frame, $C_{ST}1$ and $C_{ST}2$ is individually charged negative and positive data, respectively. Thus as above explained from T2, $C_{ST}1$ charged negative data anneals the degradation of driving TFT M11 and $C_{ST}2$ charged positive data results in the emission of OLED. The new method may be summarized as follows: the driving TFT M11 (or M12), which has positively shifted threshold voltage during odd (or even) frame, is annealed by negative bias while OLED is emitted by driving TFT M12 (or M11) on the opposite side.

CIRCUIT SIMULATION

The pixel circuit was verified by circuit simulation with SmartSpice™. The simulation parameters were extracted from measurements of fabricated unit TFT device using inverted staggered structure (Fig. 7). Also the circuit was simulated with circuit parameters that were suitable for the AM-OLED display.

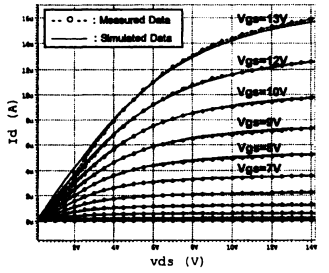


Figure 7. Measured data and simulation result using extracted parameters of a-Si:H TFT.

Detailed device parameters are as follows. Each of driving and switching TFT is W/L=200μm /5μm, W/L=20μm/5μm, W/L=20μm/10μm and 40μm/5μm, respectively. Storage capacitors are set to 0.3pF. Fig. 8(a) and (b) show the simulated results the gate voltage and source current of M11 connected storage capacitors. Throughout each frame, each of the storage capacitors C_{ST1} and C_{ST2}, which sustains the luminance of OLED display and anneals the driving TFT, maintains alternately positive and negative voltages This simulation result shows that the reversed polarity bias voltage applied to the stressed driving TFT during the frame.

(a) (b)

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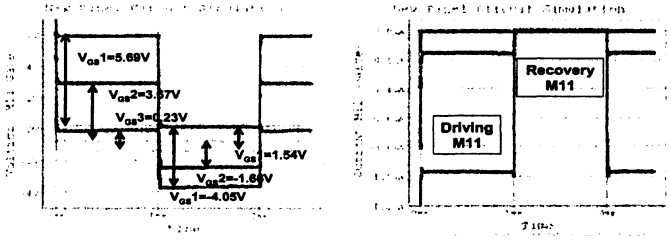


Figure 8. Simulated results of (a) gate voltage of M11 and (b) source current of M11.

CONCLUSION

We proposed a new a-Si:H TFT pixel circuit adopting negative bias annealing for OLED. The circuit consists of two driving TFTs four switching TFTs and storage capacitors. The negative bias annealing, which was determined through the experiments conducted under both DC and PBD biasing, was considerably effective to reduce the shift of threshold voltage. The circuit was also verified by simulation. AMOLED using this PBD method may contribute to the improvement of reliability.

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LOW-TEMPERATURE DEPOSITION OF POLY-Si AND SiGe THIN FILMS AT 450°C AND FABRICATION OF HIGH MOBILITY TFTS OVER 50 cm^2/Vs

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ABSTRACT

We have established a new thermal CVD technique, Reactive Thermal CVD, for polycrystalline silicon (poly-Si) and silicon germanium (poly-SiGe) thin films aiming at thin film transistors (TFTs) applications, in which a low substrate temperature of 450°C enables us to use glass substrates. This technique achieved high crystallinity at very early stage of the film growth, resulting in no amorphous incubation layer on the substrate surface. We fabricated n-and p-channel bottom gate TFTs with these of 200 nm thick films on SiO_2/Si wafers: the high field effect mobilities over 50 cm^2/Vs were achieved. Here, we discuss the general feature of the present CVD technique and its TFT applications.

INTRODUCTION

In these 10 years the amorphous silicon TFTs have been well established as an active matrix for liquid crystal display (LCD) devices for computer outputs, and more recently for TV monitors. Due to the increasing demand for large-area and high definition LCDs, the needs for the switching elements faster than amorphous silicon TFTs, whose switching speed is limited by its mobility of 0.1~1 cm^2/Vs, are coming out. In addition, the monolysic fabrication of TFT arrays and the system circuits including scanning and signal drivers is launched in small-size quality displays for mobile information devices in order not only to reduce their size but also to improve their reliability and yields and to reduce their production cost. Furthermore, new needs for high mobility TFTs has emerged to realized the back plane for organic light emitting displays, which request high current density for operation. Thus, there is an increasing demand for poly-Si TFTs whose mobility exceeds 100 cm^2/Vs.

Nowadays, the poly-Si thin films on the glass substrate for TFT applications are fabricated in two techniques, that is, excimer laser annealing and meta-induced solid phase crystallization of a-Si thin films. On the other hand, deposition of quality poly-Si thin films compatible with laser-annealed poly-Si thin films has not been achieved at low-temperatures where the glass substrate is available, in spite of a great interest in

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industrial applications. It could eliminate the costly laser anneal process and additional processes concerned with metal catalyst, and extend the application of poly-Si TFTs further. In fact, a lot of effort has been made to realize it over 20 years, especially with various plasma-enhanced CVD techniques (PECVD) [1,2,3,4,5,6]. No as-deposited crystalline Si film, however, has been utilized in the TFT fabrication industrially so far because of poor electrical properties of the film. The reason why they are in the low-temperature CVD poly-Si thin films is poor crystallinity of the films as shown in Fig.1. : the crystal growth always starts with a formation of nuclei on the substrate as a nature of the CVD process; as a result, the crystallinity of the films is always worse at the bottom, and the films often accompany amorphous tissue, so that the thick films have to be grown in order to establish high crystallinity for device application; in fact, the highest field effect mobility of 45 cm^2/Vs has been achieved with a poly-Si thin film of 0.7μm prepared by PECVD with SiH_4 and SiF_4 at 450°C so far, while the mobility remained ~10 cm^2/Vs with thinner films less than 0.2μm [7,8].



Fig. 1 Typical cross sectionalTEM image of low-temperature CVD poly-Si thin film on the glass substrate.

For improvement of crystallinity in the films, many trials for promoting the nucleation of the crystallites at the early stage of the film growth and crystal growth have been done, which include high hydrogen dilution of silane and atomic hydrogen treatment during the film growth in PECVDs. These could enhance the crystallinity of the films indeed because nuclei formation was accelerated, but these always resulted in the reduction of grain size because the nuclei density was enhanced simultaneously. Thus, we cannot improve the quality of the films in this way because the formation of nuclei and their growth are not controlled independently as schematically illustrated in Fig.2.

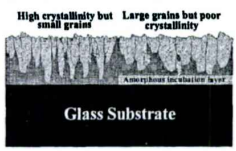


Fig. 2 Effect of promoting crystallization at the early stage of the film growth.

The possible way to solve this dilemma is to establish any CVD techniques that can form crystalline nuclei on the substrate directly without accompanying amorphous incubation layer and grow the resulting nuclei to the grains selectively as schematically illustrated in Fig.3.

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In addition, for fabrication of large-area devices, selective film deposition on the substrate, that is, no film deposition on CVD reactor walls can be beneficial to reduce a tact time and improve throughput. From this point of view, the thermal CVD technique with a cold-wall type reactor is advantageous over the conventional CVD techniques including PECVDs and hot-wire CVDs: the reduction of growth temperature in these CVDs techniques are based on a principle of generating film precursors by supplying enough energy to decompose the source materials at a space far from the substrates, so that the film can grow on the reactor walls inevitably and the powder, which is the aggregates of silane with the reactive precursors, is easy to be formed; on the other hand, the reactive space where the film precursors are formed is limited in the vicinity of the heated substrate in thermal CVDs, so that the films can hardly grow on the reactor walls and the powder formation can be suppressed significantly.

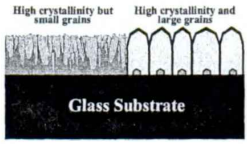


Fig.3 Conventional and ideal growth of poly-Si thin film for TFT applications.

Taking account of these requirements described above, we have proposed a new thermal CVD technique for deposition of large-area poly-Si and SiGe thin films at the low-temperatures where the glass substrates are available, which we call *Reactive Thermal CVD*. In this CVD technique, a set of reactive source gases is featured to promote low-temperature film growth and crystallization of the film, which is a redox materials system that leads to their decomposition *via* chemical reactions of their own with the aid of heat from the heated substrate. Therefore, with an appropriate selection of the set of the source materials, we could deposit a film on the substrate selectively at the temperatures lower than the pyrolysis temperatures of the source gases. Thus, we have established film growth of high crystallinity poly-SiGe [9,14] and poly-Si [25] at a low temperature of 450°C with disilane, Si_2H_6 and a small amount of either germanium tetrafluoride, GeF_4 or fluorine, F_2, respectively. Recently we have demonstrated their device grade film quality by fabricating bottom-gate TFTs on the SiO_2/Si substrates with a high mobility over 50cm^2/Vs [20,21,22, 26].

RESULTS AND DISCUSSION

1. Poly-SiGe thin films from Si_2H_6 and GeF_4 [9-22]

We selected Si_2H_6, as a Si source because of easy thermal activation at temperatures over 400°C and GeF_4 as a counterpart because of chemical reactivity as an

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oxidant for Si_2H_6: GeF_4 is very stable compound and its pyrolysis temperature is over 1000°C, but it can react with Si at elevated temperatures, e.g., 300°C, resulting in etching of Si and so does with Si_2H_6, resulting in the film deposition. In addition, the combination of Si_2H_6 and GeF_4 exhibits unique features in terms of film growth: these hardly react each other at ambient temperatures while react at elevated temperatures over 300°C, leading to the film deposition on the heated substrate and no film deposition on the cool reactor wall; the film composition varies from almost Si to Ge because of redox reactions of Si_2H_6 and GeF_4 when a gas flow ratio and temperature are changed: Si_2H_6 is oxidized by GeF_4 to afford Si and GeF_2; on the other hand, GeF_4 is reduced by Si_2H_6 to afford Ge and SiF_4.

The deposition system is a typical low-pressure CVD reactor of 40 litters in volume, whose detail is described elsewhere [9], and the substrate platform equipped with a resistive heater is faced with a gas nozzleas shown in Fig.4.

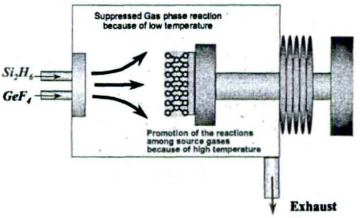


Fig. 4 Cold-wall type of CVD reactor equipped with nozzle and substrate plat form.

In this CVD, Ge-rich films are easy to deposit even if the GeF_4 flow rate is less than one twentieth of Si_2H_6 flow rate over 320°C. This is probably attributed to the effective chemical activation of GeF_4 adsorbed on the semiconductor surface. In fact, the selective epitaxial growth of Ge-rich film is observed on the SiO_2-patterned Si-wafer at 320°C. For Si-rich films, It was found that activation of Si_2H_6 was very important and a typical condition required a high gas flow ratio of Si_2H_6 to GeF_4 of 20 or more and a high substrate temperature over 400°C, basically. Fig. 5 shows the deposition rate and the film composition as a function of GeF_4 flow rates at a fixed condition, i.e., substrate temperature of 450°C and Si_2H_6 and He flow rates of 20 and 500 sccm, respectively.

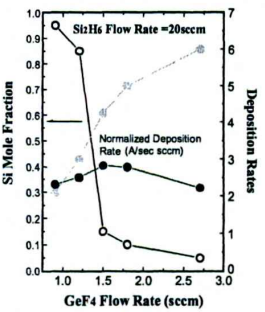


Fig. 5 Deposition rate and Si content of poly-SiGe films as a function of GeF_4 flow rate at 450°C and 0.41Torr.

Thanks to a thermal CVD-based film growth, we can tune the growth condition with a great flexibility [11]. In fact, with an appropriate

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selection of gas flow rates including a flow rate of carrier gas, e.g., He, we can deposit the Si-rich poly-Si films in a very wide range of the pressure. A typical growth conduction for Si-rich films is shown in Table 1.

Table 1 Typical conditions for Si-rich poly-SiGe film

	Low-pressure condition	High-Pressure condition
Pressure	0.5 Torr	5 Torr
Si_2H_6/ GeF_4	2 sccm/0.2 sccm	3 sccm/0.03 sccm
He	500 sccm	1000~4000 sccm

Fig. 6 exhibits a film growth rate as a function of GeF_4 flow rate at a fixed Si_2H_6 and He flow rates of 3 and 1000 sccm, substrate temperature of 450°C, and pressure of 5Torr, in which we can see two distinctive effects associated with the role of GeF_4 in the present CVD process: at a certain range of GeF_4 flow rate, e.g., 0.2sccm, deposition rate is increased with an increase in the GeF_4 flow rate, indicating promotion of decomposition of Si_2H_6; on the other hand, Ge content is increased as shown in the inset of Fig. 6, and deposition rate decreased when the GeF_4 flow rate exceeds over 0.4sccm, indicating Ge incorporation in the film and etching activity of GeF_4.

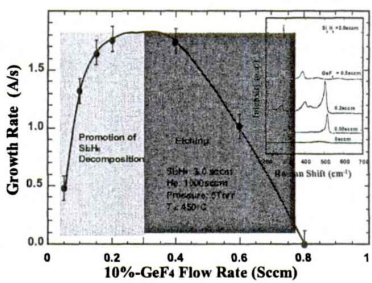
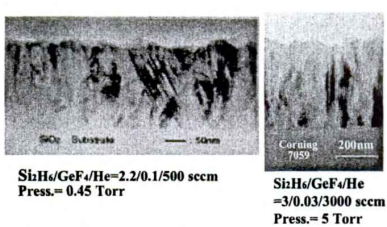


Fig. 6 Growth rate and typical Raman spectra od the films as a function of GeF_4 flow rate at 450°C and 5Torr.

Fig. 7 shows the TEM images of typical poly-Si films prepared at 0.45 Torr and 5 Torr. The film thickness is about 200nm and 400nm, respectively. These film textures are quite different from those of the films prepared by conventional low-temperature CVDs including plasma enhanced CVDs, and rather similar to those prepared at high temperatures over 600°C by LP-CVDs [14]. As is clear in the TEM images, the crystal growth starts from the interface of the substrate irrespective of the pressure, indicating



$Si_2H_6/GeF_4/He$=2.2/0.1/500 sccm Press.= 0.45 Torr

$Si_2H_6/GeF_4/He$ =3/0.03/3000 sccm Press.= 5 Torr

Fig. 7 Cross sectional TEM images of poly-SiGe films prepared at 0.45 and 5Torr at 450°C .

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that the nucleation takes place just on the substrate surface. In fact, we could observe the isolated nuclei on the substrate, when the deposition is stopped at very early stage for the film growth as shown in Fig. 8. As-deposited poly- $Si_{1-x}Ge_x$ films fabricated in this process have a small hydrogen content less than 0.01%.

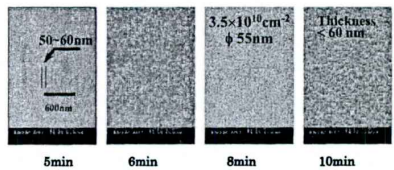


Fig. 8 SEM images of the substrate surface at the early stage of the film growth at 5Torr and 450°C.

On other hand, electron spin resonance study of the films revealed that the spin density was proportional to the grain size in their double logalithmic plot, indicating that both Si and Ge dangling bonds were accumulated on the grain boundaries and/or surface, and was on the order of $10^{18}cm^{-3}$ typically for the film having a diameter of 100nm. This number is rather high because of a high deposition temperature of 450°C where Si-H bond is easy to be dissociated thermally. In fact, the electrical properties are dominated by the dangling bonds in the as-deposited films and show conductivity around 10^{-4} S/cm and its activation energy around 0.4 eV. After the hydrogenation, the conductivity is reduced down to 10^{-5} S/cm and its activation energy goes up to 0.55 eV, showing the intrinsic behavior of crystalline silicon.

2. TFT fabrication with poly-SiGe thin films

We have fabricated n- and p-channel bottom top gate TFTs with the Si-rich poly-SiGe tihn films of 200 nm prepared at 450°C, for which a thermally oxidized SiO_2 layer of 75nm on Si-wafer was used as a gate insulator. In this TFT fabrication, the post hydrogen treatment is the necessary process as in the case of the on-going TFT fabrication using poly-Si thin films prepared by the laser annealing and solid state crystallization of amorphous silicon films, because the deposition temperature in this process is 450°C where the Si-H and Ge-H bonds are thermally dissociated. However, the dangling

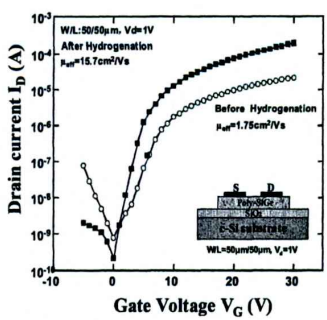


Fig. 9 Effect of hydrogen treatment by Hot-wire technique on TFT characteristics of n-channel bottom-gate TFT.

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bonds over ~10^{17} cm^{-3} are accumulated in the grain boundaries as we described above, so that they are easy to be terminated with hydrogen treatment effectively: in fact, we could confirm this with a comparison of TFT characteristics before and after the post-hydrogen treatment with Hot-wire technique as shown in Fig. 9: the field effect mobility of 1.75 cm^2/Vs in as-fabricated TFTs is very much improved up to 15.7 cm^2/Vs after the hydrogenation with the Hot-wire technique for 1hr min at 250°C. Fig. 10 shows the transfer characteristics for n-and p-type bottom-gate TFTs fabricated, whose the highest process temperature was 450°C for film deposition. The field effect mobility were 36 cm^2/Vs for n-channel TFT and 55cm^2/Vs for p-channel TFT after the hydrogen treatment. It should be noted that such a high mobility over 30 cm^2/Vs can be achieved in the bottom-gate TFT where the channel region is formed in a limited region of poly-SiGe thin film grown on the gate oxide. This result demonstrates how high the film crystallinity at the early stage of the film deposition is in the present poly-SiGe film, which is very difficult to achieve in the conventional low-temperature CVDs. It looks that the p-channel TFT fabricated is superior to the n-channel one as far as we judge from the transfer characteristics as shown in the figure, but we think that it can be improved much because of inexperienced fabrication in the first trial.

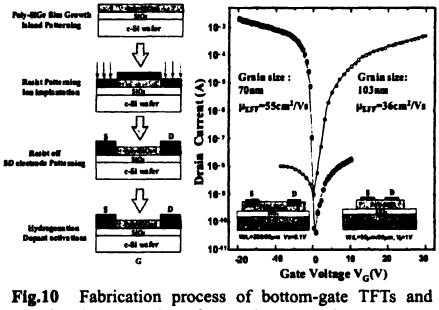


Fig.10 Fabrication process of bottom-gate TFTs and transfer characteristics of n- and p-channel bottom-gate TFTs fabricated with 200nm thick poly-SiGe films.

We also fabricated n-and p-channel top-gate TFTs with Si-rich 200nm thick poly-SiGe films on the corning 7059 glass according to the processes

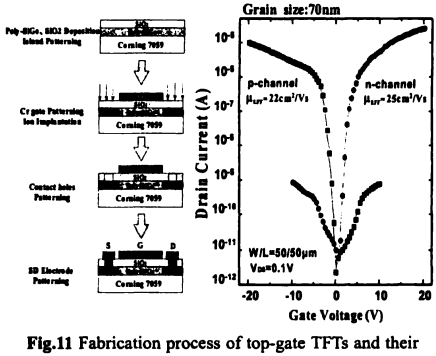


Fig.11 Fabrication process of top-gate TFTs and their transfer characteristics of n- and p-channel top-gate TFTs fabricated with 200nm thick poly-SiGe films.

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illustrated in Fig. 11. The maximum process temperature was 450°C for the film growth as well. The field effect mobility is 22cm^2/Vs and 25 cm^2/Vs for p-channel and n-channel TFTs after the hydrogenation, respectively. The transfer characteristics of n-and p-channel TFTs were very compatible and showed a good promise for the CMOS applications. Judging from the results on the effect of grain size on TFT mobility in the n-channel bottom gate TFTs fabricated, it is very plausible that the present field effect mobility is determined by a rather small grain of 70 nm in the present poly-SiGe film used for TFT fabrication and can be increased over 50 cm^2/Vs or more when the grain size is increased over 100 nm.

3. Poly-Si thin films from Si_2H_6 and F_2 [24-26]

In the polycrystalline film growth in the reactive thermal CVD with Si_2H_6 and GeF_4, it is very clear that GeF_4 itself plays a decisive role for low-temperature crystal growth of poly-SiGe, judging from a fact that amorphous films are always deposited in the absence of GeF_4 at 450°C, even if GeH_4 is used instead of GeF_4. We pay attention to the etching activity of GeF_4 for low-temperature crystallization of the films out of the unique chemical properties in Si_2H_6 and GeF_4 system as described previously. It is very probable that GeF_4 breaks Si-Si bonds during the film deposition because of its etching activity. Therefore, it is very likely that the resulting loose Si-network island at the very early stage of the film growth is easy to reorganize into a nucleus on the substrate surface, while the crystal growth is well maintained once the nucleation is formed due to the same reason of easy structural relaxation of the loose Si-network. In other words, the structural relaxation of as-formed Si-network is relaxed into thermodynamically stable crystal lattice via quasi-chemical equilibrium between Si-Si bond breaking and Si-Si bond formation mediated by GeF_4. We haven't confirmed how GeF_4 contributes to the crystal growth experimentally yet, but this idea reminds us of another possible promoter for crystal growth, e.g., fluorine that shows etching activity to Si, for the low-temperature crystal growth.

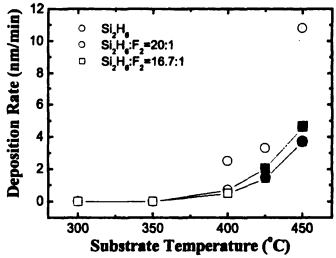


Fig. 12 Deposition rate as a function of substrate temperature and different flow ratio of Si_2H_6 to F_2.

Thus, we proposed another CVD

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technique for preparation of poly-Si thin films with Si_2H_6 and F_2 as another set of reactive gases. Although no film deposition took place at the low temperatures below 400°C, when a low gas ratio of Si_2H_6 to F_2, e.g., 20 to 1 was adopted, the film growth took place over 400°C as shown in Fig. 12 . This film deposition follows the thermal CVD process with Si_2H_6 basically, but interestingly poly-Si films grow over 425°C where amorphous films are always deposited with Si_2H_6 alone. The deposition rate is small, e.g., 4.2nm/min, probably because the deposition is balanced with etching of the film.

Fig. 13 shows a cross sectional TEM image of the film deposited at 450°C with Si_2H_6 in the presence of a small amount of fluorine. This shows that very uniform crystallinity from bottom to top-surface is established. In clear contrast to the early stage of the film growth of poly-SiGe thin films described above, we could not observe nuclei formation at the early stage of the present film growth, although the incubation layer was very thin, e.g., less than 2~5nm at best.

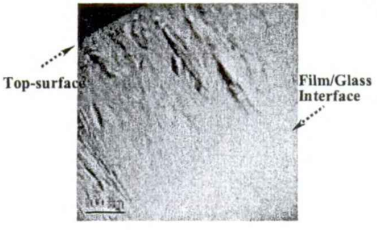


Fig. 13 Typical TEM image of poly-Si thin films on glass substrates prepared with Si_2H_6 and F_2 at 450°C.

4. TFT fabrication with poly-Si thin films

We fabricated n-and p-channel bottom gate TFTs with a Si-wafer with a thermal oxide layer of 75 nm as illustrated in Fig. 14. We found that the performance of as-fabricated n-and p-channel TFTs were very much improved after the post-hydrogenation by Hot-wire technique or thermal annealing at 400°C for 2 hours, and exhibited a very good transfer characteristics with field effect mobility as high as 54.5 and 62.6 cm^2/Vs, respectively. This excellent result is probably attributed to the high crystallinity at the early stage of the film growth as discussed above.

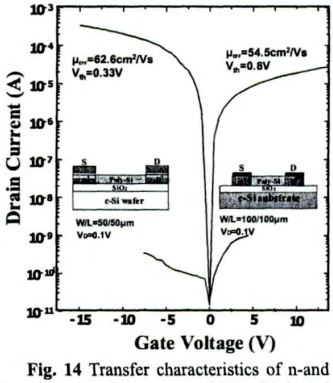


Fig. 14 Transfer characteristics of n-and p-channel bottom-gate TFTs fabricated with 200nm thick poly-Si films prepared at 450°C.

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SUMMARY

In summary, we have established a new thermal CVD technique, i.e., Reactive thermal CVD, for low-temperature growth of poly-Si and SiGe thin films at 450°C with Si_2H_6 and GeF_4 and with Si_2H_6 and F_2, respectively. These polycrystalline films exhibited high crystallinity even in very thin films less than 200nm in thickness, and were successfully applied to bottom and top-gate n-and p-channel TFTs. The high field effect mobility of 36 and 54 cm^2/Vs was achieved in bottom-gate n- and p-channel TFTs fabricated, respectively, and 25 and 22 cm^2/Vs for top-gate n- and p-channel ones, respectively. This new CVD process is very promising for a direct growth of device-grade poly-Si thin films for TFT applications. Now we are establishing a good basis for challenging a high mobility TFTs over 100 cm^2/Vs that no CVD technique has achieved yet.

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