UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 11,575,381 B1
APPLICATION NO. : 17/723145
DATED : February 7, 2023
INVENTOR(S) : Nima Badizadegan

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the Claims

Column 28, Line 22-23, Claim 1, replace:
"(a) receiving, by a deserializer in a field programmable array, a clock signal;"
With:
-- (a) receiving, by a deserializer in a field programmable gate array, a clock signal; --

Signed and Sealed this
Fourteenth Day of November, 2023

Katherine Kelly Vidal

Katherine Kelly Vidal
Director of the United States Patent and Trademark Office

Docket No. 00287-0017

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	:	HFT Solutions, LLC
Patent No.	:	11,575,381 B1
Issued	:	February 7, 2023
Appl. No.	:	17/723,145
Filing Date	:	April 18, 2022
For	:	FIELD PROGRAMMABLE GATE ARRAY WITH EXTERNAL PHASE-LOCKED LOOP
Art Unit	:	2849
Examiner	:	CHENG, Diana
Confirmation No.	:	1635
Customer No.	:	01912

REQUEST FOR CERTIFICATE OF CORRECTION UNDER 35 U.S.C. § 255 AND 37 C.F.R. § 1.323

EFS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Attn: Certificate of Corrections Branch

Sir:

In reviewing the above-identified patent, a minor typographical error was discovered therein requiring correction. The error noted is set forth on a Certificate of Correction (Form PTO/SB/44), which is attached hereto.

Specifically, Patentee requests the following correction:

At column 28 line 22-23, Claim 1, please replace "(a) receiving, by a deserializer in a field

programmable array, a clock signal;" with "(a) receiving, by a deserializer in a field programmable gate array, a clock signal;".

Patentee submits that the above error is of a typographical nature and that the correction does not constitute new matter, nor does it necessitate reexamination. Accordingly, issuance of the attached Certificate of Correction pursuant to 35 U.S.C. § 255 and 37 C.F.R. § 1.323 is respectfully requested.

Patentee submits the required fee of $160.00 for requested certificate of correction. Should any additional fee be required, authorization is hereby given to charge the amount of any such fee to Deposit Account No. 01-1785.

Respectfully submitted,

AMSTER, ROTHSTEIN & EBENSTEIN LLP
Attorneys for Applicant
405 Lexington Avenue
New York, New York, 10174
(212) 336-8000

Dated: October 18, 2023
New York, New York

By: /Keith J. Barkaus/
Keith J. Barkaus, Reg. No. 51,431

PTO/SB/44 (09-07)
Approved for use through 03/31/2023. OMB 0651-0033
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.
(Also Form PTO-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 11,575,381

APPLICATION NO.: 17/723,145

ISSUE DATE : February 7, 2023

INVENTOR(S) : Nima Badizadegan

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the Claims

Column 28, line 22-23, Claim 1, please replace "(a) receiving, by a deserializer in a field programmable array, a clock signal;" with:
-- (a) receiving, by a deserializer in a field programmable gate array, a clock signal; --

MAILING ADDRESS OF SENDER (Please do not use Customer Number below):

Keith J. Barkaus, Reg. No. 51,431
Amster, Rothstein & Ebenstein LLP
405 Lexington Avenue, New York, NY 10174

This collection of information is required by 37 CFR 1.322, 1.323, and 1.324. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1.0 hour to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Attention Certificate of Corrections Branch, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

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www.uspto.gov

ELECTRONIC ACKNOWLEDGEMENT RECEIPT

APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
17/723,145	**10/18/2023 05:18:48 PM ET**	**00287-0017**

Title of Invention

FIELD PROGRAMMABLE GATE ARRAY WITH EXTERNAL PHASE-LOCKED LOOP

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	11575381
CONFIRMATION #	1635	FILED BY	Victoria Gilmore
PATENT CENTER #	63027450	FILING DATE	04/18/2022
CUSTOMER #	1912	FIRST NAMED INVENTOR	Nima Badizadegan
CORRESPONDENCE ADDRESS	-	AUTHORIZED BY	Keith Barkaus

Documents

TOTAL DOCUMENTS: 2

DOCUMENT	PAGES	DESCRIPTION	SIZE (KB)
1-RequestforCertificateofCorrection.pdf	2	Request for Certificate of Correction	105 KB
2-CertificateofCorrection.pdf	2	Request for Certificate of Correction	171 KB

Digest

DOCUMENT	MESSAGE DIGEST(SHA-512)
1-	5D9B179831D0AEDB7BF87E61F4C5F4A6BAB1780062E7911CC

RequestforCertificateofCorrection.pdf	A3CBB73584C2AFDB8D14E1D60490EF35F4CDA3980D609B72BE411C75A6BE2CBFA0F8DF2B6E19E88
2-CertificateofCorrection.pdf	5987BDDF69E8855F4178B9ACA4EFF9E795E0C24F04D4A8D6C013031499224FBECD9C25644C9B977578D8E29EB42BCD1FCF60B40190BA64BCE7D75816EB151489

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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ELECTRONIC PAYMENT RECEIPT

APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
17/723,145	**10/18/2023 05:18:48 PM ET**	**00287-0017**

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PATENT CENTER #	63027450	AUTHORIZED BY	Keith Barkaus
CUSTOMER #	1912	FILING DATE	04/18/2022
CORRESPONDENCE ADDRESS	-	FIRST NAMED INVENTOR	Nima Badizadegan

Payment Information

PAYMENT METHOD	PAYMENT TRANSACTION ID	PAYMENT AUTHORIZED BY
CARD / 1077	**E20230HH19485413**	**Victoria Gilmore**

FEE CODE	DESCRIPTION	ITEM PRICE($)	QUANTITY	ITEM TOTAL($)
2811	CERTIFICATE OF CORRECTION	160.00	1	160.00
			TOTAL AMOUNT:	**$160.00**

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Organization _____ Bldg/Room _____

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Citadel Securities LLC, Exhibit 1003, Page 10 of 290

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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Alexandria, Virginia 22313-1450
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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/723,145	02/07/2023	11574364	00287-0017	1635

1912 7590 01/18/2023

AMSTER, ROTHSTEIN & EBENSTEIN LLP
90 PARK AVENUE
NEW YORK, NY 10016

OIPP LHDTSV-4
JAN 30 2023
PATENT & TRADEMARK OFFICE

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Patents Stakeholder Experience (OPSE), Stakeholder Support Division (SSD) at (571)-272-4200.

INVENTOR(s) (Please see PAIR WEB site http://pair.uspto.gov for additional inventors):

Nima Badizadegan, Salem, NH;

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

HFT Solutions, LLC, New Canaan, CT;

Best Available Copy

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The USA offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to encourage and facilitate business investment. To learn more about why the USA is the best country in the world to develop technology, manufacture products, and grow your business, visit SelectUSA.gov.

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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/723,145	02/07/2023	11575381	00287-0017	1635

1912 7590 01/18/2023

AMSTER, ROTHSTEIN & EBENSTEIN LLP
90 PARK AVENUE
NEW YORK, NY 10016

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Nima Badizadegan, Salem, NH;

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

HFT Solutions, LLC, New Canaan, CT;

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The USA offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to encourage and facilitate business investment. To learn more about why the USA is the best country in the world to develop technology, manufacture products, and grow your business, visit SelectUSA.gov.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via EFS-Web.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

1912 7590 09/22/2022
AMSTER, ROTHSTEIN & EBENSTEIN LLP
90 PARK AVENUE
NEW YORK, NY 10016

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via EFS-Web or by facsimile to (571) 273-2885, on the date below.

Keith J. Barkaus	(Typed or printed name)
/Keith J. Barkaus/	(Signature)
December 16, 2022	(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/723,145	04/18/2022	Nima Badizadegan	00287-0017	1635

TITLE OF INVENTION: FIELD PROGRAMMABLE GATE ARRAY WITH EXTERNAL PHASE-LOCKED LOOP

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	$600	$0.00	$0.00	$600	12/22/2022

EXAMINER	ART UNIT	CLASS-SUBCLASS
CHENG, DIANA	2849	327-156000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/AIA/122 or PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/AIA/47 or PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 Amster, Rothstein & Ebenstein LLP
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE	(B) RESIDENCE: (CITY and STATE OR COUNTRY)
HFT Solutions, LLC	New Canaan, CONNECTICUT

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ☒ Corporation or other private group entity ❑ Government

4a. Fees submitted: ☒ Issue Fee ❑ Publication Fee (if required) ❑ Advance Order - # of Copies _____

4b. Method of Payment: *(Please first reapply any previously paid fee shown above)*

☒ Electronic Payment via EFS-Web ❑ Enclosed check ❑ Non-electronic payment by credit card (Attach form PTO-2038)

☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. 011785

5. **Change in Entity Status** (from status indicated above)

❑ Applicant certifying micro entity status. See 37 CFR 1.29

❑ Applicant asserting small entity status. See 37 CFR 1.27

❑ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature /Keith J. Barkaus/ Date December 16, 2022

Typed or printed name Keith J. Barkaus Registration No. 51,431

Electronic Patent Application Fee Transmittal

Application Number:	17723145
Filing Date:	18-Apr-2022
Title of Invention:	FIELD PROGRAMMABLE GATE ARRAY WITH EXTERNAL PHASE-LOCKED LOOP
First Named Inventor/Applicant Name:	Nima Badizadegan
Filer:	Keith J. Barkaus/Victoria Gilmore
Attorney Docket Number:	00287-0017

Filed as Small Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
PUBL. FEE- EARLY, VOLUNTARY, OR NORMAL	1504	1	0	0
UTILITY APPL ISSUE FEE	2501	1	600	600
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**600**

Electronic Acknowledgement Receipt

EFS ID:	47226088
Application Number:	17723145
International Application Number:	
Confirmation Number:	1635
Title of Invention:	FIELD PROGRAMMABLE GATE ARRAY WITH EXTERNAL PHASE-LOCKED LOOP
First Named Inventor/Applicant Name:	Nima Badizadegan
Customer Number:	1912
Filer:	Keith J. Barkaus/Victoria Gilmore
Filer Authorized By:	Keith J. Barkaus
Attorney Docket Number:	00287-0017
Receipt Date:	16-DEC-2022
Filing Date:	18-APR-2022
Time Stamp:	16:29:45
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$600
RAM confirmation Number	E2022BFG30024696
Deposit Account	
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	17-PTOL-85.pdf	155739 52b71b77d1163d6d302730a817b5b102d21faaf1	no	1
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	40675 54a24325f15145be914dad0ec08e0ace4ad8206b	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	196414		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

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17/723,145	04/18/2022	Nima Badizadegan	00287-0017	1635

1912 7590 10/20/2022
AMSTER, ROTHSTEIN & EBENSTEIN LLP
90 PARK AVENUE
NEW YORK, NY 10016

EXAMINER	
CHENG, DIANA	

ART UNIT	PAPER NUMBER
2849	

MAIL DATE	DELIVERY MODE
10/20/2022	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Corrected ***Notice of Allowability***	**Application No.** 17/723,145	**Applicant(s)** Badizadegan, Nima	
	Examiner Diana J Cheng	**Art Unit** 2849	**AIA (FITF) Status** Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☑ This communication is responsive to Terminal Disclaimer 09/16/2022 and IDS 10/03/2022.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☑ The allowed claim(s) is/are 1-12 . As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see **http://www.uspto.gov/patents/init_events/pph/index.jsp** or send an inquiry to **PPHfeedback@uspto.gov.**

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some* c) ☐ None of the:

   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____ .

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____ .

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☑ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____.
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material _____.
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date. _____.
5. ☐ Examiner's Amendment/Comment
6. ☐ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/DIANA J. CHENG/
Primary Examiner, Art Unit 2849

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/723,145	Badizadegan, Nima
	Examiner	**Art Unit**
	Diana J Cheng	2849

CPC						
Symbol					**Type**	**Version**
H03L	/	7	/	085	F	2013-01-01
G06F	/	1	/	08	I	2013-01-01
G06F	/	30	/	34	I	2020-01-01
H04J	/	3	/	0658	I	2013-01-01
H03L	/	2207	/	50	A	2013-01-01

CPC Combination Sets							
Symbol					**Type**	**Set**	**Ranking**	**Version**
	/		/					

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	12	
/DIANA J. CHENG/ Primary Examiner, Art Unit 2849	19 October 2022	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	2

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/723,145	Badizadegan, Nima
	Examiner	**Art Unit**
	Diana J Cheng	2849

INTERNATIONAL CLASSIFICATION				
CLAIMED				
H03L7/085	/	7	/	085
G06F1/08	/	1	/	08
G06F30/34	/	30	/	34
H04J3/06	/	3	/	06

NON-CLAIMED				
	/		/	

US ORIGINAL CLASSIFICATION	
CLASS	**SUBCLASS**

CROSS REFERENCES(S)						
CLASS	**SUBCLASS (ONE SUBCLASS PER BLOCK)**					

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	12	
/DIANA J. CHENG/ Primary Examiner, Art Unit 2849	19 October 2022	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	2

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/723,145	Badizadegan, Nima
	Examiner	**Art Unit**
	Diana J Cheng	2849

☑ Claims renumbered in the same order as presented by applicant ☐ CPA ☑ T.D. ☐ R.1.47

CLAIMS

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	12	
/DIANA J. CHENG/ Primary Examiner, Art Unit 2849	19 October 2022	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	2

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/723,145	Badizadegan, Nima
	Examiner	**Art Unit**
	Diana J Cheng	2849

CPC - Searched*		
Symbol	**Date**	**Examiner**
H03L7/085,087,089,0891,0893,0895,0896,0898,091,093,095	09/02/2022	DJC
G06F30/30,34,343,347	09/02/2022	DJC
G06F1/04,08 H04J3/0658 H03L2207/50	09/02/2022	DJC

CPC Combination Sets - Searched*		
Symbol	**Date**	**Examiner**

US Classification - Searched*			
Class	**Subclass**	**Date**	**Examiner**

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	**Date**	**Examiner**
Double Patenting and Prior Art Search	09/02/2022	DJC
Refreshed Search	09/12/2022	DJC
Refreshed Search	09/19/2022	DJC
Interference Search	09/19/2022	DJC
Refreshed Search	10/19/2022	DJC
Refreshed Interference Search	10/19/2022	DJC

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/723,145	Badizadegan, Nima
	Examiner	Art Unit
	Diana J Cheng	2849

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner
See Search History		09/19/2022	DJC

Citadel Securities LLC, Exhibit 1003, Page 24 of 200

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (01-22)
Approved for use through 05/31/2024. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	17723145
Filing Date	2022-04-18
First Named Inventor	Nima Badizadegan
Art Unit	2849
Examiner Name	CHENG, Diana
Attorney Docket Number	00287-0017

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	7945803	B2	2011-05-17	Anthony Mark Jones et al.	
	2	8996906	B1	2015-03-31	Kent R. Townley et al.	
	3	9000801	B1	2015-04-07	Christopher D. Ebeling et al.	
	4	9954530	B2	2018-04-24	Christopher D. Ebeling et al.	
	5	10564666	B2	2020-02-18	Ross MORGAN et al.	

If you wish to add additional U.S. Patent citation information please click the Add button. Add

U.S.PATENT APPLICATION PUBLICATIONS Remove

Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					

If you wish to add additional U.S. Published Application citation information please click the Add button. Add

FOREIGN PATENT DOCUMENTS Remove

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /D.J.C/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	17723145
Filing Date	2022-04-18
First Named Inventor	Nima Badizadegan
Art Unit	2849
Examiner Name	CHENG, Diana
Attorney Docket Number	00287-0017

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2]	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1	2426164	GB	A	2006-11-15	AGILENT TECHNOLOGIES, INC.		
	2	2572463	GB	B	2020-12-16	CIRRUS LOGIC INTERNATIONAL SEMICONDUCTOR LTD.		

If you wish to add additional Foreign Patent Document citation information please click the Add button Add

NON-PATENT LITERATURE DOCUMENTS Remove

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1	U.S. Provisional Patent Application No. 62/649,783 filed March 29, 2018.	

If you wish to add additional non-patent literature document citation information please click the Add button Add

EXAMINER SIGNATURE

Examiner Signature	/DIANA J. CHENG/	Date Considered	10/19/2022

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /D.J.C/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	17723145
Filing Date	2022-04-18
First Named Inventor	Nima Badizadegan
Art Unit	2849
Examiner Name	CHENG, Diana
Attorney Docket Number	00287-0017

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☒ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

☒ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Keith J. Barkaus/	Date (YYYY-MM-DD)	2022-10-03
Name/Print	Keith J. Barkaus	Registration Number	51,431

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /D.J.C/

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /D.J.C/

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	HFT Solutions, LLC	Confirmation No.: 1635
Title:	FIELD PROGRAMMABLE GATE ARRAY WITH EXTERNAL PHASE-LOCKED LOOP	
Appl. No.:	17/723,145	
Filing Date:	April 18, 2022	
Examiner:	CHENG, Diana	OK TO ENTER: /D.J.C/
Art Unit:	2849	
Docket No.:	00287-0017	
Customer No.:	01912	

AMENDMENT AFTER NOTICE OF ALLOWANCE UNDER 37 C.F.R. 1.312

VIA EFS

Mail Stop AMENDMENT
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Pursuant to the provisions under 37 CFR 1.312, please amend this application as follows:

Amendments to the claims begin on page 2.

Remarks begin on page 5.

Citadel Securities LLC, Exhibit 1003, Page 29 of 290

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	HFT Solutions, LLC	Confirmation No.: 1635
Title:	FIELD PROGRAMMABLE GATE ARRAY WITH EXTERNAL PHASE-LOCKED LOOP	
Appl. No.:	17/723,145	
Filing Date:	April 18, 2022	
Examiner:	CHENG, Diana	
Art Unit:	2849	
Docket No.:	00287-0017	
Customer No.:	01912	

AMENDMENT AFTER NOTICE OF ALLOWANCE UNDER 37 C.F.R. 1.312

VIA EFS

Mail Stop AMENDMENT
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Pursuant to the provisions under 37 CFR 1.312, please amend this application as follows:

Amendments to the claims begin on page 2.

Remarks begin on page 5.

Citadel Securities LLC, Exhibit 1003, Page 30 of 290

CLAIMS

What is claimed is:

1. (Currently Amended) A method for processing a first serial data stream, using a field programmable gate array system, to generate a second serial data stream, wherein the method comprises the steps of:

(a) receiving, by a deserializer in a field programmable array, a clock signal;

(b) receiving, by the deserializer, the first serial data stream;

(c) generating, by the deserializer, a receiver side clock signal;

(d) converting, by the deserializer, the first serial data stream into a first plurality of parallel data streams;

(e) transmitting, from the deserializer to computational circuitry in the field programmable gate array, the first plurality of parallel data streams;

(f) transmitting, from the deserializer to a phase lock loop of the field programmable gate array system that is not within [[on]] the field programmable gate array, the receiver side clock signal;

(g) generating, using the phase lock loop, a second clock signal;

(h) generating, within the field programmable gate array, a transmitter side clock signal derived from the second clock signal;

(i) performing, by the computational circuitry, a set of operations on at least a portion of the first plurality of parallel data streams to generate a second plurality of parallel data streams; and

(j) transmitting, from the field programmable gate array system, the second serial data stream, derived from the second plurality of parallel data streams,

wherein said method does not use clock domain crossing operations that delay processing of the first set of parallel data streams.

2. (Original) The method of claim 1, wherein the first serial data stream comprises market

data, the second serial data stream comprises order entry data, and the set of operations are associated with a trading algorithm.

3. (Original) The method of claim 1, wherein the first serial data stream includes market data and the second serial data stream includes trading data.

4. (Original) The method of claim 1, wherein the set of operations includes at least one of the following:

(i) an arithmetic operation;

(ii) a logical operation;

(iii) a pipeline operation; and

(iv) a memory access operation.

5. (Original) The method of claim 1, wherein at least a portion of the set of operations performed in step (h) are performed prior to step (g).

6. (Original) The method of claim 1, wherein at least a portion of the set of operations performed in step (h) are performed after step (g).

7. (Original) The method of claim 1, wherein all of the set of operations performed in step (h) are performed after step (g).

8. (Original) The method of claim 1, wherein step (g) further comprises:

(i) generating, by the phase lock loop, a feedback clock signal associated with the transmitter side clock signal by performing the following steps until a first output of a phase detector of the field programmable gate array system is below a first threshold level:

(1) generating, by an adjustable oscillator in the field programmable gate array system, the second clock signal;

(2) generating, by the phase detector, the first output based on a comparison of the receiver side clock signal and the feedback clock signal obtained from the second clock signal;

(3) transmitting, from the phase detector to a phase controller of the field programmable gate array system, the first output;

(4) determining, by the phase controller, interim adjustment information based on the first output; and

(5) transmitting, from the phase controller to the adjustable oscillator, the interim adjustment information;

wherein, the adjustable oscillator adjusts the second clock signal based on the interim adjustment information,

wherein steps (1) through (5) are repeated until the first output of the phase detector is below the first threshold level.

9. (Original) The method of claim 1, wherein the first plurality of data streams has the same number of data streams as the second plurality of data streams.

10. (Original) The method of claim 1, wherein the first plurality of data streams and the second plurality of data streams comprise one of the following:

(i) eight (8) data streams;

(ii) ten (10) data streams;

(iii) sixteen (16) data streams;

(iv) twenty (20) data streams;

(v) thirty-two (32) data streams;

(vi) forty (40) data streams;

(vii) sixty-four (64) data streams;

(viii) eighty (80) data streams;

(ix) one hundred twenty-eight (128) data streams; and

(x) one hundred sixty (160) data streams.

11. (Original) The method of claim 1, wherein the transmitter side clock signal and the receiver side clock signal have the same frequency and phase.

12. (Original) The method of claim 1, wherein the transmitter side clock signal and the receiver side clock signal have the same frequency and different phases.

REMARKS

Original claims 1-12 were allowed in the Notice of Allowance dated September 22, 2022.

In reviewing the allowed claims, Applicant noted a small typographical error in claim 1. By the present Amendment under Rule 1.312, Applicant has amended claim 1 to correct this minor typographical error.

Favorable consideration and prompt entry of the requested amendment is respectfully requested.

Should the Examiner determine that any issues requiring consideration are raised by this amendment, the Examiner is invited to contact Applicant's undersigned attorney.

Reference to Related Patents and Co-pending Applications

The below chart provides information regarding related issued patents and co-pending applications filed by the present Applicant:

SERIAL NO.	ATTORNEY DOCKET NO.	FILING DATE	STATUS
16/672,076	00287-0007	2019-11-01	Issued USP 10,826,502
16/670,702	00287-0008	2019-10-31	Issued USP 10,771,069
16/888,218	00287-0009	2020-05-29	Issued USP 10,763,865
16/937,314	00287-0011	2020-07-23	Issued USP 10,931,286
16/937,309	00287-0012	2020-07-23	Issued USP 11,018,678
17/248,304	00287-0013	2021-01-19	Issued USP 11,128,305
17/236,577	00287-0014	2021-04-21	Issued USP 11,329,655
17/405,188	00287-0015	2021-08-18	Notice of Allowance – 2022-10-08
17/723,130	00287-0016	2022-04-18	Docketed New Case - Ready for Examination
17/723,145	**00287-0017**	**2022-04-18**	**Present Application**

The Examiner is invited to review the prosecution history of each of these applications, including the cited references of record and related office actions, as the Examiner deems appropriate.

Citadel Securities LLC, Exhibit 1003, Page 34 of 290

CONCLUSION

In view of the foregoing, Applicant respectfully submits that all pending claims are patentable over the cited art and in condition for allowance. Reconsideration and prompt allowance of this application are both respectfully solicited.

Applicant respectfully asserts that the foregoing constitutes a bona fide response to all outstanding objections and rejections within this Office Action.

This application is in condition for immediate allowance. However, should any issue(s) of a minor nature remain, the Examiner is respectfully requested to telephone the undersigned at telephone number (212) 336-8000 so that the issue(s) might be promptly resolved.

Favorable reconsideration of the present application is respectfully requested.

* * * * * *

Any claim amendment(s), claim(s) added, claim(s) canceled, argument(s), remark(s), and/or any combination(s) thereof made in this response pertain solely to the specific aspects of this specific claimed invention. Further, any claim amendment(s), claim(s) added, claim(s) canceled, argument(s), remark(s), and/or any combination(s) thereof are made without prejudice to or disclaimer of Applicant's right to seek patent protection of any unclaimed subject matter such as, but not limited, to narrower unclaimed subject matter, broader unclaimed subject matter, different unclaimed subject matter, variations of unclaimed subject matter, any combination thereof, and/or any other unclaimed subject matter that may or may not be filed, for example, in any design and/or utility patent application(s) such as, but not limited to, continuation patent application(s), continuation-in-part patent application(s), and/or divisional patent application(s) and/or any other patent application(s).

Applicant's silence as to any assertion(s) by the Examiner in the Office Action and/or to any certain fact(s) or conclusion(s) that may be implied and/or alleged by objections(s) and/or rejection(s) in the Office Action is not in any way a concession by Applicant that such assertion(s), implication(s), and/or allegation(s) are accurate, and that all requirements for any objection(s) and/or a rejection(s) have been met. Accordingly, Applicant reserves the right to analyze and dispute any such assertion(s), implication(s), and/or allegation(s) in the future.

Citadel Securities LLC, Exhibit 1003, Page 35 of 290

Respectfully submitted,

AMSTER, ROTHSTEIN & EBENSTEIN LLP
Attorneys for Applicant
90 Park Avenue
New York, NY 10016
(212) 336-8000

Dated: October 13, 2022
New York, New York

By: / Keith J. Barkaus/
Keith J. Barkaus
Registration No. 51,431

Electronic Acknowledgement Receipt

EFS ID:	46811085
Application Number:	17723145
International Application Number:	
Confirmation Number:	1635
Title of Invention:	FIELD PROGRAMMABLE GATE ARRAY WITH EXTERNAL PHASE-LOCKED LOOP
First Named Inventor/Applicant Name:	Nima Badizadegan
Customer Number:	1912
Filer:	Keith J. Barkaus/Victoria Gilmore
Filer Authorized By:	Keith J. Barkaus
Attorney Docket Number:	00287-0017
Receipt Date:	13-OCT-2022
Filing Date:	18-APR-2022
Time Stamp:	12:27:24
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		1-312Amendment.pdf	109873 e392a8cc7490453c044ec6ea0742ee636304bac8	yes	7

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
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(Not for submission under 37 CFR 1.99)

Application Number	17723145
Filing Date	2022-04-18
First Named Inventor	Nima Badizadegan
Art Unit	2849
Examiner Name	CHENG, Diana
Attorney Docket Number	00287-0017

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	2	8996906	B1	2015-03-31	Kent R. Townley et al.	
	3	9000801	B1	2015-04-07	Christopher D. Ebeling et al.	
	4	9954530	B2	2018-04-24	Christopher D. Ebeling et al.	
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Art Unit	2849
Examiner Name	CHENG, Diana
Attorney Docket Number	00287-0017

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	1	2426164	GB	A	2006-11-15	AGILENT TECHNOLOGIES, INC.		
	2	2572463	GB	B	2020-12-16	CIRRUS LOGIC INTERNATIONAL SEMICONDUCTOR LTD.		

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Application Number	17723145
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First Named Inventor	Nima Badizadegan
Art Unit	2849
Examiner Name	CHENG, Diana
Attorney Docket Number	00287-0017

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(12) UK Patent Application (19) GB (11) 2 426 164 (13) A

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(51) INT CL:
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H04L 7/00 (2006.01)

(52) UK CL (Edition X):
H4P PPF

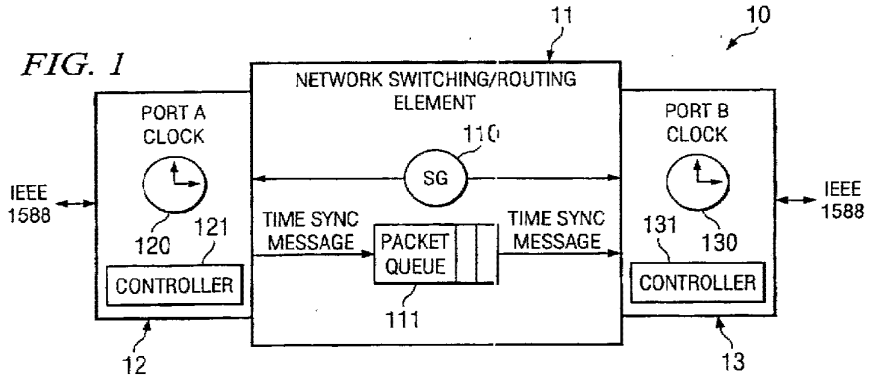
(56) Documents Cited:
GB 2418113 A **GB 2300789 A**
EP 1657619 A2 **US 5812749 A**
US 20040073718 A1

(58) Field of Search:
UK CL (Edition X) **H4P**
INT CL **G06F, H04J, H04L**
Other: **EPODOC, WPI**

(54) Abstract Title: **Network time synchronisation using a determination of network element transit times**

(57) By equipping receiving devices in a network with syncbronizable clocks it is possible to periodically send an "impulse" signal that is received by all of the clocks at the same (or relatively the same) instant of time. The accuracy of the impulse clock need not be high, only that its signal reach all the clocks approximately at the same time. In one embodiment, a transmitting device, upon receipt of the synchronizing impulse signal, sends a packet of data bearing the sending device's epoch time-stamp to a receiving device. The data packet makes its way through the network element to the receiving device and the time-stamp is used by the receiving device to calculate the difference between the epoch time of the receiver and the epoch time of the sender. Effectively, this procedure removes the unknown network element transit times from the equation and allows the devices to operate in a synchronized manner.

FIG. 1



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FIG. 1

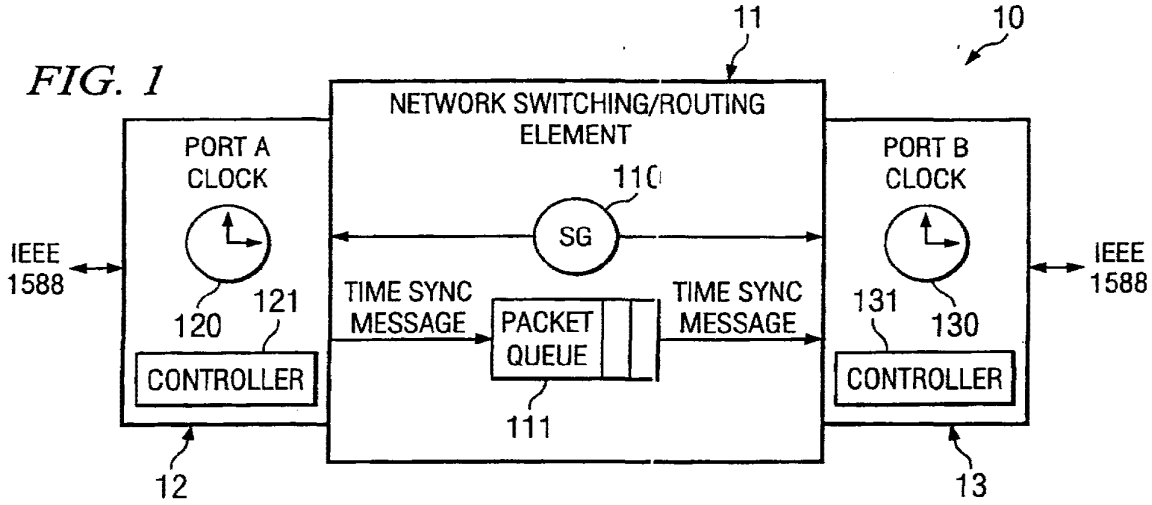


FIG. 2A

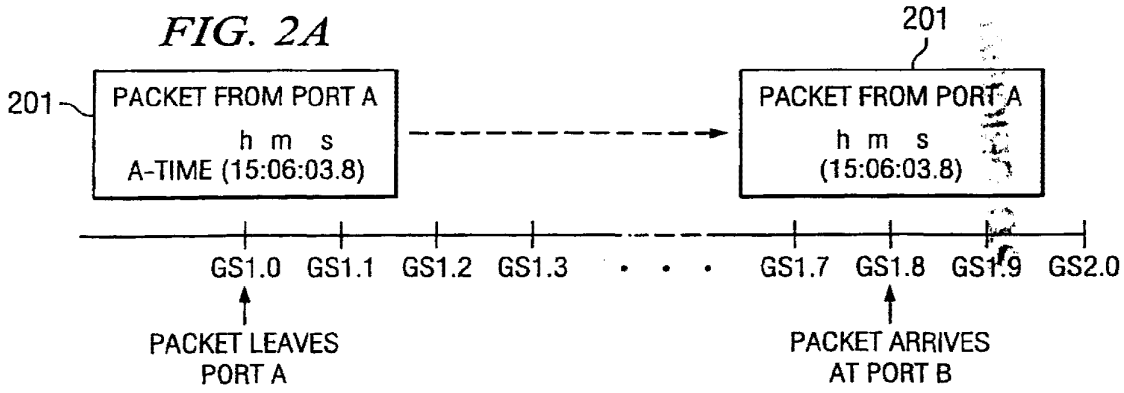


FIG. 2B

	h m s
ARRIVAL TIME (AS SEEN BY PORT B)	15:06:05.2
TRANSIT TIME (AS CALCULATED BY PORT B)	0.8
SENDING TIME (AS CALCULATED BY PORT B)	15:06:04.4
ACTUAL SENDING TIME (CONTAINED IN PACKET)	15:06:03.8
DIFFERENCE (AS CALCULATED BY PORT B)	+.6

FIG. 3A

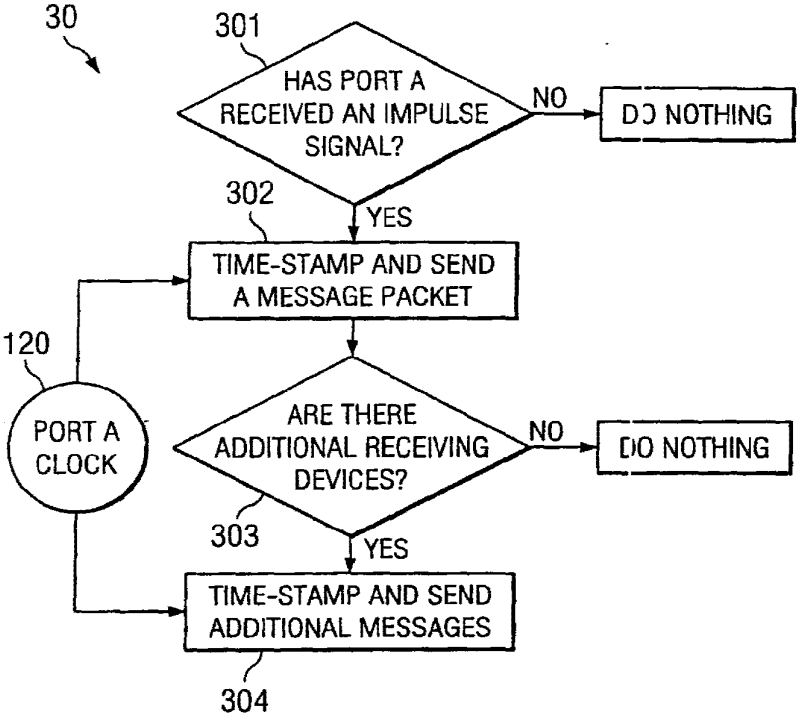
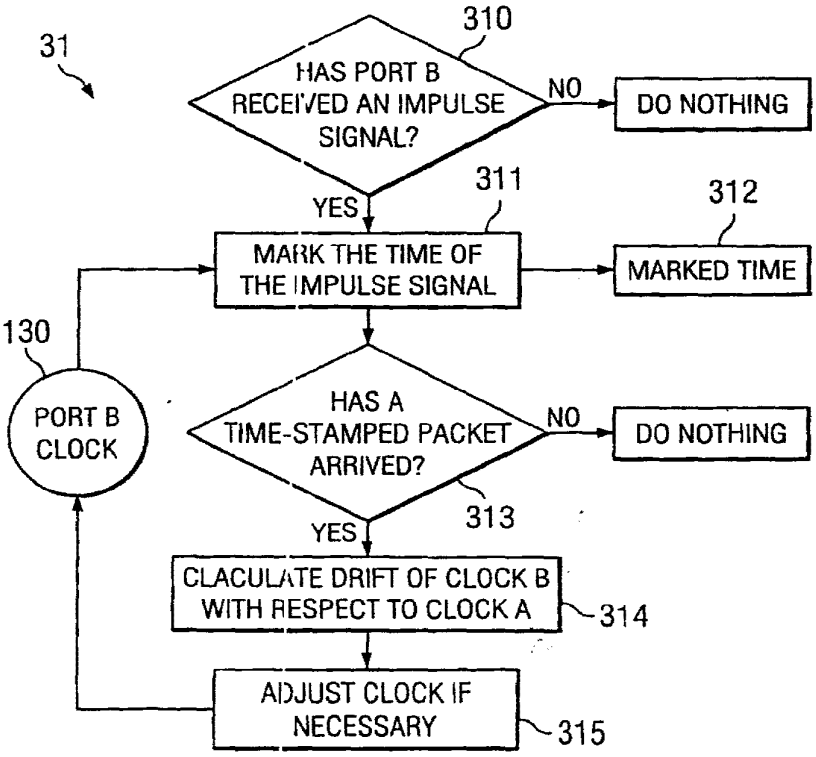

30
301
HAS PORT A RECEIVED AN IMPULSE SIGNAL?
NO
DO NOTHING
302
YES
TIME-STAMP AND SEND A MESSAGE PACKET
120
PORT A CLOCK
ARE THERE ADDITIONAL RECEIVING DEVICES?
NO
DO NOTHING
303
YES
TIME-STAMP AND SEND ADDITIONAL MESSAGES
304

FIG. 3B


31
310
HAS PORT B RECEIVED AN IMPULSE SIGNAL?
NO
DO NOTHING
YES
311
MARK THE TIME OF THE IMPULSE SIGNAL
312
MARKED TIME
130
PORT B CLOCK
HAS A TIME-STAMPED PACKET ARRIVED?
NO
DO NOTHING
313
YES
CLACULATE DRIFT OF CLOCK B WITH RESPECT TO CLOCK A
314
ADJUST CLOCK IF NECESSARY
315

SYSTEMS AND METHODS FOR SYNCHRONIZING TIME ACROSS NETWORKS

TECHNICAL FIELD

[0001] This invention relates to time synchronization and more particularly to systems and methods for synchronizing time across networks.

BACKGROUND OF THE INVENTION

[0002] Achieving time synchronization in computer networking environments is a challenging task. Different elements in a network, such as PCs/workstations/servers, routers/switches, and even VoIP phones, use NTP (Network Time Protocol), to get their epoch time for synchronization purposes. The accuracy of NTP time is in the order of tens of milliseconds. In many cases this is sufficient. In process automation, however, requirements are more rigid, and the requirement for time synchronization between networked devices is in the order of sub-microsecond accuracy.

[0003] This accuracy could be accomplished using the GPS system but the availability of the GPS signal is not assured at all locations due to the requirement of an antenna with a clear sight of the sky (to approximately 50 nsec.). In network performance measurement applications, where the one-way packet delay is measured, the accuracy has to be in the order of sub-milliseconds. Thus, deploying GPS at certain points of a network to perform network measurement is feasible except that, as discussed above, GPS signals are not available at all locations of the network.

[0004] In recent years the process automation industry has started deploying the IEEE 1588 standard to perform time synchronization between various devices. IEEE 1588 in its current form is limited to a very small network, typically a LAN segment. In order for IEEE 1588 to be deployed across wide area networks, significant investment in the network elements is required. For process automation there are a few companies that specialize in making switches that avoid delay in propagating the IEEE 1588 synchronization messages. However other manufactures, specifically router manufactures, find it economically difficult to deploy some of the solutions the IEEE 1588 standard proposes for dealing with queuing delays within the network elements.

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[0005] There are two methods in IEEE 1588 to avoid delays at the network switching routing elements. One method is to use a boundary clock and another is to utilize high priority messages. Using the boundary clock, some of the messages carry timestamps i.e., the epoch time of the devices that are trying to synchronize their clocks. This protocol works well if the communication between such devices is symmetrical with respect to delay.

[0006] A problem arises when the path becomes asymmetrical, as when switching/routing network elements add unpredictable delays. Under such a system, the sending device (device A) is a master clock and will synchronize device B's (receiver device) clock. To avoid queuing at the switch/router, the IEEE 1588 messages have to be diverted at the MAC/PHY layer. The boundary clock first synchronizes with the device A clock as a slave, and then device A clock becomes the master clock to device B, which will then synchronize it's clock to the boundary clock. This solution requires modification of the MAC/PHY chip as well as requiring a single clock to manage all possible ports. This could be done with some effort on a switch/router with bus architecture. However, doing this on a switch/router with crossbar architecture is, at best, challenging. Therefore for the foreseeable future it is doubtful if such changes will be implemented in the switching network because of complexity and cost. However, in situations, such as process automation where the cost of the switches is much higher (and the consumer's economic return is higher) than it is for the Internet, there may be freedom to implement these schemes, but in data networks synchronizing clocks remains a problem.

BRIEF SUMMARY OF THE INVENTION

[0007] By equipping receiving devices in a network with synchronizable clocks it is possible to periodically send an "impulse" signal that is received by all of the clocks at the same (or relatively the same) instant of time. The accuracy of the impulse clock need not be high, only that its signal reach all the clocks approximately at the same time. In one embodiment, a transmitting device, upon receipt of the synchronizing impulse signal, sends a packet of data bearing the sending device's epoch time-stamp to a receiving device. The data packet makes its way through the network to the receiving device and the time-stamp is used by the receiving device to calculate the difference between the epoch time of the receiver and the epoch time of the sender. Effectively, this procedure removes the unknown network transit times from the equation and allows the devices to operate in a synchronized manner.

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BRIEF DESCRIPTION OF THE DRAWING

[0008] FIGURE 1 shows one embodiment of the inventive concept having two device clocks that must be synchronized;

[0009] FIGURES 2A and 2B show an illustration of the calculations made for clock synchronization; and

[0010] FIGURES 3A and 3B show one embodiment of a process for establishing clock synchronization.

DETAILED DESCRIPTION OF THE INVENTION

[0011] FIGURE 1 shows one embodiment 10 of the inventive concept having two device clocks 120, 130 in devices 12 and 13, respectively, that are to be synchronized. It is assumed that clocks 120 and 130, as will be seen, are capable of receiving a sync signal, either via a wire, optically (either via air or in fiber), or wireless technologies of various frequencies/wave lengths and modulation schemes (such as, for example, 802.11, Bluetooth, TV RF), or via vibrations, such as impulses, etc. The sync (timing control) signal is not a signal that actually synchronizes the clocks directly as is done in GPS systems where the GPS sends an impulse every one second that is followed via a different channel (RS 232) with a value i.e., epoch time for alignment purposes, but rather the sync signal indicates that a specific event has occurred. Based on this specific event the clock to be synchronized will know how far it has wondered from the time of a system masters clock.

[0012] A Sync Generator (SG), such as SG 110, is used to provide the sync signal. SG 110 could be a part of switch/router element 11 or it could reside outside of the element. SG 110 signals an event periodically. The sync signal could be generated at each clock location based upon another event, such as a received signal and each clock then "counts" down from that signal and creates its own sync pulse.

[0013] Clocks 120 and 130 (and any other clocks to be synchronized) could either reside on a linecard of the router/switch or could be inside a Smart Gigabit Interface Converters (GBIC) or at any other location. The clocks outside the switch/router domain may synchronize with the rest of the world using IEEE 1588. Any switch/router port clock, for example, the master port clock could act as a SG. It should be noted that the SG could be one of the Smart

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GBIC clocks if the clocks that are to be synchronized are inside Smart GBICs. The SG could be an infrared strobe device that the clocks could receive via infrared receivers, or the impulse could be sound or vibration. The frequency of the SG signals will depend upon the synchronization accuracy desired, but as will be discussed, the stability of the SG itself is not an issue. In the switch/router implementation, the SG could be a backplane clock with its signal propagated to the switch/router ports. The frequency of the SG signal could be approximately 1 second but could be more often, if desired.

[0014] One key aspect is that all of the clocks associated with a specific switch/router must receive the SG signal at approximately the same instant. In some cases it is possible to permanently adjust (tune) the delay of the impulse so that it will arrive at all devices at the same time. However, some delays in propagation in the range of a few nanoseconds could be tolerated.

[0015] If desired, the system could be used as a distributed 1588 boundary clock arrangement since such device would have a low latency/low jitter short-distance communication path that sends 1-bit on a periodic basis. All receivers would be able to timestamp these "sync events". An important aspect of such a distribution system is that the communication path for the 1-bit impulse signal is low jitter. In such a system a remote 1588 master is directly connected via wire or fiber to the smart GBIC which is a slave to the remote master. The remote GBIC synchronizes its clock to the remote master using normal 1588 messages. The remote GBIC sees the sync event (impulse) and timestamps it. Because this clock is synced to the master, this timestamp is essentially the same value that the master would record if the master was close enough to also see the sync event. All local clocks that also see the sync event would generate a local timestamp with the assumption that the sync event is essentially simultaneously received by all local clocks (within the sync accuracy of concern). The slave GBIC then communicates its timestamp to all local clocks that also saw the same sync event. This communication can be high jitter and is assumed to go through the network element. All local clocks receiving this message can then adjust their local clock to track the slave GBIC.

[0016] In operation, as shown in FIGURE 1, let's assume that the port A (12) clock 120 is the master and must synchronize the port B (13) clock 130. The process begins by port A sending a time sync message (TSM) i.e., a message with port A's epoch time-stamp imbedded therein to port B. The time-stamp is put on and the message is sent immediately upon port A

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receiving the SG signal from SG source 110. The TSM could be delayed by the switch/router, for example, in packet queue 111, without causing difficulty because all the slave clocks, as will be seen, will "know" when the packet is sent and will know the epoch time of the sending port, because such time is carried by the TSM.

[0017] The packet sent with port A's time-stamp, for example, under control of controller (12), will be captured at port B (13), as well as at all other ports in which clocks are to be synchronized. Since port B knows when the packet started out (because it started when port A received the same SG signal as did port B) and since the packet has the time-stamp of port A on it, port B, upon receipt of the packet, can determine how far ahead (or behind) port B's clock is from port A's clock when the packet arrives at port B.

[0018] FIGURE 2A illustrates this such that packet 201 is sent from port A at port A's epoch time of, say, 15:06:03.8. It takes eight measures (in this case tenths of a second) to arrive at port B. When the TSM arrives, port B marks its own epoch time of, say 15:06:05.2.

[0019] FIGURE 2B shows the calculations made at port B, for example, by controller 131, FIGURE 1, to determine how far port B's clock is from port A's clock. Thus, as shown, the actual time of arrival of packet 201 is 15:06:05.2 as seen by clock 130 (port B). The transit time is 0.8 which is counted by port B (for example, by controller 131) from the SG signal which come to port B at the same instant it came to port A, which is the time the TMS was sent from port A. The sending time (as calculated by port B) is 15:06:04.4. The actual sending time (as contained in packet 201) is 15:06:03.8. Thus, port B can calculated that clock 130 at port B is running 0.6 faster than is clock 120 at port A.

[0020] Note that while it is anticipated that one packet be sent exactly when the SG signal arrives, it could be on any "tick" thereafter provided that the receiving port knows which tick it is sent on (this could be in the time code within the packet message if desired or could be a system requirement) and provided the message arrives before the next SG signal arrives at port B. Also note that messages could go out to different ports on different "ticks" again provided the receiving port knows which "tick" is being used.

[0021] In a situation when there are multiple slave clocks (multiple ports) port A would most likely send an individual message to each slave clock, since broadcasting or multicasting may not be possible if ports are on separate subnets.

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[0022] In the Smart SGBIC implementation, all SGBICs could be daisy chained via an external wire. A dedicated Smart GBIC could provide the SG signal as well as the master clock signal to all Smart GBICs by sending Time Sync Message as UDP packets.

[0023] In the situation where the SG is within the router/switch device, and the SGBICs are deployed in it's ports, structure for sending the sync pulse to the slave SGBICs is required. This could be achieved by sending the signal down one of the existing tracks on a normal GBIC/SFP socket. For instance, the signal loss output from the GBIC to the host is an open collector signal that is pulled up on the host board. When the GBIC indicates a signal loss condition, it lets the voltage level be pulled up by the resistor, creating logic 1. If the received signal is fine, the GBIC or SFP pulls the signal down to a low voltage to represent logic 0. If the host were to modulate the level of the voltage on the pull-up resistor, a suitable equipped S-GBIC could detect this modulation. However an unmodified GBIC or SFP would not detect this variation and the normal signal loss functionality would not be interfered with.

[0024] If the SG signal were to be thought of as an impulse then this "impulse" could be externally created or could be derived from statistical measurements of packets that are sent from the master to the slave(s). By synchronizing all clocks to the same frequency and phase using statistical measurements then impulses could be derived (for example one second impulses) that every port notices at the same time.

[0025] FIGURE 3A shows one embodiment 30 of a process at a master port for beginning synchronization. Process 301 waits for an SG impulse to be received. When the SG impulse signal is received, process 302, in conjunction with port A clock 120, time-stamps and sends a message packet to port B. Processes 303 and 304 send packets to other devices if required. These signals could be an sequential SG pulses or could be "offset" by a number of "focus" within the same SG pulse.

[0026] FIGURE 3B shows one embodiment 31 of a process at slave port B for finishing the synchronization. Process 310 waits for port B to receive an impulse signal. When such a signal has been received, process 311 marks the time, of the impulse signal as maintained by clock 130. This "time" is the epoch time of port B as now captured by process 312.

[0027] Process 313 determines when a time-stamped message has been received from the master-port and records the time of the arrival using its own epoch time. Then, as

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shown in FIGURE 2B, process 314 calculates the drift of clock B with respect to clock A. Process 305 makes any adjustment necessary to clock B to correct for the draft.

[0028] The accuracy of the synchronization depends upon the interval between the impulse signals and the receipt of a message with the time-stamp from port A. The slave clocks will each drift compared to the master with the rate of drift being controlled by its own nature. Since each slave clock adjusts its own drift after learning how much it has drifted. It is possible to make each clock adjustment individual to the port such that the adjustment might be made all at one time or over a period of time. The adjustment could be made using the rate of drift, as measured between SG impulses, to determine how much should be corrected at any one time. This eliminates the need for a big adjustment on any cycle.

[0029] Although the present invention and advantages thereof have been described in detail, it should be understood that various changes, substitutions and alterations can be made herein without departing from the spirit and scope of the invention as defined by the appended claims. Moreover, the scope of the present application is not intended to be limited to the particular embodiments of the process, machine, manufacture, composition of matter, means, methods and steps described in the specification. As one of ordinary skill in the art will readily appreciate from the disclosure of the present invention, processes, machines, manufacture, compositions of matter, means, methods, or steps, presently existing or later to be developed that perform substantially the same function or achieve substantially the same result as the corresponding embodiments described herein may be utilized according to the present invention. Accordingly, the appended claims are intended to include within their scope such processes, machines, manufacture, compositions of matter, means, methods, or steps.

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CLAIMS

What is claimed is:

1. A network synchronization system comprising:

network sending and receiving devices each adapted to receive a timing control signal at substantially the same time;

a controller at a sending device, said controller operable for placing a time-stamp on a message to be sent from said sending device to a receiving device through a network at a known fixed time in relation to receipt of said timing control signal, said time-stamp being the epoch time of said sending device; and

a controller at said receiving device operable for determining from a received one of said messages the difference between the epoch time of said receiving device and the epoch time of said sending device based upon said time-stamped epoch time and the transit time calculated from said known fixed time from receipt of said timing control signal at said receiving device.

2. The system of claim 1 wherein said known fixed time is immediately upon receipt of said time control signal by said sending device.

3. The system of claim 1 wherein said known fixed time is an offset from said receipt of said time control signal.

4. The system of claim 1 wherein said sending device sends a message to a plurality of receiving devices, each said message bearing a time-stamp of the epoch time of said sending device; and wherein each said message is sent at a different known offset from said receipt of said time control signal.

5. The system of claim 1 further comprising:

a clock at said receiving device; and

wherein said controller provides a drift calculation for adjusting the drift of said receiving device clock, said drift calculation based upon said determined epoch time difference.

6. The system of claim 1 wherein said timing control signal is transmitted to said clocks by a mechanism selected from the list consisting of:

wireless RF, cabled wiring, sound, vibration, and light.

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7. The system of claim 1 wherein said timing control signal is generated by a mechanism selected from the list comprising:

electronic counter, local oscillator, phase locked loop, frequency generator, and GPS receiver.

8. The system of claim 1 wherein said timing control signal is periodic.

9. The system of claim 8 wherein said period is one second.

10. A method for synchronizing clocks in spaced apart network elements, said method comprising:

sending an impulse to a plurality of said clocks, said impulse arriving at said clocks substantially at the same time;

upon receipt of said impulse at one of said clocks sending a message through a network device to at least one target clock, said message having the epoch time of said sending clock; and

calculating at said target clock, upon receipt of said message at a target clock using the epoch time of said sending clock, as contained in said time-stamp, the difference between the epoch time of said target clock and the epoch time of said sending clock.

11. The method of claim 10 wherein said calculating comprises:

comparing the epoch time of said target clock to the epoch time of said sending clock; and

adjusting for network transit time of said message bearing said time-stamp.

12. The method of claim 11 wherein said adjusting comprises:

counting the time elapsed from receipt of said impulse until the time said message arrives at said target clock.

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13. The method of claim 12 further comprising:

upon receipt of said impulse at said sending clock for also sending messages through said network device to a plurality of additional target clocks, each aid message having the epoch time of said sending clock; and

calculating at each of said additional target clocks, upon receipt of said message at said target clocks using the epoch time of said sending clock, as contained in said time-stamp, the difference between the epoch time of each said additional target clock and the epoch time of said sending clock.

14. The method of claim 12 wherein said timing control signal is transmitted to said clocks by a mechanism selected from the list consisting of:

wireless RF, cabled wiring, sound, vibration, and light.

15. The method of claim 12 wherein said timing control signal is generated by a mechanism selected from the list comprising:

electronic counter, local oscillator, phase locked loop, frequency generator, and GPS receiver.

16. The method of claim 11 wherein said timing control signal is periodic.

17. The method of claim 16 wherein said period is one second.

18. A port circuit for use in a network, said circuit comprising:

a controller for determining from a received time-stamped messages from a sending port the difference between the epoch time of said port and the epoch time of said sending port based upon said time-stamped epoch time and the transit time calculated from a known fixed time from receipt of a timing control signal received concurrently at both said port and said sending port.

19. The port circuit of claim 18 further comprising:

a clock having an drift; and wherein said controller further comprises;

means for adjusting said clock drift based upon said determined time difference.

20. The port circuit of claim 18 further comprising:

a clock; and wherein said controller further comprises:

means for synchronizing said clock with a clock in said sending port.

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21. A system for synchronizing clocks in separate ports of network elements, said system comprising:

means for sending an impulse to a plurality of said clocks, said impulse arriving at said clocks substantially at the same time;

means, operative upon receipt of said impulse at one of said clocks, for sending a message through a network to at least one target clock, said message having the epoch time of said sending clock; and

means for calculating at said target clock, upon receipt of said message at a target clock using the epoch time of said sending clock, as contained in said time-stamp, the difference between the epoch time of said target clock and the epoch time of said sending clock.

22. The system of claim 21 wherein said calculating means comprises:

means for comparing the epoch time of said target clock to the epoch time of said sending clock; and

means for adjusting for network transit time of said message bearing said time-stamp.

23. The system of claim 22 wherein said adjusting means comprises:

counting the time elapsed from receipt of said impulse until the time said message arrives at said target clock.

24. The system of claim 21 wherein said impulse generating means comprises, means for generating a signal from the list consisting of:

electronic counter, local oscillator, phase locked loop, frequency generator, and GPS receiver.

25. The system of claim 21 wherein said impulse is periodic.

26. A distributed boundary clock network comprising:

a master clock;

a plurality of other clocks;

a low-jitter communication path extending among said master clock and said other clocks;

means using 1558 messaging for synchronizing said master clock to one of said other clocks, said one other clock becoming a remote master clock; and

using said low-jitter communication path for distributing a sync signal to all said other clocks, including said remote master clock;

means at said remote master clock for sending a time-stamped message to said other clocks upon receipt of said sync signal; and

means at each said other clocks using said time-stamped message from said remote master clock and the time of said sync signal is received at said other clock for calculating the difference between said other clock and said remote master clock.

27. The distributed boundary clock network of claim 26 wherein said network comprises:

at least one Gigabit Interface Converter.

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Application No:	GB0607387.8	**Examiner:**	Joseph Wellings
Claims searched:	1-25	**Date of search:**	19 July 2006

Patents Act 1977: Search Report under Section 17

Documents considered to be relevant:

Category	Relevant to claims	Identity of document and passage or figure of particular relevance
A	-	GB 2300789 A (GEN DATACOMM)
A	-	EP 1657619 A2 (BOSCH)
A	-	US 2004/0073718 A1 (JOHANNESSEN)
A	-	US 5812749 A (FERNANDEZ)
A	-	GB 2418113 A (AGILENT)

Categories:

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
Y	Document indicating lack of inventive step if combined with one or more other documents of same category.	P	Document published on or after the declared priority date but before the filing date of this invention.
&	Member of the same patent family	E	Patent document published on or after, but with priority date earlier than, the filing date of this application.

Field of Search:

Search of GB, EP, WO & US patent documents classified in the following areas of the UKC^{X} :

H4P

Worldwide search of patent documents classified in the following areas of the IPC

G06F; H04J; H04L

The following online and other databases have been used in the preparation of this search report

EPODOC, WPI

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GB 2426164 A **US 8996906 B1**

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GB 2572463 B

Fig. 1

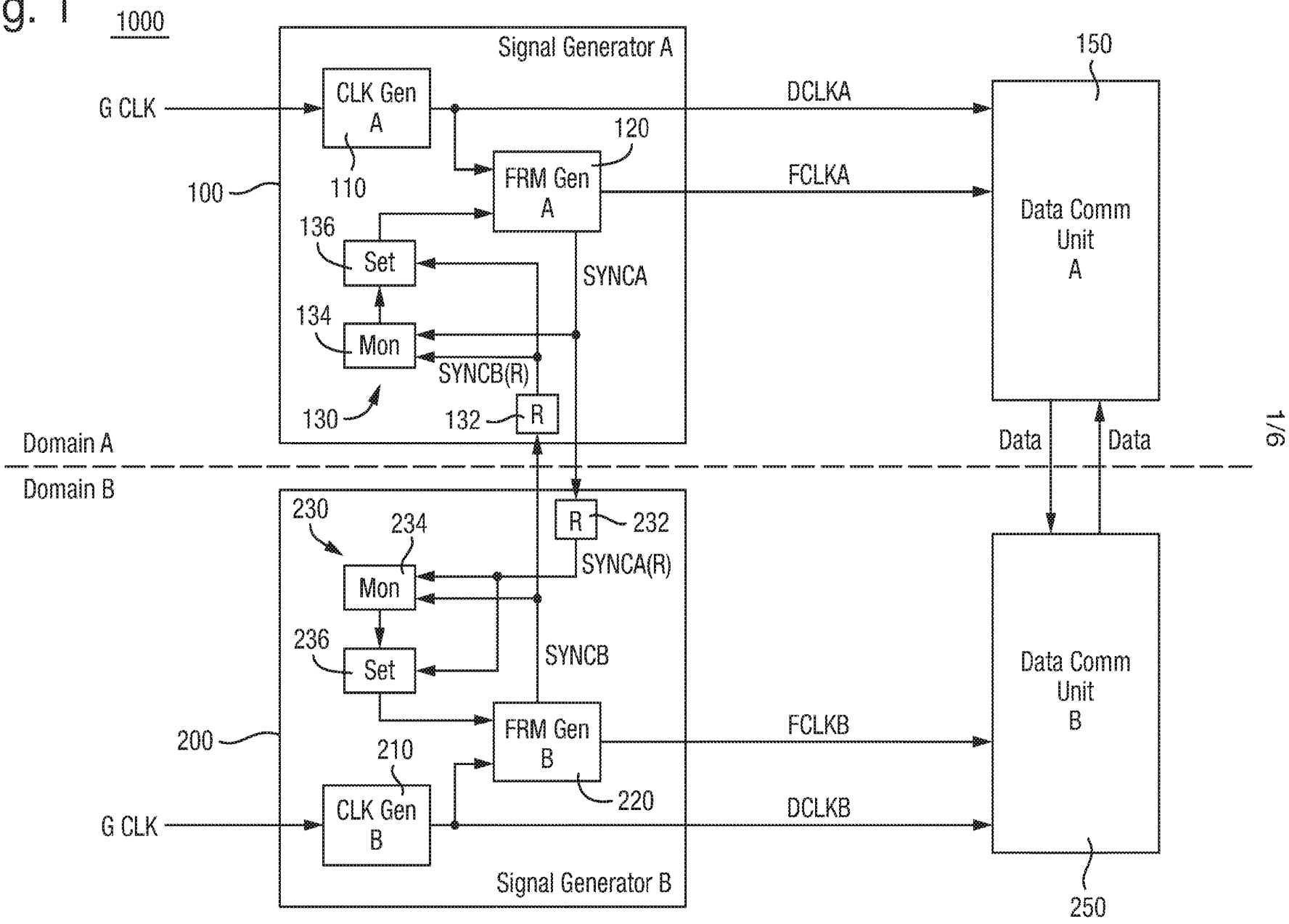

1000
Signal Generator A
CLK Gen A
G CLK
110
100
120
FRM Gen A
DCLKA
FCLKA
150
Data Comm Unit A
136
Set
SYNCA
134
Mon
SYNCB(R)
130
132
R
Domain A
Domain B
Data
Data
1/6
230
234
R
232
SYNCA(R)
Mon
236
Set
SYNCB
200
FRM Gen B
FCLKB
210
220
CLK Gen B
G CLK
DCLKB
Signal Generator B
Data Comm Unit B
250

Fig. 2

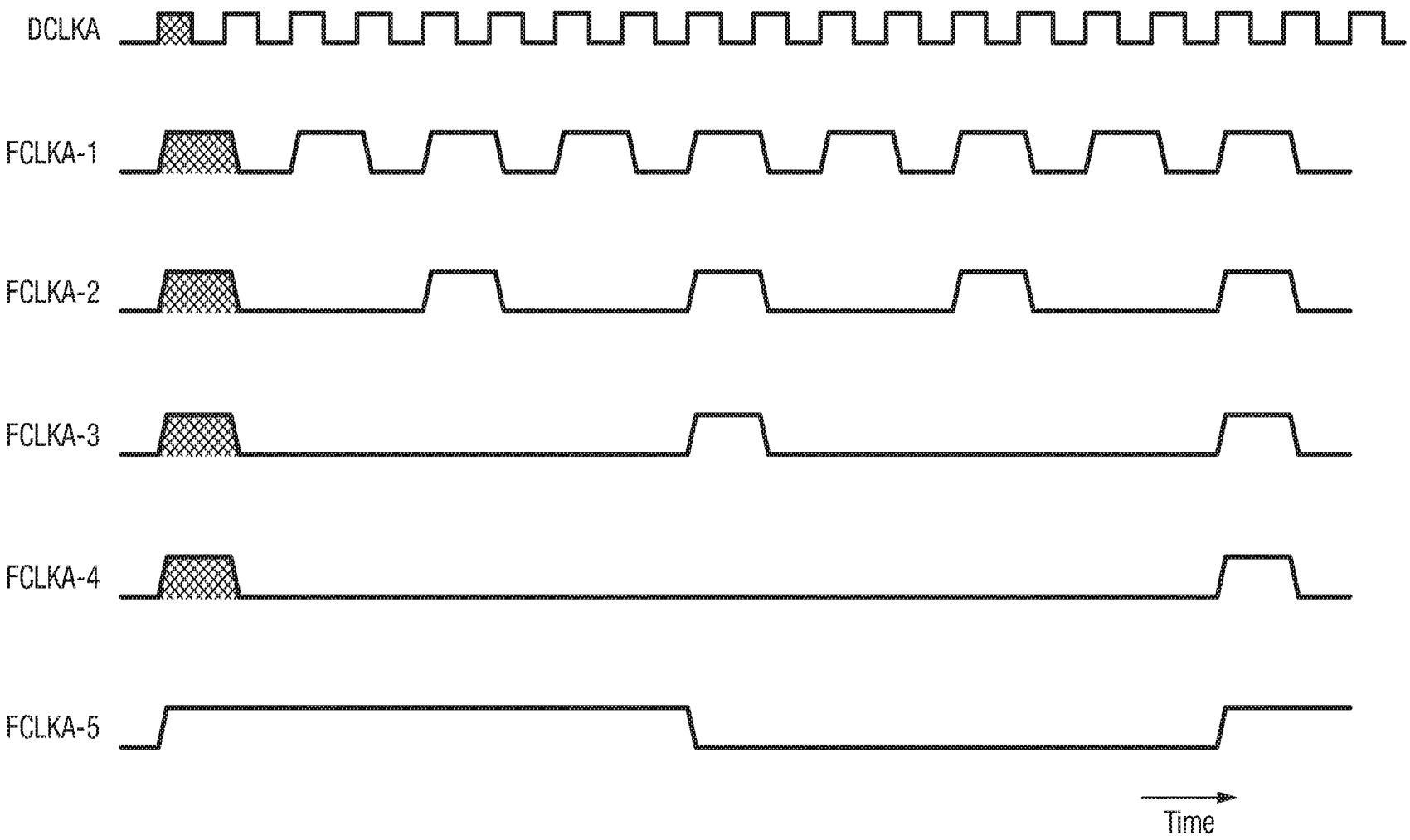
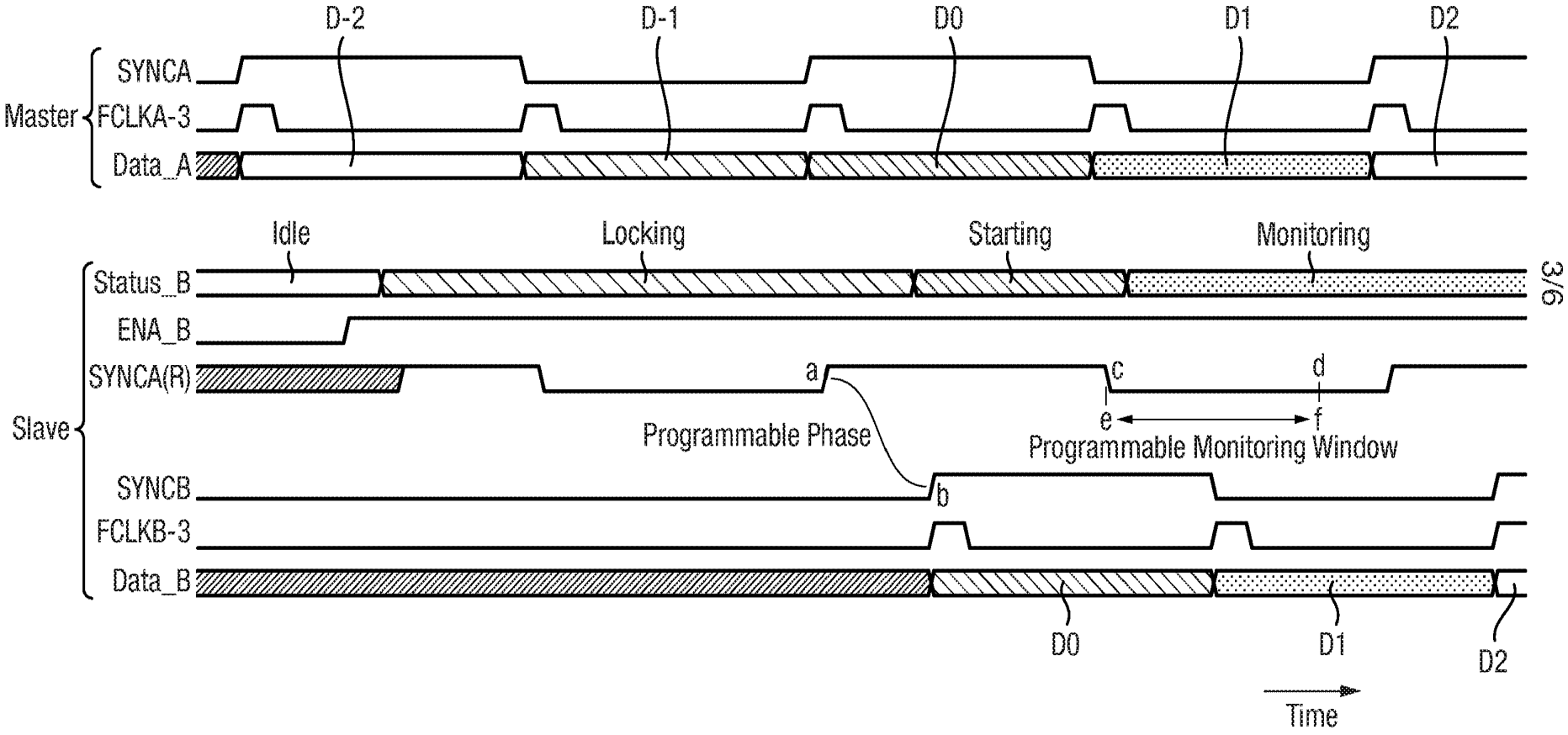
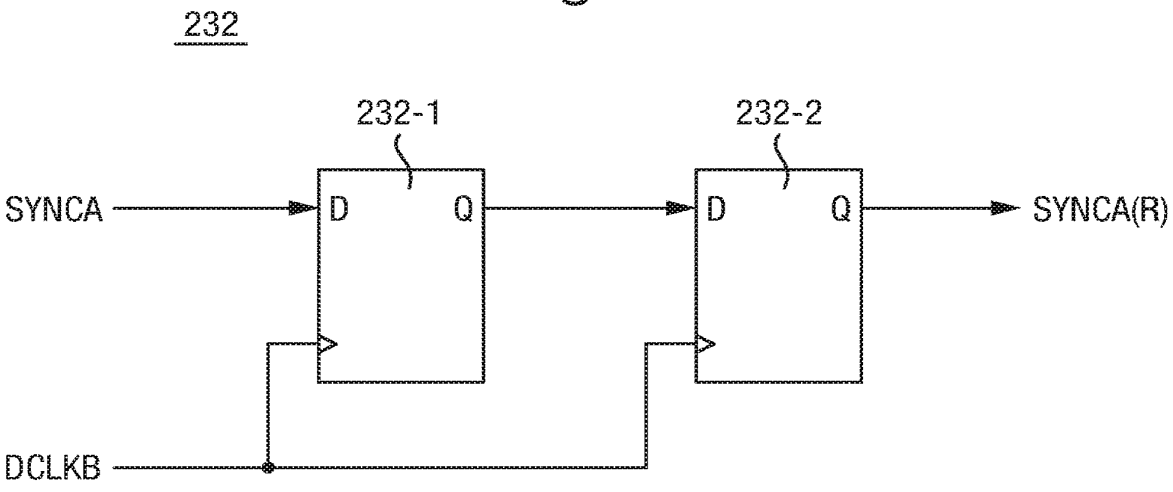


Fig. 3



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Fig. 4



25 10 18

Fig. 7

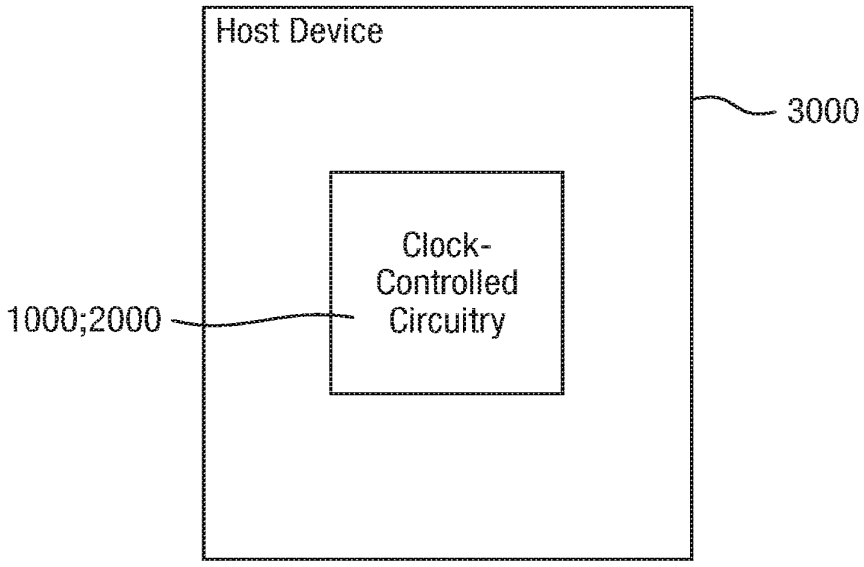
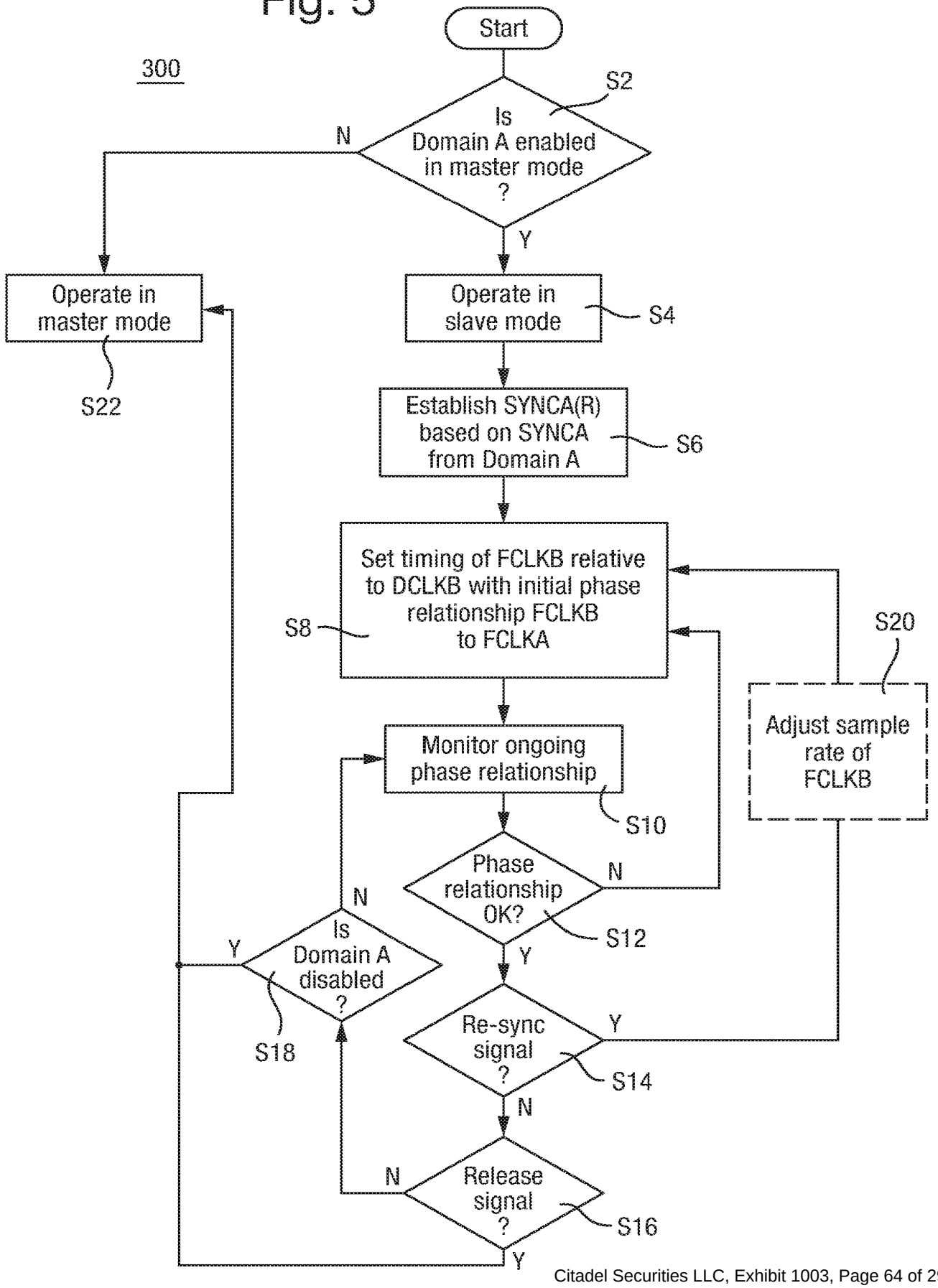


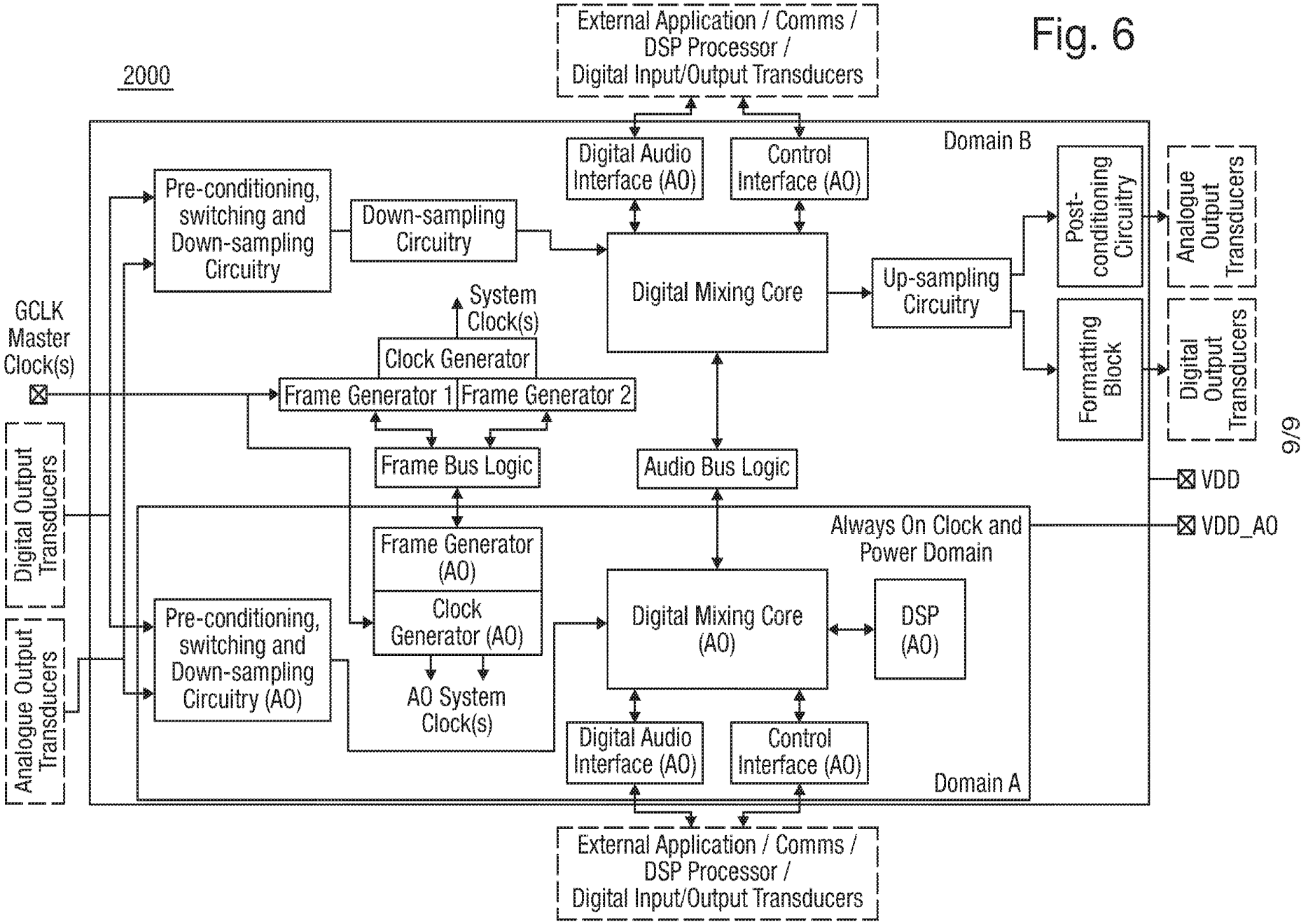
Fig. 5



25 10 18

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Fig. 6


2000
External Application / Comms / DSP Processor / Digital Input/Output Transducers
Domain B
Digital Audio Interface (A0)
Control Interface (A0)
Pre-conditioning, switching and Down-sampling Circuitry
Down-sampling Circuitry
Digital Mixing Core
Up-sampling Circuitry
Post-conditioning Circuitry
Analogue Output Transducers
Formatting Block
Digital Output Transducers
GCLK Master Clock(s)
System Clock(s)
Clock Generator
Frame Generator 1
Frame Generator 2
Frame Bus Logic
Audio Bus Logic
VDD
VDD_AO
Always On Clock and Power Domain
Digital Output Transducers
Analogue Output Transducers
Frame Generator (A0)
Clock Generator (A0)
Pre-conditioning, switching and Down-sampling Circuitry (A0)
A0 System Clock(s)
Digital Mixing Core (A0)
DSP (A0)
Digital Audio Interface (A0)
Control Interface (A0)
Domain A
External Application / Comms / DSP Processor / Digital Input/Output Transducers

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CLOCK-CONTROLLED CIRCUITRY

Technical Field

The present disclosure relates to clock-controlled circuitry, and in particular to the timing of signals between clock domains of such circuitry. Such timing may affect the transfer of data from one such domain to the other.

Background

Clock-controlled circuitry may be organised into a plurality of clock domains, where different clock domains operate based on their own clock signals. The clock signals of such different clock domains may be related in some way – for example, they may be derived ultimately from the same global or master clock signal. However, typically different clock domains have clock signals which have different frequencies and/or phases from one another, or phases and/or frequencies which are only nominally (e.g. to differing accuracies) the same. As such, a relationship between the clock signals of different clock domains may vary over time and may be unpredictable or unreliable. Such an architecture may be described in overview as a Global Asynchronous Locally Synchronous (GALS) architecture. One advantage of a GALS architecture may be that the overall amount of clock-tree balancing required may be reduced as compared to an architecture with only a single clock domain. Also, in a GALS architecture it may be possible to control which domains are on and which are off over time, with the domains then acting as power and clock domains.

Where data is transferred from one clock domain to another, timing between those domains can be important. Where the data is for example audio data, which may be packaged in frames and which may need to be handled in a time-critical manner (such as on a real-time basis), it may be desirable to minimize or reduce group delay or avoid audio artefacts related to clock domain crossing to improve end-user experience.

Clock-controlled circuitry naturally finds wide use. For example, most integrated circuits (ICs) use one or more clock signals to synchronise or otherwise control

different parts of system circuitry. Circuits operating based on clock signals may be considered synchronous circuits. Examples include processing circuits such as audio-processing circuits (which may handle data such as audio data).

Clock-controlled circuitry may therefore be implemented on ICs or systems within a host device, which may be considered an electrical or electronic device. Examples include a portable and/or battery powered host device such as a mobile telephone, an audio player, a video player, a PDA, a mobile computing platform such as a laptop computer or tablet and/or a games device.

Of course, audio data is merely one example type of data where timing issues can be important in relation to clock domain crossing. Other examples may include video or sensor/transducer (e.g. haptics) data. For convenience, however, the example of audio data will be carried forward herein.

Existing clock-controlled circuitry has been found to have shortcomings, in particular when data is passed or streamed from one clock domain to another. It is desirable to provide improved clock-controlled circuitry, in which data (such as audio data) may be transferred from one clock domain to another in an efficient manner.

Summary

According to a first aspect there is provided clock-controlled circuitry organised into at least first and second clock domains, the first clock domain configured to operate based on a first clock signal and the second clock domain configured to operate based on a second clock signal, wherein: the first clock domain comprises a first signal generator operable to generate a first repetitive signal synchronised to the first clock signal; the second clock domain comprises a second signal generator operable to generate a second repetitive signal synchronised to the second clock signal; the first signal generator is operable, when operating in master mode, to output to the second signal generator a first synchronisation signal indicative of a phase of the first repetitive signal; and the second signal generator is operable, when operating in slave mode, to: set a timing of the second repetitive signal relative to the second clock signal based on the first synchronisation signal so that the second repetitive signal is set to have a

phase relationship with the first repetitive signal which then meets a slave specification; and re-set the timing of the second repetitive signal relative to the second clock signal if it is determined that the phase relationship has changed such that it no longer meets the slave specification.

In this way, it is possible to keep the phase relationship within bounds defined by the slave specification, which can be advantageous where interrelated processes are defined by the first and second repetitive signals. For example, it may be that data transfer between the first and second clock domains is governed by the first and second repetitive signals, and in particular the relationship between them. By keeping the phase relationship within bounds defined by the slave specification, it may be that such data transfer can occur without significant errors and with reduced or minimised latency.

The slave specification may be or comprise one or more parameter values, which may define an allowable range of phase differences between the first and second repetitive signals. The slave specification may also define such a phase difference to be achieved when the timing of the second repetitive signal relative to the second clock signal is set.

The second signal generator may be operable to re-set the timing of the second repetitive signal relative to the second clock signal based on the first synchronisation signal so that the second repetitive signal is again set to have a phase relationship with the first repetitive signal which then meets the slave specification.

The second signal generator, or another signal generator of the clock-controlled circuitry, may be operable to monitor the phase relationship between the second repetitive signal and the first repetitive signal after the timing of the second repetitive signal relative to the second clock signal has been set and to determine if that phase relationship has changed such that it no longer meets the slave specification.

By (actively) monitoring the phase relationship, it is possible to detect when the phase relationship no longer meets the slave specification. The other signal generator may for

example be the first signal generator or a central signal generator (such as a control unit) other than the first and second signal generators.

The second signal generator or the other signal generator may be operable to monitor the phase relationship between the second repetitive signal and the first repetitive signal by monitoring a phase relationship between the second repetitive signal and the first synchronisation signal.

The second signal generator or the other signal generator may be operable to monitor the phase relationship between the second repetitive signal and the first repetitive signal by monitoring a phase relationship between the second repetitive signal and a retimed first synchronisation signal being a retimed version of the first synchronisation signal.

The second signal generator or the other signal generator may be operable to monitor the phase relationship between the second repetitive signal and the first repetitive signal by obtaining a count value indicative of the phase relationship by: incrementing a counter between corresponding edges of the second repetitive signal and the first synchronisation signal or retimed first synchronisation signal; or incrementing a counter while the second repetitive signal and the first synchronisation signal or retimed first synchronisation signal have the same value as one another; or incrementing a counter while the second repetitive signal and the first synchronisation signal or retimed first synchronisation signal have different values from one another.

The first synchronisation signal may be part or all of the first repetitive signal, or may be derived from the first repetitive signal. For example, the first repetitive signal may comprise a plurality of component repetitive signals, and the first synchronisation signal may be one of those repetitive signals.

The second signal generator may be operable when operating in slave mode, to receive a release signal, and, if the release signal is received, to transition its operation to free-running mode. The second signal generator may be operable in connection with the transition to free-running mode, to continue generation of the second repetitive signal at its existing timing relative to the second clock signal without taking account of

(i.e. without monitoring) the phase relationship between the second repetitive signal and the first repetitive signal.

The second signal generator may be operable, when operating in slave mode, to receive a re-synch signal indicating a change in the first repetitive signal, and, if the re-synch signal is received, to re-set the timing of the second repetitive signal relative to the second clock signal.

The re-synch signal may indicate a change in a repeating pattern of the first repetitive signal. In such a case, the second signal generator may be operable, if the re-synch signal is received, to re-set the timing of the second repetitive signal relative to the second clock signal based on the re-synch signal and re-configure the second repetitive signal based on the change in the repeating pattern indicated by the re-synch signal.

The second signal generator may be operable, when operating in slave mode, to monitor operation of the first signal generator, and, if the first signal generator is determined to become disabled (e.g. powered down or disconnected), to: transition its operation to master mode; and then continue generation of the second repetitive signal at its existing timing relative to the second clock signal without taking account of the phase relationship between the second repetitive signal and the first repetitive signal. The second signal generator may output a second synchronisation signal indicative of a phase of the second repetitive signal.

The first signal generator may be operable, when re-enabled after being disabled, to: monitor operation of the second signal generator and determine if the second clock control circuit is operating in master mode; and when it is determined that the second clock control circuit is operating in master mode, operate in slave mode.

The first signal generator may be operable, when operating in slave mode, to: set a timing of the first repetitive signal relative to the first clock signal based on the second synchronisation signal so that the first repetitive signal is set to have a phase relationship with the second repetitive signal which then meets the slave specification; and re-set the timing of the first repetitive signal relative to the first clock signal if it is

determined that that phase relationship has changed such that it no longer meets the slave specification.

The first signal generator may be operable to re-set the timing of the first repetitive signal relative to the first clock signal based on the second synchronisation signal so that the first repetitive signal is again set to have a phase relationship with the second repetitive signal which then meets the slave specification.

The first signal generator, or another signal generator of the clock-controlled circuitry, may be operable to monitor the phase relationship between the first repetitive signal and the second repetitive signal after the timing of the first repetitive signal relative to the first clock signal has been set and to determine if that phase relationship has changed such that it no longer meets the slave specification.

The first signal generator or that other signal generator may be operable to monitor the phase relationship between the first repetitive signal and the second repetitive signal by monitoring a phase relationship between the first repetitive signal and the second synchronisation signal.

The first signal generator or that other signal generator may be operable to monitor the phase relationship between the first repetitive signal and the second repetitive signal by monitoring a phase relationship between the first repetitive signal and a retimed second synchronisation signal being a retimed version of the second synchronisation signal.

The first signal generator or that other signal generator may be operable to monitor the phase relationship between the first repetitive signal and the second repetitive signal by obtaining a count value indicative of the phase relationship by: incrementing a counter between corresponding edges of the first repetitive signal and the second synchronisation signal or retimed second synchronisation signal; or incrementing a counter while the first repetitive signal and the second synchronisation signal or retimed second synchronisation signal have the same value as one another; or incrementing a counter while the first repetitive signal and the second synchronisation signal or retimed second synchronisation signal have different values from one another.

The second synchronisation signal may be part or all of the second repetitive signal, or may be derived from the second repetitive signal.

The first signal generator and second signal generator may be operable to generate the first and second clock signals, respectively, based on the same global clock signal. The first and second signal generators may be operable to generate the first and second clock signals with differing degrees of accuracy.

The first repetitive signal may comprise a plurality of different component repetitive signals synchronised with the first clock signal, and/or the second repetitive signal may comprise a plurality of different component repetitive signals synchronised with the second clock signal.

The clock-controlled circuitry may be organised into at least first and second power domains, wherein the first power domain comprises the first clock domain and the second power domain comprises the second clock domain. Such different power domains may be powered on or off (powered up or down, or in normal or low-power mode) independently of one another or at different times from one another.

The first and second power domains may be provided on different IC chips, or they could be provided on the same IC chip. The clock-controlled circuitry may comprise first and second IC chips. The first IC chip may comprise the first power domain and the second IC chip may comprise the second power domain.

The clock-controlled circuitry may comprise a first data communication unit in the first clock domain and configured to operate based on the first clock signal, and a second data communication unit in the second clock domain and configured to operate based on the second clock signal. The first data communication unit may be operable to process a first data signal which is synchronous with the first clock signal, based on the first repetitive signal. The second data communication unit may be configured to process a second data signal which is synchronous with the second clock signal, based on the second repetitive signal. The first and second communication units may be configured to transfer such a data signal between them based on their respective

first and second repetitive signals and via a retiming circuit so that the first data signal becomes the second data signal or *vice versa*.

The data signals may be audio data signals. The clock-controlled circuitry may be clock-controlled audio circuitry. The audio data signals may be organised into frames. The first and second data communication units may be configured to align the frames in their respective audio data signals with their respective repetitive signals.

The clock-controlled circuitry may comprise storage for storing information defining the slave specification. The first signal generator and/or the second signal generator may be configured to set the timing concerned based on the information. The determination that a said phase relationship has changed such that it no longer meets the slave specification may be made based on the information.

The information may comprise parameter values. The first signal generator and/or the second signal generator may be configured to set the timing concerned based on one or more of the parameter values. The determination that a said phase relationship has changed such that it no longer meets the slave specification may be made based on one or more of the parameter values.

The clock-controlled circuitry may comprise a controller operable to store the information in the storage so as to define the slave specification currently in use, optionally based on a user input.

According to a second aspect there is provided a method of controlling clock-controlled circuitry which is organised into at least first and second clock domains, the first clock domain configured to operate based on a first clock signal and the second clock domain configured to operate based on a second clock signal, wherein: the first clock domain comprises a first signal generator operable to generate a first repetitive signal synchronised to the first clock signal; the second clock domain comprises a second signal generator operable to generate a second repetitive signal synchronised to the second clock signal; and the first signal generator is operable, when operating in master mode, to output to the second signal generator a first synchronisation signal indicative of a phase of the first repetitive signal, the method comprising controlling the

second signal generator, when operating in slave mode, to: set a timing of the second repetitive signal relative to the second clock signal based on the first synchronisation signal so that the second repetitive signal is set to have a phase relationship with the first repetitive signal which then meets a slave specification; and re-set the timing of the second repetitive signal relative to the second clock signal if it is determined that the phase relationship has changed such that it no longer meets the slave specification.

According to a third aspect there is provided a computer program which, when executed on a processor of clock-controlled circuitry, causes the clock-controlled circuitry to carry out a control method, wherein: the clock-controlled circuitry is organised into at least first and second clock domains; the first clock domain is configured to operate based on a first clock signal and the second clock domain is configured to operate based on a second clock signal; the first clock domain comprises a first signal generator operable to generate a first repetitive signal synchronised to the first clock signal; the second clock domain comprises a second signal generator operable to generate a second repetitive signal synchronised to the second clock signal; and the first signal generator is operable, when operating in master mode, to output to the second signal generator a first synchronisation signal indicative of a phase of the first repetitive signal, the method comprising controlling the second signal generator, when operating in slave mode, to: set a timing of the second repetitive signal relative to the second clock signal based on the first synchronisation signal so that the second repetitive signal is set to have a phase relationship with the first repetitive signal which then meets a slave specification; and re-set the timing of the second repetitive signal relative to the second clock signal if it is determined that the phase relationship has changed such that it no longer meets the slave specification.

According to a fourth aspect there is provided a computer-readable medium having the computer program of the aforementioned third aspect stored thereon.

As apparent from the above, method aspects corresponding to the apparatus (circuitry) aspects are envisaged. Features of the apparatus aspects may thus have corresponding features in the method aspects. Computer program and storage medium aspects are also envisaged as apparent from the above, and similar comments apply. The present disclosure will be understood accordingly.

Brief Description of Drawings

Reference will now be made, by way of example, to the accompanying drawings, of which:

Figure 1 is a schematic diagram of clock-controlled circuitry embodying the present invention;

Figure 2 is a schematic diagram indicating example frame clock signals;

Figure 3 is a signal diagram useful for understanding operation of the Figure 1 circuitry;

Figure 4 is a schematic diagram of an example implementation of a retiming unit of Figure 1;

Figure 5 is a schematic diagram of a method which may be carried out by the clock-controlled circuitry of Figure 1;

Figure 6 is a schematic diagram of an example detailed implementation of clock-controlled circuitry which corresponds to the Figure 1 clock-controlled circuitry; and

Figure 7 is a schematic diagram of an electrical or electronic device in which the clock-controlled circuitry of Figure 1 or 6 may be deployed.

Detailed Description of Embodiments

Embodiments relate to clock-controlled circuitry and devices/apparatus comprising such circuitry. As will be apparent, such circuitry may find particular use as an IC SoC (System on Chip) in a host device. It will become apparent that circuitry disclosed herein is advantageous in that it enables data such as audio data to cross from one clock domain to another without significant associated power consumption, size/cost (e.g. IC chip area) impact, or delay/latency penalty.

Figure 1 is a schematic diagram of clock-controlled circuitry 1000 embodying the present invention. As indicated, circuitry 1000 is organised into first and second clock domains, denoted Domain A and Domain B, respectively. Thus, various elements and signals in Figure 1 are given the label "A" or "B" to indicate the clock domain which they are associated with. Those labels will however be omitted in the following description where possible for simplicity.

Domain A comprises a signal generator 100 and a data communication unit 150. Similarly, Domain B comprises a signal generator 200 and a data communication unit 250.

As depicted in Figure 1, the signal generators 100 and 200 are both capable of acting in a "master" or "slave" mode. For example, the signal generator 100 may operate in master mode and the signal generator 200 may operate in slave mode, in which case the timing of certain signals generated by the signal generator 200 may be (at least at some point in time) related to or dependent on the timing of certain signals generated by the signal generator 100. Similarly, the signal generator 200 may operate in master mode and the signal generator 100 may operate in slave mode, in which case the timing of certain signals generated by the signal generator 100 may be (at least at some point in time) related to or dependent on the timing of certain signals generated by the signal generator 200.

It will later be explained however that in some arrangements it may be that one of the signal generators 100 and 200 is only capable of operating in master mode, in which case certain elements depicted in Figure 1 need not be provided.

Signal generator 100 comprises a clock generator 110, a frame generator 120 and a relationship controller 130. The relationship controller 130 comprises a retiming unit 132, a monitoring unit 134 and a setting unit 136. Signal generator 200 comprises a clock generator 210, a frame generator 220 and a relationship controller 230. The relationship controller 230 comprises a retiming unit 232, a monitoring unit 234 and a setting unit 236.

The clock generators 110 and 210 operate generally in the same way as one another, in that they receive a common global clock signal GCLK and output respective domain clock signals DCLKA and DCLKB. The clock generators 110 and 210 may however differ from one another in some respects, for example in terms of their precision/accuracy. Thus, it may be that on average the frequencies of the domain clock signals DCLKA and DCLKB are the same as one another, or have some defined

relationship to one another, but that over time the relationship fluctuates. Of course, this is just an example.

The frame generators 120 and 220 also operate generally in the same way as one another, based on their respective domain clock signals DCLKA and DCLKB. Indeed, it will be appreciated that various elements in the clock domains (e.g. in the signal generators 100 and 200) will be controlled by the relevant domain clock signal, or a clock signal derived therefrom, for synchronous operation, however such connections are not shown explicitly to avoid overcomplicating Figure 1.

Focussing on the frame generator 120 by way of example, **Figure 2** is a schematic diagram indicating example frame clock signals FCLKA which the frame generator 120 may output.

In Figure 2, the domain clock signal DCLKA is presented at the top, followed by example frame clock signals FCLKA-1 to FCLKA-5. The frame generator 120 is configured to generate a repetitive signal which is synchronised to the domain clock signal DCLKA, and this repetitive signal could be considered to be FCLKA-1 to FCLKA-5 collectively or indeed any one or more of them. It will be understood that each of FCLKA-1 to FCLKA-5 is an example of a repetitive signal which is synchronised to the domain clock signal DCLKA, and that the number of them and indeed the particular repeating pattern exhibited by them may vary from arrangement to arrangement.

The signals FCLKA-1 to FCLKA-4 have the form of pulse signals, i.e. signals which comprise a regular series of pulses, with the pulse or sample rates differing from one to the next. Merely as examples, signals FCLKA-1 to FCLKA-4 may have 64kHz, 32kHz, 16kHz and 8kHz sample rates, respectively. In the context of audio data, these pulse signals may be considered strobe signals and may be used within their clock domain (i.e. by data communication unit 150) to facilitate routing or sample-rate converting of audio data while maintaining phase between channels.

The number of such strobe signals and their sample rates may for example be programmable or configurable, with the absolute periodicity and absolute time in generation dependent on the domain clock signal DCLKA.

The signal FCLKA-5 has the form of a toggle signal, and in this example toggles between high and low in line with the pulses of signal FCLKA-3. The repetitive signals may thus have the form of pulse signals or toggle signals, or indeed may exhibit any other repetitive pattern.

It will be assumed for convenience of explanation that DCLKB corresponds to DCLKA in that they both have the same nominal (average) frequency, both being generated from the global clock signal GCLK, and that the frame generator 220 generates frame clock signals FCLKB-1 to FCLKB-5 based on DLKCB which are nominally the same as FCLKA-1 to FCLKA-5, respectively. In other arrangements there may be more significant differences between DCLKA and DLKCB, and between the signal(s) which make up FCLKA and FCLKB.

In order to consider how the signal generators 100 and 200 may affect one another, it will be assumed for now that the signal generator 100 operates in master mode and that the signal generator 200 operates in slave mode.

The frame generator 120 outputs a synchronisation signal SYNCA to the signal generator 200. It will be assumed that the signal SYNCA is the same as the signal FLCKA-5, although it could be any other signal (such as another FCLKA signal in Figure 2) which is indicative of a phase of the Domain A frame clock signals FLCKA. The synchronisation signal SYNCA is indicative of a phase of the other frame clock signals FCLKA-1 to FCLKA-4, since it is synchronised with them (all are synchronised with DCLKA). The signals SYNCA and FCLKA-3 are shown as the upper two signals in the signal diagram of **Figure 3**. Each of the signal traces shown in Figure 3 may be considered to show the change in voltage level of the signal concerned over time.

The synchronisation signal SYNCA is received by the retiming unit 232 and retimed to be synchronous to the domain clock signal DCLKB to produce the retimed equivalent signal SYNCA(R). **Figure 4** is a schematic diagram of merely one simple example implementation of the retiming unit 232, in which it comprises a plurality of flip-flops 232-1 and 232-2 connected together in a chain as indicated, and clocked by the domain clock signal DCLKB (i.e. a clock signal of the receiving clock domain, Domain

B). The synchronisation signal SYNCA is received at the D input of the first flip-flop 232-1, the Q output of that flip-flop 232-1 is connected to the D input of the second flip-flop 232-2, and the retimed synchronisation signal SYNCA(R) is output from the Q output of the second flip-flop 232-2 synchronously with the domain clock signal DCLKB. This synchroniser structure is useful for avoiding metastability problems which may arise were only one flip-flop to be used.

Returning to Figure 1, the monitoring unit 234 is connected to receive the retimed signal SYNCA(R) and to control the setting unit 236 (which may also receive the retimed signal SYNCA(R) as shown) to initialise operation of the frame generator 220 based on the retimed signal SYNCA(R). In particular, the frame generator 220 is controlled to output its frame clock signal FCLKB (which is considered in this example to be composed of component frame clock signals FCLKB-1 to FCLKB-5) with a timing linked to the domain clock signal DCLKB such that the frame clock signal FCLKB is set at that time to have a phase relationship with the frame clock signal FCLKA (here, comprising component frame clock signals FCLKA-1 to FCLKA-5) which meets a slave specification. The slave specification may comprise one or more parameters, which may be configurable or programmable, and which define the desired phase relationship.

In more detail, looking at Figure 2, the frame generator 120 is controlled to output its frame clock signal FCLKA with a timing linked to the domain clock signal DCLKA as indicated by the highlighted pulses of the signals DCLKA and FCLKA. That is, the first pulses (highlighted) of the frame clock signals FCLKA-1 to FCLKA-4 and the first rising edge of the toggle signal FCLKA-5 are aligned with (linked to, or triggered by) the highlighted pulse of the signal DCLKA. The frame generator 120 is configured to continue generating the frame clock signal FCLKA with that timing relative to the domain clock signal DCLKA, e.g. by way of a counter triggered by the domain clock signal DCLKA, unless it is reset or its operation is adjusted in some way. The monitoring unit 234 and the setting unit 236 then control the frame generator 220 to link the frame clock signal FCLKB to the domain clock signal DCLKB in a similar way, but such that at that time a phase relationship (an initial phase relationship) between the frame clock signals FCLKA and FCLKB meets the slave specification. The frame generator 220 may then continue to produce the frame clock signals FCLKB to have

the relevant repeating pulse/toggle pattern using, for example, a counter triggered by the domain clock signal DCLKB.

This setting of the phase relationship between the frame clock signals FCLKA and FCLKB can be appreciated by further consideration of Figure 3. The frame generator 220 outputs a synchronisation signal SYNCB, which is assumed here to be the same as the signal FLCKB-5 for consistency with the corresponding synchronisation signal SYCNA. The synchronisation signal SYNCB is indicative of a phase of the other frame clock signals FCLKB-1 to FCLKB-4, since it is synchronised with them (all are synchronised with DCLKB). The signals SYNCB and FCLKB-3 are shown in Figure 3.

As indicated in Figure 3, once the retimed signal SYNCA(R) has been established, e.g. after the retiming unit 232 has been enabled and its operation has stabilised, the frame generator 220 is controlled, based on the retimed signal SYNCA(R), to output the signals SYNCB and FCLKB-3 (amongst others) so that there is a phase difference between corresponding edges of SYNCA(R) and SYNCB which meets the slave specification. This is indicated as being a "programmable phase" in Figure 3 as an example, since this initial phase relationship may be configured by way of a parameter - such as a delay between signal edges - defined in the slave specification.

Because the signal SYNCA(R) is a retimed version of the signal SYNCA, by setting an initial phase relationship between SYNCA(R) and SYNCB effectively an initial phase relationship is also set between SYNCA and SYNCB, and thus also between FCLKA and FCLKB. For example, as can be appreciated from Figure 3, an initial phase relationship is set between FCLKA-3 and FCLKB-3. It will become apparent that it is the relationship between signals FCLKA and FCLKB which affects how data is handled.

The monitoring unit 234 is connected to receive the signals SYNCA(R) and SYNCB as indicated in Figure 1. Based on these signals, and after the timing of the frame clock signal FCLKB has been set relative to the domain clock signal DCLKB as mentioned above, the monitoring unit 234 is configured to monitor the phase relationship between the signals SYNCB and SYNCA(R) (indicative of the relationship between SYNCB and

SYNCA) to determine if that phase relationship has changed such that it no longer meets the slave specification.

This could for example involve detecting whether an edge of the signal SYNCB is within a monitoring window of defined duration and positioned in time relative to the signal SYNCA(R). Such a window is indicated as being a "programmable monitoring window" in Figure 3 as an example, since the window may be configured again by way of a parameter - such as a range of acceptable delays between signal edges - defined in the slave specification. The programmable monitoring window in Figure 3 is defined as beginning at a falling edge of the signal SYNCA(R) and having a defined duration.

Looking at Figure 3, the status of the signal generator 200 is indicated by the signal STATUS_B (not shown in Figure 2). Firstly, the signal generator 200 is in an "idle" state until it is enabled by the rising edge of an enable signal ENA_B (also not shown in Figure 2). The status then becomes "locking" as the signal SYNCA(R) becomes established and the frame clock signal FCLKB is generated with the desired phase relationship set as mentioned above, and "starting" as data transfer across the domain boundary begins (as discussed in more detail below). The status then becomes "monitoring" as the phase relationship between the signals SYNCB and SYNCA(R) is monitored.

In the example in Figure 3, if the corresponding falling edge of the signal SYNCB falls within the programmable monitoring window as shown (the edge is depicted in Figure 3 falling approximately in the middle of the window), then it is determined that the phase relationship continues to meet the slave specification. In that case, the frame generator 220 is allowed to continue generating the frame clock signal FCLKB at its current timing relative to the domain clock signal DCLKB.

If, however, the corresponding falling edge of the signal SYNCB no longer falls within the programmable monitoring window then it is determined that the phase relationship no longer meets the slave specification. This could occur, for example, due to a temporary glitch or failure in e.g. any of the clock generators 110 and 210 and the frame generators 120 and 220 or due to a cosmic event (e.g. an ionizing particle strike). In that case, the monitoring unit 234 and setting unit 236 act to re-set the timing

of the frame clock signal FCLKB relative to the domain clock signal DCLKB (e.g. by reinitialising the frame generator 220, or by adjusting its operation) such that the frame clock signal FCLKB is again set at that time to have a phase relationship with the frame clock signal FCLKA which meets the slave specification.

In this way, the desired phase relationship between the frame clock signal FCLKB and the frame clock signal FCLKA can quickly (e.g. immediately) be re-established. Of course, if the phase relationship is continually monitored (e.g. every falling edge of SYNCB is checked, in the context of the Figure 3 example), then the desired phase relationship between the frame clock signal FCLKB and the frame clock signal FCLKA may be re-established if necessary very quickly. However, in some arrangements it may be acceptable to monitor the phase relationship intermittently, e.g. from time to time, such that the desired phase relationship may be re-established less quickly.

Looking again at Figure 3, when the desired phase relationship between the frame clock signal FCLKB and the frame clock signal FCLKA is established, a data signal DATA_A handled by the data communication unit 150 in Domain A can be transferred to the data communication unit 250 in Domain B as data signal DATA_B, with the frames (D0, D1, D2) of the data signal DATA_A being aligned with (controlled by) the signal FCLKA-3 and the corresponding (received) frames (D0, D1, D2) of the data signal DATA_B being aligned with (controlled by) the signal FCLKB-3. In this respect, it can be seen that the frame clock signals FCLKA and FCLKB may be used by the data communication units 150 and 250 to handle data signals, and in particular their alignment or phase relative to one another.

For example, in some audio applications latency may be of particular importance. For example, there may be relatively strict requirements to move e.g. PCM audio data from one system location to another in the minimal clock or frame cycles possible. This may be to help ensure that there are no notable lags for mobile telephony, contextual awareness or audio/sensor fusion. From Figure 3 it can be seen that the latency between the frame D0 in DATA_A and D0 in DATA_B is less than a single frame length, which constitutes relatively low latency.

As another example, in some audio applications the number of clock cycles per data frame may need to be consistent. In some synchronisation schemes it is acceptable for the frame size to be jittery in the destination clock domain but this may be undesirable or even unacceptable in audio applications in which there are audio converters or audio interfaces that require an exact number of system clocks (domain clock signal cycles) per data frame to ensure a correct audio signal transfer function or correct interfacing with other audio interfaces. The re-establishment of the phase relationship as described above may help ensure such consistency in clock cycles per data frame.

It is thus clear that if the phase relationship were not re-established in the event of a temporary glitch or failure as above, data (e.g. audio samples) could be dropped or repeated as data is transferred to/from either domain and/or other disadvantages as explained above may ensue.

The data communication units 150 and 250 may comprise processing, routing and/or conversion (e.g. digital-to-analogue, or *vice versa*) circuitry. The data communication units 150 and 250 may also be considered to encompass input and/or output transducers, which in the context of audio data may include *inter alia* microphones and speakers.

With the ability to quickly detect a phase relationship outside, or not meeting, the slave specification and re-establish the phase relationship in line with the slave specification as mentioned above, the data signal DATA_B may only suffer loss of one or just a few such frames as compared to the data signal DATA_A as the phase relationship is re-established, which in the context of audio data may be imperceptible to the end-user (e.g. listening to the audio via a speaker).

Another advantage of the present technique is that there is no need for a deep (large) FIFO buffer or similar between the two clock domains to buffer the data signal DATA_A as it crosses the domain boundary to become data signal DATA_B. As mentioned above, the initial phase difference between the signals SYNCA(R) and SYNCB (i.e. effectively between FCLKA and FCLKB), indicated in Figure 3 as a "programmable phase", may be configured so that simple sampling of the data signal DATA_A as it

crosses the clock domain boundary to become data signal DATA_B will be sufficient. For example, retiming circuitry (not shown) such as that described in relation to retiming units 132 and 232 (see the example in Figure 4) may be used.

Also as mentioned above, the size of the monitoring window, indicated in Figure 3 as a "programmable monitoring window", may be configured by way of the slave specification so that an expected range of fluctuation in the phase relationship may be tolerated, within the operational capability of the retiming/synchronising circuitry used to convert the data signal DATA_A to the data signal DATA_B as it crosses the clock domain boundary. The size of the monitoring window and the initial phase difference may be parameters defined in the slave specification.

It will be appreciated that in Figure 3 it is assumed that the direction of data transfer is from Domain A to Domain B, i.e. from data communication unit 150 to data communication unit 250, so that data signal DATA_A becomes data signal DATA_B. In this case, the initial phase difference may be set as in Figure 3 such that the signal SYNCA(R) leads SYNCB (i.e. effectively FCLKA leads FCLKB), allowing the data retiming/synchronising/sampling time to occur. Of course, in another arrangement (not shown in Figure 3) it may be that the direction of data transfer is from Domain B to Domain A, i.e. from data communication unit 250 to data communication unit 150, so that data signal DATA_B becomes data signal DATA_A. In this case, the initial phase difference may be set such that the signal SYNCA(R) lags SYNCB (i.e. effectively FCLKA lags FCLKB), again so that the data retiming/synchronising/sampling has time to occur. Such a situation may occur if there is already a data signal being handled in Domain A when a situation occurs where it is necessary to transfer another data signal from Domain B to Domain A.

The situation may also occur that it is necessary to simultaneously transfer one data signal from Domain A to Domain B, and another data signal from Domain B to Domain A. In that case it may be that multiple pairs of frame generators such as frame generators 120 and 220 are employed. As another example, where the signal generator 100 is operating in master mode and the signal generator 200 is operating in slave mode as described so far, it may be that the component frame clock signals making up frame clock signal FCLKB are organised so that, when the initial phase

difference is set such that the signal SYNCA(R) leads SYNCB (i.e. effectively FCLKA leads FCLKB) as in Figure 3, there is at least one component frame clock signal of FCLKB which is staggered relative to the others so that it appears to lead FCLKA.

Incidentally, although only one frame clock signal FCLKA-3 (and corresponding frame clock signal FCLKB-3) is shown in Figure 3, there may in fact be a plurality of frame clock signals used in each of the clock domains running at different sample/pulse rates (see e.g. Figure 2) with corresponding different data signals (e.g. audio data signals) running at those rates.

Where the signal generator 100 is operating in master mode and the signal generator 200 is operating in slave mode as described so far, it may be that the sample rate adopted in Domain A is changed on-the-fly, i.e. while the signal generator 200 has the "monitoring" status as in Figure 3 with the frame clock signals FCLKA and FCLKB already running with a phase relationship which meets the slave specification. Such a change in sample rate may change the frame clock signal FCLKA so that it is necessary to re-establish the phase relationship between the frame clock signals FCLKA and FCLKB, and potentially also change the format (e.g. sample rate) of the frame clock signal FCLKB. In this case, the signal generator 100 may be configured to send a re-synch signal (not shown) to the signal generator 200 to cause the phase relationship between the frame clock signals FCLKA and FCLKB to be re-established as mentioned above, and potentially to also cause the format (e.g. sample rate) of the frame clock signal FCLKB to be changed accordingly.

As another example, where the signal generator 100 is operating in master mode and the signal generator 200 is operating in slave mode, with the frame clock signals FCLKA and FCLKB already running with a phase relationship which meets the slave specification, it may be that it is no longer necessary for the frame clock signal FCLKB to be slaved (in the sense of continued monitoring) to the frame clock signal FLCKA. This may be indicated for example by a release signal (not shown) received in the signal generator 200 from the signal generator 100 or indeed from a separate control unit (not shown). In such a case, the signal generator 200 may be configured to cease the monitoring of the phase relationship and to allow the frame generator 220 to continue to generate the frame clock signal FCLKB with its current timing relative to the

domain clock signal DCLKB. In this respect, the signal generator 200 may be considered to have transitioned from slave mode to master mode or another free-running mode.

The signal generator 200 may also transition from slave mode to master mode if the signal generator 100 ceases operation for some reason, for example if it is disabled. The signal generator 200 may for example monitor an enable signal (not shown) for the signal generator 100 to determine that is has been disabled, or may for example determine that the signal generator 100 has been disabled if it no longer receives a signal from the signal generator 100 such as the synchronisation signal SYNCA. In such a case, the signal generator 200 may again be configured to cease the monitoring of the phase relationship and to allow the frame generator 220 to continue to generate the frame clock signal FCLKB with its current timing relative to the domain clock signal DCLKB. In this respect, the signal generator 200 may again be considered to have transitioned from slave mode to master mode.

So far, the case where the signal generator 100 is operating in master mode and the signal generator 200 is operating in slave mode has been considered, along with situations where the signal generator 200 may transition from slave mode to master mode. In these cases, it has not been necessary to consider the relationship controller 130, which comprises the retiming unit 132, monitoring unit 134 and setting unit 136. As such, if only such cases are needed the relationship controller 130 need not be provided.

However, it will be appreciated from the above, that there may arise the case where the signal generator 200 is operating in master mode (e.g. because the signal generator 100 has been disabled) and the signal generator 100 is then enabled (e.g. re-enabled).

One possibility is of course that the signal generator 100 starts up in master mode again, and that the signal generator 200 is returned to slave mode, with the phase relationship re-established by way of the relationship controller 230 as described above. However, this may be disadvantageous if a data signal is already being handled by the signal generator 200 with it operating in master mode, since the

retiming of the FCLKB signal(s) relative to the domain clock signal DCLKB may cause a glitch or other disruption in that data signal.

Another possibility is thus for the signal generator 100, which had previously been in master mode before it was disabled (or which had not yet been enabled), to be started up in slave mode. In that case, the relationship controller 130 may be employed analogously to how the relationship controller 230 is employed when the signal generator 200 is in slave mode as described above. This may be understood from Figure 3, but with the signals denoted with "A" swapped for the equivalent signals denoted with "B", and *vice versa*. The above description relating to the signal generator 100 operating in master mode and the signal generator 200 operating in slave mode, including the related transfer of data between the two domains, thus applies here *mutatis mutandis* but with the signal generator 200 operating in master mode and the signal generator 100 operating in slave mode.

For example, once the retimed signal SYNCB(R) has been established, e.g. after the retiming unit 132 has been enabled and its operation has stabilised, the frame generator 120 may be controlled, based on the retimed signal SYNCB(R), to output the signals SYNCA and FCLKA-3 (amongst others) so that there is a phase difference between corresponding edges of SYNCB(R) and SYNCA which meets the or another slave specification. As in Figure 1, the monitoring unit 134 is connected to receive the signals SYNCA(R) and SYNCB. Based on these signals, and after the timing of the frame clock signal FCLKA has been set relative to the domain clock signal DCLKA, the monitoring unit 134 may be configured to monitor the phase relationship between the signals SYNCA and SYNCB(R) (indicative of a relationship between SYNCB and SYNCA) to determine if that phase relationship has changed such that it no longer meets the slave specification concerned. If it is determined that the phase relationship no longer meets the slave specification, the monitoring unit 134 and setting unit 136 may then act to re-set the timing of the frame clock signal FCLKA relative to the domain clock signal DCLKA (e.g. by reinitialising the frame generator 120, or by adjusting its operation) such that the frame clock signal FCLKA is again set at that time to have a phase relationship with the frame clock signal FCLKB which meets the slave specification.

To allow this operation, the relationship controller 130 accordingly needs to be provided. In that case, the signal generators 100 and 200 may be considered to have the same general structure and function as one another.

Looking at the relationship controller 230, as a representative one of the relationship controllers 130 and 230, it will be appreciated that there are a number of ways in which to monitor the master-slave synchronicity, i.e. the phase relationship between the signals SYNCB and SYNCA(R) (effectively between SYNCB and SYNCA, or FCLKB and FCLKA).

For example, if the signals SYNCB and SYNCA(R) are toggle signals as in Figure 3, a counter (e.g. in the monitoring unit 234) can be started when SYNCB and SYNCA(R) are not equal and stopped when they are. If the count falls outside a programmable or configurable value range (whose size represents the size of the monitoring window) it can be determined that the monitoring window has been exceeded (in either direction) – i.e. the phase relationship no longer meets the slave specification. For example, the range may be represented by a single value, and a count value larger than that value (or corresponding to a negative value) may indicate that the monitoring window has been exceeded.

In another example, if the signals SYNCB and SYNCA(R) signals are pulse signals, for example being FCLKB-3 and FCLKA-3(R), where FCLKA-3(R) is a retimed version of FCLKA-3, a counter (e.g. in the monitoring unit 234) can be started on an edge-detection of FCLKA-3(R) and incremented until the corresponding FCLKB-3 edge is detected. Again if the count falls outside a programmable or configurable value range (whose size represents the size of the monitoring window) it can be determined that the monitoring window has been exceeded (in either direction) – i.e. the phase relationship no longer meets the slave specification.

As above, if the monitoring unit 234 determines that the phase relationship no longer meets the slave specification, then the setting unit 236 (which may be a finite state machine) is controlled to cause the frame generator 220 to re-establish the desired phase relationship. This can effectively occur by causing the frame generator 220 to generate the next SYNCB signal (and the related FCLKB signals) with the given phase

relationship ("programmable phase", in Figure 3) after the next appropriate edge of the SYNCA(R) signal, i.e. after the equivalent delay has elapsed.

In these examples, knowing which of the signals SYNCB and SYNCA(R) leads or lags relative to the other allows the associated hardware of the monitoring unit 234 to be minimised, especially if using a counter, as it does not then need to count up an entire frame of clock cycles.

Incidentally, in Figure 1 it has been assumed that the phase-relationship monitoring is carried out in the one of the signal generators 100 and 200 which is in slave mode. However, it would be possible for that monitoring to be carried out outside that signal generator, for example in the one of the signal generators 100 and 200 which is in master mode. For example, looking at Figure 3, when the signal generator 200 is in slave mode the monitoring could be carried out by the monitoring unit 134 using signals SYNCA and SYNCB(R), with the monitoring unit 134 then controlling the setting unit 236 or the frame generator 220 directly. Equally, in some arrangements the functionality of the monitoring and setting units could be provided outside the signal generators (e.g. in a common control unit).

Figure 5 is a schematic diagram of a method 300 which may be carried out by the clock-controlled circuitry 1000, for example by one of the signal generators 100 and 200. For consistency with Figure 3, method 300 as depicted in Figure 5 has been tailored specifically for operation by the signal generator 200 however it could equally be tailored for operation by the signal generator 100 by replacing references to Domain A and its elements with references to Domain B and its elements, and *vice versa*.

Method 300 comprises steps S2 to S22.

In step S2, it is determined whether Domain A (i.e. signal generator 100) is already enabled and in master mode, for example such that it is already generating frame clock signal FCLKA. This determination may be carried out by the signal generator 200 itself, for example based on a signal received from the signal generator 100. In such a case, the data communication unit 150 may already be handling a data signal based on frame clock signal FCLKA.

If signal generator 100 is already enabled and in master mode (S2, YES), the method proceeds to step S4. Otherwise (S2, NO), the method proceeds to step S22.

In step S4, the signal generator 200 determines that it should operate in slave mode and the method proceeds to step S6, in which the signal generator 200 establishes the retimed synchronisation signal SYNCA(R) based on SYNCA received from the signal generator 100.

The method then proceeds to step S8, in which the timing of the frame clock signal FCLKB is set relative to the domain clock signal DCLKB so that there is an initial phase relationship (defined by a slave specification) between the signals SYNCA(R) and SYNCB which translates to an acceptable initial phase relationship between the signals FCLKB and FCLKA.

The method then proceeds to step S10 in which the ongoing phase relationship is monitored. If the phase relationship continues to meet the slave specification (S12, YES), the method proceeds to step S14. Otherwise (S12, NO), the method returns to step S8 where the timing of the frame clock signal FCLKB is re-set relative to the domain clock signal DCLKB so that there is again an intended initial phase relationship (defined by a slave specification) between the signals SYNCA(R) and SYNCB.

In step S14, it is determined whether a re-synch signal has been received by the signal generator 200, for example from the signal generator 100. If a re-synch signal has been received (S14, YES), the method proceeds back to step S8, optionally via step S20 if it is necessary to adjust the sample rate or some other parameter of signal FCLKB based on the re-synch signal. If a re-synch signal has not been received (S14, NO), the method proceeds to step S16.

In step S16, it is determined whether a release signal has been received by the signal generator 200, for example from the signal generator 100. If it has (S14, YES), the method proceeds to step S22. If it has not (S16, NO), the method proceeds to step S18.

In step S18, it is determined whether Domain A (in particular, signal generator 100) has been disabled, for example based on a signal received (or no longer received) from the signal generator 100. If it has (S14, YES), the method proceeds to step S22. If it has not (S16, NO), the method returns to step S10.

In step S22 it is determined that the signal generator 200 of Domain B may operate in master mode, or in a similar free-running mode. In that case, the timing of the frame clock signal FCLKB is set (or is left set) relative to the domain clock signal DCLKB but without needing to consider (or monitor) any phase relationship between FCLKB and any signal from Domain A. The frame clock signal FCLKB may then continue to run with that timing relative to the domain clock signal DCLKB.

Although not shown in Figure 5, at any time the signal generator 200 may be disabled in which case the method 300 may terminate. It will be appreciated that the ordering of certain steps in method 300 is just an example. For example, steps S14 and S16 may occur between steps S8 and S10.

Of course, although only two clock domains are shown in Figure 1, there may be more than two clock domains with for example signal generator 100 operating in master mode and two or more signal generators (equivalent to signal generator 200 but in different clock domains) operating in slave mode in a master-slave relationship with signal generator 100. The present disclosure will be understood accordingly.

The different clock domains may be or be part of different power domains, so that the different domains may be powered on or off independently. For example, in the case of implementation in a host device such as a mobile telephone, it may be desirable to have one power domain operating as an “always on” domain which can react quickly to an external stimulus (such an audio signal picked up by a microphone), and another (e.g. central) power domain which is powered down unless it is “woken up” by the always on domain (perhaps via a higher-level application processor or the like). As another consideration, the different clock and/or power domains may be provided on the same IC chip or on different chips which are connected to one another.

It will be understood that, provided that the two (or more) clock generators share the same root, master or global clock signal (see GCLK in Figure 1) then, under programmatic control, one (or more) frame generator(s) can be slaved to the other frame generator such that their phase is guaranteed or controlled within the bounds of clock-domain-crossing and clock-jitter error. The global clock signal GCLK in Figure 1 may be used directly by the clock generators 110 and 210, or may be provided to them via a clock synthesis circuit such as a PLL (Phase Lock Loop).

By way of summary, in a possible arrangement the start-up of the slaved frame generator(s) is controlled to manage the phase relationship between itself and the master frame generator using a retimed version of a strobe or frame clock signal provided from the master frame generator as a synchronisation signal. Once started, the phase relationship is monitored e.g. in the slaved frame generator(s) to determine whether it moves unexpectedly, i.e. such that the slave specification is no longer met. If it does then the relevant slaved frame generator(s) is resynchronized automatically - re-establishing the master-slave phase relationship. If the master frame generator's sample rate is changed on-the-fly then the slave frame generator is again resynchronized automatically (e.g. on receipt of a re-synch signal). If the master frame generator is disabled the running slave frame generator may automatically become a master frame generator – i.e. no longer monitoring the master-slave phase relationship. If the original frame generator (which had been the master slave generator) is restarted it may by default be slaved to the new master frame generator. This has the benefit of avoiding unnecessary dropped or repeated samples on running data (e.g. audio) channels. At any time, a slaved frame generator may be set to free-run mode (e.g. on receipt of a release signal), i.e. no longer monitoring the master-slave phase relationship. This is akin to being set to master mode.

Figure 6 is a schematic diagram of an example detailed implementation of clock-controlled circuitry 2000 which corresponds to clock-controlled circuitry 1000, useful for better understanding a possible application of the circuitry disclosed herein.

Clock-controlled circuitry 2000 has the form of a SoC, i.e. and IC chip configured for audio processing. The circuitry 2000 is divided into an “always on” (AO) clock and power domain, labelled Domain A for comparison with Figure 1, and a central clock

and power domain, labelled Domain B again for comparison with Figure 1. External connections to input and/or output transducers are shown, along with power (VDD) connections, for both domains.

Both domains are shown having clock and frame generators, corresponding to those in Figure 1. The digital mixing core and DSP in the AO domain (along with the other circuitry in the data path(s) between transducers and e.g. the other domain and/or the external connection to an external application/comms/DSP processor) may thus correspond to the data communication unit 150 in Figure 1, and the digital mixing core in the central domain (along with the other circuitry in the data path between transducers and e.g. the other domain and/or the external connection to an external application/comms/DSP processor) may thus correspond to the data communication unit 250 in Figure 1.

In this regard, the frame generator in the AO domain (Domain A) may generate frame clock signals equivalent to FCLKA in Figure 1, and one or both of the frame generators in the central domain (Domain B) may generate frame clock signals equivalent to FCLKB in Figure 1, for use by the data communication units concerned.

Thus, one typical scenario may be that an audio data stream is first received from the relevant input transducer by the data communication unit circuitry in the AO domain (Domain A) with the frame generator in that domain thus operating in master mode. At that time, the central domain may be powered down, or in a low-power mode. The data may for example be routed to an external application processor via the external connection to the AO domain, which subsequently "wakes up" the central domain, i.e. transitions it into a powered-up or operational mode. Once powered up, one or both of the frame generators in the central domain (Domain B) may be slaved to the frame generator in the AO domain (Domain A), so that an audio data stream may be passed from the digital mixing core of the AO domain to that of the central domain without causing glitches or suffering significant latency. It will be appreciated that the functionality disclosed herein may help enable low latency transfer of such audio between domains, with reduced risk of audio artefacts or similar.

It will already be understood that clock-controlled circuitry considered herein may be implemented in a host device, for example an electrical or electronic device. Examples include a portable and/or battery powered host device such as a mobile telephone, an audio player, a video player, a PDA, a mobile computing platform such as a laptop computer or tablet and/or a games device, for example.

Figure 7 is a schematic diagram of an electrical or electronic device 3000, which may be considered such a host device. Device 3000 comprises clock-controlled circuitry 1000 or 2000 as considered earlier herein, connected to interact with other circuitry (not shown) of the electrical or electronic device 3000.

The skilled person will recognise that some aspects of the above described apparatus (circuitry) and methods may be embodied as processor control code, for example on a non-volatile carrier medium such as a disk, CD- or DVD-ROM, programmed memory such as read only memory (Firmware), or on a data carrier such as an optical or electrical signal carrier. For example, the configuration unit may be implemented as a processor operating based on processor control code.

For some applications, such aspects will be implemented on a DSP (Digital Signal Processor), ASIC (Application Specific Integrated Circuit) or FPGA (Field Programmable Gate Array). Thus the code may comprise conventional program code or microcode or, for example, code for setting up or controlling an ASIC or FPGA. The code may also comprise code for dynamically configuring re-configurable apparatus such as re-programmable logic gate arrays. Similarly, the code may comprise code for a hardware description language such as Verilog TM or VHDL. As the skilled person will appreciate, the code may be distributed between a plurality of coupled components in communication with one another. Where appropriate, such aspects may also be implemented using code running on a field-(re)programmable analogue array or similar device in order to configure analogue hardware.

Some embodiments of the present invention may be arranged as part of an audio processing circuit, for instance an audio circuit (such as a codec or the like) which may be provided in a host device as discussed above. A circuit or circuitry according to an embodiment of the present invention may be implemented as an integrated circuit (IC),

for example on an IC chip. One or more input or output transducers may be connected to the integrated circuit in use.

It should be noted that the above-mentioned embodiments illustrate rather than limit the invention, and that those skilled in the art will be able to design many alternative embodiments without departing from the scope of the appended claims. The word "comprising" does not exclude the presence of elements or steps other than those listed in the claim, "a" or "an" does not exclude a plurality, and a single feature or other unit may fulfil the functions of several units recited in the claims. Any reference numerals or labels in the claims shall not be construed so as to limit their scope.

CLAIMS:

1. Clock-controlled circuitry organised into at least first and second clock domains, the first clock domain configured to operate based on a first clock signal and the second clock domain configured to operate based on a second clock signal, wherein:

the first clock domain comprises a first signal generator operable to generate a first repetitive signal comprising a repeating pattern of pulses synchronised to the first clock signal;

the second clock domain comprises a second signal generator operable to generate a second repetitive signal comprising a repeating pattern of pulses synchronised to the second clock signal;

the first signal generator is operable, when operating in master mode, to output to the second signal generator a first synchronisation signal indicative of a phase of the first repetitive signal, wherein the first synchronisation signal is a pulse signal, and is part or all of the first repetitive signal or derived from the first repetitive signal; and

the second signal generator is operable, when operating in slave mode, to:

set a timing of the second repetitive signal relative to the second clock signal based on the first synchronisation signal so that the second repetitive signal is set to have a phase relationship with the first repetitive signal which then meets a slave specification; and

re-set the timing of the second repetitive signal relative to the second clock signal if it is determined that the phase relationship has changed such that it no longer meets the slave specification,

wherein the second signal generator, or another signal generator of the clock-controlled circuitry, is operable:

to monitor the phase relationship between the second repetitive signal and the first repetitive signal after the timing of the second repetitive signal relative to the second clock signal has been set, by monitoring a phase relationship between corresponding edges of the second repetitive signal and the first synchronisation signal or between corresponding edges of the second repetitive signal and a retimed first synchronisation signal being a retimed version of the first synchronisation signal; and

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to determine if that phase relationship has changed such that it no longer meets the slave specification.

2. The clock-controlled circuitry as claimed in claim 1, wherein the second signal generator is operable to re-set the timing of the second repetitive signal relative to the second clock signal based on the first synchronisation signal so that the second repetitive signal is again set to have a phase relationship with the first repetitive signal which then meets the slave specification.

3. The clock-controlled circuitry as claimed in claim 1 or 2, wherein the first and second repetitive signals comprise regular series of pulses.

4. The clock-controlled circuitry as claimed in any of the preceding claims, wherein the second signal generator or the other signal generator is operable to monitor the phase relationship between the second repetitive signal and the first repetitive signal by obtaining a count value indicative of the phase relationship by:

incrementing a counter between corresponding edges of the second repetitive signal and the first synchronisation signal or retimed first synchronisation signal; or

incrementing a counter while the second repetitive signal and the first synchronisation signal or retimed first synchronisation signal have the same value as one another; or

incrementing a counter while the second repetitive signal and the first synchronisation signal or retimed first synchronisation signal have different values from one another.

5. The clock-controlled circuitry as claimed in any of the preceding claims, wherein the second signal generator is operable:

when operating in slave mode, to receive a release signal, and, if the release signal is received, to transition its operation to free-running mode; and

in connection with the transition to free-running mode, to continue generation of the second repetitive signal at its existing timing relative to the second clock signal without taking account of the phase relationship between the second repetitive signal and the first repetitive signal.

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6. The clock-controlled circuitry as claimed in any of the preceding claims, wherein the second signal generator is operable:

when operating in slave mode, to receive a re-synch signal indicating a change in the first repetitive signal, and, if the re-synch signal is received, to re-set the timing of the second repetitive signal relative to the second clock signal.

7. The clock-controlled circuitry as claimed in claim 6, wherein:

the re-synch signal indicates a change in a repeating pattern of the first repetitive signal; and

the second signal generator is operable, if the re-synch signal is received, to re-set the timing of the second repetitive signal relative to the second clock signal based on the re-synch signal and re-configure the second repetitive signal based on the change in the repeating pattern indicated by the re-synch signal.

8. The clock-controlled circuitry as claimed in any of the preceding claims, wherein the second signal generator is operable, when operating in slave mode, to monitor operation of the first signal generator, and, if the first signal generator is determined to become disabled, to:

transition its operation to master mode; and then

continue generation of the second repetitive signal at its existing timing relative to the second clock signal without taking account of the phase relationship between the second repetitive signal and the first repetitive signal, and output a second synchronisation signal indicative of a phase of the second repetitive signal.

9. The clock-controlled circuitry as claimed in claim 8, wherein the first signal generator is operable, when re-enabled after being disabled, to:

monitor operation of the second signal generator and determine if the second clock control circuit is operating in master mode; and

when it is determined that the second clock control circuit is operating in master mode, operate in slave mode.

10. The clock-controlled circuitry as claimed in claim 9, wherein the first signal generator is operable, when operating in slave mode, to:

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set a timing of the first repetitive signal relative to the first clock signal based on the second synchronisation signal so that the first repetitive signal is set to have a phase relationship with the second repetitive signal which then meets the slave specification; and

re-set the timing of the first repetitive signal relative to the first clock signal if it is determined that that phase relationship has changed such that it no longer meets the slave specification.

11. The clock-controlled circuitry as claimed in claim 10, wherein the first signal generator is operable to re-set the timing of the first repetitive signal relative to the first clock signal based on the second synchronisation signal so that the first repetitive signal is again set to have a phase relationship with the second repetitive signal which then meets the slave specification.

12. The clock-controlled circuitry as claimed in claim 10 or 11, wherein the first signal generator, or another signal generator of the clock-controlled circuitry, is operable to monitor the phase relationship between the first repetitive signal and the second repetitive signal after the timing of the first repetitive signal relative to the first clock signal has been set and to determine if that phase relationship has changed such that it no longer meets the slave specification.

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13. The clock-controlled circuitry as claimed in claim 12, wherein the first signal generator or that other signal generator is operable to monitor the phase relationship between the first repetitive signal and the second repetitive signal by monitoring a phase relationship between the first repetitive signal and the second synchronisation signal.

14. The clock-controlled circuitry as claimed in claim 12 or 13, wherein the first signal generator or that other signal generator is operable to monitor the phase relationship between the first repetitive signal and the second repetitive signal by monitoring a phase relationship between the first repetitive signal and a retimed second synchronisation signal being a retimed version of the second synchronisation signal.

15. The clock-controlled circuitry as claimed in claim 13 or 14, wherein the first signal generator or that other signal generator is operable to monitor the phase relationship between the first repetitive signal and the second repetitive signal by obtaining a count value indicative of the phase relationship by:

incrementing a counter between corresponding edges of the first repetitive signal and the second synchronisation signal or retimed second synchronisation signal; or

incrementing a counter while the first repetitive signal and the second synchronisation signal or retimed second synchronisation signal have the same value as one another; or

incrementing a counter while the first repetitive signal and the second synchronisation signal or retimed second synchronisation signal have different values from one another.

16. The clock-controlled circuitry as claimed in any of claims 8 to 15, wherein the second synchronisation signal is part or all of the second repetitive signal, or is derived from the second repetitive signal.

17. The clock-controlled circuitry as claimed in any of the preceding claims, wherein the first signal generator and second signal generator are operable to generate the first and second clock signals, respectively, based on the same global clock signal.

18. The clock-controlled circuitry as claimed in any of the preceding claims, wherein the first repetitive signal comprises a plurality of different component repetitive signals synchronised with the first clock signal, and/or the second repetitive signal comprises a plurality of different component repetitive signals synchronised with the second clock signal.

19. The clock-controlled circuitry as claimed in any of the preceding claims, organised into at least first and second power domains, wherein the first power domain comprises the first clock domain and the second power domain comprises the second clock domain.

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20. The clock-controlled circuitry as claimed in claim 19, comprising first and second IC chips, wherein the first IC chip comprises the first power domain and the second IC chip comprises the second power domain.

21. The clock-controlled circuitry as claimed in any of the preceding claims, comprising a first data communication unit in the first clock domain and configured to operate based on the first clock signal, and a second data communication unit in the second clock domain and configured to operate based on the second clock signal, wherein:

the first data communication unit is operable to process a first data signal which is synchronous with the first clock signal, based on the first repetitive signal;

the second data communication unit is configured to process a second data signal which is synchronous with the second clock signal, based on the second repetitive signal; and

the first and second communication units are configured to transfer such a data signal between them based on their respective first and second repetitive signals and via a retiming circuit so that the first data signal becomes the second data signal or *vice versa*.

22. The clock-controlled circuitry as claimed in claim 21, wherein the data signals are audio data signals, and wherein the clock-controlled circuitry is clock-controlled audio circuitry.

23. The clock-controlled circuitry as claimed in claim 22, wherein the audio data signals are organised into frames, and wherein the first and second data communication units are configured to align the frames in their respective audio data signals with their respective repetitive signals.

24. The clock-controlled circuitry as claimed in any of the preceding claims, comprising storage for storing information defining the slave specification, wherein:

the first signal generator and/or the second signal generator is configured to set the timing concerned based on the information; and/or

the determination that a said phase relationship has changed such that it no longer meets the slave specification is made based on the information.

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25. The clock-controlled circuitry as claimed in claim 24, wherein the information comprises parameter values, and wherein

the first signal generator and/or the second signal generator is configured to set the timing concerned based on one or more of the parameter values; and/or

the determination that a said phase relationship has changed such that it no longer meets the slave specification is made based on one or more of the parameter values.

26. The clock-controlled circuitry as claimed in claim 24 or 25, comprising a controller operable to store the information in the storage so as to define the slave specification currently in use, optionally based on a user input.

27. The clock-controlled circuitry as claimed in any of the preceding claims, implemented as an integrated circuit.

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28. A method of controlling clock-controlled circuitry which is organised into at least first and second clock domains, the first clock domain configured to operate based on a first clock signal and the second clock domain configured to operate based on a second clock signal, wherein:

the first clock domain comprises a first signal generator operable to generate a first repetitive signal comprising a repeating pattern of pulses synchronised to the first clock signal;

the second clock domain comprises a second signal generator operable to generate a second repetitive signal comprising a repeating pattern of pulses synchronised to the second clock signal; and

the first signal generator is operable, when operating in master mode, to output to the second signal generator a first synchronisation signal indicative of a phase of the first repetitive signal, wherein the first synchronisation signal is a pulse signal, and is part or all of the first repetitive signal or derived from the first repetitive signal,

the method comprising controlling the second signal generator, when operating in slave mode, to:

set a timing of the second repetitive signal relative to the second clock signal based on the first synchronisation signal so that the second repetitive

signal is set to have a phase relationship with the first repetitive signal which then meets a slave specification; and

re-set the timing of the second repetitive signal relative to the second clock signal if it is determined that the phase relationship has changed such that it no longer meets the slave specification,

wherein the second signal generator, or another signal generator of the clock-controlled circuitry, is operable:

to monitor the phase relationship between the second repetitive signal and the first repetitive signal after the timing of the second repetitive signal relative to the second clock signal has been set, by monitoring a phase relationship between corresponding edges of the second repetitive signal and the first synchronisation signal or between corresponding edges of the second repetitive signal and a retimed first synchronisation signal being a retimed version of the first synchronisation signal; and

to determine if that phase relationship has changed such that it no longer meets the slave specification.

29. A computer program which, when executed on a processor of clock-controlled circuitry, causes the clock-controlled circuitry to carry out a control method,

wherein:

the clock-controlled circuitry is organised into at least first and second clock domains;

the first clock domain is configured to operate based on a first clock signal and the second clock domain is configured to operate based on a second clock signal;

the first clock domain comprises a first signal generator operable to generate a first repetitive signal comprising a repeating pattern of pulses synchronised to the first clock signal;

the second clock domain comprises a second signal generator operable to generate a second repetitive signal comprising a repeating pattern of pulses synchronised to the second clock signal; and

the first signal generator is operable, when operating in master mode, to output to the second signal generator a first synchronisation signal indicative of a phase of the first repetitive signal, wherein the first synchronisation signal is a pulse signal, and is part or all of the first repetitive signal or derived from the first repetitive signal,

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the method comprising controlling the second signal generator, when operating in slave mode, to:

set a timing of the second repetitive signal relative to the second clock signal based on the first synchronisation signal so that the second repetitive signal is set to have a phase relationship with the first repetitive signal which then meets a slave specification; and

re-set the timing of the second repetitive signal relative to the second clock signal if it is determined that the phase relationship has changed such that it no longer meets the slave specification,

wherein the second signal generator, or another signal generator of the clock-controlled circuitry, is operable:

to monitor the phase relationship between the second repetitive signal and the first repetitive signal after the timing of the second repetitive signal relative to the second clock signal has been set, by monitoring a phase relationship between corresponding edges of the second repetitive signal and the first synchronisation signal or between corresponding edges of the second repetitive signal and a retimed first synchronisation signal being a retimed version of the first synchronisation signal; and

to determine if that phase relationship has changed such that it no longer meets the slave specification.

30. A computer-readable medium having the computer program of claim 29 stored thereon.

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Electronic Patent Application Fee Transmittal

Application Number:	17723145
Filing Date:	18-Apr-2022
Title of Invention:	FIELD PROGRAMMABLE GATE ARRAY WITH EXTERNAL PHASE-LOCKED LOOP
First Named Inventor/Applicant Name:	Nima Badizadegan
Filer:	Keith J. Barkaus/Victoria Gilmore
Attorney Docket Number:	00287-0017

Filed as Small Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
SUBMISSION- INFORMATION DISCLOSURE STMT	2806	1	130	130
		Total in USD ($)		**130**

Electronic Acknowledgement Receipt

EFS ID:	46744973
Application Number:	17723145
International Application Number:	
Confirmation Number:	1635
Title of Invention:	FIELD PROGRAMMABLE GATE ARRAY WITH EXTERNAL PHASE-LOCKED LOOP
First Named Inventor/Applicant Name:	Nima Badizadegan
Customer Number:	1912
Filer:	Keith J. Barkaus/Victoria Gilmore
Filer Authorized By:	Keith J. Barkaus
Attorney Docket Number:	00287-0017
Receipt Date:	03-OCT-2022
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Time Stamp:	17:39:06
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1912 7590 09/22/2022

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EXAMINER	
CHENG, DIANA	
ART UNIT	PAPER NUMBER
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DATE MAILED: 09/22/2022

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/723,145	04/18/2022	Nima Badizadegan	00287-0017	1635

TITLE OF INVENTION: FIELD PROGRAMMABLE GATE ARRAY WITH EXTERNAL PHASE-LOCKED LOOP

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	$600	$0.00	$0.00	$600	12/22/2022

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Citadel Securities LLC, Exhibit 1003, Page 110 of 290

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1912 7590 09/22/2022

AMSTER, ROTHSTEIN & EBENSTEIN LLP
90 PARK AVENUE
NEW YORK, NY 10016

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via EFS-Web or by facsimile to (571) 273-2885, on the date below.

(Typed or printed name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/723,145	04/18/2022	Nima Badizadegan	00287-0017	1635

TITLE OF INVENTION: FIELD PROGRAMMABLE GATE ARRAY WITH EXTERNAL PHASE-LOCKED LOOP

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	$600	$0.00	$0.00	$600	12/22/2022

EXAMINER	ART UNIT	CLASS-SUBCLASS
CHENG, DIANA	2849	327-156000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/AIA/122 or PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/AIA/47 or PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. Fees submitted: ❑Issue Fee ❑Publication Fee (if required) ❑Advance Order - # of Copies _____

4b. Method of Payment: *(Please first reapply any previously paid fee shown above)*

❑ Electronic Payment via EFS-Web ❑ Enclosed check ❑ Non-electronic payment by credit card (Attach form PTO-2038)

❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. _____

5. **Change in Entity Status** (from status indicated above)

❑ Applicant certifying micro entity status. See 37 CFR 1.29

❑ Applicant asserting small entity status. See 37 CFR 1.27

❑ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/723,145	04/18/2022	Nima Badizadegan	00287-0017	1635

1912 7590 09/22/2022

AMSTER, ROTHSTEIN & EBENSTEIN LLP
90 PARK AVENUE
NEW YORK, NY 10016

EXAMINER	
CHENG, DIANA	
ART UNIT	PAPER NUMBER
2849	

DATE MAILED: 09/22/2022

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Citadel Securities LLC, Exhibit 1003, Page 112 of 290

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 17/723,145	Applicant(s) Badizadegan, Nima	
	Examiner Diana J Cheng	Art Unit 2849	AIA (FITF) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☑ This communication is responsive to Terminal Disclaimer 09/16/2022.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☑ The allowed claim(s) is/are 1-12 . As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see **http://www.uspto.gov/patents/init_events/pph/index.jsp** or send an inquiry to **PPHfeedback@uspto.gov.**

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some* c) ☐ None of the:

   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____ .

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____ .

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____.
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material _____.
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date. _____.
5. ☐ Examiner's Amendment/Comment
6. ☑ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/DIANA J. CHENG/
Primary Examiner, Art Unit 2849

DETAILED ACTION

Notice of Pre-AIA or AIA Status

The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

Allowable Subject Matter

Claims 1-12 are allowed.

The following is an examiner's statement of reasons for allowance:

Regarding Claim 1, the prior art does not disclose, teach or suggest a method for processing a first serial data stream, using a field programmable gate array system, to generate a second serial data stream, wherein the method comprises the steps of:

(f) transmitting, from the deserializer to a phase lock loop of the field programmable gate array system that is not within on the field programmable gate array, the receiver side clock signal;

(g) generating, using the phase lock loop, a second clock signal;

(h) generating, within the field programmable gate array, a transmitter side clock signal derived from the second clock signal;

(i) performing, by the computational circuitry, a set of operations on at least a portion of the first plurality of parallel data streams to generate a second plurality of parallel data streams; and

(j) transmitting, from the field programmable gate array system, the second serial data stream, derived from the second plurality of parallel data streams, wherein said

method does not use clock domain crossing operations that delay processing of the first set of parallel data streams;

in combination with all the other claimed limitations.

Claims 2-12 are allowed for depending from Claim 1.

.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Diana J Cheng whose telephone number is (571)270-1197. The examiner can normally be reached Monday - Friday 9 am - 5:30 pm ET.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Menatoallah Youssef can be reached on (571)270-3684. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of published or unpublished applications may be obtained from Patent Center. Unpublished application information in Patent Center is available to registered users. To file and manage patent submissions in Patent Center, visit: https://patentcenter.uspto.gov. Visit https://www.uspto.gov/patents/apply/patent-center for more information about Patent Center and https://www.uspto.gov/patents/docx for information about filing in DOCX format. For additional questions, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/DIANA J. CHENG/
Primary Examiner, Art Unit 2849

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/723,145	Badizadegan, Nima
	Examiner	Art Unit
	Diana J Cheng	2849

CPC - Searched*		
Symbol	**Date**	**Examiner**
H03L7/085,087,089,0891,0893,0895,0896,0898,091,093,095	09/02/2022	DJC
G06F30/30,34,343,347	09/02/2022	DJC
G06F1/04,08 H04J3/0658 H03L2207/50	09/02/2022	DJC

CPC Combination Sets - Searched*		
Symbol	**Date**	**Examiner**

US Classification - Searched*			
Class	**Subclass**	**Date**	**Examiner**

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	**Date**	**Examiner**
Double Patenting and Prior Art Search	09/02/2022	DJC
Refreshed Search	09/12/2022	DJC
Refreshed Search	09/19/2022	DJC
Interference Search	09/19/2022	DJC

Interference Search			
US Class/CPC Symbol	**US Subclass/CPC Group**	**Date**	**Examiner**
See Search History		09/19/2022	DJC

Citadel Securities LLC, Exhibit 1003, Page 118 of 290

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/723,145	Badizadegan, Nima
	Examiner	**Art Unit**
	Diana J Cheng	2849

Citadel Securities LLC, Exhibit 1003, Page 119 of 290

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/723,145	Badizadegan, Nima
	Examiner	**Art Unit**
	Diana J Cheng	2849

CPC						
Symbol					**Type**	**Version**
H03L	/	7	/	085	F	2013-01-01
G06F	/	1	/	08	I	2013-01-01
G06F	/	30	/	34	I	2020-01-01
H04J	/	3	/	0658	I	2013-01-01
H03L	/	2207	/	50	A	2013-01-01

CPC Combination Sets							
Symbol					**Type**	**Set**	**Ranking**	**Version**
	/		/					

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	12	
/DIANA J. CHENG/ Primary Examiner, Art Unit 2849	19 September 2022	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	2

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/723,145	Badizadegan, Nima
	Examiner	**Art Unit**
	Diana J Cheng	2849

INTERNATIONAL CLASSIFICATION				
CLAIMED				
H03L7/085	/	7	/	085
G06F1/08	/	1	/	08
G06F30/34	/	30	/	34
H04J3/06	/	3	/	06

NON-CLAIMED				
	/		/	

US ORIGINAL CLASSIFICATION	
CLASS	**SUBCLASS**

CROSS REFERENCES(S)						
CLASS	**SUBCLASS (ONE SUBCLASS PER BLOCK)**					

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	12	
/DIANA J. CHENG/ Primary Examiner, Art Unit 2849	19 September 2022	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	2

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/723,145	Badizadegan, Nima
	Examiner	**Art Unit**
	Diana J Cheng	2849

☑ Claims renumbered in the same order as presented by applicant ☐ CPA ☑ T.D. ☐ R.1.47

CLAIMS

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	12	
/DIANA J. CHENG/ Primary Examiner, Art Unit 2849	19 September 2022	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	2

U.S. Patent and Trademark Office Part of Paper No.: 20220919

Bibliographic Data

Application No: 17/723,145

Foreign Priority claimed: ○ Yes ◉ No

35 USC 119 (a-d) conditions met: ☐ Yes ☑ No ☐ Met After Allowance

Verified and Acknowledged: /DIANA J. CHENG/ Examiner's Signature | Initials

Title: FIELD PROGRAMMABLE GATE ARRAY WITH EXTERNAL PHASE-LOCKED LOOP

FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
04/18/2022	327	2849	00287-0017
RULE			

APPLICANTS

HFT Solutions, LLC, New Canaan, CT, UNITED STATES

INVENTORS

Nima Badizadegan, Salem, NH, UNITED STATES

CONTINUING DATA

This application is a CON of 17405188 08/18/2021

17405188 is a CON of 17248304 01/19/2021 PAT 11128305

17248304 is a CON of 16937314 07/23/2020 PAT 10931286

16937314 is a CON of 16672076 11/01/2019 PAT 10826502

16672076 has PRO of 62803017 02/08/2019

16672076 has PRO of 62755804 11/05/2018

FOREIGN APPLICATIONS

IF REQUIRED, FOREIGN LICENSE GRANTED**

04/21/2022

** SMALL ENTITY **

STATE OR COUNTRY

UNITED STATES

ADDRESS

AMSTER, ROTHSTEIN & EBENSTEIN LLP
90 PARK AVENUE
NEW YORK, NY 10016
UNITED STATES

FILING FEE RECEIVED

$3,000

PE2E SEARCH - Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	British Equivalents	Time Stamp
L169	7	((("BADIZADEGAN") near3 ("Nima"))).INV.	(US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT)	OR	ON	ON	2022/09/19 03:16 PM
L170	0	(fpga near tranceiver) and (deserializ$4) and ((gate data) near array) and serializ$4	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/19 03:16 PM
L171	11	tranceiver and (deserializ$4) and ((gate data) near array) and serializ$4	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/19 03:16 PM
L172	649	(deserializ$4) and ((gate data) near array) and (phase near detect$4) and serializ$4	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/19 03:16 PM
L173	616	fpga and L60	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/19 03:16 PM
L174	13	fpga and (deserializ$4) and ((gate data) near array) and (phase near detect$4) and ((adjustable variable) near oscillat$4) and serializ$4	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/19 03:16 PM
L175	9	(fpga near transceiver) and (deserializ$4) and ((gate data) near array) and (phase near detect$4) and ((adjustable variable) near oscillat$4) and serializ$4	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/19 03:16 PM
L176	61	(fpga near transceiver) and (deserializ$4) and ((gate data) near array) and serializ$4	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/19 03:16 PM
L177	239	transceiver near bank	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/19 03:16 PM
L178	27	(("9330740") or ("9001951") or ("10411720") or ("8675306") or ("20190025413")).PN.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/09/19 03:16 PM
L179	23	(("10037568") or ("10169814") or ("4068188") or	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	OFF	OFF	2022/09/19 03:16 PM

		("4745372") or ("8467418")).PN.	IBM_TDB)				
L180	25267	(H03L7/085,087,089,0891,0893,0895,0896,0898,091,093,095).cpc.	(US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT)	OR	ON	ON	2022/09/19 03:16 PM
L181	12329	(G06F30/30,34,343,347).cpc.	(US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT)	OR	ON	ON	2022/09/19 03:16 PM
L182	16322	(G06F1/04,08 H04J3/0658 H03L2207/50).cpc.	(US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT)	OR	ON	ON	2022/09/19 03:16 PM
L183	3033	(L68 L70) and FPGA	(US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT)	OR	ON	ON	2022/09/19 03:16 PM
L184	898	L69 and ((phase near lock$4 near loop) PLL)	(US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT)	OR	ON	ON	2022/09/19 03:16 PM
L185	246	(L71 L72) and (deserial$4) and (serial$4)	(US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT)	OR	ON	ON	2022/09/19 03:16 PM
L186	68	("20020110211" | "20020190751" | "20030052709" | "3473160" | "4229825" | "4680779" | "5034967" | "5084891" | "5162762" | "5184350" | "5256918" | "5357249" | "5457717" | "5481563" | "5483180" | "5552942" | "5610953" | "5689195" | "5726988" | "5757240" | "5760844" | "5781038" | "5793822" | "5802103" | "5838749" | "5896067" | "5896561" | "5909126" | "5917850" | "5920600" | "5963608" | "5974464" | "5987543" | "5999025" | "6008680" | "6031428" | "6031473" | "6091261" | "6166572" | "6178213" | "6215326" | "6223089" | "6256722" | "6259271" | "6266799" | "6292116" | "6295563" | "6327196" | "6341142" | "6374361" | "6400291" | "6407576" | "6421796" | "6463109" | "6538656" | "6631144" | "6650720" | "6834367" | "6917661").PN. OR ("7333570").URPN.	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2022/09/19 03:16 PM
L187	343	"10037568" "10169814" "4068188" "4745372"	(US-PGPUB; USPAT; USOCR; FPRS; EPO;	OR	ON	ON	2022/09/19 03:16 PM

		"8467418" "7333570" "7080345" "9330740" "9001951" "10411720" "6675306" "20190025413"	JPO; DERWENT; IBM_TDB)				
L188	12	(("10771069") or ("10826502") or ("10763865") or ("10931286") or ("11018678")).PN.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/09/19 03:16 PM
L189	23	"7084709"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/09/19 03:16 PM
L190	3630	(clock NEAR domain NEAR crossing)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/19 03:16 PM
L191	382	(clock NEAR domain NEAR crossing).clm.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/19 03:16 PM
L192	136	L141 AND ((field NEAR programmable NEAR gate NEAR array) fpga)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO,	OR	ON	ON	2022/09/19 03:16 PM

			NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L193	29	L142 AND ((phase NEAR lock$4 NEAR loop$4) PLL)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/19 03:16 PM

PE2E SEARCH - Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	British Equivalents	Time Stamp
N7	0	(fpga AND (deserializ$4) AND ((gate data) NEAR array) AND (phase NEAR detect$4) AND ((adjustable variable) NEAR oscillat$4) AND serializ$4).clm.	(US-PGPUB; USPAT)	OR	ON	ON	2022/09/19 03:17 PM
N8	1	(fpga AND (deserializ$4) AND ((gate data) NEAR array) AND (phase NEAR detect$4) AND serializ$4).clm.	(US-PGPUB; USPAT)	OR	ON	ON	2022/09/19 03:17 PM

Doc Code: DIST.E.FILE **Document Description: Electronic Terminal Disclaimer - Filed**	PTO/SB/26 U.S. Patent and Trademark Office Department of Commerce

Electronic Petition Request	**TERMINAL DISCLAIMER TO OBVIATE A DOUBLE PATENTING REJECTION OVER A "PRIOR" PATENT**
Application Number	17723145
Filing Date	18-Apr-2022
First Named Inventor	Nima Badizadegan
Attorney Docket Number	00287-0017
Title of Invention	FIELD PROGRAMMABLE GATE ARRAY WITH EXTERNAL PHASE-LOCKED LOOP

☒ Filing of terminal disclaimer does not obviate requirement for response under 37 CFR 1.111 to outstanding Office Action

☒ This electronic Terminal Disclaimer is not being used for a Joint Research Agreement.

Owner	Percent Interest
HFT SOLUTIONS, LLC	100%

The owner(s) with percent interest listed above in the instant application hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application which would extend beyond the expiration date of the full statutory term of prior patent number(s)

11128305

as the term of said prior patent is presently shortened by any terminal disclaimer. The owner hereby agrees that any patent so granted on the instant application shall be enforceable only for and during such period that it and the prior patent are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns.

In making the above disclaimer, the owner does not disclaim the terminal part of the term of any patent granted on the instant application that would extend to the expiration date of the full statutory term of the prior patent, "as the term of said prior patent is presently shortened by any terminal disclaimer," in the event that said prior patent later:
- expires for failure to pay a maintenance fee;
- is held unenforceable;
- is found invalid by a court of competent jurisdiction;
- is statutorily disclaimed in whole or terminally disclaimed under 37 CFR 1.321;
- has all claims canceled by a reexamination certificate;
- is reissued; or
- is in any manner terminated prior to the expiration of its full statutory term as presently shortened by any terminal disclaimer.

◉ Terminal disclaimer fee under 37 CFR 1.20(d) is included with Electronic Terminal Disclaimer request.

○	I certify, in accordance with 37 CFR 1.4(d)(4), that the terminal disclaimer fee under 37 CFR 1.20(d) required for this terminal disclaimer has already been paid in the above-identified application.

Applicant claims the following fee status:

- ◉ Small Entity
- ○ Micro Entity
- ○ Regular Undiscounted

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

THIS PORTION MUST BE COMPLETED BY THE SIGNATORY OR SIGNATORIES

I certify, in accordance with 37 CFR 1.4(d)(4) that I am:

- ◉ An attorney or agent registered to practice before the Patent and Trademark Office who is of record in this application

  Registration Number 51431

- ○ A sole inventor
- ○ A joint inventor; I certify that I am authorized to sign this submission on behalf of all of the inventors as evidenced by the power of attorney in the application
- ○ A joint inventor; all of whom are signing this request

Signature	/Keith J. Barkaus/
Name	Keith J. Barkaus

*Statement under 37 CFR 3.73(b) is required if terminal disclaimer is signed by the assignee (owner).
Form PTO/SB/96 may be used for making this certification. See MPEP § 324.

Electronic Patent Application Fee Transmittal

Application Number:	17723145
Filing Date:	18-Apr-2022
Title of Invention:	FIELD PROGRAMMABLE GATE ARRAY WITH EXTERNAL PHASE-LOCKED LOOP
First Named Inventor/Applicant Name:	Nima Badizadegan
Filer:	Keith J. Barkaus/Victoria Gilmore
Attorney Docket Number:	00287-0017

Filed as Small Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
STATUTORY OR TERMINAL DISCLAIMER	2814	1	170	170
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**170**

Doc Code: DISQ.E.FILE
Document Description: Electronic Terminal Disclaimer – Approved

Application No.: 17723145

Filing Date: 18-Apr-2022

Applicant/Patent under Reexamination: Badizadegan

Electronic Terminal Disclaimer filed on September 16, 2022

☒ APPROVED

This patent is subject to a terminal disclaimer

☐ DISAPPROVED

Approved/Disapproved by: Electronic Terminal Disclaimer automatically approved by EFS-Web

U.S. Patent and Trademark Office

Electronic Acknowledgement Receipt

EFS ID:	46636098
Application Number:	17723145
International Application Number:	
Confirmation Number:	1635
Title of Invention:	FIELD PROGRAMMABLE GATE ARRAY WITH EXTERNAL PHASE-LOCKED LOOP
First Named Inventor/Applicant Name:	Nima Badizadegan
Customer Number:	1912
Filer:	Keith J. Barkaus/Victoria Gilmore
Filer Authorized By:	Keith J. Barkaus
Attorney Docket Number:	00287-0017
Receipt Date:	16-SEP-2022
Filing Date:	18-APR-2022
Time Stamp:	16:48:30
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$170
RAM confirmation Number	E20229FG48271475
Deposit Account	
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Terminal Disclaimer-Filed (Electronic)	eTerminal-Disclaimer.pdf	41376 4e88e8a6a890aa74082688b6a2ecc65aa3f2ed76	no	2
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	38292 eb890fc5b0e8978924a3c74b985ab655e5aa682a	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	79668		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/723,145	04/18/2022	Nima Badizadegan	00287-0017	1635

1912 7590 09/15/2022

AMSTER, ROTHSTEIN & EBENSTEIN LLP
90 PARK AVENUE
NEW YORK, NY 10016

EXAMINER	
CHENG, DIANA	

ART UNIT	PAPER NUMBER
2849	

MAIL DATE	DELIVERY MODE
09/15/2022	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 17/723,145	Applicant(s) Badizadegan, Nima	
	Examiner Diana J Cheng	Art Unit 2849	AIA (FITF) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☑ Responsive to communication(s) filed on 09/08/2022.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☑ This action is **FINAL.** 2b) ☐ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5) ☑ Claim(s) 1-12 is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6) ☐ Claim(s) _____ is/are allowed.

7) ☑ Claim(s) 1-3,8 and 10 is/are rejected.

8) ☑ Claim(s) 4-7,9 and 11-12 is/are objected to.

9) ☐ Claim(s) _____ are subject to restriction and/or election requirement

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to **PPHfeedback@uspto.gov.**

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date _____.

4) ☐ Other: _____.

DETAILED ACTION

Notice of Pre-AIA or AIA Status

The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on nonstatutory double patenting provided the reference application or patent either is shown to be commonly owned with the examined application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement. See

MPEP § 717.02 for applications subject to examination under the first inventor to file provisions of the AIA as explained in MPEP § 2159. See MPEP § 2146 *et seq.* for applications not subject to examination under the first inventor to file provisions of the AIA. A terminal disclaimer must be signed in compliance with 37 CFR 1.321(b).

The USPTO Internet website contains terminal disclaimer forms which may be used. Please visit www.uspto.gov/patent/patents-forms. The filing date of the application in which the form is filed determines what form (e.g., PTO/SB/25, PTO/SB/26, PTO/AIA/25, or PTO/AIA/26) should be used. A web-based eTerminal Disclaimer may be filled out completely online using web-screens. An eTerminal Disclaimer that meets all requirements is auto-processed and approved immediately upon submission. For more information about eTerminal Disclaimers, refer to www.uspto.gov/patents/process/file/efs/guidance/eTD-info-I.jsp.

Claims 1-3, 8 and 10 are rejected on the ground of nonstatutory double patenting as being unpatentable over claims 1, 20, 20, 1, and 8 of U.S. Patent No. 11,128,305, respectively. Although the claims at issue are not identical, they are not patentably distinct from each other because the claimed limitations the present invention are recited in the respective claims of U.S. Patent No. 11,128,305.

Claim 1 is provisionally rejected on the ground of nonstatutory double patenting as being unpatentable over claim 10 of copending Application No. 17/405,188 (reference application). Although the claims at issue are not identical, they are not patentably distinct from each other because the claimed limitations of the present invention are recited in the respective claims of copending Application No. 17/405,188.

This is a provisional nonstatutory double patenting rejection because the patentably indistinct claims have not in fact been published as patented.

Allowable Subject Matter

Claims 4-7, 9, 11 and 12 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Contact

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Diana J Cheng whose telephone number is (571)270-1197. The examiner can normally be reached Monday - Friday 9 am - 5:30 pm ET.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Menatoallah Youssef can be reached on (571)270-3684. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of published or unpublished applications may be obtained from Patent Center. Unpublished application information in Patent Center is available to registered users. To file and manage patent submissions in Patent Center, visit: https://patentcenter.uspto.gov. Visit https://www.uspto.gov/patents/apply/patent-center for more information about Patent Center and https://www.uspto.gov/patents/docx for information about filing in DOCX format. For additional questions, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/DIANA J. CHENG/
Primary Examiner, Art Unit 2849

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/723,145	Badizadegan, Nima
	Examiner	Art Unit
	Diana J Cheng	2849

CPC - Searched*		
Symbol	Date	Examiner
H03L7/085,087,089,0891,0893,0895,0896,0898,091,093,095	09/02/2022	DJC
G06F30/30,34,343,347	09/02/2022	DJC
G06F1/04,08 H04J3/0658 H03L2207/50	09/02/2022	DJC

CPC Combination Sets - Searched*		
Symbol	Date	Examiner

US Classification - Searched*			
Class	Subclass	Date	Examiner

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	Date	Examiner
Refreshed Search	09/02/2022	DJC
Refreshed Search	09/12/2022	DJC

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner

Citadel Securities LLC, Exhibit 1003, Page 141 of 290

PE2E SEARCH - Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	British Equivalents	Time Stamp
L144	7	((("BADIZADEGAN") near3 ("Nima"))).INV.	(US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT)	OR	ON	ON	2022/09/12 01:41 PM
L145	0	(fpga near tranceiver) and (deserializ$4) and ((gate data) near array) and serializ$4	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/12 01:41 PM
L146	11	tranceiver and (deserializ$4) and ((gate data) near array) and serializ$4	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/12 01:41 PM
L147	648	(deserializ$4) and ((gate data) near array) and (phase near detect$4) and serializ$4	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/12 01:41 PM
L148	615	fpga and L60	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/12 01:41 PM
L149	13	fpga and (deserializ$4) and ((gate data) near array) and (phase near detect$4) and ((adjustable variable) near oscillat$4) and serializ$4	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/12 01:41 PM
L150	9	(fpga near transceiver) and (deserializ$4) and ((gate data) near array) and (phase near detect$4) and ((adjustable variable) near oscillat$4) and serializ$4	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/12 01:41 PM
L151	60	(fpga near transceiver) and (deserializ$4) and ((gate data) near array) and serializ$4	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/12 01:41 PM
L152	239	transceiver near bank	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/12 01:41 PM
L153	27	(("9330740") or ("9001951") or ("10411720") or ("8675306") or ("20190025413")).PN.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/09/12 01:41 PM
L154	23	(("10037568") or ("10169814") or ("4068188") or	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	OFF	OFF	2022/09/12 01:41 PM

		("4745372") or ("8467418")).PN.	IBM_TDB)				
L155	25251	(H03L7/085,087,089,0891,0893,0895,0896,0898,091,093,095).cpc.	(US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT)	OR	ON	ON	2022/09/12 01:41 PM
L156	12316	(G06F30/30,34,343,347).cpc.	(US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT)	OR	ON	ON	2022/09/12 01:41 PM
L157	16296	(G06F1/04,08 H04J3/0658 H03L2207/50).cpc.	(US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT)	OR	ON	ON	2022/09/12 01:41 PM
L158	3027	(L68 L70) and FPGA	(US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT)	OR	ON	ON	2022/09/12 01:41 PM
L159	894	L69 and ((phase near lock$4 near loop) PLL)	(US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT)	OR	ON	ON	2022/09/12 01:41 PM
L160	245	(L71 L72) and (deserial$4) and (serial$4)	(US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT)	OR	ON	ON	2022/09/12 01:41 PM
L161	68	("20020110211" | "20020190751" | "20030052709" | "3473160" | "4229825" | "4680779" | "5034967" | "5084891" | "5162762" | "5184350" | "5256918" | "5357249" | "5457717" | "5481563" | "5483180" | "5552942" | "5610953" | "5689195" | "5726988" | "5757240" | "5760844" | "5781038" | "5793822" | "5802103" | "5838749" | "5896067" | "5896561" | "5909126" | "5917850" | "5920600" | "5963608" | "5974464" | "5987543" | "5999025" | "6008680" | "6031428" | "6031473" | "6091261" | "6166572" | "6178213" | "6215326" | "6223089" | "6256722" | "6259271" | "6266799" | "6292116" | "6295563" | "6327196" | "6341142" | "6374361" | "6400291" | "6407576" | "6421796" | "6463109" | "6538656" | "6631144" | "6650720" | "6834367" | "6917661").PN. OR ("7333570").URPN.	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2022/09/12 01:41 PM
L162	341	"10037568" "10169814" "4068188" "4745372"	(US-PGPUB; USPAT; USOCR; FPRS; EPO;	OR	ON	ON	2022/09/12 01:41 PM

		"8467418" "7333570" "7080345" "9330740" "9001951" "10411720" "6675306" "20190025413"	JPO; DERWENT; IBM_TDB)				
L163	12	(("10771069") or ("10826502") or ("10763865") or ("10931286") or ("11018678")).PN.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/09/12 01:41 PM
L164	23	"7084709"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/09/12 01:41 PM
L165	3627	(clock NEAR domain NEAR crossing)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/12 01:41 PM
L166	382	(clock NEAR domain NEAR crossing).clm.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/12 01:41 PM
L167	136	L141 AND ((field NEAR programmable NEAR gate NEAR array) fpga)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO,	OR	ON	ON	2022/09/12 01:41 PM

			NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L168	29	L142 AND ((phase NEAR lock$4 NEAR loop$4) PLL)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/12 01:41 PM

PE2E SEARCH - Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	British Equivalents	Time Stamp
N5	0	(fpga AND (deserializ$4) AND ((gate data) NEAR array) AND (phase NEAR detect$4) AND ((adjustable variable) NEAR oscillat$4) AND serializ$4).clm.	(US-PGPUB; USPAT)	OR	ON	ON	2022/09/12 01:42 PM
N6	1	(fpga AND (deserializ$4) AND ((gate data) NEAR array) AND (phase NEAR detect$4) AND serializ$4).clm.	(US-PGPUB; USPAT)	OR	ON	ON	2022/09/12 01:42 PM

Doc Code: DIST.E.FILE **Document Description: Electronic Terminal Disclaimer - Filed**	PTO/SB/25 PTO/SB/26 U.S. Patent and Trademark Office Department of Commerce

Electronic Petition Request	**TERMINAL DISCLAIMER TO OBVIATE A PROVISIONAL DOUBLE PATENTING REJECTION OVER A PENDING "REFERENCE" APPLICATION AND TERMINAL DISCLAIMER TO OBVIATE A DOUBLE PATENTING REJECTION OVER A "PRIOR" PATENT**
Application Number	17723145
Filing Date	18-Apr-2022
First Named Inventor	Nima Badizadegan
Attorney Docket Number	00287-0017
Title of Invention	FIELD PROGRAMMABLE GATE ARRAY WITH EXTERNAL PHASE-LOCKED LOOP

☒ Filing of terminal disclaimer does not obviate requirement for response under 37 CFR 1.111 to outstanding Office Action

☒ This electronic Terminal Disclaimer is not being used for a Joint Research Agreement.

Owner	Percent Interest
HFT SOLUTIONS, LLC	100 %

The owner(s) of percent interest listed above in the instant application hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application which would extend beyond the expiration date of the full statutory term of any patent granted on pending reference Application Number(s)

17405188 filed on 08/18/2021

as the term of any patent granted on said reference application may be shortened by any terminal disclaimer filed prior to the grant of any patent on the pending reference application. The owner hereby agrees that any patent so granted on the instant application shall be enforceable only for and during such period that it and any patent granted on the reference application are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns.

In making the above disclaimer, the owner does not disclaim the terminal part of any patent granted on the instant application that would extend to the expiration date of the full statutory term of any patent granted on said reference application, "as the term of any patent granted on said reference application may be shortened by any terminal disclaimer filed prior to the grant of any patent on the pending reference application," in the event that any such patent granted on the pending reference application: expires for failure to pay a maintenance fee, is held unenforceable, is found invalid by a court of competent jurisdiction, is statutorily disclaimed in whole or terminally disclaimed under 37 CFR 1.321, has all claims canceled by a reexamination certificate, is reissued, or is in any manner terminated prior to the expiration of its full statutory term as shortened by any terminal disclaimer filed prior to its grant.

The owner(s) with percent interest listed above in the instant application hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application which would extend beyond the expiration date of the full statutory term of prior patent number(s)

10763865

10771069

10826502

10931286

11018678

11329655

as the term of said prior patent is presently shortened by any terminal disclaimer. The owner hereby agrees that any patent so granted on the instant application shall be enforceable only for and during such period that it and the prior patent are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns.

In making the above disclaimer, the owner does not disclaim the terminal part of the term of any patent granted on the instant application that would extend to the expiration date of the full statutory term of the prior patent, "as the term of said prior patent is presently shortened by any terminal disclaimer," in the event that said prior patent later:
- expires for failure to pay a maintenance fee;
- is held unenforceable;
- is found invalid by a court of competent jurisdiction;
- is statutorily disclaimed in whole or terminally disclaimed under 37 CFR 1.321;
- has all claims canceled by a reexamination certificate;
- is reissued; or
- is in any manner terminated prior to the expiration of its full statutory term as presently shortened by any terminal disclaimer.

◉ Terminal disclaimer fee under 37 CFR 1.20(d) is included with Electronic Terminal Disclaimer request.

○ I certify, in accordance with 37 CFR 1.4(d)(4), that the terminal disclaimer fee under 37 CFR 1.20(d) required for this terminal disclaimer has already been paid in the above-identified application.

Applicants claims the following fee status:

◉ Small Entity

○ Micro Entity

○ Regular Undiscounted

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

THIS PORTION MUST BE COMPLETED BY THE SIGNATORY OR SIGNATORIES

I certify, in accordance with 37 CFR 1.4(d)(4) that I am:

- (◉) An attorney or agent registered to practice before the Patent and Trademark Office who is of record in this application

  Registration Number 51431

- (○) A sole inventor
- (○) A joint inventor; I certify that I am authorized to sign this submission on behalf of all of the inventors as evidenced by the power of attorney in the application
- (○) A joint inventor; all of whom are signing this request

Signature	/Keith J. Barkaus/
Name	Keith J. Barkaus

*Statement under 37 CFR 3.73(b) is required if terminal disclaimer is signed by the assignee (owner).
Form PTO/SB/96 may be used for making this certification. See MPEP § 324.

Electronic Patent Application Fee Transmittal

Application Number:	17723145
Filing Date:	18-Apr-2022
Title of Invention:	FIELD PROGRAMMABLE GATE ARRAY WITH EXTERNAL PHASE-LOCKED LOOP
First Named Inventor/Applicant Name:	Nima Badizadegan
Filer:	Keith J. Barkaus/Victoria Gilmore
Attorney Docket Number:	00287-0017

Filed as Small Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
STATUTORY OR TERMINAL DISCLAIMER	2814	1	170	170
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**170**

Doc Code: DISQ.E.FILE
Document Description: Electronic Terminal Disclaimer – Approved

Application No.: 17723145

Filing Date: 18-Apr-2022

Applicant/Patent under Reexamination: Badizadegan

Electronic Terminal Disclaimer filed on September 8, 2022

☒ APPROVED

This patent is subject to a terminal disclaimer

☐ DISAPPROVED

Approved/Disapproved by: Electronic Terminal Disclaimer automatically approved by EFS-Web

U.S. Patent and Trademark Office

Electronic Acknowledgement Receipt

EFS ID:	46569347
Application Number:	17723145
International Application Number:	
Confirmation Number:	1635
Title of Invention:	FIELD PROGRAMMABLE GATE ARRAY WITH EXTERNAL PHASE-LOCKED LOOP
First Named Inventor/Applicant Name:	Nima Badizadegan
Customer Number:	1912
Filer:	Keith J. Barkaus/Victoria Gilmore
Filer Authorized By:	Keith J. Barkaus
Attorney Docket Number:	00287-0017
Receipt Date:	08-SEP-2022
Filing Date:	18-APR-2022
Time Stamp:	17:20:52
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$170
RAM confirmation Number	E202298H20492954
Deposit Account	
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Terminal Disclaimer-Filed (Electronic)	eTerminal-Disclaimer.pdf	48514 806fe75c2ac6cd400626e9c14715f1fe5b7d7090	no	3
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	38291 6b063fd71c5ace0c4914d9144610c25e0a5a0a66	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	86805		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	HFT Solutions, LLC	Confirmation No.: 1635
Title:	FIELD PROGRAMMABLE GATE ARRAY WITH EXTERNAL PHASE-LOCKED LOOP	
Appl. No.:	17/723,145	
Filing Date:	April 18, 2022	
Examiner:	CHENG, Diana	
Art Unit:	2849	
Docket No.:	00287-0017	
Customer No.:	01912	

AMENDMENT AND REPLY TO OFFICE ACTION

VIA EFS

Mail Stop AMENDMENT
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This responds to the Office Action dated September 8, 2022. A response to the Office Action is due December 8, 2022 such that the present response is being timely filed.

Claims begin on page 2**.**

Remarks begin on page 6**.**

CLAIMS

What is claimed is:

1. (Original) A method for processing a first serial data stream, using a field programmable gate array system, to generate a second serial data stream, wherein the method comprises the steps of:

(a) receiving, by a deserializer in a field programmable array, a clock signal;

(b) receiving, by the deserializer, the first serial data stream;

(c) generating, by the deserializer, a receiver side clock signal;

(d) converting, by the deserializer, the first serial data stream into a first plurality of parallel data streams;

(e) transmitting, from the deserializer to computational circuitry in the field programmable gate array, the first plurality of parallel data streams;

(f) transmitting, from the deserializer to a phase lock loop of the field programmable gate array system that is not within on the field programmable gate array, the receiver side clock signal;

(g) generating, using the phase lock loop, a second clock signal;

(h) generating, within the field programmable gate array, a transmitter side clock signal derived from the second clock signal;

(i) performing, by the computational circuitry, a set of operations on at least a portion of the first plurality of parallel data streams to generate a second plurality of parallel data streams; and

(j) transmitting, from the field programmable gate array system, the second serial data stream, derived from the second plurality of parallel data streams,

wherein said method does not use clock domain crossing operations that delay processing of the first set of parallel data streams.

2. (Original) The method of claim 1, wherein the first serial data stream comprises market

data, the second serial data stream comprises order entry data, and the set of operations are associated with a trading algorithm.

3. (Original) The method of claim 1, wherein the first serial data stream includes market data and the second serial data stream includes trading data.

4. (Original) The method of claim 1, wherein the set of operations includes at least one of the following:

(i) an arithmetic operation;

(ii) a logical operation;

(iii) a pipeline operation; and

(iv) a memory access operation.

5. (Original) The method of claim 1, wherein at least a portion of the set of operations performed in step (h) are performed prior to step (g).

6. (Original) The method of claim 1, wherein at least a portion of the set of operations performed in step (h) are performed after step (g).

7. (Original) The method of claim 1, wherein all of the set of operations performed in step (h) are performed after step (g).

8. (Original) The method of claim 1, wherein step (g) further comprises:

(i) generating, by the phase lock loop, a feedback clock signal associated with the transmitter side clock signal by performing the following steps until a first output of a phase detector of the field programmable gate array system is below a first threshold level:

(1) generating, by an adjustable oscillator in the field programmable gate array system, the second clock signal;

(2) generating, by the phase detector, the first output based on a comparison of the receiver side clock signal and the feedback clock signal obtained from the second clock signal;

(3) transmitting, from the phase detector to a phase controller of the field programmable gate array system, the first output;

(4) determining, by the phase controller, interim adjustment information based on the first output; and

(5) transmitting, from the phase controller to the adjustable oscillator, the interim adjustment information;

wherein, the adjustable oscillator adjusts the second clock signal based on the interim adjustment information,

wherein steps (1) through (5) are repeated until the first output of the phase detector is below the first threshold level.

9. (Original) The method of claim 1, wherein the first plurality of data streams has the same number of data streams as the second plurality of data streams.

10. (Original) The method of claim 1, wherein the first plurality of data streams and the second plurality of data streams comprise one of the following:

(i) eight (8) data streams;

(ii) ten (10) data streams;

(iii) sixteen (16) data streams;

(iv) twenty (20) data streams;

(v) thirty-two (32) data streams;

(vi) forty (40) data streams;

(vii) sixty-four (64) data streams;

(viii) eighty (80) data streams;

(ix) one hundred twenty-eight (128) data streams; and

(x) one hundred sixty (160) data streams.

11. (Original) The method of claim 1, wherein the transmitter side clock signal and the receiver side clock signal have the same frequency and phase.

12. (Original) The method of claim 1, wherein the transmitter side clock signal and the receiver side clock signal have the same frequency and different phases.

REMARKS

This responds to the Non-Final Office Action dated September 8, 2022. A response to this Office Action is due December 8, 2022. Accordingly, this Response is being timely filed.

Claims 1-12 are pending. No amendments are presented by this response. A listing of the claims including the status of each is included herein for the convenience of the Examiner. Reconsideration based on the following remarks is respectfully requested.

Double Patenting

Claims 1, 4, 8 and 10 have been rejected based on nonstatutory double patenting over claims 1, 5 and 8 of U.S. Patent No. 10,763,865.

Claims 1, 4 and 10 have been rejected based on nonstatutory double patenting over claims 1, 6 and 10 of U.S. Patent No. 10,771,069.

Claim 1, has been rejected based on nonstatutory double patenting over the below-identified claims of the below-identified United States patents as well as a pending patent application (also identified below):

- Claim 12 of U.S. Patent No. 10,826,502;
- Claim 10 of U.S. Patent No. 10,931,286;
- Claims 1, 6 and 8 of U.S. Patent No. 11,018,678;
- Claim 10 of of pending U.S. Patent Appl. Ser. No. 17/405,188

Claims 1-3, 8 and 10 have been rejected based on nonstatutory double patenting over claims 1, 20, and 8 of U.S. Patent No. 11,329,655.

While Applicant does not necessarily agree with these rejections, in an effort to advance prosecution, Applicant submits herewith a Terminal Disclaimer to overcome the rejections of the claims based on nonstatutory double patenting. Applicant respectfully requests reconsideration and withdrawal of the rejections of the claims.

Since there are no other rejections of claims 1-10, they are believed to be patentable and in condition for allowance.

Applicant appreciates the Examiner's indication that dependent claims 11 and 12 would be allowable if rewritten in independent form. Claims 11 and 12 depend on claim 1 which is believed

to be patentable as discussed above. Accordingly, claims 11 and 12 are believed to be patentable in their present form for at least the same reasons.

Accordingly, Applicant respectfully submits that claims 1-12 are patentable and in condition for allowance.

Reference to Related Patents and Co-pending Applications

The below chart provides information regarding related issued patents and co-pending applications filed by the present Applicant:

SERIAL NO.	ATTORNEY DOCKET NO.	FILING DATE	STATUS
16/672,076	00287-0007	2019-11-01	Issued USP 10,826,502
16/670,702	00287-0008	2019-10-31	Issued USP 10,771,069
16/888,218	00287-0009	2020-05-29	Issued USP 10,763,865
16/937,314	00287-0011	2020-07-23	Issued USP 10,931,286
16/937,309	00287-0012	2020-07-23	Issued USP 11,018,678
17/248,304	00287-0013	2021-01-19	Issued USP 11,128,305
17/236,577	00287-0014	2021-04-21	Issued USP 11,329,655
17/405,188	00287-0015	2021-08-18	Allowed – Issue Fee Paid 2022-05-31
17/723,130	00287-0016	2022-04-18	Docketed New Case - Ready for Examination
17/723,145	**00287-0017**	**2022-04-18**	**Present Application**

The Examiner is invited to review the prosecution history of each of these applications, including the cited references of record and related office actions, as the Examiner deems appropriate.

CONCLUSION

In view of the foregoing, Applicant respectfully submits that all pending claims are patentable over the cited art and in condition for allowance. Reconsideration and prompt allowance of this application are both respectfully solicited.

Applicant respectfully asserts that the foregoing constitutes a bona fide response to all outstanding objections and rejections within this Office Action.

This application is in condition for immediate allowance. However, should any issue(s) of

a minor nature remain, the Examiner is respectfully requested to telephone the undersigned at telephone number (212) 336-8000 so that the issue(s) might be promptly resolved.

Favorable reconsideration of the present application is respectfully requested.

* * * * * *

Any claim amendment(s), claim(s) added, claim(s) canceled, argument(s), remark(s), and/or any combination(s) thereof made in this response pertain solely to the specific aspects of this specific claimed invention. Further, any claim amendment(s), claim(s) added, claim(s) canceled, argument(s), remark(s), and/or any combination(s) thereof are made without prejudice to or disclaimer of Applicant's right to seek patent protection of any unclaimed subject matter such as, but not limited, to narrower unclaimed subject matter, broader unclaimed subject matter, different unclaimed subject matter, variations of unclaimed subject matter, any combination thereof, and/or any other unclaimed subject matter that may or may not be filed, for example, in any design and/or utility patent application(s) such as, but not limited to, continuation patent application(s), continuation-in-part patent application(s), and/or divisional patent application(s) and/or any other patent application(s).

Applicant's silence as to any assertion(s) by the Examiner in the Office Action and/or to any certain fact(s) or conclusion(s) that may be implied and/or alleged by objections(s) and/or rejection(s) in the Office Action is not in any way a concession by Applicant that such assertion(s), implication(s), and/or allegation(s) are accurate, and that all requirements for any objection(s) and/or a rejection(s) have been met. Accordingly, Applicant reserves the right to analyze and dispute any such assertion(s), implication(s), and/or allegation(s) in the future.

Respectfully submitted,

AMSTER, ROTHSTEIN & EBENSTEIN LLP
Attorneys for Applicant
90 Park Avenue
New York, NY 10016
(212) 336-8000

Dated: September 8, 2022
New York, New York

By: / Keith J. Barkaus/
Keith J. Barkaus
Registration No. 51,431

Electronic Acknowledgement Receipt

EFS ID:	46579849
Application Number:	17723145
International Application Number:	
Confirmation Number:	1635
Title of Invention:	FIELD PROGRAMMABLE GATE ARRAY WITH EXTERNAL PHASE-LOCKED LOOP
First Named Inventor/Applicant Name:	Nima Badizadegan
Customer Number:	1912
Filer:	Keith J. Barkaus/Victoria Gilmore
Filer Authorized By:	Keith J. Barkaus
Attorney Docket Number:	00287-0017
Receipt Date:	08-SEP-2022
Filing Date:	18-APR-2022
Time Stamp:	17:22:48
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		1-ResponsetoNFOA.pdf	133370 3fab36df371e49fc5c82748154c9788c7e7d1cdf	yes	7

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Amendment/Request for Reconsideration-After Non-Final Rejection	1	1
	Claims	2	5
	Applicant Arguments/Remarks Made in an Amendment	6	7
Warnings:			
Information:			
	Total Files Size (in bytes):	133370	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/723,145	04/18/2022	Nima Badizadegan	00287-0017	1635

1912 7590 09/08/2022

AMSTER, ROTHSTEIN & EBENSTEIN LLP
90 PARK AVENUE
NEW YORK, NY 10016

EXAMINER	
CHENG, DIANA	

ART UNIT	PAPER NUMBER
2849	

MAIL DATE	DELIVERY MODE
09/08/2022	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 17/723,145	Applicant(s) Badizadegan, Nima	
	Examiner Diana J Cheng	Art Unit 2849	AIA (FITF) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☑ Responsive to communication(s) filed on 06/02/2022.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL.** 2b) ☑ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5) ☑ Claim(s) 1-12 is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6) ☐ Claim(s) _____ is/are allowed.

7) ☑ Claim(s) 1-10 is/are rejected.

8) ☑ Claim(s) 11-12 is/are objected to.

9) ☐ Claim(s) _____ are subject to restriction and/or election requirement

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to **PPHfeedback@uspto.gov.**

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☑ The drawing(s) filed on 04/18/2022 is/are: a)☑ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☑ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date _____.

4) ☐ Other: _____.

DETAILED ACTION

Notice of Pre-AIA or AIA Status

The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on nonstatutory double patenting provided the reference application or patent either is shown to be commonly owned with the examined application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement. See

MPEP § 717.02 for applications subject to examination under the first inventor to file provisions of the AIA as explained in MPEP § 2159. See MPEP § 2146 *et seq.* for applications not subject to examination under the first inventor to file provisions of the AIA. A terminal disclaimer must be signed in compliance with 37 CFR 1.321(b).

The USPTO Internet website contains terminal disclaimer forms which may be used. Please visit www.uspto.gov/patent/patents-forms. The filing date of the application in which the form is filed determines what form (e.g., PTO/SB/25, PTO/SB/26, PTO/AIA/25, or PTO/AIA/26) should be used. A web-based eTerminal Disclaimer may be filled out completely online using web-screens. An eTerminal Disclaimer that meets all requirements is auto-processed and approved immediately upon submission. For more information about eTerminal Disclaimers, refer to www.uspto.gov/patents/process/file/efs/guidance/eTD-info-I.jsp.

Claims 1, 4, 8, and 10 are rejected on the ground of nonstatutory double patenting as being unpatentable over claims 1, 5, 1, and 8 of U.S. Patent No. 10,763,865, respectively. Although the claims at issue are not identical, they are not patentably distinct from each other because the claimed limitations the present invention are recited in the respective claims of U.S. Patent No. 10,763,865.

Claims 1, 4, and 10 are rejected on the ground of nonstatutory double patenting as being unpatentable over claims 1, 6, and 8 of U.S. Patent No. 10,771,069, respectively. Although the claims at issue are not identical, they are not patentably distinct from each other because the claimed limitations the present invention are recited in the respective claims of U.S. Patent No. 10,771,069.

Claim 1 is rejected on the ground of nonstatutory double patenting as being unpatentable over claim 12 of U.S. Patent No. 10,826,502, respectively. Although the claims at issue are not identical, they are not patentably distinct from each other because the claimed limitations the present invention are recited in the respective claims of U.S. Patent No. 10,826,502.

Claim 1 is rejected on the ground of nonstatutory double patenting as being unpatentable over claim 10 of U.S. Patent No. 10,931,286, respectively. Although the claims at issue are not identical, they are not patentably distinct from each other because the claimed limitations the present invention are recited in the respective claims of U.S. Patent No. 10,931,286.

Claims 1, 4, and 10 are rejected on the ground of nonstatutory double patenting as being unpatentable over claims 1, 6, and 8 of U.S. Patent No. 11,018,678, respectively. Although the claims at issue are not identical, they are not patentably distinct from each other because the claimed limitations the present invention are recited in the respective claims of U.S. Patent No. 11,018,678.

Claims 1-3, 8 and 10 are rejected on the ground of nonstatutory double patenting as being unpatentable over claims 1, 20, 20, 1, and 8 of U.S. Patent No. 11,128,305, respectively. Although the claims at issue are not identical, they are not patentably distinct from each other because the claimed limitations the present invention are recited in the respective claims of U.S. Patent No. 11,128,305.

Claims 1-10 are rejected on the ground of nonstatutory double patenting as being unpatentable over claims 1, 24, 24, 7, 13-15, 1, 8 and 9 of U.S. Patent No. 11,329,655, respectively. Although the claims at issue are not identical, they are not patentably

distinct from each other because the claimed limitations the present invention are recited in the respective claims of U.S. Patent No. 11,329,655.

Claim 1 is provisionally rejected on the ground of nonstatutory double patenting as being unpatentable over claim 10 of copending Application No. 17/405,188 (reference application). Although the claims at issue are not identical, they are not patentably distinct from each other because the claimed limitations of the present invention are recited in the respective claims of copending Application No. 17/405,188.

This is a provisional nonstatutory double patenting rejection because the patentably indistinct claims have not in fact been published as patented.

Allowable Subject Matter

Claims 11 and 12 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Contact

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Diana J Cheng whose telephone number is (571)270-1197. The examiner can normally be reached Monday - Friday 9 am - 5:30 pm ET.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an

interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Menatoallah Youssef can be reached on (571)270-3684. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of published or unpublished applications may be obtained from Patent Center. Unpublished application information in Patent Center is available to registered users. To file and manage patent submissions in Patent Center, visit: https://patentcenter.uspto.gov. Visit https://www.uspto.gov/patents/apply/patent-center for more information about Patent Center and https://www.uspto.gov/patents/docx for information about filing in DOCX format. For additional questions, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/DIANA J. CHENG/
Primary Examiner, Art Unit 2849

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/723,145	Badizadegan, Nima
	Examiner	Art Unit
	Diana J Cheng	2849

CPC - Searched*		
Symbol	Date	Examiner
H03L7/085,087,089,0891,0893,0895,0896,0898,091,093,095	09/02/2022	DJC
G06F30/30,34,343,347	09/02/2022	DJC
G06F1/04,08 H04J3/0658 H03L2207/50	09/02/2022	DJC

CPC Combination Sets - Searched*		
Symbol	Date	Examiner

US Classification - Searched*			
Class	Subclass	Date	Examiner

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	Date	Examiner
Refreshed Search	09/02/2022	DJC

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner

Citadel Securities LLC, Exhibit 1003, Page 170 of 200

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (01-10)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	17723145
Filing Date	2022-04-18
First Named Inventor	Nima Badizadegan
Art Unit	2849
Examiner Name	CHENG, Diana
Attorney Docket Number	00287-0017

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	10037568	B2	2018-07-31	Taylor et al.	
	2	10169814	B2	2019-01-01	Parsons et al.	
	3	4068188	A	1978-01-10	Yokoyama	
	4	4745372	A	1988-05-17	Miwa	
	5	8467418	B2	2013-06-18	Aweya et al.	
	6	7333570	B2	2008-02-19	Aung et al.	
	7	7080345	B1	2006-07-18	Iotov	
	8	9330740	B1	2016-05-03	Baeckler et al.	

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /D.J.C/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
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	Examiner Name	CHENG, Diana
	Attorney Docket Number	00287-0017

	9	9001951	B1	2015-04-07	Kumpulainen	
	10	10411720	B2	2019-09-10	Lenzen et al.	
	11	6675306	B1	2004-01-06	Baxter	
	12	7084709	B1	2006-08-01	Leong, et al.	

If you wish to add additional U.S. Patent citation information please click the Add button. Add

U.S.PATENT APPLICATION PUBLICATIONS Remove

Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20190025413	A1	2019-01-24	Liu et al.	

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FOREIGN PATENT DOCUMENTS Remove

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1							

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Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /D.J.C/

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First Named Inventor	Nima Badizadegan
Art Unit	2849
Examiner Name	CHENG, Diana
Attorney Docket Number	00287-0017

	1	XILINX, "7 Series FPGAs GTX/GTH Transceivers - User Guide," Page 26, available at https://www.xilinx.com/support/documentation/user_guides/ug476_7Series_Transceivers.pdf (August 14, 2018).	
	2	SARAH HARRIS, "Timing & Synchronization," Harvey Mudd College Engineering Department, Page 24, available at https://cseweb.ucsd.edu/classes/wi06/cse291-b/slide/let4/timingint.pdf (January 31, 2006).	
	3	SAM PALERMO, "ECEN 720 High-Speed Links: Circuits and Systems - Lab 5," Texas A&M University, Page 5, available at: http://ece.tamu.edu/~spalermo/ecen689/ECEN720_lab5_2017.pdf (2017).	
	4	ALTERA, "Stratix V Device Handbook," Volume 2: Transceivers, Intel, Page 13, available at: https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/hb/stratix-v/stx5_xcvr.pdf (February 15, 2017).	
	5	STACKEXCHANGE, "Phase Frequency Detector in PLL," StackExchange, available at: https://electronics.stackexchange.com/questions/301402/phase-frequency-detector-in-pll (April 24, 2017).	
	6	IEEE STANDARDS ASSOCIATION, "IEEE Standards for Ethernet," IEEE 802.3-2018, Section 4, Clauses 49 and 51, Section 6, Clauses 82 and 83, available at: https://standards.ieee.org/standard/802_3-2018.html (August 31, 2018).	
	7	SLOBODAN MILIJEVIC, "The basics of synchronized Ethernet," EE Times-Asia, available at: https://www.microsemi.com/document-portal/doc_view/126475-the-basics-of-synchronized-ethernet-synce.	
	8	MACIEJ LIPINSKI, et al., "White Rabbit: a PTP Application for Robust Sub-nanosecond Synchronization," 2011 IEEE International Symposium on Precision Clock Synchronization for Measurement, Control and Communication, Munich, Pages 25-30, available at: http://white-rabbit.web.cern.ch/documents/White_Rabbit-a_PTP_application_for_robust_sub-nanosecond_synchronization.pdf (2011).	
	9	FLOYD M. GARDNER, "Phaselock Techniques," Third Edition, Wiley-Interscience, Chapters 1, 4, 9, 10, 11, 13, and 17 (2005).	
	10	JENS TWIEFEL, et al., "Digital signal processing for an adaptive phase-locked loop controller," Proceedings of SPIE - The International Society for Optical Engineering, Volume 6926 (April 2008).	
	11	CHEN YAO, "Time to Digital Converter used in ALL digital PLL," Master of Science Thesis In System-on-Chip Design, Stockholm (August 2011).	

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /D.J.C/

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	First Named Inventor	Nima Badizadegan
	Art Unit	2849
	Examiner Name	CHENG, Diana
	Attorney Docket Number	00287-0017

	12	BEHZAD RAZAVI, "A CIRCUIT FOR ALL SEASONS: The StrongARM Latch," IEEE Solid-State Circuits Magazine (Spring 2015).
	13	PING LU, et al., "A 2-D GRO Vernier Time-to-Digital Converter with Large Input Range and Small Latency," Lund University - EIT Department, University of Toronto, IEEE Radio Frequency Integrated Circuits Symposium (2013).
	14	CHRISTIAN LEBER, et al. "High Frequency Trading Acceleration using FPGAs," University of Heidelberg, International Conference on Field Programmable Logic and Applications, Germany (2011).
	15	INTERNATIONAL TELECOMMUNICATION UNION, "Timing and synchronization aspects in packet networks," ITU-T, G.8261/Y.1361, International Telecommunication Union (May 2006).
	16	INTERNATIONAL TELECOMMUNICATION UNION, "Distribution of timing information through packet networks," ITU-T, G.8264/Y.1364, International Telecommunication Union (August 2017).
	17	IEEE STANDARDS ASSOCIATION, "IEEE Standards for Ethernet," IEEE 802.3-2018, Section 4, Figure 52-4, page 634 (2018)

If you wish to add additional non-patent literature document citation information please click the Add button Add

EXAMINER SIGNATURE

Examiner Signature	/DIANA J. CHENG/	Date Considered	09/02/2022

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /D.J.C/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	17723145
Filing Date	2022-04-18
First Named Inventor	Nima Badizadegan
Art Unit	2849
Examiner Name	CHENG, Diana
Attorney Docket Number	00287-0017

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Keith J. Barkaus/	Date (YYYY-MM-DD)	2022-06-02
Name/Print	Keith J. Barkaus	Registration Number	51,431

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /D.J.C/

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /D.J.C/

PE2E SEARCH - Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	British Equivalents	Time Stamp
L119	7	((("BADIZADEGAN") near3 ("Nima"))).INV.	(US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT)	OR	ON	ON	2022/09/02 01:00 PM
L120	0	(fpga near tranceiver) and (deserializ$4) and ((gate data) near array) and serializ$4	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/02 01:00 PM
L121	11	tranceiver and (deserializ$4) and ((gate data) near array) and serializ$4	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/02 01:00 PM
L122	647	(deserializ$4) and ((gate data) near array) and (phase near detect$4) and serializ$4	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/02 01:00 PM
L123	614	fpga and L60	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/02 01:00 PM
L124	13	fpga and (deserializ$4) and ((gate data) near array) and (phase near detect$4) and ((adjustable variable) near oscillat$4) and serializ$4	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/02 01:00 PM
L125	9	(fpga near transceiver) and (deserializ$4) and ((gate data) near array) and (phase near detect$4) and ((adjustable variable) near oscillat$4) and serializ$4	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/02 01:00 PM
L126	59	(fpga near transceiver) and (deserializ$4) and ((gate data) near array) and serializ$4	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/02 01:00 PM
L127	239	transceiver near bank	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/02 01:00 PM
L128	27	(("9330740") or ("9001951") or ("10411720") or ("8675306") or ("20190025413")).PN.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/09/02 01:00 PM
L129	23	(("10037568") or ("10169814") or ("4068188") or	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	OFF	OFF	2022/09/02 01:00 PM

		("4745372") or ("8467418")).PN.	IBM_TDB)				
L130	25217	(H03L7/085,087,089,0891,0893,0895,0896,0898,091,093,095).cpc.	(US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT)	OR	ON	ON	2022/09/02 01:00 PM
L131	12297	(G06F30/30,34,343,347).cpc.	(US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT)	OR	ON	ON	2022/09/02 01:00 PM
L132	16253	(G06F1/04,08 H04J3/0658 H03L2207/50).cpc.	(US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT)	OR	ON	ON	2022/09/02 01:00 PM
L133	3021	(L68 L70) and FPGA	(US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT)	OR	ON	ON	2022/09/02 01:00 PM
L134	886	L69 and ((phase near lock$4 near loop) PLL)	(US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT)	OR	ON	ON	2022/09/02 01:00 PM
L135	237	(L71 L72) and (deserial$4) and (serial$4)	(US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT)	OR	ON	ON	2022/09/02 01:00 PM
L136	68	("20020110211" | "20020190751" | "20030052709" | "3473160" | "4229825" | "4680779" | "5034967" | "5084891" | "5162762" | "5184350" | "5256918" | "5357249" | "5457717" | "5481563" | "5483180" | "5552942" | "5610953" | "5689195" | "5726988" | "5757240" | "5760844" | "5781038" | "5793822" | "5802103" | "5838749" | "5896067" | "5896561" | "5909126" | "5917850" | "5920600" | "5963608" | "5974464" | "5987543" | "5999025" | "6008680" | "6031428" | "6031473" | "6091261" | "6166572" | "6178213" | "6215326" | "6223089" | "6256722" | "6259271" | "6266799" | "6292116" | "6295563" | "6327196" | "6341142" | "6374361" | "6400291" | "6407576" | "6421796" | "6463109" | "6538656" | "6631144" | "6650720" | "6834367" | "6917661").PN. OR ("7333570").URPN.	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2022/09/02 01:00 PM
L137	341	"10037568" "10169814" "4068188" "4745372"	(US-PGPUB; USPAT; USOCR; FPRS; EPO;	OR	ON	ON	2022/09/02 01:00 PM

		"8467418" "7333570" "7080345" "9330740" "9001951" "10411720" "6675306" "20190025413"	JPO; DERWENT; IBM_TDB)				
L138	12	(("10771069") or ("10826502") or ("10763865") or ("10931286") or ("11018678")).PN.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/09/02 01:00 PM
L139	23	"7084709"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/09/02 01:00 PM
L140	3620	(clock NEAR domain NEAR crossing)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/02 03:52 PM
L141	382	(clock NEAR domain NEAR crossing).clm.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/02 03:52 PM
L142	136	L141 AND ((field NEAR programmable NEAR gate NEAR array) fpga)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO,	OR	ON	ON	2022/09/02 03:53 PM

			NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L143	29	L142 AND ((phase NEAR lock$4 NEAR loop$4) PLL)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/02 03:53 PM

PE2E SEARCH - Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	British Equivalents	Time Stamp
N3	0	(fpga AND (deserializ$4) AND ((gate data) NEAR array) AND (phase NEAR detect$4) AND ((adjustable variable) NEAR oscillat$4) AND serializ$4).clm.	(US-PGPUB; USPAT)	OR	ON	ON	2022/09/02 01:02 PM
N4	1	(fpga AND (deserializ$4) AND ((gate data) NEAR array) AND (phase NEAR detect$4) AND serializ$4).clm.	(US-PGPUB; USPAT)	OR	ON	ON	2022/09/02 01:02 PM

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 17/723,145	Filing Date 04/18/2022	☐ To be Mailed

ENTITY: ☐ LARGE ☑ SMALL ☐ MICRO

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A		N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A		N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*		x $50 =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*		x $240 =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).				
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))					
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL	

APPLICATION AS AMENDED - PART II

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT	09/08/2022	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 12	Minus	** 20	= 0		x $50 =	0
	Independent (37 CFR 1.16(h))	* 1	Minus	*** 3	= 0		x $240 =	0
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	0

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=		x $0 =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=		x $0 =	
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.	LIE
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".	/ANGELA S WHITE/
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".	
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.	

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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PTO/SB/08a (01-10)
Approved for use through 07/31/2012. OMB 0651-0031
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	17723145
Filing Date	2022-04-18
First Named Inventor	Nima Badizadegan
Art Unit	2849
Examiner Name	CHENG, Diana
Attorney Docket Number	00287-0017

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	10037568	B2	2018-07-31	Taylor et al.	
	2	10169814	B2	2019-01-01	Parsons et al.	
	3	4068188	A	1978-01-10	Yokoyama	
	4	4745372	A	1988-05-17	Miwa	
	5	8467418	B2	2013-06-18	Aweya et al.	
	6	7333570	B2	2008-02-19	Aung et al.	
	7	7080345	B1	2006-07-18	Iotov	
	8	9330740	B1	2016-05-03	Baeckler et al.	

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	Examiner Name	CHENG, Diana
	Attorney Docket Number	00287-0017

	9	9001951	B1	2015-04-07	Kumpulainen	
	10	10411720	B2	2019-09-10	Lenzen et al.	
	11	6675306	B1	2004-01-06	Baxter	
	12	7084709	B1	2006-08-01	Leong, et al.	

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U.S.PATENT APPLICATION PUBLICATIONS Remove

Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20190025413	A1	2019-01-24	Liu et al.	

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Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
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Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]

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	First Named Inventor	Nima Badizadegan
	Art Unit	2849
	Examiner Name	CHENG, Diana
	Attorney Docket Number	00287-0017

	1	XILINX, "7 Series FPGAs GTX/GTH Transceivers - User Guide," Page 26, available at https://www.xilinx.com/support/documentation/user_guides/ug476_7Series_Transceivers.pdf (August 14, 2018).	
	2	SARAH HARRIS, "Timing & Synchronization," Harvey Mudd College Engineering Department, Page 24, available at https://cseweb.ucsd.edu/classes/wi06/cse291-b/slide/let4/timingint.pdf (January 31, 2006).	
	3	SAM PALERMO, "ECEN 720 High-Speed Links: Circuits and Systems - Lab 5," Texas A&M University, Page 5, available at: http://ece.tamu.edu/~spalermo/ecen689/ECEN720_lab5_2017.pdf (2017).	
	4	ALTERA, "Stratix V Device Handbook," Volume 2: Transceivers, Intel, Page 13, available at: https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/hb/stratix-v/stx5_xcvr.pdf (February 15, 2017).	
	5	STACKEXCHANGE, "Phase Frequency Detector in PLL," StackExchange, available at: https://electronics.stackexchange.com/questions/301402/phase-frequency-detector-in-pll (April 24, 2017).	
	6	IEEE STANDARDS ASSOCIATION, "IEEE Standards for Ethernet," IEEE 802.3-2018, Section 4, Clauses 49 and 51, Section 6, Clauses 82 and 83, available at: https://standards.ieee.org/standard/802_3-2018.html (August 31, 2018).	
	7	SLOBODAN MILIJEVIC, "The basics of synchronized Ethernet," EE Times-Asia, available at: https://www.microsemi.com/document-portal/doc_view/126475-the-basics-of-synchronized-ethernet-synce.	
	8	MACIEJ LIPINSKI, et al., "White Rabbit: a PTP Application for Robust Sub-nanosecond Synchronization," 2011 IEEE International Symposium on Precision Clock Synchronization for Measurement, Control and Communication, Munich, Pages 25-30, available at: http://white-rabbit.web.cern.ch/documents/White_Rabbit-a_PTP_application_for_robust_sub-nanosecond_synchronization.pdf (2011).	
	9	FLOYD M. GARDNER, "Phaselock Techniques," Third Edition, Wiley-Interscience, Chapters 1, 4, 9, 10, 11, 13, and 17 (2005).	
	10	JENS TWIEFEL, et al., "Digital signal processing for an adaptive phase-locked loop controller," Proceedings of SPIE - The International Society for Optical Engineering, Volume 6926 (April 2008).	
	11	CHEN YAO, "Time to Digital Converter used in ALL digital PLL," Master of Science Thesis In System-on-Chip Design, Stockholm (August 2011).	

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	Art Unit	2849
	Examiner Name	CHENG, Diana
	Attorney Docket Number	00287-0017

	12	BEHZAD RAZAVI, "A CIRCUIT FOR ALL SEASONS: The StrongARM Latch," IEEE Solid-State Circuits Magazine (Spring 2015).
	13	PING LU, et al., "A 2-D GRO Vernier Time-to-Digital Converter with Large Input Range and Small Latency," Lund University - EIT Department, University of Toronto, IEEE Radio Frequency Integrated Circuits Symposium (2013).
	14	CHRISTIAN LEBER, et al. "High Frequency Trading Acceleration using FPGAs," University of Heidelberg, International Conference on Field Programmable Logic and Applications, Germany (2011).
	15	INTERNATIONAL TELECOMMUNICATION UNION, "Timing and synchronization aspects in packet networks," ITU-T, G.8261/Y.1361, International Telecommunication Union (May 2006).
	16	INTERNATIONAL TELECOMMUNICATION UNION, "Distribution of timing information through packet networks," ITU-T, G.8264/Y.1364, International Telecommunication Union (August 2017).
	17	IEEE STANDARDS ASSOCIATION, "IEEE Standards for Ethernet," IEEE 802.3-2018, Section 4, Figure 52-4, page 634 (2018)

If you wish to add additional non-patent literature document citation information please click the Add button Add

EXAMINER SIGNATURE

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	17723145
	Filing Date	2022-04-18
	First Named Inventor	Nima Badizadegan
	Art Unit	2849
	Examiner Name	CHENG, Diana
	Attorney Docket Number	00287-0017

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Keith J. Barkaus/	Date (YYYY-MM-DD)	2022-06-02
Name/Print	Keith J. Barkaus	Registration Number	51,431

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

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6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt

EFS ID:	45861122
Application Number:	17723145
International Application Number:	
Confirmation Number:	1635
Title of Invention:	FIELD PROGRAMMABLE GATE ARRAY WITH EXTERNAL PHASE-LOCKED LOOP
First Named Inventor/Applicant Name:	Nima Badizadegan
Customer Number:	1912
Filer:	Keith J. Barkaus/Victoria Gilmore
Filer Authorized By:	Keith J. Barkaus
Attorney Docket Number:	00287-0017
Receipt Date:	02-JUN-2022
Filing Date:	18-APR-2022
Time Stamp:	15:09:49
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal Letter	1-TransmittalLetter.pdf	125626 48294afca9e4bf4dc4c150eda394203384ce9560	no	3

Warnings:

Information:					
2	Information Disclosure Statement (IDS) Form (SB08)	2-IDS.pdf	622178 946afba4fe4ca6d02f73fbd979fe873ae216a3d3	no	6
Warnings:					
Information:					
			Total Files Size (in bytes):	747804	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	: HFT Solutions, LLC	Confirmation No.: 1635
Application No.	: 17/723,145	
Filed	: April 18, 2022	
For	: FIELD PROGRAMMABLE GATE ARRAY WITH EXTERNAL PHASE-LOCKED LOOP	
TC/A.U.	: 2849	
Examiner	: CHENG, Diana	
Docket No.	: 00287-0017	
Customer No.	: 01912	

INFORMATION DISCLOSURE STATEMENT LETTER
UNDER 37 CFR § 1.56

Via EFS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with the duty of disclosure under 37 C.F.R. § 1.56, Applicant would like to direct the Examiner's attention to the references that are listed on the attached forms PTO/SB/08A. In addition to any copies of Foreign Patent Documents and Non-Patent Literature Documents submitted herewith, Applicant refers the Examiner to the references previously submitted to or cited by the Patent Office during prosecution of U.S. Patent Application No. 17/405,188 filed August 18, 2021, U.S. Patent Application No. 17/248,304 filed January 19, 2021, now U.S. Patent No. 11,128,305, U.S. Patent Application No. 16/937,314 filed July 23, 2020, now U.S. Patent No. 10,931,286 and U.S. Patent Application No. 16/672,076 filed November 1, 2019, now U.S. Patent No. 10,826,502 from which the subject application claims priority under 35 U.S.C. § 120. Accordingly, pursuant to 37 C.F.R. § 1.98(d), copies of previously cited or submitted references and Non-Patent Literature Documents are not included with this Information Disclosure Statement.

Citadel Securities LLC, Exhibit 1003, Page 190 of 290

Reference to Related Patents and Co-Pending Applications

The below chart provides information regarding related issued patents and co-pending applications filed by the present Applicant:

SERIAL NO.	ATTORNEY DOCKET NO.	FILING DATE	STATUS
16/672,076	00287-0007	2019-11-01	Issued USP 10,826,502
16/670,702	00287-0008	2019-10-31	Issued USP 10,771,069
16/888,218	00287-0009	2020-05-29	Issued USP 10,763,865
16/937,314	00287-0011	2020-07-23	Issued USP 10,931,286
16/937,309	00287-0012	2020-07-23	Issued USP 11,018,678
17/248,304	00287-0013	2021-01-19	Issued USP 11,128,305
17/236,577	00287-0014	2021-04-21	Issued USP 11,329,655
17/405,188	00287-0015	2021-08-18	Allowed – Notice of Allowance mailed 2022-05-25
17/723,130	00287-0016	2022-04-18	Docketed New Case - Ready for Examination
17/723,145	00287-0017	2022-04-18	Present Application

The Examiner is invited to review the prosecution history of each of these applications, including the cited references of record and related office actions, as the Examiner deems appropriate.

* * * * *

As provided by 37 C.F.R. § 1.97(g) and (h), no representation is being made that a search has been conducted or that this statement encompasses all the possible relevant information, and no inference should be made that the information and references cited are, or are considered to be, material to patentability because they are in this statement. No inference should be made that the information and references cited are prior art merely because they are in the statement.

Since this Information Disclosure Statement is being filed within three months of the filing date and before the mailing date of a first Office Action on the merits in the present application, Applicant believes that no fee is required in connection with the filing of this Statement. Applicant(s) hereby petition(s) that the Information Disclosure Statement be considered. Please charge any fee deficiency or credit any overpayment to Deposit Account No.

01-1785 as needed to ensure consideration of the disclosed information under order no. 00287-0017.

Respectfully submitted

AMSTER, ROTHSTEIN & EBENSTEIN LLP
Attorneys for Applicant
90 Park Avenue
New York, NY 10016
(212) 336-8000

Dated: New York, New York
June 2, 2022

By: /Keith J. Barkaus /
Keith J. Barkaus
Reg. No. 51,431

Citadel Securities LLC, Exhibit 1003, Page 192 of 290

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/723,145	04/18/2022	Nima Badizadegan	00287-0017	1635

1912 7590 05/19/2022

AMSTER, ROTHSTEIN & EBENSTEIN LLP
90 PARK AVENUE
NEW YORK, NY 10016

EXAMINER	
CENTRAL, DOCKET	

ART UNIT	PAPER NUMBER
2849	

MAIL DATE	DELIVERY MODE
05/19/2022	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Decision Granting Request for Prioritized Examination (Track I)	**Application No.** 17/723,145	**Applicant(s)** Badizadegan, Nima	
	Examiner FIKIRTE A GEREMEW	**Art Unit** OMBL	**AIA (FITF) Status** Yes

1. THE REQUEST FILED 18 April 2022 IS **GRANTED** .

The above-identified application has met the requirements for prioritized examination

A. ☑ for an original nonprovisional application (Track I).
B. ☐ for an application undergoing continued examination (RCE).

2. **The above-identified application will undergo prioritized examination**. The application will be accorded special status throughout its entire course of prosecution until one of the following occurs:

A. filing a **petition for extension of time** to extend the time period for filing a reply;

B. filing an **amendment to amend the application to contain more than four independent claims, more than thirty total claims** , or a multiple dependent claim;

C. filing a **request for continued examination** ;

D. filing a notice of appeal;

E. filing a request for suspension of action;

F. mailing of a notice of allowance;

G. mailing of a final Office action;

H. completion of examination as defined in 37 CFR 41.102; or

I. abandonment of the application.

Telephone inquiries with regard to this decision should be directed to FIKIRTE GEREMEW at (703) 756-1930. In his/her absence, calls may be directed to Petition Help Desk at (571) 272-3282.

/CHERYL GIBSON BAYLOR/ Paralegal Specialist, OPET	

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
17/723,145	04/18/2022	2842	830	00287-0017	12	1

CONFIRMATION NO. 1635

1912
AMSTER, ROTHSTEIN & EBENSTEIN LLP
90 PARK AVENUE
NEW YORK, NY 10016

FILING RECEIPT

OC000000133355257

Date Mailed: 04/22/2022

Receipt is acknowledged of this non-provisional utility patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF FIRST INVENTOR, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection.

Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please submit a written request for a corrected Filing Receipt, including a properly marked-up ADS showing the changes with strike-through for deletions and underlining for additions. If you received a "Notice to File Missing Parts" or other Notice requiring a response for this application, please submit any request for correction to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections provided that the request is grantable.

Inventor(s)

Nima Badizadegan, Salem, NH;

Applicant(s)

HFT Solutions, LLC, New Canaan, CT;

Power of Attorney: The patent practitioners associated with Customer Number 01912

Domestic Priority data as claimed by applicant

This application is a CON of 17/405,188 08/18/2021
which is a CON of 17/248,304 01/19/2021 PAT 11128305
which is a CON of 16/937,314 07/23/2020 PAT 10931286
which is a CON of 16/672,076 11/01/2019 PAT 10826502
which claims benefit of 62/803,017 02/08/2019
and claims benefit of 62/755,804 11/05/2018

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.
Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access Application via Priority Document Exchange: Yes

Permission to Access Search Results: Yes

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

If Required, Foreign Filing License Granted: 04/21/2022

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 17/723,145**

Projected Publication Date: Request for Non-Publication Acknowledged

Non-Publication Request: Yes

Early Publication Request: No

**** SMALL ENTITY ****

Title

FIELD PROGRAMMABLE GATE ARRAY WITH EXTERNAL PHASE-LOCKED LOOP

Preliminary Class

327

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific

countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

SelectUSA

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The U.S. offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to promote and facilitate business investment. SelectUSA provides information assistance to the international investor community; serves as an ombudsman for existing and potential investors; advocates on behalf of U.S. cities, states, and regions competing for global investment; and counsels U.S. economic development organizations on investment attraction best practices. To learn more about why the United States is the best country in the world to develop

technology, manufacture products, deliver services, and grow your business, visit http://www.SelectUSA.gov or call +1-202-482-6800.

Citadel Securities LLC, Exhibit 1003, Page 198 of 290

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 17/723,145

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	80		N/A	
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	350		N/A	
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	400		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	12 minus 20 =	*	x 50 =	0.00	OR		
INDEPENDENT CLAIMS (37 CFR 1.16(h))	1 minus 3 =	*	x 240 =	0.00			
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			0.00			
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				0.00			
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	830		TOTAL	

APPLICATION AS AMENDED - PART II

AMENDMENT A

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
Application Size Fee (37 CFR 1.16(s))									
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

AMENDMENT B

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE($)	ADDITIONAL FEE($)		RATE($)	ADDITIONAL FEE($)
Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
Application Size Fee (37 CFR 1.16(s))									
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

Doc Code: TRACK1.REQ
Document Description: TrackOne Request

PTO/AIA/424 (04-14)

CERTIFICATION AND REQUEST FOR PRIORITIZED EXAMINATION UNDER 37 CFR 1.102(e) (Page 1 of 1)

First Named Inventor:	Nima Badizadegan	Nonprovisional Application Number (if known):	
Title of Invention:	FIELD PROGRAMMABLE GATE ARRAY WITH EXTERNAL PHASE-LOCKED LOOP		

APPLICANT HEREBY CERTIFIES THE FOLLOWING AND REQUESTS PRIORITIZED EXAMINATION FOR THE ABOVE-IDENTIFIED APPLICATION.

1. The processing fee set forth in 37 CFR 1.17(i)(1) and the prioritized examination fee set forth in 37 CFR 1.17(c) have been filed with the request. The publication fee requirement is met because that fee, set forth in 37 CFR 1.18(d), is currently $0. The basic filing fee, search fee, and examination fee are filed with the request or have been already been paid. I understand that any required excess claims fees or application size fee must be paid for the application.

2. I understand that the application may not contain, or be amended to contain, more than four independent claims, more than thirty total claims, or any multiple dependent claims, and that any request for an extension of time will cause an outstanding Track I request to be dismissed.

3. The applicable box is checked below:

I. ☑ Original Application (Track One) - Prioritized Examination under § 1.102(e)(1)

i. (a) The application is an original nonprovisional utility application filed under 35 U.S.C. 111(a). This certification and request is being filed with the utility application via EFS-Web.

---OR---

(b) The application is an original nonprovisional plant application filed under 35 U.S.C. 111(a). This certification and request is being filed with the plant application in paper.

ii. An executed inventor's oath or declaration under 37 CFR 1.63 or 37 CFR 1.64 for each inventor, **or** the application data sheet meeting the conditions specified in 37 CFR 1.53(f)(3)(i) is filed with the application.

II. ☐ Request for Continued Examination - Prioritized Examination under § 1.102(e)(2)

i. A request for continued examination has been filed with, or prior to, this form.
ii. If the application is a utility application, this certification and request is being filed via EFS-Web.
iii. The application is an original nonprovisional utility application filed under 35 U.S.C. 111(a), or is a national stage entry under 35 U.S.C. 371.
iv. This certification and request is being filed prior to the mailing of a first Office action responsive to the request for continued examination.
v. No prior request for continued examination has been granted prioritized examination status under 37 CFR 1.102(e)(2).

Signature /Keith J. Barkaus/	Date 2022-04-18
Name (Print/Typed) Keith J. Barkaus	Practitioner Registration Number 51,431

Note: *This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4(d) for signature requirements and certifications. Submit multiple forms if more than one signature is required.**

☑ *Total of 1 forms are submitted.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

PTO/AIA/01 (06-12)
Approved for use through 11/30/2020. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of Invention	FIELD PROGRAMMABLE GATE ARRAY WITH EXTERNAL PHASE-LOCKED LOOP

As the below named inventor, I hereby declare that:

This declaration is directed to:

- [x] The attached application, or
- [ ] United States application or PCT international application number _____

  filed on _____.

The above-identified application was made or authorized to be made by me.

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LEGAL NAME OF INVENTOR

Inventor: Nima Badizadegan Date (Optional): _____

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Application Number	
Filing Date	Herewith
First Named Inventor	Nima Badizadegan
Title	FIELD PROGRAMMABLE GATE ARRAY WITH EXTERNAL PHASE-LOCKED LOOP
Art Unit	
Examiner Name	
Attorney Docket Number	00287-0017

SIGNATURE of Applicant or Patent Practitioner

Signature	/Keith J. Barkaus/	Date (Optional)	2022-04-18
Name	Keith J. Barkaus	Registration Number	51,431
Title (if Applicant is a juristic entity)			
Applicant Name (if Applicant is a juristic entity)			

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The undersigned (whose title is supplied below) is authorized to act on behalf of the applicant (e.g., where the applicant is a juristic entity).

Signature		Date (Optional)	04/04/2022
Name	Corey Horowitz		
Title	Chairman and Chief Executive Officer		

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FIELD PROGRAMMABLE GATE ARRAY WITH EXTERNAL PHASE-LOCKED LOOP

REFERENCE TO RELATED APPLICATIONS

[0001] This application is a continuation of U.S. Application No. 17/405,188, filed on August 18, 2021 and entitled FIELD PROGRAMMABLE GATE ARRAY WITH EXTERNAL PHASE-LOCKED LOOP, which is a continuation of U.S. Patent Application No. 17/248,304, filed on January 19, 2021 and entitled FIELD PROGRAMMABLE GATE ARRAY WITH EXTERNAL PHASE-LOCKED LOOP, which is a continuation of U.S Application No. 16/937,314, filed on July 23, 2020 and entitled FIELD PROGRAMMABLE GATE ARRAY WITH EXTERNAL PHASE-LOCKED LOOP which in turn is a continuation of U.S. Application No. 16/672,076, filed on November 1, 2019 and entitled FIELD PROGRAMMABLE GATE ARRAY WITH EXTERNAL PHASE-LOCKED LOOP which in turn claims the benefit of and priority to U.S. Provisional Patent Application No. 62/755,804, filed on November 5, 2018 and entitled FIELD PROGRAMMABLE GATE ARRAY WITH EXTERNAL PHASE-LOCKED LOOP, and U.S. Provisional Patent Application No. 62/803,017, filed on February 8, 2019 and entitled FIELD PROGRAMMABLE GATE ARRAY WITH EXTERNAL PHASE-LOCKED LOOP, the entire content of each of which is hereby incorporated by reference herein.

FIELD

[0002] The present invention generally relates to a field programmable gate array system. In embodiments, the present invention generally relates to a field programmable gate array and an external phase controller providing phase matching between a receiver clock and a transmitter clock used in the field programmable gate array.

BACKGROUND

[0003] Field programmable gate arrays (FPGAs) may be used in applications that require fast processing since FPGAs allow for all computations to occur on a single chip that has massive fine-grained parallelism. For example, FPGAs are used in the financial industry in high frequency trading where the rapid processing of the FPGA is desired. One technological problem with

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FPGAs is that there is a need to synchronize receiving side and transmitting side clock signals within the FPGA. The prior art sought to address this problem by including a clock domain crossing circuit in the FPGA, however, these circuits inherently add a delay to the processing that takes place in the FPGA, which is not desirable since high frequency trading may include timestamps that are accurate to the microsecond such that even small delays may present a large problem.

[0004] Accordingly, a technical problem is presented in FPGAs in that phase synchronization between the receiver side clock and the transmitter side clock will introduce unwanted latency that results in delay of processing. Accordingly, it would be beneficial to provide an FPGA system that avoids these problems and provides sub-microsecond processing with throughput of at least 10 Gbps. In embodiments, the sub-microsecond processing throughput may be: 10-25 Gbps, 22-33 Gbps, 33-45 Gbps, 45-60 Gbps, 60-80Gbps, 80-120 Gbps, to name a few.

SUMMARY

[0005] An object of the present invention is to address technological challenges that currently exist in phase matching receiver side and transmitter side clocks of a FPGA without introducing unnecessary delay in processing.

[0006] This and other objects shall be addressed by embodiments of the present invention as set forth herein.

[0007] The present invention generally relates to a field programmable gate array system. In embodiments, the present invention generally relates to a field programmable gate array and an external phase controller providing phase matching between a receiver clock and a transmitter clock used in the field programmable gate array.

[0008] In embodiments, a field programmable gate array system includes (a) a field programmable gate array comprising (1) a first interface including: (A) a first reference clock pin, wherein said first reference clock pin is configured to receive a first clock signal having a first frequency and a first phase; (B) a second reference clock pin, wherein said second reference clock pin is configured to receive a second clock signal having a second frequency and a second phase; (C) a first plurality of data pins, wherein said first plurality of data pins is configured to receive a

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first serial data stream; (D) a second plurality of data pins, wherein said second plurality of data pins is configured to transmit a second serial data stream; (2) a deserializer operationally connected to: (x) the first reference clock pin to receive as a first input the first clock signal and (y) the first plurality of data pins to receive as a second input the first serial data stream, and wherein the deserializer is configured to: (A) convert the first serial data stream into a first plurality of parallel data streams having a first amount of data streams, and (B) generate a first receiver side clock signal based on the first clock signal, wherein the first receiver side clock signal has a third frequency and a third phase; and (C) transmit the first plurality of parallel data streams and the first receiver side clock signal within the field programmable gate array; (3) computational circuitry operationally connected to the deserializer to receive the first plurality of parallel data streams and the first receiver side clock signal, wherein the computational circuitry is configured to perform a first set of operations on the first plurality of parallel data streams to generate a second plurality of parallel processed data streams having a second amount of data streams; (4) a serializer operationally connected to: (x) the second reference clock pin to receive as a third input a first wire rate clock signal based on the second clock signal, wherein the first wire rate clock signal has a fourth frequency and a fourth phase; (y) the second plurality of data pins to transmit as a first output the second serial data stream; (z) the computational circuity, wherein the serializer receives the second plurality of parallel processed data streams from the computational circuity and the serializer transmits to the computational circuitry a first transmitter side clock signal including a fifth frequency and a fifth phase; and wherein the serializer is configured to: (A) convert the second plurality of parallel processed data streams into the second serial data stream; (B) generate the first transmitter side clock signal based on the first wire rate signal, wherein the first transmitter side clock signal has the fifth frequency and the fifth phase, wherein the fifth frequency is different than and less than the fourth frequency; and (C) transmit the second serial data stream to the second plurality of data pins for transmission off the field programmable gate array; (5) a second interface including: (A) a first clock output pin configured to transmit the first receiver side clock signal, wherein the first clock output pin is operationally connected to the deserializer; and (B) a second clock output pin configured to transmit the first transmitter side clock signal, wherein the second clock output pin is operationally connected to the serializer; and (b) a phase control circuit, provided outside of the field programmable gate array, wherein the phase control circuit includes: (1) a phase detector operationally connected to the first clock output pin and the second clock

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output pin of the second interface of the field programmable gate array, and wherein the phase detector is configured to compare the third phase of the receiver side clock signal to the fifth phase of the transmitter side clock signal and to generate a phase difference indicator signal based on a difference between the third phase of the receiver side clock signal and the fifth phase of the transmitter side clock signal; (2) a phase controller operationally connected to the phase detector and configured to receive the phase difference indicator signal, and wherein the phase controller is configured to determine adjustment information based on the phase difference indicator signal; and (3) an adjustable oscillator operationally connected to the phase controller and configured to receive the adjustment information as well as operationally connected to the second reference clock pin of the first interface of the field programmable gate array, wherein the adjustable oscillator is configured to generate the second clock signal including the second frequency and the second phase based on the adjustment information and transmit the second clock signal to the second reference clock pin of the first interface of the field programmable gate array; wherein the transmitter side clock signal and the receiver side clock signal are phase aligned so that there is a fixed phase difference between the third phase and the fifth phase.

[0009] In embodiments, the third frequency corresponds to the first frequency.

[0010] In embodiments, the third phase is not aligned with the first phase.

[0011] In embodiments, the third frequency is different than the first frequency.

[0012] In embodiments, the first set of operations does not include clock domain crossing operations that delays processing of the first set of parallel data streams. In embodiments, the adjustment information is used to do at least one of the following (i) set a bias to an oscillator; (ii) to set a divider ratio; and (iii) to set a delay.

[0013] In embodiments, the first set of operations includes an arithmetic operation. In embodiments, the first set of operations includes a logical operation. In embodiments, the first set of operations includes a pipeline operation. In embodiments, the first set of operations includes a memory access operation.

[0014] In embodiments, the first amount of data streams is the same as the second amount of data streams.

[0015] In embodiments, the first amount of data streams and the second amount of data streams are equal to eight (8) data streams. In embodiments, the first amount of data streams and the second amount of data streams are equal to ten (10) data streams. In embodiments, the first amount of data streams and the second amount of data streams are equal to sixteen (16) data streams. In embodiments, the first amount of data streams and the second amount of data streams are equal to twenty (20) data streams. In embodiments, the first amount of data streams and the second amount of data streams are equal to thirty-two (32) data streams. In embodiments, the first amount of data streams and the second amount of data streams are equal to forty (40) data streams. In embodiments, the first amount of data streams and the second amount of data streams are equal to sixty-four (64) data streams. In embodiments, the first amount of data streams and the second amount of data streams are equal to eighty (80) data streams. In embodiments, the first amount of data streams and the second amount of data streams are equal to one hundred twenty-eight (128) data streams. In embodiments, the first amount of data streams and the second amount of data streams are equal to one hundred sixty (160) data streams.

[0016] In embodiments, the first amount of data streams and the second amount of data streams are equal to two (2) to the power of N, where N is an integer. In embodiments, the first amount of data streams and the second amount of data streams are equal to ten (10) times two (2) to the power of N, where N is an integer. In embodiments the first amount of data streams and the second amount of data streams are equal to thirty-three (33) times two (2) to the power of N, where N is an integer.

[0017] In embodiments, the field programmable gate array further includes a phase lock loop configured to: receive the second clock signal, as a fourth input, to generate the first wire rate clock signal; and (B) transmit the first wire rate clock signal as the third input, to the serializer.

[0018] In embodiments, the fourth frequency is equal to x times the fifth frequency, where x is the second amount of data streams.

[0019] In embodiments, the fourth frequency is equal to x times the fifth frequency, where x is half of the second amount of data streams.

[0020] In embodiments, the fourth frequency is a rational multiple of the second frequency.

[0021] In embodiments, the phase difference indicator signal is a pulse signal.

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[0022] In embodiments, the adjustment information indicates a desired phase. In embodiments, the adjustment information indicates a desired frequency. In embodiments, the adjustment information indicates a change in phase. In embodiments, the adjustment information indicates a change in frequency. In embodiments, adjustment information comprises a voltage. In embodiments, adjustment information comprises a digital transmission. In embodiments adjustment information further comprises a digital transmission.

[0023] In some embodiments, the first serial data stream comprises market data, the second serial data stream comprises order entry data, and the first operation comprises a trading algorithm.

[0024] In embodiments, the trading algorithm includes the steps of: (a) parsing market data; (b) performing mathematical operations at a portion of the market data; and (c) generating order packets using at least an output of (b).

[0025] In embodiments, the first serial data stream includes market data and the second serial stream includes trading data.

[0026] In embodiments, the field programmable gate array includes a transceiver phase locked loop operatively connected between the to the serializer and the first reference clock pin.

[0027] In embodiments, the transceiver phase locked loop operatively connected between the serializer and the first reference clock pin includes a second adjustable oscillator to provide the first wire rate signal.

[0028] In embodiments, a second adjustable oscillator is provided outside of the transceiver phase locked loop and operatively connected to the serializer.

[0029] In embodiments, the second adjustable oscillator is programmable with a desired delay.

[0030] In embodiments, the desired delay is a constant value

[0031] In embodiments, the constant value is zero.

[0032] In embodiments, the adjustment information is provided to the second adjustable oscillator to provide the first wire rate signal.

[0033] A method for processing a first serial data stream comprising market data, using a field programmable gate array system, to generate a second serial data stream comprising order

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entry data, wherein the method includes the steps of: (A) receiving, by a first plurality of data pins in a first interface of a field programmable gate array in the field programmable gate array system, the first serial data stream; (B) receiving, by a first reference clock pin in the first interface, a first clock signal having a first frequency and a first phase; (C) transmitting, from the first plurality of data pins in the first interface to a deserializer in the field programmable gate array, the first serial data stream; (D) transmitting, from the first reference clock pin in the first interface to the deserializer, the first clock signal; (E) generating, by the deserializer, a first receiver side clock signal having a second frequency and a second phase, based on the first clock signal; (F) converting, by the deserializer, the first serial data stream into a first plurality of parallel data streams; (G) transmitting, from the deserializer to computational circuitry in the field programmable gate array, the first receiver side clock signal; (H) transmitting, from the deserializer to the computational circuitry, the first plurality of data streams comprising a first plurality of data items and a first amount of data streams; (I) transmitting, from the deserializer via a first clock output pin on a second interface of the field programmable gate array to a phase detector that is part of the field programmable gate array system and not part of the field programmable gate array, the first receiver side clock signal; (J) generating, using the field programmable gate array system, a first transmitter side clock signal having a third frequency and a third phase, by performing the following steps until a first output of the phase detector is below a first threshold level: (i) generating, by an adjustable oscillator in the field programmable gate array system, a second clock signal having a fourth frequency and a fourth phase; (ii) generating a first wire rate clock signal having a fifth frequency and a fifth phase based on the second clock signal; (iii) generating, by a serializer in the field programmable gate array, an interim transmitter side clock signal having a sixth frequency and a sixth phase; (iv) transmitting, from the serializer via a second clock output pin in the second interface to the phase detector, the interim transmitter side clock signal; (v) generating, by the phase detector, the first output based on a comparison of the first receiver side clock signal and the interim transmitter side clock signal; (vi) transmitting, from the phase detector to a phase controller of the field programmable gate array system which is not in the field programmable gate array, the first output; (vii) determining, by the phase controller, interim adjustment information based on the first output; and (viii) transmitting, from the phase controller to the adjustable oscillator, the interim adjustment information; wherein, the adjustable oscillator adjusts the second clock signal based on the interim adjustment information and steps (i) through

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(viii) are repeated until the first output of the phase detector is below the first threshold level; (K) transmitting, from the serializer to the computational circuitry, first transmitter side clock signal; (L) performing, by the computational circuitry, a first set of operations on at least a portion of the first plurality of data items to generate a second plurality of parallel data streams comprising a second amount of data streams; (M) transmitting, from the computational circuitry to the serializer, the second plurality of parallel data streams; (N) converting, by the serializer, the second plurality of parallel data streams into the second serial data stream; and (O) transmitting, from the serializer off the field gate programmable array system via a second plurality of data pins in the first interface, the second serial data stream.

[0034] In embodiments, step (a) is performed before step (b).

[0035] In embodiments, step (b) is performed before step (a).

[0036] In embodiments, step (a) and step (b) are performed contemporaneously.

[0037] In embodiments, step (c) is performed before step (d).

[0038] In embodiments, step (d) is performed before step (c).

[0039] In embodiments, step (c) and step (d) are performed contemporaneously.

[0040] In embodiments, step (e) is performed before step (f).

[0041] In embodiments, step (f) is performed before step (e).

[0042] In embodiments, step (e) and step (f) are performed contemporaneously.

[0043] In embodiments, the second frequency corresponds to the first frequency.

[0044] In embodiments, the second phase is not aligned with the first phase.

[0045] In embodiments, the second frequency is different from the first frequency.

[0046] In embodiments, step (g) is performed before step (h).

[0047] In embodiments, step (h) is performed before step (g).

[0048] In embodiments, step (g) and step (h) are performed contemporaneously.

[0049] In embodiments, the transmission of the first receiver side clock signal from the deserializer to the phase detector is also via a first zero delay buffer phase lock loop of the field

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programmable gate array before being transmitted via the first clock output pin of the second interface.

[0050] In embodiments, the third frequency corresponds to the second frequency.

[0051] In embodiments, the third phase is aligned with the second phase.

[0052] In embodiments, a difference between the third phase and the second phase is less than a second threshold level.

[0053] In embodiments, the sixth frequency corresponds to the third frequency.

[0054] In embodiments, the sixth phase is not aligned with the third phase prior to the first output of the phase detector being below the first threshold level.

[0055] In embodiments, the transmission of the interim transmitter side clock signal from the serializer to the phase detector is also via a second zero delay buffer phase lock loop of the field programmable gate array before being transmitted via the second clock output pin of the second interface.

[0056] In embodiments, the first set of operations does not include clock domain crossing operations that delays processing of the first set of parallel data streams.

[0057] In embodiments, the first amount of data streams is the same as the second amount of data streams.

[0058] In embodiments, the first amount of data streams and the second amount of data streams is eight (8) data streams. In embodiments, the first amount of data streams and the second amount of data streams is ten (10) data streams. In embodiments, the first amount of data streams and the second amount of data streams is sixteen (16) data streams. In embodiments, the first amount of data streams and the second amount of data streams is twenty (20) data streams. In embodiments, the first amount of data streams and the second amount of data streams is thirty-two (32) data streams. In embodiments, the first amount of data streams and the second amount of data streams is forty (40) data streams. In embodiments, the first amount of data streams and the second amount of data streams is sixty-four (64) data streams. In embodiments, the first amount of data streams and the second amount of data streams is eighty (80) data streams. In embodiments, the first amount of data streams and the second amount of data streams are equal to

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one hundred twenty-eight (128) data streams. In embodiments, the first amount of data streams and the second amount of data streams are equal to one hundred sixty (160) data streams.

[0059] In embodiments, the first amount of data streams and the second amount of data streams are equal to two (2) to the power of N, where N is an integer. In embodiments, the first amount of data streams and the second amount of data streams are equal to ten (10) times two (2) to the power of N, where N is an integer. In embodiments the first amount of data streams and the second amount of data streams are equal to thirty-three (33) times two (2) to the power of N, where N is an integer.

[0060] In embodiments, at least a portion of the first set of operations is performed prior to step (k).

[0061] In embodiments, at least a portion of the first set of operations is performed after step (k).

[0062] In embodiments, all of the first set of operations is performed after step (k).

[0063] In embodiments, the transmission of the second serial data stream from the serializer off the field programmable gate array is transmitted to an input/output module off the field programmable gate array.

[0064] In embodiments, the first serial data stream includes market data and the second serial data stream includes trading data.

[0065] In embodiments, the step of generating the first wire rate clock signal further includes: (a) receiving, from the adjustable oscillator at a transceiver phase lock loop via a second reference clock pin in the first interface, the second clock signal; (b) processing, by the transceiver phase lock loop, the received second clock signal; (c) providing, by the transceiver phase lock loop, the wire rate clock signal based on the processing of the received clock signal; and (d) transmitting, by the transceiver phase lock loop, the wire rate clock signal to the serializer.

[0066] In embodiments, a phase lock loop generates the first wire rate clock signal. In embodiments, the phase lock loop is on the field programmable gate array. In embodiments, the phase lock loop that is part of the field programmable gate array system and not part of the field programmable gate array.

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[0067] In embodiments, the step of generating the first wire rate clock signal further includes: (a) processing the second clock signal; (b)providing the wire rate clock signal based on the processing of the second clock signal; and (c) transmitting, to the serializer, the wire rate clock signal.

[0068] In embodiments, the sixth frequency corresponds to the third frequency. In embodiments, the sixth phase is not aligned with the third phase.

BRIEF DESCRIPTION OF THE DRAWINGS

[0069] Exemplary embodiments of the present invention will be described with references to the accompanying figures, wherein:

[0070] FIG. 1 is a block diagram of a conventional field programmable gate array;

[0071] FIG. 1A is a block diagram of an exemplary transceiver suitable for use in the field programmable gate array of FIG. 1;

[0072] FIG. 1B is an exemplary block diagram of a Clock Domain Crossing Circuit suitable for use in the field programmable gate array of FIG. 1;

[0073] FIG. 1C illustrates exemplary input output waveforms of the Clock Domain Crossing Circuit of the field programmable gate array of FIG. 1;

[0074] FIG. 2 is a block diagram of a field programmable gate array system in accordance with an embodiment of the present invention;

[0075] FIG. 3A is an exemplary block diagram of a deserializer suitable for use in the field programmable gate array system of FIG. 2 in accordance with an embodiment of the present invention;

[0076] FIG. 3B is an exemplary circuit diagram of a continuous-time linear equalizer (CTLE) suitable for use in the deserializer of FIG. 3A in accordance with an embodiment of the present invention;

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[0077] FIG. 3C is an exemplary block diagram of a clock and data recovery (CDR) circuit suitable for use in the deserializer of FIG. 3A in accordance with an embodiment of the present invention;

[0078] FIG. 3D is an exemplary circuit diagram of a decision circuit suitable for use in the deserializer of FIG. 3A in accordance with an embodiment of the present invention;

[0079] FIG. 3E is an exemplary block diagram of a deserializer suitable for use in the field programmable gate array system of FIG. 2 in accordance with an embodiment of the present invention;

[0080] FIG. 4A is an exemplary block diagram of a serializer suitable for use in the field programmable gate array system of FIG. 2 in accordance with an embodiment of the present invention;

[0081] FIG. 4B is an exemplary block diagram of a serializer suitable for use in field programmable gate array system of FIG. 2 in accordance with an embodiment of the present invention;

[0082] FIG. 5A is an exemplary block diagram of a phase detector suitable for use in the field programmable gate array system of FIG. 2 in accordance with an embodiment of the present invention;

[0083] FIG. 5B is another exemplary block diagram of a phase detector suitable for use in the field programmable gate array system of FIG. 2 in accordance with an embodiment of the present invention;

[0084] FIG. 5C is another exemplary block diagram of a phase detector suitable for use in the field programmable gate array system of FIG. 2 in accordance with an embodiment of the present invention;

[0085] FIG. 5D is another exemplary block diagram of a phase detector suitable for use in the field programmable gate array system of FIG. 2 in accordance with an embodiment of the present invention;

[0086] FIG. 6A illustrates an example of a phase difference between the receiver side clock and the transmitter side clock of an FPGA in accordance with an embodiment of the present invention;

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[0087] FIG. 6B illustrates an example of a phase difference between receiver clock and a transmitter clock of an FPGA in accordance with an embodiment of the present invention;

[0088] FIG. 6C illustrates an example of a phase difference between receiver clock and a transmitter clock of an FPGA in accordance with an embodiment of the present invention;

[0089] FIG. 6D illustrates an example of an inverted phase difference between receiver clock and a transmitter clock of an FPGA in accordance with an embodiment of the present invention;

[0090] FIG. 7A is a block diagram of a field programmable gate array system in accordance with another embodiment of the present invention;

[0091] FIG. 7B is a block diagram of another field programmable gate array system in accordance with another embodiment of the present invention;

[0092] FIG. 7C is a block diagram of another field programmable gate array system in accordance with another embodiment of the present invention;

[0093] FIG. 8A is a block diagram of another field programmable gate array system in accordance with an embodiment of the present invention; and

[0094] FIG. 8B is another block diagram of another field programmable gate array system in accordance with an embodiment of the present invention;

[0095] FIGs 9A-C are exemplary flow charts of a process implementing the field programmable gate array system in accordance with an embodiment of the present invention;

[0096] FIGs. 10A-10B are exemplary flow charts of a process for generating a transmitter side clock signal in accordance with an embodiment of the present invention; and

[0097] FIG. 11 is an exemplary flow chart of a process for generating a wire clock signal in accordance with an embodiment of the present invention.

DETAILED DESCRIPTION

[0098] The present invention generally relates to a field programmable gate array system. In embodiments, the present invention generally relates to a field programmable gate array and an

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external phase controller providing phase matching between a receiver clock and a transmitter clock used in the field programmable gate array.

[0099] FIG. 1 illustrates an exemplary schematic of a FPGA 100. Examples of currently available FPGAs include the XCVU3P-2FFVC1517E, Intel 1SG280LH3F55E3VG, Xilinx XCVU9P-2FLGA2104E the Vitrex® Ultrascale, the Vitrex® Ultrascale Plus, the Stratix® V, the Stratix® 10, XILINX XC3042, the Intel EP4CE6E22C8LN and the Lattice ICE40LP384-SG32, to name a few.

[0100] In embodiments, FPGA 100 may include an FPGA Core 106 and a number of peripheral systems. In embodiments, the FPGA Core 106 includes 4 main components: logic elements, digital signal processor blocks ("DSP blocks"), clock distribution components, and memories, to name a few, and may generally be referred to as the FPGA core, or simply logic core, 106. In embodiments, the peripheral systems may include CPU cores, reconfiguration controllers, security features, hardened logic functions, FPGA transceiver banks 102, hardened high-speed interface accelerators (e.g. PCIe or 100 GbE controllers, to name a few), general-purpose I/O pins, memory interface controllers, larger memories, analog components (e.g. ADCs or DACs to name a few), and 3D-stacked memories (e.g. HBM), to name a few. The FPGA Transceiver banks 102 receive serial data to be processed from outside the FPGA and then transmit serial data out of the FBGA after being processed by internal circuitry of the FPGA 100. Some FPGA's may not include FPGA Transceiver banks.

[0101] In embodiments, data may be received by a receiver side of the transceiver banks 102 in the FPGA 100 at rates such as 10 or 25 Gbps, to name a few. In embodiments, rates may be between a range of 9-25 Gbps, 10-25 Gbps, 22-33 Gbps, 33-45 Gbps, 45-60 Gbps, 60-80Gbps, or 80-120 Gbps, to name a few. An exemplary transceiver (including deserializer 104' and serializer 110') suitable for use in FPGA 100 is shown in FIG. 1A. In embodiments, the input data may be received from I/O module 120. The input data may then be deserialized, using deserializer 104, for example, and parallelized into parallel data streams, such as 16-64 bits wide at $1/16^{th}$ to $1/64^{th}$ of the frequency of the incoming data stream, to name a few. In embodiments, FPGA transceivers may support parallel streams with widths of, for example, 8 bits, 10 bits, 16 bits, 20 bits, 32 bits, 40 bits, 64 bits, 80 bits, 128 bits, and 160 bits (with corresponding clock division), to name a few. In some FPGAs, a physical coding sublayer (PCS) may be used in the

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transceiver 102. In some FPGAs, the PCS of the transceiver 102 may be bypassed and so that the corresponding PCS functions may be done in the FPGA core 106. After deserialization, data is available for computation in the FPGA logic core 106 where computation is completed. In embodiments, the computation of the data may be computed by receive-side computation 110a of the FPGA core 106. Similarly, data may be computed by the transmit-side computation 110b.

[0102] In embodiments, a REFERENCE CLOCK signal is provided, by Oscillator or Clock Generator 122, to both the deserializer 104 and the serializer 110. The REFERENCE CLOCK signal is received by the serializer 110 via the transceiver PLL 108 (Phase-Locked Loop). The receiver side clock signal RXCLOCK, however, is different in both frequency and phase from the REFERENCE CLOCK based on the deserialization process that occurs in the deserializer 104. Similarly, the transmitter clock signal TXCLOCK, while based on the REFERNCE CLOCK signal varies in frequency and phase based on processing that occurs in the serializer 110. As a result, the RXCLOCK signal and TXCLOCK signal will be out of phase. A known solution to this issue is the inclusion of the RX to TX clock domain crossing circuit 112. An exemplary Clock Domain Crossing circuit is suitable for use in FPGA 100 is shown as clock domain crossing circuit 112' in connection with FIG. 1B. As is noted above, the inclusion of the RX to TX clock domain crossing circuit 112 creates a technical problem, introducing an inherent delay in the FPGA 100, which is undesirable. The technical problem of an inherent delay is illustrated in FIG. 1C. FIG. 1C illustrates an example of a phase difference between the receiver side clock and the transmitter side clock of the conventional field programmable gate array of FIG. 1.

[0103] Thereafter, the data it transmitted out of the FPGA 100. After all computation (computation by receive-side computation 110a and/or transmit-side computation 110b) and clock domain crossing (by RX to TX clock domain crossing 112) is completed, the data goes back to the transmit side of the FPGA transceiver 102 to be serialized by the serializer 110 out on an output wire. The serializer 110 (e.g. the transmitter) typically runs off of a fast clock generated (e.g. 10 Gbps, 25 Gbps, or a range from 10 Gbps to 25 Gbps, or a range from 1Gbps to 100 Gbps, to name a few) by the transceiver phase-locked loop 108 within the transceiver bank 102 from a reference clock signal received by oscillator or clock generator 122.

[0104] The receiver (deserializer 104) and transmitter (serializer 110) of the transceiver 102 operate on different clocks that are independently generated within the transceiver 102. The

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receiver clock domain is typically generated by a clock and data recovery (CDR) circuit from the incoming data stream. The transmitter clock is typically generated by the transceiver phase-locked loop 108. In conventional FPGAs, phase matching or synchronizing is provided using the clock domain crossing circuit 112 that adjusts the phases of the two clock domains. The clock domain crossing circuit 112 may be an asynchronous FIFO or an asynchronous gearbox, to name a few. In embodiments, domain crossing circuit 112 may be a mesochronous clock crossing circuit. In embodiments, clock domain crossing circuit 112 may be instantiated within transceiver 102 of FPGA 100, although this structure has a higher latency cost than implementing it in logic fabric 106 of FPGA 100. As discussed above, a significant drawback of the clock domain crossing circuit 112 is that it adds latency related to the phase difference between the clocks plus the latency of the synchronizers used, and does not perform any computation, such that it slows the effective processing speed of FPGA 100.

[0105] FIG. 2 illustrates a block diagram of a field programmable gate array (FPGA) system in accordance with an embodiment of the present disclosure that provides phase control while minimizing latency. In embodiments, the system generally includes FPGA 2100 which preferably includes FPGA transceiver banks 2102. In embodiments, the FPGA transceiver banks 2102 includes deserializer 2104 on the receiver end of FPGA 2100, transceiver PLL 2108, and serializer 2110 on the transmitter end of FPGA 2100. Deserializer 2104 may be similar to the deserializer 2014' and deserializer 2104'' discussed below in connection with FIGS. 3A-3E, the descriptions of which applying herein. Serializer 2110 may be similar to serializer 2110' and serializer 2110'' discussed below in connection with FIGS. 4A and 4B respectively, the descriptions of which applying herein. In embodiments, deserializer 2104 receives a serial data stream via a first plurality of data pins in a first interface from the I/O module 2120 and provides deserialized data to the FPGA core 2106. More specifically, the deserializer 2104 will provide parallel data streams to the FPGA core 2106 for processing. As illustrated, this parallel data is provided to receiver side computational element 2210a where processing and computation takes place. The resulting data may then be provided to transmitting side computational element 2210b where additional computation and processing may take place. FIG. 2 illustrates computational logic 2210 as a single element. In embodiments, the computational logic 2210 may be implemented as a plurality of logic elements. In embodiments, computational logic 2210 may also include one or more of the following: RAM blocks or dedicated hardened accelerators. In

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embodiments, when all computation is complete, the resulting data may be provided to serializer 2110 and then transmitted out of FPGA 2100, preferably via I/O module 2120, for example. In embodiments, the I/O module 2120 may be a direct soldered cable, on-chip optics, or an on-board optical transceiver, to name a few. I/O Module 2120, may be, for example, a Samtec® I/O Module Firefly® I/O Module, to name a few. Additionally, the I/O module may be designed to meet one or more of the following standards: SFP, a QSFP, a MicroQSFP, QSFPDD to QSFP-DD, or a QSFPDD, to name a few.

[0106] FPGA 2100, in embodiments may include one or more interfaces, such as pins. By way of example, a first interface of the one or more interfaces, may include a first plurality of pins of FPGA 2100. The first plurality of pins may be used to transmit and/or receive data and/or signals. In embodiments, the first plurality of pins may include a first reference clock pin. The first reference clock pin may be operationally connected to deserializer 2104. In embodiments, the first reference clock pin may also be operationally connected to fixed-frequency oscillator 2000 such that a first clock signal having a first phase and a first phase may be transmitted from fixed-frequency oscillator 2000 to deserializer 2104 via the first reference clock pin. In embodiments, the first clock signal may have a frequency between 50 and 800 MHz.

[0107] In embodiments, the first plurality of pins may also include a second reference clock pin. The second reference clock pin may, in embodiments, be operationally connected to transceiver PLL 2108. The second reference clock pin, in embodiments, may be operationally connected to frequency or phase adjustable oscillator 2200 such that a second clock signal having a second phase and a second frequency may be transmitted from the frequency or phase-adjustable oscillator 2200 to transceiver PLL 2108 via the second reference clock pin. In embodiments, the second reference clock pin may be operationally connected to serializer 2110 such that the second clock signal may be transmitted from the frequency or phase-adjustable oscillator 2200 to serializer 2110 via the second reference clock pin. In embodiments, the second reference clock pin may also receive a first wire rate clock signal.

[0108] In embodiments, the first plurality of pins may also include a first plurality of data pins. The first plurality of data pins may be operationally connected deserializer 2104. In embodiments, the first plurality of data pins may also be operationally connected to I/O module 2120 such that a first serial data stream may be transmitted from external connection 2122

to deserializer via the I/O module 2120 and the first plurality of data pins. In embodiments, the first serial data stream may range between 10 to 25 Gbps.

[0109] In embodiments, the first plurality of pins may also include a second plurality of data pins. The second plurality of data pins may be operationally connected to serializer 2110. In embodiments, the second plurality of data pins may also be operationally connected to I/O module 2120 such that a second serial data stream may be transmitted from serializer 2110 to the external connection 2122 via the I/O module 2120 and the second plurality of data pins. In embodiments, the second serial data stream may range between 10 to 25 Gbps.

[0110] Although reference is made to separate first reference clock pin, second reference clock pin, first plurality of data pins and second plurality of data pins, in embodiments, each pin may be a fixed-function, fixed-location pin, connected internally through a wire. In embodiments, each pin may be a multiplexed fixed-function pin, connected internally through a multiplexer or crossbar. In embodiments, each pin may be a general purpose I/O pin connected through the FPGA core 2106. In embodiments, one or more pin may be fixed function, fixed location pines, while other pins may me multiplexed fixed function pins and/or a general purpose I/O pin.

[0111] In embodiments, the one or more interfaces may also include at least a second interface. The second interface of the one or more interfaces, may include a second plurality of pins of FPGA 2100. The second plurality of pins may be used to transmit and/or receive data and/or signals. In embodiments, the second plurality of pins may include a first clock output pin. The first clock output pin may be operationally connected to deserializer 2104. In embodiments, the first clock output pin may also be operationally connected to computation logic 2210 such that a receiver side clock signal is transmitted from the deserializer 2104 to computation logic 2210 via the first clock output pin. Additionally, in some embodiments, the first clock output pin may also be operationally connected to zero-delay buffer PLL 2208a such that the receiver side clock is transmitted from the deserializer 2104 to the zero-delay buffer PLL 2208a via the first clock output pin. In embodiments the receiver side clock signal may have a frequency ranging between 100-650 MHz.

[0112] In embodiments, the second plurality of pins may also include a second clock output pin. The second clock output pin may be operationally connected to serializer 2110. In embodiments, the second clock output pin may also be operationally connected to computation

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logic 2210 such that a transmitter side clock signal is transmitted from the serializer 2110 to computation logic 2210 via the second clock output pin. Additionally, in some embodiments, the second clock output pin may also be operationally connected to zero-delay buffer PLL 2208b such that the transmitter side clock is transmitted from the serializer 2110 to the zero-delay buffer PLL 2208b via the second clock output pin. In embodiments the transmitter side clock signal may have a frequency ranging between 100-650 MHz.

[0113] In embodiments, the serializer 2110 and deserializer 2104 (SERDES) circuit(s) may contain two major sections: (a) an analog side whose purpose is signal cleaning, and (2) a digital side which turns the analog signal into bits and converts between parallel and serial data streams. In embodiments, the analog side may include a few different types of amplifiers to provide signal cleaning. In embodiments, the adjustable oscillator 2200 may be implemented in a variety of ways. In embodiments, the adjustable oscillator 2200 may be implemented as a voltage controlled oscillator. A voltage controller oscillator may be implemented using a variety of architectures. In embodiments, other types of oscillators may be used including negative-resistance oscillators, Clapp oscillators, Colpitts oscillators, ring oscillators, and varactor-tuned oscillators, to name a few.

[0114] In embodiments, a voltage controller crystal oscillator may be used as the adjustable oscillator 2200, for example, the Si550 from Silicon Labs. In embodiments, a numerically/digitally-controlled oscillator may be used as the adjustable oscillator 2200, which is a digital version of an analog VCO, and may use switched circuit elements or a fixed frequency oscillator and a digital PLL to adjust the frequency.

[0115] In embodiments, the adjustable oscillator 2200 may be implemented with a digital delay line, e.g. the SY89295U from Micrel.

[0116] In embodiments, the adjustable oscillator 2200 may be implemented as a voltage-controlled delay element, e.g. the HMC910 provided by Analog devices.

[0117] As illustrated in FIG. 2, in embodiments, the receiver side clock signal RXCLOCK is based on, but has a different frequency and phase than the REFERENCE CLOCK signal provided by oscillator 2200 based on the operation of the deserializer 2104, as is discussed above with respect to the serializer 110. In embodiments, the transmitter side clock signal TXCLOCK provided from the deserializer 2104 may be provided by transceiver phase locked loop 2108, which

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is provided inside FPGA 2100, and may be controlled by frequency or phase adjustable oscillator 2200, external to FPGA 2100. In this manner, the frequency or phase of the transmitter side clock signal TXCLOCK may be adjusted.

[0118] In embodiments, an external phase controller 2202 is connected to the frequency or phase adjustable oscillator 2200 and provides control signals to allow for adjustment of the phase of at least the transmitter side clock signal TXCLOCK. The phase of the incoming data, in embodiments, may be adjusted by adjusting the data stream received by I/O module 2120. In embodiments, the external phase controller 2202 provides control signals based on the phase difference between the receiver clock signal RXCLOCK and the transmitter clock signal TXCLOCK. In embodiments, the phase difference may be determined using phase detector 2206 and zero-delay buffers, 2208a, 2208b. In embodiments, the zero-delay buffers 2208a, 2208b may be incorporated into the FPGA core 2106 of the FPGA 2100. In embodiments, FPGA core 2106 may not include the zero-delay buffers 2208a, 2208b. In embodiments, zero-delay buffer 2208a may have a reference trace T1 whose length is matched to a length of wire T3 between the I/O pin of FPGA 2100 and external phase detector 2206. Similarly, zero delay buffer 2208b may have a reference trace T2 whose length is matched to a second length of wire T4 between the I/O pin of the FPGA 2100 and the external phase detector 2206. Any length mismatch between reference traces T1 and wire T3 between the I/O pin of the FPGA 2100 and the external phase detector 2206 may introduce a deterministic phase error proportional to the mismatch of the length of the wires. Any length mismatch between reference traces T2 and wire T4 between the I/O pin of the FPGA 2100 and the external phase detector 2206 may introduce a deterministic phase error proportional to the mismatch of the length of the wires.

[0119] In embodiments, the transceiver PLL 2108 may include a second adjustable oscillator. In embodiments, the second adjustable oscillator of the transceiver PLL 2108 may provide the wire rate signal to the serializer 2110 which may be used to provide the transmitter clock signal TX CLOCK. In embodiments, the adjustable oscillator of the transceiver PLL 2108 may be provided outside of the transceiver PLL 2108 and operatively connected to the serializer 2110. In embodiments, where a second adjustable oscillator is provided in the FPGA 2100, the adjustable oscillator 2200 may not be necessary and the output of the controller 2202 may be provided to and used by the second adjustable oscillator to adjust the wire rate clock signal W.R. CLOCK provided to the serializer 2110 based on the information from the controller. In

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embodiments, where the second adjustable oscillator is provided on the FPGA 2100 and the adjustable oscillator 2200 is also provided off the FPGA, the delay of the second adjustable oscillator may be set to a constant value and the controller 2202 may provide instructions to the second adjustable oscillator based on this constant value. In embodiments, the constant value may be zero.

[0120] Using the configuration of FIG. 2, the receiver clock signal RXCLOCK and the transmitter clock signal TXCLOCK are sufficiently aligned in phase such that there is no need for the clock domain crossing circuit discussed above, eliminating a technical problem. The technical solution to a technical problem, in embodiments, is shown in the system of FIG. 2, which provides a wire or a logic path via the controller 2202 and adjustable oscillator 2200 to adjust the phase of the transmitter side clock TMCLOCK to correspond to that of the receiver side clock signal RXCLOCK. Some delays may be introduced in the path including min_delay and max_delay constraints of the wire and components, however, such delays are insignificant compared to the larger delays that are necessarily present when an asynchronous clock domain crossing circuit is used.

[0121] In embodiments, zero delay buffers 2208a, 2208b may be configured to add a phase offset such that the receiver clock signal RXCLOCK and the transmitter clock signal TXCLOCK may be provided with any desired fixed phase offset with respect to each other. In such embodiments, any phase difference may be used, depending on the length of the logic path between the clocks and the corresponding delay constraints. In embodiments, with a phase difference between about 45° and 360°, the min_delay should be set at 0 and the max_delay should be set equal to the time between rising edges on the receive clock signal and transmit clock signal (as shown in FIGs. 6A and 6B). The difference between 45 ° and 360 ° approximates the minimum amount of time required to safely capture data. In embodiments, the formula for the time is as follows:

Equation 1: $t_{min} = t_{setup} + t_{wire} + t_{clock\text{-}out} + \Delta t_{jitter} + t_{skew}$

[0122] Referencing the above equation, t_{setup} is the setup time of a flip-flop (i.e. a latch) on FPGA 2100. The t_{wire} is the delay of the, for example, shortest wire (as compared to other wires on the FPGA) on FPGA 2100. In embodiments, the shortest wire is the shortest possible wire. In embodiments, $t_{clock\text{-}out}$ is the clock-to-output time of a flip-flop on the FPGA 2100. In

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embodiments, Δt_{jitter} is a safety factor for jitter on both clocks. Jitter, for example, is the deviation from true periodicity of a periodic signal from a reference clock. In embodiments, t_{skew} is the skew between clock paths to the two flip-flops on FPGA 2100.

[0123] In embodiments where there is a phase difference with the transmitter clock running less than 45° ahead of the receiver clock, metastability may occur unless the clocks are treated as being greater than 360 degrees apart (as seen in FIG. 6C). In such embodiments, the min and max delay are set with the min delay greater than the time difference between rising edges and the max delay less than one full clock cycle plus the min delay. In embodiments, the transmit clock signal may also sample on the opposite edge as the receiving clock signal launch edge, but cases are symmetric. In embodiments, a change from positive to negative edge sampling adds an approximate 180 degrees offset. In embodiments, manufacturer analysis tools both may add a reasonable jitter margin to account for times when jitter causes temporary misalignment.

[0124] In embodiments, to avoid instability, both the transceiver PLL 2108 and the zero-delay buffer PLL 2208b preferably run at the highest bandwidth available, while the overall phase locking system including the phase detectors 2206, controller 2202 and oscillator 2200 runs at a low bandwidth. In such embodiments, the poles in the on-chip PLLs on the FPGA 2100 are prevented from affecting the gain or phase margin of the off-chip PLL which may be included in the controller 2202. In embodiments, any loop filter order may be used in the controller 2202 as long as the bandwidth is low enough to avoid interaction of poles in the control system. In embodiments, a low bandwidth may be, for example, 100Hz- 40kHz, 400Hz and 4khz, 4kHz and 10kHz, 100hz to 40kHz, 0Hz and 100Hz, to name a few. In embodiments, a second-order loop filter may be used in an effort to improve lock time and phase locking error. In embodiments a third-order filter may be used if the second-order filter is stable. In embodiments, a first-order filter is also an option when the second-order filter has stability problems. In embodiments, other order filters may be used, depending on the internal bandwidth of the FPGA 2100.

[0125] In embodiments, where the bandwidth of the controller 2202 is too low, the receiving clock and the transmitter clock may not track each other closely enough to consider them locked. In embodiment, such tracking issues may be solved by adjusting the min and max delay constraints appropriately to provide a cushion for the clocks being away from the expected phase. In embodiments, a PD control system may be provided after the loop filter to aid in resolving

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tracking issues. In embodiments, tracking issues may be addressed by adding some nonlinearity in the transfer function of the filter. Other solutions may also be possible.

[0126] In the embodiment of FIG. 2, the controller 2202 utilizes a phase-locked loop. In embodiments, a derivative component may be provided in the loop filter to slow down the control loop when the output value has changed recently and reduces the chance that the PLLs on the FPGA will lose lock. In embodiments, the derivative component's coefficient will be negative (i.e. the derivative component will act against the loop filter, however, some references refer to this as being a positive direction) and less than 1 (so the path straight from the filter dominates). The loop filter consists of a standard PLL loop filter with bandwidth between 400 Hz and 40 kHz of up to 4th order plus a derivative component that slows down the loop based on recent changes in the filter value. The bandwidth of the standard PLL loop filter, in some embodiments, may range between 400Hz and 4khz, 4kHz and 10kHz, 100hz to 40kHz, 0Hz and 100Hz, to name a few. The extra derivative component helps to keep the other components in the control system in their linear operating regions. The loop filter is represented by DigitalFilter() in the pseudocode provided.

[0127] FIG. 3A is an exemplary block diagram of a deserializer suitable for use in the field programmable gate array system of FIG. 2 in accordance with an embodiment of the present invention. Deserializer 2104', in embodiments, may include an input buffer 3104, a continuous time linear equalizer (CTLE) 3106, a variable gain amplifier (VGA) 3108; voltage adder 3110; decision feedback equalizer (DFE) 3110, clock and data recovery (CDR) 3116, Serial to parallel box 3118, decision circuit 3112, and clock divider 3120. In embodiments, deserializer 2104' may not include one or more of the following components: CTLE 3106, DFE 3114, and/or VGA 3108, to name a few.

[0128] A deserializer circuit accepts a data stream from an input buffer and converts it into a parallel format at a lower bit rate. First, data comes into the chip from the input pins 3102 into an input buffer 3104. In embodiments, the input buffer receives a transmission from an I/O module, such as I/O module 2120. A continuous time linear equalizer (CTLE) 3106 may be used after the input buffer 3104 to improve signal quality by placing a zero near the dominant pole of the transmission medium to cancel the first pole of the system. A variable-gain amplifier (VGA) 3108 may then be used to scale the signal up for further processing. This output is then turned into a binary 0-1 decision by the decision circuit 3112. In embodiments, the decision

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circuit 3112 includes adder 3110. A decision feedback amplifier may be included to further improve signal integrity by taking the results of the decision circuit, applying a weighting filter, and adding the result to the output from the VGA 3108. When the signal is in the digital domain, a clock and data recovery circuit (CDR) 3116 recovers the phase of the data and create a wire-rate clock that is phase-aligned to the received data. The CDR 3116 may use a reference clock and *a priori* knowledge of the nominal frequency of the data stream to set the frequency of the recovered clock. With a clock aligned to the data stream, which in some embodiments may be a high speed data stream (e.g. 10 Gbps, 25 Gbps, a range from 9-25 Gbps, 10-25 Gbps, 22-33 Gbps, 33-45 Gbps, 45-60 Gbps, 60-80Gbps, 80-120 Gbps, or 1 Gbps-100 Gbps, to name a few) the receiver can use a clock divider 3120 and a serial-to-parallel circuit 3118 to convert the serial data stream into a lower-frequency than the data stream (e.g. $1/4^{th}$ of the data rate of the high speed data stream or $1/256^{th}$ of the data rate of the high speed data stream, to name a few) parallel data stream.

[0129] In embodiments, a decision feedback equalizer 3114 (DFE) may be provided. In embodiments, the decision feedback equalizer may be a filter that subtracts or adds at least *n* decided bits to cancel inter-symbol interference on the wire. In embodiments, a clock and data recovery circuit may be provided and includes a data phase detector, which may be any of the circuits discussed above, as well as a phase-locked loop circuit.

[0130] FIG. 3B is an exemplary circuit diagram of a continuous-time linear equalizer (CTLE) suitable for use in the deserializer of FIG. 3A in accordance with an embodiment of the present invention. CTLE 3104', in some embodiments, places a zero to cancel out the dominant pole of the trans mission line for an incoming signal. In embodiments, CTLE 3104' is a linear filter applied at a receiver, in the case of FIG. 3B, input buffer 3104, that attenuates low-frequency signal components and filters off higher frequencies. The CTLE 3104' may be adjusted to optimize the ratio of low frequency attenuation to high frequency amplification. In embodiments, a variable gain amplifier may be provided and used to scale the output of the CTLE to as large of a signal as possible. In embodiments, a decision circuit may also be provided.

[0131] FIG. 3C is an exemplary block diagram of a clock and data recovery (CDR) circuit suitable for use in the deserializer of FIG. 3A in accordance with an embodiment of the present invention. In embodiments, CDR 3118' circuit recovers phase information from an incoming data stream. The data stream, in embodiments, may be received by an alexander phase detector 3302.

The CDR 3118 may also obtain frequency information from a reference clock, output. The output, may determine, in embodiments, whether the recovered clock have the same phase as the recovered data.

[0132] FIG. 3D is an exemplary circuit diagram of a decision circuit suitable 3110' for use in the deserializer of FIG. 3A in accordance with an embodiment of the present invention. FIG. 3D illustrates an exemplary embodiment of such a decision circuit 3110' utilizing a StrongARM sense amplifier. In embodiments, any comparator circuit may be used as a decision circuit.

[0133] FIG. 3E illustrates an exemplary embodiment of deserializer 2104''. In embodiments, the deserializer 2104'' may include a receiver PMA 3512 and receiver PCS 3508. The receiver PMA 3512 may include receiver buffer 3504, CDR 3516, and serial to parallel box 3118'. In embodiments, the receiver buffer 3504 receives serial differential input data 3502. In embodiments, this data is received by an I/O module, such as the I/O module 2120 of FIG. 2. In embodiments, the data is then received by the CDR 3516, from the receiver buffer 3504. The CDR, in embodiments, transmits the inputted serial data, a serial clock signal, and a parallel clock signal to the serial to parallel box 3506. The CDR may also transmits the parallel clock data to the receiver PCS 3508. The serial to parallel box 3118', in embodiments, then converts the serial data into parallel data, transmitting the parallel data to the receiver PCS 3508. The receiver PCS 3508 transmits parallel data to the FPGA Core 2106.

[0134] In addition to the components illustrated in FIG. 3E, deserializer 2104'' may also include or be electrically coupled to a continuous-time linear equalizer (CTLE) (*see* FIG. 3B) which is a pure analog circuit that may be used to correct channel issues. In embodiments, the deserializer 2104'' may include a shift register or demultiplexer with a counter.

[0135] FIG. 4A is an exemplary block diagram of a serializer suitable for use in the field programmable gate array system of FIG. 2 in accordance with an embodiment of the present invention. The serializer circuit accepts a clock running at wire rate 4112 (from transceiver PLL 2108) and accepts parallel data (e.g. TX data 4102) to serialize the data. Data is converted from a parallel format to a serial data stream in the parallel to serial box 4104. A feed-forward equalizer (FFE) 4106, which uses the history of bits serialized on the wire to filter out inter-symbol interference, may be included to improve signal integrity. Finally, the serializer outputs the serial data stream to a transmission medium using an output buffer 4114. The serializer also generates

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a parallel clock (TX Clk 4110), that operates at a lower speed than the data stream (e.g. 100-400 MHz, 100-600 MHz, to name a few), for use by other components using either a simple clock divider 4108 or a more complex clock generation block which can contain dividers and phase shifting elements for aligning multiple transmitters.

[0136] FIG. 4B illustrates an exemplary embodiment of serializer 2110''. As discussed above with respect to FIGS. 2 and 4A, serializer 2110'' receives parallel data streams from the FPGA core 2106 and serializes them for transmission out of the FPGA 2100. In embodiments, serializer 2110'' may include transmitter PCS 4206, clock generation block 4210, and transmitter PMA 4216. In embodiments, transmitter PMA 4216 may include parallel to serial box 4104' and transmitter buffer 4214. The transmitter PCS 4206 may receive parallel data from FPGA core 2106. In embodiments, the parallel data is then transmitted to the parallel to serial box 4104'. The clock generation block 4210 may receive a wire-rate clock signal 4112. The clock generation block 4210, in embodiments, may split the signal in to a parallel clock signal and serial clock signal, both the parallel and serial signals being transmitted to the parallel to serial box 4104'. The parallel to serial box 4104 may covert the data from parallel to serial, transmitting the serial differential output data 4218 to the transmitter buffer 4214. Then, in embodiments, the transmitter buffer 4214 outputs the serial differential output data 4218.

[0137] In embodiments the serializer 2110'' may be a shift register or a multiplexer with a counter. In embodiments, the serializer 2110'' may include additional components, such as a feed forward equalizer (FFE) which uses the last n bits to cancel inter symbol interference on the wire. In embodiments, a buffer amplifier may be included which provides variable gain to allow adjustable voltage swing on the output of the transmitter. In embodiments, a clock divider may be provided. In embodiments, the clock divider may generate a low-speed clock (e.g. 100-400 MHz, 100-600 MHz, to name a few) for the serializer and the PMA/PCS. In embodiments, the clock divider is typically provided using a counter. In embodiments, the clock generation block 4210 might also include a clock phase adjustment circuit to allow multiple transmitter lanes to be phase-aligned.

[0138] Referring to FIGS. 5A-5D, in embodiments, the phase detector 2206 may be an analog, single bit phase detector which may be implemented using a variety of circuit components including (1) an XOR gate; (2) S-R flip-flop; (3) D flip-flop; (4) Edge-triggered JK flip-flop; (5)

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Gilbert cell multiplier and/or (6) Diode ring mixer, to name a few. FIG. 5A illustrates an exemplary embodiment of a phase detector 2206 that utilizes D flip-flops. FIG. 5B illustrates another exemplary embodiment of a phase detector 2206 that utilizes S-R flip-flops. FIG. 5C is another exemplary block diagram of a phase detector suitable for use in the field programmable gate array system of FIG. 2 in accordance with an embodiment of the present invention. FIG. 5D is another exemplary block diagram of a phase detector suitable for use in the field programmable gate array system of FIG. 2 in accordance with an embodiment of the present invention. Other than a basic phase detector, a time-to-digital converter (TDC) can be used to detect the phase offset of the clocks. Fig. 5C shows a Vernier TDC and Fig. 5D shows a parallel delay line TDC as examples. The Vernier TDC uses a pair of unequal delay lines to delay the two signals by varying amounts and uses D-type flip-flops to quantify the phase difference between the two signals at multiple points along the delay line. The parallel delay line TDC uses a set of simple phase detectors with the two input signals delayed by varying amounts to quantify the phase difference between the two signals. In both cases, a decoding circuit is used to translate the results of the individual phase detection elements into a phase offset.

[0139] In embodiments, the phase detector 2206 may be a multi-bit phase detector, sometimes referred to as a time-to digital converter (TDC). In embodiments, such a phase detector may be a counter-based TDC that counts up the time between START and STOP. In embodiments, such a phase detector may be an interpolator TDC in which time measurement may be performed by measuring a voltage difference (e.g. by using a ramp wave and sampling at two points or by charging a capacitor). In embodiments, a phase detector may be a vernier TDC. FIG. 5C

[0140] In embodiments the phase detector 2206 may be implemented using a tapped delay line TDC. In embodiments, the phase detector 2206 may be implemented using a metastability-based phase detector. In embodiments, the metastability-based phase detector is similar to a D flip-flop phase detector but includes an averaging filter. In embodiments, a parallel-delay-line TDC may be used to implement the phase detector 2206. FIG. 5D illustrates an example of a parallel-delay-line TDC. In embodiments, the phase detector may be implemented as a pulse-shrinking TDC. Such a pulse-shrinking TDC may generate a pulse and then send it circularly through an engineered delay line to shrink it until it is gone, count the number of times it goes through the pulse-shrinking circuit.

[0141] In embodiments, the phase detector may be implemented as a scrambling TDC. Scrambling TDCs may be implemented with added digital noise shaping to suppress errors. In embodiments, the phase detector 2206 may be implemented as a PLL/DLL-based TDC. In such an embodiment, the phase detector may lock a digital PLL to the incoming feedback signal and record the internal control code.

[0142] In embodiments, all of the phase detector embodiments discussed above may be combined with or connected to a low-pass filter and an analog to digital converter (ADC). In embodiments, other examples of phase detectors may be used consistent with the teachings of this disclosure.

[0143] FIGS. 6A-6D illustrate example phase differences between the receiver side clock and the transmitter side clock. It will be understood that other examples of phase differences may be present consistent with the teachings of this disclosure. Generally, when the clocks are aligned, the minimum and maximum delays may be used to determine the time available for the computation of data.

[0144] FIG. 6A illustrates an example of a phase difference between the receiver side clock and the transmitter side clock of an FPGA in accordance with an embodiment. FIG. 6A depicts a phase difference when the clocks are under 360 degrees apart. This embodiment results in minimum delay 6106A and maximum delay 6108A, for which data may be computed. The minimum delay 6106A is from the driving clock edge back to itself, as shown in FIG. 6A.

[0145] FIG. 6B illustrates an example of a phase difference between receiver clock and a transmitter clock of an FPGA in accordance with an embodiment. The phase difference depicted in FIG. 6B shows a phase difference with minimum delay 6106B and maximum delay 6108B. The example shown in FIG. 6B shows a minimum delay 6106B of 0. However, in practice, while designers may design for the phase difference in FIG. 6B, the phase difference may end up more similar to the phase differences of FIGS. 6A and/or 6C.

[0146] FIG. 6C illustrates an example of a phase difference between receiver clock and a transmitter clock of an FPGA in accordance with an embodiment. FIG. 6C depicts a phase difference with the clocks are over 360 degrees apart. The time between minimum delay 6106C and maximum delay 6108C may allow for more data computations within the phase difference.

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[0147] FIG. 6D illustrates an example of an inverted phase difference between receiver clock and a transmitter clock of an FPGA in accordance with an embodiment. This example of an inverted phase difference between minimum delay 6106D and maximum delay 6108D shows that, even inverted, the phase difference would work similarly to the phase detectors of FIGS. 6A-6C.

[0148] FIG. 7A is a block diagram of another field programmable gate array system in accordance with an embodiment of the present invention. The system of FIG. 7A is similar to that of FIG. 2, and common components are referred to using the same reference numbers (with a differing first digit to indicate the Figure - e.g. if the first digit of a reference numeral is "7," the reference numeral is located on FIG. 7) as in FIG. 2. One difference between FIG. 2 and FIG. 7A is FIG. 7A shows multiple deserializers 7104a, 7104b, and multiple serializers 7110a, 7110b. Multiple deserializers and serializers, as opposed to one of each, allows FPGA 7100 to receive more input data and transmit more output data.

[0149] The system, in accordance with FIG. 7, may include FPGA 7100. FPGA 7100 may include FPGA transceiver banks 7102 and FPGA core 7106. The FPGA transceiver banks 7102 may include multiple serializers and deserializers, such as deserializers 7104a,7104b, and serializers 7110a, and 7110b. FPGA core 7106 may include zero-delay buffers 7208a, 7208b, and 7208c and computation logic 7210. The system may further include a fixed-frequency oscillator 7000, an I/O module 7120 connected to an external connection 7122, an adjustable delay line 7200a, a frequency or phase-adjustable oscillator 7200b, a DLL controller 7202a, a PLL/DLL controller 7202b, and phase detectors 7206a, 7206b.

[0150] In a multi-channel system, phase alignment can be achieved by using multiple serializers in a channel bonded mode, which keeps their parallel and serial clocks running at the same phase, and by using an adjustable delay line 7200a (along with an additional controller 7202a) on the data streams going to all but one of the deserializers. The adjustable delay line 7200a may have adjustment range at least as wide as one period of the parallel RX clock. This can be accomplished by using a long delay line or by using a pair of smaller delay lines with a glitch-free switchover circuit to hide the boundary conditions of the delay lines.

[0151] Similar to the system described in connection with FIG. 2, the system of FIG. 7A may or may not include zero delay buffers 7208a, 7208b, and 7208c. In embodiments, zero-delay buffer 2208a may have a reference trace T1 whose length is matched to a length of wire T4 between

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the I/O pin of FPGA 2100 and external phase detectors 7206a, 7206b. Similarly, zero delay buffer 2208b may have a reference trace T2 whose length is matched to a second length of wire T5 between the I/O pin of the FPGA 7100 and the external phase detector 7206a. Also, similarly, zero delay buffer 2208c may have a reference trace T3 whose length is matched to a second length of wire T6 between the I/O pin of the FPGA 7100 and the external phase detector 7206b. Any length mismatch between reference traces T1 and wire T4 between the I/O pin of the FPGA 7100 and the external phase detectors 7206a, 7206b may introduce a deterministic phase error proportional to the mismatch of the length of the wires. Any length mismatch between reference traces T2 and wire T5 between the I/O pin of the FPGA 7100 and the external phase detector 7206a may introduce a deterministic phase error proportional to the mismatch of the length of the wires. Any length mismatch between reference traces T3 and wire T6 between the I/O pin of the FPGA 7100 and the external phase detector 7206b may introduce a deterministic phase error proportional to the mismatch of the length of the wires.

[0152] The FPGA 7100, and all the components within the system shown in FIG. 7A, may be similar to FPGA 2100 and all of the components within the system of FIG. 2, the descriptions of which applying herein.

[0153] FIG. 7B is a block diagram of another field programmable gate array system in accordance with an embodiment of the present invention. The system of FIG. 7B is similar to that of FIGs. 2 and 7A, and common components are referred to using the same reference numbers (with a differing first digit to indicate the Figure - e.g. if the first digit of a reference numeral is "7," the reference numeral is located on FIG. 7) as in FIG. 2. XCVR PLL 7108 stands for Transceiver PLL 7108. Similar to the system shown in FIG. 7A, the system of FIG. 7B has multiple deserializers 7104a-d and multiple serializers 7110a-d. As noted above, multiple deserializers and serializers, as opposed to one of each, allows FPGA 7100' to receive more input data and transmit more output data.

[0154] The FPGA 7100', and all the components within the system shown in FIG. 7B, may be similar to FPGA 2100 and all of the components within the system of FIG. 2, the descriptions of which applying herein. The FPGA 7100', and all the components within the system shown in FIG. 7B, may be similar to FPGA 7100 and all of the components within the system of FIG. 7A, the descriptions of which applying herein.

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[0155] FIG. 7C is a block diagram of another field programmable gate array system in accordance with an embodiment of the present invention. The system of FIG. 7C is similar to that of FIGs. 2 and 7A, and common components are referred to using the same reference numbers (with a differing first digit to indicate the Figure - e.g. if the first digit of a reference numeral is "7," the reference numeral is located on FIG. 7) as in FIG. 2. XCVR PLL 7108 stands for Transceiver PLL 7108. Similar to the system shown in FIGS. 7A and 7B, the system of FIG. 7C has multiple deserializers 7104a-f and multiple serializers 7110a-f. As noted above, multiple deserializers and serializers, as opposed to one of each, allows FPGA 7100'' to receive more input data and transmit more output data.

[0156] The FPGA 7100'', and all the components within the system shown in FIG. 7C, may be similar to FPGA 2100 and all of the components within the system of FIG. 2, the descriptions of which applying herein. The FPGA 7100'', and all the components within the system shown in FIG. 7C, may be similar to FPGA 7100 and all of the components within the system of FIG. 7A, the descriptions of which applying herein.

[0157] An exemplary prototype for this system is shown in FIGs. 8A and 8B. In this embodiment, the prototype is a VITA 57.1 FMC expansion card 8410 with an SFP+ connector for 10 gigabit Ethernet 8120 and the required hardware for a PLL approach to the phase locking problem. In this embodiment, the VITA 57.1 FMC connector 8300 attaches the expansion card to a host FPGA card 8400, for example. In this embodiment, adjustments to the transmitter side clock signal may be based on frequency or phase adjustment provided via the SI571 VXCO 8200. Control of these elements may be provided via the ATSAML21 Microcontroller 8202b. Phase detection may be provided by the phase detector 8206 which may provide phase difference information to the microcontroller via the filter 8202a. A receiving side reference clock may be provided by the SI570 crystal oscillator 8000. In this embodiment, control loop filtering is done in software using the microcontroller, except for an anti-aliasing filter at half the sample rate of the microcontroller ADC. In embodiments, the high-speed transceiver channels may have a data stream of 8-12 Gbps.

[0158] In the embodiment of FIGS. 8A and 8B, the following pseudocode may be used to implement an exemplary embodiment of the system discussed above in connection with FIG. 2.

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[0159] The pseudo code shown below implements the control loop and communicates with the host. In embodiments, the pseudocode shown is run by the microcontroller (8202b) and uses an interrupt-based system to run the control algorithm for either the PLL or DLL paths on the device. The pseudocode also includes a lock indicator and a memory-mapped I^2C interface for communication with the host system. The main control loop is triggered on every sample of the internal ADC.

```
Begin:

    Set up peripherals
    Program Si5340 with configuration
    Enable Analog Comparator to measure lock indicator from the phase detector
    Set ADC in free-running mode and enable interrupts on every sample
    Enable I2C interrupt
    Wait

On ADC Interrupt:
    Read ADC value into Window[0]
    ControlCode = DigitalFilter(Window)
    Read MODE pin to Mode

    If Mode = PLL_MODE then:
        Output ControlCode on DAC channel 0
    Else:
        Coarse = 9 MSBs of ControlCode
        Fine = NonlinearCorrection(ControlCode – Coarse)
        Output Coarse to DELAY_CONTROL pins
        Output Fine to DAC channel 1

    Shift Window array by 1

On I2C Packet Received:
    Address = I2C_packet[0]
    Length = I2C_packet.length
    If I2C_READ then:
        I2C_write(I2C_regs[Address])
    Else:
        for i < Length:
            I2C_regs[Address + i] = I2C_packet[1 + i]

On Analog Comparator Interrupt:
    Read comparator value to Ind
    Output Ind to LOCK pin
```

[0160] FIGs 9A-C are exemplary flow charts of a process implementing the field programmable gate array system in accordance with an embodiment of the present invention. The field programmable gate array system, including the field programmable gate array and the components thereof, may be similar to the field programmable gate array system of FIGs. 2, 7A-7C and 8A-8C, the descriptions of which applying herein.

[0161] The process of FIGs. 9A-9C may begin at step S902. Referring to FIG. 9A, at step S902, a first serial data stream is received by a first plurality of data pins in a first interface of a field programmable gate array in the field programmable gate array system. In embodiments, the first serial data stream may include market data. In embodiments, market data may be price and trade-related data for a financial instrument reported by a trading venue (i.e. a stock exchange).

[0162] At a step S904, a first clock signal having a first frequency and a first phase is received by a first reference clock in in the first interface. In embodiments, step S904 may be performed before step S902. In embodiments step S904 may be performed contemporaneously with step S902.

[0163] The process of FIGs. 9A-9C may continue with a step S906. At step S906, the first plurality of data pins in the first interface may transmit the first serial data stream to a deserializer in the field programmable gate array.

[0164] At a step S908, the first reference clock pin in the first interface may transmit the first clock signal to the deserializer. In embodiments, step S908 may be performed before step S906. In embodiments step S908 may be performed contemporaneously with step S906.

[0165] At a step S910, a first receiver side clock signal may be generated by the deserializer. In embodiments, the first receiver side clock signal may have a second frequency and a second phase. In embodiments, the second frequency is different from the first frequency. In embodiments, the second frequency corresponds to the first frequency. In embodiments, corresponding may refer to the frequencies being the same frequency. In embodiments corresponding may also refer to frequencies being close (e.g. within an acceptable range in the art) to the same frequencies. In embodiments, the first phase and the second phase may not be aligned. In embodiments the first phase and the second phase are aligned. In embodiments, a difference between the first phase and the second phase is below a threshold level. In embodiments, the deserializer generates the first receiver clock signal based at least in part on the first clock signal.

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[0166] At a step S912, the first serial data stream received by the deserializer may be converted, by the deserializer, into a first plurality of data streams. In embodiments, the first plurality of data streams may include a first amount of data streams. In embodiments, the first amount of data streams is equal to eight (8) data streams. In embodiments, the first amount of data streams is equal to ten (10) data streams. In embodiments, the first amount of data streams is equal to sixteen (16) data streams. In embodiments, the first amount of data streams is equal to twenty (20) data streams. In embodiments, the first amount of data streams is equal to thirty-two (32) data streams. In embodiments, the first amount of data streams is equal to forty (40) data streams. In embodiments, the first amount of data streams is equal to sixty-four (64) data streams. In embodiments, the first amount of data streams is equal to eighty (80) data streams. In embodiments, the first amount of data streams is equal to one hundred twenty-eight (128) data streams. In embodiments, the first amount of data streams is equal to one hundred sixty (160) data streams. In embodiments, the first amount of data streams is equal to two (2) to the power of N, where N is an integer. In embodiments, the first amount of data streams is equal to ten (10) times two (2) to the power of N, where N is an integer. In embodiments the first amount of data streams is equal to thirty-three (33) times two (2) to the power of N, where N is an integer.

[0167] At a step S914, the first receiver side clock signal is transmitted from the deserializer to computational circuitry in the field programmable gate array.

[0168] At a step S916, the first plurality of data streams is transmitted form the deserializer to the computational circuitry. In embodiments, the first plurality of data streams includes a first plurality of data items. In embodiments, step S916 may be performed before step S914. In embodiments step S916 may be performed contemporaneously with step S914.

[0169] At a step S918, the first receiver side clock signal is transmitted from the deserializer via a first clock output pin on a second interface of the field programmable gate array to a phase detector of the field programmable gate array system which is not on the field programmable gate array. In embodiments, the transmission of the first receiver side clock signal is also via a first zero delay buffer phase lock loop of the field programmable gate array before being transmitted via the first clock output pin of the second interface.

[0170] At a step S920, a first transmitter side clock is generated by the field programmable gate array system. In embodiments, the first transmitter side clock has a third frequency and a

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third phase. In embodiments, the third frequency corresponds to the second frequency. In embodiments the third phase may be aligned with the second phase. In embodiments, the third phase and the second phase may not be aligned. In embodiments, the third phase and the second phase may have a difference in phases that is less than a second threshold level. In embodiments, the first transmitter side clock signal is generated by performing the following steps until a first output of the phase detector is below a first threshold.

[0171] Referring to FIG. 10A, generating the first transmitter side clock signal may begin at step S1002. At step S1002, a second clock signal is generated by an adjustable oscillator in the field programmable gate array system. In embodiments, the second clock signal may have a fourth frequency and a fourth phase.

[0172] The process of FIGs. 10A-B may continue at a step S1004. At step S1004, a first wire rate clock signal having a fifth phase and a fifth frequency is generated. In embodiments, the generation of the wire rate clock signal may be based in part on the second clock signal. In embodiments the fifth frequency is a rational multiple of the fourth frequency. In embodiments the fifth frequency is equal to x times the fifth frequency where x is the second amount of data streams. In embodiments the fifth frequency is equal to x times the frequency of the of the transmitter side clock signal where x is half of the second amount of data streams.

[0173] In embodiments, the generation of the wire rate clock signal may be performed with the following steps. Referring to FIG. 11, at a step S1102, the second clock signal is received from the adjustable oscillator at a transceiver phase lock loop via a second reference clock pin in the first interface. At a step S1104, the second clock signal is processed by the transceiver phase lock loop. As a step S1106, the wire rate clock signal is provided by the transceiver phase lock look. The providing of the wire rate clock signal, in embodiments, may be based at least in part on the processing of the received clock signal. Once the wire rate clock signal is provided, at a step S1108. the wire rate clock signal is transmitted by the transceiver phase lock loop to a serializer on the field programmable gate array. In embodiments, the first wire rate clock is generated by a phase lock loop. In embodiments, the phase lock loop that generates the wire clock is on field programmable gate array. In embodiments, the phase lock loop that generates the wire clock is part of the field programmable gate array system and not part of the field programmable gate array.

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[0174] In embodiments, the generation of the wire rate clock may include processing the second clock signal. Once the second clock signal is processed, the wire rate clock may be provided. The providing of the wire rate clock, in embodiments, is based at least in part on the processing of the second clock signal. After providing the wire rate clock, in embodiments, the wire rate clock may be transmitted to the serializer.

[0175] Referring back to FIG. 10A, at a step 1006, an interim transmitter side clock signal having a sixth frequency and a sixth phase is generated by the serializer in the field programmable gate array. In embodiments, the sixth frequency corresponds to the third frequency. In embodiments the sixth phase may be aligned with the third phase. In embodiments, the sixth frequency may correspond to the third frequency and the sixth phase may not be aligned with the third phase. In embodiments, the sixth phase and the third phase may not be aligned. In embodiments, the third phase and the sixth phase may have a difference in phases that is less than a second threshold level.

[0176] At a step S1008, the interim transmitter side clock signal is transmitted from the serializer via a second clock output pin in the second interface to the phase detector. In embodiments, the transmission of the interim transmitter side clock is also via a second zero delay buffer phase lock loop of the field programmable gate array before being transmitted via the second clock output in of the second interface.

[0177] The process of FIGs. 10A-10B may continue with at a step S1010. Referring to FIG. 10B, at a step S1010, a first output is generated by the phase detector. The first output, in embodiments, is based at least on a comparison of the first receiver side clock signal and the interim side clock signal. The first output, in embodiments, may include information indicating the phase differences (if there is any) between the first receiver side clock and the interim side clock signal. Additionally, in embodiments, the first output may include information indicating a difference (if there is any) of frequencies between the first receiver side clock signal and the interim side clock signal.

[0178] At a step S1012, the first output may be transmitted from the phase detector to a phase controller of the field programmable gate array system which is not in the field programmable gate array.

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[0179] At a step S1014, interim adjustment information is determined by the phase controller. In embodiments, the interim adjustment information may be based at least in part on the first output. For example, the interim adjustment information may indicate necessary adjustments to align the phases of the first receiver side clock signal and the interim side clock signal. As another example, the interim adjustment information may indicate necessary adjustments to align the frequencies of the first receiver side clock signal and the interim side clock signal.

[0180] At a step S1016, the interim adjustment information is transmitted from the phase controller to the adjustable oscillator. In embodiments, once the interim adjustment information is received, the adjustable oscillator adjusts the second clock signal based on the interim adjustment information. The adjustment of the second clock signal, in embodiments, may change the phase of the second clock signal. In embodiments, the interim adjustment information indicates a desired phase. In embodiments, the interim adjustment information indicates a desired frequency. In embodiments, the interim adjustment information indicates a change in phase. In embodiments, the interim adjustment information indicates a change in frequency. In embodiments, the adjustment information includes a voltage. In embodiments, the adjustment information includes a digital transmission. For example, the adjustment information may be a command over a serial bus (e.g. I^2C or SPI) that adjusts a clock divider or phase rotator. As another example, the adjustment information may trigger a set of parallel digital wires for "frequency/phase up," "frequency/phase down," and/or "frequency/phase step." In embodiments, the adjustment of the second clock signal may change the frequency of the second clock signal.

[0181] In embodiments, steps S1002 through steps S 1016 are repeated until the first output of the phase detector is below the first threshold level. This threshold level may indicate that the first receiver side clock signal and the interim transmitter side clock signal have phases that are aligned. This threshold level may indicate that the first receiver side clock signal and the interim transmitter side clock signal have frequencies that correspond to one another.

[0182] Referring back to FIG. 9B, once the first output of the phase detector is below a first threshold level, at a step S922, the serializer may transmit the first transmitter side clock signal to the computational circuitry. At a step S924, a first set of operations ins performed by the computational circuitry on at least a portion of the first plurality of data items to generate a second

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plurality of data streams. In embodiments, the first operation includes a trading algorithm. In embodiments the trading algorithm may include the parsing the market data. Once the market data is parsed, mathematical operations are performed at a portion of the market data. After the mathematical operations are performed, order packets are generated using at least an output of the mathematical operations. In embodiments, the first set of operations includes at least one of the following: (i) an arithmetic operation; (ii) a logical operation; (iii) a pipeline operation; and (iv) a memory access operation.

[0183] In embodiments, at least a portion of the first set of operations is performed prior to step S922. In embodiments, at least a portion of the first set of operations is performed after step S922. In embodiments all of the first set of operations is performed after step S922.

[0184] In embodiments, the second plurality of data streams may include a second amount of data streams. In embodiments, the second amount of data streams may be the same as the first amount of data streams. In embodiments, the second amount of data streams is equal to eight (8) data streams. In embodiments, the second amount of data streams is equal to ten (10) data streams. In embodiments, the second amount of data streams is equal to sixteen (16) data streams. In embodiments, the second amount of data streams is equal to twenty (20) data streams. In embodiments, the second amount of data streams is equal to thirty-two (32) data streams. In embodiments, the second amount of data streams is equal to forty (40) data streams. In embodiments, the second amount of data streams is equal to sixty-four (64) data streams. In embodiments, the second amount of data streams is equal to eighty (80) data streams. In embodiments, the second amount of data streams is equal to one hundred twenty-eight (128) data streams. In embodiments, the second amount of data streams is equal to one hundred sixty (160) data streams. In embodiments, the second amount of data streams is equal to two (2) to the power of N, where N is an integer. In embodiments, the second amount of data streams is equal to ten (10) times two (2) to the power of N, where N is an integer. In embodiments the second amount of data streams is equal to thirty-three (33) times two (2) to the power of N, where N is an integer.

[0185] At a step S926, the second plurality of data streams is transmitted from the computational circuitry to the serializer. Once received by the serializer, at a step S928, the serializer converts the second plurality of parallel data streams into the second serial data stream.

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The second serial data stream, in embodiments, includes trading data. Trading data, for example, may be any data related to purchasing or selling of stocks, commodities, goods, and/or services.

[0186] At a step S930, the second serial data stream may be transmitted from the serializer off the field gate programmable array system via a second plurality of data pins in the first interface. In embodiments, the second serial data stream is transmitted from the serializer on the field programmable gate array to an input/output module of the field gate array system but not on the field gate array. The second serial data stream may then be transmitted from the input/output module off the field gate array system.

EXAMPLES

[0187] The following examples may be used to illustrate embodiments of the present invention. They are meant solely for illustration and not intended to be limiting.

EXAMPLE 1

[0188] In embodiments a trading algorithm may be applied in a crossing auction on an option exchange. In embodiments, a third serial data stream including target price information on a set of options contracts is provided as in input to the FPGA. In embodiments, the first serial stream includes market data includes bid, asks, trades and auction notifications. When an auction is announced, as indicated in the market data, the FPGA compares the announced auction price to its target price. In embodiments, the target price is stored in the FPGA and is provided via the third serial data stream. In embodiments, the target price may be generated using a suitable pricing model, e.g. Black Sholes. When there is some overlap, the field programmable gate array generates and sends an order at its target price which is transmitted out of the FPGA in the second serial data stream. In embodiments, the target price information on a set of options contracts is streamed into the field programmable gate array as a simple set of triggers in the third serial data stream. The target price information, may include a linearization of the result of the Black Scholes computation or some other model. The field programmable gate array may implement Black-Scholes, and instead receive market data on the underlying asset as a secondary data stream.

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EXAMPLE 2

[0189] Another example of a trading algorithm is "signal based". In embodiments, signals refer to a trigger that is activated when certain events happen. In embodiments, a signal may simply track a sale price which changes every time the market information indicates a sale has taken place. In embodiments, a signal may be used as a measure of book pressure to determine whether prices are likely to rise or fall. Some signals may be calculated quickly while others are calculated more slowly because they require more data over a longer period of time. In embodiments, order information may be based on a single signal or based on a plurality of signals. Signals depending on the historical behavior of a financial instrument are programmed into the field programmable gate array. A few simple and well-known examples of a signal here are moving averages of past prices or book pressure signals (looking for an imbalance in the order book). Signal-based trading involves receiving market data on the financial instrument, constructing the order book for that instrument, calculating a predicted price based on a pre-defined collection of signals, and sending an order if the signals indicate that the signal indicates that it is a favorable time to trade. A secondary data stream here could be used to enable or disable signals or to change signal parameter values. In embodiments, the secondary data stream may be omitted. An example of a signal-based trading system might be a system that updates the quotes for a market maker when a set of signals indicates that a large directional move in the price of a stock is coming. The parallel processing advantage shows up here more so than in the first example.

* * * * * * *

[0190] Now that embodiments of the present invention have been shown and described in detail, various modifications and improvements thereon can become readily apparent to those skilled in the art. Accordingly, the exemplary embodiments of the present invention, as set forth above, are intended to be illustrative, not limiting. The spirit and scope of the present invention is to be construed broadly.

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CLAIMS

What is claimed is:

1. A method for processing a first serial data stream, using a field programmable gate array system, to generate a second serial data stream, wherein the method comprises the steps of:

(a) receiving, by a deserializer in a field programmable array, a clock signal;

(b) receiving, by the deserializer, the first serial data stream;

(c) generating, by the deserializer, a receiver side clock signal;

(d) converting, by the deserializer, the first serial data stream into a first plurality of parallel data streams;

(e) transmitting, from the deserializer to computational circuitry in the field programmable gate array, the first plurality of parallel data streams;

(f) transmitting, from the deserializer to a phase lock loop of the field programmable gate array system that is not within on the field programmable gate array, the receiver side clock signal;

(g) generating, using the phase lock loop, a second clock signal;

(h) generating, within the field programmable gate array, a transmitter side clock signal derived from the second clock signal;

(i) performing, by the computational circuitry, a set of operations on at least a portion of the first plurality of parallel data streams to generate a second plurality of parallel data streams; and

(j) transmitting, from the field programmable gate array system, the second serial data stream, derived from the second plurality of parallel data streams,

wherein said method does not use clock domain crossing operations that delay processing of the first set of parallel data streams.

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2. The method of claim 1, wherein the first serial data stream comprises market data, the second serial data stream comprises order entry data, and the set of operations are associated with a trading algorithm.

3. The method of claim 1, wherein the first serial data stream includes market data and the second serial data stream includes trading data.

4. The method of claim 1, wherein the set of operations includes at least one of the following:

(i) an arithmetic operation;

(ii) a logical operation;

(iii) a pipeline operation; and

(iv) a memory access operation.

5. The method of claim 1, wherein at least a portion of the set of operations performed in step (h) are performed prior to step (g).

6. The method of claim 1, wherein at least a portion of the set of operations performed in step (h) are performed after step (g).

7. The method of claim 1, wherein all of the set of operations performed in step (h) are performed after step (g).

8. The method of claim 1, wherein step (g) further comprises:

(i) generating, by the phase lock loop, a feedback clock signal associated with the transmitter side clock signal by performing the following steps until a first output of a phase detector of the field programmable gate array system is below a first threshold level:

(1) generating, by an adjustable oscillator in the field programmable gate array system, the second clock signal;

(2) generating, by the phase detector, the first output based on a comparison of the receiver side clock signal and the feedback clock signal obtained from the second clock signal;

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(3) transmitting, from the phase detector to a phase controller of the field programmable gate array system, the first output;

(4) determining, by the phase controller, interim adjustment information based on the first output; and

(5) transmitting, from the phase controller to the adjustable oscillator, the interim adjustment information;

wherein, the adjustable oscillator adjusts the second clock signal based on the interim adjustment information,

wherein steps (1) through (5) are repeated until the first output of the phase detector is below the first threshold level.

9. The method of claim 1, wherein the first plurality of data streams has the same number of data streams as the second plurality of data streams.

10. The method of claim 1, wherein the first plurality of data streams and the second plurality of data streams comprise one of the following:

(i) eight (8) data streams;

(ii) ten (10) data streams;

(iii) sixteen (16) data streams;

(iv) twenty (20) data streams;

(v) thirty-two (32) data streams;

(vi) forty (40) data streams;

(vii) sixty-four (64) data streams;

(viii) eighty (80) data streams;

(ix) one hundred twenty-eight (128) data streams; and

(x) one hundred sixty (160) data streams.

11. The method of claim 1, wherein the transmitter side clock signal and the receiver side clock signal have the same frequency and phase.

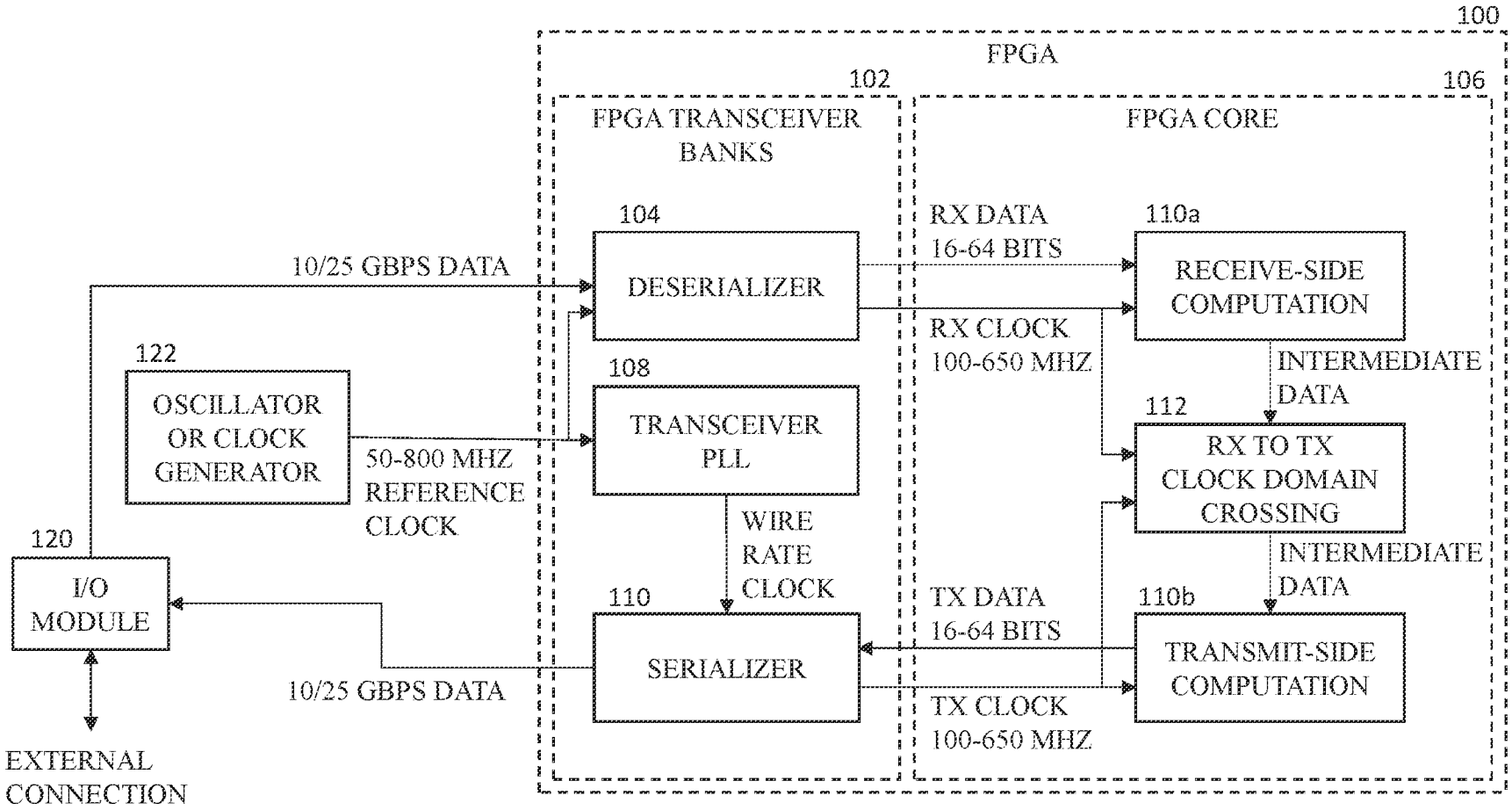
12. The method of claim 1, wherein the transmitter side clock signal and the receiver side clock signal have the same frequency and different phases.

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ABSTRACT

The present invention relates to a field programmable gate array system that provides phase control with minimal latency.

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PRIOR ART

FIG. 1

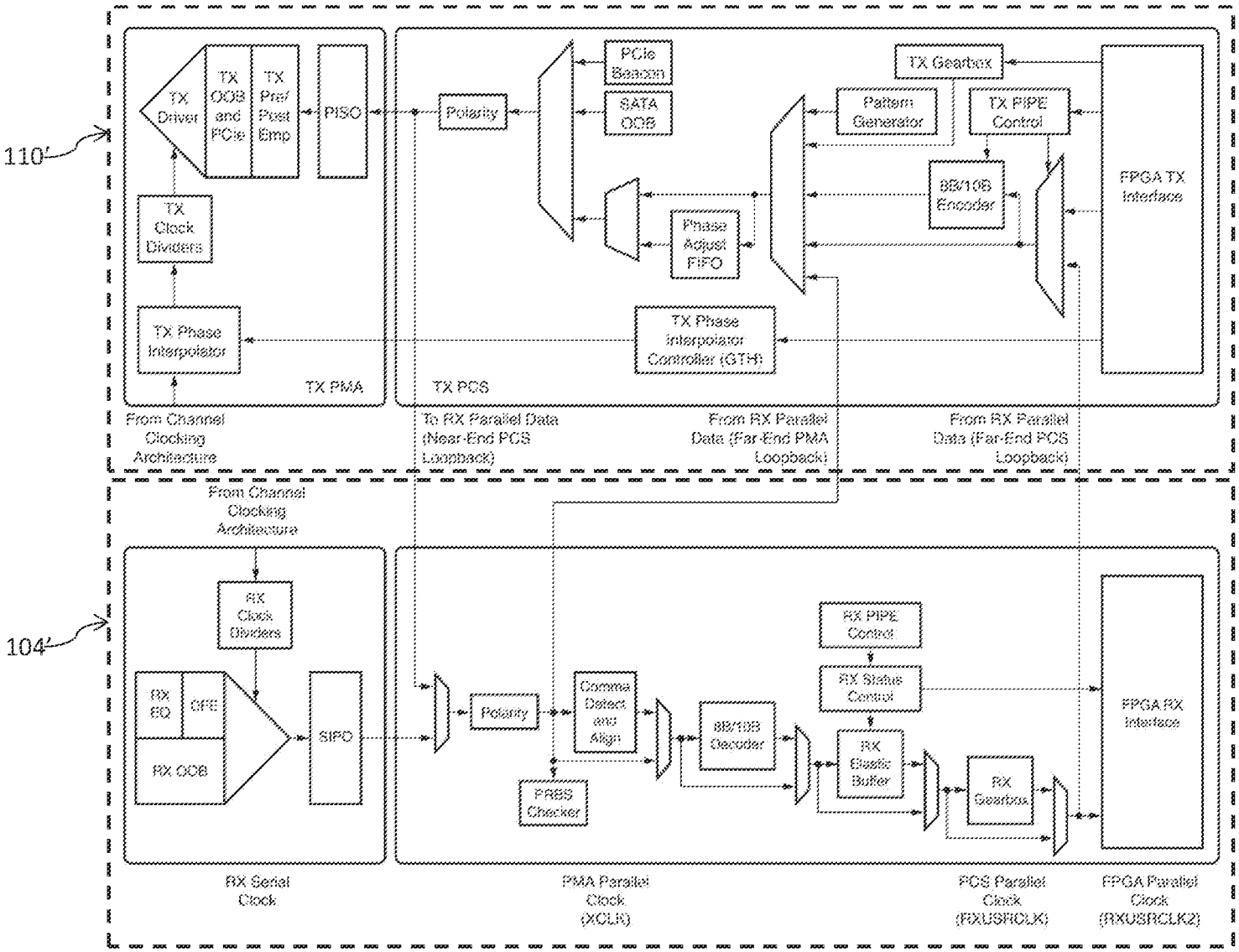


FIG. 1A

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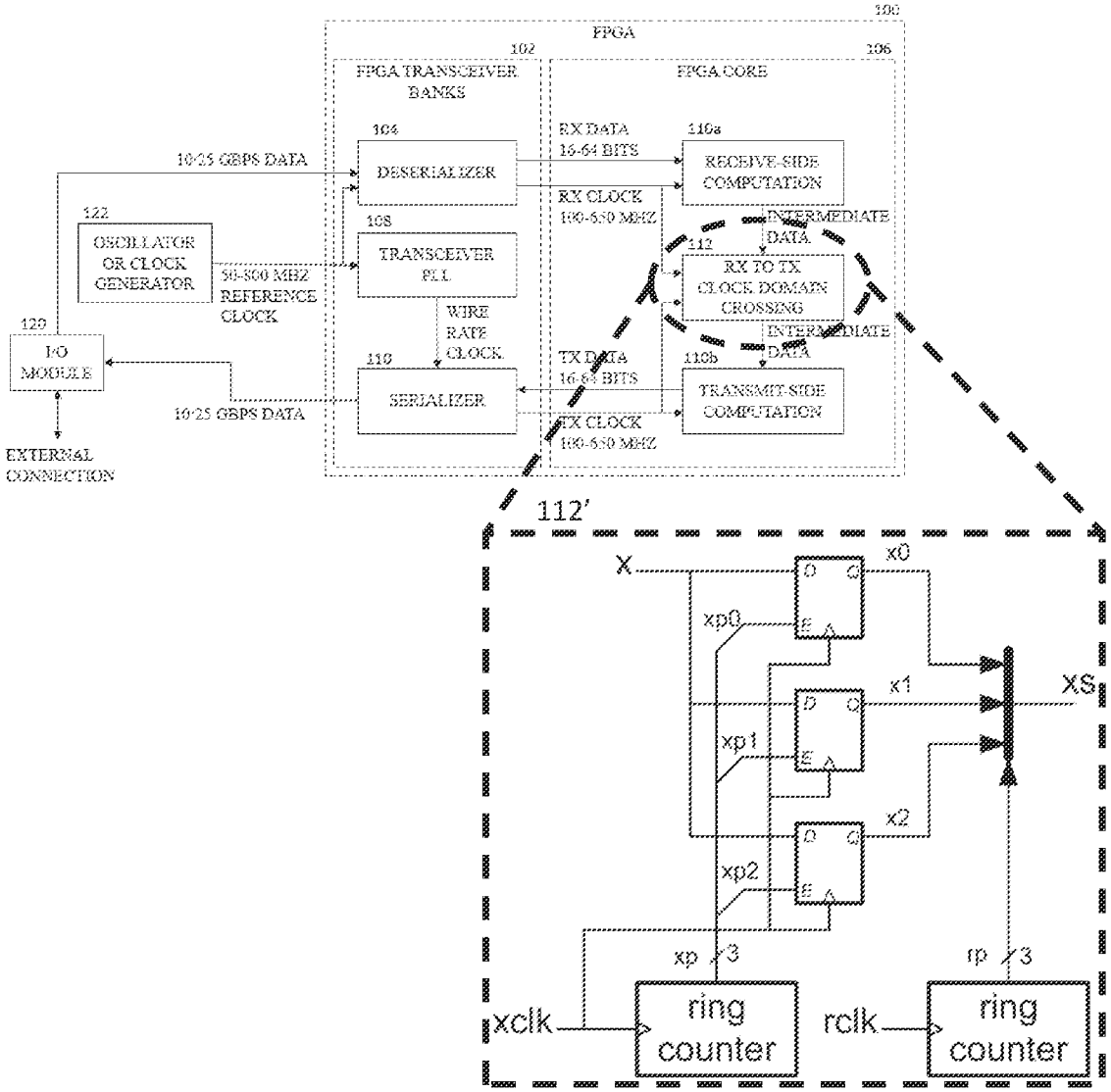

100
FPGA
102
FPGA TRANSCEIVER BANKS
106
FPGA CORE
104
DESERIALIZER
10-25 GBPS DATA
RX DATA 16-64 BITS
116a
RECEIVE-SIDE COMPUTATION
RX CLOCK 100-650 MHZ
INTERMEDIATE DATA
122
OSCILLATOR OR CLOCK GENERATOR
50-800 MHZ REFERENCE CLOCK
108
TRANSCEIVER PLL
112
RX TO TX CLOCK DOMAIN CROSSING
WIRE RATE CLOCK
INTERMEDIATE DATA
120
I/O MODULE
110
SERIALIZER
TX DATA 16-64 BITS
116b
TRANSMIT-SIDE COMPUTATION
10-25 GBPS DATA
TX CLOCK 100-650 MHZ
EXTERNAL CONNECTION
112'
X
x0
xp0
x1
xs
xp1
x2
xp2
xp
3
rp
3
xclk
ring counter
rclk
ring counter

FIG. 1B

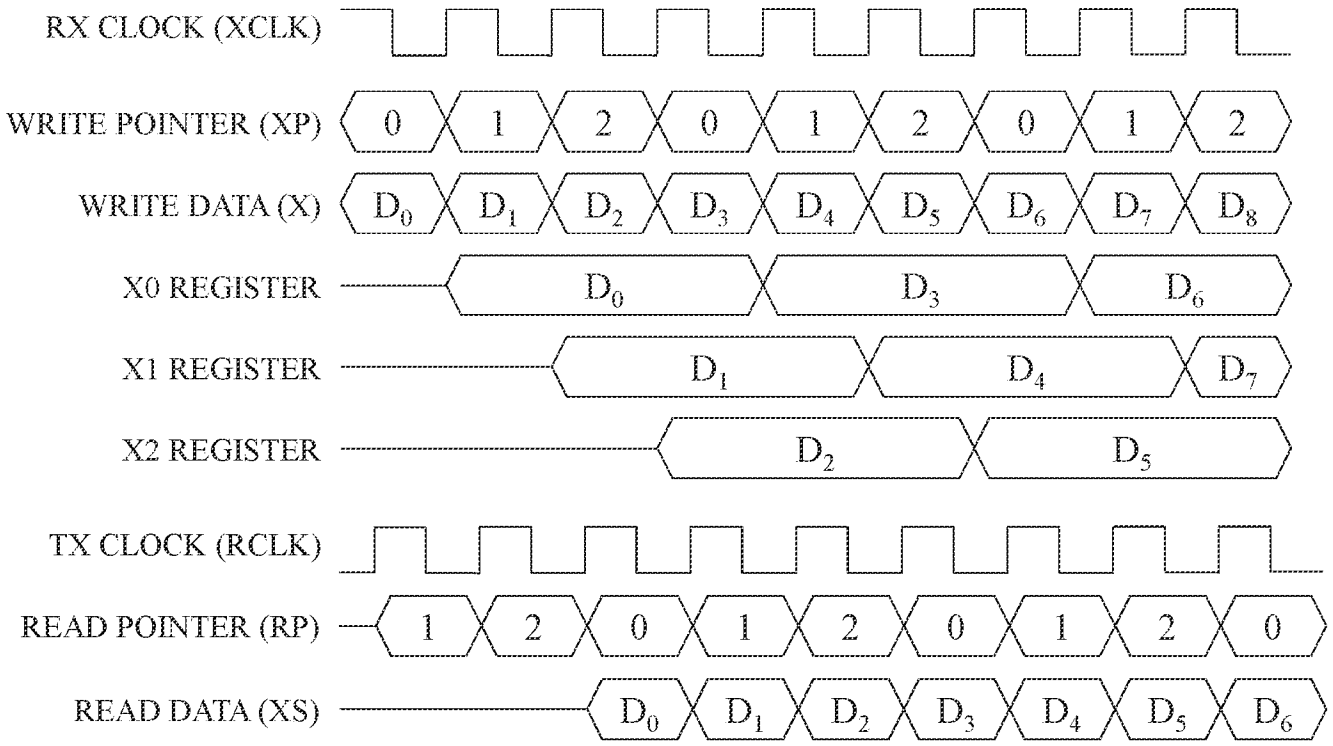

RX CLOCK (XCLK)
WRITE POINTER (XP)
0 1 2 0 1 2 0 1 2
WRITE DATA (X)
D0 D1 D2 D3 D4 D5 D6 D7 D8
X0 REGISTER
D0 D3 D6
X1 REGISTER
D1 D4 D7
X2 REGISTER
D2 D5
TX CLOCK (RCLK)
READ POINTER (RP)
1 2 0 1 2 0 1 2 0
READ DATA (XS)
D0 D1 D2 D3 D4 D5 D6

FIG. 1C

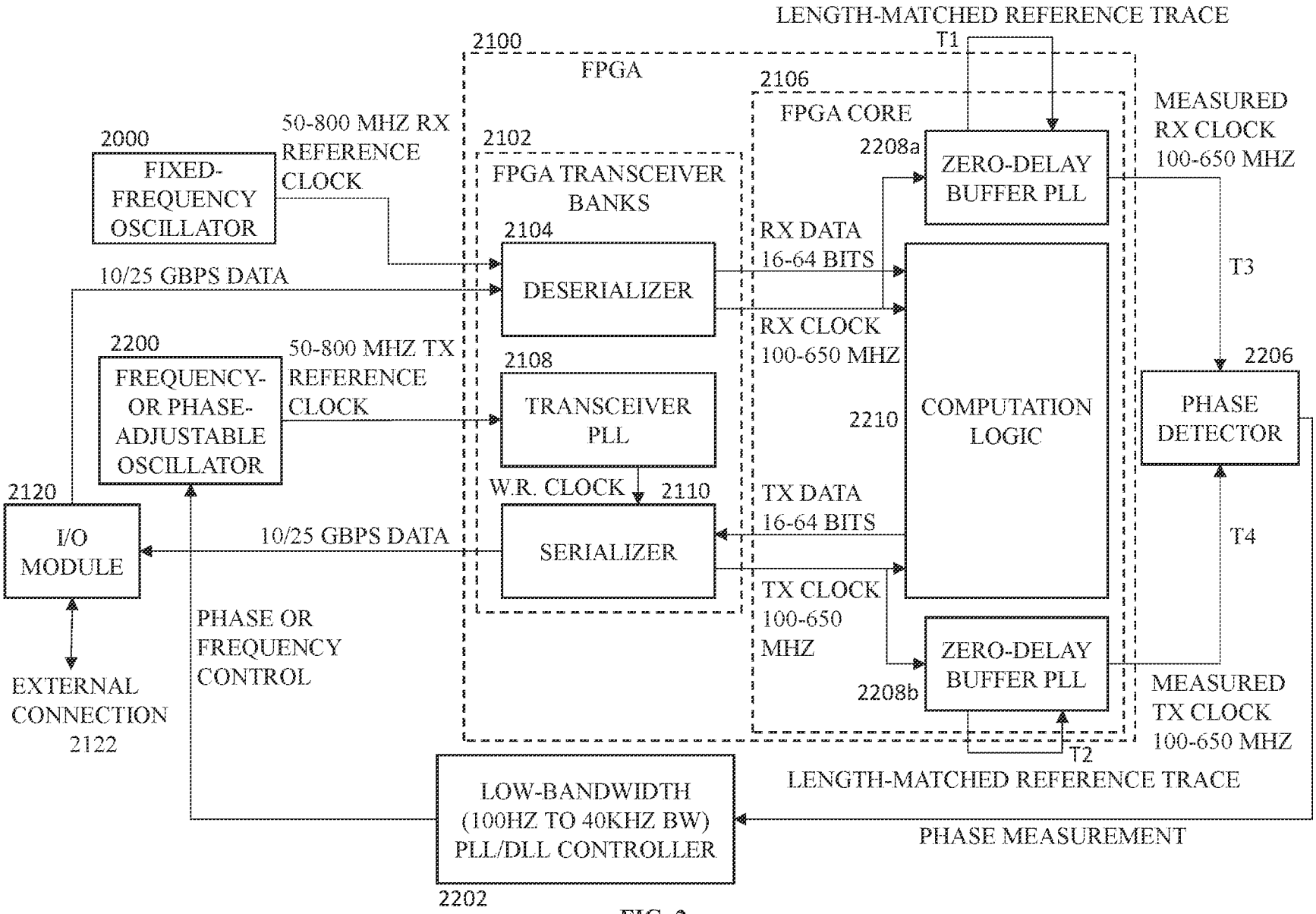

LENGTH-MATCHED REFERENCE TRACE
T1
2100
FPGA
2106
FPGA CORE
MEASURED
RX CLOCK
100-650 MHZ
2000
FIXED-
FREQUENCY
OSCILLATOR
50-800 MHZ RX
REFERENCE
CLOCK
2102
FPGA TRANSCEIVER
BANKS
2208a
ZERO-DELAY
BUFFER PLL
2104
RX DATA
16-64 BITS
10/25 GBPS DATA
DESERIALIZER
T3
RX CLOCK
100-650 MHZ
2200
FREQUENCY-
OR PHASE-
ADJUSTABLE
OSCILLATOR
50-800 MHZ TX
REFERENCE
CLOCK
2108
TRANSCEIVER
PLL
2206
PHASE
DETECTOR
2210
COMPUTATION
LOGIC
2120
I/O
MODULE
W.R. CLOCK
2110
TX DATA
16-64 BITS
10/25 GBPS DATA
SERIALIZER
T4
TX CLOCK
100-650
MHZ
PHASE OR
FREQUENCY
CONTROL
ZERO-DELAY
BUFFER PLL
2208b
MEASURED
TX CLOCK
100-650 MHZ
EXTERNAL
CONNECTION
2122
T2
LENGTH-MATCHED REFERENCE TRACE
LOW-BANDWIDTH
(100HZ TO 40KHZ BW)
PLL/DLL CONTROLLER
PHASE MEASUREMENT
2202

FIG. 2

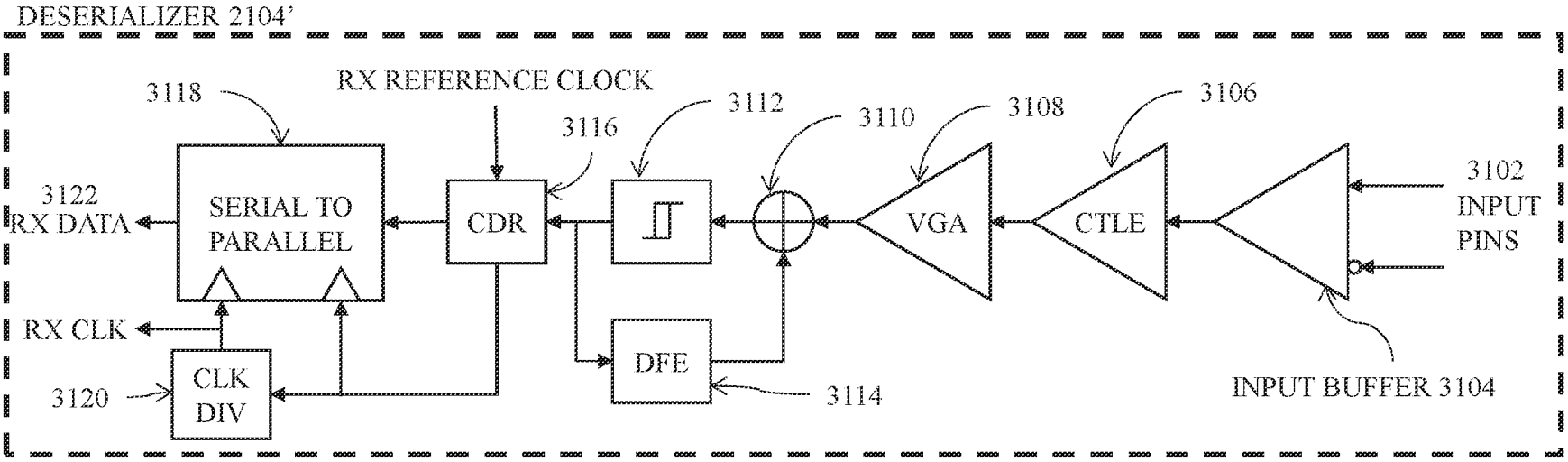

DESERIALIZER 2104'
3118
RX REFERENCE CLOCK
3116
3112
3110
3108
3106
3102
INPUT
PINS
3122
RX DATA
SERIAL TO
PARALLEL
CDR
VGA
CTLE
RX CLK
CLK
DIV
3120
DFE
3114
INPUT BUFFER 3104

FIG. 3A

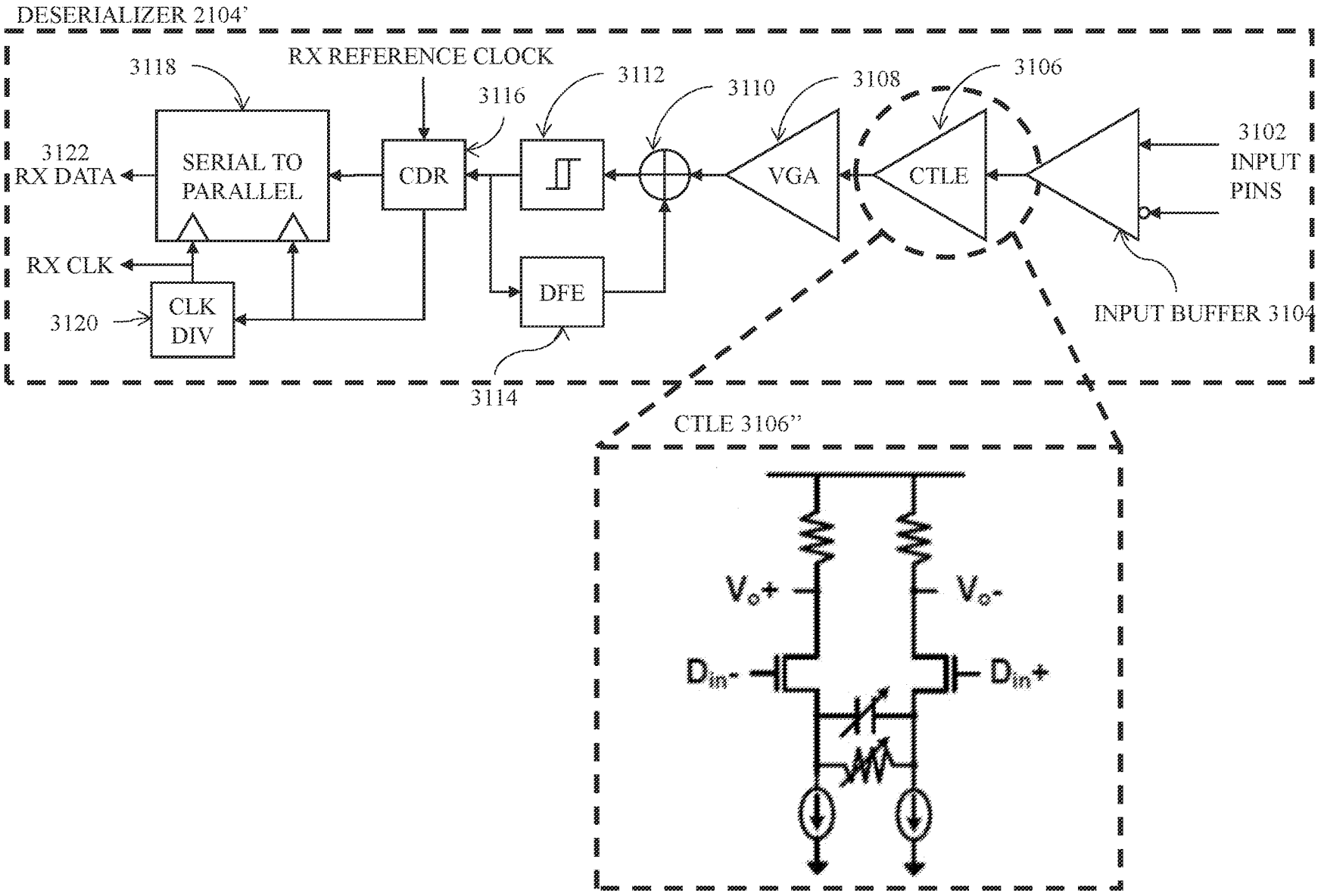

DESERIALIZER 2104'
3118
RX REFERENCE CLOCK
3116
3112
3110
3108
3106
3102
INPUT
PINS
3122
RX DATA
SERIAL TO
PARALLEL
CDR
VGA
CTLE
RX CLK
DFE
INPUT BUFFER 3104
3120
CLK
DIV
3114
CTLE 3106''
Vo+
Vo-
Din-
Din+

FIG. 3B

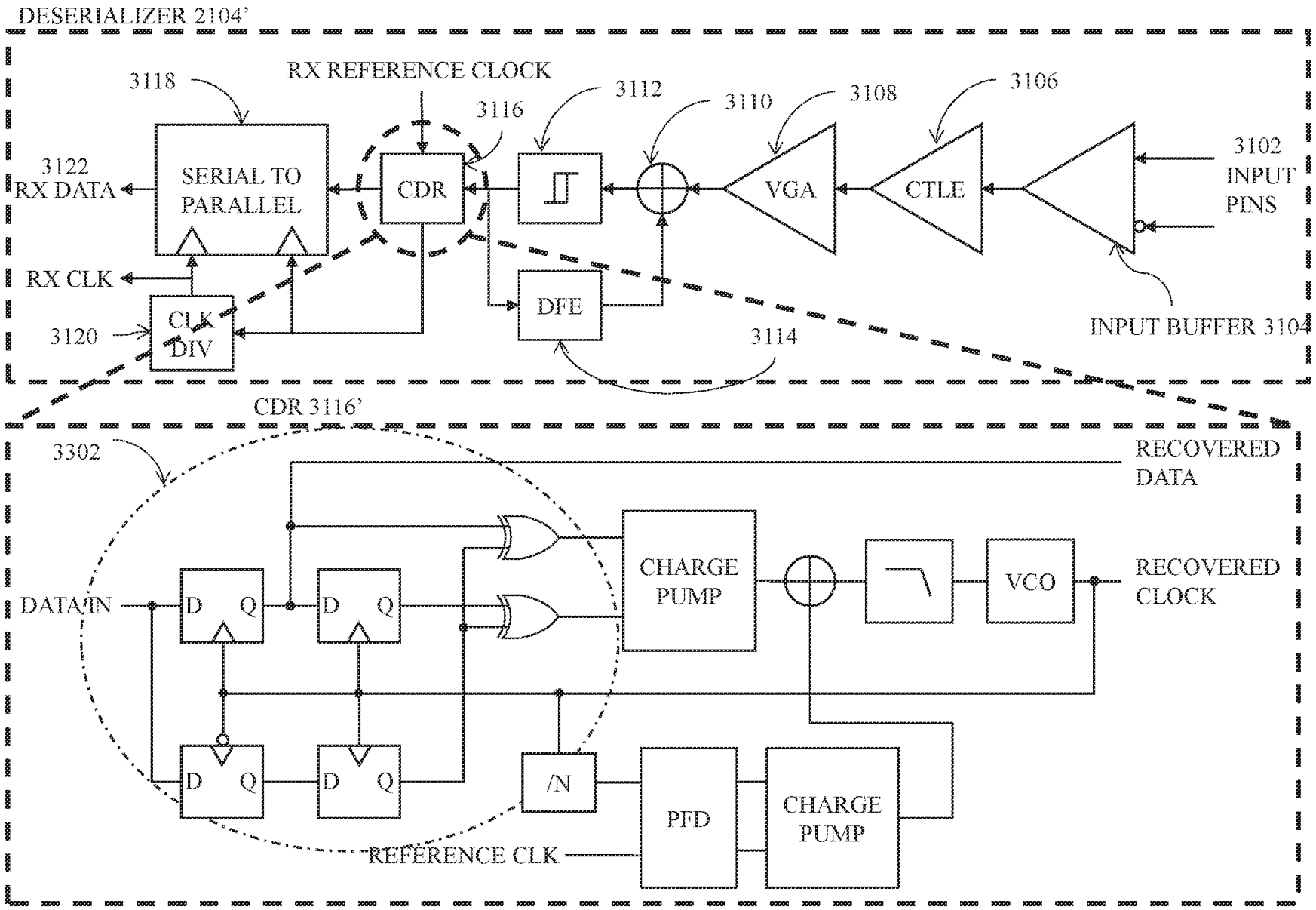

DESERIALIZER 2104'
3118
RX REFERENCE CLOCK
3116
3112
3110
3108
3106
3102
INPUT
PINS
3122
RX DATA
SERIAL TO
PARALLEL
CDR
VGA
CTLE
RX CLK
DFE
CLK
DIV
3120
3114
INPUT BUFFER 3104
CDR 3116'
3302
RECOVERED
DATA
CHARGE
PUMP
VCO
RECOVERED
CLOCK
DATA IN
D
Q
/N
PFD
CHARGE
PUMP
REFERENCE CLK

FIG. 3C

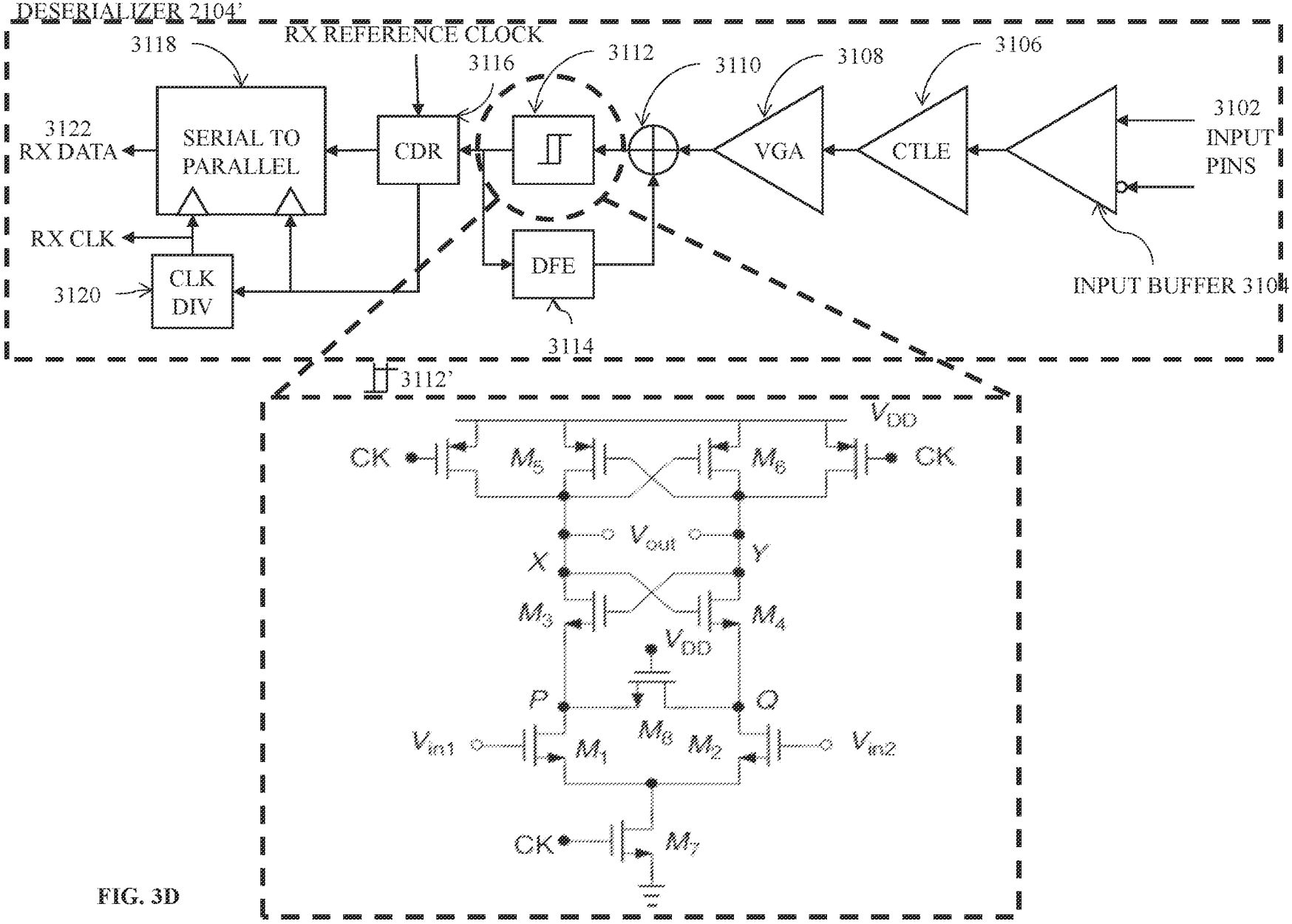

DESERIALIZER 2104'
RX REFERENCE CLOCK
3118
3116
3112
3110
3108
3106
3102
INPUT PINS
3122
RX DATA
SERIAL TO PARALLEL
CDR
VGA
CTLE
RX CLK
CLK DIV
3120
DFE
INPUT BUFFER 3104
3114
3112'
V_{DD}
CK
M_5
M_6
CK
V_{out}
X
Y
M_3
M_4
V_{DD}
P
Q
V_{in1}
M_1
M_8
M_2
V_{in2}
CK
M_7

FIG. 3D

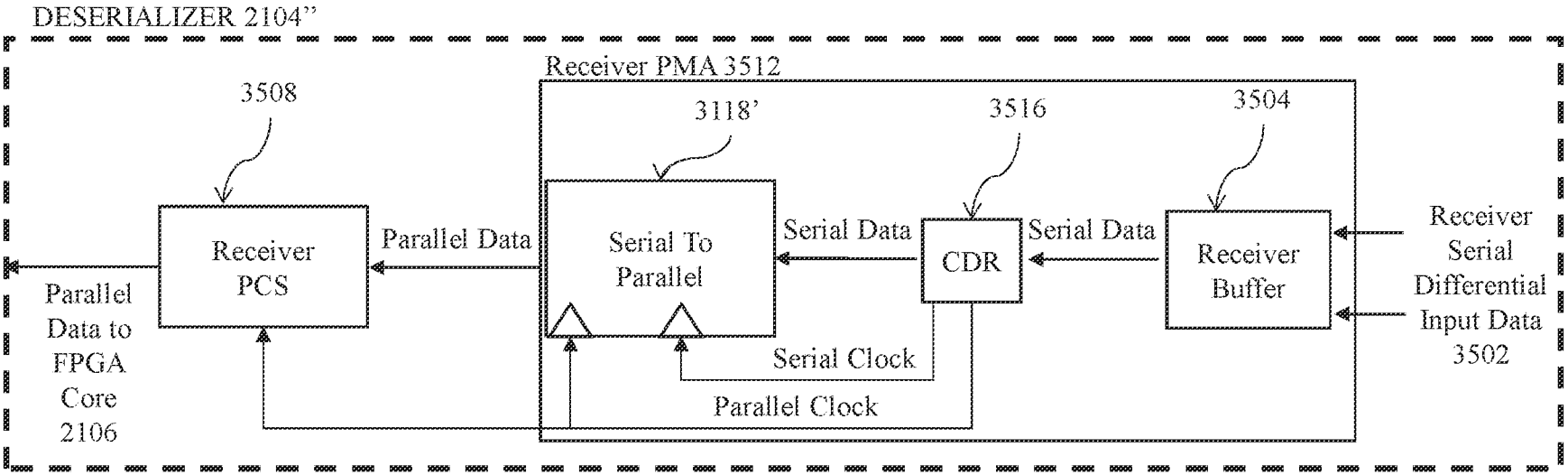

DESERIALIZER 2104''
Receiver PMA 3512
3508
3118'
3516
3504
Receiver PCS
Parallel Data
Serial To Parallel
Serial Data
CDR
Serial Data
Receiver Buffer
Receiver Serial Differential Input Data 3502
Parallel Data to FPGA Core 2106
Serial Clock
Parallel Clock

FIG. 3E

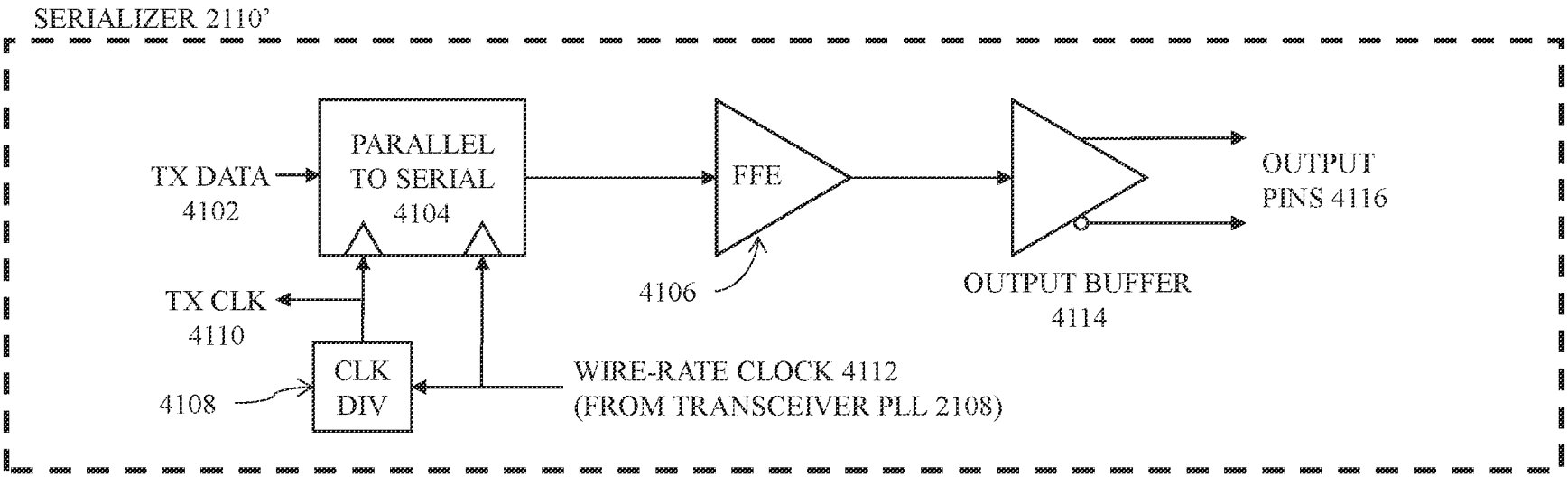

SERIALIZER 2110'
TX DATA
4102
PARALLEL
TO SERIAL
4104
FFE
4106
OUTPUT BUFFER
4114
OUTPUT
PINS 4116
TX CLK
4110
4108
CLK
DIV
WIRE-RATE CLOCK 4112
(FROM TRANSCEIVER PLL 2108)

FIG. 4A

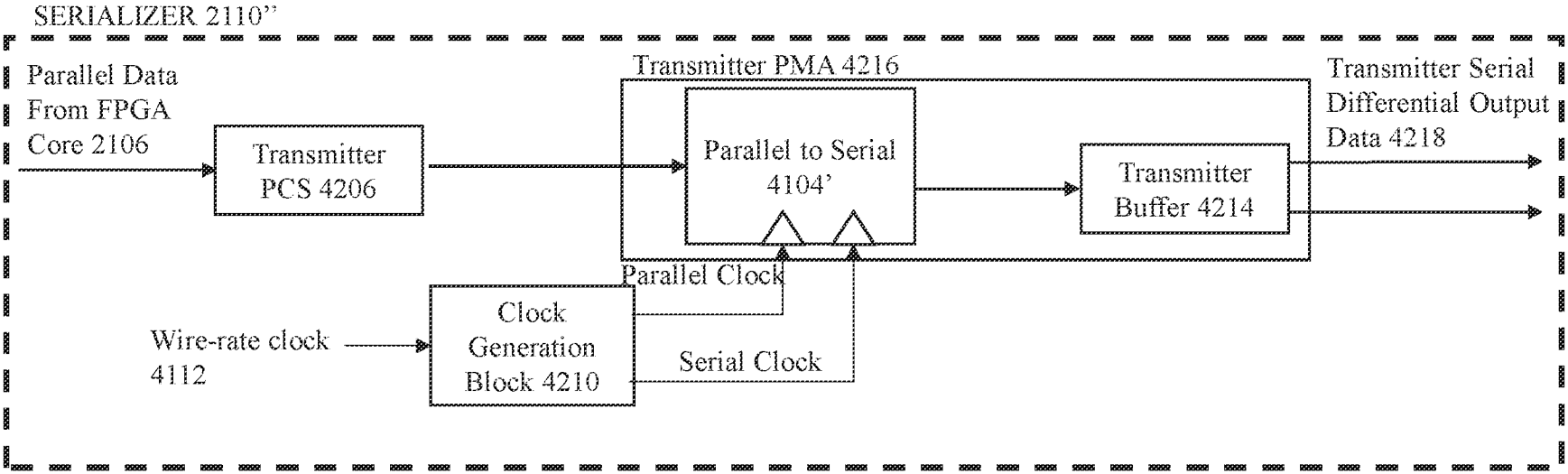

SERIALIZER 2110''
Parallel Data
From FPGA
Core 2106
Transmitter
PCS 4206
Transmitter PMA 4216
Parallel to Serial
4104'
Transmitter
Buffer 4214
Transmitter Serial
Differential Output
Data 4218
Parallel Clock
Wire-rate clock
4112
Clock
Generation
Block 4210
Serial Clock

FIG. 4B

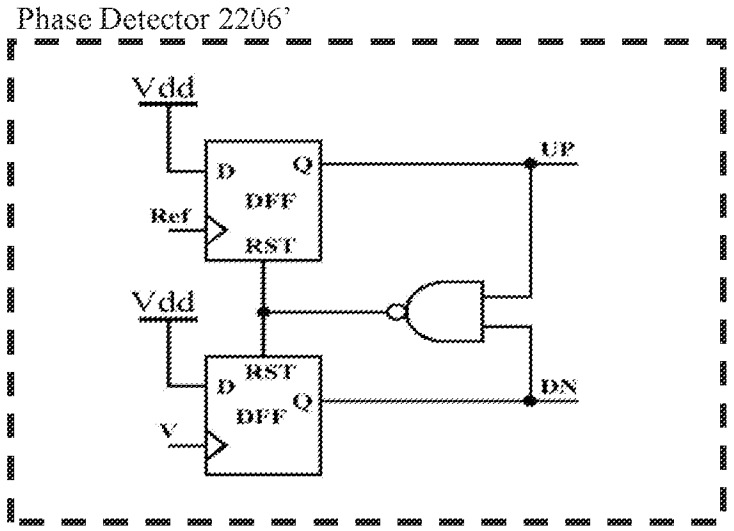


FIG. 5A

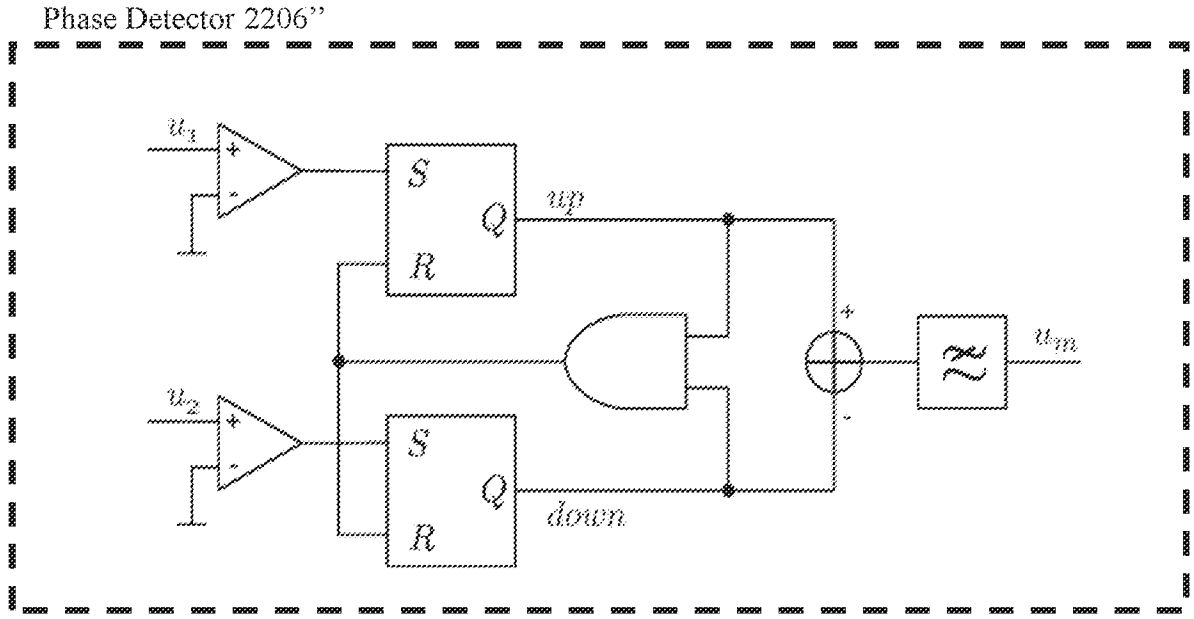


FIG. 5B

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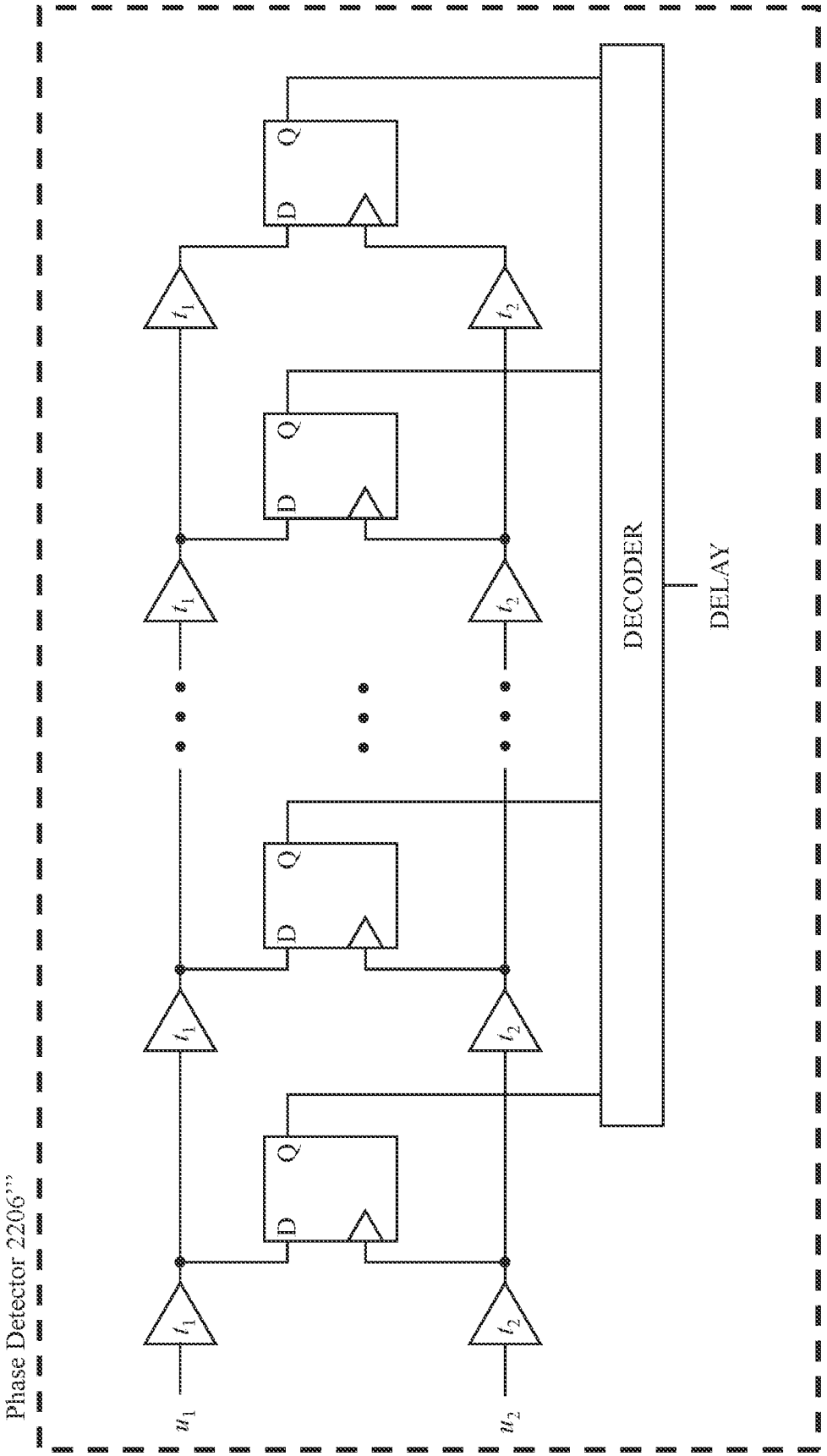


FIG. 5C

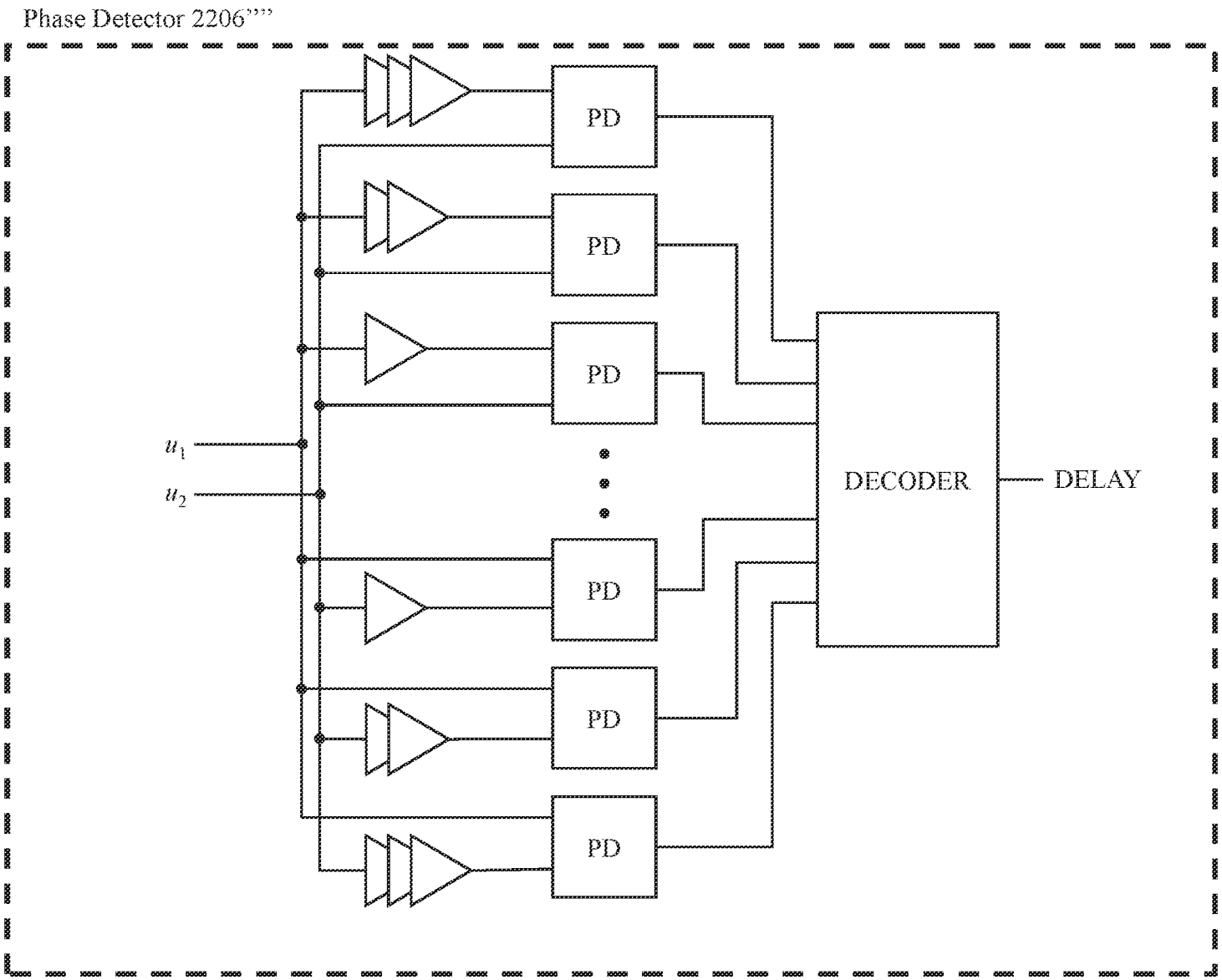


FIG. 5D

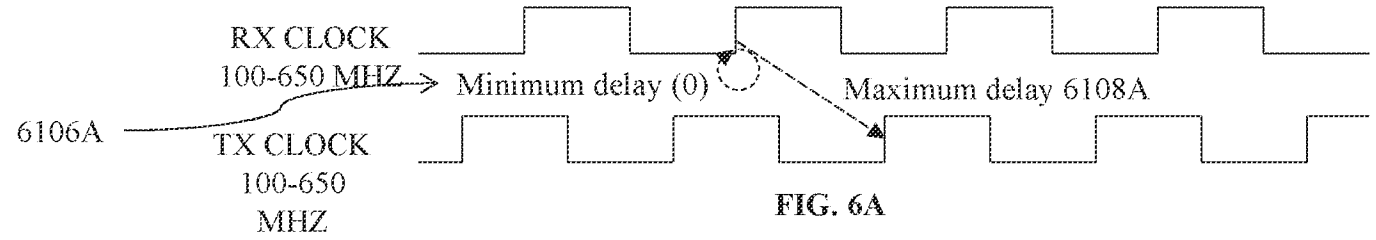


FIG. 6A

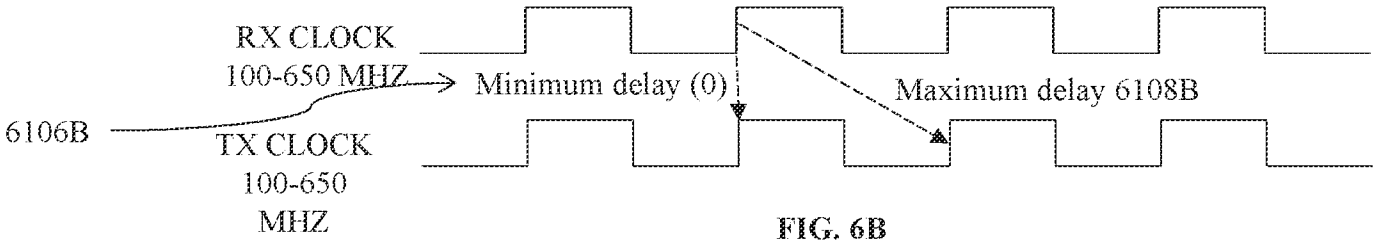


FIG. 6B

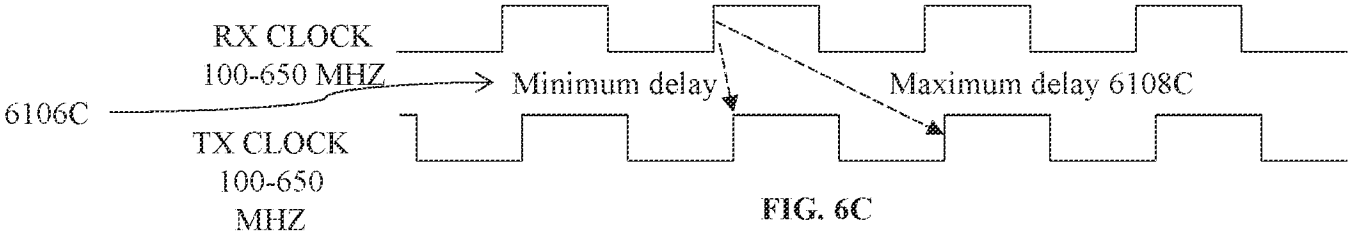


FIG. 6C

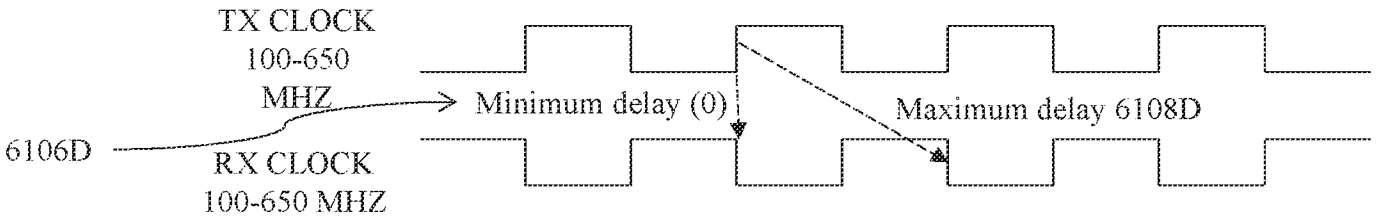


FIG. 6D

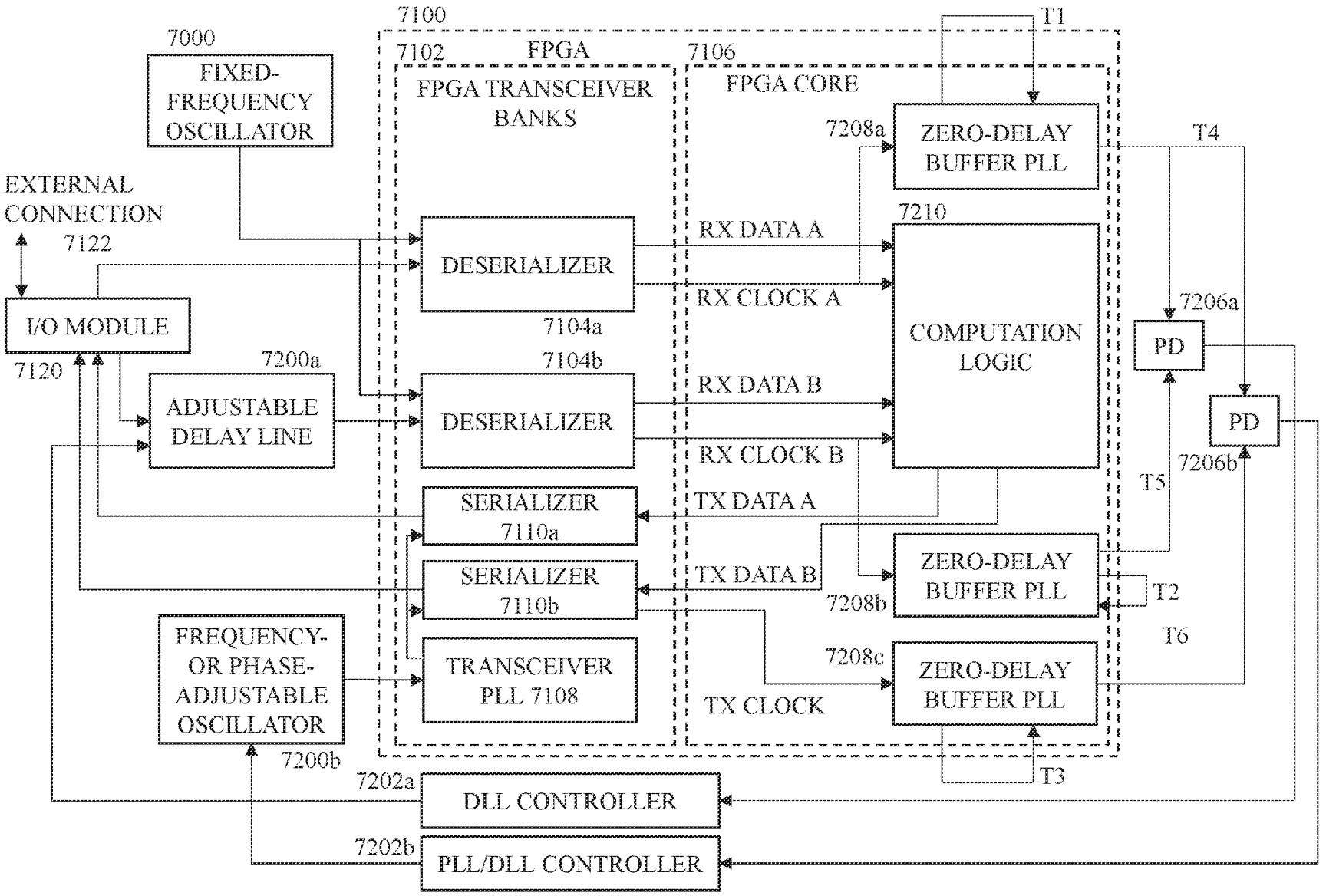

7100
T1
7000
FIXED-FREQUENCY OSCILLATOR
7102
FPGA
7106
FPGA TRANSCEIVER BANKS
FPGA CORE
7208a
ZERO-DELAY BUFFER PLL
T4
EXTERNAL CONNECTION
7122
7210
RX DATA A
DESERIALIZER
RX CLOCK A
7206a
I/O MODULE
7104a
COMPUTATION LOGIC
PD
7120
7200a
7104b
RX DATA B
ADJUSTABLE DELAY LINE
DESERIALIZER
PD
RX CLOCK B
7206b
T5
SERIALIZER 7110a
TX DATA A
SERIALIZER 7110b
TX DATA B
ZERO-DELAY BUFFER PLL
7208b
T2
T6
FREQUENCY- OR PHASE-ADJUSTABLE OSCILLATOR
TRANSCEIVER PLL 7108
7208c
ZERO-DELAY BUFFER PLL
TX CLOCK
7200b
T3
7202a
DLL CONTROLLER
7202b
PLL/DLL CONTROLLER

FIG. 7A

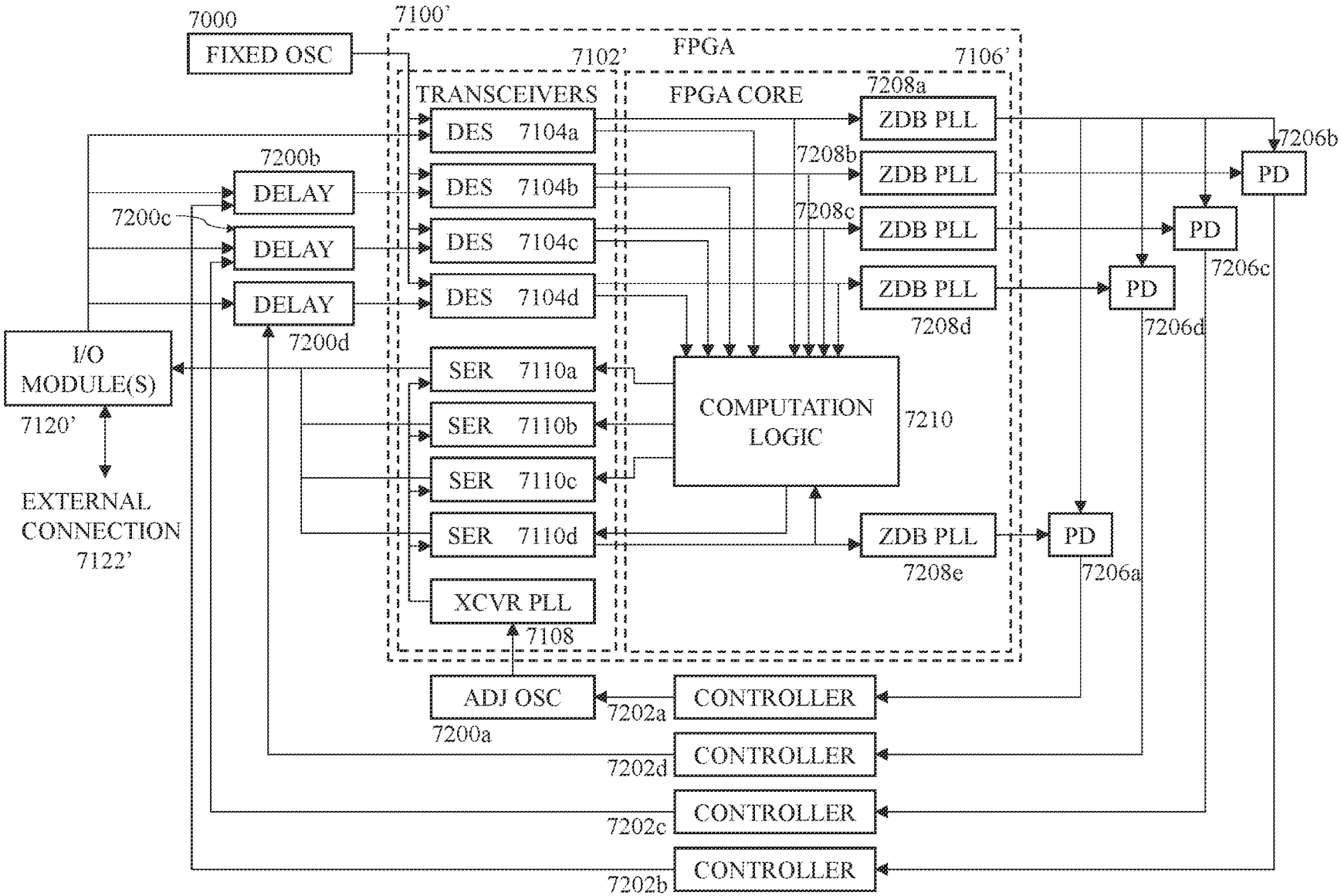

7000
FIXED OSC
7100'
FPGA
7102'
TRANSCEIVERS
FPGA CORE
7106'
7208a
ZDB PLL
7206b
PD
7200b
DELAY
DES 7104a
7208b
ZDB PLL
PD
7200c
DELAY
DES 7104b
7208c
ZDB PLL
PD
7206c
DELAY
DES 7104c
ZDB PLL
PD
7206d
7200d
DES 7104d
7208d
I/O
MODULE(S)
7120'
SER 7110a
COMPUTATION
LOGIC
7210
SER 7110b
SER 7110c
EXTERNAL
CONNECTION
7122'
SER 7110d
ZDB PLL
PD
7208e
7206a
XCVR PLL
7108
ADJ OSC
7200a
CONTROLLER
7202a
CONTROLLER
7202d
CONTROLLER
7202c
CONTROLLER
7202b

FIG. 7B

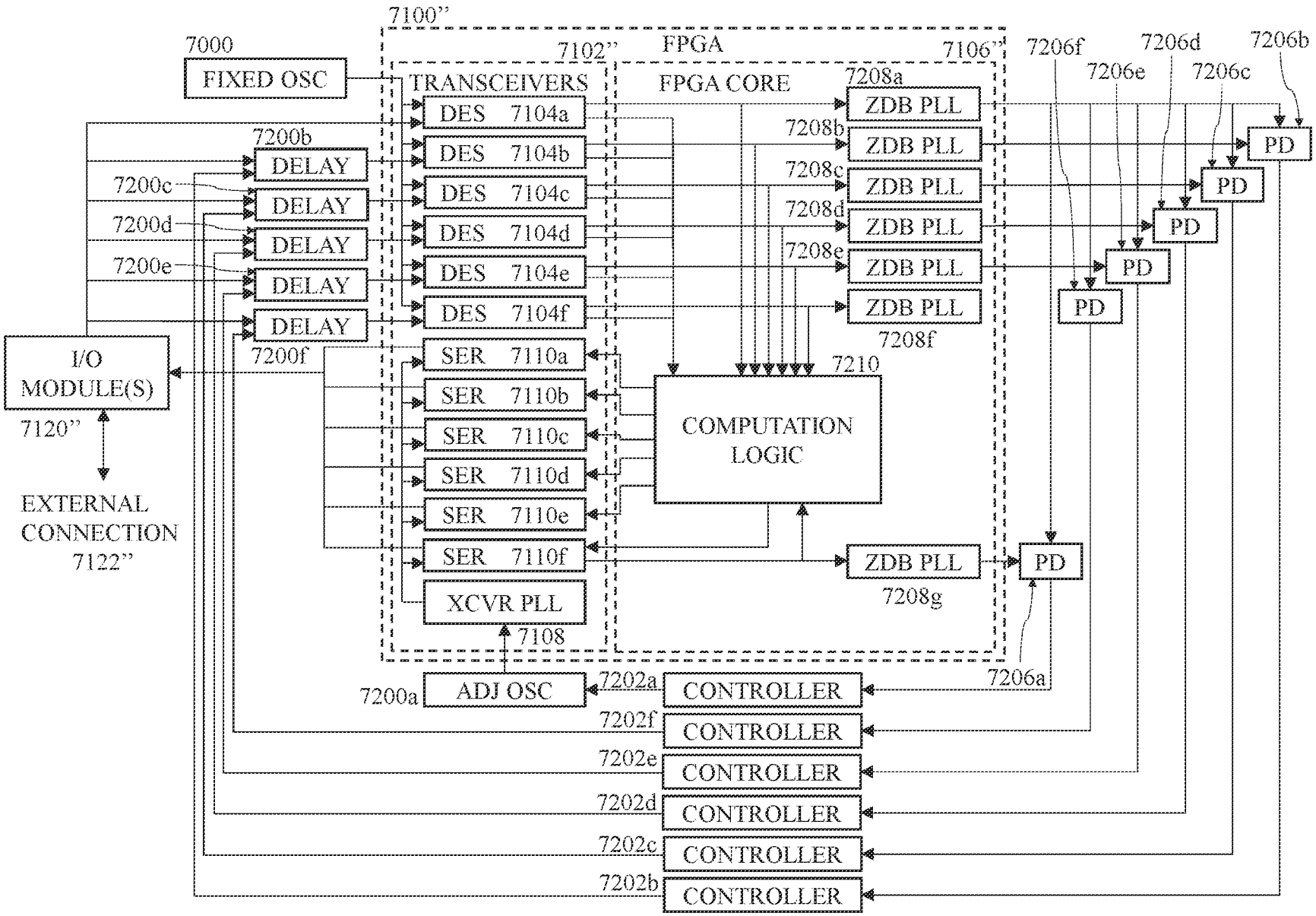

7100''
7000
FIXED OSC
7102''
FPGA
7106''
TRANSCEIVERS
FPGA CORE
DES 7104a
DES 7104b
DES 7104c
DES 7104d
DES 7104e
DES 7104f
7200b
DELAY
7200c
DELAY
7200d
DELAY
7200e
DELAY
DELAY
7200f
I/O MODULE(S)
7120''
EXTERNAL CONNECTION 7122''
SER 7110a
SER 7110b
SER 7110c
SER 7110d
SER 7110e
SER 7110f
XCVR PLL
7108
7210
COMPUTATION LOGIC
7208a
ZDB PLL
7208b
ZDB PLL
7208c
ZDB PLL
7208d
ZDB PLL
7208e
ZDB PLL
ZDB PLL
7208f
ZDB PLL
7208g
7206f
7206e
7206d
7206c
7206b
PD
PD
PD
PD
PD
PD
7206a
7200a
ADJ OSC
7202a
CONTROLLER
7202f
CONTROLLER
7202e
CONTROLLER
7202d
CONTROLLER
7202c
CONTROLLER
7202b
CONTROLLER

FIG. 7C

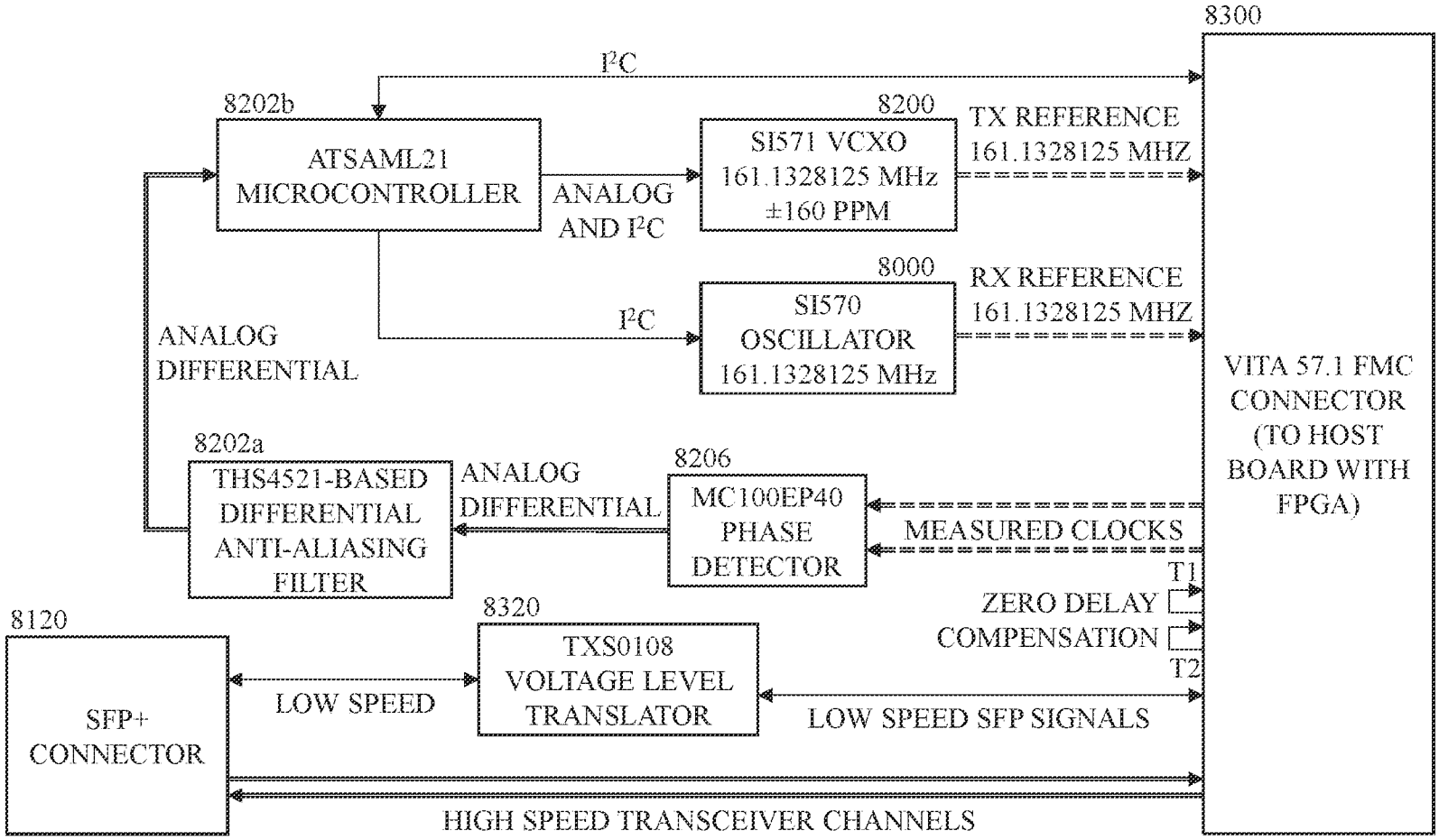

8300
I²C
8202b
ATSAML21
MICROCONTROLLER
ANALOG
AND I²C
8200
SI571 VCXO
161.1328125 MHz
±160 PPM
TX REFERENCE
161.1328125 MHZ
8000
SI570
OSCILLATOR
161.1328125 MHz
I²C
RX REFERENCE
161.1328125 MHZ
ANALOG
DIFFERENTIAL
VITA 57.1 FMC
CONNECTOR
(TO HOST
BOARD WITH
FPGA)
8202a
THS4521-BASED
DIFFERENTIAL
ANTI-ALIASING
FILTER
ANALOG
DIFFERENTIAL
8206
MC100EP40
PHASE
DETECTOR
MEASURED CLOCKS
T1
ZERO DELAY
COMPENSATION
T2
8120
SFP+
CONNECTOR
8320
TXS0108
VOLTAGE LEVEL
TRANSLATOR
LOW SPEED
LOW SPEED SFP SIGNALS
HIGH SPEED TRANSCEIVER CHANNELS

FIG. 8A

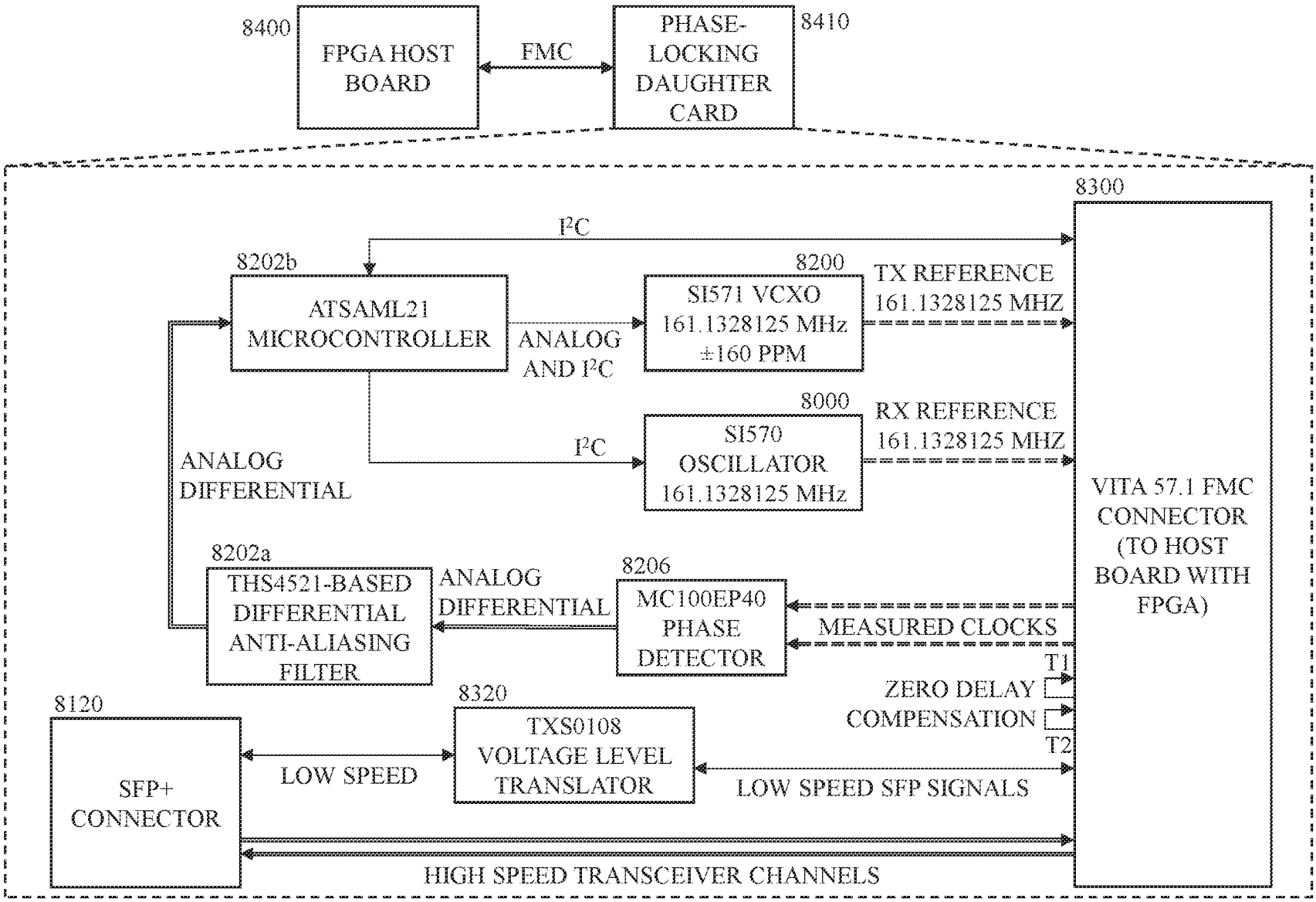

8400
FPGA HOST BOARD
FMC
PHASE-LOCKING DAUGHTER CARD
8410
8300
I²C
8202b
ATSAML21 MICROCONTROLLER
ANALOG AND I²C
8200
SI571 VCXO 161.1328125 MHz ±160 PPM
TX REFERENCE 161.1328125 MHZ
8000
SI570 OSCILLATOR 161.1328125 MHz
RX REFERENCE 161.1328125 MHZ
I²C
ANALOG DIFFERENTIAL
VITA 57.1 FMC CONNECTOR (TO HOST BOARD WITH FPGA)
8202a
THS4521-BASED DIFFERENTIAL ANTI-ALIASING FILTER
ANALOG DIFFERENTIAL
8206
MC100EP40 PHASE DETECTOR
MEASURED CLOCKS
T1
ZERO DELAY COMPENSATION
T2
8120
SFP+ CONNECTOR
8320
TXS0108 VOLTAGE LEVEL TRANSLATOR
LOW SPEED
LOW SPEED SFP SIGNALS
HIGH SPEED TRANSCEIVER CHANNELS

FIG. 8B

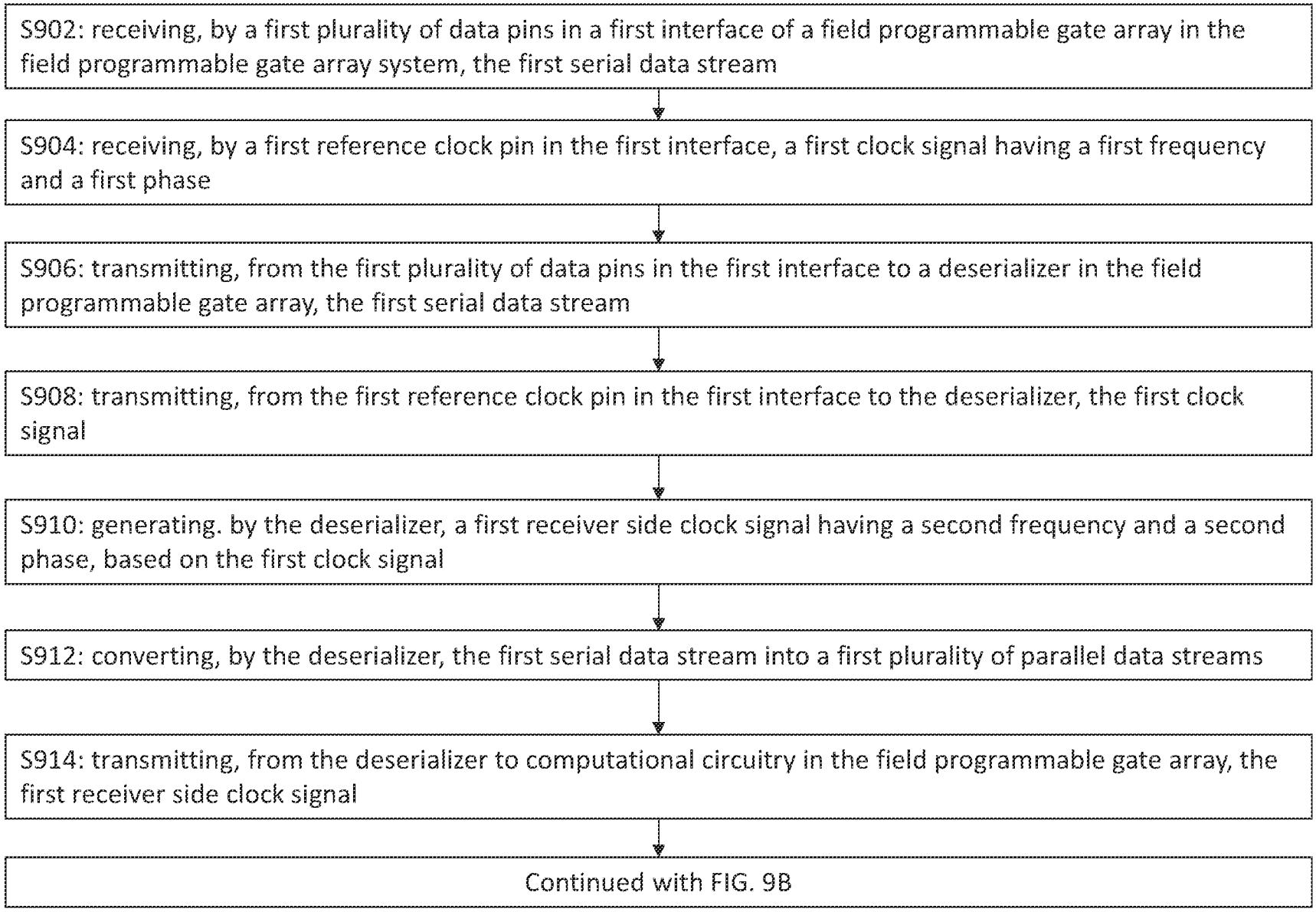

S902: receiving, by a first plurality of data pins in a first interface of a field programmable gate array in the field programmable gate array system, the first serial data stream
S904: receiving, by a first reference clock pin in the first interface, a first clock signal having a first frequency and a first phase
S906: transmitting, from the first plurality of data pins in the first interface to a deserializer in the field programmable gate array, the first serial data stream
S908: transmitting, from the first reference clock pin in the first interface to the deserializer, the first clock signal
S910: generating. by the deserializer, a first receiver side clock signal having a second frequency and a second phase, based on the first clock signal
S912: converting, by the deserializer, the first serial data stream into a first plurality of parallel data streams
S914: transmitting, from the deserializer to computational circuitry in the field programmable gate array, the first receiver side clock signal
Continued with FIG. 9B

FIG. 9A

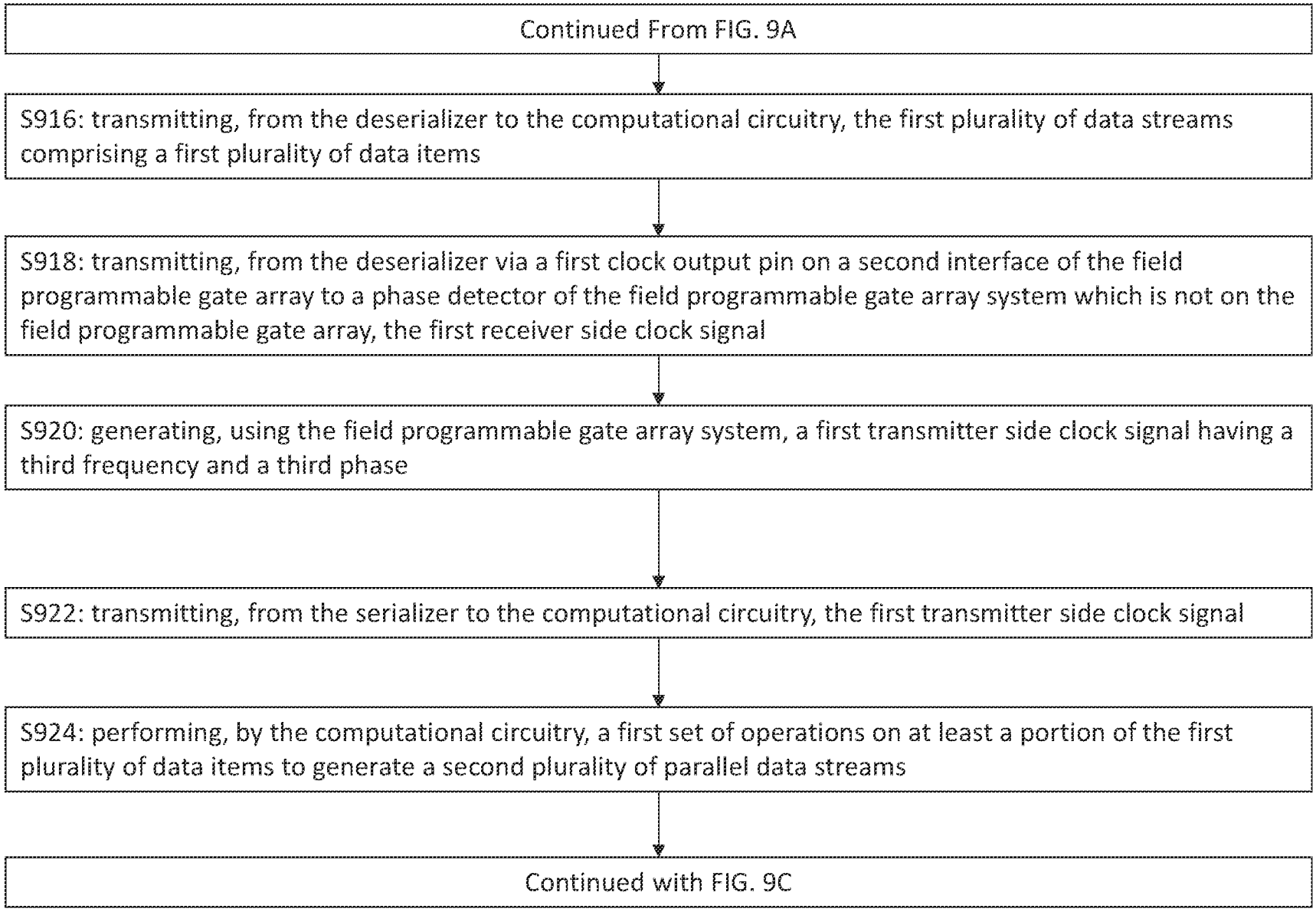

Continued From FIG. 9A
S916: transmitting, from the deserializer to the computational circuitry, the first plurality of data streams comprising a first plurality of data items
S918: transmitting, from the deserializer via a first clock output pin on a second interface of the field programmable gate array to a phase detector of the field programmable gate array system which is not on the field programmable gate array, the first receiver side clock signal
S920: generating, using the field programmable gate array system, a first transmitter side clock signal having a third frequency and a third phase
S922: transmitting, from the serializer to the computational circuitry, the first transmitter side clock signal
S924: performing, by the computational circuitry, a first set of operations on at least a portion of the first plurality of data items to generate a second plurality of parallel data streams
Continued with FIG. 9C

FIG. 9B

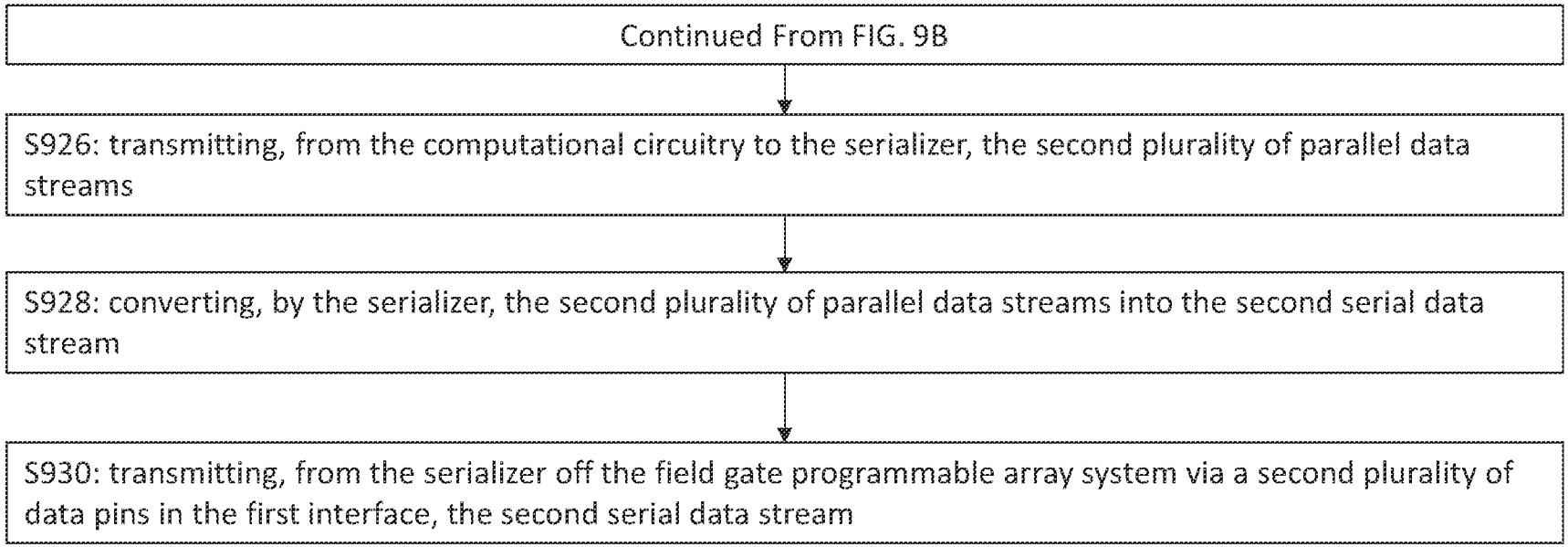

Continued From FIG. 9B
S926: transmitting, from the computational circuitry to the serializer, the second plurality of parallel data streams
S928: converting, by the serializer, the second plurality of parallel data streams into the second serial data stream
S930: transmitting, from the serializer off the field gate programmable array system via a second plurality of data pins in the first interface, the second serial data stream

FIG. 9C

S920: generating, using the field programmable gate array system, a first transmitter side clock signal having a third frequency and a third phase, by performing the following steps until a first output of the phase detector is below a first threshold level

S1002: generating, by an adjustable oscillator in the field programmable gate array system, a second clock signal having a fourth frequency and a fourth phase

S1004: generating a first wire rate clock signal having a fifth frequency and a fifth phase based on the second clock signal

S1006: generating, by a serializer in the field programmable gate array, an interim transmitter side clock signal having a sixth frequency and a sixth phase

S1008: transmitting, from the serializer via a second clock output pin in the second interface to the phase detector, the interim transmitter side clock signal

Continued with FIG. 10B

FIG. 10A

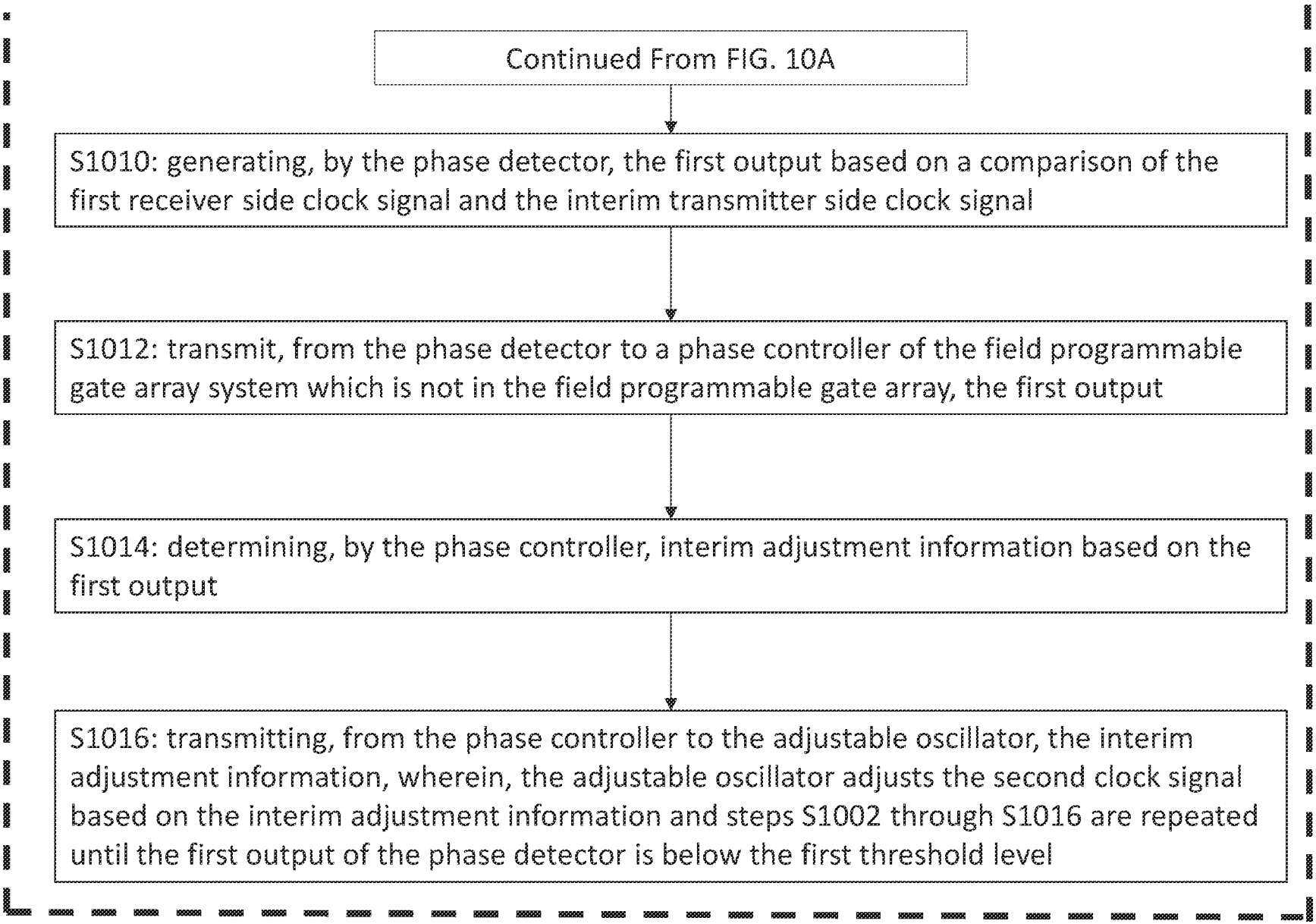

Continued From FIG. 10A
S1010: generating, by the phase detector, the first output based on a comparison of the first receiver side clock signal and the interim transmitter side clock signal
S1012: transmit, from the phase detector to a phase controller of the field programmable gate array system which is not in the field programmable gate array, the first output
S1014: determining, by the phase controller, interim adjustment information based on the first output
S1016: transmitting, from the phase controller to the adjustable oscillator, the interim adjustment information, wherein, the adjustable oscillator adjusts the second clock signal based on the interim adjustment information and steps S1002 through S1016 are repeated until the first output of the phase detector is below the first threshold level

FIG. 10B

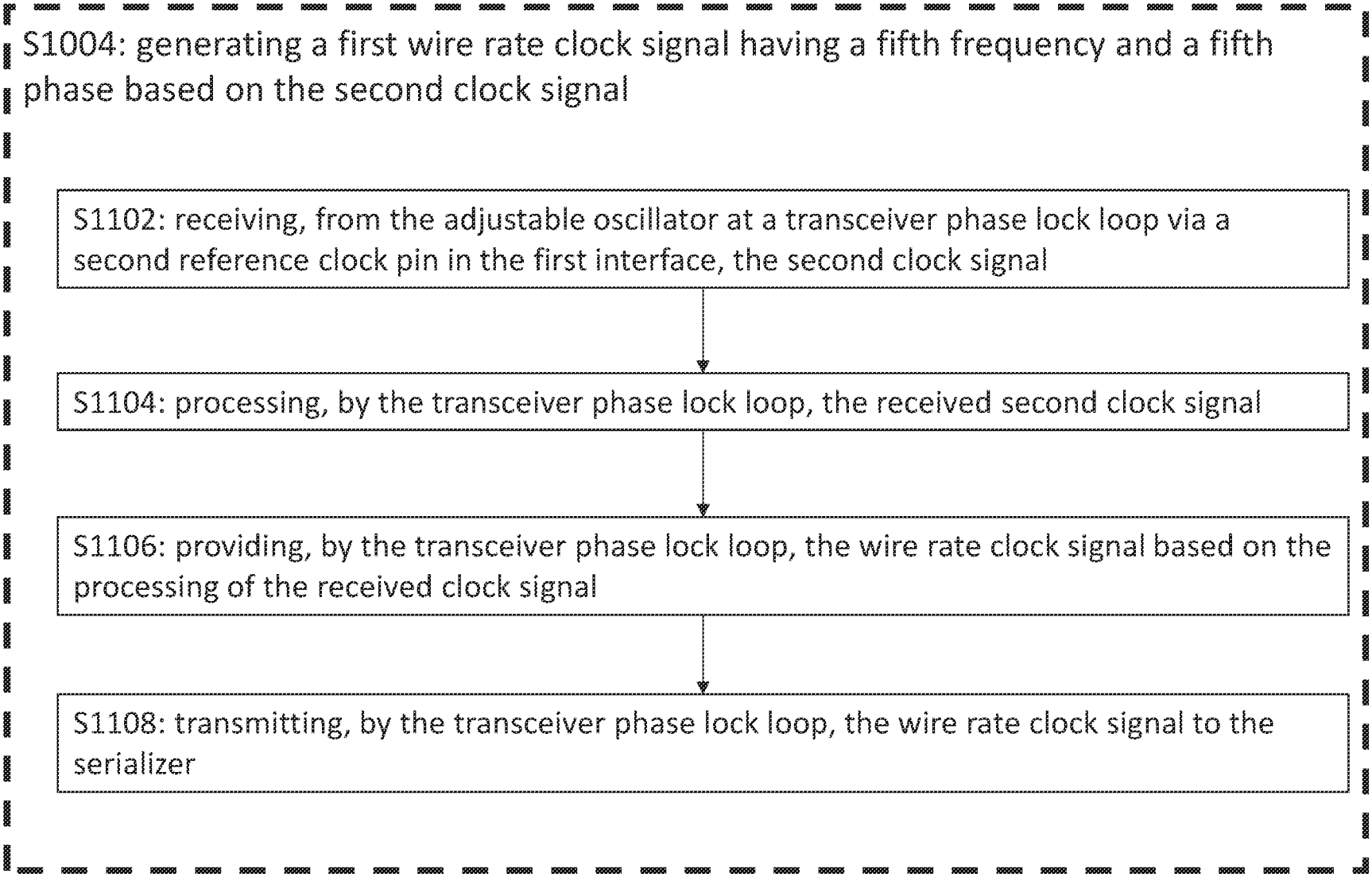

S1004: generating a first wire rate clock signal having a fifth frequency and a fifth phase based on the second clock signal
S1102: receiving, from the adjustable oscillator at a transceiver phase lock loop via a second reference clock pin in the first interface, the second clock signal
S1104: processing, by the transceiver phase lock loop, the received second clock signal
S1106: providing, by the transceiver phase lock loop, the wire rate clock signal based on the processing of the received clock signal
S1108: transmitting, by the transceiver phase lock loop, the wire rate clock signal to the serializer

FIG. 11

PTO/SB/35 (07-09)
Approved for use through 11/30/2020. OMB 0651-0031
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NONPUBLICATION REQUEST UNDER 35 U.S.C. 122(b)(2)(B)(i)

First Named Inventor	Nima Badizadegan
Title	FIELD PROGRAMMABLE GATE ARRAY WITH
Attorney Docket Number	00287-0017

I hereby certify that the invention disclosed in the attached application **has not and will not be** the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

I hereby request that the attached application not be published under 35 U.S.C. 122(b).

/Keith J. Barkaus/ — Signature

2022-04-18 — Date

Keith J. Barkaus — Typed or printed name

51,431 — Registration Number, if applicable

212-336-8000 — Telephone Number

This request must be signed in compliance with 37 CFR 1.33(b) and submitted with the application **upon filing.**

Applicant may rescind this nonpublication request at any time. If applicant rescinds a request that an application not be published under 35 U.S.C. 122(b), the application will be scheduled for publication at eighteen months from the earliest claimed filing date for which a benefit is claimed.

If applicant subsequently files an application directed to the invention disclosed in the attached application in another country, or under a multilateral international agreement, that requires publication of applications eighteen months after filing, the applicant **must** notify the United States Patent and Trademark Office of such filing within forty-five (45) days after the date of the filing of such foreign or international application. **Failure to do so will result in abandonment of this application (35 U.S.C. 122(b)(2)(B)(iii)).**

This collection of information is required by 37 CFR 1.213(a). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 6 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal

Application Number:	
Filing Date:	
Title of Invention:	FIELD PROGRAMMABLE GATE ARRAY WITH EXTERNAL PHASE-LOCKED LOOP
First Named Inventor/Applicant Name:	Nima Badizadegan
Filer:	Keith J. Barkaus/Victoria Gilmore
Attorney Docket Number:	00287-0017

Filed as Small Entity

Filing Fees for Track I Prioritized Examination - Nonprovisional Application under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
UTILITY FILING FEE (ELECTRONIC FILING)	4011	1	80	80
UTILITY SEARCH FEE	2111	1	350	350
UTILITY EXAMINATION FEE	2311	1	400	400
REQUEST FOR PRIORITIZED EXAMINATION	2817	1	2100	2100
Pages:				
Claims:				
Miscellaneous-Filing:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
PUBL. FEE- EARLY, VOLUNTARY, OR NORMAL	1504	1	0	0
PROCESSING FEE, EXCEPT PROV. APPLS.	2830	1	70	70

Petition:	
Patent-Appeals-and-Interference:	
Post-Allowance-and-Post-Issuance:	
Extension-of-Time:	
Miscellaneous:	
Total in USD ($)	**3000**

Electronic Acknowledgement Receipt

EFS ID:	45498717
Application Number:	17723145
International Application Number:	
Confirmation Number:	1635
Title of Invention:	FIELD PROGRAMMABLE GATE ARRAY WITH EXTERNAL PHASE-LOCKED LOOP
First Named Inventor/Applicant Name:	Nima Badizadegan
Customer Number:	1912
Filer:	Keith J. Barkaus/Victoria Gilmore
Filer Authorized By:	Keith J. Barkaus
Attorney Docket Number:	00287-0017
Receipt Date:	18-APR-2022
Filing Date:	
Time Stamp:	17:42:52
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$3000
RAM confirmation Number	E20224HH43071520
Deposit Account	
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Application Data Sheet	WebADS.pdf	196933 6d69670333e796d0c9b6c3b31af9956785e72cb9	no	8
Warnings:					
Information:					
2	Track One Request	1-424.pdf	129650 9e7ed0d58235b87cfc9f7092603eb3fa27458f87	no	2
Warnings:					
Information:					
3	Oath or Declaration filed	2-ParentDeclaration.pdf	156542 0c9d6692764db60d7989a36d0f737b306e300114	no	1
Warnings:					
Information:					
4	Power of Attorney	3-PowerofAtty.pdf	272022 8e434df72eeec83b14152a710e728e7ff48f59ec	no	2
Warnings:					
Information:					
5		4-Specification.pdf	248988 4773765a1d49539e8242a5eb8254f552ff7fa584	yes	45

Multipart Description/PDF files in .zip description

Document Description	Start	End
Specification	1	40
Claims	41	44
Abstract	45	45

Warnings:					
Information:					
6	Drawings-only black and white line drawings	5-Drawings.pdf	905645 cb90dd66e46aa5f4b0edb3e2e8f78569442f73cb	no	26
Warnings:					
Information:					
7	Nonpublication request from applicant	6-NonPublicationRqst.pdf	211313 3564e7419bbddbec5d6e8e6cbe25a0ba4ea72f7a	no	2
Warnings:					
Information:					
8	Fee Worksheet (SB06)	fee-info.pdf	50994 e5dac24e059fccf5aef7dab4d5d1ce702c89efd2	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	2172087		

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	00287-0017
	Application Number	
Title of Invention	FIELD PROGRAMMABLE GATE ARRAY WITH EXTERNAL PHASE-LOCKED LOOP	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2:

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor 1

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Nima		Badizadegan	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

City	Salem	State/Province	NH	Country of Residence i	US

Mailing Address of Inventor:

Address 1	61 Kelly Rd		
Address 2			
City	Salem	State/Province	NH
Postal Code	03079	Country i	US

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

☐ **An Address is being provided for the correspondence Information of this application.**

Customer Number	1912		
Email Address	ptodocket@arelaw.com	Add Email	Remove Email

Application Information:

Title of the Invention	FIELD PROGRAMMABLE GATE ARRAY WITH EXTERNAL PHASE-LOCKED LOOP		
Attorney Docket Number	00287-0017	Small Entity Status Claimed	☒
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	26	Suggested Figure for Publication (if any)	

PTO/AIA/14 (08-15)
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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	00287-0017
	Application Number	
Title of Invention	FIELD PROGRAMMABLE GATE ARRAY WITH EXTERNAL PHASE-LOCKED LOOP	

Filing By Reference:

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☒ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32).
Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:	◉ Customer Number	○ US Patent Practitioner	○ Limited Recognition (37 CFR 11.9)
Customer Number	1912		

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Registration Number					

Prefix	**Given Name**	Middle Name	**Family Name**	Suffix	Remove
Registration Number					

Additional Representative Information blocks may be generated within this form by selecting the **Add** button.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	00287-0017
	Application Number	
Title of Invention	FIELD PROGRAMMABLE GATE ARRAY WITH EXTERNAL PHASE-LOCKED LOOP	

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, 365(c), or 386(c) or indicate National Stage entry from a PCT application. Providing benefit claim information in the Application Data Sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.
When referring to the current application, please leave the "Application Number" field blank.

Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
	Continuation of	17405188	2021-08-18

Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
17405188	Continuation of	17248304	2021-01-19	11128305	2021-09-21

Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
17248304	Continuation of	16937314	2020-07-23	10931286	2021-02-23

Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
16937314	Continuation of	16672076	2019-11-01	10826502	2020-11-03

Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16672076	Claims benefit of provisional	62803017	2019-02-08

Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16672076	Claims benefit of provisional	62755804	2018-11-05

Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button.

Foreign Priority Information:

PTO/AIA/14 (08-15)
Approved for use through 04/30/2017. OMB 0651-0032
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	00287-0017
	Application Number	
Title of Invention	FIELD PROGRAMMABLE GATE ARRAY WITH EXTERNAL PHASE-LOCKED LOOP	

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55. When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX) the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(i)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

Application Number	Country[i]	Filing Date (YYYY-MM-DD)	Access Code[i] (if applicable)

Additional Foreign Priority Data may be generated within this form by selecting the **Add** button.

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.
NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

PTO/AIA/14 (08-15)
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	00287-0017
	Application Number	
Title of Invention	FIELD PROGRAMMABLE GATE ARRAY WITH EXTERNAL PHASE-LOCKED LOOP	

Authorization or Opt-Out of Authorization to Permit Access:

When this Application Data Sheet is properly signed and filed with the application, applicant has provided written authority to permit a participating foreign intellectual property (IP) office access to the instant application-as-filed (see paragraph A in subsection 1 below) and the European Patent Office (EPO) access to any search results from the instant application (see paragraph B in subsection 1 below).

Should applicant choose not to provide an authorization identified in subsection 1 below, applicant **must opt-out** of the authorization by checking the corresponding box A or B or both in subsection 2 below.

NOTE: This section of the Application Data Sheet is **ONLY** reviewed and processed with the **INITIAL** filing of an application. After the initial filing of an application, an Application Data Sheet cannot be used to provide or rescind authorization for access by a foreign IP office(s). Instead, Form PTO/SB/39 or PTO/SB/69 must be used as appropriate.

1. Authorization to Permit Access by a Foreign Intellectual Property Office(s)

A. Priority Document Exchange (PDX) - Unless box A in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the State Intellectual Property Office of the People's Republic of China (SIPO), the World Intellectual Property Organization (WIPO), and any other foreign intellectual property office participating with the USPTO in a bilateral or multilateral priority document exchange agreement in which a foreign application claiming priority to the instant patent application is filed, access to: (1) the instant patent application-as-filed and its related bibliographic data, (2) any foreign or domestic application to which priority or benefit is claimed by the instant application and its related bibliographic data, and (3) the date of filing of this Authorization. See 37 CFR 1.14(h)(1).

B. Search Results from U.S. Application to EPO - Unless box B in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the EPO access to the bibliographic data and search results from the instant patent application when a European patent application claiming priority to the instant patent application is filed. See 37 CFR 1.14(h)(2).

The applicant is reminded that the EPO's Rule 141(1) EPC (European Patent Convention) requires applicants to submit a copy of search results from the instant application without delay in a European patent application that claims priority to the instant application.

2. Opt-Out of Authorizations to Permit Access by a Foreign Intellectual Property Office(s)

☐ A. Applicant **DOES NOT** authorize the USPTO to permit a participating foreign IP office access to the instant application-as-filed. If this box is checked, the USPTO will not be providing a participating foreign IP office with any documents and information identified in subsection 1A above.

☐ B. Applicant **DOES NOT** authorize the USPTO to transmit to the EPO any search results from the instant patent application. If this box is checked, the USPTO will not be providing the EPO with search results from the instant application.

NOTE: Once the application has published or is otherwise publicly available, the USPTO may provide access to the application in accordance with 37 CFR 1.14.

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Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Applicant 1

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.

Clear

◉ Assignee	○ Legal Representative under 35 U.S.C. 117	○ Joint Inventor
○ Person to whom the inventor is obligated to assign.	○ Person who shows sufficient proprietary interest	

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor:	
If the Applicant is an Organization check here.	☒
Organization Name	HFT Solutions, LLC

Mailing Address Information For Applicant:

Address 1	65 Locust Avenue		
Address 2			
City	New Canaan	**State/Province**	CT
Country[i]	US	Postal Code	06840
Phone Number		Fax Number	
Email Address			

Additional Applicant Data may be generated within this form by selecting the Add button.

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Assignee Information including Non-Applicant Assignee Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Assignee 1

Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication. An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.

If the Assignee or Non-Applicant Assignee is an Organization check here. ☐

Prefix	**Given Name**	Middle Name	**Family Name**	Suffix

Mailing Address Information For Assignee including Non-Applicant Assignee:

Address 1			
Address 2			
City		**State/Province**	
Country i		Postal Code	
Phone Number		Fax Number	
Email Address			

Additional Assignee or Non-Applicant Assignee Data may be generated within this form by selecting the Add button.

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Signature:

NOTE: This Application Data Sheet must be signed in accordance with 37 CFR 1.33(b). **However, if this Application Data Sheet is submitted with the INITIAL filing of the application and either box A or B is not checked in subsection 2 of the "Authorization or Opt-Out of Authorization to Permit Access" section, then this form must also be signed in accordance with 37 CFR 1.14(c).**

This Application Data Sheet **must** be signed by a patent practitioner if one or more of the applicants is a **juristic entity** (e. g., corporation or association). If the applicant is two or more joint inventors, this form must be signed by a patent practitioner, **all** joint inventors who are the applicant, or one or more joint inventor-applicants who have been given power of attorney (e.g., see USPTO Form PTO/AIA/81) on behalf of **all** joint inventor-applicants.

See 37 CFR 1.4(d) for the manner of making signatures and certifications.

Signature	/Keith J. Barkaus/			Date (YYYY-MM-DD)	
First Name	Keith J.	Last Name	Barkaus	Registration Number	51431

Additional Signature may be generated within this form by selecting the Add button.