

Clock Networks and PLLs in Stratix V Devices

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This chapter describes the advanced features of hierarchical clock networks and phase-locked loops (PLLs) in Stratix® V devices. The Quartus® II software enables the PLLs and their features without external devices.

Related Information

Stratix V Device Handbook: Known Issues

Lists the planned updates to the *Stratix V Device Handbook* chapters.

Clock Networks

The Stratix V devices contain the following clock networks that are organized into a hierarchical structure:

- Global clock (GCLK) networks
- Regional clock (RCLK) networks
- Periphery clock (PCLK) networks

Clock Resources in Stratix V Devices

The clock networks provide up to 450 unique clock domains. Stratix V devices support up to 127 unique GCLK, RCLK, and PCLK clock sources (16 GCLKs + 23 RCLKs + 88 PCLKs) per device quadrant.

Table 4-1: Clock Resources in Stratix V Devices—Preliminary

Clock Resource	Device	Number of Resources Available	Source of Clock Resource
Clock input pins	All	48 single-ended or 24 differential	CLK[0..23][p,n] pins
GCLK networks	All	16	CLK[0..23][p,n] pins, PLL clock outputs, and logic array
RCLK networks	All	92	CLK[0..23][p,n] pins, PLL clock outputs, and logic array

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Clock Resource	Device	Number of Resources Available	Source of Clock Resource
PCLK networks	- Stratix V GS D3 and D4 - Stratix V GX A3 (with 24 transceivers)	210	DPA clock outputs, PLD-transceiver interface clocks, I/O pins, and logic array
	- Stratix V GS D5 - Stratix V GX A3 (with 36 transceivers), A4, B5, and A6	282	
	- Stratix V GS D6 and D8 - Stratix V GT C5 and C7 - Stratix V GX A5 and A7	306	
	- Stratix V E E9 and EB - Stratix V GX A9, AB, B9, and BB	342	
GCLKs and RCLKs per quadrant	All	39	16 GCLKs + 23 RCLKs
GCLKs and RCLKs per device	All	108	16 GCLKs + 92 RCLKs

For more information about the clock input pins connections, refer to the pin connection guidelines.

Related Information

[Stratix V E, GS, and GX Device Family Pin Connection Guidelines](#)

[Stratix V GT Device Family Pin Connection Guidelines](#)

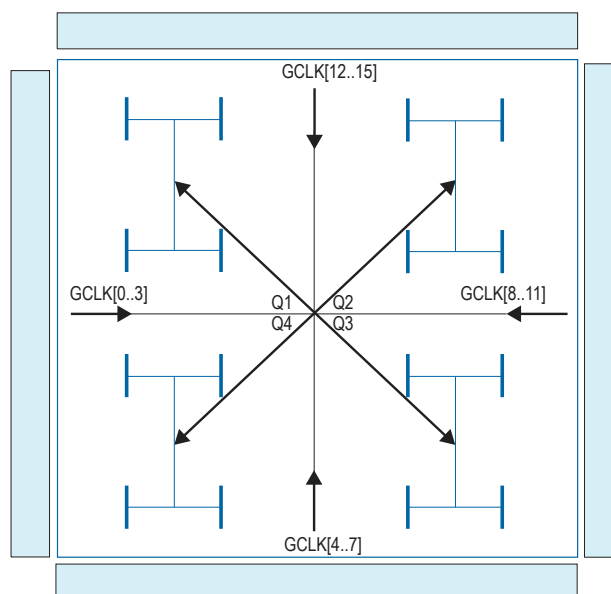
Types of Clock Networks

Global Clock Networks

Stratix V devices provide GCLKs that can drive throughout the device. The GCLKs serve as low-skew clock sources for functional blocks, such as adaptive logic modules (ALMs), digital signal processing (DSP), embedded memory, and PLLs. Stratix V I/O elements (IOEs) and internal logic can also drive GCLKs to create internally-generated global clocks and other high fan-out control signals, such as synchronous or asynchronous clear and clock enable signals.

Figure 4-1: GCLK Networks in Stratix V Devices

This figure represents the top view of the silicon die that corresponds to a reverse view of the device package.

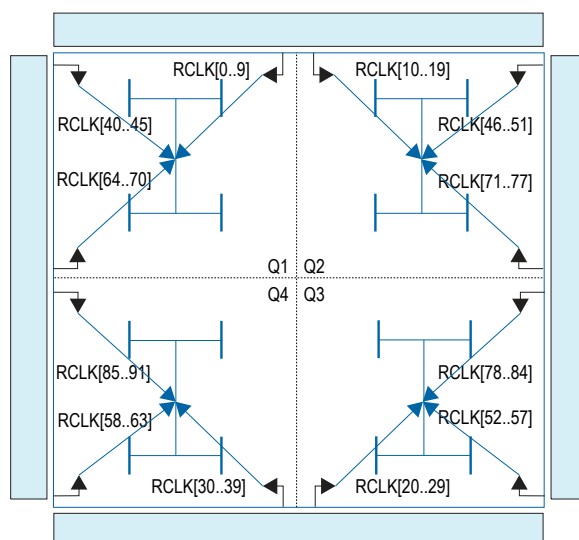


Regional Clock Networks

RCLK networks are only applicable to the quadrant they drive into. RCLK networks provide the lowest clock insertion delay and skew for logic contained within a single device quadrant. The Stratix V IOEs and internal logic within a given quadrant can also drive RCLKs to create internally generated regional clocks and other high fan-out control signals.

Figure 4-2: RCLK Networks in Stratix V Devices

This figure represents the top view of the silicon die that corresponds to a reverse view of the device package.



Periphery Clock Networks

Depending on the routing direction, Stratix V devices provide vertical PCLKs from the top and bottom periphery, and horizontal PCLKs from the left and right periphery.

Clock outputs from the dynamic phase aligner (DPA) block, programmable logic device (PLD)-transceiver interface clocks, I/O pins, and internal logic can drive the PCLK networks.

PCLKs have higher skew when compared with GCLK and RCLK networks. You can use PCLKs for general purpose routing to drive signals into and out of the Stratix V device.

Figure 4-3: PCLK Networks for Stratix V GS D5 Device, and Stratix V GX A3 (with 36 transceivers) and A4 Devices

This figure represents the top view of the silicon die that corresponds to a reverse view of the device package.

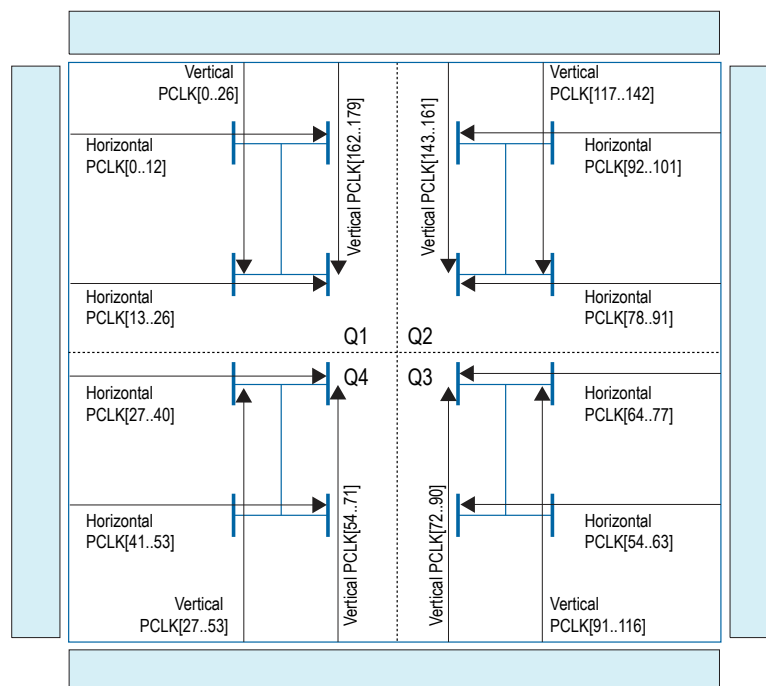


Figure 4-4: PCLK Networks for Stratix V GX B5 and B6 Devices

This figure represents the top view of the silicon die that corresponds to a reverse view of the device package.

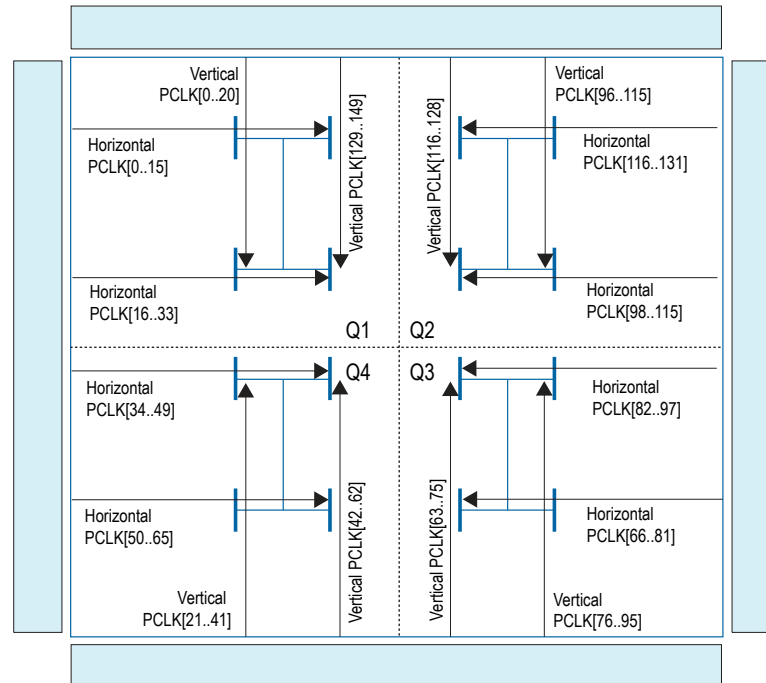


Figure 4-5: PCLK Networks for Stratix V GT C5 and C7 Devices, and Stratix V GX A5 and A7 Devices

This figure represents the top view of the silicon die that corresponds to a reverse view of the device package.

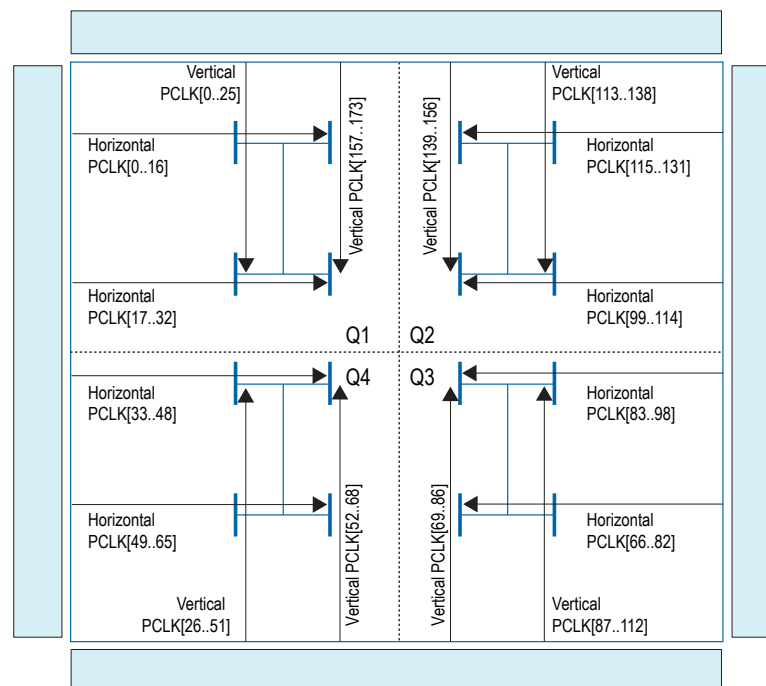


Figure 4-6: PCLK Networks for Stratix V GS D3 and D4 Devices, and Stratix V GX A3 (with 24 transceivers) Device

This figure represents the top view of the silicon die that corresponds to a reverse view of the device package.

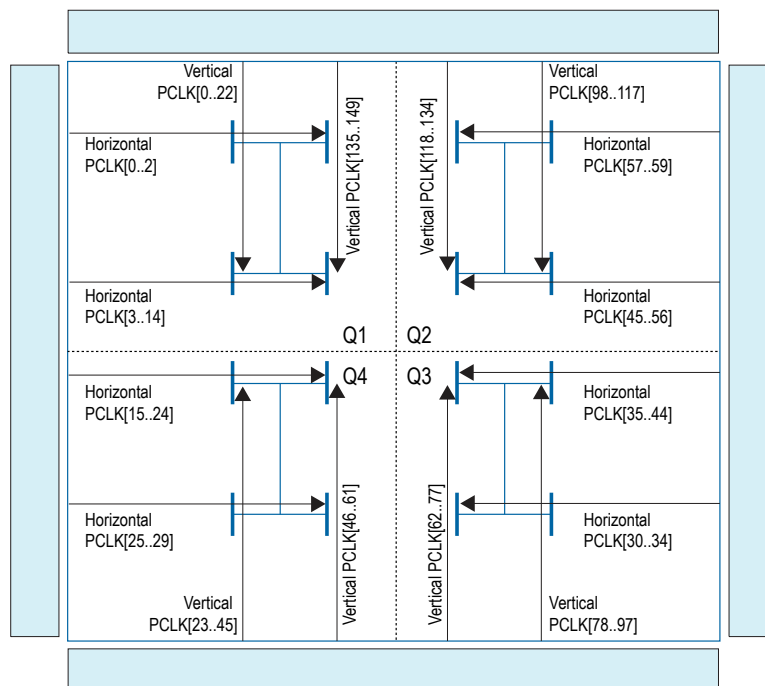


Figure 4-7: PCLK Networks for Stratix V GS D6 and D8 Devices

This figure represents the top view of the silicon die that corresponds to a reverse view of the device package.

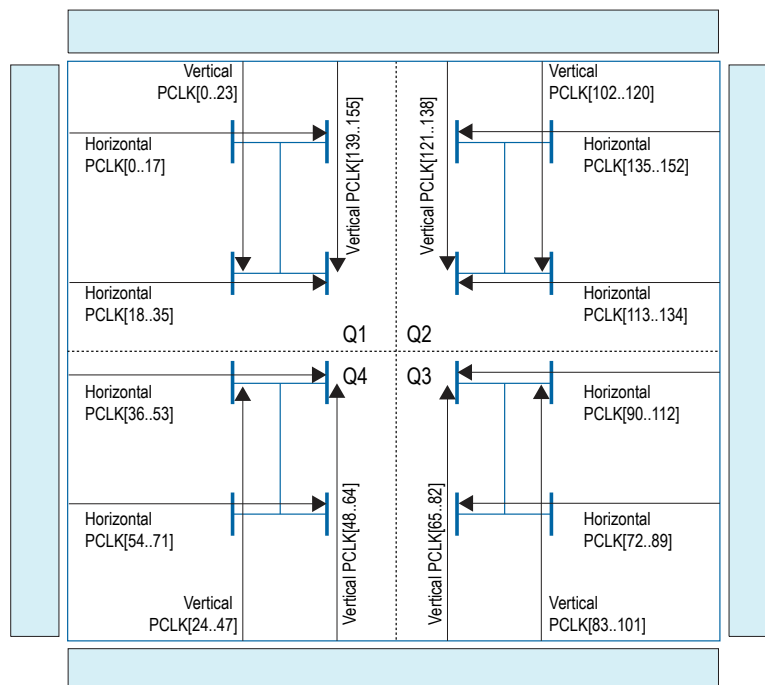
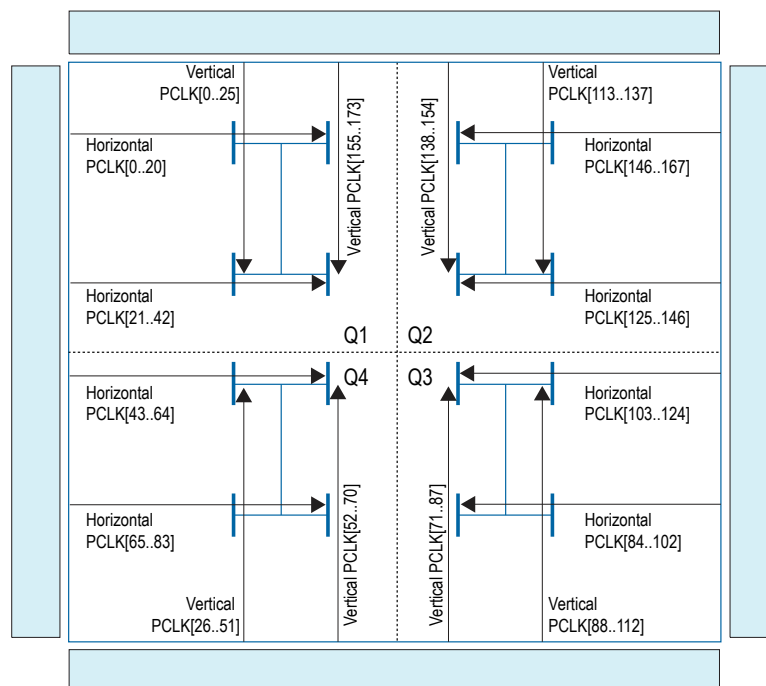


Figure 4-8: PCLK Networks for Stratix V E E9 and EB Devices, and Stratix V GX A9, AB, BB, and B9 Devices

This figure represents the top view of the silicon die that corresponds to a reverse view of the device package.

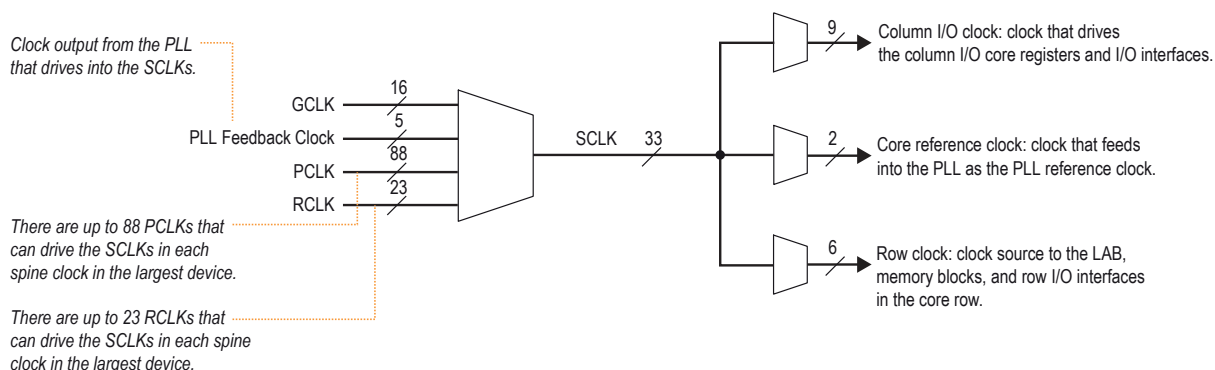


Clock Sources Per Quadrant

The Stratix V devices provide 33 section clock (SCLK) networks in each spine clock per quadrant. The SCLK networks can drive six row clocks in each logic array block (LAB) row, nine column I/O clocks, and two core reference clocks. The SCLKs are the clock resources to the core functional blocks, PLLs, and I/O interfaces of the device.

A spine clock is another layer of routing between the GCLK, RCLK, and PCLK networks before each clock is connected to the clock routing for each LAB row. The settings for spine clocks are transparent. The Quartus II software automatically routes the spine clock based on the GCLK, RCLK, and PCLK networks.

The following figure shows SCLKs driven by the GCLK, RCLK, PCLK, or the PLL feedback clock networks in each spine clock per quadrant. The GCLK, RCLK, PCLK, and PLL feedback clocks share the same routing to the SCLKs. To ensure successful design fitting in the Quartus II software, the total number of clock resources must not exceed the SCLK limits in each region.

Figure 4-9: Hierarchical Clock Networks in Each Spine Clock Per Quadrant

Types of Clock Regions

This section describes the types of clock regions in Stratix V devices.

Entire Device Clock Region

To form the entire device clock region, a source drives a signal in a GCLK network that can be routed through the entire device. The source is not necessarily a clock signal. This clock region has the maximum insertion delay when compared with other clock regions, but allows the signal to reach every destination in the device. It is a good option for routing global reset and clear signals or routing clocks throughout the device.

Regional Clock Region

To form a regional clock region, a source drives a signal in a RCLK network that you can route throughout one quadrant of the device. This clock region provides the lowest skew in a quadrant. It is a good option if all the destinations are in a single quadrant.

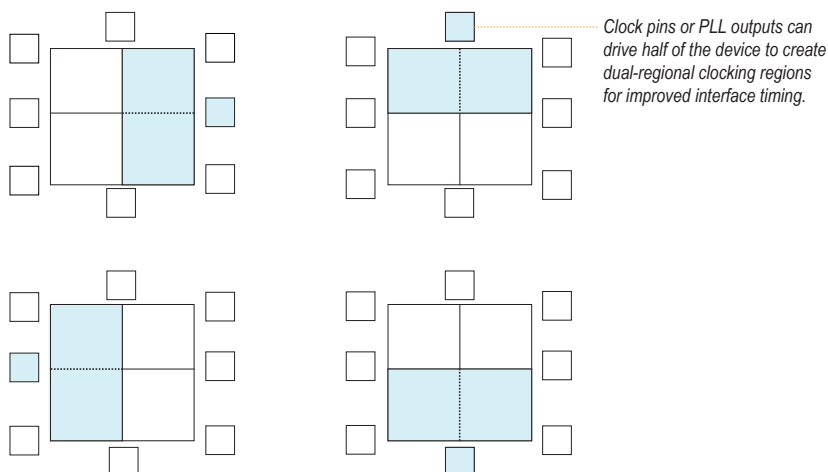
Dual-Regional Clock Region

To form a dual-regional clock region, a single source (a clock pin or PLL output) generates a dual-regional clock by driving two RCLK networks (one from each quadrant). This technique allows destinations across two adjacent device quadrants to use the same low-skew clock. The routing of this signal on an entire side has approximately the same delay as a RCLK region. Internal logic can also drive a dual-regional clock network.

Corner PLL outputs only span one quadrant, they cannot generate a dual-regional clock network.

Figure 4-10: Dual-Regional Clock Region for Stratix V Devices

This figure represents the top view of the silicon die that corresponds to a reverse view of the device package.



Clock Network Sources

In Stratix V devices, clock input pins, PLL outputs, high-speed serial interface (HSSI) outputs, DPA outputs, and internal logic can drive the GCLK, RCLK, and PCLK networks.

Dedicated Clock Input Pins

You can use the dedicated clock input pins ($\text{CLK}[0..23][p, n]$) for high fan-out control signals, such as asynchronous clears, presets, and clock enables, for protocol signals through the GCLK or RCLK networks.

CLK pins can be either differential clocks or single-ended clocks. When you use the CLK pins as single-ended clock inputs, only the $\text{CLK}\langle\#>p$ pins have dedicated connections to the PLL. The $\text{CLK}\langle\#>n$ pins drive the PLLs over global or regional clock networks and do not have dedicated routing paths to the PLLs.

Driving a PLL over a global or regional clock can lead to higher jitter at the PLL input, and the PLL will not be able to fully compensate for the global or regional clock. Altera recommends using the $\text{CLK}\langle\#>p$ pins for optimal performance when you use single-ended clock inputs to drive the PLLs.

Internal Logic

You can drive each GCLK, RCLK, and horizontal PCLK network using LAB-routing and row clock to enable internal logic to drive a high fan-out, low-skew signal.

Note: Internally-generated GCLKs, RCLKs, or PCLKs cannot drive the Stratix V PLLs. The input clock to the PLL has to come from dedicated clock input pins, PLL-fed GCLKs, or PLL-fed RCLKs.

DPA Outputs

Every DPA generates one PCLK to the core.

Related Information

[High-Speed Differential I/O Interfaces and DPA in Stratix V Devices](#)

Provides more information about DPA and HSSI outputs.

HSSI Outputs

Every three HSSI outputs generate a group of six PCLKs to the core.

Related Information

[High-Speed Differential I/O Interfaces and DPA in Stratix V Devices](#)

Provides more information about DPA and HSSI outputs.

PLL Clock Outputs

The Stratix V PLL clock outputs can drive both GCLK and RCLK networks.

Clock Input Pin Connections to GCLK and RCLK Networks

Table 4-2: Dedicated Clock Input Pin Connectivity to the GCLK Networks for Stratix V Devices—Preliminary

Clock Resources	CLK (p/n Pins)
GCLK[0, 1, 2, 3]	CLK[0, 1, 2, 3, 20, 21, 22, 23]
GCLK[4, 5, 6, 7]	CLK[4, 5, 6, 7]
GCLK[8, 9, 10, 11]	CLK[8, 9, 10, 11, 12, 13, 14, 15]
GCLK[12, 13, 14, 15]	CLK[16, 17, 18, 19]

Table 4-3: Dedicated Clock Input Pin Connectivity to the RCLK Networks for Stratix V Devices—Preliminary

A given clock input pin can drive two adjacent RCLK networks to create a dual-regional clock network.

Clock Resources	CLK (p/n Pins)
RCLK[58, 59, 60, 61, 62, 63, 64, 68, 85, 89]	CLK[0]
RCLK[58, 59, 60, 61, 62, 63, 65, 69, 86, 90]	CLK[1]
RCLK[58, 59, 60, 61, 62, 63, 66, 70, 87, 91]	CLK[2]
RCLK[58, 59, 60, 61, 62, 63, 67, 88]	CLK[3]
RCLK[20, 24, 28, 30, 34, 38]	CLK[4]
RCLK[21, 25, 29, 31, 35, 39]	CLK[5]
RCLK[22, 26, 32, 36]	CLK[6]
RCLK[23, 27, 33, 37]	CLK[7]
RCLK[52, 53, 54, 55, 56, 57, 71, 75, 78, 82]	CLK[8]
RCLK[52, 53, 54, 55, 56, 57, 72, 76, 79, 83]	CLK[9]
RCLK[52, 53, 54, 55, 56, 57, 73, 77, 80, 84]	CLK[10]
RCLK[52, 53, 54, 55, 56, 57, 74, 81]	CLK[11]
RCLK[46, 47, 48, 49, 50, 51, 71, 75, 78, 82]	CLK[12]
RCLK[46, 47, 48, 49, 50, 51, 72, 76, 79, 83]	CLK[13]
RCLK[46, 47, 48, 49, 50, 51, 73, 77, 80, 84]	CLK[14]

Clock Resources	CLK (p/n Pins)
RCLK [46, 47, 48, 49, 50, 51, 74, 81]	CLK [15]
RCLK [0, 4, 8, 10, 14, 18]	CLK [16]
RCLK [1, 5, 9, 11, 15, 19]	CLK [17]
RCLK [2, 6, 12, 16]	CLK [18]
RCLK [3, 7, 13, 17]	CLK [19]
RCLK [40, 41, 42, 43, 44, 45, 64, 68, 85, 89]	CLK [20]
RCLK [40, 41, 42, 43, 44, 45, 65, 69, 86, 90]	CLK [21]
RCLK [40, 41, 42, 43, 44, 45, 66, 70, 87, 91]	CLK [22]
RCLK [40, 41, 42, 43, 44, 45, 67, 88]	CLK [23]

Clock Output Connections

For Stratix V PLL connectivity to GCLK and RCLK networks, refer to the PLL connectivity to GCLK and RCLK networks spreadsheet.

Related Information

[PLL Connectivity to GCLK and RCLK Networks for Stratix V Devices](#)

Clock Control Block

Every GCLK, RCLK, and PCLK network has its own clock control block. The control block provides the following features:

- Clock source selection (dynamic selection available only for GCLKs)
- Global clock multiplexing
- Clock power down (static or dynamic clock enable or disable available only for GCLKs and RCLKs)

Pin Mapping in Stratix V Devices

Table 4-4: Mapping Between the Input Clock Pins, PLL Counter Outputs, and Clock Control Block Inputs

Clock	Fed by
inclk[0] and inclk[1]	Any of the four dedicated clock pins on the same side of the Stratix V device.
inclk[2]	PLL counters C0 and C2 from the two center PLLs on the same side of the Stratix V devices.
inclk[3]	PLL counters C1 and C3 from the two center PLLs on the same side of the Stratix V devices.

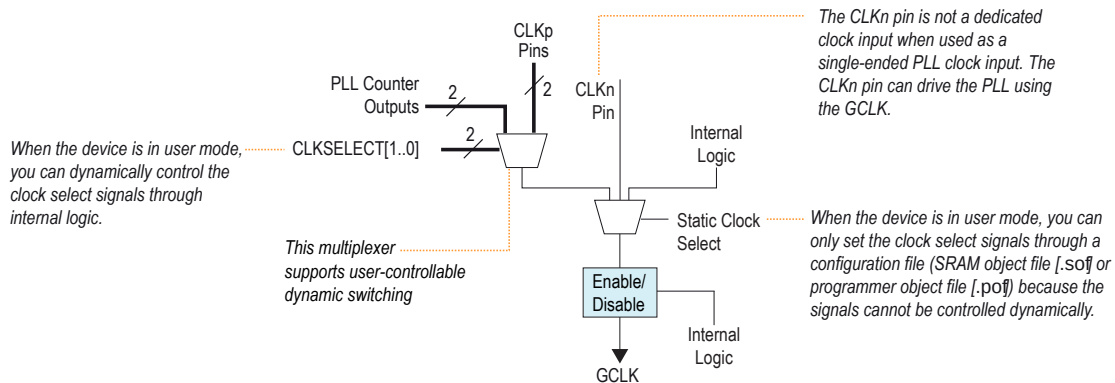
Note: You cannot use corner PLLs for dynamic clock control selection.

GCLK Control Block

You can select the clock source for the GCLK select block either statically or dynamically using internal logic to drive the multiplexer-select inputs.

When selecting the clock source dynamically, you can select either PLL outputs (such as C0 or C1), or a combination of clock pins or PLL outputs.

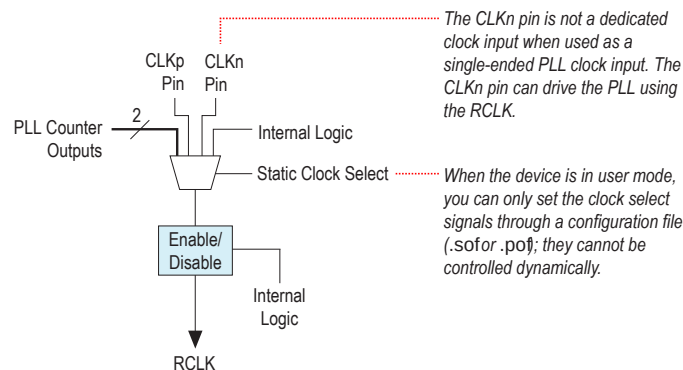
Figure 4-11: GCLK Control Block for Stratix V Devices



RCLK Control Block

You can only control the clock source selection for the RCLK select block statically using configuration bit settings in the configuration file (.sof or .pof) generated by the Quartus II software.

Figure 4-12: RCLK Control Block for Stratix V Devices



You can set the input clock sources and the `clk_ena` signals for the GCLK and RCLK network multiplexers through the Quartus II software using the ALTCLKCTRL megafunction.

Note: When selecting the clock source dynamically using the ALTCLKCTRL megafunction, choose the inputs using the `CLKSELECT[0..1]` signal. The inputs from the clock pins feed the `inclk[0..1]` ports of the multiplexer, and the PLL outputs feed the `inclk[2..3]` ports.

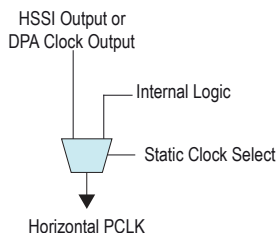
Related Information**[Clock Control Block \(ALTCLKCTRL\) Megafunction User Guide](#)**

Provides more information about ALTCLKCTRL megafunction.

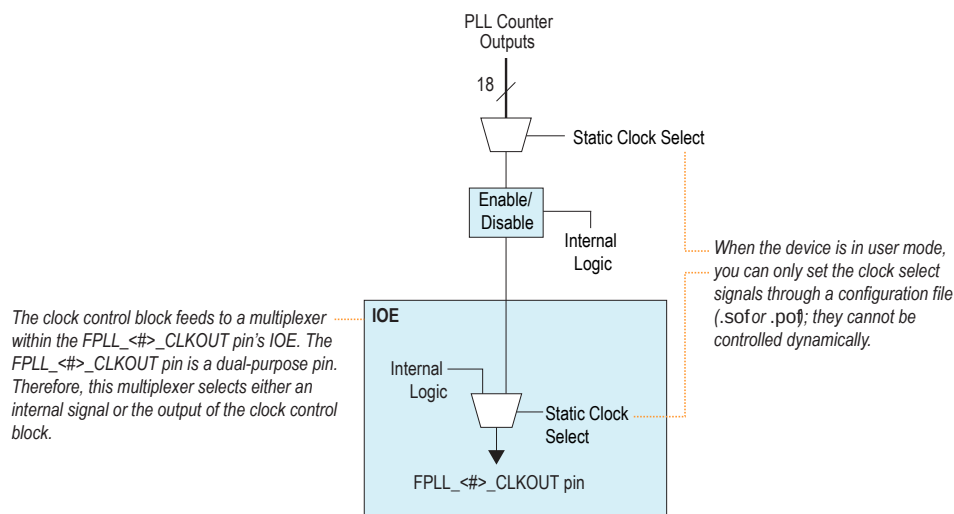
PCLK Control Block

To drive the HSSI horizontal PCLK control block, select the HSSI output or internal logic .

To drive the DPA horizontal PCLK, select the DPA clock output or internal logic. You can only use the DPA clock output to generate the vertical PCLK to the core.

Figure 4-13: Horizontal PCLK Control Block for Stratix V Devices**External PLL Clock Output Control Block**

You can enable or disable the dedicated external clock output pins using the ALTCLKCTRL megafunction.

Figure 4-14: External PLL Output Clock Control Block for Stratix V Devices**Related Information****[Clock Control Block \(ALTCLKCTRL\) Megafunction User Guide](#)**

Provides more information about ALTCLKCTRL megafunction.

Clock Power Down

You can power down the GCLK and RCLK clock networks using both static and dynamic approaches.

When a clock network is powered down, all the logic fed by the clock network is in off-state, reducing the overall power consumption of the device. The unused GCLK, RCLK, and PCLK networks are automatically powered down through configuration bit settings in the configuration file (.sof or .pof) generated by the Quartus II software.

The dynamic clock enable or disable feature allows the internal logic to control power-up or power-down synchronously on the GCLK and RCLK networks, including dual-regional clock regions. This feature is independent of the PLL and is applied directly on the clock network.

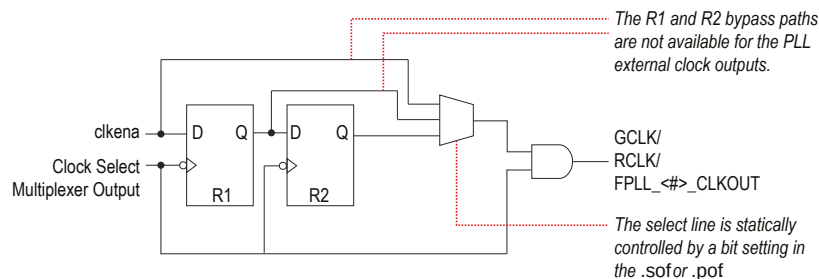
Note: You cannot dynamically enable or disable GCLK or RCLK networks that drive PLLs.

Clock Enable Signals

You cannot use the clock enable and disable circuit of the clock control block if the GCLK or RCLK output drives the input of a PLL.

Figure 4-15: `clkena` Implementation with Clock Enable and Disable Circuit

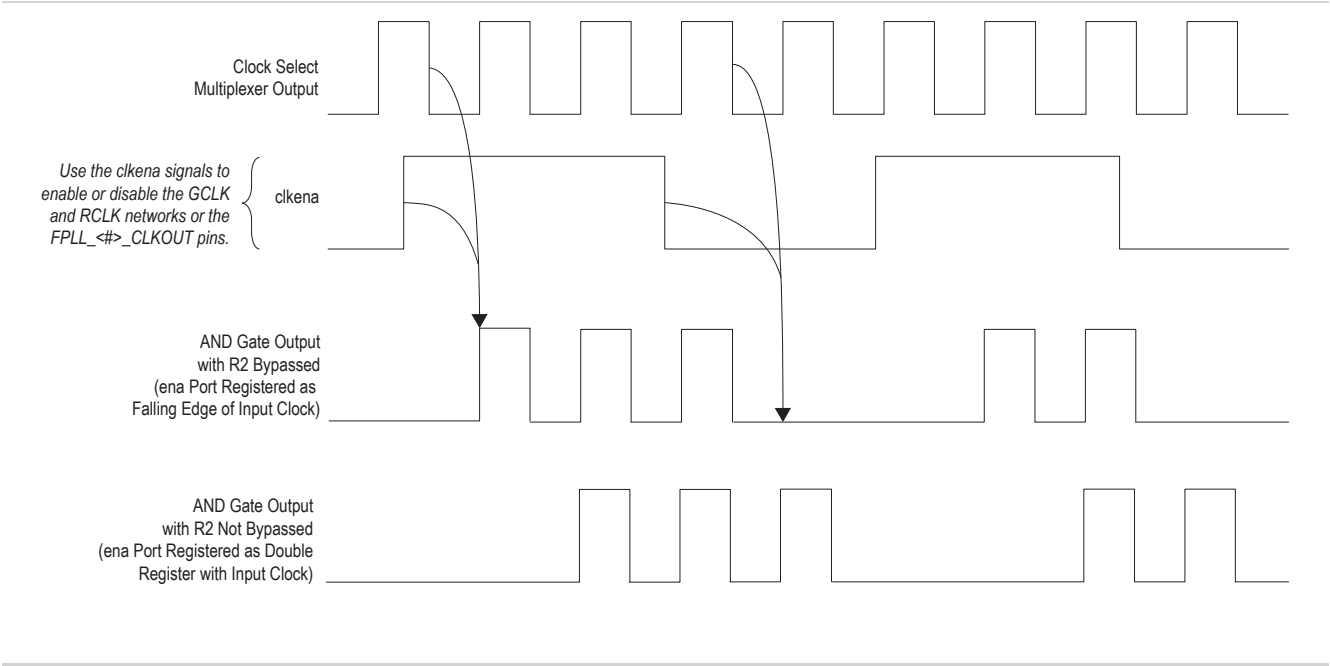
This figure shows the implementation of the clock enable and disable circuit of the clock control block.



The `clkena` signals are supported at the clock network level instead of at the PLL output counter level. This allows you to gate off the clock even when you are not using a PLL. You can also use the `clkena` signals to control the dedicated external clocks from the PLLs.

Figure 4-16: Example of clkena Signals

This figure shows a waveform example for a clock output enable. The `clkena` signal is synchronous to the falling edge of the clock output.



Stratix V devices have an additional metastability register that aids in asynchronous enable and disable of the GCLK and RCLK networks. You can optionally bypass this register in the Quartus II software.

The PLL can remain locked, independent of the `clkena` signals, because the loop-related counters are not affected. This feature is useful for applications that require a low-power or sleep mode. The `clkena` signal can also disable clock outputs if the system is not tolerant of frequency overshoot during resynchronization.

Stratix V PLLs

PLLs provide robust clock management and synthesis for device clock management, external system clock management, and high-speed I/O interfaces.

The Stratix V device family contains fractional PLLs that can function as fractional PLLs or integer PLLs. The output counters in Stratix V devices are dedicated to each fractional PLL that support integer or fractional frequency synthesis.

Two adjacent PLLs share 18 C output counters. Any number of C counters can be assigned to each PLL, as long as the total number used by the two PLLs is 18 or less.

The Stratix V devices offer up to 32 fractional PLLs in the larger densities. All Stratix V fractional PLLs have the same core analog structure and features support.

Table 4-5: PLL Features in Stratix V Devices —Preliminary

Feature	Support
Integer PLL	Yes

Feature	Support
Fractional PLL	Yes
C output counters	18
M, N, C counter sizes	1 to 512
Dedicated external clock outputs	4 single-ended or 2 single-ended and 1 differential
Dedicated clock input pins	4 single-ended or 4 differential
External feedback input pin	Single-ended or differential
Spread-spectrum input clock tracking	Yes ¹
Source synchronous compensation	Yes
Direct compensation	Yes
Normal compensation	Yes
Zero-delay buffer compensation	Yes
External feedback compensation	Yes
LVDS compensation	Yes
Voltage-controlled oscillator (VCO) output drives the DPA clock	Yes
Phase shift resolution	78.125 ps ²
Programmable duty cycle	Yes
Power down mode	Yes

PLL Physical Counters in Stratix V Devices

The physical counters for the fractional PLLs are arranged in the following sequences:

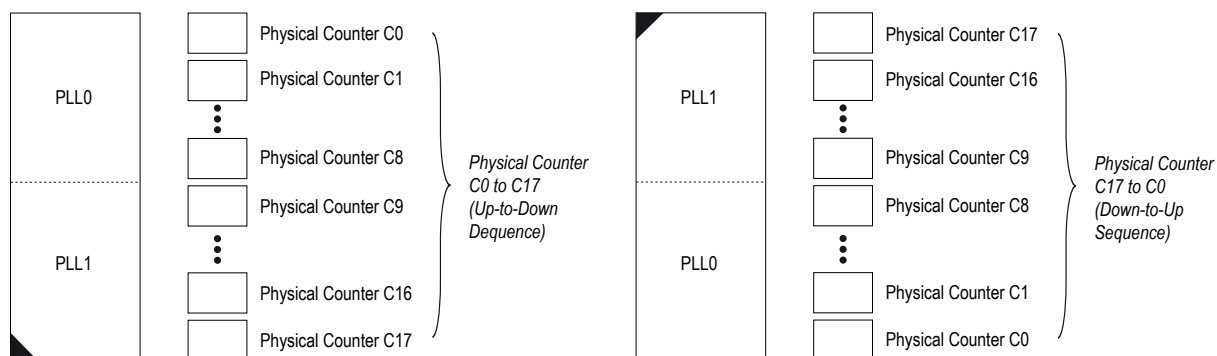
- Up-to-down
- Down-to-up

¹ Provided input clock jitter is within input jitter tolerance specifications.

² The smallest phase shift is determined by the VCO period divided by eight. For degree increments, the Stratix V device can shift all output frequencies in increments of at least 45°. Smaller degree increments are possible depending on the frequency and divide parameters.

Figure 4-17: PLL Physical Counters Orientation for Stratix V Devices

This figure represents the top view of the silicon die that corresponds to a reverse view of the device package.



PLL Locations in Stratix V Devices

The following figures show the physical locations of the fractional PLLs. Every index represents one fractional PLL in the device. The physical locations of the fractional PLLs correspond to the coordinates in the Quartus II Chip Planner.

Figure 4-18: PLL Locations for Stratix V GS D5 Device, and Stratix V GX A3 (with 36 transceivers) and A4 Devices

This figure represents the top view of the silicon die that corresponds to a reverse view of the device package.

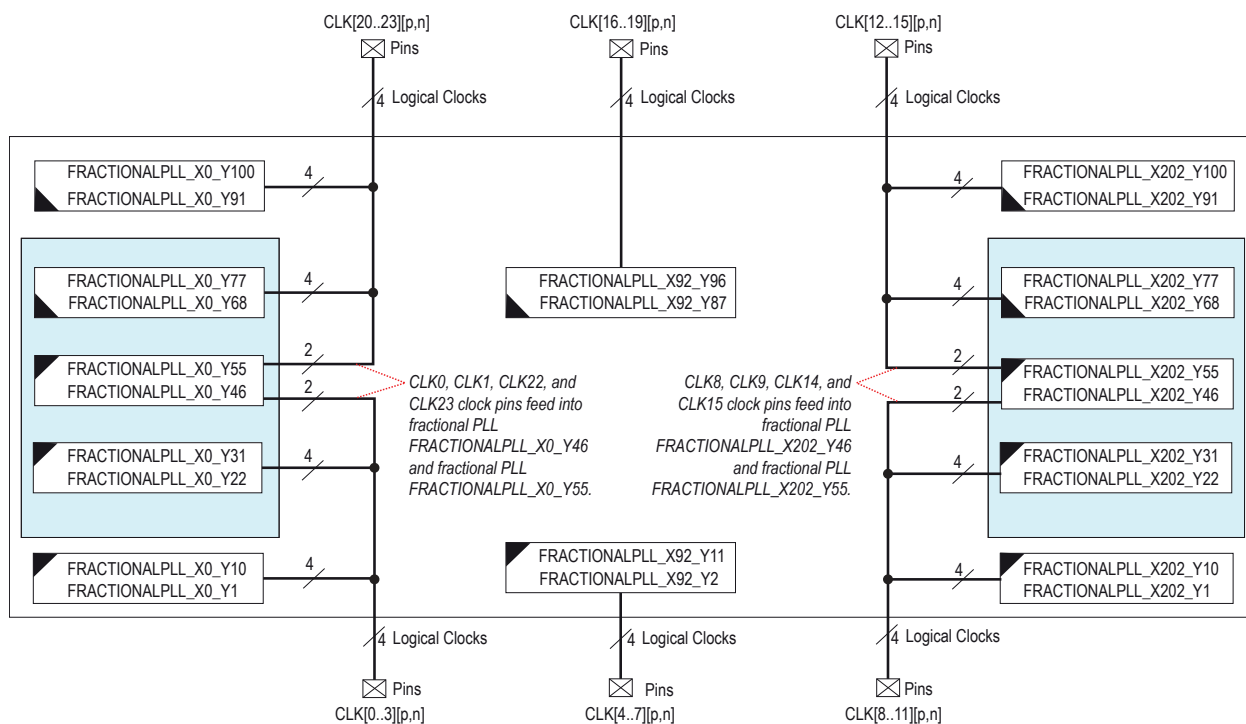


Figure 4-19: PLL Locations for Stratix V GX B5 and B6 Devices

This figure represents the top view of the silicon die that corresponds to a reverse view of the device package.

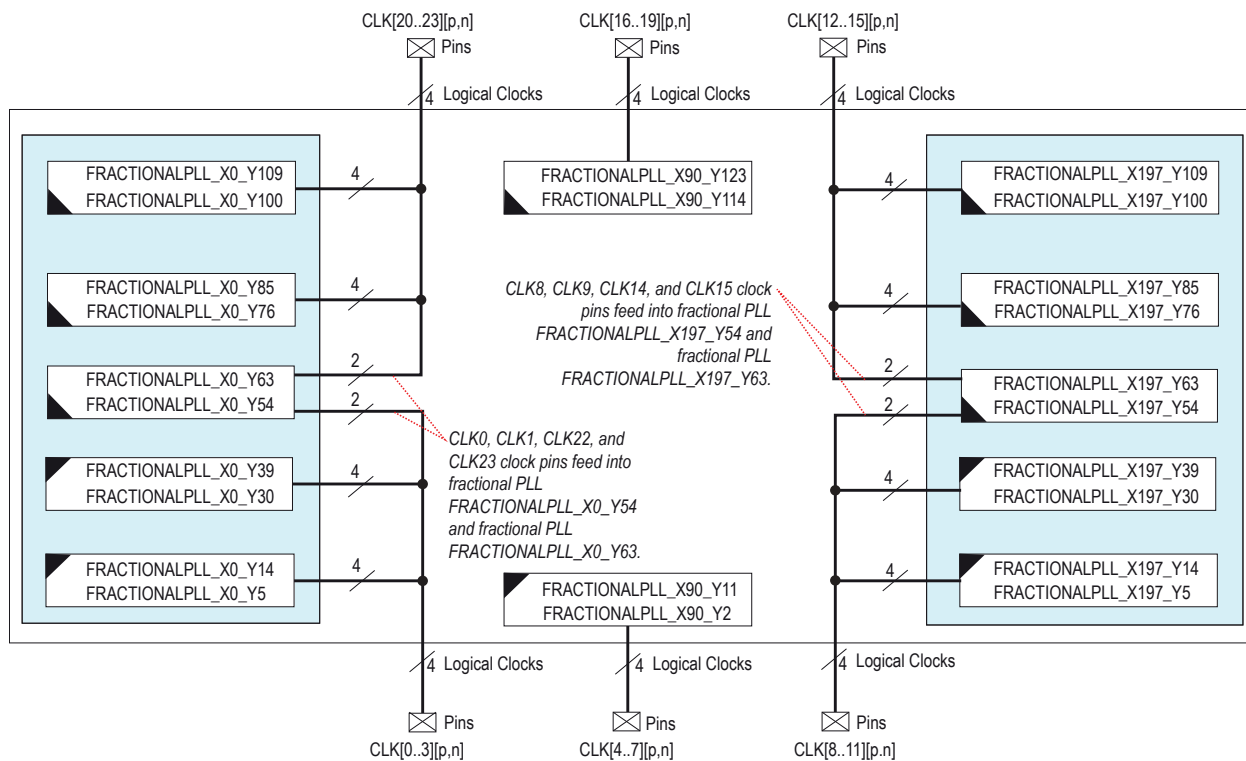


Figure 4-20: PLL Locations for Stratix V GT C5 and C7 Devices, and Stratix V GX A5 and A7 Devices

This figure represents the top view of the silicon die that corresponds to a reverse view of the device package.

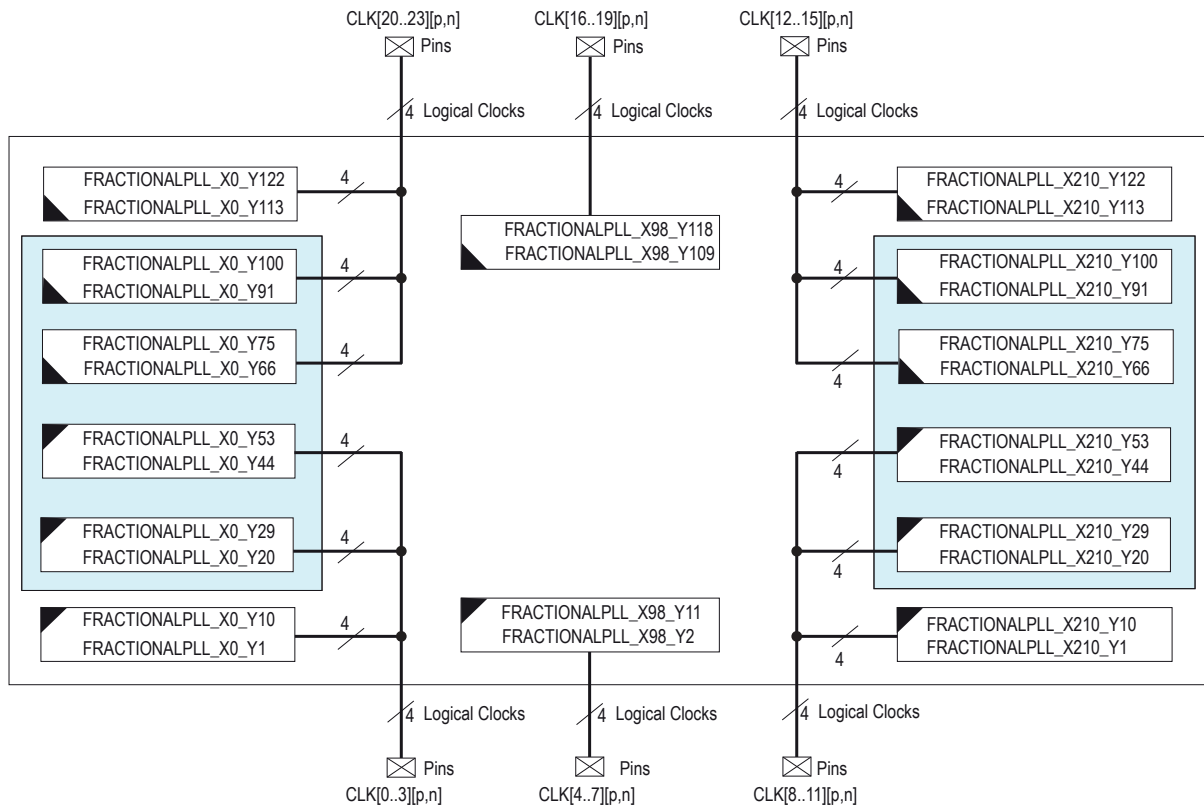


Figure 4-21: PLL Locations for Stratix V GS D3 and D4 Devices, and Stratix V GX A3 (with 24 transceivers) Device

This figure represents the top view of the silicon die that corresponds to a reverse view of the device package.

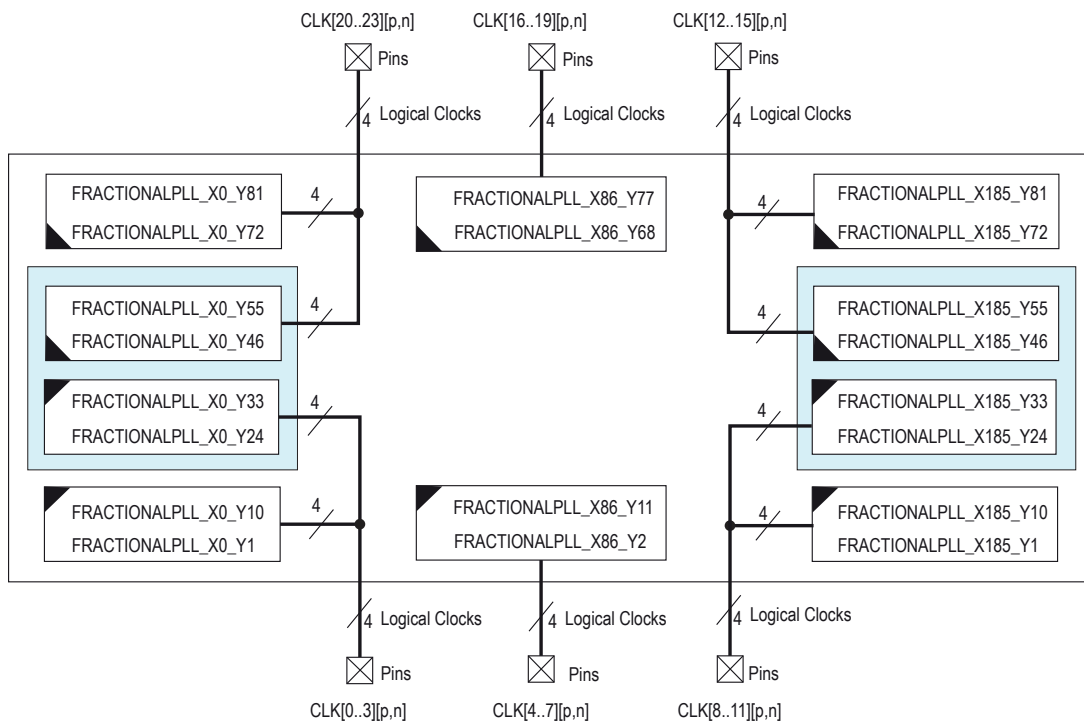


Figure 4-22: PLL Locations for Stratix V GS D6 and D8 Devices

This figure represents the top view of the silicon die that corresponds to a reverse view of the device package.

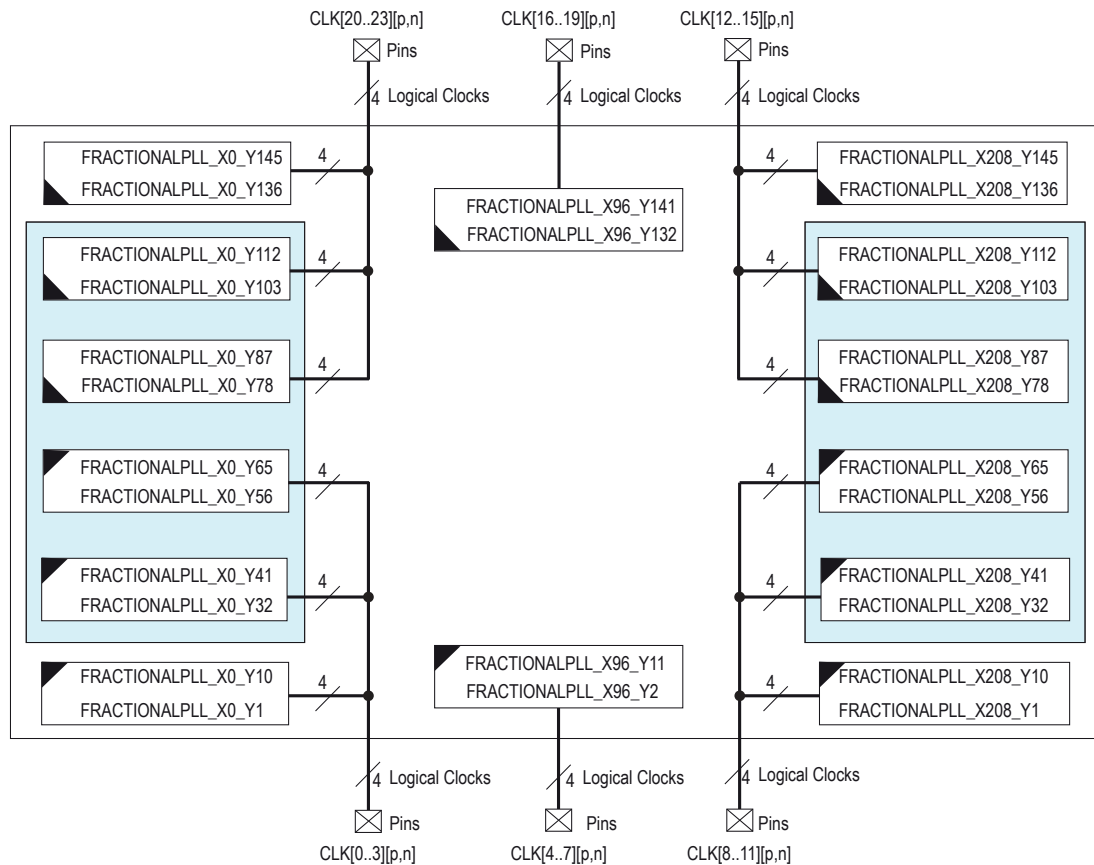
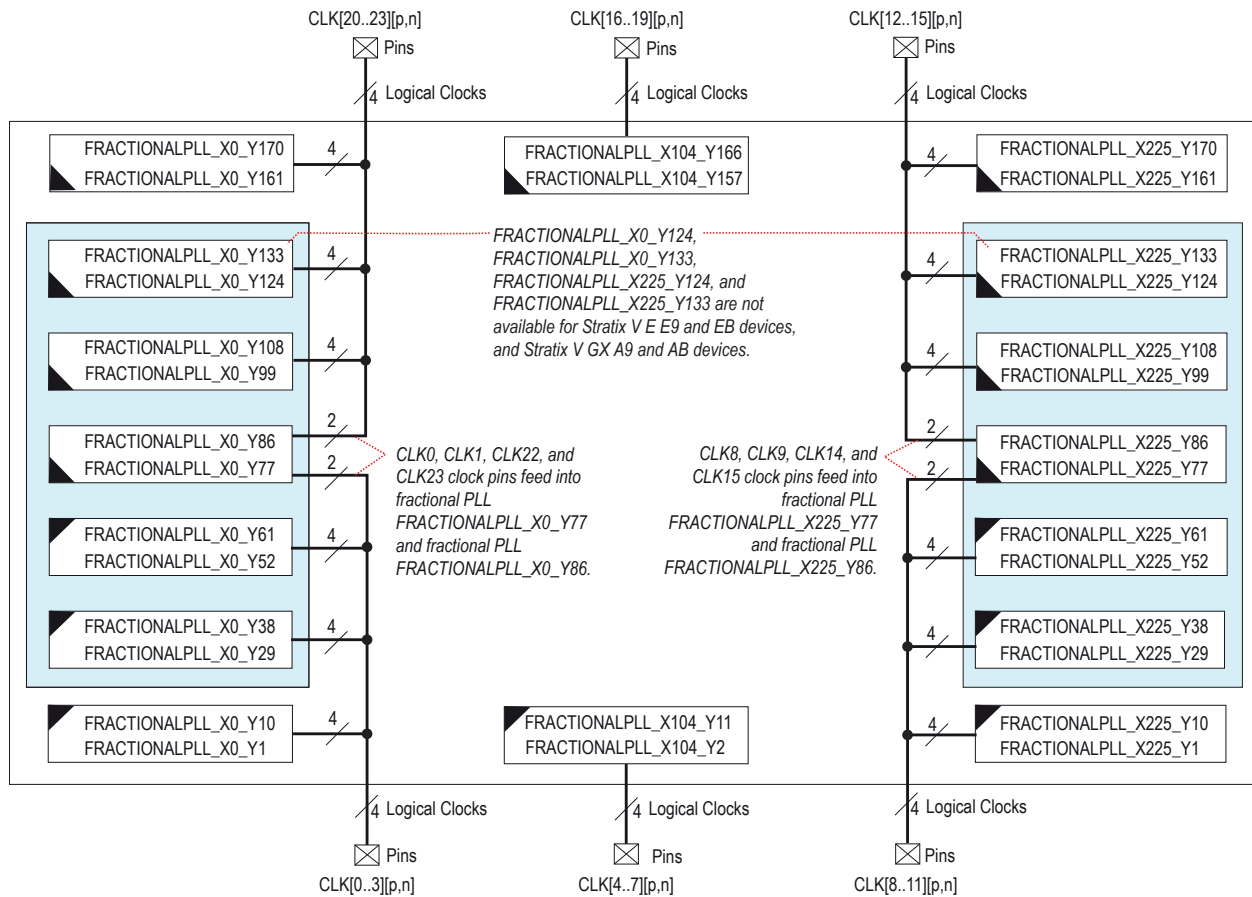


Figure 4-23: PLL Locations for Stratix V E E9 and EB Devices, and Stratix V GX A9, AB, B9, and BB Devices

This figure represents the top view of the silicon die that corresponds to a reverse view of the device package.



Related Information

[PLL Migration Guidelines](#) on page 4-22

PLL migration between Stratix V GX A5, A7, A9, AB, B9, BB, D6, and D8 devices.

PLL Migration Guidelines

If you plan to migrate your design between Stratix V GX A5, A7, A9, AB, B9, BB, D6, and D8 devices with 48 transceiver channels, and your design requires a PLL to drive the HSSI and clock network (GCLK or RCLK) simultaneously, use the 2 middle PLLs on the left or right side of the device.

Table 4-6: Location of Middle PLLs

Variant	Member Code	Middle PLL Location	
		Left Side	Right Side
Stratix V GX	A5	FRACTIONALPLL_X0_Y53, FRACTIONALPLL_X0_Y66	FRACTIONALPLL_X210_Y53, FRACTIONALPLL_X210_Y66
	A7		
	A9		
	AB	FRACTIONALPLL_X0_Y77, FRACTIONALPLL_X0_Y86	FRACTIONALPLL_X225_Y77, FRACTIONALPLL_X225_Y86
	B9		
	BB		
	D6	FRACTIONALPLL_X0_Y65, FRACTIONALPLL_X0_Y78	FRACTIONALPLL_X208_Y65, FRACTIONALPLL_X208_Y78
	D8		

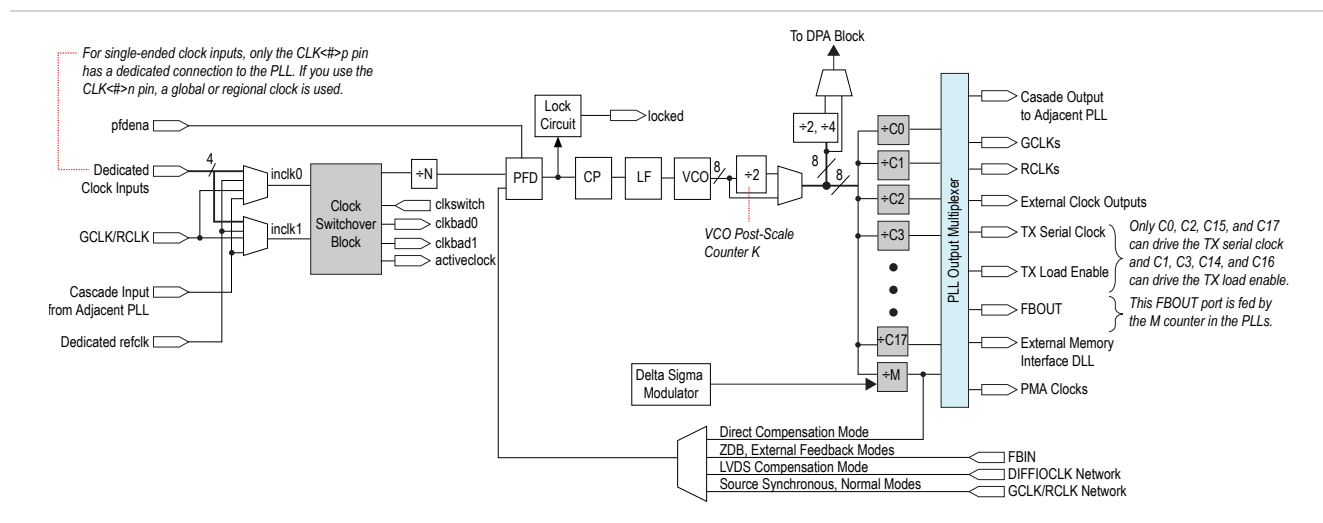
Related Information

PLL Locations in Stratix V Devices on page 4-17

CLKIN pin connectivity to the middle PLLs.

Fractional PLL Architecture

Figure 4-24: Fractional PLL High-Level Block Diagram for Stratix V Devices

**Fractional PLL Usage**

You can configure the fractional PLL to function either in the integer or in the enhanced fractional mode. One fractional PLL can use up to 18 output counters and all external clock outputs. Two adjacent fractional PLLs share the 18 output counters.

Fractional PLLs can be used as follows:

- Reduce the number of required oscillators on the board
- Reduce the clock pins used in the FPGA by synthesizing multiple clock frequencies from a single reference clock source
- Compensate clock network delay
- Zero delay buffering
- Transmit clocking for transceivers

PLL External Clock I/O Pins

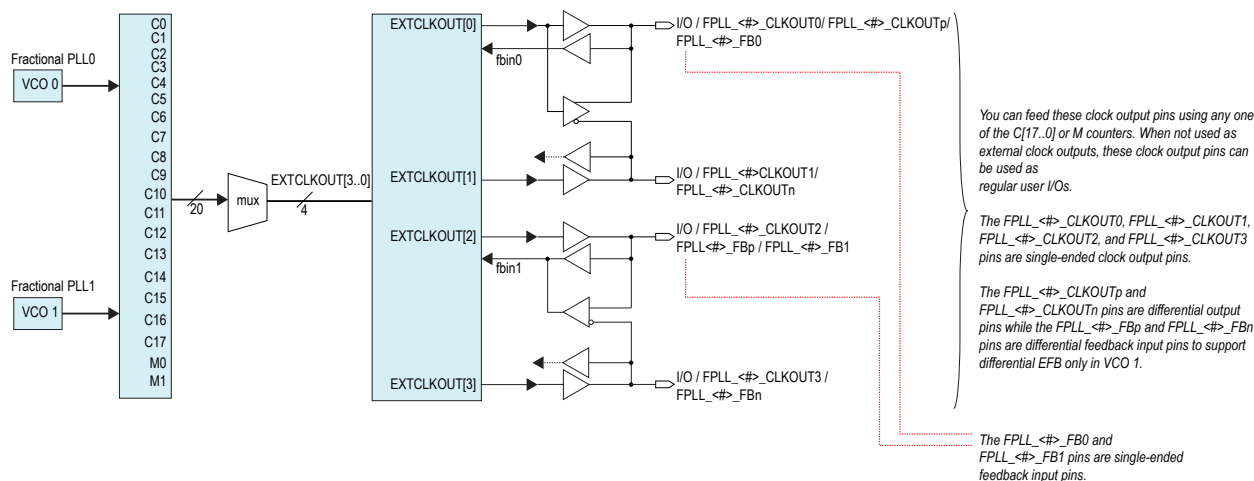
Two adjacent corner and center fractional PLLs share four dual-purpose clock I/O pins, organized as one of the following combinations:

- Four single-ended clock outputs
- Two single-ended outputs and one differential clock output
- Four single-ended clock outputs and two single-ended feedback inputs in the I/O driver feedback for zero delay buffer (ZDB) mode support
- Two single-ended clock outputs and two single-ended feedback inputs for single-ended external feedback (EFB) mode support
- One differential clock output and one differential feedback input for differential EFB support (only one of the two adjacent fractional PLLs can support differential EFB at one time while the other fractional PLL can be used for general-purpose clocking)

Note: All left and right fractional PLLs in Stratix V devices do not support external clock outputs.

The following figure shows that any of the output counters ($C[0..17]$) or the M counter on the PLLs can feed the dedicated external clock outputs. Therefore, one counter or frequency can drive all output pins available from a given PLL.

Figure 4-25: Dual-Purpose Clock I/O Pins Associated with PLL for Stratix V Devices



Each pin of a single-ended output pair can be either in-phase or 180° out-of-phase. To implement the 180° out-of-phase pin in a pin pair, the Quartus II software places a NOT gate in the design into the IOE.

The clock output pin pairs support the following I/O standards:

- Same I/O standard for the pin pairs
- LVDS
- Differential high-speed transceiver logic (HSTL)
- Differential SSTL

Stratix V PLLs can drive out to any regular I/O pin through the GCLK or RCLK network. You can also use the external clock output pins as user I/O pins if you do not require external PLL clocking.

Related Information

[I/O Features in Stratix V Devices](#)

Provides more information about I/O standards supported by the PLL clock input and output pins.

[Zero-Delay Buffer Mode](#) on page 4-28

[External Feedback Mode](#) on page 4-30

PLL Control Signals

You can use the `areset` signal to control PLL operation and resynchronization, and use the `locked` signal to observe the status of the PLL.

areset

The `areset` signal is the reset or resynchronization input for each PLL. The device input pins or internal logic can drive these input signals.

When `areset` is driven high, the PLL counters reset, clearing the PLL output and placing the PLL out-of-lock. The VCO is then set back to its nominal setting. When `areset` is driven low again, the PLL resynchronizes to its input as it re-locks.

You must assert the `areset` signal every time the PLL loses lock to guarantee the correct phase relationship between the PLL input and output clocks. You can set up the PLL to automatically reset (self-reset) after a loss-of-lock condition using the Quartus II MegaWizard™ Plug-In Manager.

You must include the `areset` signal if either of the following conditions is true:

- PLL reconfiguration or clock switchover is enabled in the design
- Phase relationships between the PLL input and output clocks must be maintained after a loss-of-lock condition

Note: If the input clock to the PLL is not toggling or is unstable after power up, assert the `areset` signal after the input clock is stable and within specifications.

locked

The `locked` signal output of the PLL indicates the following conditions:

- The PLL has locked onto the reference clock.
- The PLL clock outputs are operating at the desired phase and frequency set in the MegaWizard Plug-In Manager.

The lock detection circuit provides a signal to the core logic. The signal indicates when the feedback clock has locked onto the reference clock both in phase and frequency.

Clock Feedback Modes

This section describes the following clock feedback modes:

- Source synchronous
- LVDS compensation
- Direct compensation
- Normal
- ZDB
- EFB

Each mode allows clock multiplication and division, phase shifting, and programmable duty cycle.

The input and output delays are fully compensated by a PLL only when using the dedicated clock input pins associated with a given PLL as the clock source.

The input and output delays may not be fully compensated in the Quartus II software for the following conditions:

- When a GCLK or RCLK network drives the PLL
- When the PLL is driven by a dedicated clock pin that is not associated with the PLL

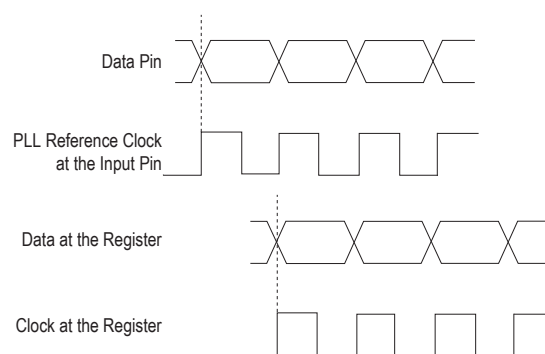
For example, when you configure a PLL in ZDB mode, the PLL input is driven by an associated dedicated clock input pin. In this configuration, a fully compensated clock path results in zero delay between the clock input and one of the clock outputs from the PLL. However, if the PLL input is fed by a non-dedicated input (using the GCLK network), the output clock may not be perfectly aligned with the input clock.

Source Synchronous Mode

If the data and clock arrive at the same time on the input pins, the same phase relationship is maintained at the clock and data ports of any IOE input register. Data and clock signals at the IOE experience similar buffer delays as long as you use the same I/O standard.

Altera recommends source synchronous mode for source synchronous data transfers.

Figure 4-26: Example of Phase Relationship Between Clock and Data in Source Synchronous Mode



The source synchronous mode compensates for the delay of the clock network used and any difference in the delay between the following two paths:

- Data pin to the IOE register input
- Clock input pin to the PLL phase frequency detector (PFD) input

The Stratix V PLL can compensate multiple pad-to-input-register paths, such as a data bus when it is set to use source synchronous compensation mode.

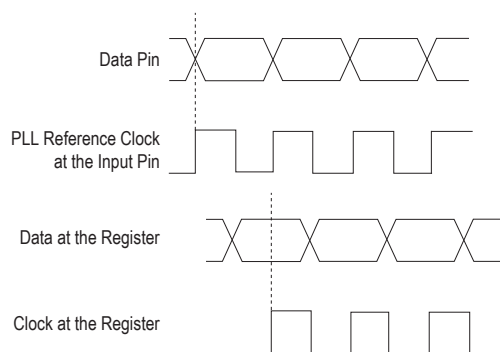
Source Synchronous Mode for LVDS Compensation

The purpose of source synchronous mode is to maintain the same data and clock timing relationship seen at the pins of the internal serializer/deserializer (SERDES) capture register, except that the clock is inverted (180° phase shift). Thus, source synchronous mode ideally compensates for the delay of the LVDS clock network, including the difference in delay between the following two paths:

- Data pin-to-SERDES capture register
- Clock input pin-to-SERDES capture register

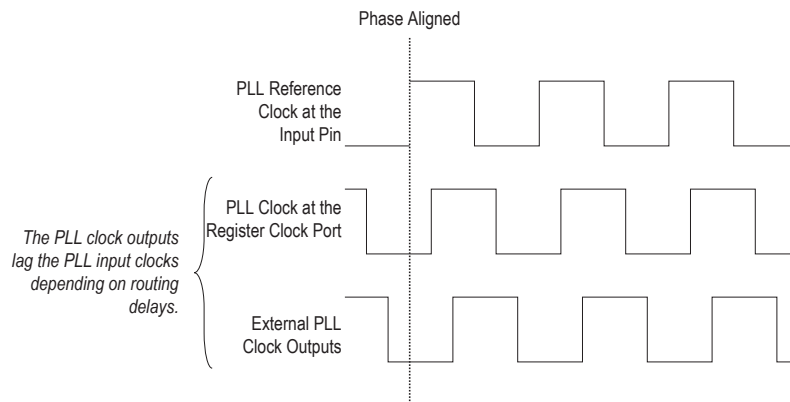
The output counter must provide the 180° phase shift.

Figure 4-27: Example of Phase Relationship Between the Clock and Data in LVDS Compensation Mode



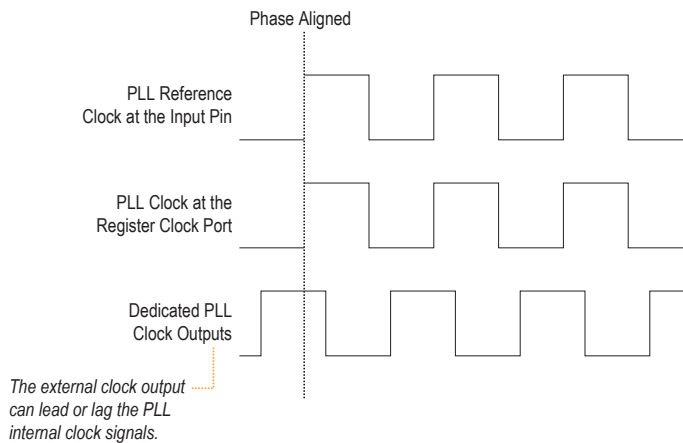
Direct Compensation Mode

In direct compensation mode, the PLL does not compensate for any clock networks. This mode provides better jitter performance because the clock feedback into the PFD passes through less circuitry. Both the PLL internal- and external-clock outputs are phase-shifted with respect to the PLL clock input.

Figure 4-28: Example of Phase Relationship Between the PLL Clocks in Direct Compensation Mode

Normal Mode

An internal clock in normal mode is phase-aligned to the input clock pin. The external clock output pin has a phase delay relative to the clock input pin if connected in this mode. The Quartus II TimeQuest Timing Analyzer reports any phase difference between the two. In normal mode, the delay introduced by the GCLK or RCLK network is fully compensated.

Figure 4-29: Example of Phase Relationship Between the PLL Clocks in Normal Mode

Zero-Delay Buffer Mode

In ZDB mode, the external clock output pin is phase-aligned with the clock input pin for zero delay through the device. This mode is supported only on the center and corner PLLs in Stratix V devices.

When using this mode, you must use the same I/O standard on the input clocks and clock outputs to guarantee clock alignment at the input and output pins. You cannot use differential I/O standards on the PLL clock input or output pins.

To ensure phase alignment between the `clk` pin and the external clock output (`CLKOUT`) pin in ZDB mode, instantiate a bidirectional I/O pin in the design. The bidirectional I/O pin serves as the feedback path connecting the `fbout` and `fbin` ports of the PLL. The bidirectional I/O pin must always be assigned a

single-ended I/O standard. The PLL uses this bidirectional I/O pin to mimic and compensate for the output delay from the clock output port of the PLL to the external clock output pin.

Note: To avoid signal reflection when using ZDB mode, do not place board traces on the bidirectional I/O pin.

Figure 4-30: ZDB Mode in Stratix V PLLs

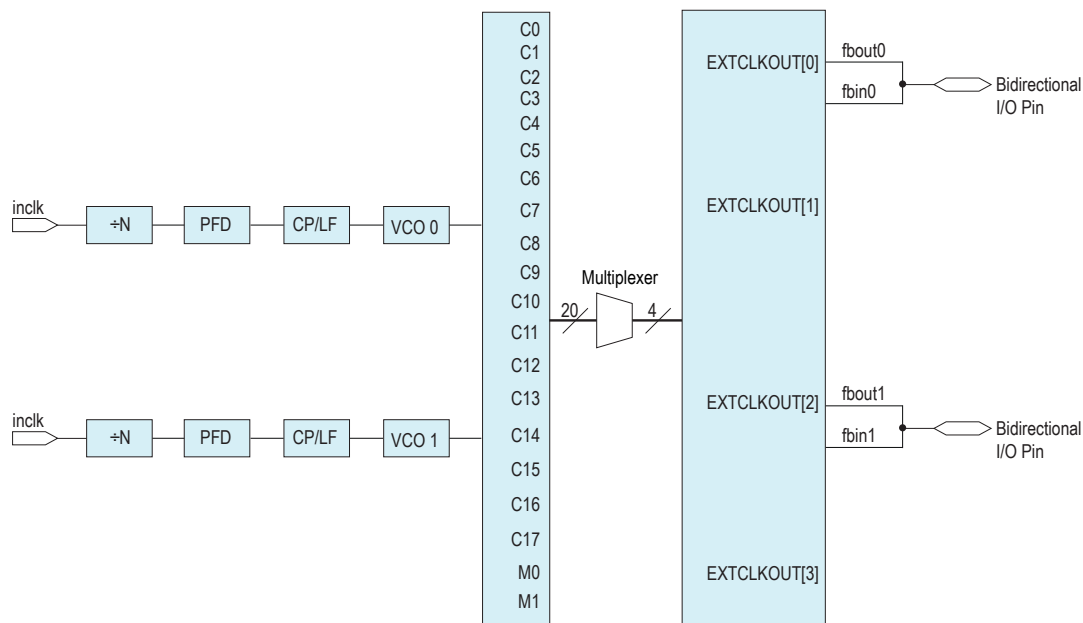
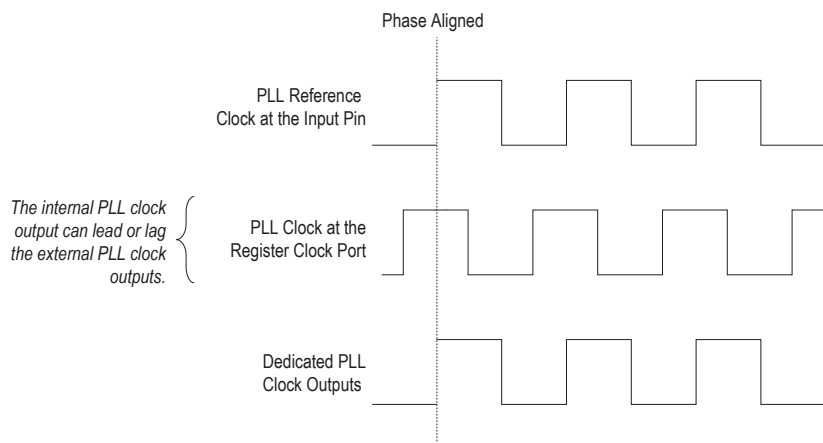


Figure 4-31: Example of Phase Relationship Between the PLL Clocks in ZDB Mode



Related Information

[PLL External Clock I/O Pins](#) on page 4-24

Provides more information about PLL clock outputs.

External Feedback Mode

In EFB mode, the output of the M counter ($fbout$) feeds back to the PLL $fbin$ input (using a trace on the board) and becomes part of the feedback loop.

One of the dual-purpose external clock outputs becomes the $fbin$ input pin in this mode. The external feedback input pin, $fbin$ is phase-aligned with the clock input pin. Aligning these clocks allows you to remove clock delay and skew between devices.

When using EFB mode, you must use the same I/O standard on the input clock, feedback input, and clock outputs.

This mode is supported only on the center and corner fractional PLLs in Stratix V devices.

Figure 4-32: EFB Mode in Stratix V Devices

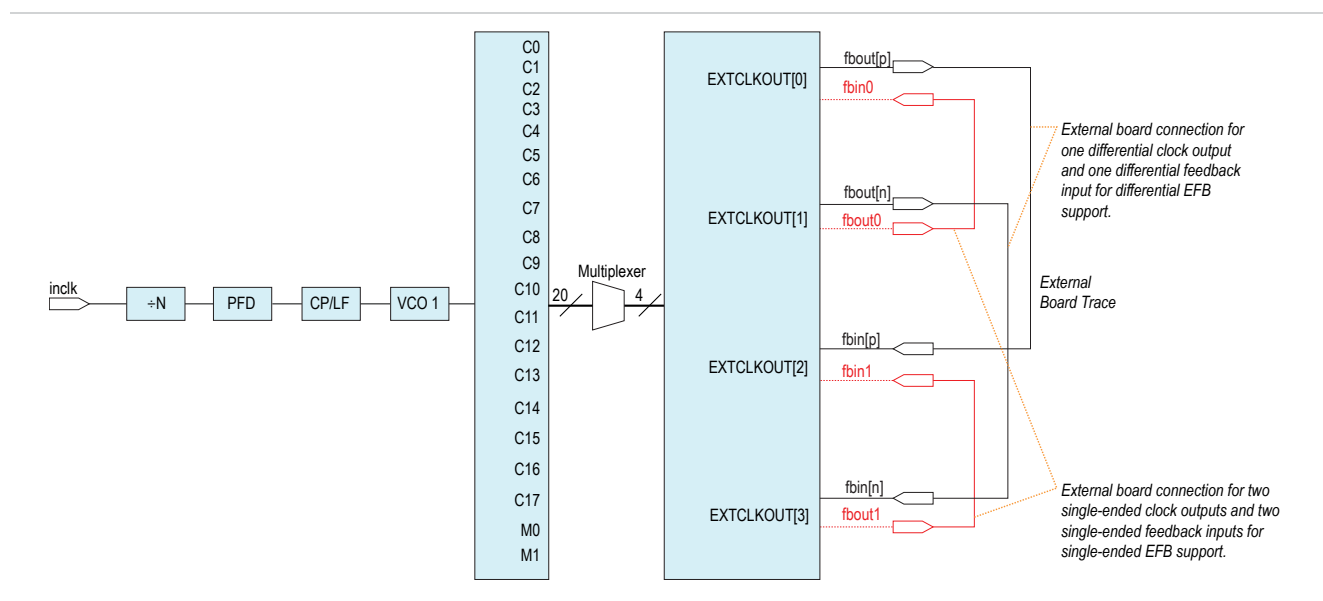
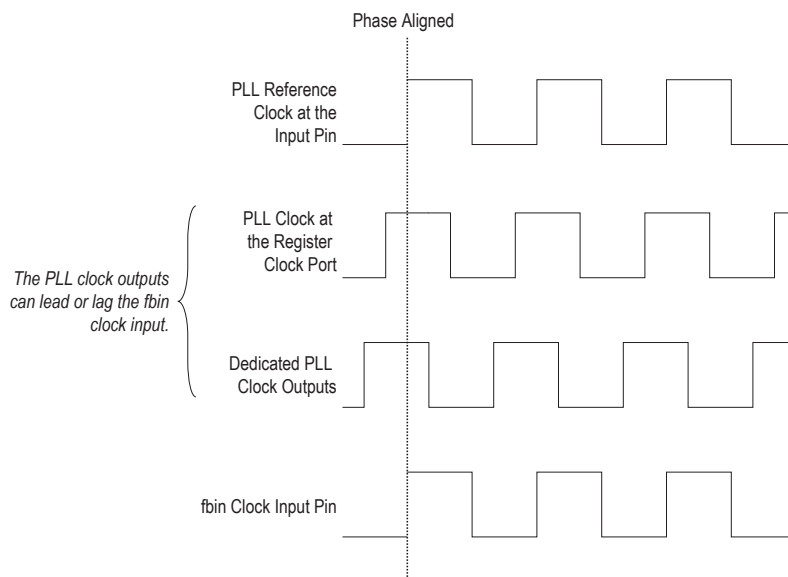


Figure 4-33: Example of Phase Relationship Between the PLL Clocks in EFB Mode**Related Information**

[PLL External Clock I/O Pins](#) on page 4-24

Provides more information about PLL clock outputs.

Multiple PLLs in Normal Mode and Source Synchronous Mode

Normal and source synchronous compensation feedback mode require GCLK or RCLK feedback path to achieve the required phase relationship. Source synchronous mode for LVDS compensation does not require the GCLK or RCLK feedback path.

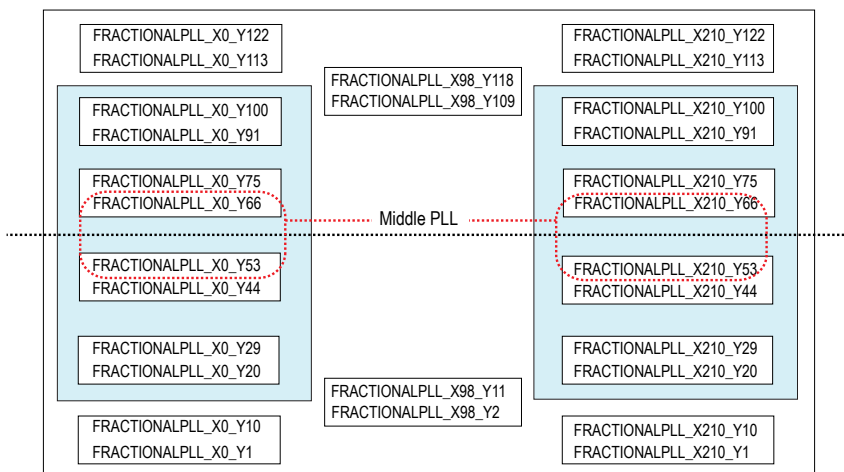
The GCLK or RCLK network feedback paths are fewer than the PLLs available on the device. You cannot implement the compensation mode that requires GCLK or RCLK feedback path on all the PLLs available on the device simultaneously.

Consider the following guidelines when implementing normal compensation or source synchronous compensation mode on multiple PLLs for the device:

- You can implement normal compensation or source synchronous compensation mode on all the center PLLs simultaneously.
- The Stratix V device has two middle PLLs on the left and right side of the device. All PLLs that reside on each side of the device can be divided equally into 2 groups as shown in the following figure.

Figure 4-34: Example of the PLL Grouping for Stratix V GX A5 and A7 Devices, and Stratix V GT C5 and C7 Devices

This figure represents the top view of the silicon die that corresponds to a reverse view of the device package.



From the PLL grouping example, the PLLs can be divided into 4 different sections (upper left, lower left, upper right, and lower right). The PLLs in each of these sections can be further divided into first and second group. The first group consists of the 2 corner PLLs and one middle PLL located in each section. The remaining PLLs in the same section are grouped into the second group. For each section, you can use up to 3 PLLs to implement source synchronous or normal compensation mode in the following combinations:

- Any of the 3 PLLs in the first group
- Any of the 2 PLLs in the first group and 1 PLL in the second group

Table 4-7: Example of the PLL Grouping for Stratix V GX A5 and A7 Devices, and Stratix V GT C5 and C7 Devices

PLL Section	PLL Location	
	First Group	Second Group
Upper left	FRACTIONALPLL_X0_Y122, FRACTIONALPLL_X0_Y113, FRACTIONALPLL_X0_Y66	FRACTIONALPLL_X0_Y100, FRACTIONALPLL_X0_Y91, FRACTIONALPLL_X0_Y75
Lower left	FRACTIONALPLL_X0_Y53, FRACTIONALPLL_X0_Y10, FRACTIONALPLL_X0_Y1	FRACTIONALPLL_X0_Y44, FRACTIONALPLL_X0_Y29, FRACTIONALPLL_X0_Y20
Upper right	FRACTIONALPLL_X210_Y122, FRACTIONALPLL_X210_Y113, FRACTIONALPLL_X210_Y66	FRACTIONALPLL_X210_Y100, FRACTIONALPLL_X210_Y91, FRACTIONALPLL_X210_Y75
Lower right	FRACTIONALPLL_X210_Y53, FRACTIONALPLL_X210_Y10, FRACTIONALPLL_X210_Y1	FRACTIONALPLL_X210_Y44, FRACTIONALPLL_X210_Y29, FRACTIONALPLL_X210_Y20

Clock Multiplication and Division

Each Stratix V PLL provides clock synthesis for PLL output ports using the $M/(N \times C)$ scaling factors. The input clock is divided by a pre-scale factor, N , and is then multiplied by the M feedback factor. The control loop drives the VCO to match $f_{in} \times (M/N)$.

The Quartus II software automatically chooses the appropriate scaling factors according to the input frequency, multiplication, and division values entered into the ALTERA_PLL megafunction.

Post-Scale Counter, K

A post-scale counter, K , is inserted after the VCO. When you enable the VCO post-scale counter, the counter divides the VCO frequency by two. When the K counter is bypassed, the VCO frequency goes to the output port without being divided by two.

Post-Scale Counter, C

Each output port has a unique post-scale counter, C , that divides down the output from the K counter. For multiple PLL outputs with different frequencies, the VCO is set to the least common multiple of the output frequencies that meets its frequency specifications. For example, if the output frequencies required from one PLL are 33 and 66 MHz, the Quartus II software sets the VCO to 660 MHz (the least common multiple of 33 and 66 MHz within the VCO range). Then the post-scale counters, C , scale down the VCO frequency for each output port.

Pre-Scale Counter, N and Multiply Counter, M

Each PLL has one pre-scale counter, N , and one multiply counter, M , with a range of 1 to 512 for both M and N . The N counter does not use duty-cycle control because the only purpose of this counter is to calculate frequency division. The post-scale counters have a 50% duty cycle setting. The high- and low-count values for each counter range from 1 to 256. The sum of the high- and low-count values chosen for a design selects the divide value for a given counter.

Delta-Sigma Modulator

The delta-sigma modulator (DSM) is used together with the M multiply counter to enable the PLL to operate in fractional mode. The DSM dynamically changes the M counter divide value on a cycle to cycle basis. The different M counter values allow the "average" M counter value to be a non-integer.

Fractional Mode

In fractional mode, the M counter divide value equals to the sum of the "clock high" count, "clock low" count, and the fractional value. The fractional value is equal to $K/2^X$, where K is an integer between 0 and $(2^X - 1)$, and $X = 8, 16, 24$, or 32.

Integer Mode

For PLL operating in integer mode, M is an integer value and DSM is disabled.

Related Information

[Altera Phase-Locked Loop \(ALTERA_PLL\) Megafunction User Guide](#)

Provides more information about PLL software support in the Quartus II software.

Programmable Duty Cycle

The programmable duty cycle allows PLLs to generate clock outputs with a variable duty cycle. This feature is supported on the PLL post-scale counters.

The duty-cycle setting is achieved by a low and high time-count setting for the post-scale counters. To determine the duty cycle choices, the Quartus II software uses the frequency input and the required multiply or divide rate.

The post-scale counter value determines the precision of the duty cycle. The precision is defined as 50% divided by the post-scale counter value. For example, if the `C0` counter is 10, steps of 5% are possible for duty-cycle choices from 5% to 90%. If the PLL is in external feedback mode, set the duty cycle for the counter driving the `fbin` pin to 50%.

Combining the programmable duty cycle with programmable phase shift allows the generation of precise non-overlapping clocks.

Clock Switchover

The clock switchover feature allows the PLL to switch between two reference input clocks. Use this feature for clock redundancy or for a dual-clock domain application where a system turns on the redundant clock if the previous clock stops running. The design can perform clock switchover automatically when the clock is no longer toggling or based on a user control signal, `clkswitch`.

The following clock switchover modes are supported in Stratix V PLLs:

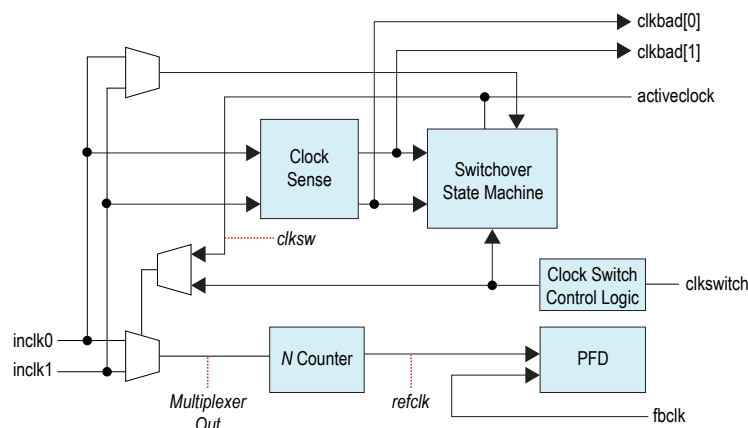
- Automatic switchover—The clock sense circuit monitors the current reference clock. If the current reference clock stops toggling, the reference clock automatically switches to `inclk0` or `inclk1` clock.
- Manual clock switchover—Clock switchover is controlled using the `clkswitch` signal. When the `clkswitch` signal goes from logic low to logic high, and stays high for at least three clock cycles, the reference clock to the PLL is switched from `inclk0` to `inclk1`, or vice-versa.
- Automatic switchover with manual override—This mode combines automatic switchover and manual clock switchover. When the `clkswitch` signal goes high, it overrides the automatic clock switchover function. As long as the `clkswitch` signal is high, further switchover action is blocked.

Automatic Switchover

Stratix V PLLs support a fully configurable clock switchover capability.

Figure 4-35: Automatic Clock Switchover Circuit Block Diagram

This figure shows a block diagram of the automatic switchover circuit built into the PLL.



When the current reference clock is not present, the clock sense block automatically switches to the backup clock for PLL reference. You can select a clock source as the backup clock by connecting it to the `inclk1` port of the PLL in your design.

The clock switchover circuit sends out three status signals—`clkbad[0]`, `clkbad[1]`, and `activeclock`—from the PLL to implement a custom switchover circuit in the logic array.

In automatic switchover mode, the `clkbad[0]` and `clkbad[1]` signals indicate the status of the two clock inputs. When they are asserted, the clock sense block detects that the corresponding clock input has stopped toggling. These two signals are not valid if the frequency difference between `inclk0` and `inclk1` is greater than 20%.

The `activeclock` signal indicates which of the two clock inputs (`inclk0` or `inclk1`) is being selected as the reference clock to the PLL. When the frequency difference between the two clock inputs is more than 20%, the `activeclock` signal is the only valid status signal.

Note: Glitches in the input clock may cause the frequency difference between the input clocks to be more than 20%.

Use the switchover circuitry to automatically switch between `inclk0` and `inclk1` when the current reference clock to the PLL stops toggling. You can switch back and forth between `inclk0` and `inclk1` any number of times when one of the two clocks fails and the other clock is available.

For example, in applications that require a redundant clock with the same frequency as the reference clock, the switchover state machine generates a signal (`clksw`) that controls the multiplexer select input. In this case, `inclk1` becomes the reference clock for the PLL.

When using automatic clock switchover mode, the following requirements must be satisfied:

- Both clock inputs must be running.
- The period of the two clock inputs can differ by no more than 20%.

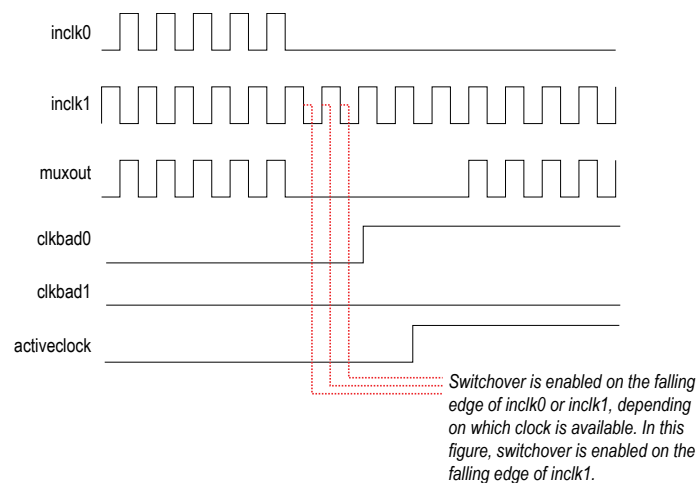
If the current clock input stops toggling while the other clock is also not toggling, switchover is not initiated and the `clkbad[0..1]` signals are not valid. If both clock inputs are not the same frequency, but their

period difference is within 20%, the clock sense block detects when a clock stops toggling. However, the PLL may lose lock after the switchover is completed and needs time to relock.

Note: Altera recommends resetting the PLL using the `areset` signal to maintain the phase relationships between the PLL input and output clocks when using clock switchover.

Figure 4-36: Automatic Switchover After Loss of Clock Detection

This figure shows an example waveform of the switchover feature in automatic switchover mode. In this example, the `inclk0` signal is stuck low. After the `inclk0` signal is stuck at low for approximately two clock cycles, the clock sense circuitry drives the `clkbad[0]` signal high. Since the reference clock signal is not toggling, the switchover state machine controls the multiplexer through the `clkswitch` signal to switch to the backup clock, `inclk1`.



Automatic Switchover with Manual Override

In automatic switchover with manual override mode, you can use the `clkswitch` signal for user- or system-controlled switch conditions. You can use this mode for same-frequency switchover, or to switch between inputs of different frequencies.

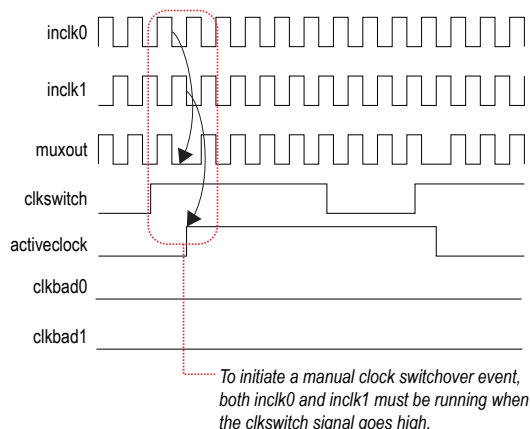
For example, if `inclk0` is 66 MHz and `inclk1` is 200 MHz, you must control switchover using the `clkswitch` signal. The automatic clock-sense circuitry cannot monitor clock input (`inclk0` and `inclk1`) frequencies with a frequency difference of more than 100% (2×).

This feature is useful when the clock sources originate from multiple cards on the backplane, requiring a system-controlled switchover between the frequencies of operation.

You must choose the backup clock frequency and set the M, N, C, and K counters so that the VCO operates within the recommended operating frequency range. The ALTERA_PLL MegaWizard Plug-in Manager notifies you if a given combination of `inclk0` and `inclk1` frequencies cannot meet this requirement.

Figure 4-37: Clock Switchover Using the `clkswitch` (Manual) Control

This figure shows a clock switchover waveform controlled by the `clkswitch` signal. In this case, both clock sources are functional and `inclk0` is selected as the reference clock; the `clkswitch` signal goes high, which starts the switchover sequence. On the falling edge of `inclk0`, the counter's reference clock, `muxout`, is gated off to prevent clock glitching. On the falling edge of `inclk1`, the reference clock multiplexer switches from `inclk0` to `inclk1` as the PLL reference. The `activeclock` signal changes to indicate the clock which is currently feeding the PLL.



In automatic override with manual switchover mode, the `activeclock` signal mirrors the `clkswitch` signal. Since both clocks are still functional during the manual switch, neither `clkbad` signal goes high. Because the switchover circuit is positive-edge sensitive, the falling edge of the `clkswitch` signal does not cause the circuit to switch back from `inclk1` to `inclk0`. When the `clkswitch` signal goes high again, the process repeats.

The `clkswitch` signal and automatic switch work only if the clock being switched to is available. If the clock is not available, the state machine waits until the clock is available.

Related Information

[Altera Phase-Locked Loop \(ALTERA_PLL\) Megafunction User Guide](#)

Provides more information about PLL software support in the Quartus II software.

Manual Clock Switchover

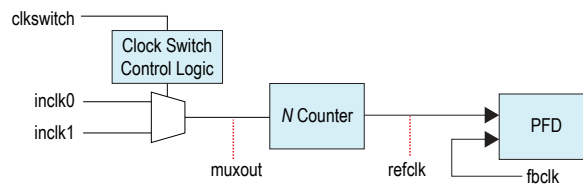
In manual clock switchover mode, the `clkswitch` signal controls whether `inclk0` or `inclk1` is selected as the input clock to the PLL. By default, `inclk0` is selected.

A clock switchover event is initiated when the `clkswitch` signal transitions from logic low to logic high, and being held high for at least three `inclk` cycles.

You must bring the `clkswitch` signal back low again to perform another switchover event. If you do not require another switchover event, you can leave the `clkswitch` signal in a logic high state after the initial switch.

Pulsing the `clkswitch` signal high for at least three `inclk` cycles performs another switchover event.

If `inclk0` and `inclk1` are different frequencies and are always running, the `clkswitch` signal minimum high time must be greater than or equal to three of the slower frequency `inclk0` and `inclk1` cycles.

Figure 4-38: Manual Clock Switchover Circuitry in Stratix V PLLs

You can delay the clock switchover action by specifying the switchover delay in the `ALTERA_PLL` megafunction. When you specify the switchover delay, the `clkswitch` signal must be held high for at least three `inclk` cycles plus the number of the delay cycles that has been specified to initiate a clock switchover.

Related Information

[Altera Phase-Locked Loop \(ALTERA_PLL\) Megafunction User Guide](#)

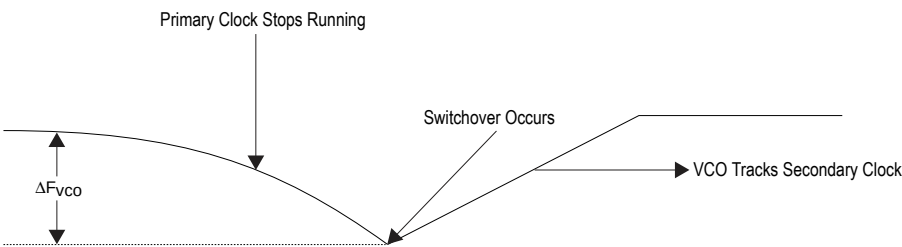
Provides more information about PLL software support in the Quartus II software.

Guidelines

When implementing clock switchover in Stratix V PLLs, use the following guidelines:

- Automatic clock switchover requires that the `inclk0` and `inclk1` frequencies be within 20% of each other. Failing to meet this requirement causes the `clkbad[0]` and `clkbad[1]` signals to not function properly.
- When using manual clock switchover, the difference between `inclk0` and `inclk1` can be more than 100% (2×). However, differences in frequency, phase, or both, of the two clock sources will likely cause the PLL to lose lock. Resetting the PLL ensures that you maintain the correct phase relationships between the input and output clocks.
- Both `inclk0` and `inclk1` must be running when the `clkswitch` signal goes high to initiate the manual clock switchover event. Failing to meet this requirement causes the clock switchover to not function properly.
- Applications that require a clock switchover feature and a small frequency drift must use a low-bandwidth PLL. When referencing input clock changes, the low-bandwidth PLL reacts more slowly than a high-bandwidth PLL. When switchover happens, a low-bandwidth PLL propagates the stopping of the clock to the output more slowly than a high-bandwidth PLL. However, be aware that the low-bandwidth PLL also increases lock time.
- After a switchover occurs, there may be a finite resynchronization period for the PLL to lock onto a new clock. The time it takes for the PLL to relock depends on the PLL configuration.
- The phase relationship between the input clock to the PLL and the output clock from the PLL is important in your design. Assert `areset` for at least 10 ns after performing a clock switchover. Wait for the locked signal to go high and be stable before re-enabling the output clocks from the PLL.
- The VCO frequency gradually decreases when the current clock is lost and then increases as the VCO locks on to the backup clock, as shown in the following figure.

Figure 4-39: VCO Switchover Operating Frequency



PLL Reconfiguration and Dynamic Phase Shift

For more information about PLL reconfiguration and dynamic phase shifting, refer to AN661.

Related Information
[AN661: Implementing Fractional PLL Reconfiguration with ALTERA_PLL and ALTERA_PLL_RECONFIG Megafunctions](#)

Document Revision History

Date	Version	Changes
May 2013	2013.05.06	• Added link to the known document issues in the Knowledge Base. • Updated PCLK clock sources per device quadrant. • Added PCLK networks resources and diagram for Stratix V E devices. • Updated PCLK clock sources in hierarchical clock networks in each spine clock per quadrant diagram. • Added PCLK networks in clock network sources section. • Updated dedicated clock input pins in clock network sources section. • Added information on C output counters for PLLs. • Added power down mode in PLL features table. • Added information on PLL physical counters. • Updated the PLL locations index from CEN_X<#>_Y<#>, COR_X<#>_Y<#>, and LR_X<#>_Y<#> to FRACTIONALPLL_X<#>_Y<#>. • Removed LVPECL I/O standard support for clock output pin pairs. • Updated PLL support for EFB mode. • Updated the scaling factors for PLL output ports. • Updated the fractional value for PLL in fractional mode. • Moved all links to the Related Information section of respective topics for easy reference. • Reorganized content.

Date	Version	Changes
December 2012	2012.12.28	- Added note to indicate that the figures shown are the top view of the silicon die. - Added diagram for PLL physical counter orientation. - Updated PLL locations diagrams. - Removed information on pfdena PLL control signal. - Removed information on PLL Compensation assignment in the Quartus II software. - Updated the fractional value for PLL in fractional mode. - Reorganized content and updated template.
June 2012	1.4	- Added Table 4-5 and Table 4-6. - Added Figure 4-6, Figure 4-8, Figure 4-20, Figure 4-22, and Figure 4-33. - Updated Table 4-1, Table 4-2, and Table 4-3. - Updated Figure 4-3, Figure 4-5, Figure 4-17, Figure 4-18, Figure 4-19, and Figure 4-21. - Added “PLL Migration Guidelines”, “Implementing Multiple PLLs in Normal Mode and Source Synchronous Mode”, “Clock Switchover”, and “PLL Reconfiguration and Dynamic Phase Shift” sections. - Updated “Clock Networks in Stratix V Devices”, “Clock Network Sources”, and “Clock Multiplication and Division” sections.
November 2011	1.3	Updated Figure 4-19 and Figure 4-28.
May 2011	1.2	- Chapter moved to volume 2 for the 11.0 release. - Updated Table 4-1. - Updated Figure 4-3, Figure 4-4, Figure 4-5, Figure 4-6, Figure 4-15, Figure 4-17, Figure 4-18, Figure 4-20, Figure 4-25, and Figure 4-28. - Updated “Zero-Delay Buffer Mode” and “External Feedback Mode” sections. - Added “PLL Clock Outputs” section.
December 2010	1.1	No changes to the content of this chapter for the Quartus II software 10.1.
July 2010	1.0	Initial release.