

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

AMAZON.COM, INC. and AMAZON.COM SERVICES LLC,
Petitioners,

V.

INTERDIGITAL VC HOLDINGS, INC.,
Patent Owner.

IPR2026-00193
U.S. Patent No. 11,936,876

PETITIONERS' PRELIMINARY REPLY

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Patent Trial and Appeal Board
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EXHIBIT LIST

No.	Exhibit
1001	U.S. Patent No. 11,936,876 (“’876 patent”)
1002	File History of the ’876 patent
1003	Declaration of Dr. Scott T. Acton, Ph.D.
1004	Curriculum Vitae of Dr. Scott T. Acton, Ph.D.
1005	WO2008/083633 (“Xiong”)
1006	Certified English Translation of WO2008/083633 (“Xiong”)
1007	European Patent No. EP2081388 (“Xiong EP”)
1008	Enlarging MB size for high fidelity video coding beyond HD (“VCEG-AJ21”), available at https://www.itu.int/wftp3/av-arch/video-site/0810_San/VCEG-AJ21.zip
1009	M. Faundez-Zanuy, F. Vallverdú_Bayes, F. Tarrés-Ruiz “Contributions to interframe coding.” Workshop on image analysis & synthesis in image coding. October 1994.
1010	ITU-T Recommendation H.264 (May 2003) (“H.264”)
1011	Editing State of Text Relating to ITU-T Rec. H.264 ISO/IEC 14496-10 Amendments 1 and 2 (“ITU-T H.264 Draft”)
1012	Declaration of Dr. Clifford Reader (“Reader”)
1013	Declaration of June Ann Munford (“Munford”)
1014	“The H.264/AVC Advanced Video Coding Standard: Overview and Introduction to the Fidelity Range Extensions,” Gary J. Sullivan, et al. (August 2004) (“Sullivan1”)
1015	“The H.264/AVC Advanced Video Coding Standard: Overview and Introduction to the Fidelity Range Extensions,” Gary J. Sullivan, Ph.D (August 2004) (“Sullivan2”)

No.	Exhibit
1016	ITU-T Recommendation H.264 (March 2005) (“H.264 (03/2005)”)
1017	Recommendation H.264 (2005) Amendment 2 (04/07) (Munford, Appendix H26403) (“Amendment 2”)
1018	“The H.264/MPEG-4 Advanced Video Coding (AVC) Standard,” Gary J. Sullivan, Ph.D (July 2005) (“Sullivan2”), available at https://www.itu.int/ITU-T/worksem/vica/docs/presentations/S3_P1_Sullivan.pdf
1019	Stipulation Letter, dated February 23, 2026
1020	InterDigital 10-K (Fiscal Year 2022)
1021	U.S. Patent Pub. No. 2010/0086029A1 (“Chen”)
1022	U.S. Patent Pub. No. 2009/0046781A1 (“Moriya”)
1023	U.S. Patent Pub. No. 2008/0123947 (“Moriya ’947”)
1024	U.S. Patent Pub. No. 2009/0219991 (“Po”)

I. Xiong discloses intra prediction of a 32x32 macroblock

Patent Owner (“PO”) relies solely on the Background Art section of Xiong to argue that Xiong does not disclose an intra prediction method using a 32x32 block. POPR, 20-21 (citing EX-1006, 1-2 (“Background Art”)). But that discloses only what existed previously. In particular, the Background Art section provides a “brief introduction to the intra frame prediction encoding technology of H.264/AVC....” EX-1006, 1. When considered in its entirety, however, Xiong discloses an intra prediction method for 32x32 (and larger) blocks.

PO asserts that displacement intra prediction (DIP) “applies to H.264/AVC and is therefore also described as only applying to 4×4, 8×8, and 16×16 block sizes.” POPR, 21 (citing EX-1006, 2). Xiong says no such thing. Rather, Xiong explains that DIP “is generally applied at the macroblock level.” EX-1006, 2. And while H.264/AVC may have been limited to 16x16 and smaller macroblocks, Xiong explicitly discloses “the macroblock here is not necessarily limited to a 16×16 macroblock; it can also be of other sizes, such as a 32×32 macroblock.” EX-1006, 6. Xiong thus discloses a 32x32 (and potentially larger) macroblock as well as an intra prediction method applied at the macroblock level, and taken together, these disclosures teach intra prediction for macroblocks that are 32x32 or larger.

II. VCEG-AJ21 was used only as an alternative reference to show a 64x64 macroblock

PO dismisses the Petition's use of VCEG-AJ21 by arguing that it discloses only inter prediction techniques, not intra prediction techniques. *See* POPR, 27-28, 36-37. This argument ignores, however, that the Petition does not rely on VCEG-AJ21 for disclosure of intra prediction; rather, the Petition points to VCEG-AJ21 only for alternative disclosure of a 64x64 macroblock in the event that the Board finds Xiong alone does not teach a 64x64 macroblock. Petition, 23-24.

For disclosure of intra prediction methods, the Petition relies on Xiong's teachings as applied to the 64x64 macroblock. *See, e.g.,* Petition, 28 ("a POSITA would have understood, *based on Xiong's teachings*, there would also be an ext_32x32_pred_flag and an ext_64x64_pred_flag for those [32x32 and 64x64] blocks.") (emphasis added), 29 ("a POSITA would have understood, *based on Xiong's teachings*, that for a 64x64 macroblock, as disclosed by VCEG-AJ21, if ext_64x64_pred_flag....") (emphasis added), 31 ("VCEG-AJ21 discloses or suggests a 64x64 macroblock, and a POSITA would have understood, *based on Xiong's teachings*, there would also be an ext_64x64_pred_flag....") (emphasis added).

The Petition similarly relies in the first instance on Xiong for disclosure of a 64x64 macroblock. Petition, 24 ("a POSITA would have understood that the reference to macroblocks 'of other sizes' would include a 64x64 macroblock"). The

use of VCEG-AJ21's 64x64 macroblock is therefore an alternative argument that is not strictly necessary for finding the claims invalid.

Nor is disclosure of a 64x64 macroblock necessary to show invalidity of any independent claim, each of which recites a "block size equal to or larger than 32x32." Showing a 64x64 macroblock is only necessary for dependent claims 3, 7, 13, 17, which require "sub-blocks" of the original large block to be "greater than a basic coding unit size" (i.e., larger than 16x16). In that case, the 64x64 block provides the original large block, and 32x32 blocks provide the sub-blocks. *See* Petition, 36 (describing 64x64 blocks that are split into 32x32 sub-blocks, where at least one of those 32x32 blocks is further split into smaller sub-blocks).

III. Dr. Havlicek recognized that a POSITA would understand that VCEG-AJ21 discloses intra-prediction modes

In arguing that VCEG-AJ21 does not disclose intra prediction, PO also misrepresents Dr. Havlicek's declaration from a *different* IPR proceeding (IPR2026-00192). POPR, 27 ("Petitioner's expert in a parallel proceeding admitting that VCEG-AJ21 applies solely to *inter* prediction") (emphasis in original) (citing EX-2012, ¶¶72-73), 37 (same). Dr. Havlicek did not admit that VCEG-AJ21 applies solely to inter prediction; rather, he explained that while VCEG-AJ21 explicitly disclosed modes for inter prediction, "a POSITA would have understood that the [listed] inter prediction modes ... are a super set of the intra prediction modes for enlarged macroblocks." EX-2012, ¶73. And Dr. Havlicek further explained that "a

POSITA would have been well aware of and appreciated the fact that, within the context of ‘H.264-like’ video codecs providing spatial intra prediction at the time, the set of macroblock partition types available for intra prediction was a subset of the types available for inter prediction—specifically consisting of the ‘square’ partition types and omitting the ‘oblong rectangular’ partition types.” *Id.* Thus, contrary to PO’s assertion, Dr. Havlicek opined that VCEG-AJ21 *does* disclose intra prediction modes.

IV. The Petition relies on different syntax elements for limitations 1[b] and 1[e]

PO likewise mischaracterizes Petitioner’s position when PO argues that “Petitioner ... attempts to equate Xiong’s ext_16×16_pred_flag to both the claimed *binary split signaling syntax* **and** the claimed *second syntax element indicating a single spatial intra partition type for at least one basic coding unit sized sub-block.*” POPR, 38-39 (emphasis in original); *see also id.* at 3 (“Petitioner relies on a particular flag described in Xiong for 16×16 blocks, but this flag cannot teach both a *binary split signaling syntax* **and** the claimed *second syntax element.*”) (emphasis in original).

PO is incorrect. For limitation 1[b] (reciting a *binary split signaling syntax element*), the Petition points to Xiong and explains that, “when using a 32x32 macroblock, there would also be an ext_32x32_pred_flag,” providing the *binary*

split signaling syntax element. Petition, 26.¹ It is only for limitation 1[e] (reciting *a second syntax element*) that the Petition relies on Xiong’s `ext_16x16_pred_flag`. Petition, 32.

PO nevertheless further incorrectly argues that “[o]nce Petitioner assigns that extrapolated `ext_32x32_pred_flag` to element 1[b], `ext_16x16_pred_flag` cannot simultaneously be elevated to satisfy element 1[e].” POPR, 40. As the Petition explains, Xiong discloses encoding in a hierarchical tree structure, and “at each level of the hierarchy, a flag (`ext_[NxN]_pred_flag`) is set.” Petition, 18. Thus, when using a 32x32 macroblock, there would be an `ext_32x32_pred_flag` (POPR, 26) that exists at a different level of the hierarchy than the `ext_16x16_pred_flag` that meets limitation 1[e]. Petition, 32-33.

Notwithstanding PO’s misrepresentation of Petitioner’s arguments and focus on out-of-context portions of the cited references, considering the Petition and the cited references in their entirety demonstrates the invalidity of challenged claims, and trial on the Petition should be instituted.

¹ Similarly, for a 64x64 macroblock, necessary for dependent claims 3, 7, 13, 17, “there would be a flag (e.g., `ext_64x64_pred_flag`) that indicates that block should be partitioned into four 32x32 sub-blocks.” Petition, 26-27.

Dated: May 5, 2026

Respectfully submitted,

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CERTIFICATE OF SERVICE

I hereby certify that on May 5, 2026 true and correct copies of the foregoing PETITIONERS' PRELIMINARY REPLY was served via electronic mail upon the following counsel of record for Patent Owner:

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