

Comparison of Challenged Claims In '286 Patent and '381 Patent

'286 Patent Claims	Comparison to '381 Patent's Claims
[1.preamble] A method for processing a first serial data stream comprising market data, using a field programmable gate array system, to generate a second serial data stream comprising order entry data, wherein the method comprises the steps of:	The question whether the preamble to claim 1 of the '286 patent is limiting is unique to this Petition. The preamble to claim 1 of the '381 patent contains the same limitation regarding market and order-entry data. But that limitation appears in dependent claims 2 and 3, not a claim preamble. Thus, the question whether this term is limiting was not posed in the '381 Petition. '381 Petition at 71-74. Without the market and order-entry data language, the rest of the preamble is the same as claim 1 of the '381 patent, and the arguments are materially the same as those raised in that petition. '381 Petition at 29-30.
[1.a] receiving, by a first plurality of data pins in a first interface of a field programmable gate array in the field programmable gate array system, the first serial data stream;	This limitation does not have an explicit corresponding limitation in the '381 patent.
[1.b] receiving, by a first reference clock pin in the first interface, a first clock signal having a first frequency and a first phase;	This limitation does not have an explicit corresponding limitation in the '381 patent.
[1.c] transmitting, from the first plurality of data pins in the first interface to a deserializer in the field programmable gate array, the first serial data stream;	This limitation describes transmission of the first serial data stream from the data pins to the deserializer. This is analogous to—but not identical to—the '381 patent's claim 1(b), which simply describes the deserializer's receipt of the first serial data stream. '381 Petition at 32-34.

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[1.d] providing, from the first reference clock pin in the first interface to the deserializer, a clock signal based at least on the first clock signal;	This limitation describes providing, from the first reference clock pin in the first interface to the deserializer, a clock signal based at least on the first clock signal. This is analogous to—but not identical to—the '381 patent's claim 1(a), which simply describes the deserializer's receipt of a clock signal. '381 Petition at 30-31.
[1.e] generating, by the deserializer, a first receiver side clock signal having a second frequency and a second phase, based at least in part on the first clock signal;	This limitation is the same as claim 1(c) in the '381 patent but adds limitations relating to frequency and phase attributes. '381 Petition at 34-37
[1.f] converting, by the deserializer, the first serial data stream into a first plurality of parallel data streams;	Claim 1(f) is materially the same as claim 1(d) in the '381 patent. '381 Petition at 37-39.
[1.g] transmitting, from the deserializer to the computational circuitry, the first plurality of data streams comprising a first plurality of data items and a first amount of data streams;	Claim 1(g) is materially the same as claim 1(e) in the '381 patent except that the '286 patent's claim 1(g) adds that the data streams comprise a first plurality of data items and a first amount of data streams. '381 Petition at 39-41.
[1.h] transmitting, via a first clock output pin on a second interface of the field programmable gate array to a phase detector that is part of the field programmable gate array system and not part of the field programmable gate array, the first receiver side clock signal;	Claim 1(h) is materially the same as claim 1(f) of the '381 patent except that '286 patent's claim 1(h) references the first output pin on a second interface and specifies that the phase detector within the phase lock loop receives the clock signal. '381 Petition at 41-42.

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[1.i] generating, using the field programmable gate array system, a feedback clock signal associated with a first transmitter side clock signal, the feedback clock signal having a third frequency and a third phase, by performing the following steps until a first output of the phase detector is below a first threshold level:	Claim 1(i)'s preamble is materially the same as the preamble to claim 8(i) of the '381 patent except that the '286 patent's claim 1(i) preamble describes generation by the field programmable gate array system (as opposed to the phase lock loop); and describes the feedback clock as having a third frequency and phase. '381 Petition at 53-55.
[1.i.i] generating, by an adjustable oscillator in the field programmable gate array system, a second clock signal having a fourth frequency and a fourth phase;	Claim 1(i)(i) is materially the same as claim 8(i)(1) of the '381 patent except that '286 patent's claim 1(i) describes the second clock signal as having a fourth frequency and phase. '381 Petition at 55.
[1.i.ii] generating, by the phase detector, the first output based on a comparison of the first receiver side clock signal and the feedback clock signal obtained from the second clock signal;	Claim 1(i)(ii) is materially the same as claim 8(i)(2) of the '381 patent. '381 Petition at 56.
[1.i.iii] transmitting, from the phase detector to a phase controller of the field programmable gate array system which is not in the field programmable gate array, the first output;	Claim 1(i)(iii) is materially the same as claim 8(i)(3) of the '381 patent except that the '286 patent specifies that the phase controller is "not in the field programmable gate array"—an additional limitation that does not affect the analysis. '381 Petition at 57.

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[1.i.iv] determining, by the phase controller, interim adjustment information based on the first output; and	Claim 1(i)(iv) is identical to claim 8(i)(4) of the '381 patent. '381 Petition at 57-58.
[1.i.v] transmitting, from the phase controller to the adjustable oscillator, the interim adjustment information;	Claim 1(i)(v) is identical to claim 8(i)(5) of the '381 patent. '381 Petition at 58-59.
[1.i.wherein] wherein, the adjustable oscillator adjusts the second clock signal based on the interim adjustment information and steps (i) through (v) are repeated until the first output of the phase detector is below the first threshold level;	Claim 1(i)(wherein) is identical to claim 8(i)(wherein) of the '381 patent. '381 Petition at 59-60
[1.j] generating, by the serializer, a first transmitter side clock signal based on the second clock signal; and	Claim 1(j) is materially the same as claim 1(h) of the '381 patent except that claim 1(j) specifies that the serializer generates the first transmitter side clock signal and that this clock signal is based on (as opposed to derived from) the second clock signal. '381 Petition at 43-44.
[1.k] transmitting, by the serializer to the computational circuitry, the first transmitter side clock signal;	Claim 1(k) does not have an explicit corresponding limitation in the '381 patent.

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[1.l] performing, by the computational circuitry, a first set of operations on at least a portion of the first plurality of data items to generate a second plurality of parallel data streams comprising a second amount of data streams;	Claim 1(l) is materially the same as claim 1(i) of the '381 patent except that the '286 patent's claim 1(l) specifies the computational circuitry performs operations on the data items (as opposed to the data streams) and that the second plurality of data streams comprises a second amount of data streams. '381 Petition at 44-46.
[1.m] transmitting, from the computational circuitry to the serializer, the second plurality of parallel data streams;	Claim 1(m) does not have a corresponding limitation in the '381 patent.
[1.n] converting, by the serializer, the second plurality of parallel data streams into the second serial data stream; and	Claim 1(n) does not have an exactly corresponding limitation in the '381 patent except that claim 1(j) of the '381 patent describes the serial data stream as "derived from" the second plurality of parallel data streams, which is similar to the generating limitation in claim 1(n). '381 Petition at 46-47.
[1.o] transmitting, from the serializer off the field programmable gate array system via a second plurality of data pins in the first interface, the second serial data stream.	Claim 1(o) is materially the same as claim 1(j) in the '381 patent except that claim 1(o) describes the transmission from the serializer and the use of data pins to transmit the serial data. '381 Petition at 46-47; <i>see also</i> above (describing limitation of '381 patent's claim 1(j) that is similar to a limitation in '286 patent's claim 1(n)).
[2] The method of claim 1, wherein the second frequency corresponds to the first frequency.	Claim 2 does not have an explicit corresponding limitation in the '381 patent.

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[8] The method of claim 1, wherein a difference between the third phase and the second phase is less than a second threshold level.	Claim 8 does not have an explicit corresponding limitation in the '381 patent.
[10] The method of claim 1, wherein the first set of operations does not include clock domain crossing operations that delay processing of the first set of parallel data streams.	Claim 10 is materially the same as claim 1's wherein clause in the '381 patent except that the '286 patent's claim 10 says that the "claimed operations does not include clock domain crossing operations" and the '381 patent's wherein clause in claim 1 says that "the method does not use" a CDC. '381 Petition at 47-48, 79-80.
[11] The method of claim 1, wherein the first amount of data streams is the same as the second amount of data streams.	Claim 11 is similar to claim 9 in the '381 patent, although the language used is different. Claim 11 recites the amount of data streams whereas claim 9 in the '381 patent recites the same number of data streams. '381 Petition at 60.
[19] The method of claim 1, wherein the transmission of the second serial data stream from the serializer off the field programmable gate array is transmitted to an input/output module off the field programmable gate array.	Claim 19 does not have an explicit corresponding limitation in the '381 patent.