

Filed: January 9, 2026

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

CITADEL SECURITIES LLC,

PETITIONER,

V.

HFT SOLUTIONS, LLC,

PATENT OWNER.

Case No. IPR2026-00212

U.S. Patent No. 10,931,286

PETITION FOR *INTER PARTES* REVIEW
OF CLAIMS 1, 2, 8, 10-11, 19 AND 20 OF U.S. PATENT NO. 10,931,286

TABLE OF CONTENTS

I.	INTRODUCTION.....	1
II.	MANDATORY NOTICES.....	3
	A. Real Parties in Interest.....	3
	B. Related Matters.....	4
	C. Identification of Counsel and Service Information.....	5
III.	REQUIREMENTS FOR REVIEW.....	5
IV.	DISCRETIONARY DENIAL NOT WARRANTED.....	6
V.	SUMMARY OF THE PRIOR ART	8
	A. Altera	9
	B. Stratix Handbook.....	11
	C. Si5345 Manual	13
	D. “A Low-Latency Library in FPGA Hardware for High-Frequency Trading (HFT)” by John W. Lockwood.....	17
VI.	THE ’286 PATENT.....	20
	A. Effective Filing Date	20
	B. Specification.....	21
	C. Challenged Claims	22
	D. Prosecution History	23
	E. Level of Ordinary Skill	23
	F. HFT’s Theory of Infringing the ’286 Patent	24
VII.	CLAIM CONSTRUCTION	25
VIII.	THE CHALLENGED CLAIMS ARE UNPATENTABLE	26

A.	Ground 1A: Altera Anticipates Claims 1, 2, 8, 10-11, and 19.....	27
1.	A Skilled Artisan Would Recognize that the Features of the Stratix FPGA and Si5345 PLL Are Necessarily Present in Altera	27
2.	Limitation-By-Limitation Analysis.....	30
B.	Ground 1B: Altera, the Stratix Handbook, and the Si5345 Manual Render Claims 1, 2, 8, 10, 11, and 19 Obvious	76
C.	Ground 2: Altera and Lockwood render claim 1, 2, 8, 10-11, and 19-20 obvious	78
1.	A Skilled Artisan Would Have Been Motivated to Combine Altera and Lockwood.....	79
2.	Claim 1 preamble: “a first serial data stream comprising market data” and “a second serial data stream comprising order entry data”	84
3.	Claim 20: “The method of claim 1, wherein the first serial data stream includes market data and the second serial data stream includes trading data”	86
4.	Claim 1(k) and 1(l): It Would Have Been Obvious to Use the Computational Circuitry Present in Altera	87
5.	Claims 2, 8, 10, 11, and 19.....	89
IX.	CONCLUSION	89

TABLE OF AUTHORITIES

Cases

<i>Cochlear Bone Anchored Sols. AB v. Oticon Med. AB</i> , 958 F.3d 1348 (Fed. Cir. 2020).....	32
<i>FMC Corp. v. Sharda USA, LLC</i> , 145 F.4th 1326 (Fed. Cir. 2025)	30
<i>HFT Solutions, LLC v. Citadel Securities LLC</i> , 1:24-cv-13213 (N.D. Ill.)	4
<i>HFT Solutions, LLC v. Jump Trading, LLC</i> , 1:24-cv-13214 (N.D. Ill.)	4
<i>HFT Solutions, LLC v. Optiver US LLC</i> , 7:25-cv-00415 (W.D.	4
<i>In re Haines</i> , No. 2024-2338, 2025 WL 1403578 (Fed. Cir. May 15, 2025).....	28
<i>Monsanto Tech. LLC v. E.I. DuPont de Nemours & Co.</i> , 878 F.3d 1336 (Fed. Cir. 2018).....	29
<i>Neapco Drivelines LLC v. Am. Axle & Mfg., Inc.</i> , 847 F. App'x 856 (Fed. Cir. 2021)	31
<i>Norian Corp. v. Stryker Corp.</i> , 363 F.3d 1321 (Fed. Cir. 2004).....	
<i>Sage Prods., LLC v. Stewart</i> , 133 F.4th 1376 (Fed. Cir. 2025)	28
<i>Schumer v. Lab'y Computer Sys., Inc.</i> , 308 F.3d 1304 (Fed. Cir. 2002).....	30
<i>Symantec Corp. v. Computer Assocs. Int'l, Inc.</i> , 22 F.3d 1279 (Fed. Cir. 2008).....	30
<i>Telemac Cellular Corp. v. Topp Telecom, Inc.</i> , 247 F.3d 1316 (Fed. Cir. 2001).....	28

<i>W. Digital Corp. v. Spex Techs., Inc.</i> , No. IPR2018–00084, 2018 WL 1990268 (PTAB Apr. 25, 2018).....	25
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<i>Weber, Inc. v. Provisur Techs., Inc.</i> , 92 F.4th 1059 (Fed. Cir. 2024)	11, 13,
---	---------

Statutes

35 U.S.C. § 112	26
-----------------------	----

Regulations

37 C.F.R. § 42.100(b)	26
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37 C.F.R. § 42.104(a).....	5
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LIST OF EXHIBITS

EXHIBIT NO.	DESCRIPTION
1001	U.S. Patent No. 10,931,286
1002	Expert Declaration of Kevin B. Stanton, Ph.D.
1003	File History of U.S. Patent No. 10,931,286
1004	Synchronous Ethernet Solutions with Altera FPGAs and Silicon Labs Jitter-Attenuating PLLs (“Altera”)
1005	Altera Stratix V Handbook (“Stratix Handbook”)
1006	Any-Frequency, Any-Output Jitter-Attenuators/Clock Multipliers Si5345, Si5344, Si5342 Family Reference Manual, August 2015 (“Si5345 Manual”)
1007	A Low-Latency Library in FPGA Hardware for High-Frequency Trading (HFT) by John W. Lockwood et al., 2012 IEEE 20th Annual Symposium on High-Performance Interconnects (September 2012), https://doi.org/10.1109/HOTI.2012.15 (“Lockwood”)
1008	(Intentionally Omitted)
1009	Declaration of Mina Ching regarding website of Altera White Papers
1010	Declaration of Mina Ching regarding website of Stratix V Device Handbook
1011	Declaration of Mina Ching regarding website of Si5345/44/33 Data Sheet
1012	Patent Owner’s Initial Infringement Contentions for the ’286 Patent
1013	Altera and IDT Synchronous Ethernet Solution for ITU-T G.8262
1014	“The Race to Zero Latency for High Frequency Trading” by Saul Sahoo
1015	U.S. Patent No. 10,169,814

EXHIBIT NO.	DESCRIPTION
1016	High-Frequency Trading, A Practical Guide to Algorithmic Strategies and Trading Systems by Irene Aldridge (2013)
1017	Implementing Fractional PLL Reconfiguration with Altera PLL and Altera PLL Reconfig Megafunctions, Application Note AN-661-3.0, Altera Corporation, November 2013
1018	Exploring Algorithmic Trading in Reconfigurable Hardware by Stephen Wray (2010)
1019	HDL Chip Design, A practical guide for designing, synthesizing and simulating ASICs and FPGAs using VHDL or Verilog by Douglas J. Smith, Doone Publications (1999)
1020	UltraScale Architecture Clocking Resources – User Guide, Xilinx, April 9, 2018
1021	Chip Hall of Fame: XC2064 FPGA, IEEE Spectrum, June 30, 2017
1022	List and comparison of FPGA companies by Jeff Johnson, FPGA Developer, July 15, 2011
1023	Understanding Clock Domain Crossing (CDC) Checks and Techniques by Saurabh Verna, <i>et al.</i> , EE Times, December 24, 2007
1024	Phaselock Techniques by Floyd Gardner, Third Edition (2005)
1025	Interactive Brokers’ Founder Changed Trading Forever. What He Sees Next by David Wignall, Barrons (October 2, 2025)
1026	Wall Street’s Quest to Process Data at the Speed of Light by Richard Martin, Rubinow (April 21, 2017)
1027	FPGA accelerated low-latency market data feed processing by Gareth W. Morris, <i>et al.</i> , 17 th IEEE Symposium on High Performance Interconnects (2009)
1028	The Once and Future Ethernet by Daniel Svensson, Design Lines (May 1, 2001)
1029	An Introduction to Synchronized Internet, Embedded (March 3, 2009)

EXHIBIT NO.	DESCRIPTION
1030	Design of Control Systems by A. Frank D'Souza, Prentice-Hall (1988)
1031	Comparison of Challenged Claims in '286 Patent and '381 Patent

I. INTRODUCTION

Citadel Securities challenges claims 1, 2, 8, 10-11, and 19-20 of U.S. Patent No. 10,931,286. This is the second IPR against the same Patent Owner that Petitioner has filed challenging unpatentable claims that merely recite a simple and long-known arrangement for synchronizing clock signals on a programmable chip called a field programmable gate array (FPGA) using an external system called a phase-locked loop (PLL).¹ In fact, the '286 patent overlaps so much with the prior Petition regarding U.S. Patent No. 11,575,381, the arguments regarding patentability are almost the same. In fact, to facilitate review of these two related petitions, Petitioner has indicated throughout where the invalidating disclosures overlap and where they differ. The supporting expert declaration of Kevin Stanton likewise contains a nearly identical analysis to his declaration in support of the '381 Petition. *See generally* Ex. 1002. It is therefore unsurprising that the same prior art renders both patents invalid.

As this Petition demonstrates, both patents repackage the same known arrangements to perform the same well-known process. Indeed, the patents' independent claims follow the same pattern: a longwinded description of an FPGA

¹ Pet. for IPR (Paper 2), *Citadel Secs LLC v. HFT Solutions, LLC*, IPR2026-00151 (Dec. 3, 2025) (“’381 Petition”).

system that receives serial data, converts that data to parallel data streams, performs unspecified and unclaimed operations in computational circuitry, and then turns those parallel streams back into a serial stream. Where the '286 patent's claims differ, it is only by specifying which of the conventional components perform the steps of their materially identical methods. The claims describe the use of an external PLL that syncs the clocks with minimal latency. That's it. Each claim buries this well-known process under a mountain of words describing conventional components, but such verbosity does not change the simplicity—or prior existence—of what is claimed.

As described in the '381 Petition, no aspect of the challenged claims is new. The '286 patent makes the same claim as the '381 patent—that the use of a PLL external to the FPGA avoids the use of clock domain crossing circuits and therefore reduces unwanted latency. Yet, as noted in the '381 Petition, there is nothing new about using an *external* PLL. Years before both the '381 and '286 patents, Altera (a top FPGA manufacturer) gave skilled artisans a clear map to ensuring proper synchronization in an FPGA with a commonly used external PLL, which was all set out in a white paper—the prior art cited here. Ex. 1004. Altera therefore accomplished exactly what the '286 patent later claimed—an FPGA and external PLL system for synchronizing a receiver-side clock and transmitter-side clock such that clock-domain crossing circuitry was not needed, thus anticipating the majority

of the claims of the '286 patent. And as with the '381 patent, the use of such a system in financial instrument trading was known, as the patent itself recognizes: "FPGAs are used in the financial industry in high frequency trading where the rapid processing of the FPGA is desired." Ex. 1001 at 1:34-36.

For these reasons, as more fully detailed below, Citadel Securities requests institution of its IPR petition for claims 1, 2, 8, 10-11, and 19-20 of the '286 patent and the cancellation of all challenged claims as unpatentable.

II. MANDATORY NOTICES

A. Real Parties in Interest

Petitioner identifies itself, Citadel Securities LLC, as the real party-in-interest. Additionally, while Petitioner does not believe that the following entities must be disclosed as real parties-in-interest because these entities (or any of them) have not exercised control and could not have exercised control over Petitioner's participation in this IPR, out of an abundance of caution, Petitioner discloses the following entities as additional real parties-in-interest who will be bound by the outcome of this IPR to the same extent as Petitioner:

Citadel Securities GP LLC

Citadel Securities Holdings LP

CSIPTRS LP

Citadel Securities Global Holdings LLC

Citadel Securities Group LP

Citadel Securities Group Holdings LLC

CSHC US LLC

Citadel ENTP Services Group LLC

Citadel Enterprise Americas LLC

Citadel Enterprise Americas Services LLC

Citadel Securities Americas Services LLC

Citadel Securities Americas LLC

Board of Citadel Securities Group LP

B. Related Matters

Patent Owner has asserted the '286 patent in two actions currently pending in the United States District Court for the Northern District of Illinois and another action currently pending in the United States District Court for the Western District of Texas:

HFT Solutions, LLC v. Citadel Securities LLC, 1:24-cv-13213 (N.D. Ill.)

HFT Solutions, LLC v. Jump Trading, LLC, 1:24-cv-13214 (N.D. Ill.)

HFT Solutions, LLC v. Optiver US LLC, 7:25-cv-00415 (W.D. TEx.)

Petitioner also recently petitioned for *inter partes* review of another patent within the same family owned by Patent Owner. *See* '381 Petition. No decision has been rendered on that petition.

C. Identification of Counsel and Service Information

Petitioner designates the following counsel as Lead and Back-up Counsel. A power of attorney is filed concurrently with this petition.

Lead Counsel	Back-Up Counsel
Meg E. Fasulo Reg. No. 75,820 meg.fasulo@bartlitbeck.com Bartlit Beck LLP 54 West Hubbard Street, Suite 300 Chicago, IL 60654 Tel: (312) 494-4400 Fax: (312) 494-4440	Matthew R. Ford <i>Pro Hac Vice</i> pending matthew.ford@bartlitbeck.com Bartlit Beck LLP 54 West Hubbard Street, Suite 300 Chicago, IL 60654 Tel: (312) 494-4400 Fax: (312) 494-4440

Please direct all correspondence to the above counsel. Petitioner consents to electronic service to the follow addresses:

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III. REQUIREMENTS FOR REVIEW

Standing: Petitioner certifies under 37 C.F.R. § 42.104(a) that the '286 patent is eligible for inter partes review and that Petitioner is not barred or estopped from requesting inter partes review on the grounds set forth below.

Petitioner requests cancellation of the challenged claims under the following grounds:

Ground	Claims	Basis	References
1A	1, 2, 8, 10-11, and 19	§ 102	Altera
1B	1, 2, 8, 10-11, and 19	§ 103	Altera, Stratix Handbook, Si5345 Manual
2	1, 2, 8, 10-11, and 19-20	§ 103	Altera, Lockwood

IV. DISCRETIONARY DENIAL NOT WARRANTED

The Director should not exercise discretion to deny the present petition. The '286 patent issued less than five years ago (Feb. 23, 2021), and no forum has previously adjudicated the validity or patentability of the challenged claims. There is no basis for any settled expectation that the challenged claims are valid or enforceable.

HFT Solutions has asserted the '286 patent against Citadel Securities in the Northern District of Illinois. This co-pending district court case is in its infancy, with no trial date or other deadlines set and no discovery completed. Indeed, Patent Owner has yet to propound *any* discovery in that litigation, and thus investment in this parallel proceeding by the court and the parties is negligible. The early stage of the district court litigation also suggests that a stay may be granted if IPR is instituted. Overlap between the issues in the parallel proceeding and the issues raised in this petition is at most partial—for example, Citadel Securities intends to assert in the district court that the claims of the '286 patent are invalid under § 112.

The primary references relied on in this IPR were not before the patent examiner during prosecution. The Altera reference in particular was located by Citadel Securities' engineers, who are persons of at least ordinary skill in the relevant field, through a Google search using the terms "FPGA PLL synchronous ethernet," which returned the Altera white paper on the first page of search results. Altera was not art of record during prosecution, and the only non-patent database searched by the examiner was the IBM Technical Disclosure Bulletin (IBM_TDB), which does not contain Altera. The only non-patent literature in the prosecution history was identified by the applicant, and the prosecution history contains no rejections for anticipation or obviousness.

There are no economic, public health, or national security interests which favor denial. To the contrary, Citadel Securities is not controlled by any foreign entity, and economic interests favor institution. Patent owner HFT Solutions does not practice the challenged (or any) high-frequency trading patent. Rather, HFT seeks to stifle innovation in financial services by asserting patents that purport to claim known and regularly used hardware and techniques for high-frequency trading, which will disrupt well-established practices of Citadel Securities and other market participants in this space. Nor is Citadel Securities a serial petitioner—the only petition that Citadel Securities has filed is the co-pending petition relating to another HFT patent in the same family, relying on the same grounds.

Finally, as demonstrated below, the merits of this petition are strong. The challenged claims are nothing more than verbose, obfuscated recitations of known techniques for clock synchronization using FPGAs and external PLLs. And this petition's reliance on expert testimony is limited to a single expert declaration of approximately 135 pages. Even that lone declaration overlaps substantially with the declaration from the same expert in the co-pending petition for *inter partes* review challenging another HFT patent in this family. *See* '381 Petition.

V. SUMMARY OF THE PRIOR ART

The claims of the '286 patent take two well-known components (an FPGA and a PLL) and put them together in not only the exact the way they are designed to be combined, but as they have in fact been combined in prior art. By the time the '286 patent was filed, numerous FPGAs were commercially available. Ex. 1001 at 9:22-28; *see also* Ex. 1002 at ¶¶ 34-40. FPGAs are useful “in applications that require fast processing since FPGAs allow for all computations to occur on a single chip that has massive fine-grained parallelism,” including “in the financial industry in high frequency trading.” Ex. 1001 at 1:30-36. Likewise, numerous PLLs, a

component used to synchronize clock signals, were also available at the time the patent was filed. Ex. 1002 at ¶¶ 47-54.²

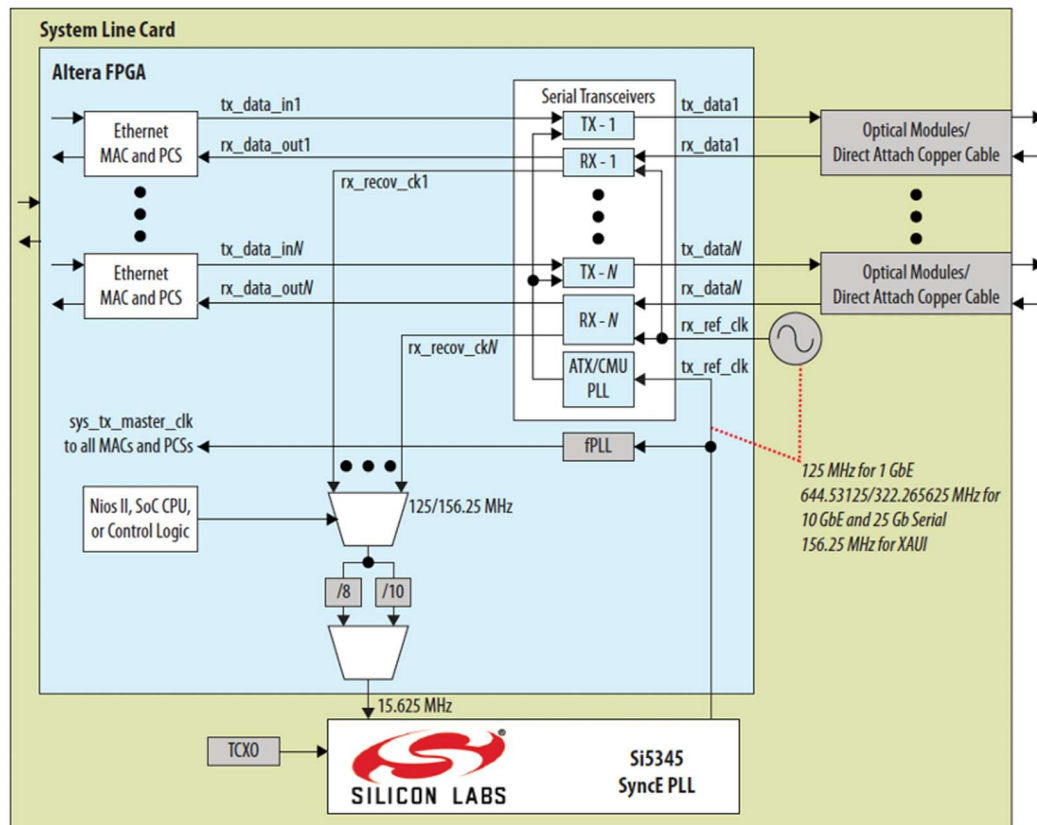
A. Altera

In November 2015, Altera Corporation published a white paper describing “a multiple-port 1G/10 Gbps Ethernet SyncE [Synchronous Ethernet] synchronization solution jointly developed by Altera and Silicon Labs, with a complete stable clock loop.” Ex. 1004 at 1. As the Altera white paper states, “[t]he solution consists of an Altera® SyncE reference design implementing up to ten 1G/10 Gbps Ethernet (1G/10GbE) ports in Altera’s Stratix® V FPGA interoperating with Silicon Labs’ Si5345 jitter-attenuating phase-locked loop (PLL) to provide a complete SyncE clock recovery, clock selection, and synchronization sub-system. This solution can be used in wireless or wireline networking equipment to realize an accurate SyncE clock synchronization.” *Id.* at 2. More simply, the Altera solution consisted of an off-the-shelf FPGA combined with an off-the-shelf external PLL for high-

² The Summary of the Prior Art is the same as the Summary of the Prior Art in the ’381 Petition. ’381 Petition at 8-20. To facilitate review of these petitions, Petitioner indicates in Ex. 1031 those sections of this petition that are the same as the ’381 Petition, including how the limitations of the ’286 patent correspond to those of the ’381 patent.

performance clock synchronization for use with Ethernet networking. The Altera system—using a Stratix FPGA and Si5345 PLL—is shown in Figure 1. Altera also describes test results using the Stratix FPGA and Si5345 system. *Id.* at 5-7; *see also* Ex. 1002 at ¶¶ 82-91.

Figure 1. High-Level Example of a SyncE System Line Card Using Altera FPGA and Silicon Labs SyncE PLL



Altera’s white paper is dated November 2015, and it was intended for dissemination to prospective customers and available for download from Altera’s website long before November 2018. Ex. 1004 at 1 (advising “Altera customers . . . to obtain the latest version of device specifications before relying on any published information and before placing orders for products or services”); Ex. 1009 at 4-5

(showing that the Altera White Paper was available online no later than October 18, 2016). Altera is therefore prior art under § 102(a)(1) (AIA) as a printed publication available before the effective filing date of the '286 patent (November 5, 2018). *Weber, Inc. v. Provisur Techs., Inc.*, 92 F.4th 1059, 1067 (Fed. Cir. 2024).

B. Stratix Handbook

The Stratix FPGA used in the Altera white paper is an off-the-shelf product sold by Altera (now an Intel company) before the effective filing date of the '286 patent. Numerous printed publications describe the FPGA's operation in detail. The Stratix Handbook—a lengthy reference manual published by Altera—is one such printed publication. Ex. 1005.

As relevant for the challenged claims, Volume 2 of the Stratix Handbook is intended to give “a complete understanding of Stratix® V transceivers,” which transmit and receive data and therefore make up a crucial component of an FPGA. *Id.* at 6. The Handbook begins by explaining the transceivers' operation at a high level: “Stratix V transceivers are divided into two blocks: physical medium attachment (PMA) and physical coding sublayer (PCS). The PMA block connects the FPGA to the channel, generates the required clocks, and converts the data from parallel to serial or serial to parallel. The PCS block performs digital processing logic between the PMA and the FPGA core.” *Id.* The Stratix Handbook has numerous accompanying block diagrams to further explain the operation of the receiver (RX)

and transmitter (TX) portions of the transceivers. *E.g., id.* at 14 (showing RX PMA and TX PMA in more detail); *see also* Ex. 1002 at ¶¶ 92-108.

PMA Architecture

The PMA receives and transmits off-chip high-speed serial data streams.

Figure 1-7: Receiver PMA Block Diagram

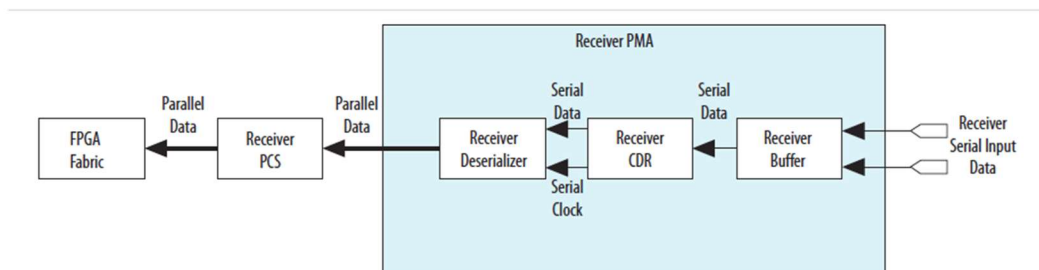
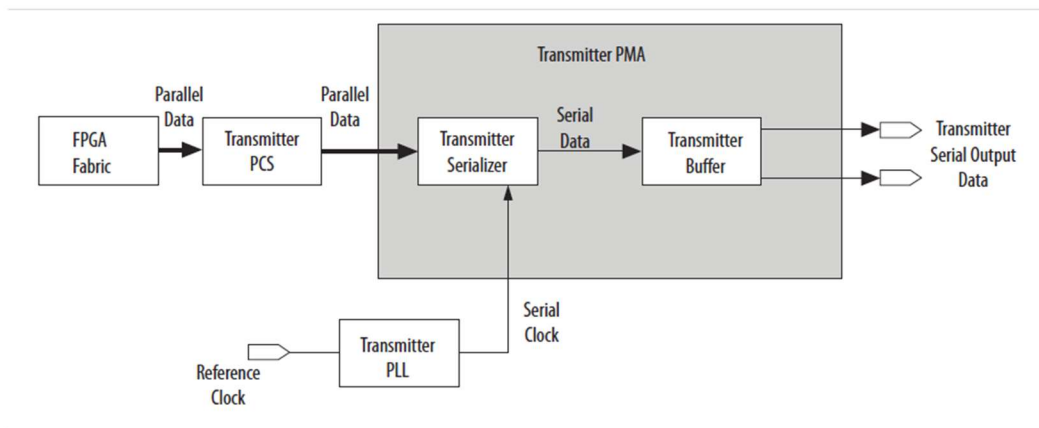


Figure 1-8: Transmitter PMA Block Diagram



The Stratix Handbook, dated January 23, 2015, was (and is) intended for dissemination to prospective customers and current users of the Stratix FPGA and was also available for download from Altera’s website long before November 2018. Ex. 1005 at 6 (encouraging “Altera customers . . . to obtain the latest version of device specifications before relying on any published information” in the Handbook); Ex. 1010 at 4-5 (showing that the Stratix Handbook was available

online no later than January 9, 2017). The Stratix Handbook is prior art under § 102(a)(1) (AIA) as a printed publication available before the effective filing date of the '286 patent (November 5, 2018). *Weber*, 92 F.4th at 1067.

The '286 patent concedes that the Stratix FPGA is prior art. Ex. 1001 at 9:22-28 (“Examples of currently available FPGAs include . . . the Stratix® V”). Although the examiner considered one page of the Stratix Device Handbook during prosecution, *id.* at 2, the primary Altera white paper that directs a skilled artisan to combine the Stratix FPGA with an external PLL was not art of record and therefore was not considered.

C. Si5345 Manual

The Si5345 PLL used in the Altera white paper is an off-the-shelf product sold by Silicon Labs (now Skyworks) before the effective filing date of the '286 patent. Like the Stratix FPGA, numerous printed publications describe in detail the operation of Silicon Labs PLLs. The Si5345 Manual is a Family Reference Manual that describes three “Any-frequency, Any-output Jitter-Attenuator/Clock Multipliers” made by Silicon Labs—specifically, the Si5345, Si5344, and Si5342. Ex. 1006 at 1. “This Family Reference Manual is intended to provide system, PCB design, signal integrity, and software engineers the necessary technical information to successfully use the Si5345/44/42 devices in end applications.” *Id.* at 9.

As the Si5345 Manual describes, “[t]he Si5345/44/42 jitter attenuating clock multipliers combine 4th generation DSPLL and MultiSynth™ technologies to enable any-frequency clock generation for applications that require the highest level of jitter performance.” *Id.* Simply put, the PLLs are designed to clean and distribute clocks in systems that require extremely low levels of jitter (i.e., variations of the timing of a clock signal) and are capable of generating any combination of output frequency from any input frequency within specified ranges. *Id.*

The three PLLs significantly overlap in their function, structure, and capability, with the differences primarily being in the numbers of MultiSynths and available outputs. *Id.* at 9. Figure 1 provides a block diagram for all three PLLs.

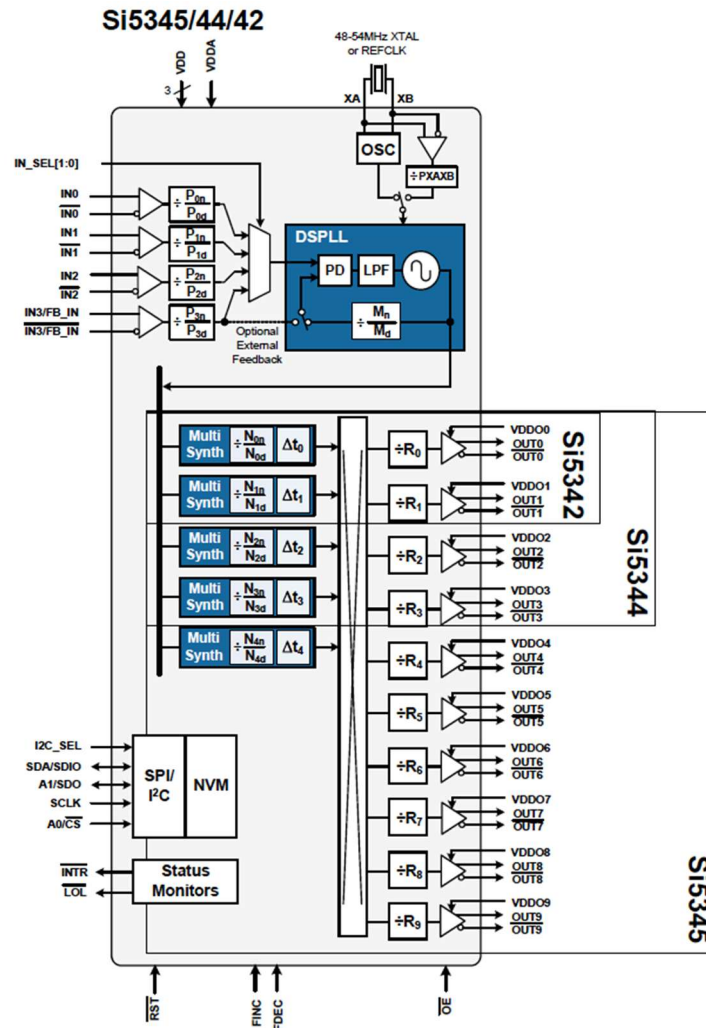
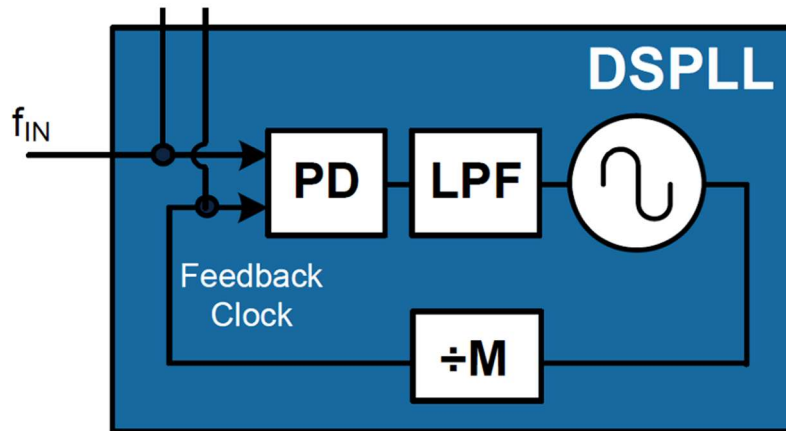


Figure 1. Block Diagram Si5345/44/42

Each PLL described in the Manual has a digital signal processor phase-locked loop (DSPLL, shown in blue box below) that includes a phase detector, a low pass filter, and voltage-controlled oscillator. *E.g.*, Ex. 1006 at 27. The DSPLL uses those components in an iterative process to synchronize an input clock to a reference clock. *Id.* at 17 (describing “Acquisition Mode”); *see also* Ex. 1002 at ¶¶ 109-112.



Si5345/44/42 Figure 13 Excerpt

The Si5345 Manual—dated August 2015—was created and published by Silicon Labs for dissemination to prospective and current customers. Ex. 1006 at 1 (“Rev. 1.0 8/15” and “Copyright© 2015”), 9 (“This Family Reference Manual is intended to provide . . . engineers the necessary technical information to successfully use the Si5345/44/42 devices in end applications.”), 183 (“Silicon Laboratories intends to provide customers with the latest, accurate, and in-depth documentation” and providing contact information). The Manual also directs readers to Silicon Labs’ website, where Silicon Labs made its data sheets and other information available for download. *Id.* at 183; Ex. 1011 at 4-5 (showing that Si5345/44/22 documentation was available online no later than November 22, 2015). Accordingly, the Si5345 Manual is prior art under § 102(a)(1) (AIA) as a printed publication available long before the effective filing date of the ’286 patent (November 5, 2018). *Weber*, 92 F.4th at 1067.

D. “A Low-Latency Library in FPGA Hardware for High-Frequency Trading (HFT)” by John W. Lockwood

As the '286 patent acknowledges, by 2018, it was common knowledge that FPGAs were being “used in the financial industry in high frequency trading where the rapid processing of the FPGA is desired.” Ex. 1001 at 1:34-36. Even as early as 2012, financial systems were implemented on FPGA-based systems. For example, John W. Lockwood’s 2012 paper describes the advantages of FPGA-based systems to reduce latency for high-frequency trading. Ex. 1007.

In his paper, Lockwood explained “why latency matters” in electronic trading, which was “growing rapidly” at the time of the 2012 publication. *Id.* at 2. Lockwood further explained that high frequency “traders attempt to exploit fleeting inefficiencies in the market. . . . However, due to the increase in number of players in the HFT space which try to exploit these opportunities, the first few players to execute orders may be the only ones able to profit from a given opportunity.” *Id.* “The longer the time between a trader making a decision to trade and the order reaching the execution venue, the greater is the possibility and magnitude of slippage which translates into cost for traders.” *Id.* Lockwood also noted that some trading strategies “depend upon the ability to access market data and execute orders faster than other investors. Profiting from this activity requires traders to be able to react in real time to market events using both low-latency and low-jitter market access.” *Id.* Every “reduction in latency can improve arbitrage profitability.” *Id.*

Lockwood provided examples of how such systems could be implemented, including using an FPGA-based system to act “as the bridge between the host computer and the network,” which “allows user-designed custom processing logic to be integrated directly into the data path.” *Id.* at 3. Specifically, market data from an exchange enters the FPGA system, where it is processed in the FPGA to result in orders back to the market. The system is shown in Figure 2 of Lockwood:

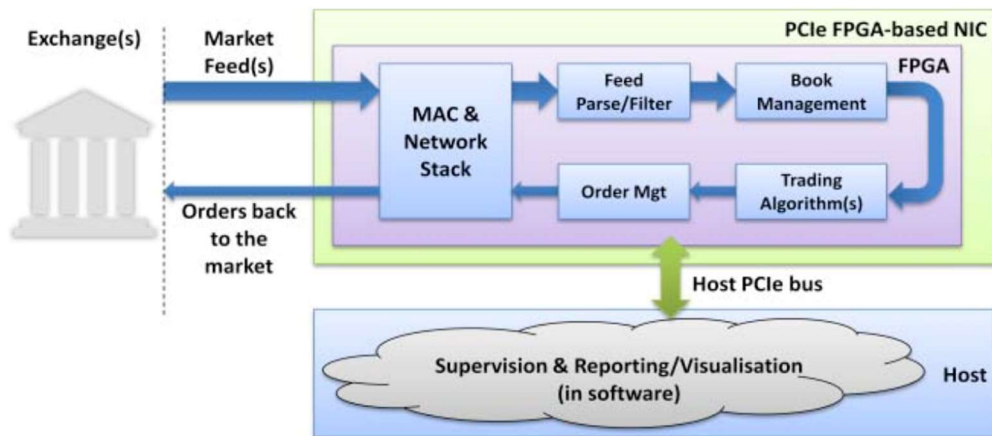


Figure 2 Typical Smart NIC in a supervised financial trading application

Lockwood further explained that “some financial processing systems are completely implemented on FPGA-based platforms without any host CPU,” which “yield[s] best possible latencies.” In this implementation, the data “no longer needs to make a round trip” through system’s interface for processing in the CPU, so “the inherent latency and jitter introduced by the host’s operating system are entirely avoided.” Ex. 1007 at 3. Such as system is shown in the bottom portion of Figure 3.

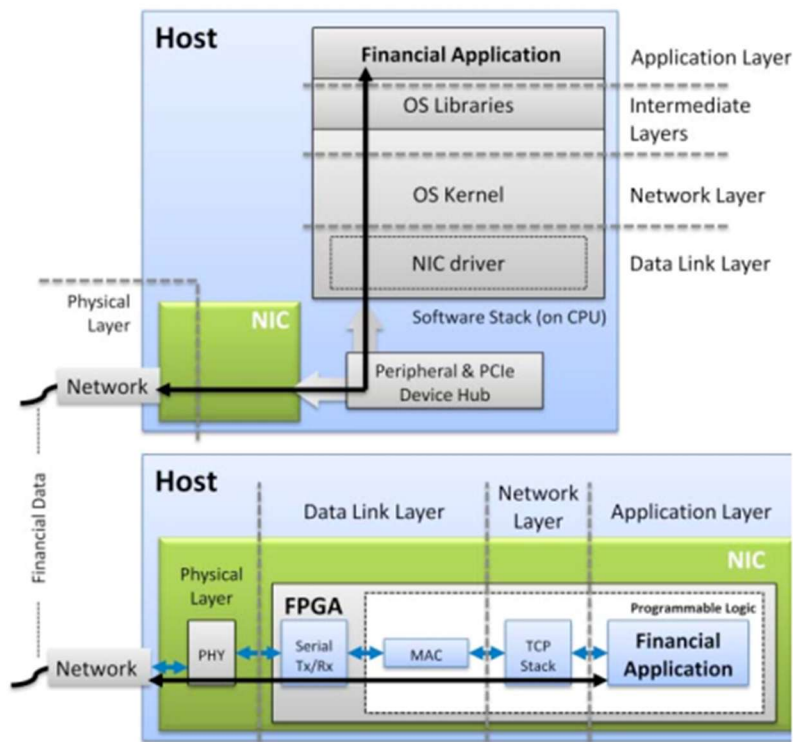


Figure 3 Software-based (top) and FPGA-based (bottom) trading platforms

Lockwood described numerous advantages to using FPGAs for high-frequency trading. For example, “[m]odern FPGAs can implement most aspects of any HFT trading application,” such that “[i]ncoming market data can typically be processed completely on the FPGA without needing to travel over and back to a host CPU.” *Id.* Additionally, “in the FPGA implementation, the incoming network data is fed directly into a custom-designed, highly-optimized and application-specific processing pipeline via hardware PHY [Physical] and MAC [Media Access Control] blocks.” *Id.* at 4 (referring to the “Serial Tx/Rx” and “MAC” blocks in Figure 3). “Along with lower latency and minimal jitter, FPGAs can achieve significantly

higher throughput using parallelism,” due to the FPGA’s ability to perform many operations simultaneously. *Id.* And “FPGAs offer the[se] performances benefits of custom hardware while retaining programmability” so that “[t]rading algorithms” implemented on the FPGAs “can be continually improved.” *Id.*; *see also* Ex. 1002 at ¶¶ 113-116.

Lockwood is prior art under § 102(a)(1) (AIA) as a printed publication available before the effective filing date of the ’286 patent. Lockwood was published in September 2012 and is available for download at <https://doi.org/10.1109/HOTI.2012.15>.

VI. THE ’286 PATENT

A. Effective Filing Date

The ’286 patent issued on February 23, 2021 from an application filed on July 30, 2020. The ’286 patent is a continuation of a previous application. The ’286 patent also claims priority to two provisional applications, the earliest of which was filed on November 5, 2018. For the purposes of this IPR, Petitioner treats November 5, 2018 as the earliest effective filing date.

B. Specification

The purported invention of the '286 patent is a field programmable gate array with an external phase-locked loop.³ Ex. 1001 at 1. But both FPGAs and PLLs were developed well before November 2018. The '286 patent acknowledges that it was known that “FPGAs[] may be used in applications that require fast processing since FPGAs allow for all computations to occur on a single chip that has massive fine-grained parallelism.” Ex. 1001 at 1:31-34. Indeed, the '286 patent concedes that, at the time of the invention, FPGAs were already being “used in the financial industry in high frequency trading,” *id.* at 1:34-36, and discloses that numerous FPGAs were commercially available, including “XCVU3P-2FFVC1517E, Intel 1SG280LH3F55E3VG, Xilinx XCVU9P-2FLGA2104E the Vitrex® [sic] Ultrascale, the Vitrex® [sic] Ultrascale Plus, the Stratix® V, the Stratix® 10, XILINX XC3042, the Intel EP4CE6E22C8LN and the Lattice ICE40LP384-SG32, to name a few,” *id.* at 9:22-28.

The '286 patent contends that it solves “a technical problem [] presented in FPGAs in that phase synchronization between the receiver side clock and the

³ The '286 patent shares a specification with the '381 patent. Ex. 1001; '381 Petition. As a result, the discussion here is the same as the discussion in the co-pending '381 Petition. '381 Petition at 20-22.

transmitter side clock will introduce unwanted latency that result in delay of processing.” Ex. 1001 at 1:46-49. According to the patent, “[t]he prior art sought to address this problem by including a clock domain crossing circuit in the FPGA.” *Id.* at 1:39-41. Rather than use a clock-domain crossing circuit, the ’286 patent addresses that concern with “a field programmable gate array and an external phase controller providing phase matching between a receiver clock and a transmitter clock used in the field programmable gate array.” *Id.* at 1:67-2:3. But as detailed below, there is nothing novel or nonobvious about using an external PLL to provide phase matching for an FPGA.

C. Challenged Claims

The ’286 patent contains twenty-two claims, six of which are challenged in this IPR. The challenged claims of the ’286 patent are unnecessarily long, but their length belies their simplicity. They are also materially the same as the claims in the ’381 patent, which is the subject of a co-pending IPR petition.

At a high level, the ’286 patent claims methods for using a field programmable gate array (FPGA) that receives serial data, converts it to parallel data, syncs the internal clock to the received data, performs certain calculations, and then converts the stream back to serial before transmission of data off the FPGA.

The ’286 patent has one independent method claim that incorporates more than twenty subparts. These subparts consist of several structural limitations

(interfaces, pins, deserializer, circuitry, phase detector, oscillator, phase controller, and serializer) and data limitations (data streams, clock signals, and output).

D. Prosecution History

The prosecution of the '286 patent was brief and uneventful. Patent Owner submitted the application on July 23, 2020, as a continuation of U.S. Pat. Appl. No. 16/672,076 (now U.S. Pat. No. 10,826,502) and claiming priority from two provisional applications (No. 62/803,017, filed on Feb. 8, 2019; and provisional application No. 62/755,804, filed on Nov. 5, 2018). Ex. 1003 at 100-102.

The Examiner performed a search and issued a Notice of Allowance in the first office action on November 2, 2020. Ex. 1003 at 27, 47. The Examiner's reasons for allowance identified the generation of a second clock signal using componentry that was external to the FPGA, as defined in limitations 1(h)-(i) (when combined with the other limitations). Ex. 1003 at 27-34. About a year later, Patent Owner requested a post-issuance Certificate of Correction to claim 1 for three "typographical errors," which the Patent Office issued on November 23, 2021. Ex. 1003 at 1.

E. Level of Ordinary Skill

At the time of the claimed invention, a POSA would have a bachelor's degree in electrical or computer engineering and 3-5 years of academic or industry experience working with clocking techniques for FPGAs with high-speed

transceivers.⁴ Ex. 1002 at ¶¶ 31-32. This person could also be someone with a lower degree of education but with greater practical experience. It could also be someone with a higher degree of education and lower practical experience.

F. HFT's Theory of Infringing the '286 Patent

Patent Owner's infringement theory in the district court bears directly on why the Petitioner's cited prior art discloses each limitation in the challenged claims. Ex. 1012.⁵

First, Patent Owner accuses systems that include a Xilinx Ultrascale+ FPGA, which is an off-the-shelf FPGA sold by a third party. That is the same type of product as the Altera FPGA that Petitioner cites as the primary reference.

Second, Patent Owner accuses systems that include an external Si5346 Phase-Locked Loop (PLL). As discussed *infra*, a PLL synchronizes clock signals for use with the FPGA. The accused Si5346 PLL is an off-the-shelf PLL that is closely related to the Si5345 PLL used in this petition. In relevant respects, the Si5346 shares architecture and componentry with the Si5345 PLL, the prior-art reference Petitioner

⁴ Petitioner's proposed level of ordinary skill in the art is the same as what is proposed in the '381 Petition. '381 Petition at 23.

⁵ HFT's theory of infringing the '286 patent is materially the same as the corresponding discussion in the '381 Petition. '381 Petition at 24-25.

cites with respect to claim 1(g) and claim 8. *E.g.*, Ex. 1012 at 9 (citing UltraScale+), 17 (citing Si5346).

Petitioner recognizes that Patent Owner’s infringement theories do not resolve the question of patentability or claim construction for an inter partes review. But the constructions implicit in the Patent Owner’s infringement allegations ought to be considered when evaluating the elements of the prior art that disclose the recited limitations, and Petitioner adopts those implicit constructions here. *Cf. W. Digital Corp. v. Spex Techs., Inc.*, No. IPR2018-00084, 2018 WL 1990268, at *5 (PTAB Apr. 25, 2018) (“Petitioner’s statement that its Petition ‘is based on the claim constructions urged by Patent Owner’ in related District Court litigation . . . suffices to identify claim constructions Petitioner is adopting for purposes of the requested review in compliance with § 104(b)(3).”). Where appropriate, Petitioner indicates where the Patent Owner’s implied constructions relate to the disclosures in the prior art.

VII. CLAIM CONSTRUCTION

Without conceding that the ’286 patent’s claims are supported under 35 U.S.C. § 112, for the purposes of this IPR, Petitioner interprets the claims “in

accordance with the ordinary and customary meaning . . . as understood by one of ordinary skill in the art.” 37 C.F.R. § 42.100(b).⁶

Where the challenged claims refer to a “deserializer,” Petitioner adopts the specification’s description that the deserializer may include a receiver PMA and receiver PCS. Ex. 1002 at ¶¶ 75-80; Ex. 1001 at Figs. 3A-E, 17:25-17:48. This is consistent with the construction that the Patent Owner has implicitly adopted in its infringement contentions before the district court. Ex. 1012 at 11-17.

Likewise, where the challenged claims refer to a “serializer,” Petitioner adopts the specification’s description that the serializer may include a transmitter PCS, a transmitter PMA, a transmitter buffer, clock generation blocks, and clock dividers. Ex. 1001 at Figs. 4A-B; 17:52-18:21. This is consistent with the construction that the Patent Owner has implicitly adopted in its infringement contentions before the district court. Ex. 1012 at 22-25.

VIII. THE CHALLENGED CLAIMS ARE UNPATENTABLE

As with the ’286 Patent, the ’381 patent claims nothing other than the conventional use of an FPGA with an external PLL. Altera taught that use years before Patent Owner filed its application, and FPGAs had been used in financial

⁶ Petitioner’s claim construction arguments are the same as those raised in the ’381 Petition. ’381 Petition at 25-26.

applications for even longer. For the reasons that follow, those claims are unpatentable.

A. Ground 1A: Altera Anticipates Claims 1, 2, 8, 10-11, and 19

Altera—a white paper published by a leading FPGA manufacturer—instructs using a Stratix FPGA in conjunction with an external Si5345 PLL for clock synchronization. Altera therefore anticipates claims 1, 2, 8, 10-11, and 19.⁷

1. A Skilled Artisan Would Recognize that the Features of the Stratix FPGA and Si5345 PLL Are Necessarily Present in Altera

Altera is a white paper that describes the operation of “a high-performance SyncE solution based on . . . Altera’s Stratix® V FPGA interoperating with Silicon Labs’ Si5345 jitter-attenuating phase-locked loop (PLL).”⁸ Ex. 1004 at 2. Altera provides both a “SyncE reference design” and a test setup for “interoperability” between the Stratix FPGA and Si5345 PLL. Ex. 1004 at 3, 5. A POSA reading Altera

⁷ The only limitation in claim 1 that Altera does not anticipate is claim 1’s preamble. As discussed below, claim 1’s preamble is not limiting and therefore Altera discloses every limitation in claim 1. But if the Board finds that the preamble to claim 1 is limiting, Altera and Lockwood together disclose the preamble, as discussed in Ground 2. *See infra* at VIII.C.

⁸ The arguments in this section are materially the same as the corresponding section in the ’381 Petition. ’381 Petition at 27-29.

would understand that the features of the Stratix FPGA and Si5345 PLL are necessarily present in the solution described in Altera. Ex. 1002 at ¶ 118. The white paper assumes that the reader can and will locate any information about the operation of the FPGA and PLL separately and so does not describe in depth every aspect of their operation. *Id.*

In this situation, it is proper to turn to extrinsic evidence that describes the operation of each of the referenced components in detail to understand their inherent features.

“[R]ecourse to extrinsic evidence is proper to determine whether a feature, while not explicitly discussed, is necessarily present in a reference. The evidence must make clear that the missing feature is necessarily present, and that it would be so recognized by persons of ordinary skill in the relevant art.” *Telemac Cellular Corp. v. Topp Telecom, Inc.*, 247 F.3d 1316, 1328 (Fed. Cir. 2001) (internal citations omitted); *see also In re Haines*, No. 2024-2338, 2025 WL 1403578, at *2 (Fed. Cir. May 15, 2025) (examiner properly used another publication “as evidence to explain why [the prior art’s] disclosure of a mass spectrometer implicitly discloses ‘obtaining mass spectral channel signals (m/z)’” (cleaned up)); *Sage Prods., LLC v. Stewart*, 133 F.4th 1376, 1385 (Fed. Cir. 2025) (“There was likewise nothing improper in the Board relying on evidence outside of the PAR to make findings as to what the skilled artisan would understand the PAR to be disclosing.”); *Monsanto*

Tech. LLC v. E.I. DuPont de Nemours & Co., 878 F.3d 1336, 1345 (Fed. Cir. 2018) (“It is well established that such reliance on extrinsic evidence is proper in an inherency analysis.”).

Here, the Altera FPGA and Si5345 are explicitly referenced, and a POSA would be intimately familiar with the fact that if they wanted to learn more about either, they would easily be able to find and rely on extensive information about those devices available from Altera and Silicon Labs. Ex. 1002 at ¶ 119. In fact, the Altera white paper encourages customers “to obtain the latest version of device specifications before relying on any published information.” Ex. 1004 at 1. Altera and Silicon Labs made specifications and data sheets available for download from their respective websites, including the Stratix Handbook and Si5345 Manual used here. Ex. 1002 at ¶ 119; Ex. 1010; Ex. 1011. The ’286 patent even provides a URL for the Stratix Handbook. Ex. 1001 at 2.

Accordingly, the Stratix Handbook and Si5345 Manual demonstrate features that a skilled artisan would understand are necessarily present in the FPGA and PLL used in the Altera white paper, and it is proper to use them to explain why the Altera white paper is anticipatory.

2. Limitation-By-Limitation Analysis

The preamble is not limiting, but if it is, Altera and Lockwood disclose it

Claim 1's preamble is not limiting. Claim 1's preamble only describes an intended use for the claimed method, and therefore it does not limit the scope of the claims. As a rule, language in the preamble is not limiting unless it recites essential steps or gives life, meaning, and vitality to the claims. *Symantec Corp. v. Computer Assocs. Int'l, Inc.*, 522 F.3d 1279, 1288 (Fed. Cir. 2008); *Schumer v. Lab'y Computer Sys., Inc.*, 308 F.3d 1304, 1310 (Fed. Cir. 2002). But where the body of the claim describes a complete invention, "[p]reamble language that merely states the purpose or intended use of an invention is generally not treated as limiting the scope of the claim." *FMC Corp. v. Sharda USA, LLC*, 145 F.4th 1326, 1334 (Fed. Cir. 2025).

Claim 1's preamble says that the claimed invention could be used with serial "market data" and "order entry data." Ex. 1001 at 28:9-13. The preamble contains the only mention of market or order-entry data in the claim, so the terms do not provide any antecedent basis for remaining limitations. And the preamble does not provide any additional structure to the claim, which operates on serial data streams without regard to the nature of the data, whether market/order data or information about the weather.

The patent’s written description confirms that the FPGA system—and not the type of data it processed—was the invention. The Background section describes limitations with prior-art FPGA processing that are agnostic as to the type of information that is processed. Ex. 1001 at 1:31-55. The Summary of the Invention similarly says that the object of the invention is to “address technological challenges that currently exist in phase matching receiver side and transmitter side clocks of a FPGA without introducing unnecessary delay in processing.” *Id.* at 1:59-62. Using that system for market or order-entry data is not the invention—it is one embodiment among many. *Id.* at 4:35-38.

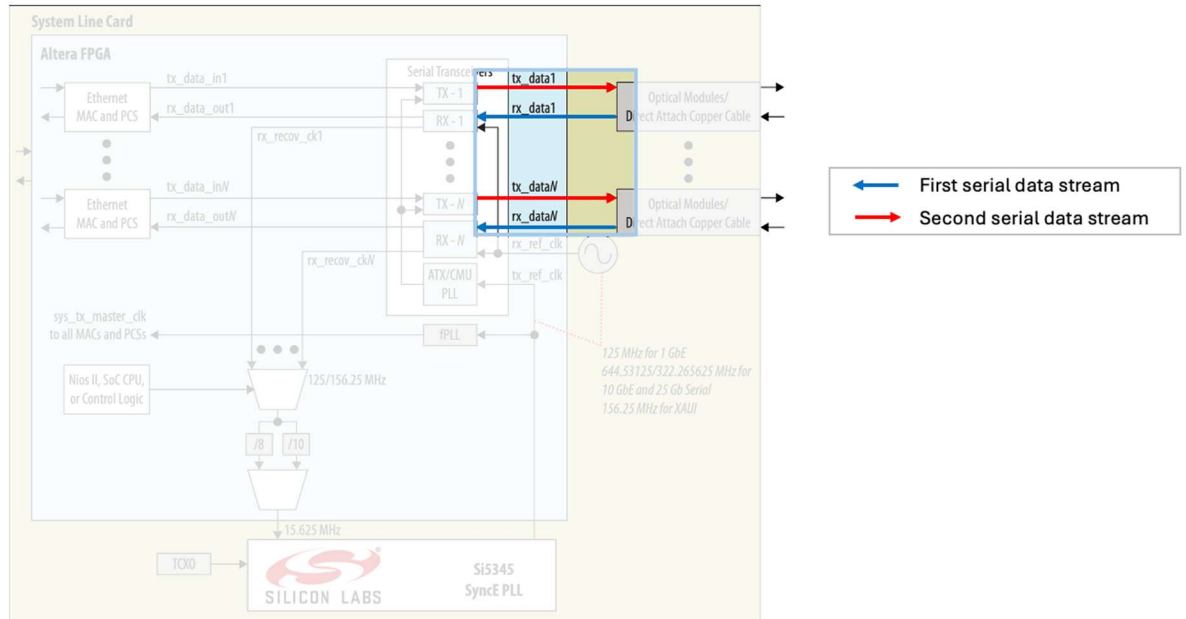
The claims also show that the preamble describes a potential use, and does not inform or direct the structure of the claimed method. Dependent claim 20 recites the same intended use as is set forth in the preamble, replacing “order entry data” with the broader term “trading data.” *Id.* at 30:32-34. Claim 20 would have no limiting effect if claim 1’s preamble narrowed the scope of the claimed method to only order data even though dependent claim 20 is broader. *Neapco Drivelines LLC v. Am. Axle & Mfg., Inc.*, 847 F. App’x 856, 858 (Fed. Cir. 2021) (“That claim 6 requires venting to ‘the driveshaft’ shows Neapco knew how to recite the vent destination more narrowly, which suggests the broader language in claim 11 was intentional.”). The preamble “states only an intended use, adds no structural element, and provides no

antecedent basis for the body of the claims, [and therefore] is not limiting.” *Cochlear Bone Anchored Sols. AB v. Oticon Med. AB*, 958 F.3d 1348, 1355 (Fed. Cir. 2020).

If Claim 1’s preamble is limiting, Altera discloses the first and second serial data streams. To the extent that the preamble is limiting, Altera discloses a “method for processing a first serial data stream . . ., using a field programmable gate array system, to generate a second serial data stream” Ex. 1002 at ¶¶ 121-124.

Altera is a system using “Altera’s Stratix® V FPGA interoperating with Silicon Labs’ Si5345 jitter-attenuating phase-locked loop (PLL) to provide a complete SyncE clock recovery, clock selection, and synchronization sub-system.” Ex. 1004 at 2. In Altera, first serial data streams (rx_data1-rx_dataN) are received by the system and second serial data streams (tx_data1-tx_dataN) are generated and transmitted by the system. The system is designed for wireless or wireline networking, *id.*, indicating that the received data is processed for those networking applications. Ex. 1002 at ¶ 122. Altera Figure 1, shown below, is annotated throughout this petition.

Figure 1. High-Level Example of a SyncE System Line Card Using Altera FPGA and Silicon Labs SyncE PLL



Altera and Lockwood disclose the market and order-entry-data limitations. If claim 1’s preamble is limiting, the combination of Altera and Lockwood render the preamble obvious, as discussed in Ground 2. *See infra* at VIII.C. For the same reasons described there, Lockwood discloses the market and order-entry-data limitations and a person of ordinary skill in the art would be motivated to combine Altera and Lockwood with an expectation of success.

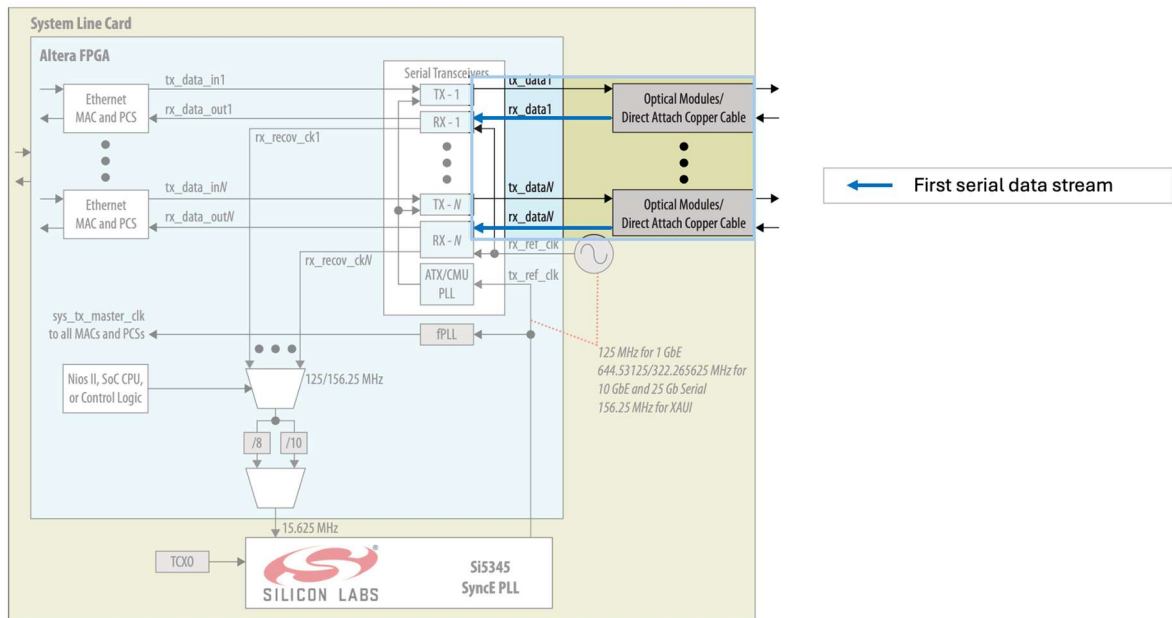
Claim 1(a)

Altera discloses “receiving, by a first plurality of data pins in a first interface of a field programmable gate array in the field programmable gate array system, the first serial data stream.” Ex. 1002 at ¶¶ 125-127.

Altera discloses that the receivers (RX-1 through RX-N) in the Serial Transceivers receive serial data (rx_data1-rx_dataN) from Optical Modules/Direct Attach Copper Cables. Ex. 1004 at 2. The “serial” nomenclature indicates that the serial transceiver receives serial data. Ex. 1002 at ¶ 126.

Altera therefore discloses the *first* serial data stream, which is reflected as rx_data1, passing into the FPGA’s serial transceivers from the Optical Modules/Direct Attach Copper Cable physical media.

Figure 1. High-Level Example of a SyncE System Line Card Using Altera FPGA and Silicon Labs SyncE PLL



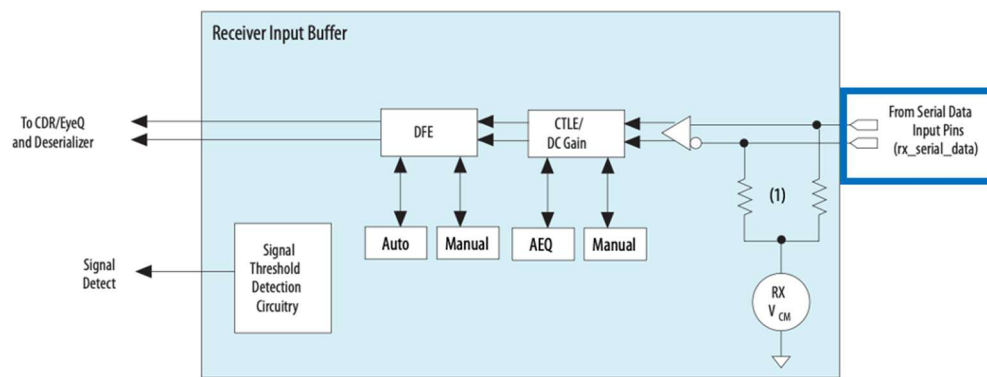
As part of that reception, the first serial data stream is received by physical data pins in the first interface of the FPGA.

The Stratix Handbook confirms this. It depicts that the serial data stream is received via multiple data pins. As seen in Figure 1-9 below, the Stratix architecture groups data pins into pairs, and there are multiple pairs of data pins, each

corresponding to a rx_data stream depicted in Altera Figure 1 above (e.g., rx_data1, rx_data2). Accordingly, the multiple pins associated with rx_data1 constitute a first plurality of data pins that receive the first serial data stream. Ex. 1005 at 6-15. Although not specifically labeled, a person of skill would understand that the data pins are part of an FPGA interface, a means of communicating with and/or is physically connection to devices external to the FPGA. Ex. 1002 at ¶ 127.

Figure 1-9: Receiver Input Buffer

Stratix V GT channels do not support AEQ and DFE.



Note:

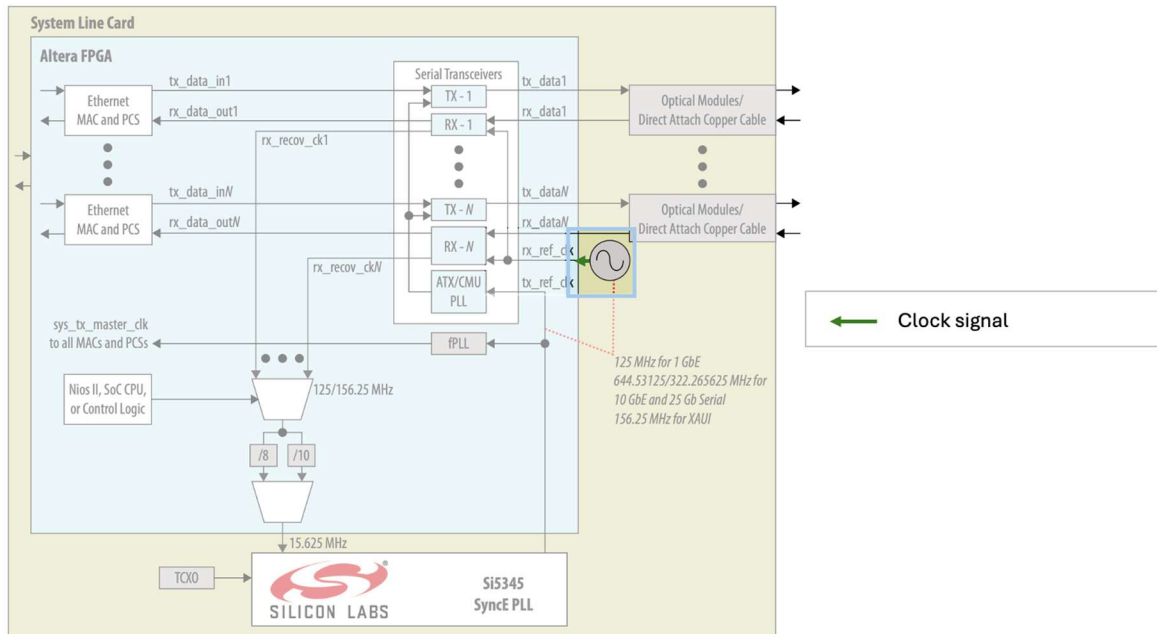
1. For Stratix V GX channels, the available options are OFF, 85, 100, 120, and 150 Ω . Stratix V GT channels only support 100 Ω .

Claim 1(b)

Altera discloses “receiving, by a first reference clock pin in the first interface, a first clock signal having a first frequency and a first phase.” Ex. 1002 at ¶¶ 128-129. Altera depicts the first serial clock signal (rx_ref_clk) passing into the FPGA’s serial transceivers from an external clock source. To pass into the FPGA system from the external clock source, a person of skill in the art would understand

that the clock signal passes through a dedicated physical I/O pin that is distinct from the pins that receive serial data. *Id.* at ¶ 129.

Figure 1. High-Level Example of a SyncE System Line Card Using Altera FPGA and Silicon Labs SyncE PLL

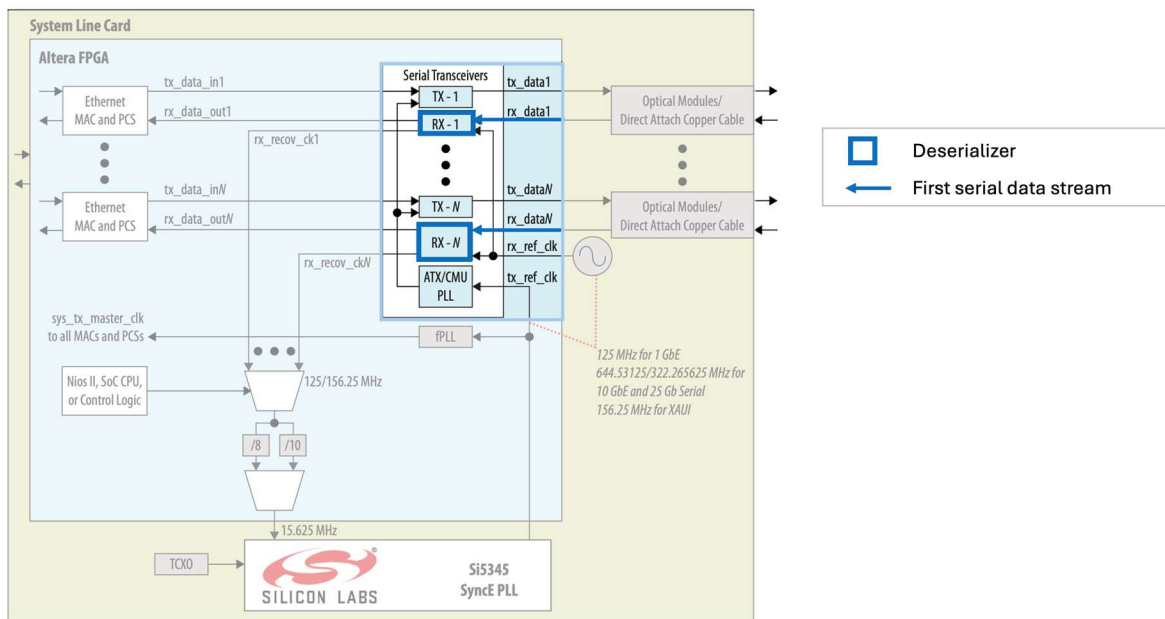


Claim 1(c)

Altera discloses “transmitting, from the first plurality of data pins in the first interface to a deserializer in the field programmable gate array, the first serial data stream.” Ex. 1002 at ¶¶ 130-133. Altera discloses a first serial data stream (e.g., rx_data1 through rx_dataN) that is transmitted from the serial data input pins of the Optical Modules/Direct Attach Copper Cables to receiver blocks (e.g., RX-1 through RX-N) of the serial transceivers (i.e., deserializers). Ex. 1004 at 2. The “serial” nomenclature indicates that the serial transceiver receives serial data that is transmitted through the data pins. Ex. 1002 at ¶ 131.

Altera therefore discloses a first serial data stream (e.g., rx_data1) that is transmitted from the serial data input pins to receiver blocks (i.e., RX-1) of the Serial Transceivers (i.e., a deserializer).

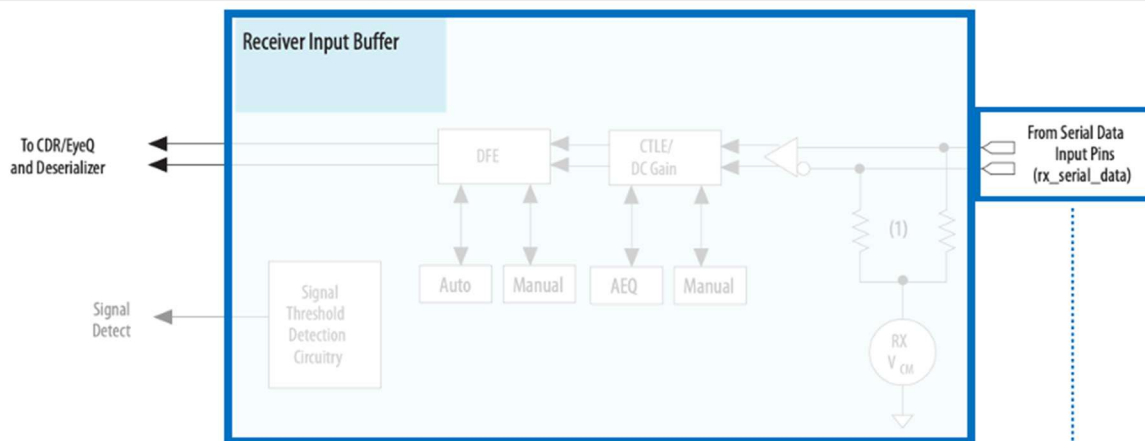
Figure 1. High-Level Example of a SyncE System Line Card Using Altera FPGA and Silicon Labs SyncE PLL



As part of this transmission to the receiver blocks, rx_data1 through rx_dataN pass from the serial data input pins to the receiver buffer, which in turn is a part of the receiver blocks (RX1-RX-N) within the deserializer. Ex. 1005 at 14-15.

Figure 1-9: Receiver Input Buffer

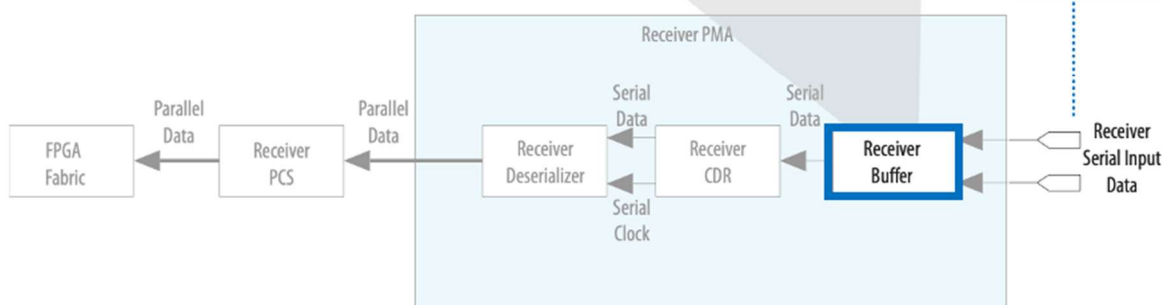
Stratix V GT channels do not support AEQ and DFE.



Note:

1. For Stratix V GX channels, the available options are OFF, 85, 100, 120, and 150 Ω . Stratix V GT channels only support 100 Ω .

Figure 1-7: Receiver PMA Block Diagram



The deserializer in claim 1(c) is represented by the receiver blocks (RX-1 through RX-N) and the receiver portion of the Ethernet MAC and PCS blocks shown in Altera. Ex. 1002 at ¶ 133. Altera's Figure 1-7 depicts the components that comprise the receiver blocks RX-1 to RX-N. The '286 patent demonstrates that the claimed deserializer can include a receiver PMA and receiver PCS, as shown in Figure 3E below. *E.g.*, Ex. 1001 at 17:26-29 ("the deserializer 2104" may include a receiver PMA 3512 and receiver PCS 3508. The receiver PMA 3512 may include

receiver buffer 3504, CDR 3516, and serial to parallel box 3118’.”); Fig. 3E. Like the ’286 patent, each receiver of Altera includes a receiver PMA and a receiver PCS. Ex. 1005 at 14.

Figure 1-7: Receiver PMA Block Diagram

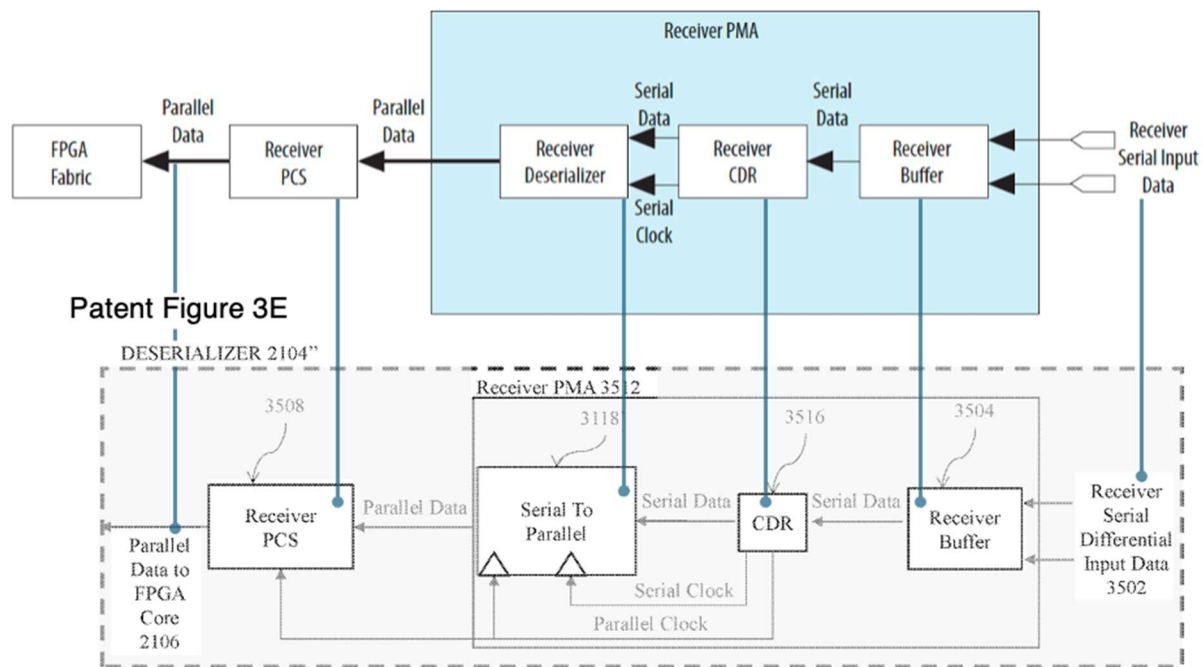
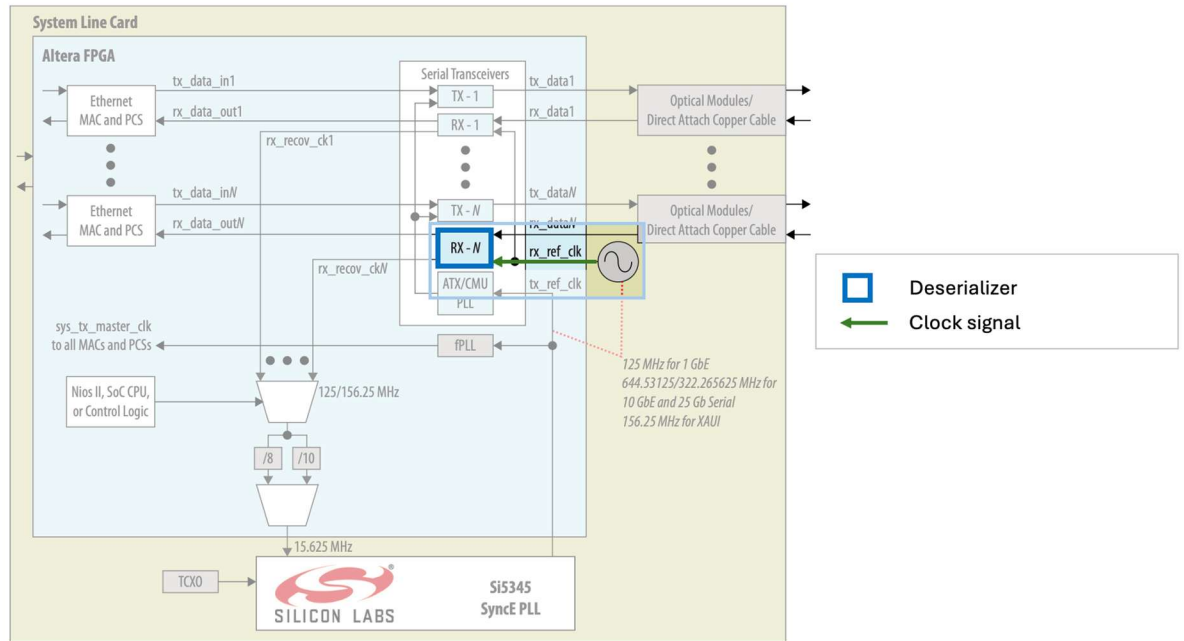


FIG. 3E

Claim 1(d)

Altera discloses “providing, from the first reference clock pin in the first interface to the deserializer, a clock signal based at least on the first clock signal.” Ex. 1002 at ¶¶ 134-138. As discussed in the preceding sections, rx_ref_clk passes into the FPGA through a clock pin. *Id.* at ¶ 135. From the clock pin, Altera depicts the rx_ref_clk clock signal passing into RX-1 through RX-*N* receiver blocks. Ex. 1004 at 2.

Figure 1. High-Level Example of a SyncE System Line Card Using Altera FPGA and Silicon Labs SyncE PLL

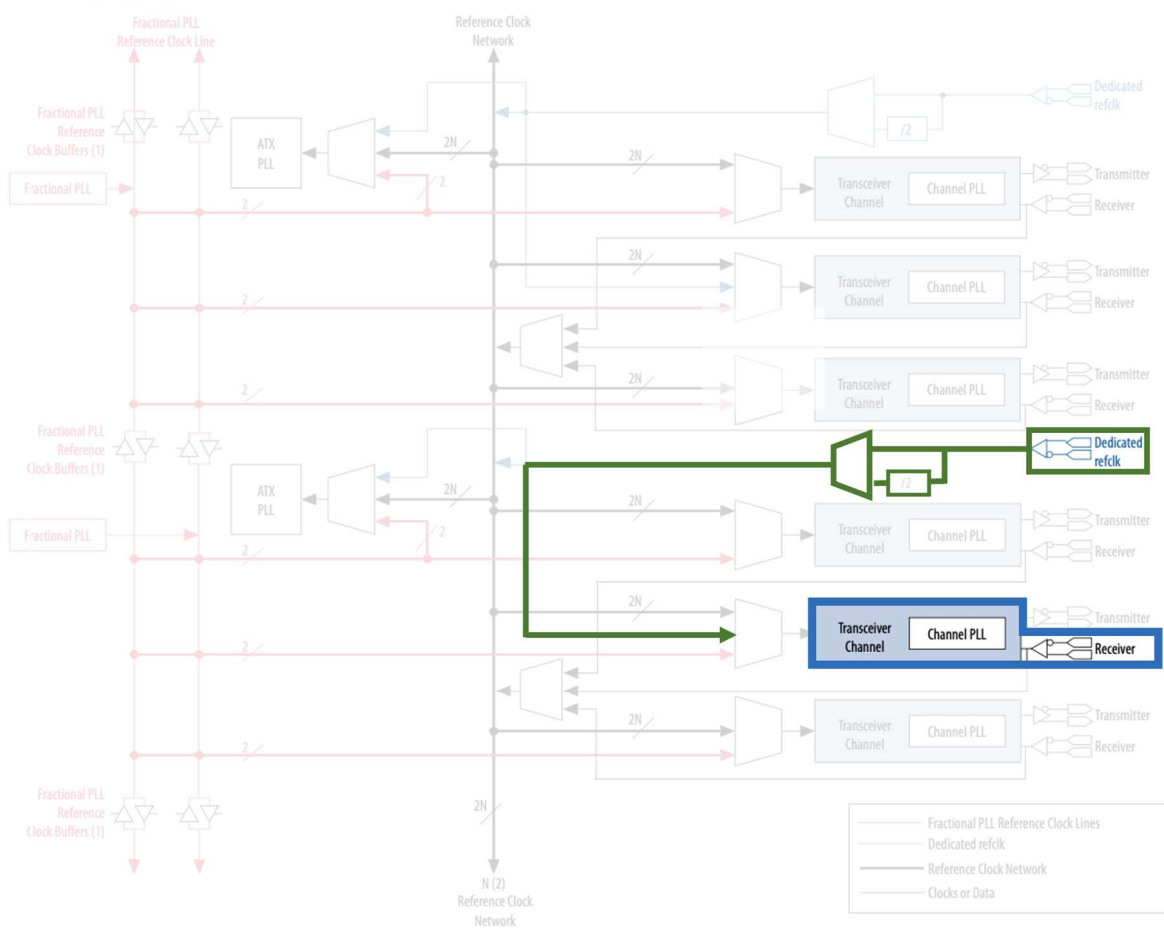


As disclosed in the Stratix Handbook, after the clock signal rx_ref_clk identified in Altera passes through the clock pin and, before it reaches the receiver block, it passes through multiplexers, the clock network, and clock dividers. Ex. 1005 at 71. As a result, the clock signal that reaches the receiver block is a clock signal based on the clock signal that passes through the clock pin.

Claim 1(d) does not specify the precise clock path that the clock signal must follow, and the Stratix Handbook depicts several, all of which disclose this limitation. The annotated figure below from the Stratix Handbook depicts one clock path going to the transceiver without passing through the Reference Clock Network (RCN). Ex. 1005 at 71; Ex. 1002 at ¶ 137. There are other clock-signal paths as well, such as through the Reference Clock Network.

Figure 2-3: Input Reference Clock Sources for GX Transceiver Channels

For more information about the fractional PLL input clock sources shown in the following figure, refer to **Figure 2-6**.

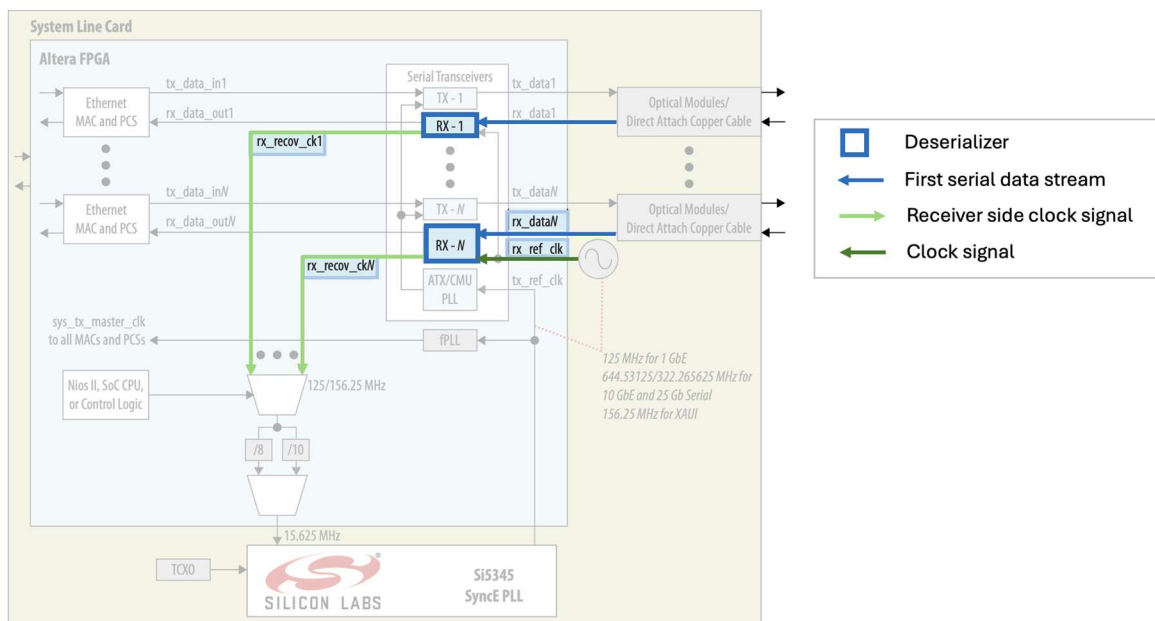


Claim 1(e)

Altera discloses “generating, by the deserializer, a first receiver side clock signal having a second frequency and a second phase, based at least in part on the first clock signal.” Ex. 1002 at ¶¶ 139-142. In Altera, the “PHY IP cores recover the receiver (RX) clocks from their respective 1G/10G Gbps Ethernet ports.” Ex. 1004 at 3. The PHY IP core refers to the serial transceivers—specifically, the PHY IP core is the “physical coding sublayer (PCS) and physical medium attachment (PMA)

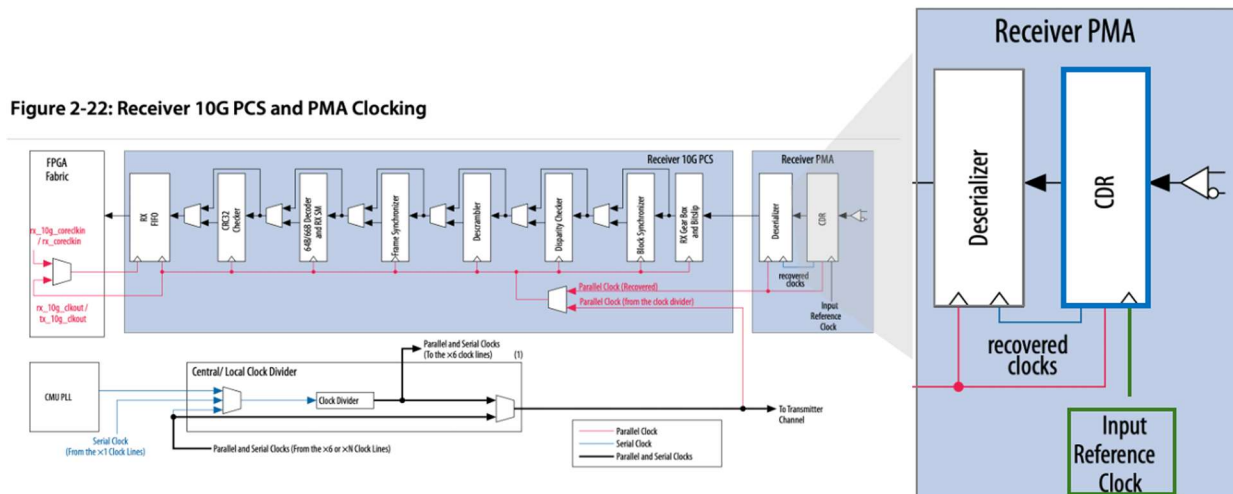
(PHY) intellectual property (IP) instances.” Ex. 1004 at 3. Accordingly, a POSA would understand that in Altera each receiver (e.g., receiver blocks (RX-1 through RX-N) located in the PMA) recovers the receiver (RX) serial clock and generates the corresponding first receiver side clock associated with the parallel received data using or based at least in part on the clock signal rx_ref_clk. Ex. 1002 at ¶ 140. The first receiver side clock signal has a frequency and phase. As indicated in Altera Figure 1, the receiver block (a part of the claimed deserializer) generates the first receiver side clock signals rx_recov_ck1-N.

Figure 1. High-Level Example of a SyncE System Line Card Using Altera FPGA and Silicon Labs SyncE PLL



The receiver PMA's role in recovering the receiver serial clock and generating the corresponding receiver-side parallel clock is confirmed by the Stratix Handbook. Ex. 1002 at ¶ 141; Ex. 1005 at 97 (Figures 2-22 and 2-23); *see also id.* at 6 ("The

PMA block . . . generates the required clocks”), 33 (Figure 1-19). Those figures illustrate that the CDR—a clock and data recovery circuit—within the Receiver PMA generates two recovered clocks, the parallel receiver side clock (shown in red) and the serial clock (shown in blue). Ex. 1002 at ¶ 141.



A CDR is a common circuit that can be used to generate a clock signal from a serial data stream and reference clock signal. *Id.* Like Altera, the '286 patent explains that the claimed deserializer can include a CDR for generating a clock signal. *E.g.*, Ex. 1001 at 8:5-8 (“FIG. 3C is an exemplary block diagram of a clock and data recovery (CDR) circuit suitable for use in the deserializer”), 10:48-50 (“The receiver clock domain is typically generated by a clock and data recovery (CDR) circuit from the incoming data stream.”), 16:9-17, 17:26-29 (“the deserializer 2104” may include a receiver PMA 3512 and receiver PCS 3508. The receiver PMA 3512 may include receiver buffer 3504, CDR 3516, and serial to parallel box 3118’.”).

Figure 1-7: Receiver PMA Block Diagram

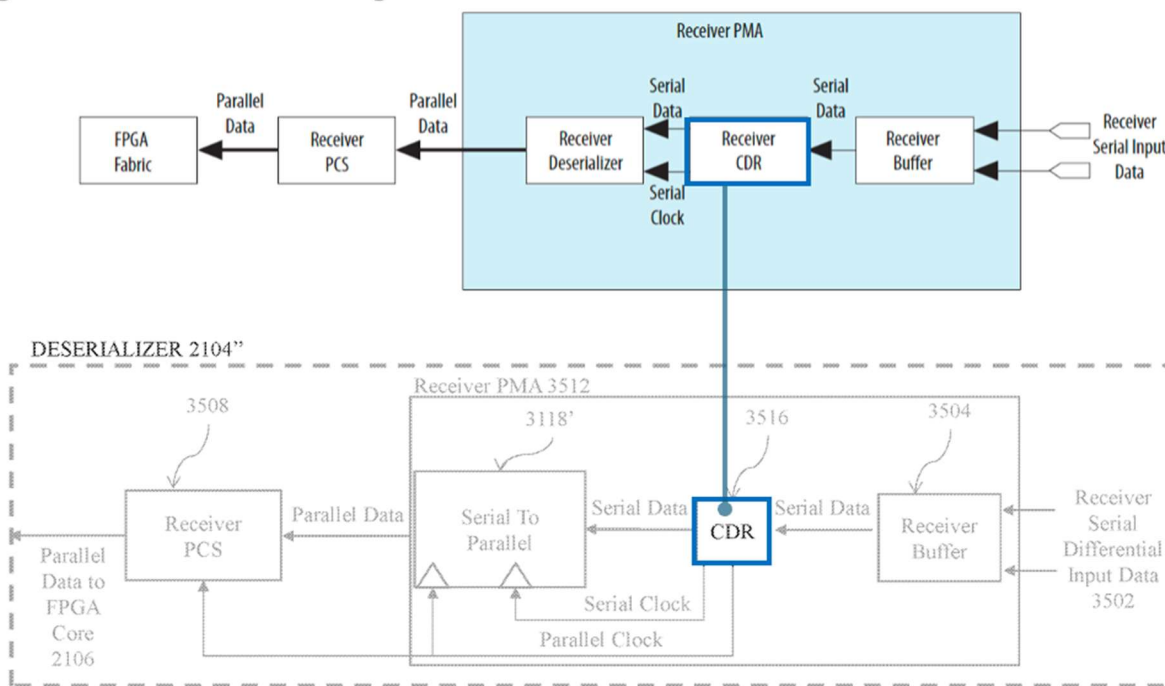
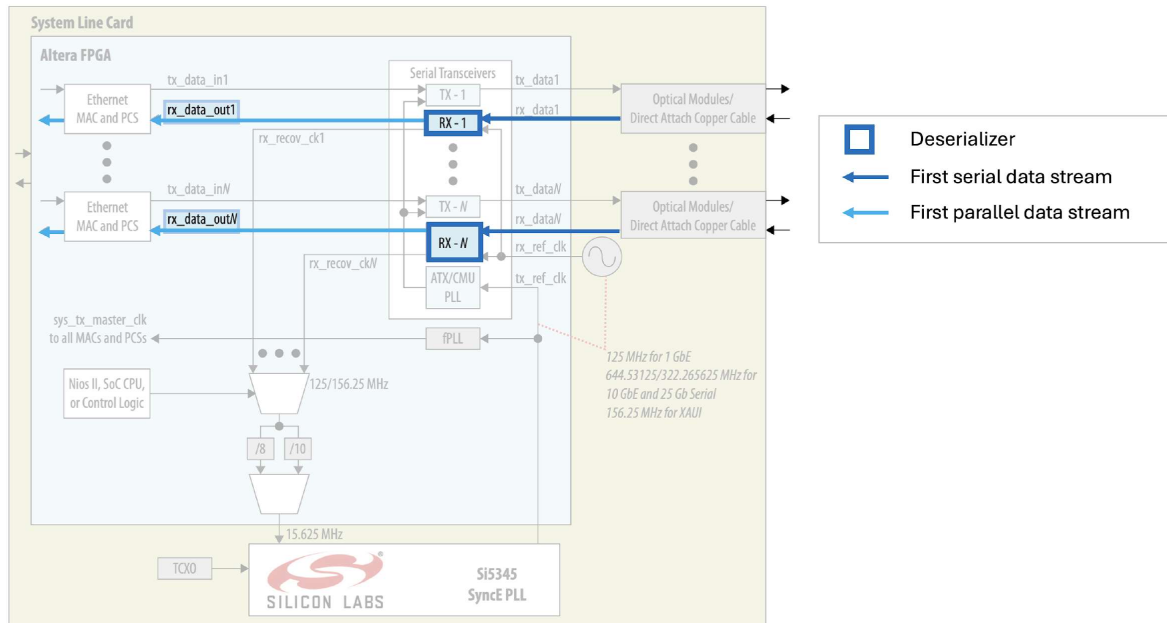


FIG. 3E

Claim 1(f)

Altera discloses “converting, by the deserializer, the first serial data stream into a first plurality of parallel data streams. Ex. 1002 at ¶¶ 143-145. A skilled artisan would understand from Figure 1 of Altera that serial rx_data is converted into parallel data, labeled rx_data_out, in the receiver (RX). *Id.* at ¶ 144. Altera also discloses that there are multiple sets of these parallel data streams, as there are multiple receivers (a total of *N* of them), each of which converts a serial data stream to a parallel data stream. *Id.*

Figure 1. High-Level Example of a SyncE System Line Card Using Altera FPGA and Silicon Labs SyncE PLL



The Stratix Handbook confirms that the receiver converts serial data to parallel data. *Id.* at ¶ 145. The Stratix Handbook explains that “[t]he PMA block connects the FPGA to the channel, generates the required clocks, and converts the data from parallel to serial or serial to parallel.” Ex. 1005 at 6. Figure 1-7 shows that the “Receiver Deserializer” of the Receiver PMA converts serial data to parallel data. *Id.* at 14; *see also id.* at 20. The one-to-one relationship between the Stratix Handbook and the claimed deserializer can be seen in the below chart comparing Figure 1-7 from the Stratix Handbook with Figure 3D from the ’286 patent.

Figure 1-7: Receiver PMA Block Diagram

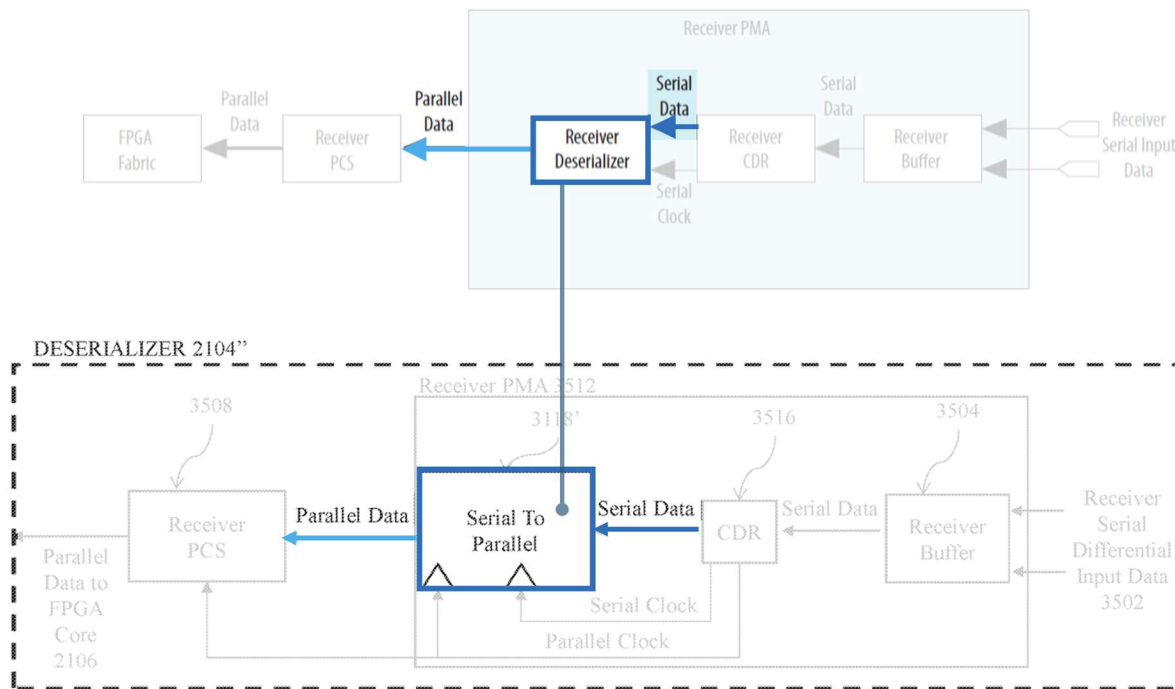
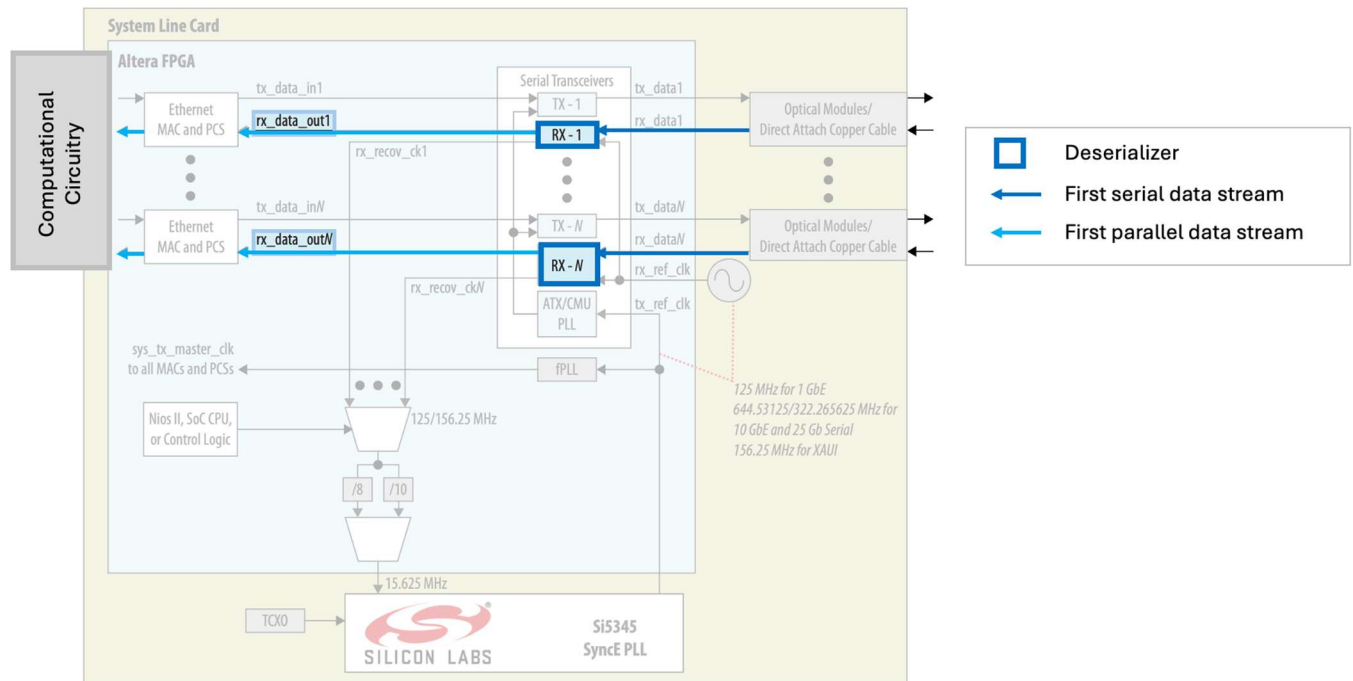


FIG. 3E

Claim 1(g)

Altera discloses “transmitting, from the deserializer to computational circuitry, the first plurality of data streams comprising a first plurality of data items and a first amount of data streams.” Ex. 1002 at ¶¶ 146-150. As shown in Figure 1, a POSA would recognize that in Altera, the deserializers, comprising for example the RX and the receiver portion of the MAC/PCS blocks, transmit parallel data streams to computational circuitry within the FPGA. *Id.* at ¶ 147. Although the Altera white paper does not explicitly draw a representation of the computational circuitry, a POSA would understand that the computational circuitry is present in the Altera FPGA as shown in the gray box below (annotated in the diagram for sake of clarity). *Id.*

Figure 1. High-Level Example of a SyncE System Line Card Using Altera FPGA and Silicon Labs SyncE PLL (Modified to add Computational Circuitry)



The Stratix Handbook confirms this. Ex. 1005 at 14. Figure 1-7 of the Handbook shows that parallel data is transmitted from the Receiver PCS of the receiver to the FPGA fabric. *Id.* A POSA would understand that FPGA fabric shown in Figure 1-7 from Altera refers to computational circuitry of the FPGA. Ex. 1002 at

¶ 148.

Figure 1-7: Receiver PMA Block Diagram

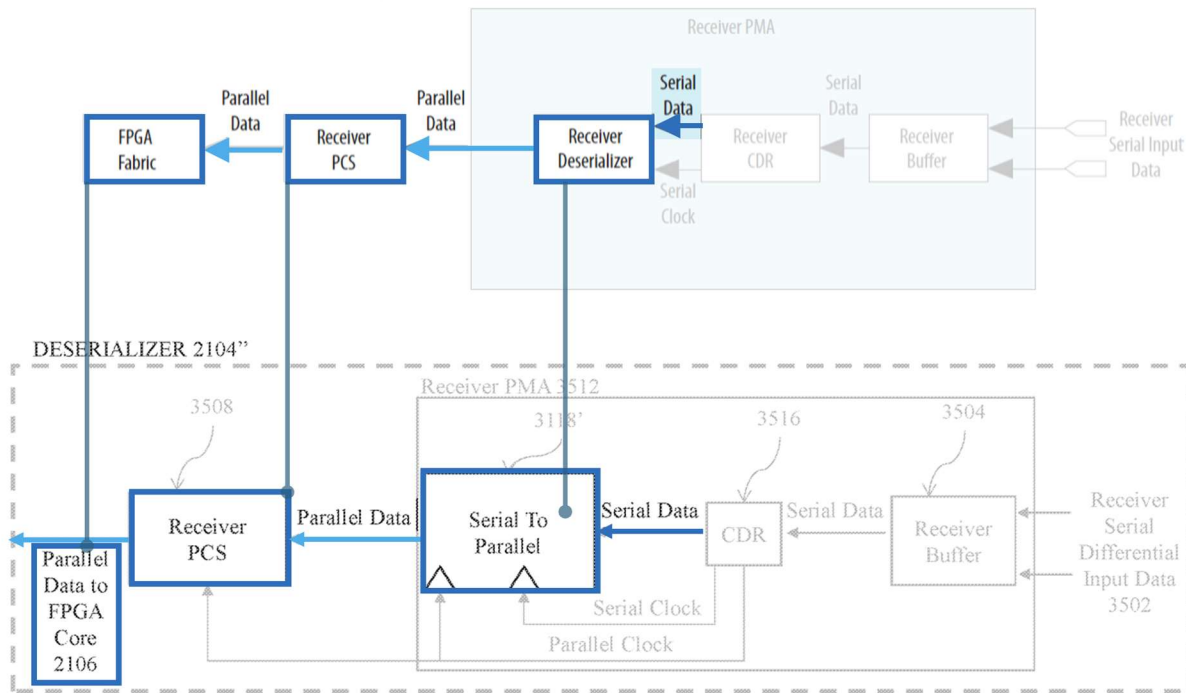


FIG. 3E

Altera also discloses that the data streams comprise a first plurality of data items and a first amount of data streams. The terms “data items” and “amount of data streams” do not have a specialized meaning to a person of ordinary skill in the art, and the specification does not define the terms.⁹

⁹ Petitioner offers these arguments without prejudice to any future arguments before the district court that this limitation is invalid under 35 U.S.C. § 112. Also, the term first plurality of data streams in claim 1(g) has no antecedent basis.

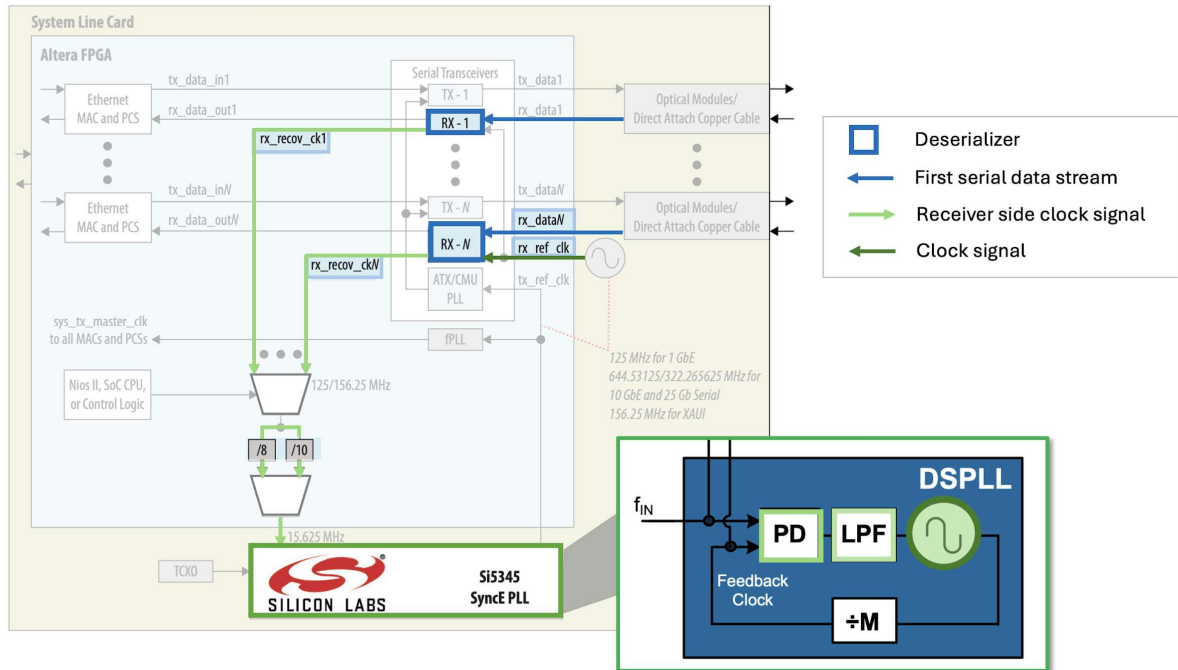
Applying the plain and ordinary meaning, Stratix Handbook discloses several data items consistent with the term's usage in the claims. The "items" constituting data within Altera are groupings of bits of data (e.g., a semantic organization of the bits, such as bytes, words, double words, quad words, or similar arrangements) that have meaning in the computational logic. Ex. 1005 at 35. Prior to transmitting the data to the computational circuitry, the receiver (deserializer) ensures that the bits of data are properly aligned into bytes or words for subsequent processing. *Id.* The data passed to the computational circuitry are a plurality of data items. In addition, because the data passes through multiple transceivers, the first amount of data streams is, for example, the total number of channels (e.g., an amount of data streams N for RX-1 through RX- N). Ex. 1002 at ¶ 150.

Claim 1(h)

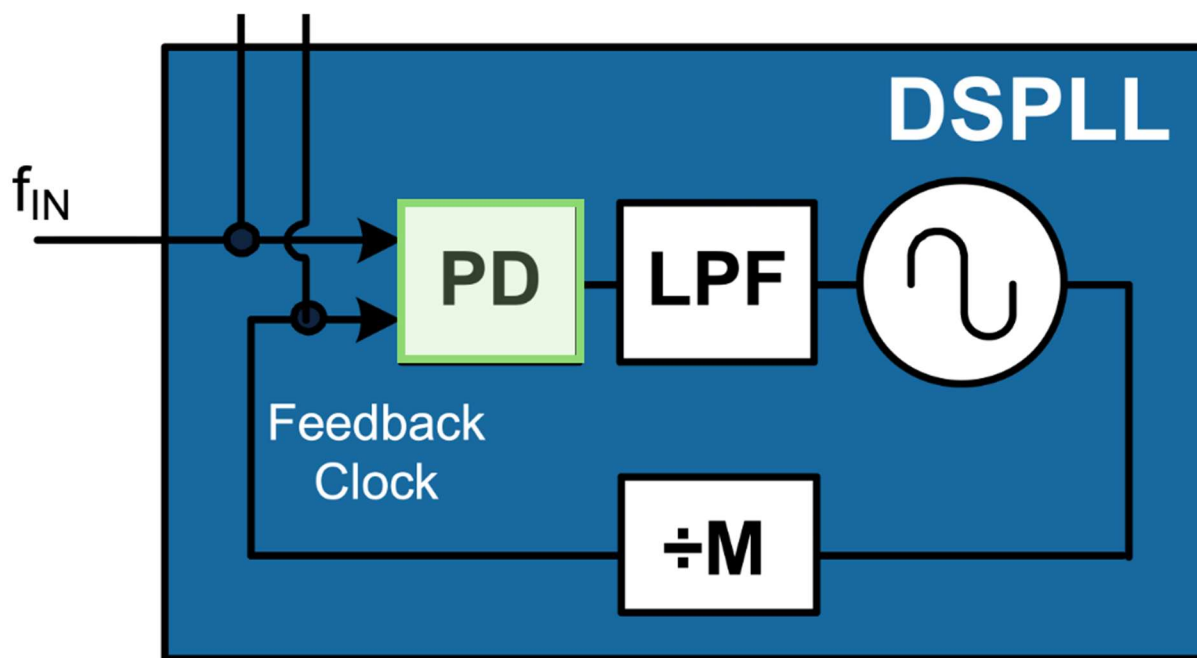
Altera discloses "transmitting, via a first clock output pin on a second interface of the field programmable gate array to a phase detector that is part of the field programmable gate array system and not part of the field programmable gate array, the first receiver side clock signal." Ex. 1002 at ¶¶ 151-153. Altera Figure 1 depicts the receiver-side clock signal (e.g., rx_recov_ck1) being transmitted from the receiver to the external Si5345 PLL (the light green lines below). *Id.* at ¶ 152. Altera also describes that step: "the RX clocks from multiple Ethernet ports are

multiplexed in the FPGA fabric to the external jitter-attenuating PLL.” Ex. 1004 at 4.

Figure 1. High-Level Example of a SyncE System Line Card Using Altera FPGA and Silicon Labs SyncE PLL



The Si5345 PLL is external to the FPGA in Altera and is thus not part of the FPGA, although it operates as part of the FPGA system. The `rx_recovered_clk` signals pass through multiplexers and Physical Media (I/O) before the first receiver side clock signal is transmitted off the FPGA to the Si5345 SyncE PLL within the overall FPGA system. Ex. 1002 at ¶ 152. The physical media (I/O) is a second interface on the FPGA device. *Id.* The first receiver side clock signal passes to the external PLL through a first clock output pin on the FPGA in the physical media. *Id.*

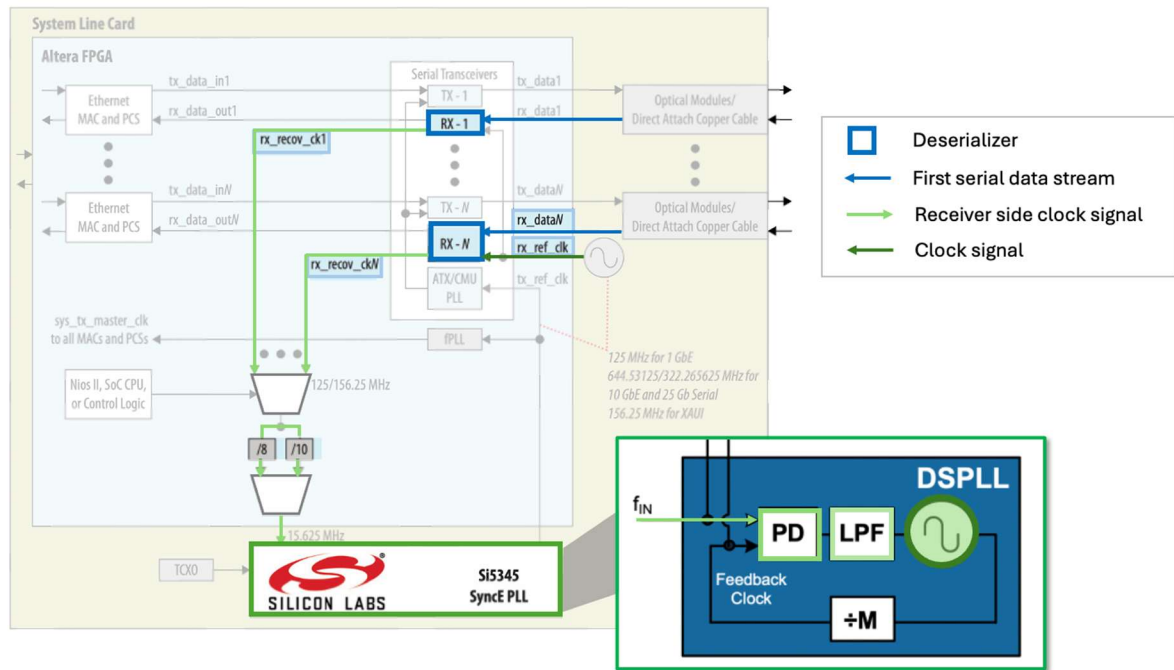


Si5345/44/42 Figure 13 Excerpt

Claim 1(i)

Altera discloses “generating, using the field programmable gate array system, a feedback clock signal associated with a first transmitter side clock signal, the feedback clock signal having a third frequency and a third phase, by performing the following steps until a first output of the phase detector is below a first threshold level.” Ex. 1002 at ¶¶ 154-158. The step of generating, using the field programmable gate array system, a feedback clock signal takes place within the Si5345 PLL used in Altera, which is part of the overall FPGA system. *Id.* The limitations in claim 1(i) describe a normal operation of a PLL. *Id.* at ¶ 155.

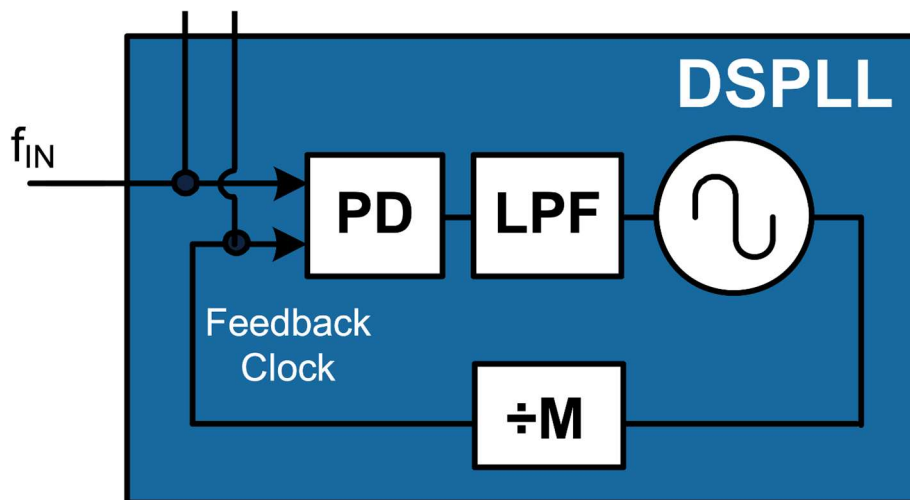
Figure 1. High-Level Example of a SyncE System Line Card Using Altera FPGA and Silicon Labs SyncE PLL



With respect to the PLL’s generation of the feedback clock signal in Si5345, “[i]f at least one valid clock is available for synchronization [e.g., the input clock], the DSPLL will automatically start the lock acquisition process. . . . During lock acquisition the outputs will generate a clock [e.g., the feedback clock] that follows the VCO [voltage-controlled oscillator] frequency change as it pulls-in to [e.g., approaches] the input clock frequency.” Ex. 1006 at 17.

Figure 13 of Si5345 discloses that during lock acquisition, the PLL generates a “feedback clock” signal that is iteratively compared against the input clock signal. *Id.* at 27. This feedback clock has a third frequency and a third phase. Ex. 1002 at ¶ 157. The DSPLL continues in lock acquisition mode, following the steps set out in claim 1(i), until the output of the phase detector is below a first threshold level. “An

example configuration where LOCK is indicated [is] when there is less than 0.2 ppm frequency difference at the inputs of the phase detector.” Ex. 1005 at 27; *see also* Ex. 1002 at ¶ 157. A POSA would understand that a DSPLL is a PLL that employs digital signal processing.

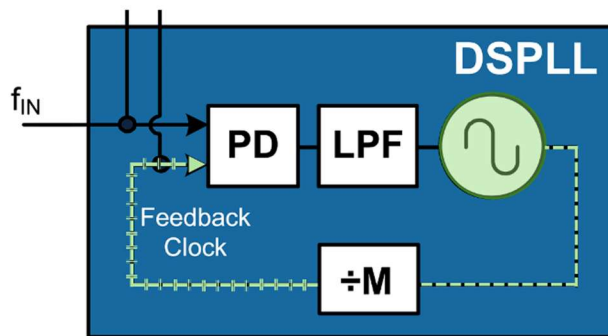


Additionally, in Altera, the feedback clock is associated with the transmitter side clock signal—because it is connected to and drives the tx_ref_clk signal of the FPGA. Ex. 1002 at ¶ 158; Ex. 1004 at 2. Specifically, the feedback clock is used by the external PLL in generating the second clock signal (tx_ref_clk), and the second clock signal is in turn used to derive the transmitter side clock signal (sys_tx_master_clk).

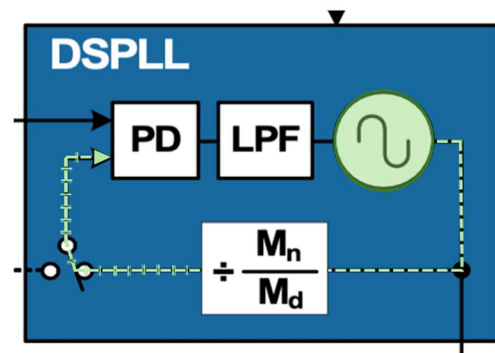
Claim 1(i)(i)

Altera discloses “generating, by an adjustable oscillator in the field programmable gate array system, a second clock signal having a fourth frequency and a fourth phase.” Ex. 1002 at ¶¶ 159-162. The Si5345 SyncE PLL includes an

adjustable oscillator, shown in green, which generates a second clock signal, which has a fourth frequency and fourth phase. *Id.* at ¶ 160; Ex. 1006 at 10, 11, 27. When the PLL is in lock acquisition mode, as shown in Figure 13, the second clock signal is then transmitted to a divide-by-M, which generates the feedback clock signal. Ex. 1002 at ¶ 160; Ex. 1006 at 27. Ultimately, as shown in the line exiting the DSPLL in Figure 2, “the DSPLL will generate output clocks that are both frequency and phase locked to its selected input clock.” Ex. 1006 at 17.



Si5345/44/42 Figure 13 Excerpt

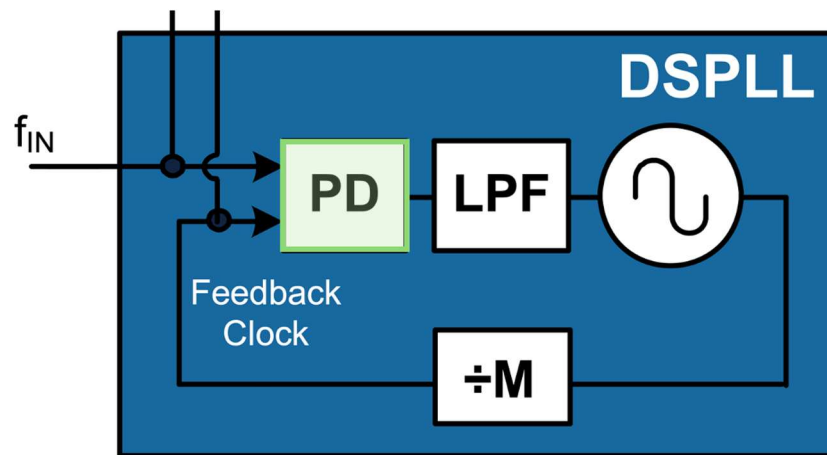


Si5345/44/42 Figure 2 Excerpt

Claim 1(i)(ii)

Altera discloses “generating, by the phase detector, the first output based on a comparison of the receiver side clock signal and the feedback clock signal obtained from the second clock signal.” Ex. 1002 at ¶¶ 161-162. The Si5345 includes a phase detector, abbreviated as “PD” and shown in red in Figure 13 below. *Id.*; Ex. 1006 at 10, 11, 27. The phase detector compares the input clock signal to the feedback clock signal. In Altera, the input clock signal is the receiver side clock signal, *see* Claim

1(f) above, and as discussed in Claim 8(i)(1), the feedback clock signal is obtained from the second clock signal passing through the (programmable) divider. Based on that comparison, the phase detector generates an output signal proportional to the phase difference between the two clock signals. Ex. 1002 at ¶ 162.

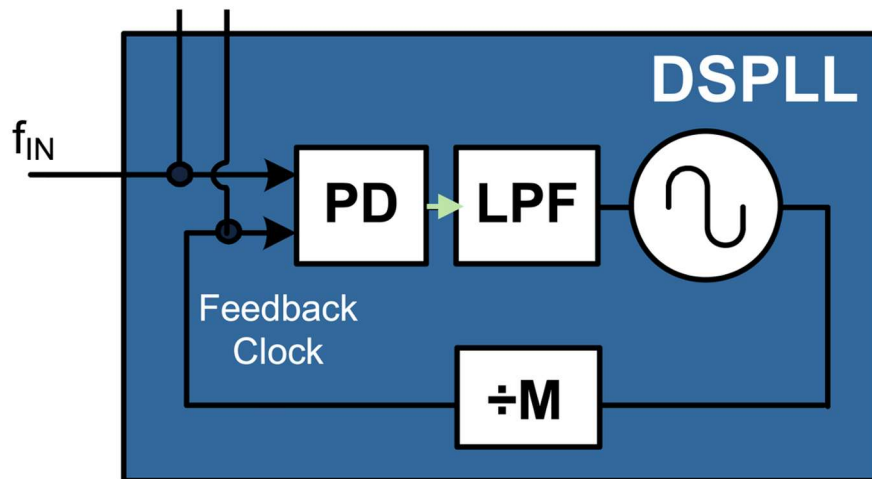


Claim 1(i)(iii)

Altera discloses “transmitting, from the phase detector to a phase controller of the field programmable gate array system which is not in the field programmable gate array, the first output.” Ex. 1002 at ¶¶ 163-166.

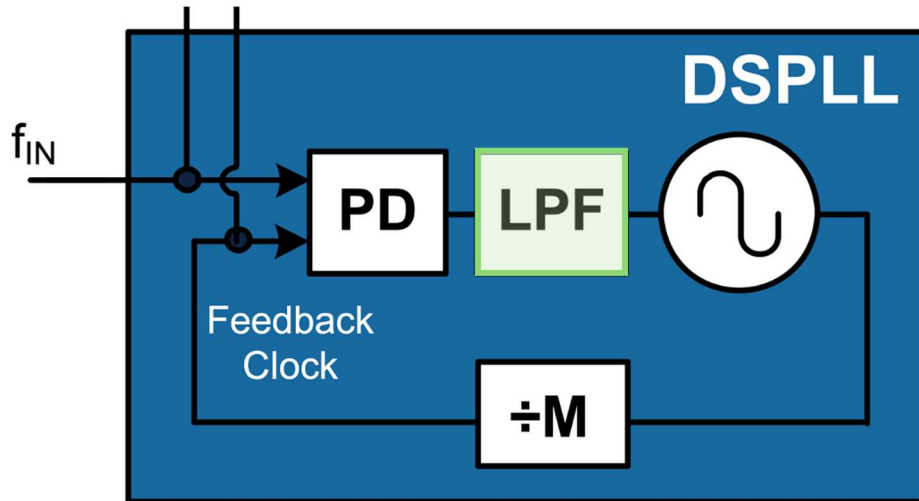
In Si5345, the phase detector (PD) transmits the first output signal to the low-pass filter (LPF), which controls the phase by allowing only frequencies lower than a certain threshold to pass through the filter. Ex. 1006 at 10, 11, 27. The LPF is a phase controller because it controls the signal. Ex. 1002 at ¶ 164. In sum, the LPF receives the output of the phase detector, allows frequencies below a threshold to pass through the filter, and outputs phase control information. *Id.*

As discussed above, the phase controller within the Si5345 is within the field programmable gate array system, but it is external to the field programmable gate array. *See* Claim 1(i).



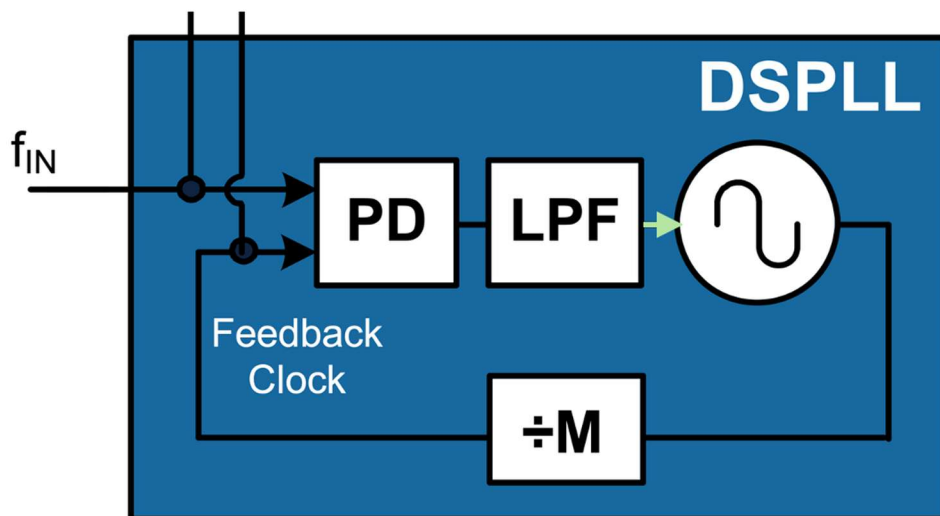
Claim 1(i)(iv)

Altera discloses “determining, by the phase controller, interim adjustment information based on the first output.” Ex. 1002 at ¶ 167. As explained above, the LPF is the phase controller. The LPF uses the first output from the phase detector to determine how to adjust the phase of the clock signal by selectively passing only certain frequencies through toward the VCO. *Id.* The LPF operation results in interim adjustment information. *Id.*



Claim 1(i)(v)

Altera discloses “transmitting, from the phase controller to the adjustable oscillator, the interim adjustment information.” Ex. 1002 at ¶¶ 168-169. In Si5345, the LPF transmits the interim adjustment information to the adjustable oscillator so the adjustable oscillator can adjust the clock signal. *Id.*; Ex. 1006 at 10, 11, 27.



Claim 1(i-wherein)

Altera discloses “wherein, the adjustable oscillator adjusts the second clock signal based on the interim adjustment information.” Ex. 1002 at ¶¶ 170-172. As discussed for claim 1(i)(i), the adjustable oscillator adjusts the second clock signal. When the PLL is in lock acquisition mode, as shown in Figure 13, the second clock signal is then transmitted to a divide-by-M, which generates the feedback clock signal. Ex. 1006 at 27. Ultimately, as shown in Figure 2 above, “the DSPLL will generate output clocks that are both frequency and phase locked to its selected input clock.” *Id.* at 17.

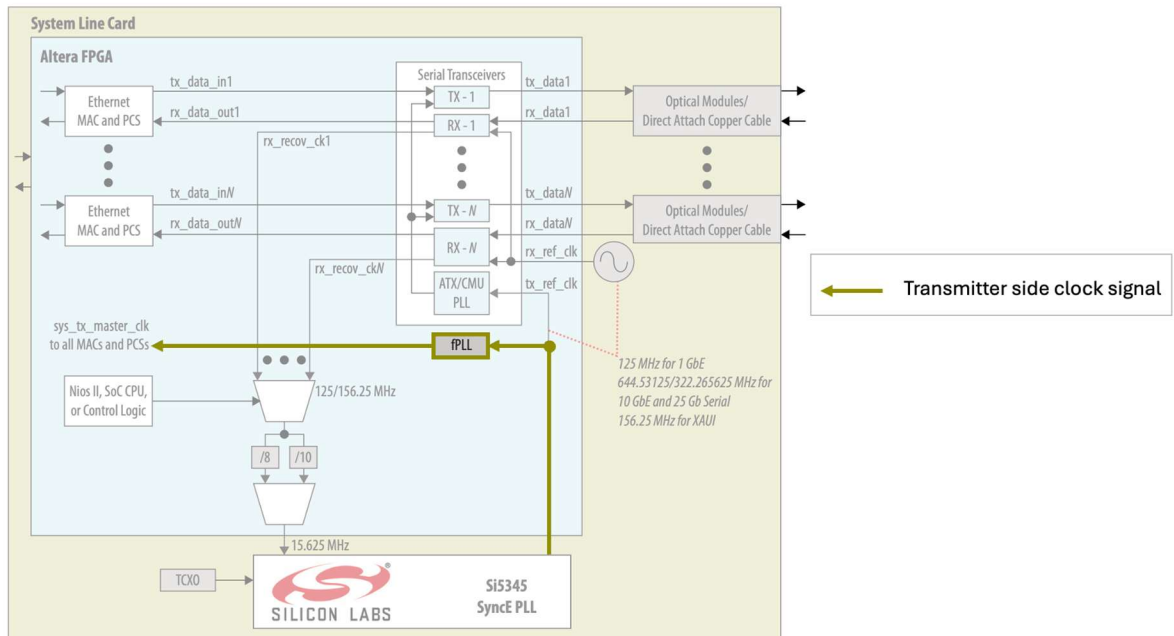
Altera also discloses “steps (i) through (v) are repeated until the first output of the phase detector is below the first threshold level.” Ex. 1002 at ¶ 172. The DSPLL continues in lock acquisition mode, following the steps set out in claim 1(i)(i-v), until the output of the phase detector is below a first threshold level, at which point it enters the locked state. *Id.* “An example configuration where LOCK is indicated when there is less than 0.2 ppm frequency difference at the inputs of the phase detector.” Ex. 1006 at 27.

Claim 1(j)

Altera discloses “generating, by a serializer, a first transmitter side clock signal based on the second clock signal.” Ex. 1002 at ¶¶ 173-177. Figure 1 shows one possible configuration of the Altera FPGA wherein the tx_ref_clk clock is

transmitted first to the fPLL (fractional PLL) within the FPGA, which then generates a transmitter-side clock signal (sys_tx_master_clk) derived from the tx_ref_clk (the second clock signal) generated by the external PLL. *Id.* at ¶ 174. Specifically, Altera explains that the “stabilized clock” generated by the Si5345 PLL (i.e., the “second clock signal”) “is used to feed the FPGA’s serial transmitter (TX) PLL in sync with the master Ethernet port’s clock frequency to realize a complete synchronization loop.” Ex. 1004 at 3; *see also id.* at 4 (Si5345 PLL “suppl[ies] a clean reference clock for the serial transceivers’ TX PLLs synchronous to the RX recovered clock”).

Figure 1. High-Level Example of a SyncE System Line Card Using Altera FPGA and Silicon Labs SyncE PLL



Although not explicitly indicated in Altera Figure 1, the Stratix V Handbook discloses a configuration where the sys_tx_master_clk (transmitter side clock signal) is generated inside the serializer (transmitter) by clock dividers and then forwarded

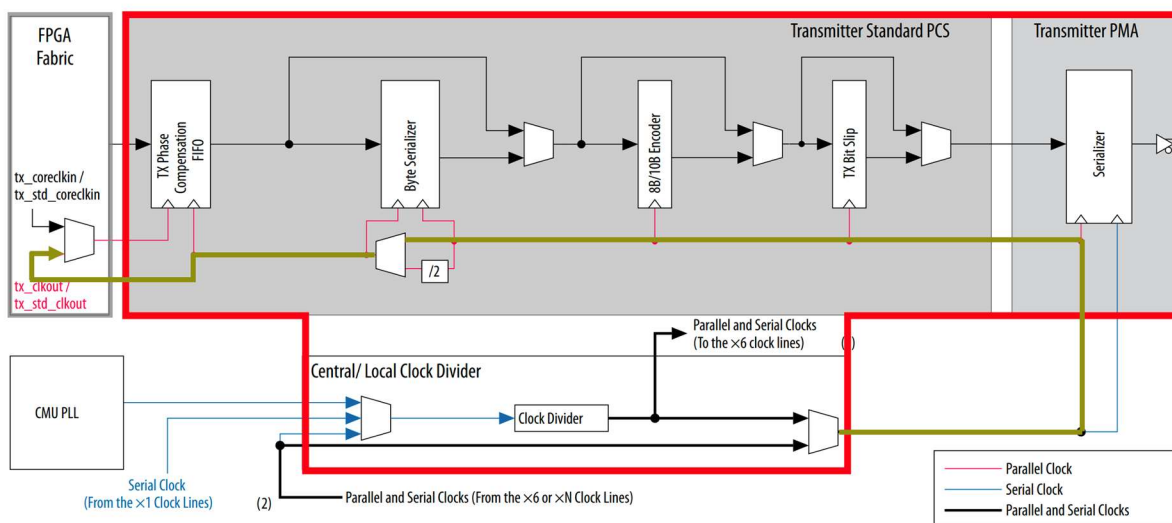
to the FPGA fabric (computational circuitry). Each transmitter channel contains or is configured to contain a clock divider: “Each transmitter channel has a clock divider called a local clock divider. The clock dividers generate the parallel and serial clock sources for the transmitter and optionally for the receiver PCS.” Ex. 1005 at 24. Stratix V can be configured such that “[t]he local clock divider block of each channel generates its own parallel clock by dividing the serial clock from the xN clock line.” Ex. 1005 at 90.

In annotated Figure 2-15 below, the red outline denotes the serializer (i.e., transmitters TX-1 through TX-N from Altera). The serial clock (depicted through the blue line), which is the second clock signal from the Si5345 SyncE, goes into the local clock divider for a given transmitter channel, which generates a parallel clock signal (tx_clkout) that passes from the Transmitter PCS to the FPGA Fabric (depicted in brown). Ex. 1005 at 105. (“The transmitter PCS forwards the following clocks to the FPGA fabric: tx_clkout for each transmitter channel in non-bonded configuration; tx_clkout[0] for all transmitter channels in bonded configuration.”). The tx_clkout is the same parallel clock depicted in Altera Figure 1 above (tx_sys_master_clk). As a result, Altera and Stratix V Handbook disclose generating, by the serializer, a first transmitter side clock signal based on the second clock signal.

Altera also anticipates a configuration where multiple serializers are bonded together and share the same transmitter side clock, stating that “[i]n bonded channel configurations the parallel clock is generated by a central clock divider for all channels, rather than using a local clock divider for each transmitter channel.” Ex. 1005 at 25.

Figure 2-15: Transmitter Standard PCS and PMA Clocking

The clock divider block provides the serial clock to the serializer of the transmitter PMA and the parallel clock to the transmitter PCS.



Notes: (1) Available only in the central clock dividers of channel 1 and channel 4 in a transceiver bank.
(2) x1 clock lines can be driven by a CMU PLL, ATX PLL, or a fractional PLL.

This configuration is consistent with the disclosures in the '286 patent, which depict the claimed serializers generating a parallel clock through “a simple clock divider.” Ex. 1001 at 17:61-67 (“The serializer also generates a parallel clock (TX Clk 4110), that operates at a lower speed than the data stream (e.g. 100-400 MHz, 100-600 MHz, to name a few), for use by other components using either a simple

clock divider 4108 or a more complex clock generation block which can contain dividers and phase shifting elements for aligning multiple transmitters.”).

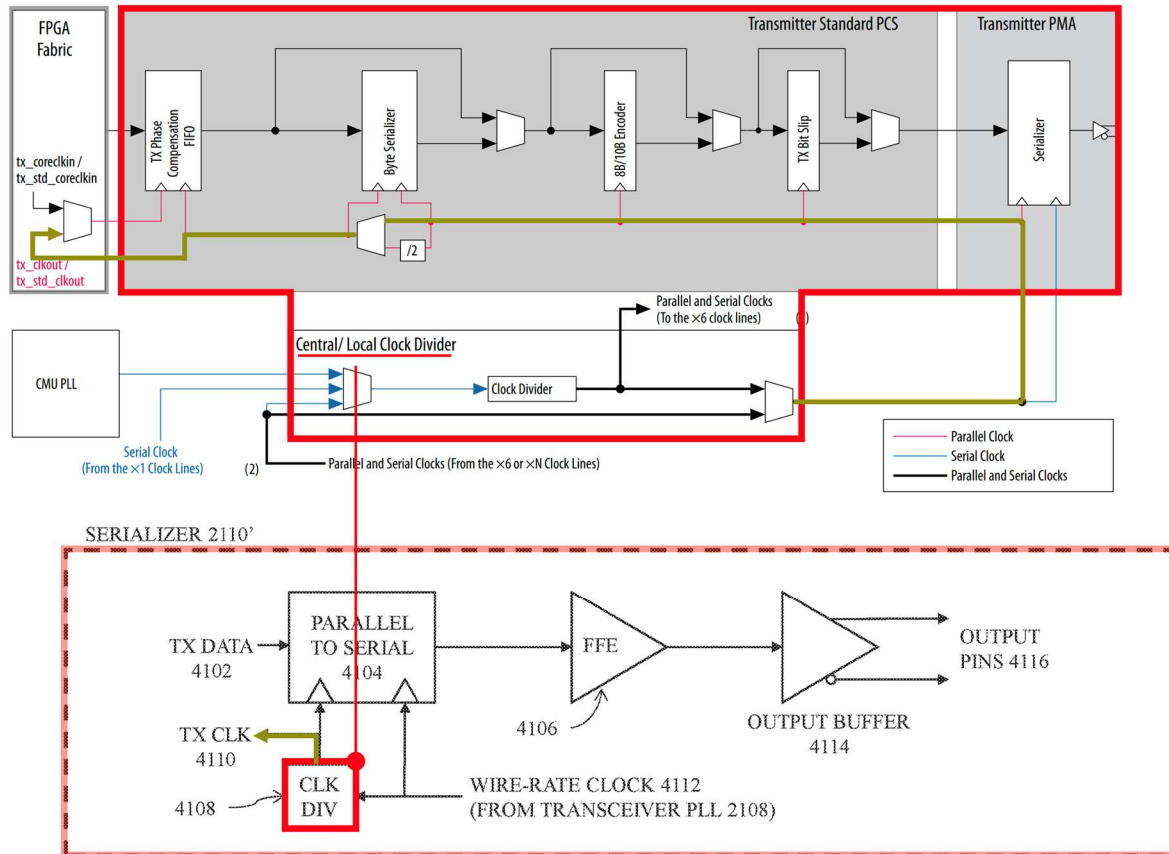


FIG. 4A

Claim 1(k)

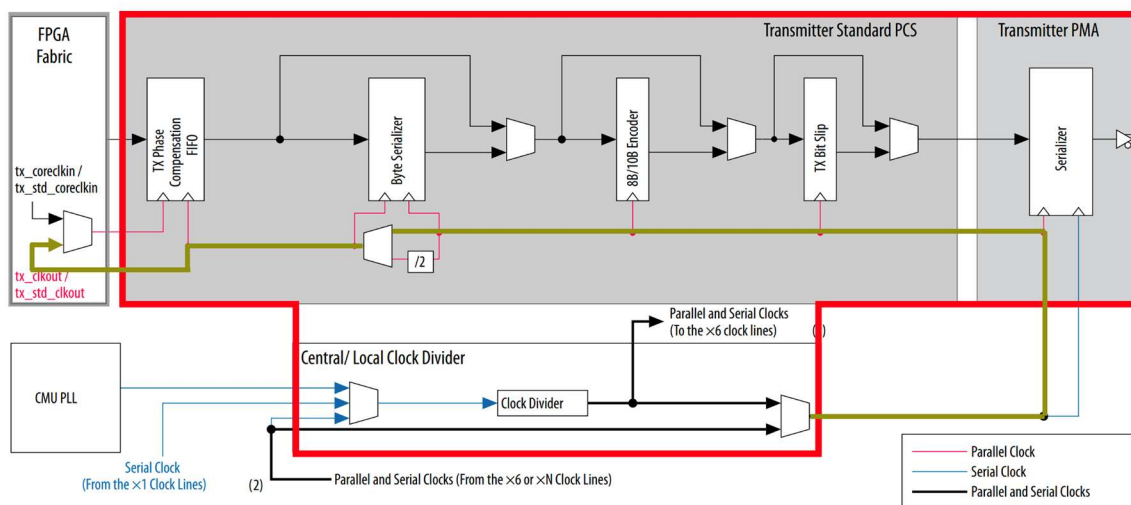
Altera and Stratix disclose transmitting, by the serializer to the computational circuitry, the first transmitter side clock signal.” Ex. 1002 at ¶¶ 178-179. As discussed above, the Transmitter PCS sends the first transmitter side clock signal (including tx_clkout in Stratix and tx_sys_master_clk in Altera Figure 1) to the FPGA fabric. Ex. 1005 at 105. (“The transmitter PCS forwards the following clocks to the FPGA fabric: tx_clkout for each transmitter channel in non-bonded

configuration; tx_clkout[0] for all transmitter channels in bonded configuration.”).

A POSA would understand that FPGA fabric refers to computational circuitry of the FPGA. Ex. 1002 at ¶ 179.

Figure 2-15: Transmitter Standard PCS and PMA Clocking

The clock divider block provides the serial clock to the serializer of the transmitter PMA and the parallel clock to the transmitter PCS.



Notes: (1) Available only in the central clock dividers of channel 1 and channel 4 in a transceiver bank.
(2) x1 clock lines can be driven by a CMU PLL, ATX PLL, or a fractional PLL.

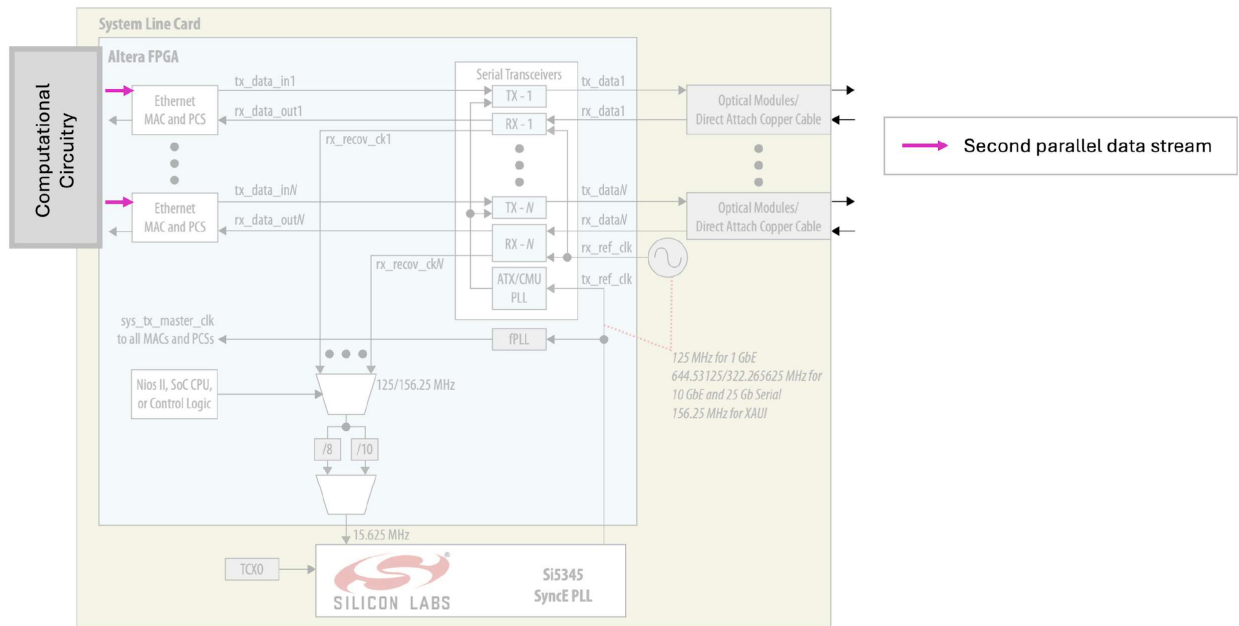
Claim 1(l)

Altera discloses “performing, by the computational circuitry, a first set of operations on at least a portion of the first plurality of data items to generate a second plurality of parallel data streams comprising a second amount of data streams.” Ex. 1002 at ¶¶ 180-185. Like all FPGAs, the Stratix FPGA used in Altera includes computational circuitry for performing operations on the first plurality of data items generate the second parallel data streams. *Id.* at ¶ 181; Ex. 1004 at 3 (discussing “FPGA core”).

The Stratix Handbook describes “the features of the logic array block (LAB) in the Stratix[®] V core fabric.” Ex. 1005 at 256. The logic array block “is composed of basic building blocks known as adaptive logic modules (ALMs) that you can configure to implement logic functions, arithmetic functions, and register functions.” *Id.* That logic array block is the computational circuitry within Altera. Ex. 1002 at ¶¶ 181-182.

A skilled artisan would understand that any useful application of an FPGA that uses the transceivers (the RX and TX blocks) must also use the computational circuitry. Altera explains that the FPGA-based solution was used for “voice, data, and video” applications. Ex. 1004 at 1. Accordingly, a POSA would understand that, in order to use the FPGA-based solution of Altera, the parallel data streams received from the deserializer must go through the computational circuitry and undergo operations. Ex. 1002 at ¶ 183; *see also* Ex. 1013 at 2 (“In this system, the programmable logic in the FPGA is loaded with a design that includes one or more Ethernet cores, along with any other application logic needed on the card.”).

Figure 1. High-Level Example of a SyncE System Line Card Using Altera FPGA and Silicon Labs SyncE PLL



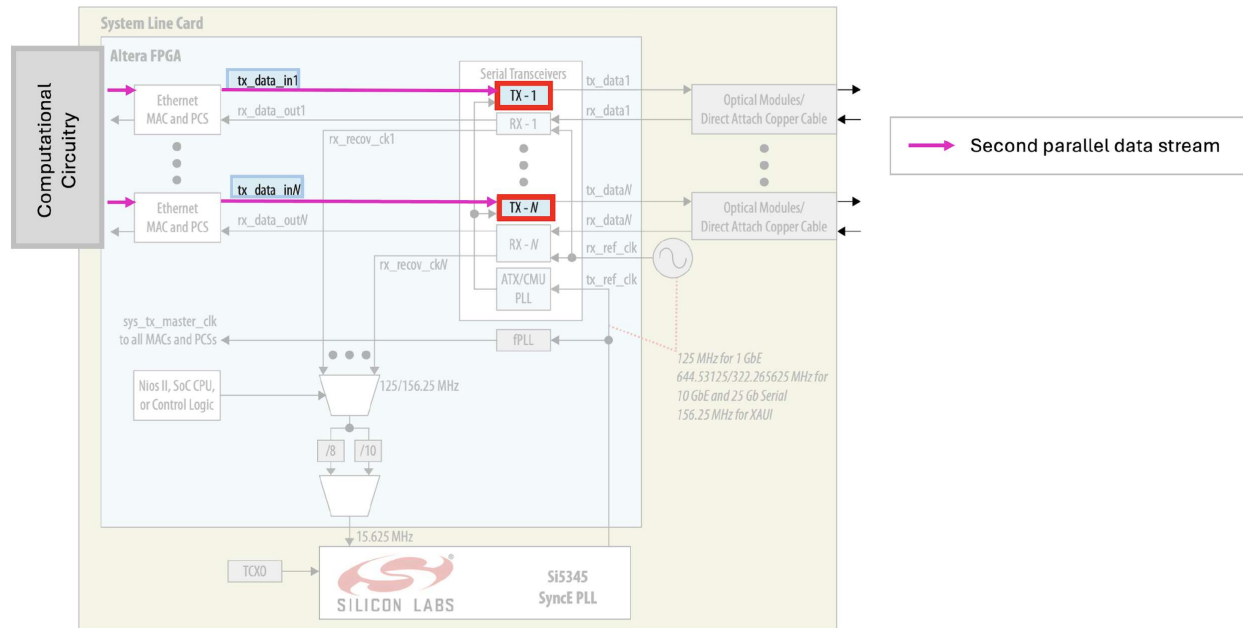
The computational circuitry performs operations on the data items transmitted within the plurality of parallel data streams, such as the individual words, bytes, or other units of data that are transferred from the FPGA to the computational circuitry. *See* Claim 1(g). The second plurality of parallel data streams also comprise a second amount of data streams because, as shown above, those streams pass through multiple channels. Ex. 1002 at ¶ 185.

Claim 1(m)

Altera discloses “transmitting, from the computational circuitry to the serializer, the second plurality of parallel data streams.” Ex. 1002 at ¶¶ 186-188. As shown in Figure 1, the second plurality of parallel data streams (tx_data_in1 through

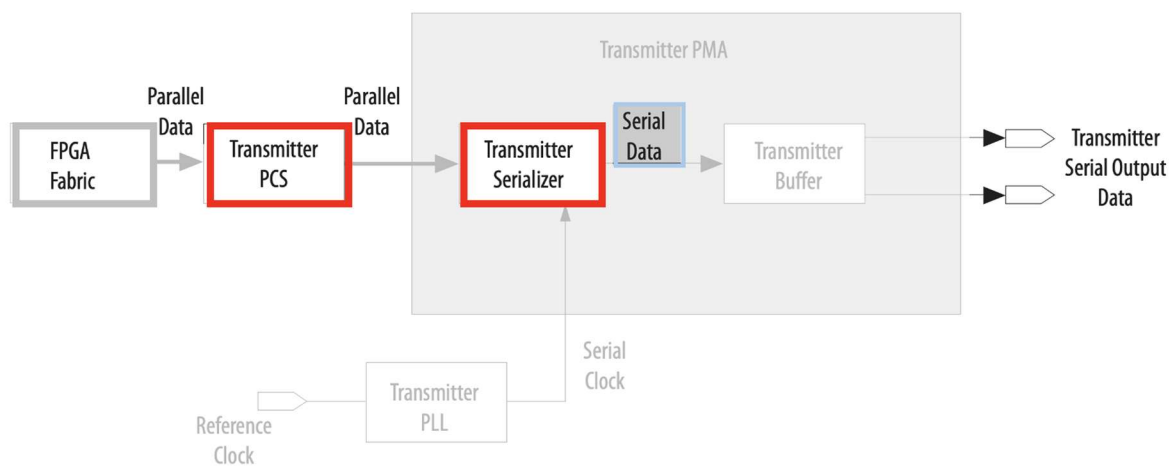
tx_data_inN) are transmitted from the computational circuitry to the transmitter portions (TX-1 through TX-N) of the serial transceivers.

Figure 1. High-Level Example of a SyncE System Line Card Using Altera FPGA and Silicon Labs SyncE PLL



The Stratix Handbook confirms that Altera discloses this limitation. *Id.* at ¶ 188. Figure 1-8 depicts parallel data being transmitted from the FPGA fabric into at least one serializer in the Transmitter PMA. Ex. 1005 at 14.

Figure 1-8: Transmitter PMA Block Diagram



Claim 1(n)

Altera discloses “converting, by the serializer, the second plurality of parallel data streams into the second serial data stream.” Ex. 1002 at ¶¶ 189-191. After the second plurality of parallel data streams, (tx_data_in1 — tx_data_inN) are transmitted to the transmitter portion (TX-1 through TX-N) of the serial transceivers, the transmitters convert the parallel data streams into a second serial data stream (tx_data1 — tx_dataN). Ex. 1004 at 2.

Figure 1: System Line Card Block Diagram

The diagram illustrates the architecture of a system line card, divided into three main functional blocks:

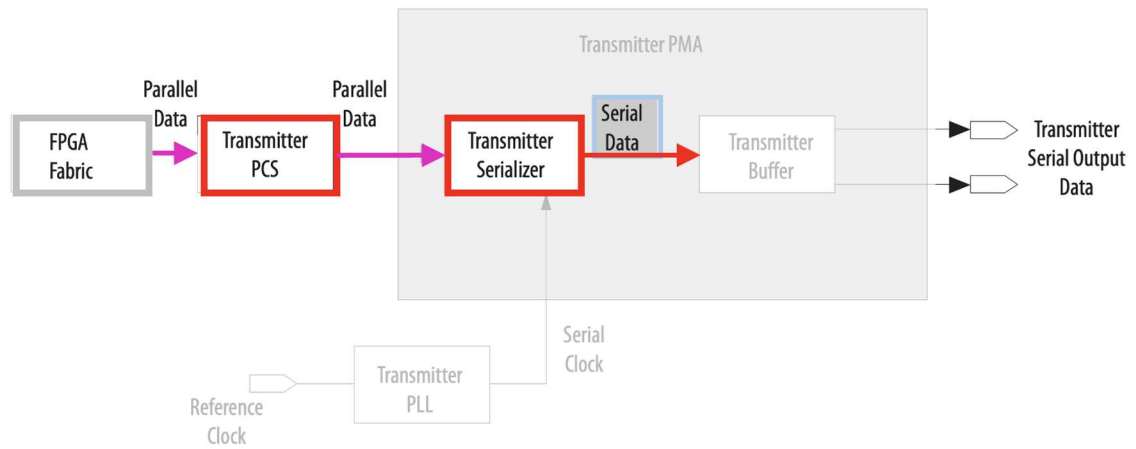
- Computational Circuitry:** Contains Ethernet MAC and PCS blocks. It interfaces with the Altera FPGA via tx_data_in1 to tx_data_inN and rx_data_out1 to rx_data_outN .
- System Line Card:** Contains the Altera FPGA, Serial Transceivers (TX-1 to TX-N), and an fPLL. The Altera FPGA interfaces with the Serial Transceivers via rx_recov_clk1 to rx_recov_clkN . The Serial Transceivers interface with Optical Modules/Direct Attach Copper Cable via tx_data1 to tx_dataN and rx_data1 to rx_dataN . The fPLL provides clock signals to the Serial Transceivers and the Altera FPGA via tx_ref_clk and rx_ref_clk .
- Reference Block:** Contains a TCXO and a Si5345 SyncE PLL. The TCXO provides a 15.625 MHz clock signal to the Si5345 SyncE PLL, which provides a 125/156.25 MHz clock signal to the Altera FPGA.

Legend:

- Red square: Serializer
- Purple arrow: Second parallel data stream
- Red arrow: Second serial data stream

69

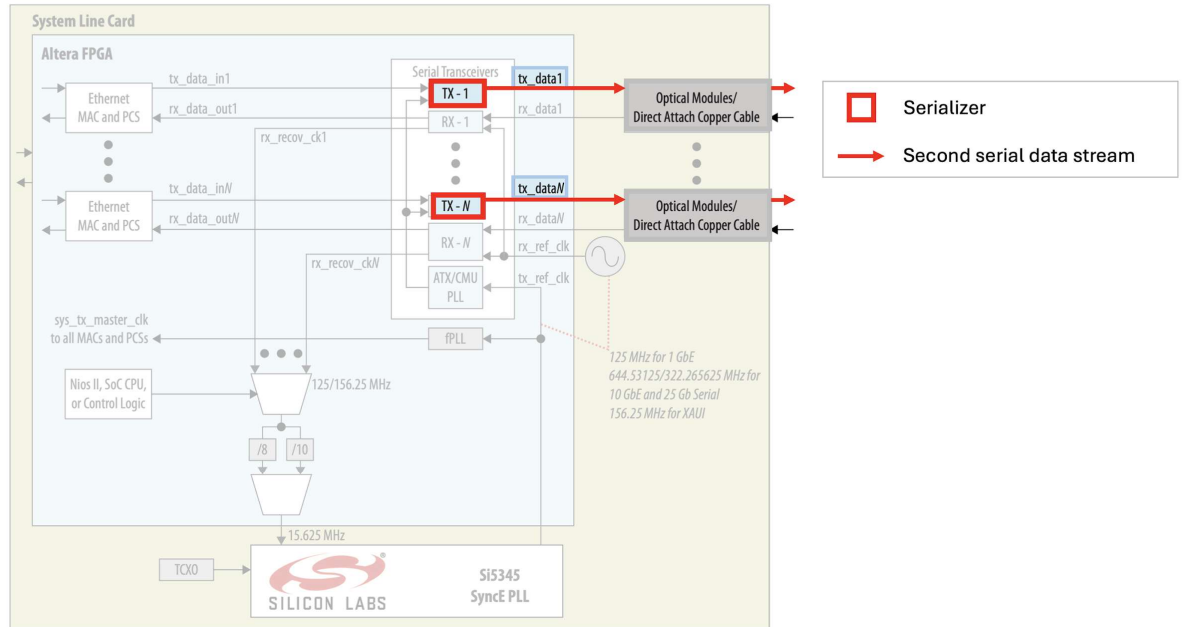
Figure 1-8: Transmitter PMA Block Diagram



Claim 1(o)

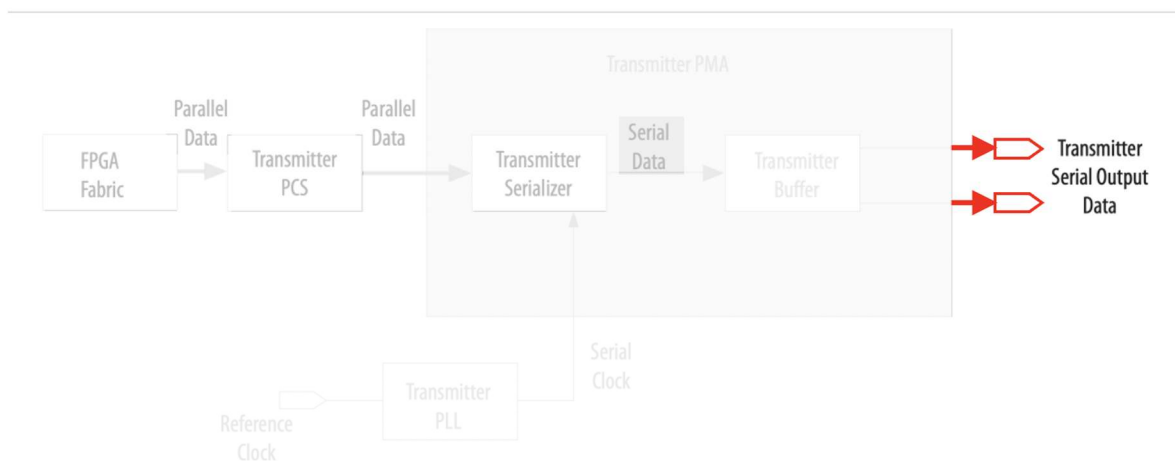
Altera discloses “transmitting, from the serializer off the field gate programmable [sic] array system via a second plurality of data pins in the first interface, the second serial data stream.” Ex. 1002 at ¶¶ 192-194. As shown in Figure 1, the serialized data, tx_data1 through tx_dataN, is transmitted to the transmitter portion (TX-1 through TX-N) of the serial transceivers to the Optical Modules/Direct Attach copper cable. *Id.* at ¶ 193. This data is derived from the second plurality of parallel data streams (tx_data_in1 through tx_data_inN). The transmitter portion (TX-1 through TX-N) of the serial transceivers (i.e., the serializer) converts the parallel data streams to serial data streams *Id.*

Figure 1. High-Level Example of a SyncE System Line Card Using Altera FPGA and Silicon Labs SyncE PLL



The Stratix Handbook confirms that Altera discloses this limitation. Ex. 1002 at ¶ 194. As shown in Figure 1-8, the serializer generates serial data streams that are then transmitted off the FPGA system via a transmitter buffer connected to serial output data pins. Ex. 1005 at 14 (“The PMA . . . transmits off-chip high-speed serial data streams.”), 26 (“The serializer converts the incoming low-speed parallel data from the transceiver PCS or FPGA fabric to high-speed serial data and sends the data to the transmitter buffer.”). As shown in Figure 1-8 below, the serial data is transmitted off the FPGA system through the Optical Modules / Direct Attach Copper Cables using data pins in the first interface.

Figure 1-8: Transmitter PMA Block Diagram



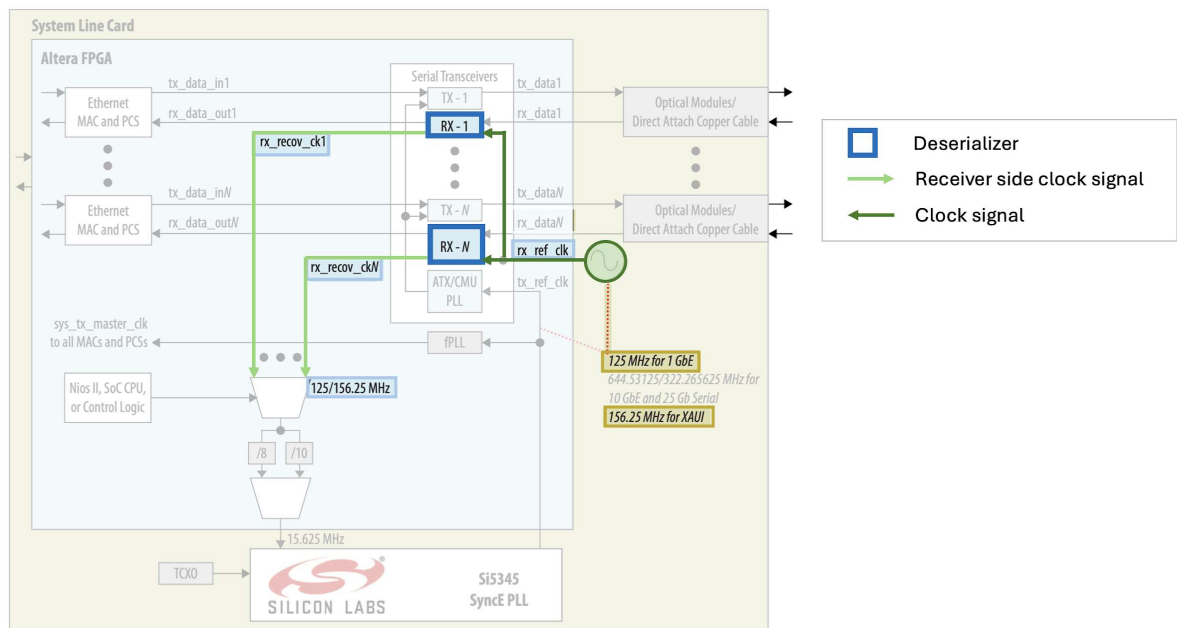
Claim 2

Altera discloses “[t]he method of claim 1, wherein the second frequency corresponds to the first frequency.” Ex. 1002 at ¶¶ 195-197. Per claim 1, the first frequency is the frequency associated with the first clock signal (claim 1(b)) and the second frequency is the frequency associated with the first receiver side clock signal (claim 1(e)).

Altera’s Figure 1 depicts a first clock signal rx_ref_clk with a first frequency of either 125MHz for 1GbE or 156.25 MHz for XAUI. Figure 1 likewise depicts a first receiver side clock signal rx_recov_ck1-N with a second frequency of either 125 MHz or 156.25 MHz. The ’286 patent describes “corresponds” as including circumstances where the two frequencies are the same or are close (e.g., within an acceptable range in the art). Ex. 1001 at 23:14-19 (“In embodiments, the second

frequency is different from the first frequency. In embodiments, the second frequency corresponds to the first frequency. In embodiments, corresponding may refer to the frequencies being the same frequency. In embodiments corresponding may also refer to frequencies being close (e.g. within an acceptable range in the art) to the same frequencies.”). As a result, Altera discloses the second frequency corresponding to the first frequency.

Figure 1. High-Level Example of a SyncE System Line Card Using Altera FPGA and Silicon Labs SyncE PLL



Claim 8

Altera discloses “[t]he method of claim 1, wherein a difference between the third phase and the second phase is less than a second threshold level.” Ex. 1002 at ¶¶ 198-199. The Si5345 Manual explains “[o]nce locked, the DSPLL will generate output clocks that are both frequency and phase locked to its selected input clock.” Ex. 1006 at 17. Prior to generating these output clocks, the phase of the feedback

clock in the Si5345 SyncE PLL is compared to the phase of the receiver-side clock signal (e.g., rx_recov_ck1). The phases of the feedback clock and the receiver-side clock signal (e.g., rx_recov_ck1) are locked only when the difference between the two is below a threshold. As such, in addition to the PLL system being “locked” when the third and second phases are aligned, the PLL system is also “locked” when the difference between the third phase and the second phase are below the threshold programmed into the PLL (a second threshold).

Claim 10

Altera discloses “wherein the first set of operations does not include clock domain crossing operations that delay processing of the first set of parallel data streams.” Ex. 1002 at ¶¶ 200-204. A clock domain crossing operation within the computational logic is necessary only when asynchronous clock domains exist within the computational logic. *Id.* at ¶ 202. Altera explains that its SyncE solution supports “[g]eneration of all system clock frequencies from a single recovered clock frequency,” (e.g., rx_recov_clk) using the “PLL to maintain stability and accuracy.” Ex. 1004 at 3; *see also id.* at 2 (showing a “sys_tx_master_clk”). “[A]ll system clock frequencies” refers to, among other things, the clocks depicted in Altera Figure 1, including the clocks used by the computational logic that processes the parallel data streams, all MACs, all PCSs, and serializers. Ex. 1002 at ¶ 203. In other words, there are no clock domains to cross because the processing of the parallel, deserialized

data uses a single clock—the clock derived from the selected deserializer. *Id.* at ¶ 204.

Claim 11

Altera discloses “[t]he method of claim 1, wherein the first amount of data streams is the same as the second amount of data streams.” Ex. 1002 at ¶¶ 205-206. Altera Figure 1 depicts the same amount of data streams going to the computational circuitry (e.g., rx_data_out1 through N) as the amount of data streams coming back from the computational circuitry into the serializer (e.g., tx_data_in_1 through N). In addition, Figure 1 shows that for every RX block there is also a TX block (e.g., RX-1 and TX-1), totaling N number for each. Ex. 1004 at 2; *see also* Ex. 1005 at 7 (showing each transceiver channel has one receiver and one transmitter). And Altera explains that the “Altera® SyncE reference design implement[s] up to ten 1G/10 Gbps Ethernet (1G/10 GbE) ports,” indicating that in Altera there are up to 10 transceiver channels (e.g., 10 deserializers and 10 serializers) in the reference design. Ex. 1004 at 2. As noted in the Stratix Handbook, the transceivers are full-duplex; “Stratix V devices provide up to 66 backplane-capable full-duplex clock data recovery (CDR)-based transceivers.” Ex. 1005 at 6.

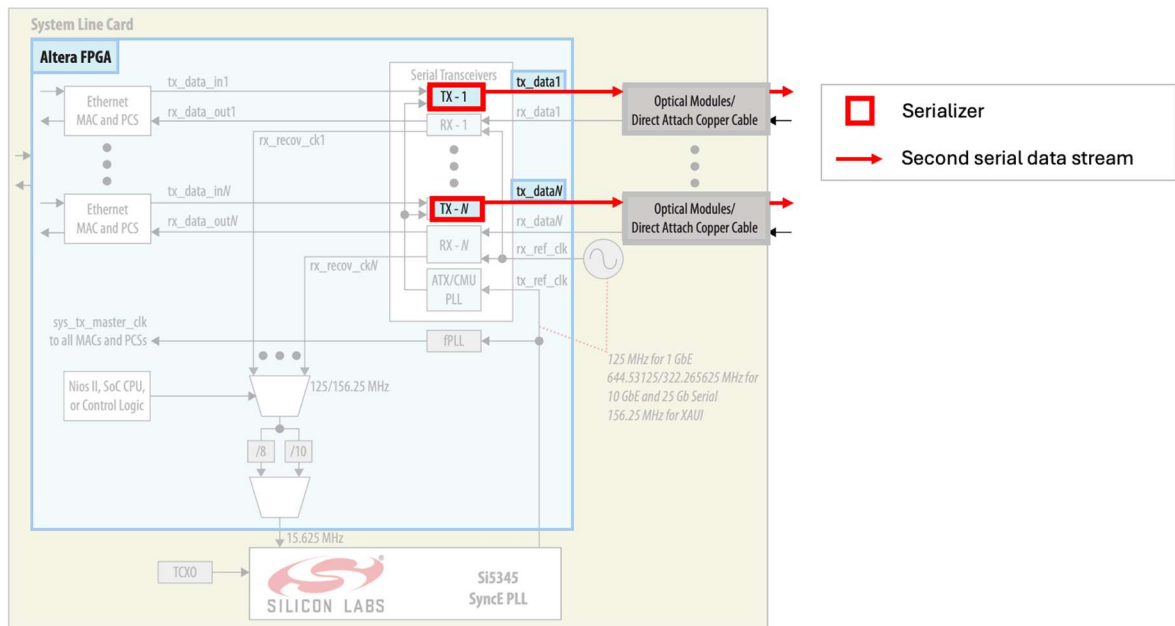
Claim 19

Altera discloses “[t]he method of claim 1, wherein the transmission of the second serial data stream from the serializer off the field programmable gate array

is transmitted to an input/output module off the field programmable gate array.”

Ex. 1002 at ¶¶ 207-208. Figure 1 shows the second serial data streams tx_data1 — tx_dataN transmitted from serializers TX1-N to Optical Modules/Direct Attach copper cables. Input/output modules include the physical interface for transmitting data, such as Optical Modules/Direct Attach copper cables. Figure 1 depicts Optical Modules/Direct Attach cables that are outside the Altera FPGA and transmit the serial data off the FPGA system.

Figure 1. High-Level Example of a SyncE System Line Card Using Altera FPGA and Silicon Labs SyncE PLL



B. Ground 1B: Altera, the Stratix Handbook, and the Si5345 Manual Render Claims 1, 2, 8, 10, 11, and 19 Obvious

To the extent that a POSA would not have understood that the features of Stratix FPGA and Si5345 PLL are necessarily present in Altera, it would have been

obvious to combine the Altera white paper, the Stratix Handbook, and the Si5345 Manual. Ex. 1002 at ¶¶ 209-211.

A POSA would have been motivated to combine the Stratix Handbook and Si5345 Manual using Altera. *Id.* at ¶ 209. Altera describes “a high-performance SyncE solution” that consists of “Altera’s Stratix® V FPGA interoperating with Silicon Labs’ Si5345 jitter-attenuating phase-locked loop (PLL) to provide a complete SyncE clock recovery, clock selection, and synchronization sub-system.” Ex. 1004 at 2. The Altera solution was developed by “Altera and Silicon Labs” and specifically used “the two companies’ products.” *Id.* at 2. And, as described above, a POSA would have been able to easily find and rely on the Stratix Handbook and Si5345 Manual, as they are among the specifications and data sheets that Altera and Silicon Labs made available for download from their respective websites. *See* § V.A above.

Further, a POSA would have reasonably expected the combination of Stratix and Si5345 as set out in Altera to succeed, as Altera reports that its technique was successfully tested. Ex. 1002 at ¶ 210; Ex. 1004 at 6. For example, “Altera and Silicon Labs have validated that the jitter performance of Silicon Labs’ Si5345 PLL meets the requirement of Altera’s Stratix FPGA input reference clock and that the serial transceiver output jitter meets G.8262 requirements. The test includes Silicon Labs’ Si5345 PLL output jitter, phase noise tolerance at the PLL input, the clock

synchronization loop’s phase noise filtering capability, and the ability of the loop to withstand short-term and long-term input interruptions and discontinuities.” *Id.* A POSA would have been confident in the success of the system since Altera “demonstrated a high-performance and flexible solution for frequency synchronization of telecom and data communication networks based on the Sync standard using the Ethernet infrastructure.” *Id.*; Ex. 1002 at ¶ 210.

Therefore, a POSA would have had reason to combine the Stratix FPGA with the Si5345 PLL in precisely the same way that Altera says they should be combined. *See Norian Corp. v. Stryker Corp.*, 363 F.3d 1321, 1328 (Fed. Cir. 2004) (affirming that a POSA would have been motivated to combine two references where one reference “expressly discussed the” other one). That combination of Altera, the Stratix Handbook, and the Si5345 Manual discloses all the limitations of claims 1, 2, 8, 10-11, and 19 for the same reasons as Altera anticipates those claims. Ex. 1002 at ¶ 211.

C. Ground 2: Altera and Lockwood render claim 1, 2, 8, 10-11, and 19-20 obvious

Altera (alone or in combination with the Stratix Handbook and Si5345 Manual) presents a solution to the latency inherent in clock-domain crossing that would have been obvious and attractive to a POSA for use in high-frequency trading

applications, as Lockwood teaches.¹⁰ The combination of Altera and Lockwood renders obvious the preamble to claim 1’s preamble reciting “a first serial data stream comprising market data” and “a second serial data stream comprising order entry data.” The same combination renders obvious claim 20, which recites the “method of claim 1, wherein the first serial data stream includes market data and the second serial data stream includes trading data.” Ex. 1002 at ¶¶ 212-233.

1. A Skilled Artisan Would Have Been Motivated to Combine Altera and Lockwood

It was common knowledge before the ’286 patent that FPGA-based systems are useful for performing high-frequency trading operations, as even the patent acknowledges. Ex. 1001 at 1:34-36 (“FPGAs are used in the financial industry in high frequency trading where the rapid processing of the FPGA is desired.”); Ex. 1002 at ¶ 212. Lockwood demonstrates how a skilled artisan would have put an FPGA such as those from Altera to use for such trading. *Id.*

Lockwood emphasized, back in 2012, “the race to minimize latency in high frequency trading.” Ex. 1007 at 7. In high-frequency trading, “[a] custom-designed datapath in an FPGA circuit offers the benefits of minimal, deterministic processing

¹⁰ The motivation to combine and the rationale for the combining Altera and Lockwood are the same as those described in the ’381 Petition. ’381 Petition at 63-68.

times down to clock cycles,” which are the smallest unit of time in which logic operations can occur. *Id.* at 8. In a regime like high-frequency trading in which even a few clock cycles can make a difference, a skilled artisan would have recognized that Altera offers a solution that eliminates the latency cost associated with clock-domain crossing circuits. *Id.* at 2 (“[T]he first few players to execute orders may be the only ones able to profit from a given opportunity” and “reduction in latency can improve arbitrage profitability”); Ex. 1014 at 1 (“HFT is all about speed and minimizing latency: the faster you can run trading strategies and algorithms for analyzing minute price changes and executing trade orders, the higher the probability to win over competition.”); Ex. 1015 at 2:13-14 (cited on the face of the ’286 patent and noting that speed of information delivery is a valuable dimension to the financial instrument trading and brokerage industry); Ex. 1002 at ¶ 214.

Additionally, Altera explains that the benefit of its SyncE synchronization solution is “high reliability,” resulting in “a high-performance and flexible solution for frequency synchronization of telecom and data networks based on the SyncE standard using the Ethernet infrastructure.” Ex. 1004 at 2, 6. Lockwood explained that, even as of 2012, “Ethernet is currently more prevalent in the HFT ecosystem” and “will continue to dominate for the foreseeable future”—and the passage of time has demonstrated this to be true. Ex. 1007 at 2. Thus, long before 2018, as Lockwood

demonstrated, a POSA would have been motivated to use Altera in high-frequency trading applications. Ex. 1002 at ¶ 215.

Lockwood provided several different examples in which a POSA would recognize that the Altera system could be utilized. *Id.* at ¶ 216. For example, Lockwood described FPGA-based Smart Network Interface Controllers (NICs) as “another way to apply programmable logic” to the development of financial applications. “Smart NICs typically bring together high-speed network interfaces, a PCIe host interface, memory and an FPGA,” and in this arrangement, “some of the processing” is “offload[ed]” to the FPGA. Ex. 1007 at 8. Specifically, “[t]he FPGA implements the NIC controller, acting as the bridge between the host computer and the network and allows user-designed custom processing logic to be integrated directly into the data path.” *Id.* at 3. This allowed a smart NIC to “function as a programmable trading platform.” *Id.* at 11. A POSA would recognize that Altera—which touts its usefulness in networking equipment, among other things—could be used as the FPGA in Lockwood Figure 2 and the computational circuitry of the Altera FPGA would “function as a programmable trading platform.” *Id.*; *see also* Ex. 1004 at 2; Ex. 1002 at ¶ 216.

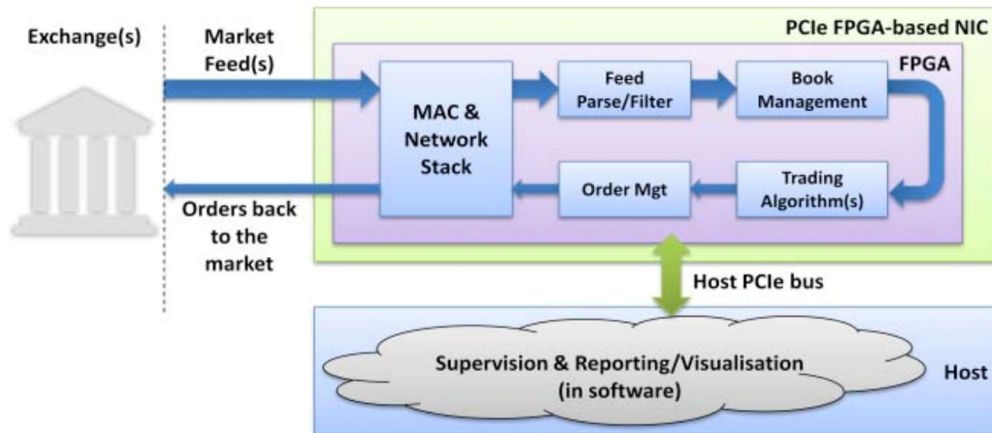
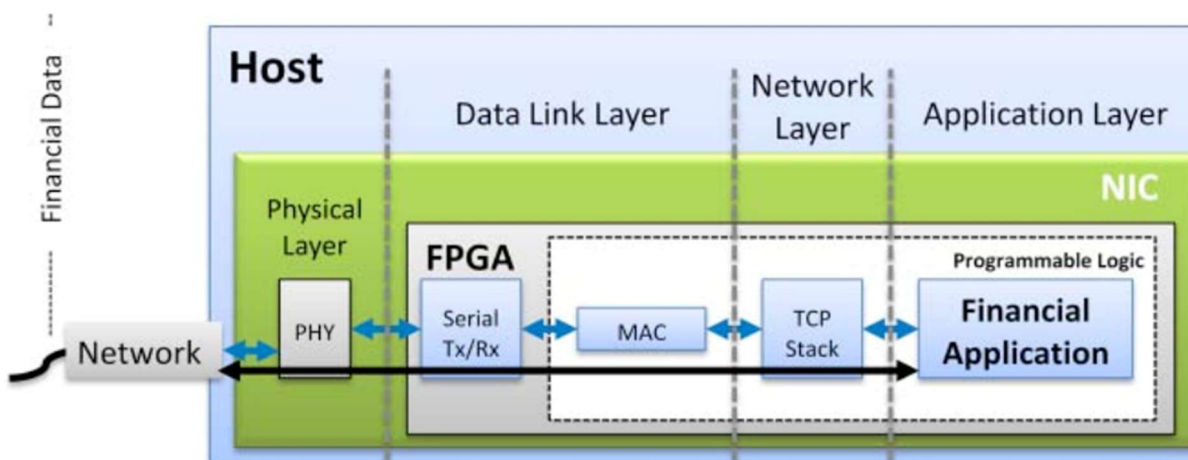


Figure 2 Typical Smart NIC in a supervised financial trading application

A skilled artisan would also recognize that Altera would be an attractive option to use for the FPGA shown in the FPGA-based trading platform displayed in Lockwood’s Figure 3, below. Ex. 1002 at ¶ 217. Altera’s solution largely relates to the data link layer shown in Figure 3 (e.g., the transceivers), and a skilled artisan would recognize that the “programmable logic” of the Altera FPGA could be used for financial applications, including high-frequency trading. *Id.*



A POSA seeking to implement the Altera FPGA for high-frequency trading would have a reasonable expectation of success. Ex. 1002 at ¶ 218. An FPGA is programmable, meaning the computational circuitry can be programmed for whatever function the user desires. Ex. 1005 at 256 (The “logic array block (LAB) in the Stratix® V core fabric . . . is composed of basic building blocks known as adaptive logic modules (ALMs) that you can configure to implement logic functions, arithmetic functions, and register functions.”); Ex. 1016 at 39 (“an FPGA provides a blank slate of bitwise functional units that can be programmed to create any desired circuit or processor”). Therefore, a skilled artisan would recognize that the Altera FPGA’s programmable logic could be used to process financial data in high-frequency trading. Ex. 1002 at ¶ 218.

To the extent that a POSA would not have understood that the features of Stratix FPGA and Si5345 PLL are necessarily present in Altera, a POSA would have been motivated to combine Altera, the Stratix Handbook, and the Si5345 Manual for the reasons discussed above, *see* Ground 1A above, and would have would have implemented this combination for the purposes and applications described in Lockwood for all the same reasons discussed in this section. Ex. 1002 at ¶ 219.

2. Claim 1 preamble: “a first serial data stream comprising market data” and “a second serial data stream comprising order entry data”

Lockwood discloses “a first serial data stream comprising market data” and “a second serial data stream comprising order entry data.” Ex. 1002 at ¶¶ 220-223. As described in Ground 1, Altera discloses first serial data received by the deserializer and second serial data transmitted from the FPGA system. *See* Claim 1(a) and 1(o) above.

A POSA would have been motivated by Lockwood to use Altera in trading applications. In a trading setting, a POSA would understand that the purpose of the FPGA system would be to consume market data such that an algorithm implemented in the FPGA can determine the orders to transmit to the marketplace. *Id.* at ¶ 221; Ex. 1007 at 1 (“Traders receive multiple high-data rate UDP/IP market data streams over the network from trading venues.”), 2 (“HFT strategies therefore require low-latency market access both to receive market data as well as to transmit new orders.”). In that application, the first serial data would include market data—e.g., price and quantity-related data for orders and executions by market participants in a financial instrument, as reported by a trading venue, such as bid, asks, trades, and options auction notifications. Ex. 1002 at ¶ 221; Ex. 1001 at 26:58-60, 27:17-19. For example, Lockwood Figure 2 showed the first serial data as “market feed(s)” entering the FPGA. Ex. 1007 at 3; *see also id.* at Figure 3.

The second serial data would include order entry data—e.g., data related to entering orders to purchase or sell stocks, commodities, goods, and/or services. Ex. 1002 at ¶ 222; Ex. 1001 at 26:58-60. Lockwood Figure 2 showed the second serial data as “[o]rders back to the market” exiting the FPGA system. Ex. 1007 at 3; *see also id.* at 1 (“The final step is to enter these orders into the exchange”), Fig. 3.

A POSA would understand that the set of operations used on the market data to generate the order entry data would be trading algorithms—e.g., a set of rules implemented in the FPGA to determine which orders to send for execution in financial markets. Ex. 1002 at ¶ 223. Lockwood Figure 2 showed that “Trading Algorithm(s)” are implemented in the FPGA computational circuitry. Ex. 1007 at 3; *see also id.* at 1 (“Traders employ a range of algorithms and heuristics to decide when and what to trade. These approaches combine current market data with historical data and outputs from computational models.”), Fig. 3.

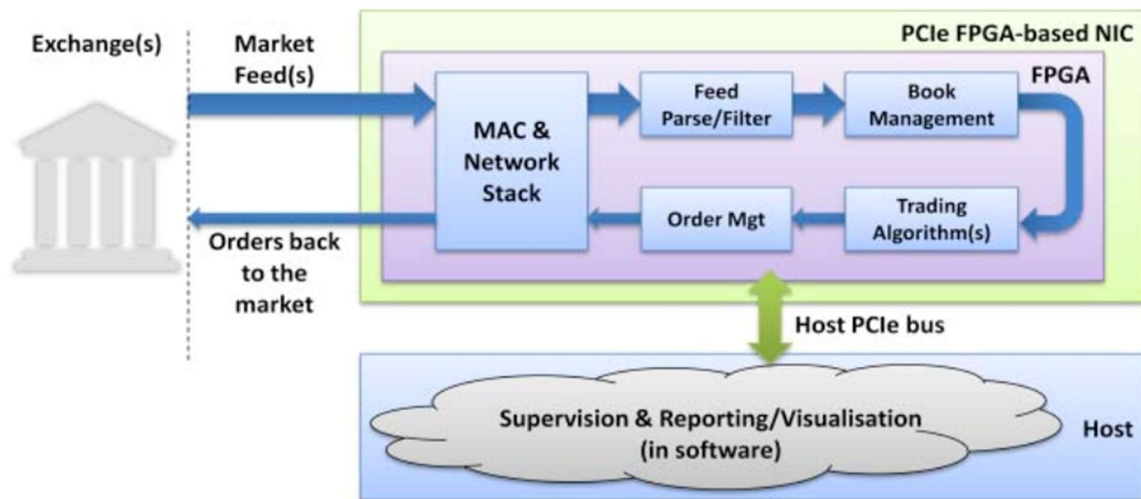


Figure 2 Typical Smart NIC in a supervised financial trading application

3. Claim 20: “The method of claim 1, wherein the first serial data stream includes market data and the second serial data stream includes trading data”

Lockwood discloses the “method of claim 1, wherein the first serial data stream includes market data and the second serial data stream includes trading data.” Ex. 1002 at ¶¶ 224-225. Lockwood’s disclosed “orders back to the market” constitutes “trading data.” Ex. 1007 at 1 (“we survey existing solutions and describe how FPGAs are being used in electronic trading to approach the goal of zero latency”), *id.* (“Traders monitor these streams, reconstructing pricing and demand for relevant stocks, options, futures and currencies to determine when and what to trade. Buy/Sell orders are then sent to the exchange as soon as possible.”). For the same reasons described above regarding order entry data, Lockwood discloses this limitation.

4. Claim 1(k) and 1(l): It Would Have Been Obvious to Use the Computational Circuitry Present in Altera

To the extent that a POSA would not have understood that Altera describes using the computational circuitry of the Stratix FPGA—e.g., in claim limitations 1(k) and 1(l)—a POSA would have been motivated to use the Stratix computational circuitry with Altera. Ex. 1002 at ¶¶ 226-233.

Claims 1(k) and 1(l)

Altera and Lockwood teach “transmitting, by the serializer to the computational circuitry, the first transmitter side clock signal” and “performing, by the computational circuitry, a first set of operations on at least a portion of the first plurality of data items to generate a second plurality of parallel data streams comprising a second amount of data streams.” Ex. 1002 at ¶¶ 226-233.

The Stratix FPGA contains a “logic array block (LAB) in the Stratix[®] V core fabric.” Ex. 1005 at 256. The logic array block “is composed of basic building blocks known as adaptive logic modules (ALMs) that you can configure to implement logic functions, arithmetic functions, and register functions.” *Id.* As explained above, that logic array block is the computational circuitry within Altera. Ex. 1002 at ¶ 228. It would have been obvious and beneficial for a POSA to put this computational circuitry to use in the Altera solution. *Id.* at ¶¶ 230-231.

One key benefit of an FPGA relative to other integrated circuits is that an FPGA is programmable, meaning that a customer can configure the FPGA to carry

out any operations it needs, rather than the internal circuitry being fixed in manufacturing. *Id.* at ¶¶ 34-40, 230. In the case of Altera, it would be obvious that a customer using the SyncE solution would use the programmable FPGA computational circuit to perform operations on the incoming data. *Id.* at ¶ 230. For example, another Altera SyncE white paper discloses that “[i]n this system, the programmable logic in the FPGA is loaded with a design that includes one or more Ethernet cores, along with any other application logic needed on the card.” Ex. 1013 at 2; *see also* Ex. 1016 at 39 (“an FPGA provides a blank slate of bitwise functional units that can be programmed to create any desired circuit or processor”).

Lockwood reinforces that conclusion. Ex. 1002 at ¶¶ 232-233. Lockwood Figure 3 depicted financial applications (e.g., trading algorithms) implemented in the programmable logic of the FPGA. Lockwood explained that “FPGAs offer the performance benefits of custom hardware while retaining programmability,” such that “[t]rading algorithms can be continually improved.” Ex. 1007 at 4; *see also id.* at 2 (“Flexibility is also vital to enable trading platforms to adapt to changing market conditions and trading strategies.”). Accordingly, it would have been obvious to perform operations using the programmable computational circuitry of the Stratix FPGA in Altera. Ex. 1002 at ¶¶ 226-233.

5. Claims 2, 8, 10, 11, and 19

Altera and Lockwood would make obvious claims 2, 8, 10, 11, and 19, which depend on claim 1, for the same reasons that Altera and Lockwood make claim 1 obvious as described above. *See also* Ground 1A (explaining how the additional limitations of claims 2, 8, 10, 11, and 19 are taught by Altera).

IX. CONCLUSION

Petitioner respectfully requests that inter partes review of the '286 patent be instituted and that the challenged claims be canceled as unpatentable.

Dated: January 9, 2026

Respectfully submitted,

/Meg E. Fasulo/

Meg E. Fasulo (Reg. No. 75,820)
Lead Counsel for Petitioner

CERTIFICATE OF WORD COUNT AND TYPE STYLE

Under the provisions of 37 CFR § 42.24(d), the undersigned hereby certifies that the Microsoft Office word count for the foregoing Petition, excluding the table of contents, table of authorities, certificate of word count, and certificate of service, totals 13,948 words, which is less than the words allowed under 37 C.F.R. § 42.24(b)(1).

This Petition complies with the general format requirements of 37 C.F.R. § 42.6(a) and has been prepared using Microsoft Word in 14-point Times New Roman.

Dated: January 9, 2026

Respectfully submitted,

/Meg E. Fasulo/

Meg E. Fasulo (Reg. No. 75,820)
Lead Counsel for Petitioner

CERTIFICATE OF SERVICE

In accordance with 37 C.F.R. §§ 42.6(e) and 42.105, the undersigned certifies that a complete and entire copy of the PETITION FOR INTER PARTES REVIEW OF CLAIMS 1, 2, 8, 10-11, 19, AND 20 OF U.S. PATENT NO. 10,931,286 UNDER 35 U.S.C. §§ 311-319 AND 37 C.F.R. §§ 42.100 ET SEQ. including exhibits and testimony relied upon were served on Patent Owner via FedEx overnight at the correspondence address of record for the subject patent, as included below:

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