IN THE UNITED STATES DISTRICT COURT
FOR THE NORTHERN DISTRICT OF ILLINOIS
EASTERN DIVISION

HFT SOLUTIONS, LLC, Plaintiff, v. CITADEL SECURITIES LLC, Defendant.	Case No. 1:24-cv-13213 JURY TRIAL DEMANDED

DEFENDANT CITADEL SECURITIES LLC'S FINAL INVALIDITY CONTENTIONS

Defendant Citadel Securities LLC sets forth its final invalidity contentions according to Local Patent Rule 3.1.

INTRODUCTION

Plaintiff HFT Solutions, LLC brought this action for purported infringement of three patents that relate to field-programmable gate arrays, or FPGAs. As set forth below, the Asserted Claims are invalid as anticipated by the prior art, obvious in light of the prior art to a person of ordinary skill in the art, claiming ineligible subject matter, and failing to meet the enablement and written description requirements and indefiniteness.

On December 16, 2025, HFT served its final infringement contentions and asserted the following claims:

- U.S. Patent No. 10,931,286 – claims 1, 2, 8, 10-11, and 19-20
- U.S. Patent No. 11,128,305 – claims 1, 3, 7, and 20-22
- U.S. Patent No. 11,575,381 – claims 1-4 and 10-12

Citadel Securities contends that it does not infringe any claim of the Asserted Patents. Citadel Securities also contends that each of the Asserted Claims is invalid under 35 U.S.C. § 101 for ineligible subject matter, and that each of the Asserted Claims is invalid as anticipated by the prior art under 35 U.S.C. §102, obvious based on the prior art under §103, invalid under §112, and/or under §§ 115 and 116 for improper inventorship.

These invalidity contentions address the claims identified in HFT's final infringement contentions. Citadel Securities reserves the right to modify, amend, or supplement these final invalidity contentions to the extent the Court permits HFT to amend, supplement, or otherwise modify its final infringement contentions.

Further, HFT's final infringement contentions are deficient and fail to provide allegations as to how the accused products infringe each and every claim limitation. Rather, they simply parrot the claim language and then cite and provide figures from various documents—and in some circumstances, point to no evidence at all. Further, HFT cites documents relating to only the accused Bittware XUP-VV8 product; it cites no documents at all concerning the accused AMD/Xilinx Alveo UL-3524 and Alveo UL-3422 products, and in fact does not chart those products other than to mention them in a footnote. HFT therefore has prejudiced Citadel Securities' ability to understand, for purposes of preparing these final invalidity contentions, what HFT alleges to be the scope of the Asserted Claims. Citadel Securities reserves the right to amend these final invalidity contentions if and when HFT provides proper infringement contentions as to each Asserted Claim.

Nothing in these final invalidity contentions is intended, nor should be construed, as waiver of any claim construction argument or non-infringement position or response to HFT's use of figures from various documents in its charts. Citadel Securities' statements herein (including the accompanying charts) reflect Citadel Securities' understanding of the purported potential scope of the claims that HFT appears to be advocating in its final infringement contentions. Citadel Securities' statements herein are not to be construed as acquiescence to HFT's interpretation of any claims or claim terms.

Nothing herein shall be interpreted as an admission that: (1) the Asserted Claims are infringed by any of the instrumentalities Citadel Securities uses; (2) any particular feature or aspect of any of the accused instrumentalities practices any limitation of the Asserted Claims; (3) there is § 112 support for any limitation of the Asserted Claims; or (4) any of HFT's proposed or implied constructions are supportable.

A. Priority Date

These final invalidity contentions are based on the earliest priority dates as identified by HFT in its final infringement contentions. Nothing in these final invalidity contentions shall be understood as an agreement that any Asserted Patent or Asserted Claim is entitled to claim priority on the dates identified by HFT, or to any continuation or provisional application. Citadel Securities reserves the right to amend these final invalidity contentions and identify additional prior art references if HFT is permitted by the Court to later assert an earlier priority date.

Any reference to an "asserted priority date" or a "priority date" in these final invalidity contentions refers to the priority dates identified in HFT's final infringement contentions. Reference to a "priority date" or an "asserted priority date" should not be construed to mean that Citadel Securities agrees that any of the Asserted Patents or Asserted Claims are in fact entitled to such priority date, or that HFT has provided proper notice as to its contentions for a priority date. Citadel Securities reserves the right to rely on additional documents, evidence, and expert testimony, including, without limitation, the documents cited in HFT's final infringement contentions in the event that HFT fails to establish that any Asserted Claim of any Asserted Patent is entitled to its asserted priority date.

To the extent HFT alleges that any prior art relied on in these final invalidity contentions does not actually qualify as prior art to an Asserted Patent, HFT reserves the right to rebut those allegations.

Asserted Patent	**Asserted Priority Date**
'286 patent	November 5, 2018
'305 patent	November 5, 2018

’381 patent	November 5, 2018

B. Claim Construction

Citadel Securities’ final invalidity contentions are based on (1) Citadel Securities’ present understanding of the Asserted Claims, and (2) the claim constructions HFT appears to be using based on the infringement contentions, all without regard to whether Citadel Securities agrees with HFT’s apparent or expressed claim constructions. Citadel Securities reserves the right to supplement or otherwise amend these final invalidity contentions in response to any Court-ordered clarifications on claim constructions, any report from any expert witness for HFT regarding the scope of the claims, any briefing filed by HFT relating to the scope of the claims, and any position taken by HFT concerning claim scope, infringement, or invalidity.

In the respective invalidity charts, Citadel Securities identified terms that it contends are governed by 35 U.S.C. § 112(f), as set forth in Local Patent Rule 2.3(b)(3). Citadel Securities otherwise takes no position on any matter of claim construction in these final invalidity contentions. If Citadel Securities’ disclosures herein are consistent with any explicit, apparent, or implied claim constructions in HFT’s final infringement contentions, no inference is intended and no inference should be drawn that Citadel Securities agrees with any of HFT’s claim constructions. Any statement herein describing or tending to describe any claim element is provided solely for the purpose of understanding and/or applying the cited prior art. In addition, to the extent that these final invalidity contentions rely on or otherwise embody a particular order in which the steps of method claims are performed, Citadel Securities does not necessarily propose that the method claims must be limited to such order, although Citadel Securities may later propose such an order.

Nothing herein should be read to suggest that Citadel Securities agrees that any particular claim term is sufficiently definite, enabled or supported by the written description to meet the

requirements of 35 U.S.C. § 112. Likewise, nothing herein should be read to suggest that Citadel Securities agrees that the preamble of any claim is or is not limiting.

Because any positions taken in these disclosures are based on the claim scope apparently asserted by HFT in its final infringement contentions, with which Citadel Securities may disagree, Citadel Securities may take positions with respect to claim construction issues that are inconsistent with, or even contradictory to, positions expressed or implied in these final invalidity contentions.

Prior art not included in these final invalidity contentions, whether or not now known to Citadel Securities, might become relevant depending on the claim constructions proposed by HFT, Citadel Securities, and/or the Court's claim construction rulings. Citadel Securities reserves all rights to supplement or modify the positions and information in these final invalidity contentions, including, without limitation, the prior art and grounds of invalidity set forth herein, after the Court has construed any term of the Asserted Claims.

C. Ongoing Discovery and Supplementation

Citadel Securities bases these final invalidity contentions on information ascertained to date and its current knowledge and understanding of the Asserted Patents, HFT's final infringement contentions, and other facts and information available as of the date of these contentions. Citadel Securities reserves all rights to modify, supplement, or further amend the disclosures herein to reflect information that is obtained in the future or on the Court's claim construction.

Citadel Securities' investigation into prior art—including prior art identified in these disclosures, third-party prior art (including system art and related evidence), documents, and knowledgeable witnesses—is ongoing. Furthermore, Citadel Securities anticipates seeking and obtaining discovery, including third-party discovery, that further evidences and supports the invalidity of the Asserted Claims. Thus, Citadel Securities expects to revise, amend, and/or

supplement these final invalidity contentions accordingly in a manner consistent with the Federal Rules of Civil Procedure and the Court's rules and applicable orders.

Furthermore, Citadel Securities is investigating and pursuing information from additional sources of discovery that may bear on prior art and other aspects of potential invalidity, and may serve discovery requests on those sources if necessary. Citadel Securities reserves the right to revise, amend, and/or supplement these final invalidity contentions with any relevant information obtained from those additional sources.

Citadel Securities further reserves the right to rely on statements or admissions from those owing a duty of candor, such as the named inventor, prosecution counsel, and others involved in the prosecution of the patent applications or related applications, concerning the scope of the prior art relevant to the Asserted Patents found in, among others, the following: the respective prosecution histories of the Asserted Patents and related patent applications; deposition testimony of the named inventor; and the papers filed and any evidence submitted by HFT in connection with this litigation.

Further, these disclosures are prepared prior to the Court's claim construction ruling and disclosure of claim construction positions from HFT. Citadel Securities' positions on invalidity of particular claims will depend on how the claims are construed by the Court. Citadel Securities reserves the right to supplement or further amend its contentions based on claim construction positions taken by HFT or any construction adopted by the Court. Citadel Securities' contentions herein should not be seen as a suggestion that HFT's reading of the patent claims, such as it can be determined, is correct.

Prior art not identified in this disclosure, whether known or not known to Citadel Securities, may become relevant, including prior art concerning the state of the art at the time of invention, as

well as simultaneous or near-simultaneous independent invention by others. For instance, Citadel Securities currently is unaware of the extent, if any, to which HFT will contend that limitations of the Asserted Claims are not disclosed in the prior art identified by Citadel Securities. To the extent that such an issue arises, Citadel Securities reserves the right to identify other references that would disclose, practice, or render obvious the allegedly missing limitation(s) of the disclosed subject matter.

D. Prior Art

In these final invalidity contentions, Citadel Securities identifies specific portions of prior art references that disclose every element of the Asserted Claims. Citadel Securities has endeavored to cite to the most relevant portions of the identified prior art. Other portions of the identified prior art may additionally disclose, either expressly or inherently, and/or render obvious one or more elements or limitations of the Asserted Claims. While Citadel Securities has identified exemplary prior art references for each element, it does not necessarily identify every disclosure of the same element in each prior art reference. A person of ordinary skill in the art would read a prior art reference as a whole and in the context of other publications, literature, and general knowledge in the field and would rely upon other information including other publications and general scientific or engineering knowledge. Citadel Securities therefore reserves the right to rely upon other unidentified or uncited portions of the prior art references and on other publications and prior art products and expert testimony to provide context and to aid in the understanding and interpretation of the identified portions of the prior art.

Citadel Securities also reserves the right to rely upon (1) other portions of the cited prior art references, other publications, prior art products, and the testimony of experts to establish that the alleged inventions would have been obvious to a person of ordinary skill in the art, including on the basis of modifying or combining certain cited references; (2) admissions relating to prior

art in the Asserted Patents or related patents, the prosecution history of the Asserted Patents or related patents, or other admissions obtained during discovery; (3) foreign counterparts of any U.S. patents identified in Citadel Securities' final invalidity contentions; and (4) any prior art references, other publications, prior art products, and the testimony of experts to establish that the alleged inventions would have been obvious to a person of ordinary skill in the art used during any reexamination, inter partes review, post-grant review, or any other proceeding at the Patent Office involving the Asserted Patents. Where a prior art reference includes citations to other references, those other references are considered incorporated by reference for context.

The prior art references discussed in the claim charts may disclose the elements of the Asserted Claims explicitly and/or inherently, and/or they may be relied upon to show the state of the art in the relevant time frame. These statements are not to be construed to suggest that any prior art reference included in the combinations is not by itself anticipatory. The suggested obviousness combinations are provided in the alternative to Citadel Securities' anticipation contentions.

In addition to the above, where Citadel Securities identifies in the claim charts a particular figure in a prior art reference, the identification should be understood to encompass the caption and description of the figure as well as any text relating to the figure in the specification and prosecution history in addition to the figure itself. Similarly, where an identified portion of text refers to a figure or other material, the identification should be understood to include the referenced figure or other material as well.

E. No Patentable Weight

Citadel Securities reserves the right to argue that various portions of the Asserted Claims, such as an intended use or result, nonfunctional descriptive material, and certain preamble language, are entitled to no patentable weight. Mapping of a portion of an Asserted Claim to a

prior art reference does not represent that such portion of the claim is entitled to patentable weight when comparing the claimed subject matter to the prior art.

Nothing herein should be read to suggest that Citadel Securities agrees that any particular claim term is sufficiently definite, enabled or supported by the written description to meet the requirements of 35 U.S.C. § 112. In addition, nothing herein admits in any way that any of Citadel Securities' accused products infringe any of the Asserted Claims. Citadel Securities reserves the right to amend and supplement these final invalidity contentions, including in response to any amendments to, and revisions of, HFT's final infringement contentions or application of the Asserted Claims. Citadel Securities further reserves the right to supplement its corresponding document production should it later find additional, responsive documents.

CONTENTIONS

I. Invalidity Under §§ 102 and 103

Citadel makes the following invalidity contentions based on information ascertained to date and reserves the right to modify, supplement, or further amend the disclosures contained herein based on the Court's claim construction or to reflect information that is ascertained in the future.

Citadel Securities contends that the Asserted Claims are invalid as anticipated by the prior art under 35 U.S.C. § 102 and/or as obvious in view of the prior art, the knowledge of a person having ordinary skill in the art, and/or secondary factors of obviousness under 35 U.S.C. § 103.

The obviousness combinations of references provided in Citadel Securities' invalidity claim charts under 35 U.S.C. § 103 are exemplary and are not intended to be exhaustive. In particular, Citadel Securities is currently unaware of the extent, if any, to which HFT will contend that limitations of the Asserted Claims are not disclosed in the art identified by HFT as anticipatory. To the extent an issue arises with any such limitation, Citadel Securities will identify

other obviousness combinations and/or other references that would have made obvious the addition of the allegedly missing limitation to the disclosed device, system, or method of operation.

Citadel Securities reserves the right to present additional items of prior art under 35 U.S.C. § 102 and/or 35 U.S.C. § 103 located during the course of discovery or further investigation. For example, Citadel Securities expects to issue subpoenas to third parties believed to have knowledge, documentation, and/or corroborating evidence concerning some of the prior art listed below and/or additional prior art. These third parties include without limitation the authors, inventors, or assignees of the references listed in these disclosures.

A patentee bears the burden of production with respect to evidence of secondary considerations of non-obviousness. *See ZUP, LLC v. Nash Mfg., Inc.*, 896 F.3d 1365, 1373 (Fed. Cir. 2018). As of the date of these final invalidity contentions, HFT has not identified any evidence of secondary considerations, nor does HFT offer any evidence or explanation to support its allegations. As shown in these final invalidity contentions, other companies and individuals described, built, and/or patented the exact same concepts in the Asserted Patents before HFT ever did—often many years before. Even where others' invention(s) occurred around the same time as the Asserted Patents, such simultaneous invention demonstrates the obviousness of the Asserted Patents.

Potentially relevant evidence includes any prior art reference cited herein that was publicly known or available before or around the alleged inventions claimed in the Asserted Patents. This also includes any prior art asserted in these final invalidity contentions that Citadel Securities is able to pre-date based on its asserted priority dates by proving, inter alia, corroborated conception and diligent reduction to practice.

Citadel Securities reserves all rights to further respond to any secondary considerations of non-obviousness raised by HFT, including by updating, modifying, and/or adding to these final invalidity contentions. Citadel Securities is not aware of any unexpected results, long-felt need, commercial success (or any nexus to any allegedly successful commercial embodiment), or awards for the alleged inventions of the Asserted Patents.

A. State of the Art

The subject matter of the Asserted Claims was well understood to those of skill in the art as of the respective priority dates of the Asserted Patents. To describe the state of the art at the time of the alleged inventions, in addition to the references listed on the face of the Asserted Patents and those references listed below and charted in Exhibits A through D, Citadel Securities may rely on any admitted prior art discussed in the Asserted Patent and file histories. The background state of the art includes that which is set forth in the patent, the file history, and the prior art references disclosed herein. A more detailed discussion is provided below.

Field Programmable Gate Arrays

An integrated circuit, colloquially known as a "chip," is a series of electrical components etched onto a semiconductor, used for data storage and processing. Prior to the introduction of integrated circuits in 1960, electrical functions were isolated into individual transistors, which were time-consuming and difficult to create, and represented only part of an entire circuit's functionality. The introduction of the integrated circuit allowed an entire circuit, including the transistors, to be etched onto a singular device.

Field Programmable Gate Arrays (FPGAs) are versatile integrated circuits whose configuration can be altered after they have been released by the manufacturer. As hardware, they have a processing speed advantage over software. The FPGA can be reprogrammed in the field, and is therefore more flexible than an integrated circuit designed for a singular purpose. FPGAs

have been commercially available since at least 1985, with the density of their transistors increasing over time. Used for telecommunications in the 1990s, FPGAs are now often used for low-latency trading and in the automotive and aerospace industries.

Clock Domain Crossing Circuits

Circuits that include FPGAs receive data as electrical signals, execute a designated set of operations, and transmit the resulting data as a separate electrical signal off the circuit. The outgoing data is synchronized with an external clock signal, also called the reference clock. The FPGA's input, however, often runs on a separate clock, which is known as the receiver-side clock signal. Therefore, the data received by the FPGA must be synchronized from the receiver-side clock signal to the reference clock.

The original method of synchronizing the processed data from a FPGA to the reference clock used additional circuits. Specifically, through that method, the processed data is transmitted from the FPGA to a clock domain crossing circuit (or "synchronizer"), which transmits the processed data through additional circuits to bring the data into alignment with the reference clock. Clock domain crossing circuits developed in the 1970s as a way to synchronize clock signals. *See* Chaney, T.J. and Molnar, C.E., *Anomalous Behavior of Synchronizer and Arbiter Circuits*, 22 IEE Transactions on Computers 421 (1973). Although effective, this method introduces latency as the data moves through the additional circuits, a challenge which researchers sought to address. *See* Dobkin, Rostislav, Ginosar, Ran, *Fast Universal Synchronizers*, PATMOS 199 (2008).

Phase Lock Loops

A phase lock loop (PLL) is an alternate way to synchronize a reference clock signal with a receiver-side clock without using a clock domain crossing circuit. PLLs are a type of circuit which internally implements a feedback loop to align a generated clock with an input clock. PLLs can be

"internal," meaning the PLL is located inside the FPGA itself, or "external," meaning the PLL is located on the same board as the FPGA, but not within the chip itself.

PLLs were first developed in the 1930s in order to synchronize a receiver radio's frequency with the transmitter's frequency, preventing frequency drift over time. The devices were used for televisions in the 1940s, missile tracking in the 1950s, and eventually, to synchronize data beginning in the 1970s. They have been described as "common" since the early 2010s, *see Phase-Locked Loop Design Through the Decades*, Embedded (Sept. 20, 2011), https://www.embedded.com/phase-locked-loop-design-through-the-decades-part-1/. Indeed, "millions of PLLs are now used in virtually all digital communication systems, from satellites to mobile phones, as well as in many other applications such as clock generation for microprocessors." *See* Althoff, Matthias, Rajhans, Ashkay, et al., *Formal Verification of Phase-Locked Loops Using Reachability Analysis and Coninuization*, Communications of the ACM (Oct. 1, 2013), https://cacm.acm.org/research/formal-verification-of-phase-locked-loops-using-reachability-analysis-and-continuization/.

B. Identification of Prior Art

Citadel Securities identifies in the chart further below the prior art now known to Citadel Securities that anticipate or render obvious one or more of the Asserted Claims. Each of the identified patents, publications, systems, and products is prior art under at least 35 U.S.C. § 102 (post-AIA). Citadel Securities' reliance on each prior art reference identified throughout these final invalidity contentions includes the reference itself, anything incorporated by the reference, and any testimony by those with knowledge of the reference, such as named authors and inventors. On information and belief, each listed document or item became prior art at least as early as the dates specified.

To the extent any limitation of any of the Asserted Claims is construed to have a similar meaning, or to encompass similar feature(s) and/or function(s), to any other claim limitation, and to the extent at least any claim chart in Exhibits B through L hereto identifies any prior art reference as disclosing or teaching one of the similarly construed claim limitations, such identified prior art reference and Citadel Securities' contentions with respect to the other similarly construed claim limitations are incorporated by reference.

Priority dates identified for the prior art references are based on information currently available to Citadel Securities, and Citadel Securities will amend this disclosure to the extent additional information becomes available.

To the extent that they are prior art, Citadel Securities reserves the right to rely upon (1) foreign counterparts of the U.S. Patents identified in Citadel Securities' final invalidity contentions, (2) U.S. counterparts of foreign patents and foreign patent applications identified in Citadel Securities' final invalidity contentions, and (3) U.S. and foreign patents and patent applications corresponding to articles and publications identified in Citadel Securities' final invalidity contentions.

The prior art identified below is exemplary. The claimed features are similarly described or disclosed in additional prior art. Thus, Citadel Securities reserves the right to rely on other evidence of the prior art beyond the example references identified herein.

The references identified below, and as further described in Exhibits B through L, each disclose, either expressly or inherently, every element of the Asserted Claims, thereby anticipating those claims. To the extent HFT contends that any reference does not anticipate the Asserted Claims, it would have been obvious to combine or modify these references with concepts from other prior art, as explained herein.

In particular, for each limitation of the Asserted Claims that HFT contends is not met by a particular reference, Citadel Securities contends that the limitation (and claim as a whole) is obvious based on a combination of that particular reference with (1) any other reference disclosing that limitation, (2) any admitted prior art, as explained in the background of each patent or discussed in the file history, (3) any reference identified in Exhibits B through L as disclosing that limitation, and/or (4) the knowledge of a person of ordinary skill in the art and/or any of the references and concepts discussed herein regarding the relevant background and state of the art. The specific combinations of prior art that Citadel Securities contends render the Asserted Claims obvious are readily determinable as described herein, which is the most efficient manner of identifying the combinations. Citadel Securities' obviousness grounds for each dependent claim incorporate the obviousness grounds for the claim(s) on which the dependent claim depends in addition to any obviousness grounds identified in the charts for the dependent claim.

Citadel Securities does not yet have the benefit of HFT's positions on the prior art, including which (if any) elements it contends are missing in each prior art reference, whether HFT agrees that a reference is in fact prior art, and whether HFT agrees that a person of ordinary skill in the art would be motivated to combine specific references. Citadel Securities reserves the right to supplement these obviousness positions (including identifying additional prior art combinations and the associated reasons to combine) as discovery in the case progresses, including expert discovery.

1. Prior Art Patents and Publications – LPR 2.3(b)(1)

1. Orthogone/REFLEX CES XpressVUP. XpressVUP is prior art that is described in a printed publication, in public use, on sale, or otherwise available to the public before the effective filing date of the '286 patent. In particular, XpressVUP is a product that was developed by Reflex CES and/or Orthogone, as reflected in the documents referenced below. Altera is prior art to the

asserted patents under at least AIA 35 U.S.C. § 102(a)(1). Documents showing the operation of XpressVUP include but are not limited to:

- The Ultra-Low Latency FPGA Solution for Electronic Trading and Networking Applications White Paper – Xilinx UltraScale + FPGA ("XpressVUP White Paper") (CITADEL_HFT_0002812)
- XpressVUP – LP5P Data Sheet ("XpressVUP Data Sheet") (CITADEL_HFT_0002180)
- UltraScale Architecture GTY Transceivers User Guide, UG578 (v1.3) September 20, 2017 ("Transceiver User Guide") (CITADEL_HFT_0002366)
- Any-Frequency, Any-Output Jitter-Attenuators/Clock Multiplies Si5345, Si5344, Si5342 Family Reference Manual ("Si5345 Reference Manual") (CITADEL_HFT_0002183)

2. Altera® SyncE solution consisting of Altera's Stratix® V FPGA interoperating with Silicon Labs' 5345 jitter-attenuating phase-locked loop (PLL) ("Altera"). Altera is prior art that is described in a printed publication, in public use, on sale, or otherwise available to the public before the effective filing date of the '286 patent. In particular, Altera is a product that was developed by Altera and Silicon Labs, as reflected in the documents referenced below. Altera is prior art to the asserted patents under at least AIA 35 U.S.C. § 102(a)(1). Documents showing the operation of XpressVUP include but are not limited to:

- Synchronous Ethernet Solutions with Altera FPGAs and Silicon Labs Jitter-Attenuating PLLs ("Altera White Paper") (CITADEL_HFT_0004708)
- Stratix V Device Handbook ("Stratix Handbook") (CITADEL_HFT_0004128)

- Any-Frequency, Any-Output Jitter-Attenuators/Clock Multiplies Si5345, Si5344, Si5342 Family Reference Manual ("Si5345 Reference Manual") (CITADEL_HFT_0002183)
- Altera Phase-Locked Loop (Altera PLL) IP Core User Guide, August 1, 2014 (CITADEL_HFT_0004049)
- Altera Low Latency Ethernet 10G MAC IP Core Migration Guidelines, May 4, 2015 (CITADEL_HFT_0004065)
- Transceiver Signal Integrity Development Kit, Stratix V GX Edition User Guide, July 2012 (CITADEL_HFT_0004076)

3. High Precision Timing IP Core developed by Eduardo Mendes for use with Xilinx FPGAs ("Mendes"). Mendes is prior art that is described in a printed publication, in public use, or otherwise available to the public before the effective filing date of the '286 patent. In particular, Mendes is a product that was developed by Mendes for use in Xilinx FPGAs, as reflected in the documents referenced below. Altera is prior art to the asserted patents under at least AIA 35 U.S.C. § 102(a)(1). Documents showing the operation of Mendes include but are not limited to:

- HPT IP Core for High-Speed Links Using Xilinx FPGAs ("HPT IP Core") (CITADEL_HFT_0002143)
- Tx Phase Aligner for Xilinx transceivers (CITADEL_HFT_0004715)
- UltraScale Architecture GTY Transceivers User Guide, UG578 (v1.3) September 20, 2017 ("Transceiver User Guide") (CITADEL_HFT_0002366)
- Any-Frequency, Any-Output Jitter-Attenuators/Clock Multiplies Si5345, Si5344, Si5342 Family Reference Manual ("Si5345/44/42 Reference Manual") (CITADEL_HFT_0002183)

- Implementing the High Precision Timing IP for Xilinx Ultrascale, September 19, 2018 (CITADEL_HFT_0004691)

4. Xilinx VCU118 Evaluation Board ("VCU118"). Xilinx VCU118 was in public use, on sale, and/or otherwise available to the public by January 3, 2018. Xilinx VCU118 is prior art to the asserted patents under at least AIA 35 U.S.C. § 102(a)(1). Documents showing the operation of Mendes include but are not limited to:

- VCU118 Evaluation Board User Guide, UG1224 (v1.5) March 15, 2023 ("VCU118 User Guide v1.5") (AMD-HFT-00000254-AMD-HFT-00000385)
- UltraScale Architecture GTY Transceivers User Guide, UG578 (v1.3) September 20, 2017 ("Transceiver User Guide") (CITADEL_HFT_0002366)
- Si5328 Skyworks ITU-T G.8262 Synchronous Ethernet Jitter- Attenuating Clock Multiplier, Rev. 1.0 ("Si5328 Manual") (AMD-HFT-00000002-AMD-HFT-00000071)
- Skyworks ANY-FREQUENCY PRECISION CLOCKS Si5316, Si5319, Si5322, Si5323, Si5324, Si5325, Si5326, Si5327, Si5328, Si5365, Si5366, Si5367, Si5368, Si5369, Si5374, Si5375, Si5376 FAMILY REFERENCE MANUAL, Rev. 1.3 10.16 ("Si53xx-RM") (AMD-HFT-00000072-AMD-HFT-00000253)
- VCU118 Evaluation Board User Guide, UG1224 (V1.4) October 17, 2018 ("VCU118 User Guide v1.43") (AMD-HFT-00000386-AMD-HFT-00000518)
- VCU118 Evaluation Board User Guide, UG1224 (v1.0) December 15, 2016 ("VCU118 User Guide v1.0") (AMD-HFT-00001401-AMD-HFT-00001564)
- VCU118 Evaluation Board User Guide, UG1224 (v1.1) October 31, 2017 ("VCU118 User Guide v1.13") (AMD-HFT-00001565-AMD-HFT-00001735)

- VCU118 Evaluation Board User Guide, UG1224 (v1.2) November 10, 2017 ("VCU118 User Guide V1.2") (AMD-HFI-00001736-AMD-HFT-00001906)
- VCU118 Evaluation Board HW-UI-VCU118 (XCVU9P-2FLGA2104) Schematic, Ver. 1.0, Rev. 01 ("CU118 Schematic Ver. 1.0") (AMD-HFT-00000519-AMD-HFT-00000594)
- VCU118 Evaluation Board HW-U1-VCU118 (XCVU9P-2FLGA2104) Schematic, Ver. 1.1, Rev. 02 ("VCU118 Schematic Ver. 1.1") (AMD-HFT-00000595-AMD-HFT-00000670)
- VCU118 Evaluation Board HW-U1-VCU118 (XCVU9P-2FLGA2104) Schematic, Ver. 2.0, Rev. 03 ("VCU118 Schematic Ver. 2.0") (AMD-HFT-00000671-AMD-HFT-00000746
- VCU118 Rev 1.1 Change Doc (AMD-HFT-00000747-AMD-HFT-00000749)
- VCU118 Rev 2.0 Change Doc (AMD-HFT-00000750-AMD-HFT-00000752)

5. "A Low-Latency Library in FPGA Hardware for High-Frequency Trading (HFT)" by John W. Lockwood (CITADEL_HFT_0004732)

Citadel Securities reserves the right to rely on the prior art disclosed above, as well as other art, to show, for example, the state of the art in the relevant time frame.

2. Prior Art Systems

Citadel Securities identifies the following systems—including constituent software, hardware, methods, and processes—as prior art that anticipate or render obvious the Asserted Claims of these patents. Each system was in public use, on sale, or otherwise available to the public before the effective filing date of the Asserted Patents.

Evidence of public use and/or sale of the listed system art includes webpages and data sheets from the time of the alleged invention, for example as saved on the Internet Archive, and/or certain patents related to these systems. Exemplary documents have been produced herewith. Discovery is ongoing and Citadel Securities will supplement as discovery continues.

Product	**Date Offered or Publicly Used or Known**
Orthogone/REFLEX CES XpressVUP	No later than November 2018
Altera® SyncE solution consisting of Altera's Stratix® V FPGA interoperating with Silicon Labs' 5345 jitter-attenuating phase-locked loop (PLL) ("Altera")	No later than November 2015
High Precision Timing IP Core developed by Eduardo Mendes for use with Xilinx FPGAs ("Mendes")	No later than June 26, 2018
Xilinx VCU118	No later than January 3, 2018

C. Invalidating Prior Art – LPR 2.3(b)(2)

Based on currently available information, and without the benefit of the Court's construction of the asserted patent claims under *Markman v. Westview Instruments, Inc.*, 52 F.3d 967 (Fed. Cir. 1995) (en banc), *aff'd*, 517 U.S. 370 (1996), Citadel Securities currently contends that asserted claims 1, 2, 8, 10-11, and 19-20 of the '286 patent are invalid based on at least the following prior art grounds:

Claims 1, 2, 8, 10-11, and 19-20 are anticipated under 35 U.S.C. § 102 by, and/or obvious under 35 U.S.C. § 103 over, Orthogone/REFLEX CES XpressVUP.

Claims 1, 2, 8, 10-11, and 19-20 are anticipated under 35 U.S.C. § 102 by, and/or obvious under 35 U.S.C. § 103 over, Altera, optionally combined with Lockwood.

Claims 1, 2, 8, 10-11, and 19-20 are anticipated under 35 U.S.C. § 102 by, and/or obvious under 35 U.S.C. § 103 over, Mendes, optionally combined with Lockwood.

Claims 1, 2, 8, 10-11, and 19-20 are anticipated under 35 U.S.C. § 102 by, and/or obvious under 35 U.S.C. § 103 over, VCU118, optionally combined with Lockwood.

Based on currently available information, and without the benefit of the Court's construction of the asserted patent claims under *Markman v. Westview Instruments, Inc.*, 52 F.3d 967 (Fed. Cir. 1995) (en banc), *aff'd*, 517 U.S. 370 (1996), Citadel Securities currently contends that asserted claims 1, 3, 7, and 20-22 of the '305 patent are invalid based on at least the following prior art grounds:

Claims 1, 3, 7, and 20-22 are anticipated under 35 U.S.C. § 102 by, and/or obvious under 35 U.S.C. § 103 over, Orthogone/REFLEX CES XpressVUP.

Claims 1, 3, 7, and 20-22 are anticipated under 35 U.S.C. § 102 by, and/or obvious under 35 U.S.C. § 103 over, Altera, optionally combined with Lockwood.

Claims 1, 3, 7, and 20-22 are anticipated under 35 U.S.C. § 102 by, and/or obvious under 35 U.S.C. § 103 over, Mendes, optionally combined with Lockwood.

Claims 1, 3, 7, and 20-22 are anticipated under 35 U.S.C. § 102 by, and/or obvious under 35 U.S.C. § 103 over, VCU118, optionally combined with Lockwood.

Based on currently available information, and without the benefit of the Court's construction of the asserted patent claims under *Markman v. Westview Instruments, Inc.*, 52 F.3d 967 (Fed. Cir. 1995) (en banc), *aff'd*, 517 U.S. 370 (1996), Citadel Securities currently contends that asserted claims 1-4 and 10-12 of the '381 patent are invalid based on at least the following prior art grounds:

Claims 1-4 and 10-12 are anticipated under 35 U.S.C. § 102 by, and/or obvious under 35 U.S.C. § 103 over, Orthogone/REFLEX CES XpressVUP.

Claims 1-4 and 10-12 are anticipated under 35 U.S.C. § 102 by, and/or obvious under 35 U.S.C. § 103 over, Altera, optionally combined with Lockwood.

Claims 1-4 and 10-12 are anticipated under 35 U.S.C. § 102 by, and/or obvious under 35 U.S.C. § 103 over, Mendes, optionally combined with Lockwood.

Claims 1-4 and 10-12 are anticipated under 35 U.S.C. § 102 by, and/or obvious under 35 U.S.C. § 103 over, VCU118, optionally combined with Lockwood.

D. Claim Charts – LPR 2.3(b)(3)

Charts specifically identifying where each element of each Asserted Claim is found in the prior art, either expressly or inherently, are found in Exhibits B through L. However, this prior art is exemplary. The claimed features are similarly described or disclosed in other prior art.

- Exhibit A-1, A-2, A-3 – Invalidity based on Orthogone/REFLEX CES XpressVUP
- Exhibit B-1, B-2, B-3 – Invalidity based on Altera
- Exhibit C-1, C-2, C-3 – Invalidity based on Mendes
- Exhibit D-1, D-2, D-3 – Invalidity based on VCU118

In the claim charts included in this disclosure, Citadel Securities identifies specific portions of prior art references that disclose or render obvious the elements of the Asserted Claims. Although Citadel Securities has identified at least one citation per element, each and every disclosure of the same element in a given reference is not necessarily identified. That Citadel Securities did not identify each similar disclosure should not be construed as a concession by Citadel Securities that such disclosure is not relevant. It should be recognized that a person of ordinary skill in the art would generally read a prior art reference as a whole and in the context of

other publications, literature, and general knowledge in the field. To understand and interpret any specific statement or disclosure in a prior art reference, a person of ordinary skill in the art would rely upon other information including other publications and general scientific or engineering knowledge.

Where Citadel Securities identifies a particular figure in a prior art reference, the identification should be understood to encompass the caption and description of the figure as well as any text relating to the figure in the specification and prosecution history in addition to the figure itself. Similarly, where an identified portion of text refers to a figure or other material, the identification should be understood to include the referenced figure or other material as well.

Certain pieces of identified prior art disclose features of the Asserted Claims inherently. Citadel Securities may rely on any evidence, including expert testimony, to establish the inherency of certain features of the prior art to invalidate the Asserted Claims.

E. Anticipation and Obviousness

Each of the references listed above render these patents anticipated under 35 U.S.C. § 102, or at least obvious in view of the knowledge of a person of ordinary skill in the art. In addition, these references may be combined with each other to render these patents obvious under 35 U.S.C. § 103. One of ordinary skill in the art would be motivated to combine these references as explained below.

No showing of a specific motivation to combine prior art is required to combine the references disclosed in the attached charts. There was a reason to make each combination, each combination of art would have produced no unexpected results, and each combination at most would simply represent a known alternative to one of ordinary skill in the art. *See KSR Int'l Co. v. Teleflex, Inc.*, 550 U.S. 398, 414-18 (2007) (rejecting the Federal Circuit's "rigid" application of the teaching, suggestion, or motivation to combine test instead espousing an "expansive and

flexible" approach). Indeed, the Supreme Court held that a person of ordinary skill in the art is "a person of ordinary creativity, not an automaton" and "in many cases a person of ordinary skill in the art will be able to fit the teachings of multiple patents together like a pieces of a puzzle." *Id.* at 420–21.

In view of *KSR*, the Patent and Trademark office issued a set of new Examination Guidelines. *See* Examination Guidelines for Determining Obviousness Under 35 U.S.C. § 103 in View of the Supreme Court Decision in *KSR International Co. v. Teleflex Inc.*, 72 Fed. Reg. 57,526 (Oct. 10, 2007). Those Guidelines identified various rationales for finding a claim obvious, including:

a) Combining prior art elements according to known methods to yield predictable results;

b) Simple substitution of one known element for another to obtain predictable results;

c) Use of known technique to improve similar devices (methods, or products) in the same way;

d) Applying a known technique to a known device (method, or product) ready for improvement to yield predictable results;

e) "Obvious to try"—choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success;

f) Known work in one field of endeavor may prompt variations of it for use in either the same field or a different one based on design incentives or other market forces if the variations would have been predictable to one of ordinary skill in the art;

g) Some teaching, suggestion, or motivation in the prior art that would have led one of ordinary skill to modify the prior art reference or to combine prior art reference teachings to arrive at the claimed invention.

Id. at 57,529.

One or more combinations of the prior art references identified above would have been obvious because these references would have been combined using: known methods to yield predictable results; known techniques in the same way; a simple substitution of one known, equivalent element for another to obtain predictable results; and/or a teaching, suggestion, or motivation in the prior art generally. In addition, it would have been obvious to try combining the prior art references identified above because there were only a finite number of predictable solutions and/or because known work in one field of endeavor prompted variations based on predictable design incentives and/or market forces either in the same field or a different one. In addition, the combination of the prior art references identified above would have been obvious because the combination represents the known potential options with a reasonable expectation of success.

Additional evidence that there would have been a motivation to combine the prior art references identified above includes the interrelated teachings of multiple prior art references; the effects of demands known to the design community or present in the marketplace; the existence of a known problem for which there was an obvious solution encompassed by the asserted claims; the existence of a known need or problem in the field of the endeavor at the time of the invention(s); and the background knowledge that would have been possessed by a person having ordinary skill in the art.

Thus, the motivation to combine the teachings of the prior art references disclosed herein is found in the references themselves and in: (1) the nature of the problem being solved; (2) the express, implied and inherent teachings of the prior art; (3) the knowledge of persons of ordinary skill in the art; (4) the predictable results obtained in combining the different elements of the prior art; (5) the predictable results obtained in simple substitution of one known element for another; (6) the use of a known technique to improve similar devices, methods, or products in the same way; (7) the predictable results obtained in applying a known technique to a known device, method, or product ready for improvement; (8) the finite number of identified predictable solutions that had a reasonable expectation of success; and (9) known work in various technological fields that could be applied to the same or different technological fields based on design incentives or other market forces.

Any reference or combination of references that anticipates or makes obvious an asserted independent claim also makes obvious any asserted claim dependent on that independent claim because every element of each dependent claim was known by a person of ordinary skill at the time of the alleged invention, and it would have been obvious to combine those known elements with the independent claims at least as a matter of common sense and routine innovation.

In addition, the motivation to combine or modify prior art references is significantly stronger when, as here, the references seek to solve the same problem, come from the same field, and correspond well. *See In re Inland Steel Co.*, 265 F.3d 1354, 1362 (Fed. Cir. 2001) (allowing two references to be combined as invalidating art under similar circumstances where the art "focus[ed] on the same problem . . . [,] c[a]me from the same field of art [and] . . . the identified problem found in the two references correspond[ed] well").

Citadel Securities has identified several exemplary motivations and reasons to combine the various references cited herein, and those motivations would have been supported, in part, by a reasonable expectation of success. The various teachings, suggestions, and/or reasons to modify any of the references and/or to combine any two or more of the references in Exhibits A through D come from various sources, including the prior art (specific and as a whole), common knowledge, common sense, predictability, expectations, industry trends, design incentives or need, market demand or pressure, market forces, the nature of the problem faced, and/or the knowledge possessed by one of ordinary skill in the art. In addition, it would have been obvious to try combining the prior art references identified above.

These exemplary combinations demonstrate that there were only a finite number of predictable solutions to known problems addressed by the Asserted Patents. Furthermore, known work in one field or endeavor prompted variations based on predictable design incentives and/or market forces either in the same field or a different one. The combination of features found in the prior art references identified in these contentions would have been obvious because the claimed combinations represent the known potential options, with each such option having a reasonable expectation of success. Additionally, one of ordinary skill in the art would have been motivated to create combinations identified in these contentions using: known methods to yield predictable results; known techniques in the same way; a simple substitution of one known, equivalent element for another to obtain predictable results; and/or teaching, suggestion, or motivation in the prior art generally. Also, market forces in the industry, and the desire to improve features and performance, would have motivated the addition of features to systems as they became available, became less expensive, became more commonly used, provided better performance and reliability, reduced costs, or predictably achieved other clearly desirable results.

To the extent HFT alleges that any other claimed limitation or limitations are not disclosed in any reference, it would have been obvious to combine the teachings of the reference with the background knowledge of a person of ordinary skill in the art and/or it would have been obvious to incorporate the missing limitation(s), including as disclosed in Exhibits B through L, into the reference for the reasons disclosed herein. For example, one of ordinary skill in the art would have found substantial motivation to combine one or more of the references with one more of each other or the secondary references in order to disclose the alleged inventions recited in the Asserted Claims. Each of the references disclosed herein as invalidating an Asserted Patent was directed at the same or similar field of technology and the same or similar problem as that Asserted Patent.

To the extent HFT alleges that any particular claim limitation is not disclosed or inherent in the charted references, it would have been obvious to combine the charted reference with one or more of the references identified herein for the particular claim limitations. Also, as Citadel Securities is currently unaware of the extent, if any, to which HFT will contend that limitations of the Asserted Claims are not disclosed in the art identified herein as anticipatory, Citadel Securities reserves the right to identify other references and combinations that may render an allegedly missing limitation obvious. In addition, if and to the extent that HFT challenges the relevance of any of these references with respect to particular limitations of the Asserted Claims of the Asserted Patents, Citadel Securities reserves its right to identify further motivation to combine particular references with additional particularity.

In particular, the motivation to combine FPGAs with external PLLs was explicitly discussed in the prior art. *See* Fred Hirning, *Improve FPGA communications interface clock jitters with external PLLs* (Sept. 20, 2014), https://www.embedded.com/improve-fpga-communications-interface-clock-jitters-with-external-plls/ (noting that there are a variety of issues with PLLs

internal to FPGAs and "[t]he answer to these clocking issues is to take low noise PLLs externally"); 2013 Silicon Labs white paper, Choosing the Optimal Internal or External Clocking Solution for FPGA-Based Designs ("Ultimately, it is up to the hardware engineer to select the right combination of internal and external clocking solutions for their FPGA-based applications. Now more than ever, hardware designers have a wide range of timing choices (see Table 1) to choose from to optimize their next design."). Thus, a person of ordinary skill in the art would be motivated to use FPGAs with an external PLL. The Orthogone/REFLEX CES XpressVUP product, as well as the other cited prior art, is evidence of such a motivation to combine, as it includes the Xilinx Virtex UltraScale+ FPGA and the Si5345 PLL.

In addition, it was common knowledge before the asserted patents that FPGA-based systems are useful for performing high-frequency trading operations, as even the patent acknowledges. '381 patent at 1:42-44 ("FPGAs are used in the financial industry in high frequency trading where the rapid processing of the FPGA is desired."). Lockwood demonstrates how, even as early as 2012, a skilled artisan would have put Altera to use for such trading.

Lockwood emphasized, back in 2012, "the race to minimize latency in high frequency trading." Lockwood at 7. Lockwood further noted that, in high-frequency trading, "[a] custom-designed datapath in an FPGA circuit offers the benefits of minimal, deterministic processing times down to clock cycles," which are the smallest unit of time in which logic operations can occur. *Id.* at 8. In a regime like high-frequency trading in which even a few clock cycles can make a difference, a skilled artisan would have recognized that Altera offers a solution that eliminates the latency cost associated with clock-domain crossing circuits. *See id.* at 2 ("[T]he first few players to execute orders may be the only ones able to profit from a given opportunity" and "reduction in latency can improve arbitrage profitability"); "The Race to Zero Latency for High

Frequency Trading" by Saul Sahoo at 1 ("HFT is all about speed and minimizing latency: the faster you can run trading strategies and algorithms for analyzing minute price changes and executing trade orders, the higher the probability to win over competition."); U.S. Patent No. 10,169,814 at 2:13-14 (cited on the face of the '381 patent and noting that speed of information delivery is a valuable dimension to the financial instrument trading and brokerage industry).

Additionally, Lockwood explained that, even as of 2012, "Ethernet is currently more prevalent in the HFT ecosystem" and "will continue to dominate for the foreseeable future"—and the passage of time has demonstrated this to be true. Lockwood at 2. Thus, long before 2018, as Lockwood demonstrated, a POSA would have been motivated to use products like Altera in high-frequency trading applications.

Lockwood provided several different examples in which a POSA would recognize that the Altera system could be utilized. For example, Lockwood described FPGA-based Smart Network Interface Controllers (NICs) as "another way to apply programmable logic" to the development of financial applications. "Smart NICs typically bring together high-speed network interfaces, a PCIe host interface, memory and an FPGA," and in this arrangement, "some of the processing" is "offload[ed]" to the FPGA. *Id.* at 8. Specifically, "[t]he FPGA implements the NIC controller, acting as the bridge between the host computer and the network and allows user-designed custom processing logic to be integrated directly into the data path." *Id.* at 3. This allowed a smart NIC to "function as a programmable trading platform." Id. at 11. A POSA would recognize that Altera, Mendes, and other FGPA systems could be used as the FPGA in Lockwood Figure 2 and the computational circuitry of the FPGA would "function as a programmable trading platform." *Id.*

A skilled artisan would also recognize that Altera would be an attractive option to use for the FPGA shown in the FPGA-based trading platform displayed in Lockwood's Figure 3, below.

A skilled artisan would recognize that the "programmable logic" of the FPGA products could be used for financial applications, including high-frequency trading. *Id.*

A POSA seeking to implement an FPGA like Altera and other products identified in these contentions for high-frequency trading would have a reasonable expectation of success. An FPGA is programmable, meaning the computational circuitry can be programmed for whatever function the user desires. *See, e.g.*, Stratix Handbook at 256 (The "logic array block (LAB) in the Stratix® V core fabric . . . is composed of basic building blocks known as adaptive logic modules (ALMs) that you can configure to implement logic functions, arithmetic functions, and register functions."); High-Frequency Trading, A Practical Guide to Algorithmic Strategies and Trading Systems by Irene Aldridge (2013) at 39 ("an FPGA provides a blank slate of bitwise functional units that can be programmed to create any desired circuit or processor"). Therefore, a skilled artisan would recognize that the Altera FPGA's programmable logic could be used to process financial data in high-frequency trading.

Citadel Securities has identified several exemplary motivations and reasons to combine the various references cited herein. For any reference for which there is a claim element that does not have a corresponding citation in that reference, it would be obvious to combine with the knowledge of a person of skill and/or any other reference in the charts for which there is a citation for that element. These combinations would have been obvious to try given that there were a finite number of identified, predictable solutions in the prior art, and there would have been a reasonable expectation of success to simply implement one prior art solution with concepts from prior art in the same field.

II. Invalidity Under § 112

The Asserted Claims are invalid under 35 U.S.C. § 112 as indefinite and for failing to satisfy the written description and enablement requirements. Citadel Securities reserves all rights

to amend these final invalidity contentions, including after the Asserted Claims are ultimately construed by the Court, in response to any interpretation of the Asserted Claims embodied in HFT's infringement positions, and/or to account for any changes in the law concerning invalidity under 35 U.S.C. § 112. Citadel Securities also reserves the right to provide additional explanation and/or argument for its final invalidity contentions under § 112, including, for example, based on expert testimony. Citadel Securities' contentions that the Asserted Claims are invalid under § 112 are not admissions regarding the construction or scope of the claims of the Asserted Patents, or that any of the claims of the Asserted Patents are not anticipated or rendered obvious by any prior art. All of the below statements are by way of example only. Any item disclosed below with respect to any patent or claim may, as appropriate, be asserted as a defense against any other patent or claim that has a similar claim limitation and patent disclosure.

A. Indefiniteness

Claims are indefinite under 35 U.S.C. § 112(b) when they "fail to inform, with reasonable certainty, those skilled in the art about the scope of the invention." *Nautilus, Inc. v. Biosig Instruments, Inc.*, 572 U.S. 898, 901 (2014). For example, to the extent an asserted apparatus claim includes both apparatus and method limitations, that claim is invalid for indefiniteness under § 112(b) because it fails to identify or notify the public of what constitutes direct infringement. *See IPXL Holdings, L.L.C. v. Amazon.com, Inc.*, 430 F.3d 1377 (Fed. Cir. 2005). Similarly, a claim that uses means-plus function claiming is indefinite "[i]f the patentee fails to disclose adequate corresponding structure." *Williamson v. Citrix Online, LLC*, 792 F. 3d 1339, 1352 (Fed. Cir. 2015). A claim can also be found indefinite if it uses terms of degree. *See Interval Licensing LLC v. AOL, Inc.*, 766 F.3d 1364, 1371 (Fed. Cir. 2014). As the Federal Circuit has "explained, a term of degree fails to provide sufficient notice of its scope if it depends 'on the unpredictable vagaries of any one

person's opinion.'" *Id.* (citation omitted). In addition, "a claim term that lacks an antecedent basis may . . . render a claim indefinite." *In re Downing*, 754 F. App'x 988, 996 (Fed. Cir. 2018).

Citadel Securities contends that the following Asserted Claims are invalid under § 112(b). Each Asserted Claim identified below (and each Asserted Claim that depends thereon) is invalid under § 112(b) because they fail to inform, with reasonable certainty, those skilled in the art about the scope of the claimed invention. For each listed term or phrase, Citadel Securities believes the term or phrase is invalid under § 112(b), and any limitation including such term or phrase is also indefinite.

1. '286 Patent

The following terms render one or more of the claims of the '286 patent invalid for indefiniteness under 35 U.S.C. § 112, as they fail to inform, with reasonable certainty, those skilled in the art about the scope of the claimed invention:

- Claim 1: "receiving, by a first plurality of data pins in a first interface of a field programmable gate array in the field programmable gate array system, the first serial data stream"
- Claim 1: "transmitting, from the first plurality of data pins in the first interface to a deserializer in the field programmable gate array, the first serial data stream"
- Claim 1: "generating, by the deserializer, a first receiver side clock signal having a second frequency and a second phase, based at least in part on the first clock signal"
- Claim 1: "the feedback clock signal having a third frequency and a third phase"
- Claim 1: "generating, by the phase detector, the first output based on a comparison of the first receiver side clock signal and the feedback clock signal obtained from the second clock signal"

- Claim 1: "generating, by the serializer, a first transmitter side clock signal based on the second clock signal"
- Claim 1: "converting, by the deserializer, the first serial data stream into a first plurality of parallel data streams"
- Claim 1: "generating, using the field programmable gate array system, a feedback clock signal associated with a first transmitter side clock signal, the feedback clock signal having a third frequency and a third phase"
- Claim 1: "transmitting, from the deserializer to the computational circuitry, the first plurality of data streams comprising a first plurality of data items and a first amount of data streams"
- Claim 1: "transmitting, from the serializer off the field gate programmable array system via a second plurality of data pins in the first interface, the second serial data stream"
- Claims 1 and 3: "operationally connected"
- Claim 8: "wherein a difference between the third phase and the second phase is less than a second threshold level"
- Claim 10: "the first set of operations does not include clock domain crossing operations that delay processing or the first set of parallel data streams."
- Claim 19: "the transmission of the second serial data stream from the serializer off the field programmable gate array is transmitted to an input/output module off the field programmable gate array"

For example, a POSA would not have understood, with reasonable certainty, the meaning and scope of the phrases "a first plurality of parallel data streams," "the first plurality of data

streams," and "the first set of parallel data streams." It is indefinite whether these three different terms represent the same or different data streams because there is no objective guidance as to whether they denote the same or different sets.

A POSA would not have understood, with reasonable certainty, the meaning and scope of the phrase "delay processing." For example, the phrase is a term of degree where there is no standard for measuring such degree with reasonable certainty provided in the specification or the prosecution history.

A POSA would not have understood, with reasonable certainty, the meaning and scope of the phrase "generating . . . a feedback clock signal." For example, a POSA would not have understood, with reasonable certainty: how "a feedback clock signal" is generated, such as what signals are used for generating the "feedback clock signal," or what steps are used to generate the "feedback clock signal."

A POSA would not have understood, with reasonable certainty, the meaning and scope of the phrases "a first threshold level" and "a second threshold level." For example, the phrases are terms of degree where there is no standard for measuring such degree with reasonable certainty provided in the specification or the prosecution history.

A POSA would not have understood, with reasonable certainty, the meaning and scope of the phrase "generating, by the serializer, a first transmitter side clock signal based on the second clock signal." For example, it is indefinite whether the first transmitter side clock signal generated based on the second clock signal is the same as or different from the first transmitter side clock signal associated with the feedback clock signal.

A POSA would not have understood, with reasonable certainty, the meaning and scope of the phrase "a first threshold level." For example, the phrase is a term of degree where there is no

standard for measuring such degree with reasonable certainty provided in the specification or the prosecution history.

A POSA would not have understood, with reasonable certainty, the meaning and scope of the phrase "the transmission of the second serial data stream . . . is transmitted to an input/output module." It is indefinite how the transmission of the second serial data stream can be transmitted.

Additionally, claim 1 of the '286 patent lacks proper antecedent basis for "the computational circuitry," "the first plurality of data streams," "the first transmitter side clock signal," and "the serializer" and is therefore indefinite. Claim 10 of the '286 patent lacks proper antecedent basis for "the first set of parallel data streams" and is therefore indefinite.

2. '305 Patent

The following terms render one or more of the claims of the '286 patent invalid for indefiniteness under 35 U.S.C. § 112, as they fail to inform, with reasonable certainty, those skilled in the art about the scope of the claimed invention:

- Claim 1: "a first plurality of data pins, wherein said first plurality of data pins is configured to receive a first serial data stream"
- Claim 1: "a second plurality of data pins, wherein said second plurality of data pins is configured to transmit a second serial data stream"
- Claim 1: "the deserializer is configured to . . . generate a first receiver side clock signal based on the first clock signal, wherein the first receiver side clock signal has a third frequency and a third phase"
- Claim 1: "convert the first serial data stream into a first plurality of parallel data streams having a first amount of data streams"

- Claim 1: “the second reference clock pin to receive as a third input a first wire rate clock signal, based on the second clock signal, having a fourth frequency and a fourth phase”
- Claim 1: “the serializer is configured to . . . generate the first transmitter side clock signal, based on the first wire rate signal, having the fifth frequency and the fifth phase, wherein the fifth frequency is different than and less than the fourth frequency”
- Claim 1: “a third clock signal having a sixth frequency”
- Claim 1: “compare the third phase of the receiver side clock signal to a sixth phase of a third clock signal having a sixth frequency”
- Claim 1: “generate a phase difference indicator signal based on a difference between the third phase of the receiver side clock signal and the sixth phase of the third clock signal”
- Claim 1: “wherein the third clock signal and the receiver side clock signal are phase aligned so that there is a fixed phase difference between the third phase and the sixth phase”
- Claim 2: “wherein the fifth frequency corresponds to sixth frequency and the fifth phase third clock signal corresponds to the sixth phase”
- Claim 3: “wherein the second clock output pin is configured to transmit the third clock signal”
- Claim 3: “wherein the fifth frequency corresponds to sixth frequency and the fifth phase third clock signal corresponds to the sixth phase”

- Claim 7: "the first set of operations does not include clock domain crossing operations that delay processing the first set of parallel data streams"

For example, from the patent specification, a POSA would not have understood, with reasonable certainty, the meaning and scope of the phrase "said second reference clock pin is configured to receive a second clock signal" and "the second reference clock pin to receive…a first wire rate clock signal, based on the second clock signal" because the patent specification fails to describe whether the first wire rate clock signal is received through a pin and how the same clock pin (i.e., the second reference clock pin) can receive both of the second clock signal and the first wire rate clock signal where one signal (i.e., the first wire rate clock signal) is based on the other signal (i.e., the second clock signal).

A POSA would not have understood, with reasonable certainty, the meaning and scope of the phrases "a first plurality of parallel data streams," "the first plurality of data streams," and "the first set of parallel data streams." It is indefinite whether these three different terms represent the same or different data streams because they are used without definition throughout the '305 patent claims.

A POSA would not have understood, with reasonable certainty, the meaning and scope of the phrase "delay processing." For example, the term is a word of degree where there is no standard for measuring such degree with reasonable certainty.

A POSA would not have understood, with reasonable certainty, the meaning and scope of the phrase "fifth phase third clock signal."

Claim 2 of the '305 patent lacks proper antecedent basis for "sixth frequency" and "third clock signal" and is indefinite. Claim 3 of the '305 patent lacks proper antecedent basis for "sixth frequency" and "third clock signal" and is indefinite. Claim 7 of the '305 patent lacks proper

antecedent basis for "the first set of parallel data streams" and is indefinite. Claim 20 of the '305 patent lacks proper antecedent basis for "the first operation" and is indefinite.

3. '381 Patent

The following terms render one or more of the claims of the '381 patent invalid for indefiniteness under 35 U.S.C. § 112, as they fail to inform, with reasonable certainty, those skilled in the art about the scope of the claimed invention:

- Claim 1: "converting, by the deserializer, the first serial data stream into a first plurality of parallel data streams"
- Claim 1: "generating, by the deserializer, a receiver side clock signal"
- Claim 1: "generating, using the phase lock loop, a second clock signal"
- Claim 1: "said method does not use clock domain crossing operations that delay processing of the first set of parallel data streams"
- Claim 1: "transmitting, from the field programmable gate array system, the second serial data stream, derived from the second plurality of parallel data streams"
- Claim 1: "generating, within the field programmable gate array, a transmitter side clock signal derived from the second clock signal"
- Claim 1: "performing, by the computational circuitry, a set of operations on at least a portion of the first plurality of parallel data streams to generate a second plurality of parallel data streams"

A POSA would not have understood, with reasonable certainty, the meaning and scope of the phrase "a first plurality of parallel data streams," "the first set of parallel data streams," and "the first plurality of data streams." It is indefinite whether these three different terms represent the same or different data streams because all three different terms are recited throughout the

claims of the ’381 patent. For the same reasons, a POA would not have understood, with reasonable certainty, the meaning and scope of the phrase “the second plurality of parallel data streams” and “the second plurality of data streams.” It is indefinite whether these two different terms represent the same or different data streams.

Additionally a POSA would not have understood, with reasonable certainty, the meaning and scope of the phrase “delay processing.” For example, the term is a word of degree where there is no standard for measuring such degree with reasonable certainty.

Additionally, claim 1 of the ’381 patent lacks proper antecedent basis for “the first set of parallel data streams” and is therefore indefinite. Claim 10 of the ’381 patent lacks proper antecedent basis for “the first plurality of data streams” and “the second plurality of data streams” and is therefore indefinite.

B. Lack of Written Description Support

35 U.S.C. § 112(a) requires that the specification contain a written description of the invention. “[T]he hallmark of written description is disclosure.” *Boston Sci. Corp. v. Johnson & Johnson*, 647 F.3d 1353, 1361-62 (Fed. Cir. 2011) (citation omitted). “To satisfy the written description requirement, the applicant must convey with reasonable clarity to those skilled in the art that, as of the filing date sought, he or she was in possession of the invention, and demonstrate that by disclosure in the specification of the patent.” *Novozymes A/S v. DuPont Nutrition Biosciences APS*, 723 Fed. 1336, 1344 (Fed. Cir. 2013) (internal quotation marks omitted); *see also Ariad Pharms., Inc. v. Eli Lilly and Co.*, 598 F.3d 1336, 1351 (Fed. Cir. 2010) (en banc); *Boston Scientific*, 647 F.3d at 1362.

1. ’286 Patent

The following terms render one or more of the claims of the ’286 patent invalid for lack of written description under 35 U.S.C. § 112, as the specification of the ’286 patent does not demonstrate that the inventors were in possession of the claimed subject matter:

- Claim 1: “the feedback clock signal having a third frequency and a third phase”
- Claim 1: “generating, by the phase detector, the first output based on a comparison of the first receiver side clock signal and the feedback clock signal obtained from the second clock signal”

2. ’305 Patent

The following terms render one or more of the claims of the ’305 patent invalid for lack of written description under 35 U.S.C. § 112, as the specification of the ’305 patent does not demonstrate that the inventors were in possession of the claimed subject matter:

- Claim 1: “compare the third phase of the receiver side clock signal to a sixth phase of a third clock signal having a sixth frequency”
- Claim 1: “generate a phase difference indicator signal based on a difference between the third phase of the receiver side clock signal and the sixth phase of the third clock signal”
- Claim 1: “wherein the third clock signal and the receiver side clock signal are phase aligned so that there is a fixed phase difference between the third phase and the sixth phase”
- Claim 3: “wherein the second clock output pin is configured to transmit the third clock signal”

- Claim 3: "wherein the fifth frequency corresponds to sixth frequency and the fifth phase third clock signal corresponds to the sixth phase"

3. '381 Patent

The following terms render one or more of the claims of the '381 patent invalid for lack of written description under 35 U.S.C. § 112, as the specification of the '381 patent does not demonstrate that the inventors were in possession of the claimed subject matter:

- Claim 1: "generating, using the phase lock loop, a second clock signal"

C. Lack of Enablement

The enablement requirement of § 112 demands that the patent specification enable "those skilled in the art to make and use the full scope of the claimed invention without 'undue experimentation.'" *Genentech, Inc. v. Novo Nordisk A/*S, 108 F.3d 1361, 1365 (Fed. Cir. 1997) (quoting *In re Wrigh*t, 999 F.2d 1557, 1561 (Fed. Cir. 1993)). "[T]he scope of the claims must be less than or equal to the scope of the enablement." *Nat'l Recovery Tech., Inc. v. Magnetic Separation Sys., Inc.*, 166 F.3d 1190, 1196 (Fed. Cir. 1999). In other words, the claims must be enabled over their entire claimed range. *See id.* (finding lack of enablement because the "claim [] [was] broader than the enablement as taught in the specification").

The asserted claims are invalid for lack of enablement under 35 U.S.C. § 112 as the specifications do not enable a person of ordinary skill in the art to make the asserted inventions because they do not specify, among other things: (1) all of the connections that need to be made between the various components; (2) the way the PLL needs to be configured; and (3) the way the serializer and deserializer need to be configured and sequenced

1. '286 Patent

The following terms render one or more of the claims of the '286 patent invalid for lack of enablement under 35 U.S.C. § 112, as the specification of the '286 patent does not enable those

skilled in the art to make and use the full scope of the claimed invention without undue experimentation:

- Claim 1: "generating, by the deserializer, a first receiver side clock signal having a second frequency and a second phase, based at least in part on the first clock signal"
- Claim 1: "the feedback clock signal having a third frequency and a third phase"
- Claim 1: "generating, by the phase detector, the first output based on a comparison of the first receiver side clock signal and the feedback clock signal obtained from the second clock signal"
- Claim 1: "generating, by the serializer, a first transmitter side clock signal based on the second clock signal"
- Claim 8: "wherein a difference between the third phase and the second phase is less than a second threshold level"
- Claim 10: "wherein the first set of operations does not include clock domain crossing operations that delay processing of the first set of parallel data streams"

The asserted claims of the '286 patent, as Citadel Securities best understands HFT's contentions at this time, are invalid under 35 U.S.C. § 112(a) because the patent specification of the '286 patent fails to describe the manner and process of making and using the invention so as to enable a POSA to make and use the full scope of the invention without undue experimentation. For example, the patent specification fails to describe the manner and process of making and using the claimed invention regarding at least the claim terms and phrases identified above and with respect to indefiniteness above, for similar reasons described above.

2. ’305 Patent

The following terms render one or more of the claims of the ’305 patent invalid for lack of enablement under 35 U.S.C. § 112, as the specification of the ’305 patent does not enable those skilled in the art to make and use the full scope of the claimed invention without undue experimentation:

- Claim 1: “a first plurality of data pins, wherein said first plurality of data pins is configured to receive a first serial data stream”
- Claim 1: “a second plurality of data pins, wherein said second plurality of data pins is configured to transmit a second serial data stream”
- Claim 1: “the deserializer is configured to . . . generate a first receiver side clock signal based on the first clock signal, wherein the first receiver side clock signal has a third frequency and a third phase”
- Claim 1: “the second reference clock pin to receive as a third input a first wire rate clock signal, based on the second clock signal, having a fourth frequency and a fourth phase”
- Claim 1: “the serializer is configured to . . . generate the first transmitter side clock signal, based on the first wire rate signal, having the fifth frequency and the fifth phase, wherein the fifth frequency is different than and less than the fourth frequency”
- Claim 1: “a phase detector operationally connected to the first clock output pin such that the phase detector is configured to”
- Claim 1: “a third clock signal having a sixth frequency”

- Claim 1: "compare the third phase of the receiver side clock signal to a sixth phase of a third clock signal having a sixth frequency"
- Claim 1: "generate a phase difference indicator signal based on a difference between the third phase of the receiver side clock signal and the sixth phase of the third clock signal"
- Claim 1: "wherein the third clock signal and the receiver side clock signal are phase aligned so that there is a fixed phase difference between the third phase and the sixth phase"
- Claim 3: "wherein the second clock output pin is configured to transmit the third clock signal"
- Claim 3: "wherein the fifth frequency corresponds to sixth frequency and the fifth phase third clock signal corresponds to the sixth phase"

The asserted claims of the '305 patent, as Citadel Securities best understands HFT's contentions at this time, are invalid under 35 U.S.C. § 112(a) because the patent specification of the '305 patent fails to describe the manner and process of making and using the invention so as to enable a POSA to make and use the full scope of the invention without undue experimentation. For example, the patent specification fails to describe the manner and process of making and using the claimed invention regarding at least the claim terms and phrases identified above and with respect to indefiniteness above, for similar reasons described above.

3. '381 Patent

The following terms render one or more of the claims of the '381 patent invalid for lack of enablement under 35 U.S.C. § 112, as the specification of the '381 patent does not enable those

skilled in the art to make and use the full scope of the claimed invention without undue experimentation:

- Claim 1: "generating, by the deserializer, a receiver side clock signal"
- Claim 1: "generating, using the phase lock loop, a second clock signal"
- Claim 1: "wherein said method does not use clock domain crossing operations that delay processing of the first set of parallel data streams"

The asserted claims of the '381 patent, as Citadel Securities best understands HFT's contentions at this time, are invalid under 35 U.S.C. § 112(a) because the patent specification of the '381 patent fails to describe the manner and process of making and using the invention so as to enable a POSA to make and use the full scope of the invention without undue experimentation. For example, the patent specification fails to describe the manner and process of making and using the claimed invention regarding at least the claim terms and phrases identified above and with respect to indefiniteness above, for similar reasons described above.

III. Invalidity Under § 101

As detailed in Citadel Securities' motion to dismiss, the Asserted Patents are directed to patent-ineligible subject matter. *See* Dkt. 30; Dkt. 39. The claims of the Asserted Patents cover receiving, transmitting, generating, and converting data and signals to synchronize "clocks." Fundamentally, the claims are about manipulating data, a concept which numerous courts have recognized is abstract. *See, e.g.*, *iLife Techs., Inc. v. Nintendo of Am., Inc.*, 839 F. App'x 534, 536 (Fed. Cir. 2021) ("We have routinely held that claims directed to gathering and processing data are directed to an abstract idea."); *Glasswall Solutions Ltd. v. Clearswift Ltd.*, 754 F. App'x 996, 998 (Fed. Cir. 2018) ("The claims merely require the conventional manipulation of information by a computer. We have often held similar conventional data manipulation to be abstract."). And

there is nothing about the claims that would transform them into any more than the abstract idea at their core. The claims use well-known computer components that have been in existence for decades in the conventional ways they were designed to be used. *See Chamberlain Grp., Inc. v. Techtronic Indus. Co.*, 935 F.3d 1341, 1349 (Fed. Cir. 2019) (nothing transformative where claims "could be performed with off-the-shelf technology").

IV. Unenforceability

Citadel Securities is not presently asserting that the Asserted Patents are unenforceable. However, discovery is in the beginning stages, and Citadel Securities reserves the right to supplement these unenforceability contentions in response to facts learned through the discovery process.

V. Accompanying Document Production

Citadel Securities is concurrently producing prior art references and corroborating evidence concerning prior art systems, including CITADEL_HFT_0004049 through CITADEL_HFT_0004739. Citadel Securities' search for prior art references, additional documentation, and/or corroborating evidence concerning prior art systems is ongoing. Accordingly, Citadel Securities reserves the right to continue to supplement its production as Citadel Securities obtains additional prior art references, documentation, and/or corroborating evidence concerning invalidity during the course of discovery.

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Respectfully submitted,

/s/ Meg E. Fasulo

Sean W. Gallagher (IL Bar No. 6239367)
Mark L. Levine (IL Bar No. 6201501)
Meg E. Fasulo (IL Bar No. 6320595)
Matthew R. Ford (IL Bar No. 6292833)
Rachel Smith (*pro hac vice*)
BARTLIT BECK LLP
54 West Hubbard Street, Suite 300
Chicago, IL 60654
Telephone: (312) 494-4400
sean.gallagher@bartlitbeck.com
mark.levine@bartlitbeck.com
meg.fasulo@bartlitbeck.com
matthew.ford@bartlitbeck.com
rachel.smith@bartlitbeck.com

Taylor J.S. Kelson (*pro hac vice*)
BARTLIT BECK LLP
1801 Wewatta St., Suite 1200
Denver, CO 80202
Telephone: (303) 592-3100
taylor.kelson@bartlitbeck.com

Attorneys for Defendant Citadel Securities LLC