

Exhibit B-1 to Citadel Securities' Invalidity Contentions:
Invalidity of U.S. Patent No. 10,931,286 based on Altera

As described in the following claim chart, claims 1, 2, 8, 10-11, and 19-20 of U.S. Patent No. 10,931,286 are invalid under 35 U.S.C. §§ 102 and/or 103 in view of the Altera® SyncE solution consisting of Altera's Stratix® V FPGA interoperating with Silicon Labs' 5345 jitter-attenuating phase-locked loop (PLL) ("Altera").¹ Altera is prior art that is described in a printed publication, in public use, on sale, or otherwise available to the public before the effective filing date of the '286 patent. In particular, Altera is a product that was developed by Altera and Silicon Labs, as reflected in the documents referenced below.

Documents showing the operation of Altera include but are not limited to:

- Synchronous Ethernet Solutions with Altera FPGAs and Silicon Labs Jitter-Attenuating PLLs ("Altera White Paper") (CITADEL_HFT_0004708)
- Stratix V Device Handbook ("Stratix Handbook") (CITADEL_HFT_0004128)
- Any-Frequency, Any-Output Jitter-Attenuators/Clock Multiplies Si5345, Si5344, Si5342 Family Reference Manual ("Si5345 Reference Manual") (CITADEL_HFT_0002183)
- Altera Phase-Locked Loop (Altera PLL) IP Core User Guide, August 1, 2014 (CITADEL_HFT_0004049)
- Altera Low Latency Ethernet 10G MAC IP Core Migration Guidelines, May 4, 2015 (CITADEL_HFT_0004065)
- Transceiver Signal Integrity Development Kit, Stratix V GX Edition User Guide, July 2012 (CITADEL_HFT_0004076)

Citations to particular documents or passages are merely exemplary of where each limitation is found. Citadel Securities reserves the right to rely on other documents or passages providing comparable evidence of how Altera alone or in combination with other prior art and general knowledge renders the '286 patent claims invalid. Citadel Securities intends to offer expert testimony and opinions establishing the general knowledge of a person of ordinary skill in the art, known design objectives, motivations to combine references and elements within the general knowledge of a POSA, the state-of-the-art, how a POSA would understand the disclosures of the cited prior art references, and any secondary considerations/objective indicia identified by HFT.

To the extent that Altera is found not to anticipate one or more of the claims of the '286 patent, those claims are obvious in view of Altera alone or in combination with other prior art references, such as "A Low-Latency Library in FPGA Hardware for High-

¹ The analysis in this chart is based, in part, on HFT's proposed claim constructions and the apparent claim scope required to support HFT's infringement contentions. Nothing in this chart should be interpreted as conceding that HFT's claim constructions or interpretation of claim scope are correct or supported by intrinsic or extrinsic evidence. Nor should this chart be interpreted as conceding that claim terms are definite or that claim preambles are limiting.

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Frequency Trading (HFT)'' by John W. Lockwood, and/or the general knowledge of a POSA and commonly understood design objectives, including, *inter alia*, the desire to reduce delays associated with using clock-domain crossing operations by incorporating a PLL external to an FPGA. Motivation to combine these references is provided in the references themselves. Citadel Securities' Invalidation Contentions provide additional details regarding the motivation to combine Altera with these Lockwood and/or the general knowledge of a POSA.

Citadel Securities also incorporates by reference the petition for institution of IPR2026-00151 for additional details about how claims 1, 2, 8, 10-11, and 19-20 are rendered invalid by Altera.

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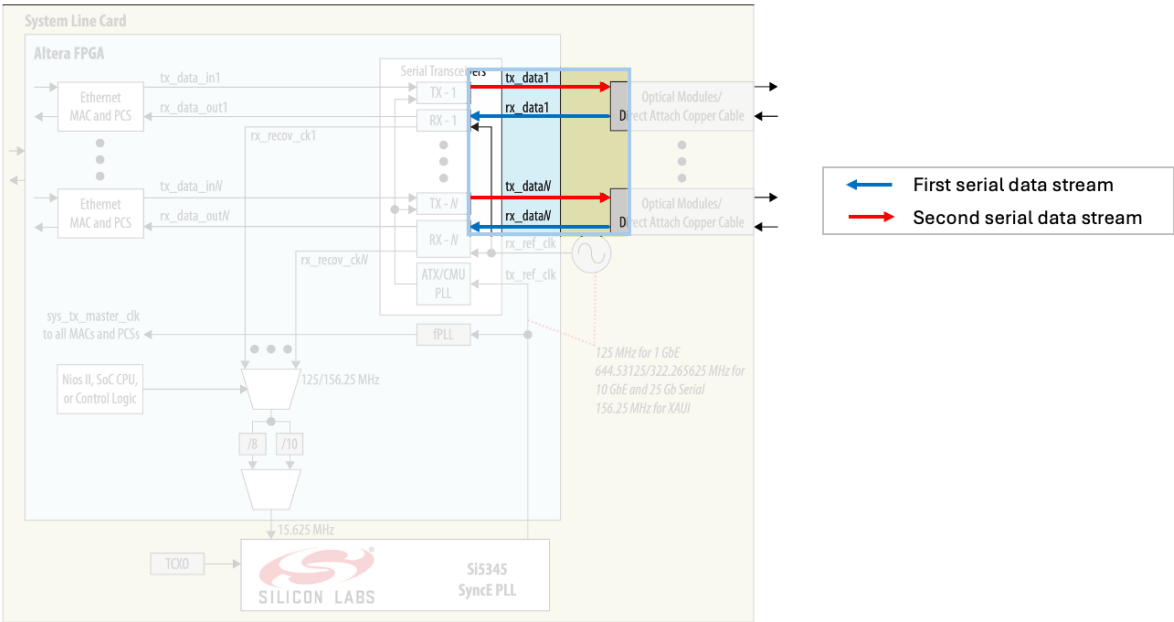
Claims	Exemplary Disclosures from the Prior Art
[1.preamble] A method for processing a first serial data stream comprising market data, using a field programmable gate array system, to generate a second serial data stream comprising order entry data, wherein the method comprises the steps of:	The preamble is not limiting. To the extent the preamble is limiting, Altera discloses a method of processing a serial data stream using a field-programmable gate array system to generate a second serial data stream, and a person of ordinary skill in the art would understand that the method could be applied to convert market data to order entry data, as taught by Lockwood. <i>See, e.g.:</i> Figure 1. High-Level Example of a SyncE System Line Card Using Altera FPGA and Silicon Labs SyncE PLL  Lockwood:

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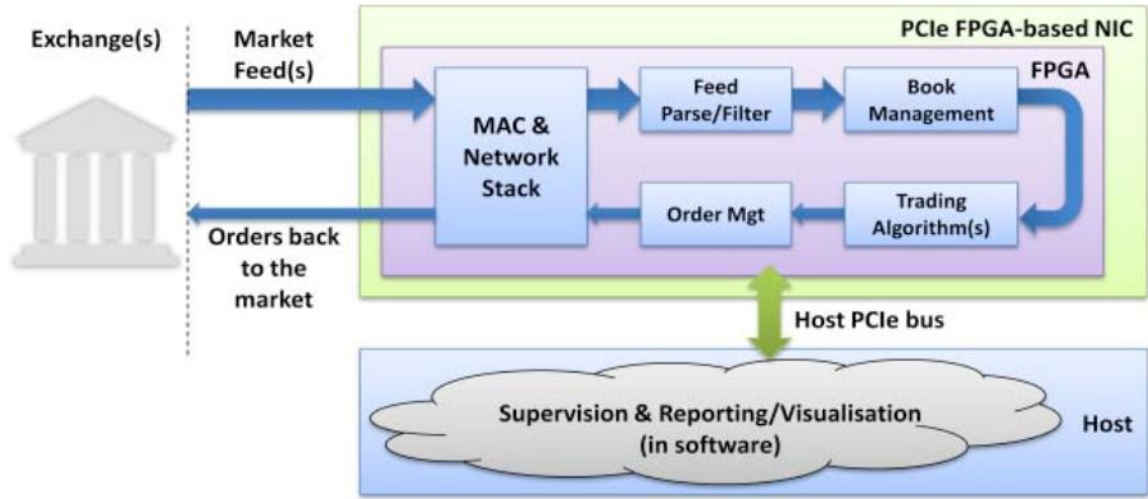
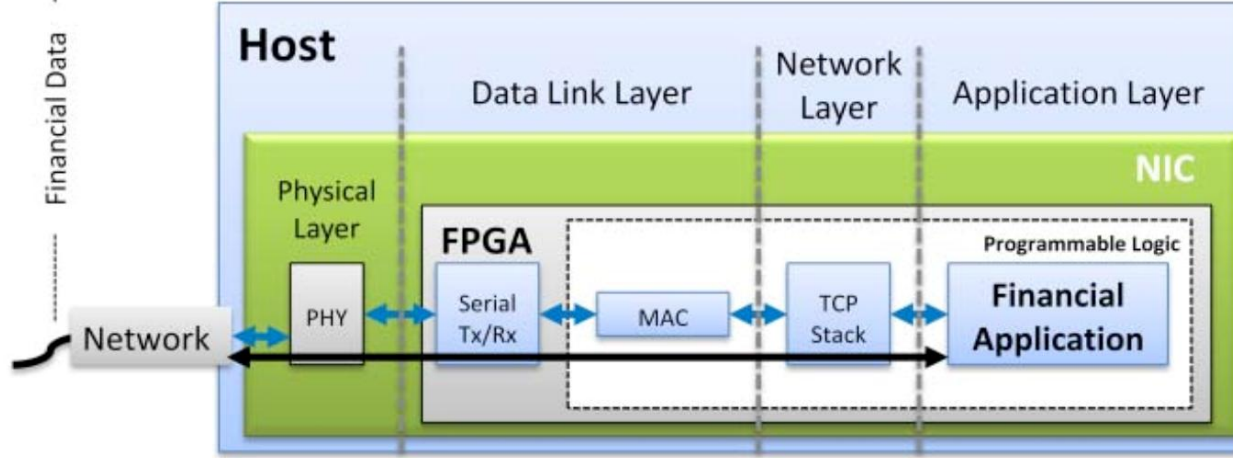
Claims	Exemplary Disclosures from the Prior Art
	 Figure 2 illustrates a typical Smart NIC in a supervised financial trading application. The system consists of an Exchange(s) connected to a Market Feed(s), which feeds into a PCIe FPGA-based NIC. Inside the NIC, data flows through a MAC & Network Stack, Feed Parse/Filter, Book Management, Order Mgt, and Trading Algorithm(s). The NIC is connected to a Host via a Host PCIe bus, which also connects to Supervision & Reporting/Visualisation (in software) on the Host.
	 Figure 3 illustrates the Host and NIC architecture. The Host contains the Data Link Layer, Network Layer, and Application Layer. The NIC contains the Physical Layer and Programmable Logic. The Programmable Logic includes a Serial Tx/Rx, MAC, TCP Stack, and Financial Application. The Network is connected to the PHY in the Physical Layer.

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Claims	Exemplary Disclosures from the Prior Art
	A person of ordinary skill in the art would have been motivated to combine Altera and Lockwood. Specifically, a POSA would have been motivated to use Altera in high-frequency trading applications as described in Lockwood to minimize latency. A POSA seeking to implement the Altera FPGA for high-frequency trading would have a reasonable expectation of success because a skilled artisan would recognize that the Altera FPGA's programmable logic could be used to process financial data in high-frequency trading.
[1.a] receiving, by a first plurality of data pins in a first interface of a field programmable gate array in the field programmable gate array system, the first serial data stream;	Altera discloses receiving a serial data stream by a first plurality of data pins in a first interface. <i>See, e.g.:</i> Altera at 2: Figure 1. High-Level Example of a SyncE System Line Card Using Altera FPGA and Silicon Labs SyncE PLL Stratix Handbook:

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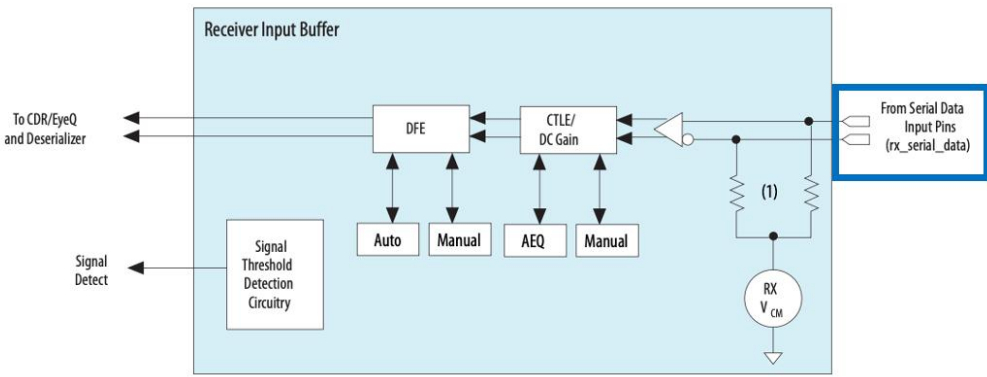
Claims	Exemplary Disclosures from the Prior Art
	Figure 1-9: Receiver Input Buffer Stratix V GT channels do not support AEQ and DFE.  Note: 1. For Stratix V GX channels, the available options are OFF, 85, 100, 120, and 150 Ω. Stratix V GT channels only support 100 Ω. To the extent HFT contends that Altera fails to teach this limitation, this limitation would have been obvious to a person of ordinary skill in the art based on this reference either alone or in combination with the knowledge of one of ordinary skill in the art.
[1.b] receiving, by a first reference clock pin in the first interface, a first clock signal having a first frequency and a first phase;	Altera discloses receiving, by a first reference clock pin in the first interface, a first clock signal having a first frequency and a first phase. <i>See, e.g.:</i> Altera at 2:

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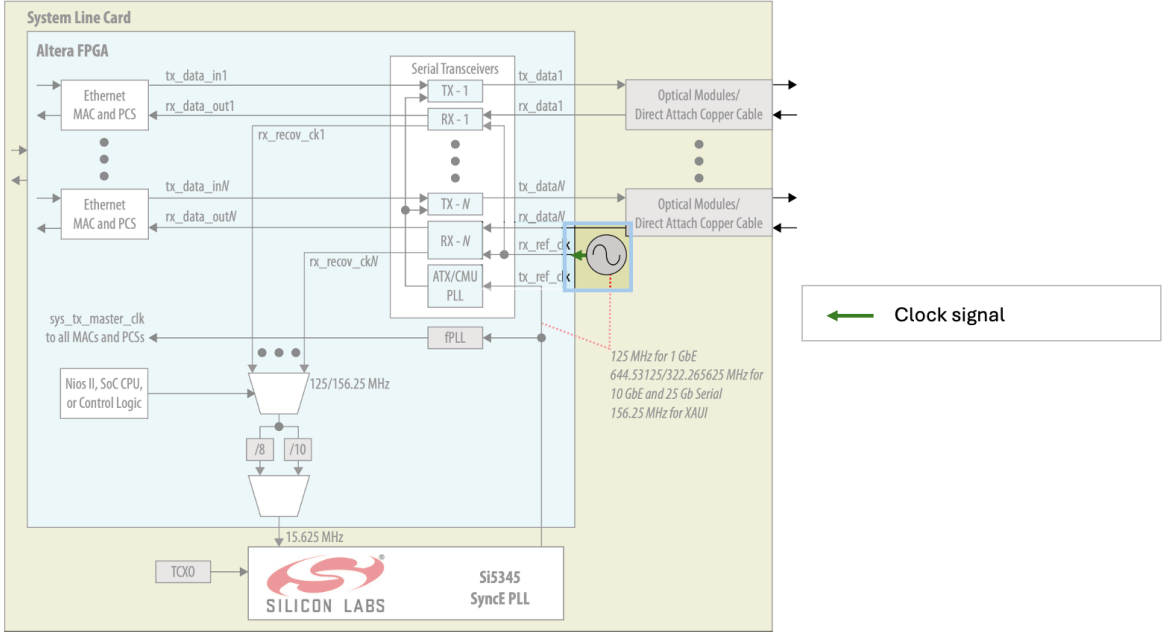
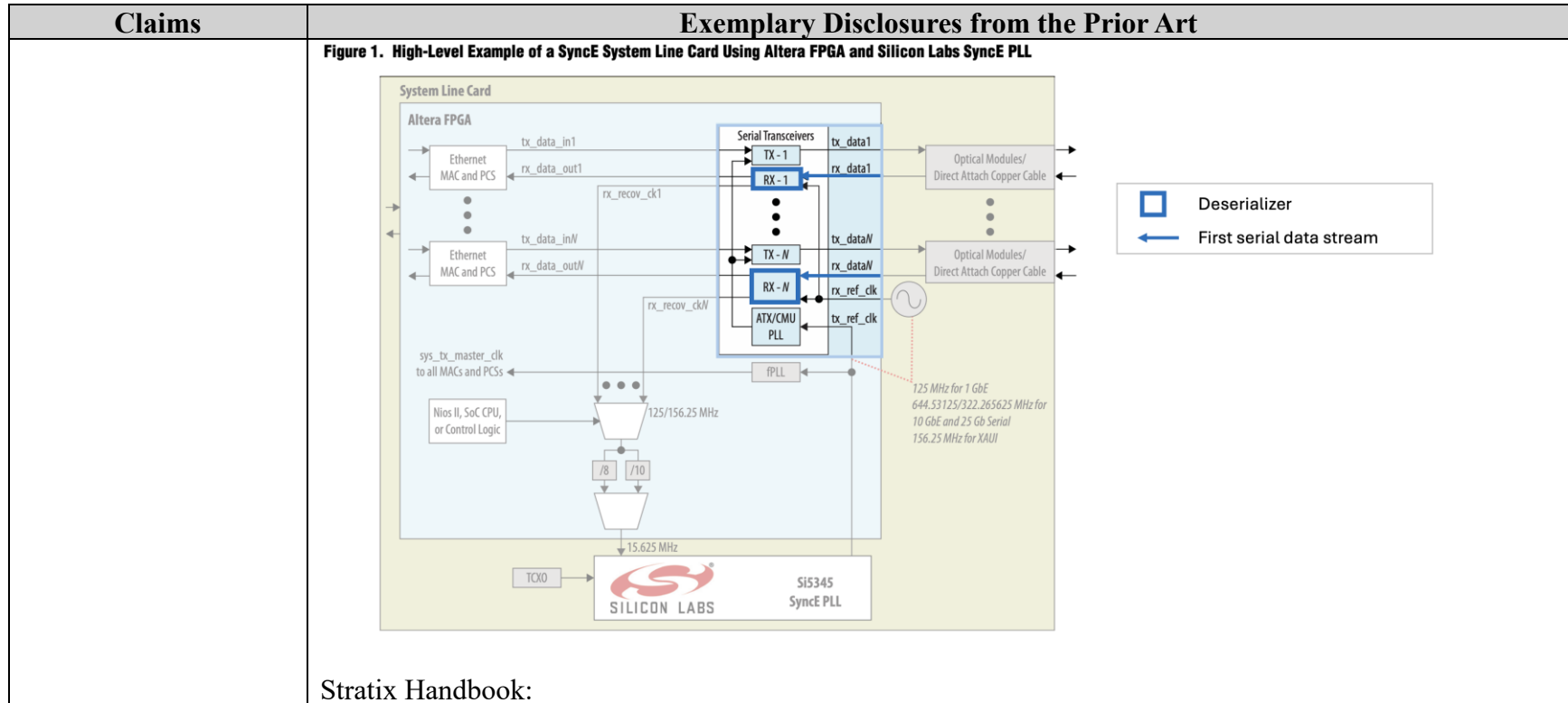
Claims	Exemplary Disclosures from the Prior Art
	Figure 1. High-Level Example of a SyncE System Line Card Using Altera FPGA and Silicon Labs SyncE PLL  To the extent HFT contends that Altera fails to teach this limitation, this limitation would have been obvious to a person of ordinary skill in the art based on this reference either alone or in combination with the knowledge of one of ordinary skill in the art.
[1.c] transmitting, from the first plurality of data pins in the first interface to a deserializer in the field programmable gate array, the first serial data stream;	Altera discloses transmitting from the first plurality of data pins in the first interface to a deserializer the first serial data stream. <i>See, e.g.:</i> Altera at 2:

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Stratix Handbook:

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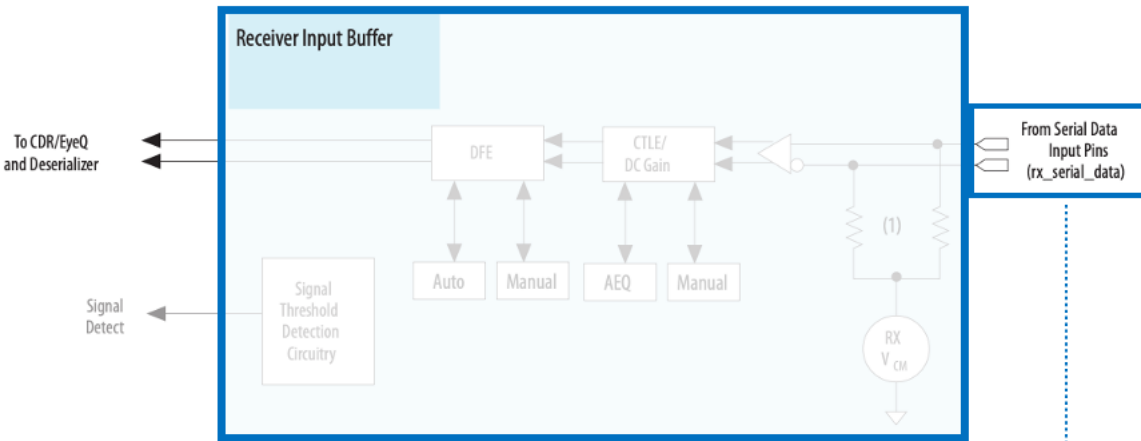
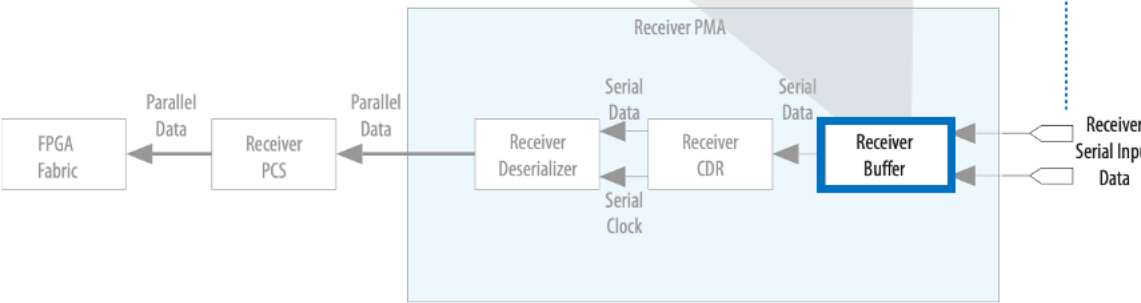
Claims	Exemplary Disclosures from the Prior Art
	Figure 1-9: Receiver Input Buffer Stratix V GT channels do not support AEQ and DFE.  Note: 1. For Stratix V GX channels, the available options are OFF, 85, 100, 120, and 150 Ω . Stratix V GT channels only support 100 Ω . Figure 1-7: Receiver PMA Block Diagram 

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Claims	Exemplary Disclosures from the Prior Art
	Figure 1-7: Receiver PMA Block Diagram FIG. 3E To the extent HFT contends that Altera fails to teach this limitation, this limitation would have been obvious to a person of ordinary skill in the art based on this reference either alone or in combination with the knowledge of one of ordinary skill in the art.
[1.d] providing, from the first reference clock pin in the first interface to the deserializer, a clock signal based at least on the first clock signal;	Altera discloses providing a clock signal from the first reference clock pin to the deserializer. <i>See, e.g.:</i> Altera at 2:

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Claims	Exemplary Disclosures from the Prior Art
	Figure 1. High-Level Example of a SyncE System Line Card Using Altera FPGA and Silicon Labs SyncE PLL The diagram illustrates a high-level example of a SyncE System Line Card. The system is composed of an Altera FPGA, Ethernet MAC and PCS blocks, Serial Transceivers (TX-N, RX-N), and a Silicon Labs Si5345 SyncE PLL. The PLL provides a 15.625 MHz clock to the FPGA and a 125/156.25 MHz clock to the transceivers. The transceivers are connected to Optical Modules/Direct Attach Copper Cables. A legend indicates that a blue square represents a Deserializer and a green arrow represents a Clock signal. Stratix Handbook:

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Claims	Exemplary Disclosures from the Prior Art
	Figure 2-3: Input Reference Clock Sources for GX Transceiver Channels For more information about the fractional PLL input clock sources shown in the following figure, refer to Figure 2-6.

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Claims	Exemplary Disclosures from the Prior Art
	Figure 2-3: Input Reference Clock Sources for GX Transceiver Channels For more information about the fractional PLL input clock sources shown in the following figure, refer to Figure 2-6. To the extent HFT contends that Altera fails to teach this limitation, this limitation would have been obvious to a person of ordinary skill in the art based on this reference either alone or in combination with the knowledge of one of ordinary skill in the art.
[1.e] generating, by the deserializer, a first receiver side clock	Altera discloses generating by the deserializer a first receiver side clock signal having a second frequency and a second phase, based at least in part on the first clock signal. <i>See, e.g.:</i>

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[illegible]

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Claims

Exemplary Disclosures from the Prior Art

Figure 2-22: Receiver 10G PCS and PMA Clocking

The diagram illustrates the clocking architecture for a receiver, showing the flow of signals from the FPGA Fabric through various clock dividers and synchronizers to the Receiver 10G PCS and Receiver PMA blocks.

Key Components and Connections:

- FPGA Fabric:** Provides input signals $rx_10g_coreclk$ and rx_10g_dflow to the clocking logic.
- Receiver 10G PCS:** Contains a 64000 Divider and 64 SM, a Frame Synchronizer, a Deserializer, a Disparity Checker, a Block Synchronizer, and a RX Core Clock and Enable.
- Receiver PMA:** Contains a Deserializer and a CDR (Clock Data Recovery) block.
- Input Reference Clock:** Provides the reference clock signal to the CDR.
- Recovered Clocks:** Output from the CDR, used for the Deserializer and other components.
- Central/Local Clock Divider:** Divides the input clock into Parallel and Serial Clocks (To the x6 clock lines).
- Clock Divider:** Divides the input clock into Parallel and Serial Clocks (From the x6 or xN Clock Lines).
- Legend:**
 - Parallel Clock (Red line)
 - Serial Clock (Blue line)
 - Parallel and Serial Clocks (Black line)

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	Figure 1-7: Receiver PMA Block Diagram FIG. 3E To the extent HFT contends that Altera fails to teach this limitation, this limitation would have been obvious to a person of ordinary skill in the art based on this reference either alone or in combination with the knowledge of one of ordinary skill in the art.
[1.f] converting, by the deserializer, the first serial data stream into a first plurality of parallel data streams;	Altera discloses converting, by the deserializer, the first serial data stream into a plurality of parallel data streams. <i>See, e.g.:</i> Altera at 2:

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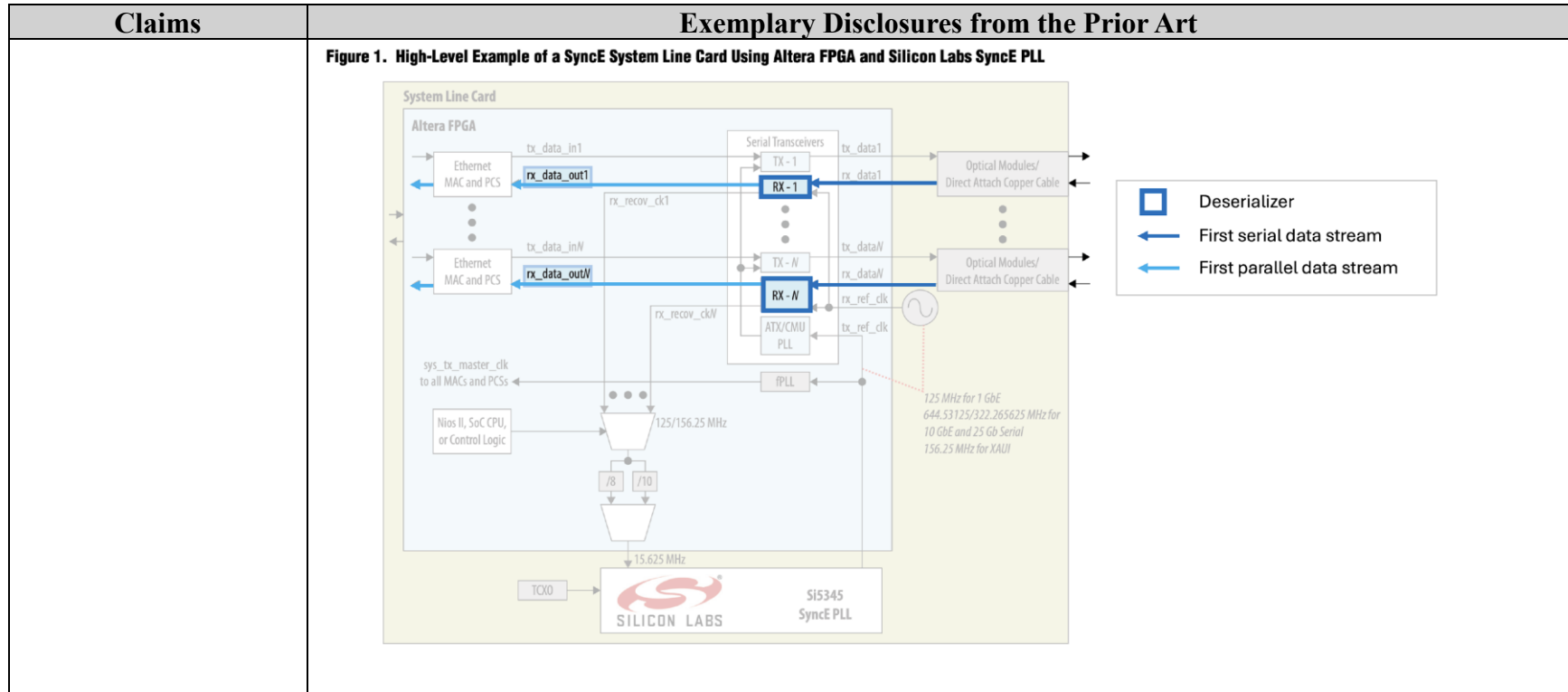


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Claims	Exemplary Disclosures from the Prior Art
	Figure 1-7: Receiver PMA Block Diagram FIG. 3E To the extent HFT contends that Altera fails to teach this limitation, this limitation would have been obvious to a person of ordinary skill in the art based on this reference either alone or in combination with the knowledge of one of ordinary skill in the art.
[1.g] transmitting, from the deserializer to the computational circuitry, the first plurality of data streams comprising a	Altera discloses transmitting from the deserializer to the computational circuitry the first plurality of data streams comprising a first plurality of data items and a first amount of data streams. <i>See, e.g.:</i> Altera at 2:

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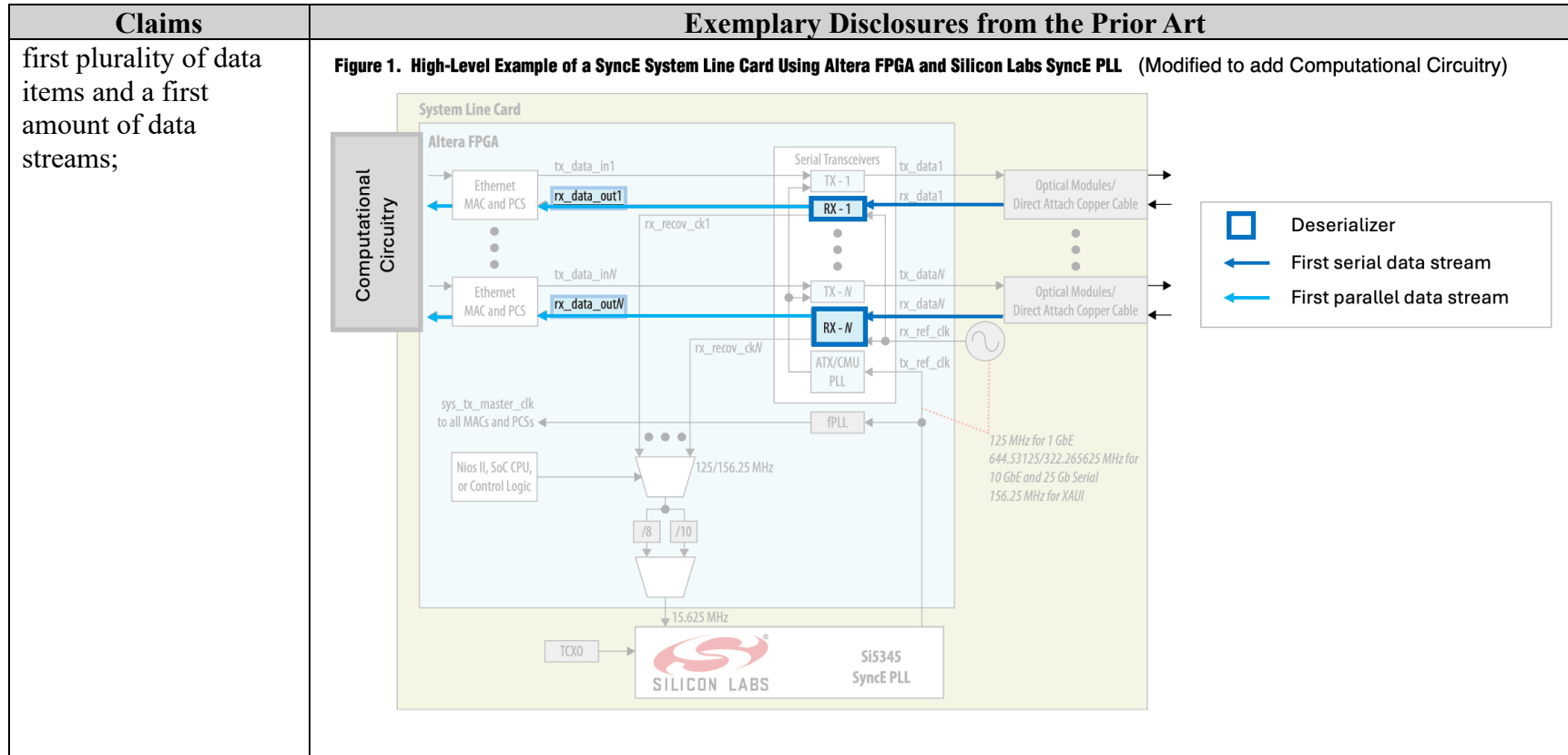


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Claims	Exemplary Disclosures from the Prior Art
	Figure 1-7: Receiver PMA Block Diagram FIG. 3E To the extent HFT contends that Altera fails to teach this limitation, this limitation would have been obvious to a person of ordinary skill in the art based on this reference either alone or in combination with the knowledge of one of ordinary skill in the art.
[1.h] transmitting, via a first clock output pin on a second interface of the field programmable gate array to a phase	Altera discloses transmitting via a first clock output pin on a second interface of the field programmable gate array to a phase detector not part of the field programmable gate array the first receiver side clock signal. <i>See, e.g.:</i> Altera at 2:

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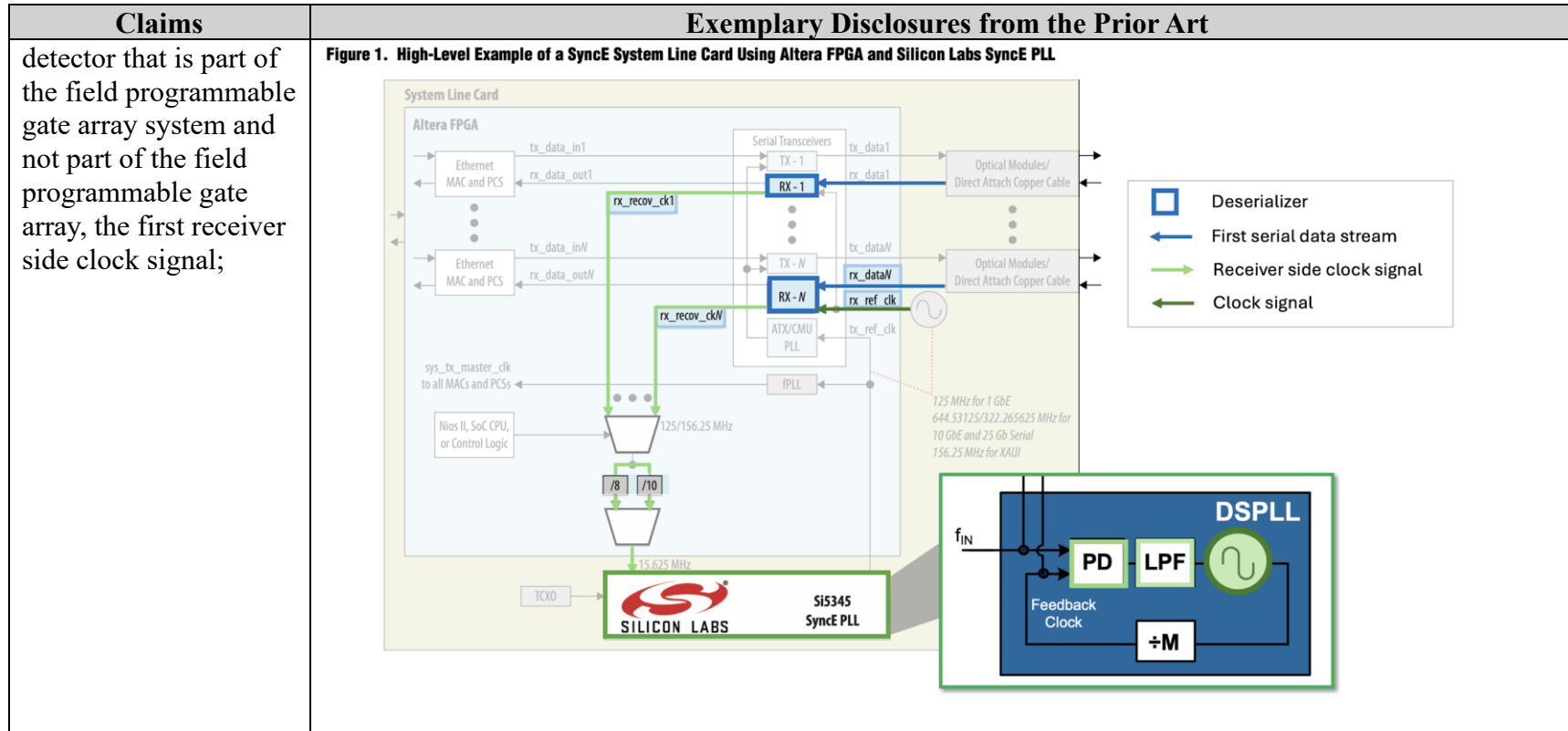


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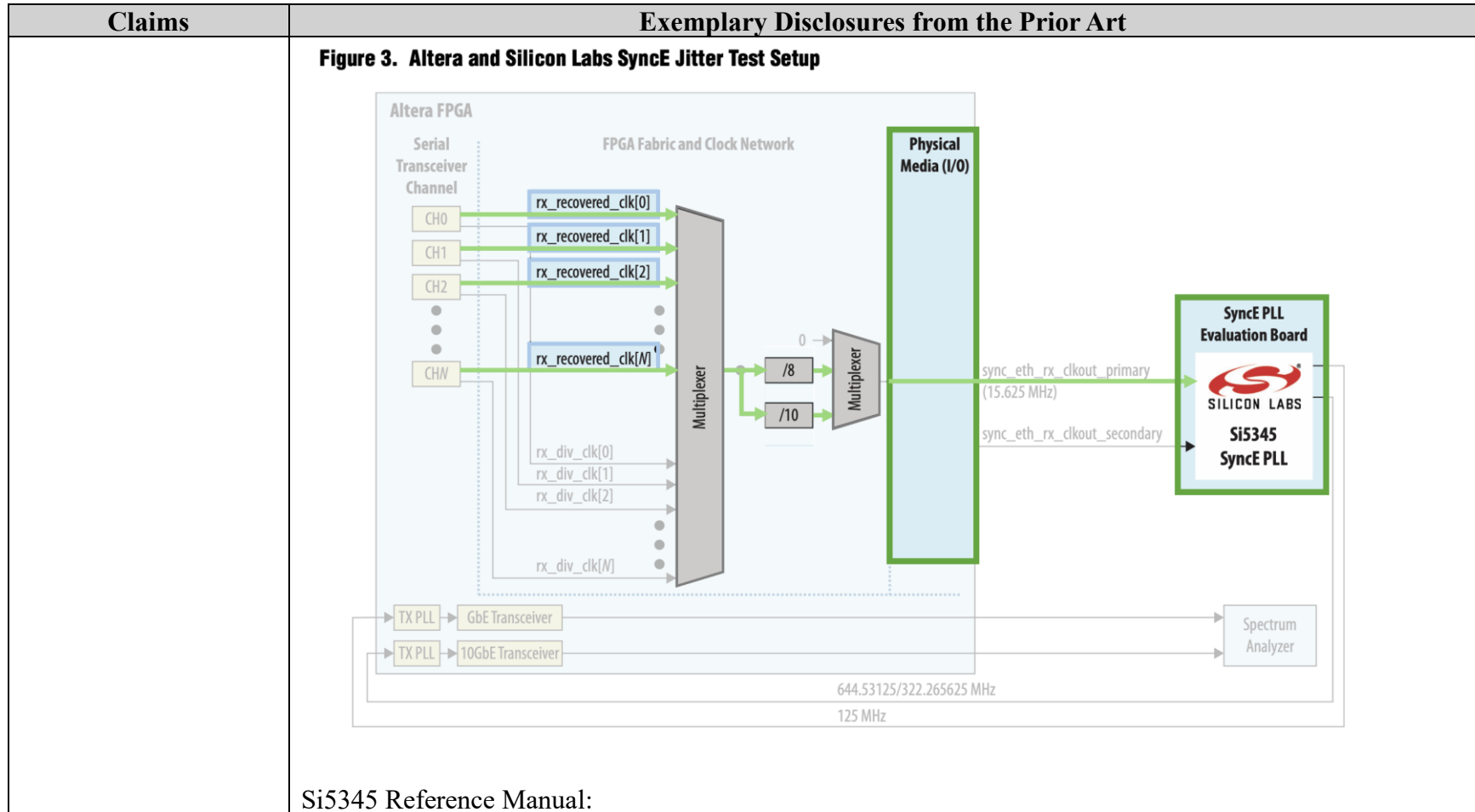


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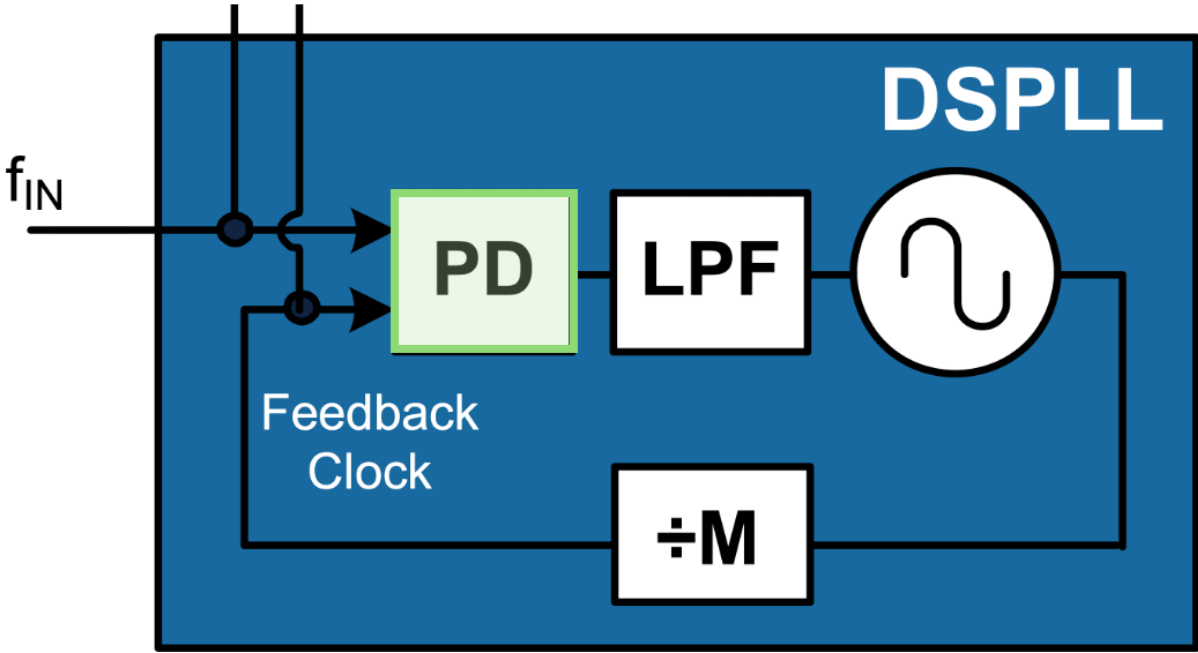
Claims	Exemplary Disclosures from the Prior Art
	 Si5345/44/42 Figure 13 Excerpt To the extent HFT contends that Altera fails to teach this limitation, this limitation would have been obvious to a person of ordinary skill in the art based on this reference either alone or in combination with the knowledge of one of ordinary skill in the art.
[1.i] generating, using the field programmable gate array system, a feedback clock signal	Altera discloses using a field programmable gate array system to generate a feedback clock signal associated with a first transmitter side clock signal, the feedback clock signal having a third frequency and a third phase, by performing the following steps until a first output of the phase detector is below a first threshold level. <i>See, e.g.:</i>

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Claims	Exemplary Disclosures from the Prior Art
associated with a first transmitter side clock signal, the feedback clock signal having a third frequency and a third phase, by performing the following steps until a first output of the phase detector is below a first threshold level:	Altera at 2: Figure 1. High-Level Example of a SyncE System Line Card Using Altera FPGA and Silicon Labs SyncE PLL Si5345 Reference Manual:

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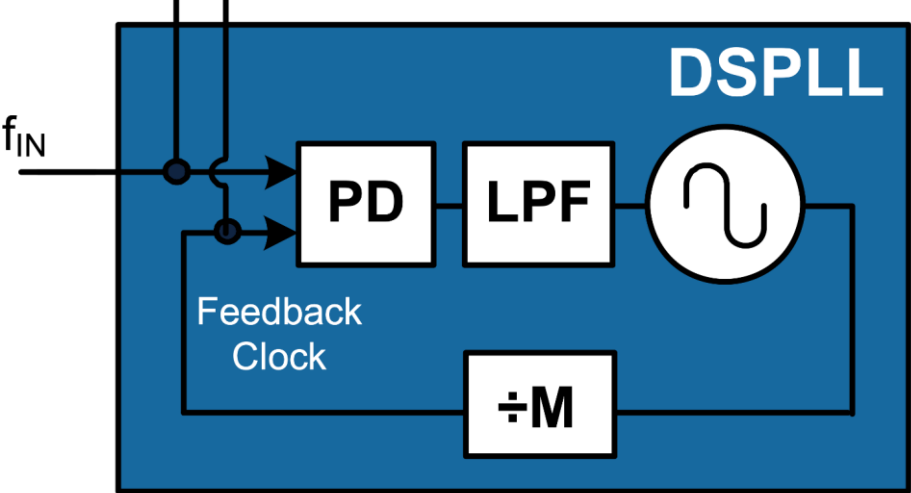
Claims	Exemplary Disclosures from the Prior Art
	 To the extent HFT contends that Altera fails to teach this limitation, this limitation would have been obvious to a person of ordinary skill in the art based on this reference either alone or in combination with the knowledge of one of ordinary skill in the art.
[1.i.i] generating, by an adjustable oscillator in the field programmable gate array system, a second clock signal having a fourth frequency and a fourth phase;	Altera discloses generating, by an adjustable oscillator, a second clock signal having a fourth frequency and a fourth phase. <i>See, e.g.:</i> Si5345 Reference Manual:

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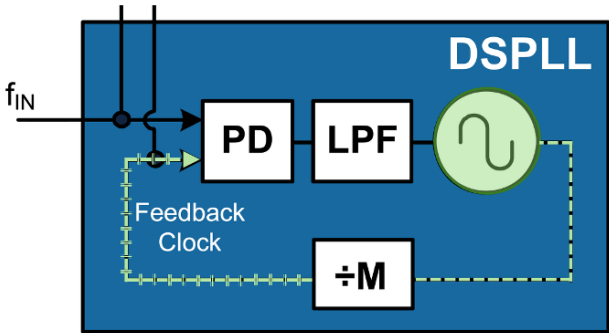
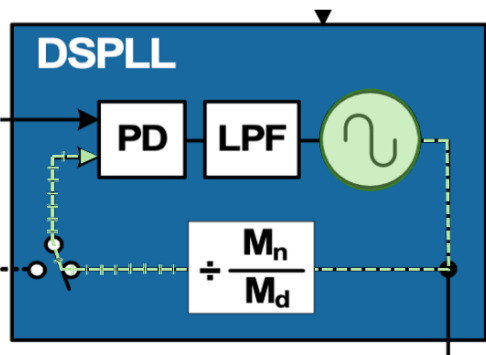
Claims	Exemplary Disclosures from the Prior Art
	 Si5345/44/42 Figure 13 Excerpt  Si5345/44/42 Figure 2 Excerpt To the extent HFT contends that Altera fails to teach this limitation, this limitation would have been obvious to a person of ordinary skill in the art based on this reference either alone or in combination with the knowledge of one of ordinary skill in the art.
[1.i.ii] generating, by the phase detector, the first output based on a comparison of the first receiver side clock signal and the feedback clock signal obtained from the second clock signal;	Altera discloses generating by the phase detector the first output based on a comparison of the first receiver side clock signal and the feedback clock signal obtained from the second clock signal. <i>See, e.g.:</i> Si5345 Reference Manual:

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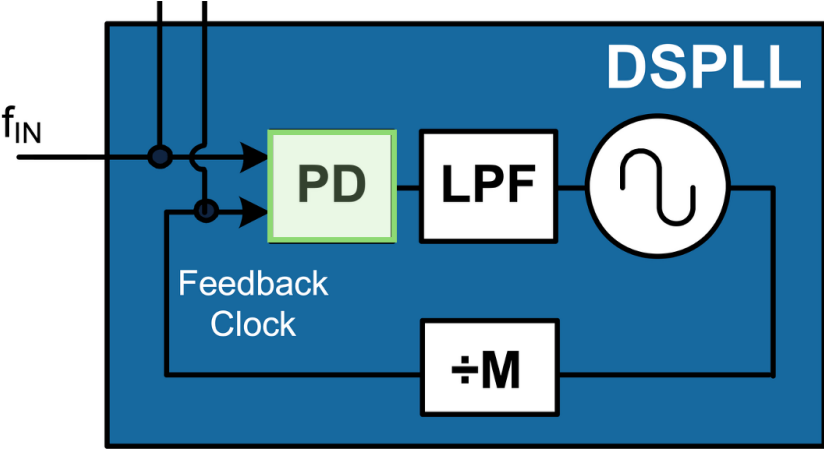
Claims	Exemplary Disclosures from the Prior Art
	 To the extent HFT contends that Altera fails to teach this limitation, this limitation would have been obvious to a person of ordinary skill in the art based on this reference either alone or in combination with the knowledge of one of ordinary skill in the art.
[1.i.iii] transmitting, from the phase detector to a phase controller of the field programmable gate array system which is not in the field programmable gate array, the first output;	Altera discloses transmitting from the phase detector to a phase controller of the field programmable gate array system which is not in the field programmable gate array, the first output. <i>See, e.g.:</i> Si5345 Reference Manual:

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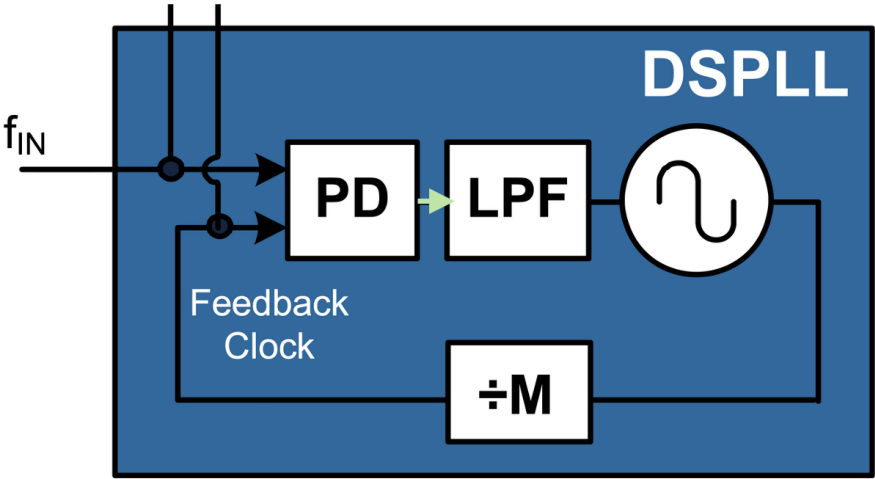
Claims	Exemplary Disclosures from the Prior Art
	 To the extent HFT contends that Altera fails to teach this limitation, this limitation would have been obvious to a person of ordinary skill in the art based on this reference either alone or in combination with the knowledge of one of ordinary skill in the art.
[1.i.iv] determining, by the phase controller, interim adjustment information based on the first output; and	Altera discloses determining interim adjustment information based on the first output with a phase controller. <i>See, e.g.:</i> Si5345 Reference Manual:

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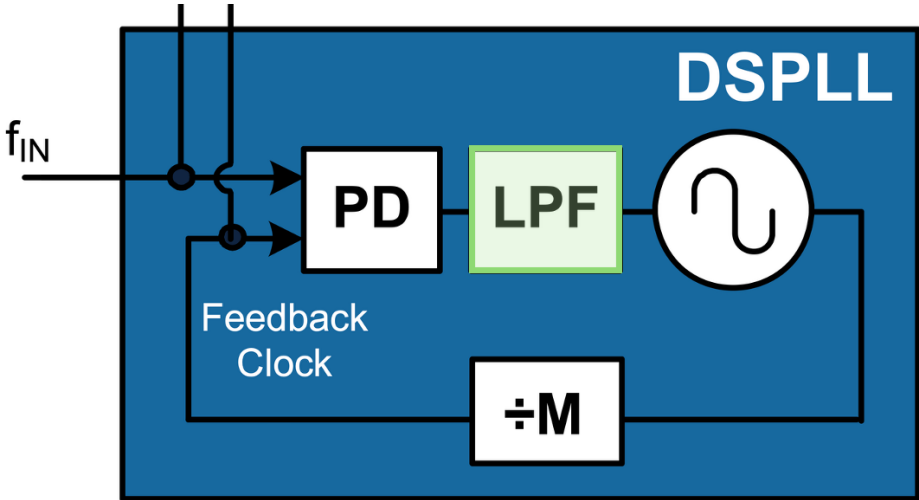
Claims	Exemplary Disclosures from the Prior Art
	 To the extent HFT contends that Altera fails to teach this limitation, this limitation would have been obvious to a person of ordinary skill in the art based on this reference either alone or in combination with the knowledge of one of ordinary skill in the art.
[1.i.v] transmitting, from the phase controller to the adjustable oscillator, the interim adjustment information;	Altera discloses transmitting from the phase controller to the oscillator the interim adjustment information. <i>See, e.g.:</i> Si5345 Reference Manual:

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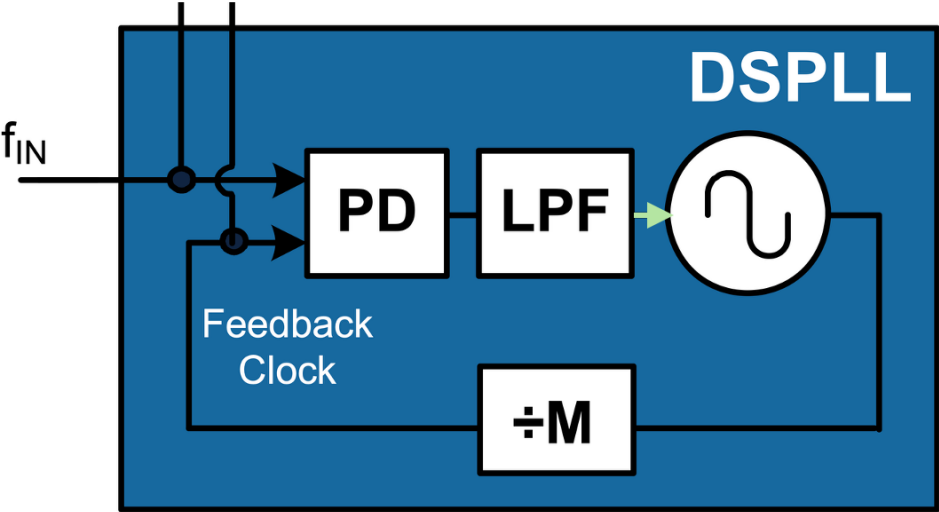
Claims	Exemplary Disclosures from the Prior Art
	 To the extent HFT contends that Altera fails to teach this limitation, this limitation would have been obvious to a person of ordinary skill in the art based on this reference either alone or in combination with the knowledge of one of ordinary skill in the art.
[1.i.vi] wherein, the adjustable oscillator adjusts the second clock signal based on the interim adjustment information and steps (i) through (v) are repeated until the first output of the phase detector is below the first threshold level;	Altera discloses the adjustable oscillator adjusts the second clock signal based on the interim adjustment information and steps (i) through (v) are repeated until the first output of the phase detector is below the first threshold level. <i>See, e.g.:</i> Si5345 Reference Manual at 10:

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Claims	Exemplary Disclosures from the Prior Art
	Si5345/44/42 Figure 1. Block Diagram Si5345/44/42 <i>Id.</i> at 9:

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Claims	Exemplary Disclosures from the Prior Art
	2. Overview The Si5345/44/42 jitter attenuating clock multipliers combine 4th generation DSPLL and MultiSynth™ technologies to enable any-frequency clock generation for applications that require the highest level of jitter performance. These devices are programmable via a serial interface with in-circuit programmable non-volatile memory (NVM) ensuring power up with a known frequency configuration. Free-run, synchronous, and holdover modes of operation are supported offering both automatic and manual input clock switching. The loop filter is fully integrated on-chip eliminating the risk of potential noise coupling associated with discrete solutions. Further, the jitter attenuation bandwidth is digitally programmable providing jitter performance optimization at the application level. These devices are capable of generating any combination of output frequency from any input frequency within the specified input and output range. <i>Id.</i> at 19: 5.1. Inputs (IN0, IN1, IN2, IN3) The inputs accept both standard format inputs and low-duty-cycle pulsed CMOS clocks. Input selection from CLK_SWITCH_MODE can be manual (pin or register controlled) or automatic with user definable priorities. Register 0x052A is used to select pin or register control, and to configure the input as shown below in Table 7. <i>Id.</i> at 17: 4.5. Acquisition Mode The device monitors all inputs for a valid clock. If at least one valid clock is available for synchronization, the DSPLL will automatically start the lock acquisition process. If the fast lock feature is enabled, the DSPLL will acquire lock using the Fastlock Loop Bandwidth setting and then transition to the DSPLL Loop Bandwidth setting when lock acquisition is complete. During lock acquisition the outputs will generate a clock that follows the VCO frequency change as it pulls-in to the input clock frequency. 4.6. Locked Mode Once locked, the DSPLL will generate output clocks that are both frequency and phase locked to its selected input clock. At this point any XTAL frequency drift will typically not affect the output frequency. A loss of lock pin (LOL) and status bit indicate when lock is achieved. See “5.3.3. Loss of Lock Fault Monitoring” for more details on the operation of the loss of lock circuit.

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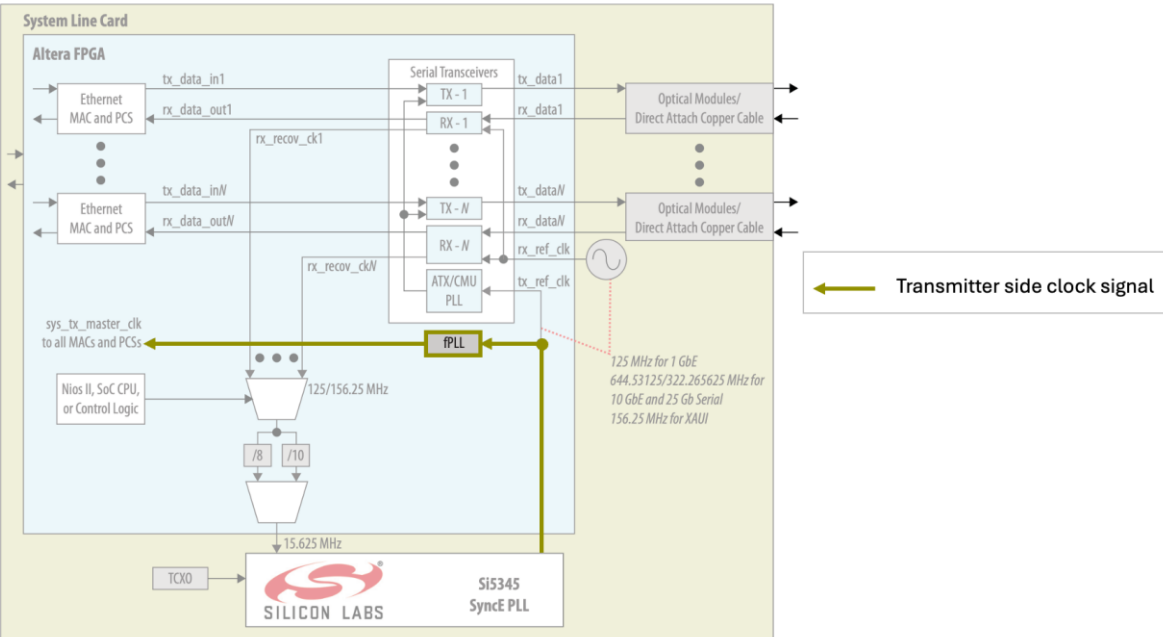
Claims	Exemplary Disclosures from the Prior Art
	To the extent HFT contends that Altera fails to teach this limitation, this limitation would have been obvious to a person of ordinary skill in the art based on this reference either alone or in combination with the knowledge of one of ordinary skill in the art.
[1.j] generating, by the serializer, a first transmitter side clock signal based on the second clock signal; and	Altera discloses generating, by the serializer, a first transmitter side clock signal based on the second clock signal. <i>See, e.g.:</i> Altera at 2: Figure 1. High-Level Example of a SyncE System Line Card Using Altera FPGA and Silicon Labs SyncE PLL  Stratix Handbook:

**Exhibit B-1 to Citadel Securities' Invalidity Contentions:
Invalidity of U.S. Patent No. 10,931,286 based on Altera**

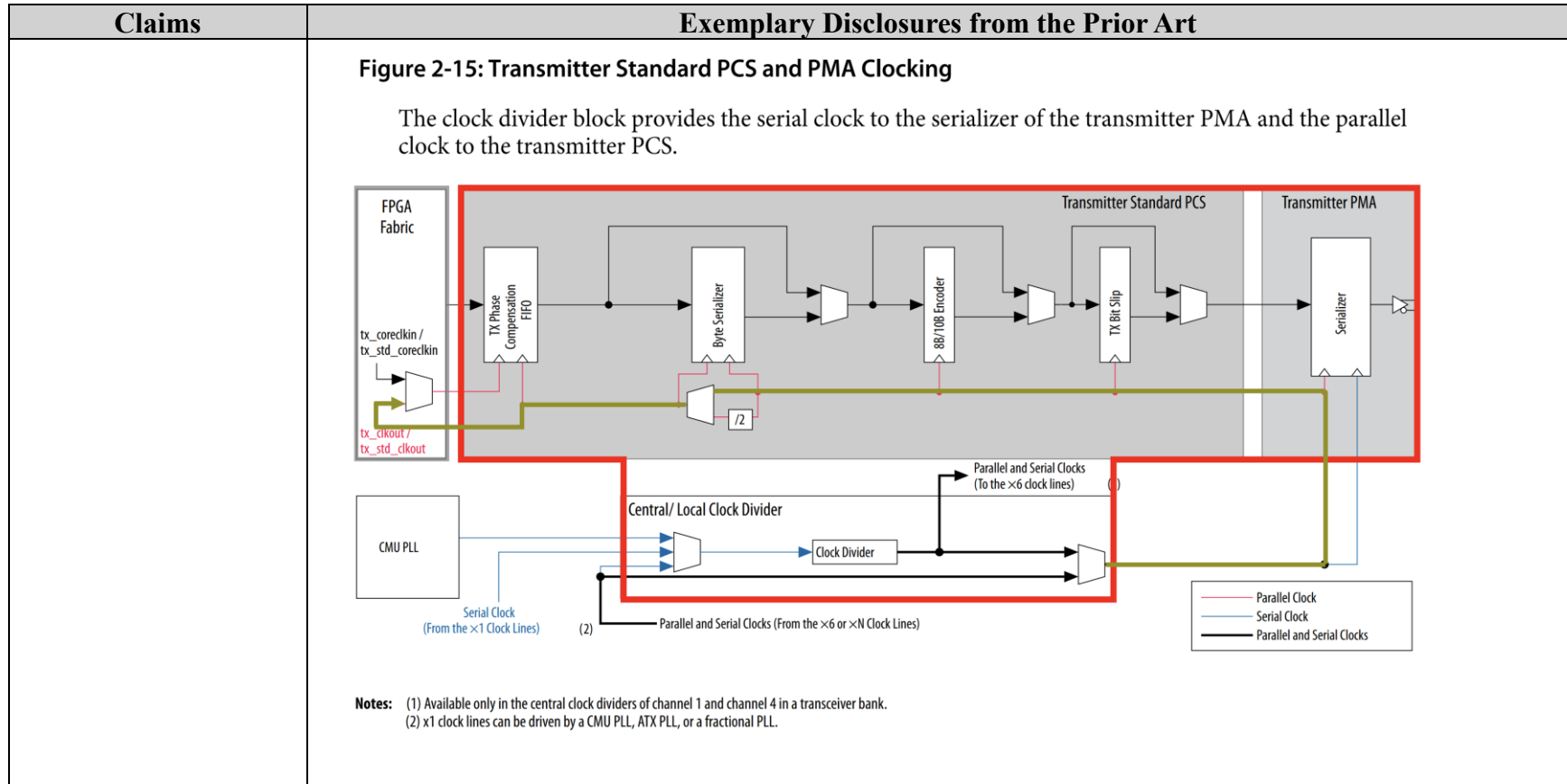


Exhibit B-1 to Citadel Securities' Invalidity Contentions:
Invalidity of U.S. Patent No. 10,931,286 based on Altera

Claims	Exemplary Disclosures from the Prior Art
	FIG. 4A To the extent HFT contends that Altera fails to teach this limitation, this limitation would have been obvious to a person of ordinary skill in the art based on this reference either alone or in combination with the knowledge of one of ordinary skill in the art.
[1.k] transmitting, by the serializer to the	Altera discloses transmitting, by the serializer to the computational circuitry, the first transmitter side clock signal. <i>See, e.g.:</i>

**Exhibit B-1 to Citadel Securities' Invalidity Contentions:
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Claims	Exemplary Disclosures from the Prior Art
computational circuitry, the first transmitter side clock signal;	Altera at 2: Figure 1. High-Level Example of a SyncE System Line Card Using Altera FPGA and Silicon Labs SyncE PLL The diagram illustrates a System Line Card architecture. It features an Altera FPGA and a Silicon Labs Si5345 SyncE PLL. The Altera FPGA contains multiple Ethernet MAC and PCS blocks, Serial Transceivers (TX-N, RX-N), and an ATX/CMU PLL. The Silicon Labs PLL is connected to a TCXO and provides a 15.625 MHz clock signal to the ATX/CMU PLL. The ATX/CMU PLL outputs a 125/156.25 MHz clock signal to the Ethernet MAC and PCS blocks and a 125 MHz clock signal to the Serial Transceivers. The Serial Transceivers output data to Optical Modules/Direct Attach Copper Cables. A Transmitter side clock signal is shown as a yellow arrow pointing left. Stratix Handbook:

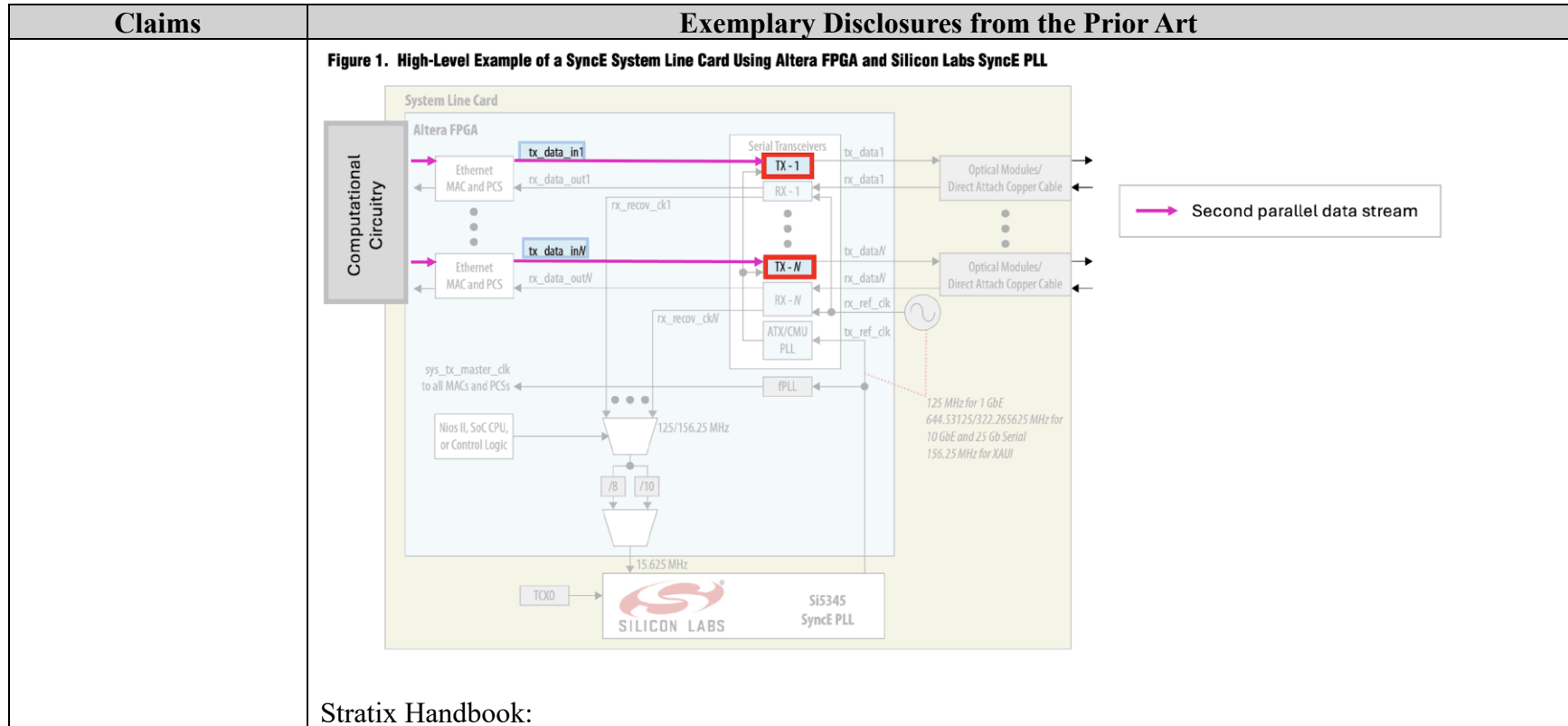
**Exhibit B-1 to Citadel Securities' Invalidity Contentions:
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Claims	Exemplary Disclosures from the Prior Art
	Figure 2-15: Transmitter Standard PCS and PMA Clocking The clock divider block provides the serial clock to the serializer of the transmitter PMA and the parallel clock to the transmitter PCS. Notes: (1) Available only in the central clock dividers of channel 1 and channel 4 in a transceiver bank. (2) x1 clock lines can be driven by a CMU PLL, ATX PLL, or a fractional PLL. To the extent HFT contends that Altera fails to teach this limitation, this limitation would have been obvious to a person of ordinary skill in the art based on this reference either alone or in combination with the knowledge of one of ordinary skill in the art.
[1.1] performing, by the computational circuitry, a first set of operations on at least a portion of the first plurality of data items to generate a second	Altera discloses performing, by the computational circuitry, a first set of operations on at least a portion of the first plurality of data items to generate a second plurality of parallel data streams comprising a second amount of data streams. <i>See, e.g.:</i> Altera at 2:

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Claims	Exemplary Disclosures from the Prior Art
plurality of parallel data streams comprising a second amount of data streams;	Figure 1. High-Level Example of a SyncE System Line Card Using Altera FPGA and Silicon Labs SyncE PLL To the extent HFT contends that Altera fails to teach this limitation, this limitation would have been obvious to a person of ordinary skill in the art based on this reference either alone or in combination with the knowledge of one of ordinary skill in the art.
[1.m] transmitting, from the computational circuitry to the serializer, the second plurality of parallel data streams;	Altera discloses transmitting from the computational circuitry to a serializer the second plurality of parallel data streams. <i>See, e.g.:</i> Altera at 2:

**Exhibit B-1 to Citadel Securities' Invalidity Contentions:
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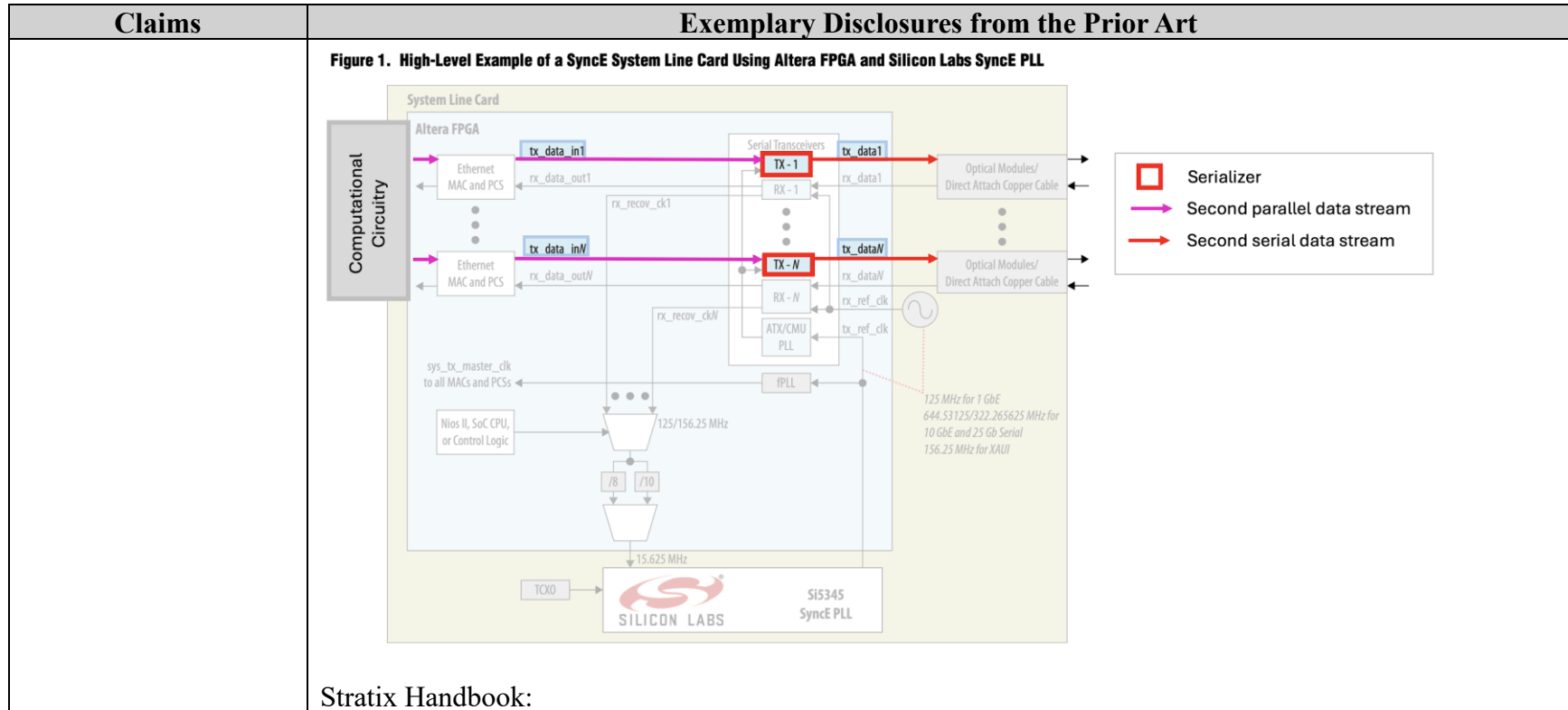


Stratix Handbook:

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Claims	Exemplary Disclosures from the Prior Art
	Figure 1-8: Transmitter PMA Block Diagram <pre> graph LR FPGA[FPGA Fabric] -- Parallel Data --> PCS[Transmitter PCS] PCS -- Parallel Data --> Serializer[Transmitter Serializer] Serializer -- Serial Data --> Buffer[Transmitter Buffer] Buffer --> Output[Transmitter Serial Output Data] RefClk[Reference Clock] --> PLL[Transmitter PLL] PLL -- Serial Clock --> Serializer subgraph PMA [Transmitter PMA] PCS Serializer Buffer end </pre> To the extent HFT contends that Altera fails to teach this limitation, this limitation would have been obvious to a person of ordinary skill in the art based on this reference either alone or in combination with the knowledge of one of ordinary skill in the art.
[1.n] converting, by the serializer, the second plurality of parallel data streams into the second serial data stream; and	Altera discloses converting by the serializer the second plurality of parallel data streams into the second serial data stream. <i>See, e.g.:</i> Altera at 2:

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Stratix Handbook:

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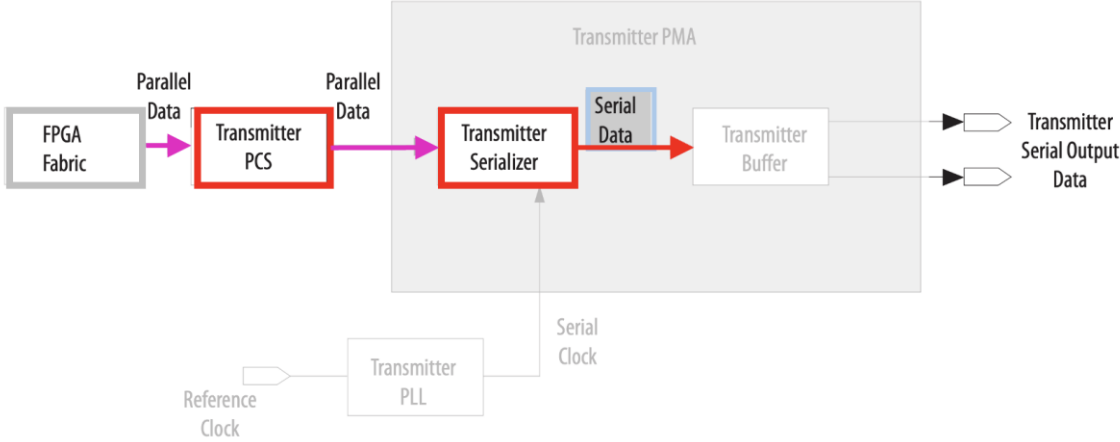
Claims	Exemplary Disclosures from the Prior Art
	Figure 1-8: Transmitter PMA Block Diagram  To the extent HFT contends that Altera fails to teach this limitation, this limitation would have been obvious to a person of ordinary skill in the art based on this reference either alone or in combination with the knowledge of one of ordinary skill in the art.
[1.o] transmitting, from the serializer off the field programmable gate array system via a second plurality of data pins in the first interface, the second serial data stream.	Altera discloses transmitting from the serializer off the field programmable gate array system via a second plurality of data pins in the first interface the second serial data stream. <i>See, e.g.:</i> Altera at 2:

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Claims	Exemplary Disclosures from the Prior Art
	Figure 1. High-Level Example of a SyncE System Line Card Using Altera FPGA and Silicon Labs SyncE PLL Stratix Handbook:

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Invalidity of U.S. Patent No. 10,931,286 based on Altera**

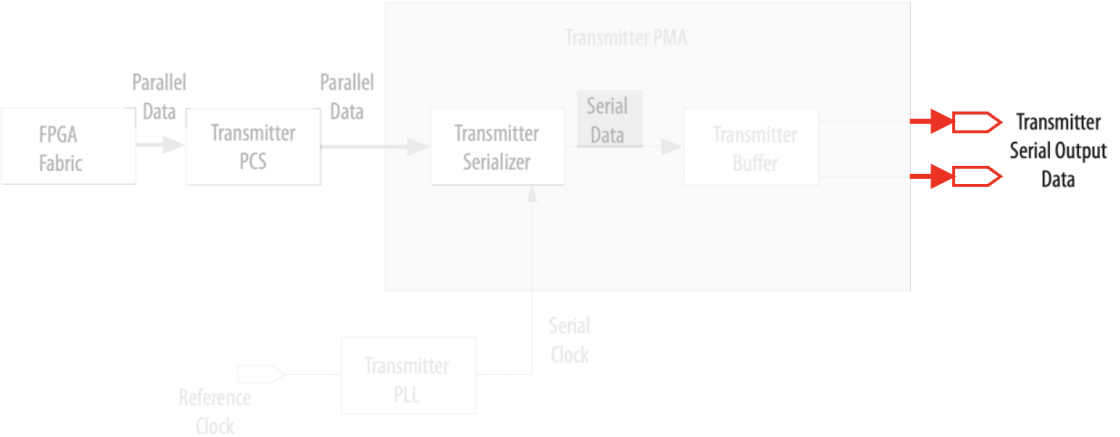
Claims	Exemplary Disclosures from the Prior Art
	Figure 1-8: Transmitter PMA Block Diagram  To the extent HFT contends that Altera fails to teach this limitation, this limitation would have been obvious to a person of ordinary skill in the art based on this reference either alone or in combination with the knowledge of one of ordinary skill in the art.
[2] The method of claim 1, wherein the second frequency corresponds to the first frequency.	A person of ordinary skill in the art would understand that when using Altera, the second frequency can correspond to the first frequency. <i>See, e.g.:</i> Altera at 2:

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Claims	Exemplary Disclosures from the Prior Art
	Figure 1. High-Level Example of a SyncE System Line Card Using Altera FPGA and Silicon Labs SyncE PLL To the extent HFT contends that Altera fails to teach this limitation, this limitation would have been obvious to a person of ordinary skill in the art based on this reference either alone or in combination with the knowledge of one of ordinary skill in the art.
[8] The method of claim 1, wherein a difference between the third phase and the second phase is less than a second threshold level.	Altera discloses a difference between the third phase and the second phase is less than a second threshold level. <i>See, e.g.:</i> Si5345 Reference Manual at 10:

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Claims	Exemplary Disclosures from the Prior Art
	Si5345/44/42 Figure 1. Block Diagram Si5345/44/42 <i>Id.</i> at 9:

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Claims	Exemplary Disclosures from the Prior Art
	2. Overview The Si5345/44/42 jitter attenuating clock multipliers combine 4th generation DSPLL and MultiSynth™ technologies to enable any-frequency clock generation for applications that require the highest level of jitter performance. These devices are programmable via a serial interface with in-circuit programmable non-volatile memory (NVM) ensuring power up with a known frequency configuration. Free-run, synchronous, and holdover modes of operation are supported offering both automatic and manual input clock switching. The loop filter is fully integrated on-chip eliminating the risk of potential noise coupling associated with discrete solutions. Further, the jitter attenuation bandwidth is digitally programmable providing jitter performance optimization at the application level. These devices are capable of generating any combination of output frequency from any input frequency within the specified input and output range. <i>Id.</i> at 19: 5.1. Inputs (IN0, IN1, IN2, IN3) The inputs accept both standard format inputs and low-duty-cycle pulsed CMOS clocks. Input selection from CLK_SWITCH_MODE can be manual (pin or register controlled) or automatic with user definable priorities. Register 0x052A is used to select pin or register control, and to configure the input as shown below in Table 7. <i>Id.</i> at 17: 4.5. Acquisition Mode The device monitors all inputs for a valid clock. If at least one valid clock is available for synchronization, the DSPLL will automatically start the lock acquisition process. If the fast lock feature is enabled, the DSPLL will acquire lock using the Fastlock Loop Bandwidth setting and then transition to the DSPLL Loop Bandwidth setting when lock acquisition is complete. During lock acquisition the outputs will generate a clock that follows the VCO frequency change as it pulls-in to the input clock frequency. 4.6. Locked Mode Once locked, the DSPLL will generate output clocks that are both frequency and phase locked to its selected input clock. At this point any XTAL frequency drift will typically not affect the output frequency. A loss of lock pin (LOL) and status bit indicate when lock is achieved. See “5.3.3. Loss of Lock Fault Monitoring” for more details on the operation of the loss of lock circuit. <i>Id.</i> at 27:

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Claims	Exemplary Disclosures from the Prior Art
	5.3.3. Loss of Lock Fault Monitoring The Loss of Lock (LOL) monitor asserts a LOL register bit when the DSPLL has lost synchronization with its selected input clock. There is also a dedicated loss of lock pin that reflects the loss of lock condition. The LOL monitor functions by measuring the frequency difference between the input and feedback clocks at the phase detector. There are two LOL frequency monitors, one that sets the LOL indicator (LOL Set) and another that clears the indicator (LOL Clear). An optional timer is available to delay clearing of the LOL indicator to allow additional time for the DSPLL to completely lock to the input clock. A block diagram of the LOL monitor is shown in Figure 13. The live LOL register always displays the current LOL state and a sticky register always stays asserted until cleared. The LOL pin reflects the current state of the LOL monitor. Si5345/44/42 Figure 13. LOL Status Indicators <i>Id.</i> at 14:

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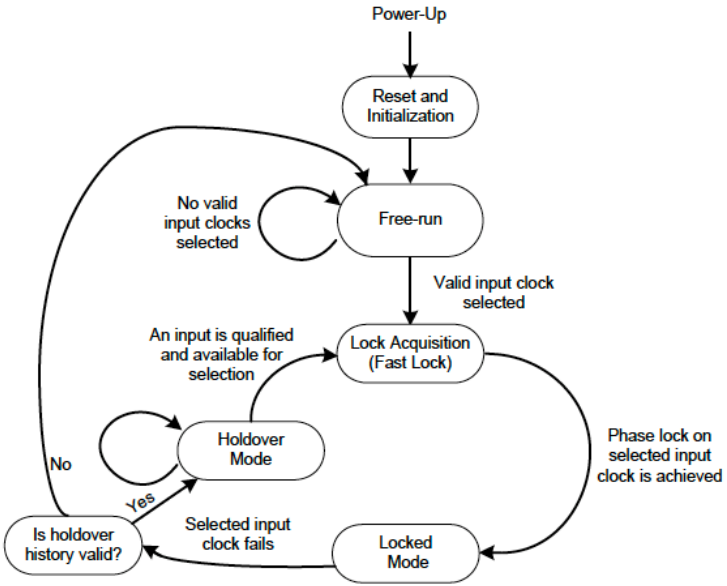
Claims	Exemplary Disclosures from the Prior Art
	After initialization the DSPLL will operate in one of the following modes: Free-run, lock-acquisition, locked, or holdover.  <pre> graph TD PowerUp[Power-Up] --> Reset[Reset and Initialization] Reset --> FreeRun[Free-run] FreeRun -- "No valid input clocks selected" --> FreeRun FreeRun -- "Valid input clock selected" --> LockAcq[Lock Acquisition (Fast Lock)] LockAcq -- "Phase lock on selected input clock is achieved" --> Locked[Locked Mode] Locked -- "Selected input clock fails" --> Holdover[Holdover Mode] Holdover -- "An input is qualified and available for selection" --> LockAcq Holdover -- "No" --> HoldoverHistory{Is holdover history valid?} HoldoverHistory -- "Yes" --> Holdover HoldoverHistory -- "No" --> FreeRun </pre> Figure 3. Modes of Operation To the extent HFT contends that Altera fails to teach this limitation, this limitation would have been obvious to a person of ordinary skill in the art based on this reference either alone or in combination with the knowledge of one of ordinary skill in the art.
[10] The method of claim 1, wherein the first set of operations does not include clock domain crossing operations that delay processing of the first	Altera discloses the first set of operations does not include clock domain crossing operations that delay processing of the first set of parallel data streams. For example, as discussed in previous limitations, Altera uses PLL(s). <i>See, e.g.:</i> Altera at 2:

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Claims set of parallel data streams.	Exemplary Disclosures from the Prior Art Figure 1. High-Level Example of a SyncE System Line Card Using Altera FPGA and Silicon Labs SyncE PLL The diagram illustrates a System Line Card architecture. It features an Altera FPGA (light blue box) and a Silicon Labs Si5345 SyncE PLL (white box with red logo). The Altera FPGA contains multiple Ethernet MAC and PCS blocks, Serial Transceivers (TX and RX), and an fPLL. The Si5345 PLL provides a 15.625 MHz clock to the FPGA. The system is connected to Optical Modules/Direct Attach Copper Cable. A note specifies clock frequencies: 125 MHz for 1 GbE, 644.53125/322.265625 MHz for 10 GbE and 25 Gb Serial, and 156.25 MHz for XAUI.
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Claims	Exemplary Disclosures from the Prior Art
	Altera’s SyncE Reference Design Figure 1 illustrates an Altera Stratix V FPGA SyncE reference design that consists of multiple 1G/10Gb Ethernet media access control (MAC) and physical coding sublayer (PCS) and physical medium attachment (PMA) (PHY) intellectual property (IP) instances. These PHY IP cores recover the receiver (RX) clocks from their respective 1G/10 Gbps Ethernet ports. The reference design selects one clock as a master system clock based on the SyncE management software control and sends it to an FPGA output. Under the standard, a SyncE clock system has only one primary master clock traceable to a carrier atomic or GPS-driven PRC, similar to the clock configuration of an SDH network. The FPGA core is filled with instances of a digital noise-maker design to create a real world scenario for measuring the clock parameters. The Si5345 ITU-T G.8262 SyncE standard-compliant PLL from Silicon Labs then attenuates the selected clock signal’s wander and jitter to within the SyncE specification. This stabilized clock is used to feed the FPGA’s serial transmitter (TX) PLL in sync with the master Ethernet port’s clock frequency to realize a complete synchronization loop. This reference design can support multiple reconfigurable serial transceiver channels in SyncE mode at 1 Gbps or 10 Gbps line rate using Altera’s Stratix V GX FPGA Transceiver Signal Integrity Development Kit. The design can be modified to support 40Gb and 100Gb Ethernet MAC and PHY IP, and clocks as well. For the Si5345 G.8262 synchronous Ethernet full compliance test results, refer to the Si5345 Synchronous Ethernet G.8262 Compliance Test Results document on the Silicon Labs website (www.silabs.com). In addition to providing G.8262-compliant timing, the Si5345 PLL helps to minimize system cost and complexity. The Si5345 requires no external VCXO, which keeps bill of materials cost to a minimum. In addition, the Si5345 contains on-chip power supply regulation, which allows it to be connected directly to switching power supplies with no need for expensive power supply filtering to achieve high performance. To the extent HFT contends that Altera fails to teach this limitation, this limitation would have been obvious to a person of ordinary skill in the art based on this reference either alone or in combination with the knowledge of one of ordinary skill in the art.

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Claims	Exemplary Disclosures from the Prior Art
[11] The method of claim 1, wherein the first amount of data streams is the same as the second amount of data streams.	Altera discloses the first amount of data streams is the same as the second amount of data streams. <i>See, e.g.:</i> Altera at 2: Figure 1. High-Level Example of a SyncE System Line Card Using Altera FPGA and Silicon Labs SyncE PLL The diagram illustrates a System Line Card architecture. It features an Altera FPGA and a Silicon Labs Si5345 SyncE PLL. The Altera FPGA contains multiple Ethernet MAC and PCS blocks, Serial Transceivers (TX and RX), and an fPLL. Data streams flow from the Ethernet MACs through the transceivers to Optical Modules/Direct Attach Copper Cables. Clock signals are managed by the Si5345 PLL, which receives a TCXO input and provides a 15.625 MHz output to the FPGA. The fPLL in the FPGA generates a sys_tx_master_clk and rx_ref_clk signals. A note specifies clock frequencies: 125 MHz for 1 GbE, 644.53125/322.265625 MHz for 10 GbE and 25 Gb Serial, and 156.25 MHz for XAUI.

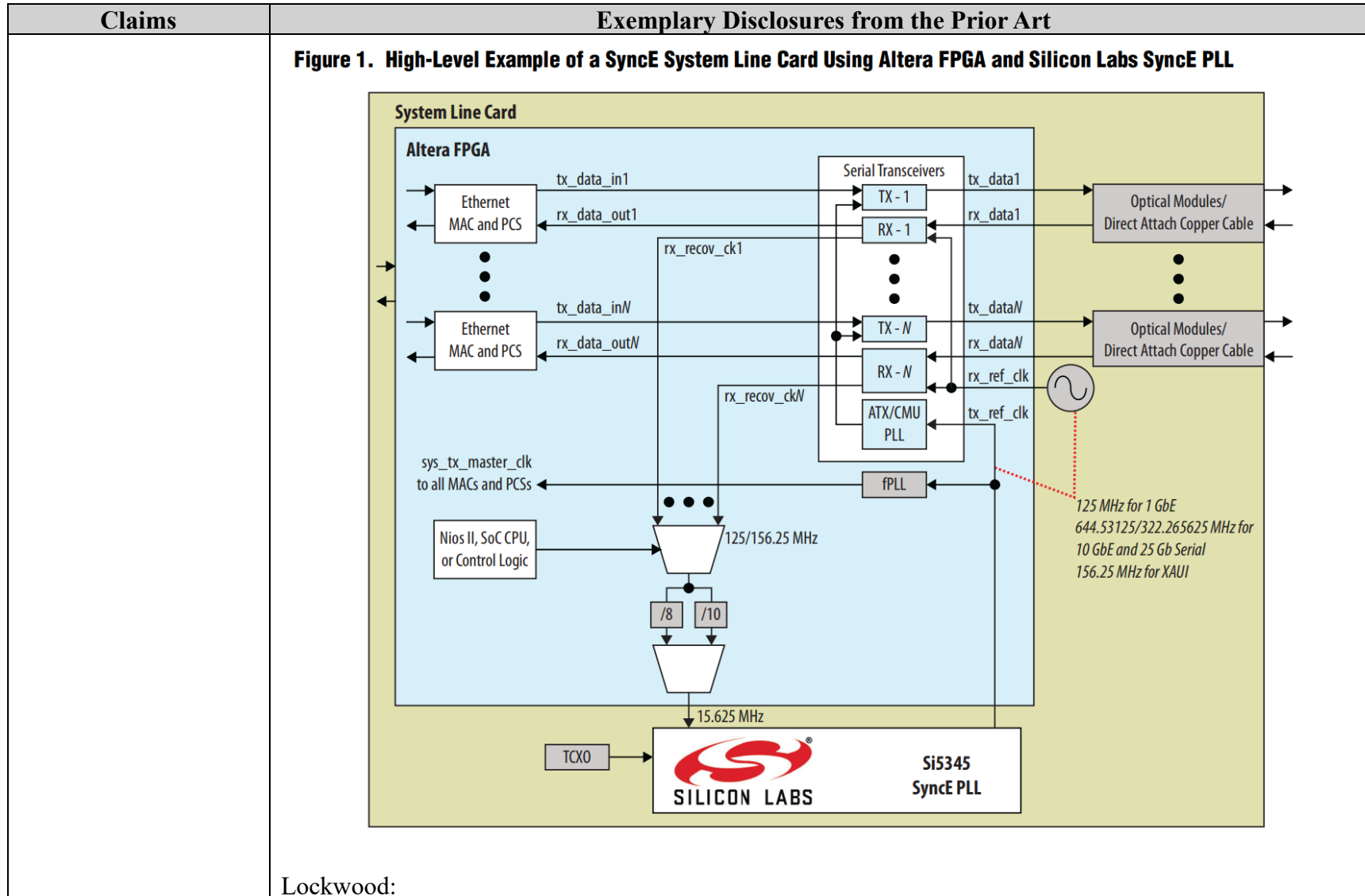
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Claims	Exemplary Disclosures from the Prior Art
	Altera at 2: Altera and Silicon Labs have developed a high-performance SyncE solution based on the two companies' products. A high-level system diagram is shown in Figure 1. This solution consists of an Altera® SyncE reference design implementing up to ten 1G/10 Gbps Ethernet (1G/10GbE) ports in Altera's Stratix® V FPGA interoperating with Silicon Labs' Si5345 jitter-attenuating phase-locked loop (PLL) to provide a complete SyncE clock recovery, clock selection, and synchronization sub-system. This solution can be used in wireless or wireline networking equipment to realize an accurate SyncE clock synchronization. To the extent HFT contends that Altera fails to teach this limitation, this limitation would have been obvious to a person of ordinary skill in the art based on this reference either alone or in combination with the knowledge of one of ordinary skill in the art.
[19] The method of claim 1, wherein the transmission of the second serial data stream from the serializer off the field programmable gate array is transmitted to an input/output module off the field programmable gate array.	Altera discloses transmitting the second serial data stream from the serializer off the field programmable gate array to an input/output module off the field programmable gate array. <i>See, e.g.:</i> Altera at 2:

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Claims	Exemplary Disclosures from the Prior Art
	Figure 1. High-Level Example of a SyncE System Line Card Using Altera FPGA and Silicon Labs SyncE PLL To the extent HFT contends that Altera fails to teach this limitation, this limitation would have been obvious to a person of ordinary skill in the art based on this reference either alone or in combination with the knowledge of one of ordinary skill in the art.
[20] The method of claim 1, wherein the first serial data stream includes market data and the second serial data stream includes trading data.	A person of ordinary skill in the art would understand that Altera could be used wherein the first serial data stream includes market data and the second serial data stream includes trading data, as taught by Lockwood. Altera at 2:

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Lockwood:

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Claims	Exemplary Disclosures from the Prior Art
	Figure 2 illustrates a typical Smart NIC in a supervised financial trading application. The system consists of an Exchange(s) connected to a Market Feed(s), which feeds into a PCIe FPGA-based NIC. Inside the NIC, data flows through a MAC & Network Stack, Feed Parse/Filter, Book Management, Order Mgt, and Trading Algorithm(s). The NIC is connected to a Host via a Host PCIe bus. The Host contains Supervision & Reporting/Visualisation (in software).
	Figure 3 illustrates the Host and NIC architecture. The Host is divided into Data Link Layer, Network Layer, and Application Layer. The NIC is divided into Physical Layer and Programmable Logic. The Physical Layer contains a PHY. The Programmable Logic contains a Serial Tx/Rx, MAC, TCP Stack, and Financial Application. The Network is connected to the PHY. Financial Data is shown entering the Host.

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Claims	Exemplary Disclosures from the Prior Art
	A person of ordinary skill in the art would have been motivated to combine Altera and Lockwood. Specifically, a POSA would have been motivated to use Altera in high-frequency trading applications as described in Lockwood to minimize latency. A POSA seeking to implement the Altera FPGA for high-frequency trading would have a reasonable expectation of success because a skilled artisan would recognize that the Altera FPGA's programmable logic could be used to process financial data in high-frequency trading.