

**IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
MIDLAND/ODESSA DIVISION**

HFT Solutions, LLC,

Plaintiff,

v.

OPTIVER US LLC and OPTIVER TRADING
US LLC,

Defendant.

Civil Action No. 7:25-CV-00415

JURY TRIAL DEMANDED

**DEFENDANT OPTIVER US LLC AND OPTIVER TRADING US LLC’S
PRELIMINARY INVALIDITY CONTENTIONS**

Pursuant to Judge Counts’s Standing Order Governing Patent Proceedings, entered August 2, 2022; Magistrate Judge Gilliland’s Standing Order Governing Patent Proceedings (OGP) 4.4 – Patent Cases, signed May 30, 2024; and the Court’s Scheduling Order (Dkt. 24), Defendants Optiver US LLC and Optiver Trading US LLC (“Optiver”) hereby provides the following contentions to Plaintiff HFT Solutions LLC (“HFT” or “Plaintiff”) for United States Patent Nos. 10,931,286 (“’286 Patent”); 11,128,305 (“’305 Patent”); and 11,575,381 (“’381 Patent”).

I. INTRODUCTION

On December 8, 2025, HFT served its Preliminary Infringement Contentions, asserting the following claims:

’286 patent: Claims 1-4, 6-8, 10-13, 16-22

’305 patent: Claims 1-11 and 14-22; and

’381 patent: Claims 1-12

(collectively, the “Asserted Patents” and the “Asserted Claims”). Optiver contends that each of the Asserted Claims is not patent-eligible under 35 U.S.C. § 101, and is invalid under at least 35 U.S.C. §§ 102, 103, and/or 112.

These Preliminary Invalidity Contentions address the claims identified in HFT’s December 8, 2025 Preliminary Infringement Contentions, and are based on HFT’s apparent infringement positions. Nothing in these contentions should be taken as an admission that an element that these Preliminary Invalidity Contentions identify as being in the prior art would infringe under the proper interpretation of the claims. These Preliminary Invalidity Contentions reflect Optiver’s knowledge, thinking, and contentions as of the date of service. Optiver reserves the right to modify, amend, or supplement these Preliminary Invalidity Contentions as appropriate and for any permissible reason, including those not explicitly stated herein. For example, Optiver shall serve its final invalidity contentions pursuant to the schedule set forth in this Court’s Scheduling Order. Optiver further reserves the right to supplement these Preliminary Invalidity Contentions in view of subsequent case events, including the Court’s claim construction order, HFT’s disclosures, any amended or supplemental infringement contentions (including by modifying the claims asserted), arguments made and positions taken by HFT during fact and expert discovery, arguments made and positions taken by HFT in any matter involving the Asserted Patents, and any forthcoming document productions or other information or testimony produced by HFT or any third parties, including in response to third party subpoenas.¹ Optiver also reserves the right to further supplement these Preliminary Invalidity Contentions if it becomes aware of

¹ Optiver intends to serve subpoenas regarding, at least, one or more of the system art references identified in Section II.B.2.

additional prior art, becomes aware of additional features of the prior art references cited below, or becomes aware of any other relevant information obtained through discovery or otherwise.

Furthermore, Optiver may subsequently amend or supplement these disclosures because HFT's Infringement Contentions are deficient in numerous respects. For example, HFT has failed to specifically identify where each element of each Asserted Claim is found within each accused instrumentality and/or failed to identify any coherent theory that the accused instrumentalities perform or are capable of performing key claim limitations.² HFT has further failed to identify the type of conduct alleged to infringe or the persons or entities that allegedly engage in such conduct for indirect infringement.³ Because any attempt to cure such deficiencies may lead to further grounds for invalidity of the Asserted Claims, Optiver specifically reserves the right to modify, amend, or supplement these disclosures should HFT amend or supplement its Infringement Contentions to address any deficiencies.

Optiver may also amend this disclosure in response to any positions taken by HFT during the course of the litigation, or positions taken by HFT in any matter involving the Asserted Patents, including without limitation in response to HFT's positions on claim construction or any contention by HFT that one or more of the prior art references described herein fail to render the Asserted Claims anticipated or obvious. Optiver further reserves the right to amend these Preliminary Invalidity Contentions to rely upon inventor and party admissions concerning the scope of the Asserted Claims and the teachings of the prior art and in response to any additional claim construction order from the Court.

² See, e.g., December 22, 2025, Correspondence from J. Tabat to J. Scheufler.

³ *Id.*

A. Priority Date

In its Preliminary Infringement Contentions, HFT contends that the Asserted Claims of all Asserted Patents are entitled to a priority date of November 5, 2018. Nothing in these Preliminary Invalidity Contentions shall be understood as an agreement that any Asserted Patent or Asserted Claim is entitled to claim priority to the date identified by HFT, nor that any Asserted Claim was allegedly invented by such date. Optiver reserves the right to argue that one or more claims of the Asserted Patents are not entitled to claim priority to Provisional Application No. 62/755,804 (“the ’804 Provisional”) or Provisional Application No. 62/803,017. Optiver further reserves the right to all relief, including the right to amend these Preliminary Invalidity Contentions and identify additional prior art references, if HFT is permitted by the Court to later assert an earlier priority date.

Any reference to a “priority date” or an “asserted priority date” in these Preliminary Invalidity Contentions refers to the priority date identified by HFT above. Reference to a “priority date” or an “asserted priority date” should not be construed to mean that Optiver agrees that any of the Asserted Patents or Asserted Claims is in fact entitled to such priority date, or that HFT has provided proper notice as to its contentions for a priority date. To the extent HFT alleges that any prior art relied on in these Preliminary Invalidity Contentions does not actually qualify as prior art to an Asserted Patent, HFT bears the burden of coming forward with evidence that the Asserted Claims are entitled to the benefit of a filing or invention date earlier than the prior art. *See Tech. Licensing Corp. v. Videotek Inc.*, 545 F.3d 1316, 1327 (Fed. Cir. 2008). To the extent that HFT meets its burden of production, Optiver reserves the right to rebut any such allegations by, for example, demonstrating an earlier effective date for the challenged prior art and/or a later priority

date for a particular Asserted Patent and/or Asserted Claim.⁴ To the extent HFT successfully establishes a filing or invention date earlier than a prior art reference relied on by Optiver, that reference serves at least as evidence of secondary considerations of obviousness, particularly, contemporaneous invention by others.

B. Claim Construction

The Court has not yet construed any terms of the Asserted Claims. Optiver's Preliminary Invalidity Contentions are based on (1) Optiver's present understanding of the Asserted Claims and (2) the claim constructions HFT appears to be proposing based on the Infringement Contentions and/or the positions HFT has taken in other proceedings involving the Asserted Patents, all without regard to whether Optiver agrees with HFT's apparent or expressed claim constructions. Optiver explicitly does not agree with HFT's apparent or expressed claim constructions in certain instances, but to the extent HFT's constructions are accepted, the limitations are disclosed by the prior art.

Optiver reserves the right to supplement or otherwise amend these Preliminary Invalidity Contentions in response to any court-ordered claim constructions, proposed claim constructions or alleged supporting evidence offered by HFT, any report from any expert witness for HFT regarding claim construction issues, any claim construction briefing filed by HFT, and any position taken by HFT concerning claim construction, infringement, or invalidity.

Optiver takes no position on any matter of claim construction in these Preliminary Invalidity Contentions, including whether any particular claim element should be construed according to 35 U.S.C. § 112(f). If Optiver's disclosures herein are consistent with any explicit, apparent, or implied claim constructions in HFT's Infringement Contentions, no inference is

⁴ Optiver reserves the right to rely on additional documents and evidence to rebut any efforts by HFT to allege any reference was not publicly available or otherwise available as prior art.

intended and no inference should be drawn that Optiver agrees with any of HFT's claim constructions. Any statement herein describing or tending to describe any claim element is provided solely for the purpose of understanding and/or applying the cited prior art. In addition, to the extent that these Preliminary Invalidity Contentions rely on or otherwise embody a particular order in which the steps of method claims are performed, Optiver does not necessarily propose that the method claims must be limited to such order, although Optiver may later propose such an order.

Nothing herein should be read to suggest that Optiver agrees that any particular claim term is sufficiently definite, enabled or supported by the written description to meet the requirements of 35 U.S.C. § 112. Likewise, nothing herein should be read to suggest that Optiver agrees that the preamble of any claim is or is not limiting. In addition, nothing herein admits in any way that any of Optiver's accused instrumentalities infringes any of the Asserted Claims.

Optiver expressly reserves the right to propose any claim construction Optiver considers appropriate and to contest any claim construction proposed by HFT that Optiver considers inappropriate or inaccurate. Because any positions taken in these disclosures are based on the claim scope apparently asserted by Optiver in its Infringement Contentions, with which Optiver may disagree, Optiver may take positions with respect to claim construction issues that are inconsistent with, or even contradictory to, positions expressed or implied in these Preliminary Invalidity Contentions. The parties' proposed schedule has established separate deadlines for the parties' proposed claim constructions, and Optiver will disclose any terms requiring construction as well as its proposed constructions accordingly, or with any schedule ordered by the Court.

Prior art not included in these Preliminary Invalidity Contentions, whether or not now known to Optiver, might become relevant depending on the claim constructions proposed by

Optiver and/or the Court's claim construction rulings. Optiver reserves all rights to supplement or modify the positions and information in these Preliminary Invalidity Contentions, including, without limitation, the prior art and grounds of invalidity set forth herein, after the Court has construed the Asserted Claims.

C. Ongoing Investigation and Discovery

Optiver bases these Preliminary Invalidity Contentions on its current knowledge and understanding of the Asserted Patents, HFT's Infringement Contentions, and other facts and information available as of the date of these contentions. Optiver's investigation into prior art—including prior art identified in these disclosures, prior art in the possession of HFT, third-party prior art (including system art and related evidence), documents, and knowledgeable witnesses—is ongoing.

Once discovery begins, Optiver expects to present additional information and evidence in support of its Preliminary Invalidity Contentions, and to revise, amend, and/or supplement these Preliminary Invalidity Contentions accordingly in a manner consistent with the Federal Rules of Civil Procedure and the Court's rules and applicable orders.

Optiver further reserves the right to rely on statements or admissions from those owing a duty of candor, such as named inventors, prosecution counsel, and others involved in the prosecution of the patent applications or related applications or patents and applications on related technology, concerning the scope of the prior art relevant to the Asserted Patents found in, *inter alia*, the following: the respective prosecution histories of the Asserted Patents and related patent applications; any deposition testimony of the named inventors; and the papers filed and any evidence submitted by HFT in connection with this litigation or other litigation related to the Asserted Patents.

Prior art not identified in this disclosure, whether known or not known to Optiver, may become relevant, including prior art concerning the state of the art at the time of invention, as well as simultaneous or near-simultaneous independent invention by others. For instance, Optiver currently is unaware of the extent, if any, to which HFT will contend that limitations of the Asserted Claims are not disclosed in the prior art identified by Optiver. To the extent that such an issue arises, Optiver reserves the right to identify other references that would disclose, practice, or render obvious the allegedly missing limitation(s) of the disclosed subject matter.

D. Prior Art Identification

In these Preliminary Invalidity Contentions, Optiver identifies specific portions of prior art references that disclose the elements of the Asserted Claims. While Optiver has identified exemplary prior art references for each element, it does not necessarily identify every disclosure of the same element in each prior art reference. A person of ordinary skill in the art would read a prior art reference as a whole and in the context of other publications, literature, and general knowledge in the field and would rely upon other information, including other publications and general scientific or engineering knowledge. Optiver therefore reserves the right to rely upon other unidentified portions of the prior art references and on other publications and prior art products and expert testimony to provide context and to aid understanding and interpretation of the identified portions of the prior art.

Optiver also reserves the right to rely upon (1) other portions of the cited prior art references, other publications, prior art products, and the testimony of experts to establish that the alleged inventions would have been obvious to a person of ordinary skill in the art, including on the basis of modifying or combining certain cited references; (2) admissions relating to prior art in the Asserted Patents or related patents, the prosecution history of the Asserted Patents or related patents, or other admissions obtained during discovery; and (3) foreign counterparts of any U.S.

patents, and their file histories, identified in Optiver's Preliminary Invalidity Contentions. Where a prior art reference includes citations to other references, those other references are considered incorporated by reference for context.

The references discussed in the claim charts may disclose all elements of the Asserted Claims explicitly and/or inherently, and/or they may be relied upon to show the state of the art in the relevant time frame. The suggested obviousness combinations are provided in the alternative to Optiver's anticipation contentions and are not to be construed to suggest that any reference included in the combinations is not by itself anticipatory.

Where Optiver identifies in the claim charts a particular figure in a prior art reference, the identification should be understood to encompass the caption and description of the figure as well as any text relating to the figure in the specification and prosecution history in addition to the figure itself. Similarly, where an identified portion of text refers to a figure or other material, the identification should be understood to include the referenced figure or other material as well.

E. No Patentable Weight

Optiver reserves the right to argue that various portions of the Asserted Claims, such as an intended use or result, non-functional descriptive material, and certain preamble language, are entitled to no patentable weight. Mapping of a portion of an Asserted Claim to a prior art reference does not represent that such portion of the claim is entitled to patentable weight when comparing the claimed subject matter to the prior art.

II. INVALIDITY UNDER 35 U.S.C. §§ 102 AND 103

Optiver contends that each Asserted Claim is invalid as anticipated by the prior art under 35 U.S.C. § 102 and/or as obvious in view of the prior art, the knowledge of a person having ordinary skill in the art, and/or secondary factors of obviousness under 35 U.S.C. § 103.

The obviousness combinations of references provided in Optiver's invalidity claim charts under 35 U.S.C. § 103 are exemplary and are not intended to be exhaustive. In particular, Optiver is currently unaware of the extent, if any, to which HFT will contend that limitations of the Asserted Claims are not disclosed in the art identified by Optiver as anticipatory. To the extent an issue arises with any such limitation, Optiver will identify other obviousness combinations and/or other references that would have made obvious the addition of the allegedly missing limitation to the disclosed device, system, or method of operation.

Optiver's prior art investigation and third-party discovery is not yet complete. Optiver reserves the right to present additional items of prior art under 35 U.S.C. §§ 102 and/or 103 located during the course of discovery or further investigation. For example, Optiver may issue subpoenas to third parties believed to have knowledge, documentation, and/or corroborating evidence concerning some of the prior art listed below and/or additional prior art. These third parties include without limitation the authors, inventors, or assignees of the references listed in these disclosures. In addition, Optiver reserves the right to assert invalidity under other subsections of 35 U.S.C. § 102 to the extent that discovery or further investigation yields information forming the basis for such invalidity.

A patentee bears the burden of production with respect to evidence of secondary considerations of non-obviousness. *ZUP, LLC v. Nash Mfg., Inc.*, 896 F.3d 1365, 1373 (Fed. Cir. 2018). As of the date of these Preliminary Invalidity Contentions, HFT has not identified any evidence of secondary considerations, nor does HFT offer any evidence or explanation to support its allegations. As shown in these Preliminary Invalidity Contentions, other companies and individuals described, built, and/or patented the exact same concepts in the Asserted Patents before HFT ever did—often many years before. Even where others' invention(s) occurred around the

same time as the Asserted Patents, such simultaneous invention demonstrates the obviousness of the Asserted Patents.

Potentially relevant evidence includes any prior art reference cited herein that was publicly known or available before or around the alleged inventions claimed in the Asserted Patents. This also includes any prior art asserted in these Preliminary Invalidity Contentions that HFT is able to pre-date based on its asserted priority dates by proving, *inter alia*, that the subject matter of the Asserted Claims was publicly disclosed by the inventor or a joint inventor or another who obtained the subject matter disclosed directly or indirectly from the inventor or a joint inventor within one year prior to HFT's asserted priority date.

Optiver reserves all rights to further respond to any secondary considerations of non-obviousness raised by HFT, including by updating, modifying, and/or adding to these Preliminary Invalidity Contentions. Optiver is not aware of any unexpected results (none is mentioned in the Asserted Patents or their file histories), long-felt need, commercial success (or any nexus to any allegedly successful commercial embodiment), or awards for the alleged inventions of the Asserted Patents.

A. State of the Art

The subject matter of the Asserted Claims was well understood to those of skill in the art as of the respective priority dates of the Asserted Patents. To describe the background state of the art at the time of the alleged priority dates, Optiver may rely on at least that which is set forth in the Asserted Patents, the file histories, the prior references discussed therein, those references listed in Section IIB.B and charted in Exhibits A-1 to C-16, any references produced in Optiver's accompanying document production, and the references listed below:

- U.S. Patent No. 10,491,722 ("Snowdon")
- U.S. Patent No. 9,521,636 ("Shor")

- U.S. Patent No. 10,326,457 (“Perez”)
- U.S. Patent No. 11,088,695 (“Bae”)
- U.S. Patent No. 8,045,669 (“Ballantyne”)
- U.S. Patent No. 9,559,881 (“Carvalho”)
- U.S. Patent No. 6,675,306 (“Baxter”)
- U.S. Patent No. 8,650,429 (“Starr”)
- U.S. Patent No. 10,037,568 (“Taylor”)
- U.S. Patent No. 7,921,046 (“Parsons”)
- U.S. Patent No. 5,621,774
- U.S. Patent No. 5,892,370
- U.S. Patent No. 6,130,552
- U.S. Patent No. 6,188,255
- U.S. Patent No. 6,252,419
- U.S. Patent No. 6,542,096
- U.S. Patent No. 7,015,838
- U.S. Patent No. 7,046,056
- U.S. Patent No. 7,210,052
- U.S. Patent No. 7,227,875
- U.S. Patent No. 7,366,270
- U.S. Patent No. 7,434,080
- U.S. Patent No. 7,439,788
- U.S. Patent No. 7,486,718
- U.S. Patent No. 7,656,323
- U.S. Patent No. 7,668,524
- U.S. Patent No. 7,743,168
- U.S. Patent No. 7,986,190
- U.S. Patent No. 8,344,769
- U.S. Patent No. 8,384,453
- U.S. Patent No. 8,665,928
- U.S. Patent No. 8,873,606
- U.S. Patent No. 8,949,680
- U.S. Patent No. 9,002,693
- U.S. Patent No. 9,197,397
- U.S. Patent No. 9,379,880
- U.S. Patent No. 9,564,905
- U.S. Patent No. 9,792,247
- U.S. Patent No. 10,063,367
- U.S. Patent No. 10,305,495
- U.S. Patent No. 10,389,372
- U.S. Patent No. 10,447,463
- U.S. Patent Pub. No. 2003/0012322
- U.S. Patent Pub. No. 2003/0093703
- U.S. Patent Pub. No. 2005/0078683
- U.S. Patent Pub. No. 2007/0105495

- U.S. Patent Pub. No. 2008/0130891
- U.S. Patent Pub. No. 2009/0063889
- U.S. Patent Pub. No. 2012/0087418
- U.S. Patent Pub. No. 2015/0095109
- U.S. Patent Pub. No. 2016/0218818
- U.S. Patent Pub. No. 2017/0222792
- U.S. Patent Pub. No. 2018/0123775
- U.S. Patent Pub. No. 2019/0020466
- CN 101951313
- CN 103338041
- Japan Patent Pub. No. 2000/138661
- Japan Patent No. 5,535,753
- WO 2013/022192
- High Precision Timing IP Core by Mendes (“Mendes”)
- John W. Lockwood et al., *A Low-Latency Library in FPGA Hardware for High-Frequency Trading (HFT)*, IEEE 20th Annual Symposium on High-Performance Interconnects 9 (2012) (“Lockwood”)
- Fred Hirning, *Improve FPGA communications interface clock jitters with external PLLs*, Embedded (Sept. 26, 2014, 3:23 PM), <https://www.embedded.com/improve-fpga-communications-interface-clock-jitters-with-external-plls/> (“Hirning”)
- Synchronous Ethernet Solutions with Altera FPGAs and Silicon Labs Jitter-Attenuating PLLs by Rahbar et al. (“Rahbar”)
- Altera and IDT Synchronous Ethernet Solution for ITU-T G.8262 by Auyeung et al. (“Auyeung”)
- Common Public Radio Interface (CPRI); Interface Specification V5.0 by Ericsson AB et al. (“CPRI”)
- Low Latency Transceiver Designs for Quantitative Finance by Ireland
- FELIX: The new detector readout system for the ATLAS experiment by Ryu
- The GBT-FPGA core: features and challenges by Marin et al.
- Development of FPGA-based High Speed Serial Links for High Energy Physics Experiments by Perrella
- Low Latency Data Transmission in LLRF Systems by Makowski et al.
- Fixed-Latency, Multi-Gigabit Serial Links With Xilinx FPGAs by Giordano et al.
- Xilinx VCU118 Evaluation Board (“Xilinx VCU118”)
- Xilinx ZC706 Evaluation Board (“Xilinx ZC706”)
- Intel Cyclone 10 GX FPGA (“Intel Cyclone 10 GX”)
- Bittware XUPVV4
- XpressVUP
- Altera SyncE (Stratix V + Si 5345) (“Altera SyncE”)
- Silicon Labs Si5347, Si5346 Family Reference Manual
- Silicon Labs Si5345/44/42 Rev D Data Sheet; Si5347/46 Datasheet
- Xilinx 7 Series
- Altera PHYLite
- Terasic DE5

- Texas Instruments LMK05028
- Metamako MetaConnect
- National Instruments NI 5761R
- Xilinx Virtex 7
- Xilinx ZCU111 Evaluation Board
- Altera Xilinx Alveo U200 and U250 Accelerator Cards
- Altera Stratix V Device Handbook Volume 1: Device Interfaces and Integration
- Altera Arria 10 Transceiver PHY User Guide

The information discussed in the prior art raised in these Invalidity Contentions (including all referenced listed in Section IIB.B) forms part of the background knowledge of a person of ordinary skill in the art at the time each of the Asserted Patents was filed and would have been used in determining whether and how to combine references to achieve the claimed invention(s), as discussed herein.⁵ Indeed, the existence, nature, and content of each prior art reference, including the prior art references cited here, provide further evidence regarding the knowledge of a person of ordinary skill in the art at the relevant time. Optiver expressly reserves the right to rely on each of the prior art references, systems, concepts, and technologies discussed in these Invalidity Contentions, including to demonstrate that a particular claim element was known at the time of the Asserted Patents to a person of ordinary skill in the art, to show that the differences between a claimed invention and a prior art reference would have been obvious to a person of ordinary skill in the art, and to establish that a person of ordinary skill in the art would have been motivated to combine teachings of one or more references to achieve a claimed invention.

B. Identification of Prior Art

Optiver identifies the following prior art now known to Optiver that anticipates or renders obvious one or more of the Asserted Claims. Each of the following patents, publications, systems,

⁵ See *Randall Mfg. v. Rea*, 733 F.3d 1355, 1362 (Fed. Cir. 2013) (stating that “the knowledge [of a person of ordinary skill in the art] is part of the store of public knowledge that must be consulted when considering whether a claimed invention would have been obvious”).

and products is prior art under at least one or more of 35 U.S.C. § 102(a)(1) or (a)(2), as applicable. Optiver's reliance on each prior art reference identified throughout these Preliminary Invalidity Contentions includes the reference itself, anything incorporated by the reference, and any testimony by those with knowledge of the reference, such as named authors and inventors. On information and belief, each listed document or item became prior art at least as early as the dates specified.

To the extent any limitation of any of the Asserted Claims is construed to have a similar meaning, or to encompass similar feature(s) and/or function(s), with any other claim limitation, and to the extent at least one claim chart in Exhibits A-1 to C-16 hereto identifies any prior art reference as disclosing or teaching such similarly construed claim limitation, such identified prior art reference and Optiver's contentions with respect to same are incorporated by reference. Priority dates identified for the prior art references are based on information currently available to Optiver, and Optiver will amend this disclosure to the extent additional information becomes available.

To the extent that they are prior art, Optiver reserves the right to rely upon (1) foreign counterparts of the U.S. Patents identified in Optiver's Preliminary Invalidity Contentions, (2) U.S. counterparts of foreign patents and foreign patent applications identified in Optiver's Preliminary Invalidity Contentions, and (3) U.S. and foreign patents and patent applications corresponding to articles and publications identified in Optiver's Preliminary Invalidity Contentions.

The prior art identified below is exemplary; the claimed features are similarly described or disclosed in additional prior art. Thus, Optiver reserves the right to rely on other evidence of the prior art beyond the example references identified, including the prior art identified in Section II.A.

The primary references identified below, and as further described in Exhibits A-1 to C-16, each discloses, either expressly or inherently, every element of the Asserted Claims, thereby

anticipating those claims. To the extent HFT contends that any primary reference does not anticipate the Asserted Claims, it would have been obvious to combine or modify the primary references with concepts from other prior art, as explained herein and in Appendices A–C.

In particular, for each limitation of the Asserted Claims that HFT contends is not met by a particular primary reference, Optiver contends that the limitation (and claim as a whole) is obvious based on a combination of that particular primary reference with (1) any other primary reference disclosing that limitation, (2) any admitted prior art, as explained in the background of each patent or discussed in the file history, (3) any reference identified in Appendices A–C as disclosing that limitation, and/or (4) the knowledge of a person of ordinary skill in the art and/or any of the references and concepts discussed herein regarding the relevant background and state of the art. The specific combinations of prior art that Optiver contends render the Asserted Claims obvious are readily determinable as described herein, which is the most efficient manner of identifying the combinations in light of the fact that HFT has asserted a total of 50 claims across three related patents. Optiver’s obviousness grounds for each dependent claim incorporate the obviousness grounds for the claim(s) from which the dependent claim depends in addition to any obviousness grounds identified in the charts for the dependent claim.

Optiver does not yet have the benefit of HFT’s positions on the prior art, including what (if any) elements it contends are missing in each prior art reference, whether HFT agrees that a reference is in fact prior art, and whether HFT agrees that a person of ordinary skill in the art would be motivated to combine specific references. Optiver reserves the right to supplement these obviousness positions (including identifying additional prior art combinations and the associated reasons to combine) as discovery in the case progresses, including expert discovery.

Optiver further incorporates by reference the arguments, prior art, expert testimony, and any filings or findings in the following *inter partes* review proceedings challenging the Asserted Patents or any related patents, as well as any invalidity theories advanced against the Asserted Claims in any other litigation or other patent office proceedings that may be brought involving the Asserted Claims or that HFT has been made aware of.

1. Prior Art Patents / Publications

- U.S. Patent No. 10,491,722 (“Snowdon”)
- U.S. Patent No. 9,521,636 (“Shor”)
- U.S. Patent No. 10,326,457 (“Perez”)
- U.S. Patent No. 11,088,695 (“Bae”)
- U.S. Patent No. 8,045,669 (“Ballantyne”)
- U.S. Patent No. 9,559,881 (“Carvalho”)
- U.S. Patent No. 6,675,306 (“Baxter”)

2. Prior Art Systems

Optiver may argue that the below and other systems, including constituent software, hardware, methods, and processes, constitute prior art that renders the Asserted Claims of the Asserted Patents invalid. Optiver will supplement as discovery progresses.

- Xilinx VCU118 Evaluation Board (“Xilinx VCU118”)
- Xilinx ZC706 Evaluation Board (“Xilinx ZC706”)
- Intel Cyclone 10 GX FPGA (“Intel Cyclone 10 GX”)
- Bittware XUPVV4
- XpressVUP
- Altera SyncE (Stratix V + Si 5345) (“Altera SyncE”)
- High Precision Timing IP Core by Mendes (“Mendes”)
- Terasic DE5
- Texas Instruments LMK05028

3. Obviousness and Secondary References

Optiver identifies each of the references listed above as primary references that render this patent anticipated, or at least obvious in view of the knowledge of a person of ordinary skill in the art. In addition, these primary references may be combined with each other or with the secondary

references listed below to render this patent obvious under 35 U.S.C. § 103. One of ordinary skill in the art would be motivated to combine these references as explained in Section II.D:

- U.S. Patent No. 7,921,046 (“Parsons”)
- U.S. Patent No. 8,650,429 (“Starr”)
- U.S. Patent No. 10,037,568 (“Taylor”)
- John W. Lockwood et al., *A Low-Latency Library in FPGA Hardware for High-Frequency Trading (HFT)*, IEEE 20th Annual Symposium on High-Performance Interconnects 9 (2012) (“Lockwood”)
- Fred Hirning, *Improve FPGA communications interface clock jitters with external PLLs*, Embedded (Sept. 26, 2014, 3:23 PM), <https://www.embedded.com/improve-fpga-communications-interface-clock-jitters-with-external-plls/> (“Hirning”)

C. Claim Charts

Charts specifically identifying where each element of each Asserted Claim is found in the prior art, either expressly or inherently, are found in Exhibits A-1 to C-16. However, this prior art is exemplary; the claimed features are similarly described or disclosed in other prior art.

In the claim charts included in this disclosure, Optiver identifies specific portions of prior art references that disclose or render obvious the elements of the Asserted Claims. Although Optiver has identified at least one citation per element, each and every disclosure of the same element in a given reference is not necessarily identified. That Optiver did not identify each similar disclosure should not be construed as a concession by Optiver that such disclosure is not relevant. It should be recognized that a person of ordinary skill in the art would generally read a prior art reference as a whole and in the context of other publications, literature, and general knowledge in the field. To understand and interpret any specific statement or disclosure in a prior art reference, a person of ordinary skill in the art would rely upon other information, including other publications and general scientific or engineering knowledge.

Where Optiver identifies a particular figure in a prior art reference, the identification should be understood to encompass the caption and description of the figure as well as any text relating

to the figure in the specification and prosecution history in addition to the figure itself. Similarly, where an identified portion of text refers to a figure or other material, the identification should be understood to include the referenced figure or other material as well.

Certain pieces of identified prior art disclose features of the Asserted Claims inherently. Optiver may rely on any evidence, including expert testimony, to establish the inherency of certain features of the prior art to invalidate the Asserted Claims.

D. Motivation to Combine Prior Art

Optiver believes that no showing of a specific motivation to combine prior art is required to combine the references disclosed in the attached charts; there was a reason to make each combination, each combination of art would have produced no unexpected results, and each combination at most would simply represent a known alternative to one of ordinary skill in the art. *See KSR Int'l Co. v. Teleflex, Inc.*, 550 U.S. 398, 414–18 (2007) (rejecting the Federal Circuit’s “rigid” application of the teaching, suggestion, or motivation to combine test, and instead espousing an “expansive and flexible” approach). Indeed, the Supreme Court held that a person of ordinary skill in the art is “a person of ordinary creativity, not an automaton” and “in many cases a person of ordinary skill in the art will be able to fit the teachings of multiple patents together like a pieces of a puzzle.” *Id.* at 420–21.

In view of *KSR*, the PTO issued a set of new Examination Guidelines. *See* Examination Guidelines for Determining Obviousness Under 35 U.S.C. § 103 in View of the Supreme Court Decision in *KSR International Co. v. Teleflex Inc.*, 72 Fed. Reg. 57,526 (Oct. 10, 2007). Those Guidelines identified various rationales for finding a claim obvious, including:

- a) Combining prior art elements according to known methods to yield predictable results;
- b) Simple substitution of one known element for another to obtain predictable results;

- c) Use of known technique to improve similar devices (methods, or products) in the same way;
- d) Applying a known technique to a known device (method, or product) ready for improvement to yield predictable results;
- e) “Obvious to try”—choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success;
- f) Known work in one field of endeavor may prompt variations of it for use in either the same field or a different one based on design incentives or other market forces if the variations would have been predictable to one of ordinary skill in the art; and
- g) Some teaching, suggestion, or motivation in the prior art that would have led one of ordinary skill to modify the prior art reference or to combine prior art reference teachings to arrive at the claimed invention.

Id. at 57,529.

In addition, the motivation to combine or modify prior art references is significantly stronger when, as here, the references seek to solve the same problem, come from the same field, and correspond well. *In re Inland Steel Co.*, 265 F.3d 1354, 1362 (Fed. Cir. 2001) (allowing two references to be combined as invalidating art under similar circumstances where the art “focus[ed] on the same problem . . . [,] c[a]me from the same field of art [and] . . . the identified problem found in the two references correspond[ed] well”).

The Asserted Claims are further obvious in view of the admitted prior art in the specification and file histories of the Asserted Patents. That is, the Asserted Patents themselves admit that certain features and claim elements were known in the prior art before the effective date of the Asserted Patents. Optiver reserves the right to rely on any admissions in the Asserted Patents as part of any obviousness combination, as part of the motivation to combine, and also to explain the state of the art at the time of the Asserted Patents.

Optiver has identified several exemplary motivations and reasons to combine the various references cited herein, and those motivations would have been supported, in part, by a reasonable

expectation of success. The various teachings, suggestions, and/or reasons to modify any of the references and/or to combine any two or more of the references in Exhibits A-1 to C-16 come from various sources, including the prior art (specific and as a whole), common knowledge, common sense, predictability, expectations, industry trends, design incentives or need, market demand or pressure, market forces, the nature of the problem faced, and/or the knowledge possessed by one of ordinary skill in the art. In addition, it would have been obvious to try combining the prior art references identified above.

These exemplary combinations demonstrate that there were only a finite number of predictable solutions to known problems addressed by the Asserted Patents. Furthermore, known work in one field or endeavor prompted variations based on predictable design incentives and/or market forces either in the same field or a different one. The combination of features found in the prior art references identified in these contentions would have been obvious because the claimed combinations represent the known potential options, with each such option having a reasonable expectation of success. Additionally, one of ordinary skill in the art would have been motivated to create combinations identified in these contentions using: known methods to yield predictable results; known techniques in the same way; a simple substitution of one known, equivalent element for another to obtain predictable results; and/or teaching, suggestion, or motivation in the prior art generally. Also, market forces in the industry, and the desire to improve features and performance, would motivate the addition of features to systems as they become available, become less expensive, become more commonly used, provide better performance and reliability, reduce costs, or predictably achieve other clearly desirable results.

Optiver has identified several exemplary motivations and reasons to combine the various references cited herein. For any reference for which there is a claim element that does not have a

corresponding citation in that reference, it would have been obvious to combine with the knowledge of a person of skill and/or any other reference in the primary or secondary charts for which there is a citation for that element. These combinations would have been obvious to try given that there were a finite number of identified, predictable solutions in the prior art, and there would have been a reasonable expectation of success to simply implement one prior art solution with concepts from prior art in the same field.

For example, a person of ordinary skill in the art would have been aware that an integrated circuit or FPGA necessarily uses pins for input and output to the chip. *See, e.g., '286 patent at 9:40, 12:25–36; Miha Smolnikar et al., A Framework for Developing a Microchip PIC Microcontroller Based Applications, 5 WSEAS Transactions on Advances in Engineering Education 83, 85–87 (2008).* For example, a person of ordinary skill in the art would have known that a clock signal necessarily possesses a phase and frequency, and thus that a clock signal inherently discloses a particular phase and frequency. *See, e.g., Andrew S. Tanenbaum & Maarten van Steen, Distributed Systems: Principles and Paradigms 241–46 (2002); Carvalho at 1:55-2:15.* As another example, a person of ordinary skill in the art would have known that an FPGA system necessarily uses a clock signal oscillator. *See, e.g., J. Serrano, Introduction to FPGA Design, CAS-CERN Accelerator School: Digital Signal Processing, 231-247 (2008).* As another example, a person of ordinary skill in the art would have been familiar with synchronous ethernet (SyncE), including that a phase-locked loop could be used to synchronize the phases of network clock signals and logic clock signals. *See, e.g., Rahbar at 3–5; Auyeung at 1, 5–6.* A person of ordinary skill in the art would have also known that low latency was particularly important in financial applications, and that FPGAs were thus particularly useful for financial or market uses. *See, e.g., Lockwood at 10–12; Parsons at 1:49–50.* A person of ordinary skill in the art would have also

known that programmable logic devices, including chips made by, e.g., Altera, could be used for high frequency trading. *From Hardware Emulation to High-Frequency Trading Riding the FPGA Wave*, EETimes, January 23, 2017 (available at <https://www.eetimes.com/from-hardware-emulation-to-high-frequency-trading-riding-the-fpga-wave/>); T. Verry, *Intel Launches Stratix 10 FPGA with ARM CPU and HBM2*, PC Perspective, October 10, 2016 (available at <https://pcper.com/2016/10/intel-launches-stratix-10-fpga-with-arm-cpu-and-hbm2/>). As another example, a person of ordinary skill in the art would have known that using a serializer/deserializer (SerDes) required clock synchronization to align data and process operations or transactions in the appropriate order. *See, e.g.*, Carvalho at 1:39–3:19; Tanenbaum & van Steen, *supra*, at 281–83, 288–89. And thus a person of ordinary skill in the art would have also recognized that basic clock management techniques could be applicable to a SerDes. *See, e.g.*, J. Patil et al., *Clock and Data Recovery for a 6 Gbps SerDes Receiver*, IEEE 3rd International Conference on Computer Science and Information Technology 217 (2010).

For example, for the Asserted Claims of the Asserted Patents, to the extent the references charted in any of Exhibits A-1 to C-16 do not disclose field programmable gate arrays (FPGAs) or FPGA systems, it would have been obvious to combine any of these charted references with any of the other charted references or those detailed in Appendices A–C, including, for example, Xilinx VCU118, Xilinx ZC706, Intel Cyclone 10 GX, Altera SyncE, or TI LMK05028. As evidenced by the references in these Invalidity Contentions, it was well known in the prior art to use FPGAs for fast processing of parallel data streams. *E.g.*, '286 patent at 1:31-36. As also evidenced by the references in these Invalidity Contentions, it was well known in the prior art to use a variety of methods to efficiently synchronize clocks across multiple processors or processing elements. *E.g.*, Shor, Bae, or Ballentyne. A person of skill in the art would be motivated to

combine these references because they disclose solutions in the same general field, namely techniques for improving processing speeds in electronic microprocessors. FPGAs, CPUs, GPUs, and application specific integrated circuits (ASICs) are all examples of different types of electronic microprocessors or computer processors. It is the nature of those of skill in the art of microprocessor development to attempt to increase the processing speed of the devices they are designing and to monitor developments in competing products, including other types of microprocessors and associated systems. A person of skill in the art would have been motivated to look at how other microprocessor systems increased processing speed, including by different types of parallel processing and different ways of managing the clock synchronization issues associated with parallel processing, and mimic those techniques. For example, it would have been obvious to a person of skill in the art to look at how other parallel processing systems avoid collisions and synchronize processing across different clock domains and apply those techniques to improve clock synchronization on FPGAs. As another example, it would have been obvious to a person of skill in the art to consider using an FPGA in place of or together with other microprocessors to improve parallel processing speeds for certain applications. *E.g.*, '286 patent at 1:31-37. These combinations would have also been obvious to try given that there were a finite number of identified, predictable solutions in the prior art, and there would have been a reasonable expectation of success to simply implement one prior art solution with concepts from prior art in the same field. Moreover, these combinations would have been the result of applying known techniques to a known method that was ready for improvement to yield predictable results.

For example, for the Asserted Claims of the Asserted Patents, to the extent the references charted in any of Exhibits A-1 to C-16 do not disclose applying the data processing methods to market or financial data, it would have been obvious to combine any of these charted references

with any of the other charted references or those detailed in Appendices A–C, including, for example, Lockwood, Starr, or Parsons. A person of skill in the art would be motivated to combine these references because they disclose high-speed computing and synchronization techniques directed to applications where precise timing is critical, including financial applications. It was well known before the priority dates that FPGAs and other high-speed hardware were widely used for financial and market applications because “FPGAs are used in the financial industry in high frequency trading where the rapid processing of the FPGA is desired.” ’286 patent at 1:34-36. It was also well known that financial and market applications were particularly sensitive to clock jitter and phase error because even sub-microsecond inaccuracies could materially affect trade execution, sequencing of market events, and financial outcomes: “[s]peed of information delivery is a valuable dimension to the financial instrument trading and brokerage industry.” Parsons at 1:49–50. It is the nature of those of skill in the art of high-performance and financial computing to monitor developments in related high-speed data systems and to combine relevant features to improve speed and timing accuracy. A person of skill would therefore have been motivated to look to known clock-alignment and jitter-reduction techniques and apply them to known FPGA-based market-data and trading architectures. These combinations would have also been obvious to try given that there were a finite number of identified, predictable solutions in the prior art, and there would have been a reasonable expectation of success to simply implement one prior art solution with concepts from prior art in the same field. Moreover, these combinations would have been the result of applying known techniques to a known method that was ready for improvement to yield predictable results.

To the extent HFT alleges that any other claimed limitation or limitations are not disclosed in any primary reference, it would have been obvious to combine the teachings of the reference

with the background knowledge of a person of ordinary skill in the art and/or it would have been obvious to incorporate the missing limitation(s), including as disclosed in Exhibits A-1 to C-16, into the primary reference for the reasons disclosed herein. Thus, one of ordinary skill in the art would have found substantial motivation to combine one or more of the primary references with one more of each other or the secondary references in order to disclose the alleged inventions recited in the Asserted Claims. Each of the references disclosed herein as invalidating an Asserted Patent was directed at the same or similar field of technology and the same or similar problem as that Asserted Patent. To the extent HFT alleges that any particular claim limitation is alleged to not be disclosed or inherent in the charted references, it would have been obvious to combine the charted reference with one or more of the references identified herein for the particular claim limitations. Also, as Optiver is currently unaware of the extent, if any, to which HFT will contend that limitations of the Asserted Claims are not disclosed in the art identified herein as anticipatory, Optiver reserves the right to identify other references and combinations that may render an allegedly missing limitation obvious. In addition, if and to the extent that HFT challenges the relevance of any of these references with respect to particular limitations of the Asserted Claims of the Asserted Patents, Optiver reserves the right to identify further motivation to combine particular references with additional particularity.

Primary Reference	In Combination with One or More of the Following References or with the Knowledge of One of Skill in the Art
Xilinx VCU118	• Xilinx ZC706 • Intel Cyclone 10 GX • Bittware XUPVV4 • XpressVUP • Altera SyncE • Mendes • Terasic DE5 • Texas Instruments LMK05028 • Snowden

Primary Reference	In Combination with One or More of the Following References or with the Knowledge of One of Skill in the Art
	• Shor • Perez • Bae • Ballantyne • Carvalho • Baxter • Starr • Lockwood • Taylor • Parsons • Hirning
Xilinx ZC706	• Xilinx VCU118 • Intel Cyclone 10 GX • Bittware XUPVV4 • XpressVUP • Altera SyncE • Mendes • Terasic DE5 • Texas Instruments LMK05028 • Snowdon • Shor • Perez • Bae • Ballantyne • Carvalho • Baxter • Starr • Lockwood • Taylor • Parsons • Hirning
Intel Cyclone 10 GX	• Xilinx VCU118 • Xilinx ZC706 • Bittware XUPVV4 • XpressVUP • Altera SyncE • Mendes • Terasic DE5 • Texas Instruments LMK05028 • Snowdon • Shor

Primary Reference	In Combination with One or More of the Following References or with the Knowledge of One of Skill in the Art
	• Perez • Bae • Ballantyne • Carvalho • Baxter • Starr • Lockwood • Taylor • Parsons • Hirning
Bittware XUPVV4	• Xilinx VCU118 • Xilinx ZC706 • Intel Cyclone 10 GX • XpressVUP • Altera SyncE • Mendes • Terasic DE5 • Texas Instruments LMK05028 • Snowdon • Shor • Perez • Bae • Ballantyne • Carvalho • Baxter • Starr • Lockwood • Taylor • Parsons • Hirning
XpressVUP	• Xilinx VCU118 • Xilinx ZC706 • Intel Cyclone 10 GX • Bittware XUPVV4 • Altera SyncE • Mendes • Terasic DE5 • Texas Instruments LMK05028 • Snowdon • Shor • Perez

Primary Reference	In Combination with One or More of the Following References or with the Knowledge of One of Skill in the Art
	• Bae • Ballantyne • Carvalho • Baxter • Starr • Lockwood • Taylor • Parsons • Hirning
Altera SyncE	• Xilinx VCU118 • Xilinx ZC706 • Intel Cyclone 10 GX • Bittware XUPVV4 • XpressVUP • Mendes • Terasic DE5 • Texas Instruments LMK05028 • Snowdon • Shor • Perez • Bae • Ballantyne • Carvalho • Baxter • Starr • Lockwood • Taylor • Parsons • Hirning
Mendes	• Xilinx VCU118 • Xilinx ZC706 • Intel Cyclone 10 GX • Bittware XUPVV4 • XpressVUP • Altera SyncE • Snowdon • Shor • Perez • Bae • Ballantyne • Carvalho

Primary Reference	In Combination with One or More of the Following References or with the Knowledge of One of Skill in the Art
	• Baxter • Starr • Lockwood • Taylor • Parsons • Hirning
Snowdon	• Xilinx VCU118 • Xilinx ZC706 • Intel Cyclone 10 GX • Bittware XUPVV4 • XpressVUP • Altera SyncE • Mendes • Shor • Perez • Bae • Ballantyne • Carvalho • Baxter • Starr • Lockwood • Taylor • Parsons • Hirning
Shor	• Xilinx VCU118 • Xilinx ZC706 • Intel Cyclone 10 GX • Bittware XUPVV4 • XpressVUP • Altera SyncE • Mendes • Terasic DE5 • Texas Instruments LMK05028 • Snowdon • Perez • Bae • Ballantyne • Carvalho • Baxter • Starr • Lockwood

Primary Reference	In Combination with One or More of the Following References or with the Knowledge of One of Skill in the Art
	• Taylor • Parsons • Hirning
Perez	• Xilinx VCU118 • Xilinx ZC706 • Intel Cyclone 10 GX • Bittware XUPVV4 • XpressVUP • Altera SyncE • Mendes • Terasic DE5 • Texas Instruments LMK05028 • Snowdon • Shor • Bae • Ballantyne • Carvalho • Baxter • Starr • Lockwood • Taylor • Parsons • Hirning
Bae	• Xilinx VCU118 • Xilinx ZC706 • Intel Cyclone 10 GX • Bittware XUPVV4 • XpressVUP • Altera SyncE • Mendes • Terasic DE5 • Texas Instruments LMK05028 • Snowdon • Shor • Perez • Ballantyne • Carvalho • Baxter • Starr • Lockwood • Taylor

Primary Reference	In Combination with One or More of the Following References or with the Knowledge of One of Skill in the Art
	• Parsons • Hirning
Ballantyne	• Xilinx VCU118 • Xilinx ZC706 • Intel Cyclone 10 GX • Bittware XUPVV4 • XpressVUP • Altera SyncE • Mendes • Terasic DE5 • Texas Instruments LMK05028 • Snowdon • Shor • Perez • Bae • Carvalho • Baxter • Starr • Lockwood • Taylor • Parsons • Hirning
Carvalho	• Xilinx VCU118 • Xilinx ZC706 • Intel Cyclone 10 GX • Bittware XUPVV4 • XpressVUP • Altera SyncE • Mendes • Terasic DE5 • Texas Instruments LMK05028 • Snowdon • Shor • Perez • Bae • Ballantyne • Baxter • Starr • Lockwood • Taylor • Parsons

Primary Reference	In Combination with One or More of the Following References or with the Knowledge of One of Skill in the Art
	• Hirning
Baxter	• Xilinx VCU118 • Xilinx ZC706 • Intel Cyclone 10 GX • Bittware XUPVV4 • XpressVUP • Altera SyncE • Mendes • Terasic DE5 • Texas Instruments LMK05028 • Snowdon • Shor • Perez • Bae • Ballantyne • Carvalho • Starr • Lockwood • Taylor • Parsons • Hirning
Terasic DE5	• Xilinx VCU118 • Xilinx ZC706 • Intel Cyclone 10 GX • Bittware XUPVV4 • XpressVUP • Altera SyncE • Mendes • Texas Instruments LMK05028 • Snowdon • Shor • Perez • Bae • Ballantyne • Carvalho • Baxter • Starr • Lockwood • Taylor • Parsons

Primary Reference	In Combination with One or More of the Following References or with the Knowledge of One of Skill in the Art
	• Hirning
Texas Instruments LMK05028	• Xilinx VCU118 • Xilinx ZC706 • Intel Cyclone 10 GX • Bittware XUPVV4 • XpressVUP • Altera SyncE • Mendes • Terasic DE5 • Snowdon • Shor • Perez • Bae • Ballantyne • Carvalho • Baxter • Starr • Lockwood • Taylor • Parsons • Hirning

III. INVALIDITY UNDER 35 U.S.C. § 112

Optiver further contends that, at least under HFT’s actual and/or apparent application of the claims, the claims are invalid based on inadequate written description and/or a lack of enablement under 35 U.S.C. § 112(a), and/or based on indefiniteness under 35 U.S.C. § 112(b).

Optiver reserves all rights to amend its Preliminary Invalidity Contentions under 35 U.S.C. § 112, including after the Asserted Claims are ultimately construed by the Court, in response to any interpretation of the Asserted Claims embodied in HFT’s infringement positions, to account for any changes in the law concerning invalidity under 35 U.S.C. § 112, and/or any other relevant subsequent case events, such as those discussed herein. Optiver also reserves the right to provide additional explanation and/or argument for its Preliminary Invalidity Contentions under Section

112, including, for example, based on expert testimony. Optiver’s investigation is ongoing, as is discovery in this action. Optiver accordingly may supplement these contentions to further identify bases for invalidity under 35 U.S.C. § 112 as any other additional information becomes available. Optiver’s contentions that the Asserted Claims are invalid under Section 112 are not admissions regarding the construction or scope of the claims of the Asserted Patents, or that any of the claims of the Asserted Patents are not anticipated or rendered obvious by any prior art. All of the below statements are by way of example only. Any item disclosed below with respect to any patent or claim may, as appropriate, be asserted as a defense against any other patent or claim that has a similar claim limitation and patent disclosure.

A. Invalidity Under 35 U.S.C. § 112(a)

35 U.S.C. § 112(a) requires that the specification contain a written description of the invention. “[T]he hallmark of written description is disclosure.” *Boston Sci. Corp. v. Johnson & Johnson*, 647 F.3d 1353, 1361–62 (Fed. Cir. 2011) (citation omitted). The test for whether a specification adequately describes an invention is “whether the disclosure of the application relied upon reasonably conveys to those skilled in the art that the inventor had possession of the claimed subject matter as of the filing date. . . . [T]he test requires an objective inquiry into the four corners of the specification from the perspective of a person of ordinary skill in the art [It] is a question of fact.” *Ariad Pharms., Inc. v. Eli Lilly and Co.*, 598 F.3d 1336, 1351 (Fed. Cir. 2010) (en banc); *Boston Scientific*, 647 F.3d at 1362.

The enablement requirement of Section 112 demands that the patent specification enable “those skilled in the art to make and use the full scope of the claimed invention without ‘undue experimentation.’” *Genentech, Inc. v. Novo Nordisk A/S*, 108 F.3d 1361, 1365 (Fed. Cir. 1997) (quoting *In re Wright*, 999 F.2d 1557, 1561 (Fed. Cir. 1993)). “[T]he scope of the claims must be less than or equal to the scope of the enablement.” *Nat’l Recovery Tech., Inc. v. Magnetic*

Separation Sys., Inc., 166 F.3d 1190, 1196 (Fed. Cir. 1999). In other words, the claims must be enabled over their entire claimed range. *See id.* (finding lack of enablement because the “claim [] [was] broader than the enablement as taught in the specification”).

Optiver contends that the following Asserted Claims are invalid under 35 U.S.C. § 112(a). Each Asserted Claim identified below (and each Asserted Claim that depends therefrom) is invalid under Section 112(a) because the specification of the respective Asserted Patent fails to provide a sufficient written description and/or enabling disclosure. For each listed term or phrase, Optiver believes the term or phrase is invalid under Section 112(a), as is any limitation including such terms or phrases, for the same reason(s).

Optiver further contends that HFT’s apparent claim constructions render the asserted claims extremely broad in scope and well beyond the purported inventions described in the Asserted Patents. Based on a review of HFT’s Preliminary Infringement Contentions, HFT is attempting to construe the Asserted Patents in an idiosyncratic manner that is entirely inconsistent with the written specifications and prosecution histories of the Asserted Patents as well as with the understanding of one of ordinary skill in the art at the time the applications that issued as the Asserted Patents were filed. These allegations are inconsistent with the plain language of the claims, the supporting description, and the prosecution history.

Additionally, the Asserted Claims do not meet the written description or enablement requirements of 35 U.S.C. § 112 for at least the reason that the patent specification does not provide support for the full scope of the claims to the extent HFT asserts that the claims are broad enough to cover the accused functionalities. *See LizardTech Inc. v. Earth Resource Mapping*, 424 F.3d 1336, 1345 (Fed. Cir. 2005). The patent specification as interpreted by HFT would not enable a person of ordinary skill in the art to practice the alleged invention without undue experimentation.

See LizardTech, 424 F.3d at 1345. Also, a person of ordinary skill in the art would not understand the named inventor to be in possession of the purported invention as interpreted by HFT. *See id.* Thus, the claims are invalid under 35 U.S.C. § 112(a) for lack of written description and lack of enablement. *See id.*; *Ariad Pharms.*, 598 F.3d at 1351-52.

Asserted Patent	Asserted Claim(s)	Term(s) and/or Phrase(s) Lacking Written Description and Enablement
'286 patent	1	the feedback clock signal having a third frequency and a third phase
'286 patent	1	generating, by the phase detector, the first output based on a comparison of the first receiver side clock signal and the feedback clock signal obtained from the second clock signal;
'286 patent	1	determining, by the phase controller, interim adjustment information based on the first output; and
'286 patent	1	wherein, the adjustable oscillator adjusts the second clock signal based on the interim adjustment information and steps (i) through (v) are repeated until the first output of the phase detector is below the first threshold level;
'286 patent	1	generating, by the serializer, a first transmitter side clock signal based on the second clock signal
'286 patent	2	wherein the second frequency corresponds to the first frequency.
'286 patent	4	The method of claim 1, wherein the second frequency is different from the first frequency.
'286 patent	6	wherein the third frequency corresponds to the second frequency.
'305 patent	1	said second reference clock pin is configured to receive a second clock signal having a second frequency and a second phase
'305 patent	1	the second reference clock pin to receive as a third input a first wire rate clock signal, based on the second clock signal, having a fourth frequency and a fourth phase

Asserted Patent	Asserted Claim(s)	Term(s) and/or Phrase(s) Lacking Written Description and Enablement
'305 patent	1	generate the first transmitter side clock signal, based on the first wire rate signal, having the fifth frequency and the fifth phase, wherein the fifth frequency is different than and less than the fourth frequency
'305 patent	1	compare the third phase of the receiver side clock signal to a sixth phase of a third clock signal having a sixth frequency
'305 patent	1	generate a phase difference indicator signal based on a difference between the third phase of the receiver side clock signal and the sixth phase of the third clock signal
'305 patent	1	determine adjustment information based on the phase difference indicator signal
'305 patent	1	generate the second clock signal including the second frequency and the second phase based on the adjustment information
'305 patent	1	wherein the third clock signal and the receiver side clock signal are phase aligned so that there is a fixed phase difference between the third phase and the sixth phase
'305 patent	2	wherein the fifth frequency corresponds to sixth frequency and the fifth phase third clock signal corresponds to the sixth phase.
'305 patent	3	wherein the second clock output pin is configured to transmit the third clock signal
'305 patent	3	wherein the fifth frequency corresponds to sixth frequency and the fifth phase third clock signal corresponds to the sixth phase
'305 patent	4	wherein the third frequency corresponds to the first frequency.
'305 patent	6	The system of claim 1, wherein the third frequency is different than the first frequency.
'305 patent	14	The system of claim 1, wherein the fourth frequency is equal to x times the fifth frequency, where x is the second amount of data streams.

Asserted Patent	Asserted Claim(s)	Term(s) and/or Phrase(s) Lacking Written Description and Enablement
'305 patent	15	The system of claim 1, wherein the fourth frequency is equal to x times the fifth frequency, where x is half of the second amount of data streams.
'305 patent	16	The system of claim 1, wherein the fourth frequency is a rational multiple of the second frequency.
'381 patent	1	generating, using the phase lock loop, a second clock signal
'381 patent	1	generating, within the field programmable gate array, a transmitter side clock signal derived from the second clock signal
'381 patent	8	generating, by the phase detector, the first output based on a comparison of the receiver side clock signal and the feedback clock signal obtained from the second clock signal;
'381 patent	8	determining, by the phase controller, interim adjustment information based on the first output
'381 patent	8	wherein, the adjustable oscillator adjusts the second clock signal based on the interim adjustment information,

B. Invalidity Under 35 U.S.C. § 112(b)

Claims are indefinite under 35 U.S.C. § 112(b) when they “fail to inform, with reasonable certainty, those skilled in the art about the scope of the invention.” *Nautilus, Inc. v. Biosig Instruments, Inc.*, 134 S. Ct. 2120, 2124 (2014). For example, to the extent an asserted apparatus claim includes both apparatus and method limitations, that claim is invalid for indefiniteness under Section 112(b) because it fails to identify or notify the public of what constitutes direct infringement. *See IPXL Holdings, L.L.C. v. Amazon.com, Inc.*, 430 F.3d 1377 (Fed. Cir. 2005). Similarly, a claim that uses means-plus function claiming is indefinite “[i]f the patentee fails to disclose adequate corresponding structure.” *Williamson v. Citrix Online, LLC*, 792 F.3d 1339, 1352 (Fed. Cir. 2015). A claim can also be found indefinite if it uses terms of degree. *See Interval*

Licensing LLC v. AOL, Inc., 766 F.3d 1364, 1371 (Fed. Cir. 2014). As the Federal Circuit has “explained, a term of degree fails to provide sufficient notice of its scope if it depends ‘on the unpredictable vagaries of any one person’s opinion.’” *Id.* (citation omitted). In addition, “a claim term that lacks an antecedent basis may . . . render a claim indefinite.” *In re Downing*, 754 F. App’x 988, 996 (Fed. Cir. 2018).

Optiver contends that the following Asserted Claims are invalid under Section 112(b). Each Asserted Claim identified below (and each Asserted Claim that depends therefrom) is invalid under Section 112(b) because they fail to inform, with reasonable certainty, those skilled in the art about the scope of the claimed invention. For each listed term or phrase, Optiver believes the term or phrase is invalid under Section 112(b), and any limitation including such term or phrase is also indefinite. Therefore, identification of a term or phrase below necessarily identifies any broad term/phrase or claim limitation in which the identified term or phrase appears.

Asserted Patent	Asserted Claim(s)	Term(s) and/or Phrase(s) That Are Indefinite
'286 patent	1	receiving, by a first plurality of data pins in a first interface of a field programmable gate array in the field programmable gate array system, the first serial data stream
'286 patent	1	transmitting, from the first plurality of data pins in the first interface to a deserializer in the field programmable gate array, the first serial data stream
'286 patent	1	generating, by the deserializer, a first receiver side clock signal having a second frequency and a second phase, based at least in part on the first clock signal
'286 patent	1	converting, by the deserializer, the first serial data stream into a first plurality of parallel data streams
'286 patent	1	transmitting, from the deserializer to the computational circuitry, the first plurality of data streams comprising a first plurality of data items and a first amount of data streams

Asserted Patent	Asserted Claim(s)	Term(s) and/or Phrase(s) That Are Indefinite
'286 patent	1	the feedback clock signal having a third frequency and a third phase
'286 patent	1	generating, using the field programmable gate array system, a feedback clock signal associated with a first transmitter side clock signal, the feedback clock signal having a third frequency and a third phase, by performing the following steps until a first output of the phase detector is below a first threshold level
'286 patent	1	generating, by the phase detector, the first output based on a comparison of the first receiver side clock signal and the feedback clock signal obtained from the second clock signal;
'286 patent	1	wherein, the adjustable oscillator adjusts the second clock signal based on the interim adjustment information and steps (i) through (v) are repeated until the first output of the phase detector is below the first threshold level;
'286 patent	1	generating, by the serializer, a first transmitter side clock signal based on the second clock signal
'286 patent	1	transmitting, from the serializer off the field gate programmable array system via a second plurality of data pins in the first interface, the second serial data stream
'286 patent	1	the computational circuitry
'286 patent	1	a first plurality of parallel data streams
'286 patent	1	the first plurality of data streams
'286 patent	1	the first transmitter side clock signal
'286 patent	1	the serializer
'286 patent	1, 3	operationally connected
'286 patent	2	wherein the second frequency corresponds to the first frequency.
'286 patent	4	The method of claim 1, wherein the second frequency is different from the first frequency.
'286 patent	6	wherein the third frequency corresponds to the second frequency.

Asserted Patent	Asserted Claim(s)	Term(s) and/or Phrase(s) That Are Indefinite
'286 patent	8	wherein a difference between the third phase and the second phase is less than a second threshold level
'286 patent	10	the first set of operations does not include clock domain crossing operations that delay processing of the first set of parallel data streams
'286 patent	10	the first set of parallel data streams
'286 patent	10	delay processing
'286 patent	19	the transmission of the second serial data stream from the serializer off the field programmable gate array is transmitted to an input/output module off the field programmable gate array
'305 patent	1	said second reference clock pin is configured to receive a second clock signal having a second frequency and a second phase
'305 patent	1	a first plurality of data pins, wherein said first plurality of data pins is configured to receive a first serial data stream
'305 patent	1	a second plurality of data pins, wherein said second plurality of data pins is configured to transmit a second serial data stream
'305 patent	1	the deserializer is configured to . . . generate a first receiver side clock signal based on the first clock signal, wherein the first receiver side clock signal has a third frequency and a third phase
'305 patent	1	convert the first serial data stream into a first plurality of parallel data streams having a first amount of data streams
'305 patent	1	the second reference clock pin to receive as a third input a first wire rate clock signal, based on the second clock signal, having a fourth frequency and a fourth phase
'305 patent	1	the serializer is configured to . . . generate the first transmitter side clock signal, based on the first wire rate signal, having the fifth frequency and the fifth phase, wherein the fifth frequency is different than and less than the fourth frequency

Asserted Patent	Asserted Claim(s)	Term(s) and/or Phrase(s) That Are Indefinite
'305 patent	1	a first plurality of parallel data streams
'305 patent	1	the first plurality of parallel data streams
'305 patent	1, 7	the first set of parallel data streams
'305 patent	1, 2, 3	sixth frequency
'305 patent	1, 2, 3	third clock signal
'305 patent	2	wherein the fifth frequency corresponds to sixth frequency and the fifth phase third clock signal corresponds to the sixth phase.
'305 patent	4	wherein the third frequency corresponds to the first frequency.
'305 patent	6	The system of claim 1, wherein the third frequency is different than the first frequency.
'305 patent	7	the first set of operations does not include clock domain crossing operations that delay processing the first set of parallel data streams
'305 patent	7	the first set of parallel data streams
'305 patent	7	delay processing
'305 patent	14	The system of claim 1, wherein the fourth frequency is equal to x times the fifth frequency, where x is the second amount of data streams.
'305 patent	15	The system of claim 1, wherein the fourth frequency is equal to x times the fifth frequency, where x is half of the second amount of data streams.
'305 patent	16	The system of claim 1, wherein the fourth frequency is a rational multiple of the second frequency.
'305 patent	20	the first operation
'381 patent	1	converting, by the deserializer, the first serial data stream into a first plurality of parallel data streams
'381 patent	1	generating, by the deserializer, a receiver side clock signal
'381 patent	1	generating, using the phase lock loop, a second clock signal

Asserted Patent	Asserted Claim(s)	Term(s) and/or Phrase(s) That Are Indefinite
'381 patent	1	generating, within the field programmable gate array, a transmitter side clock signal derived from the second clock signal
'381 patent	1	said method does not use clock domain crossing operations that delay processing of the first set of parallel data streams
'381 patent	1	transmitting, from the field programmable gate array system, the second serial data stream, derived from the second plurality of parallel data streams
'381 patent	1	performing, by the computational circuitry, a set of operations on at least a portion of the first plurality of parallel data streams to generate a second plurality of parallel data streams
'381 patent	1	the first set of parallel data streams
'381 patent	1	a first plurality of parallel data streams
'381 patent	1	the first plurality of data streams
'381 patent	1	delay processing
'381 patent	5	The method of claim 1, wherein at least a portion of the set of operations performed in step (h) are performed prior to step (g).
'381 patent	6	The method of claim 1, wherein at least a portion of the set of operations performed in step (h) are performed after step (g).
'381 patent	7	The method of claim 1, wherein all of the set of operations performed in step (h) are performed after step (g).
'381 patent	9, 10	the first plurality of data streams
'381 patent	9, 10	the second plurality of data streams

C. Improper New Matter

Optiver contends that some of the Asserted Claims violate the prohibition on new matter under AIA 35 U.S.C. § 132. *See also* 35 U.S.C. § 112(a). Section 132 provides that “[n]o amendment shall introduce new matter into the disclosure of the invention.” Although the

Asserted Patents purport to claim priority to the '804 Provisional, the applicant added disclosure in the Asserted Patents that is not supported in the '804 Provisional, and certain claims of the Asserted Patents purport to derive written description from the new matter. For example, the following claim limitations do not find support in the '804 Provisional:

Asserted Patent	Asserted Claim(s)	Term(s) and/or Phrase(s) Lacking Support in the '804 Provisional
'286 patent	21	receiving, from the adjustable oscillator at a transceiver phase lock loop via a second reference clock pin in the first interface, the second clock signal;
'286 patent	21	processing, by the transceiver phase lock loop, the received second clock signal;
'286 patent	21	providing, by the transceiver phase lock loop, the wire rate clock signal based on the processing of the received second clock signal; and
'286 patent	21	transmitting, by the transceiver phase lock loop, the wire rate clock signal to the serializer.

The amendment to the specification to include purported written description for these claims was a violation of the prohibition on new matter. As such, these claims do not have sufficient written description support in the specification as filed, and are therefore invalid. *See Tan v. Integrated Silicon Sols., Inc.*, No. C 07-06166 WHA, 2008 WL 2340217, at *2 (N.D. Cal. June 5, 2008) (“The written-description requirement and its corollary, the new-matter prohibition of 35 U.S.C. 132, both serve to ensure that the patent applicant was in full possession of the claimed subject matter at the time the original application was filed.”).

IV. INELIGIBILITY UNDER 35 U.S.C. § 101

The Asserted Claims of each of the patents-in-suit are not patent-eligible under 35 U.S.C. § 101. Optiver reserves all rights to amend its Preliminary Invalidity Contentions under Section 101, including after the Asserted Claims are ultimately construed by the Court, in response to any

interpretation of the Asserted Claims embodied in HFT’s infringement positions, and/or to account for any changes in the law concerning ineligibility under Section 101. Optiver also reserves the right to provide additional explanation and/or argument for its Preliminary Invalidity Contentions under Section 101, including, for example, based on expert testimony. In particular, the abstract ideas set forth below are exemplary and based on Optiver’s current understanding of the patents.

Subject to the reservation of rights above and based on Optiver’s present understanding of the Asserted Claims, and the apparent constructions Plaintiff is asserting based on its Supplemental Preliminary Infringement Contentions, each asserted claim is invalid at least because they are directed to subject matter that is not patent-eligible and thus fails to satisfy the requirements of 35 U.S.C. § 101. Optiver reserves the right to amend, clarify, change, or alter the below positions and contentions regarding invalidity for lack of patentable subject matter.

Pursuant to the OGP, Optiver identifies the following abstract ideas in the asserted claims:

- **U.S. Patent No. 10,931,286**, all asserted claims: synchronizing data processing with a clock.
- **U.S. Patent No. 11,128,305**, all asserted claims: synchronizing data processing with a clock.
- **U.S. Patent No. 11,575,381**, all asserted claims: synchronizing data processing with a clock.

Courts have recognized that similar claims are directed to abstract ideas.⁶ Pursuant to the OGP, Optiver alleges that each element of each asserted claim is well-understood, routine, and/or conventional.

⁶ *Elec. Power Grp., LLC v. Alstom S.A.*, 830 F.3d 1350, 1353 (Fed. Cir. 2016) (“Information as such is an intangible . . . [a]ccordingly, we have treated collecting information, including when limited to particular content (which does not change its character as information), as within the realm of abstract ideas.”); *Affinity Labs of Texas, LLC v. DIRECTV, LLC*, 838 F.3d 1253, 1261 (Fed. Cir. 2016) (“the conveyance and manipulation of information using wireless communication

V. ACCOMPANYING DOCUMENT PRODUCTION

Optiver is producing invalidating prior art references and corroborating evidence concerning prior art systems, including the prior art references described in this document and the attached exhibits, in production volume Optiver VOL 001. These prior art references and corroborating evidence are cited in and support the provided invalidity claim charts. Optiver reserves the right to supplement its corresponding document production should it later find additional, responsive documents.

Additionally, pursuant to the OGP and the Court's Scheduling Order (Dkt. 24), Optiver has produced technical documents sufficient to show the operation of the accused products. In addition, Optiver will make certain highly sensitive material available for inspection after the Parties reach agreement on the appropriate protective measures for such material.

and computer technology" is an abstract idea); *Glasswall Solutions Ltd. v. Clearswift Ltd.*, 754 F. App'x 996, 998 (Fed. Cir. 2018) ("The claims merely require the conventional manipulation of information by a computer. We have often held similar conventional data manipulation to be abstract."); *iLife Techs., Inc. v. Nintendo of Am., Inc.*, 839 F. App'x 534, 536 (Fed. Cir. 2021) ("We have routinely held that claims directed to gathering and processing data are directed to an abstract idea."); *Intellectual Ventures I LLC v. Capital One Fin. Corp.*, 850 F.3d 1332, 1340 (Fed. Cir. 2017) ("We have held other patent claims ineligible under § 101 for reciting similar data manipulation steps."); *SAP Am., Inc. v. InvestPic, LLC*, 898 F.3d 1161, 1167 (Fed. Cir. 2018) ("The focus of the claims . . . is on selecting certain information, analyzing it using mathematical techniques, and reporting or displaying the results of the analysis. That is all abstract."); *Beteiro, LLC v. DraftKings Inc.*, 104 F.4th 1350, 1355-56 (Fed. Cir. 2024) (finding ineligible claims directed to "detecting information, generating and transmitting a notification based on the information, . . . , and processing information"); *Dropbox, Inc. v. Synchronoss Techs., Inc.*, 815 F. App'x 529, 536 (Fed. Cir. 2020) (finding ineligible claims related to data synchronization); *Gottschalk v. Benson*, 409 U.S. 63, 65-73 (1972) (method of "converting signals" using mathematical operations is not patent eligible).

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Respectfully submitted,

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CERTIFICATE OF SERVICE

I hereby certify that on February 4, 2026, the foregoing was served upon all counsel of record who have consented to electronic service.

/s/ Max Stewart

Max Stewart