

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

CITADEL SECURITIES LLC,

Petitioner

v.

HFT SOLUTIONS, LLC,

Patent Owner

Case No. IPR2026-00212

Patent No. 10,931,286

PATENT OWNER'S PRELIMINARY RESPONSE

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35 U.S.C. § 312(a)(3)	20
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PATENT OWNER’S EXHIBIT LIST

No.	Description
Ex. 2001	<i>HFT Solutions, LLC v. Jump Trading LLC</i> , 1:24-cv-13214, Dkt. 30-1 (N.D. Ill.) - Agreed Schedule
Ex. 2002	<i>HFT Solutions, LLC v Optiver US LLC et al</i> , Case No. 7:25-cv-00415, Dkt. 24 (W.D. Tex.) - Scheduling Order
Ex. 2003	<i>HFT Solutions, LLC v. Citadel Securities LLC</i> , 1:24-cv-13214, Dkt. 30 (N.D. Ill.) – Motion to Dismiss
Ex. 2004	<i>HFT Solutions, LLC v. Citadel Securities LLC</i> , 1:24-cv-13214, Dkt. 57 (N.D. Ill.) – Order Denying Motion to Dismiss
Ex. 2005	<i>HFT Solutions, LLC v. Citadel Securities LLC</i> , 1:24-cv-13214 (N.D. Ill.) – Final Invalidity Contentions
Ex. 2006	<i>HFT Solutions, LLC v. Citadel Securities LLC</i> , 1:24-cv-13214, Dkt. 64 (N.D. Ill.) – Agreed Schedule
Ex. 2007	<i>HFT Solutions, LLC v. Citadel Securities LLC</i> , 1:24-cv-13214 (N.D. Ill.) – Final Invalidity Contentions Exhibit B-1
Ex. 2008	<i>HFT Solutions, LLC v. Citadel Securities LLC</i> , 1:24-cv-13214, Dkt. 63 (N.D. Ill.) – Citadel Securities Answer, Affirmative Defenses, and Counterclaims
Ex. 2009	U.S. Patent No.
Ex. 2010	Email title “HFT v. Citadel – deadlines” from Meg Fasulo to Dale Chang dated May 2, 2025
Ex. 2011	<i>HFT Solutions, LLC v. Citadel Securities LLC</i> , 1:24-cv-13214, Dkt. 49 (N.D. Ill.) – Unopposed Motion to Request A Status Conference
Ex. 2012	<i>HFT Solutions, LLC v Optiver US LLC et al</i> , Case No. 7:25-cv-00415 – Preliminary Invalidity Contentions
Ex. 2013	<i>HFT Solutions, LLC v. Citadel Securities LLC</i> , 1:24-cv-13214, Dkt. 1 (N.D. Ill.) – Complaint
Ex. 2014	A-UL3422-p16G-PQ-G Avnet Listing found at https://www.avnet.com/americas/product/amd/a-ul3422-p16g-pq-g/evolve-116907021/

No.	Description
Ex. 2015	A-MA35D-P16G-PQ-G Mouser Listing found at https://www.mouser.com/ProductDetail/AMD-Xilinx/A-MA35D-P16G-PQ-G?qs=amGC7iS6iy%252BuPYexH3EZzg%3D%3D
Ex. 2016	BittWare XUP-VV8 Datasheet
Ex. 2017	AMD Alveo UL3524 Accelerator Card Datasheet
Ex. 2018	AMD Alveo UL 3422 FPGA Accelerator Card Datasheet
Ex. 2019	Zynq UltraScale+ MP SOC Family Avnet Listing found at https://www.avnet.com/americas/product/amd/xczu2cg-1sbva484i/evolve-13010752/
Ex. 2020	Citadel Securities LLC 2024 Financial Statement
Ex. 2021	Declaration of Dale Chang In Support of Patent Owner's Preliminary Response
Ex. 2022	Internet Archive Redirect Failure from Website Identified in Ex. 1009

I. INTRODUCTION

The present Petition fails to establish a reasonable likelihood of success on the merits for numerous reasons. First and as a threshold matter, the Petition fails to establish that either Altera or Lockwood qualifies as prior art. Second, the Petition fails to show that Altera teaches using computational circuitry with the parallel data streams to perform any set of operations as claimed. Third, the Petition fails to demonstrate “data items” or “amount of data streams” are anticipated, inherent, or obvious.

Any one of these failures shows the Petition cannot succeed and justifies denial of institution. Together, they make it clear there is no likelihood of success on the merits. Because the Petition does not present any grounds that can be instituted, much less any that present a reasonable likelihood of success, institution should be denied.

II. BACKGROUND

A. Citadel’s Petition

Petitioner Citadel Securities LLC (“Citadel” or “Petitioner”) challenges claims 1, 2, 8, 10-11 and 19-20 of U.S. Patent No. 10,931,286 (the “’286 Patent”).

Petitioner structures its asserted grounds for unpatentability as follows:

- Ground 1: Altera Anticipates Claims 1, 2, 8, 10-11, and 19

- Ground 1A: Altera in view of Stratix Handbook and SI5345 Manual Render Obvious Claims 1, 2, 8, 10-11, and 19
- Ground 2: Altera and Lockwood Render Obvious Claims 1, 2, 8, 10-11, and 19-20

Because all challenged dependent claims across all grounds depend from claim 1, this Preliminary Response need only address the Petition's arguments concerning claim 1. If the Petition does not show a reasonable likelihood of prevailing on claim 1, then it cannot prevail on any other challenged claim.

B. Overview of the '286 Patent

At a high level, the '286 Patent is directed to addressing a need for phase control to minimize latency in high-speed FPGA systems. Ex. 1001 at 1:36-39, Abstract. Latency reduction is important "in the financial industry in high frequency trading where the rapid processing of the FPGA is desired." *Id.* at 1:35-36. Contrary to the prior art method of using a clock domain crossing circuit to synchronize clock signals, which adds delay, the invention teaches a technique that avoids clock domain crossings. *Id.* at 1:39-45

In particular, the '286 Patent teaches utilizing an external phase-locked loop to avoid the need for clock domain crossing circuits. *Id.* 1:23-27. This solution is reflected, for example, in claim 1 of the '286 Patent, which recites:

1. 1. A method for processing a first serial data stream comprising market data, using a field programmable gate array system, to generate

a second serial data stream comprising order entry data, wherein the method comprises the steps of:

- a) receiving, by a first plurality of data pins in a first interface of a field programmable gate array in the field programmable gate array system, the first serial data stream;
- b) receiving, by a first reference clock pin in the first interface, a first clock signal having a first frequency and a first phase;
- c) transmitting, from the first plurality of data pins in the first interface to a deserializer in the field programmable gate array, the first serial data stream;
- d) providing, from the first reference clock pin in the first interface to the deserializer, a clock signal based at least on the first clock signal;
- e) generating, by the deserializer, a first receiver side clock signal having a second frequency and a second phase, based at least in part on the first clock signal;
- f) converting, by the deserializer, the first serial data stream into a first plurality of parallel data streams;
- g) transmitting, from the deserializer to the computational circuitry, the first plurality of data streams comprising a first plurality of data items and a first amount of data streams;
- h) transmitting, via a first clock output pin on a second interface of the field programmable gate array to a phase detector that is part of the field programmable gate array system and not part of the field programmable gate array, the first receiver side clock signal;
- i) generating, using the field programmable gate array system, a feedback clock signal associated with a first transmitter side clock signal, the feedback clock signal having a third frequency and a third

phase, by performing the following steps until a first output of the phase detector is below a first threshold level:

- i. generating, by an adjustable oscillator in the field programmable gate array system, a second clock signal having a fourth frequency and a fourth phase;
 - ii. generating, by the phase detector, the first output based on a comparison of the first receiver side clock signal and the feedback clock signal obtained from the second clock signal;
 - iii. transmitting, from the phase detector to a phase controller of the field programmable gate array system which is not in the field programmable gate array, the first output;
 - iv. determining, by the phase controller, interim adjustment information based on the first output; and
 - v. transmitting, from the phase controller to the adjustable oscillator, the interim adjustment information;
- wherein, the adjustable oscillator adjusts the second clock signal based on the interim adjustment information and steps (i) through (v) are repeated until the first output of the phase detector is below the first threshold level;
- j) generating, by the serializer, a first transmitter side clock signal based on the second clock signal; and
 - k) transmitting, by the serializer to the computational circuitry, the first transmitter side clock signal;
 - l) performing, by the computational circuitry, a first set of operations on at least a portion of the first plurality of data items to generate a second plurality of parallel data streams comprising a second amount of data streams;

- m) transmitting, from the computational circuitry to the serializer, the second plurality of parallel data streams;
- n) converting, by the serializer, the second plurality of parallel data streams into the second serial data stream; and
- o) transmitting, from the serializer off the field gate programmable array system via a second plurality of data pins in the first interface, the second serial data stream.

Ex. 1001 at claim 1.

All other challenged claims (2, 8, 10-11 and 19-20) depend from claim 1.

III. LEVEL OF ORDINARY SKILL IN THE ART

The Petition proposes that a person of ordinary skill in the art in the field of the '286 Patent “would have a bachelor’s degree in electrical or computer engineering and 3-5 years of academic or industry experience working with clocking techniques for FPGAs with high-speed transceivers.” Paper 1 (“Petition” or “Pet.”) at 23-24. For purposes of this preliminary response, Patent Owner does not challenge that definition.

IV. THE PETITION DOES NOT DEMONSTRATE A LIKELIHOOD OF SUCCESS ON THE MERITS

The Petition fails on multiple independent counts. First, the Petition fails to make the threshold showing that either Altera or Lockwood are prior art. Second, the Petition fails to show performing a set of operations using computational circuitry is taught by, inherent to, or obvious in light of Altera whether in

combination with Stratix or Lockwood. Finally, Citadel fails to demonstrate the claimed “data items” or “amount of data streams” are anticipated, inherent, or obvious.

A. The Asserted Grounds Are Not Based On Prior Art

Before addressing the technical shortcomings of the Petition, Citadel fails even to establish that either Altera or Lockwood is prior art. Neither reference is a patent or patent application, as such the Petition must show that they were publicly available, i.e., that each reference was “disseminated or otherwise made available to the extent that persons interested and ordinarily skilled in the subject matter or art exercising reasonable diligence, can locate it.” *Kyocera Wireless Corp. v. Int'l Trade Comm'n*, 545 F.3d 1340, 1350 (Fed.Cir.2008). “[T]he burden is on the petitioner to identify with particularity evidence sufficient to establish a reasonable likelihood that the reference was publicly accessible before the critical date of the challenged patent, and therefore that there is a reasonable likelihood that it qualifies as a printed publication.” *Hulu, LLC v. Sound View Innovations, LLC*, IPR2018-01039, Paper 29 at 16 (PTAB Dec. 20, 2019) (precedential). Here, the Petition fails to meet this burden as to Altera or Lockwood.

The Petition does not show Altera to have been available “long before November 2018” as it claims. Neither of the two pieces of evidence raised by the Petition, the white paper itself and a declaration by the internet archive, establish

when or even if Altera was ever publicly available. Without showing Altera was publicly available before November 2018, neither of the Petition's two grounds have a reasonable likelihood of success and institution should be denied.

The Petition first contends that the date on the face of Altera, November 2015, suggests it was publicly available by that date. Pet. at 9-11. However, such a position has been repeatedly rejected as not actually showing when a document was distributed. *See e.g. Navico Inc. v. Garmin Int'l, Inc.*, No. 216CV00190JRGRSP, 2017 WL 3750252, at *3 (E.D. Tex. July 28, 2017), *report and recommendation adopted*, No. 216CV00190JRGRSP, 2017 WL 3764213 (E.D. Tex. Aug. 29, 2017) (copyright and revision dates insufficient to show date of distribution); *Finjan, Inc. v. Sophos, Inc.*, No. 14-CV-01197-WHO, 2016 WL 2988834, at *26 (N.D. Cal. May 24, 2016) (copyright date and screen shot from decades later showing "Published/distributed" in 1995 insufficient to show date of distribution); *ServiceNow, Inc. v. Hewlett-Packard Co.*, Case IPR2015- 00716, slip op. at 17 (Paper 13) (PTAB Aug. 26, 2015) (finding a copyright notice unreliable hearsay for purposes of establishing the date of a printed publication). Moreover, looking at Altera itself, there is no statement that the November 2015 relates to publication or other distribution. *See* Ex. 1004. Rather, "November 2015" is found at the bottom of every page with no context and then at the end of the document as part of the "Document Revision History." *See id.* A date lacking context, as at the bottom of each page,

certainly does not suggest public dissemination much less the kind of public dissemination to the interested public that is required. Indeed, this date could represent the date of authorship or the date of internal circulation or any number of other relevant dates than public dissemination. Likewise, a “Document Revision History” is just that, a history of revision, not a history of dissemination or publication.

Further and contrary to the Petition, Altera is entirely different in nature to those characteristics relied upon by *Weber, Inc. v. Provisur Techs., Inc.*, 92 F.4th 1059, 1067 (Fed. Cir. 2024). Altera is not an operating manual and is not clearly “created for dissemination to the interested public to provide instructions about how to assemble, use, clean, and maintain” a product. *See id.* Rather, Altera merely describes a potential functionality, one that the Petition makes no effort to show was ever sold or used by anyone. *See* Ex. 1004 at 1 (“This paper describes a multiple-port 1G/10Gbps Ethernet SyncE synchronization solution....”). Rather, the portion cited by the Petition urging action by customers is part of a copyright notice with nothing to do with the actual substance of Altera. *Id.* By contrast, in *Weber* public accessibility was shown by testimony corroborated by delivery notes, invoices, price lists, declarations, and emails exchanged with customers. *Weber*, 92 F.4th at 1068. This showed both when and to whom distribution was made. Neither is present here.

Here, the only corroboration offered by the Petition is an Internet Archive declaration for a website, not Altera itself, where Altera is *not* available. The Petition contends Ex. 1009 shows “that the Altera White Paper was available online no later than October 18, 2016.” Pet. at 11. But examining Ex. 1009 does nothing to demonstrate the website shown was indexed, accessible, or well known to the community interested in the subject matter of Altera and moreover does not even show the Altera cited was ever available at the website.

First, and as noted above, to be publicly accessible “persons interested and ordinarily skilled in the subject matter or art exercising reasonable diligence” must be able to locate the reference. *See Kyocera*, 545 F.3d at 1350. Here, even if Ex. 1009 showed a website offering Altera for download (as explained below, it does not) it does not show that website was known or findable to the community interested in the subject matter of the reference. Indeed, the Affidavit of Mina Ching provides only how the Internet Archive and the Wayback Machine operate and does not even nominally authenticate Altera. Ex. 1009 at 1. Notably, it provides no suggestion that the underlying website was indexed or that an interested member of the public would or even could find the website shown in Ex. 1009. Neither does Dr. Stanton’s declaration. All Dr. Stanton provides is that “Altera and Silicon Labs made specifications and data sheets available for download from their respective websites...,” Ex. 1002 at ¶118, not that the website was accessible via an internet

search or otherwise known by the interested public. Addressing a similar situation and a similar Internet Archive affidavit, the Board found reliance on the Internet Archive to show a reference was publicly available failed. *See First Solar, Inc. v. Rovshan Sade*, IPR2023-00827, Paper 13 at 18 (PTAB Nov. 16, 2023) (explaining the Internet Archive affidavit “only indicates that the Wayback Machine is searchable ‘by URL,’” same as Ex. 1009, and “not by a query of a search engine before the critical date”). The Petition and Ex. 1009 fail to show Altera was publicly accessible given they do not show the underlying website could be found or was otherwise known.

Second, the website shown in Ex. 1009 does not allow access or download of the relevant entry. Visiting the cited Internet Archive website and attempting to select the relevant entry returns an error. Ex. 2021, Ex. 2022 (showing the error resulting from following the link in the Ex. 1009 website). As far as Ex. 1009 shows, the relevant entry could have led to a different document or indeed have been broken from the beginning and never allowed an interested member of the public to access Altera. As such there is no evidence in the Petition that the listing in Ex. 1009 refers to the same document as Ex. 1004. Indeed, the Board addressed such a situation where the included Internet Archive affidavit was directed to a ***different document of the same name*** as the reference used throughout the petition and denied institution. *See First Solar, Inc. v. Rovshan Sade*, IPR2023-00827, Paper 13 at 24 (PTAB Nov.

16, 2023). Given Ex. 1009 does not even show Ex. 1004, much less when or if it was available, it does nothing to corroborate any date for Altera.

Similarly, the Petition fails to show Lockwood was publicly available prior to the critical date. Rather, the Petition merely points to a current website, not even an exhibit, to suggest when Lockwood was published. *See* Pet. at 20. This is improper, because the website only demonstrates Lockwood is **now** available, not that it was available prior to the critical date. Rather, the date provided on Lockwood itself and the cited website are hearsay. *See e.g. ServiceNow, Inc. v. Hewlett-Packard Co.*, Case IPR2015- 00716, slip op. at 17 (PTAB Aug. 26, 2015) (Paper 13) (finding a copyright notice unreliable hearsay for purposes of establishing the date of a printed publication). With no evidence of distribution such as an archived version of an indexed website, the Petition cannot meet its burden to show Lockwood is prior art. As the Petition and its expert declaration offer no other support for the proposed date of Lockwood, the Petition fails to demonstrate Lockwood is prior art to the '286 Patent.

Because the Petition has not established that Altera is prior art, Grounds 1, 1A, and 2 do not demonstrate any likelihood of success on the merits. Similarly, because the Petition has not established that Lockwood is prior art, Ground 2 fails. As none of the asserted grounds rely on prior art, institution should be denied.¹

¹ Should the Director find that these issues can or should be addressed through

B. The Petition Fails to Show Limitation 1(l) Is Either Disclosed or Obvious

Here, the Petition attributes much to its seven-page primary reference which is never actually disclosed. Limitation 1(l) requires “performing, by the computational circuitry, a first set of operations on at least a portion of the first plurality of data items to generate a second plurality of parallel data streams comprising a second amount of data streams.” But the Petitioner must draw “computational circuitry” onto Altera and presume it performs the claimed set of operations. Pet. at 64-66; *see also id.* at 46-47. Without showing limitation 1(l) is met, the Petition cannot show any claim is invalid and institution should be denied. However, as explained below, the Petition fails to show that this limitation is disclosed either expressly or inherently, and additionally fails to set forth any theory of obviousness.

1. The Petition fails to show Altera discloses limitation 1(l).

Altera does not explicitly disclose this limitation. For example, Altera itself does not show *any* computational circuitry is used to analyze the serial data stream or related data items. Indeed, the only alleged mention in Altera of anything the Petition alleges is “computational circuitry” is a single reference to the “FPGA core”

further discovery after institution, Patent Owner urges discretionary denial because the dispute would be far better suited for evaluation by a district court given the fact-intensive nature dependent on witness testimony, as explained in Patent Owner’s Request for Discretionary Denial. Paper 10 at 7-8.

that is only provided as a noisemaker, not performing operations on any data. *See* Ex. 1004 at 3 (“The FPGA core is filled with instances of a digital noise-maker design to create a real-world scenario for measuring the clock parameters.”). The Petition concedes as much when it adds the computational circuitry into the data stream shown in Figure 1. Pet. at 46-47. Without the computational circuitry being expressly present in this data stream and performing the claimed set of operations, Altera does not expressly disclose limitation 1(l).

Because Altera does not *expressly* disclose limitation 1(l), the Petition must show that Altera either inherently discloses the limitation or renders it obvious. The Petition fails on both counts, as explained below and in the following section.

To establish inherency, the Petition “must show that *the natural result flowing* from the operation as taught would result in the performance of the questioned function.” *PersonalWeb Techs., LLC v. Apple, Inc.*, 917 F.3d 1376, 1382 (Fed. Cir. 2019) (emphasis original; internal citations and quotations omitted). The Petition does not even attempt to show performing operations on any data items of parallel data streams is inherent to Altera. While the Stratix FPGA used in Altera includes computational circuitry, the Petition makes no effort to show it would be “the natural result flowing from the operation” of Altera to use it in any way on the claimed data stream, much less in the specific manner recited by the challenged claims. Indeed, Stratix only provides computational circuitry *can* be configured to perform

operations, the only such operation that is actually disclosed by Altera being a noise-making operation. *See* Ex. 1005 at 256, Ex. 1004 at 3. But *can* is insufficient. *Par Pharm., Inc. v. TWI Pharms., Inc.*, 773 F.3d 1186, 1195 (Fed. Cir. 2014) (“Inherency, however, may not be established by probabilities or possibilities.”).

The Petition does imply that the limitation is inherent. Pet. at 65 (“any useful application of an FPGA that uses the transceivers (the RX and TX blocks) *must* also use the computational circuitry.” (emphasis added)). However, the Petition offers no explanation, not even a citation, for why this *must* be the case. Instead, the Petition notes Altera mentions “voice, data, and video” applications, but it cannot tie that disclosure to any use of computational circuitry much less any set of operations. *See* Pet. at 65. Indeed, Altera does not teach hosting any such operations on the FPGA, instead Altera merely mentions “[e]thernet networks can be used to transport voice, data, and video.” Ex. 1004 at 1. Neither Altera nor the Petition demonstrate transporting such data requires the performance of any functions, much less that it must be on the claimed computational circuitry. Likewise, while the Petition cites Ex. 1013 mentioning Ethernet and application logic needed for its implementation, there is no attempt to show this makes anything in Altera inherent.

2. The Petition fails to show Altera renders obvious limitation 1(l).

The Petition also fails to show limitation 1(l) is obvious under either ground. First, under Ground 1, at best the Petition contends it would be obvious that “in order

to use the FPGA-based solution of Altera, the parallel data streams received from the deserializer must go through the computational circuitry and undergo operations.” Pet. at 45 (citing Ex. 1002 at ¶183 and Ex. 1013 at 2). However, this assertion is based on the incorrect understanding of Petitioner’s expert Dr. Stanton that because Altera “was used for ‘voice, data, and video’ applications,” “computational circuitry performs operations ... that such computational circuitry constructs, modifies, or triggers transmission of zero, one, or more packet(s) through each of one or more parallel interface(s) to the associated serializer(s) as a consequence.” Ex. 1002 at ¶183. However, Altera’s FPGA (i.e., the alleged “computational circuitry”) was *not* used for voice, data, and video applications; instead, Altera discloses only that ethernet may *transport* such data, not operate any application. Ex. 1004 at 1.

In addition to the Petition’s obviousness argument being based on the false premise that Altera was used for voice, data, and video applications, neither the Petition nor Dr. Stanton explain why such applications would even potentially require the computational circuitry, as opposed to other circuitry whether on or off the FPGA, to perform any particular operations. Altera already explains what the FPGA core does, it is *filled* with noise makers, not voice, data, or video applications. Ex. 1004 at 3. As to Ex. 1013, it is not part of any ground. Moreover, it offers a completely different approach to Ex. 1004.² While both white papers show very similar figure

² Patent Owner refers to Altera here as Ex. 1004 to avoid confusion as Ex. 1013 is

1's, where Ex. 1004 explains "Figure 1 illustrates ... multiple 1G/10Gb Ethernet media access control (MAC) and physical coding sublayer (PCS) and physical medium attachment (PMA) (PHY) intellectual property (IP) instances," Ex. 1013 provides "the programmable logic ... includes one or more Ethernet cores" and these Ethernet cores contain the MAC and PCS. *See* Ex. 1004 at 2; Ex. 1013 at 2. Because Ex. 1013 uses computational circuitry to perform operations that Ex. 1004 has different components to perform, a POSITA would not have looked to Ex. 1013 for any suggestion that using computational in Ex. 1004 would be obvious. As such, Ex. 1013 says nothing as to what is obvious in a completely different system.

Ground 2 is no better. Again, the Petition contends using the computational circuitry to perform operations as claimed would be obvious by pointing to Ex. 1013 as well as Ex. 1016. Pet. at 87-88. But as explained above, because Ex. 1013 describes a completely different solution as to the computational circuitry, it is irrelevant and it would be illogical to implement its teachings on Ex. 1004. Ex. 1016 only offers a generalized description of an FPGA's capability and makes no suggestion that those capabilities would be useful in Ex. 1004 or Lockwood. *See* Pet. at 87-88 (citing Ex. 1016 with no analysis).

likewise an Altera white paper that could logically also be given the Altera shorthand.

Likewise, Lockwood does not suggest modifying Altera to perform limitation 1(l). To the extent Lockwood suggests performing operations (i.e., trading algorithms), a POSITA would not seek to perform time-sensitive operations on the FPGA taught by Altera. As explained below, Altera is not a low latency solution, Altera is not compatible with Lockwood, and Lockwood suggests other tools, nearly teaching away from Altera.

First, the Petition recognizes that Lockwood requires a low latency FPGA, but never actually shows this is consistent with the FPGA disclosed in Altera. Altera having “high reliability” or being “high performance” is not equivalent to low latency. *See* Pet. at 80. Rather, “reliability” relates to synchronizing a frequency across an ethernet network. Ex. 1004 at 2 (reliability “is essential for telecommunications data transmission”). Likewise, “performance” here is directly tied with this same “frequency synchronization.” *Id.* at 6 (the white paper demonstrates “a high-performance and flexible solution for frequency synchronization of telecom and data communication networks...”). Neither has anything to do with speed or low latency. Indeed, Stratix shows significant latency when using the FPGA for ethernet. Ex. 1005 at 230 (showing a latency of 23 to 46 additional clock cycles for the 10G Ethernet configuration used by Altera in comparison to lower latencies available for other configurations).

Second, Altera is not compatible with Lockwood. Lockwood's repeated mention of "Smart NICs" as a possible implementation does not suggest Altera. Indeed, Altera is never referred to as a "Smart NIC." Altera lacks key functionality, notably a PCIe host interface is never mentioned in Altera, nor any suggestion one could be implemented with the functionality taught by Altera. *See* Ex. 1004; *see also* Pet. at 79-83, Ex. 1002 at ¶¶213-219 (never considering if Altera would be considered a Smart NIC or that Altera could implement Lockwood's PCIE). Indeed, Lockwood relies on this interface and the computational circuitry that Altera provides is "filled with instances of a digital noise-maker design" in its proposed trading set up. *See* Ex. 1007 at Fig. 3.

Third, Lockwood explicitly identifies available smart NICs a POSITA can use, with no mention of Altera, Stratix, or even any synchronous ethernet products. *See id.* at Table I. Rather, Lockwood focuses on specifically low latency ethernet NICs and stated a preference for non-ethernet networking. *See id.* at II. A ("Infiniband-based networking can reduce latency significantly compared to Ethernet.") Accordingly, a POSITA would have believed Altera to be incompatible with Lockwood's trading algorithm and would have never considered Altera to implement Lockwood.

Lastly and in addition to all of the above, the Petition offers no analysis as to "to generate a second plurality of parallel data streams" at all. Instead, all of the

Petition's analysis is directed to adding computational circuitry and a set of operations without even nominally addressing the generation of the second plurality of parallel data streams. *See* Pet. at 64-66. Even assuming “computational circuitry [that] constructs, modifies, or triggers transmission of zero, one, or more packet(s)” neither the Petition nor Dr. Stanton offer an explanation that this generates a second plurality rather than simply retransmitting the first plurality or the like. *See* Ex. 1002 at ¶183; *see also* Pet. at 65-66. Likewise, as to Ground 2, the Petition fails to even identify what it contends would be the “second plurality of parallel data streams.” *See* Pet. at 87-88.

Because neither Ground 1 nor Ground 2 demonstrate Limitation 1(l) is disclosed or obvious, institution should be denied.

C. The Petition Likewise Fails to Show Any Claimed “Data Items” or “Amount of Data Streams”

In addition to failing to show the claimed computational circuitry or set of operations, the Petition fails to show that Altera uses “data items” and to set forth a rational explanation for the claimed “amount of data streams.” Instead, the Petition points to a hardware functionality without any suggestion Altera uses that functionality or even could and points to multiple sets of parallel data streams rather than anything comprising those data streams. Pet. at 49. This does not meet the Petitioner's burden to show limitation 1(g) is disclosed or obvious.

Rather, a Petitioner must explain *with particularity* how the prior art would have rendered the challenged claims unpatentable. 35 U.S.C. § 312(a)(3); 37 CFR § 42.104(b)(4) (“The petition must specify where each element of the claim is found in the prior art patents or printed publications relied upon.”). “The IPR petition, thus, must provide an understandable explanation of the element-by-element specifics of the patentability challenges, including the identification of particular portions of prior art on which the petitioner is relying.” *Corephotonics, Ltd. v. Apple Inc.*, 84 F.4th 990, 1001 (Fed. Cir. 2023). Because, as detailed below, the Petition does not even address the operation of Altera with “data items,” it has not shown limitation 1(g) is met. *See, e.g., Apple, Inc. v. Ginko LLC*, IPR2025-01388, Paper 14, slip op. at 3 (PTAB Mar. 2, 2026) (Squires).

Limitation 1(g) requires “transmitting, from the deserializer to computational circuitry, the first plurality of data streams *comprising a first plurality of data items and a first amount of data streams*.” First, the Petition must draw the computational circuitry because indeed Altera does not use computational circuitry in the manner claimed as explained above. Pet. at 46-47. It then identifies the claimed “first plurality of data streams” as Altera’s “rx_data_out.” *Id. see also id.* at 44 (“A skilled artisan would understand from Figure 1 of Altera that serial rx_data is converted into parallel data, labeled rx_data_out...”.) But when considering what “rx_data_out” is comprised of the Petition baselessly contends “Altera also discloses that the data

streams comprise a first plurality of data items and a first amount of data streams.” Pet. at 48. Instead of citing Altera, the Petition points to the Stratix Handbook’s discussion of “groupings of bits of data” regarding Stratix’s “Word Aligner” to show “data items.” *Id.* at 49 (citing Ex. 1005 at 35 (discussing a “Word Aligner”)). As to the “amount of data streams” the Petition explains “because the data passes through multiple transceivers, the first amount of data streams is, for example, the total number of channels (e.g., an amount of data streams N for RX-1 through RX- N).” But this does not show “data items” are inherent to Altera or obvious in light of Altera and Stratix and as to the amount of data streams this inverts the claimed relationship.

First, that the “Stratix Handbook discloses several data items consistent with the term’s usage in the claims” does nothing to show “data items” are inherent to or otherwise disclosed by Altera. As noted above, inherency must be “*the natural result flowing* from the operation as taught would result in the performance of the questioned function.” *PersonalWeb Techs., LLC v. Apple, Inc.*, 917 F.3d 1376, 1382 (Fed. Cir. 2019) (emphasis original; internal citations and quotations omitted). That the Stratix FPGA of Altera supports certain data formats does not mean using that data format is the natural result of using that hardware. *See Par Pharm., Inc. v. TWI Pharms., Inc.* 773 F.3d 1186, 1195 (Fed. Cir. 2014) (“Inherency, however, may not be established by probabilities or possibilities.”). Nor does the Petition make any

other argument to support inherency. Because there is no showing that Altera must or does use the cited Stratix functionality, there is no inherency.

Similarly, there is no obviousness as to “data items.” First, the Petition makes no express obviousness argument. *See* Pet. at 49. Second, the arguments the Petition makes for including the Stratix Handbook do not justify implementing any particular functionality discussed by Stratix. The Petition offers two bases for its inclusion of Stratix in its proposed grounds: 1) a POSITA “would recognize that the features of [Stratix]... are necessarily present in Altera;” 2) a POSITA “would have been motivated to combine the Stratix Handbook with Si5345 Manual using Altera.” Pet. at 27 and 77. The first only proposes the features of Stratix are present in Altera, not that they are used. Because claim 1 claims a method of use, not the inclusion of certain features, Stratix having features Altera does not use is irrelevant. The second relies on Altera to explain the use of the Stratix hardware where the explanation of “data items” turns this on its head and asks the Board use Stratix to dictate the use in Altera. *See* Pet. at 49. But Altera teaches the method of using Stratix, indeed only a portion of Stratix’s functionality.³ *See* Pet. at 77 (“Altera describes ‘a high-performance SyncE solution’ that consists of Altera’s Stratix...”). But the Petition offers no explanation for why the ethernet data that Altera uses would be formatted

³ Indeed, the Petition never discusses the dynamic reconfiguration functionality, Ex. 1005 at 6-1, or any PCIe functionality, *id.* at 4-24.

according to this section of Stratix. *See id* at 49. As such, there is no basis to find obviousness here either.

Second, the Petition's discussion of the "amount of data streams" is non-sensical. Again, limitation 1(g) claims "the first plurality of data streams comprising ... a first amount of data streams." That is, "the first plurality of data streams" is comprised of the claimed "amount of data streams." The Petition contends the first plurality of parallel data streams is "rx_data_out" and "that there are multiple sets of parallel data streams, as there are multiple receivers (a total of N of them)." Pet. at 44.⁴ Despite this, the Petition points to the multiple sets of parallel data streams to demonstrate what one plurality of data streams comprises. *Id.* at 49 ("because the data passes through multiple transceivers, the first amount of data streams is, for example, the total number of channels (e.g. an amount of data streams N for RX-1 through RX- N)."). "The plurality of data streams" cannot logically be comprised of itself and other such pluralities. As such, the Petition fails to show the claimed "first amount of data streams."

Third, Ground 2 relies on the showing of Ground 1/1A for this limitation. The Petition makes no obviousness argument as to this limitation with regard to Lockwood. As such, Ground 2 fails for the same reasons articulated for Ground 1.

⁴ While "the first plurality of data streams" lacks an exact antecedent basis, it is clear from context, and the Petition agrees as shown in the annotated figure on page 47, the antecedent basis is "a first plurality of parallel data stream" of limitation 1(f).

Because the Petition cannot demonstrate Altera, Stratix, or Lockwood disclose the claimed “data items” or “amount of data streams,” it does not demonstrate a likelihood of success on the merits and institution should be denied.

V. CONCLUSION

Because of the failures noted above, Patent Owner respectfully asks the Director to find the Petition has failed to establish any likelihood of success on the merits and deny institution.

Date: April 15, 2026

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CERTIFICATE OF COMPLIANCE WITH 37 C.F.R. § 42.24

I certify that there are 5,714 words in this paper, excluding the portions exempted under 37 C.F.R. § 42.24(a)(1), according to the word count tool in Microsoft Word.

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CERTIFICATE OF SERVICE (37 C.F.R. § 42.6(e))

The undersigned hereby certifies that the above document was served on April 15, 2026 by filing this document through the Patent Trial and Appeal Case Tracking System (PTACTS) as well as delivering a copy via electronic mail upon the following attorneys of record for Petitioner:

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