

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		
	Filing Date		
	First Named Inventor	Chun-Hsien Lin	
	Art Unit		
	Examiner Name		
	Attorney Docket Number	JCLA31951	

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ None

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Jiawei Huang/	Date (YYYY-MM-DD)	2009-10-02
Name/Print	Jiawei Huang	Registration Number	43330

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal				
Application Number:				
Filing Date:				
Title of Invention:		SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME		
First Named Inventor/Applicant Name:		CHUN-HSIEN LIN		
Filer:		Jiawei Huang/Michelle Chang		
Attorney Docket Number:		JCLA31951		
Filed as Large Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Utility application filing	1011	1	330	330
Utility Search Fee	1111	1	540	540
Utility Examination Fee	1311	1	220	220
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				1090

Electronic Acknowledgement Receipt	
EFS ID:	6192695
Application Number:	12572498
International Application Number:	
Confirmation Number:	4019
Title of Invention:	SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME
First Named Inventor/Applicant Name:	CHUN-HSIEN LIN
Customer Number:	23900
Filer:	Jiawei Huang/Michelle Chang
Filer Authorized By:	Jiawei Huang
Attorney Docket Number:	JCLA31951
Receipt Date:	02-OCT-2009
Filing Date:	
Time Stamp:	13:52:00
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	\$1090
RAM confirmation Number	101
Deposit Account	500710
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees)	

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Application Data Sheet	31951_ADS_Form.pdf	838098	no	4
			e10453d350504c11492a74f5f4386823de727e9f		
Warnings:					
Information:					
2	Oath or Declaration filed	31951_DECLARATION.pdf	94773	no	3
			d108fb51b6b3a1690801e171838885b7c2fe0ba3		
Warnings:					
Information:					
3	Specification	31951_Specification.pdf	1055821	no	33
			c2e465095fe3f264e8fb3fd0fca262fd428efa7		
Warnings:					
Information:					
4	Information Disclosure Statement (IDS) Filed (SB/08)	31951_IDS_Form.pdf	573337	no	4
			f97b998279ea4f3486f9842bd7ae316babe033a		
Warnings:					
Information:					
5	Fee Worksheet (PTO-875)	fee-info.pdf	32975	no	2
			eff5de81e253fbdaf41772a79ec13f552acbd896		
Warnings:					
Information:					
Total Files Size (in bytes):			2595004		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	JCLA31951
		Application Number	
Title of Invention	SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME		
The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76. This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.			

Secrecy Order 37 CFR 5.2

- ☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Applicant Information:

Applicant 1					Remove
Applicant Authority		☒ Inventor		☐ Legal Representative under 35 U.S.C. 117	☐ Party of Interest under 35 U.S.C. 118
Prefix	Given Name	Middle Name	Family Name	Suffix	
	Chun-Hsien		Lin		
Residence Information (Select One) ☐ US Residency ☒ Non US Residency ☐ Active US Military Service					
City	Tainan County	Country Of Residenceⁱ	TW		
Citizenship under 37 CFR 1.41(b)ⁱ		TW			
Mailing Address of Applicant:					
Address 1	No.32, Ln. 326, Bade St., Yongkang City,				
Address 2					
City	Tainan County	State/Province			
Postal Code	710	Countryⁱ	TW		
All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the Add button.					Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below. For further information see 37 CFR 1.33(a).			
☐ An Address is being provided for the correspondence information of this application.			
Customer Number	23900		
Email Address	jcpatents@sbcbglobal.net	Add Email	Remove Email
Email Address	jcpi@msn.com	Add Email	Remove Email

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	JCLA31951
		Application Number	
Title of Invention	SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME		

Application Information:

Title of the Invention	SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME		
Attorney Docket Number	JCLA31951	Small Entity Status Claimed	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Suggested Class (if any)		Sub Class (if any)	
Suggested Technology Center (if any)			
Total Number of Drawing Sheets (if any)	8	Suggested Figure for Publication (if any)	

Publication Information:

☐	Request Early Publication (Fee required at time of Request 37 CFR 1.219)
☐	Request Not to Publish. I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application has not and will not be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32). Enter either Customer Number or complete the Representative Name section below. If both sections are completed the Customer Number will be used for the Representative Information during processing.			
Please Select One:	☒ Customer Number	☐ US Patent Practitioner	☐ Limited Recognition (37 CFR 11.9)
Customer Number	23900		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, or 365(c) or indicate National Stage entry from a PCT application. Providing this information in the application data sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78(a)(2) or CFR 1.78(a)(4), and need not otherwise be made part of the specification.			
Prior Application Status		Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the Add button.			Add

Foreign Priority Information:

This section allows for the applicant to claim benefit of foreign priority and to identify any prior foreign application for which priority is not claimed. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55(a).

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	JCLA31951
		Application Number	
Title of Invention	SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME		

			Remove
Application Number	Country ⁱ	Parent Filing Date (YYYY-MM-DD)	Priority Claimed
			☐ Yes ☒ No
Additional Foreign Priority Data may be generated within this form by selecting the Add button.			Add

Assignee Information:

Providing this information in the application data sheet does not substitute for compliance with any requirement of part 3 of Title 37 of the CFR to have an assignment recorded in the Office.			
Assignee ¹			Remove
If the Assignee is an Organization check here. ☒			
Organization Name	United Microelectronics Corp.		
Mailing Address Information:			
Address 1	No. 3, Li-Hsin Rd. II,		
Address 2	Science-Based Industrial Park,		
City	Hsinchu	State/Province	
Country ⁱ	TW	Postal Code	
Phone Number		Fax Number	
Email Address			
Additional Assignee Data may be generated within this form by selecting the Add button.			Add

Signature:

A signature of the applicant or representative is required in accordance with 37 CFR 1.33 and 10.18. Please see 37 CFR 1.4(d) for the form of the signature.					
Signature	/Jiawei Huang/			Date (YYYY-MM-DD)	2009-10-02
First Name	Jiawei	Last Name	Huang	Registration Number	43330

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4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
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6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
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9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

DECLARATION FOR UTILITY OR DESIGN PATENT APPLICATION

As the below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name and that I believe I am an original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a design or Utility patent is sought on the invention entitled

SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME

the specification of which

 X is attached hereto.

 was filed on _____

as Application Serial No. _____ and was amended on _____.

I hereby state that I have reviewed and understand the contents of the above-identified application, including the specification, claims and figures if any, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, § 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, § 119(a)-(d) or 365(b) of any foreign application(s) for patent or 365(a) of any PCT international application which designated at least one country other than the United States of America, or inventor's certificate listed on the Application Data Sheet, and have also identified on the Application Data Sheet any foreign application for patent or inventor's certificate having a filing date before that of each application on which priority is claimed:

I hereby claim the benefit under Title 35 U.S. Code § 119(e) of any U.S. provisional applications listed on the Application Data Sheet.

I hereby claim the benefit under Title 35, United States Code § 120 of any United States application(s) or PCT international application(s) designating The United States of America listed on the Application Data Sheet, and, insofar as the subject matter of each of the claims of this application is not disclosed in that/those prior application(s) in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulation, § 1.56 which become available between the filing date of the prior application(s) and the national or PCT international filing date of this application.

DECLARATION FOR UTILITY OR DESIGN PATENT APPLICATION

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any design or utility patents issued thereon.

Signature: Chun-Hsien Lin

Date: 2009. Sep. 18

Sole or First Joint Inventor: Chun-Hsien Lin

Citizenship: Taiwan, R.O.C.

Residence : Tainan County, Taiwan

Post Office Address: No.32, Ln. 326, Bade St., Yongkang City, Tainan County 710, Taiwan
(R.O.C.)

POWER OF ATTORNEY
AND
CORRESPONDENCE ADDRESS INDICATION FORM

First Names Inventor	Chun-Hsien Lin		
Title	: SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME		
Attorney Docket Number	: JCLA31951		
Application Number	:	Filing Date	:
Art Unit	:	Examiner Name	:

As the below named inventor(s), I hereby appoint : practitioners associated with the
Customer Number : **23900**

as my/our attorney(s) or patent agent(s) to prosecute the application identified above,
and to transact business in the United States Patent and Trademark Office connected therewith.

Please recognize the correspondence address for the above-identified application to : the
address associated with the above-mentioned Customer Number.

SIGNATURE(s) of Applicant/Inventor

Signature:

Chun-Hsien Lin

Date:

2009 Sep 18

Sole or First Joint Inventor: Chun-Hsien Lin

SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME

BACKGROUND OF THE INVENTION

Field of the Invention

[0001] The invention relates to a semiconductor device and a method of fabricating the same. More particularly, the invention relates to a void-free semiconductor device and a method of fabricating the same.

Description of Related Art

[0002] With the continual miniaturization of semiconductor devices, dimensions of gate structures are also gradually reduced. Therefore, the thickness of gate dielectric layers also needs to be reduced to prevent the performance of the devices from being affected. Generally, the material of the gate dielectric layers usually includes silicon oxide. However, the leakage current phenomenon frequently occurs when reducing the thickness of the gate dielectric layers adopting silicon oxide. In order to reduce the occurrence of leakage current, a conventional method is to replace silicon oxide with high dielectric constant (high-k) material for the gate dielectric layers. When applying high dielectric constant material in the gate dielectric layers, the gates adopting polysilicon then react with high dielectric constant material to generate Fermi-level pinning, thereby resulting in an increase in the threshold voltage so as to affect device performance. In one of the conventional techniques, the metal layer is applied as the gate, that is, the work function metal layer known in the art, to prevent the threshold voltage from increasing and therefore reducing the resistance of the device.

[0003] In a conventional gate structure composed of a high dielectric constant dielectric layer and a metal gate, the dummy patterns are first formed and then the gate structures are formed in the current method. In other words, the dummy patterns and the interlayer dielectric layer are first formed on the substrate. Next, the dummy patterns are removed, and then the metal gate structures are formed in the openings that are formed after the removal of the dummy patterns.

[0004] However, in the process of patterning the dummy pattern material layer to form the dummy patterns, due to the constraints of the etching process, the resultant dummy patterns are usually shaped into trapezoids having a narrow top and a wide bottom, so that an included angle between the top sidewall of each the dummy pattern and the surface of the interlayer dielectric layer is about $88^{\circ}\sim 89^{\circ}$. Since the trapezoid dummy patterns have a narrow top and a wide bottom, an opening with a narrower top portion is formed after the dummy patterns are removed. Hence, when the opening is filled with the metal layer by a sputtering process, the effect of metal gap fill is poor, so that problems such as overhang and the like usually occur to cause the formation of voids in the metal layer, thereby affecting the reliability and performance of the device.

SUMMARY OF THE INVENTION

[0005] Accordingly, the invention provides a method of fabricating a semiconductor device to carry out an ion implantation process before dummy patterns are formed, so as to enhance the reliability and performance of the device.

[0006] The invention provides a semiconductor device, in which a gate structure thereof is disposed in a trench having a wider opening in a top, and the semiconductor device therefore includes a void-free metal layer.

[0007] The invention provides a method of fabricating a semiconductor device. Firstly, a polysilicon layer is formed on a substrate. An N-type dopant is doped into the polysilicon layer. Next, a portion of the polysilicon layer is removed to form a plurality of dummy patterns. Each dummy pattern includes a top, a bottom, and a neck arranged between the top and the bottom. Here, the width of the neck is narrower than that of the top. Thereafter, a dielectric layer is formed on the substrate. The dielectric layer covers the substrate between adjacent dummy patterns and exposes the top of each dummy pattern. Subsequently, the dummy patterns are removed to form a plurality of trenches in the dielectric layer. Afterwards, a plurality of gate structures is formed in the trenches respectively.

[0008] According to an embodiment of the invention, the depth of the polysilicon layer doped with the highest concentration of the N-type dopant and the neck are substantially located on the same horizontal level of height.

[0009] According to an embodiment of the invention, the concentration of the N-type dopant doped in the bottom of the polysilicon layer is greater than the concentration of the N-type dopant doped in the top of the same.

[0010] According to an embodiment of the invention, the concentration of the N-type dopant doped increases gradually from the top to the bottom of the polysilicon layer.

[0011] According to an embodiment of the invention, the method of fabricating the semiconductor device further includes a step of doping another N-type dopant into the polysilicon layer.

[0012] According to an embodiment of the invention, the N-type dopant is phosphorus (P), antimony (Sb), or arsenic (As).

[0013] According to an embodiment of the invention, when the N-type dopant is

phosphorus, the energy for doping is greater than 1 Kev but less than 20 KeV and the dose therefor is greater than $1\text{E}15\text{ cm}^{-2}$ but less than $8\text{E}15\text{ cm}^{-2}$.

[0014] According to an embodiment of the invention, the top and the neck have a first height therebetween, the neck and the bottom have a second height therebetween, and the ratio of the first height to the second height is substantially 2:1.

[0015] According to an embodiment of the invention, an included angle between the sidewall of the top of each trench and the surface of the dielectric layer is larger than 90° .

[0016] According to an embodiment of the invention, the method of removing a portion of the polysilicon layer further includes an etching process using a halogen-containing reactant.

[0017] According to an embodiment of the invention, before the dummy patterns are removed, a high dielectric constant layer is further formed between the substrate and each of the dummy patterns.

[0018] According to an embodiment of the invention, the method of fabricating the semiconductor device further includes a step of forming a source/drain region in the substrate at respective sides of the gate structure. The method of forming the source/drain region, for example, includes performing an ion implantation process or a selective epitaxy growth (SEG) process.

[0019] According to an embodiment of the invention, after the dummy patterns are formed and before the dielectric layer is formed, a spacer is further formed on the sidewall of each dummy pattern.

[0020] The invention further provides a semiconductor device including a substrate, a gate structure, and a source/drain region. A dielectric layer is formed on the substrate,

and a trench is disposed in the dielectric layer. The gate structure is located in the trench and includes a high dielectric constant layer, a work function metal layer, and a metal layer sequentially disposed on the substrate. The source/drain region is disposed in the substrate at the respective sides of the gate structure. The trench includes a top, a bottom, and a neck arranged between the top and the bottom. The width of the neck is narrower than that of the top, and the width of the neck is narrower than or equal to that of the bottom.

[0021] According to an embodiment of the invention, the top and the neck have a first height therebetween, the neck and the bottom have a second height therebetween, and the ratio of the first height to the second height is substantially 2:1.

[0022] According to an embodiment of the invention, an included angle between the sidewall of the top of each trench and the surface of the dielectric layer is larger than 90°.

[0023] According to an embodiment of the invention, the semiconductor device further includes an insulation layer disposed between the substrate and the high dielectric constant layer.

[0024] According to an embodiment of the invention, the source/drain region is a doped region or an epitaxial layer.

[0025] According to an embodiment of the invention, the semiconductor device further includes a spacer disposed on the sidewall of the gate structure.

[0026] In light of the foregoing, in the method of fabricating the semiconductor device of the invention, the ion implantation process is performed after the polysilicon layer is formed. Thus, when removing a portion of the polysilicon layer, different etching rates at different depth locations of the doped polysilicon layer are utilized to

form the dummy patterns having the width of the neck narrower than the width of the top. Hence, when removing the dummy patterns and filling the metal layer, not only are the dummy patterns removed rapidly, but the effect of metal gap fill is also improved, such that voids do not form easily, thereby greatly enhancing the reliability and performance of the device.

[0027] The gate structure of the semiconductor device in the invention is disposed in the trench having a wide opening in the top portion. Therefore, the metal layer of the gate structure does not include voids and can have superior device performance.

[0028] In order to make the aforementioned and other features and advantages of the invention more comprehensible, several embodiments accompanied with figures are described in detail below.

BRIEF DESCRIPTION OF THE DRAWINGS

[0029] The accompanying drawings are included to provide a further understanding of the invention, and are incorporated in and constitute a part of this specification. The drawings illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention.

[0030] Figs. 1A through 1E are cross-sectional views schematically illustrating a process for fabricating a semiconductor device according to an embodiment of the invention.

[0031] Fig. 2 and Fig. 3 respectively illustrate schematic cross-sectional views of dummy patterns according to another embodiment of the invention.

[0032] Fig. 4 is a cross-sectional view schematically illustrating a semiconductor device according to another embodiment of the invention.

DESCRIPTION OF EMBODIMENTS

[0033] Figs. 1A through 1E are cross-sectional views schematically illustrating a process for fabricating a semiconductor device according to an embodiment of the invention. It should be noted that the method of fabricating the semiconductor device described in the following adopts a gate last process to form a complementary metal oxide semiconductor (CMOS) device for illustration. People skilled in the art should be able to embody the invention based on the illustration, whereas the scope of the invention is not limited thereto. The formation of a single metal oxide semiconductor (MOS) device may also be implemented. Moreover, the disposition locations, the manners and the sequence of formation of other components such as metal gate structures, doped regions, spacers, stop layers, and the like are all fabricated with techniques known to people skilled in the art based on conventional arts, and are not limited to the descriptions illustrated in the following embodiments.

[0034] Referring to Fig. 1A, a substrate 100 is provided. The substrate 100, for example, is a semiconductor substrate such as an N-type or a P-type silicon substrate, group III-V semiconductor substrate, and the like. The substrate 100 includes a first region 101a and a second region 101b. The first region 101a and the second region 101b are spaced by isolation structures 102. In one embodiment, when the first region 101a is a P-type metal oxide semiconductor (PMOS) region, the second region 101b is an N-type metal oxide semiconductor (NMOS) region. The isolation structures 102 are shallow trench isolation structures, for example.

[0035] Next, a high dielectric constant (high-k) material layer 104 and a polysilicon layer 106 are sequentially formed on the substrate 100. The material of the high

dielectric constant material layer 104 is, for example, a dielectric material with a dielectric constant greater than 4, such as TiO_2 , HfO_2 , ZrO_2 , Al_2O_3 , La_2O_3 , Y_2O_3 , Gd_2O_3 , Ta_2O_5 , or a combination thereof. The high dielectric constant material layer 104 is fabricated by a chemical vapor deposition (CVD) process, for instance. In one embodiment, before the high dielectric constant material layer 104 is formed, an insulation material layer 103 is also optionally formed on a surface of the substrate 100 to enhance an adhesion between the high dielectric constant material layer 104 and the substrate 100. The insulation material layer 103 is made of, for example, silicon oxide and formed, for example, in a thermal oxidizing process. The polysilicon layer 106 can be used as a material layer of dummy patterns to be formed subsequently, and is formed in a CVD process, for instance.

[0036] Afterwards, an ion implantation process 107 is performed to dope an N-type dopant into the polysilicon layer 106. In the ion implantation process 107, a blanket doping process is performed to the polysilicon layer 106 using a vertical ion implantation manner, for example. The N-type dopant, for example, is phosphorus (P), antimony (Sb), or arsenic (As). A concentration of the N-type dopant distributed in the polysilicon layer 106 varies with different depth locations in the polysilicon layer 106. For instance, the depth with the highest concentration of the doped N-type dopant is between the top and the bottom of the polysilicon layer 106. Alternatively, the concentration of the doped N-type dopant gradually increases from the top to the bottom of the polysilicon layer 106. In one embodiment, when the thickness of the polysilicon layer 106 is about 500 Å to 600 Å and the N-type dopant implanted is phosphorus, an appropriate energy within a range of 1 Kev to 20KeV and a dose within a range of $1\text{E}15$ to $8\text{E}15 \text{ cm}^{-2}$ are utilized in the ion implantation process 107. As a

consequence, the location with the highest concentration of the N-type dopant is at a depth of about 300 Å to 400 Å away from the surface of the polysilicon layer 106.

[0037] Referring to Fig 1B, a patterned hard mask layer 108 is formed on the polysilicon layer 106. The patterned hard mask layer 108, for example, has openings to expose a portion of the surface of the polysilicon layer 106. In this step, the disposition of the openings of the patterned hard mask layer 108 is designed according to locations of gate structures to be formed subsequently. That is, the locations of the polysilicon layer 106 covered by the patterned hard mask layer 108 are the locations of the gate structures subsequently formed. The material of the patterned hard mask layer 108 is selected from materials having etching selectivity different from that of the polysilicon layer 106. Here, the material is silicon nitride, silicon oxide, or silicon oxynitride, for example. In a formation of the patterned hard mask layer 108, a layer of hard mask material layer (not shown) is first formed on the substrate 100 using the CVD process, for example. Thereafter, a photolithographic process and an etching process are sequentially performed by adopting a photoresist material to remove a portion of the hard mask material layer.

[0038] Subsequently, the patterned hard mask layer 108 is used as a mask to remove the exposed polysilicon layer 106, so as to form a plurality of dummy patterns 110. Afterwards, the high dielectric constant material layer 104 and the insulation material layer 103 are patterned to form the high dielectric constant layer 104a and the insulation layer 103a. Here, the high dielectric constant layer 104a and the insulation layer 103a are adopted jointly as a gate dielectric layer of the gate structure to be subsequently formed. Each dummy pattern 110 includes a top 110a, a neck 110b, and a bottom 110c. The neck 110b is arranged between the top 110a and the bottom 110c. The

width of the neck 110b is narrower than that of the top 110a, and the width of the neck 110b is narrower than that of the bottom 110c, for example. Therefore, a cross-section with a funnel-like shape is formed. In one embodiment, when the top 110a and the neck 110b have a first height H_1 therebetween, and the neck 110b and the bottom 110c have a second height H_2 therebetween, the ratio of the first height H_1 to the second height H_2 is substantially 2:1. In a method of removing a portion of the polysilicon layer 106 to form the dummy patterns 110, a halogen-containing reactant is used for etching. A plasma gas source adopted in dry etching to remove a portion of the polysilicon layer 106 contains fluorine radicals, chlorine radicals, or bromine radicals, for instance.

[0039] It should be noted that the etching rate of the polysilicon layer 106 doped with the N-type dopant is higher than the etching rate of the undoped polysilicon material, and the etching rate increases as the concentration of the N-type dopant enhances. Therefore, the depth of the polysilicon layer 106 doped with the highest concentration of the N-type dopant and the neck 110b are substantially located on the same horizontal level of height as illustrated in Fig. 1B.

[0040] The above-mentioned embodiment is illustrated with the dummy patterns 110 having funnel-like cross-sections. However, the invention is not limited thereto. People of ordinary skills in the art should understand that as long as the width of the neck is narrower than that of the top, the dummy patterns can also be in other shapes. In other words, the concentration distribution of the N-type dopant in the polysilicon layer 106 is adjusted by controlling parameters such as an implantation energy of the ion implantation process 107 and the like. As a result, the location of the horizontal level of height of the highest N-type dopant concentration substantially corresponds to

the location of the horizontal level of height of the narrowest width of the dummy patterns formed later. Fig. 2 and Fig. 3 respectively illustrate schematic cross-sectional views of dummy patterns according to another embodiment of the invention. In Figs. 2 and 3, identical reference numerals are used for the same elements as those in Fig. 1B, and description of those elements is omitted.

[0041] In one embodiment, the concentration of the N-type dopant doped in the bottom of the polysilicon layer 106 is made greater than the concentration of the N-type dopant doped in the top thereof by controlling parameters such as the energy for implanting the N-type dopant in the ion implantation process 107 and the like. As illustrated in Fig. 2, after a portion of the polysilicon layer 106 is removed by the etching process, the width of a neck 200b of each dummy pattern 200 is, for instance, narrower than the width of a top 200a. Moreover, the width of the neck 200b substantially equals to the width of a bottom 200c, so as to form a cross-section with a wide top and a narrow bottom.

[0042] In one embodiment, the concentration of the doped N-type dopant is increased from the top to the bottom of the polysilicon layer 106 by controlling the parameters such as the energy for implanting the N-type dopant in the ion implantation process 107 and the like. As illustrated in Fig. 3, after a portion of the polysilicon layer 106 is removed by the etching process, the width a neck 300b of each dummy pattern 300 is, for instance, narrower than the width of a top 300a. Moreover, the width of the neck 300b is greater than the width of a bottom 300c, for example, so as to form a trapezoid cross-section reducing gradually from the top to the bottom.

[0043] Moreover, in other embodiments of the invention, a plurality of N-type dopants is doped into the polysilicon layer 106, so that the polysilicon layer 106 has the

etching rate required at different depths, thereby facilitating the formation of dummy patterns. Obviously, the method of doping the N-type dopant into the polysilicon layer 106 is not limited to the embodiments aforementioned. That is, various methods are acceptable as long as the N-type dopant is doped into the polysilicon material to form dummy patterns having the width of the top greater than that of the neck. People with ordinary skills in the art can make necessary adjustments based on actual demands.

[0044] Referring to Fig. 1C simultaneously, the dummy patterns 110 are used as masks for carrying out the ion implantation process so as to form lightly-doped regions 113a in the substrate 100 at respective sides of the dummy pattern 110 within the first region 101a, and to form lightly-doped regions 113b in the substrate 100 at respective sides of the dummy pattern 110 within the second region 101b. The lightly-doped regions 113a and 113b serve as source/drain extension regions of respective MOS transistors to be formed. When the first region 101a is the PMOS region, the lightly-doped regions 113a are P-type lightly-doped regions. When the second region 101b is the NMOS region, the lightly-doped regions 113b are N-type lightly-doped regions. Thereafter, spacers 112 are formed on sidewalls of the dummy patterns 110. The material of the spacers 112 is silicon oxide, silicon nitride, or silicon oxynitride, for example. In a method of forming the spacers 112, for example, a layer of spacer material (not illustrated) is first formed on the substrate 100 by the CVD process, and a portion of the spacer material layer is removed by an anisotropic etching process. In addition, although the spacers 112 are merely illustrated with single-layer structures in Fig. 1C, the spacers 112 can also be multi-layer spacer structures.

[0045] Afterwards, source/drain regions 114a are formed in the substrate 100 at the respective sides of the dummy pattern 110 within the first region 101a, and source/drain

regions 114b are formed in the substrate 100 at the respective sides of the dummy pattern 110 within the second region 101b. When the first region 101a is the PMOS region, the source/drain regions 114a are P-type heavily-doped regions or SiGe epitaxial layers, for example. When the second region 101b is the NMOS region, the source/drain regions 114b are N-type heavily-doped regions, for instance. In one embodiment, the source/drain regions 114a and 114b are formed by the ion implantation process, for example, so as to form the P-type or the N-type heavily-doped regions respectively in the substrate 100. In another embodiment, in the formation of the source/drain regions 114a, a portion of the substrate 100 at the respective sides of the dummy pattern 110 within the first region 101a is first removed to form trenches (not shown), for example. Subsequently, a selective epitaxy growth (SEG) process is performed to form the SiGe epitaxial layer in each trench. The SiGe epitaxial layer is not only used as the source/drain region of the PMOS transistor, but also increases a compressive stress of a channel of the PMOS transistor, so that mobility of holes increases, thereby enhancing operation speed and performance of the PMOS transistor.

[0046] After the source/drain regions 114a and 114b are formed, a stop layer 116 is optionally formed on the substrate 100 to cover the first region 101a and the second region 101b entirely. The stop layer 116 is made of silicon nitride, and formed by the CVD process, for example. In one embodiment, the stop layer 116 is utilized as a stress layer providing compressive stress or tensile stress to a channel region. Moreover, the stop layer 116 is capable of generating the tensile stress suitable for the channel of the NMOS transistor or the compressive stress suitable for the channel of the PMOS transistor by changing process parameters in the formation of the stop layer 116. Afterwards, a dielectric layer 118 is formed on the substrate 100 as an interlayer

dielectric (ILD) layer. The dielectric layer 118 covers the substrate 100 and the dummy patterns 110 entirely, for instance. The dielectric layer 118, for example, is made of silicon oxide, and can be formed by the CVD process.

[0047] Referring to Fig. 1D, a portion of the dielectric layer 118 and a portion of the stop layer 116 are removed to expose upper surfaces of the dummy patterns 110. A portion of the dielectric layer 118 and a portion of the stop layer 116 are removed by performing a chemical-mechanical polishing (CMP) process or an etching-back process, for example. Thereafter, the dummy patterns 110 are removed to form the trenches 120 and a surface of the high dielectric constant layer 104a is exposed. The dummy patterns 110 are removed, for example, by carrying out a wet etching process, which utilizes KOH solution as an etching solution.

[0048] It should be illustrated that the polysilicon doped with the N-type dopant usually has a higher etching rate than the undoped polysilicon. In addition, the etching rate of the polysilicon doped with the N-type dopant is far higher than the etching rate of the polysilicon doped with the P-type dopant. In the previous step, the polysilicon layer is doped with the N-type dopant before the dummy patterns 110 are formed. Therefore, when the dummy patterns 110 are removed by wet etching, a rapid removing rate results and the residual polysilicon material does not remain easily in the trenches 120. Additionally, the doping of the N-type dopant into the polysilicon layer further compensates the P-type dopant implanted in the formation of the lightly-doped regions 113a and 113b or the source-drain regions 114a and 114b. Thus, problems such as troublesome removal of the dummy patterns 110 resulted from P-type dopant overdope are prevented.

[0049] Referring to Fig. 1E, a work function metal layer 122 is formed conformally

on the surface of the trench 120 in the first region 101a, and a work function metal layer 124 is formed conformally on the surface of the trench 120 in the second region 101b. The material of the work function metal layers 122 and 124 includes all materials capable of achieving the work function required, such as TiN, TiAl_x, TaC, TaCNO, TaCN, or TaN, for instance. The work function metal layers 122 and 124 are formed by the CVD or a physical vapor deposition (PVD) process, for example. The material of the work function metal layer 122 and that of the work function metal layer 124 are different, for instance. In one embodiment, when the first region 101a is the PMOS region, the material of the work function metal layer 122 is TiN, for instance. When the second region 101b is the NMOS region, the material of the work function metal layer 124 is TiAl_x, for example. Next, a metal layer 126 is filled into the trenches 120 so as to form gate structures 130a and 130b respectively. The metal layer 126 is made of, for example, Al, aluminum-rich TiAl_x, Ti, or a combination thereof, and formed by the CVD process or the PVD process.

[0050] Generally, the work function value required by the PMOS transistor is approximately from 5 eV to 5.1 eV, and the work function value required by the NMOS transistor is approximately from 4 eV to 4.1 eV. The work function of the gate structure 130a is determined by the metal layer 126 and the work function metal layer 122 underneath. The work function of the gate structure 130b is determined by the metal layer 126 and the work function metal layer 124 underneath. Therefore, the work function values respectively required by the PMOS transistor and the NMOS transistor can be achieved by adjusting the material and the thickness of the work function metal layers 122 and 124.

[0051] It should be illustrated that since the width of the neck is narrower than that of

the top of each dummy pattern, the trench 120 formed after the removal of each dummy pattern is shaped into a structure having a wide opening in the top portion. That is, an included angle θ_1 between the sidewall of the top 120a of the trench 120 and the surface of the dielectric layer 118 is larger than 90° , for instance. Hence, the trenches 120 each having a wide opening in the top portion not only facilitate the rapid removal of the dummy patterns, but also have superior metal gap fill effect when forming the metal layer 126 so that voids are not formed easily.

[0052] Fig. 1E is used as an exemplary example in the following to further illustrate the structure of the semiconductor device of the invention.

[0053] Referring to Fig. 1E, the semiconductor device of the present embodiment includes the substrate 100, the gate structures 130a and 130b, and the source/drain regions 114a and 114b. The substrate 100 includes the first region 101a and the second region 101b spaced by the isolation structures 102. When the first region 101a, for instance, is the PMOS region, the second region 101b is the NMOS region. The dielectric layer 118 is disposed on the substrate 100, and the trenches 120 are disposed in the dielectric layer 118. Each trench 120 includes a top 120a, a neck 120b, and a bottom 120c. The neck 120b is arranged between the top 120a and the bottom 120c.

[0054] The gate structure 130a, for example, is disposed within the first region 101a, and includes the insulation layer 103a, the high dielectric constant layer 104a, the work function metal layer 122, and the metal layer 126 disposed sequentially on the substrate 100. The high dielectric constant layer 104a and the insulation layer 103a are adopted jointly as a gate dielectric layer of the gate structure 130a, for example. The work function of the gate structure 130a is determined by the metal layer 126 and the work function metal layer 122 underneath, for example. The source/drain regions 114a are

disposed in the substrate 100 at respective sides of the gate structure 130a. In one embodiment, the lightly-doped regions 113a are disposed in the substrate 100 between the gate structure 130a and the source/drain regions 114a.

[0055] The gate structure 130b, for example, is disposed within the second region 101b, and includes the insulation layer 103a, the high dielectric constant layer 104a, the work function metal layer 124, and the metal layer 126 disposed sequentially on the substrate 100. The high dielectric constant layer 104a and the insulation layer 103a are adopted jointly as a gate dielectric layer of the gate structure 130b. The work function of the gate structure 130b is determined by the metal layer 126 and the work function metal layer 124 underneath, for example. The source/drain regions 114b are disposed in the substrate 100 at the respective sides of the gate structure 130b. In one embodiment, the lightly-doped regions 113b are disposed in the substrate 100 between the gate structure 130b and the source/drain regions 114b.

[0056] As aforementioned, the gate structures 130a and 130b are disposed in the trenches 120, for example. The insulation layer 103a is disposed on the surface of the substrate 100 in the trenches 120. The high dielectric constant layer 104a is disposed on the surface of the insulation layer 103a. The work function metal layer 122 and the work function metal layer 124 are conformally disposed on the surfaces of the trenches 120 in the first region 101a and the second region 101b, and cover the high dielectric constant layer 104a, respectively. The metal layer 126 fills the trenches 120 and covers the work function metal layers 122 and 124.

[0057] It should be noted that each trench 120 is a structure having a wide opening in the top portion, for example. That is, an included angle θ_1 between the sidewall of the top 120a of each trench 120 and the surface of the dielectric layer 118 is larger than 90° ,

for example. The width of the neck 120b of each trench 120 is narrower than that of the top 120a, and the width of the neck 120b is narrower than that of the bottom 120c, for example. Therefore, cross-sections with a funnel-like shape are formed. In one embodiment, the ratio of the height from the neck 120b to the top 120a and the height from the neck 120b to the bottom 120c is substantially 2:1. In other words, when the depth of the trenches 120 is about 500 Å to 600 Å, the difference in height between the neck 120b and the top 120a of each trench 120, for example, is about 300 Å to 400 Å.

[0058] In addition, the gate structures in the semiconductor device of the invention not only form the funnel-like trenches aforementioned, but can also form trenches of other shapes. Fig. 4 is a cross-sectional view schematically illustrating a semiconductor device according to another embodiment of the invention. In Fig. 4, identical reference numerals are used for the same elements as those in Fig. 1E, and description of those elements is omitted.

[0059] Referring to Fig. 4, in another embodiment, the main components constituting the semiconductor device illustrated in Fig. 4 are generally identical to those constituting the semiconductor device illustrated in Fig. 1E. However, the difference between the two semiconductor devices mainly regards to the forms of the trenches. The gate structures 130a and 130b are disposed in the trenches 400, for example. Each trench 400 is a structure having a wide opening in the top portion, and an included angle θ_2 between a sidewall of a top 400a thereof and the surface of the dielectric layer 118 is larger than 90°, for instance. The width of a neck 400b of each trench 400 is narrower than the width of the top 400a, for example. Furthermore, the width of the neck 400b of each trench 400 substantially equals to the width of a bottom 400c, so as to form a cross-section having a wide top and a narrow bottom.

[0060] In light of the foregoing, the semiconductor device and the method of fabricating the same in the embodiments aforementioned have at least the following advantages:

1. The gate structures of the semiconductor device in the embodiments above-mentioned are disposed in the trenches each having the width of the neck narrower than that of the top. Therefore, the metal layers filled in the trenches do not have voids, and thereby have superior device performance.

2. Each trench of the semiconductor device in the embodiments above-mentioned has the design of the width of the neck narrower or equal to that of the bottom, so that trench having a wide opening can be formed without reducing the width of the bottom. Consequently, the critical dimension (CD) of the device is not affected.

3. In the method of fabricating the semiconductor device in the embodiments above-mentioned, before the dummy patterns are formed, the N-type dopant is doped into the polysilicon layer to enhance the etching rate of the polysilicon layer regionally. As a result, the dummy patterns each having the width of the neck narrower than that of the top are formed so as to enhance the metal gap fill ability, so that voids do not form easily.

4. In the method of fabricating the semiconductor device in the embodiments above-mentioned, the doping of the N-type dopant into the polysilicon layer further compensates the P-type dopant implanted in the process, so that the dummy patterns can be removed rapidly without leaving residual polysilicon material in the trenches.

5. The method of fabricating the semiconductor device in the embodiments aforementioned can be applied in all gate last processes, especially in the gate last process for forming metal gates, and can be integrated with the existing semiconductor

process. The process aforementioned is not only simple, but can also improve the reliability of the device effectively.

[0061] Although the present invention has been described with reference to the above embodiments, it will be apparent to one of the ordinary skill in the art that modifications to the described embodiment may be made without departing from the spirit of the invention. Accordingly, the scope of the invention will be defined by the attached claims not by the above detailed descriptions.

WHAT IS CLAIMED IS:

1. A method of fabricating a semiconductor device, comprising:
forming a polysilicon layer on a substrate;
doping an N-type dopant into the polysilicon layer;
removing a portion of the polysilicon layer to form a plurality of dummy patterns, each of the plurality of dummy patterns having a top, a bottom, and a neck arranged between the top and the bottom, wherein a width of the neck is narrower than a width of the top;
forming a dielectric layer on the substrate, the dielectric layer covering the substrate disposed between two adjacent dummy patterns and exposing the top of each dummy pattern;
removing the plurality of dummy patterns to form a plurality of trenches in the dielectric layer; and
forming a plurality of gate structures in the trenches respectively.
2. The method of fabricating the semiconductor device as claimed in claim 1, wherein a depth of the polysilicon layer doped with a highest concentration of the N-type dopant and the neck are substantially located on the same horizontal level of height.
3. The method of fabricating the semiconductor device as claimed in claim 1, wherein a concentration of the N-type dopant doped in a bottom of the polysilicon layer is greater than a concentration of the N-type dopant doped in a top of the polysilicon layer.
4. The method of fabricating the semiconductor device as claimed in claim 1, wherein a concentration of the N-type dopant doped increases gradually from a top to a

bottom of the polysilicon layer.

5. The method of fabricating the semiconductor device as claimed in claim 1, further comprising doping another N-type dopant into the polysilicon layer.

6. The method of fabricating the semiconductor device as claimed in claim 1, wherein the N-type dopant is phosphorus (P), antimony (Sb), or arsenic (As).

7. The method of fabricating the semiconductor device as claimed in claim 1, wherein when the N-type dopant is phosphorus, an energy for doping is within a range of 1 Kev to 20 KeV and a dose for doping is within a range of $1E15\text{ cm}^{-2}$ to $8E15\text{ cm}^{-2}$.

8. The method of fabricating the semiconductor device as claimed in claim 1, wherein the top and the neck have a first height therebetween, the neck and the bottom have a second height therebetween, and a ratio of the first height to the second height is substantially 2:1.

9. The method of fabricating the semiconductor device as claimed in claim 1, wherein an included angle between a sidewall of a top of each of the plurality of trenches and a surface of the dielectric layer is larger than 90° .

10. The method of fabricating the semiconductor device as claimed in claim 1, wherein the step of removing a portion of the polysilicon layer comprises performing an etching process using a halogen-containing reactant.

11. The method of fabricating the semiconductor device as claimed in claim 1, before removing the plurality of dummy patterns, further comprising forming a high dielectric constant layer between the substrate and each of the plurality of dummy patterns.

12. The method of fabricating the semiconductor device as claimed in claim 1, further comprising forming a source/drain region in the substrate at respective sides of

the gate structure.

13. The method of fabricating the semiconductor device as claimed in claim 12, wherein the step of forming the source/drain region comprises performing an ion implantation process or a selective epitaxy growth process.

14. The method of fabricating the semiconductor device as claimed in claim 1, after forming the plurality of dummy patterns and before forming the dielectric layer, further comprising forming a spacer on a sidewall of each of the plurality of dummy patterns.

15. A semiconductor device, comprising:

a substrate, disposed with a dielectric layer thereon, wherein a trench is disposed in the dielectric layer;

a gate structure, located in the trench and comprising a high dielectric constant layer, a work function metal layer, and a metal layer sequentially disposed on the substrate; and

a source/drain region, disposed in the substrate at respective sides of the gate structure,

wherein the trench comprises a top, a bottom, and a neck arranged between the top and the bottom, a width of the neck is narrower than a width of the top, and the width of the neck is narrower than or equal to a width of the bottom.

16. The semiconductor device as claimed in claim 15, wherein the top and the neck have a first height therebetween, the neck and the bottom have a second height therebetween, and a ratio of the first height to the second height is substantially 2:1.

17. The semiconductor device as claimed in claim 15, wherein an included angle between a sidewall of the top of each of the plurality of trenches and a surface of the

dielectric layer is larger than 90° .

18. The semiconductor device as claimed in claim 15, further comprising an insulation layer disposed between the substrate and the high dielectric constant layer.

19. The semiconductor device as claimed in claim 15, wherein the source/drain region is a doped region or an epitaxial layer.

20. The semiconductor device as claimed in claim 15, further comprising a spacer disposed on a sidewall of the gate structure.

ABSTRACT OF THE DISCLOSURE

A semiconductor device and a method for fabricating the same are described. A polysilicon layer is formed on a substrate. The polysilicon layer is doped with an N-type dopant. A portion of the polysilicon layer is then removed to form a plurality of dummy patterns. Each dummy pattern has a top, a bottom, and a neck arranged between the top and the bottom, where the width of the neck is narrower than that of the top. A dielectric layer is formed on the substrate to cover the substrate disposed between adjacent dummy patterns, and the top of each dummy pattern is exposed. Thereafter, the dummy patterns are removed to form a plurality of trenches in the dielectric layer. A plurality of gate structures is formed in the trenches, respectively.

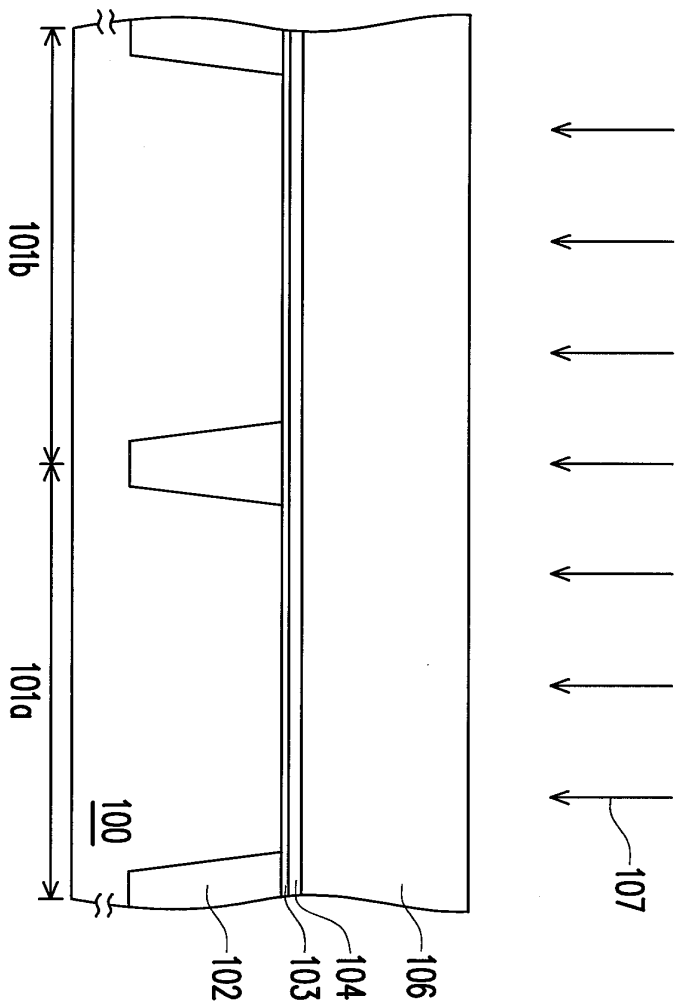


FIG. 1A

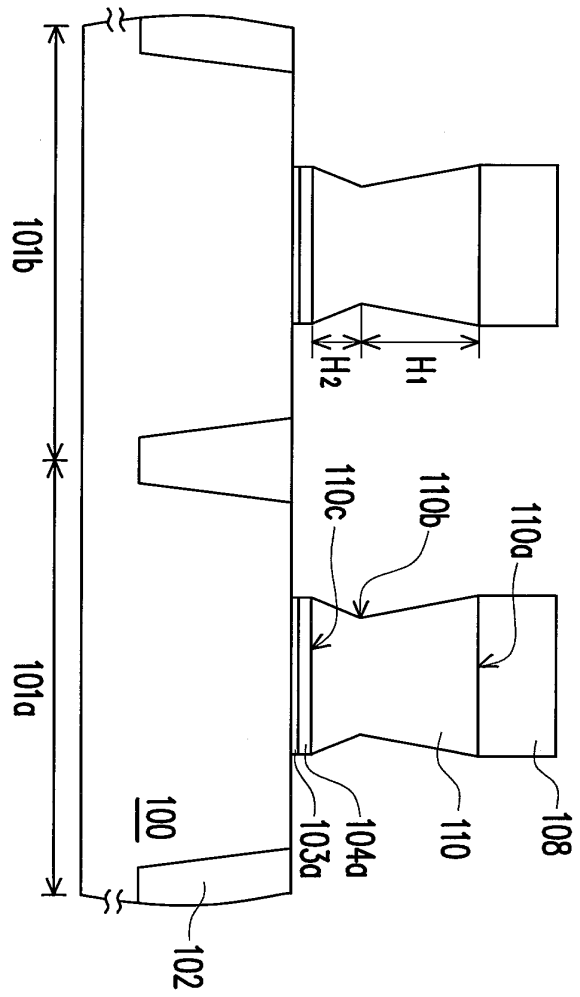


FIG. 1B

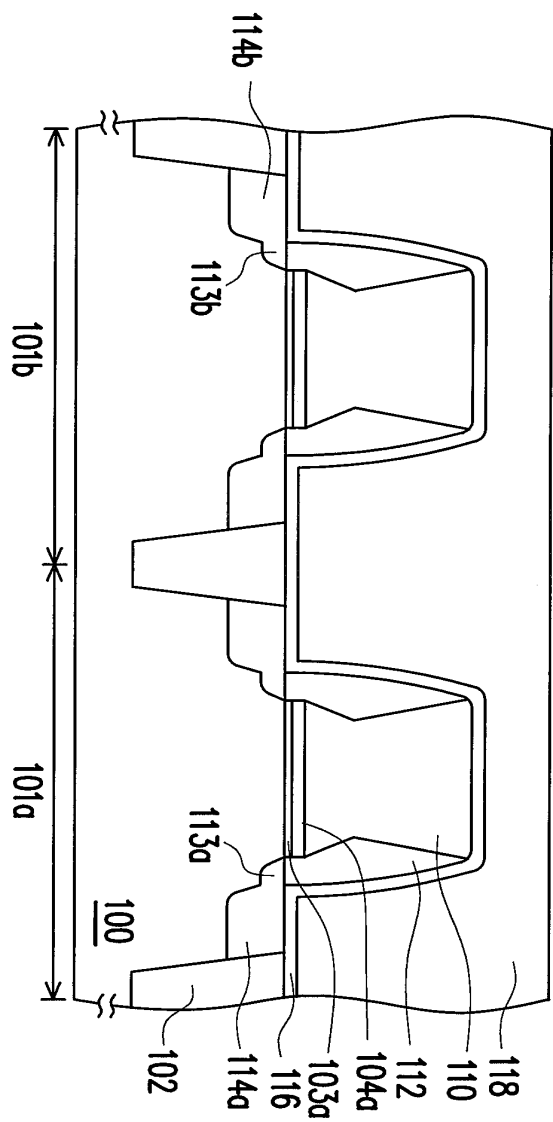


FIG. 1C

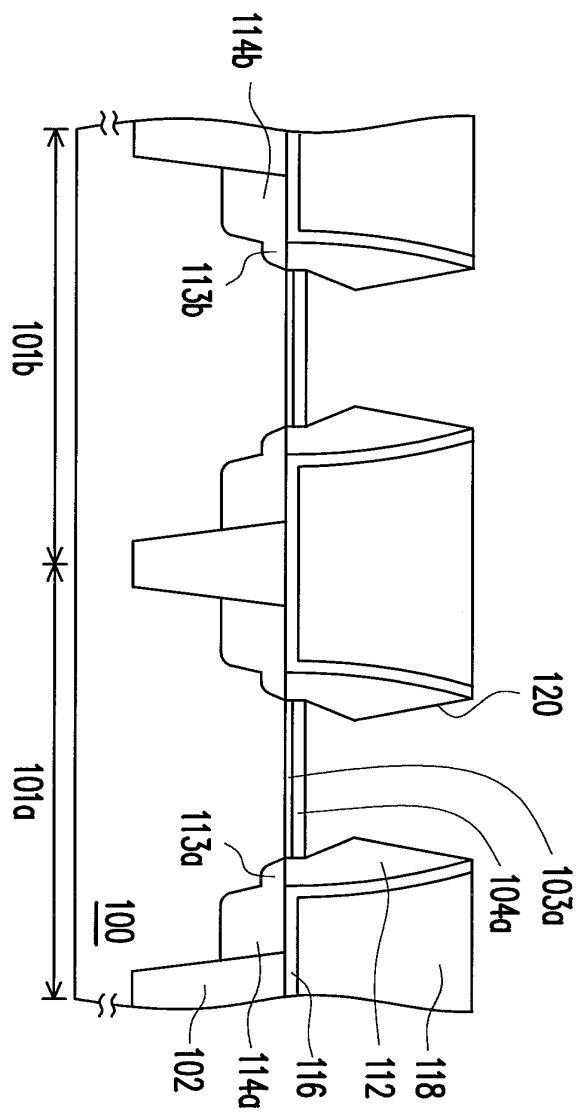


FIG. 1D



FIG. 1E

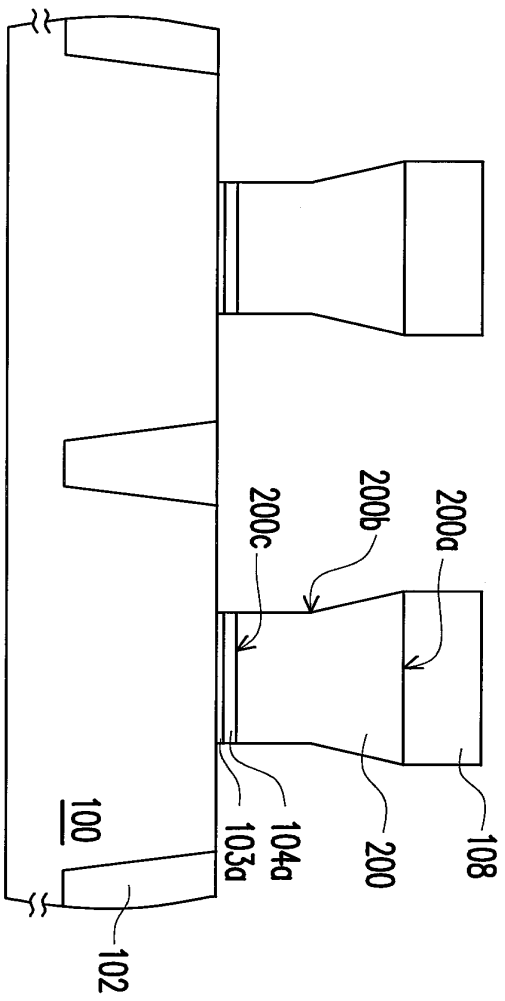


FIG. 2

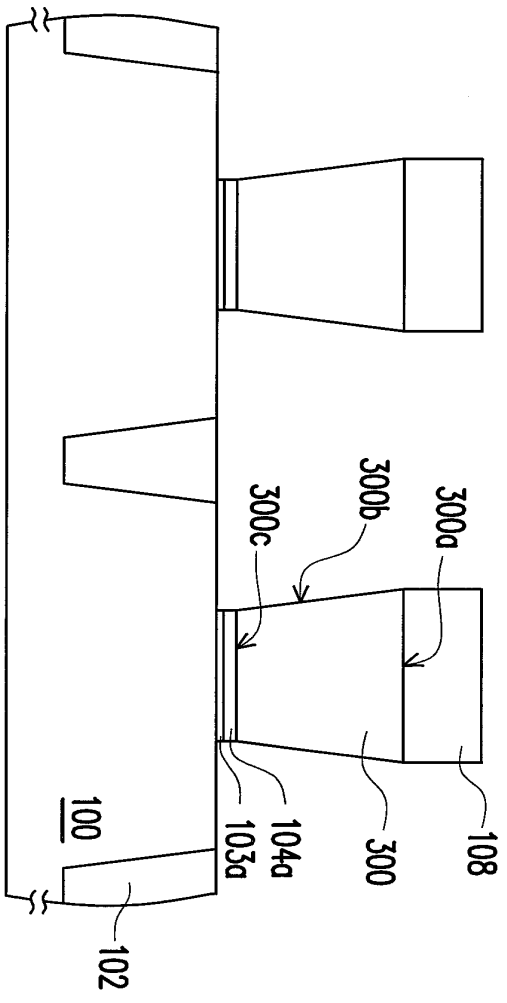


FIG. 3



FIG. 4

Electronic Acknowledgement Receipt	
EFS ID:	6192695
Application Number:	12572498
International Application Number:	
Confirmation Number:	4019
Title of Invention:	SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME
First Named Inventor/Applicant Name:	CHUN-HSIEN LIN
Customer Number:	23900
Filer:	Jiawei Huang/Michelle Chang
Filer Authorized By:	Jiawei Huang
Attorney Docket Number:	JCLA31951
Receipt Date:	02-OCT-2009
Filing Date:	
Time Stamp:	13:52:00
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	\$1090
RAM confirmation Number	101
Deposit Account	500710
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees)	

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Application Data Sheet	31951_ADS_Form.pdf	838098	no	4
			e10453d350504c11492a74f5f4386823de727e9f		
Warnings:					
Information:					
2	Oath or Declaration filed	31951_DECLARATION.pdf	94773	no	3
			df08fb51b6b3a1690801e171838885b7c2fe0ba3		
Warnings:					
Information:					
3	Specification	31951_Specification.pdf	1055821	no	33
			c2e465095fe3f264e8fb3fd0fca262fd428efa7		
Warnings:					
Information:					
4	Information Disclosure Statement (IDS) Filed (SB/08)	31951_IDS_Form.pdf	573337	no	4
			f97b998279ea4f3486f9842bd7ae316babe033a		
Warnings:					
Information:					
5	Fee Worksheet (PTO-875)	fee-info.pdf	32975	no	2
			eff5de81e253fbdaf41772a79ec13f552acbd896		
Warnings:					
Information:					
Total Files Size (in bytes):			2595004		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					

Filing Date: 10/02/09

Approved for use through 7/31/2006. OMB 0651-0032

U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875					Application or Docket Number 12/572,498	
APPLICATION AS FILED – PART I						
(Column 1)		(Column 2)		SMALL ENTITY		OR
OTHER THAN SMALL ENTITY						
FOR	NUMBER FILED	NUMBER EXTRA	RATE (\$)	FEE (\$)	RATE (\$)	FEE (\$)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A		N/A	330
SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A		N/A	540
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A		N/A	220
TOTAL CLAIMS (37 CFR 1.16(i))	20	minus 20 =	x\$26		x\$52	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	2	minus 3 = *	x\$110		x\$220	
APPLICATION SIZE FEE (37 CFR 1.16(s))			If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$260 (\$130 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR			
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))			195		390	
			TOTAL		TOTAL	1090
* If the difference in column 1 is less than zero, enter "0" in column 2.						
APPLICATION AS AMENDED – PART II						
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY
OTHER THAN SMALL ENTITY						OR
AMENDMENT A	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	RATE (\$)
	Total (37 CFR 1.16(i))	Minus **	=	X =		X =
	Independent (37 CFR 1.16(h))	Minus ***	=	X =		X =
	Application Size Fee (37 CFR 1.16(s))			N/A		N/A
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))			TOTAL ADD'T FEE		TOTAL ADD'T FEE
AMENDMENT B	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	RATE (\$)
	Total (37 CFR 1.16(i))	Minus **	=	X =		X =
	Independent (37 CFR 1.16(h))	Minus ***	=	X =		X =
	Application Size Fee (37 CFR 1.16(s))			N/A		N/A
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))			TOTAL ADD'T FEE		TOTAL ADD'T FEE
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.						

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.



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United States Patent and Trademark Office
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	TOT CLAIMS	IND CLAIMS
12/572,498	10/02/2009	2812	1090	JCLA31951	20	2

CONFIRMATION NO. 4019

23900
J C PATENTS
4 VENTURE, SUITE 250
IRVINE, CA 92618

FILING RECEIPT



OC000000038305430

Date Mailed: 10/21/2009

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Applicant(s)

Chun-Hsien Lin, Tainan County, TAIWAN;

Assignment For Published Patent Application

UNITED MICROELECTRONICS CORP., Hsinchu, TAIWAN

Power of Attorney: The patent practitioners associated with Customer Number 23900

Domestic Priority data as claimed by applicant

Foreign Applications

If Required, Foreign Filing License Granted: 10/15/2009

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 12/572,498**

Projected Publication Date: 04/07/2011

Non-Publication Request: No

Early Publication Request: No

Title

SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME

Preliminary Class

438

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at <http://www.uspto.gov/web/offices/pac/doc/general/index.html>.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, <http://www.stopfakes.gov>. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4158).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

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NOT GRANTED

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
12/572,498	10/02/2009	Chun-Hsien Lin	JCLA31951

CONFIRMATION NO. 4019

POA ACCEPTANCE LETTER

23900
J C PATENTS
4 VENTURE, SUITE 250
IRVINE, CA 92618



Date Mailed: 10/21/2009

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 10/02/2009.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

/bpham/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

PATENT

Docket No. JCLA31951

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of : CHUN-HSIEN LIN et al.
Application No. : 12/572,498
Filed : October 02,2009
For : SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING
THE SAME

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Enclosed is a form PTO-1449 listing (2) reference(s) that are also attached. Applicants submit the reference(s) in compliance with their duty of disclosure pursuant to 37 CFR §1.56 and 1.97. The Examiner is requested to make the citation(s) of official record.

This IDS is being submitted before first Office Action. Thus, no fee is due. However, if a first Office Action has been sent, the Commissioner is authorized to charge any necessary fee in connection with the submission of the IDS to Account No. 50-0710 (Order No. JCLA31951).

The submission of the references should not be interpreted as admitting them as prior art.

Respectfully submitted,

Dated: November 30, 2009

By: /JIAWEI HUANG/
Jiawei Huang
Registration No. 43,330

Correspondence Address:
J.C. Patents
4 Venture, Suite 250
Irvine, California 92618
Tel: (949) 660-0761

FORM PTO-1449 U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT	ATTY. DOCKET NO.: JCLA31951	APPLICATION No.: 12/572,498
	APPLICANT: CHUN-HSIEN LIN et al.	
	FILING DATE: October 02, 2009	GROUP:

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (IF APPROPRIATE)

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	PUBLICATION DATE	COUNTRY	CLASS	SUBCLASS	T

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or county where published.	T
		H. SEIDEL et al., "Anisotropic Etching of Crystalline Silicon in Alkaline Solutions: I. Orientation Dependence and Behavior of Passivation Layers" Journal of the Electrochemical Society, Vol. 37, No. 11, November 1990, pp 3612-3626	✓
		H. SEIDEL et al., "Anisotropic Etching of Crystalline Silicon in Alkaline Solutions: II. Influence of Dopants" Journal of the Electrochemical Society, Vol. 37, No. 11, November 1990, pp 3626-3632	✓

EXAMINER	DATE CONSIDERED
----------	-----------------

EXAMINER: INITIAL IF CITATION CONSIDERED, WHETHER OR NOT CITATION IS IN CONFORMANCE WITH MPEP 609; DRAW LINE THROUGH CITATION IF NOT IN CONFORMANCE AND NOT CONSIDERED. INCLUDE COPY OF THIS FORM WITH NEXT COMMUNICATION TO APPLICANT.

Electronic Acknowledgement Receipt	
EFS ID:	6543445
Application Number:	12572498
International Application Number:	
Confirmation Number:	4019
Title of Invention:	SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME
First Named Inventor/Applicant Name:	Chun-Hsien Lin
Customer Number:	23900
Filer:	Jiawei Huang/Michelle Chang
Filer Authorized By:	Jiawei Huang
Attorney Docket Number:	JCLA31951
Receipt Date:	30-NOV-2009
Filing Date:	02-OCT-2009
Time Stamp:	19:54:10
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal Letter	31951_IDS.pdf	49010 c43ea185b4c056bb0482b88c982b5aa7edd a2785	no	2

Warnings:

Information:

2	NPL Documents	31951_IDS_NPL-Seidel-1.pdf	3342596 84239e81f3933f07f9bd6e530f7a310bb1968f0e	no	15
Warnings:					
Information:					
3	NPL Documents	31951_IDS_NPL-Seidel-2.pdf	1222994 f0d3c4892901577ef09cc3e7d6a0d6178e69a2c	no	7
Warnings:					
Information:					
Total Files Size (in bytes):			4614600		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					



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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
12/572,498	10/02/2009	Chun-Hsien Lin	JCLA31951

CONFIRMATION NO. 4019

23900
J C PATENTS
4 VENTURE, SUITE 250
IRVINE, CA 92618

PUBLICATION NOTICE



OC000000047006255

Title:SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME

Publication No.US-2011-0079854-A1

Publication Date:04/07/2011

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently <http://www.uspto.gov/patft/>.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Office of Public Records. The Office of Public Records can be reached by telephone at (703) 308-9726 or (800) 972-6382, by facsimile at (703) 305-8759, by mail addressed to the United States Patent and Trademark Office, Office of Public Records, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently <http://pair.uspto.gov/>. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 1-866-217-9197.

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

POWER OF ATTORNEY TO PROSECUTE APPLICATIONS BEFORE THE USPTO

I hereby revoke all previous powers of attorney given in the application identified in the attached statement under 37 CFR 3.73(b).

I hereby appoint:

☒ Practitioners associated with the Customer Number:

65358 WPAT., P. C.

OR

☐ Practitioner(s) named below (if more than ten patent practitioners are to be named, then a customer number must be used):

Name	Registration Number	Name	Registration Number

as attorney(s) or agent(s) to represent the undersigned before the United States Patent and Trademark Office (USPTO) in connection with any and all patent applications assigned globally to the undersigned according to the USPTO assignment records or assignment documents attached to this form in accordance with 37 CFR 3.73(b).

Please change the correspondence address for the application identified in the attached statement under 37 CFR 3.73(h) to:

☒ The address associated with Customer Number:

65358 WPAT., P. C.

OR

☐ Firm or Individual Name			
Address			
City	State	Zip	
Country			
Telephone	Email		

Assignee Name and Address:

UNITED MICROELECTRONICS CORP.
 NO. 3, LI-HSIN RD. II, SCIENCE-BASED INDUSTRIAL PARK, HSINCHU, TAIWAN, R. O. C.

A copy of this form, together with a statement under 37 CFR 3.73(b) (Form PTO/SB/96 or equivalent) is required to be filed in each application in which this form is used. The statement under 37 CFR 3.73(b) may be completed by one of the practitioners appointed in this form if the appointed practitioner is authorized to act on behalf of the assignee, and must identify the application in which this Power of Attorney is to be filed.

SIGNATURE of Assignee of Record

The individual whose signature and title is supplied below is authorized to act on behalf of the assignee

Signature		Date	2011.04.13
Name	Yu-Tai Tsai	Telephone	
Title	UMC Patent Prosecution Dept / Intellectual Property Right Division Manager		

This collection of information is required by 37 CFR 1.31, 1.32 and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, reviewing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1480, Alexandria, VA 22313-1480. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

STATEMENT UNDER 37 CFR 3.73(b)

Applicant/Patent Owner: Chun-Hsien Lin

Application No./Patent No.: 12/572,498

Filed/Issue Date: 10-02-2009

Titled: SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME

UNITED MICROELECTRONICS CORP., a Corporation

(Name of Assignee)

(Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that it is:

1. ☒ the assignee of the entire right, title, and interest in;
2. ☐ an assignee of less than the entire right, title, and interest in
(The extent (by percentage) of its ownership interest is _____ %); or
3. ☐ the assignee of an undivided interest in the entirety of (a complete assignment from one of the joint inventors was made)

the patent application/patent identified above, by virtue of either:

- A. ☒ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel 023323, Frame 0944, or for which a copy therefore is attached.

OR

- B. ☐ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

2. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

3. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

☐ Additional documents in the chain of title are listed on a supplemental sheet(s).

- ☒ As required by 37 CFR 3.73(b)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

/Justin King/

Signature

05/12/2011

Date

Justin King

Printed or Typed Name

Attorney on Record

Title

This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt	
EFS ID:	10077588
Application Number:	12572498
International Application Number:	
Confirmation Number:	4019
Title of Invention:	SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME
First Named Inventor/Applicant Name:	Chun-Hsien Lin
Customer Number:	23900
Filer:	Anthony King/Justin King
Filer Authorized By:	Anthony King
Attorney Docket Number:	JCLA31951
Receipt Date:	12-MAY-2011
Filing Date:	02-OCT-2009
Time Stamp:	15:22:21
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Power of Attorney	Form80.pdf	1097679	no	2
			e9ac26daee1d826ca0446f0da5f9b15c37a4c50		

Warnings:

Information:

2	Power of Attorney	sb0096.pdf	423112 4a01da0479aae880905bf98d144fbc560fb141cb	no	2
Warnings:					
Information:					
Total Files Size (in bytes):				1520791	
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
12/572,498	10/02/2009	Chun-Hsien Lin	JCLA31951

CONFIRMATION NO. 4019

POA ACCEPTANCE LETTER

65358
WPAT, PC
INTELLECTUAL PROPERTY ATTORNEYS
7225 BEVERLY ST.
ANNANDALE, VA 22003



Date Mailed: 05/23/2011

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 05/12/2011.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

/erimando/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
12/572,498	10/02/2009	Chun-Hsien Lin	JCLA31951

23900
J C PATENTS
4 VENTURE, SUITE 250
IRVINE, CA 92618

CONFIRMATION NO. 4019
POWER OF ATTORNEY NOTICE



Date Mailed: 05/23/2011

NOTICE REGARDING CHANGE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 05/12/2011.

- The Power of Attorney to you in this application has been revoked by the assignee who has intervened as provided by 37 CFR 3.71. Future correspondence will be mailed to the new address of record(37 CFR 1.33).

/erimando/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
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Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/572,498	10/02/2009	Chun-Hsien Lin	66007-405	4019
65358 7590 07/01/2011 WPAT, PC INTELLECTUAL PROPERTY ATTORNEYS 7225 BEVERLY ST. ANNANDALE, VA 22003			EXAMINER SOWARD, IDA M	
			ART UNIT 2822	PAPER NUMBER
			MAIL DATE 07/01/2011	DELIVERY MODE PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	12/572,498	LIN, CHUN-HSIEN	
	Examiner	Art Unit	
	IDA M. SOWARD	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 30Days MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on 02 October 2009.

2a) ☐ This action is **FINAL**. 2b) ☐ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) 1-20 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☐ Claim(s) _____ is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☒ Claim(s) 1-20 are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☐ All b) ☐ Some * c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.

2. ☐ Certified copies of the priority documents have been received in Application No. _____.

3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892) 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.	4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____. 5) ☐ Notice of Informal Patent Application 6) ☐ Other: _____.
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DETAILED ACTION

Election/Restrictions

Restriction to one of the following inventions is required under 35 U.S.C. 121:

- I. Claims 15-20, drawn to a semiconductor device, classified in class 257, subclass 365.
- II. Claims 1-14, drawn to a method of fabricating a semiconductor device, classified in class 438, subclass 284.

The inventions are distinct, each from the other because of the following reasons:

Inventions I and II are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make another and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f)). Unpatentability of the Group I invention would not necessarily imply unpatentability of the Group II invention, since the device of the Group I invention could be made by a process materially different from those/that of the Group II invention. In the instant case, the plurality of trenches could have been formed without using dummy patterns to achieve the same structure.

Restriction for examination purposes as indicated is proper because all these inventions listed in this action are independent or distinct for the reasons given above and there would be a serious search and/or examination burden if restriction were not required because at least the following reason(s) apply: the inventions have acquired a

separate status in the art in view of their different classification and would require a different knowledge base and a different thought processes for a search.

Applicant is advised that the reply to this requirement to be complete must include (i) an election of a invention to be examined even though the requirement may be traversed (37 CFR 1.143) and (ii) identification of the claims encompassing the elected invention.

The election of an invention may be made with or without traverse. To reserve a right to petition, the election must be made with traverse. If the reply does not distinctly and specifically point out supposed errors in the restriction requirement, the election shall be treated as an election without traverse. Traversal must be presented at the time of election in order to be considered timely. Failure to timely traverse the requirement will result in the loss of right to petition under 37 CFR 1.144. If claims are added after the election, applicant must indicate which of these claims are readable upon the elected invention.

Should applicant traverse on the ground that the inventions are not patentably distinct, applicant should submit evidence or identify such evidence now of record showing the inventions to be obvious variants or clearly admit on the record that this is the case. In either instance, if the examiner finds one of the inventions unpatentable over the prior art, the evidence or admission may be used in a rejection under 35 U.S.C. 103(a) of the other invention.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to IDA M. SOWARD whose telephone number is (571)272-

1845. The examiner can normally be reached on Monday - Thursday 6:00am to 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra V. Smith can be reached on 571-272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

IMS
June 29, 2011
/IDA M SOWARD/
Primary Examiner, Art Unit 2822

<i>Index of Claims</i> 	Application/Control No. 12572498	Applicant(s)/Patent Under Reexamination LIN, CHUN-HSIEN
	Examiner IDA M SOWARD	Art Unit 2822

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant											☐ CPA											☐ T.D.											☐ R.1.47										
CLAIM			DATE																																								
Final	Original	06/29/2011																																									
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	2	÷																																									
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Applicant: CHUN-HSIEN LIN
Application No.: 12/572,498

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
P.O. BOX 1450
ALEXANDRIA, VA 22313-1450**

Appl No.: 12/572,498
Applicant: CHUN-HSIEN LIN
Filing Date: 10/2/2009
Art Unit: 2822
Examiner: SOWARD, IDA M
Attorney Docket No.: 66007-405

Title: SEMICONDUCTOR DEVICE AND
METHOD FOR FABRICATING THE
SAME

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE TO ELECTION/RESTRICTION REQUIREMENT

Sir:

This paper responds to the Office Action dated July 01, 2011. Please amend the above-identified application as follows:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks/Arguments begin on page 6 of this paper.

Amendments to the Claims

This listing of claims replaces all prior versions, and listings, of claims in the application:

WHAT IS CLAIMED IS:

1. (Withdrawn) A method of fabricating a semiconductor device, comprising:

forming a polysilicon layer on a substrate;

doping an N-type dopant into the polysilicon layer;

removing a portion of the polysilicon layer to form a plurality of dummy patterns, each of the plurality of dummy patterns having a top, a bottom, and a neck arranged between the top and the bottom, wherein a width of the neck is narrower than a width of the top;

forming a dielectric layer on the substrate, the dielectric layer covering the substrate disposed between two adjacent dummy patterns and exposing the top of each dummy pattern;

removing the plurality of dummy patterns to form a plurality of trenches in the dielectric layer; and

forming a plurality of gate structures in the trenches respectively.
2. (Withdrawn) The method of fabricating the semiconductor device as claimed in claim 1, wherein a depth of the polysilicon layer doped with a highest concentration of the N-type dopant and the neck are substantially located on the same horizontal level of height.
3. (Withdrawn) The method of fabricating the semiconductor device as claimed in claim 1, wherein a concentration of the N-type dopant doped in a bottom of the polysilicon layer is greater than a concentration of the N-type dopant doped in a top of the polysilicon layer.

4. (Withdrawn) The method of fabricating the semiconductor device as claimed in claim 1, wherein a concentration of the N-type dopant doped increases gradually from a top to a bottom of the polysilicon layer.

5. (Withdrawn) The method of fabricating the semiconductor device as claimed in claim 1, further comprising doping another N-type dopant into the polysilicon layer.

6. (Withdrawn) The method of fabricating the semiconductor device as claimed in claim 1, wherein the N-type dopant is phosphorus (P), antimony (Sb), or arsenic (As).

7. (Withdrawn) The method of fabricating the semiconductor device as claimed in claim 1, wherein when the N-type dopant is phosphorus, an energy for doping is within a range of 1 Kev to 20 KeV and a dose for doping is within a range of $1\text{E}15\text{ cm}^{-2}$ to $8\text{E}15\text{ cm}^{-2}$.

8. (Withdrawn) The method of fabricating the semiconductor device as claimed in claim 1, wherein the top and the neck have a first height therebetween, the neck and the bottom have a second height therebetween, and a ratio of the first height to the second height is substantially 2:1.

9. (Withdrawn) The method of fabricating the semiconductor device as claimed in claim 1, wherein an included angle between a sidewall of a top of each of the plurality of trenches and a surface of the dielectric layer is larger than 90° .

10. (Withdrawn) The method of fabricating the semiconductor device as claimed in claim 1, wherein the step of removing a portion of the polysilicon layer comprises performing an etching process using a halogen-containing reactant.

11. (Withdrawn) The method of fabricating the semiconductor device as claimed in claim 1, before removing the plurality of dummy patterns, further

comprising forming a high dielectric constant layer between the substrate and each of the plurality of dummy patterns.

12. (Withdrawn) The method of fabricating the semiconductor device as claimed in claim 1, further comprising forming a source/drain region in the substrate at respective sides of the gate structure.

13. (Withdrawn) The method of fabricating the semiconductor device as claimed in claim 12, wherein the step of forming the source/drain region comprises performing an ion implantation process or a selective epitaxy growth process.

14. (Withdrawn) The method of fabricating the semiconductor device as claimed in claim 1, after forming the plurality of dummy patterns and before forming the dielectric layer, further comprising forming a spacer on a sidewall of each of the plurality of dummy patterns.

15. (Original) A semiconductor device, comprising:

a substrate, disposed with a dielectric layer thereon, wherein a trench is disposed in the dielectric layer;

a gate structure, located in the trench and comprising a high dielectric constant layer, a work function metal layer, and a metal layer sequentially disposed on the substrate; and

a source/drain region, disposed in the substrate at respective sides of the gate structure,

wherein the trench comprises a top, a bottom, and a neck arranged between the top and the bottom, a width of the neck is narrower than a width of the top, and the width of the neck is narrower than or equal to a width of the bottom.

16. (Original) The semiconductor device as claimed in claim 15, wherein the top and the neck have a first height therebetween, the neck and the bottom have a

second height therebetween, and a ratio of the first height to the second height is substantially 2:1.

17. (Original) The semiconductor device as claimed in claim 15, wherein an included angle between a sidewall of the top of each of the plurality of trenches and a surface of the dielectric layer is larger than 90° .

18. (Original) The semiconductor device as claimed in claim 15, further comprising an insulation layer disposed between the substrate and the high dielectric constant layer.

19. (Original) The semiconductor device as claimed in claim 15, wherein the source/drain region is a doped region or an epitaxial layer.

20. (Original) The semiconductor device as claimed in claim 15, further comprising a spacer disposed on a sidewall of the gate structure.

Remarks

The Office considered the claims of the present application to be directed to patentably distinct inventions. Specifically, the Examiner required restriction to one of the two inventions:

I. Claims 15-20 drawn to a semiconductor device, classified in class 257, subclass 365.

II. Claims 1-14 drawn to a method of fabricating a semiconductor device, classified in class 438, subclass 284.

The applicant hereby makes a provisional election, to prosecute the invention of

I. Claims 15-20 drawn to a semiconductor device, classified in class 257, subclass 365.

The applicant further withdraws claims 1-14.

The election of the group of claims is being made solely to comply with the examiner's requirement. The right to file divisional application on non-elected subject matter is reserved.

Request For Allowance

Claims 1-20 are pending in this application. The applicant hereby withdraws the claims not selected. The applicant hereby respectfully requests allowance of claims elected.

Respectfully submitted,
WPAT, P.C.

By ___/Justin I. King/___
Justin I. King
Registration No. 50,464

July 07, 2011
WPAT, P.C.
Intellectual Property Attorneys
1940 Duke Street, Suite 200
Alexandria, VA 22314
Telephone (703) 684-4411

Electronic Acknowledgement Receipt	
EFS ID:	10490241
Application Number:	12572498
International Application Number:	
Confirmation Number:	4019
Title of Invention:	SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME
First Named Inventor/Applicant Name:	Chun-Hsien Lin
Customer Number:	65358
Filer:	Anthony King/Justin King
Filer Authorized By:	Anthony King
Attorney Docket Number:	66007-405
Receipt Date:	11-JUL-2011
Filing Date:	02-OCT-2009
Time Stamp:	15:25:39
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Response to Election / Restriction Filed	Invention_Species.pdf	23902 5d77532249fea82f95a2e35175a6de6e3418bbbc	no	7

Warnings:

Information:

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		12572498	
	Filing Date		2009-10-02	
	First Named Inventor	Chun-Hsien Lin		
	Art Unit	2822		
	Examiner Name	SOWARD, IDA M		
	Attorney Docket Number	66007-405		

U.S. PATENTS							Remove	
Examiner Initial*	Cite No	Patent Number	Kind Code ¹	Issue Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear		
	1	7208361		2007-04-24	Shah , et al.			
If you wish to add additional U.S. Patent citation information please click the Add button.							Add	
U.S. PATENT APPLICATION PUBLICATIONS							Remove	
Examiner Initial*	Cite No	Publication Number	Kind Code ¹	Publication Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear		
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If you wish to add additional U.S. Published Application citation information please click the Add button.							Add	
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Examiner Initial*	Cite No	Foreign Document Number ³	Country Code ² j	Kind Code ⁴	Publication Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear	T ⁵
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If you wish to add additional Foreign Patent Document citation information please click the Add button								Add
NON-PATENT LITERATURE DOCUMENTS							Remove	
Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.						T ⁵

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		12572498
	Filing Date		2009-10-02
	First Named Inventor	Chun-Hsien Lin	
	Art Unit	2822	
	Examiner Name	SOWARD, IDA M	
	Attorney Docket Number	66007-405	

	1		☐
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If you wish to add additional non-patent literature document citation information please click the Add button **Add**

EXAMINER SIGNATURE

Examiner Signature		Date Considered	
--------------------	--	-----------------	--

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. ² Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). ³ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁴ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁵ Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	12572498
	Filing Date	2009-10-02
	First Named Inventor	Chun-Hsien Lin
	Art Unit	2822
	Examiner Name	SOWARD, IDA M
	Attorney Docket Number	66007-405

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ None

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Justin King/	Date (YYYY-MM-DD)	2011-07-11
Name/Print	Justin King	Registration Number	50,464

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt	
EFS ID:	10490283
Application Number:	12572498
International Application Number:	
Confirmation Number:	4019
Title of Invention:	SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME
First Named Inventor/Applicant Name:	Chun-Hsien Lin
Customer Number:	65358
Filer:	Anthony King/Justin King
Filer Authorized By:	Anthony King
Attorney Docket Number:	66007-405
Receipt Date:	11-JUL-2011
Filing Date:	02-OCT-2009
Time Stamp:	15:27:43
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	SB08.pdf	612358 8b21097dcc40fcd4e758bae341175ad3c5057a99	no	4

Warnings:

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New International Application Filed with the USPTO as a Receiving Office

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Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875					Application or Docket Number 12/572,498		Filing Date 10/02/2009		☐ To be Mailed	
APPLICATION AS FILED – PART I										
(Column 1)			(Column 2)		SMALL ENTITY ☐ OR		OTHER THAN SMALL ENTITY			
FOR	NUMBER FILED	NUMBER EXTRA	RATE (\$)	FEE (\$)	OR	RATE (\$)	FEE (\$)			
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A				
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A				
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A				
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X \$ =		OR	X \$ =				
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X \$ =			X \$ =				
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$250 (\$125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).									
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))										
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL				
APPLICATION AS AMENDED – PART II										
(Column 1)			(Column 2)		(Column 3)		SMALL ENTITY OR		OTHER THAN SMALL ENTITY	
AMENDMENT	07/11/2011	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	OR	RATE (\$)	ADDITIONAL FEE (\$)	
	Total (37 CFR 1.16(i))	* 4	Minus	** 20	= 0	X \$ =		OR	X \$2= 0	
	Independent (37 CFR 1.16(h))	* 1	Minus	***3	= 0	X \$ =		OR	X \$220= 0	
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))									
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	0	
AMENDMENT	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	OR	RATE (\$)	ADDITIONAL FEE (\$)		
	Total (37 CFR 1.16(i))	*	Minus	**	=	X \$ =		OR	X \$ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X \$ =		OR	X \$ =	
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))									
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE		
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.										
Legal Instrument Examiner: /LAMONT MCLAUCHLIN/										

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

65358 7590 08/12/2011
WPAT, PC
INTELLECTUAL PROPERTY ATTORNEYS
7225 BEVERLY ST.
ANNANDALE, VA 22003

EXAMINER

SOWARD, IDA M

ART UNIT

PAPER NUMBER

2822

DATE MAILED: 08/12/2011

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/572,498	10/02/2009	Chun-Hsien Lin	66007-405	4019

TITLE OF INVENTION: SEMICONDUCTOR DEVICE WITH TRENCH OF VARIOUS WIDTHS

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1510	\$300	\$0	\$1810	11/14/2011

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

**Complete and send this form, together with applicable fee(s), to: Mail Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885**

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

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65358 7590 08/12/2011
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INTELLECTUAL PROPERTY ATTORNEYS
7225 BEVERLY ST.
ANNANDALE, VA 22003

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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12/572,498	10/02/2009	Chun-Hsien Lin	66007-405	4019
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TITLE OF INVENTION: SEMICONDUCTOR DEVICE WITH TRENCH OF VARIOUS WIDTHS

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1510	\$300	\$0	\$1810	11/14/2011

EXAMINER	ART UNIT	CLASS-SUBCLASS
SOWARD, IDA M	2822	257-407000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

- (1) the names of up to 3 registered patent attorneys or agents OR, alternatively, 1 _____
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☐ Issue Fee
☐ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
☐ Payment by credit card. Form PTO-2038 is attached.
☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____

Date _____

Typed or printed name _____

Registration No. _____

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UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/572,498	10/02/2009	Chun-Hsien Lin	66007-405	4019
65358	7590	08/12/2011	EXAMINER	
WPAT, PC INTELLECTUAL PROPERTY ATTORNEYS 7225 BEVERLY ST. ANNANDALE, VA 22003			SOWARD, IDA M	
			ART UNIT	PAPER NUMBER
			2822	

DATE MAILED: 08/12/2011

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 211 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 211 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

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8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

DETAILED ACTION

This Office Action is in response to the election filed July 11, 2011.

Election/Restrictions

Applicant's election of Group I, claims 15-20 in the reply filed on July 11, 2011 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Justin I. King on August 10, 2011.

The application has been amended as follows:

1. Claims 1-14, non-elected without traverse, have been cancelled; and
2. TITLE

Semiconductor device with trench of various widths.

Allowable Subject Matter

Claims 15-20 are allowed.

The following is an examiner's statement of reasons for allowance: The prior art of record does not disclose, make obvious, or otherwise suggest the structure of the applicant's together with the other limitations of the independent claims, such as "a gate structure, located in the trench and comprising a high dielectric constant layer, a work function metal layer, and a metal layer sequentially disposed on the substrate, wherein the trench comprises a top, a bottom, and a neck arranged between the top and the bottom, a width of the neck is narrower than a width of the top, and the width of the neck is narrower than or equal to a width of the bottom".

The dependent claims being further limiting and definite are also allowable.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The following patents are cited to further show the state of the art with respect to semiconductor devices:

Brask et al. (US 2009/0218603 A1)	Chien et al. (US 2011/0070702 A1)
Fukasaku (US 7,939,895 B2)	Hattendorf et al. (US 2007/0126067 A1)
Jang (5,834,816)	Karlsson et al. (5,879,975)
Kuroi et al. (US 6,661,066 B2)	Lee et al. (5,840,611)
Nissa (US 6,674,137 B2)	Owyang et al. (6,060,375)
Sato (5,685,950)	Shimizu (JP 08055863 A)
Shinbori et al. (US 2009/0189219 A1)	Wu et al. (US 7,749,911 B2).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to IDA M. SOWARD whose telephone number is (571)272-1845. The examiner can normally be reached on Monday - Thursday 6:00am to 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra V. Smith can be reached on 571-272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

IMS
August 10, 2011
/IDA M SOWARD/
Primary Examiner, Art Unit 2822

Notice of References Cited	Application/Control No. 12/572,498		Applicant(s)/Patent Under Reexamination LIN, CHUN-HSIEN	
	Examiner IDA M. SOWARD		Art Unit 2822	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-2009/0218603	09-2009	Brask et al.	257/255
*	B	US-2011/0070702	03-2011	Chien et al.	438/211
*	C	US-7,939,895	05-2011	Fukasaku, Katsuhiko	257/369
*	D	US-2007/0126067	06-2007	Hattendorf et al.	257/412
*	E	US-5,834,816	11-1998	Jang, Seong Jin	257/382
*	F	US-5,879,975	03-1999	Karlsson et al.	438/162
*	G	US-6,661,066	12-2003	Kuroi et al.	257/412
*	H	US-5,840,611	11-1998	Lee et al.	438/307
*	I	US-6,674,137	01-2004	Nissa, Mitsuo	257/408
*	J	US-6,060,375	05-2000	Owyang et al.	438/585
*	K	US-5,685,950	11-1997	Sato, Junichi	438/713
*	L	US-2009/0189219	07-2009	SHINBORI et al.	257/334
*	M	US-7,749,911	07-2010	Wu et al.	438/701

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N	JP 08055863 A	02-1996	Japan	SHIMIZU, KEIJI	
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
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	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
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BIB DATA SHEET

CONFIRMATION NO. 4019

SERIAL NUMBER 12/572,498	FILING or 371(c) DATE 10/02/2009 RULE	CLASS 257	GROUP ART UNIT 2822	ATTORNEY DOCKET NO. 66007-405		
APPLICANTS Chun-Hsien Lin, Tainan County, TAIWAN; ** CONTINUING DATA ***** ** FOREIGN APPLICATIONS ***** ** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** 10/15/2009						
Foreign Priority claimed ☐ Yes ☒ No 35 USC 119(a-d) conditions met ☐ Yes ☒ No Verified and Acknowledged <u>/IDA M SOWARD/</u> Examiner's Signature		☐ Met after Allowance IMS Initials	STATE OR COUNTRY TAIWAN	SHEETS DRAWINGS 8	TOTAL CLAIMS 20	INDEPENDENT CLAIMS 2
ADDRESS WPAT, PC INTELLECTUAL PROPERTY ATTORNEYS 7225 BEVERLY ST. ANNANDALE, VA 22003 UNITED STATES						
TITLE Semiconductor device with trench of various widths						
FILING FEE RECEIVED 1090	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:	☐ All Fees				
		☐ 1.16 Fees (Filing)				
		☐ 1.17 Fees (Processing Ext. of time)				
		☐ 1.18 Fees (Issue)				
		☐ Other _____				
		☐ Credit				

Receipt date: 07/11/2011

Doc code: IDS

Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (01-10)

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		12572498	
	Filing Date		2009-10-02	
	First Named Inventor	Chun-Hsien Lin		
	Art Unit	2822		
	Examiner Name	SOWARD, IDA M		
	Attorney Docket Number	66007-405		

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	1	7208361		2007-04-24	Shah , et al.	

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Receipt date: 07/11/2011 INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		12572498
	Filing Date		2009-10-02
	First Named Inventor	Chun-Hsien Lin	
	Art Unit	2822	
	Examiner Name	SOWARD, IDA M	
	Attorney Docket Number	66007-405	

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EXAMINER SIGNATURE

Examiner Signature	/Ida Soward/	Date Considered	08/04/2011
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¹ See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. ² Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). ³ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁴ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁵ Applicant is to place a check mark here if English language translation is attached.

<i>Search Notes</i> 	Application/Control No. 12572498	Applicant(s)/Patent Under Reexamination LIN, CHUN-HSIEN
	Examiner IDA M SOWARD	Art Unit 2822

SEARCHED			
Class	Subclass	Date	Examiner
257	310, 407, E29.15, E29.16	8/3/2011	IMS

SEARCH NOTES		
Search Notes	Date	Examiner
EAST (See Search History Printout)	8/3/2011	IMS

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner
	See Interference Search Printout	8/3/2011	IMS

	/IDA M SOWARD/ Primary Examiner.Art Unit 2822
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Receipt date: 11/30/2009

FORM PTO-1449 U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT	ATTY. DOCKET NO.: JCLA31951	APPLICATION No.: 12/572,498
	APPLICANT: CHUN-HSIEN LIN et al.	
	FILING DATE: October 02, 2009	GROUP: 2822

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (IF APPROPRIATE)

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	PUBLICATION DATE	COUNTRY	CLASS	SUBCLASS	T

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or county where published.	T
		H. SEIDEL et al., "Anisotropic Etching of Crystalline Silicon in Alkaline Solutions: I. Orientation Dependence and Behavior of Passivation Layers" Journal of the Electrochemical Society, Vol. 37, No. 11, November 1990, pp 3612-3626	✓
		H. SEIDEL et al., "Anisotropic Etching of Crystalline Silicon in Alkaline Solutions: II. Influence of Dopants" Journal of the Electrochemical Society, Vol. 37, No. 11, November 1990, pp 3626-3632	✓

EXAMINER /Ida Soward/	DATE CONSIDERED 08/04/2011
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ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /I.S./

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	55	lin-chun-hsien.inv.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/08/03 14:02
L2	3	"7208361".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/08/03 14:02
L3	2960	257/310	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/08/03 14:55
L4	824	257/407	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/08/03 14:57
L5	45	257/e29.16	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/08/03 15:17
L6	21	257/e29.15	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/08/03 15:18
L7	113	(tapered or ((hourglass or hour \$1glass) adj shape\$1)) adj gate adj electrode	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/08/03 15:42

L8	0	(bone adj shape\$1) adj gate adj electrode	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/08/03 15:50
L9	0	(ntama adj shape\$1) adj gate adj electrode	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/08/03 15:53
L10	0	(nebula adj shape\$1) adj gate adj electrode	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/08/03 15:54
L11	0	(biconic adj shape\$1) near (gate adj electrode)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/08/03 15:56
L12	0	(biconic adj shape\$1) same (gate adj electrode)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/08/03 15:56
L13	25	(biconic adj shape\$1)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/08/03 15:56
L14	0	((((Figure adj (8 or eight)) or leminscate) adj shape\$1) adj gate adj electrode	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/08/03 16:02
L15	0	((((Figure adj (8 or eight)) or leminscate or infinity) adj shape \$1) same (gate adj electrode)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/08/03 16:02

L16	6	(inverted adj (sidewall or side\$1wall or side)) same (gate adj electrode)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/08/03 16:16
L17	268	((convex\$2 or concav \$3 or indent\$4 or tapered) adj (sidewall or side\$1wall or side)) same (gate adj electrode)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/08/03 16:19
L18	1	(bow adj tie adj shape \$1) same (gate adj electrode)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/08/03 16:22
L19	1	(bow adj tie) same (gate adj electrode)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/08/03 16:42
L20	0	((Figure adj (8 or eight)) or leminscate)) same (gate adj electrode)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/08/03 16:42
L21	140	((convex\$2 or concav \$3 or indent\$4 or tapered) adj (edge)) same (gate adj electrode)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/08/03 16:45
L22	0	(cinch\$2) same (gate adj electrode)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/08/03 16:52
L23	203	(work adj function adj metal adj (layer or film)) same (high adj dielectric adj constant adj (layer or film)) same (metal adj (layer or film))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/08/03 17:15

L24	7	(work adj function adj metal adj (layer or film)) same (high adj dielectric adj constant adj (layer or film)) same (metal adj (layer or film))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/08/03 17:20
L25	1	"20110070702".pn. and conductive	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/08/03 17:54

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L26	90	(tapered or ((hourglass or hour\$1glass) adj shape\$1)) adj gate adj electrode	US-PGPUB; USPAT; UPAD	OR	ON	2011/08/03 18:34
L27	0	(bone adj shape\$1) adj gate adj electrode	US-PGPUB; USPAT; UPAD	OR	ON	2011/08/03 18:34
L28	0	(ntama adj shape\$1) adj gate adj electrode	US-PGPUB; USPAT; UPAD	OR	ON	2011/08/03 18:34
L29	0	(nebula adj shape\$1) adj gate adj electrode	US-PGPUB; USPAT; UPAD	OR	ON	2011/08/03 18:34
L30	0	(biconic adj shape\$1) near (gate adj electrode)	US-PGPUB; USPAT; UPAD	OR	ON	2011/08/03 18:34
L31	0	(biconic adj shape\$1) same (gate adj electrode)	US-PGPUB; USPAT; UPAD	OR	ON	2011/08/03 18:34
L32	21	(biconic adj shape\$1)	US-PGPUB; USPAT; UPAD	OR	ON	2011/08/03 18:34
L33	0	((Figure adj ("8" or eight)) or leminscate) adj shape\$1) adj gate adj electrode	US-PGPUB; USPAT; UPAD	OR	ON	2011/08/03 18:34

L34	2	((Figure adj ("8" or eight)) or leminscate or infinity) adj shape\$1) same (gate adj electrode)	US-PGPUB; USPAT; UPAD	OR	ON	2011/08/03 18:34
L35	5	(inverted adj (sidewall or side\$1wall or side)) same (gate adj electrode)	US-PGPUB; USPAT; UPAD	OR	ON	2011/08/03 18:35
L36	217	((convex\$2 or concav\$3 or indent\$4 or tapered) adj (sidewall or side \$1wall or side)) same (gate adj electrode)	US-PGPUB; USPAT; UPAD	OR	ON	2011/08/03 18:35
L37	1	(bow adj tie adj shape \$1) same (gate adj electrode)	US-PGPUB; USPAT; UPAD	OR	ON	2011/08/03 18:35
L38	1	(bow adj tie) same (gate adj electrode)	US-PGPUB; USPAT; UPAD	OR	ON	2011/08/03 18:35
L39	5	((Figure adj ("8" or eight)) or leminscate)) same (gate adj electrode)	US-PGPUB; USPAT; UPAD	OR	ON	2011/08/03 18:35
L40	119	((convex\$2 or concav\$3 or indent\$4 or tapered) adj (edge)) same (gate adj electrode)	US-PGPUB; USPAT; UPAD	OR	ON	2011/08/03 18:35
L41	0	(cinch\$2) same (gate adj electrode)	US-PGPUB; USPAT; UPAD	OR	ON	2011/08/03 18:35
L42	170	(work adj function adj metal ad (layer or film)) same (high adj dielectric adj constant adj (layer or film)) same (metal adj (layer or film))	US-PGPUB; USPAT; UPAD	OR	ON	2011/08/03 18:35
L43	5	(work adj function adj metal adj (layer or film)) same (high adj dielectric adj constant adj (layer or film)) same (metal adj (layer or film))	US-PGPUB; USPAT; UPAD	OR	ON	2011/08/03 18:35
L44	1	"20110070702".pn. and conductive	US-PGPUB; USPAT; UPAD	OR	ON	2011/08/03 18:36

8/ 3/ 2011 6:54:06 PM

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<i>Index of Claims</i> 	Application/Control No. 12572498	Applicant(s)/Patent Under Reexamination LIN, CHUN-HSIEN
	Examiner IDA M SOWARD	Art Unit 2822

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☒ Claims renumbered in the same order as presented by applicant				☐ CPA		☐ T.D.		☐ R.1.47	
CLAIM		DATE							
Final	Original	06/29/2011	08/10/2011						
	1	÷	-						
	2	÷	-						
	3	÷	-						
	4	÷	-						
	5	÷	-						
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EXAMINER

SOWARD, IDA M

ART UNIT

PAPER NUMBER

2822

DATE MAILED: 08/12/2011

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/572,498	10/02/2009	Chun-Hsien Lin	66007-405	4019

TITLE OF INVENTION: SEMICONDUCTOR DEVICE WITH TRENCH OF VARIOUS WIDTHS

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1510	\$300	\$0	\$1810	11/14/2011

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: **Mail** **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

65358 7590 08/12/2011
 WPAT, PC
 INTELLECTUAL PROPERTY ATTORNEYS
 7225 BEVERLY ST.
 ANNANDALE, VA 22003

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

Justin King	(Depositor's name)
/Justin King/	(Signature)
11/07/2011	(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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12/572,498	10/02/2009	Chun-Hsien Lin	66007-405	4019
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TITLE OF INVENTION: SEMICONDUCTOR DEVICE WITH TRENCH OF VARIOUS WIDTHS

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1510	\$300	\$0	\$1810	11/14/2011

EXAMINER	ART UNIT	CLASS-SUBCLASS
SOWARD, IDA M	2822	257-407000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☒ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

- (1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
- (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 **WPAT, PC**
 2 **Justin King**
 3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

UNITED MICROELECTRONICS CORP.

HSINCHU, TAIWAN R.O.C.

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☒ Issue Fee
- ☒ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
- ☒ Payment by credit card. Form PTO-2038 is attached.
- ☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature /Justin King/

Date 11/07/2011

Typed or printed name Justin King

Registration No. 50464

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

"FEE ADDRESS" INDICATION FORM

Address to:
Mail Stop M Correspondence
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Fax to:
571-273-6500

- OR -

INSTRUCTIONS: The issue fee must have been paid for application(s) listed on this form. In addition, only an address represented by a Customer Number can be established as the fee address for maintenance fee purposes (hereafter, fee address). A fee address should be established when correspondence related to maintenance fees should be mailed to a different address than the correspondence address for the application. **When to check the first box below:** If you have a Customer Number to represent the fee address. **When to check the second box below:** If you have no Customer Number representing the desired fee address, in which case a completed Request for Customer Number (PTO/SB/125) must be attached to this form. For more information on Customer Numbers, see the Manual of Patent Examining Procedure (MPEP) § 403.

For the following listed application(s), please recognize as the "Fee Address" under the provisions of 37 CFR 1.363 the address associated with:

☒ Customer Number: 65358

OR

☐ The attached Request for Customer Number (PTO/SB/125) form.

PATENT NUMBER (if known)	APPLICATION NUMBER
	12/572,498

Completed by (check one):

☐ Applicant/Inventor	/Justin King/ Signature
☒ Attorney or Agent of record 50,464 (Reg. No.)	Justin King Typed or printed name
☐ Assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)	703-684-4411 Requester's telephone number
☐ Assignee recorded at Reel _____ Frame _____	11/07/2011 Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below.

☐ * Total of _____ forms are submitted.

This collection of information is required by 37 CFR 1.363. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 5 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND COMPLETE D FORMS TO THIS ADDRESS. SEND TO: Mail Stop M Correspondence, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal				
Application Number:		12572498		
Filing Date:		02-Oct-2009		
Title of Invention:		SEMICONDUCTOR DEVICE WITH TRENCH OF VARIOUS WIDTHS		
First Named Inventor/Applicant Name:		Chun-Hsien Lin		
Filer:		Anthony King/Justin King		
Attorney Docket Number:		66007-405		
Filed as Large Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl issue fee	1501	1	1740	1740
Publ. Fee- early, voluntary, or normal	1504	1	300	300

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				2040

Electronic Acknowledgement Receipt	
EFS ID:	11349002
Application Number:	12572498
International Application Number:	
Confirmation Number:	4019
Title of Invention:	SEMICONDUCTOR DEVICE WITH TRENCH OF VARIOUS WIDTHS
First Named Inventor/Applicant Name:	Chun-Hsien Lin
Customer Number:	65358
Filer:	Anthony King/Justin King
Filer Authorized By:	Anthony King
Attorney Docket Number:	66007-405
Receipt Date:	07-NOV-2011
Filing Date:	02-OCT-2009
Time Stamp:	14:19:39
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	\$2040
RAM confirmation Number	571
Deposit Account	
Authorized User	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
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1	Issue Fee Payment (PTO-85B)	85.pdf	462752 5c6898515b0b1b760f20cc0ad4ff6bda0c93c5e8	no	2
Warnings:					
Information:					
2	Issue Fee Payment (PTO-85B)	sb0047.pdf	276713 b58af5656e88a3b4399403a4ba3f6d661344d4c	no	2
Warnings:					
Information:					
3	Fee Worksheet (SB06)	fee-info.pdf	32069 7431c0297c527d50c4b32ffcec072267c3b394fb	no	2
Warnings:					
Information:					
Total Files Size (in bytes):			771534		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					



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UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/572,498	12/13/2011	8076735	66007-405	4019

65358 7590 11/22/2011
WPAT, PC
INTELLECTUAL PROPERTY ATTORNEYS
7225 BEVERLY ST.
ANNANDALE, VA 22003

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment is 211 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site <http://pair.uspto.gov> for additional applicants):

Chun-Hsien Lin, Tainan County, TAIWAN;