

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re Patent of: Chun-Hsien Lin  
U.S. Patent No.: 8,076,735 Attorney Docket No.: 57998-0002IP1  
Issue Date: December 13, 2011  
Appl. Serial No.: 12/572,498  
Filing Date: October 2, 2009  
Title: SEMICONDUCTOR DEVICE WITH TRENCH OF VARIOUS  
WIDTHS

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**PETITION FOR *INTER PARTES* REVIEW OF UNITED STATES PATENT  
NO. 8,076,735 PURSUANT TO 35 U.S.C. §§ 311–319, 37 C.F.R. § 42**

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**LIST OF EXHIBITS**

|           |                                                                                                                                                                                                                                                                                      |
|-----------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| TSMC-1001 | U.S. Patent No. 8,076,735 to Lin (“the ’735 Patent”)                                                                                                                                                                                                                                 |
| TSMC-1002 | Excerpts from the Prosecution History of the ’735 Patent (“the Prosecution History”)                                                                                                                                                                                                 |
| TSMC-1003 | Expert Declaration and Curriculum Vitae of Dr. Jack Lee, Ph.D.                                                                                                                                                                                                                       |
| TSMC-1004 | U.S. Pub. No. 2010/0044783 (“Chuang”)                                                                                                                                                                                                                                                |
| TSMC-1005 | U.S. Pub. No. 2008/0265322 (“Lin”)                                                                                                                                                                                                                                                   |
| TSMC-1006 | U.S. Pub. No. 2006/0011994 (“Hong Lin”)                                                                                                                                                                                                                                              |
| TSMC-1007 | U.S. Patent No. 7,208,361 (“Shah”)                                                                                                                                                                                                                                                   |
| TSMC-1008 | RESERVED                                                                                                                                                                                                                                                                             |
| TSMC-1009 | U.S. Pub. No. 2010/0065926 (“Yeh”)                                                                                                                                                                                                                                                   |
| TSMC-1010 | U.S. Pub. No. 2005/0051854 (“Cabral”)                                                                                                                                                                                                                                                |
| TSMC-1011 | RESERVED                                                                                                                                                                                                                                                                             |
| TSMC-1012 | U.S. Patent No. 7,176,090 (“Brask”)                                                                                                                                                                                                                                                  |
| TSMC-1013 | U.S. Pub. No. 2007/0037343 (“Colombo”)                                                                                                                                                                                                                                               |
| TSMC-1014 | A. Chatterjee et al., “CMOS metal replacement gate transistors using tantalum pentoxide gate insulator,” International Electron Devices Meeting 1998, Technical Digest (Cat. No.98CH36217), San Francisco, CA, USA, 1998, pp. 777-780, doi: 10.1109/IEDM.1998.746471. (“Chatterjee”) |

|           |                                                                                                                                                                                                                                              |
|-----------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| TSMC-1015 | S. R. Hofstein et al., “The silicon insulated-gate field-effect transistor,” Proceedings of the IEEE 51 (9), p. 1190-1202 (1963) (“Hofstein”)                                                                                                |
| TSMC-1016 | U.S. Patent No. 8,288,262 (“Lin-262”)                                                                                                                                                                                                        |
| TSMC-1017 | U.S. Pub. No. 2010/0006955 (“Takimoto”)                                                                                                                                                                                                      |
| TSMC-1018 | U.S. Patent No. 6,348,385 (“Cha”)                                                                                                                                                                                                            |
| TSMC-1019 | U.S. Patent No. 6,559,051 (“Buynoski”)                                                                                                                                                                                                       |
| TSMC-1020 | Excerpts from the Prosecution History of U.S. Patent No. 8,288,262                                                                                                                                                                           |
| TSMC-1021 | RESERVED                                                                                                                                                                                                                                     |
| TSMC-1022 | U.S. Patent No. 6,225,168 (“Gardner”)                                                                                                                                                                                                        |
| TSMC-1023 | RESERVED                                                                                                                                                                                                                                     |
| TSMC-1024 | U.S. Pub. No. 2009/0218603 (“Brask-603”)                                                                                                                                                                                                     |
| TSMC-1025 | U.S. Patent No. 9,166,022 B2 (“Xu”)                                                                                                                                                                                                          |
| TSMC-1026 | C. Auth et al., <i>45nm High-k + Metal Gate Strain-Enhanced-Transistors</i> , 2008 Symposium on VLSI Technology, pp. 128-129, (2008)                                                                                                         |
| TSMC-1027 | S. Mayuzumi et al., <i>High-Performance Metal/High-k n- and p-MOSFETs With Top-Cut Dual Stress liners Using Gate-Last Damascene Process on (100) Substrates</i> , IEEE Transactions on Electron Devices, Vol. 56, No. 4, pp. 620-626, (2009) |
| TSMC-1028 | U.S. Patent No. 6,797,572 (“Jeon”)                                                                                                                                                                                                           |
| TSMC-1029 | U.S. Pub. No. 2006/0115937 (“Barnett”)                                                                                                                                                                                                       |

TSMC-1030      U.S. Patent No. 6,444,592 (“Ballantine”)

TSMC-1031      E.P. Patent No. 1,637,626 (“Ji”)

## LISTING OF CLAIMS

| Claim 1   |                                                                                                      |
|-----------|------------------------------------------------------------------------------------------------------|
| [1.pre]   | A semiconductor device comprising:                                                                   |
| [1.1]     | a substrate, disposed with a dielectric layer thereon,                                               |
| [1.2]     | wherein a trench is disposed in the dielectric layer;                                                |
| [1.3.i]   | a gate structure, located in the trench and                                                          |
| [1.3.ii]  | [a gate structure ... comprising] a high dielectric constant layer,                                  |
| [1.3.iii] | [a gate structure ... comprising ... ] a work function metal layer,<br>and                           |
| [1.3.iv]  | [a gate structure ... comprising] a metal layer;                                                     |
| [1.3.v]   | sequentially disposed on the substrate;                                                              |
| [1.4]     | a source/drain region, disposed in the substrate at respective sides<br>of the gate structure,       |
| [1.5]     | wherein the trench comprises a top, a bottom, and a neck arranged<br>between the top and the bottom, |
| [1.6]     | a width of the neck is narrower than a width of the top, and                                         |
| [1.7]     | the width of the neck is narrower than or equal to a width of the<br>bottom.                         |

| Claim 2 |                                                                                                                                                                                                                                                      |
|---------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| [2]     | The semiconductor device as claimed in claim 1, wherein the top and the neck have a first height therebetween, the neck and the bottom have a second height therebetween, and a ratio of the first height to the second height is substantially 2:1. |

| Claim 3 |                                                                                                                                                                                                        |
|---------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| [3]     | The semiconductor device as claimed in claim 1, wherein an included angle between a sidewall of the top of each of the plurality of trenches and a surface of the dielectric layer is larger than 90°. |

| Claim 4 |                                                                                                                                                               |
|---------|---------------------------------------------------------------------------------------------------------------------------------------------------------------|
| [4]     | The semiconductor device as claimed in claim 1, further comprising an insulation layer disposed between the substrate and the high dielectric constant layer. |

| Claim 5 |                                                                                                                          |
|---------|--------------------------------------------------------------------------------------------------------------------------|
| [5]     | The semiconductor device as claimed in claim 1, wherein the source/drain region is a doped region or an epitaxial layer. |

| Claim 6 |                                                                                                                           |
|---------|---------------------------------------------------------------------------------------------------------------------------|
| [6]     | The semiconductor device as claimed in claim 1, further comprising a spacer disposed on a sidewall of the gate structure. |

Taiwan Semiconductor Manufacturing Company Ltd. (“Petitioner” or “TSMC”) petitions for *Inter Partes* Review (“IPR”) under 35 U.S.C. §§ 311–319 and 37 C.F.R. § 42 of claims 1-6 (“the Challenged Claims”) of U.S. Patent No. 8,076,735 (“the ’735 Patent”). Compelling evidence in this Petition demonstrates a reasonable likelihood that Petitioner will prevail with respect to at least one of the Challenged Claims and that the Challenged Claims are unpatentable.

**I. REQUIREMENTS FOR IPR UNDER 37 C.F.R. § 42.104**

**A. Grounds for Standing Under 37 C.F.R. § 42.104(a)**

Petitioner certifies that the ’735 Patent is available for IPR. Petitioner is not barred or estopped from requesting this review challenging the Challenged Claims on the below-identified grounds.

**B. Challenge Under 37 C.F.R. § 42.104(b) and Relief Requested**

Petitioner requests IPR and cancellation of the Challenged Claims on the following grounds:

| Ground | Challenged Claims | Statutory Basis <sup>1</sup> | Prior Art                 |
|--------|-------------------|------------------------------|---------------------------|
| 1A     | 1, 3-6            | § 102                        | Chuang (TSMC-1004)        |
| 1B     | 2                 | § 103                        | Chuang, Brask (TSMC-1012) |
| 2A     | 1, 3-6            | § 102                        | Lin (TSMC-1005)           |
| 2B     | 2                 | § 103                        | Lin, Brask                |
| 3A     | 1, 2              | § 102                        | Brask                     |
| 3B     | 1, 2              | § 103                        | Brask                     |

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<sup>1</sup> To the extent Patent Owner argues or the Board deems any of claims 1 or 3-6 not anticipated by Chuang (Ground 1A) or Lin (Ground 2A), the evidence in this Petition demonstrates that, based on the teachings of Chuang and Lin, the features of these claims and, thus, the claims would have been obvious to a POSITA under § 103 based on the POSITAs understanding of disclosures referenced in each of Chuang and Lin and reasonable inferences and suggestions drawn by a POSITA from the same, accounting for reasons discussed in Grounds 1A and 2A, respectively. TSMC-1003, ¶75, ¶119, ¶209. For efficiency, the above table and following description nevertheless make express reference to these claims only with respect to Grounds 1A and 2A.

The '735 Patent was filed on October 2, 2009 and makes no claim of priority to any earlier-filed applications. For purposes of the analysis in this Petition, Petitioner treats October 2, 2009 as the Critical Date of the Challenged Claims.

The references applied in Grounds 1A-3B qualify as prior art to the '735 Patent under at least the following provisions of pre-AIA 35 U.S.C. § 102:

| Reference | Filed      | Published  | Pre-AIA Prior Art Qualification |
|-----------|------------|------------|---------------------------------|
| Chuang    | 11/21/2008 | 02/25/2010 | § 102(e)                        |
| Lin       | 04/24/2007 | 10/30/2008 | §§ 102(a), 102(e)               |
| Brask     | 09/07/2004 | 02/13/2007 | §§ 102(a), 102(b), 102(e)       |

This Petition is further supported by the declaration of Jack Lee, Ph.D., cited throughout this Petition. *See generally* TSMC-1003 (detailed technical overview).

## II. SUMMARY OF THE '735 PATENT

### A. Technical Background

Metal-oxide-semiconductor field-effect transistors (MOSFETs) are semiconductor devices commonly used as switches in modern integrated circuits. TSMC-1003, ¶¶36-40. A MOSFET includes a gate structure above a substrate of semiconductor material such as silicon. *Id.*, ¶38. A thin dielectric layer separates the gate structure from the substrate. *Id.* The substrate further includes source and drain regions located at respective sides of the gate structure. *Id.* Through this configuration, a voltage applied to the gate structure can be used to modulate the conductivity of a

channel region in the substrate beneath the gate structure and between the source and drain regions to attain a controlled flow of electrical current. *Id.*, ¶¶38-39 (citing TSMC-1004, [0007], FIG. 9; TSMC-1005, [0019], FIG. 6; TSMC-1009; TSMC-1010; TSMC-1014; TSMC-1015; TSMC-1019; TSMC-1022, 1:24-1:60). These basic elements of a FET have been known for decades, as illustrated by the following figure from a 1963 IEEE article:

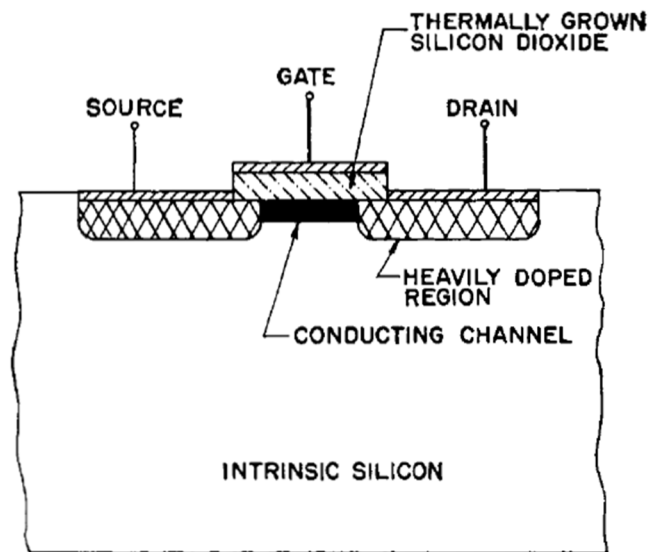


Fig. 2—Insulated-gate field-effect transistor.

TSMC-1015, FIG. 2

*See also* TSMC-1003, ¶39; TSMC-1015, 1190-1202, FIGs. 1-3; TSMC-1022, 1:14-2:4, FIG. 1 (patent filed more than ten years before the '735 patent describing how “[o]ver the last few decades, the electronics industry has undergone a revolution by the use of semiconductor technology” including MOSFETs).

Before the Critical Date of the '735 Patent (October 2, 2009), MOSFET fabrication processes commonly involved use of a “replacement metal gate” process (also referred to as a “gate last” process) to form the metal gate structure. TSMC-1003, ¶¶41-46. The '735 Patent's background section describes this process, which generally involves forming “dummy patterns” (also referred to as “sacrificial structures”) in the shape of the gate structures over the substrate, forming a dielectric over the substrate and around the dummy patterns, removing the dummy patterns from the surrounding dielectric by a selective etching process, and then filling the openings left by removal of the dummy patterns with one or more metals for the gate structure. TSMC-1001, 1:13:39; TSMC-1003, ¶44. The opening that results from removal of a dummy pattern in the gate-last process is referred to as a “trench.” TSMC-1003, ¶44.

To reduce the overall size of the device, it was often desirable to reduce the effective SiO<sub>2</sub> thickness of layers including the gate dielectric layer that separates the metal gate structure from the substrate. TSMC-1003, ¶42; TSMC-1001, 1:12-31. A high dielectric constant (high-k) material was commonly used to achieve a reduced effective SiO<sub>2</sub> thickness while mitigating against increased leakage current. *Id.* In some fabrication processes, the high-k dielectric layer was deposited along the sidewalls and bottom of the trench after the dummy pattern was removed TSMC-1003, ¶¶42-44. In other fabrication process, the high-k dielectric layer was formed

before the dummy pattern and remained at the bottom of the trench after removal of the dummy pattern. *Id.*; *see also id.* ¶47. In either process, a work-function metal was deposited over the high-k dielectric layer to set the work function of the gate structure. *Id.* If the work-function metal did not fill the entirety of trench, the remaining trench volume was filled with a low-resistivity metal, commonly tungsten or a similar conductor, to form the bulk of the gate. *Id.*; *see also id.* ¶47 (citing TSMC-1007, TSMC-1013).

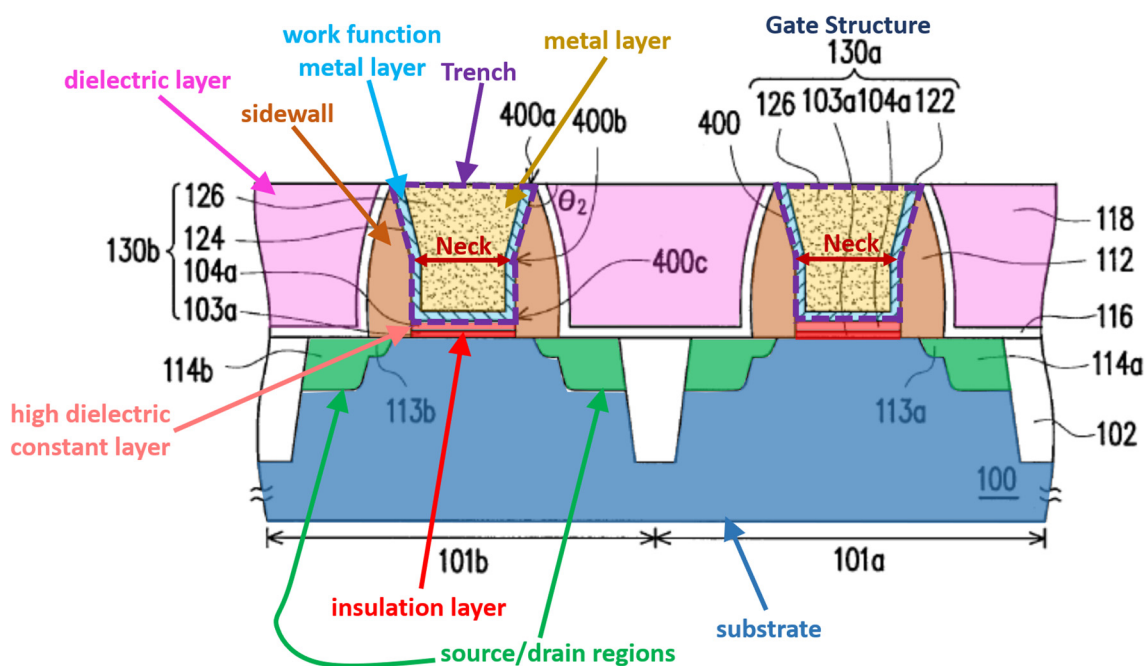
Trenches for metal gate structures formed by gate-last processes were often trapezoidal in shape, where the top was narrower than the neck and bottom. TSMC-1001, 1:40-54; TSMC, 1003, ¶¶48-51. Trapezoidal trenches were difficult to fill with metal, however, and often led to voids forming in the metal that filled the trenches, which negatively impacted the reliability and performance of the transistor. *Id.*, ¶48. This problem was well known in the prior art, and engineers before the Critical Date of the '735 Patent experimented with various trench geometries with the aim of achieving “void-free” fills. *See* TSMC-1003, ¶¶49-51 (citing TSMC-1007, [0015]-[0017], [0019], FIGs. 1C, 2A-2M; TSMC-1006, [0021]-[0024], [0031], FIGs. 10-14, TSMC-1017, TSMC-1018, TSMC-1019, TSMC-1004, TSMC-1005, TSMC-1012, TSMC-1024).

Although never acknowledged in the '735 Patent, one technique known in the prior art for mitigating void formation was to shape the trench such that the top of

the trench was wider than the neck and bottom. TSMC-1003, ¶¶49-51. As described in the next section, the inventor of the '735 Patent nonetheless described and claimed this prior art solution as his own. *Id.*

## **B. Overview of the '735 Patent**

The '735 Patent describes “a void-free semiconductor device and a method of fabricating the same.” TSMC-1001, 1:5-11. *see also id.* Abstract; TSMC-1003, ¶¶52-59. Specifically, as alluded to above, the '735 Patent purports to reduce void formation in the metal that fills the trench of a metal gate structure by shaping the trench to have a “neck” located between the top and the bottom of the trench, where the neck is narrower than the top and narrower or equal to a width of the bottom. *See* TSMC-1001, 1:62-65, 1:43-49, 3:26-31; TSMC-1003, ¶56. FIG. 4 illustrates one embodiment of such a semiconductor device having gate structures 130a, 130b formed in a y-shaped trench that narrows from the top for a first distance (to the neck) before maintaining a constant width for a second distance from the neck to the bottom of the trench:



'735 Patent, FIG. 4 (annotated)

### C. Prosecution History

The '735 Patent was allowed on a first action without the Examiner having issued a single rejection. TSMC-1002, 89-97 The Examiner's reasons for allowance focused on limitations in claim 1 directed to the "gate structure" and the shape of the "trench." TSMC-1002, 95. Specifically, the Examiner alleged that the prior art failed to disclose "a gate structure, located in the trench and comprising a high dielectric constant layer, a work function metal layer, and a metal layer sequentially disposed on the substrate, wherein the trench comprises a top, a bottom, and a neck arranged between the top and the bottom, a width of the neck is narrower than a width of the top, and the width of the neck is narrower than or equal to a width of the bottom."

*Id.*

The Examiner’s first-action allowance was in error. As this Petition demonstrates, a host of prior art references disclose the same trench geometry that the Examiner mistakenly believed was novel. This Petition alone presents *three* anticipatory prior art references including Chuang (TSMC-1004), Lin (TSMC-1005), and Brask (TSMC-1012)<sup>2</sup>—all of which show that the ’735 Patent never should have been allowed. TSMC-1003, ¶209.

#### **D. Level of Ordinary Skill in the Art**

A person having ordinary skill in the art (“POSITA”) would possess a Master of Science degree from an accredited institution in electrical engineering, materials science, physics, chemistry or related fields, and would have at least three years of experience in manufacturing semiconductors including planar and non-planar transistors. Additional graduate education could substitute for professional experience, and significant work experience or training could substitute for formal education. TSMC-1003, ¶¶33-35.

#### **E. Claim Construction**

Claim terms in an *inter partes* review are interpreted “using the same claim construction standard that would be used to construe the claim in a civil action under

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<sup>2</sup> Brask was cited during prosecution of a divisional application (TSMC-1016) of the ’735 Patent. *See* TSMC-1020, 66, *see also* TSMC-1016, Cover.

35 U.S.C. 282(b),” which is the *Phillips* standard. 37 CFR § 42.100(b); *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005).

Petitioner submits that no formal constructions are presently necessary. This Petition instead maps the prior art consistent with the plain and ordinary meaning of the claims in light of the specification and file history. Petitioner reserves the right to respond to any constructions that may later be offered by Patent Owner or the Board. TSMC-1003, ¶¶21-22.

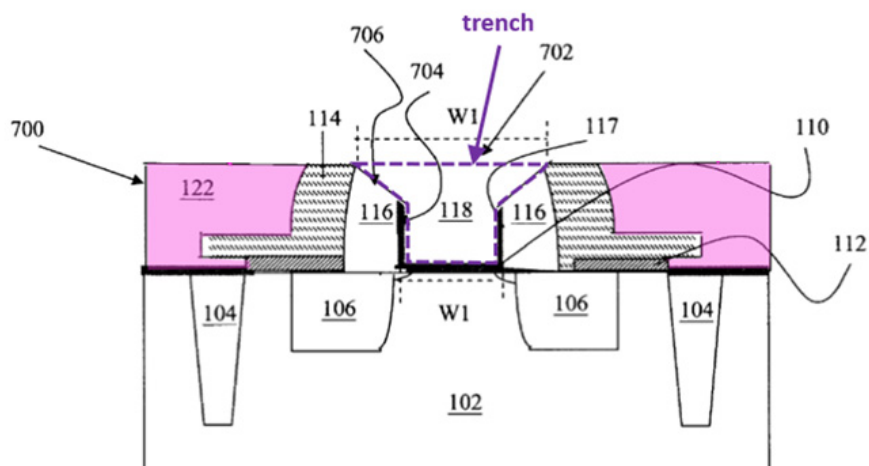
### **III. THE CHALLENGED CLAIMS ARE UNPATENTABLE**

#### **A. [GROUND 1A] – Chuang Anticipates Claims 1, 3-6**

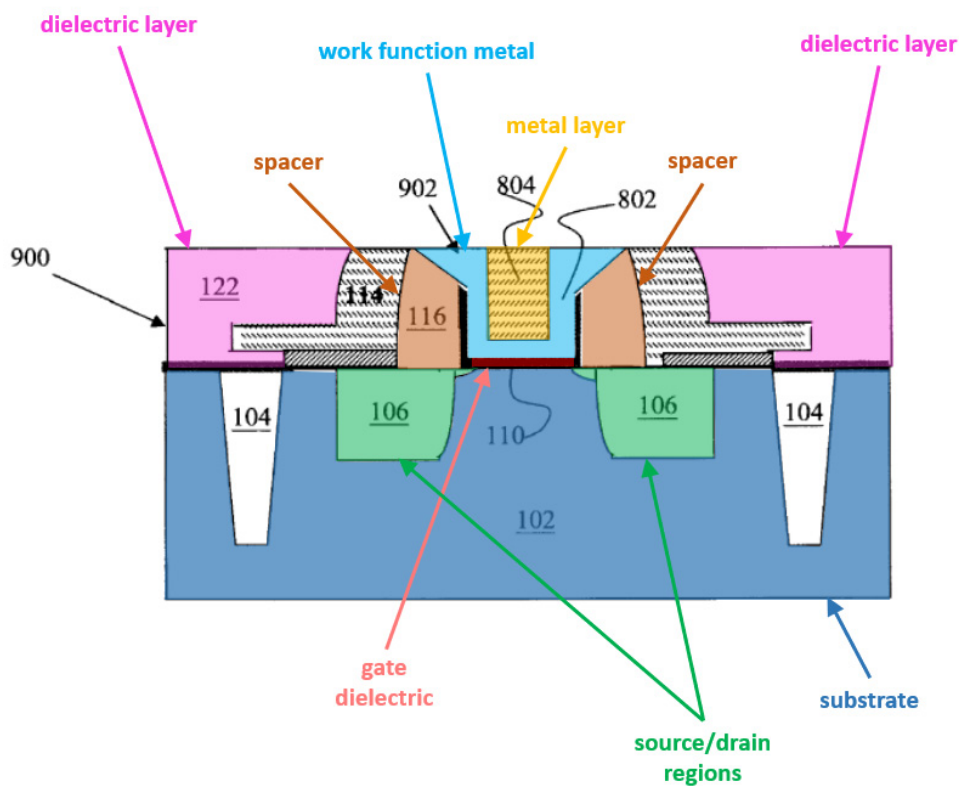
##### **1. Overview of Chuang**

Like the '735 Patent, Chuang discloses a metal gate structure disposed in a trench having a neck narrower than the top and of equal width as the bottom. *See generally* TSMC-1004, [0028]-[0036], FIGs. 6-9; TSMC-1003, ¶¶60-62.

FIGs. 7 and 9 (reproduced below), for example, depict an embodiment of Chuang’s semiconductor device that includes a metal gate structure including a gate dielectric 110, work function metal 802, and metal layer 804 disposed in a trench that extends vertically from the bottom and then widens toward the top. Moreover, Chuang discloses that “[t]he [trench] profile may be modified such that the opening of the trench (*e.g.*, top portion or aperture of the trench) is wider than the bottom of the trench.” TSMC-1004, [0031], FIGs. 6-9.



Chuang, FIG. 7 (annotated)



Chuang, FIG. 9 (annotated)

## 2. Analysis

Chuang anticipates claims 1 and 3-6 of the '735 Patent.<sup>3</sup> TSMC-1003, ¶¶74-75.

### (a) Claim 1

#### ***[1.pre] A semiconductor device comprising:***

To the extent the preamble is limiting, Chuang discloses the recited “semiconductor device.” TSMC-1003, ¶76. For example, in the Abstract of the disclosure, Chuang describes “a semiconductor device including a gate structure having a larger width at the top of the gate than the bottom of the gate.” TSMC-1004, Abstract<sup>4</sup>; *see also id.*, [0007] (“a semiconductor device is provided”), [0014] (“The present disclosure relates generally to forming an integrated circuit device on a substrate and, more particularly, to fabricating a gate structure as part of an integrated circuit (including FET devices).”), [0015]-[0016], [0024], [0034]-[0041], FIGs. 9, 11; TSMC-1003, ¶76.

#### ***[1.1] a substrate, disposed with a dielectric layer thereon,***

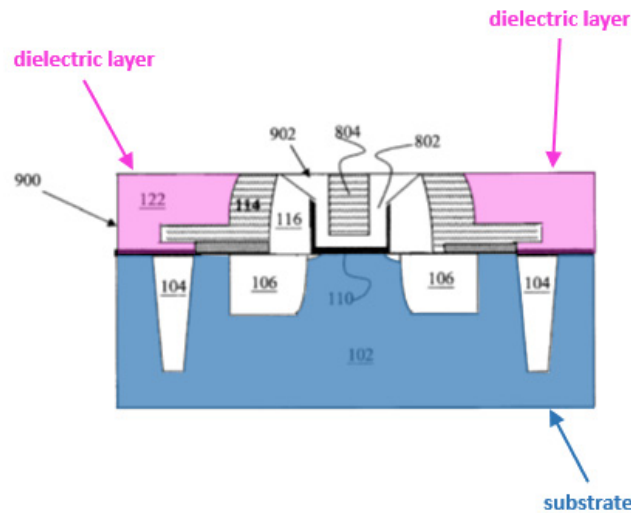
Chuang discloses this limitation. TSMC-1003, ¶¶77-80. For example, Chuang discloses that its semiconductor device includes a dielectric layer 122 (*dielectric*

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<sup>3</sup> *Supra*, Footnote 1.

<sup>4</sup> All emphasis is added unless otherwise noted.

*layer*) disposed on a substrate 102 (*substrate*). TSMC-1004, [0007], [0016]-[0017], [0023]-[0024], [0037]. FIG. 9 depicts these features:



Chuang, FIG. 9 (annotated)

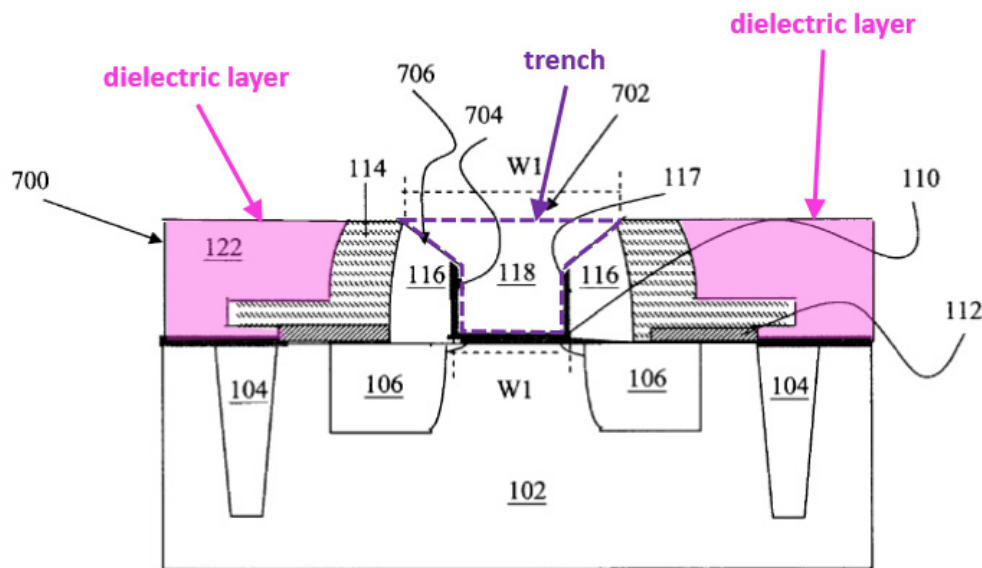
Chuang discloses that dielectric layer 122 is “[f]ormed on” substrate 102 such that substrate 102 is disposed with dielectric layer 122 thereon. TSMC-1004, [0016] (“The semiconductor device 100 includes a substrate 102. Formed on the substrate 102 are ... a dielectric layer 122.”); *see also id.*, [0014] (“forming an integrated circuit device on a substrate”), [0024]; TSMC-1003, ¶78. Chuang’s device is thus substantially similar to the preferred embodiments of the ’735 Patent, which similarly include a dielectric layer disposed on a substrate along with various additional structures including a stop layer 114. *Cf.*, TSMC-1001, 8:43-45 & FIGs. 1E, 4 (“The dielectric layer 118 is disposed on the substrate 100”), 7:12-28 & FIG. 4; TSMC-1003, ¶¶78-79.

Further, as discussed below with respect to [1.2], the collection of Chuang’s

stop layer 114, spacers 116, and inter-level dielectric layer 122 provides an alternative mapping to the claimed “dielectric layer.” *Infra*, [1.2]; TSMC-1003, ¶¶80. Each of these components is likewise disposed on substrate 102 of Chuang’s device. TSMC-1004, [0014], [0016], [0024], FIG. 9.

***[1.2] wherein a trench is disposed in the dielectric layer;***

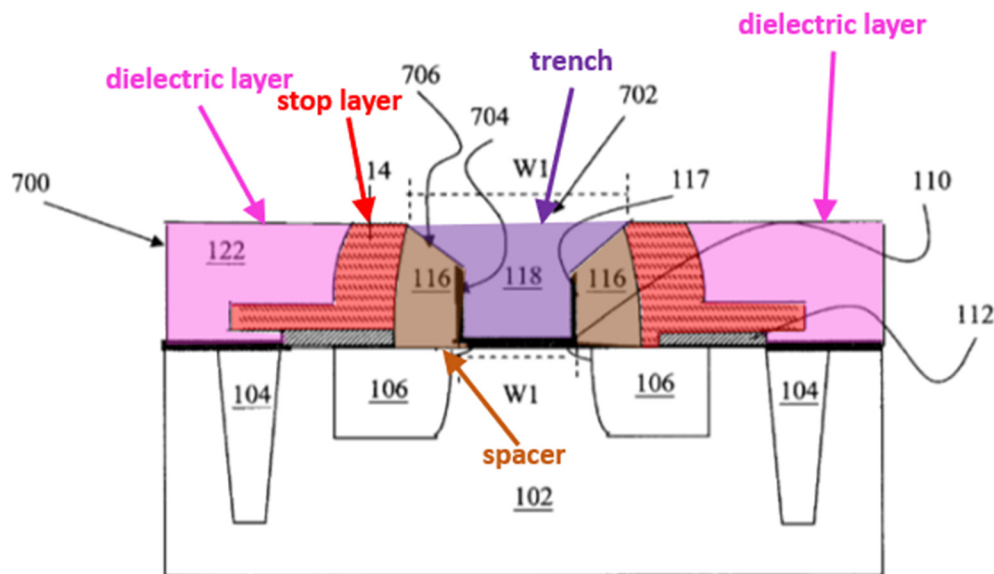
Chuang discloses this limitation. TSMC-1003, ¶¶81-84. For example, FIG. 7 depicts a trench disposed in the dielectric layer 122 (*dielectric layer*) during an intermediate stage of fabrication of Chuang’s semiconductor device (*i.e.*, before filling the trench with metal for the gate structure):



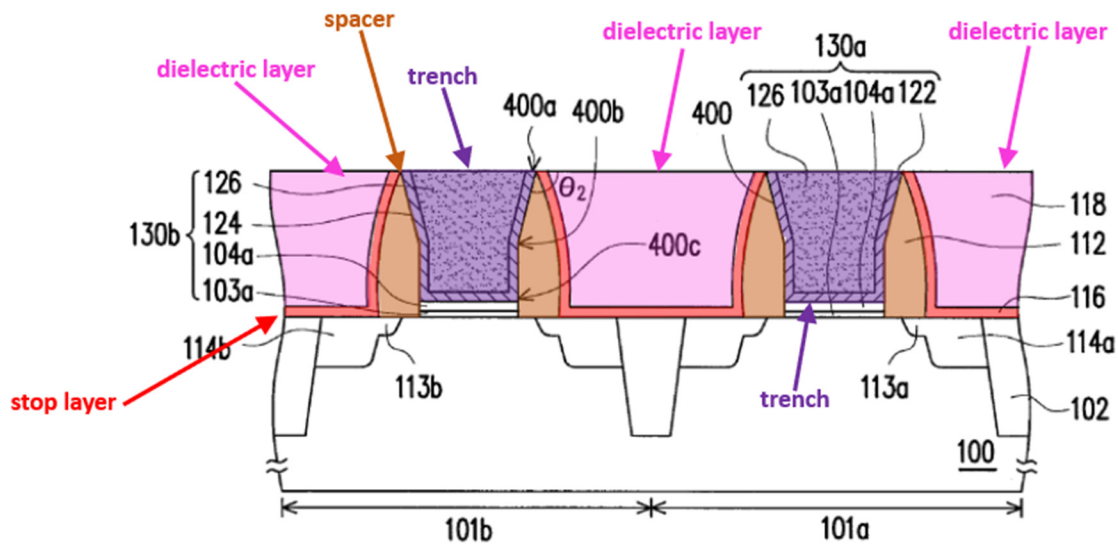
Chuang, FIG. 7 (annotated)

*See also id.*, [0024], [0025], [0030]-[0033], FIG. 3 (depicting trench 302 immediately following removal of dummy gate structure 118).

For comparison, like Chuang’s device, the ’735 Patent’s device includes a trench 400 “disposed in” a dielectric layer 118 notwithstanding the presence of intervening spacers 112 and stop layer 116. *Cf.*, TSMC-1001, FIG. 4, 9:36-58; *see also id.*, claim 6 (“a spacer disposed on a sidewall of the gate structure”), 8:43-45 (“The dielectric layer 118 is disposed on the substrate 100, and the trenches 120 are disposed in the dielectric layer 118.”). The following figures illustrate the like configurations of Chuang’s trench disposed in dielectric layer 122 and the ’735 Patent’s trench 120 disposed in dielectric layer 118, flanked similarly by spacers and a stop layer:



Chuang, FIG. 7 (annotated)



'735 Patent, FIG. 4 (annotated)

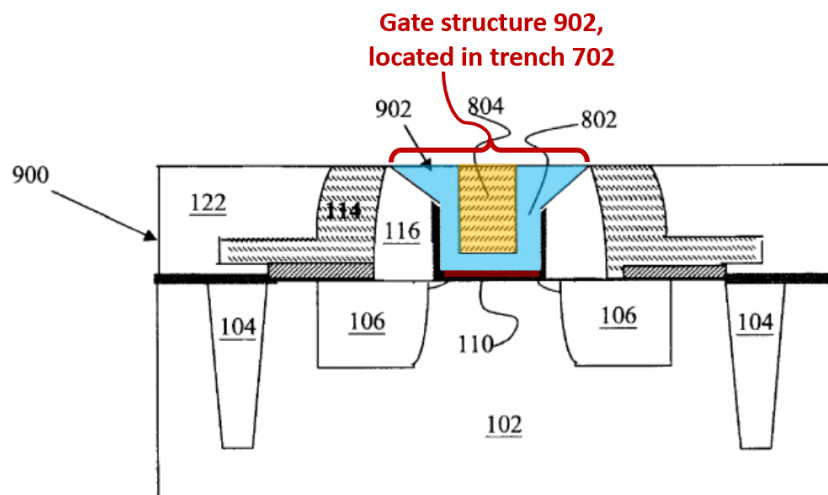
See also TSMC-1004, [0024], [0028], [0030]-[0032], [0036], FIGs. 3, 6; TSMC-1003, ¶¶82-83.

Claim 1 does not require that the trench directly abuts the dielectric layer. TSMC-1003, ¶¶82-83. Still, to the extent Patent Owner argues that limitation [1.2] does not allow for intervening structures between the gate structure and the dielectric layer, Chuang would still anticipate. TSMC-1003, ¶84. This follows because Chuang discloses that dielectric layer 122, contact etch stop layer (CESL) 114, and spacers 116 are each formed from dielectric materials, and together constitute the claimed “*dielectric layer*.” TSMC-1003, ¶84; TSMC-1004, [0022] (CESL 114 “formed of silicon nitride, silicon oxynitride, and/or other suitable materials”), [0023] (dielectric layer 122 “may include silicon oxide, silicon oxynitride, or a low k material”), [0020] (spacers 116 “formed of silicon oxide, silicon nitride, silicon

oxynitride, silicon carbide, fluoride-doped silicate glass (FSG), a low k dielectric material, combinations thereof” and may include “liner layer 116 [that] may include a dielectric material”; “spacers 116 may be formed by ... deposition of suitable dielectric material”). Chuang’s trench is disposed directly in this dielectric layer. *Id.*

**[1.3.i] a gate structure, located in the trench and**

Chuang discloses this limitation. TSMC-1003, ¶85. FIG. 9, for example, depicts a “metal gate structure 902” formed in a trench 702 whose shape includes a widened aperture at the top:

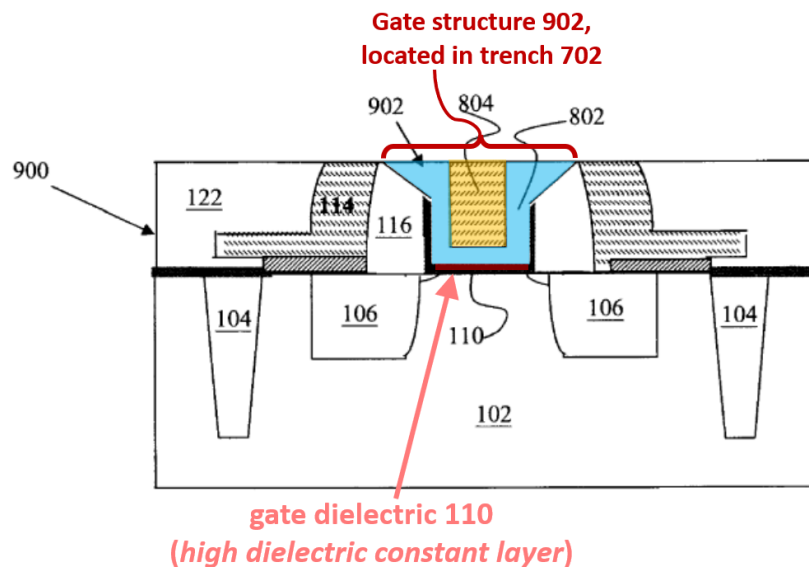


Chuang FIG. 9 (annotated)

*See also* TSMC-1004, [0006] (“A metal gate is formed in the trench having the modifying profile.”), [0008] (“A gate is then formed in the trench.”), [0034], [0033] (“The method 600 then proceeds step 610 where metal is deposited in the modified profile trench.”), Cls. 1, 16.

***[1.3.ii] [a gate structure ... ] comprising a high dielectric constant layer,***

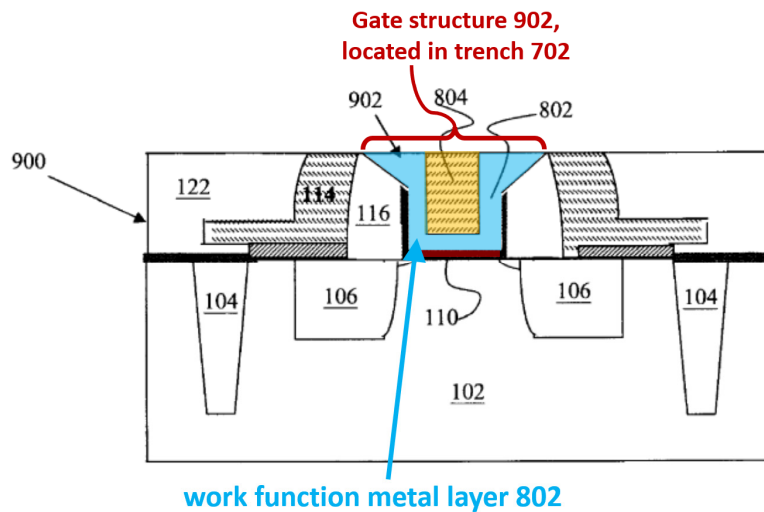
Chuang discloses this limitation. TSMC-1003, ¶86. For example, Chuang discloses a gate dielectric layer 110, and specifically states that “the gate dielectric includes a high dielectric constant (high K) material.” TSMC-1004, [0007]; *see also id.*, [0019], Cl. 6, Cl. 20, [0016], [0034], [0037], FIGs. 1-3, 6, 9. FIG. 9 depicts the high dielectric constant layer 110, in an embodiment:



Chuang, FIG. 9 (annotated)

***[1.3.iii] [a gate structure ... comprising ... ] a work function metal layer, and***

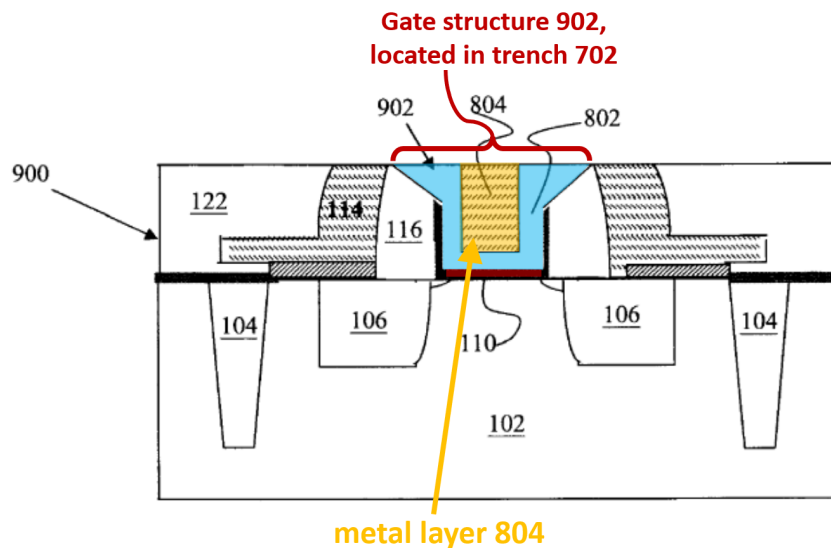
Chuang discloses this limitation. TSMC-1003, ¶87. For example, Chuang discloses that “[t]he metal gate structure 902 includes the work function metal 802, the metal gate fill material 804 and the gate dielectric layer 110.” TSMC-1004, [0034]; *see also id.*, [0033].



Chuang, FIG. 9 (annotated)

***[1.3.iv] [a gate structure ... comprising ... ] a metal layer;***

Chuang discloses this limitation. TSMC-1003, ¶¶88-89. For example, Chuang discloses that “[t]he metal gate structure 902 includes the work function metal 802, the metal gate fill material 804 and the gate dielectric layer 110.” TSMC-1004, [0034].



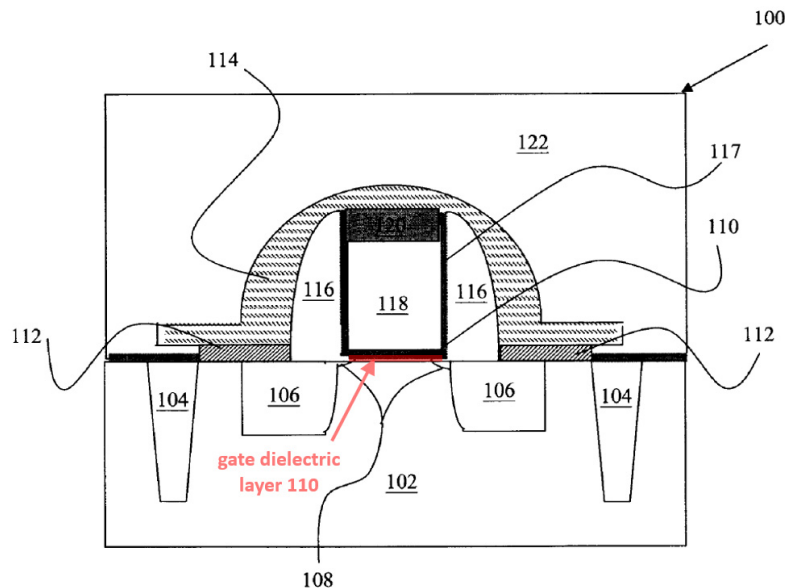
Chuang, FIG. 9 (annotated)

According to Chuang, “[i]n addition to the n-type and/or p-type metals, a fill

metal may be deposited to substantially or completely fill the remainder of the trench.” *Id.*, [0033]. “The fill metal may include titanium nitride, tungsten, titanium, aluminum, tantalum, tantalum nitride, cobalt, copper, nickel, and/or other suitable materials.” *Id.*

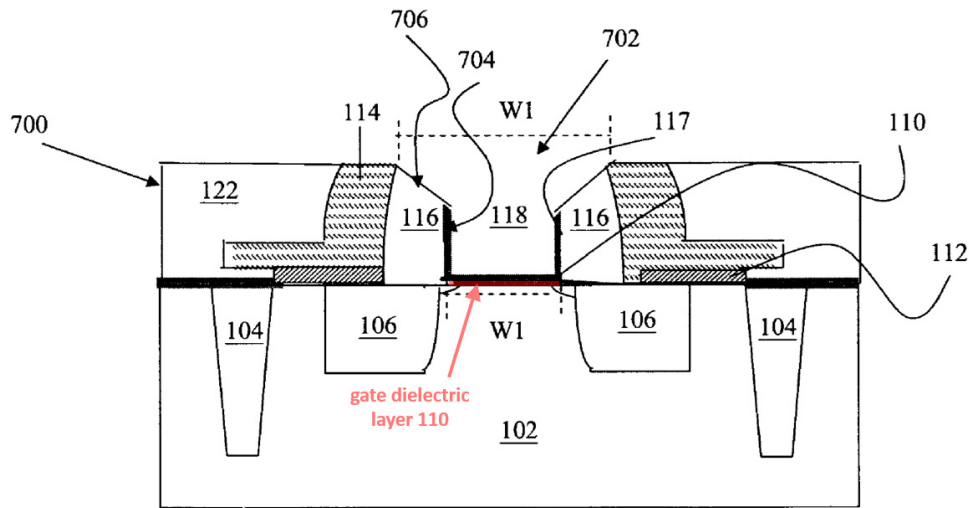
***[1.3.v] sequentially disposed on the substrate;***

Chuang discloses this limitation. TSMC-1003, ¶¶90-93. For example, Chuang discloses that the gate dielectric layer 110 (***high dielectric constant layer***), the work function metal 802 (***work function metal layer***), and the gate fill metal 804 (***metal layer***) are sequentially disposed on substrate 102 (***substrate***). This is evident from FIG. 9, which shows the gate fill metal layer 804 over the work function metal layer 802 and the work function metal layer 802 over the gate dielectric layer 110—*i.e.*, an arrangement that results from sequential disposition of the layers as recited in [1.3.v]. TSMC-1004, FIG. 9; *see also id.*, [0033], FIG. 6. This understanding is also consistent with Chuang’s method of forming “a metal gate by a ‘gate last’ process” as described with respect to FIG. 6. *Id.*, [0028]; *generally id.*, [0029]-[0036], FIG. 6. Chuang states that this method “begins” at step 602 with a transistor structure that includes a “dummy gate structure” that is “substantially similar to the dummy gate structure 118” depicted in FIG. 1:



Chuang, FIG. 1 (annotated)

As shown in FIG. 1, the gate dielectric layer 110 (*high dielectric constant layer*) is already formed and disposed over substrate 102 by the time dummy gate structure 118 is formed—and before the trench is formed or any metal layers are filled in the trench. TSMC-1004, [0016], [0019], [0022]. For example, FIG. 7 shows the device after formation of trench 702 (*i.e.*, after removal of dummy gate structure 118 and after modification of the trench profile) but before trench 702 is filled with either work function metal layer 802 or gate fill metal layer 804. Here again, gate dielectric layer 110 (*high dielectric constant layer*) is already formed and disposed over substrate 102:



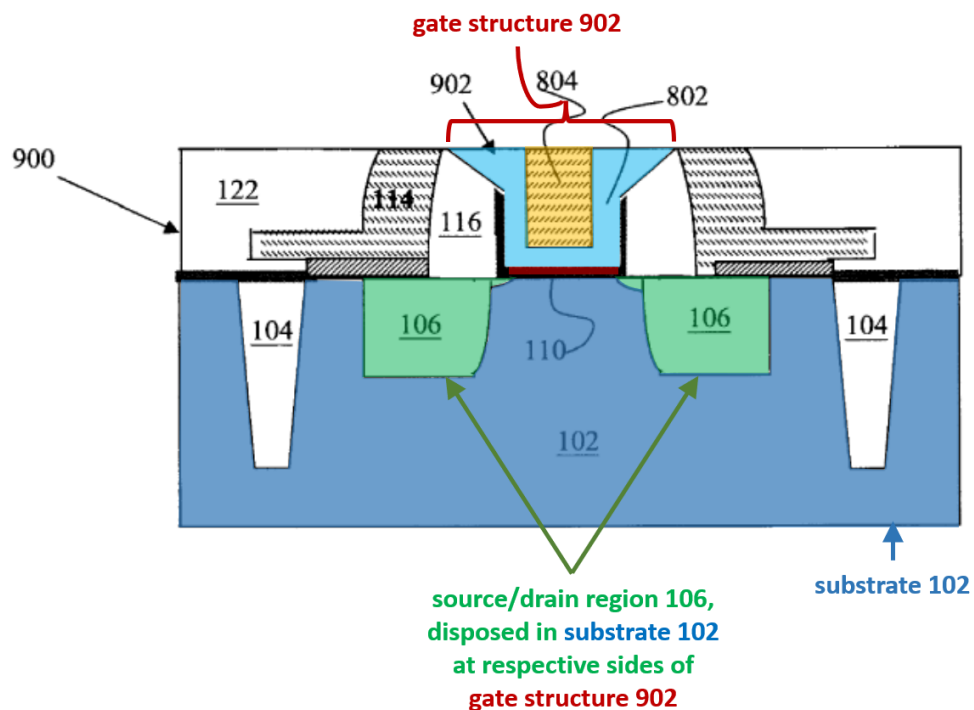
Chuang, FIG. 7 (annotated)

After the trench is formed and its profile modified to include a wider top, the trench is filled with work function metal layer 802 followed by gate fill metal layer 804. TSMC-1004, [0033] (“The deposited layers substantially fill the trench provided above in steps 606 and 608. It is noted that a first deposited layer (e.g., work function metal 802) provides a vertical sidewall ...”), [0025] (“deposition of a first metal 402 such as ... work function metal” and “subsequent deposition of metal layer 406”), FIGs. 4-6; *see also id.*, [0016], [0019], [0022], [0028].

For each of these reasons, Chuang discloses that gate dielectric layer 110 (*high dielectric constant layer*), work function metal layer 802 (*work function metal layer*), and gate fill metal layer 804 (*metal layer*) are sequentially disposed on substrate 102 (*substrate*). TSMC-1003, ¶¶90-93.

**[1.4] a source/drain region, disposed in the substrate at respective sides of the gate structure,**

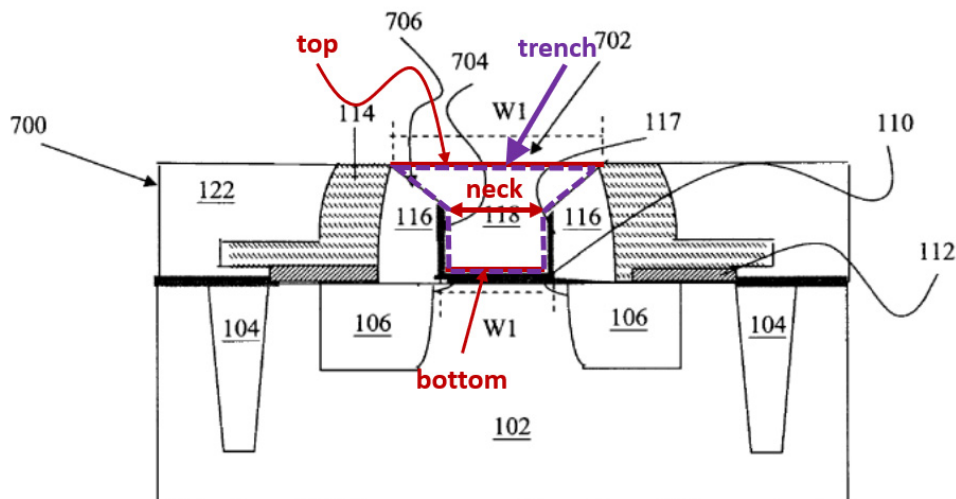
Chuang discloses this limitation. TSMC-1003, ¶94. For example, Chuang discloses a “semiconductor device” that includes “a gate structure disposed on the substrate between the source and drain regions.” TSMC-1004, [0007], Claim 11 (same); *see also id.*, [0016], [0022], FIGs. 1, 6. FIG. 9 shows source/drain region 106 (***a source/drain region***) disposed in substrate 102 at respective sides of metal gate structure 902:



Chuang, FIG. 9 (annotated)

**[1.5] wherein the trench comprises a top, a bottom, and a neck arranged between the top and the bottom,**

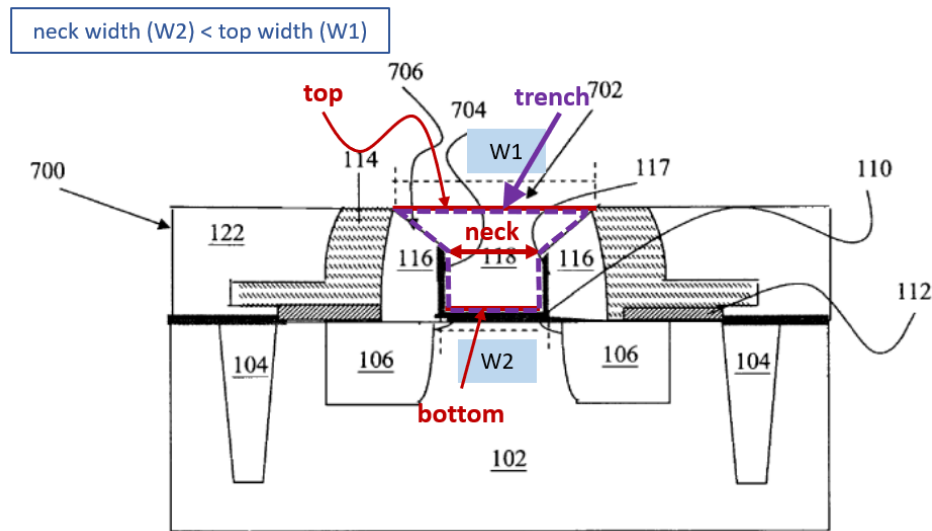
Chuang discloses this limitation. TSMC-1003, ¶95. For example, Chuang discloses a trench 702 (**trench**) that includes an aperture (**top**), a bottom (**bottom**), vertical sidewalls 704, and oblique sidewalls 706. Like the necks 200b and 400b depicted respectively in FIGs. 2 and 4 of the '735 Patent, Chuang's trench 702 further includes a "**neck**" at the uppermost portion of vertical sidewalls 704 where the sidewalls begin to taper to form oblique sidewalls 706. *Compare* TSMC-1004, FIGs. 7 & 9 *with* TSMC-1001, FIGs. 2 & 4; *see also* TSMC-1004, [0002]-[0006], [0019], [0024], [0028], [0030]-[0032], [0041]. Chuang depicts the claimed elements of the trench in FIG. 7:



Chuang, FIG. 7 (annotated)

**[1.6] a width of the neck is narrower than a width of the top, and**

Chuang discloses this limitation. TSMC-1003, ¶¶96-97. As described above in the analysis of [1.5], Chuang discloses a trench 702 (**trench**) that includes an aperture (**top**), a bottom (**bottom**), vertical sidewalls 704, and oblique sidewalls 706. *Supra*, [1.5]. A “**neck**” is formed at the top of vertical sidewalls 704 where the vertical sidewalls 704 meet oblique sidewalls 706. *Id.* As shown in FIG. 7, Chuang discloses that the width of the neck is narrower than a width of the top of the trench 702:



Chuang, FIG. 7 (annotated and modified<sup>5</sup>)

<sup>5</sup> Chuang identifies two different widths W1 and W2 for the top and bottom of the trench 702, respectively: “The trench 702 includes a width at its aperture W1 that is greater than the width at the bottom of the trench W2.” TSMC-1004, [0032]. The

In particular, Chuang explains that “the trench 702 includes a width at its aperture W1 that is greater than the width at the bottom of the trench W2.” TSMC-1004, [0032]. “The sidewalls of the trench, such as sidewall 704 extend vertically from the bottom of the trench, and then extend in an oblique manner to form the top of the trench illustrated by oblique sidewall 706.” *Id.* Because the neck is located at the top of sidewalls 704 that extend vertically from the bottom of the trench 702 having width W2, the width of the neck is also W2, which is narrower than the width W1 at the top. *Id.*; *see also id.*, [0031], [0041], [0002]-[0006], [0008], [0024], [0038], [0040]-[0041], cls. 1, 16.

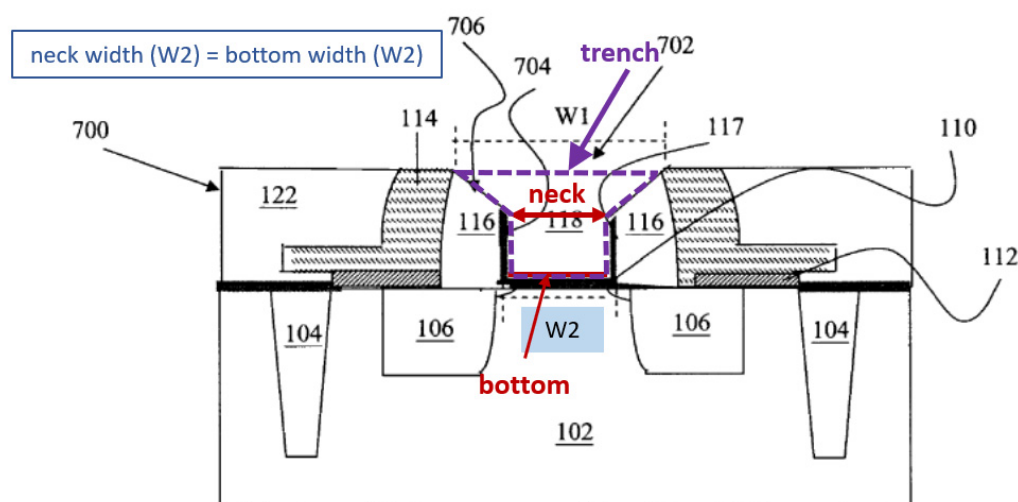
***[1.7] the width of the neck is narrower than or equal to a width of the bottom.***

Chuang discloses this limitation. TSMC-1003, ¶¶98-99. As described above in connection with limitations [1.5]-[1.6], because the neck of Chuang’s trench 702 is located at the top of sidewalls 704 that extend vertically from the bottom of the

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depiction of FIG. 7 nonetheless labels both widths at the top and bottom of the trench 702 as “W1.” *Id.*, FIG. 7. A POSITA would have understood that the “W1” label applied to the width at the bottom of the trench 702 is a typographical error that should instead be labeled “W2” as described in the text at ¶[0032]. For clarity, Petitioner has corrected this label in the annotated version of FIG. 7 reproduced above.

trench 702 having width W2, the width of the neck is also W2. FIG. 7 illustrates this limitation:



Chuang, FIG. 7 (annotated and modified<sup>6</sup>)

In particular, as shown in FIG. 7, the width of the neck is equal to the width of the bottom of the trench W2 as both widths are between the opposing vertical sidewalls 704. TSMC-1004, [0032] (“[T]he width at the bottom of the trench [is] W2. The sidewalls of the trench, such as sidewall 704 extend vertically from the bottom of the trench ... .”), [0031], [0006]-[0008], [0038], [0040]-[0041], cls. 1, 16; *supra* Ground 1A, [1.5]-[1.6].

<sup>6</sup> *Supra*, Footnote 5.

(b) Claim 3

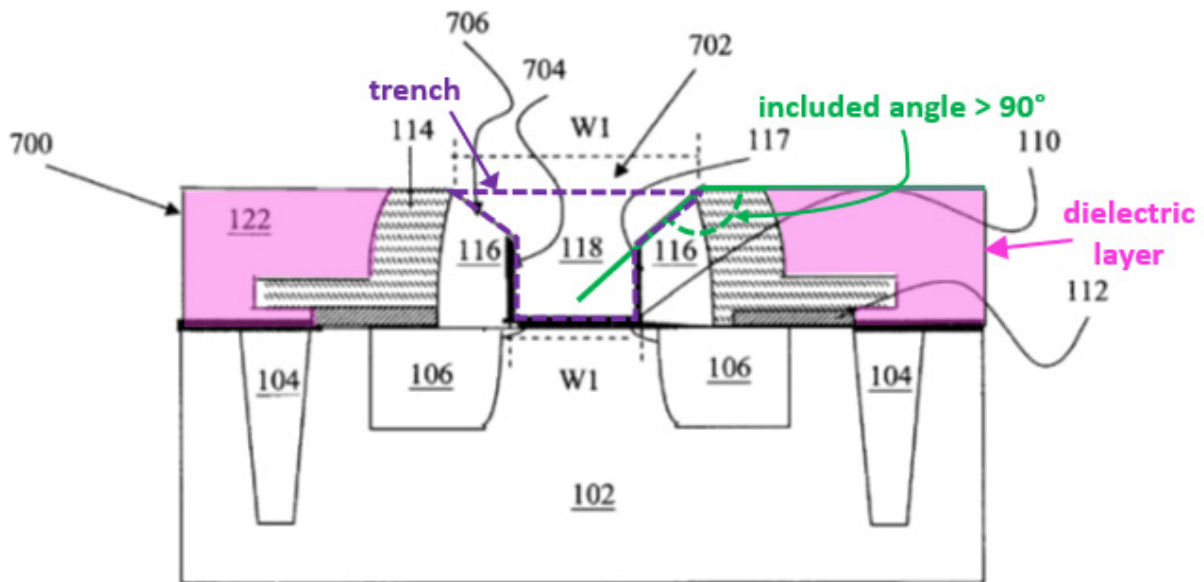
***[3]<sup>7</sup> The semiconductor device as claimed in claim 1, wherein an included angle between a sidewall of the top of each of the plurality of trenches and a surface of the dielectric layer is larger than 90°.***

Chuang discloses this limitation. TSMC-1003, ¶¶100-101. For example, Chuang discloses that, after initially forming the trench by removal of the dummy

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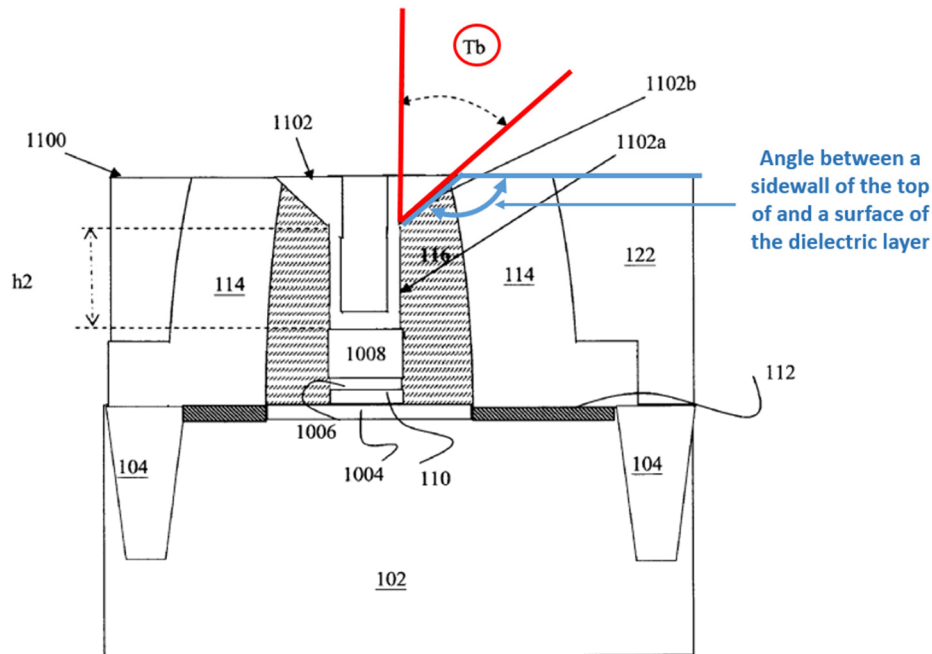
<sup>7</sup> Claim 3 lacks antecedent basis for the term “the plurality of trenches.” This Petition treats claim 3 as referring to “the trench” recited in claim 1, and thus encompassing a semiconductor device having even a single trench. TSMC-1003, Footnote 9. Still, even if claim 3 did require that the semiconductor device include multiple trenches, Chuang at least implies or renders this feature obvious. *Id.* For example, Chuang discloses that its transistors are provided in “integrated circuit” devices that each includes many transistors, including complementary NMOS and PMOS devices each having a respective trench. TSMC-1004, [0002], [0014]-[0015] (“CMOS”). Each transistor in the integrated circuit device formed according to the techniques disclosed in Chuang has a tapered profile trench, and considered collectively, they provide a “plurality of trenches” that exhibit the geometry recited in claim 3. TSMC-1003, Footnote 9 (citing TSMC-1012, FIGs. 1A-1I (illustrating CMOS device having a plurality of trenches); *In re Harza*, 274 F.2d 669 (CCPA 1960) (“It is well settled that the mere duplication of parts has no patentable significance.”)).

gate structure, “[t]he profile [of the trench] may be modified such that the opening of the trench (*e.g.*, top portion or aperture of the trench) is wider than the bottom of the trench.” TSMC-1004, [0031], FIGs. 6-9. “The modified profile includes tapered sidewalls” and “may be referred to as a tapered profile trench.” *Id.*, [0032], [0036]. Noticeably, the oblique sidewalls 706 of the trench form an included angle with a surface of the dielectric layer 122 (*dielectric layer*) that is larger than 90° as shown in FIG. 7:



Chuang, FIG. 7 (annotated)

Chuang also explains that the gate includes a “tapered profile” that “provides a taper having an angle Tb (e.g., angle between the vertical portion 1202a and the tapered portion 1202b)”:



Chuang, FIG. 11 (annotated)

TSMC-1004, [0040], FIG. 11; *see also id.*, [0038]. Chuang explains that “the angle Tb is between approximately 30 and 5 degrees.” *Id.*, [0040]. Accordingly, Chuang expressly discloses that the angle between the sidewall at the top of the trench and the surface of the dielectric layer can be between approximately 120° and 95°, larger than 90°. TSMC-1003, ¶101.

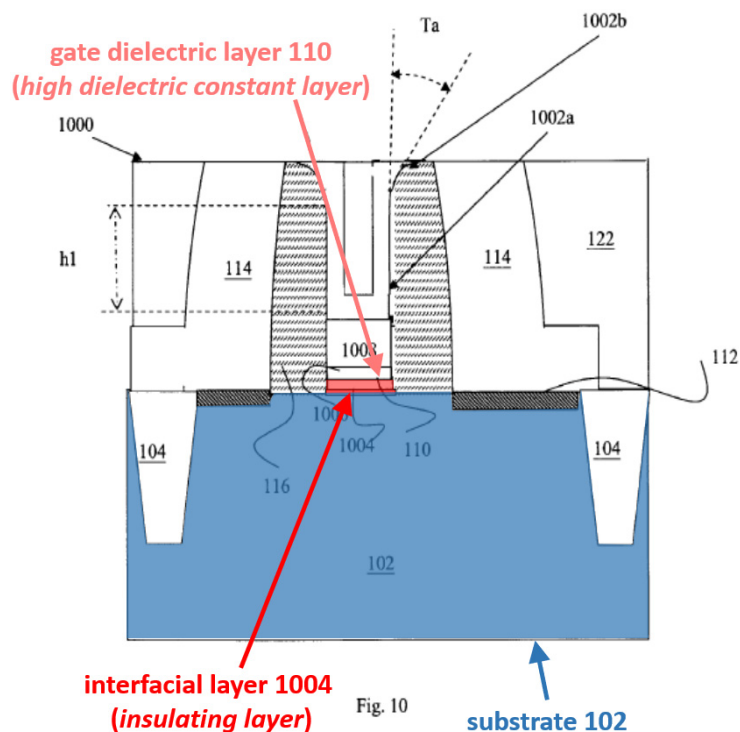
(c) Claim 4

***[4] The semiconductor device as claimed in claim 1, further comprising an insulation layer disposed between the substrate and the high dielectric constant layer.***

Chuang discloses this limitation. TSMC-1003, ¶¶102-105. For example, Chuang discloses that “[t]he semiconductor device 100 may further include, various

other dielectric and/or conductive layers, for example, interfacial layers and/or capping layers underlying the dummy gate pattern 118. TSMC-1004, [0019]; *see also id.*, [0023] (“Other layers may be present on the device 100 ... interfacial layers.”), [0033].

Chuang illustrates an example “interface layer 1004” in Figure 10:



Chuang, FIG. 10 (annotated)

FIG. 10 explicitly shows interface layer 1004 disposed between substrate 102 (*substrate*) and gate dielectric layer 110 (*high dielectric constant layer*). TSMC-1004, [0037], FIG. 10. Chuang notes that FIG. 10 includes features that are “substantially similar to the respective features described above with respect to FIG. 1.” *Id.*, [0037]. The more detailed description of FIG. 10 indicates that the interface layer Chuang

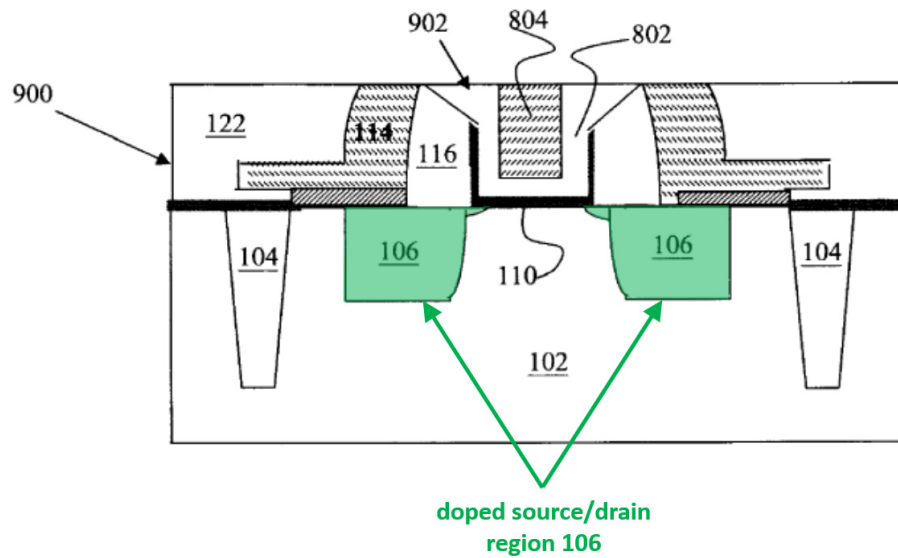
describes with respect to FIGs. 1 and 6-9 is also disposed between the substrate 102 and gate dielectric layer 110.

Chuang's interface layer includes "silicon, oxygen, and/or nitrogen"—*i.e.*, materials that insulate when disposed between a substrate and a high-dielectric constant layer like Chuang's. TSMC-1004, [0037]. A POSITA would have understood Chuang's "interface layer" to be an "*insulation layer*" as recited in claim 4. TSMC-1003, ¶105 (citing TSMC-1030, 1:57-2:18; TSMC-1031, [0001]). The '735 Patent similarly discloses that "[t]he insulation material layer 103 is made of, for example, silicon oxide and formed, for example, in a thermal oxidizing process." *Cf.*, TSMC-1001, 4:34-36; *see also* TSMC-1003, ¶¶104-105 (citing TSMC-1029, [0005], [0029], Title; TSMC-1028, 1:65-2:7).

**(d) Claim 5**

***[5] The semiconductor device as claimed in claim 1, wherein the source/drain region is a doped region or an epitaxial layer.***

Chuang further discloses this limitation. TSMC-1003, ¶106. For example, Chuang discloses that "source/drain regions 106 includ[e] lightly doped source/drain regions and heavy doped source/drain regions." TSMC-1004, [0022]; *see also id.*, [0016], [0022], FIG. 9.

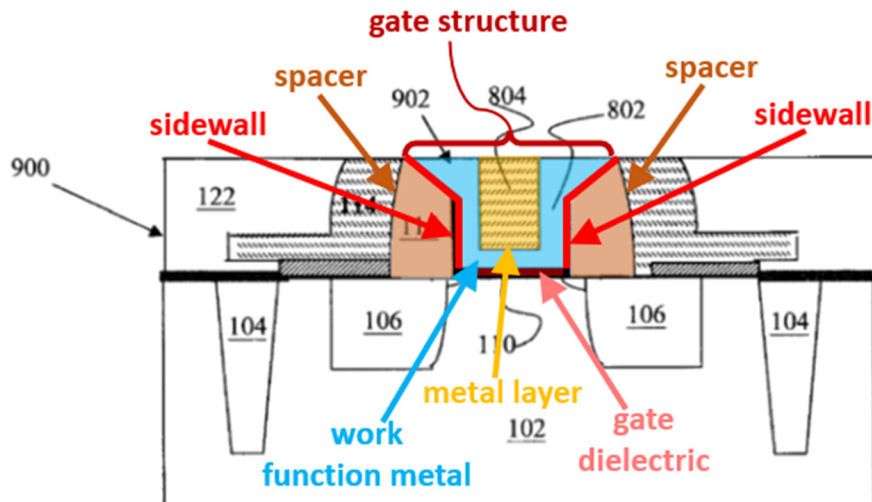


Chuang, FIG. 9 (annotated)

(e) Claim 6

**[6] The semiconductor device as claimed in claim 1, further comprising a spacer disposed on a sidewall of the gate structure.**

Chuang discloses this limitation. TSMC-1003, ¶¶107-108. FIG. 9, for example, shows spacers 116 disposed on opposing sidewalls of gate structure 902:



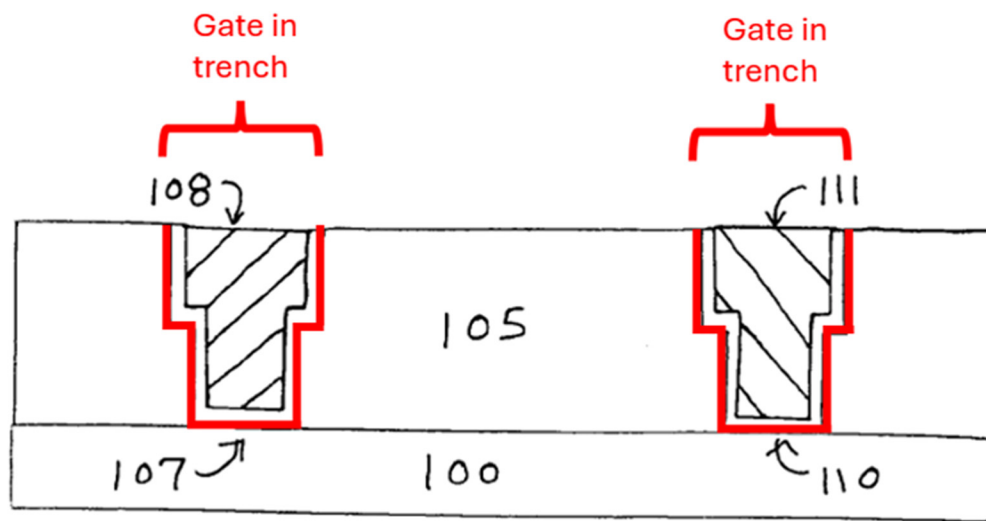
Chuang, FIG. 9 (annotated)

Chuang also discloses that “spacers 116 may be formed on both sidewalls of the dummy gate structure 118.” TSMC-1004, [0020]; *see also id.*, [0037], FIGs. 10-11.

**B. [GROUND 1B] – Chuang in view of Brask Renders Obvious  
Claim 2**

**1. Overview of Brask**

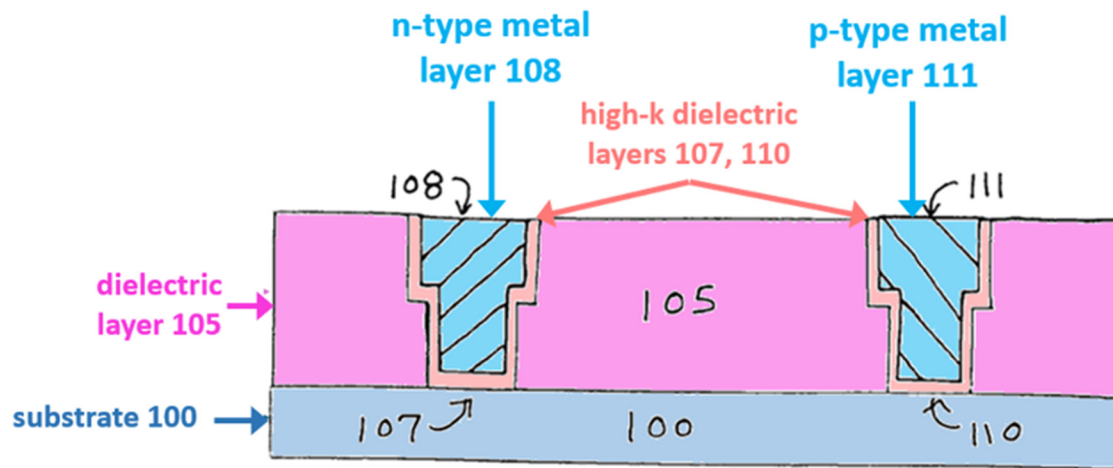
Like the '735 Patent, Brask discloses a gate structure for a complementary metal-oxide semiconductor (CMOS) transistor disposed in a trench having a neck, where the top of the trench is wider than the neck to promote void-free metal deposition in the trench:



TSMC-1012, FIG. 11 (annotated)

*See also id.*, 1:7-20, 1:31-38, 1:58-63, 2:64-67, 3:14-21, 4:10-18, cls. 1, 9; TSMC-1003, ¶¶66-73.

Brask discloses several embodiments, but only illustrates one of them in detail. TSMC-1012, FIGs. 1a-11. In this embodiment, the gate structure, which is disposed in a dielectric layer 105, includes a high-k dielectric 107/110 and a single metal layer in each trench, namely an n-type metal layer 108 or a p-type metal layer 111, as shown:

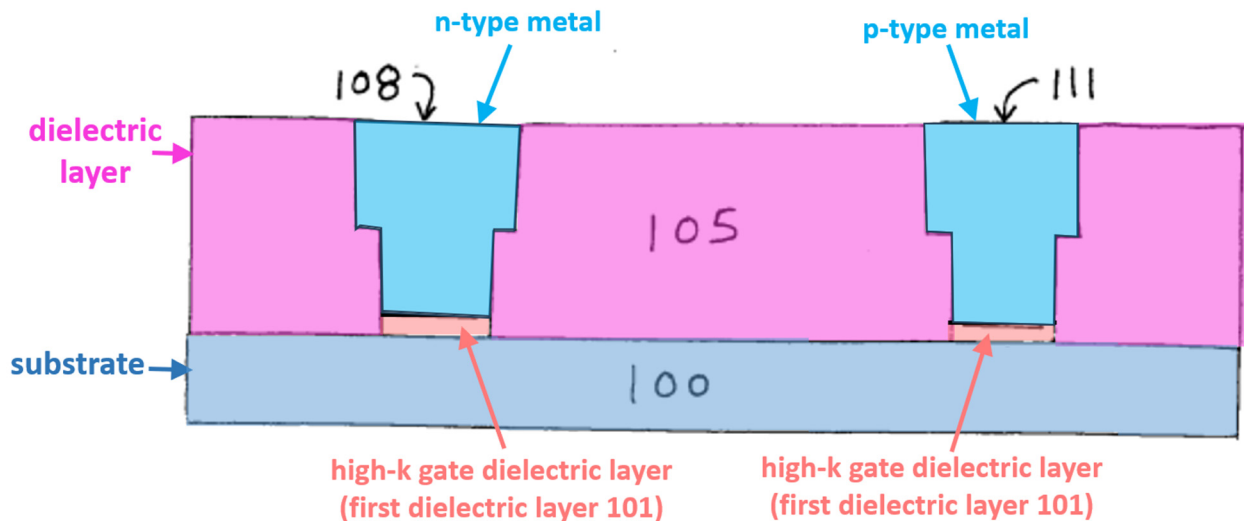


TSMC-1012, FIG. 11 (annotated).

This IPR is notably based not on the embodiment illustrated above, but rather on an alternative embodiment that differs from the illustrated embodiment in two ways relative to the high-k dielectric and metal layer elements. TSMC-1003, ¶¶67.

First, Brask discloses that the high-k dielectric 107/110 (which completely lines the trench) could be substituted for a high-k dielectric 101, which lines only the bottom of the trench. TSMC-1012, 7:3-6 (“In an alternative embodiment, first dielectric layer 101 may comprise a high-k gate dielectric layer”). “In that alternative embodiment, metal layers 108 and 111 are formed directly on first dielectric layer

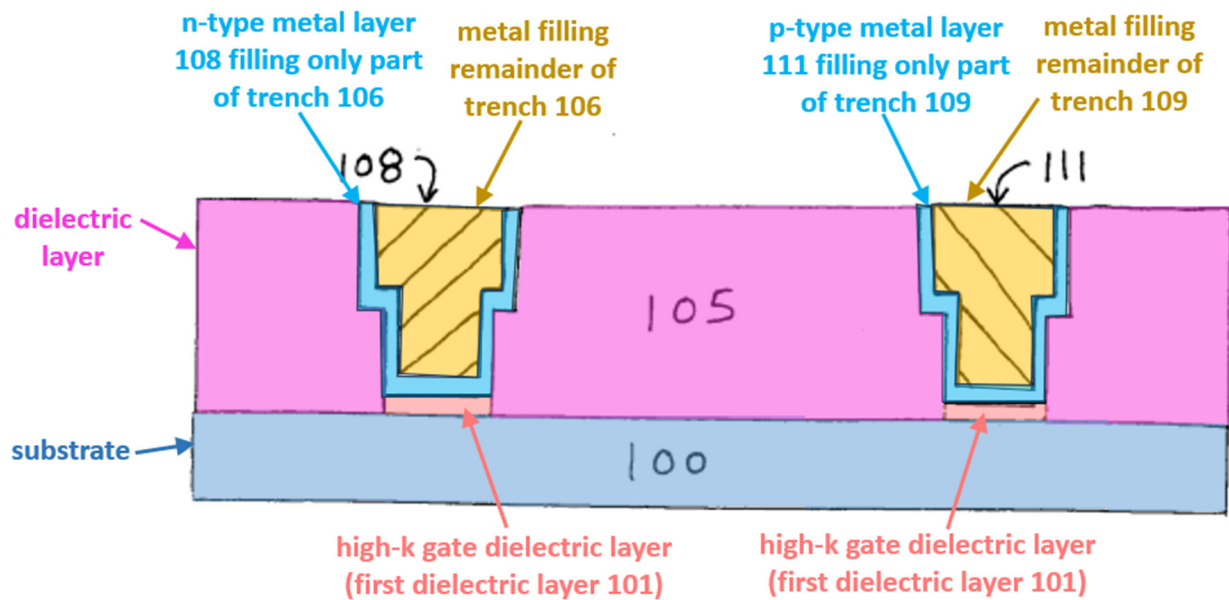
101, without first replacing first dielectric layer 101 with a high-k gate dielectric layer.” *Id.*, 7:6-9. Dr. Lee illustrated this alternative configuration of the high-k dielectric layer, based on a modification of FIG. 11:



TSMC-1003, ¶¶68-69 (showing annotated and modified version of Brask Fig. 11).

Second, Brask discloses the option of filling the trench with multiple metal layers to form the gate structure, rather than the single n-type metal 108 or p-type metal 111 used in the illustrated embodiment. Specifically, Brask teaches that “n-type metal layer 108 may fill only part of trench 106, with the remainder of the trench being filled with a material that may be easily polished, e.g., tungsten, aluminum, titanium, or titanium nitride.” TSMC-1012, 6:7-12. Likewise, “in alternative embodiments, p-type metal layer 111 may fill only part of trench 109” and “the remainder of the trench may be filled with a material that may be easily polished, e.g., tungsten,

aluminum, titanium, or titanium nitride.” *Id.*, 6:54-60. Dr. Lee illustrated this embodiment as follows, retaining the high-k gate dielectric 101 at the bottom of the trench as discussed above:



TSMC-1003, ¶¶70-72 (showing annotated and modified version of Brask Fig. 11).

For purposes of this Petition, this illustration and the associated disclosure in Brask are referred to as Brask’s “Representative Embodiment.” As explained below, Grounds 1B, 2B, and 3A-3B map Brask’s Representative Embodiment to the Challenged Claims and explain why it both anticipates and renders them obvious. TSMC-1003, ¶¶109, 173, ¶181, ¶204, ¶209.

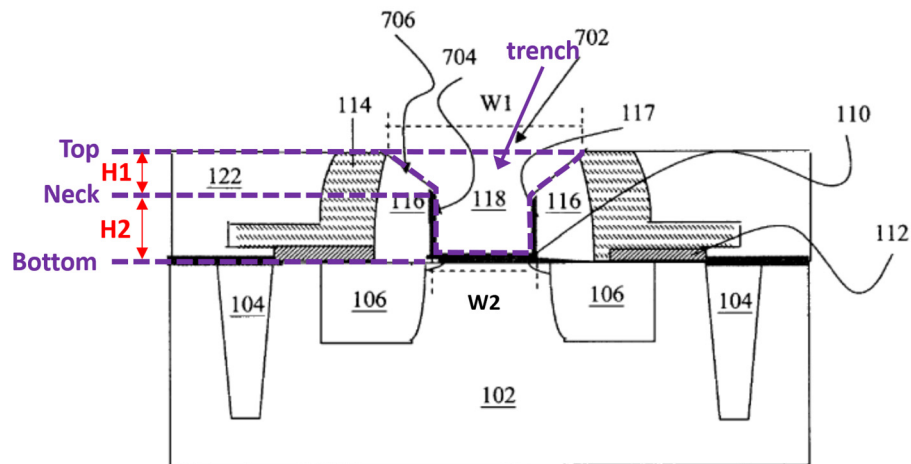
## 2. Analysis

Chuang in view of Brask renders obvious claim 2 of the ’735 Patent. TSMC-1003, ¶109.

**(a) Claim 2**

***[2] The semiconductor device as claimed in claim 1, wherein the top and the neck have a first height therebetween, the neck and the bottom have a second height therebetween, and a ratio of the first height to the second height is substantially 2:1.***

The combination of Chuang and Brask renders claim 2 obvious. TSMC-1003, ¶¶110-117. As discussed in Ground 1A, Chuang discloses a trench 702 (**trench**) that includes an aperture (**top**), a bottom (**bottom**), and a **neck** between the top and the bottom. TSMC-1004, [0002]-[0006], [0019], [0024], [0028], [0030]-[0032], [0041], FIGs. 7, 9; *supra* Ground 1A, [1.5]-[1.7]; TSMC-1003, ¶110. Chuang's trench is illustrated in the figure below:



Chuang, FIG. 7 (annotated)

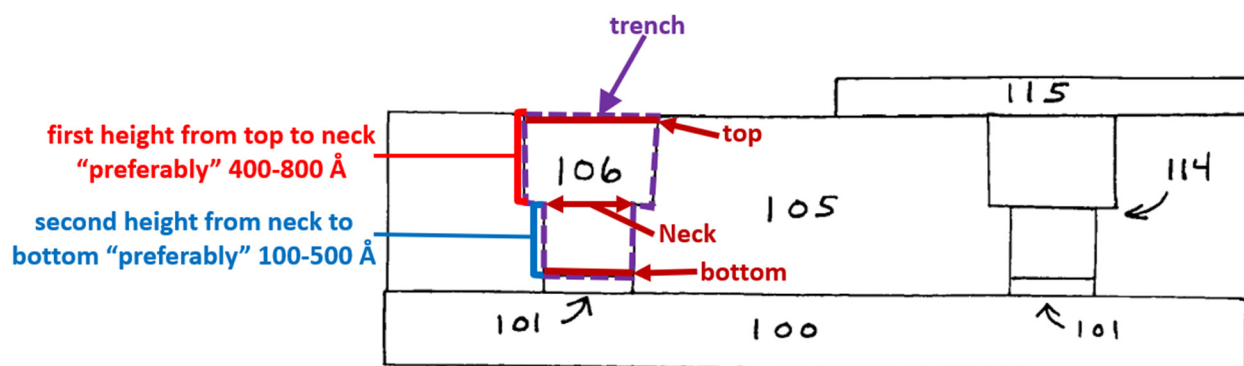
As shown, the top and neck of Chuang's trench 702 have a first height (H1) therebetween and the neck and the bottom of Chuang's trench 702 have a second height (H2) therebetween. *Id.*

Chuang discloses its trench broadly, not placing any limitation on the relative heights of its trench segments. To the extent that PO argues that Chuang does not expressly disclose the claimed 2:1 height ratio, Brask discloses it. TSMC-1003, ¶111.

A POSITA would have looked to Brask to supply information regarding appropriate heights for the Chuang trench segments. TSMC-1003, ¶¶112-117. Brask expressly discloses trench segment height ranges that include the claimed substantially 2:1 height ratio. Specifically, Brask discloses that the upper trench segment “preferably is between about 400 and about 800 angstroms” and the lower trench segment “preferably is between about 100 and about 500 angstroms.”<sup>8</sup> TSMC-1012, 2:15-27. This is illustrated below:

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<sup>8</sup> As Dr. Lee explains, Brask’s trenches are formed by (1) stacking two layers 102/103 of material having different widths to form “sacrificial” structures 104/114, (2) surrounding the sacrificial structures 104/114 with dielectric 105; and (3) removing the sacrificial structures 104/114, thereby leaving trenches 106/109 within dielectric 105 that have the same size and shape as the sacrificial structures 104/114. TSMC-1012, 2:4-3:43, FIGs. 1a-1e; TSMC-1003, ¶¶73, 112.



Brask, FIG. 1e (annotated)

Brask's trench segment height ranges encompass many examples of the claimed substantially 2:1 ratio. Among others, a first height of 400 angstroms and a second height of 200 angstroms satisfies this limitation, as does a first height of 600 angstroms and a second height of 300 angstroms. In fact, a 600 angstroms/300 angstroms combination would be the result if a POSITA simply applied the midpoint of each of the two ranges (400-800 angstroms and 100-500 angstroms). Brask thus discloses the claimed "***ratio of the first height to the second height is substantially 2:1.***" TSMC-1003, ¶113.

Brask's disclosure also renders the claimed substantially 2:1 height ratio obvious. TSMC-1003, ¶114. It is well settled that a claimed property or range is obvious where it overlaps or lies inside ranges disclosed by the prior art, which is the case here. *In re Wertheim*, 541 F.2d 257 (CCPA 1976); *In re Woodruff*, 919 F.2d 1575 (Fed. Cir. 1990); *In re Geisler*, 116 F.3d 1465, 1469-71 (Fed. Cir. 1997); *In re Peterson*, 315 F.3d 1325, 1330 (Fed. Cir. 2003); *In re Harris*, 409 F.3d 1339 (Fed.

Cir. 2005); MPEP § 2144.05. Moreover, the '735 Patent attributes no criticality, benefit, or unexpected result to the “substantially 2:1” height ratio recited in claim 2. *See* TSMC-1001, 5:27-31, 9:21-35. This feature instead reflects a mere design choice that would have been obvious to try and arrive at through routine experimentation, as discussed below. *E.I. du Pont de Nemours & Co. v. Synvina C.V.*, 904 F.3d 996, 1008 (Fed. Cir. 2018) (“[I]n the absence of evidence indicating that there is something special or critical about the claimed range, an overlap suffices to show that the claimed range was disclosed in—and therefore obvious in light of—the prior art.”); TSMC-1003, ¶¶115. The combination of Chuang and Brask thus renders claim 2 obvious, with Chuang supplying the basic overall structure of the device, and Brask supplying the 2:1 height ratio limitation. *Id.*

Further establishing obviousness, a POSITA would have looked to Brask as disclosing the basic height ranges under which a device like Chuang’s would be expected to work. TSMC-1003, ¶116. A POSITA would have experimented with Brask’s ranges to optimize Chuang’s device. *Id.* As noted above, a POSITA simply using the midpoint of the first range (600 angstroms, the midpoint of 400-800 angstroms) and the midpoint of the second range (300 angstroms, the midpoint of 100-500 angstroms) would result in a device satisfying the 2:1 height ratio limitation. *Id.*

Such optimization would have been obvious because the height ratio was known to impact both the electrical characteristics of the transistor and the quality

of the metal fill in the trench. TSMC-1003, ¶117. In this context, a POSITA would have engaged in routine experimentation involving adjustments to the height ratio to optimize these characteristics. *Id.* Achieving a substantially 2:1 ratio through routine experimentation would have been obvious and predictable in at least some implementations of the Chuang-Brask device, as evidenced by the preferred heights disclosed in Brask. *Id.* A POSITA would have reasonably expected success because a myriad of designs were known before the Critical Date that used various height ratios, including substantially 2:1. *Id.*

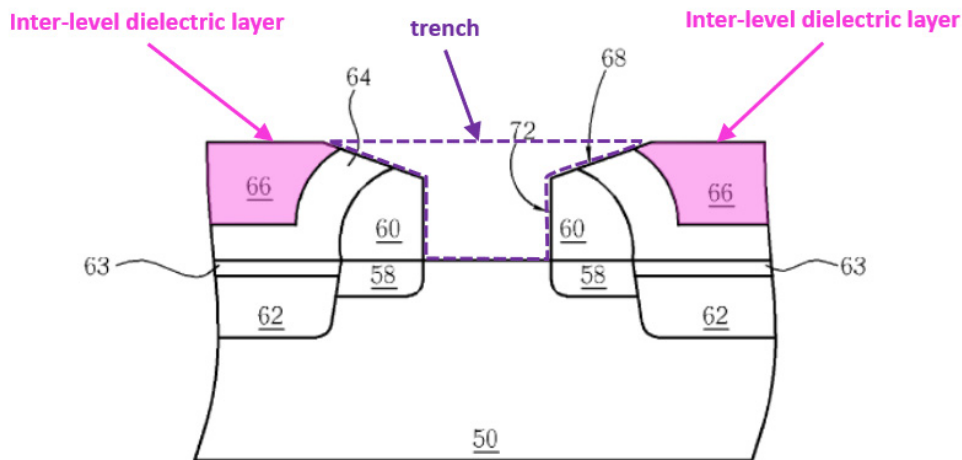
Finally, court decisions confirm the obviousness of claim 2 in light of this combination. Specifically, courts have held that, “where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation.” *E.I. du Pont*, 904 F.3d at 1006; *see also In re Peterson*, 315 F.3d at 1329 (Fed. Cir. 2003); *In re Brandt*, 886 F.3d 1171, 1176-1177 (Fed. Cir. 2018); *Titanium Metals Corp. v. Banner*, 778 F.2d 775, 783 (Fed. Cir. 1985); *In re Aller*, 220 F.2d 454, 456 (CCPA 1955)); MPEP §2144.05.

Accordingly, the Chuang-Brask combination discloses and renders obvious claim 2. TSMC-1003, ¶¶110-117.

## C. [GROUND 2A] – Lin Anticipates Claims 1 and 3-6

### 1. Overview of Lin

Similar to the '735 Patent, Lin discloses “a method of manufacturing a metal oxide semiconductor transistor with a Y structure metal gate.” TSMC-1005, [0002]; *see also* TSMC-1003, ¶¶63-65 (citing TSMC-1005, [0004]-[0008], [0012], [0020], [0024], [0025]). FIG. 4 illustrates the Y-shaped recess (*e.g.*, trench) in which Lin’s metal gate structure is formed, in an embodiment:



Lin, FIG. 4 (annotated)

### 2. Analysis

Lin anticipates each of claims 1 and 3-6 of the '735 Patent.<sup>9</sup> TSMC-1003, ¶¶118-119.

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<sup>9</sup> *Supra*, Footnote 1.

(a) Claim 1

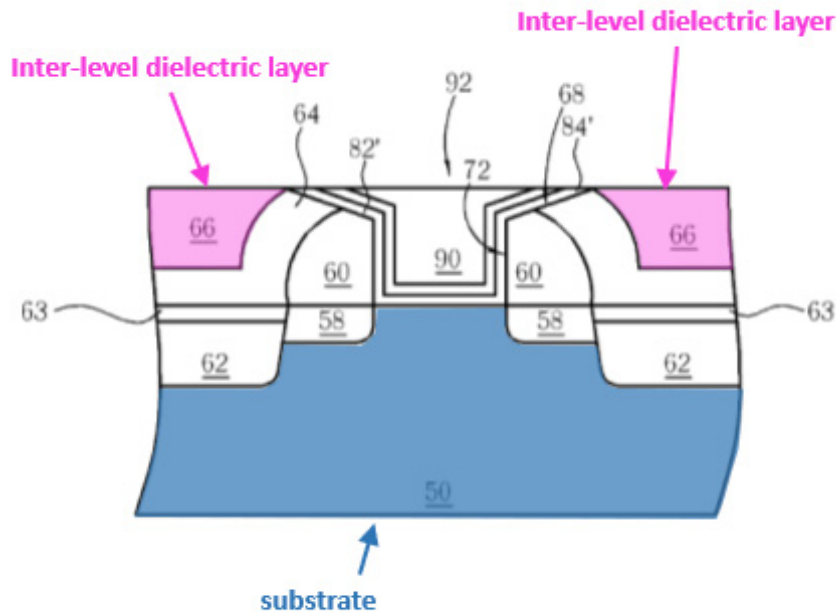
***[1.pre] A semiconductor device comprising:***

To the extent the preamble is limiting, Lin discloses this limitation. TSMC-1003, ¶120. For example, Lin describes a “method of manufacturing a metal oxide semiconductor transistor having a metal gate is provided.” TSMC-1005, Abstract; *see also id.*, [0009], Cl. 17. The transistor provides a “***semiconductor device***” as claimed. TSMC-1003, ¶120.

***[1.1] a substrate, disposed with a dielectric layer thereon,***

Lin discloses this limitation. TSMC-1003, ¶121-125. For example, Lin discloses an inter-level dielectric (ILD) layer (***dielectric layer***) disposed on a substrate (***substrate***). TSMC-1005, [0018], [0019], [0028], [0030].

FIG. 6 depicts a substrate 50 with an ILD layer 66 disposed thereon:

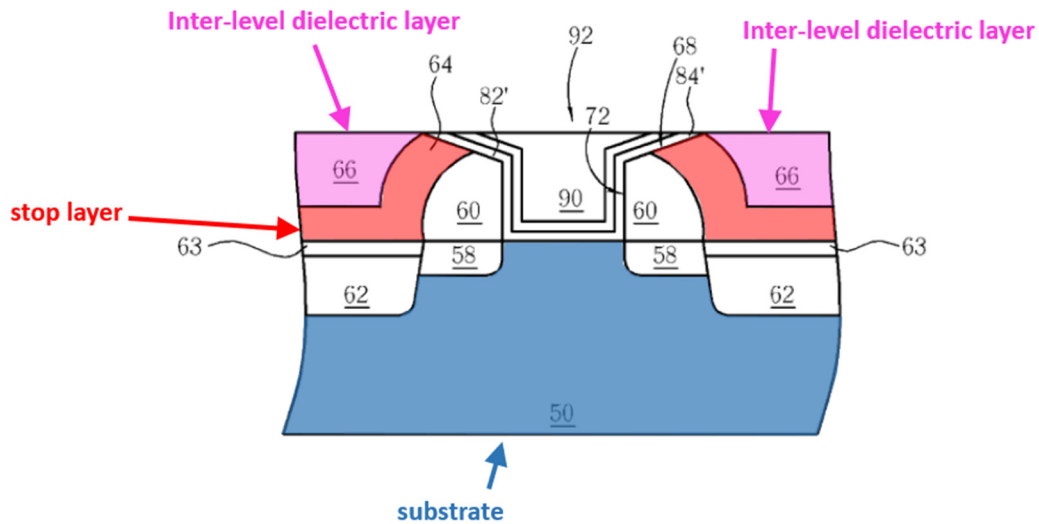


Lin, FIG. 6 (annotated)

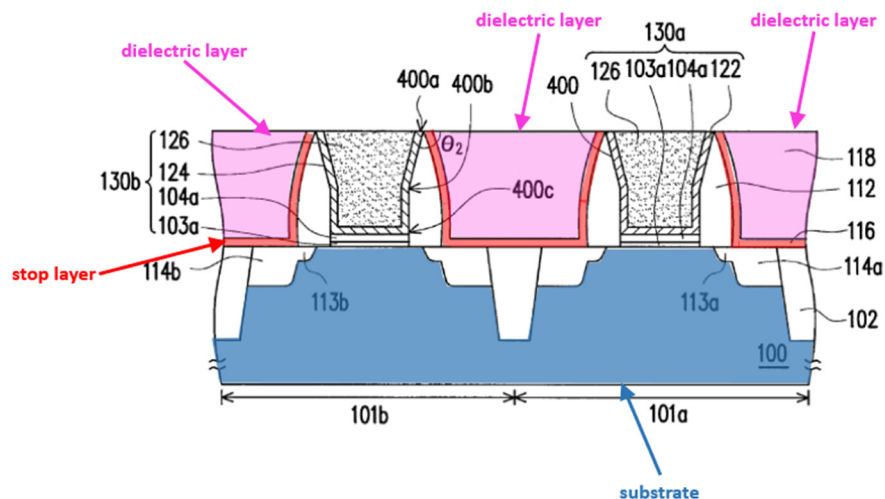
Lin discloses that “[t]he substrate 50 is made from semiconductor materials, such as silicon substrate, Si-containing substrate, or silicon-on-insulator (SOI).” TSMC-1005, [0018]. “[T]he ILD layer 66 is made by silicon oxide, or doped silicon oxide comprising phosphosilicate glass (PSG) or borophosphosilicate glass (BPSG).” *Id.*, [0019]; *see also* TSMC-1003, ¶125 (mapping corresponding elements in a second embodiment and citing TSMC-1005, [0028], [0030], FIG. 10).

Lin’s disclosure that the ILD layer 66 “covers” a “contact etch stop layer (CESL) 64” noticeably aligns with the preferred embodiments of the ’735 Patent, which similarly provide a stop layer 116 “formed on the substrate 100.” *Compare* TSMC-1005 at [0019]-[0020] & FIG. 6 *with* TSMC-1001, at 7:12-28 & FIG. 4. The specification of the ’735 Patent thus confirms that a substrate is disposed with a

dielectric layer thereon, notwithstanding the presence of a stop layer like Lin's CESL 64. *See* TSMC-1001, 7:23-25 ("Afterwards, a dielectric layer 118 is formed on the substrate 100 as an interlayer dielectric (ILD) layer."), 4:4-10 ("stop players, and the like are all fabricated with techniques known to people skilled in the art based on conventional arts"), 8:43-45 & FIGs. 1E, 4 ("The dielectric layer 118 is disposed on the substrate 100"); TSMC-1003, ¶124.



Lin, FIG. 6 (annotated)



'735 Patent, FIG. 4 (annotated)

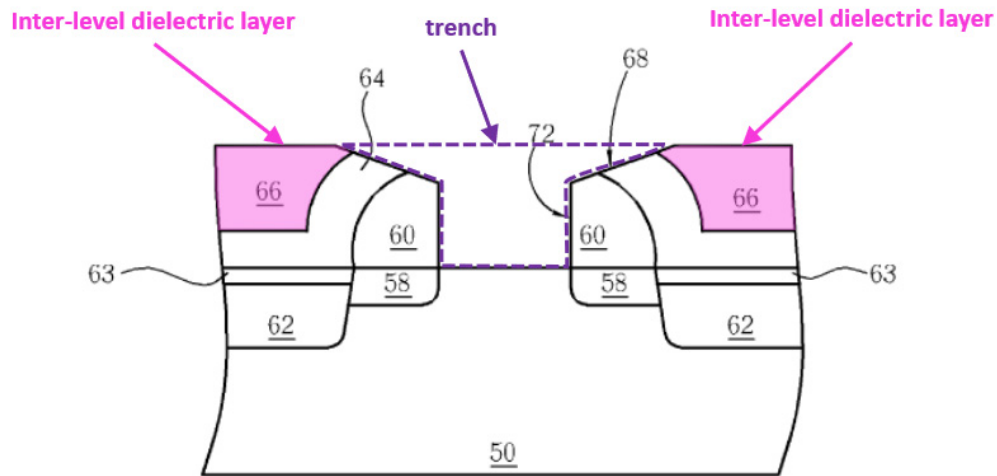
***[1.2] wherein a trench is disposed in the dielectric layer;***

Lin discloses this limitation. TSMC-1003, ¶¶126-131 For example, Lin discloses a recess 72 (***trench***) disposed in ILD layer 66 (***dielectric layer***).<sup>10</sup> TSMC-1005 [0023]-[0025]; *see also* TSMC-1003, ¶130 (mapping corresponding elements in the second embodiment and citing TSMC-1005, [0031], [0035], FIG. 9). Lin discloses “a recess 72 is formed by an etching process to remove the gate temporary layer ...” *Id.*, [0023]; *see also id.*, Abstract, [0031].

FIG. 4 depicts Lin’s recess 72 (***trench***) disposed in ILD layer 66 (***dielectric layer***):

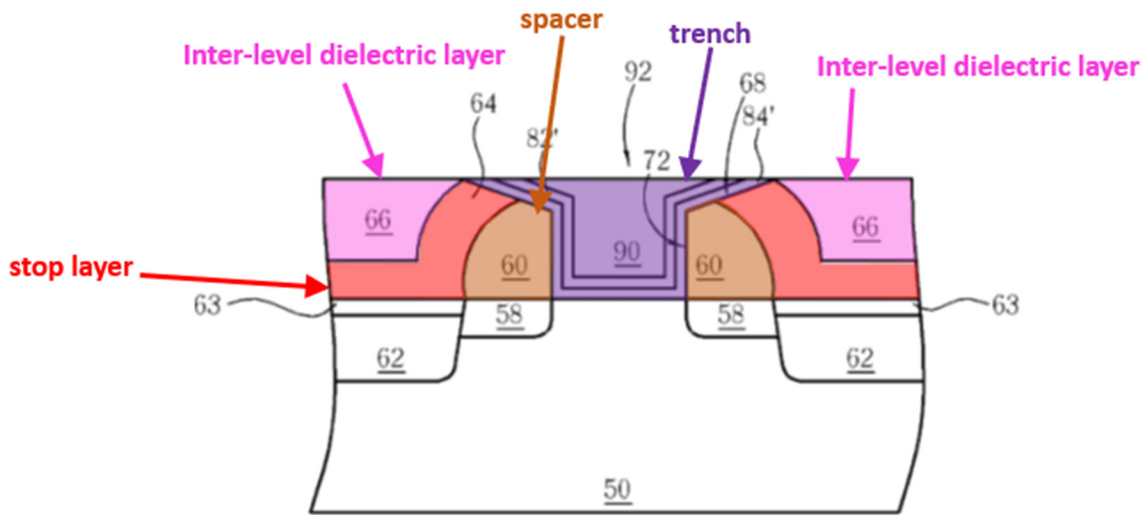
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<sup>10</sup> This Petition treats the entire Y-shaped opening in which Lin’s metal gate is formed as the “recess” corresponding to the claimed “***trench***.” References in this Petition to Lin’s recess 72 should be understood to further include the areas defined by bevel edges 68. TSMC-1005, [0025]-[0026]; *see also id.*, [0032]-[0033]; TSMC-1003, ¶126, Footnote 11.

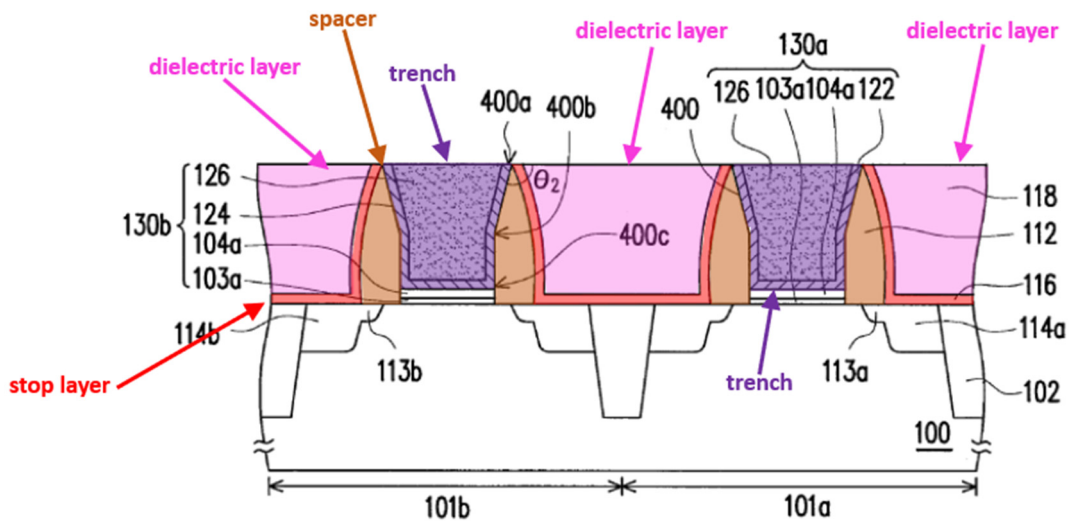


Lin, FIG. 4 (annotated)

For comparison, like Lin's device, the '735 Patent's device includes a trench 400 "disposed in" a dielectric layer 118 notwithstanding the presence of intervening spacers 112 and stop layer 116. *Cf.*, TSMC-1001, FIG. 4, 9:36-58; *see also id.*, claim 6 ("a spacer disposed on a sidewall of the gate structure"), 8:43-45 ("The dielectric layer 118 is disposed on the substrate 100, and the trenches 120 are disposed in the dielectric layer 118."). The following figures illustrate the like configurations of recess 72 (**trench**) disposed in ILD layer 66 (**dielectric layer**) and the '735 Patent's trench 120 disposed in dielectric layer 118, flanked similarly by spacers and a stop layer:



Lin, FIG. 6 (annotated)

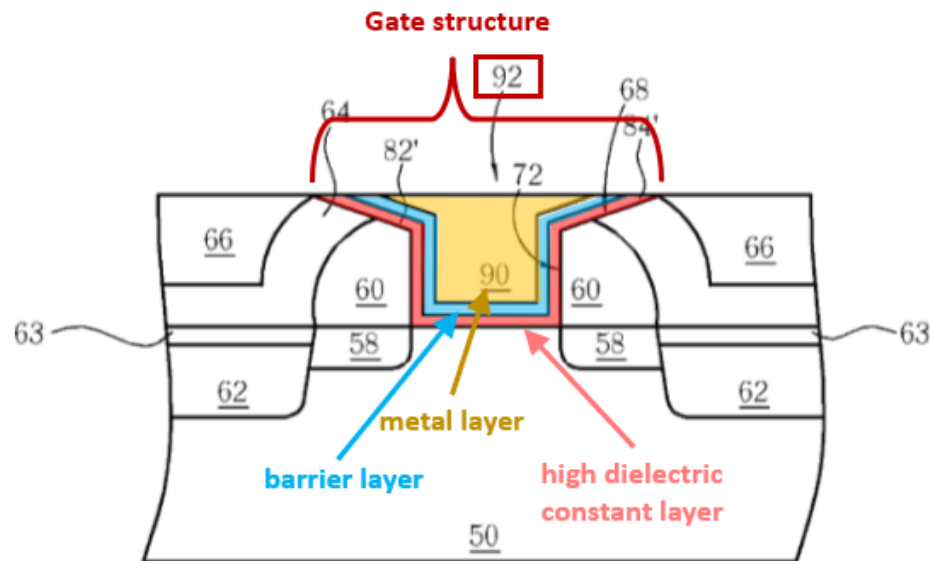


'735 Patent, FIG. 4 (annotated)

See also TSMC-1003, ¶¶82-83, 131 (citing TSMC-1004, [0024], [0028], [0030]-[0032], [0036], FIGs. 3, 6); see also TSMC-1003, ¶¶ 128-129, 131 (explaining the similarities between the structures in Lin and the '735 patent).

***[1.3.i] a gate structure, located in the trench and comprising***

Lin discloses this limitation. TSMC-1003, ¶¶132-134. For example, Lin discloses a metal gate 92 (*gate structure*) having a “High-k materials layer,” a “barrier layer,” and a “conductive layer” located in the recess 72 (*trench*). TSMC-1005, [0026]; *see also* TSMC-1003, ¶134 (mapping corresponding elements in the second embodiment and citing TSMC-1005, FIG. 10, [0033]). FIG. 6 depicts Lin’s metal gate 92 (*gate structure*) located in the recess 72 (*trench*):



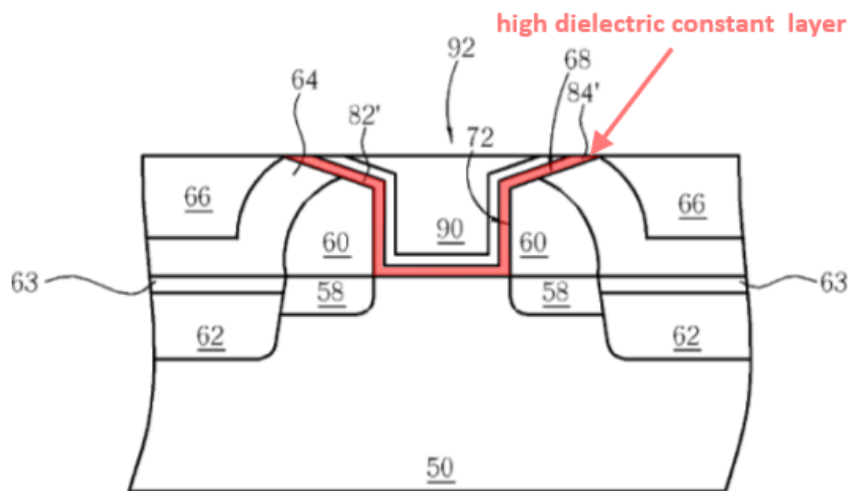
Lin, FIG. 6 (annotated)

***[1.3.ii] [a gate structure ... ] comprising a high dielectric constant layer,***

Lin discloses this limitation. TSMC-1003, ¶¶135-138. For example, Lin discloses a “high dielectric constant (High-k) material layer 82” formed “in the inter sidewall of the recess 72, and on the bevel edge 68 and the ILD layer 66.” TSMC-

1005, [0024]. After further processing, “[t]he metal gate 92” (*gate structure*) is formed and the portion of High-K material layer 82 that remains is referred to as “High-k materials layer 82” (*high dielectric constant layer*). *Id.*, [0026]; TSMC-1003, ¶137-138 (mapping corresponding elements in the second embodiment and citing TSMC-1005, [0033]-[0034], FIG. 10 ).

FIG. 6 depicts Lin’s metal gate 92 (*gate structure*) including remaining high dielectric constant (High-k) material layer 82’ (*high dielectric constant layer*):



Lin, FIG. 6 (annotated)

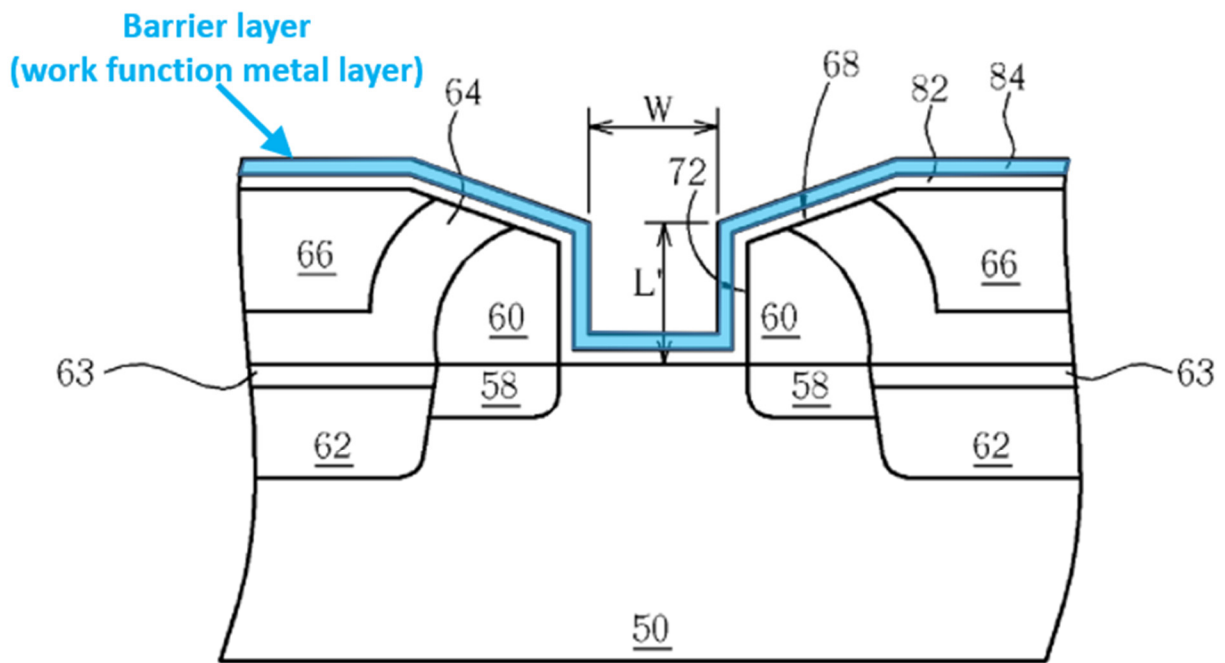
**[1.3.iii] [a gate structure ... comprising ... ] a work function metal layer, and**

Lin discloses this limitation. TSMC-1003, ¶¶139-143. For example, Lin discloses a barrier layer 84 that provides work function adjustment properties as claimed:

The barrier layer 84 material could be selected from a

group of metal comprising refractory, noble, and lanthanide series elements such as Ti, Ta, Mo, Ru, and W and their aluminates and silicates and nitrogen or carbon incorporated, such as TiN, TaN, TaSiN, TaC, MoAlN, . . . etc. Some of the barrier layer 84 has the work function adjustment properties for threshold voltage tuning.

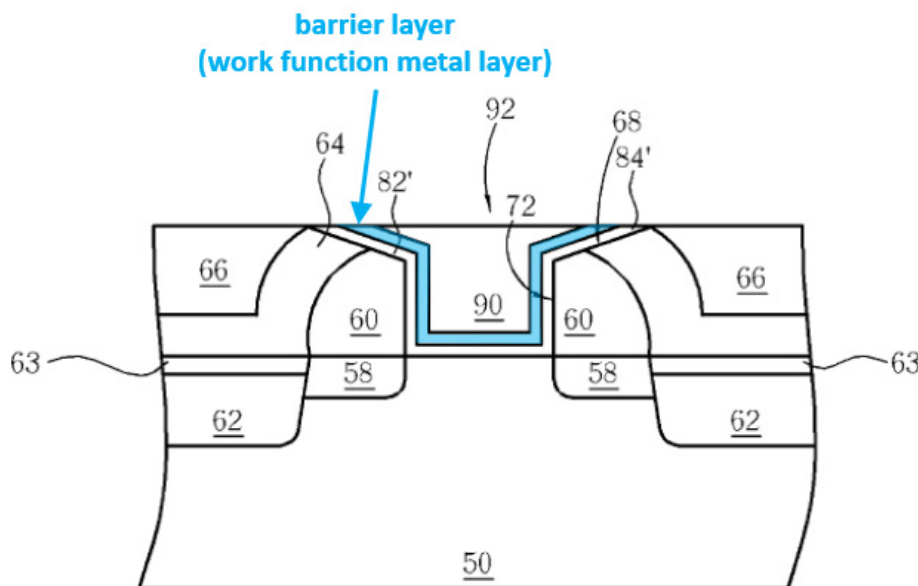
TSMC-1005, [0024]; *see also id.*, [0026]; TSMC-1003, ¶142 ( mapping corresponding elements in the second embodiment and citing TSMC-1005, [0033]-[0034], FIG. 10). FIG. 5 depicts the barrier layer 84 formed over High-k material layer 82:



Lin, FIG. 5 (annotated)

After further processing of the device, a barrier layer 84' (*work function metal layer*) remains that retains the work adjustment properties of the original barrier layer 84 described above. TSMC-1005, [0024]-[0026]. FIG. 6 depicts Lin's metal

gate 92 (*gate structure*) including remaining barrier layer 84' (*work function metal layer*):



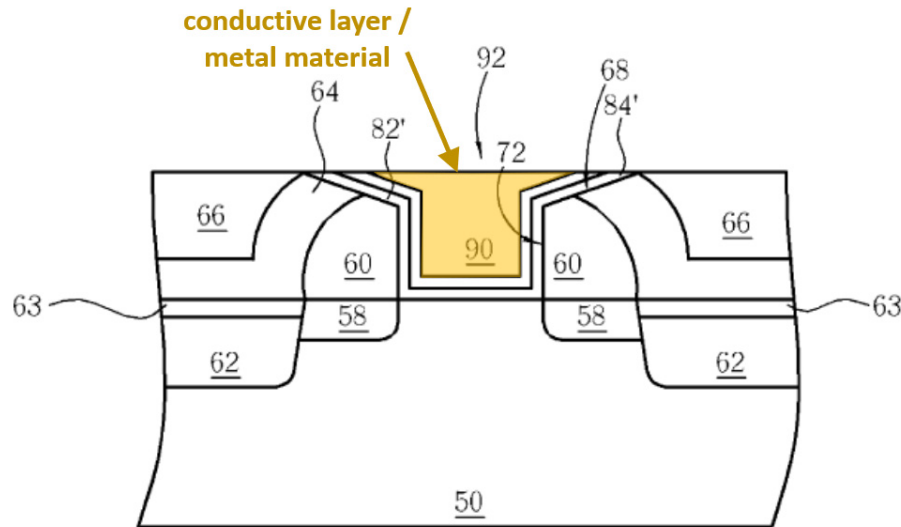
Lin, FIG. 6 (annotated)<sup>11</sup>

Lin also discloses an optional “work function adjusting layer.” TSMC-1005, [0024] (“for those barrier layer 84 without work function adjustment properties, a work function adjusting layer (not shown) is formed on the barrier layer 84.”); *see also id.*, [0034], Claim 15, Claim 27; TSMC-1003, ¶143.

<sup>11</sup> Lin erroneously directs reference numeral 84' (remaining barrier layer) in FIG. 6 to the underlying high dielectric constant layer, which is also labeled as 82'. Annotated figure 6 correctly highlights in blue the layer “formed on” the high-K material layer 82/82' as the barrier layer 84', consistent with the written description and FIG. 5. TSMC-1003, ¶¶140-141, Footnote 12; *see also* [0024]-[0026], FIGs. 5-6.

**[1.3.iv] [a gate structure ... comprising ... ] a metal layer;**

Lin discloses this limitation. TSMC-1003, ¶¶144-145. For example, Lin’s conductive layer 90 of metal gate 92 (*gate structure*) is a “*metal layer*” as claimed:

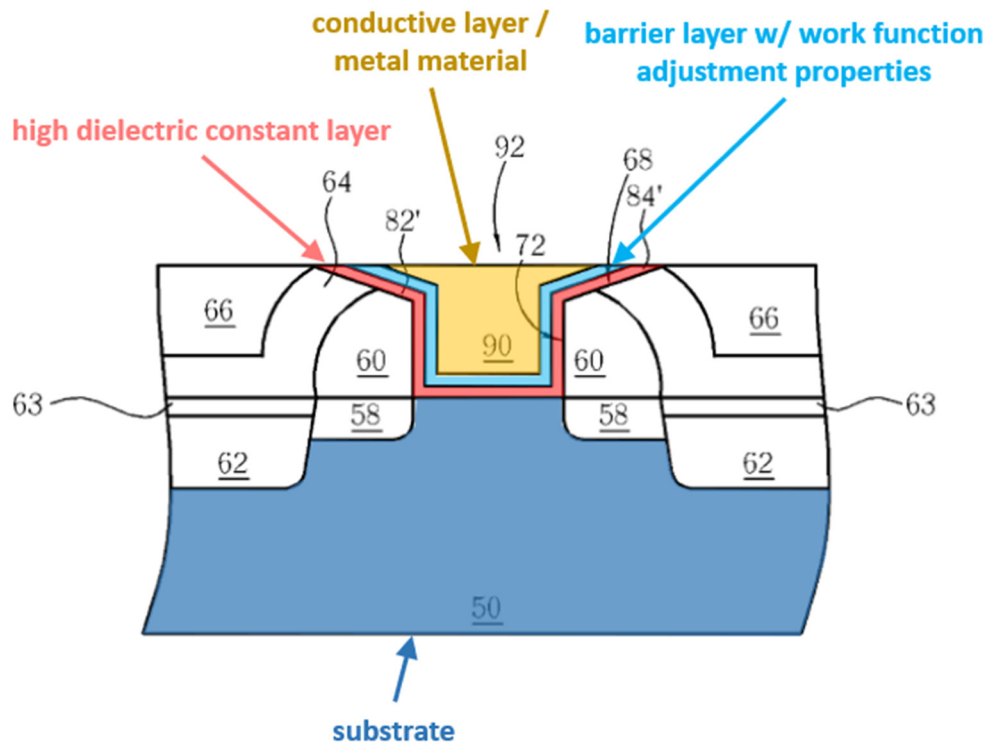


Lin, FIG. 6 (annotated)

*See* TSMC-1005, [0026] (“After the barrier layer 84 is formed, a conductive layer (not shown) is formed on the ILD layer 66 and the bevel edge 68, where the recess 72 is filled with the conductive layer. The conductive layer (not shown) is made by a metal material or compound comprising tungsten (W), titanium nitride (TiN), and titanium tungsten (TiW), . . . etc. . . . The metal gate 92 is formed and consists of the remaining High-k materials layer 82', the remaining barrier layer 84', and the remaining conductive layer 90 in the recess 72 and the bevel edge 68.”); *see also* TSMC-1003, ¶145 (mapping corresponding elements in the second embodiment and citing TSMC-1005, FIG. 10, [0033], [0035]).

**[1.3.v] sequentially disposed on the substrate;**

Lin discloses this limitation. TSMC-1003, ¶146-149. For example, the order of layers shown in FIG. 6 illustrates how the remaining high dielectric constant (High-k) material layer 82' (**high dielectric constant layer**), remaining barrier layer 84' (**work function metal layer**), and remaining conductive layer 90 (**metal layer**) are sequentially disposed on substrate 50 (**substrate**):



Lin, FIG. 6 (annotated)

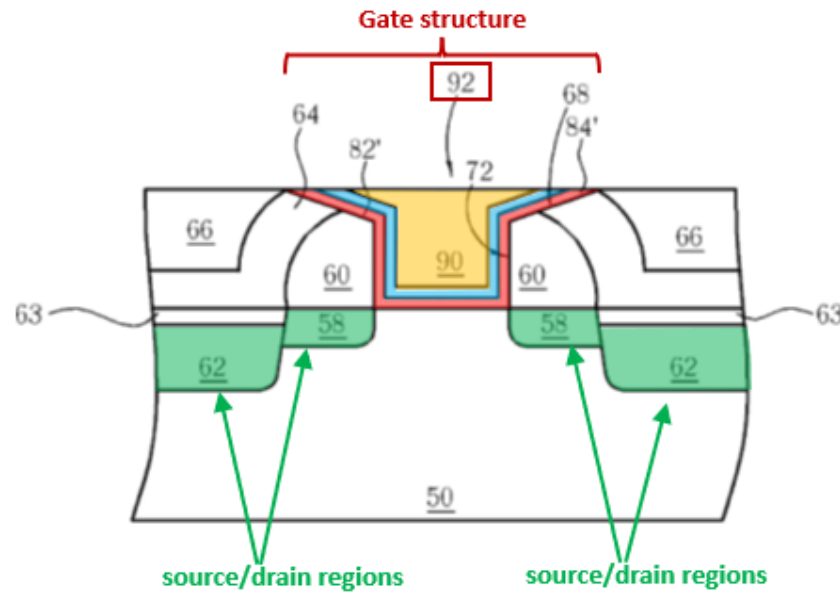
See also TSMC-1005, [0024] (“After the High-k material layer 82 is formed, a barrier layer 84 is formed on the High-k material layer 82 surface.”), [0026] (“After the barrier layer 84 is formed, a conductive layer (not shown) is formed

on the ILD layer 66 and the bevel edge 68, where the recess 72 is filled with the conductive layer.”); *see also* TSMC-1003, ¶148 (mapping corresponding elements in the second embodiment and citing TSMC-1005, FIG. 10, [0033]).

For configurations that provide a work function adjusting layer separate from the barrier layer, the high dielectric constant layer, work function adjusting layer, and conductive layers are also “*sequentially disposed*” on Lin’s substrate. TSMC-1005, [0024] (“[F]or those barrier layer 84 without work function adjustment properties, a work function adjusting layer (not shown) is formed on the barrier layer 84.”); *see also id.*, [0034]; *supra* Ground 2A, [1.3.i]-[1.3.iv]; TSMC-1003, ¶149.

***[1.4] a source/drain region, disposed in the substrate at respective sides of the gate structure,***

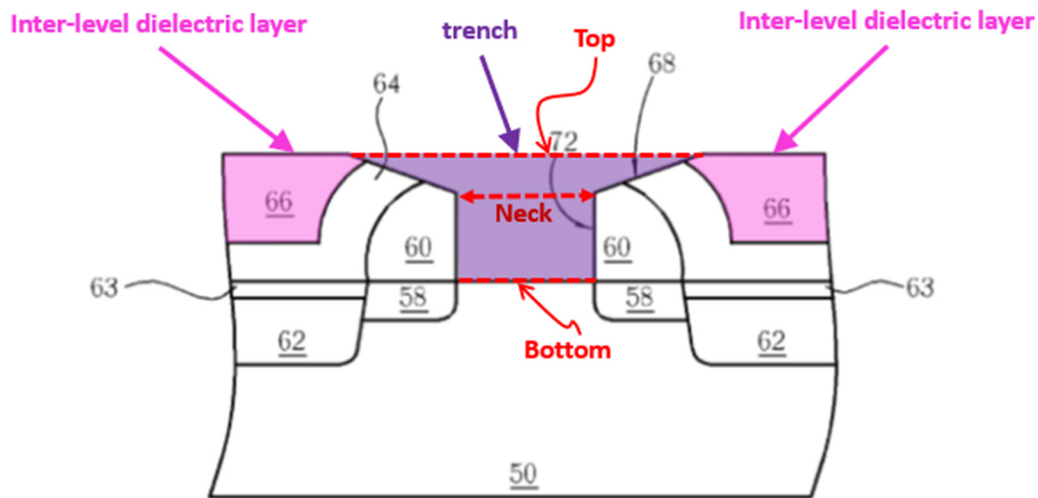
Lin discloses this limitation. TSMC-1003, ¶¶150-151. For example, Lin discloses that “lightly doped drains 58 (LDDs, also called lightly doped sources) and source/drain dopants 62 are formed in two sides of the gate structure 57 in the substrate 50.” TSMC-1005, [0019]; *see also* TSMC-1003, ¶151 (mapping corresponding elements in the second embodiment and citing TSMC-1005, [0029], FIG. 10). FIG. 6 depicts the source/drain region:



Lin, FIG. 6 (annotated)

**[1.5] wherein the trench comprises a top, a bottom, and a neck arranged between the top and the bottom,**

Lin discloses this limitation. TSMC-1003, ¶¶152-154. As discussed above in the analysis of [1.2], Lin's semiconductor device includes a recess including beveled edges (*e.g.*, recess 68+72) (***trench***) disposed in a ***substrate*** (*e.g.*, substrate 50). *Supra*, Ground 2A at [1.2]. Lin's recess (***trench***) includes a ***top***, a ***bottom***, and a ***neck*** arranged between the top and the bottom. FIG. 4 shows these aspects of the recess 72:



Lin, FIG. 4 (annotated)

See TSMC-1005, [0020], [0023], [0025]; see also TSMC-1003, ¶153 (mapping corresponding elements in the second embodiment and citing TSMC-1005, [0031]-[0032], [0035], FIG. 9) .

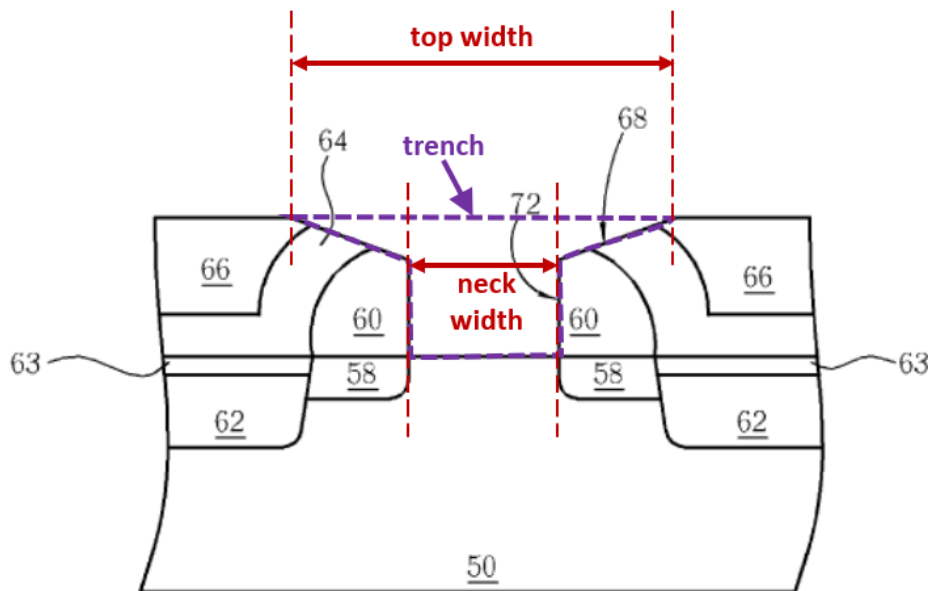
Like the necks 200b and 400b depicted respectively in FIGs. 2 and 4 of the '735 Patent, Lin's trench includes a "**neck**" at an uppermost portion of the vertical sidewalls of the recess (*e.g.*, recess 72) where the sidewalls begin to taper and extend outward as beveled edges (*e.g.*, bevel edges 68). Compare TSMC-1005, FIGs. 4 & 9 with TSMC-1001, FIGs. 2 & 4; TSMC-1003, ¶154.

**[1.6] a width of the neck is narrower than a width of the top, and**

Lin discloses this limitation. TSMC-1003, ¶¶155-157. For example, Lin discloses that a width of the recess (**trench**) at a location between the vertical sidewalls of the spacers (**a width of the neck**) is narrower than a width at its aperture (*e.g.*, at the top of the beveled edges) (**a width of the top**). TSMC-1005 [0012], [0025] ("a

bevel edge 68” is formed and “the opening of the recess 72 is wider”), FIGs. 4-6; *see also* TSMC-1003, ¶157 (mapping corresponding elements in the second embodiment and citing TSMC-1005, [0032], FIGs. 9-10). This follows from the “Y” shaped profile of Lin’s recess, where the top of the “Y” is wider than its stem. TSMC-1005, Abstract, [0002], [0009], [0011], [0026]; *see also id.*, [0035]. Lin explains how this shape promotes better step coverage and reduces voids when metal is deposited in the trench. *Id.*, [0036].

FIG. 4 depicts Lin’s recess (*trench*), where the width of the neck is narrower than a width of the top:

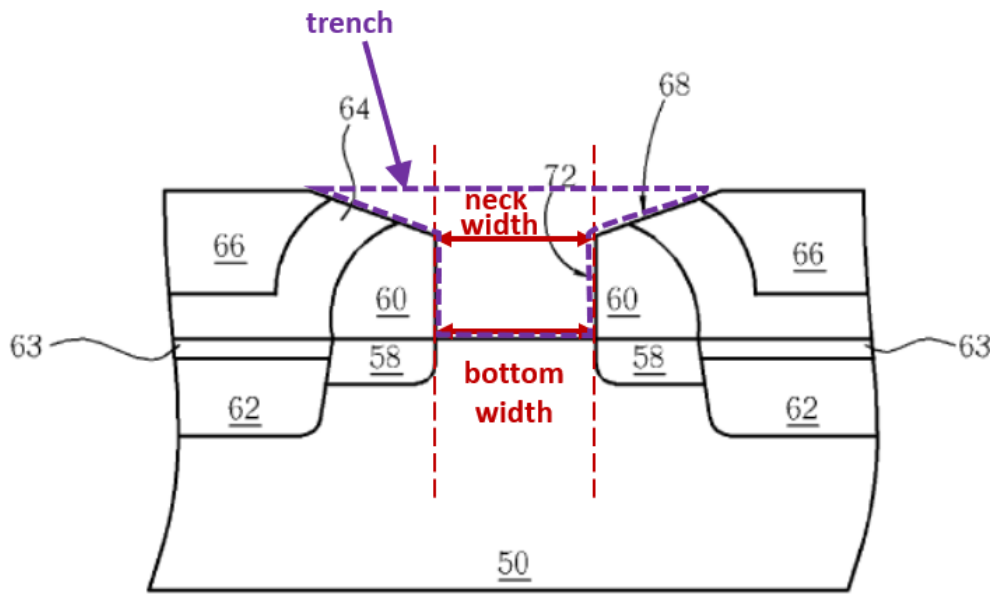


Lin, FIG. 4 (annotated)

***[1.7] the width of the neck is narrower than or equal to a width of the bottom.***

Lin discloses this limitation. TSMC-1003, ¶¶158-160. For example, Lin discloses that “[t]he spacer has a vertical sidewall, and the vertical sidewall surrounds a recess.” TSMC-1005, [0011]; *see also id.*, [0023] (“substantially vertical sidewalls of the spacer 60 surround the recess 72”); *see also id.*, [0031], Claim 17. Since the vertical sidewalls of the spacer run from the bottom of the recess to the start of the beveled edges (*e.g.*, the location of the neck), the width of the recess remains constant along the entire distance from the bottom to the neck—and hence the width of the neck is equal to a width of the bottom. *Id.*, FIGs. 4, 6; *see also* TSMC-1003, ¶¶158, 160 (mapping corresponding elements in the second embodiment and citing FIGs. 9-10).

FIG. 4 depicts equal widths of the bottom of the recess and the neck:



Lin, FIG. 4 (annotated)

(b) Claim 3

*[3]<sup>12</sup> The semiconductor device as claimed in claim 1, wherein an included angle between a sidewall of the top of each of the plurality of trenches and a surface of the dielectric layer is larger than 90°.*

Lin discloses this limitation. TSMC-1003, ¶¶161-163. According to Lin, a bevel edge 68 defines a “*sidewall*” of the top of the recess 72 (*trench*) as part of a

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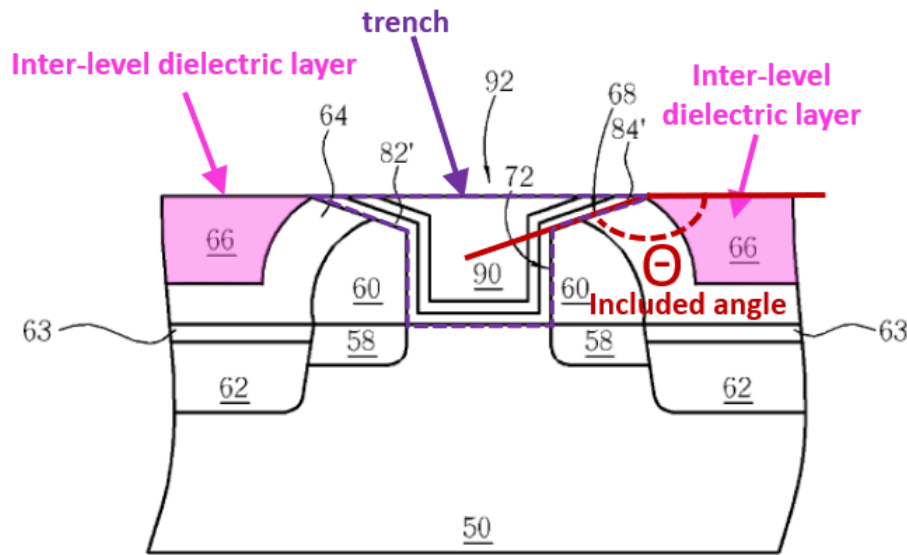
<sup>12</sup> Claim 3 lacks antecedent basis for the term “the plurality of trenches.” This Petition treats claim 3 as referring to “the trench” recited in claim 1, and thus encompassing a semiconductor device having even a single trench. TSMC-1003, Footnote 13. Still, even if claim 3 did require that the semiconductor device include more than one trench, Lin at least implies or renders this feature obvious. *Id.* For example, Lin

“Y structure.” TSMC-1005, [0025]-[0027], FIGs. 4, 6; *see also* TSMC-1003, ¶¶161, 163 (citing [0032]-[0033], [0035]-[0036], FIGs. 9-10). Because the bevel edge 68 is non-vertical and slanted relative to the horizontal top surface of the ILD layer 66, an included angle between the bevel edge 68 of the top of the Y-shaped recess (*trench*) and the horizontal surface of the ILD layer 66 is larger than 90°.

FIG. 6 depicts the included angle larger than 90°:

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explains that semiconductor devices include multiple “MOSFETs.” TSMC-1005, [0001], [0004]. Each transistor in such semiconductor device formed according to the techniques disclosed in Lin has a “Y structure,” and considered collectively, they provide a “plurality of trenches” that exhibit the geometry recited in claim 3. TSMC-1003, Footnote 13; *In re Harza*, 274 F.2d 669 (CCPA 1960) (“It is well settled that the mere duplication of parts has no patentable significance.”).



Lin, FIG. 6 (annotated)

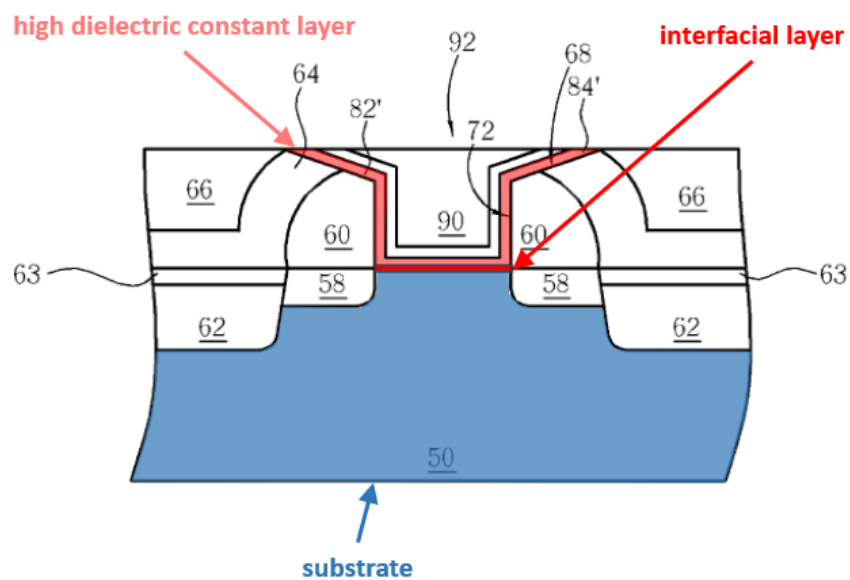
**(c) Claim 4**

**[4] The semiconductor device as claimed in claim 1, further comprising an insulation layer disposed between the substrate and the high dielectric constant layer.**

Lin discloses this limitation. TSMC-1003, ¶¶164-167. For example, Lin discloses that “[p]rior to the High-k materials layer 82 formation, an interfacial layer (not shown) comprising SiON, Si<sub>3</sub>N<sub>4</sub> or SiO<sub>2</sub> is formed between High-k material layer 82 and the substrate 50.” TSMC-1005, [0024].

Lin’s “interfacial layer” provides an “*insulation layer*” disposed between a substrate (*e.g.*, substrate 50) and a high dielectric constant layer (*e.g.*, High-k material layer 82) as recited in claim 4. Indeed, Lin specifically discloses that the interfacial layer can include “SiON, Si<sub>3</sub>N<sub>4</sub> or SiO<sub>2</sub>”—*i.e.*, materials known to insulate when arranged between a substrate and a high-dielectric constant layer like Lin’s.

*Cf.*, TSMC-1001, 4:34-36 ('735 Patent similarly disclosing that “[t]he insulation material layer 103 is made of, for example, silicon oxide and formed, for example, in a thermal oxidizing process.”); TSMC-1003, ¶166 (citing TSMC-1030, 1:57-2:18; TSMC-1031, [0001]); *see also* TSMC-1003, ¶165 (citing TSMC-1029, [0005], [0029], Title; TSMC-1028, 1:65-2:7).



Lin, FIG. 6 (annotated)

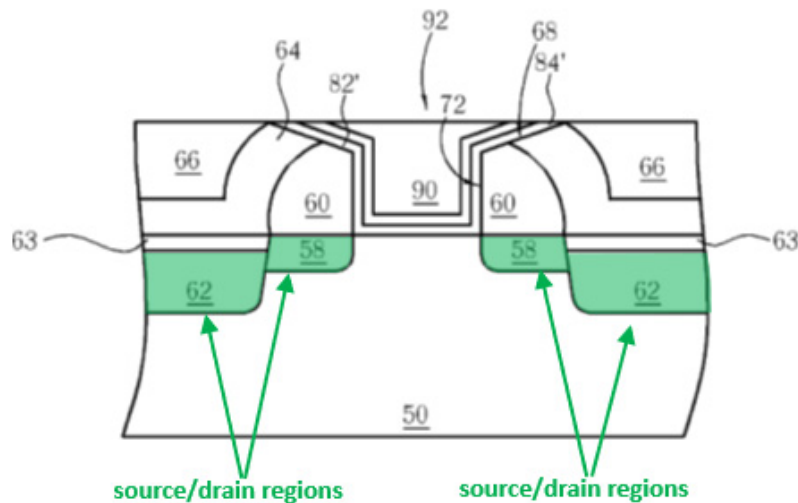
*See also* TSMC-1003, ¶167 (mapping corresponding elements in the second embodiment and citing TSMC-1005, [0033], FIG. 10).

**(d) Claim 5**

***[5] The semiconductor device as claimed in claim 1, wherein the source/drain region is a doped region or an epitaxial layer.***

Lin discloses this limitation. TSMC-1003, ¶168-¶169. For example, and as described above in the analysis of [1.4], Lin discloses that “lightly doped drains 58

(LDDs, also called lightly doped sources) and source/drain dopants 62 are formed in two sides of the gate structure 57 in the substrate 50.” TSMC-1005, [0019]; *supra* Ground 2A, [1.4]. FIG. 6 depicts the doped source/drain regions:



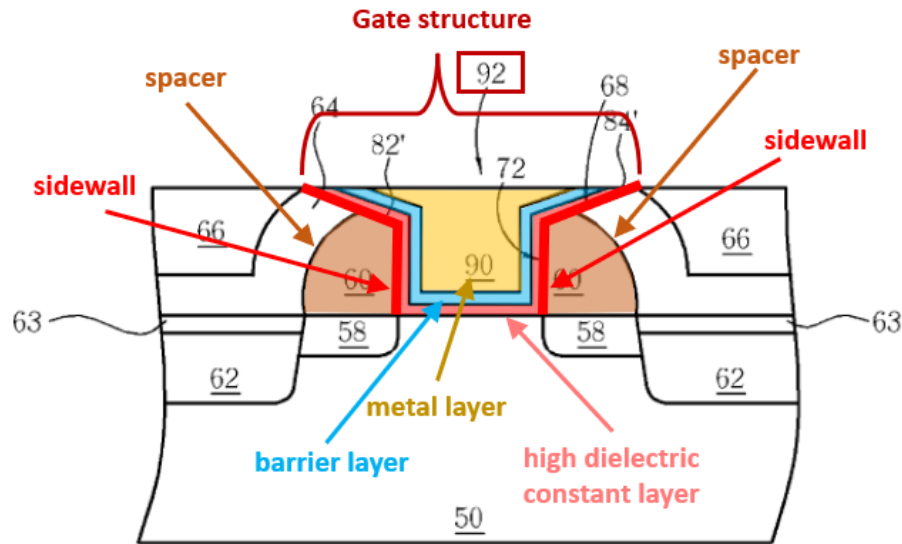
Lin, FIG. 6 (annotated)

*See also* TSMC-1003, ¶169 (mapping corresponding elements in the second embodiment and citing TSMC-1005, [0029], FIG. 10).

(e) Claim 6

***[6] The semiconductor device as claimed in claim 1, further comprising a spacer disposed on a sidewall of the gate structure.***

Lin discloses this limitation. TSMC-1003, ¶¶170-171. For example, Lin discloses “a spacer 60 ... is formed around the gate structure 57.” TSMC-1005, [0019], FIG. 6 *see also id.*, Abstract, [0010]-[0011], [0023], [0029]-[0031], FIGs. 8, 10.



Lin, FIG. 6 (annotated)

See also TSMC-1003, ¶171 (mapping corresponding elements in the second embodiment and citing TSMC-1005, [0023], [0031], FIG. 10).

#### D. [GROUND 2B] – Lin in view of Brask Renders Obvious

## 1. Analysis

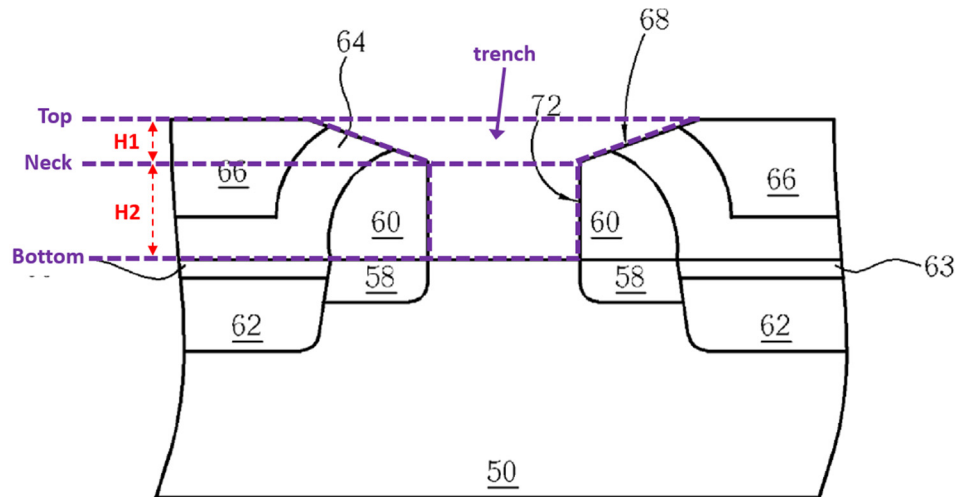
Lin in view of Brask renders obvious claim 2 of the '735 Patent. TSMC-1003, ¶172.

**(a) Claim 2**

**[2] The semiconductor device as claimed in claim 1, wherein the top and the neck have a first height therebetween, the neck and the bottom have a second height therebetween, and a ratio of the first height to the second height is substantially 2:1.**

As discussed in Ground 2A, Lin discloses a Y-shaped recess (***trench***) that includes an aperture (***top***), a bottom (***bottom***), and a ***neck*** between the top and the

bottom. TSMC-1005, [0020], [0023], [0025], FIGs. 4, 9; *supra* Ground 2A, [1.5]-[1.7]; TSMC-1003, ¶173. The top and neck of Lin's trench have a first height (H1) therebetween and the neck and the bottom of Lin's trench have a second height (H2) therebetween, as illustrated below:

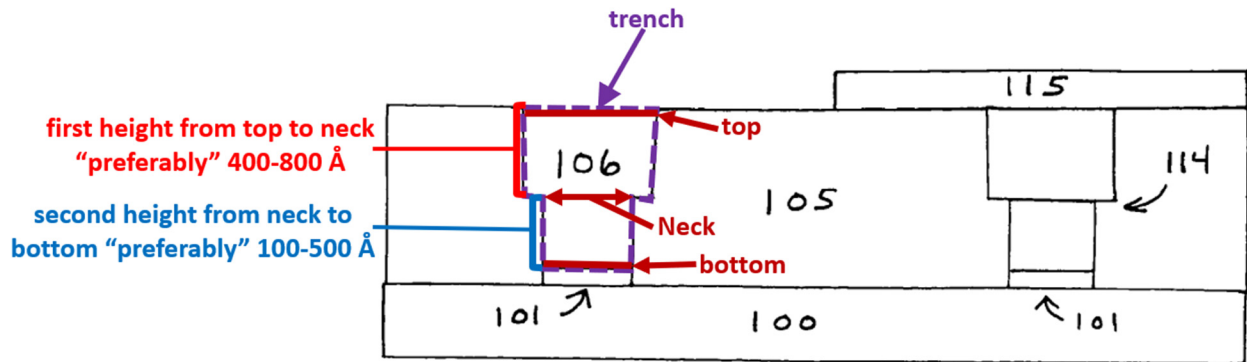


Lin, FIG. 4 (annotated)

Lin discloses its trench broadly, not placing any limitation on the relative heights of its trench segments. To the extent that PO argues that Lin does not expressly disclose the claimed 2:1 height ratio, Brask discloses it. TSMC-1003, ¶¶174-176.

A POSITA would have looked to Brask to supply information regarding appropriate heights for the Lin trench segments. TSMC-1003, ¶¶177-179. Brask expressly discloses trench segment height ranges that include the claimed substantially 2:1 height ratio. Specifically, Brask discloses that the upper trench segment “preferably is between about 400 and about 800 angstroms thick” and the lower trench

segment “preferably is between about 100 and about 500 angstroms thick.”<sup>13</sup> TSMC-1012, 2:15-27. This is illustrated below:



Brask, FIG. 1e (annotated)

Brask’s trench segment height ranges encompass many examples of the claimed substantially 2:1 ratio. Among others, a first height of 400 angstroms and a second height of 200 angstroms satisfies this limitation, as does a first height of 600 angstroms and a second height of 300 angstroms. In fact, a 600 angstroms/300 angstroms combination would be the result if a POSITA simply applied the midpoint of each of the two ranges (400-800 angstroms and 100-500 angstroms). Brask thus discloses the claimed “*ratio of the first height to the second height is substantially 2:1.*” TSMC-1003, ¶176.

<sup>13</sup> *Supra*, Footnote 8.

Brask's disclosure also renders the claimed substantially 2:1 height ratio obvious. TSMC-1003, ¶177. It is well settled that a claimed property or range is obvious where it overlaps or lies inside ranges disclosed by the prior art, which is the case here. *In re Wertheim*, 541 F.2d 257 (CCPA 1976); *In re Woodruff*, 919 F.2d 1575 (Fed. Cir. 1990); *In re Geisler*, 116 F.3d 1465, 1469-71 (Fed. Cir. 1997); *In re Peterson*, 315 F.3d 1325, 1330 (Fed. Cir. 2003); *In re Harris*, 409 F.3d 1339 (Fed. Cir. 2005); MPEP § 2144.05. Moreover, the '735 Patent attributes no criticality, benefit, or unexpected result to the "substantially 2:1" height ratio recited in claim 2. *See* TSMC-1001, 5:27-31, 9:21-35. This feature instead reflects a mere design choice that would have been obvious to try and arrive at through routine experimentation, as discussed below. *E.I. du Pont de Nemours & Co. v. Synvina C.V.*, 904 F.3d 996, 1008 (Fed. Cir. 2018) ("[I]n the absence of evidence indicating that there is something special or critical about the claimed range, an overlap suffices to show that the claimed range was disclosed in—and therefore obvious in light of—the prior art."); TSMC-1003, ¶177. The combination of Lin and Brask thus renders claim 2 obvious, with Lin supplying the basic overall structure of the device, and Brask supplying the 2:1 height ratio limitation. *Id.*

Further establishing obviousness, a POSITA would have looked to Brask as disclosing the basic height ranges under which a device like Lin's would be expected to work. TSMC-1003, ¶178. A POSITA would have experimented with Brask's

ranges to optimize Lin's device. *Id.* As noted above, a POSITA simply using the midpoint of the first range (600 angstroms, the midpoint of 400-800 angstroms) and the midpoint of the second range (300 angstroms, the midpoint of 100-500 angstroms) would result in a device satisfying the 2:1 height ratio limitation. *Id.*

Such optimization would have been obvious because the height ratio was known to impact both the electrical characteristics of the transistor and the quality of the metal fill in the trench. TSMC-1003, ¶179. In this context, a POSITA would have engaged in routine experimentation involving adjustments to the height ratio to optimize these characteristics. *Id.* Achieving a substantially 2:1 ratio through routine experimentation would have been obvious and predictable in at least some implementations of the Lin-Brask device, as evidenced by the preferred heights disclosed in Brask. *Id.* A POSITA would have reasonably expected success because a myriad of designs were known before the Critical Date that used various height ratios, including substantially 2:1. *Id.*

Finally, court decisions confirm the obviousness of claim 2 in light of this combination. Specifically, courts have held that, "where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." *E.I. du Pont*, 904 F.3d at 1006; *see also In re Peterson*, 315 F.3d at 1329 (Fed. Cir. 2003); *In re Brandt*, 886 F.3d 1171,

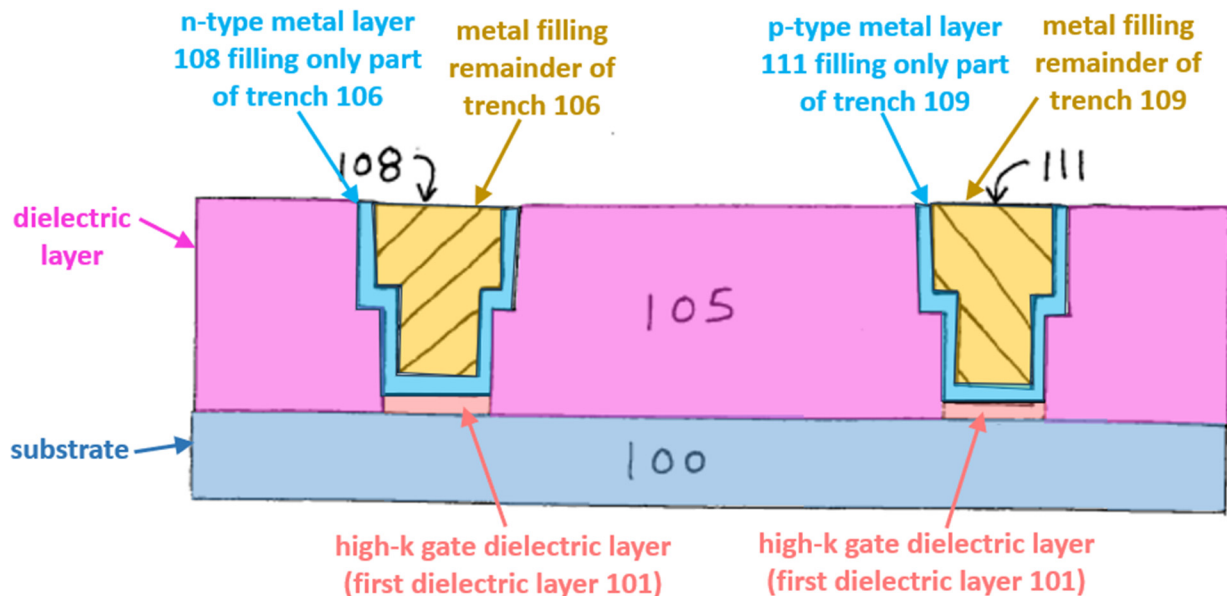
1176-1177 (Fed. Cir. 2018); *Titanium Metals Corp. v. Banner*, 778 F.2d 775, 783 (Fed. Cir. 1985); *In re Aller*, 220 F.2d 454, 456 (CCPA 1955)); MPEP §2144.05.

Accordingly, the Lin-Brask combination discloses and renders obvious claim 2. TSMC-1003, ¶¶173-179.

## E. [GROUND 3A] – Brask Anticipates Claims 1-2

### 1. Analysis

Brask anticipates claims 1-2 of the '735 Patent. TSMC-1003, ¶180. For purposes of demonstrating anticipation, Ground 3A maps Brask's Representative Embodiment as described above in the overview of Brask (*supra* §III.B.1) to each limitation of claims 1 and 2. TSMC-1003, ¶180. An illustration of this Representative Embodiment is shown below:



TSMC-1012, FIG. 11 (modified and annotated as in *supra* §III.B.1)

See also TSMC-1003, ¶¶66-73.

(a) Claim 1

**[1.pre] A semiconductor device comprising:**

To the extent the preamble is limiting, Brask discloses the recited “semiconductor device.” TSMC-1003, ¶181. For example, Brask describes “semiconductor devices with metal gate electrodes.” TSMC-1012, 1:5-10; *see also id.*, Abst., 1:58-64, 2:4-14, 6:54-7:64, 7:1-9, FIGs. 1a-11; *supra* §III.B.1.

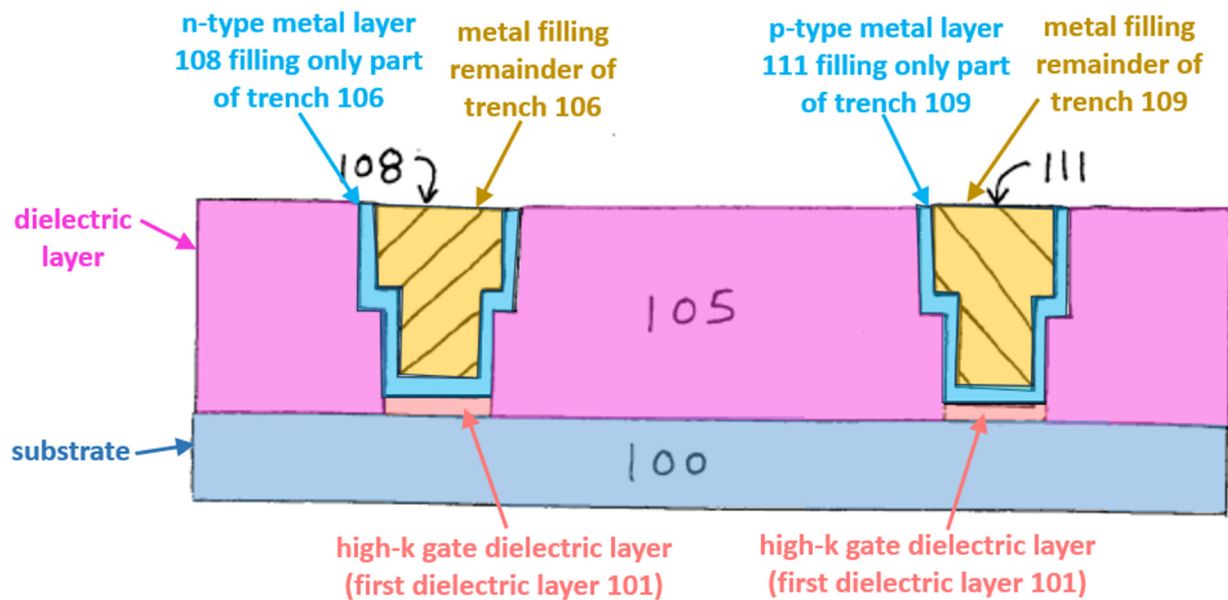


Illustration of Brask’s Representative Embodiment (based on FIG. 11)

**[1.1] a substrate, disposed with a dielectric layer thereon,**

Brask discloses this limitation. TSMC-1003, ¶182. Brask discloses a “substrate 100.” TSMC-1012, 2:4-14; *see also id.*, 1:58-64, 3:56-4:2, 4:30-59. Brask also

discloses that a “second dielectric layer 105 may be deposited over the device.” *Id.*, 3:22-34, FIGs. 1d-1l; *see also id.*, 3:34-43, 4:19-29, 4:60-5:5, 5:63-6:3, 6:13-27, 6:39-53, 7:45-53; *supra* §III.B.1.

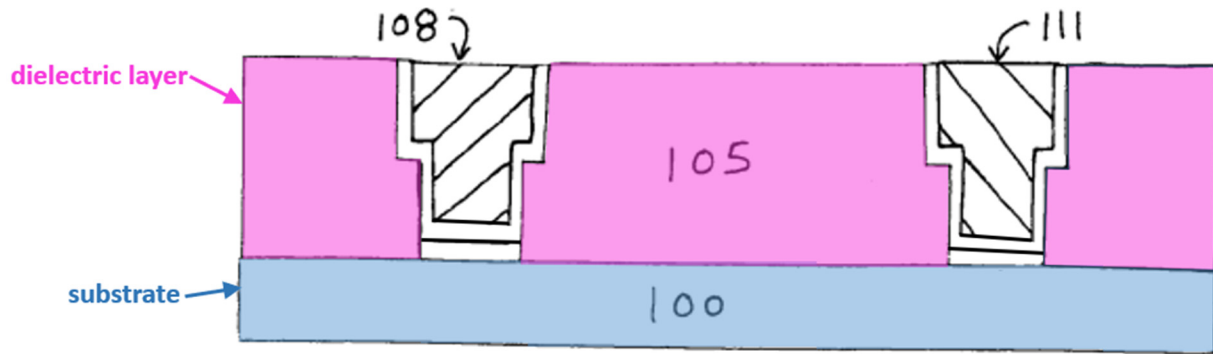
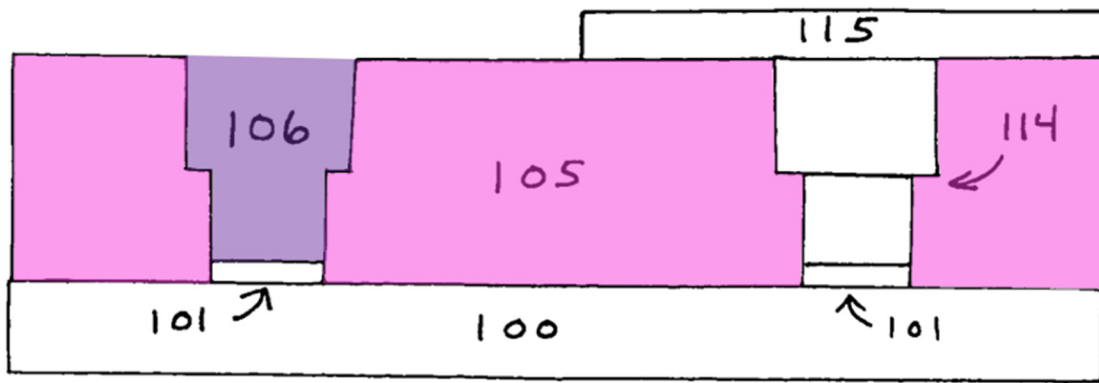


Illustration of Brask’s Representative Embodiment (based on FIG. 1l)

*See also id.*, 3:14-34. Accordingly, Brask’s “substrate 100” (*substrate*) is disposed with the “second dielectric layer 105” (*dielectric layer*) thereon. TSMC-1003, ¶182.

***[1.2] wherein a trench is disposed in the dielectric layer;***

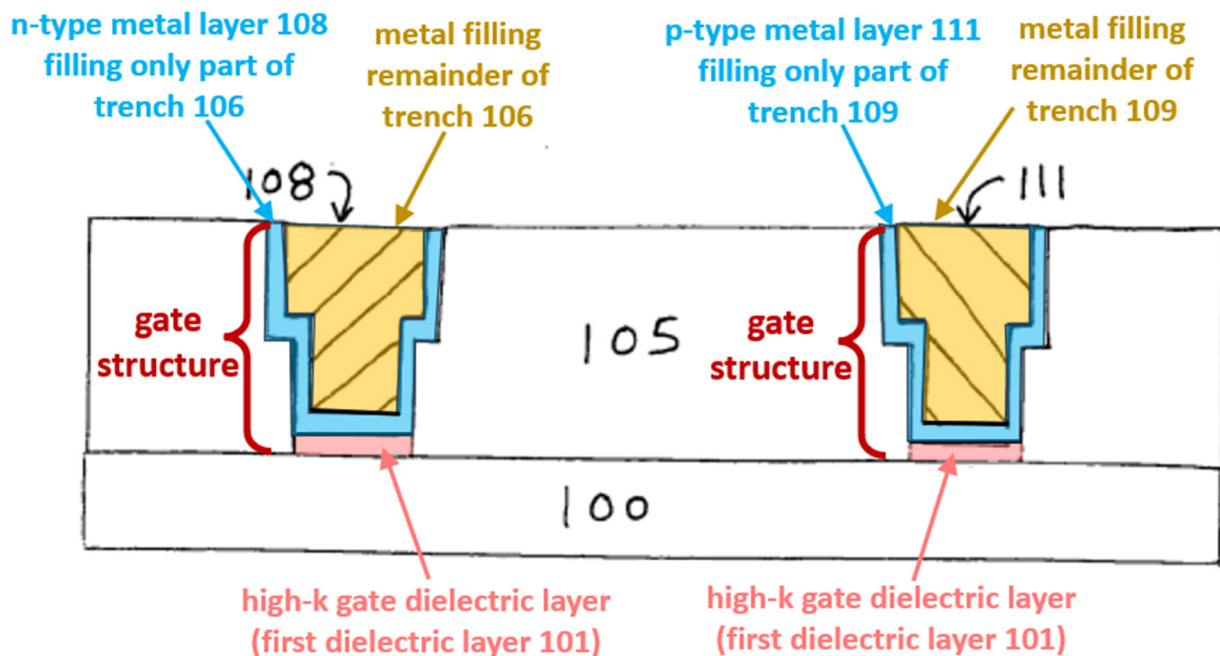
Brask discloses this limitation. TSMC-1003, ¶183. For example, Brask discloses that “trench 106 ... is nested within second dielectric layer 105.” TSMC-1012, 3:34-43, 4:10-18, FIGs. 1d-1f; *see also id.*, 4:30-44, 4:60-5:5, 5:49-6:38, 7:1-9, 7:19-64, FIG. 1j; *supra* §III.B.1.



Brask, FIG. 1e (annotated)

**[1.3.i] a gate structure, located in the trench and**

Brask discloses this limitation. TSMC-1003, ¶184. For example, Brask discloses that “a metal gate electrode” (*gate structure*) “is formed within the trench” (*located in the trench*). TSMC-1012, 1:58-64, 7:1-9; *supra* §III.B.1; *infra*, [1.3.ii]-[1.3.v].



### Illustration of Brask's Representative Embodiment (based on FIG. 11)

***[1.3.ii] [a gate structure ... ] comprising a high dielectric constant layer,***

Brask discloses this limitation. TSMC-1003, ¶185. As explained above, Brask discloses forming an NMOS gate electrode (*gate structure*) within trench 106 and a PMOS gate electrode (*gate structure*) within trench 109. *Supra*, Ground 3A, [1.3.i]. In the Representative Embodiment (*supra* §III.B.1), the NMOS and PMOS gate electrodes each include a “first dielectric layer 101 [that] comprise[s] a high-k gate dielectric layer” (*high dielectric constant layer*). TSMC-1012, 7:1-9, 2:12-14 (“high-k dielectric layer”); *see also id.*, 4:30-6:3, 6:27-53; 7:19-33, FIGs. 1g-1i; *supra* §III.B.1.

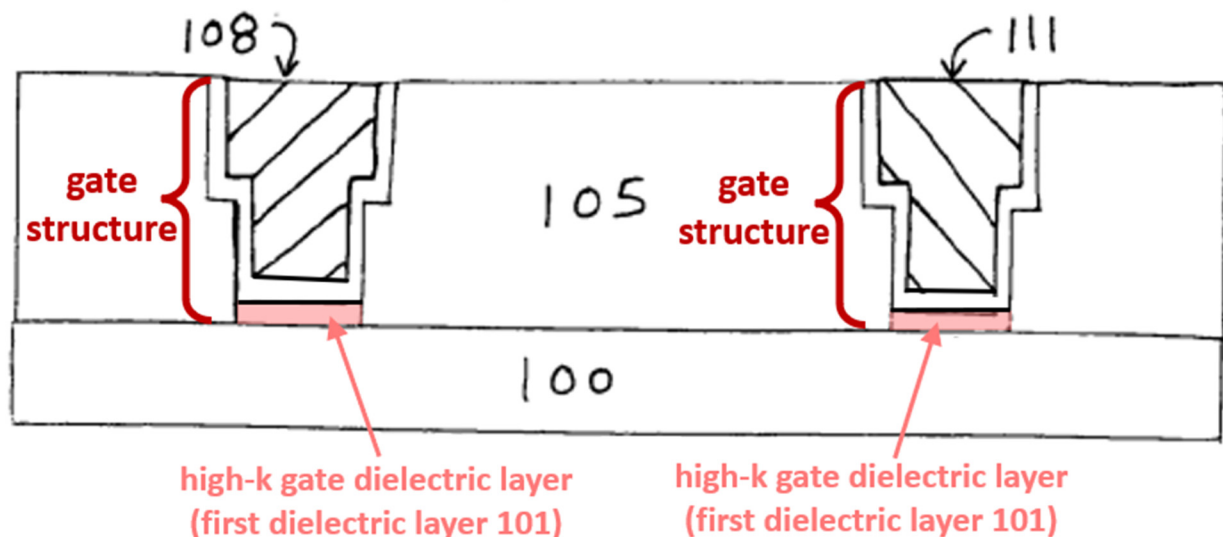


Illustration of Brask’s Representative Embodiment (based on FIG. 11)

***[1.3.iii] [a gate structure ... comprising ... ] a work function metal layer, and***

Brask discloses this limitation. TSMC-1003, ¶¶186-188. For example, Brask explains that an “[n]-type metal layer 108 preferably serves as a metal NMOS gate electrode that has a workfunction that is between about 3.9 e V and about 4.2 e V.” TSMC-1012, 5:49-6:12; *see also id.*, 6:27-38, 6:39-53, FIGs. 1h-k. Likewise, a “[p]-type metal layer 111 may serve as a metal PMOS gate electrode with a workfunction that is between about 4.9 eV and about 5.2 eV.” *Id.*, 6:39-53. Accordingly, the n-type metal layer 108 and the p-type metal layer 111 each provide a respective “***work function metal layer***” for their respective gate structures as claimed. TSMC-1003, ¶¶186.

Moreover, in Brask’s Representative Embodiment (*supra* §III.B.1), “n-type metal layer 108 may fill only part of trench 106” and “p-type metal layer 111 may fill only part of trench 109.” TSMC-1012, 6:4-12, 6:54-67; *supra* §III.B.1; TSMC-1003, ¶187. The following figure illustrates metal layers 108, 111 (***work function metal layers***) filling only parts of trenches 106, 109 consistent with Brask’s description of this embodiment:

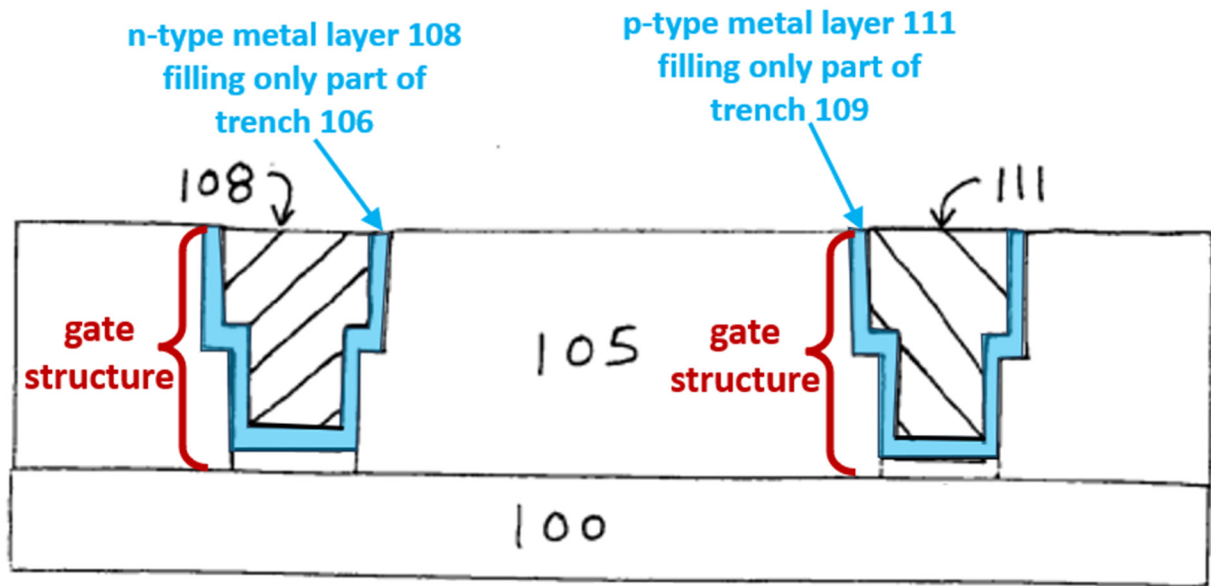


Illustration of Brask's Representative Embodiment (based on FIG. 11)

See also TSMC-1012, 6:4-12, 5:49-6:76, 7:19-33, FIGs. 1h-1l; TSMC-1003, ¶188 (citing TSMC-1007, 7:48-8:5, 8:47-60).

**[1.3.iv] [a gate structure ... comprising ... ] a metal layer;**

Brask discloses this limitation. TSMC-1003, ¶¶189-190. As discussed above, in Brask's Representative Embodiment (*supra* §III.B.1), “n-type metal layer 108 may fill only part of trench 106, with the remainder of the trench being filled with a material that may be easily polished, e.g., tungsten, aluminum, titanium, or titanium nitride.” TSMC-1012, 6:4-12; see also *id.*, 6:54-76 (“As with the metal NMOS gate electrode, the remainder of the trench [109] may be filled with a material that may be easily polished, e.g., tungsten, aluminum, titanium, or titanium nitride.”); *supra* §III.B.1, Ground 3A, [1.3.iii]. The metal that fills the “remainder of the trench” in the Representative Embodiment provides a “*metal layer*” of the gate structure as

claimed. TSMC-1003, ¶189; *see also supra* §III.B.1; TSMC-1012, 7:1-9. Notably, the metal that fills “the remainder of the trench” (e.g., aluminum) in Brask is the same metal that the ’735 Patent uses in its “metal layer.” *Compare* TSMC-1012, 6:4-12 *with* TSMC-1001, 8:7-10.

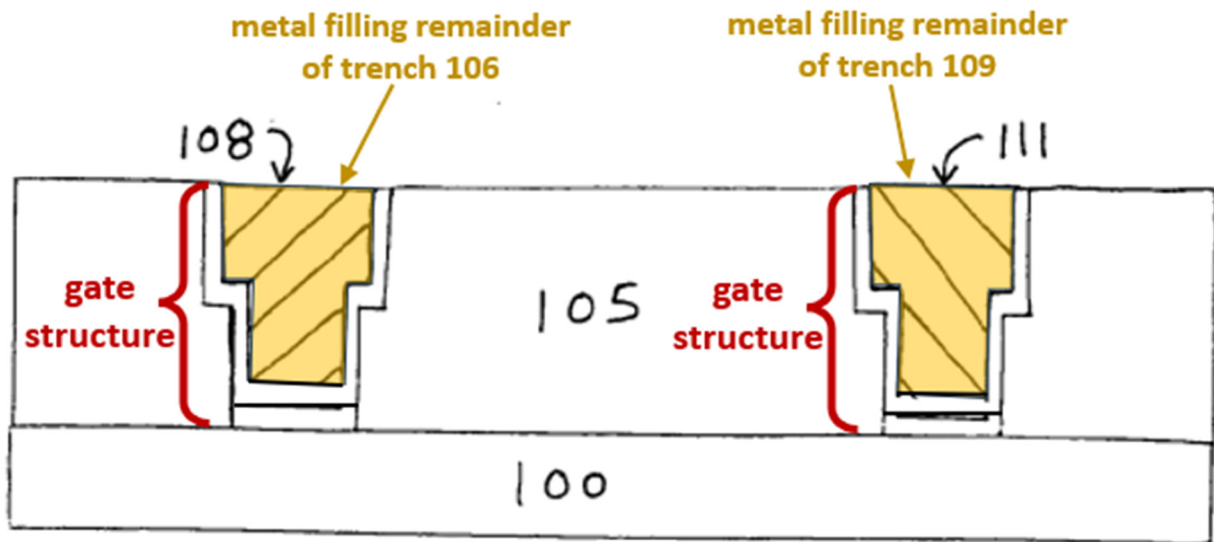


Illustration of Brask’s Representative Embodiment (based on FIG. 11)

*See* TSMC-1012, 6:4-12, 6:54-76; *see also id.*, 7:19-33; *supra* Ground 3A, [1.3.iii]; TSMC-1003, ¶190 (citing TSMC-1007, 7:48-8:5, 8:47-60).

***[1.3.v] sequentially disposed on the substrate;***

Brask discloses this limitation. TSMC-1003, ¶¶191-192. For example, Brask discloses that “metal layers 108 and 111 are formed directly on first dielectric layer 101, without first replacing first dielectric layer 101 with a high-k gate dielectric layer.” TSMC-1012, 7:3-9; *supra* §III.B.1; *see also* TSMC-1012, 4:45-59, 4:30-5:5, 2:4-14, 6:54-67, FIGs. 1f-1g. Brask also explains that “[n]-type metal layer 108 may

be formed on high-k gate dielectric layer.” TSMC-1012, 5:63-6:12; 7:1-9. The n-type metal layer 108 first fills part of the trench (*work function metal layer*), and then the “remainder of the trench [is] filled” with the *metal layer*. *Id.*, 6:4-12; *supra* Ground 3A, [1.3.iii]-[1.3.iv], §III.B.1; *see also* TSMC-1012, 7:19-33. Accordingly, in the Representative Embodiment (*supra* §III.B.1), the high-k gate dielectric layer 101, work function metal layers 108 and 111, and metal layer are *sequentially disposed on the substrate* (e.g., substrate 100). TSMC-1003, ¶192, *see also id.* (citing TSMC-1007, 7:48-8:5, 8:47-60).

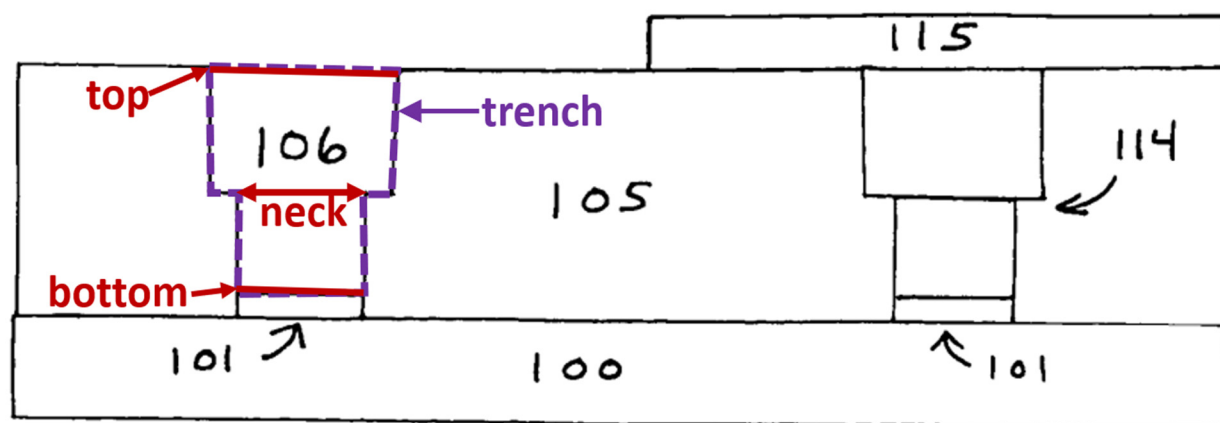
***[1.4] a source/drain region, disposed in the substrate at respective sides of the gate structure,***

Brask discloses this limitation. TSMC-1003, ¶¶193-194. Indeed, Brask explicitly describes “source and drain regions” of the semiconductor device. TSMC-1012, 3:22-34. The source and drain regions are disposed in the substrate 100 at respective sides of each metal gate electrode (*gate structure*). This is evident because Brask’s device is a complementary metal oxide semiconductor (CMOS) device having a complementary pair of NMOS and PMOS field-effect transistors (FETs). *Id.*, 1:13-20, 3:22-34, FIG. 11; TSMC-1003, ¶193. In such FETs, the source and drain regions are necessarily located to the sides of the gate structure because this allows for the creation of a conductive channel through which an electrical current can flow between the source and the drain when a voltage is applied to the gate.

TSMC-1003, ¶193 (citing TSMC-1022, 1:24-1:60 (“When an input voltage is applied to the gate electrode 103, a transverse electric field is set up in the channel region 107. By varying the transverse electric field, it is possible to modulate the conductance of the channel region 107 between the source region and the drain region. In this manner, an electric field controls the current flow through the channel region 107”); TSMC-1004, [0007] (“a gate structure disposed on the substrate between the source and drain regions.”), FIG. 9); TSMC-1005, [0019] (“lightly doped drains 58 (LDDs, also called lightly doped sources) and source/drain dopants 62 are formed in two sides of the gate structure 57 in the substrate 50.”), FIG. 6; TSMC-1009; TSMC-1010; TSMC-1019). The location of the source and drain regions in the substrate at the respective sides of the gate structure is therefore implicitly and inherently disclosed in Brask. TSMC-1003, ¶¶193-194.

***[1.5] wherein the trench comprises a top, a bottom, and a neck arranged between the top and the bottom,***

Brask discloses this limitation. TSMC-1003, ¶195-196. For example, Brask shows in FIG. 1e the trench 106 with a ***top***, a ***bottom***, and a ***neck*** arranged between the top and the bottom:



Brask, FIG. 1e (annotated)

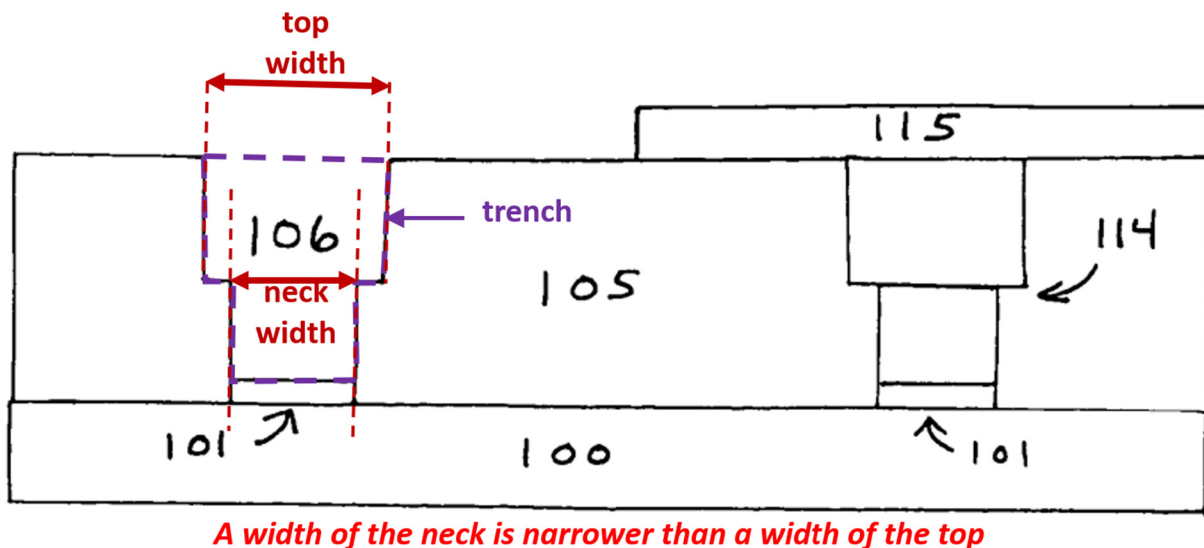
See also TSMC-1012, 4:10-18 (explaining that the “trench is wider at the top than at the bottom.”), 3:14-21. The shape of trench 109 is substantially the same as trench 106, and likewise has top, a neck, and a bottom. *Id.*, FIG. 1j.

In more detail, Brask's trench 106 is formed by removal of structure 104. *Supra*, Ground 3A, [1.1]-[1.2]. Brask explains that structure 104 includes a first layer 102 and a second layer 103 above layer 102. TSMC-1012, FIGs. 1a-1d. Brask explains that "second layer 103 is wider than first layer 102." *Id.*, 2:43-3:31, 4:19-44, FIGs. 1c-1d; *see also id.*, Abstract, 1:58-64, 4:10-18, 6:27-38, 7:1-9. When structure 104 is "removed to form trench 106, the resulting trench is wider at the top than at the bottom because second layer 103 of sacrificial structure 104 was wider than underlying first layer 102." *Id.*, 4:10-18. And like the '735 Patent, Brask's trench 106 includes a narrowed portion having sidewalls that extend vertically from the bottom to the neck, maintaining a constant width therebetween. The neck is disposed at the

location corresponding to the top of removed layer 102. *Compare* TSMC-1012, FIGs. 1e-1f *with* TSMC-1001, FIGs. 2 & 4 (depicting necks 200b, 400b); TSMC-1003, ¶196.

***[1.6] a width of the neck is narrower than a width of the top, and***

Brask discloses this limitation. TSMC-1003, ¶¶197-198. For example, Brask shows in FIG. 1e the neck of trench 106 having a narrower width than a width at the top:



Brask, FIG. 1e (annotated)

In more detail, and as discussed above, the neck of Brask's trench 106 is disposed at the location corresponding to the top of removed layer 102. *Supra*, Ground 3A, [1.5]. Brask explains that the "the resulting trench is wider at the top than at the bottom because second layer 103 of sacrificial structure 104 was wider than underlying first layer 102." TSMC-1012, 4:10-18; *see also id.*, Abstract, 1:58-64, 2:50-

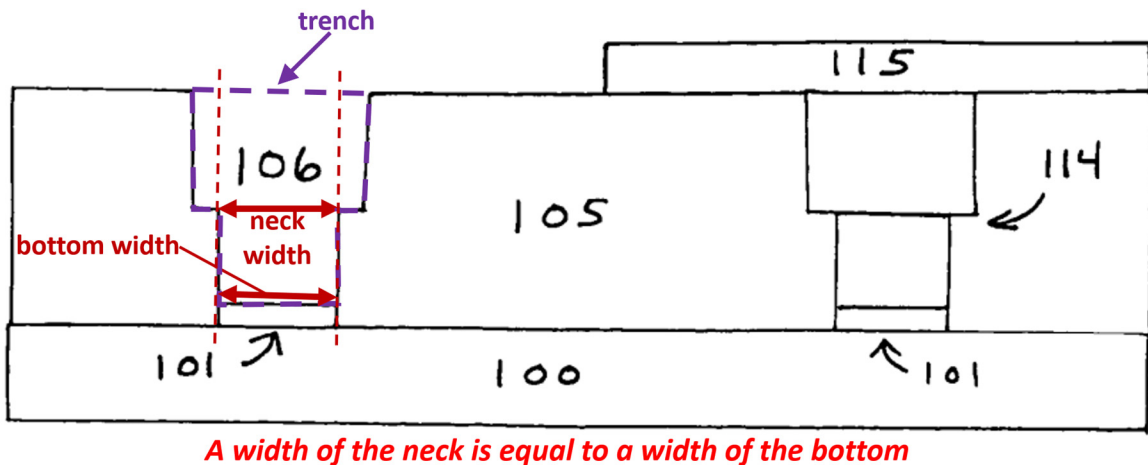
63, 3:14-21. Because the width of Brask's trench 106 at the top corresponds to the width of the second sacrificial layer 103 and the width of Brask's trench 106 at the neck corresponds to the width of the first sacrificial layer 102, the width of Brask's trench 106 is narrower at the neck than that at the top. TSMC-1003, ¶198; *see also* TSMC-1020, 66 (examiner of continuation (TSMC-1016) of the '735 Patent citing Brask and finding that Brask "teaches to form a plurality of dummy patterns comprising silicon in which each of the patterns has a top, a bottom , and a neck arranged between the top and bottom, wherein the width of the neck is narrower than a width of the top, see figures 1a-1l.").

***[1.7] the width of the neck is narrower than or equal to a width of the bottom.***

Brask discloses this limitation. TSMC-1003, ¶¶199-200. For example, Brask shows in FIG. 1e that the width of the neck of trench 106 is equal to a width of the bottom<sup>14</sup>:

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<sup>14</sup> *Supra* Footnote 8.



Brask, FIG. 1e (annotated)

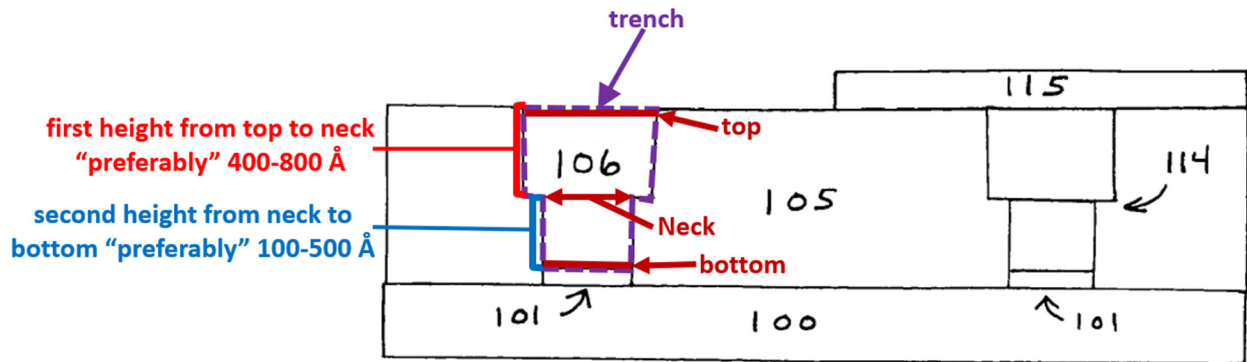
Specifically, the “neck” of Brask’s trench 106 is disposed at the location corresponding to the top of removed layer 102. *See supra* Ground 3A, [1.5]-[1.6]. As discussed above and depicted in FIG. 1e, Brask’s “neck” and “bottom” have a same width corresponding to the width of first layer 102, whose width is constant from top to bottom. *See* TSMC-1012, 2:50-3:13 (“first layer 102 has a width that is less than about 300 angstroms”), 3:14-21, 4:10-18; TSMC-1003, ¶200; *see also, id.*, FIG. 1e (annotated above), 1:58-64, 2:50-63, 3:14-21, 4:10-18. 1.

**(a) Claim 2**

***[2] The semiconductor device as claimed in claim 1, wherein the top and the neck have a first height therebetween, the neck and the bottom have a second height therebetween, and a ratio of the first height to the second height is substantially 2:1.***

Brask discloses this limitation. TSMC-1003, ¶¶201-202. Specifically, Brask discloses that the upper trench segment “preferably is between about 400 and about 800 angstroms thick” and the lower trench segment “preferably is between about

100 and about 500 angstroms thick.”<sup>15</sup> TSMC-1012, 2:15-27. This is illustrated below:



Brask, FIG. 1e (annotated)

Brask’s trench segment height ranges encompass many examples of the claimed substantially 2:1 ratio. Among others, a first height of 400 angstroms and a second height of 200 angstroms satisfies this limitation, as does a first height of 600 angstroms and a second height of 300 angstroms. In fact, a 600 angstroms/300 angstroms combination would be the result if a POSITA simply applied the midpoint of each of the two ranges (400-800 angstroms and 100-500 angstroms). Brask thus discloses the claimed “ratio of the first height to the second height is substantially 2:1.” TSMC-1003, ¶202.

## F. [GROUND 3B] – Brask Renders Obvious Claims 1-2

### 1. Analysis

Brask renders obvious claims 1-2 of the ’735 Patent. TSMC-1003, ¶203.

<sup>15</sup> *Supra*, Footnote 8.

**(a) Claim 1**

***Elements [1.pre]–[1.3.v], [1.5]–[1.7]***

Brask discloses and renders obvious each of elements [1.pre]–[1.3.v] and [1.5]–[1.7], for each of the reasons addressed above in Ground 3A. *Supra*, Ground 3A at [1.pre]–[1.3.v], [1.5]–[1.7]; *Real Time Data, LLC v. Iancu*, 912 F.3d 1368, 1373 (Fed. Cir. 2019) (“[I]t is well settled that ‘a disclosure that anticipates under § 102 also renders the claim invalid under § 103, for ‘anticipation is the epitome of obviousness.’”) (quoting *Connell v. Sears, Roebuck & Co.*, 722 F.2d 1542, 1548 (Fed. Cir. 1983)); TSMC-1003, ¶205.

***[1.4] a source/drain region, disposed in the substrate at respective sides of the gate structure,***

Brask renders this limitation obvious. TSMC-1003, ¶¶205-207. As discussed above, Brask discloses “source and drain regions” in the semiconductor device. TSMC-1012, 3:22-34; *supra* Ground 3A, [1.4].

To the extent Patent Owner argues that Brask does not expressly or inherently disclose that the source and drain regions are disposed in the substrate at respective sides of the gate structure, it would have been obvious to a POSITA. TSMC-1003, ¶206. Specifically, a POSITA would have found it obvious to dispose Brask’s source and drain regions at respective sides of the gate structure to enable the device to function as an operational field-effect transistor (FET) in which an electric field applied to the gate structure would form a conductive channel that allows electrical

current to flow between the source and drain regions. *Id.* (citing TSMC-1022, 5:14-60 (“When an input voltage is applied to the gate electrode 103, a transverse electric field is set up in the channel region 107. By varying the transverse electric field, it is possible to modulate the conductance of the channel region 107 between the source region and the drain region. In this manner, an electric field controls the current flow through the channel region 107”); TSMC-1004, [0007] (“a gate structure disposed on the substrate between the source and drain regions.”), FIG. 9); TSMC-1005, [0019] (“lightly doped drains 58 (LDDs, also called lightly doped sources) and source/drain dopants 62 are formed in two sides of the gate structure 57 in the substrate 50.”), FIG. 6; TSMC-1009; TSMC-1010; TSMC-1019). Brask’s device could then find beneficial application as an electrical switch in a range of applications that commonly used FETs as switches before the Critical Date of the ’735 patent. *Id.*, ¶¶206-207; *see also id.* ¶¶36-40. A POSITA would have reasonably expected success because disposing source and drain regions at respective sides of the gate structure had been achieved and was the conventional practice in FETs before the Critical Date. *Id.*; TSMC-1003, ¶206 (citing TSMC-1022, 1:24-1:60; TSMC-1004, [0007], FIG. 9; TSMC-1005, [0019], FIG. 6; TSMC-1009; TSMC-1010; TSMC-1019).

(a) Claim 2

***[2] The semiconductor device as claimed in claim 1, wherein the top and the neck have a first height therebetween, the neck and the bottom have a second height therebetween, and a ratio of the first height to the second height is substantially 2:1.***

To the extent it is argued that Brask does not anticipate the additional limitations recited in claim 2, they were at least obvious. TSMC-1003, ¶208; *supra* §§III.B.2(a), III.B.1. It is well settled that a claimed property or range is obvious where it overlaps or lies inside ranges disclosed by the prior art, which is the case here. *In re Wertheim*, 541 F.2d 257 (CCPA 1976); *In re Woodruff*, 919 F.2d 1575 (Fed. Cir. 1990); *In re Geisler*, 116 F.3d 1465, 1469-71 (Fed. Cir. 1997); *In re Peterson*, 315 F.3d 1325, 1330 (Fed. Cir. 2003); *In re Harris*, 409 F.3d 1339 (Fed. Cir. 2005); MPEP § 2144.05.

Moreover, “where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation.” *E.I. du Pont*, 904 F.3d at 1006; *In re Peterson*, 315 F.3d at 1329 (Fed. Cir. 2003); *In re Brandt*, 886 F.3d 1171, 1176-1177 (Fed. Cir. 2018); *Titanium Metals Corp. v. Banner*, 778 F.2d 775, 783 (Fed. Cir. 1985); *In re Aller*, 220 F.2d 454, 456 (CCPA 1955)); MPEP §2144.05. A POSITA would have found it obvious to implement Brask’s trench in a manner that would have achieved the substantially 2:1 ratio between the first height (top to neck) and second height (neck to bottom).

TSMC-1003, ¶208. Because the height ratio was known to influence both the electrical characteristics of the transistor and the quality of the metal fill in the trench, a POSITA would have engaged in routine experimentation involving adjustments to the height ratio to optimize these characteristics. *Id.* A POSITA would have predictably arrived at a substantially 2:1 ratio through routine experimentation in at least some implementations of Brask's device—especially since the ratio could be achieved using the preferred heights explicitly disclosed in Brask. *Id.* A POSITA would have reasonably expected success because a myriad of designs were known before the Critical Date that used various height ratios, including substantially 2:1. *Id.*

#### **IV. PAYMENT OF FEES – 37 C.F.R. § 42.103**

Petitioner authorizes the Patent and Trademark Office to charge Deposit Account No. 06-1050 for the fee set in 37 C.F.R. § 42.15(a) for this Petition and further authorizes payment for any additional fees to be charged to this Deposit Account.

#### **V. CONCLUSION**

Petitioner respectfully requests institution IPR and cancellation of all Challenged Claims as unpatentable based on Grounds 1A-3B.

#### **VI. MANDATORY NOTICES UNDER 37 C.F.R. § 42.8(a)(1)**

##### **A. Real Party-In-Interest Under 37 C.F.R. § 42.8(b)(1)**

Petitioner, Taiwan Semiconductor Manufacturing Company Ltd., is the real

party-in-interest.

**B. Related Matters Under 37 C.F.R. § 42.8(b)(2)**

Petitioner is not aware of any disclaimers, reexamination certificates or petitions for *inter partes* review for the '735 Patent. Petitioner is not aware of any civil actions involving the subject matter for the '735 Patent.

**C. Lead And Back-Up Counsel Under 37 C.F.R. § 42.8(b)(3)**

Petitioner provides the following designation of counsel.

| Lead Counsel                                                                                                                                                                                                                                       | Backup counsel                                                                                                                                                                                                                                                                                                    |
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**D. Service Information**

Please address all correspondence and service to the address listed above. Petitioner consents to electronic service by email at [IPR57998-0002IP1@fr.com](mailto:IPR57998-0002IP1@fr.com) (referencing No. 57998-0002IP1).

Respectfully submitted,

Dated: January 16, 2026

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**CERTIFICATION UNDER 37 CFR § 42.24**

Under the provisions of 37 CFR § 42.24(d), the undersigned hereby certifies that the word count for the foregoing Petition for *Inter partes* Review totals 13,074 words, which is less than the 14,000 allowed under 37 CFR § 42.24.

Dated: January 16, 2026

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**CERTIFICATE OF SERVICE**

Pursuant to 37 CFR §§ 42.6(e)(4)(i) *et seq.* and 42.105(b), the undersigned certifies that on January 16, 2026, a complete and entire copy of this Petition for *Inter partes* Review, Power of Attorney, and all supporting exhibits were provided via Federal Express, to the Patent Owner by serving the correspondence address of record and Patent Owner's IPR counsel as follows:

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