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Samsung CHIPS Act Grant Brings Its Leading Edge Plus R&D To Texas

By [Willy Shih](#), Former Contributor. ⓘ Willy Shih teaches in operation management at Harvard... ⌵

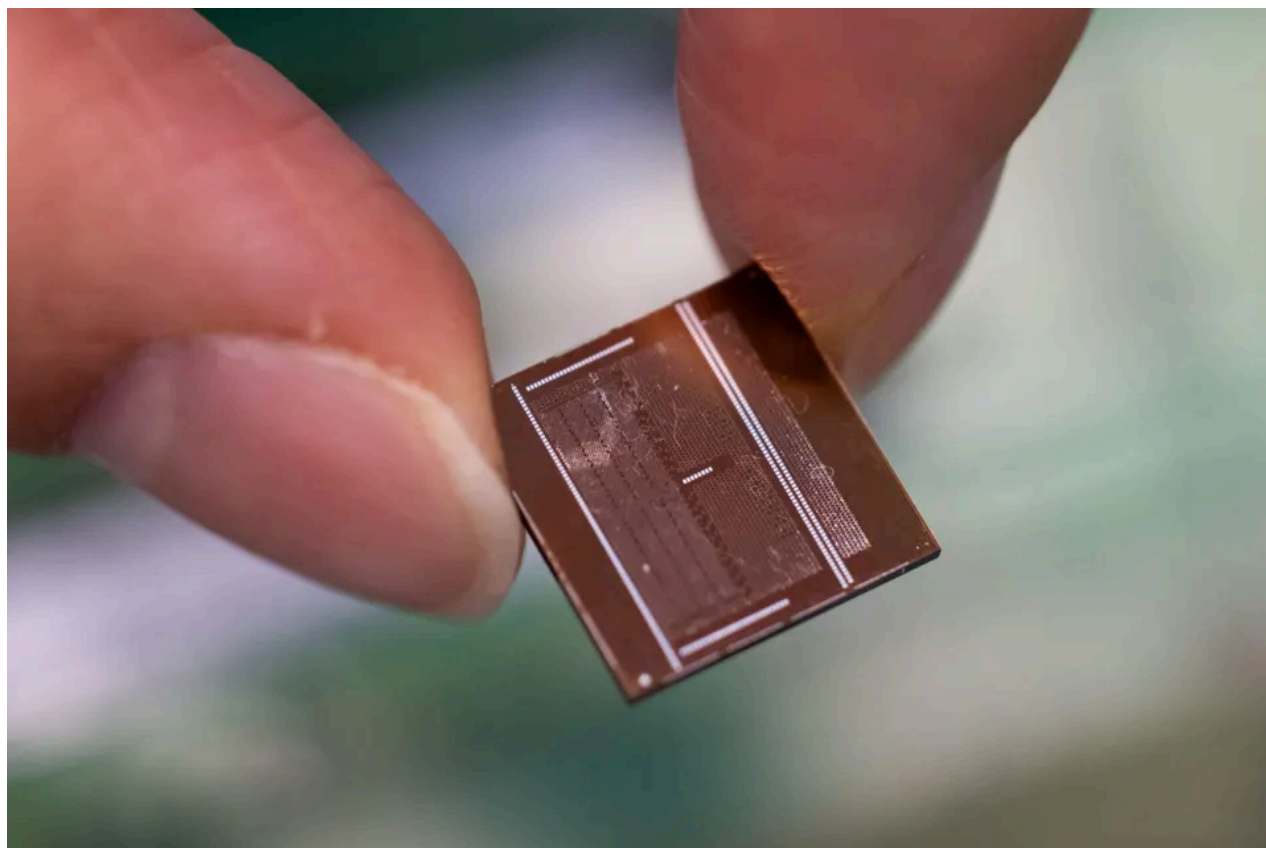
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A Samsung High-bandwidth Memory Chip. Samsung is a global leader in memory chips, and is #2 as a foundry supplier. Photographer: SeongJoon Cho/Bloomberg
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Samsung Electronics won a \$6.4 billion CHIPS grant, right behind [Intel](#) INTC+2.6% and [TSMC](#), the Department of Commerce announced Monday morning. There are several noteworthy aspects of this deal. In addition to the usual factory (“fab”) expansion, the company has committed to bring its most advanced chip manufacturing technology to its new site in Taylor, Texas. It will also establish an advanced packaging operation, an R&D fab, and R&D as well.

Samsung is the largest memory chip manufacturer in the world with a global market share of over 45% in Q4 of 2023, and it also has the second largest foundry business after Taiwan Semiconductor Manufacturing Company (TSMC). The [Taylor site](#) is already a massive construction project, and Samsung has committed to build a second fab there. They will also upgrade the first fab from what was originally slated to be their 4 nm process to their most advanced 2 nm process, which the second fab will run as well. That means Intel, TSMC, and Samsung will all offer their most advanced manufacturing processes in the U.S. This will be good for competition, and it will be good for the U.S. Recently, Commerce Secretary Gina Raimondo

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Samsung also committed to a significant expansion of its existing fab in Austin, which is about 20 miles southwest of Taylor. It will bring its Fully Depleted Silicon on Insulator process to the Austin fab. FD-SOI is a variation on the widely used “bulk CMOS” technology used for most chips. It relies on an ultra-thin layer of an insulator, called a buried oxide layer. This technology offers very high transistor switching speeds, which makes FD-SOI chips excellent for radio-frequency (Rf) devices, and a good platform for integrating analog and digital devices in applications like car radars and 5G smartphones. Consumer electronics, automotive, and aerospace companies use FD-SOI chips, and GlobalFoundries also makes them domestically. Samsung also committed to working with the Department of Defense (DoD), but there were no more specifics on that.

The most significant part of the deal is what else Samsung is committing to. Let’s start with packaging.



Chip packages protect the die and provide a means to communicate with the world. This vintage AMD chip has an array of “bumps” on the back for connection to a printed circuit board. Photo by DANIEL SLIM, AFP VIA GETTY IMAGES

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Samsung Will Build An Advanced Packaging Plant At Taylor

When we talk about chip packaging, we mean the process that occurs after the semiconductor chips, also known as “die,” are cut out of the wafers on which they are made and encapsulated in a package. This package both protects the chip and provides a means for it to talk to the outside world. The first chip packages had tiny wires that were bonded to the die by technicians looking through microscopes, which is the main reason that most of this work moved to Asia in the 1970s. The packages in turn have leads or bumps that allow them to be connected to printed circuit boards (another vital industry that I have [written](#) about recently). As chips grew more complicated, at first with thousands, then millions, and more recently billions of transistors, engineers figured out how to connect the die to the package using automated wire bonding machines or tiny solder/conductive bumps on the die that could be flipped and “sweated” to tiny pads. Modern packages have thousands of connections.

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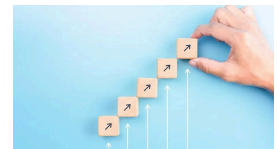
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But chips keep getting more complicated, and as they run faster and faster, physical distance between them really matters. We tend not to think about this, but electrical signals travel at the speed of light in whatever medium they are moving. On a circuit board, this equates to six inches in one nanosecond (one billionth of a second). While that may not seem like a long time, that turns out to be eons of delay if you are trying to make things run fast, so you would like to cram the chips as physically close together as possible. Also, as you connect more and more chips with lots of signal lines, you get many other undesirable electrical effects. The answer is to either put more circuits on a single chip or try to connect multiple chips in a single package.

Putting more circuits on an individual chip using the most advanced processes is both expensive and risky. Wouldn't it be nice if one could mix and match known good chips made in a cheaper and older process with leading edge chips where you put the really performance sensitive functions? Or what if the processes needed to manufacture some chips, like the logic for a graphics processing unit (GPU) for AI, are different from the process to make high bandwidth memory (HBM) chips and I want to connect them really close to each other to maximize speed?

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This is where advanced packaging comes in. If you want to put chips as close as possible side-by-side, a technique that is called 2.5D, Samsung has a technology that it calls [I-Cube](#). This uses a piece of patterned silicon called an interposer that the chips sit on top of. The interposer connects them together with lots of wiring, and also connects the whole assembly to the package. You generally don't have to worry as much about the chips heating up at different rates in this scheme. If you want to stack chips vertically, something that is called 3D packaging, this is more complicated. But 3D chip stacking is widely considered to be the pathway to future performance and keeping Moore's Law going. Samsung has a process that it calls X-Cube for this.

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US Secretary of State Antony Blinken tours an Amkor Technology facility in Manila, the Philippines last month. (Photo by EVELYN

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most of the routine commodity packaging is done there as well. This means even though we will have all these shiny new fabs in the U.S., the finished wafers largely will have to go to Asia for packaging. Intel will be doing packaging in New Mexico, Amkor recently announced plans to build a packaging plant in Arizona, and Samsung memory competitor SK Hynix recently [announced](#) a packaging plant in West Lafayette, Indiana. Samsung setting up a packaging facility in Taylor adds to this momentum. This is an important step towards rebuilding domestic chip capabilities.

Establishing An R&D Lab Far From Asia Is Challenging, Establishing An R&D Fab In The U.S. Is A Statement

Historically semiconductor process R&D has been kept close to a company's R&D fabs. Taiwan Semiconductor Manufacturing Company (TSMC) has long resisted moving R&D away from its main fabs in Hsinchu and nearby science parks. This is important because in semiconductor manufacturing, the *process is the product*, and engineers have to be able to test things in real production conditions. The constant iteration and refinement favors keeping things close. Intel keeps its R&D in Hillsboro, Oregon, TSMC in Taiwan, Samsung in Korea.

But Samsung has also committed to building an R&D fab in Texas. That says they are serious about innovating in the U.S. Perhaps it is to stay close to American researchers in advanced materials and new device structures, or maybe it's because they see a new wave of R&D investments coming with all the spending and hype around artificial intelligence (AI) as a driver of spending for chips. But setting up an R&D fab and opening R&D operations in Texas means the company is in the U.S. in a big way for the long-term. Because the semiconductor business is a long game.

Since March, Commerce has announced grant packages for Intel, TSMC, and now Samsung. This is kind of Commerce's logic chip domestic manufacturing trifecta. The last leg could be a real winner.

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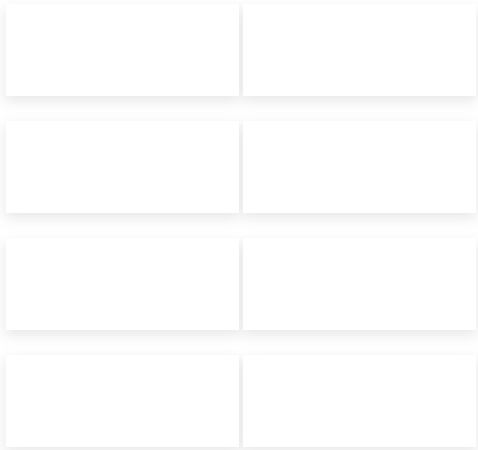
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