

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY LTD.,

Petitioner,

v.

MARLIN SEMICONDUCTOR LIMITED,

Patent Owner.

Case No. IPR2026-00220

U.S. Patent No. 8,076,735 B2

DECLARATION OF JOSEPH MCALEXANDER

I. QUALIFICATIONS

1. I am a Registered Professional Engineer (#79454) and the President of M^cAlexander Sound, Inc. I hold a Bachelor of Science degree in Electrical Engineering from North Carolina State University. I have been associated with the integrated circuit and electronics industry as a designer and consultant for the past 53 years and am a named inventor on 31 U.S. patents and a number of foreign patents, many of which are directly related to the design and operation of transistors and circuits incorporating transistors, including control, addressing, comparing and sensing, and fabrication.

2. My skills and experience are in areas of circuit design and analysis, device and board fabrication and assembly, testing, marketing, control system design and analysis, manufacturing operations, and respective areas of quality, reliability, and defect/failure analysis. Specifically, I have:

- designed memories, including Dynamic Random Access Memories (DRAMs), Static Random Access Memories (SRAMs), Charge Coupled Devices (CCDs), Shift Registers (SRs), and functional circuits including I/O buffers for address and data, decoders, clocks, sense amplifiers, fault tolerant (incorporating both non-volatile EPROM and random access memory components), parallel-to-serial data paths for video applications, level shifters, converters, pumps, and logic, as well as wireless communication systems and MEMs;
- managed operations including engineering, training, and quality assurance for device fabrication, assembly, test, analysis, and reliability assessment, as well as manufacturing control, each of which involved both volatile and non-volatile memory; testing, analysis, and control involved use of mechanical calibration and

measuring equipment, including optical, scanning e-beam, IR, capacitive, and laser using phase contrast and FFT for HARI applications;

- taught courses in solid-state device physics, integrated circuit design, integrated circuit fabrication, and statistical control;
- provided expert services, investigating both process and design technologies of various devices (microprocessor and controller, volatile and non-volatile memory, programmable logic, card, tag, module, mixed signal, custom, and other), systems (PC and peripheral, computer, control, laser measurement, switch, architecture, software, and other), and consumer products (medical, TV, telephone, VCR, facsimile, copier, lighting, game, and other); and
- designed and managed development, testing, and evaluation of memory devices and systems incorporating such devices, including simulation of operation. I have also had experience in programming, erasing, and wearout of electrically programmable and erasable non-volatile memories.

3. Because of my background, training, and experience, I am qualified as an expert to opine on the challenged patent. A more detailed account of my work experience and other qualifications is listed in my Curriculum Vitae, which is submitted as Exhibit 2003.

II. OVERVIEW

4. In my opinion, none of the Petition grounds establishes a reasonable likelihood that Petitioners will prevail on any challenged claim of U.S. Patent Number 8,076,735 (“the ’735 Patent”). For example, none of the references of Grounds 1A, 1B, 2A, or 2B teach the claimed specially shaped “trench,” while none of the references of Grounds 3A-B teach the claimed “work function metal layer.”

5. **Grounds 1A-2B:** The '735 Patent concerns semiconductor devices that include a “trench,” which the patent describes is a recess formed from the removal of a dummy gate. Each challenged claim requires that this “trench” must have a certain shape, reciting a “trench [comprising] a top, a bottom, and a neck arranged between the top and the bottom, *a width of the neck is narrower than a width of the top.*” Such a trench is illustrated in the '735 Patent's Figure 1D, annotated below:

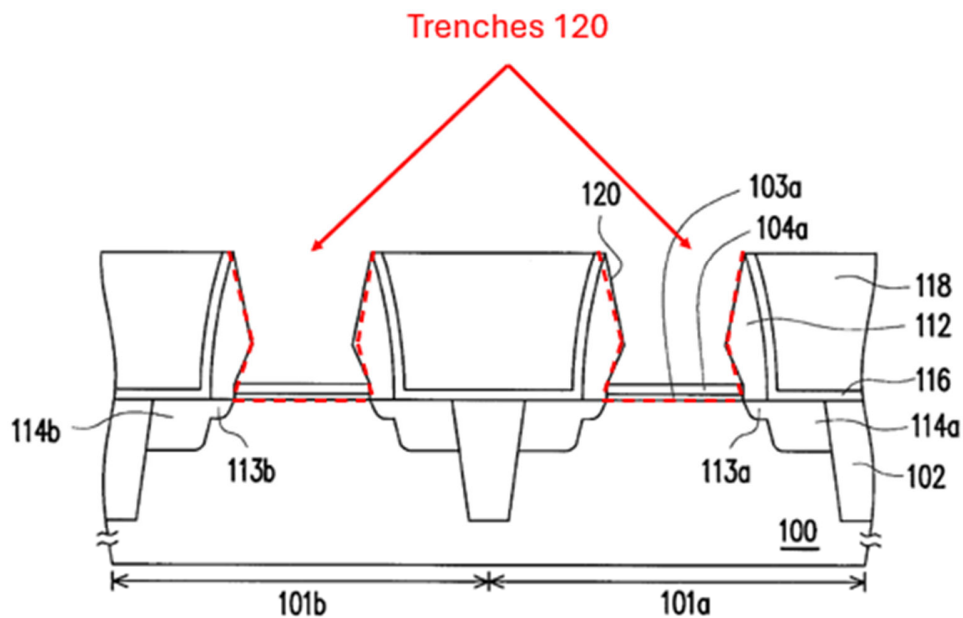


FIG. 1D

6. But the asserted references of Grounds 1A-2B do not disclose such a trench. In each of the references relied on as supposedly disclosing the claimed trench—Chuang in Grounds 1A and 1B, Lin in Grounds 2A and 2B—the recess

7. For example, in Ground 1A-B's Chuang reference, the trench formed by removing a dummy gate is rectangular with a uniform width, and does not have a neck width narrower than the top's width:



8. Similarly, in Ground 2A-B's Lin reference the trench formed by removing a dummy gate is rectangular with a uniform width, and does not have a neck width narrower than the top's width:



10. But although Grounds 3A-B rely solely on the Brask as supposedly teaching the claimed “work function metal,” the Petition does not even assert, much less provide sufficient evidence to establish, that the identified Brask metal layer “prevent[s] the threshold voltage from increasing and therefore reducing the resistance of the device.” The Petition could not because Brask does not describe the layer relied on by the Petition as preventing the threshold from increasing and reducing the resistance.

11. Because all of the claims require this missing “work function metal, Grounds 3A-B fail.

III. MATERIALS CONSIDERED

12. In preparing this declaration, I have reviewed the Petition and the declaration of Petitioner’s expert, as well as the materials that they cite, including U.S. Patent No. 8,076,735 B2 (the “’735 Patent”), the ’735 Patent prosecution history, and the asserted prior art. The prior art asserted by the Petition to which I direct my analysis includes:

- a. TSMC 1004 - US Patent Publication 2010/0044783 A1 (Chuang);
- b. TSMC 1012 - US Patent Number 7,176,090 B2 (Brask); and
- c. TSMC 1005 - US Patent Publication 2008/0265322 A1 (Lin)

IV. UNDERSTANDING OF THE LAW

13. In preparing and expressing my opinions and considering the subject matter of the challenged patent, I am relying on certain basic legal principles that counsel have explained to me. These principles are discussed below.

A. Claim Construction

14. I understand that the scope of a patent is defined by its claims. I understand that a claim can be:

- a. a method claim, which covers a process/activity, or
- b. an apparatus claim, which covers a physical machine, etc.

15. I understand that the first step in determining the validity of a claim is for the claim to be properly construed. I have been further advised that, in an *inter partes* review proceeding, the claims of a patent are typically given their ordinary and customary meaning as would be understood by one of ordinary skill in the art in the context of the claims and the patent disclosure (specification).

16. I further understand that an inventor can provide special definitions for specific claim term(s) within the patent. However, any special definition for a claim term must be set forth in the specification with reasonable clarity and precision.

B. Invalidity

17. I have been informed that a claim may be invalid as obvious if the subject matter described by the claim, as a whole, would have been obvious to a POSITA at the time the claimed invention was made. I understand that the standard for obviousness in an inter partes review proceeding is by a preponderance of the evidence.

18. I have also been informed that a determination of obviousness involves an analysis of the scope and content of the prior art, the similarities between the claimed invention and the prior art, and the level of ordinary skill in the art. I have been informed and understand that a prior art reference should be viewed as a whole.

19. I have been informed that, in considering whether an invention for a claimed combination would have been obvious, I may assess whether there are

apparent reasons to combine known elements in the prior art in the manner claimed in view of interrelated teachings of multiple prior art references, the effects of demands known to the design community or present in the market place, and/or the background knowledge possessed by a POSITA. I also understand that other principles may be relied on in evaluating whether a claimed invention would have been obvious.

20. I have been informed that, in making a determination as to whether or not the claimed invention would have been obvious to a POSITA, one is to consider certain objective indicators of non-obviousness if they are present, such as: commercial success of product(s) practicing the claimed invention; long-felt but unsolved need; teaching away; unexpected results; copying; and praise by others in the field. I understand that, for such objective evidence to be relevant to the non-obviousness of claim, there must be a causal relationship (called a “nexus”) between the claim and the evidence. I also understand that this nexus must be based on a novel element of the claim rather than something available in the prior art.

21. I have also been informed and understand that, when considering the obviousness of a patent claim, one should consider whether a reason or motivation existed for combining the elements of the references in the manner claimed, and that the prior art must create a reasonable expectation of success in producing the claimed subject matter.

V. SEMICONDUCTOR TRANSISTOR TECHNOLOGY PRIMER

22. The following is a brief primer of semiconductor transistors to establish a foundation of common terms and concepts that can be used in addressing the defects in the Petition. These terms and concepts focus on: (1) the basic components of transistors; and (2) common process steps for creating transistors.

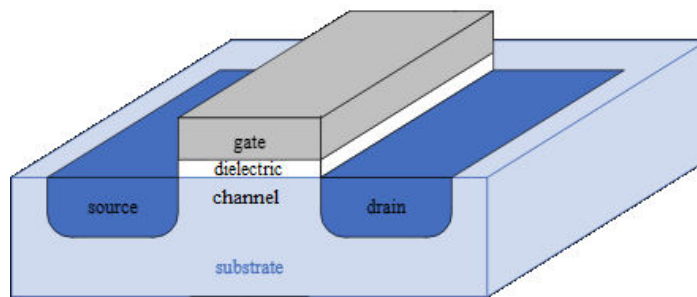
A. Basic Transistor Components

23. Today's semiconductor devices trace their lineage back to the first computers of the 1940s, which used vacuum tubes to perform two key electrical functions: switching (*i.e.*, turning access to electrical current on and off) and amplification (*i.e.*, increasing the amplitude of a signal while retaining its electrical characteristics). EX2002 at 1-2. Where earlier tube devices used a vacuum tube to control the flow of electrons (turning electrical current on and off), today's semiconductor devices use transistors. EX2002 at 3.

24. One type of transistor typically used in an integrated circuit (or "chip") is a "field effect transistor," or FET. Materials used to build such transistors are divided into three categories based on their ability to conduct electrical current: conductors, dielectrics, and semiconductors. EX2002 at 29-34. In a conductor (*e.g.*, a metal), electric current can flow freely. EX2002 at 29. A dielectric (*e.g.*, silicon dioxide) is an insulative material at the opposite end of the conductivity spectrum and has a high resistance to the flow of current. EX2002 at 30. Semiconductors

(e.g., silicon) fall between conductors and dielectrics and have some conducting and some resisting ability. EX2002 at 31-34.

25. The simplified FET below illustrates how these materials may be used to create a semiconductor transistor device. As shown, the transistor is built on a semiconductor substrate and comprises a source, a drain, a gate, and a channel. *See, e.g.,* EX2002 at 510-511. The source, drain and channel comprise semiconductor material, the gate comprises a conductor, and the gate and channel are separated by a thin dielectric layer.



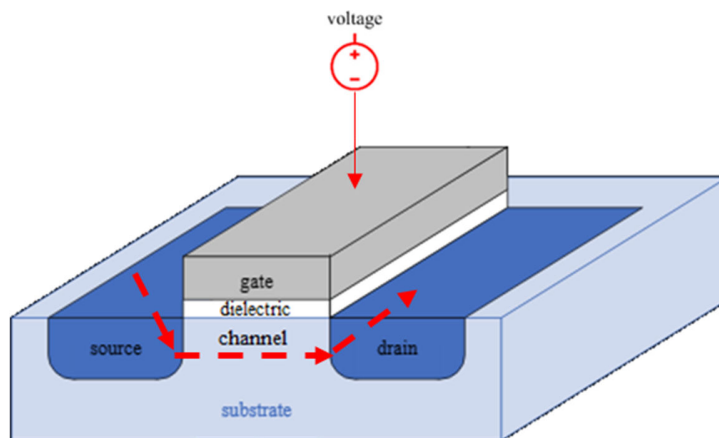
See, e.g., EX2002 at 510-511.

26. The source and drain are regions in the semiconductor substrate that are either rich in electrons (a negative, or n-type, region) or rich in holes (a positive, or p-type, region). EX2002 at 26-28, 427-28. The channel is a region under the gate and between the source and drain, and is of the opposite type to that of the source and drain. In other words, if the source and drain are n-type regions, then the channel will be a p-type region (and vice versa). EX2002 at 510-511.

27. The gate is a conductor (or semiconductor) located above the channel.

In this simplified version of a FET, there is a dielectric between the channel and the gate. EX2002 at 510-511. When a voltage is applied to the gate, the dielectric prevents the “flow of charge” (current) between the gate and the channel, but the applied voltage results in the creation of a “field effect” in the channel. EX2002 at 510-511. This “field effect” either builds up or depletes the charges in the channel (depending on whether it is a p- or n-type channel). EX2002 at 510-511.

28. As illustrated below, this field effect allows charge to flow from the source, through the channel, to the drain. Thus, selectively applying voltage to the gate switches the transistor on and off, starting and stopping drain-to-source or source-to-drain current.



See, e.g., EX2002 at 510-511 (annotated).

B. Processes For Manufacturing Integrated Circuits And Transistors

1. The Four Stages Of Fabricating Integrated Circuits

29. The intricate, complex manufacturing process developed over the years for achieving such highly-dense integrated circuits can be divided into four distinct stages: (1) material preparation; (2) wafer preparation; (3) wafer fabrication; and (4) packaging.

30. In the first stage, the semiconductor material itself is created. EX2002 at 13. For a silicon semiconductor, the raw starting material is sand, which is converted to pure silicon with a polysilicon structure. EX2002 at 13.

31. In the second stage, the semiconductor material is first formed into a silicon crystal with specific electrical and structural parameters, and it is then sliced into thin disks called “wafers.” EX2002 at 13-14. A wafer acts as a semiconductor substrate on and in which transistors may be formed.

32. The third stage is wafer fabrication, during which individual integrated circuits are formed in and on the wafer semiconductor substrate. EX2002 at 14. Thousands of integrated circuits can be formed on the substrate of a single wafer. EX2002 at 14.

33. In the packaging stage, the wafer is separated into individual chips. EX2002 at 14-15.

2. The Wafer Fabrication Stage

34. The third manufacturing stage, wafer fabrication, is the one most relevant here, and it can take several thousand steps, during which transistors and other devices are formed in and on the wafer's substrate. EX2002 at 14. These steps are generally performed using three categories of materials (conductors, semiconductors, and dielectrics) in four basic operations (layering, patterning, doping, and heat treatments). *See* EX2002 at 29-31, 71. For purposes of understanding the Petition and its deficiencies, the two most important basic operations are layering and patterning.

35. **Layering** is the operation used to add thin layers to the semiconductor substrate. EX2002 at 72. The layers may be conductors, semiconductors, or dielectrics; and they can have a variety of functions and be made in a variety of ways. EX2002 at 72.

36. For example, one way of adding a layer of material is to deposit that material onto the semiconductor substrate. Another way of adding a layer of material is to grow the material on the semiconductor substrate. After an initial layer is added to the semiconductor substrate, additional layers may be added to the earlier layers using similar growth or deposition processes. To illustrate, the transistor structure shown below shows a number of layers that have been added to the wafer's semiconductor substrate, some deposited, some grown. EX2002 at 72.

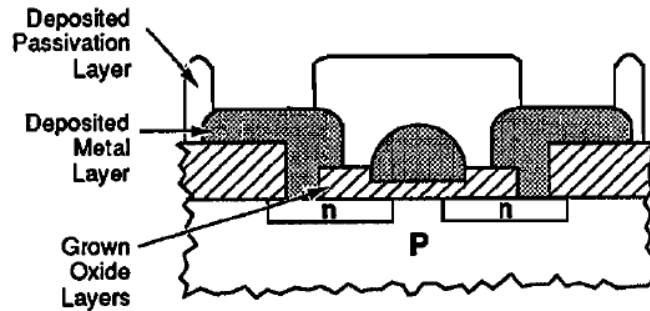


Figure 4.4 Cross section of completed metal gate MOS transistor with grown and deposited layers.

37. **Patterning** is the series of steps to remove (etch away) selected portions of the semiconductor substrate or one or more layers of materials that were added during one or more prior layering operations. EX2002 at 72-73. This creates a pattern on the wafer surface. EX2002 at 72-73.

38. The patterning may result in one or more holes in the layered material or one or more remaining islands of material. EX2002 at 72-73. For example, the following figures illustrate the use of patterning to make (1) a hole in a previously formed layer: and (2) an island from a previously formed layer:

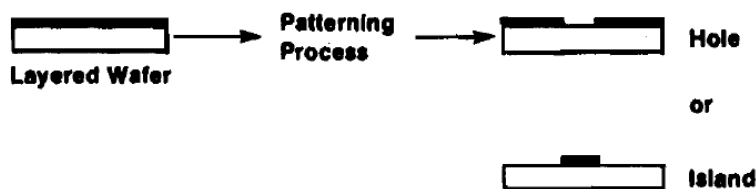


Figure 4.7 Patterning.

39. The repeated combination of layering and patterning in different sequences and variations is critical to the formation of transistors in and on the semiconductor wafer:

These parts are created one layer at a time by the combination of putting a layer on the surface and removing a portion, with a patterning process, to leave a specific shape. The goal of the patterning operations is to create the desired shapes in the exact dimensions (feature size) required by the circuit design, and to locate them in their proper location on the wafer surface and in relation to the other parts.

EX2002 at 73.

VI. THE CHALLENGED '735 PATENT

A. The Prior Art Problem And Exemplary Inventive Embodiments

40. The '735 Patent describes and claims an improved “void-free semiconductor device and a method of fabricating the same.” EX1001, 1:8-10. Specifically, the patent describes methods for eliminating the formation of voids in a gate structure when fabricating a metal gate using a “gate last process.” *Id.*, 1:63-67.

41. Generally, a “gate last” process (also commonly referred to as a “replacement metal gate” or “RMG” process) is a semiconductor manufacturing process where a sacrificial “dummy gate” is initially formed. Subsequently, after high-temperature processing is performed on the source/drain regions, the dummy gate is removed, leaving a trench. A metal gate is then formed within the trench. Beneficially, this technique avoids potential damage to the delicate metal gate due to high temperatures. The '735 Patent's Background section describes a conventional gate-last process:

In a conventional gate structure composed of a high dielectric constant dielectric layer and a metal gate, the dummy patterns are first formed and then the gate structures are formed in the current method. In other words, the dummy patterns and the interlayer dielectric layer are first formed on the substrate. Next, the dummy patterns are removed, and then the metal gate structures are formed in the openings that are formed after the removal of the dummy patterns.

EX1001, 1:32-39.

42. However, such conventional gate-last processes result in the formation of voids in the metal gate, resulting in problems with performance and reliability of the transistor. EX1001, 1:40-54. These issues stem from the fact that conventional dummy gate patterns were “usually shaped into trapezoids having a narrow top and a wide bottom, so that an included angle between the top side wall of each the dummy pattern and the surface of the inter layer dielectric layer is about 88°-89°.” *Id.*, 1:40-46. Thus, when the dummy pattern was removed, the resulting trench had “an opening with a narrower top.” *Id.*, 1:46-49. “Hence, when the opening is filled with the metal layer by a sputtering process, the effect of metal gap fill is poor, so that problems such as overhang and the like usually occur to cause the formation of voids in the metal layer, thereby affecting the reliability and performance of the device.” *Id.*, 1:49-54.

43. The '735 Patent provides a novel solution to this void-formation problem by using a particularly-shaped dummy gate pattern: “Each dummy pattern includes a top, a bottom, and a neck arranged between the top and the bottom” where “the width of the neck is narrower than that of the top.” *Id.*, 2:3-6. Figure 1B illustrates such a dummy pattern:

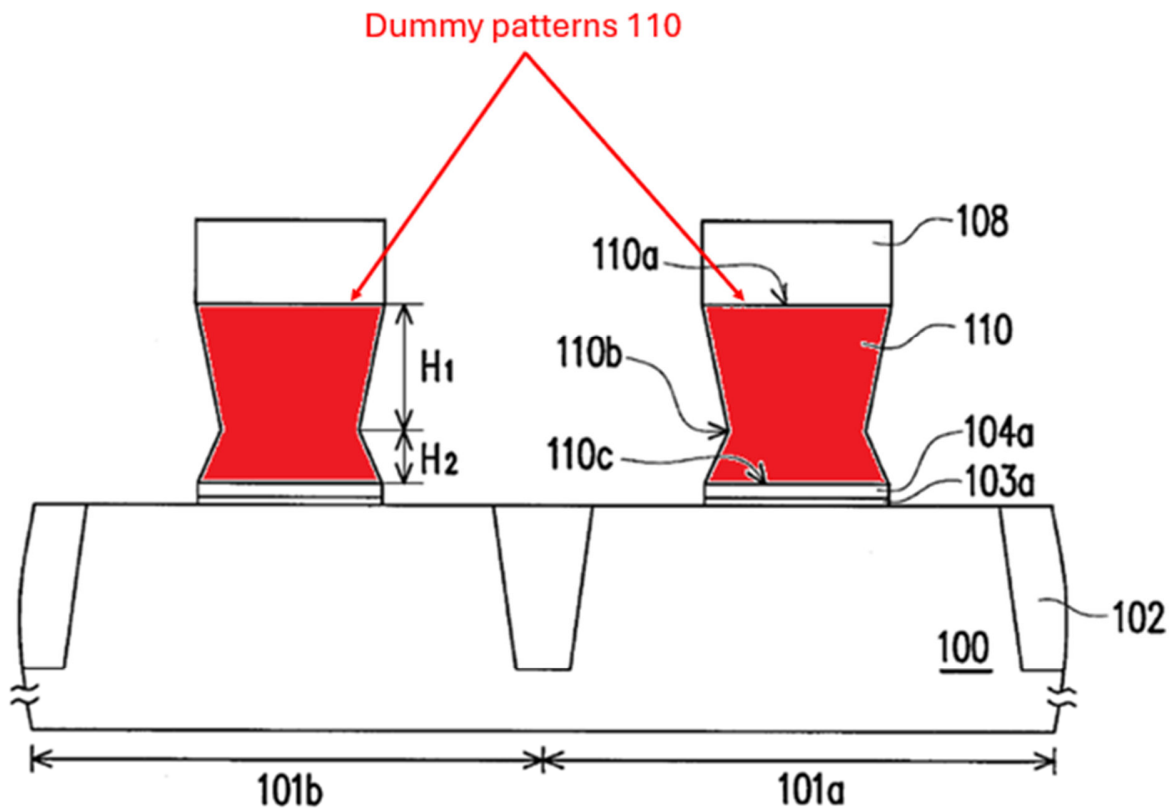


FIG. 1B

EX1001, Fig. 1B (annotated).

44. “Each dummy pattern 110 includes a top 110a, a neck 110b, and a bottom 110c.” *Id.*, 5:21-22. As shown in Figure 1B above, “[t]he width of the neck

45. Subsequently, several high-temperature processing steps are carried out. These high-temperature steps include that: (1) “the dummy patterns 110 are used as masks for carrying out the ion implantation process so as to form lightly-doped regions 113a”; (2) “spacers 112 are formed on sidewalls of the dummy patterns 110”; and (3) “[a]fterwards, source/drain regions 114a are formed in the substrate 100 at the respective sides of the dummy pattern 110”:



46. The dummy patterns 110 absorb all the thermal stress generated during these processing steps.

B. The Formation Of Trenches By Removing The Dummy Patterns

47. As described in the '735 Patent, the disclosed inventive embodiment next includes removing the foregoing specially-shaped dummy gate to form a “trench” with that same shape. For example, as shown in Figure 1D, “the dummy patterns 110 are removed to form the trenches 120”:

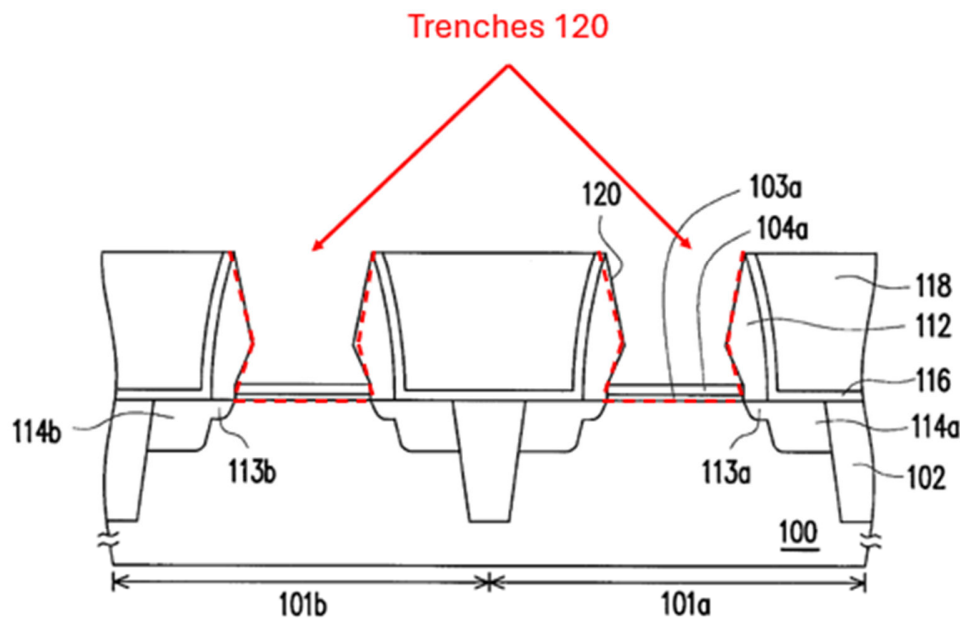


FIG. 1D

EX1001, 7:35-37, Fig. 1D (annotated).

48. As shown above, “since the width of the neck is narrower than that of the top of each dummy pattern, the trench 120 formed after the removal of each dummy pattern is shaped into a structure having a wide opening in the top portion.”

Id., 8:23-27. “That is, an included angle θ_1 [labelled in Fig. 1E below] between the sidewall of the top 120a of the trench 120 and the surface of the dielectric layer 118 is larger than 90° , for instance.” *Id.*, 8:27-29.

49. The '735 Patent consistently describes the disclosed (and claimed) “trench” as the recess that is formed from removing the dummy gate pattern. EX1001, Abstract, 2:9-10, 7:35-39, 8:23-27. Thus, the trench that is formed from removing the dummy gate pattern has the same geometry as the dummy pattern. EX1001, 8:23-27. For example, the '735 Patent explains: “It should be illustrated that since the width of the neck is narrower than that of the top of each dummy pattern, the trench 120 formed after the removal of each dummy pattern is shaped into a structure having a wide opening in the top portion.” EX1001, 8:23-27. As shown in Figures 1C and 1D of the '735 Patent, because the dummy gate pattern 110 has a width of the neck that is narrower than a width of the top, the resulting trench 120 also has “a width of the neck [that] is narrower than a width of the top”:

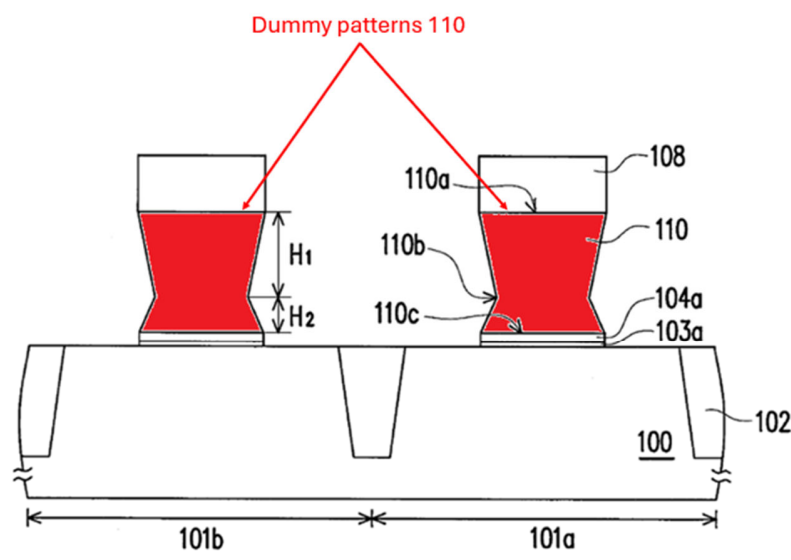


FIG. 1B

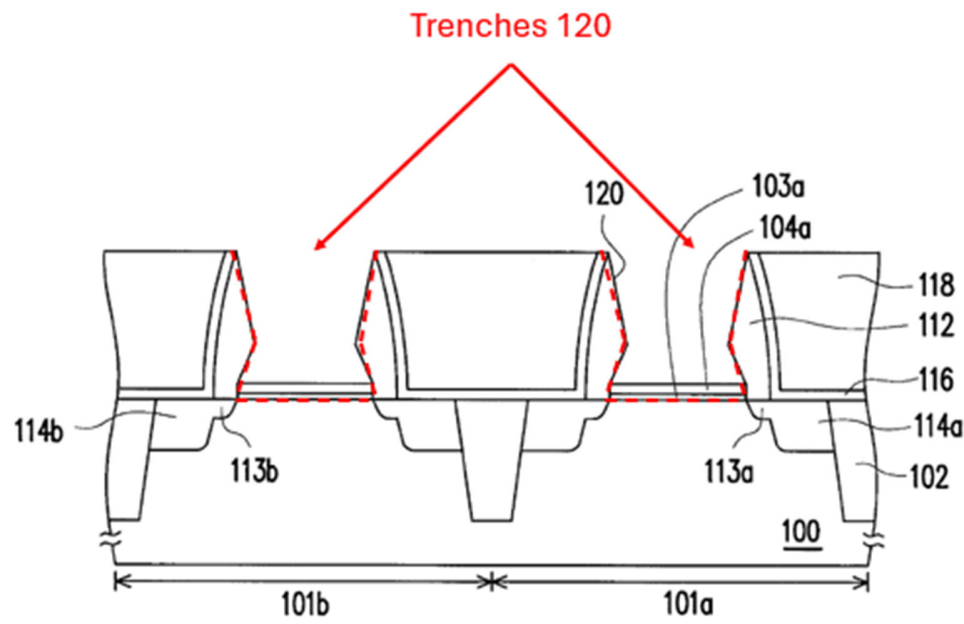


FIG. 1D

EX1001, Figs. 1C and 1D (annotated)

50. The '735 Patent explains that having the trench geometry match the dummy pattern's geometry grants the additional advantage of "facilitat[ing] rapid removal of the dummy patterns." EX1001, 8:29-33. That is, because the dummy pattern is wider at the top, when removing the dummy pattern by wet etching, the dummy pattern material is more easily removed to form the trench. *See id.*, 7:47-49. Moreover, unlike the prior art, forming the dummy pattern with the required geometry of the trench also obviates the need to perform further processing steps to ensure good gap fill effects when depositing the gate metal into the trench, as explained in more detail below.

C. The Formation Of Gate Structures In The Resulting Trenches

51. Finally, formed in each trench is a metal gate structure 130 comprising high dielectric layer 104a, work metal function layer 122, and metal layer 126. EX1001, 7:49-55. As illustrated below in annotated Figure 1E, a work function metal layer 122 is formed conformally on the surface of the trench 120, including the exposed high dielectric layer 104a. EX1001, 7:57-58, 8:49-9:2. "Next, a metal layer 126 is filled into the trenches 120 so as to form gate structures 130a and 130b respectively":

Gate structures 130a
and 130b comprising:
high dielectric constant
layers 104a, work
function metal layers
122, and metal layers
126

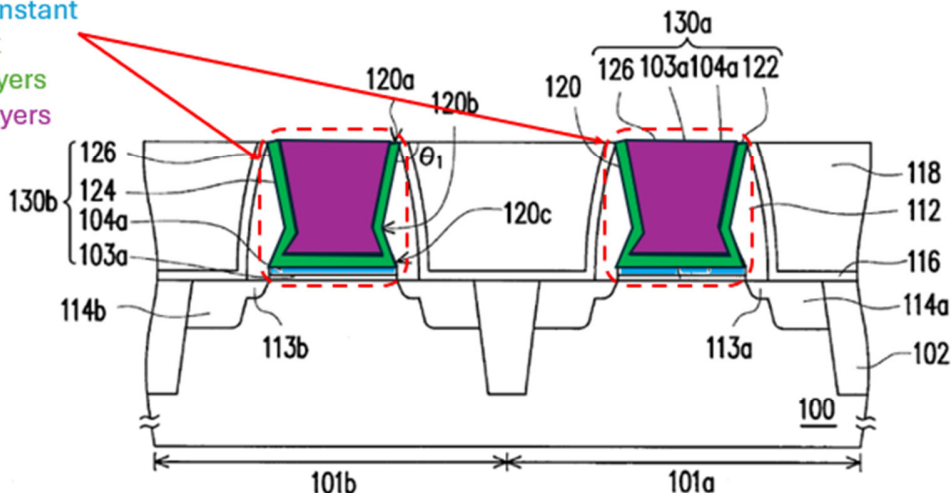


FIG. 1E

Id., 8:6-7, Fig. 1E (annotated).

52. Due to the geometry of the trenches, “the trenches 120 each having a wide opening in the top portion not only facilitate the rapid removal of the dummy patterns, but also have superior metal gap fill effect when forming the metal layer 126 so that voids are not formed easily.” *Id.*, 8:29-33. In this way, “[t]he invention provides a semiconductor device, in which a gate structure thereof is disposed in a trench having a wider opening in a top, and the semiconductor therefore includes a void-free metal layer.” *Id.*, 1:62-65.

53. As described, a critical part of each gate structure is its “work function metal layer,” which the ’735 Patent describes is a metal layer that “prevent[s] the

threshold voltage from increasing and therefore reducing the resistance of the device.” EX1001, 1:27-31.

54. The purpose of employing these dual metal layers is to ensure that the gate has a suitable electrical threshold voltage, or “work function.” As explained above, a metal gate serves as a conductor which allows for controlling the charge in the channel underlying the gate. Thus, a suitable gate metal must be selected based on several requirements: the gate metal must be electrically conductive to transmit the gate voltage uniformly, structurally stable, and compatible with the gate dielectric layer to avoid interface issues that degrade mobility and reliability. However, the gate material must also allow for tight control of the device’s threshold voltage, which determines when the transistor turns on. A single metal that includes all of these characteristics is often impractical, motivating a layered gate stack such as the ’735 Patent’s claimed gate structure.

55. In the ’735 Patent’s gate structure, “[t]he work function of the gate structure 130a is determined by the metal layer 126 and the work function metal layer 122 underneath.” EX1001, 8:14-16. As the ’735 Patent explains, the purpose of the work function metal layer is “to prevent the threshold voltage from increasing and therefore reducing the resistance of the device.” EX1001, 1:27-31. Thus, the ’735 Patent’s claimed “work function metal layer” is a thin metal layer that serves to tune the threshold voltage value of the gate, while the second “metal layer” acts

as the main gate electrode. In other words, put simply, the work function metal layer is necessary because the metal chosen as the main gate electrode (e.g., aluminum or titanium) cannot provide a suitable threshold voltage. The work function metal layer, therefore, serves to tune or adjust the threshold voltage of the gate as a whole.

D. The Challenged Claims

56. The Petition challenges independent claim 1 and dependent claims 2-6, each of which includes the foregoing inventive concepts and combinations. For example, independent claim 1 recites:

A semiconductor device, comprising:

a substrate, disposed with a dielectric layer thereon, wherein a trench is disposed in the dielectric layer;

a gate structure, located in the trench and comprising a high dielectric constant layer, a work function metal layer, and a metal layer sequentially disposed on the substrate; and

a source/drain region, disposed in the substrate at respective sides of the gate structure,

wherein the trench comprises a top, a bottom, and a neck arranged between the top and the bottom, *a width of the neck is narrower than a width of the top, and the width of the neck is narrower than or equal to a width of the bottom.*

EX1001, claim 1.

VII. THE PETITION GROUNDS AND ASSERTED ART

57. The Petition asserts the following grounds challenging claims 1-6 of the '735 Patent:

Ground	Challenged Claims	Statutory Basis ¹	Prior Art
1A	1, 3-6	§ 102	Chuang (TSMC-1004)
1B	2	§ 103	Chuang, Brask (TSMC-1012)
2A	1, 3-6	§ 102	Lin (TSMC-1005)
2B	2	§ 103	Lin, Brask
3A	1, 2	§ 102	Brask
3B	1, 2	§ 103	Brask

Pet., 2.

A. Chuang (Grounds 1A and 1B)

58. Grounds 1A and 1B rely solely or primarily on the Chuang reference. Chuang “relates generally [to] an integrated circuit device and, more particularly, to a gate structure and method of forming a gate of an integrated circuit device.” EX1004-Chuang, ¶[0002]. Contrary to the Petition’s assertions, Chuang’s approach differs from that of the ’735 Patent in that Chuang’s dummy pattern is not shaped such that it is wider at the top than in the neck, but rather is rectangular. As a result, the trench formed from removing the dummy pattern is also rectangular, rather than having varying widths.

59. For example, as illustrated in Chuang’s annotated Figure 1, Chuang’s fabrication process employs a conventional, **rectangular** “dummy gate pattern 118”:

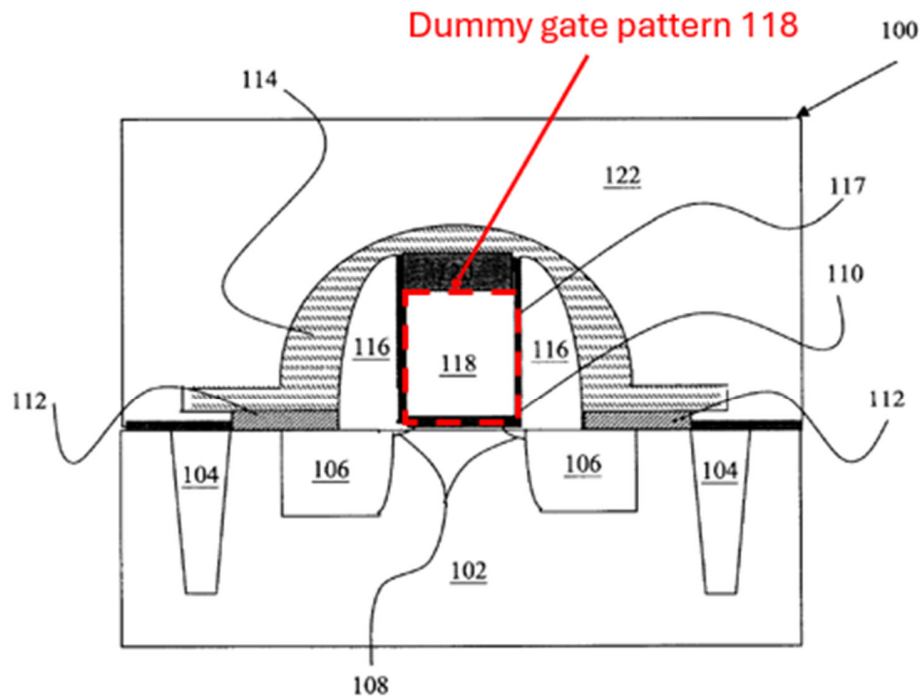


Fig. 1

EX1004-Chuang, ¶[0016], Fig. 1 (annotated).

60. Subsequently, “the dummy gate structure 118 may be removed.” “The selective removal of the dummy gate structure 118 provides a trench 302 within which a metal gate may be formed.” *Id.*, ¶[0024]. As illustrated below in annotated Chuang Fig. 3, because Chuang’s dummy gate pattern is rectangular, the resulting trench 302 is also rectangular:

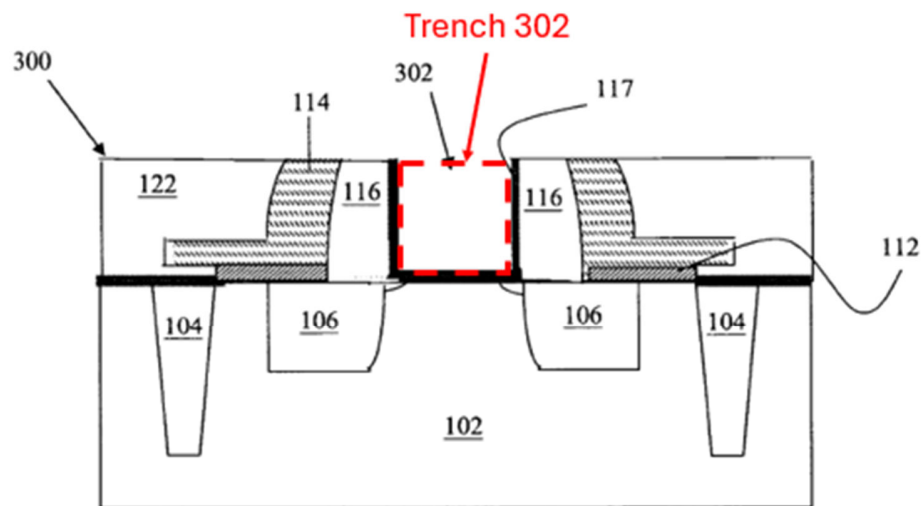


Fig. 3

EX1004-Chuang, Fig. 3 (annotated).

61. Thus, rather than create a trench with a wider top and a narrow neck, Chuang discloses forming a rectangular trench of uniform width. It is only after the dummy gate and the trench is formed that Chuang then describes subsequently using additional processes to widen the area surrounding the top of the trench to form the profile shown in Chuang's Figure 7:

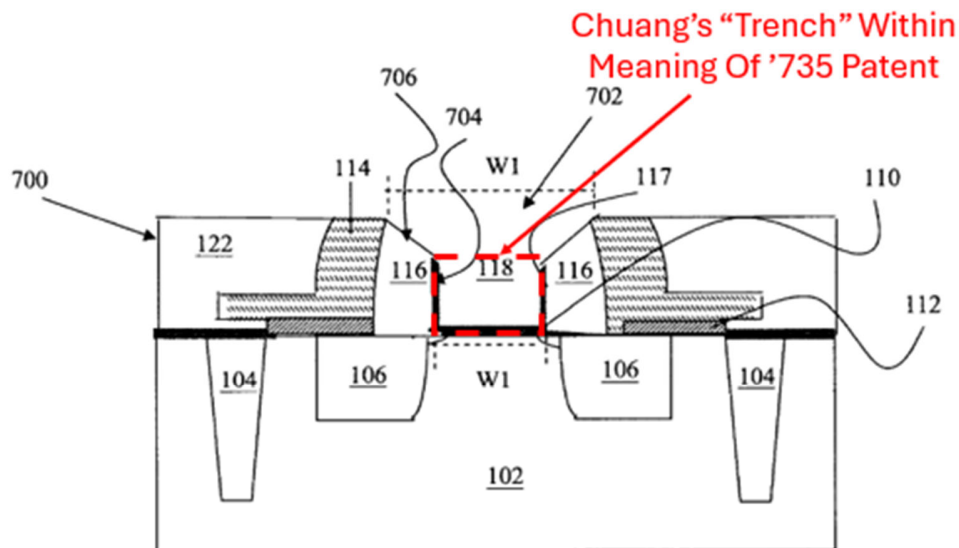


Fig. 7

Id., Fig. 7 (annotated).

62. This profile is not the claimed “trench,” which is the recess formed by removing the dummy gate. This is reinforced by Chuang’s disclosure that “[t]he profile may be modified using . . . suitable processes capable of removal of portions of the adjacent layers.” EX1004-Chuang, ¶[0031]. That is, the modified profile is formed by etching away portions of the spacers 116 and stop layer 114, rather than the dielectric layer 122.

B. Lin (Grounds 2A and 2B)

63. Grounds 2A and 2B rely solely or primarily on the Lin reference. But like Chuang—and unlike the ’735 Patent—Lin’s dummy pattern and resulting trench

is not shaped such that they are wider at the top than in the neck, but rather are rectangular.

64. For example, as annotated below in Lin Figure 2, like Chuang, Lin employs a **rectangular** dummy gate pattern 54:

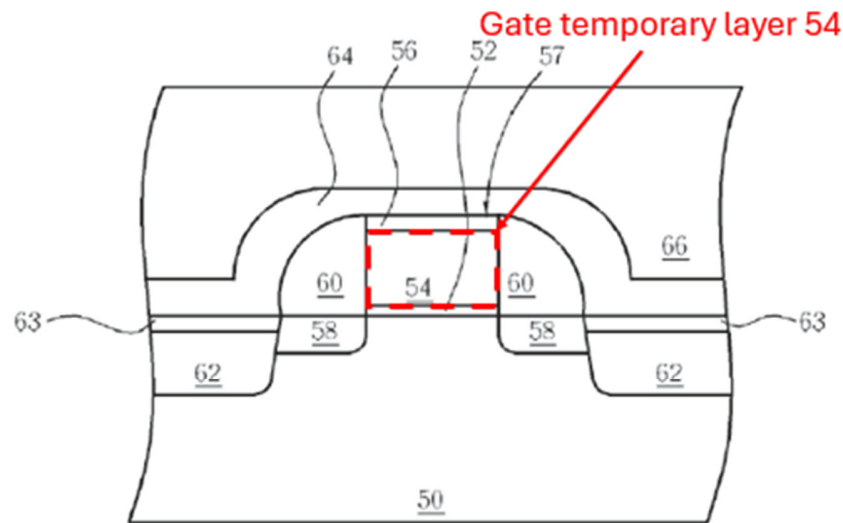


Fig. 2

EX1005-Lin, ¶[0018], Fig. 2 (annotated).

65. Next, as shown in Figure 3, an etching process is performed and “a bevel edge 68” is formed above the dummy gate pattern 54:

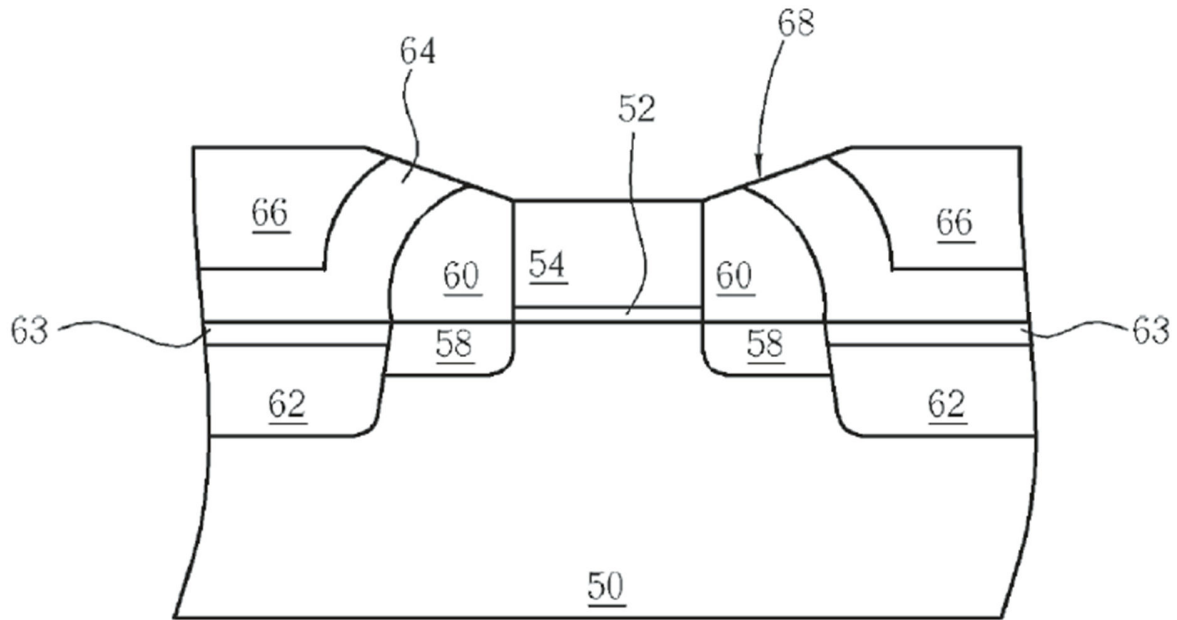


Fig. 3

EX1005-Lin, $\nabla[0020]$, Fig. 3.

66. “After the bevel edge is finished... a recess 72 is formed by an etching process to remove the [dummy] gate temporary layer 54 and the gate insulating layer 52,” as shown in Figure 4:

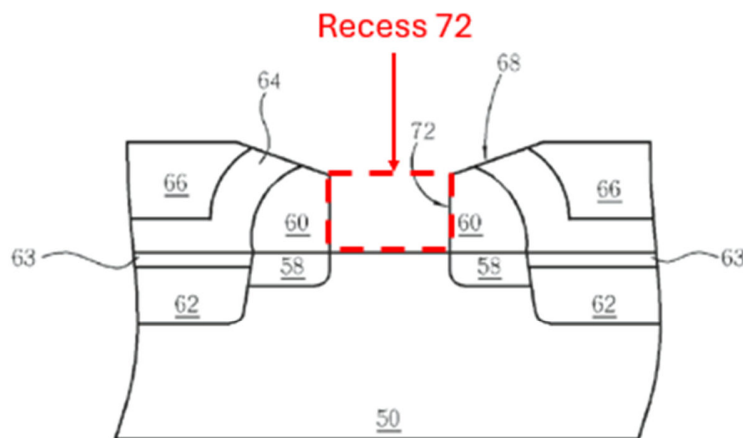


Fig. 4

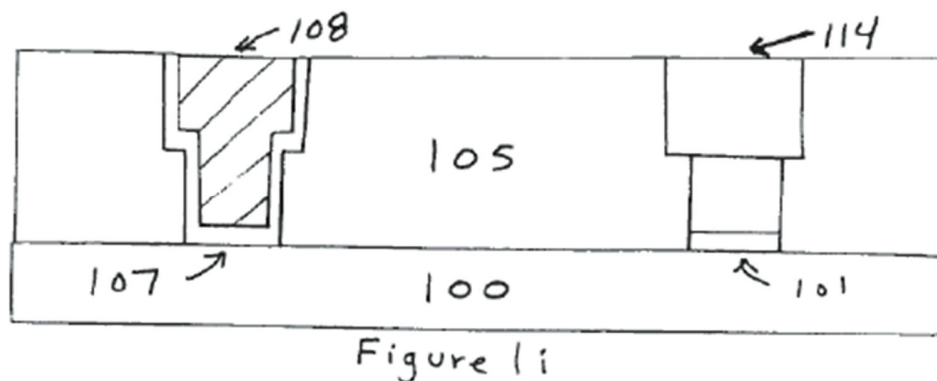
EX1005-Lin, ¶[0023], Fig. 4 (annotated).

67. Notably, the “recess 72” (i.e., trench) formed from the removal of the dummy gate 52 is **rectangular** in shape and does **not** include the bevel edge 68.

68. Lin also discloses an embodiment where, like in Chuang, the bevel edge is formed **after** the formation of a trench. *See* EX1005-Lin, ¶[0032] Figs. 7-9. But consistent with the '735 patent, which describes that the trench is the opening formed by removing the dummy gate, Lin describes that the bevel edge is separate from the trench. For example, Lin's Abstract distinguishes between the two, describing that “[a] bevel edge is formed on the spacer, and a trench is formed in the inner sidewall of the spacer” and that “[a] barrier layer, and a metal gate are formed in the trench and on the bevel edge.” EX1005-Lin, Abstract.

C. Brask (Grounds 3A and 3B)

69. Grounds 3A and 3B rely solely on the Brask reference. Brask also relates to a gate-last or replacement gate process. Unlike the '735 Patent, however, in Brask's primary embodiment, the gate structure comprises only a gate dielectric layer 107 and a metal layer 108, as shown in Brask's Figure 1i:

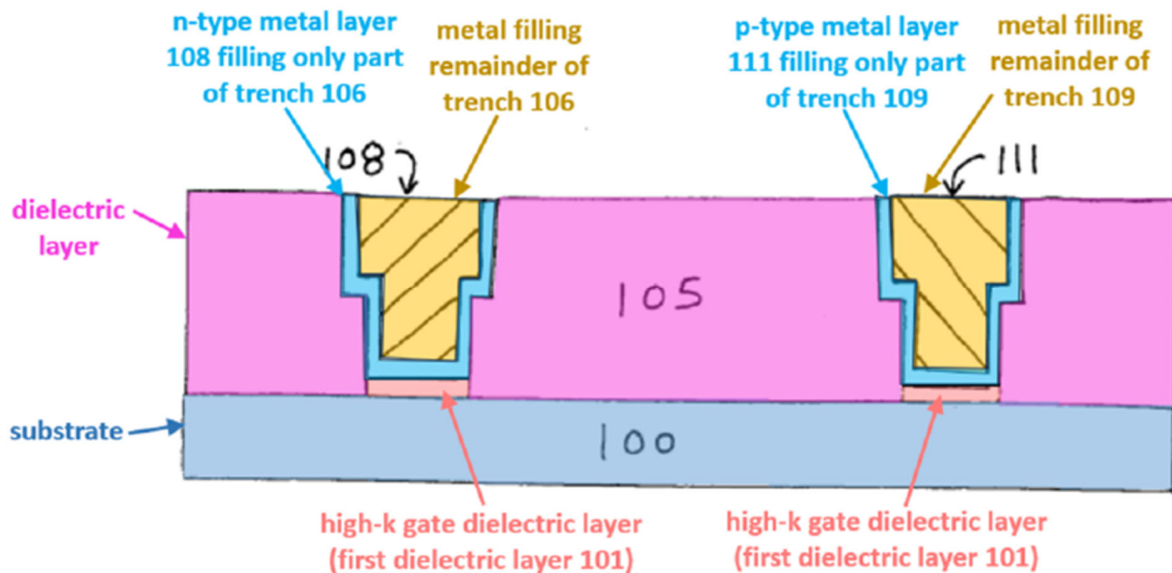


EX1012-Brask, Fig. 1i.

70. Critically, Brask does not describe any of its metal layers—including the one the Petition identifies as the purported “work function metal layer—as “prevent[ing] the threshold voltage from increasing and therefore reducing the resistance of the device.”

71. The Petition points to teachings in three separate embodiments in Brask (Brask's main embodiment and two separate alternative embodiments). Pet., 35-36. First, the Petition points to an alternative embodiment in which “first dielectric layer 101 may comprise a high-k gate dielectric layer that is retained after sacrificial structure 104 and 114 are removed.” Pet., 35-36 (citing EX1012-Brask, 7:3-9).

Second, the Petition points to another alternative embodiment in which “n-type metal layer 108 may fill only part of trench 106, with the remainder of the trench being filled with a material that may be easily polished, e.g., tungsten, aluminum, titanium, or titanium nitride.” Pet., 36 (citing EX1012-Brask, 6:7-12). The Petition provides a figure purporting to illustrate a “Representative Embodiment” of Brask that comprises teachings from each of these three separate embodiments:



Pet., 37.

VIII. THE PETITION FAILS TO ESTABLISH THE REQUIRED LIKELIHOOD OF SUCCESS

A. Grounds 1A And 1B

72. Both Grounds 1A and 1B fail because Chuang does not disclose the claim limitations “wherein the trench comprises a top, a bottom, and a neck arranged

between the top and the bottom, a width of the neck is narrower than a width of the top,” as recited by independent claim 1.

73. As explained above in Section VI.B, the '735 Patent's claimed “trench” is a recess formed from the removal of a dummy gate pattern. EX1001, Abstract, 2:9-10, 7:35-39, 8:23-27. As shown in Figures 1C and 1D of the '735 Patent, because the dummy gate pattern 110 has a width of the neck that is narrower than a width of the top, the resulting trench 120 also has “a width of the neck [that] is narrower than a width of the top”:

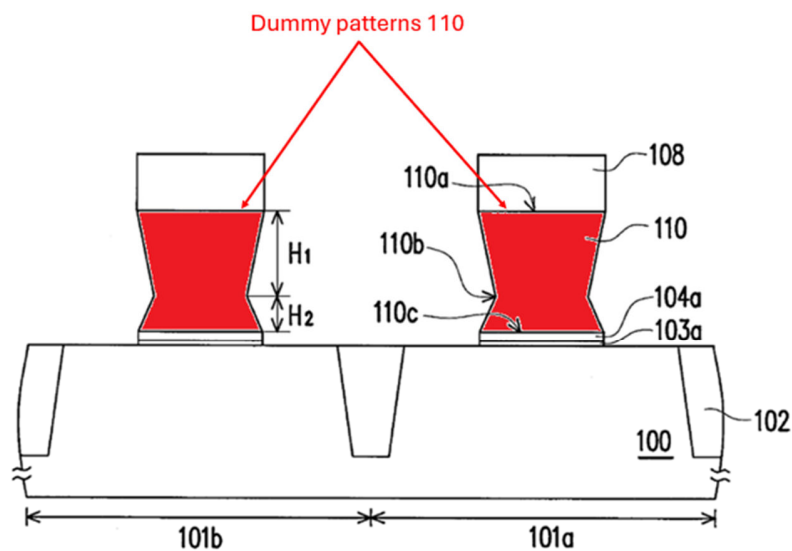


FIG. 1B

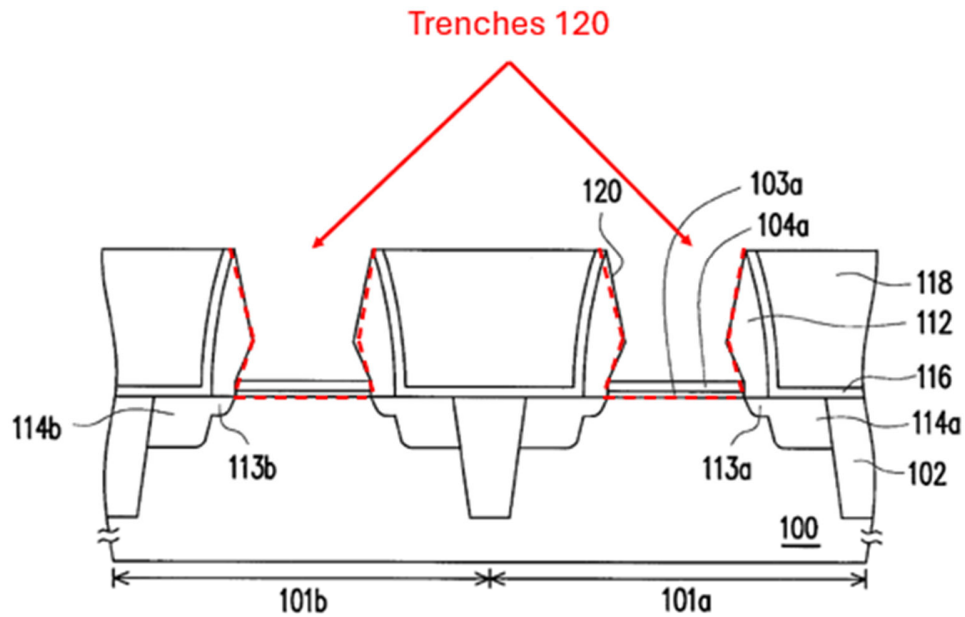


FIG. 1D

EX1001, Figs. 1C and 1D (annotated).

74. In contrast, Chuang discloses using a rectangular “dummy gate pattern 118,” as shown in Figure 1 of Chuang:

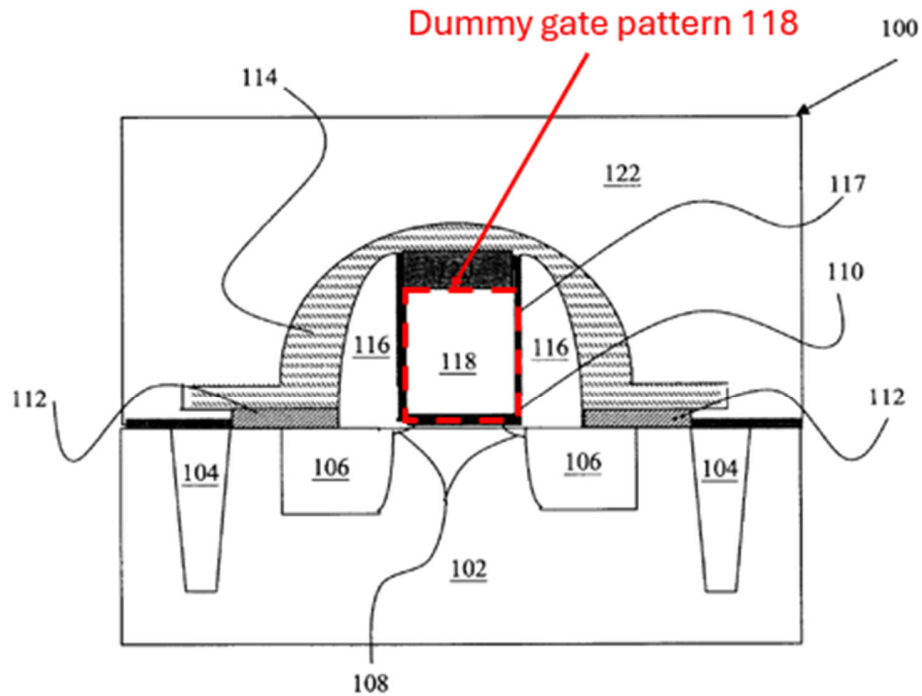


Fig. 1

EX1004-Chuang, ¶[0016], Fig. 1 (annotated).

75. Subsequently, “the dummy gate structure 118 may be removed, providing the device 300 of FIG. 3,” as shown below:

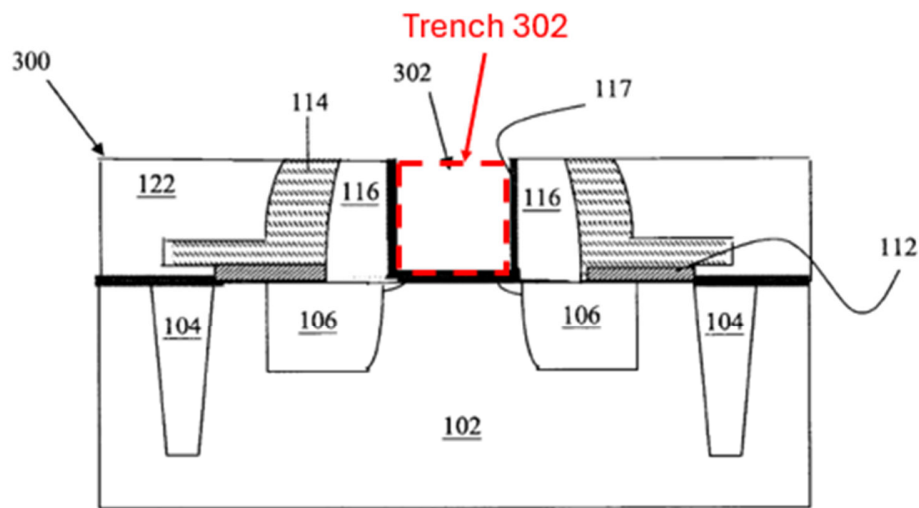


Fig. 3

EX1004-Chuang, Fig. 3 (annotated).

76. “The selective removal of the dummy gate structure 118 provides a trench 302 within which a metal gate may be formed.” *Id.*, ¶[0024]. As illustrated in Chuang’s Fig. 3, because Chuang’s dummy gate pattern is rectangular with uniform widths, the resulting trench 302 is also rectangular with uniform widths. Thus, Chuang does not disclose a trench with “a width of the neck is narrower than a width of the top,” as required by all challenged claims.

77. In alleging that Chuang discloses the claimed “trench,” the Petition fails to consider the ’735 Patent’s explicit disclosure that the trench is the recess formed by removal of the dummy pattern. The Petition alleges that Chuang discloses this limitation because Chuang describes that after the formation of the trench, “[t]he

profile may be modified such that the opening of the trench (e.g., top portion or aperture of the trench) is wider than the bottom of the trench.” *See* Pet., 25-26. In particular, the Petition cites to paragraph 32 of Chuang, which states that “the trench 702 includes a width at its aperture W1 that is greater than the width at the bottom of the trench W2.” Pet., 26 (citing EX1004-Chuang, ¶[0032]. However, a POSITA would have understood that Chuang’s profile modification process only widens the aperture of the trench (i.e., the area immediately outside the trench), rather than the *top portion of the trench*.

78. Instead, a POSITA would have understood that Chuang’s “trench”—within the meaning of the term in the ’735 Patent—is rectangular as shown below:

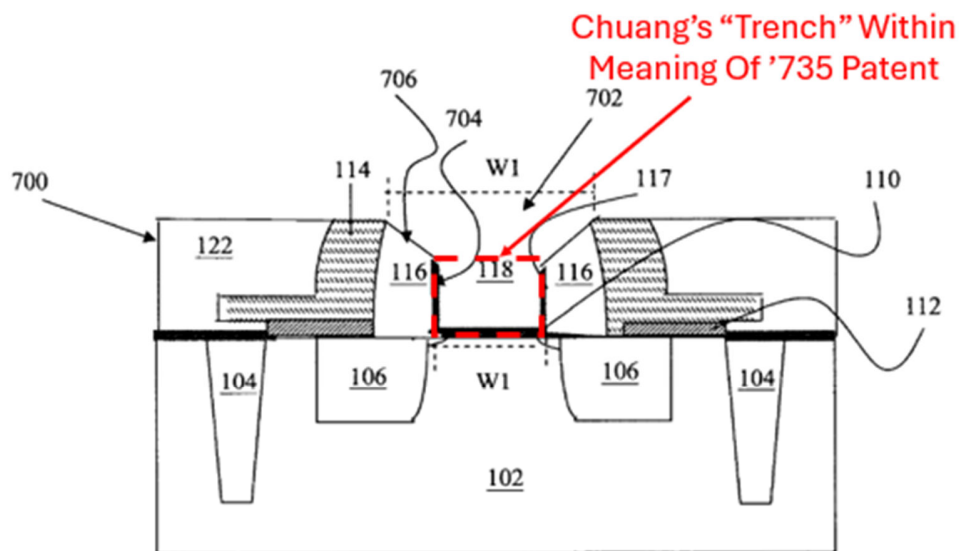


Fig. 7

EX1004-Chuang, Fig. 7 (annotated).

79. Chuang's "modified profile trench 702" does not disclose the '735 Patent's claimed "trench" because it is not the recess formed by removing the dummy gate pattern. The modified profile is formed—after the formation of the trench—by etching away portions of the spacers 116 and stop layer 114, rather than the dielectric layer 122. EX1004-Chuang, ¶[0031].

80. The Petition's analysis does not address the '735 Patent's description of the claimed "trench" as being the recess formed by removing the dummy gate pattern. Pet., 14-17, 24-27. Moreover, the Petition does not propose a construction of the word "trench" and does not allege that Chuang discloses the claimed "trench" in light of the '735 Patent's specification. *Id.* Nor could it, because Chuang's "trench"—within the meaning ascribed by the '735 Patent—is rectangular, rather than being wider at the top.

81. Accordingly, Chuang fails to disclose "wherein the trench comprises a top, a bottom, and a neck arranged between the top and the bottom, *a width of the neck is narrower than a width of the top,*" as required by all challenged claims.

B. Grounds 2A And 2B

82. Both Grounds 2A and 2B fail because Lin does not disclose the claim limitations "wherein the trench comprises a top, a bottom, and a neck arranged

between the top and the bottom, a width of the neck is narrower than a width of the top,” as recited in independent claim 1 and required by all challenged claims.

83. Lin fails to disclose “a width of the neck is narrower than a width of the top” of the trench. As explained above, the ’735 Patent’s claimed “trench” is the recess that is formed from removing the dummy gate pattern. EX1001, Abstract, 2:9-10, 7:35-39, 8:23-27; Thus, the trench has the same geometry as the dummy pattern. EX1001, 8:23-27.

84. In contrast, like Chuang, Lin employs a rectangular dummy gate pattern (“gate temporary layer 54”) with uniform widths, as illustrated in Lin’s Figure 2:

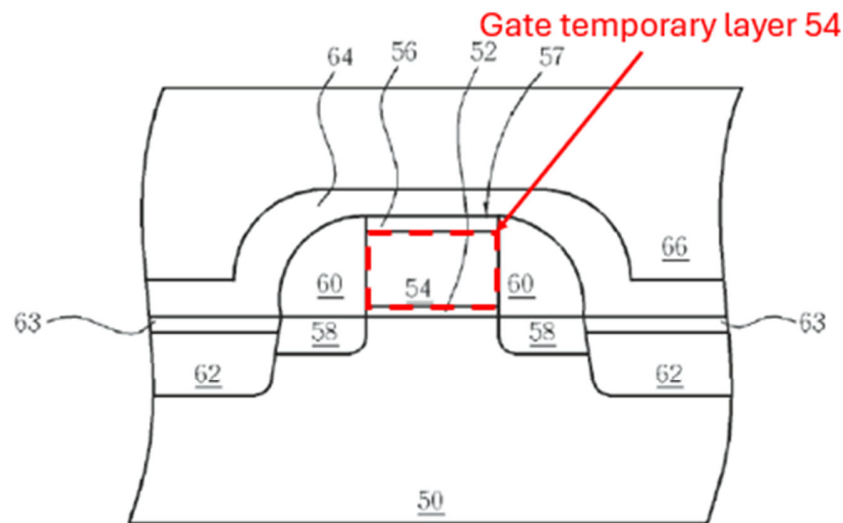


Fig. 2

EX1005-Lin, ¶[0018], Fig. 2 (annotated).

85. Next, as shown in Figure 3, an etching process is performed and “a bevel edge 68” is formed above the gate temporary layer 54:

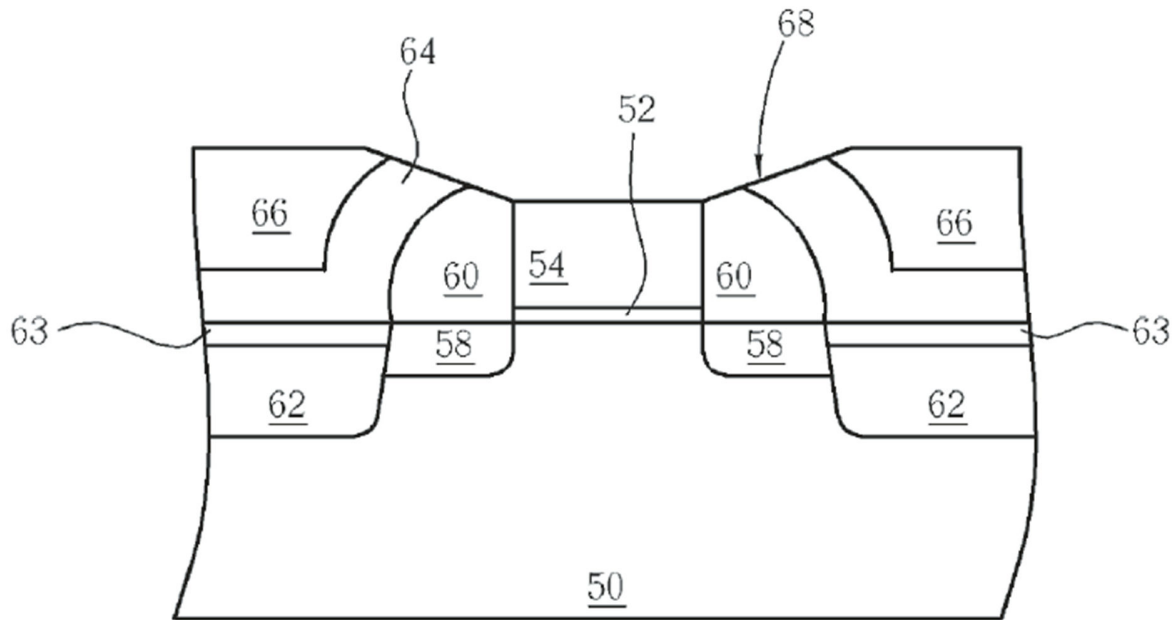


Fig. 3

EX1005-Lin, $\nabla[0020]$, Fig. 3.

86. “After the bevel edge is finished... a recess 72 is formed by an etching process to remove the gate temporary layer 54 and the gate insulating layer 52,” as shown in Figure 4:

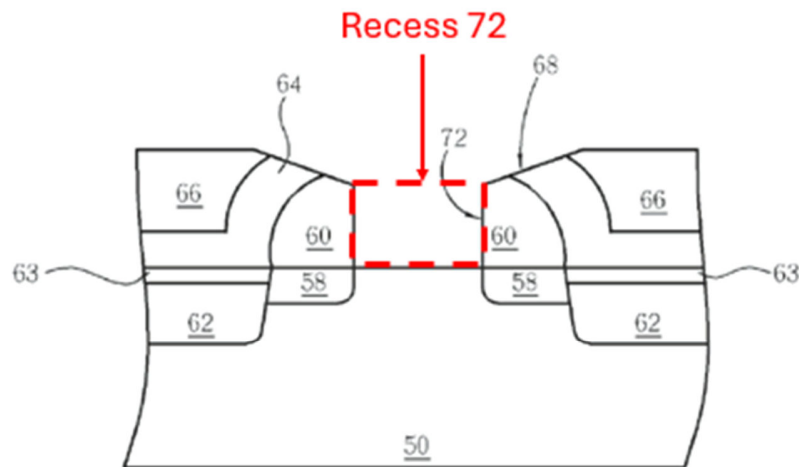


Fig. 4

EX1005-Lin, ¶[0023], Fig. 4 (annotated).

87. As illustrated in Lin's Figure 4 above, because Lin's dummy gate pattern is rectangular with uniform widths, the resulting recess 72 is also rectangular with uniform widths. This is made clear from Lin's Figure 8, which depicts an alternative embodiment in which the recess is formed before the bevel edges:

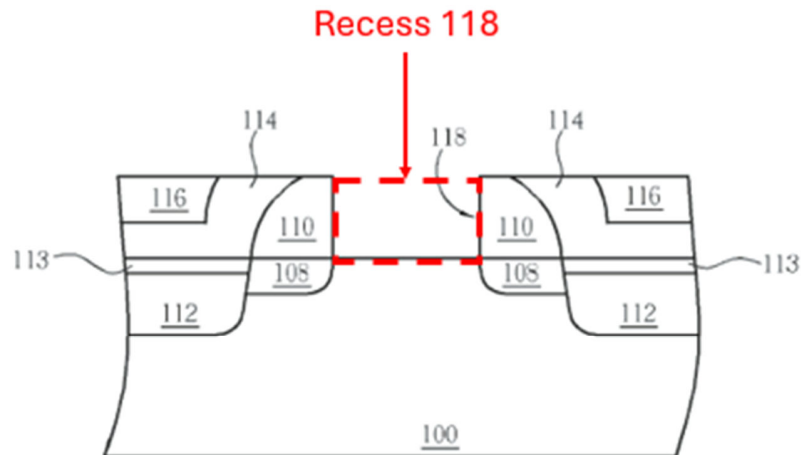


Fig. 8

EX1005-Lin, Fig. 8 (annotated).

88. Thus, Lin does not disclose a trench with “a width of the neck is narrower than a width of the top,” as required by all challenged claims.

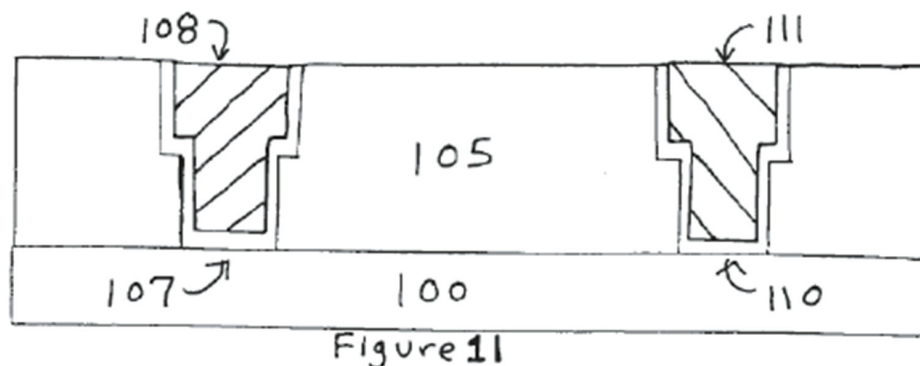
89. The Petition alleges that Lin discloses this limitation by arguing that the bevel edge area in Lin is the top of the trench. *See* Pet., 58-59. But this contradicts Lin, which expressly distinguishes the bevel edge from the trench. EX1005-Lin, Abstract. For example, Lin’s Abstract explains that the bevel edge is separate from the trench itself, stating that “[a] bevel edge is formed on the spacer, and a trench is formed in the inner sidewall of the spacer” and that “[a] barrier layer, and a metal gate are formed in the trench and on the bevel edge.” EX1005-Lin, Abstract.

90. Regardless, the Petition's alleged "trench" in Lin does not disclose the '735 Patent's claimed "trench" because it is not the recess formed by removing the dummy gate pattern. In its analysis, the Petition does not address the '735 Patent's description of the claimed "trench". Pet., 47-49, 57-60. Moreover, the Petition does not propose a construction of the word "trench" and does not allege that Lin discloses the claimed "trench" in light of the '735 Patent's specification. *Id.* Nor could it, because Lin's "trench"—within the meaning ascribed by the '735 Patent—is rectangular, rather than being wider at the top.

C. Grounds 3A And 3B

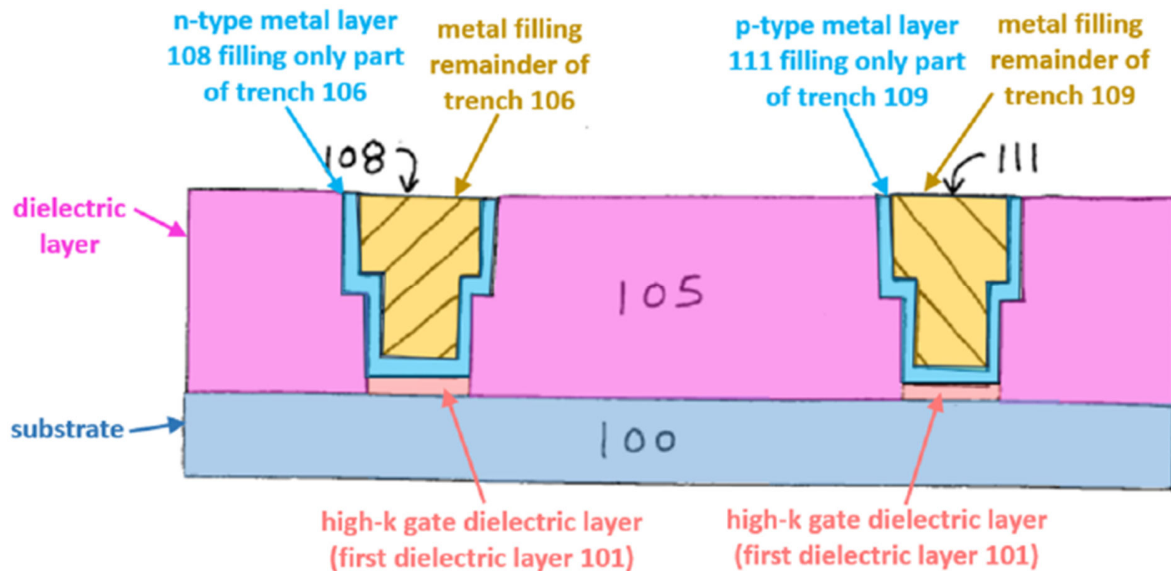
1. The Petition Combines Separate Embodiments In Brask Without Further Analysis

91. Brask does not disclose any single embodiment that contains each of the teachings that the Petition alleges discloses all elements of claim 1. Brask's main embodiment (as depicted in Brask's figures) clearly does not disclose all elements of claim 1. For example, Brask's gate structures have only one metal layer, rather than a work function metal layer and a second metal layer:



EX1012-Brask, Fig. 11.

92. Indeed, the Petition concedes this—after describing Brask’s main embodiment, the Petition clarifies that “[t]his IPR is notably based not on the embodiment illustrated above, but rather on an alternative embodiment that differs from the illustrated embodiment in two ways relative to the high-k dielectric and metal layer elements.” Pet., 35. First, the Petition points to an alternative embodiment in which “first dielectric layer 101 may comprise a high-k gate dielectric layer that is retained after sacrificial structure 104 and 114 are removed.” Pet., 35-36 (citing EX1012-Brask, 7:3-9). In Brask’s main embodiment, first dielectric layer 101 is removed and replaced by gate dielectric layer 107. EX1012-Brask, 4:19-33. Second, the Petition points to another alternative embodiment in which “n-type metal layer 108 may fill only part of trench 106, with the remainder of the trench being filled with a material that may be easily polished, e.g., tungsten, aluminum, titanium, or titanium nitride.” Pet., 36 (citing EX1012-Brask, 6:7-12). The Petition provides a figure purporting to illustrate a “Representative Embodiment” of Brask that comprises teachings from each of these three embodiments (Brask’s main embodiment and the two identified alternative embodiments):



Pet., 37.

93. I understand that anticipation is not proven by multiple, distinct teachings that the artisan might somehow combine to achieve the claimed invention. On the other hand, I also understand that a reference does not need to expressly spell out all limitations combined as in the claim if a POSITA would “at once envisage” the arrangement or combination. Here, neither the Petition nor Petitioner’s expert declaration provides any rationale for why a POSITA would at once envisage that these specific teachings from multiple distinct embodiments in Brask could be combined. Pet., 35-37; EX1003-Lee-Decl, ¶¶68-72.

2. Brask Fails To Disclose “A Work Function Metal Layer”

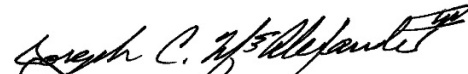
94. Brask additionally fails to disclose the claimed “work function metal layer.” As explained above in Section VI.C, the purpose of the work function metal layer is “to prevent the threshold voltage from increasing and therefore reducing the

resistance of the device.” EX1001, 1:27-31. Thus, the ’735 Patent’s claimed “work function metal layer” is a metal layer that serves to tune the threshold voltage value of the gate, while the second gate “metal layer” acts as the main gate conductor.

95. The Petition alleges that Brask’s n-type metal layer 108 and p-type metal layer 111 are work function metal layers. Pet., 76. The Petition’s sole basis for this allegation is that Brask discloses that “[n]-type metal layer 108 preferably serves as a metal NMOS gate electrode that has a workfunction that is between about 3.9 eV and about 4.2 eV” and that “[p]-type metal layer 111 may serve as a metal PMOS gate electrode with a workfunction that is between about 4.9 eV and about 4.2 eV.” Pet., 76 (citing EX1012-Brask, 5:49-6:12, 6:39-53). But this disclosure in Brask does not establish that that these layers “prevent the threshold voltage from increasing and therefore reducing the resistance of the device,” and the Petition does not assert or explain otherwise. Nor could it, because Brask’s “n-type metal layer 108” and “p-type metal layer 111” are not “work function metal layers” within the meaning ascribed by the ’735 Patent.

96. Thus, Brask does not disclose the claimed “work function metal layer.”

Dated: April 22, 2026


Joseph C. McAlexander III