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(54) **TUNING TENSILE STRAIN ON FINFET**

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(Continued)

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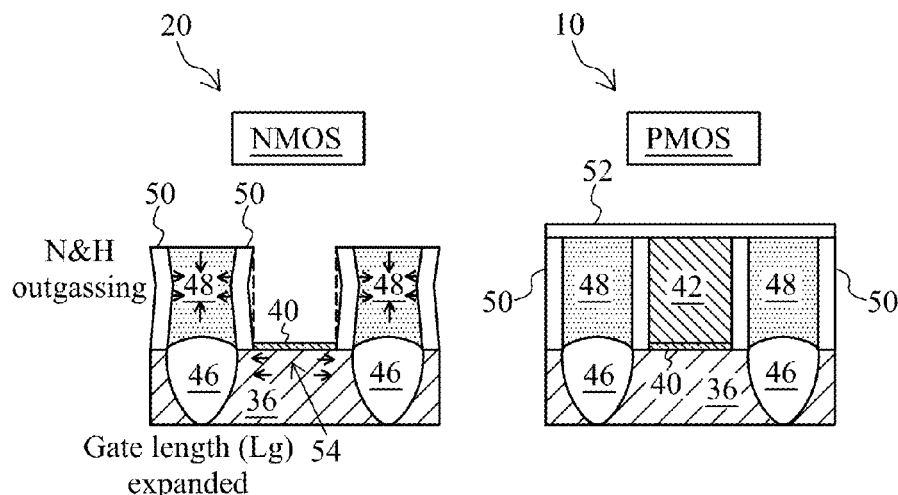
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(57) **ABSTRACT**

A fin field effect transistor (FinFET) having a tunable tensile strain and an embodiment method of tuning tensile strain in an integrated circuit are provided. The method includes forming a source/drain region on opposing sides of a gate region in a fin, forming spacers over the fin, the spacers adjacent to the source/drain regions, depositing a dielectric between the spacers; and performing an annealing process to contract the dielectric, the dielectric contraction deforming the spacers, the spacer deformation enlarging the gate region in the fin.

20 Claims, 11 Drawing Sheets



of application No. 13/901,399, filed on May 23, 2013,
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See application file for complete search history.

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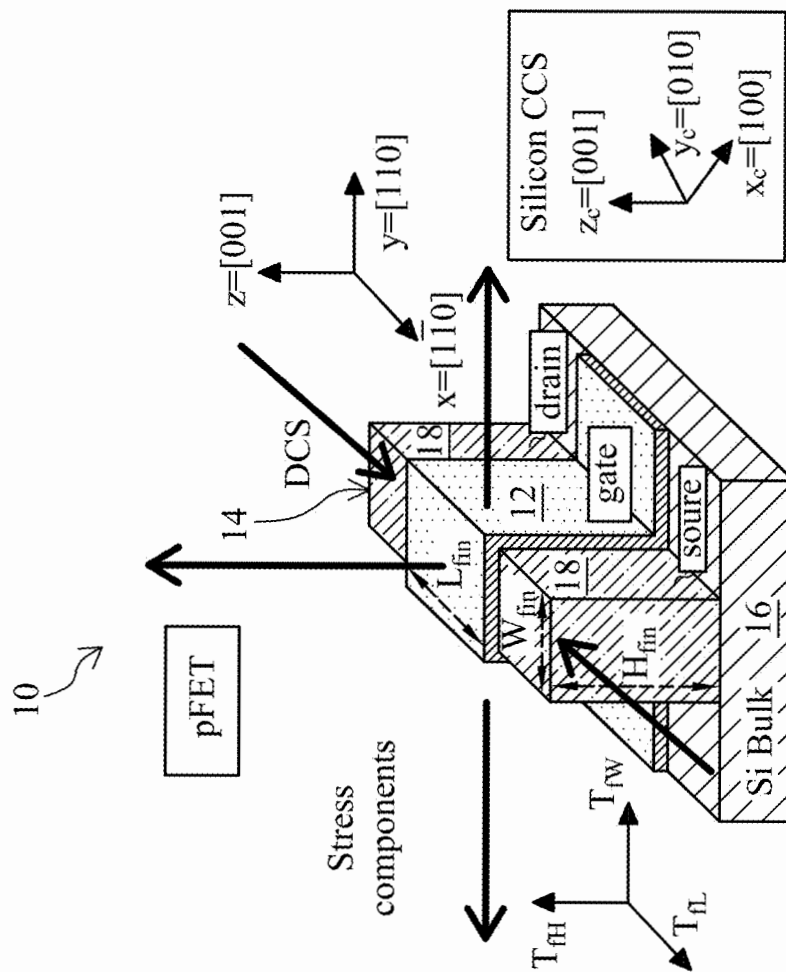


Fig. 1

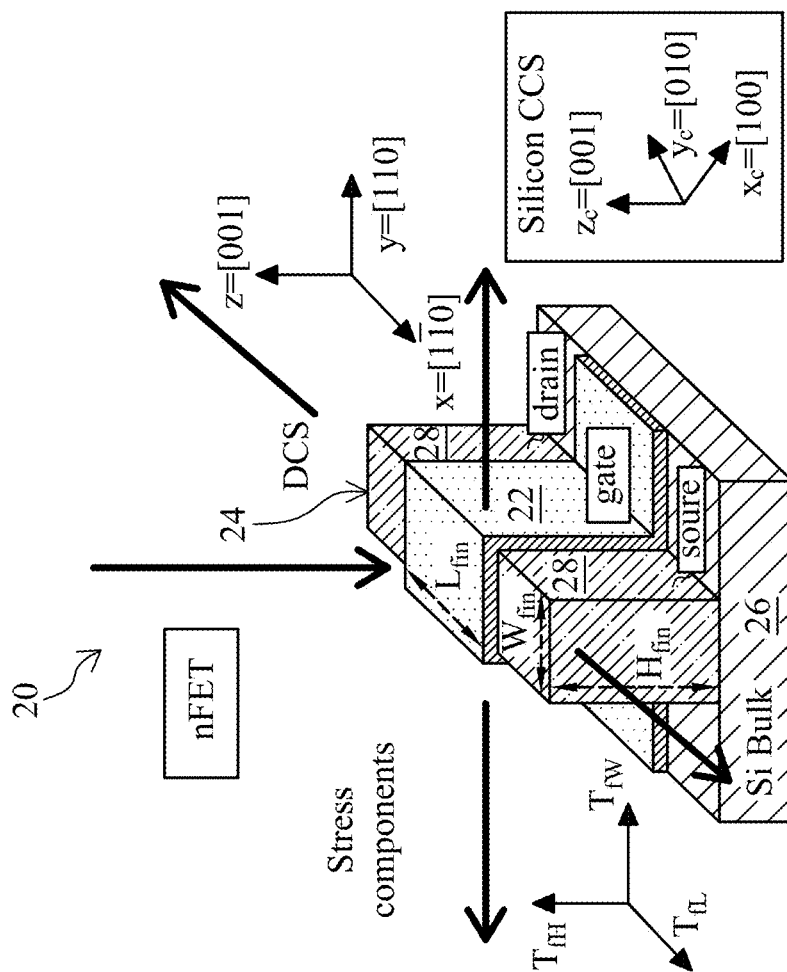


Fig. 2

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FinFET stress components $\begin{cases} T_{FH}: \text{fin-height} \\ T_{FW}: \text{fin-width} \\ T_{FL}: \text{source-drain} \end{cases}$

	Compressive			Tensile		
	T_{FL}	T_{FW}	T_{FH}	T_{FH}	T_{FW}	T_{FL}
Electron mobility	↘	↘	↗	↘	↗	↘
Hole mobility	↗	↗	=	↗	↘	↗

Table summarizing the impact of different stress components on the electron and hole $(110)/[\bar{1}\bar{1}0]$ FinFETs mobility

Fig. 3

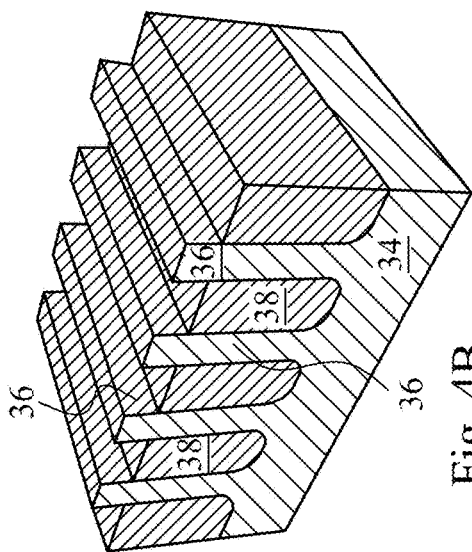


Fig. 4B

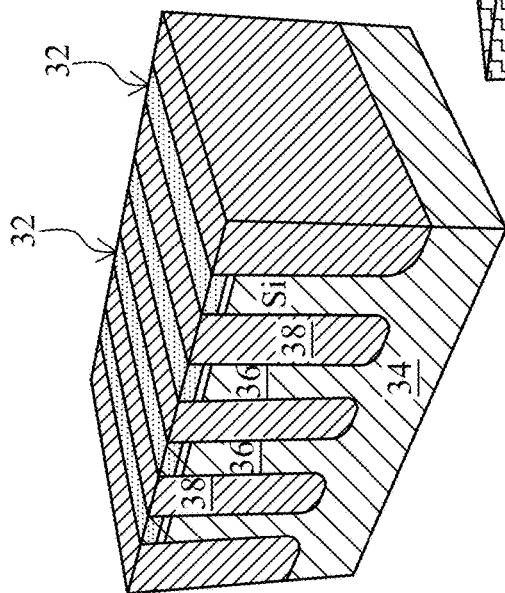


Fig. 4A

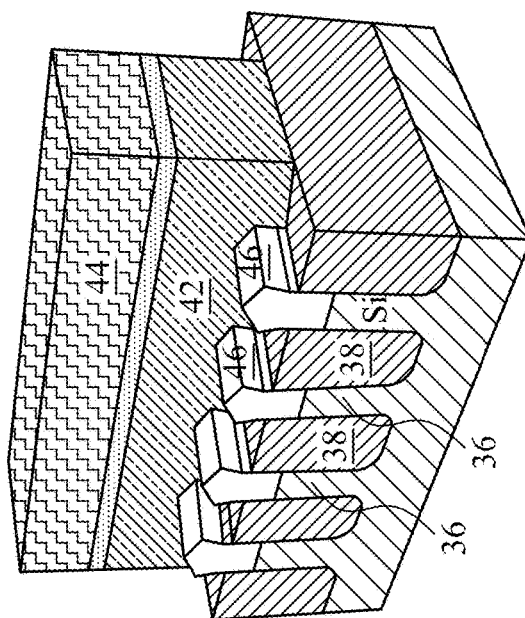


Fig. 5

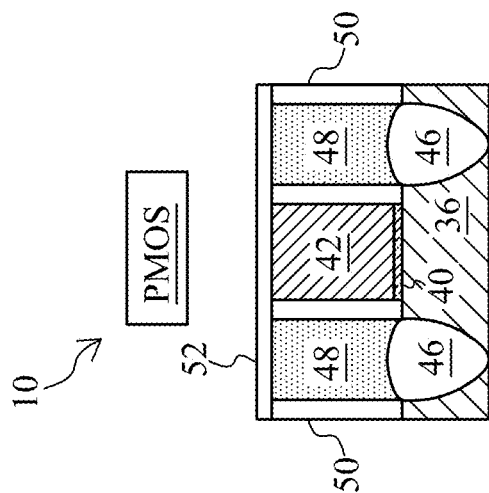


Fig. 6

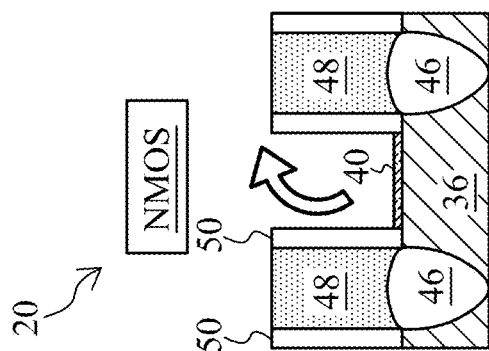


Fig. 7

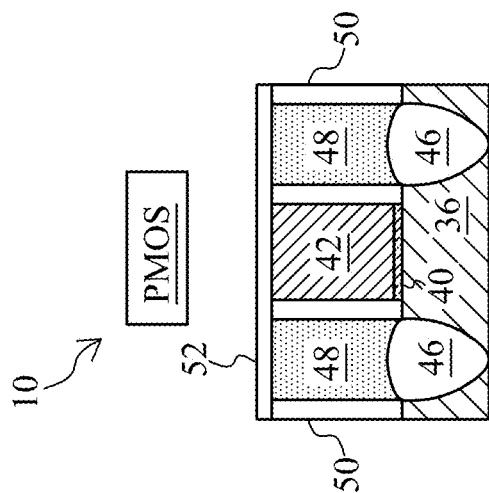


Fig. 8

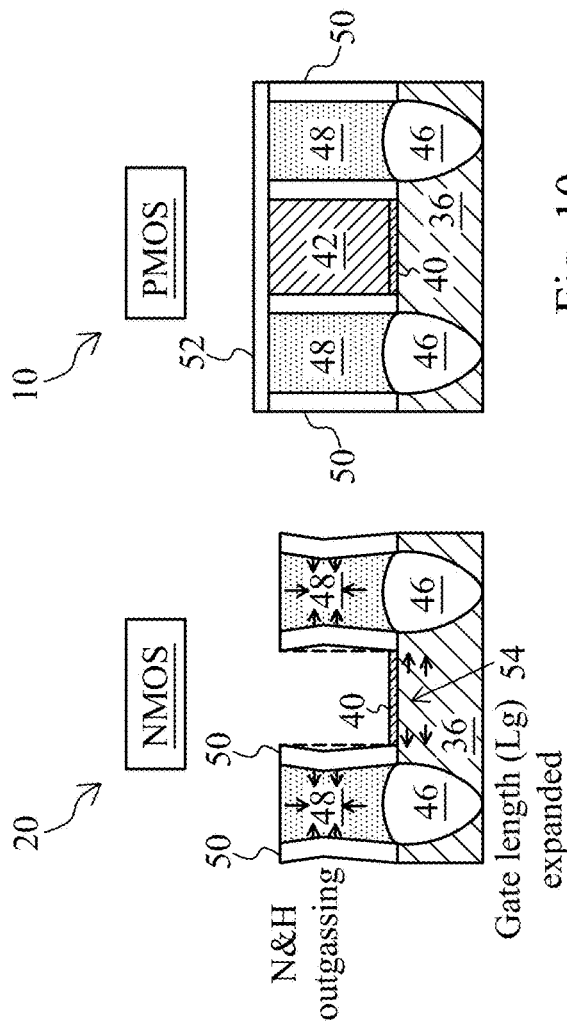


Fig. 9

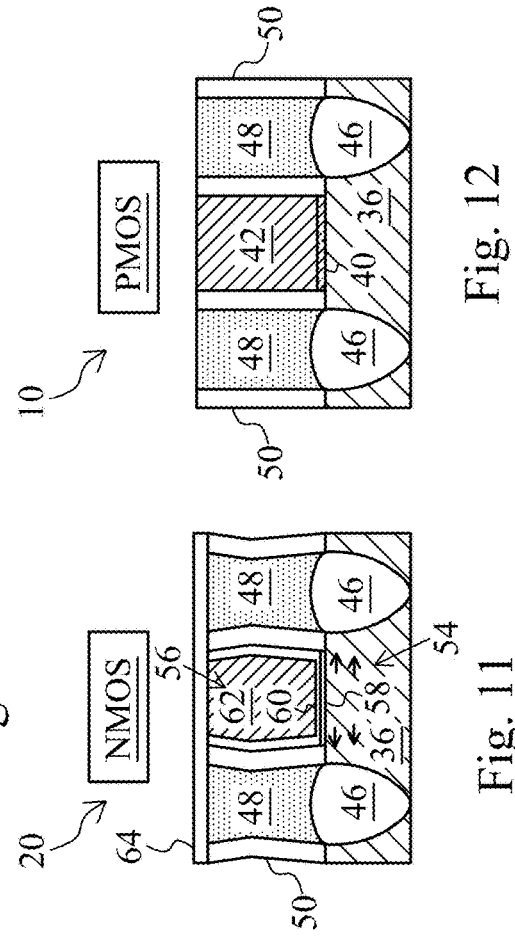


Fig. 10

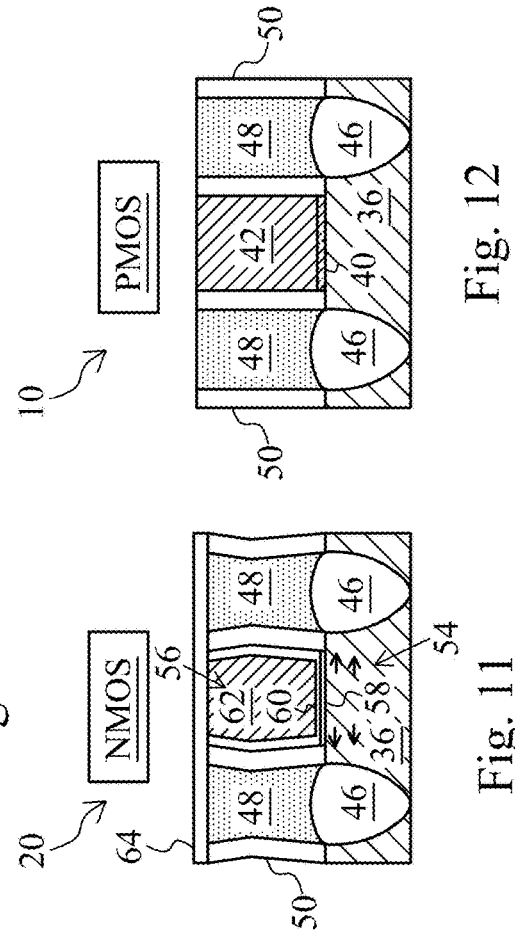


Fig. 11

Fig. 12

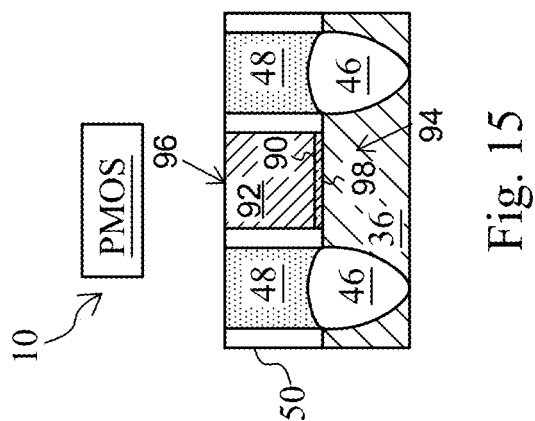


Fig. 13

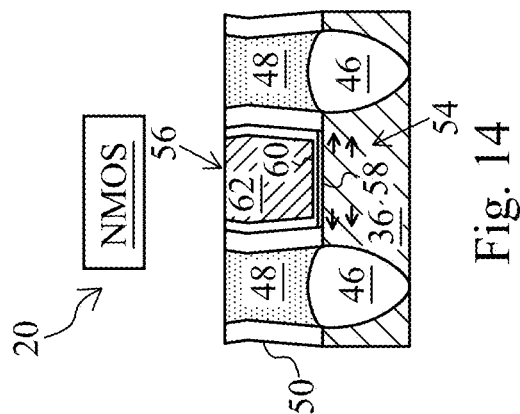


Fig. 14

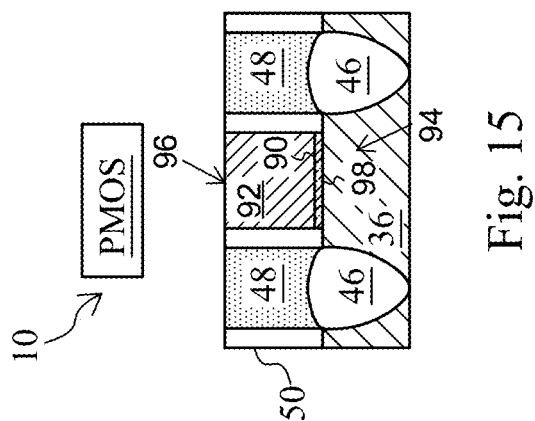


Fig. 15

66 

Lot ID	Ctrl-1	N stressor-1	Ctrl-2	N stressor-2
Process	No extra ANL	600C 2hr a/f PORM	No extra ANL	600C 1hr a/f PORM
Lg(nm)	30.4	34.3	31.9	33.6
Δ Lg(nm)	+3.9		+1.7	

Fig. 16

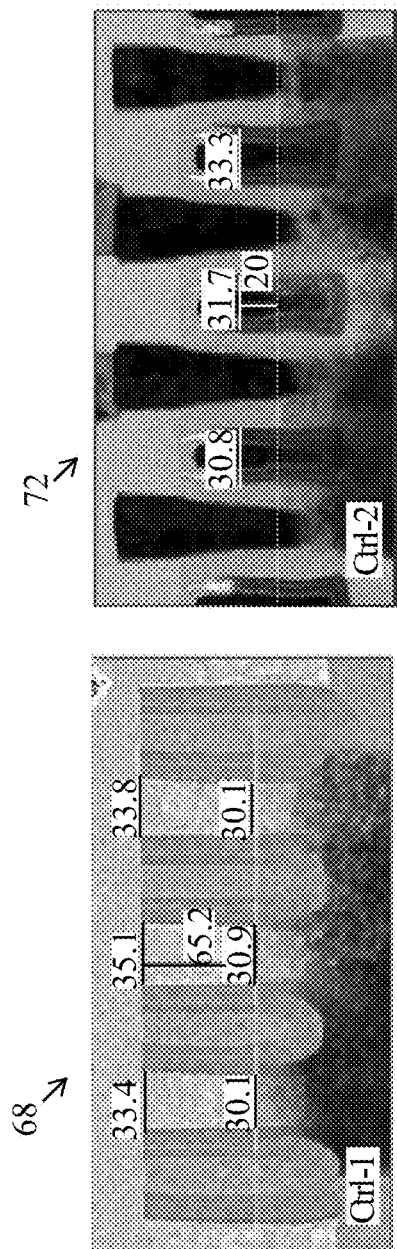


Fig. 17

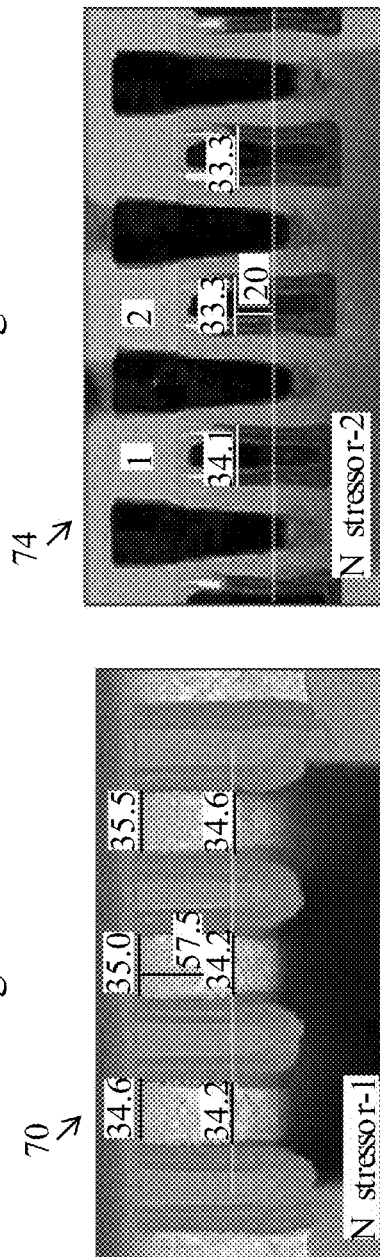


Fig. 19

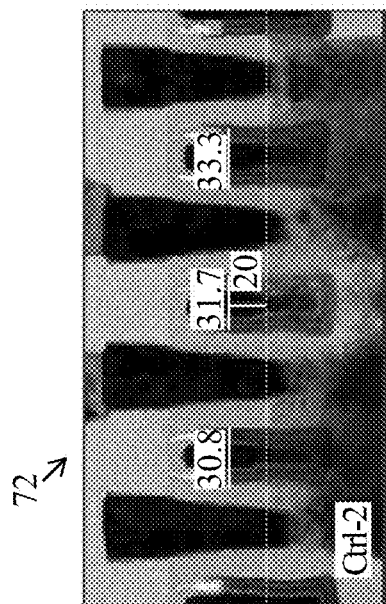


Fig. 18

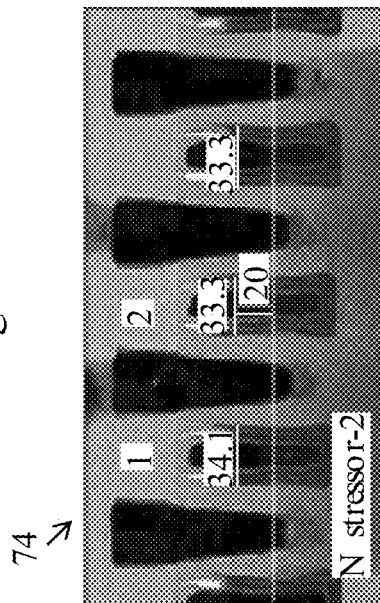


Fig. 20

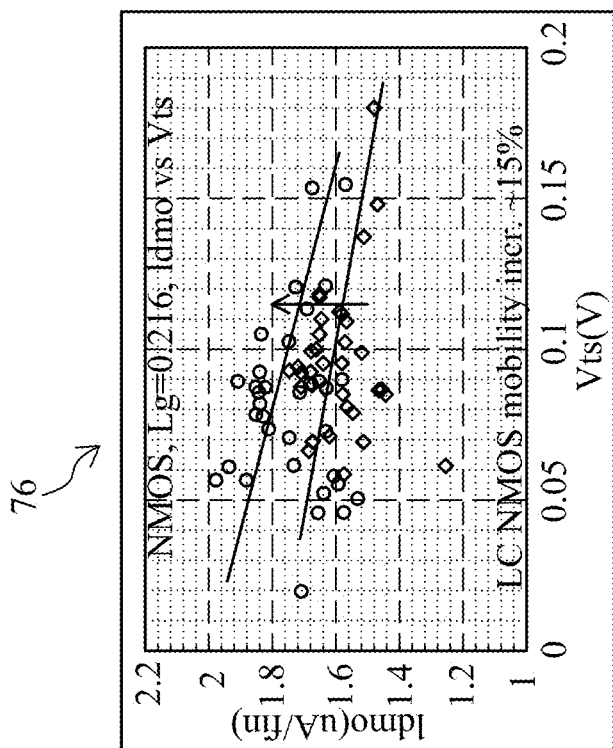


Fig. 21

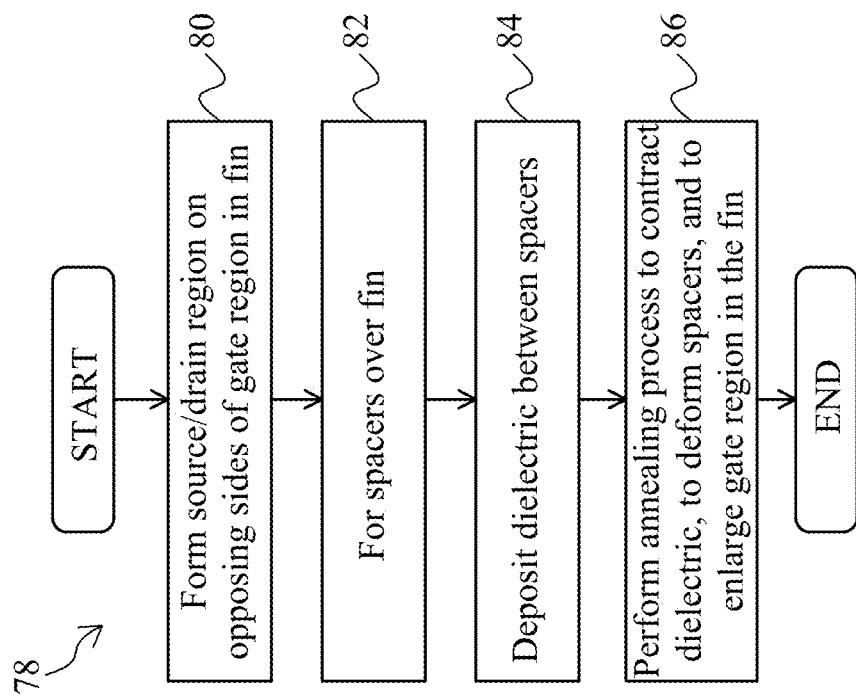


Fig. 22

TUNING TENSILE STRAIN ON FINFET

This application is a divisional of U.S. patent application Ser. No. 14/839,560, entitled "Tuning Tensile Stress on FinFET," filed on Aug. 28, 2015, which is a divisional of U.S. patent application Ser. No. 13/901,399, now U.S. Pat. No. 9,153,668, entitled "Tuning Tensile Stress on FinFET," filed on May 23, 2013, which applications are incorporated herein by reference in their entirety.

BACKGROUND

Semiconductor devices are used in a large number of electronic devices, such as computers, cell phones, and others. Semiconductor devices comprise integrated circuits that are formed on semiconductor wafers by depositing many types of thin films of material over the semiconductor wafers, and patterning the thin films of material to form the integrated circuits. Integrated circuits include field-effect transistors (FETs) such as metal oxide semiconductor (MOS) transistors.

One of the goals of the semiconductor industry is to continue shrinking the size and increasing the speed of individual FETs. To achieve these goals, fin FETs (FinFETs) or multiple gate transistors are used in sub 32 nm transistor nodes. FinFETs not only improve areal density, but also improve gate control of the channel.

In some cases, FinFETs have been constructed using a replacement gate process. During such process, the FinFET is initially provided with polysilicon gates, which are better able to withstand the more severe processing conditions of the immediately subsequent processing operations. Thereafter, in later stages of processing when processing conditions are less severe, the polysilicon gates are removed from the FinFET structures and replaced with permanent metal gates.

In recent years, attempts have been made to improve the performance or manipulate the characteristics of FinFETs with a stressor. Several methods of forming these stressors for FinFETs have been proposed or used in fabrication.

BRIEF DESCRIPTION OF THE DRAWINGS

For a more complete understanding of the present disclosure, and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawing, in which:

FIGS. 1-2 illustrate a p-type fin field-effect transistor (FinFET) and an n-type FinFET;

FIG. 3 is a table summarizing the impact of different stress components on the electron and hole (110/[110]) FinFETs mobility;

FIGS. 4A, 4B, and 5-15 collectively illustrate a method of forming an embodiment n-type FinFET 20 with tunable tensile strain relative to the p-type FinFET;

FIG. 16 is a chart illustrating how subjecting the dielectric in the n-type FinFET to the annealing process (i.e., the thermal process) affects gate length of the transistor;

FIGS. 17-20 illustrate the transistors used to generate the data in the chart of FIG. 16;

FIG. 21 illustrates the N-stressor split providing mobility increase for the n-type FinFET; and

FIG. 22 illustrates an embodiment method of tuning tensile strain in an integrated circuit (e.g., the n-type FinFET of FIG. 2).

Corresponding numerals and symbols in the different figures generally refer to corresponding parts unless other-

wise indicated. The figures are drawn to clearly illustrate the relevant aspects of the embodiments and are not necessarily drawn to scale.

DETAILED DESCRIPTION OF ILLUSTRATIVE EMBODIMENTS

The making and using of the present embodiments are discussed in detail below. It should be appreciated, however, that the present disclosure provides many applicable inventive concepts that can be embodied in a wide variety of specific contexts. The specific embodiments discussed are merely illustrative, and do not limit the scope of the disclosure.

The present disclosure will be described with respect to embodiments in a specific context, namely a FinFET. The disclosure may also be applied, however, to other integrated circuits, electronic structures, and the like.

Referring now to FIG. 1, a p-type FinFET 10 is illustrated. As shown, the p-type FinFET 10 (a.k.a., pFET or PMOS) includes a gate 12 disposed over a fin 14 projecting above a silicon (Si) bulk substrate 16 or silicon-on-insulator (SOI) substrate (not shown). In addition, a source/drain 18 are found at opposing ends of the fin 14 outside the gate 12. In real production, an effective stressor is produced in the p-type FinFET 10 by forming the source/drain 18 using silicon germanium (SiGe).

Referring now to FIG. 2, an n-type FinFET 20 is illustrated. As shown, the n-type FinFET 20 (a.k.a., nFET or NMOS) includes a gate 22 disposed over a fin 24 projecting above a silicon bulk substrate 26 or SOI substrate (not shown). In addition, a source/drain 28 are found at opposing ends of the fin 24 outside the gate 22. Unlike the p-type FinFET 10, an effective stressor is difficult to produce in the n-type FinFET 20 during real production.

Referring now to both FIGS. 1-2, the p-type FinFET 10 and the n-type FinFET 20 each define a fin height, H_{fin} , a fin width, W_{fin} , and a gate length, L_{fin} . Stress components for the fin height, T_{FH} , the fin width, T_{FW} , and the source-drain, T_{FL} , direction for the two transistors are shown in the device coordinate system (DCS). In addition, the silicon crystal coordinate system (CCS) for the two transistors is also depicted.

Referring now to FIG. 3, a table 30 summarizing the impact of different stress components on the electron and hole (110/[110]) FinFETs mobility is provided. As highlighted, the electron mobility increases and the hole mobility decreases when the tensile strain is increased in the source-drain, T_{FL} , direction. Therefore, an n-type FinFET 20 with a stressor configured to provide sufficient tensile strain in the source-drain, T_{FL} , direction would be beneficial.

Referring collectively to FIGS. 4A, 4B, and 5-15, a method of forming an embodiment n-type FinFET 20 with tunable tensile strain is illustrated relative to the p-type FinFET 10. Referring now to FIGS. 4A and 4B, the method generally begins with fin patterning. In an embodiment, both the fins 36 and the substrate 34 are formed from silicon. However, the fins 36 and substrate 34 may be formed from a variety of suitable semiconductor materials, such as Ge, SiGe, or III-V material.

After the fins 36 have been formed, an oxide deposition process is performed to generate the shallow trench isolation (STI) regions 38 on opposing sides of the fins 36. Thereafter, a chemical-mechanical polishing (CMP) process is performed to smooth the top surface of the device. Next, the hard mask 32 shown in FIG. 4 is removed. In an embodi-

3

ment, the hard mask 32 was formed from two layers, namely a nitride layer over an oxide layer.

After the hard mask 32 has been removed, a well implantation and an annealing step are performed. Thereafter, a dummy gate oxide 40 (i.e., IO OX) (see FIG. 7) is deposited. Once the dummy gate oxide 40 has been deposited, a polysilicon layer 42 is deposited and patterned using a hard mask 44 as shown in FIG. 5. Next, a lightly doped drain (LDD) implantation process and an annealing process are performed.

Still referring to FIG. 5, after the LDD implantation and annealing steps, source/drain recessing is performed to provide a place to form the source/drain regions 46. With recesses having been generated, the source/drain regions 46 shown in FIG. 5 are epitaxially grown. As shown in FIG. 7, the source/drain regions 46 are disposed on opposing sides of the dummy gate oxide 40.

Next, as shown in FIG. 6, a dielectric 48 is formed over the source/drain regions 46 and the adjacent STI regions 38. In an embodiment, the dielectric 48 is an interlayer dielectric (ILD). In an embodiment, the dielectric 48 is formed using a flowable chemical vapor deposition (FCVD) process.

As shown in FIG. 7, spacers 50 are disposed on opposing sides of the dielectric 48. In an embodiment, the spacers 50 are formed after the polysilicon layer 42 has been formed. After the dielectric 48 has been formed, a CMP process is performed to smooth a top surface of the device.

Next, referring collectively to FIGS. 6-8, a hard mask 52 is formed over both the embodiment n-type FinFET 20 (i.e., NMOS) and the neighboring p-type FinFET 10 (i.e., PMOS), which are depicted in an intermediate stage. Thereafter, a portion of the hard mask 52 is selectively removed from the n-type FinFET 20 using a photo mask. Next, the polysilicon layer 42 (see FIG. 5) disposed over the dummy gate oxide 40 and between two of the spacers 50 in the n-type FinFET 20 is removed as represented by the arrow in FIG. 7.

After the polysilicon layer 42 has been removed, an extra annealing process is performed. In an embodiment, the extra annealing process is performed at a temperature of between about 500° C. to about 650° C., for a time of between about 60 minutes to about 120 minutes, and/or at a pressure of about 1 atmosphere. In other embodiments, other temperatures, times, and pressures may be employed in order to achieve desired results.

In an embodiment, the annealing process causes elements such as, for example, nitrogen and hydrogen, to be off gassed from dielectric 48 as shown in FIG. 9. When the elements are off gassed, the dielectric 48 in FIG. 9 contracts or shrinks (as represented by the arrows in FIG. 9). In an embodiment, the annealing process shrinks the dielectric 48 between about 15% to about 18% relative to a size of the dielectric 48 prior to the annealing process. In an embodiment, the annealing process reduces a height and a width of the dielectric 48 as shown in FIG. 9 relative to the dielectric 48 in the p-type FinFET 10 in FIG. 10, which is not subjected to the extra annealing process.

The contraction or shrinking of the dielectric 48 bends or otherwise deforms the spacers 50 in the n-type FinFET 20 as shown in FIG. 9. Indeed, the spacers 50 in FIG. 9 are bent or curved inwardly relative to the straight or unbent spacers 50 in the p-type FinFET 10 in FIG. 10. In an embodiment, a contour of the contracted dielectric 48 is equivalent to a contour of the spacers 50 in FIG. 9. In an embodiment, the contracted dielectric 48 is generally vertically aligned with the source/drain regions 46.

4

Still referring to FIG. 9, the bending or deformation of the spacers 50 in the n-type FinFET 20 laterally expands the gate region 54 of the fin 36. Indeed, the spacers 50 are drawn inwardly toward the source/drain region 46 and each other by the shrinking dielectric 48, which provides additional surface area where a gate structure may be subsequently formed over the fin 36. In other words, an amount of deformation of the spacers 50 is due to the contracted dielectric 48 and contributes to a length of the enlarged gate region 54 in the fin 36. Notably, the enlarged gate region 54 allows for a longer channel in the n-type FinFET 20.

In an embodiment, a middle portion of each of the spacers 50 in FIG. 9 is deformed more than top and bottom portions of the spacers 50. In addition, in an embodiment the spacers 50 in FIG. 9 are laterally adjacent to the enlarged gate region 54 and the source/drain regions 46. Moreover, in an embodiment the spacers 50 in FIG. 9 are on opposing sides of the contracted dielectric 48.

After the extra annealing process has been performed and the spacers 50 of the n-type FET 20 bent or deformed as shown in FIG. 9, the dummy gate oxide 40 in FIG. 9 is removed and the gate electrode structure 56 of FIGS. 11, 13-14 is constructed. In an embodiment, the gate electrode structure 56 includes an interfacial oxide 58, a high-k value dielectric 60, and a metal gate 62.

After the gate electrode structure 56 has been formed in the n-type FinFET 20 as shown in FIG. 11, a CMP process is performed to smooth the top surface of the transistor. Thereafter, a hard mask 64 is formed over both the embodiment n-type FinFET 20 and the neighboring p-type FinFET 10 and then selectively removed from the p-type FinFET 10 using a photo mask as shown in FIGS. 11-12. Next, the polysilicon layer 42 disposed over the dummy gate oxide 40 and between two of the spacers 50 in the p-type FinFET 10 of FIG. 12 is removed.

Thereafter, the dummy gate oxide 40 in FIG. 12 is removed and the gate electrode structure 96 of FIG. 15 is generated. In an embodiment, the gate electrode structure 96 includes an interfacial oxide 98, a high-k value dielectric 90, and a metal gate 92 as shown in FIG. 15. After the gate electrode structure 96 has been formed in the p-type FinFET 10 as shown in FIG. 15, a CMP process is performed to smooth the top surface of the transistor. In an embodiment, the n-type FinFET 20 and the neighboring p-type FinFET 10 are disposed on the same silicon substrate 36 or wafer.

Referring to FIGS. 14-15, it should be recognized that the horizontal or lateral length of the gate region 54 in the n-type FinFET 20 is greater than the length of the gate region 94 in the p-type FinFET 10, which has not been stretched by shrinking dielectric 48 and inwardly drawn spacers 50. In addition, the height of the gate in the n-type FinFET 20 is less than the height of the gate in the p-type FinFET 10. In an embodiment, the dielectric 48 in the n-type FinFET 20 is formed from a different material than the dielectric 48 in the p-type FinFET 10.

Referring now to FIG. 16, a chart 66 illustrating how subjecting the dielectric 48 in the n-type FinFET 20 to the annealing process (i.e., the thermal process) affects gate length of the transistor.

The n-type FinFETs 70, 74 in FIGS. 19-20 were subjected to an annealing process to shrink the dielectric and bend the spacers. The transistor in FIG. 19 was subjected to the extra annealing process at about 600° C. for a period of about 2 hours. The transistor in FIG. 20 was subjected to an annealing process at about 600° C. for a period of about 1 hour. Thereafter, the gate length of the transistors in FIGS. 19-20 was measured. The average gate length (L_g) in the transistor

5

in FIG. 19 was measured as 34.3 nm and the average gate length of the transistor in FIG. 20 was measured as 33.6 nm.

Unlike the transistors in FIGS. 19-20, the n-type FinFETs 68, 72 in FIGS. 17-18 were not subjected to the extra annealing process used to shrink the dielectric and bend the spacers. The average gate length (L_g) in the transistor in FIG. 17 was measured as 30.4 nm and the average gate length of the transistor in FIG. 18 was measured as 31.9 nm. Therefore, as shown in the chart 66 in FIG. 16, the average gate length in the transistor of FIG. 19 increased by about 3.9 nm relative to the average gate length in the transistor of FIG. 17. Likewise, the average gate length in the transistor of FIG. 20 increased by about 1.7 nm relative to the average gate length in the transistor of FIG. 18.

Referring now to FIG. 21, a chart 76 indicates that the N-stressor split showed mobility increase for the n-type FinFET 20. In FIG. 21, the circle data points correspond to the transistor with the extra annealing process described above while the diamond data points correspond to the transistor without the benefit of the extra annealing process. When the mobility index (I_{dmo}) is plotted relative to the voltage threshold (V_{ts}), the long channel (LC) NMOS mobility increased about 15%.

In FIG. 22, an embodiment method 78 of tuning tensile strain in an integrated circuit (e.g., the n-type FinFET 20) is illustrated. In block 80, a source/drain region is formed on opposing sides of a gate region in a fin. In block 82, spacers are formed over the fin. The spacers are generally adjacent to the source/drain regions. In block 84, a dielectric is deposited between the spacers. In block 86, an annealing process is performed to contract the dielectric. The dielectric contraction deforms the spacers, which causes the gate region in the fin to enlarge or expand.

An embodiment method of method of tuning tensile strain in an integrated circuit includes forming a source/drain region on opposing sides of a gate region in a fin, forming spacers over the fin, the spacers adjacent to the source/drain regions, depositing a dielectric between the spacers; and performing an annealing process to contract the dielectric, the dielectric contraction deforming the spacers, the spacer deformation enlarging the gate region in the fin.

An embodiment fin field effect transistor (FinFET) having a tunable tensile strain includes a source/drain region on opposing sides of an enlarged gate region in a fin, a contracted dielectric disposed over the source/drain regions, and spacers disposed over the fin, an amount of deformation of the spacers due to the contracted dielectric and contributing to a length of the enlarged gate region in the fin.

An embodiment integrated circuit having a tunable tensile strain includes a p-type metal-oxide-semiconductor (PMOS) device with a first gate region, and an n-type metal-oxide-semiconductor (NMOS) device adjacent the PMOS device, the NMOS device including deformed spacers on opposing sides of a contracted dielectric, the deformed spacers adjacent a second gate region, a length of the second gate region greater than a length of the first gate region.

While the disclosure provides illustrative embodiments, this description is not intended to be construed in a limiting sense. Various modifications and combinations of the illustrative embodiments, as well as other embodiments, will be apparent to persons skilled in the art upon reference to the description. It is therefore intended that the appended claims encompass any such modifications or embodiments.

What is claimed is:

1. A semiconductor device comprising:
 - a first device comprising:
 - a first fin;

6

first source/drain regions in the first fin on opposing sides of a first channel region;

a first gate electrode overlying the first channel region; and

a first dielectric layer on opposing sides of the first gate electrode, the first gate electrode having linear sidewalls; and

a second device comprising:

a second fin;

second source/drain regions in the second fin on opposing sides of a second channel region;

a second gate electrode overlying the second channel region; and

a second dielectric layer on opposing sides of the second gate electrode, the second dielectric layer being a contracted dielectric, the second gate electrode having convex sidewalls projecting toward concave sidewalls of the second dielectric layer.

2. The semiconductor device of claim 1, wherein the first device is a p-type metal-oxide-semiconductor (PMOS) device, and the second device comprises an n-type metal-oxide-semiconductor (NMOS) device.

3. The semiconductor device of claim 1, further comprising a second spacer interposed between the second gate electrode and the second dielectric layer.

4. The semiconductor device of claim 3, further comprising a first spacer interposed between the first gate electrode and the first dielectric layer.

5. The semiconductor device of claim 1, wherein the second device has a longer channel than the first device.

6. The semiconductor device of claim 1, wherein the first dielectric layer comprises a different material than the second dielectric layer.

7. The semiconductor device of claim 1, wherein the second dielectric layer is more dense than the first dielectric layer.

8. A semiconductor device comprising:

a first fin extending from a substrate;

first source/drain regions in the first fin on opposing sides of a first channel region;

a first gate over the first channel region;

a contracted dielectric disposed over the first source/drain regions;

first spacers interposed between the first gate and the contracted dielectric, the first spacers having a concave surface extending toward the contracted dielectric;

a second fin extending from the substrate;

second source/drain regions in the second fin on opposing sides of a second channel region;

a second gate over the second channel region;

a dielectric disposed over the second source/drain regions; and

second spacers interposed between the second gate and the dielectric, the second spacers having a linear surface facing the dielectric.

9. The semiconductor device of claim 8, wherein a contour of sidewalls of the contracted dielectric is equivalent to a contour of the first spacers.

10. The semiconductor device of claim 8, wherein the contracted dielectric has been reduced in size about 15% to about 18% relative to an original size of the contracted dielectric.

11. The semiconductor device of claim 8, wherein the contracted dielectric is vertically aligned with the first source/drain regions.

7

12. The semiconductor device of claim **8**, further comprising an interfacial oxide and a high-k dielectric interposed between the first fin and the first gate.

13. The semiconductor device of claim **8**, wherein the first gate comprises a metal gate electrode.

14. A semiconductor device comprising:

a first device comprising:

a first fin;

first source/drain regions in the first fin on opposing sides of a first channel region;

a first gate electrode overlying the first channel region; and

a first dielectric layer on opposing sides of the first gate electrode, the first dielectric layer being a contracted dielectric layer, the first gate electrode having convex sidewalls projecting toward concave sidewalls of the first dielectric layer;

a second device comprising:

a second fin;

second source/drain regions in the second fin on opposing sides of a second channel region;

a second gate electrode overlying the second channel region, sidewalls of the second gate electrode having a different shape than sidewalls of the first gate electrode; and

8

a second dielectric layer on opposing sides of the second gate electrode, the second dielectric layer being uncontracted; and

an interlayer dielectric layer over the first fin and the second fin, the interlayer dielectric layer extending along sidewalls of the first dielectric layer and the second dielectric layer.

15. The semiconductor device of claim **14**, wherein the second gate electrode has linear sidewalls.

16. The semiconductor device of claim **14**, wherein the first device is an NMOS device.

17. The semiconductor device of claim **14**, further comprising spacers interposed between the first gate electrode and the first dielectric layer, the spacers having curved sidewalls facing the first gate electrode.

18. The semiconductor device of claim **14**, wherein the first dielectric layer and the second dielectric layer are different materials.

19. The semiconductor device of claim **14**, wherein the first gate electrode has a first height, the second gate electrode has a second height, the first height being different than the second height.

20. The semiconductor device of claim **14**, wherein the first dielectric layer is denser than the second dielectric layer.

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