

[0021] 4) 在非晶硅层上局部覆盖硼掺杂剂

可选地(第一种方法),是通过丝网印刷的方法在非晶硅层上印刷一定图案的硼浆,并烘干硼浆,烘干工艺可采用平板式加热或链式的快速热处理炉(以下简称“快速热处理炉”),烘干温度一般在100-500°C(优选:100-200°C),烘干时间1-10 min(优选:1-2 min),氮气气氛;或者采用打印(比如inkjet printing or aerosol jet printing)的方法在非晶硅层上印硼墨水,并烘干硼墨水,烘干工艺与上述的硼浆烘干类似。

[0022] 可选地(第二种方法),也可以采用选择性的硼离子注入在非晶硅薄膜来局部覆盖硼掺杂剂,在使用选择性离子注入技术时,通过掩膜版的配合来实现特定区域的掺杂剂注入。

[0023] 局部覆盖硼掺杂剂的图案(也即最终所形成的空穴局部钝化接触结构中的局部硼掺杂多晶硅区域的图案)可以设计成等间距栅线状分布(也即H pattern),也可以设计成点阵分布,并不局限于此。由于考虑到所述空穴局部钝化接触结构主要应用于电池正面用以钝化金属电极区域,同时本步所述的局部覆盖硼掺杂剂的图案需要和后续金属化电极的图案要相互对应,因此这里需兼顾考虑金属电极图案设计中遮光率和串联电阻两个因素,所以在实际应用中,更为典型的是采用栅线状分布的图案设计。

[0024] 在本步完成后如图2-a所示。

[0025] 5) 通过退火完成从非晶硅到多晶硅的晶化,并且在退火中,上述步骤4)中所覆盖的局部硼掺杂剂也得以激活并在多晶硅薄膜内进行再分布。退火可以采用高温退火(炉管或快速热处理炉)或激光退火(只针对局部覆盖硼掺杂剂的非晶硅薄膜区域),退火工艺参数需要兼顾非晶硅到多晶硅的充分晶化,以及局部硼掺杂剂的充分激活和再分布。一般地,通过炉管或快速热处理炉的退火温度是750-1100°C,时间是20-100 min,气氛是氮气。需要注意的是,采用炉管或快速热处理炉的高温退火,由前述步骤3)在样品上沉积的整个面的非晶硅都会晶化成多晶硅。另一方面,如果采用激光退火,由于激光“冷加工”的局部热处理特性,只会将局部覆盖硼掺杂剂区域的多晶硅晶化为非晶硅,而其他无硼掺杂剂覆盖的区域非晶硅则不会被晶化,在激光退火中也完成了局部硼掺杂剂的充分激活以及硼掺杂剂在多晶硅薄膜内再分布。可选地,激光退火工艺参数是,激光波长范围是100-1100 nm,例如,355 nm、532 nm或1064 nm,激光功率可以在几瓦到几千兆瓦范围,脉冲宽度一般采用纳秒级,但也不局限于此。需要强调的是,本步所述的炉管或快速热处理的高温退火以及激光退火,对步骤3)所沉积的非晶硅不同区域(有或无局部硼掺杂剂)的影响,对应于后续的化学刻蚀(步骤6)工艺会略有不同,这点会在步骤6)中给出。

[0026] 经过本步所述的退火后,局部覆盖有硼掺杂剂的多晶硅薄膜的硼掺杂表面浓度要不低于 $7 \times 10^{19} \text{ cm}^{-3}$,以便能有效地阻挡碱溶液的刻蚀。在具体应用于电池时,局部掺硼多晶硅薄膜在满足不低于 $7 \times 10^{19} \text{ cm}^{-3}$ 的表面硼掺杂浓度的基础上,为能更好地实现掺硼多晶硅层的场钝化作用,其表面硼掺杂浓度可以更优选地不低于 $1 \times 10^{20} \text{ cm}^{-3}$,方块电阻为20-80 $\Omega/\square$ (优选:30-50 $\Omega/\square$)。

[0027] 本步完成后,如图2-b所示。

[0028] 6) 通过碱溶液的化学刻蚀来完成对局部硼掺杂之外区域的多晶硅层或非晶硅层的刻蚀,具体地,基于步骤5)中采用是炉管(快速热处理炉)退火或是激光退火,分述如下:

6-1) 如果步骤5)中采用的是炉管或快速热处理炉来退火,在样品上形成的是整面均匀

的多晶硅层以及局部硼掺杂。在这种情况下,可以通过一定温度、浓度的碱溶液来刻蚀样品。由于在有局部硼掺杂的多晶硅薄膜区域的表面硼掺杂浓度不低于 $9 \times 10^{17} \text{ cm}^{-3}$,这些区域可以有效地阻挡碱溶液的化学刻蚀,从而使该区域的掺硼多晶硅薄膜在化学刻蚀后会完全保留。另一方面,无硼掺杂的多晶硅薄膜区域则被本步所述的碱溶液完全刻蚀掉。这里,碱溶液可以是NaOH或KOH,也不局限于此。碱溶液的温度、浓度和刻蚀时间等参数范围根据多晶硅层的厚度进行选择。一般地,NaOH或KOH的质量浓度是1-30%(优选:2-5%),温度是10-95°C(优选:40-80°C),刻蚀时间是4-40 min(优选:5-10 min)。

[0029] 6-2)如果步骤5)中采用的是激光退火,则只有在局部覆盖硼掺杂剂的非晶硅会被晶化为多晶硅,其他无硼掺杂剂覆盖区域的非晶硅薄膜则不会被晶化。在这种情况下,本步中需要化学刻蚀的就是无局部硼掺杂的非晶硅薄膜。由于非晶硅相比于多晶硅更容易被碱溶液刻蚀,因此相应的碱溶液刻蚀工艺条件会与6-1)中略有不同,其工艺窗口会更加灵活。另一方面,同样地,由于有局部硼掺杂的多晶硅薄膜区域的表面硼掺杂浓度不低于 $9 \times 10^{17} \text{ cm}^{-3}$,这些区域可以有效地阻挡碱溶液的化学刻蚀,从而得以完全保留。这里,碱溶液可以是NaOH或KOH,也不局限于此。碱溶液的温度、浓度和刻蚀时间等参数范围也要根据非晶硅厚度进行选择。一般地,NaOH或KOH的质量浓度是0.5-20%(优选:0.5-5%),温度是10-95°C(优选:20-80°C),刻蚀时间是2-20 min(优选:2-7 min)。

[0030] 需要说明的是,如果在步骤4)中采用的是丝网印刷硼浆或打印硼墨水来局部覆盖硼掺杂剂,并且在步骤5)中采用的是炉管或快速热处理炉来退火,那么在样品表面,被烘干后的硼浆或硼墨水中的硼掺杂剂可能会有少量的会在高温下挥发到热处理炉的气氛中。这样一来,在高温退火中,这些挥发的硼掺杂剂会扩散进入到原本不需要硼掺杂的多晶硅薄膜区域(也即非金属电极区域),这并不是所希望的。但是,这部分由于高温挥发而导致掺杂到非金属电极区域的硼的表面浓度并不会很高,一般会低于 $1 \times 10^{18} \text{ cm}^{-3}$,在该硼表面浓度下的多晶硅或非晶硅层阻挡碱溶液刻蚀的能力是远远不够的。因此在这种情况下,本步的碱溶液化学刻蚀可以顺利地刻蚀掉这些区域的多晶硅层或非晶硅层。

[0031] 此外还需要注意一点,本步需要实现的是对所述区域的多晶硅(或非晶硅)层完成纵向刻蚀,但在实际中也同步会发生横向刻蚀。考虑到在具体应用于电池时,一般地,电池正面的局部硼掺杂多晶硅的图案(这里以栅线状图案为例)的每根栅线的线宽一般在20-200 μm ,而在纵向上需要刻蚀的多晶硅(非晶硅)层厚度最多也就在200-300 nm范围。因此相应地,横向刻蚀宽度最多也就在200-300 nm范围内,即使考虑到实际中的工艺窗口一般也不会超过1-2 μm 。因此这种横向刻蚀对最终所需要形成的空穴局部钝化接触结构影响并不大,可以忽略。

[0032] 本步完成后,如图2-c所示。

[0033] 7)最后对局部掺硼多晶硅薄膜区域进行金属化,金属化材料一般选用银,具体制备方法可以采用丝网印刷、电镀或PVD等技术并结合快速热处理退火工艺,也不局限于此。通过对准式的金属化技术,金属化电极图案和局部掺硼多晶硅层的图案要相互对应。一般地,金属电极区域的面积要小于或等于局部掺硼多晶硅层的图案面积(最优选是两个图案完全重叠)。本步完成后如图2-d所示。

[0034] 至此,形成了本发明所给出的空穴局部钝化接触结构(图2-d)。

[0035] 基于实施例1中给出的实现空穴局部钝化接触的制备方法,下面的实施例2又继续

将这种实现空穴局部钝化接触的制备方法应用于具体的晶体硅太阳能电池,下面给出这种具有局部空穴钝化接触结构的太阳能电池的结构特征描述以及相应的电池制备方法。

[0036] 概况地说,这种电池结构的主要特征是将上述空穴局部钝化接触结构应用于电池正面,用以钝化电池正面的金属电极区域,而电池背面结构设计则可以兼容目前绝大多数晶体硅太阳能电池的背面结构设计。基于此,本发明所给出的电池结构可分为两类:第1类电池结构是电池两个面都采用钝化接触结构,也即正面采用空穴局部钝接触化,背面采用全面积的电子钝化接触,以及相应的正背面金属化(如图3所示);第2类电池结构是电池正面采用空穴局部钝化接触,背面采用常规的n型掺杂结和钝化膜,以及相应的正背面金属化(如图4所示)。相应地,电池制备方法则结合了前述给出的制备空穴局部钝化接触结构的方法。下面结合具体电池结构的特征描述,具体给出电池制备方法。

[0037] 首先,在衬底材料的选择上,所述的晶体硅太阳能电池可以选用单晶n型或p型硅片,也可以选用多晶或类单晶硅片;厚度是100-300 μm ,电阻率是0.1-10 $\Omega \cdot \text{cm}$,更优选地,选用单晶n型硅片或p型硅片,厚度130-170 μm ,电阻率0.5-3 $\Omega \cdot \text{cm}$ 。

[0038] 电池正面具有绒面;电池正面的非金属电极区域需要有p型掺杂结,而金属电极区域则采用所述的空穴局部钝化接触结构;电池正面还需要有减反射膜,该减反射膜兼起到钝化非金属电极区域p型掺杂结的作用。由于前述已经详细给出了空穴局部钝化接触结构的制备方法,此处不再赘述;下面会在此基础上,给出电池正面结构中其他几项特征要素的制备方法。

[0039] ①. 电池正面的绒面

电池正面需要具有绒面,比如随机金字塔绒面结构,也可以是倒金字塔结构,或V型槽结构,也不局限于此。因为电池正面的空穴局部钝化接触结构只需要在金属电极区域(也即局部掺硼区域)形成多晶硅层,所以非金属电极区域的多晶硅层(或是非晶硅层,对应于在激光退火方法)需要通过碱溶液刻蚀反应来刻蚀掉。这样一来,所述该碱溶液同样有条件对多晶硅(或非晶硅)层下方的硅衬底进行化学刻蚀形成结构化绒面结构。因此在实际电池制备中,就可以利用这步碱溶液的化学刻蚀来完成电池正面的绒面结构制备。

[0040] 这里可以分为两种情况,下面以单晶硅衬底为例对两种情况进行分别说明。第一种情况是,用来刻蚀非金属电极区域的多晶硅(或非晶硅)层的碱溶液刻蚀工艺参数条件,刚好也适合用于在单晶硅衬底上进行制绒,那么就可以利用所述该碱溶液,在化学刻蚀掉非金属电极区域的多晶硅(或非晶硅)层之后,随即进行碱制绒得到随机金字塔绒面。第二种情况是,用来刻蚀非金属电极区域的多晶硅(或非晶硅)层的碱溶液刻蚀工艺参数条件,并不适合用于在单晶硅衬底上进行制绒,那么在完成非金属电极区域的多晶硅(或非晶硅)层的化学刻蚀后,再继续利用合适的碱溶液工艺条件来制备绒面。在实际应用中,第一种情况会使电池工艺流程更为简明,成本更低,但同时也要结合具体电池工艺来看。一般地,碱制绒工艺条件是,温度是65-85 $^{\circ}\text{C}$ (优选:70-80 $^{\circ}\text{C}$),NaOH或KOH质量浓度是2%-5%(优选:2%-3%),制绒时间是4-20 min(优选:5-12 min)。

[0041] 综上,在实际的电池制备中,可先通过化学溶液刻蚀去除损伤层,然后制备正面的空穴局部钝化接触结构(除金属化以前的步骤),再通过碱溶液刻蚀非金属电极区域的多晶硅(或非晶硅)层,随即再完成正面金字塔绒面的制备。

[0042] ②. 电池正面的非金属电极区域的p型掺杂结

电池正面的非金属电极区域下方需要有p型掺杂结,可以是pn结(对应于n型硅衬底),也可以是高低结(对应于p型衬底)。该p型掺杂结的制备,一般地,可以放在空穴局部钝化接触结构制备过程中的碱溶液化学刻蚀无局部硼掺杂的多晶硅(或非晶硅)薄膜区域以及电池正面碱制绒都完成之后,也即实施例1的第6)步之后再进行。具体制备方法不限,可以采用比如炉管硼扩散(三氯化硼或三氯化硼)、离子注入硼结合退火或APCVD沉积硼硅玻璃结合退火,等等。应该注意到,上述硼掺杂结制备工艺方法多是实施整面均匀的硼掺杂,而本步骤只需要在非金属电极区域制备p型掺杂结,那么如果在本步中采用上述工艺方法在电池正面实施了整面的硼掺杂,其结果是对已经完成的局部掺硼多晶硅区域(也即电池正面的金属电极区域),是进一步增强了该区域的场钝化作用的,并无明显副作用。考虑到电池工艺制备的简洁性,更为优选地,可以采用选择性的硼离子注入结合退火来完成该步制备(也即只在非金属电极区域实施硼掺杂)。在完成本步制备后,一般地,非金属电极区域p型掺杂结的表面硼掺杂浓度是 $7E18-5E19\text{ cm}^{-3}$ (优选: $1E19-2E19\text{ cm}^{-3}$),方块电阻是 $40-130\text{ }\Omega/\square$ (优选: $80-110\text{ }\Omega/\square$)。

[0043] ③. 电池正面的钝化减反射膜

所述电池正面的钝化减反膜可以是氧化铝、氧化硅、氮氧化硅、氮化硅中的一种或者多种的叠加,也并不局限于此,制备方法不限。可选地,所述钝化减反膜的厚度是 $60-100\text{ nm}$,折射率是 $1.5-2.3$;优选地,厚度 $70-80\text{ nm}$,折射率 $1.8-2.1$ 。

[0044] 此外,一般地,在掺硼多晶硅层上会再覆盖上一层氮化硅或氮氧化硅膜,作为后续金属化的缓冲阻挡层,用来缓冲阻挡金属在后续烧结退火中过多地扩散穿过掺硼多晶硅层和隧穿氧化硅层而进入硅衬底,最理想的是将金属完全限制在多晶硅层内。这层氮化硅或氮氧化硅一般通过PECVD工艺制备,也不局限于此;其厚度一般是 $50-180\text{ nm}$ (优选: $70-100\text{ nm}$),折射率是 $1.8-2.3$ (优选 $1.9-2.1$)。

[0045] 因此,在实际的电池工艺制备中,正面的钝化减反射膜如果采用氮化硅或氮氧化硅,正好可以起到上述金属化缓冲层的作用。

[0046] ④. 电池正面的金属化

电池正面的金属化也就是对有局部硼掺杂的多晶硅薄膜区域进行金属化,其制备方法和图案设计前面已经给出,此处不再赘述。

[0047] 电池背面可以采用全面积(也即整面均匀的)的电子钝化接触结构,也可以采用常规的n型掺杂结和钝化膜,以及相应的金属化。具体说明如下:

(1)结合图3所示,电池背面是全面积的电子钝化接触结构。

[0048] ①. 电池背面的形貌可以是抛光面或绒面形貌,抛光面结构可以通过前述的碱溶液或酸溶液抛光刻蚀去除损伤层的步骤来完成,绒面结构制备则可以整合在电池制备中的合适步骤通过碱溶液刻蚀完成。

[0049] ②. 隧穿氧化硅层:电池背面的隧穿氧化硅层的厚度和折射率以及相应的制备方法,与电池正面的隧穿氧化硅层相同,不再赘述。一般地,可以采用热氧化或者化学氧化(比如硝酸)同时完成电池正面和背面的隧穿氧化硅膜的生长。

[0050] ③. 掺磷多晶硅层

掺磷多晶硅层主要有两类制备方法,也不局限于此。第一类方法,通过LPCVD、PECVD或PVD等方法沉积本征非晶硅,然后采用三氯氧磷扩散,或离子注入结合退火,来完成磷掺杂。

第二类方法是在PECVD沉积非晶硅时,通入磷烷(工艺气体一般是硅烷、氢气和磷烷,以及氮气)来在线掺入磷掺杂剂,然后退火。退火可以采用炉管或快速热处理炉的高温退火等,也不限于此。退火工艺参数的选择要兼顾考虑完成从非晶硅到多晶硅的充分晶化,以及磷的充分激活和在多晶硅层内的再分布。上述制备完成后,可选地,掺磷多晶硅层的厚度是30-200 nm(优选:70-150 nm),多晶硅层表面的磷掺杂浓度 $1\text{E}19\text{-}1\text{E}21\text{ cm}^{-3}$ (优选: $1\text{E}20\text{-}5\text{E}20\text{ cm}^{-3}$),磷方块电阻30-150 $\Omega/\square$ (优选:50-100 $\Omega/\square$)。

[0051] 一般地,在掺磷多晶硅层上会再覆盖上一层氮化硅或氮氧化硅膜,作为后续金属化的缓冲阻挡层,用来缓冲阻挡金属在后续烧结退火中过多地扩散穿过多晶硅层和隧穿氧化硅层而进入硅衬底,最理想的是将金属完全限制在多晶硅层内。这层氮化硅或氮氧化硅膜一般通过PECVD工艺制备,也不局限于此;其厚度一般是50-180 nm(优选:70-100 nm),折射率是1.8-2.3(优选1.9-2.1)。

[0052] ④. 电池背面金属化的材料选择和制备方法与电池正面的金属化相同,不再赘述;不同的是,背面金属化一般不需要进行对准。背面金属化电极图案一般也采用等间距栅线设计,也可以采用全面积的金属化(往往与PVD银技术相结合),也不局限于此。

[0053] (2) 结合图4所示,电池背面是常规的n型掺杂结和钝化膜

①. 电池背面的形貌同上(1)-①,不再赘述。

[0054] ②. 电池背面的n型掺杂结可以是pn结(对应于p型硅衬底)或高低结(对应于n型硅衬底);可以是整面的均匀结,也可以是选择性掺杂结(也即非金属电极区轻掺杂,金属电极区重掺杂)。具体制备方法可以采用三氯氧磷扩散、离子注入、APCVD沉积磷硅玻璃结合退火、磷源旋涂或激光掺杂等,也不限于此。电池背面的n型掺杂结,表面浓度一般在 $5\text{E}19\text{ cm}^{-3}\text{-}2\text{E}20\text{ cm}^{-3}$ 范围,方块电阻是30-150 $\Omega/\square$,也不限于此。

[0055] ③. 电池背面钝化膜可以是氮化硅、氧化硅、氮氧化硅、氧化铝中的一种或多种叠加,制备方式不限。背面钝化层厚度50-200 nm,折射率1.5-2.5,也不局限于此。

[0056] ④. 电池背面金属化的材料一般选用银,具体制备方法与前述相同,不再赘述。金属电极图案一般采用等间距栅线状设计,也不局限于此。如果电池背面的n型掺杂结是选择性掺杂结,金属化需要采用对准技术。

[0057] 基于上述说明,下面通过具体的实施例说明将本发明所述的局部空穴钝化接触应用于具体的电池结构并给出相应的电池制备方法。以下实施例仅用于更加清楚地说明本发明的技术方案,而不能以此来限制本发明的保护范围。

[0058] 实施例3公开一种具有空穴局部钝化接触结构的太阳能电池结构及其制备方法。本实施例所给出的电池结构如图3所示,电池正面采用空穴局部钝化接触,电池背面采用全面积的电子钝化接触。衬底材料这里选用n型单晶硅(也可以选用p型单晶硅)。

[0059] 该电池的制备方法具体如下:

A1:选用一种156mm*156mm的(100)晶向的n型单晶硅片,电阻率 $1\text{ }\Omega\cdot\text{cm}$,厚度180 μm 。

[0060] A2:采用氢氧化钠抛光去除所述n型硅片表面的损伤层(约10 μm)。

[0061] A3:采用热氧化工艺在所述n型硅片的两个面制备隧穿氧化硅层,厚度1.5 nm,折射率1.46。

[0062] A4:采用PECVD工艺在所述n型硅片正面制备本征非晶硅,厚度是80 nm。由于PECVD方法的绕镀很少,并且绕镀的本征非晶硅主要产生在所述n型硅片背面边缘很窄的范围内

(小于0.5 mm),所以对电池背面结构影响非常小,后续可以通过激光边缘隔离工艺来消除这种影响。

[0063] A5:采用PECVD工艺在所述n型硅片背面制备非晶硅膜,同时在工艺中通入磷烷实现在线掺入磷掺杂剂,膜厚是100 nm。如上A4步中所述,在本步骤PECVD沉积的非晶硅绕镀到所述n型硅片正面的影响也同样非常小,后续可以通过激光边缘隔离工艺来消除这种影响。

[0064] A6:通过选择性离子注入硼的方法,在所述n型硅片正面的本征非晶硅薄膜层上覆盖局部硼掺杂剂,硼离子注入的剂量 $4E15-1E16\text{ cm}^{-2}$,能量是5-10 keV。局部覆盖硼掺杂剂的图案采用栅线分布设计,其线宽是75 μm ,两根相邻栅线的间距(轴心线之间)1.5 mm。

[0065] A7:采用炉管退火,将所述n型硅片正面的非晶硅充分晶化为多晶硅,在步骤S6中通过选择性硼离子注入所覆盖的局部硼掺杂剂也在退火中完成激活以及在多晶硅薄膜内的再分布;同步地,在退火中,所述硅片背面的非晶硅也充分晶化为多晶硅,在步骤A5中在线掺入的磷掺杂剂也完成激活以及在多晶硅薄膜内的再分布。炉管退火温度是950-1000°C,时间30-45 min,氮气气氛。经过退火,硅片正面局部掺硼的多晶硅层的硼表面浓度是 $9E19-1E20\text{ cm}^{-3}$,方块电阻是30-40 $\Omega/\square$;硅片背面的掺磷多晶硅层的磷表面浓度是 $3E20\text{ cm}^{-3}$,方块电阻是50 $\Omega/\square$ 。

[0066] A8:采用PECVD工艺在所述n型硅片背面沉积氮化硅膜,厚度100 nm,折射率2.0。这层氮化硅也作为硅片背面的保护层,用来有效地阻挡后续步骤A9中的碱溶液刻蚀。

[0067] A9:采用NaOH溶液对所述n型硅片正面无局部硼掺杂的多晶硅薄膜区域进行化学刻蚀,将该区域的多晶硅薄膜全部刻蚀掉。NaOH溶液质量浓度是2.5%,温度70°C,刻蚀时间5 min。然后继续利用该NaOH溶液对硅片正面进行制绒,制绒时间5 min。在本步的碱溶液刻蚀多晶硅层和碱制绒中,由A8步在硅片背面沉积的氮化硅膜对所述n型硅片背面起到了很好的保护作用。

[0068] A10:在所述n型硅片正面无局部硼掺杂的区域(此时该区域的多晶硅层已经被刻蚀掉,并且具有随机金字塔绒面的形貌)制备均匀硼掺杂结。采用选择性离子注入硼的方法,再利用激光退火完成离子注入的硼的激活以及在所述n型硅片内的再分布。具体激光退火参数是,采用Nd:YVO₄固态激光器,波长532 nm,激光功率500-1000 兆瓦,脉冲宽度10-40 ns,重复频率是20 kHz。经过退火,本步所述的区域(非金属电极区域)的硼掺杂表面浓度是 $1E19\text{ cm}^{-3}$,方块电阻是90 $\Omega/\square$ 。

[0069] A11:在所述n型硅片正面制备钝化减反膜,利用PECVD工艺沉积氮氧化硅膜,厚度75 nm,折射率1.9。

[0070] A12:通过丝网印刷银浆结合烧结的方法在所述n型硅片正面和背面实施金属化,其中硅片正面的金属化需要采用对准技术,也即实现前述的局部掺硼多晶硅区域和金属电极区域的对准。电池正面金属化的栅线图案设计,其线宽是30 μm ,两根相邻栅线的间距(轴心线之间)1.5 mm。

[0071] A13:采用激光边缘隔离工艺,将所述n型硅片边缘进行电学隔离。

[0072] 实施例4公开另一种具有空穴局部钝化接触结构的太阳能电池结构及制备方法。本实施例所给出的电池结构如图4所示,电池正面采用空穴局部钝化接触,电池背面采用n型掺杂结和相应的钝化膜。本例中衬底材料选用p型单晶硅。电池制备方法具体如下:

- B1: 选用一种156mm*156mm的(100)晶向的p型单晶硅片,电阻率 $1\ \Omega \cdot \text{cm}$,厚度180 μm 。
- [0073] B2: 利用氢氧化钠溶液抛光去除所述p型硅片表面的损伤层(约10 μm)。
- [0074] B3: 采用热氧化工艺在所述p型硅片表面制备隧穿氧化硅层,厚度1.3 nm,折射率1.46。
- [0075] B4: 采用LPCVD工艺在所述p型硅片的正面制备本征非晶硅,厚度是70 nm。
- [0076] B5: 通过丝网印刷的方法在所述p型硅片正面的非晶硅层上印刷硼浆,将其烘干(烘干温度150-200°C,烘干时间1-2 min)。局部覆盖硼掺杂剂的图案采用栅线分布设计,其线宽是100 μm ,两根相邻栅线的间距(轴心线之间)1.6 mm。
- [0077] B6: 采用激光退火,将所述p型硅片正面局部覆盖含硼掺杂剂区域的非晶硅充分晶化为多晶硅,硼浆中的硼掺杂剂也完成激活以及在多晶硅薄膜内的再分布。激光退火参数,采用Nd:YVO₄固态激光器,波长532 nm,激光功率500-1000 兆瓦,激光脉宽10-50 ns,重复频率是10-20 kHz。经过退火,局部掺硼多晶硅层的硼表面浓度是 $2\text{E}20\ \text{cm}^{-3}$,方块电阻55 $\Omega/\square$ 。
- [0078] B7: 采用KOH溶液对所述p型硅片正面的无局部硼掺杂的非晶硅薄膜区域进行刻蚀,将该区域的非晶硅层全部刻蚀掉。KOH溶液质量浓度是2%,温度70°C,刻蚀时间2 min。紧接着,继续利用本步所述的KOH溶液对硅片进行制绒,制绒时间5 min。需要强调,在本步的化学刻蚀后,前述步骤B3中在硅片背面也生长的隧穿氧化硅层也被刻蚀掉,随后在硅片背面也得到了随机金字塔形貌的绒面。
- [0079] B8: 在所述p型硅片正面无局部硼掺杂的区域(此时该区域的非晶硅层已被刻蚀掉,并且是随机金字塔绒面形貌)制备均匀硼掺杂结。采用选择性离子注入硼的方法,只在未覆盖硼掺杂剂(前述步骤B5中的硼浆)的区域实施硼离子注入,然后采用炉管退火对离子注入的硼进行激活和再分布,退火温度960°C,时间是45 min,氮气气氛。经过退火,本步骤所述区域(非金属电极区域)的硼掺杂表面浓度 $1\text{E}19\ \text{cm}^{-3}$,方块电阻90 $\Omega/\square$ 。此处需要强调的是,经过这步炉管退火,前述通过印刷硼浆和激光退火(步骤B5和B6)所实现局部掺硼多晶硅薄膜区域的硼掺杂会进一步再分布,硼表面浓度变为 $1\ \text{E}20\ \text{cm}^{-3}$,方块电阻变为40 $\Omega/\square$ 。
- [0080] B9: 采用硝酸和氢氟酸的混合溶液结合水上漂的湿法刻蚀设备,对所述p型硅片背面进行化学刻蚀。经过这步化学刻蚀,在步骤B7中使得硅片背面得到的随机金字塔绒面被刻蚀掉,背面形成抛光面。所述硝酸质量浓度40%,氢氟酸质量浓度4%,溶液温度为7°C 刻蚀时间20 sec。
- [0081] B10: 通过离子注入结合炉管退火的方法对所述p型硅片背面实施整面均匀的磷掺杂,磷表面浓度是 $1\ \text{E}20\ \text{cm}^{-3}$,方块电阻是80 $\Omega/\square$ 。由于本步的退火温度比较低,一般用830-850°C,因此对硅片正面的硼掺杂影响并不大,可以忽略。
- [0082] B11: 在所述p型硅片背面制备钝化膜,利用PECVD工艺沉积氮化硅膜,厚度90 nm,折射率2.0。
- [0083] B12: 在所述p型硅片正面制备钝化减反膜,采用PECVD方法沉积氮氧化硅膜,厚度75 nm,折射率1.9。
- [0084] B13: 通过丝网印刷银浆结合烧结的方法在所述p型硅片的正面和背面实施金属化,其中硅片正面的金属化需要采用对准技术,也即实现前述的局部掺硼多晶硅区域和金

属化区域的对准。电池正面金属化的栅线图案设计,其线宽是30 μm ,两根相邻栅线的间距(轴心线之间)1.6 mm。

[0085] B14:采用激光边缘隔离工艺,将所述p型硅片边缘进行电学隔离。

[0086] 最后需要说明的是,尽管以上结合附图对本发明的实施方案进行了描述,但本发明并不局限于上述的具体实施方案和应用领域,上述的具体实施方案仅仅是示意性的、指导性的,而不是限制性的。本领域的普通技术人员在本说明书的启示下,在不脱离本发明权利要求所保护的范围的情况下,还可以做出很多种的形式,这些均属于本发明保护之列。

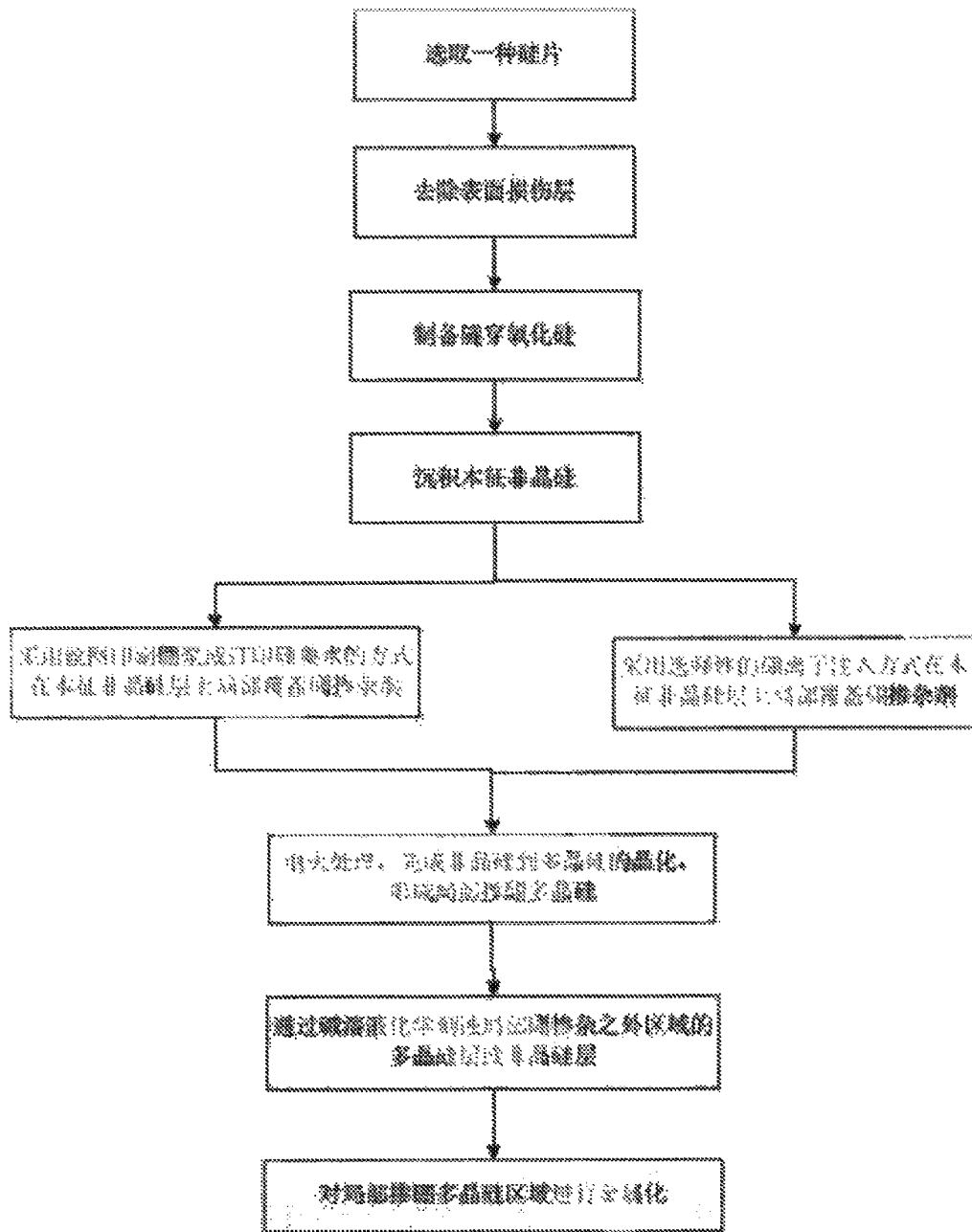


图1

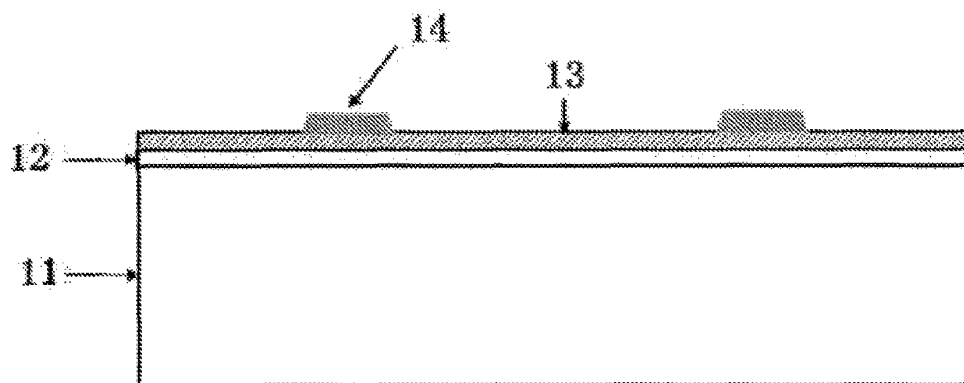


图2-a

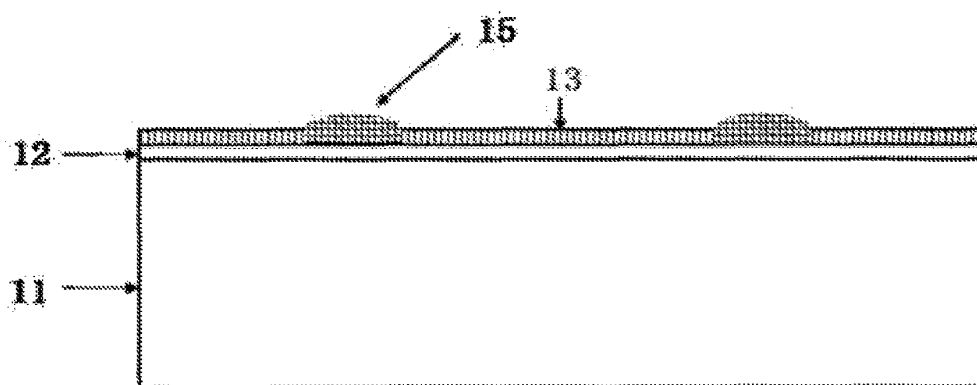


图2-b

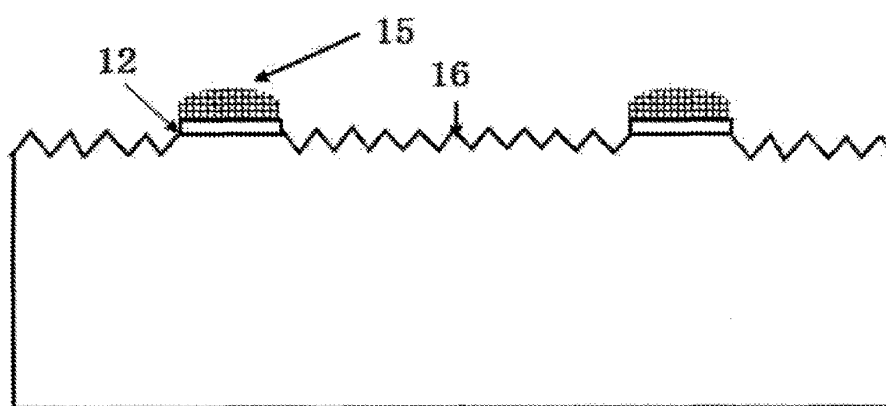


图2-c

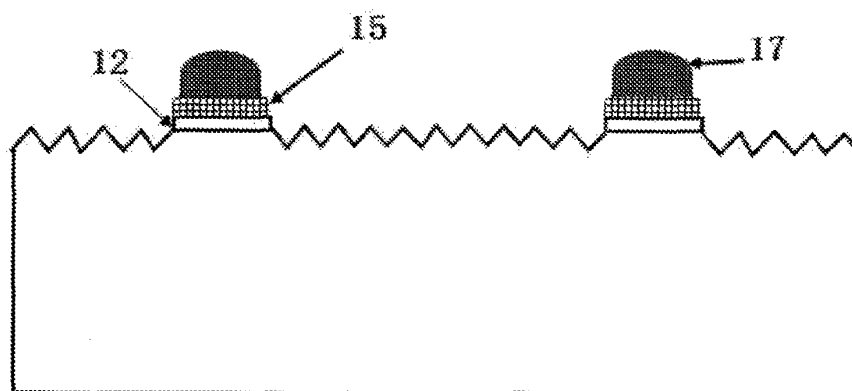


图2-d

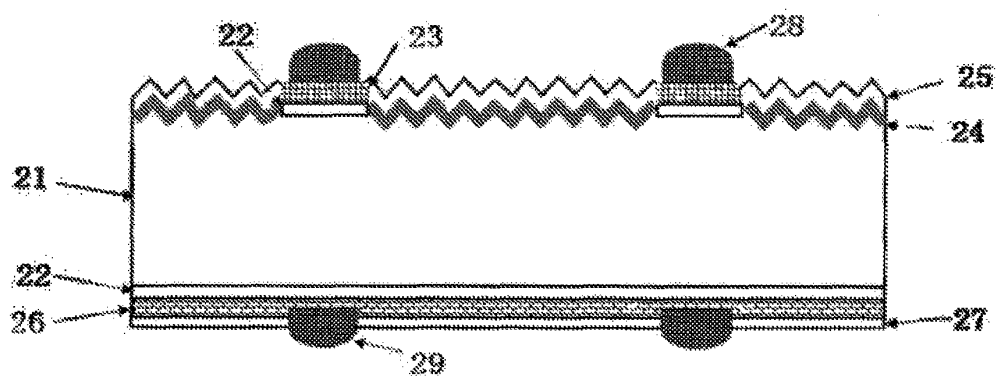


图3

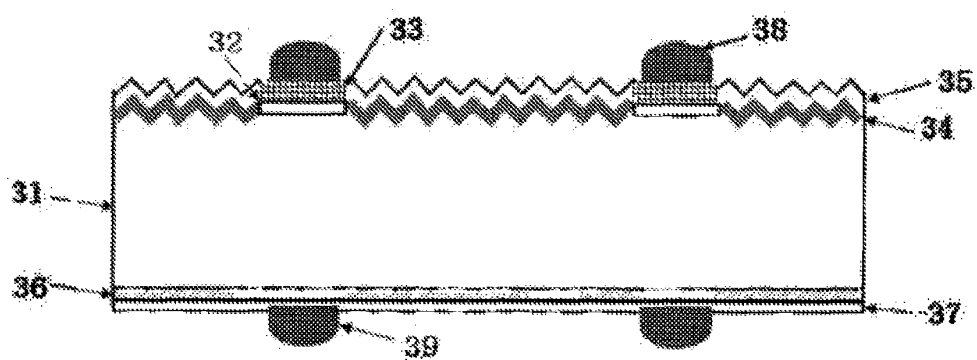


图4



Espacenet

Bibliographic data: CN212750903 (U) — 2021-03-19

Solar cell

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Applicant(s): CSI SOLAR TECH JIAXING CO LTD ± (嘉兴阿特斯光伏技术有限公司)

Classification: - international: H01L31/0216; H01L31/0236
- cooperative: Y02E10/50 (EP)

Application number: CN202022300702U 20201015

Priority number(s): CN202022300702U 20201015

Abstract of CN212750903 (U)

The invention provides a solar cell. The solar cell comprises a silicon substrate, and a tunneling layer and a polycrystalline silicon layer which are sequentially arranged on the back surface of the silicon substrate, wherein the back surface of the silicon substrate is pyramid-shaped, and the height of the back surface of the silicon substrate is set to be 0.5-1.5 [μm]. According to the solar cell, the back face of the silicon substrate is arranged to be of the pyramid structure with the set height, so that the polycrystalline silicon layer prepared through subsequent deposition is also in a pyramid shape, the contact area between the metal electrode and the polycrystalline silicon layer is increased, the contact performance between the metal electrode and the polycrystalline silicon layer is improved, the contact resistance is reduced, and the conversion efficiency of the cell is improved.



(12) 实用新型专利

(10) 授权公告号 CN 212750903 U

(45) 授权公告日 2021.03.19

(21) 申请号 202022300702.5

(22) 申请日 2020.10.15

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(51) Int.Cl.

H01L 31/0216 (2014.01)

H01L 31/0236 (2006.01)

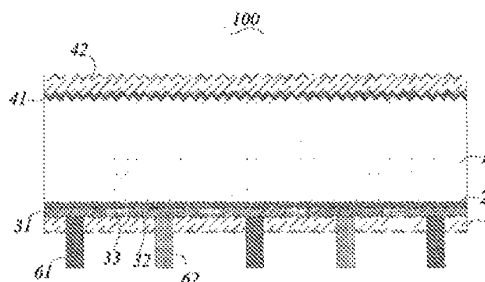
权利要求书1页 说明书4页 附图2页

(54) 实用新型名称

太阳能电池

(57) 摘要

本申请提供了一种太阳能电池,包括硅基底、依次设置在所述硅基底背面的隧穿层与多晶硅层;所述硅基底的背面设置呈金字塔状,且所述硅基底背面的绒面高度设置为 $0.5\sim 1.5\mu\text{m}$ 。所述太阳能电池通过将硅基底背面设置呈具有既定绒面高度的金字塔结构,使得后续沉积制备的多晶硅层亦呈金字塔状,增大金属电极与多晶硅层的接触面积,改善金属电极与多晶硅层的接触性能,降低接触电阻,利于提高电池转换效率。



1. 一种太阳能电池,包括硅基底、依次设置在所述硅基底背面的隧穿层与多晶硅层,其特征在于:所述硅基底的背面设置呈金字塔状,且所述硅基底背面的绒面高度设置为 $0.5\sim 1.5\mu\text{m}$ 。

2. 根据权利要求1所述的太阳能电池,其特征在于:所述硅基底的正面同样设置呈金字塔状,且所述硅基底正面的绒面高度设置为 $2\sim 4\mu\text{m}$ 。

3. 根据权利要求1所述的太阳能电池,其特征在于:所述硅基底具有第一区域与第二区域;所述多晶硅层包括设置在所述第一区域的第一掺杂多晶硅层、设置在所述第二区域的第二掺杂多晶硅层。

4. 根据权利要求3所述的太阳能电池,其特征在于:所述第一掺杂多晶硅层设置为掺硼的P型多晶硅层;所述第二掺杂多晶硅层设置为掺磷的N型多晶硅层。

5. 根据权利要求3所述的太阳能电池,其特征在于:所述第一区域包括若干第一条形区,所述第二区域包括若干第二条形区,所述第一条形区与第二条形区依次交替排布且呈相互间隔设置。

6. 根据权利要求5所述的太阳能电池,其特征在于:所述第一条形区与第二条形区两者的宽度均设置为 $40\sim 500\mu\text{m}$,相邻所述第一条形区与第二条形区的间隙宽度设置为 $50\sim 500\mu\text{m}$ 。

7. 根据权利要求3所述的太阳能电池,其特征在于:所述太阳能电池还包括设置在所述硅基底背面的背表面膜层与金属电极,所述金属电极包括穿过所述背表面膜层并与第一掺杂多晶硅层接触的第一电极、穿过所述背表面膜层并与第二掺杂多晶硅层接触的第二电极。

8. 根据权利要求1所述的太阳能电池,其特征在于:所述太阳能电池还包括设置在所述硅基底正面的钝化层、设置在所述钝化层背离所述硅基底一侧的减反射层。

9. 根据权利要求8所述的太阳能电池,其特征在于:所述钝化层设置为 SiO_2 膜且所述钝化层的厚度设置为 $2\sim 6\text{nm}$ 。

10. 根据权利要求8所述的太阳能电池,其特征在于:所述减反射层包括邻近所述钝化层设置的氮化硅膜层,所述氮化硅膜层的折射率设置为 $2.1\sim 2.4$,且该氮化硅膜层的厚度设置为 $5\sim 30\text{nm}$ 。

太阳能电池

技术领域

[0001] 本申请涉及太阳能电池生产技术领域,尤其涉及一种太阳能电池。

背景技术

[0002] 近年,随着光伏技术与市场的快速发展,业内对太阳能电池的转换效率也提出越来越高的需求。TOPCon (Tunnel Oxide Passivated Contact,隧穿氧化层钝化接触)电池通过在表面制备一层超薄的隧穿氧化层和一层掺杂多晶硅层,提高表面钝化性能,有效提升电池的开路电压与短路电流。上述TOPCon电池生产过程中通常包括将硅基底表面清洗、抛光,再依次沉积制备上述隧穿氧化层与掺杂多晶硅层,所述硅基底的表面形态对其表面膜层性能影响较大。业内还公开一种POLO-IBC电池,将上述电池钝化结构与背电池设计相结合,以提高电池转换效率。但整体生产工艺较为复杂,工艺精度要求也比较严格,电池生产成本也较高,产业化应用较为困难。

[0003] 鉴于此,有必要提供一种新的太阳能电池。

实用新型内容

[0004] 本实用新型的目的在于提供一种太阳能电池,能够改善金属电极的接触性能,提高电池转换效率。

[0005] 为实现上述实用新型目的,本申请提供了一种太阳能电池,包括硅基底、依次设置在所述硅基底背面的隧穿层与多晶硅层;所述硅基底的背面设置呈金字塔状,且所述硅基底背面的绒面高度设置为 $0.5\sim 1.5\mu\text{m}$ 。

[0006] 作为本申请的进一步改进,所述硅基底的正面同样设置呈金字塔状,且所述硅基底正面的绒面高度设置为 $2\sim 4\mu\text{m}$ 。

[0007] 作为本申请的进一步改进,所述硅基底具有第一区域与第二区域;所述多晶硅层包括设置在所述第一区域的第一掺杂多晶硅层、设置在所述第二区域的第二掺杂多晶硅层。

[0008] 作为本申请的进一步改进,所述第一掺杂多晶硅层设置为掺硼的P型多晶硅层;所述第二掺杂多晶硅层设置为掺磷的N型多晶硅层。

[0009] 作为本申请的进一步改进,所述第一区域包括若干第一条形区,所述第二区域包括若干第二条形区,所述第一条形区与第二条形区依次交替排布且呈相互间隔设置。

[0010] 作为本申请的进一步改进,所述第一条形区与第二条形区两者的宽度均设置为 $40\sim 500\mu\text{m}$,相邻所述第一条形区与第二条形区的间隙宽度设置为 $50\sim 500\mu\text{m}$ 。

[0011] 作为本申请的进一步改进,所述太阳能电池还包括设置在所述硅基底背面的背表面膜层与金属电极,所述金属电极包括穿过所述背表面膜层并与第一掺杂多晶硅层接触的第一电极、穿过所述背表面膜层并与第二掺杂多晶硅层接触的第二电极。

[0012] 作为本申请的进一步改进,所述太阳能电池还包括设置在所述硅基底正面的钝化层、设置在所述钝化层背离所述硅基底一侧的减反射层。

[0013] 作为本申请的进一步改进,所述钝化层设置为 SiO_2 膜且所述钝化层的厚度设置为2~6nm。

[0014] 作为本申请的进一步改进,所述减反射层包括邻近所述钝化层设置的氮化硅膜层,所述氮化硅膜层的折射率设置为2.1~2.4,且该氮化硅膜层的厚度设置为5~30nm。

[0015] 本申请的有益效果是:采用本申请太阳能电池,通过将所述硅基底背面设置呈具有既定绒面高度的金字塔结构,使得所述硅基底背面后续沉积制备的多晶硅层亦呈金字塔状,增大金属电极与多晶硅层的接触面积,改善金属电极与多晶硅层的接触性能,降低接触电阻,利于提高电池转换效率。

附图说明

[0016] 图1是本申请太阳能电池的结构示意图;

[0017] 图2是本申请太阳能电池中硅基底的背面示意图;

[0018] 图3是本申请太阳能电池的制备方法的主要流程示意图。

[0019] 100-太阳能电池;1-硅基底;11-第一区域;110-第一条形区;12-第二区域;120-第二条形区;2-隧穿层;31-第一掺杂多晶硅层;32-第二掺杂多晶硅层;33-本征多晶硅层;41-钝化层;42-减反射层;5-背表面膜层;61-第一电极;62-第二电极。

具体实施方式

[0020] 以下将结合附图所示的实施方式对本实用新型进行详细描述。但该实施方式并不限制本实用新型,本领域的普通技术人员根据该实施方式所做出的结构、方法、或功能上的变换均包含在本实用新型的保护范围内。

[0021] 参图1所示,本申请提供的太阳能电池100包括硅基底1、设置在所述硅基底1背面的隧穿层2与多晶硅层。在此,所述太阳能电池100为背接触电池,所述硅基底1采用N型单晶硅片;所述隧穿层2设置为 SiO_2 膜层或 SiO_xN_y 膜层;所述多晶硅层包括依次交替排布的第一掺杂多晶硅层31、第二掺杂多晶硅层32及本征多晶硅层33。

[0022] 所述硅基底1的电阻率设置为 $0.3\sim 7\ \Omega\cdot\text{cm}$,优选为 $0.7\sim 3.5\ \Omega\cdot\text{cm}$;所述隧穿层2的厚度优选设置为 $0.5\sim 3\text{nm}$;所述多晶硅层的厚度优选设置为 $60\text{nm}\sim 200\text{nm}$ 。此处,所述第一掺杂多晶硅层31为掺硼的P型多晶硅层,所述第一掺杂多晶硅层31的硼掺杂浓度为 $1\text{E}19\sim 5\text{E}20\text{cm}^{-3}$;所述第二掺杂多晶硅层32为掺磷的N型多晶硅层,所述第二掺杂多晶硅层32的磷掺杂浓度为 $1\text{E}20\sim 5\text{E}20\text{cm}^{-3}$ 。

[0023] 所述太阳能电池100还包括设置在所述硅基底1正面的钝化层41与减反射层42,所述钝化层41设置为 SiO_2 膜且其厚度设置为2~6nm。所述减反射层42可设置为氮化硅膜、氮氧化硅膜、氧化硅膜或氟化镁膜中的一种或由至少两种前述膜层构成的复合膜层。所述减反射层42设置为复合膜层时,不同膜层的折射率由内向外逐渐减小,当然,所述减反射层42或构成所述减反射层42的任一前述膜层还可设置为渐变膜。此处,所述减反射层42包括邻近所述钝化层41设置的氮化硅膜层,该氮化硅膜层的折射率设置为2.1~2.4,且其厚度设置为5~30nm,所述氮化硅膜层还起着氢钝化的作用。

[0024] 所述太阳能电池还包括设置在多晶硅层背离硅基底1一侧的背表面膜层5、穿过所述背表面膜层5并与所述多晶硅层相接触的金属电极。所述金属电极包括设置在所述第一

掺杂多晶硅层31上的第一电极61、设置在所述第二掺杂多晶硅层32上的第二电极62。所述第一电极61、第二电极62通常采用既定的银浆，并经丝网印刷、烧结制得，根据实际产品需求与银浆性能，所述第一电极61、第二电极62两者所采用的银浆可以相同也可以不同。

[0025] 所述硅基底1的正面呈金字塔状，且其绒面高度设置为 $2\sim 4\mu\text{m}$ ，通常采用碱溶液刻蚀对所述硅基底1正面进行刻蚀得到，上述绒面高度的设置确保常规工艺条件下的绒面整体分布更为均匀，有效降低入射光线的反射率。所述硅基底1的背面同样设置呈金字塔状，且其绒面高度设置为 $0.5\sim 1.5\mu\text{m}$ ，进而使得所述硅基底1背面沉积的多晶硅层也呈上述金字塔状。此处，所述硅基底1背面的绒面高度不能设置太大，否则会影响所述隧穿层2与本征非晶硅层的沉积制备。通过上述设计，在不改变金属电极的条件下，所述第一电极61与第一掺杂多晶硅层31、第二电极62与第二掺杂多晶硅层32的接触面积得以增大，提高所述金属电极与多晶硅层的接触性能，降低接触电阻。

[0026] 结合图2所示，所述硅基底1的背面具有第一区域11与第二区域12，所述第一区域11对应设置第一掺杂多晶硅层31；所述第二区域12对应设置第二掺杂多晶硅层32。具体地，所述第一区域11包括若干第一条形区110，所述第二区域12包括若干第二条形区120，所述第一条形区110与第二条形区120依次交替排布且呈相互间隔设置。在此，所述第一条形区110与第二条形区120两者的宽度均设置为 $40\sim 500\mu\text{m}$ ，相邻所述第一条形区110与第二条形区120的间隙宽度设置为 $50\sim 500\mu\text{m}$ 。

[0027] 参图3所示，上述太阳能电池100的制备方法包括：

[0028] 提供硅基底1，对硅基底1进行第一次制绒；

[0029] 在硅基底1的背面制备隧穿层2与本征非晶硅层；

[0030] 在所述硅基底1背面的第一区域11、第二区域12分别设置第一掺杂源层、第二掺杂源层；

[0031] 退火，使得第一区域11、第二区域12分别形成第一掺杂多晶硅层31与第二掺杂多晶硅层32，所述第一掺杂多晶硅层31与第二掺杂多晶硅层32两者的掺杂类型相反且呈相互间隔设置；

[0032] 对硅基底1的正面进行第二次制绒；

[0033] 依次进行清洗、镀膜与金属化，得到相应的太阳能电池100。

[0034] 所述第一次制绒与第二次制绒均采用碱溶液对硅基底进行刻蚀，所述碱溶液是指KOH或NaOH或TMAH的水溶液，其可将所述硅基底1表面刻蚀生成金字塔状的绒面结构。所述第一次制绒过程控制所述硅基底1的背面的绒面高度介于 $0.5\sim 1.5\mu\text{m}$ ；所述第二次制绒过程控制所述硅基底1的正面的绒面高度介于 $2\sim 4\mu\text{m}$ 。当然，所述第一次制绒、第二次制绒过程均可根据实际生产需求添加相应的制绒添加剂。

[0035] 在对硅基底1进行第一次制绒前，先采用酸溶液或碱溶液对所述硅基底1进行粗抛，去除所述硅基底1表面的机械损伤层。所述第一次制绒可以仅对所述硅基底1背面进行单面制绒，也可以采用双面制绒；所述第二次制绒是指对所述硅基底1的正面进行单面制绒。

[0036] 本实施例中，所述隧穿层2采用 SiO_2 膜层，所述 SiO_2 膜层采用湿化学氧化、热氧化、臭氧氧化三者中的任一种或任意两种方法相结合制得；所述本征非晶硅层采用LPCVD或PECVD方法制得。

[0037] 所述“在所述硅基底1背面的第一区域11、第二区域12分别设置第一掺杂源层、第二掺杂源层”是指在所述硅基底1背面的第一区域11的本征非晶硅层上设置硼浆,并在所述硅基底1背面的第二区域12的本征非晶硅层上设置磷浆。具体地,所述硼浆与磷浆可以采用丝网印刷或喷涂的方式转移至所述硅基底1的背面,或采用3D打印的方式在所述硅基底1背面直接形成图案化的第一掺杂源层、第二掺杂源层。

[0038] 所述退火步骤的温度设置为850~1100℃,通过高温过程使得前述本征非晶硅层转变为多晶硅层,同时,所述第一区域11、第二区域12分别形成掺硼的P型第一掺杂多晶硅层31与掺磷的N型第二掺杂多晶硅层32。所述退火步骤还包括向反应腔内通入氧气,使得所述硅基底1的正面形成氧化层,且使得所述硅基底1的背面形成掩膜层,通入的氧气氧气也有利于去除残留的少量有机成分。所述氧化层主要是指氧化硅层;所述掩膜层包括形成在所述第一掺杂多晶硅层31表面的BSG层、形成在所述第二掺杂多晶硅层32表面的PSG层以及形成在所述BSG层与PSG层两者间隙区域的氧化硅层。

[0039] 在对所述硅基底1进行第二次制绒前,需要去除所述硅基底1正面的氧化层,通常可采用链式清洗设备对所述硅基底1正面进行清洗;同时,保留所述硅基底1背面的掩膜层,避免第二次制绒过程破坏所述硅基底1背面的多晶硅层结构。

[0040] 所述第二次制绒后的硅基底1再进行清洗,去除表面的氧化层与掩膜层;再对清洗、干燥完成后的硅基底1进行镀膜。所述镀膜步骤包括先采用PECVD方法在所述硅基底1正面沉积钝化层41;再于所述钝化层41背离所述硅基底1的一侧表面制备减反射层42。当然,所述镀膜步骤还包括在所述硅基底1的背面制备背表面膜层5,所述背表面膜层5及减反射层42的具体结构与制备过程不再赘述。此处,所述钝化层41设置为 SiO_2 膜且其厚度设置为2~6nm,所述硅基底1的背面可同时沉积得到相应的 SiO_2 膜,即所述背表面膜层5包括与所述多晶硅层相接触的 SiO_2 膜。

[0041] 所述金属化步骤主要是将既定浆料通过网版印刷在所述硅基底1背面的背表面膜层5上;再经烘干、烧结,使得所述浆料烧穿所述背表面膜层5并与所述多晶硅层形成欧姆接触。

[0042] 综上所述,本申请太阳能电池100将多晶硅钝化接触结构与背接触设计相结合,提高电池转换效率。上述制备方法的工艺较为简洁,避免多次高温制程可能对硅基底1及相应膜层结构造成的损伤;通过第一次制绒后在硅基底1背面形成相应的绒面结构,再沉积隧穿层2与本征非晶硅层,改善后续金属电极与第一掺杂多晶硅层31、第二掺杂多晶硅层32的接触性能,降低接触电阻;再通过第二次制绒确保所述硅基底1正面的减反射性能,提高电池转换效率。

[0043] 应当理解,虽然本说明书按照实施方式加以描述,但并非每个实施方式仅包含一个独立的技术方案,说明书的这种叙述方式仅仅是为清楚起见,本领域技术人员应当将说明书作为一个整体,各实施方式中的技术方案也可以经适当组合,形成本领域技术人员可以理解的其他实施方式。

[0044] 上文所列出的一系列的详细说明仅仅是针对本实用新型的可行性实施方式的具体说明,它们并非用以限制本实用新型的保护范围,凡未脱离本实用新型技艺精神所作的等效实施方式或变更均应包含在本实用新型的保护范围之内。

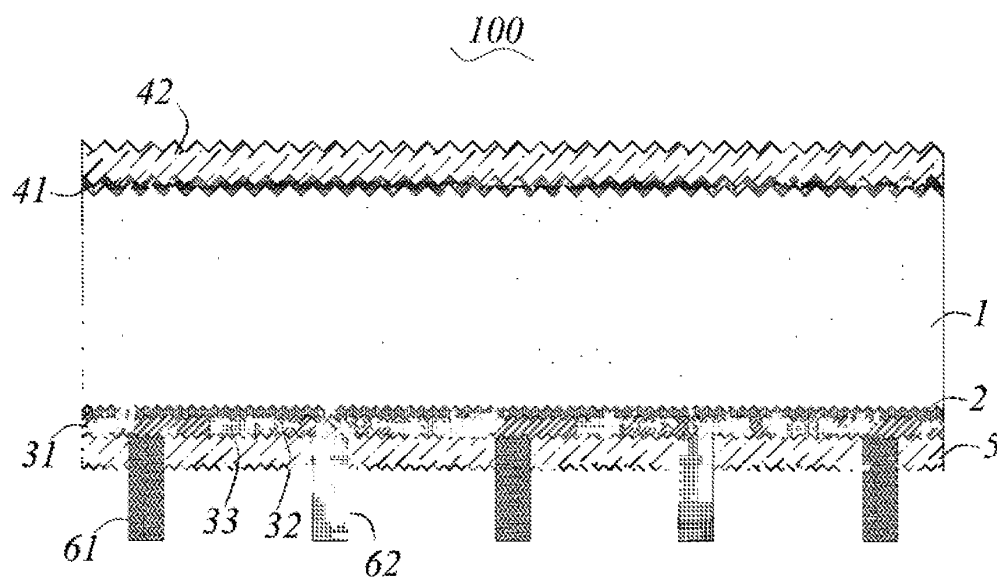


图1

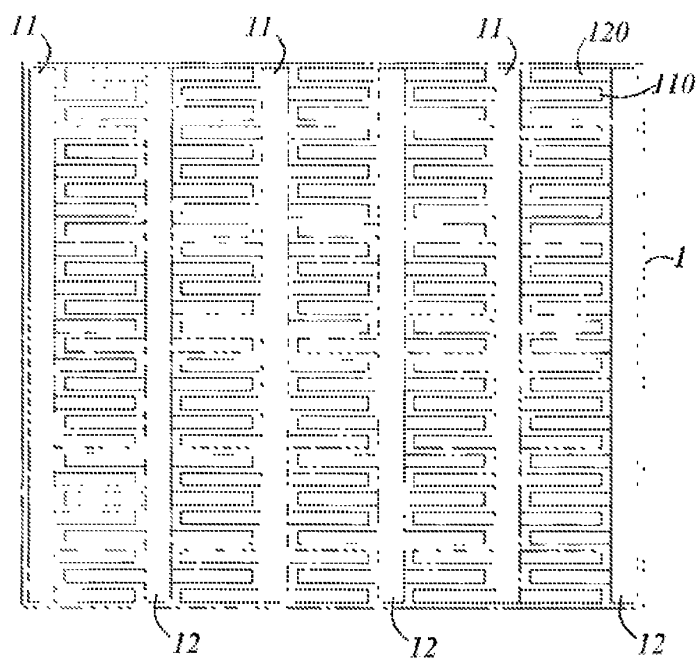


图2

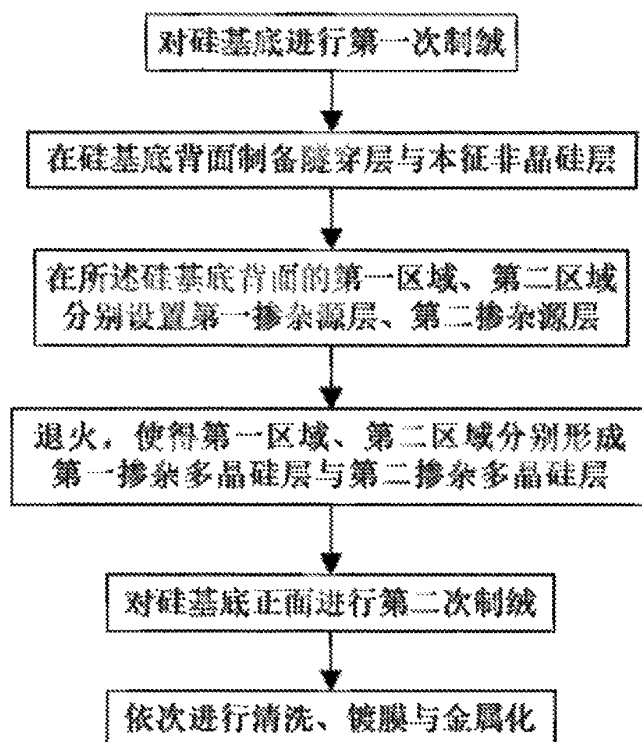


图3



(11) **EP 2 149 915 A2**

(12) **EUROPEAN PATENT APPLICATION**

(43) Date of publication:
03.02.2010 Bulletin 2010/05

(51) Int Cl.:
H01L 31/18^(2006.01) H01L 31/0236^(2006.01)

(21) Application number: **09004691.3**

(22) Date of filing: **31.03.2009**

(84) Designated Contracting States:
**AT BE BG CH CY CZ DE DK EE ES FI FR GB GR
HR HU IE IS IT LI LT LU LV MC MK MT NL NO PL
PT RO SE SI SK TR**
Designated Extension States:
AL BA RS

(30) Priority: **31.07.2008 KR 20080075261**

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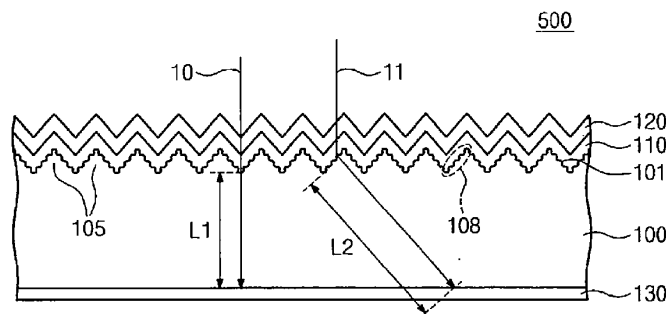
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(54) **Method of manufacturing photovoltaic device**

(57) A method of manufacturing a photovoltaic device includes preparing a semiconductor substrate having a light incidence surface receiving light and including single crystalline silicon, wet-etching the light incidence surface to form a plurality of first protrusions on the light incidence surface, dry etching a plurality of surfaces of

the first protrusions to form a plurality of second protrusions on the plurality of surfaces of the first protrusions, and forming a semiconductor layer on the light incidence surface. The method further includes forming a first electrode on the semiconductor layer and forming a second electrode on a rear surface of the semiconductor substrate facing the light incidence surface.

Fig. 1



EP 2 149 915 A2

Printed by Jouve, 75001 PARIS (FR)

Description**CROSS-REFERENCE TO RELATED APPLICATION**

[0001] This application relies for priority upon Korean Patent Application No. 2008-75261 filed on July 31, 2008, the contents of which are hereby incorporated by reference herein in their entirety.

BACKGROUND**1. Technical Field**

[0002] The present disclosure relates to a method of manufacturing a photovoltaic device. More particularly, the present disclosure relates to a method of manufacturing a photovoltaic device capable of improving photoelectric conversion efficiency.

2. Description of the Related Art

[0003] A photovoltaic device may convert optical energy into electric energy. Generally, the photovoltaic device includes a semiconductor layer which may induce photovoltaic effect by absorbing external optical energy, and first and second electrodes between which the semiconductor layer is interposed.

[0004] Meanwhile, photoelectric conversion efficiency of the photovoltaic device may be determined by characteristics such as, for example, open circuit voltage, a fill factor, and a short circuit current density. Among them, the short circuit current density may increase by increasing light absorbing efficiency representing quantity of current generated from the photovoltaic device in relation to quantity of light supplied from an exterior to the semiconductor layer. Although the photoelectric conversion efficiency of the photovoltaic device may increase by enlarging the thickness of the semiconductor layer to lengthen a path of light traveling in the semiconductor layer, the manufacturing costs and manufacturing time of the photovoltaic device may increase if the thickness of the semiconductor layer increases. In addition, as the characteristic of the fill factor may degraded, improvement in the photoelectric conversion efficiency may be difficult to obtain.

SUMMARY

[0005] An exemplary embodiment of the present invention may provide a method of manufacturing a photovoltaic device capable of improving photoelectric conversion efficiency.

[0006] In accordance with an exemplary embodiment of the present invention, a method of manufacturing a photovoltaic device is provided. The method includes preparing a semiconductor substrate having a light incidence surface receiving light and including single crystalline silicon, wet-etching the light incidence surface to

form a plurality of first protrusions on the light incidence surface, dry etching a plurality of surfaces of the plurality of first protrusions to form a plurality of second protrusions on the plurality of surfaces of the first protrusion, and forming a semiconductor layer on the light incidence surface. The method further includes forming a first electrode on the semiconductor layer and forming a second electrode on a rear surface of the semiconductor substrate facing the light incidence surface.

[0007] Accordingly, a light introduced into the semiconductor substrate from an exterior through the light incidence surface may be scattered on the light incidence surface by the plurality of first and second protrusions, so that an optical path of the light is lengthened in the semiconductor substrate, thereby improving photoelectric conversion efficiency. As a result, as optical energy is more smoothly absorbed into the semiconductor substrate, the photoelectric conversion efficiency of the photovoltaic device can be improved.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] Exemplary embodiments of the present invention can be understood in more detail from the following description when considered in conjunction with the accompanying drawings wherein:

FIG. 1 is a sectional view showing an exemplary embodiment of a photovoltaic device according to an exemplary embodiment of the present invention; FIG. 2A is an enlarged view of first protrusions shown in FIG. 1;

FIG. 2B is an enlarged view of a portion of a sectional surface of the photovoltaic device shown in FIG. 1; FIG. 3 is a sectional view showing an exemplary embodiment of a photovoltaic device according to the present invention;

FIGS. 4A and 5A are sectional views illustrating an exemplary embodiment of a method of manufacturing the photovoltaic device shown in FIG. 3;

FIG. 4B is a photograph showing a light incidence surface of a semiconductor substrate in the manufacturing step of the photovoltaic device shown in FIG. 4A;

FIG. 5B is a photograph showing a light incidence surface of a semiconductor substrate in the manufacturing step of the photovoltaic device shown in FIG. 5A;

FIGS. 6A to 6C are photographs showing a light incidence surface of a semiconductor substrate according to types of etchant gas used for a dry-etching process; and

FIG. 7 is a graph representing reflective indexes of a semiconductor substrate.

DESCRIPTION OF THE EXEMPLARY EMBODIMENTS OF THE INVENTION

[0009] Hereinafter, exemplary embodiments of the present invention will be described in detail with reference to accompanying drawings. It is understood that the present invention should not be limited to the following exemplary embodiments but various changes and modifications can be made by one ordinary skilled in the art within the spirit and scope of the present invention. The present invention is defined only by the scope of the appended claims. Meanwhile, elements shown in the drawings can be simplified or magnified for the purpose of clear explanation. In addition, the same reference numerals are used to designate the same elements throughout the drawings.

[0010] FIG. 1 is a sectional view showing an exemplary embodiment of a photovoltaic device according to the present invention.

[0011] Referring to FIG. 1, a photovoltaic device 500 includes a semiconductor substrate 100, a semiconductor layer 110, a first electrode 120, and a second electrode 130.

[0012] The semiconductor substrate 100 includes single crystalline silicon, and is formed by doping a 5-group element such as, for example, phosphorus (P) into a silicon wafer, so that the semiconductor substrate 100 has an electric characteristic of an N-type semiconductor. In addition, the semiconductor substrate 100 has a light incidence surface 101 receiving light from an exterior. When the semiconductor substrate 100 receives light from an exterior through the light incidence surface 101, photovoltaic effect may be induced. Through the photovoltaic effect, electrons are created in the semiconductor substrate 100, and emitted to an exterior through the first electrode 120 or the second electrode 130.

[0013] The light incidence surface 101 includes first protrusions 105. The first protrusions 105 have a pyramid shape, and have a triangular shape when viewed in a sectional view. The first protrusions 105 may scatter light introduced into the semiconductor substrate 100 from an exterior through the light incidence surface 101 to lengthen an optical path of the light in the semiconductor substrate 100.

[0014] For example, when a first light 10 and a second light 11 reach the light incidence surface 101 from an exterior perpendicularly to the semiconductor substrate 100, if the direction of a first optical path L1 of a first light 10 is not changed on the light incidence surface 101, but the direction of a second optical path L2 of a second light 11 is changed on the light incidence surface 101, the second optical path L2 of the second light 11 may be longer than the first optical path L1 of the first light 10. This is because the direction of the second optical path L2 of the second light 11 is inclined with respect to the semiconductor substrate 100 due to one of the first protrusions 105 differently from the direction of the first optical path L1 of the first light 10 that is perpendicular to

the semiconductor substrate 100.

[0015] If a thickness of the semiconductor substrate 100 increases, a short circuit current density of the photovoltaic device 500 may increase, so that the photoelectric conversion efficiency of the photovoltaic device 500 can be improved. Similarly, if an optical path is lengthened in the semiconductor substrate 100, optical energy may be more smoothly absorbed into the semiconductor substrate 100, and thus the photoelectric conversion efficiency of the photovoltaic device 500 can be improved.

[0016] Second protrusions 108 are provided on the surface of the first protrusions 105. The second protrusions 108 may randomly protrude from the surface of the first protrusions 105. The second protrusions 108 have the same function as that of the first protrusions 105. In other words, the second protrusions 108 may scatter light received introduced into the semiconductor substrate 100 from an exterior through the light incidence surface 101. Accordingly, the light introduced into the semiconductor substrate 100 from an exterior through the light incidence surface 101 can be more dispersed by the second protrusions 108 provided on the surface of the first protrusions 105, so that the photoelectric conversion efficiency of the photovoltaic device 500 can be more improved.

[0017] The semiconductor layer 110 is provided above the semiconductor substrate 100. The semiconductor layer 110 includes non-single crystalline silicon such as, for example, amorphous silicon (a-Si) or microcrystalline silicon (μ c-Si). In addition, the semiconductor layer 110 is doped with a 3-group element such as, for example, boron (B) to have an electric characteristic of a P-type semiconductor. Accordingly, the semiconductor layer 110 makes P-N junction with the semiconductor substrate 100 having an electric characteristic of an N-type semiconductor. In addition, to increase photoelectric conversion efficiency, an intrinsic non-single crystalline silicon layer having a thin thickness of, for example, about 20Å to about 100Å may be interposed between the semiconductor substrate 100 having an N-type semiconductor characteristic and the semiconductor layer 110 having a P-type semiconductor characteristic. The structure of a photovoltaic device, in which an intrinsic non-single crystalline silicon layer is interposed between the semiconductor substrate 100 and the semiconductor layer 110, will be described in more detail with reference to FIG. 3.

[0018] The first electrode 120 is provided on the semiconductor layer 110. The first electrode 120 includes a transparent conductive material such as, for example, indium tin oxide (ITO), indium zinc oxide (IZO), zinc oxide (ZnO), or tin oxide (SnO₂) such that external light can smoothly reach the semiconductor layer 110 and the semiconductor substrate 100.

[0019] The second electrode 130 is provided on a rear surface of the semiconductor substrate 100. The second electrode 130 may include metal, such as, for example,

aluminum (Al) or silver (Ag), having high reflectance. The second electrode 130 may include the same material as that of the first electrode 120. Electrons, which are created from the semiconductor substrate 100 and the semiconductor layer 110 due to photovoltaic effect, may be emitted to an exterior through the first and second electrodes 120 and 130.

[0020] Meanwhile, the photovoltaic device 500 may further include an N+ non-single crystalline silicon layer, which is interposed between the semiconductor substrate 100 and the second electrode 130, and an intrinsic non-single crystalline silicon layer, which is interposed between the semiconductor substrate 100 and the N+ non-single crystalline silicon layer. The N+ non-single crystalline silicon layer serves as a back surface field (BSF) to improve collection of electrons. A photovoltaic device further including the N+ non-single crystalline silicon layer and the intrinsic non-single crystalline silicon layer will be described in more detail with reference to FIG. 3.

[0021] FIG. 2A is an enlarged view of the first protrusions 105 shown in FIG. 1, and FIG. 2B is an enlarged view of a portion of a sectional surface of the photovoltaic device 500 shown in FIG. 1.

[0022] Referring to FIGS. 2A and 2B, the first protrusions 105 have a pyramid shape. This is because the etching rate of the semiconductor substrate 100 including single crystalline silicon is higher in a <100> direction than in a <111> direction.

[0023] The second protrusions 108 are provided on the surface of the first protrusions 105. The size of the first protrusions 105 is greater than that of the second protrusion 108. For example, when comparing the size of the first protrusions 105 with the size of the second protrusions 108 by using parameters (e.g., height, width, and length) capable of determining the size of a protrusion in general, the size of the first protrusions 105 is greater than that of the second protrusions 108.

[0024] A ratio of a first height H1 of the first protrusions 105 to a second height H2 of the second protrusion 108 is in the range of, for example, about 20:1 to about 200:1. For example, the first height H1 is in the range of about 2 μm to about 7 μm, and the second height H2 is in the range of about 50 nm to about 100 nm.

[0025] Meanwhile, when light is supplied to the semiconductor substrate 100 through the light incidence surface 101, a reflective index of the light is reduced on the light incidence surface 101 due to the first and second protrusions 105 and 108. As the reflective index of the light is reduced on the light incidence surface 101, quantity of absorbed light used to induce photovoltaic effect may increase in the semiconductor substrate 100, so that the photoelectric conversion efficiency of the photovoltaic device 500 (see FIG. 1) may increase. This will be described in more detail with reference to FIG. 7.

[0026] FIG. 3 is a sectional view showing another exemplary embodiment of a photovoltaic device according to the present invention. In FIG. 3, the same reference

numerals denote the same elements in FIG. 1, and thus detailed descriptions of the same elements will be omitted.

[0027] Referring to FIG. 3, a photovoltaic device 501 further includes a first intrinsic non-single crystalline silicon layer 115, a second intrinsic non-single crystalline silicon layer 116, and a silicon layer 119 including heavily doped impurities, as compared with the photovoltaic device 500 (see FIG. 1) according to the previous embodiment of the present invention.

[0028] The first intrinsic non-single crystalline silicon layer 115 includes intrinsic non-single crystalline silicon such as, for example, amorphous silicon (a-Si) or microcrystalline silicon (μc-Si), and may have a thickness of, for example, about 20 Å to about 100 Å. The first intrinsic non-single crystalline silicon layer 115 is interposed between the semiconductor substrate 100 and the semiconductor layer 110 to increase photoelectric conversion efficiency of the photovoltaic device 501 and to reduce contact resistance between the semiconductor substrate 100 and the semiconductor layer 110.

[0029] The silicon layer 119 including heavily doped impurities is interposed between the second intrinsic non-single crystalline silicon layer 116 and the second electrode 130. When the semiconductor substrate 100 and the semiconductor layer 110 have N-type and P-type semiconductor characteristics, respectively, the silicon layer 119 including heavily doped impurities includes silicon (such as, for example, N+ non-single crystalline silicon) with impurity concentration greater than that of the semiconductor substrate 100, so that electrons created due to photovoltaic effect are more smoothly emitted to an exterior through the second electrode 130.

[0030] The second intrinsic non-single crystalline silicon layer 116 includes intrinsic non-single crystalline silicon such as, for example, amorphous silicon (a-Si) or microcrystalline silicon (μc-Si). The second intrinsic non-single crystalline silicon layer 116 is formed on a rear surface 104 of the semiconductor substrate 100 to reduce contact resistance between the semiconductor substrate 100 and the silicon layer 119 including heavily doped impurities.

[0031] Meanwhile, third protrusions 106 are provided on the rear surface 104, and fourth protrusions 109 are provided on the surface of the third protrusions 106. The third protrusions 106 may have the same shape as that of the first protrusions 105, and the fourth protrusions 109 may have the same shape as that of the second protrusions 108. In addition, similarly to the first and second protrusions 105 and 108, the third and fourth protrusions 106 and 109 increase an optical path in the semiconductor substrate 100 to raise photoelectric conversion efficiency of the photovoltaic device 501.

[0032] For example, when the second electrode 130 includes a material (e.g., aluminum (Al) or silver (Ag)) reflecting light according to the present exemplary embodiments, light, which is incident through the light incidence surface 101, but not absorbed in the semiconduc-

tor substrate 100, is reflected on the second electrode 130. The light reflected on the second electrode 130 is again scattered by the third and fourth protrusions 106 and 109. Accordingly, an optical path of the light may be increased in the semiconductor substrate 100, so that photoelectric conversion efficiency of the photovoltaic device 501 can be improved.

[0033] FIGS. 4A and 5A are sectional views illustrating an exemplary embodiment of a method of manufacturing the photovoltaic device 501 shown in FIG. 3, and FIGS. 4B and 5B are photographs showing the light incidence surface 101 of the semiconductor substrate 100 in the manufacturing step of the photovoltaic device 501 of FIGS. 4A and 5A. For example, FIG. 4A is a sectional view showing a process of wet-etching the semiconductor substrate 100, and FIG. 4B is a photograph showing the light incidence surface 101 of the semiconductor substrate 100 after the semiconductor substrate 100 is wet-etched. In addition, FIG. 5A is a sectional view showing a process of dry-etching the semiconductor substrate 100, and FIG. 5B is a photograph showing the light incidence surface 101 of the semiconductor substrate 100 after the semiconductor substrate 100 is dry-etched.

[0034] Referring to FIGS. 4A and 4B, the semiconductor substrate 100 having the light incidence surface 101 is wet-etched, so that the first protrusions 105 are formed on the light incidence surface 101. In the present exemplary embodiment, the semiconductor substrate 100 is immersed into a vessel receiving etchant solution such that the semiconductor substrate 100 is etched. As a result, the light incidence surface 101 and the rear surface 104 of the semiconductor substrate 100 facing the light incidence surface 101 are etched by the etchant solution. Accordingly, the third protrusions 106 having the same shape as that of the first protrusions 105 are formed on the rear surface 104.

[0035] The etchant solution used to wet-etch the semiconductor substrate 100 may include, for example, an alkaline solution. In more detail, the etchant solution may include, for example, potassium hydroxide (KOH) and isopropyl alcohol (IPA). When the etchant solution includes potassium hydroxide (KOH), as the potassium hydroxide (KOH) provides an etching rate for the semiconductor substrate 100 slower than an etching rate provided by another etchant solution (e.g., sodium hydroxide (NaOH)), the first protrusions 105, which are formed by etching the light incidence surface 101, can have a more uniform size. In addition, when the etchant solution includes the potassium hydroxide (KOH), even if potassium ions (K⁺) remain on the surface of the semiconductor substrate 100 after the semiconductor substrate 100 is wet-etched, the potassium ions (K⁺) are less bonded with electrons when compared to other ions (e.g., sodium ions (Na⁺)). Accordingly, if the etchant solution includes potassium hydroxide (KOH), positive ions generated from the etchant solution are bonded with electrons created due to the photovoltaic effect, so that the reduction of quantity of current in the photovoltaic device 501 can be

minimized.

[0036] Meanwhile, according to the present exemplary embodiment, although the semiconductor substrate 100 is etched by immersing the semiconductor substrate 100 into etchant solution to form the first protrusions 105, the semiconductor substrate 100 may be etched by spraying the etchant solution to the semiconductor substrate 100.

[0037] Referring to FIGS. 5A and 5B, the semiconductor substrate 100 including the first and third protrusions 105 and 106 is dry-etched. Accordingly, the second protrusions 108 are formed on the surface of the first protrusions 105, and the fourth protrusions 109 are formed on the surface of the third protrusions 106.

[0038] The dry-etching is performed by using, for example, a gas mixture of first gas including fluorine (F) and second gas including chlorine (Cl). In more detail, the first gas may include, for example, sulfur hexafluoride (SF₆), and the second gas may include, for example, chlorine gas (Cl₂). In the mixed gas, the flow rate ratio of the first gas and the second gas is, for example, about 1: 1 to about 3:1. In more detail, preferably, the flow rate ratio of the first gas and the second gas is, for example, about 1: 1. The reason to employ the flow rate ratio of about 1:1 will be described with reference to FIGS. 6A to 6C.

[0039] Meanwhile, when the second protrusions 108 are formed by dry-etching the semiconductor substrate 100, edges of the first protrusions 105 are rounded by the second protrusions 108 as shown in FIG. 5B. Accordingly, if the second protrusions 108 are formed on the first protrusions 105, thin films formed on the first protrusions 105 are prevented from being cut by sharp edges of inclined surfaces defining the first protrusions 105 in a region at which the inclined surfaces meet each other.

[0040] FIGS. 6A to 6C are photographs showing the light incidence surface 101 (see FIG. 5A) of the semiconductor substrate 100 according to types of etchant gas used for the dry-etching. In more detail, FIG. 6A is a photograph showing a state of the light incidence surface 101 after etching the light incidence surface 101 by applying, for example, chlorine gas (Cl₂) into a plasma dry etching device, which is supplied with RF power of about 2000W under an internal pressure of about 100mT, at a flow rate of about 200 sccm, in which "sccm" represents standard cubic centimeters per minute. FIG. 6B is a photograph showing a state of the light incidence surface 101 after etching the light incidence surface 101 by applying, for example, sulfur hexafluoride (SF₆) into the plasma dry etching device, which is supplied with RF power of about 2000W under an internal pressure of about 100mT, at a flow rate of 200 sccm. FIG. 6C is a photograph showing a state of the light incidence surface 101 after etching the light incidence surface 101 by applying, for example, chlorine gas (Cl₂) and sulfur hexafluoride (SF₆) into the plasma dry etching device, which is supplied with RF power of about 2000W under an internal pressure of about 100mT, at a flow rate of about 200 sccm.

[0041] Referring to FIG. 6A, when the semiconductor substrate 100 is dry-etched by using, for example, only chlorine gas (Cl_2), the second protrusions 108 are rarely formed on the light incidence surface 101 of the semiconductor substrate 100. Referring to FIGS. 6B and 6C, the second protrusions 108 are formed on the light incidence surface 101. However, the number of the second protrusions 108 per unit area shown in FIG. 6C is greater than the number of the second protrusions 108 per unit area shown in FIG. 6B. In other words, when the semiconductor substrate 100 is dry-etched by using, for example, gas obtained by mixing chlorine gas (Cl_2) and sulfur hexafluoride (SF_6) at the same flow rate, the texturing effect for the light incidence surface 101 may be maximized.

[0042] Referring again to FIGS. 5A and 5B, when the semiconductor substrate 100 is dry-etched to form the second and fourth protrusions 108 and 109, the dry-etching is preferably performed for, example, about 15 seconds to about 120 seconds, in more detail, about 30 seconds. This is because the semiconductor substrate 100 should be subjected to the dry-etching process for at least 15 seconds by taking stabilization time of plasma into consideration. In addition, when the semiconductor substrate 100 is dry-etched for more than about 120 seconds, even if light absorbance of the semiconductor substrate 100 increases with respect to light having a wavelength of about 1000nm or more, the light absorbance of the semiconductor substrate 100 may be reduced with respect to light having a wavelength of about 400nm to about 1000nm, so that the light absorbance is rarely increased over the whole wavelength band of light.

[0043] Meanwhile, before the second and fourth protrusions 108 and 109 are formed by dry-etching the semiconductor substrate 100, an oxide layer, which is formed on the semiconductor substrate 100 after the first and third protrusions 105 and 106 are formed, is removed from the surface of the semiconductor substrate 100. The oxide layer may include, for example, silicon oxide (SiO_x) formed by combining external oxygen (O) with silicon (Si) of the semiconductor substrate 100. The oxide layer may be etched by using, for example, boron trichloride (BCl_3) or a gas mixture of boron trichloride (BCl_3) and chlorine gas (Cl_2).

[0044] Referring again to FIG. 3, the first intrinsic non-single crystalline silicon layer 115 is formed on the light incidence surface 101 of the semiconductor substrate 100, the semiconductor layer 110 having a P-type semiconductor characteristic is formed on the first intrinsic non-single crystalline silicon layer 115, and the first electrode 120 is formed on the semiconductor layer 110. In addition, the second intrinsic non-single crystalline silicon layer 116 is formed on the rear surface 104 of the semiconductor substrate 100, the silicon layer 119 including heavily doped impurities is formed on the second intrinsic non-single crystalline silicon layer 116, and the second electrode 130 is formed on the silicon layer 119 including heavily doped impurities, thereby manufactur-

ing the photovoltaic device 501.

[0045] FIG. 7 shows first to third curves G1, G2, and G3 representing reflective indexes of the semiconductor substrate 100. In more detail, FIG. 7 shows the first to third curves G1, G2, and G3 showing the reflective indexes of the semiconductor substrate 100 obtained from experiment according to three states of the light incidence surface 101 of the semiconductor substrate 100.

[0046] Referring to FIG. 7, the reflective indexes of the semiconductor substrate 100 (see FIG. 1) according to wavelengths of light are classified according to three states of the light incidence surface 101 (see FIG. 1) of the semiconductor substrate 100 (see FIG. 1). For the convenience of the explanation, the three states are classified into first to third surface states. The first to third curves G1 to G3 represent reflective indexes of the semiconductor substrate 100 having the first to third surface states, respectively.

[0047] The first surface state represents a flat surface of the light incidence surface 101 when the light incidence surface 101 is not subject to any etching processes. The second surface state represents a state of the light incidence surface 101 when the light incidence surface 101 is wet-etched to form the first protrusions 105 (see FIG. 4A) on the light incidence surface 101. The third surface state represents a state of the light incidence surface 101 when the light incidence surface 101 is wet-etched and dry-etched, so that the first protrusions 105 are formed on the light incidence surface 101, and the second protrusions 108 (see FIG. 5B) are formed on the surface of the first protrusions 105.

[0048] Referring to the first to third curves G1 to G3, the reflective index of the semiconductor substrate 100 having the second surface state is lower than the reflective index of the semiconductor substrate 100 having the first surface state over the whole wavelength region of light. In addition, the reflective index of the semiconductor substrate 100 having the third surface state is lower than the reflective index of the semiconductor substrate 100 having the second surface state over the whole wavelength region of the light. In particular, regarding light having wavelengths in the range of about 250nm to about 400nm and the range of about 900nm to about 1100nm, the reflective index of the semiconductor substrate 100 having the third surface state is significantly lower than the reflective index of the semiconductor substrate 100 having the second surface state. In other words, when the second protrusions 108 (see FIG. 5B) are additionally formed by dry-etching the semiconductor substrate 100 after the first protrusions 105 (see FIG. 4) are formed by wet-etching the semiconductor substrate 100, the semiconductor substrate 100 can absorb much more of the light in a specific wavelength band.

[0049] Having described the exemplary embodiments of the present invention, it is further noted that it is readily apparent to those of reasonable skill in the art that various modifications may be made without departing from the spirit and scope of the invention which is defined by the

metes and bounds of the appended claims.

Claims

1. A method of manufacturing a photovoltaic device, the method comprising:

preparing a semiconductor substrate having a light incidence surface receiving a light, and including single crystalline silicon;
wet-etching the light incidence surface to form a plurality of first protrusions on the light incidence surface;
dry-etching a plurality of surfaces of the plurality of first protrusions to form a plurality of second protrusions on the plurality of surfaces of the plurality of first protrusions;
forming a semiconductor layer on the light incidence surface;
forming a first electrode on the semiconductor layer; and
forming a second electrode on a rear surface of the semiconductor substrate facing the light incidence surface.

2. The method of claim 1, wherein a height ratio of the plurality of first protrusions to the plurality of second protrusions is in a range of about 20:1 to about 200:1.

3. The method of claim 2, wherein a height of the plurality of first protrusions is in a range of about 2 μ m to about 7 μ m.

4. The method of claim 3, wherein a height of the plurality of second protrusions are in a range of about 50nm to about 100nm.

5. The method of claim 1, wherein an etchant used for the wet-etching comprises potassium hydroxide (KOH).

6. The method of claim 1, further comprising:

forming a plurality of third protrusions on a rear surface of the semiconductor substrate, wherein the plurality of third protrusions have a same shape as a shape of the plurality of first protrusions; and
dry-etching the surfaces of the plurality of third protrusions to form a plurality of fourth protrusions on the plurality of surfaces of the plurality of third protrusions,

wherein the plurality of third protrusions are formed together with the plurality of first protrusions.

7. The method of claim 1, wherein an etchant used for the dry-etching comprises a gas mixture of a first gas comprising fluorine (F) and a second gas comprising chlorine (Cl).

8. The method of claim 7, wherein the first gas comprises sulfur hexafluoride (SF₆), and the second gas comprises chlorine (Cl).

9. The method of claim 8, wherein a flow rate ratio of the first gas to the second gas is in a range of about 1:1 to about 3:1.

10. The method of claim 9, wherein the dry-etching is performed for about 15 seconds to 120 seconds.

11. The method of claim 1, wherein the semiconductor layer comprises non-single crystalline silicon, and is formed through a chemical vapor deposition scheme.

12. The method of claim 1, wherein the semiconductor substrate is an N-type semiconductor, and the semiconductor layer is a P-type semiconductor.

13. The method of claim 1, further comprising:

forming a first intrinsic non-single crystalline silicon layer between the semiconductor substrate and the semiconductor layer;
forming a second intrinsic non-single crystalline silicon layer between the semiconductor substrate and the second electrode; and
forming a silicon layer comprising heavily doped impurities between the second intrinsic non-single crystalline silicon layer and the second electrode, the silicon layer having an impurity concentration greater than an impurity concentration of the semiconductor substrate.

14. The method of claim 1, further comprising removing an oxide layer formed on the semiconductor substrate by using an etchant comprising one of boron trichloride (BCl₃) or a gas mixture of boron trichloride (BCl₃) and chlorine gas (Cl₂), before the dry-etching is performed.

Fig. 1

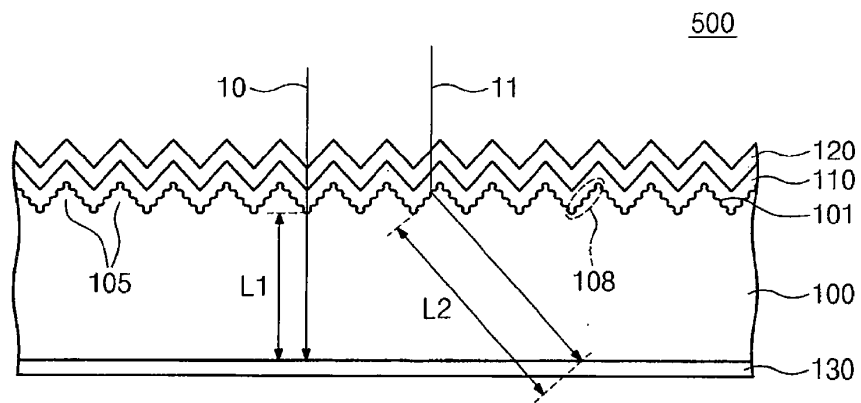


Fig. 2A

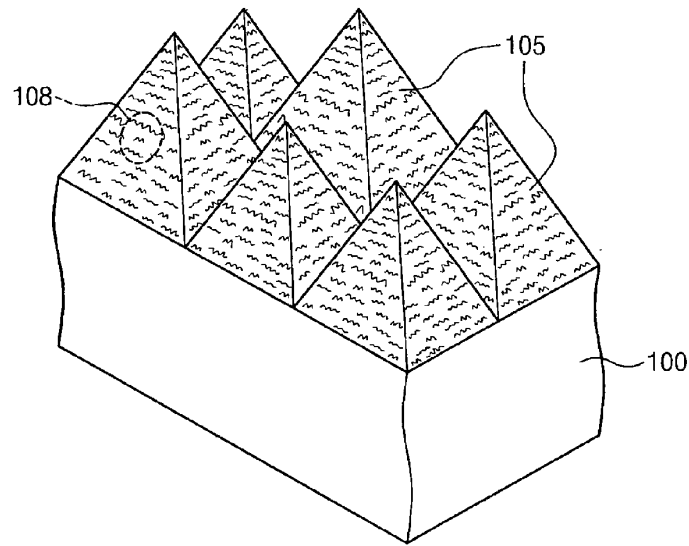


Fig. 2B

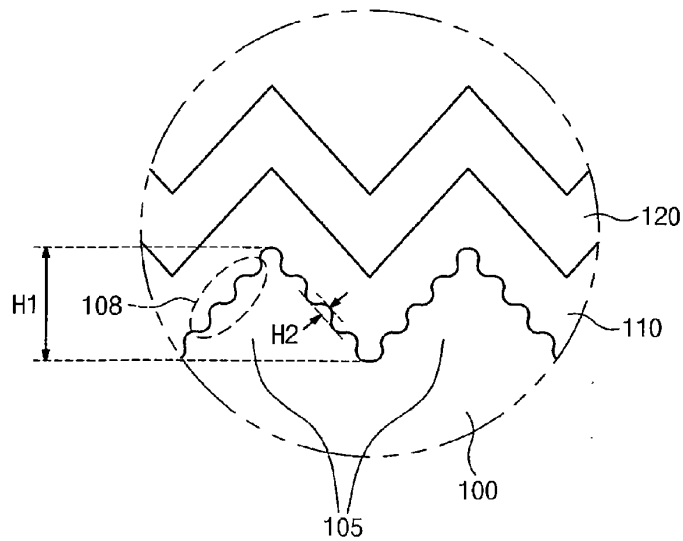


Fig. 3

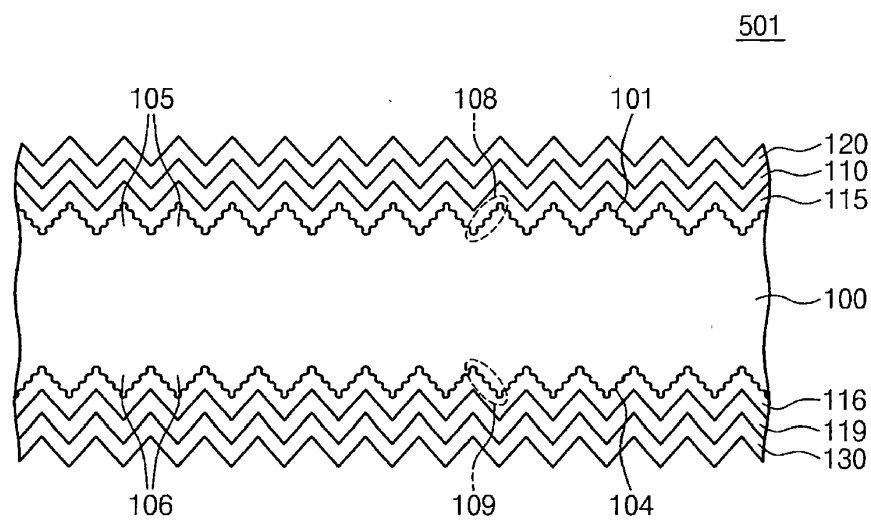


Fig. 4A

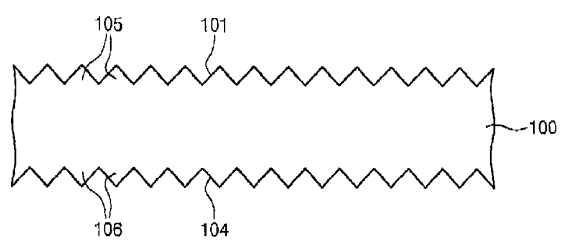


Fig. 4B

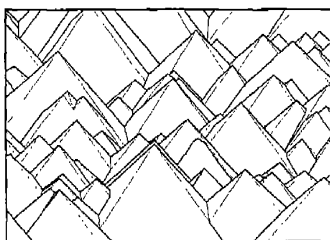


Fig. 5A

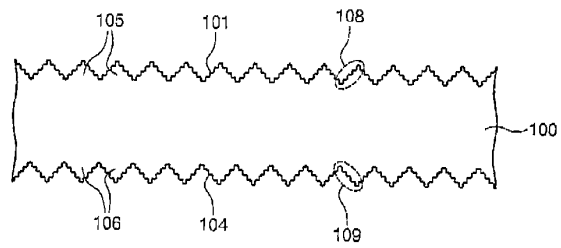


Fig. 5B

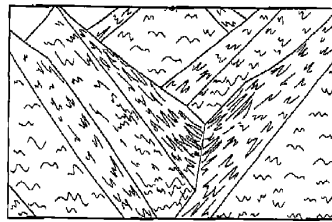


Fig. 6A

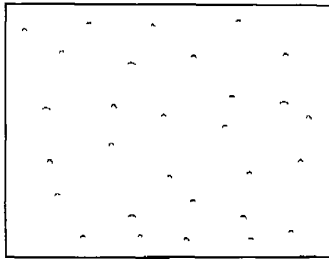


Fig. 6B

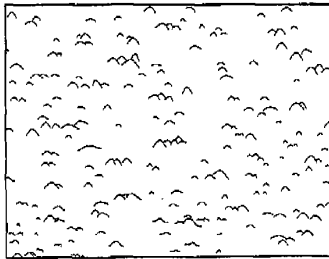


Fig. 6C

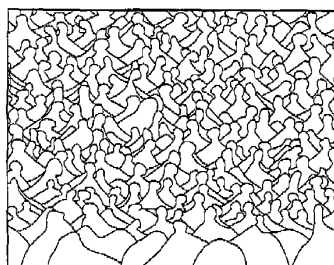
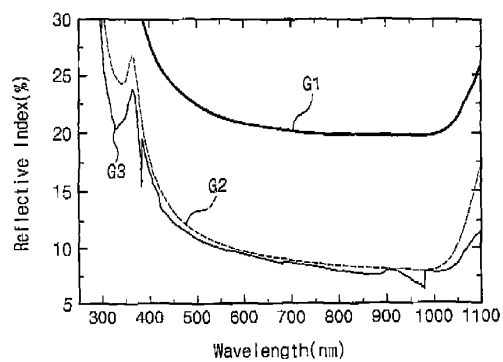


Fig. 7



EP 2 149 915 A2

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(11) **EP 2 149 915 A3**

(12) **EUROPEAN PATENT APPLICATION**

(88) Date of publication A3:
31.10.2012 Bulletin 2012/44

(51) Int Cl.:
H01L 31/18 (2006.01) H01L 31/0236 (2006.01)

(43) Date of publication A2:
03.02.2010 Bulletin 2010/05

(21) Application number: **09004691.3**

(22) Date of filing: **31.03.2009**

(84) Designated Contracting States:
**AT BE BG CH CY CZ DE DK EE ES FI FR GB GR
HR HU IE IS IT LI LT LU LV MC MK MT NL NO PL
PT RO SE SI SK TR**
Designated Extension States:
AL BA RS

(30) Priority: **31.07.2008 KR 20080075261**

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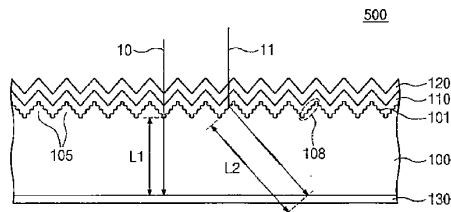
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(54) **Method of manufacturing photovoltaic device**

(57) A method of manufacturing a photovoltaic device includes preparing a semiconductor substrate having a light incidence surface receiving light and including single crystalline silicon, wet-etching the light incidence surface to form a plurality of first protrusions on the light incidence surface, dry etching a plurality of surfaces of

the first protrusions to form a plurality of second protrusions on the plurality of surfaces of the first protrusions, and forming a semiconductor layer on the light incidence surface. The method further includes forming a first electrode on the semiconductor layer and forming a second electrode on a rear surface of the semiconductor substrate facing the light incidence surface.

Fig. 1



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EP 2 149 915 A3



EUROPEAN SEARCH REPORT

 Application Number
EP 09 00 4691

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			TECHNICAL FIELDS SEARCHED (IPC)
			H01L
1 The present search report has been drawn up for all claims			
Place of search Berlin		Date of completion of the search 19 September 2012	Examiner Persat, Nathalie
CATEGORY OF CITED DOCUMENTS X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document			

EPO FORM 1503 (03.02.2004) (POMC01)

EP 2 149 915 A3

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ON EUROPEAN PATENT APPLICATION NO.

EP 09 00 4691

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(11) **EP 2 645 421 A1**

(12) **EUROPEAN PATENT APPLICATION**

(43) Date of publication:
02.10.2013 Bulletin 2013/40

(51) Int CL:
H01L 31/0236^(2006.01) H01L 31/0216^(2006.01)
H01L 31/068^(2012.01)

(21) Application number: **12006262.5**

(22) Date of filing: **05.09.2012**

(84) Designated Contracting States:
AL AT BE BG CH CY CZ DE DK EE ES FI FR GB
GR HR HU IE IS IT LI LT LU LV MC MK MT NL NO
PL PT RO RS SE SI SK SM TR
Designated Extension States:
BA ME

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(30) Priority: **28.03.2012 KR 20120031644**

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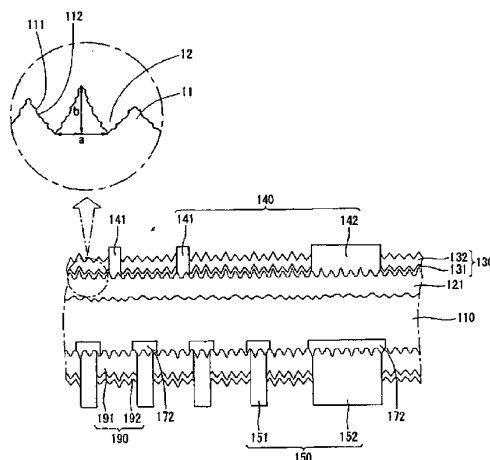
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(54) **Solar cell and method for manufacturing the same**

(57) A solar cell and a method for manufacturing the same are discussed. The solar cell includes a substrate formed of an n-type crystalline semiconductor (110), an emitter region (121) of a p-type positioned at a first surface of the substrate, a first dielectric layer (191) positioned on a second surface opposite the first surface of the substrate, second dielectric layers (131, 192) respectively positioned on the emitter region (121) and the first dielectric layer (191), a third dielectric layer (132) posi-

tioned on the second dielectric layer (131) that is positioned on the emitter region, a first electrode (140) which is positioned on the first surface of the substrate and is connected to the emitter region, and a second electrode (150) which is positioned on the second surface of the substrate and is connected to the substrate. The emitter region (121) has a first textured surface including a plurality of first protrusions (11, 12), each of said first protrusions having a textured surface including a plurality of second protrusions (111, 112).

FIG. 2



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EP 2 645 421 A1

Description

BACKGROUND OF THE INVENTION

Field of the Invention

[0001] Embodiments of the invention relate to a solar cell and a method for manufacturing the same.

Description of the Related Art

[0002] Recently, as existing energy sources such as petroleum and coal are expected to be depleted, interests in alternative energy sources for replacing the existing energy sources are increasing. Among the alternative energy sources, solar cells for generating electric energy from solar energy have been particularly spotlighted.

[0003] A solar cell generally includes semiconductor parts, for example, a substrate and an emitter region, which respectively have different conductive types, for example, a p-type and an n-type and thus form a p-n junction, and electrodes respectively connected to the semiconductor parts of the different conductive types.

[0004] When light is incident on the solar cell, electrons inside the semiconductor parts become free electrons (hereinafter referred to as 'electrons') by the photoelectric effect. Further, electrons and holes respectively move to the n-type semiconductor (e.g., the emitter region) and the p-type semiconductor (e.g., the substrate) under the influence of the p-n junction of the semiconductor parts. The electrons moving to the emitter region and the holes moving to the substrate are respectively collected by the respective electrodes electrically connected to the emitter region and the substrate. The electrodes are connected to each other using electric wires to thereby obtain electric power.

SUMMARY OF THE INVENTION

[0005] In one aspect, there is a solar cell including a substrate formed of an n-type crystalline semiconductor, an emitter region of a p-type positioned at a first surface of the substrate, a first dielectric layer positioned on a second surface opposite the first surface of the substrate, second dielectric layers respectively positioned on the emitter region and the first dielectric layer, a third dielectric layer positioned on the second dielectric layer that is positioned on the emitter region, a first electrode which is positioned on the first surface of the substrate and is connected to the emitter region, and a second electrode which is positioned on the second surface of the substrate and is connected to the substrate, wherein the emitter region has a first textured surface including a plurality of first protrusions each having a protruding height and a maximum diameter which are within a range of about 5 μm to 10 μm , and wherein each of the plurality of first protrusions has a second textured surface including a plurality of second protrusions each having a protruding

height and a maximum diameter which are within a range of about 300 nm to 600 nm.

[0006] The first dielectric layer and the third dielectric layer may be formed of hydrogenated silicon nitride. The second dielectric layer may be formed of aluminum oxide.

[0007] The second dielectric layer may have a thickness of about 5 nm to 15 nm.

[0008] Each of the first dielectric layer and the third dielectric layer may have a thickness of about 70 nm to 100 nm.

[0009] The solar cell may further include a hydrogenated silicon oxide layer positioned between the first dielectric layer and the third dielectric layer. The hydrogenated silicon oxide layer may have a thickness of about 50 nm to 100 nm.

[0010] The solar cell may further include a silicon oxide layer positioned between the second surface of the substrate and the first dielectric layer. The silicon oxide layer may have a thickness of about 2 nm to 3 nm.

[0011] The first surface and the second surface of the substrate may be incident surfaces on which light is incident.

[0012] The solar cell may further include a hydrogenated silicon oxide layer positioned on the second dielectric layer that is positioned on the first dielectric layer. The hydrogenated silicon oxide layer may have a thickness of about 50 nm to 100 nm.

[0013] The solar cell may further include a silicon oxide layer positioned between the emitter region and the second dielectric layer. The silicon oxide layer may have a thickness of about 2 nm to 3 nm.

[0014] Acicular ends of the plurality of second protrusions may point in a parallel direction as vertices of the plurality of first protrusions.

[0015] Each of the plurality of second protrusions may have an acicular end, and acicular ends of adjacent second protrusions may be connected by serrated edges.

[0016] According to the above-described characteristics of the solar cell, because the surface of the substrate has the first and second textured surfaces, an amount of light incident on the substrate increases. Hence, the efficiency of the solar cell is improved.

[0017] Furthermore, because an anti-reflection layer including the plurality of dielectric layers and a passivation layer including the plurality of dielectric layers are respectively formed on a front surface and a back surface of the substrate, a reflection amount of light decreases. Hence, a surface passivation effect is generated at the surface of the substrate, and the efficiency of the solar cell is further improved.

[0018] Furthermore, because a field passivation effect is obtained by stacking a layer having negative fixed charges on the n-type substrate, a loss amount of carriers of the solar cell decreases.

[0019] In addition, because the problem resulting from a natural oxide layer is reduced by thinly coating the silicon oxide layer on at least one of the front surface and

the back surface of the substrate, the efficiency of the solar cell is further improved.

[0020] In another aspect, there is a method for manufacturing a solar cell including performing a wet etching process to form a first textured surface on at least one surface of a substrate, performing a dry etching process to form a second textured surface on the first textured surface, and performing an ion implantation process to implant impurity ions into the first textured surface and the second textured surface and performing an activation process to form at least one of an emitter region and a back surface field region.

[0021] The wet etching process may be performed using an alkali solution such as isopropyl alcohol (IPA) or potassium hydroxide (KOH).

[0022] The first textured surface including a plurality of first protrusions and a plurality of first depressions may be formed through the wet etching process using the alkali solution. A protruding height and a diameter of each of the plurality of first protrusions may be within the range of about 5 μm to 10 μm .

[0023] The dry etching process may be performed using a reaction ion etching (RIE) method.

[0024] The second textured surface including a plurality of second protrusions and a plurality of second depressions may be formed through the dry etching process using the reaction ion etching method. A protruding height and a diameter of each of the plurality of second protrusions may be within the range of about 300 nm to 600 nm.

[0025] The method may further include, after forming the second textured surface, performing the dry etching process to remove a remainder of the substrate.

[0026] The first and second textured surfaces may be formed on a first surface of the substrate, and the first and second textured surfaces are formed on a second surface opposite the first surface. In this instance, the emitter region may be formed at the first surface of the substrate, and the back surface field region may be locally formed at the second surface of the substrate.

[0027] In the embodiment of the invention, the local formation of the back surface field region indicates that the back surface field region is formed in the same pattern as the plurality of finger electrodes of the second electrode part at the second surface of the substrate.

[0028] Accordingly, the back surface field region is locally formed at the second surface of the substrate, unlike the emitter region entirely formed at the first surface of the substrate.

[0029] In the embodiment of the invention, the formation of the emitter region at the entire first surface of the substrate indicates that the emitter region is formed at the entire first surface of the substrate except an edge.

[0030] The emitter region may be formed by implanting and activating first impurity ions, and the back surface field region may be formed by implanting and activating second impurity ions of a conductive type opposite the first impurity ions. An activation process of the first im-

purity ions and the second impurity ions may be performed at a temperature of about 1,000 °C to 2,000 °C capable of activating the first impurity ions for about 20 minutes to 60 minutes.

[0031] The method may further include performing the activation process to remove damaged portions of the first and second surfaces of the substrate resulting from the dry etching process.

[0032] The method may further include forming a first dielectric layer on the second surface of the substrate, simultaneously forming second dielectric layers respectively on the emitter region and the first dielectric layer, forming a third dielectric layer on the second dielectric layer that is positioned on the emitter region, and forming a first electrode part, which includes a plurality of finger electrodes and is connected to the emitter region, and a second electrode part, which includes a plurality of finger electrodes and is connected to the back surface field region.

[0033] At least one of the first electrode part and the second electrode part may include at least one bus electrode extending in a direction crossing the finger electrodes.

[0034] Each of the first dielectric layer and the third dielectric layer may be formed by depositing hydrogenated silicon nitride at a thickness of about 70 nm to 100 nm. The second dielectric layer may be formed by depositing aluminum oxide at a thickness of about 5 nm to 15 nm using an atomic layer deposition (ALD) method.

[0035] The method may further include forming a fourth dielectric layer between the first dielectric layer and the second dielectric layer and on the third dielectric layer. The fourth dielectric layer may be formed by depositing hydrogenated silicon oxide at a thickness of about 50 nm to 100 nm.

[0036] The method may further include, before forming the first dielectric layer, forming a fifth dielectric layer on the first and second surfaces of the substrate. The forming of the fifth dielectric layer may include immersing the substrate in a nitric acid solution having a hydrogen ion concentration (pH) of about 2 to 4 for about 5 minutes to 30 minutes to form a silicon oxide layer having a thickness of about 2 nm to 3 nm.

[0037] The back surface field region may be formed in the same pattern as the plurality of finger electrodes of the second electrode part.

BRIEF DESCRIPTION OF THE DRAWINGS

[0038] The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of this specification, illustrate embodiments of the invention and together with the description serve to explain the principles of the invention. In the drawings:

[0039] FIG. 1 is a partial perspective view of a solar cell according to an example embodiment of the invention;

[0040] FIG. 2 is a cross-sectional view taken along line II-II of FIG. 1;

[0041] FIG. 3 illustrates a portion of a substrate of the solar cell shown in FIGS. 1 and 2, on which a wet etching process and a dry etching process are performed;

[0042] FIGS. 4A to 4H sequentially illustrate a method for manufacturing a solar cell according to an example embodiment of the invention;

[0043] FIG. 5 is a partial cross-sectional view of another example of a solar cell according to an example embodiment of the invention; and

[0044] FIGS. 6 and 7 are partial cross-sectional views of other examples of a solar cell according to an example embodiment of the invention.

DETAILED DESCRIPTION OF THE EMBODIMENTS

[0045] Reference will now be made in detail to embodiments of the invention, examples of which are illustrated in the accompanying drawings. This invention may, however, be embodied in many different forms and should not be construed as limited to the embodiments set forth herein. Wherever possible, the same reference numbers will be used throughout the drawings to refer to the same or like parts. It will be paid attention that detailed description of known arts will be omitted if it is determined that the arts can mislead the embodiments of the invention.

[0046] In the drawings, the thickness of layers, films, panels, regions, etc., are exaggerated for clarity. It will be understood that when an element such as a layer, film, region, or substrate is referred to as being "on" another element, it can be directly on the other element or intervening elements may also be present. In contrast, when an element is referred to as being "directly on" another element, there are no intervening elements present.

[0047] Further, it will be understood that when an element such as a layer, film, region, or substrate is referred to as being "entirely" on other element, it may be on the entire surface of the other element and may not be on a portion of an edge of the other element.

[0048] Example embodiments of the invention will be described in detail with reference to FIGS. 1 to 7.

[0049] A solar cell according to an example embodiment of the invention is described in detail with reference to FIGS. 1 and 2.

[0050] As shown in FIGS. 1 and 2, a solar cell according to an example embodiment of the invention includes a substrate 110, an emitter region 121 positioned at a front surface (or a first surface) of the substrate 110, an anti-reflection layer 130 positioned on the emitter region 121, a passivation layer 190 positioned on a back surface (or a second surface) opposite the front surface of the substrate 110, a front electrode part (or a first electrode part) 140 which is positioned on the front surface of the substrate 110, is connected to the emitter region 121, and includes a plurality of front electrodes (or a plurality of first electrodes) 141 and a plurality of front bus bars

(or a plurality of first bus bars) 142, a back electrode part (or a second electrode part) 150 which is positioned on the back surface of the substrate 110 and includes a plurality of back electrodes (or a plurality of second electrodes) 151 and a plurality of back bus bars (or a plurality of second bus bars) 152, and a plurality of back surface field regions 172 positioned under the plurality of back electrodes 151 and the plurality of back bus bars 152 at the back surface of the substrate 110.

[0051] In the embodiment of the invention, light is incident on at least one of the front surface and the back surface of the substrate 110.

[0052] The substrate 110 is a semiconductor substrate formed of a semiconductor such as first conductive type silicon, for example, n-type silicon, though not required. The semiconductor used in the substrate 110 is a crystalline semiconductor, such as single crystal silicon and polycrystalline silicon. The n-type substrate 110 is doped with impurities of a group V element such as phosphorus (P), arsenic (As), and antimony (Sb).

[0053] As shown in FIGS. 1 to 3, a separate texturing process is entirely performed on the flat front surface of the substrate 110 to form a first textured surface corresponding to an uneven surface or having uneven characteristics, and including a plurality of first protrusions 11 and a plurality of first depressions 12. In this instance, the emitter region 121 and the anti-reflection layer 130 positioned on the front surface of the substrate 110 have the textured surface.

[0054] Each of the first protrusions 11 has a pyramid shape or a similar shape.

[0055] In the embodiment of the invention, a diameter (i.e., size) 'a' and a protruding height 'b' of each of the first protrusions 11 may be within the range of several μm , for example, about $5\ \mu\text{m}$ to $10\ \mu\text{m}$. An aspect ratio 'b/a' of each first protrusion 11 may be about 1.0 to 1.5. In the embodiment of the invention, the aspect ratio 'b/a' is obtained by dividing the protruding height 'b' of the first protrusion 11 by the diameter 'a' of the first protrusion 11. The diameter 'a' of the first protrusion 11 is a width of the base of the first protrusion 11.

[0056] Because the plurality of first protrusions 11 are positioned on the front surface of the substrate 110, an incident area of the substrate 110 increases and a light reflectance decreases due to a plurality of reflection operations resulting from each first protrusion 11. Hence, an amount of light incident on the substrate 110 increases, and the efficiency of the solar cell is improved.

[0057] As shown in FIGS. 2 and 3, a plurality of second protrusions 111 and a plurality of second depressions 112 are formed on the surface of each first protrusion 11. Thus, the surface of each first protrusion 11 has a second textured surface corresponding to an uneven surface or having uneven characteristics, and including the plurality of second protrusions 111 and the plurality of second depressions 112.

[0058] A diameter (i.e., size) and a protruding height of each of the second protrusions 111 included in each

first protrusion 11 are less than the diameter (i.e., size) and the protruding height of each first protrusion 11.

[0059] For example, the diameter and the protruding height of each second protrusion 111 may be within the range of several hundreds of nm. For example, each second protrusion 111 may have the maximum diameter and the protruding height of about 300 nm to 600 nm.

[0060] Because the surface of each first protrusion 11 has the second textured surface, the incident area of the substrate 110 further increases. Further, because a reflection operation of light is repeatedly performed, an amount of light incident on the substrate 110 further increases.

[0061] As described above, the surface of the substrate 110 forms the first textured surface having the first protrusions 11 and the first depressions 12, and the surface of each first protrusion 11 forms the second textured surface having the second protrusions 111 and the second depressions 112. Namely, the surface of the substrate 110 has the first and second textured surfaces. Thus, a reflectance (for example, an average weighted reflectance) of light having a wavelength of about 300 nm to 1,100 nm has a small value of about 1 % to 10 %.

[0062] As shown in FIGS. 2 and 3, the first protrusions 11 have a plurality of surfaces that meet at respective vertices that are generally piked. Each of the plurality of surfaces of the first protrusions 11 has a plurality of second protrusions 111 that have acicular ends. Each of the second protrusions 111 are connected to other second protrusions 111 by serrated edges that defined the plurality of depressions 112. The plurality of second protrusions 111 generally point in a parallel direction as the vertices of the plurality of first protrusions 11. The plurality of depressions 112 are also generally hollowed out in the parallel direction as the vertices of the plurality of first protrusions 11.

[0063] In the embodiment of the invention, when the substrate 110 is formed of single crystal silicon, the first textured surface 11(12) may be formed through a wet etching method using an alkali solution such as Isopropyl alcohol (IPA) or potassium hydroxide (KOH), and the second textured surface 111(112) may be formed through a dry etching method such as a reaction ion etching (RIE) method.

[0064] The emitter region 121 positioned at the front surface of the substrate 110 is an impurity region doped with impurities of a second conductive type (for example, p-type) opposite the first conductive type (for example, n-type) of the substrate 110. Thus, the emitter region 121 of the second conductive type forms a p-n junction along with a first conductive type region (for example, an n-type region) of the substrate 110.

[0065] In the embodiment of the invention, the emitter region 121 may have a sheet resistance of about 70 Ω /sq. to 80 Ω /sq.

[0066] Regarding carriers, for example, electrons and holes produced by light incident on the substrate 110, the electrons and the holes respectively move to the n-

type semiconductor and the p-type semiconductor by a built-in potential difference resulting from the p-n junction between the substrate 110 and the emitter region 121. Thus, when the substrate 110 is of the n-type and the emitter region 121 is of the p-type, the electrons and the holes move to the substrate 110 and the emitter region 121, respectively.

[0067] When the emitter region 121 is of the p-type, the emitter region 121 may be formed by doping the substrate 110 with impurities of a group III element such as boron (B), gallium (Ga), and indium (In). In this instance, the emitter region 121 may be formed using an ion implantation method.

[0068] The anti-reflection layer 130 includes a first anti-reflection layer 131 positioned on the emitter region 121 and a second anti-reflection layer 132 positioned on the first anti-reflection layer 131.

[0069] In the embodiment of the invention, the first anti-reflection layer 131 may be formed of aluminum oxide (Al_2O_3), and the second anti-reflection layer 132 may be formed of hydrogenated silicon nitride (SiN_xH).

[0070] The first anti-reflection layer 131 formed of aluminum oxide (Al_2O_3) may have a thickness of about 5 nm to 15 nm and a refractive index of about 1.1 to 1.6. The second anti-reflection layer 132 formed of hydrogenated silicon nitride (SiN_xH) may have a thickness of about 70 nm to 100 nm and a refractive index of about 2.0 to 2.2.

[0071] In this instance, because the refractive index of the first anti-reflection layer 131 adjacent to the substrate 110 is less than the refractive index of the second anti-reflection layer 132 adjacent to air, an anti-reflection effect is reduced by the refractive index of the first anti-reflection layer 131. It is preferable, but not required, that the thickness of the first anti-reflection layer 131 is much less than the thickness of the second anti-reflection layer 132, so as to prevent a reduction in the anti-reflection effect.

[0072] The first anti-reflection layer 131 formed of aluminum oxide (Al_2O_3) is positioned on the front surface of the substrate 110, i.e., directly on the emitter region 121 positioned at the front surface of the substrate 110.

[0073] In general, aluminum oxide (Al_2O_3) has the characteristic of negative fixed charges.

[0074] Thus, positive fixed charges (i.e., holes) are drawn to the p-type emitter region 121 and electrons are pushed to the back surface of the substrate 110 by the first anti-reflection layer 131 formed of aluminum oxide (Al_2O_3) having negative fixed charges. Namely, a field passivation effect is obtained.

[0075] Accordingly, an amount of holes moving to the emitter region 121 further increases by the first anti-reflection layer 131 formed of aluminum oxide (Al_2O_3), and an amount of electrons moving to the emitter region 121 decreases by the first anti-reflection layer 131. Hence, a recombination of electrons and holes at and around the emitter region 121 is reduced.

[0076] Oxygen (O) contained in aluminum oxide

(Al₂O₃) for forming the first anti-reflection layer 131 moves to the surface of the substrate 110 abutting on the first anti-reflection layer 131 to thereby perform a passivation function for converting a defect, for example, dangling bonds existing at and around the surface of the substrate 110 into stable bonds.

[0077] The first anti-reflection layer 131 formed of aluminum oxide (Al₂O₃) may be formed using an atomic layer deposition (ALD) method having an excellent step coverage.

[0078] As described above, the first textured surface 11(12) using the wet etching method and the second textured surface 111(112) using the dry etching method are formed on the front surface of the substrate 110. Therefore, a roughness of the front surface (i.e., the surface of the emitter region 121) of the substrate 110 abutting on the first anti-reflection layer 131 further increases compared to when only the first textured surface 11(12) is formed.

[0079] If the first anti-reflection layer 131 is formed directly on the emitter region 121 using a deposition method such as a plasma enhanced chemical vapor deposition (PECVD) method, the first anti-reflection layer 131 may not be normally coated on the first and second protrusions 11 and 111 and the first and second depressions 12 and 112. Hence, a non-formation area of the first anti-reflection layer 131 may increase in the first and second textured surfaces of the substrate 110.

[0080] In this instance, a surface passivation effect may be not generated in the non-formation area of the first anti-reflection layer 131. As a result, an amount of carriers lost at and around the surface of the substrate 110 may increase.

[0081] On the other hand, in the embodiment of the invention, the first anti-reflection layer 131 is formed on the emitter region 121 using the atomic layer deposition method having the excellent step coverage. Therefore, the first anti-reflection layer 131 is normally formed on the first and second protrusions 11 and 111 and the first and second depressions 12 and 112. Hence, the non-formation area of the first anti-reflection layer 131 decreases in the first and second textured surfaces of the substrate 110.

[0082] Accordingly, because a formation area of the first anti-reflection layer 131 increases in the first and second textured surfaces of the substrate 110, the surface passivation effect using the first anti-reflection layer 131 is improved. Hence, an amount of carriers lost at and around the surface of the substrate 110 decreases, and the efficiency of the solar cell is improved.

[0083] The second anti-reflection layer 132 formed of hydrogenated silicon nitride (SiNx:H) is positioned directly on the first anti-reflection layer 131 on the front surface of the substrate 110.

[0084] Hydrogen (H) contained in hydrogenated silicon nitride (SiNx:H) for forming the second anti-reflection layer 132 moves to the surface of the substrate 110 via the first anti-reflection layer 131 to thereby perform a passivation function at and around the surface of the substrate 110.

10

[0085] An amount of carriers lost at and around the surface of the substrate 110 further decreases by the passivation function using both the first and second anti-reflection layers 131 and 132.

[0086] As described above, because the double-layered anti-reflection layer 130 including the first anti-reflection layer 131 formed of aluminum oxide (Al₂O₃) and the second anti-reflection layer 132 formed of hydrogenated silicon nitride (SiNx:H) is formed on the front surface of the substrate 110, the field passivation effect using the fixed charges of the first anti-reflection layer 131 and the surface passivation effect using the first and second anti-reflection layers 131 and 132 are obtained in addition to the anti-reflection effect of light using changes in the refractive indexes of the first and second anti-reflection layers 131 and 132.

[0087] When the thickness of the first anti-reflection layer 131 formed of aluminum oxide is equal to or greater than about 5 nm, the aluminum oxide layer 131 is more uniformly formed and the field passivation effect using the fixed charges of the first anti-reflection layer 131 is more stably obtained. When the thickness of the first anti-reflection layer 131 is equal to or less than about 15 nm, manufacturing time and cost of the first anti-reflection layer 131 are reduced without a reduction in the anti-reflection effect resulting from the refractive index of the first anti-reflection layer 131.

[0088] When the thickness of the second anti-reflection layer 132 formed of hydrogenated silicon nitride is equal to or greater than about 70 nm, the silicon nitride layer 132 is more uniformly formed and the surface passivation effect using hydrogen (H) is more stably obtained. When the thickness of the second anti-reflection layer 132 is equal to or less than about 100 nm, manufacturing time and cost of the second anti-reflection layer 132 are reduced without a reduction in the field passivation effect using silicon nitride having positive fixed charges.

[0089] Each of the plurality of back surface field regions 172 positioned at the back surface of the substrate 110 is a region that is more heavily doped than the substrate 110 with impurities of the same conductive type (for example, the n-type) as the substrate 110.

[0090] The back surface field regions 172 abut on the back electrodes 151 and the back bus bars 152 positioned on the back surface of the substrate 110, and are selectively or locally positioned at the back surface of the substrate 110.

[0091] Hence, the back surface field regions 172 are not positioned between the adjacent back electrodes 151, between the back electrodes 151 and the back bus bars 152, and between the adjacent back bus bars 152.

[0092] A potential barrier is formed by a difference between impurity concentrations of the first conductive type region (for example, the n-type region) of the substrate 110 and the back surface field regions 172. Hence, the

potential barrier prevents or reduces holes from moving to the back surface field regions 172 used as a moving path of electrons and makes it easier for electrons to move to the back surface field regions 172.

[0093] Thus, the back surface field regions 172 reduce an amount of carriers lost by a recombination and/or a disappearance of the electrons and the holes at and around the back surface of the substrate 110 and accelerate a movement of desired carriers (for example, electrons), thereby increasing an amount of carriers moving to the back electrode part 150.

[0094] Because the impurity concentration of the back surface field regions 172 is higher than the impurity concentration of the substrate 110, the conductivity of the back surface field regions 172 abutting on the back electrode part 150 is greater than the conductivity of the substrate 110. Hence, a movement of carriers from the back surface field regions 172 to the back electrode part 150 is easily carried out.

[0095] The passivation layer 190 includes a first passivation layer 191 positioned directly on the back surface of the substrate 110 and a second passivation layer 192 positioned directly on the first passivation layer 191.

[0096] The first passivation layer 191 may be formed of hydrogenated silicon nitride (SiNx:H), and the second passivation layer 192 may be formed of aluminum oxide (Al₂O₃).

[0097] In the embodiment of the invention, the first passivation layer 191 and the second anti-reflection layer 132 may be simultaneously formed through the same process, or the second passivation layer 192 and the first anti-reflection layer 131 may be simultaneously formed through the same process.

[0098] Hence, the first passivation layer 191 may be formed of the same material as the second anti-reflection layer 132 and thus may have the same characteristics, for example, thickness, properties, component, composition (or composition ratio), refractive index, etc., as the second anti-reflection layer 132. Further, the second passivation layer 192 may be formed of the same material as the first anti-reflection layer 131 and thus may have the same characteristics, for example, thickness, properties, component, composition (or composition ratio), refractive index, etc., as the first anti-reflection layer 131.

[0099] More specifically, the first passivation layer 191 formed of hydrogenated silicon nitride (SiNx:H) may have a thickness of about 70 nm to 100 nm and a refractive index of about 2.0 to 2.2. The second passivation layer 192 formed of aluminum oxide (Al₂O₃) may have a thickness of about 5 nm to 15 nm and a refractive index of about 1.1 to 1.6.

[0100] Because the first passivation layer 191 formed of hydrogenated silicon nitride (SiNx:H) is positioned on the back surface field regions 172 positioned directly on the back surface of the substrate 110, the surface passivation function using hydrogen (H) is performed. Hence, an amount of carriers lost at and around the back surface of the substrate 110 decreases.

[0101] Hydrogenated silicon nitride (SiNx:H) has the characteristic of positive fixed charges opposite aluminum oxide (Al₂O₃).

[0102] In the embodiment of the invention, the substrate 110 is of the n-type, and the first passivation layer 191, which is formed directly on the back surface of the substrate 110 using silicon nitride, has the characteristic of positive fixed charges. Hence, negative charges (i.e., electrons) moving to the first passivation layer 191 have a polarity opposite the first passivation layer 191 formed of silicon nitride. As a result, the electrons are drawn to the first passivation layer 191 because of the positive polarity of the first passivation layer 191. On the other hand, positive charges (i.e., holes) have the same polarity as the first passivation layer 191 and thus are pushed to the front surface of the substrate 110 opposite the first passivation layer 191 because of the positive polarity of the first passivation layer 191.

[0103] Hence, when the first passivation layer 191 is formed directly on the back surface of the n-type substrate 110 using hydrogenated silicon nitride (SiNx:H), an amount of electrons moving to the back surface of the substrate 110 further increases because of the influence of positive fixed charges. Further, the recombination of the electrons and the holes at and around the back surface of the substrate 110 is reduced.

[0104] The second passivation layer 192, which is formed on the first passivation layer 191 using aluminum oxide (Al₂O₃), prevents hydrogen (H) contained in the first passivation layer 191 from moving to the back electrode part 150 opposite the front surface of the substrate 110 because of heat applied when the solar cell is manufactured. As a result, the surface passivation effect of the back surface of the substrate 110 using hydrogen (H) contained in the first passivation layer 191 is improved.

[0105] As described above, the double-layered passivation layer 190 including the first passivation layer 191 formed of hydrogenated silicon nitride (SiNx:H) and the second passivation layer 192 formed of aluminum oxide (Al₂O₃) is formed on the back surface of the substrate 110, in the same manner as the double-layered anti-reflection layer 130 positioned on the front surface of the substrate 110. Hence, the surface passivation effect of the back surface of the substrate 110 is improved.

[0106] It is preferable, but not required, that the thickness of the first passivation layer 191 is greater than the thickness of the second passivation layer 192 positioned on the first passivation layer 191, so that the second passivation layer 192 having the negative fixed charges does not adversely affect the first passivation layer 191 having the positive fixed charges. Further, the thickness of the first passivation layer 191 may be greater than the thickness of the second anti-reflection layer 132 on the front surface of the substrate 110.

[0107] Accordingly, if necessary, the thickness of the hydrogenated silicon nitride layer (i.e., the second anti-reflection layer 132) positioned on the front surface of the substrate 110 may be different from the thickness of

the silicon nitride layer (i.e., the first passivation layer 191) positioned on the back surface of the substrate 110. In this instance, the silicon nitride layer (i.e., the second anti-reflection layer 132) positioned on the front surface of the substrate 110 may have the thickness of about 90 nm, and the silicon nitride layer (i.e., the first passivation layer 191) positioned on the back surface of the substrate 110 may have the thickness of about 100 nm.

[0108] When light is incident on the back surface of the substrate 110, a refractive index in going from air to the substrate 110 increases. Therefore, a reflection amount of light incident on the back surface of the substrate 110 decreases, and an amount of light absorbed in the substrate 110 increases. Hence, when light is incident on the back surface of the substrate 110, the passivation layer 190 serves as an anti-reflection layer.

[0109] The plurality of front electrodes 141 of the front electrode part 140 are connected to the emitter region 121, and the plurality of front bus bars 142 of the front electrode part 140 are connected to the front electrodes 141 as well as the emitter region 121.

[0110] The front electrodes 141 are electrically and physically connected to the emitter region 121 and are separated from one another. The front electrodes 141 extend parallel to one another in a fixed direction. The front electrodes 141 collect carriers (for example, holes) moving to the emitter region 121.

[0111] The front bus bars 142 are electrically and physically connected to the emitter region 121 and extend parallel to one another in a direction crossing the front electrodes 141.

[0112] The front bus bars 142 have to collect not only carriers (for example, holes) moving from the emitter region 121 but also carriers collected by the front electrodes 141 crossing the front bus bars 142 and have to move the collected carriers in a desired direction. Thus, a width of each front bus bar 142 may be greater than a width of each front electrode 141.

[0113] In the embodiment of the invention, the front bus bars 142 are positioned on the same level layer as the front electrodes 141 and are electrically and physically connected to the front electrodes 141 at crossings of the front electrodes 141 and the front bus bars 142.

[0114] Accordingly, as shown in FIG. 1, the plurality of front electrodes 141 have a stripe shape extending in a transverse (or longitudinal) direction, and the plurality of front bus bars 142 have a stripe shape extending in a direction crossing the front electrodes 141, for example, in a longitudinal (or transverse) direction. Hence, the front electrode part 140 has a lattice shape on the front surface of the substrate 110.

[0115] The front bus bars 142 are connected to an external device and output the collected carriers to the external device.

[0116] The front electrode part 140 including the front electrodes 141 and the front bus bars 142 is formed of at least one conductive material, for example, silver (Ag).

[0117] The plurality of back electrodes 151 of the back

electrode part 150 are positioned on the back surface field regions 172 and directly abut on the back surface field regions 172. The back electrodes 151 are separated from one another and extend in a fixed direction in the same manner as the front electrodes 141. In this instance, the back electrodes 151 extend in the same direction as the front electrodes 141. The back electrodes 151 collect carriers (for example, electrons) moving to the back surface field regions 172.

[0118] The plurality of back bus bars 152 of the back electrode part 150 are positioned on the back surface field regions 172 and abut on the back surface field regions 172. The back bus bars 152 extend parallel to one another in a direction crossing the back electrodes 151. In this instance, the back bus bars 152 extend in the same direction as the front bus bars 142. The back bus bars 152 may be positioned opposite the front bus bars 142 with the substrate 110 interposed between them.

[0119] The back bus bars 152 collect carriers (for example, electrons) collected by the back electrodes 151 crossing the back bus bars 152 and move the collected carriers in a desired direction. Thus, a width of each back bus bar 152 may be greater than a width of each back electrode 151.

[0120] The back bus bars 152 are positioned on the same level layer as the back electrodes 151 and are electrically and physically connected to the back electrodes 151 at crossings of the back electrodes 151 and the back bus bars 152.

[0121] Thus, the back electrode part 150 has a lattice shape on the back surface of the substrate 110 in the same manner as the front electrode part 140.

[0122] The back electrodes 151 and the back bus bars 152 may contain the same conductive material, for example, silver (Ag) as the front electrodes 141 and the front bus bars 142. Alternatively, the back electrode part 150 may be formed of a material different from the front electrode part 140, and the back electrodes 151 may be formed of a material different from the back bus bars 152.

[0123] As described above, in the embodiment of the invention, the back surface field regions 172 are positioned under the back electrodes 151 and the back bus bars 152 and extend along the back electrodes 151 and the back bus bars 152. Hence, the back surface field regions 172 are selectively or locally positioned at the back surface of the substrate 110 and have a lattice shape in the same manner as the back electrode part 150. Thus, as described above, a non-formation portion of the back surface field regions 172 exists at the back surface of the substrate 110.

[0124] In the embodiment of the invention, the number of front electrode 141, which are positioned on the front surface of the substrate 110 and receive the most of light, is less than the number of back electrode 151, which are positioned on the back surface of the substrate 110 and receive a smaller amount of light than the front surface of the substrate 110. Thus, a distance between the two adjacent front electrodes 141 is greater than a distance

between the two adjacent back electrodes 151.

[0125] As described above, because the front electrode part 140 and the back electrode part 150 contain a metal material such as silver (Ag), the front electrode part 140 and the back electrode part 150 do not transmit light.

[0126] Because the distance between the front electrodes 141 is greater than the distance between the back electrodes 151, a reduction in an incident area of light at the front surface of the substrate 110 is reduced or prevented by the arrangement of the front electrodes 141. Hence, an amount of light incident on the front surface of the substrate 110 increases.

[0127] In another embodiment, the front bus bars 142, the back bus bars 152, or both may be omitted if needed or desired.

[0128] In the embodiment of the invention, at least one of the front electrode part 140 and the back electrode part 150 may be formed using a plating method.

[0129] When at least one of the front electrode part 140 and the back electrode part 150 is formed using the plating method, at least one of the front electrode part 140 and the back electrode part 150 may have a single-layered structure as in the embodiment of the invention. Alternatively, at least one of the front electrode part 140 and the back electrode part 150 may have a multi-layered structure such as a double-layered structure and a triple-layered structure. When at least one of the front electrode part 140 and the back electrode part 150 formed using the plating method has the single-layered structure, at least one of the front electrode part 140 and the back electrode part 150 may be formed of silver (Ag).

[0130] When at least one of the front electrode part 140 and the back electrode part 150 formed using the plating method has the double-layered structure, a lower layer (or a first layer), which abuts on the emitter region 121 (i.e., a second conductive type region of the substrate 110) or abuts on the back surface field regions 172 (i.e., a heavily doped region of the substrate 110 doped with impurities of the first conductive type), may be formed of nickel (Ni), and an upper layer (or a second layer) on the lower layer may be formed of silver (Ag).

[0131] When at least one of the front electrode part 140 and the back electrode part 150 formed using the plating method has the triple-layered structure, a lower layer (or a first layer) abutting on the emitter region 121 or the back surface field regions 172 may be formed of nickel (Ni), a middle layer (or a second layer) on the lower layer may be formed of copper (Cu), and an upper layer (or a third layer) on the middle layer may be formed of silver (Ag) or tin (Sn).

[0132] When at least one of the front electrode part 140 and the back electrode part 150 formed using the plating method has the double-layered structure, a thickness of the lower layer may be about 0.5 μm to 1 μm , and a thickness of the upper layer may be about 5 μm to 10 μm . When at least one of the front electrode part 140 and the back electrode part 150 formed using the

plating method has the triple-layered structure, each of the lower layer and the upper layer may have a thickness of about 0.5 μm to 1 μm , and a thickness of the middle layer may be about 5 μm to 10 μm .

[0133] In this instance, the lower layer is to reduce a contact resistance between the lower layer and the emitter region 121 or the back surface field regions 172 abutting on the lower layer, and is to improve contact characteristics. The middle layer may be formed of a relatively inexpensive material with good conductivity, for example, copper (Cu) in consideration of cost reduction. If the middle layer is formed of copper (Cu), the lower layer underlying the middle layer may prevent copper (Cu), which is smoothly bonded to silicon (Si), from serving as an impurity region, which is penetrated (absorbed) in the emitter region 121 or the back surface field regions 172 formed of silicon (Si) to thereby reduce or prevent the movement of carriers.

[0134] The upper layer prevents the oxidation of the layer (for example, the lower layer or the middle layer) underlying the upper layer and improves an adhesive strength between the layer (for example, the lower layer or the middle layer) and a conductive film, for example, a ribbon positioned on the upper layer.

[0135] As described above, at least one of the front electrode part 140 and the back electrode part 150 formed using the plating method may have the double-layered structure or the triple-layered structure, and the lower layer may be formed of nickel (Ni). In this instance, nickel silicide compounds exist between the lower layer and the emitter region 121 or between the lower layer and the back surface field regions 172 because of a bond between nickel (Ni) and silicon (Si) of the emitter region 121 (i.e., the second conductive type region of the substrate 110) or a bond between nickel (Ni) and silicon (Si) of the back surface field regions 172 (i.e., the heavily doped region of the substrate 110 doped with impurities of the first conductive type).

[0136] Alternatively, at least one of the front electrode part 140 and the back electrode part 150 may be formed through a screen printing method using an Ag paste containing a glass frit or an Al paste containing the glass frit. In this instance, the glass frit may pass through the anti-reflection layer 130 or the passivation layer 190 and may abut on the emitter region 121 or the back surface field regions 172.

[0137] Accordingly, at least one of components of the glass frit is detected in a contact portion between the front electrode part 140 and the emitter region 121 or a contact portion between the back electrode part 150 and the back surface field regions 172. For example, at least one of lead (Pb)-based material such as PbO, bismuth (Bi)-based material such as Bi₂O₃, aluminum (Al)-based material such as Al₂O₃, boron (B)-based material such as B₂O₃, tin (Sn)-based material, zinc (Zn)-based material such as ZnO, titanium (Ti)-based material such as TiO₂, and phosphorus (P)-based material such as P₂O₅ contained in the glass frit may be detected.

[0138] On the other hand, when at least one of the front electrode part 140 and the back electrode part 150 is formed using the plating method, the component of the glass frit is not detected between the substrate 110 (i.e., the emitter region 121) and the front electrode part 140 including the front electrodes 141 and the front bus bars 142 and between the substrate 110 (i.e., the back surface field regions 172) and the back electrode part 150 including the back electrodes 151 and the back bus bars 152.

[0139] As described above, when at least one of the front electrode part 140 and the back electrode part 150 has the multi-layered structure, the lower layer, the middle layer, and the upper layer are sequentially formed using the plating method to have a desired thickness.

[0140] In the embodiment of the invention, the number of front electrodes 141, the number of front bus bars 142, the number of back electrodes 151, and the number of back bus bars 152 may vary, if desired or necessary.

[0141] Each front bus bar 142 and each back bus bar 152 respectively collect carriers from the emitter region 121 and the back surface field regions 172, and also respectively output carriers collected by the front electrodes 141 and carriers collected by the back electrodes 151 to the external device.

[0142] In another embodiment, at least one of the front bus bar 142 and the back bus bar 152 may be positioned directly on at least one of the anti-reflection layer 130 and the passivation layer 190 and may abut on at least one of the anti-reflection layer 130 and the passivation layer 190.

[0143] As described above, because each of the front surface and the back surface of the substrate 110 has the first and second textured surfaces, a surface area of the substrate 110 increases.

[0144] Hence, an area of the emitter region 121 contacting each front electrode 141 and an area of the back surface field region 172 contacting each back electrode 151 increase. Therefore, even if a width W11 of each front electrode 141 and a width W12 of each back electrode 151 decrease, a contact area between the emitter region 121 and the front electrode 141 and a contact area between the back surface field region 172 and the back electrode 151 may not decrease.

[0145] As a result, even if the width W11 of each front electrode 141 and the width W12 of each back electrode 151 decrease, an amount of carriers moving from the emitter region 121 to the front electrodes 141 and an amount of carriers moving from the back surface field regions 172 to the back electrodes 151 may not decrease.

[0146] In the embodiment of the invention, the width W11 of each front electrode 141 and the width W12 of each back electrode 151 may be about 40 μm to 50 μm . The widths W11 and W12 are much less than a width (of about 60 μm to 100 μm) of electrodes of a comparative example.

[0147] As described above, because formation areas of the front electrodes 141 and the back electrodes 151

to prevent or reduce the incidence of light at the front surface and the back surface of the substrate 110 are reduced, an amount of light incident on the front surface and the back surface of the substrate 110 increases.

[0148] However, a moving distance of carriers moving to the front electrodes 141 along the emitter region 121 and a moving distance of carriers moving to the back electrodes 151 along the back surface field regions 172 increase because of the first and second textured surfaces of the substrate 110.

[0149] Accordingly, in the embodiment of the invention, a distance D11 between the two adjacent front electrodes 141 and a distance D12 between the two adjacent back electrodes 151 may decrease, so as to compensate for an increase in the moving distance of carriers resulting from an increase in a surface area of the emitter region 121 and a surface area of the back surface field regions 172. For example, the distance D11 between the two adjacent front electrodes 141 and the distance D12 between the two adjacent back electrodes 151 may be equal to or greater than about 1.5 mm and less than about 2.0 mm.

[0150] As described above, because the width W11 of each front electrode 141 and the width W12 of each back electrode 151 decrease, an incident area of light at the front surface and the back surface of the substrate 110 does not decrease even if the distances D11 and D12 increase.

[0151] An operation of the solar cell having the above-described structure is described below.

[0152] When light irradiated to the solar cell is incident on the substrate 110 and at least one of the emitter region 121 and the back surface field region 172, each of which is the semiconductor part, through at least one of the anti-reflection layer 130 and the passivation layer 190, electrons and holes are generated in the substrate 110 by light energy produced based on the incident light. In this instance, because a reflection loss of the light incident on the substrate 110 is reduced by the first and second textured surfaces of the substrate 110, the anti-reflection layer 130, and the passivation layer 190, an amount of light incident on the substrate 110 increases.

[0153] The electrons move to the n-type semiconductor part (for example, the substrate 110) and the holes move to the p-type semiconductor part (for example, the emitter region 121) by the p-n junction of the substrate 110 and the emitter region 121.

[0154] The holes moving to the emitter region 121 are collected by the front electrodes 141 and the front bus bars 142 and then move along the front bus bars 142. The electrons moving to the substrate 110 pass through the back surface field regions 172, are collected by the back electrodes 151 and the back bus bars 152, and move along the back bus bars 152. When the front bus bars 142 are connected to the back bus bars 152 using electric wires such as a conductive film, current flows therein to thereby enable use of the current for electric power.

[0155] As described above, each of the front surface and the back surface of the substrate 110 has the double texturing structure including the first protrusions 11 having the size of several μm and the second protrusions 111 having the size of several hundreds of nm, the incident area of the substrate 110 increases. Further, a reflection amount of light decreases due to a reflection operation using the first and second protrusions 11 and 111, and an amount of light incident on the substrate 110 increases.

[0156] The efficiency of the solar cell is improved by the anti-reflection effect using the refractive indexes of the anti-reflection layer 130 and the passivation layer 190, the field passivation effect using the fixed charges, and the surface passivation effect using hydrogen (H) or oxygen (O).

[0157] A method for manufacturing the solar cell according to the embodiment of the invention is described below with reference to FIGS. 4A to 4H.

[0158] As shown in FIG. 4A, a wet etching process is performed on a front surface and a back surface of a substrate 110 of a first conductive type (for example, n-type) to form a first textured surface having a plurality of first protrusions 11 and a plurality of first depressions 12.

[0159] The substrate 110 may be a crystalline semiconductor formed of single crystal silicon.

[0160] When the substrate 110 is formed of single crystal silicon, the first textured surface 11(12) may be formed using an alkali solution such as isopropyl alcohol (IPA) or potassium hydroxide (KOH).

[0161] Each of the first protrusions 11 may have a pyramid shape, such as a triangular pyramid. A diameter (i.e., size) and a protruding height of each first protrusion 11 may be about 5 μm to 10 μm .

[0162] Next, as shown in FIG. 4B, after the first textured surface 11 (12) is formed, a second textured surface having a plurality of second protrusions 111 and a plurality of second depressions 112 is formed on the surface of each first protrusion 11 using a dry etching method such as a reaction ion etching (RIE) method.

[0163] A maximum diameter (i.e., size) and a protruding height of each second protrusion 111 may be about 300 nm to 600 nm.

[0164] In the embodiment of the invention, an etching gas used in the RIE method may be a mixture of SF_6 and Cl_2 . Other gases may be used.

[0165] After the second textured surface 111(112) is formed, a process for removing a remainder of the surface (or a portion of a surface layer) of the substrate 110 may be additionally performed. The remainder may be removed using a dry gas (used in the dry etching method) of a process room (or chamber) used to form the second textured surface 111(112), instead of the use of a separate process room (or chamber). In this instance, time required in the removing process of the remainder using the dry etching method is further reduced as compared to the wet etching method.

[0166] Further, if the remainder is removed using the

wet etching method, the uneven portions of the first and second textured surfaces may be deformed. However, when the remainder is removed using the dry etching method, the uneven portions of the first and second textured surfaces are not deformed, and thus changes or deviations in the reflectance of light resulting from the first and second textured surfaces are not generated.

[0167] Next, as shown in FIG. 4C, ions (hereinafter, referred to as "first impurity ions") of first impurities of a predetermined conductive type are implanted into the front surface of the substrate 110 using an ion implantation method.

[0168] In this instance, the predetermined conductive type may be a second conductive type (for example, p-type) opposite the first conductive type of the substrate 110. In the embodiment of the invention, the first impurities may use boron (B). Thus, the first impurity ions may be positive ions B^+ of boron (B).

[0169] More specifically, the first impurity ions of the second conductive type are implanted into the exposed front surface of the substrate 110 to form an impurity region, i.e., a first impurity region 120 of the second conductive type at the front surface of the substrate 110.

[0170] Subsequently, ions (hereinafter, referred to as "second impurity ions") of second impurities of a predetermined conductive type (i.e., the first conductive type) are implanted into the back surface of the substrate 110 using the ion implantation method to form a second impurity region 170 of the first conductive type at the back surface of the substrate 110.

[0171] In the embodiment of the invention, the second impurities may use phosphorus (P). Thus, the second impurity ions may be positive ions P^+ of phosphorus (P).

[0172] A mask to implant the ions only into a desired region of each of the front surface and the back surface of the substrate 110 may be used in the ion implantation process for forming the first and second impurity regions 120 and 170.

[0173] For example, the mask positioned on the front surface of the substrate 110 may block only an edge of the front surface of the substrate 110 and may expose a remaining portion of the front surface of the substrate 110 except the edge. Further, the mask positioned on the back surface of the substrate 110 may expose only a region to form a back surface field region and may block a remaining portion of the back surface of the substrate 110.

[0174] Acceleration energy of ions for implanting the first and second impurity ions into the substrate 110 may be about 1 keV to 20 keV. An implantation depth of ions may be determined depending on the acceleration energy.

[0175] Thus, acceleration energy for the first impurity region 120 may be different from acceleration energy for the second impurity region 170. For example, acceleration energy used to implant ions of p-type impurities into the substrate 110 may be greater than acceleration energy used to implant ions of n-type impurities into the

substrate 110.

[0176] In the embodiment of the invention, formation order of the first impurity region 120 and the second impurity region 170 may vary. The first impurity region 120 and the second impurity region 170 may be formed in the same chamber or respective chambers.

[0177] Next, as shown in FIG. 4D, after the first and second impurity regions 120 and 170 are formed, a thermal process is performed on the substrate 110 having the first and second impurity regions 120 and 170 in an atmosphere of nitrogen (N_2) or oxygen (O_2). Thus, the first and second impurity regions 120 and 170 are completely activated. Hence, the first impurity region 120 forms an emitter region 121 positioned at the front surface of the substrate 110, and thus the emitter region 121 and the substrate 110 form a p-n junction. Further, the second impurity region 170 forms a plurality of back surface field regions 172 positioned at the back surface of the substrate 110.

[0178] In other words, an implantation state of the p-type and n-type impurity ions of the first and second impurity regions 120 and 170 changes from an interstitial state to a substitutional state because of the activation of the first and second impurity regions 120 and 170 through the thermal process. Hence, silicon and the p-type and n-type impurity ions are rearranged. As a result, the first and second impurity regions 120 and 170 respectively serve as the p-type emitter region 121 and the n-type back surface field regions 172.

[0179] Solubility of boron (B) used to form the emitter region 121 is less than solubility of phosphorus (P) used to form the back surface field regions 172. Therefore, an activation temperature of the first and second impurity regions 120 and 170 is determined based on the first impurity region 120, so as to stably activate the first impurity region 120.

[0180] The activation temperature of the first and second impurity regions 120 and 170 may be about 1,000 °C to 2,000 °C, and time required in the thermal process may be about 20 minutes to 60 minutes.

[0181] In the embodiment of the invention, because the activation process is performed at a high temperature equal to or higher than about 1,000 °C capable of stably activating boron (B), the first impurity region 120 as well as the second impurity region 170 are stably activated. Hence, the emitter region 121 and the back surface field regions 172 are smoothly formed.

[0182] Furthermore, because the thermal process is performed at the high temperature equal to or higher than about 1,000 °C, a damaged portion generated in the ion implantation process for the first and second impurity regions 120 and 170 is recrystallized. Hence, the damaged portion generated in the ion implantation process is recovered without a separate damage removal process using the wet etching method, etc.

[0183] When the second textured surface 111(112) is formed using the RIE method, a damaged portion of the surface of the substrate 110 is generated because of

plasma generated in the process. However, as described above, the damaged portion is recovered by the recrystallization of silicon (Si) through the thermal process performed at the high temperature equal to or higher than about 1,000 °C. Therefore, a separate damage removal process using the wet etching method, etc., is not necessary.

[0184] Because of these reasons, the removing process of the remainder, which may be performed after the formation of the first and second textured surfaces, may be omitted.

[0185] In the embodiment of the invention, the damaged portion, which is formed in the surface of the substrate 110 (or the emitter region 121) in the RIE process and the ion implantation process, is recovered by the activation process of the first impurity region 120 at the high temperature (equal to or higher than about 1,000 °C) for the p-type emitter region 121. Hence, the reflectance of light of a short wavelength band incident on the emitter region 121 does not increase.

[0186] Next, as shown in FIG. 4E, a first passivation layer 191 formed of hydrogenated silicon nitride ($SiNx:H$) is formed on the back surface of the substrate 110. The first passivation layer 191 may be formed using a deposition method such as a plasma enhanced chemical vapor deposition (PECVD) method. In the embodiment of the invention, the first passivation layer 191 may have a thickness of about 70 nm to 100 nm.

[0187] Next, as shown in FIG. 4F, layers formed of aluminum oxide (Al_2O_3) are respectively formed on the emitter region 121 positioned at the front surface of the substrate 110 and the first passivation layer 191 positioned on the back surface of the substrate 110 to form a first anti-reflection layer 131 on the emitter region 121 and a second passivation layer 192 on the first passivation layer 191.

[0188] The aluminum oxide layers may be formed using the PECVD method, an atomic layer deposition (ALD) method, etc.

[0189] When the aluminum oxide layer is formed using the PECVD method, the layer is stacked only in a portion exposed by a process gas. Therefore, the first anti-reflection layer 131 and the second passivation layer 192, each of which is formed of aluminum oxide, are respectively formed on the front surface and the back surface of the substrate 110 through the separate PECVD method.

[0190] In this instance, the first anti-reflection layer 131 and the second passivation layer 192 respectively positioned on the front surface and the back surface of the substrate 110 may be formed under the same process conditions to thereby have the same characteristics. Alternatively, the first anti-reflection layer 131 and the second passivation layer 192 may be formed under different process conditions to thereby have different characteristics.

[0191] However, when the aluminum oxide layers are formed using the ALD method, the aluminum oxide layers

may be formed on the front surface, the back surface, and the lateral surface of the substrate 110 through one stacking process. Thus, the aluminum oxide layers are simultaneously formed on the front surface and the back surface of the substrate 110 through one ALD process to form the first anti-reflection layer 131 and the second passivation layer 192.

[0192] Because the first anti-reflection layer 131 and the second passivation layer 192 respectively positioned on the front surface and the back surface of the substrate 110 are formed under the same process conditions, the first anti-reflection layer 131 and the second passivation layer 192 have the same characteristics.

[0193] In the embodiment of the invention, the first anti-reflection layer 131 and the second passivation layer 192 may have a thickness of about 5 nm to 15 nm.

[0194] Hence, a passivation layer 190 including the first and second passivation layers 191 and 192 is formed on the back surface of the substrate 110.

[0195] Next, as shown in FIG. 4G, a second anti-reflection layer 132 formed of hydrogenated silicon nitride (SiNx:H) is formed on the first anti-reflection layer 131 using the PECVD method at a thickness of about 70 nm to 100 nm. Hence, an anti-reflection layer 130 including the first and second anti-reflection layers 131 and 132 is formed.

[0196] As described above, the anti-reflection layer 130 including the first anti-reflection layer 131 formed of aluminum oxide (Al_2O_3) and the second anti-reflection layer 132 formed of hydrogenated silicon nitride (SiNx:H) is formed on the front surface of the substrate 110, and the passivation layer 190 including the first passivation layer 191 formed of hydrogenated silicon nitride (SiNx:H) and the second passivation layer 192 formed of aluminum oxide (Al_2O_3) is formed on the back surface of the substrate 110. Afterward, a front electrode part 140 including a plurality of front electrodes 141 and a plurality of front bus bars 142, which pass through the anti-reflection layer 130 and abut on the emitter region 121 underlying the anti-reflection layer 130, is formed. Further, a back electrode part 150 including a plurality of back electrodes 151 and a plurality of back bus bars 152, which pass through the passivation layer 190 and abut on the back surface field regions 172 underlying the passivation layer 190, is formed. As a result, the solar cell shown in FIGS. 1 and 2 is completed.

[0197] An example of a method for forming the front electrode part 140 and the back electrode part 150 is described with reference to FIG. 4H.

[0198] For example, as shown in FIG. 4H, a laser beam is selectively irradiated onto each of the front surface and the back surface of the substrate 110 to form a plurality of first and second openings 181 and 182 at a location to form the front electrode part 140 and the back electrode part 150.

[0199] The plurality of first openings 181 pass through the anti-reflection layer 130 and expose the emitter region 121 underlying the opened portions of the anti-re-

flexion layer 130. The plurality of second openings 182 pass through the passivation layer 190 and expose the back surface field regions 172 underlying the opened portions of the passivation layer 190.

[0200] The plurality of first openings 181 are used to form the plurality of front electrodes 141 and the plurality of front bus bars 142. In this instance, a width of the first opening 181 for each front electrode 141 is less than a width of the first opening 181 for each front bus bar 142.

[0201] The plurality of second openings 182 are used to form the plurality of back electrodes 151 and the plurality of back bus bars 152. In this instance, a width of the second opening 182 for each back electrode 151 is less than a width of the second opening 182 for each back bus bar 152.

[0202] The number of first openings 181 for the front electrodes 141 may be less than the number of second openings 182 for the back electrodes 151. Hence, a distance between the two adjacent first openings 181 may be greater than a distance between the two adjacent second openings 182.

[0203] The first openings 181 for the front bus bars 142 may be positioned opposite the second openings 182 for the back bus bars 152 with the substrate 110 between them.

[0204] Subsequently, the front electrode part 140 and the back electrode part 150 are respectively formed on the emitter region 121 and the back surface field regions 172 exposed by the first and second openings 181 and 182 using an electroplating method or an electroless plating method.

[0205] In another embodiment, the front electrodes 141, the front bus bars 142, the back electrodes 151, and the back bus bars 152 may be formed by coating a metal paste containing a metal material such as silver (Ag) on the first and second openings 181 and 182 using a screen printing method, etc., and then performing a thermal process on the metal paste at a desired temperature.

[0206] In another embodiment, the front electrodes 141, the front bus bars 142, the back electrodes 151, and the back bus bars 152 may be formed by coating and drying a metal paste containing at least one of silver (Ag) and aluminum (Al) on the anti-reflection layer 130 and the passivation layer 190 and then performing a thermal process on the metal paste. Hence, the front electrode part 140 including the front electrodes 141 and the front bus bars 142 may be formed on the emitter region 121, and the back electrode part 150 including the back electrodes 151 and the back bus bars 152 may be formed on the back surface field regions 172.

[0207] Because the front electrode part 140 and the back electrode part 150 have to partially pass through the anti-reflection layer 130 and the passivation layer 190, respectively, the metal paste may contain an etchant, for example, PbO for etching the anti-reflection layer 130 and the passivation layer 190. An amount and a kind of the etchant contained in the metal paste may be determined depending on a thickness or a material of the

anti-reflection layer 130 and the passivation layer 190.

[0208] When the thermal process is performed on the metal paste coated on the anti-reflection layer 130 and the passivation layer 190, the metal paste passes through the anti-reflection layer 130 and the passivation layer 190 and is chemically bonded to the emitter region 121 and the back surface field regions 172 underlying the anti-reflection layer 130 and the passivation layer 190. Hence, the front electrode part 140 electrically and physically connected to the emitter region 121 and the back electrode part 150 electrically and physically connected to the back surface field regions 172 are formed.

[0209] When at least one of the anti-reflection layer 130 and the passivation layer 190 is omitted, at least one of the front electrode part 140 and the back electrode part 150 may not contain the etchant because it does not need to pass through the omitted component (i.e., at least one of the anti-reflection layer 130 and the passivation layer 190).

[0210] When at least one of the front bus bar 142 and the back bus bar 152 is positioned directly on the anti-reflection layer 130 or the passivation layer 190, at least one of the front bus bar 142 and the back bus bar 152 may not contain the etchant because it does not need to pass through the anti-reflection layer 130 or the passivation layer 190. Alternatively, at least one of the front bus bar 142 and the back bus bar 152 may contain a small amount of the etchant which may not pass through the anti-reflection layer 130 or the passivation layer 190.

[0211] In this instance, at least one of the front electrode 141, the front bus bar 142, the back electrode 151, and the back bus bar 152 may be formed of a material different from other components.

[0212] Another example of a solar cell according to an example embodiment of the invention is described below with reference to FIG. 5.

[0213] Structures and components identical or equivalent to those described in the solar cell shown in FIGS. 1 to 3 are designated with the same reference numerals, and a further description may be briefly made or may be entirely omitted.

[0214] Unlike the solar cell shown in FIGS. 1 and 2, a solar cell shown in FIG. 5 further includes hydrogenated silicon oxide (SiOx:H) layers on hydrogenated silicon nitride (SiNx:H) layers respectively positioned on a front surface and a back surface of a substrate 110.

[0215] More specifically, an anti-reflection layer 130a positioned on the front surface of the substrate 110 further includes a third anti-reflection layer 133, which is positioned directly on a second anti-reflection layer 132 and is formed of hydrogenated silicon oxide (SiOx:H), in addition to a first anti-reflection layer 131 formed of aluminum oxide (Al₂O₃) and the second anti-reflection layer 132 formed of hydrogenated silicon nitride (SiNx:H). Hence, the anti-reflection layer 130a has a triple-layered structure including the layers 131 to 133.

[0216] Further, a passivation layer 190a positioned on the back surface of the substrate 110 includes a first pas-

sivation layer 191 formed of hydrogenated silicon nitride (SiNx:H), a second passivation layer 192a, which is positioned directly on the first passivation layer 191 and is formed of hydrogenated silicon oxide (SiOx:H), and a third passivation layer 193, which is positioned directly on the second passivation layer 192a and is formed of aluminum oxide (Al₂O₃).

[0217] In other words, the solar cell shown in FIG. 5 further includes the hydrogenated silicon oxide layer between the hydrogenated silicon nitride layer and the aluminum oxide layer, unlike the solar cell shown in FIGS. 1 and 2. Thus, the passivation layer 190a has a triple-layered structure including the layers 191, 192a, and 193.

[0218] As described above, the hydrogenated silicon oxide layers 133 and 192a positioned directly on the hydrogenated silicon nitride layers 132 and 191 prevent hydrogen (H), which is contained in the hydrogenated silicon nitride layers 132 and 191 and performs a surface passivation function, from moving in a direction opposite the substrate 110. Thus, the hydrogenated silicon oxide layers 133 and 192a included in the anti-reflection layer 130a and the passivation layer 190a serve as capping layers of the hydrogenated silicon nitride layers 132 and 191 underlying the hydrogenated silicon oxide layers 133 and 192a.

[0219] The hydrogenated silicon oxide layers 133 and 192a contain hydrogen (H) capable of recovering a defect. Hence, hydrogen (H) contained in the hydrogenated silicon oxide layers 133 and 192a moves to the surface of the substrate 110 and performs the surface passivation function.

[0220] Accordingly, a surface passivation effect is further improved by the hydrogenated silicon oxide layers 133 and 192a respectively positioned on the front surface and the back surface of the substrate 110.

[0221] The hydrogenated silicon oxide layers 133 and 192a are formed using a PECVD method. Unlike the formation order of the anti-reflection layer 130 and the passivation layer 190 in the solar cell shown in FIGS. 1 and 2, the anti-reflection layer 130a and the passivation layer 190a are formed in the following formation order.

[0222] For example, after the first passivation layer 191 formed of hydrogenated silicon nitride (SiNx:H) is formed on the back surface of the substrate 110 using the PECVD method, the second passivation layer 192a formed of hydrogenated silicon oxide (SiOx:H) is formed on the first passivation layer 191 using the PECVD method. Then, the third passivation layer 193 and the first anti-reflection layer 131, each of which is formed of aluminum oxide (Al₂O₃), are simultaneously formed on the second passivation layer 192a and the emitter region 121 positioned at the front surface of the substrate 110 using an ALD method, respectively. Then, the second anti-reflection layer 132 formed of hydrogenated silicon nitride (SiNx:H) and the third anti-reflection layer 133 formed of hydrogenated silicon oxide (SiOx:H) are sequentially formed on the first anti-reflection layer 131 positioned on the front surface of the substrate 110 using the PECVD

method.

[0223] The solar cell shown in FIG. 5 is manufactured through the manufacturing processes illustrated in FIGS. 4A to 4F, except the formation method and the formation order of the anti-reflection layer 130a and the passivation layer 190a.

[0224] The third anti-reflection layer 133 and the second passivation layer 192a, each of which is formed of hydrogenated silicon oxide (SiOx:H) may have a thickness of about 50 nm to 100 nm and a refractive index of about 1.5.

[0225] As described above, the second anti-reflection layer 132 and the first passivation layer 191 formed of hydrogenated silicon nitride (SiNx:H) are respectively capped by the third anti-reflection layer 133 and the second passivation layer 192a formed of hydrogenated silicon oxide (SiOx:H). Hence, the passivation function performed by the second anti-reflection layer 132 and the first passivation layer 191 is further improved. Further, the passivation effect of the solar cell shown in FIG. 5 is further improved because of the passivation function performed by the third anti-reflection layer 133 and the second passivation layer 192a.

[0226] Because the anti-reflection layer 130a and the passivation layer 190a further include the third anti-reflection layer 133 and the second passivation layer 192a formed of hydrogenated silicon oxide (SiOx:H), the anti-reflection effect at the front surface and the back surface of the substrate 110 is improved. Hence, an amount of light incident on the substrate 110 increases, and an amount of electric current output from the solar cell increases.

[0227] Other examples of the solar cell shown in FIGS. 1 to 3 and the solar cell shown in FIG. 5 are described below with reference to FIGS. 6 and 7.

[0228] FIG. 6 illustrates another example of the solar cell shown in FIGS. 1 to 3, and FIG. 7 illustrates another example of the solar cell shown in FIG. 5.

[0229] The solar cells shown in FIGS. 6 and 7 further include a silicon oxide (SiOx) layer 180 between an emitter region 121 and an anti-reflection layer 130 (130a) and between a back surface of a substrate 110 and a first passivation layer 191, unlike the solar cell shown in FIGS. 1 to 3 and the solar cell shown in FIG. 5.

[0230] The solar cells shown in FIGS. 6 and 7 substantially have the same configuration as the solar cell shown in FIGS. 1 to 3 and the solar cell shown in FIG. 5, except the silicon oxide layer 180, respectively.

[0231] As shown in FIGS. 6 and 7, the silicon oxide layer 180 is positioned directly on the emitter region 121 positioned at a front surface of the substrate 110 and directly on the back surface of the substrate 110. The anti-reflection layer 130 (130a) and a passivation layer 190 (190a) are positioned directly on the silicon oxide layer 180.

[0232] The silicon oxide layer 180 is an oxide layer deliberately formed by immersing the substrate 110 in a desired chemical solution. A thickness of the silicon oxide

layer 180 may be about 2 nm to 3 nm.

[0233] In the method for manufacturing the solar cell illustrated in FIGS. 4A to 4F, after the emitter region 121 is formed, the silicon oxide layer 180 is formed before forming the anti-reflection layer 130 and the passivation layer 190.

[0234] The silicon oxide layer 180 is formed by immersing the substrate 110 in a nitric acid (HNO_3) solution having a hydrogen ion concentration (pH) of about 2 to 4 at a process temperature of the normal temperature to about 70 °C for about 5 minutes to 30 minutes. A concentration of HNO_3 in the HNO_3 solution, i.e., an amount of HNO_3 in the HNO_3 solution may be about 65 % to 70 %.

[0235] In the process for forming the anti-reflection layer 130 (130a) and the passivation layer 190 (190a) on the emitter region 121 and the back surface field regions 172, a natural oxide layer generated by oxygen existing in the atmosphere or the process room is generally formed directly on the emitter region 121. The natural oxide layer formed thus is unstably bonded to silicon existing in the substrate 110 or the emitter region 121, thereby generating a defect. In embodiments of the invention, the natural oxide layer is one that is formed spontaneously and unintentionally.

[0236] When the layer such as the aluminum oxide (Al_2O_3) layer is formed on the natural oxide layer, water (H_2O) is generated by the bond between hydrogen (H) contained in a process material for the layer formation and the natural oxide layer having the unstable bond. Further, a blistering phenomenon such as a spot resulting from the formation of a hydrogen molecule is generated.

[0237] However, in the embodiment of the invention, the silicon oxide layer 180 having the characteristics better than the natural oxide layer is formed directly on each of the front surface and the back surface of the substrate 110 using the separate PECVD method. Therefore, the frequency of problem generated by a bond of hydrogen and oxygen is greatly reduced.

[0238] Oxygen contained in the silicon oxide layer 180 performs the passivation function for converting the bonds existing at the surface of the substrate 110 into stable bonds, thereby further improving the surface passivation effect.

[0239] As shown in FIGS. 6 and 7, the silicon oxide layer 180 is formed on both the front surface and the back surface of the substrate 110. In another embodiment, the silicon oxide layer 180 may be formed on only one of the front surface and the back surface of the substrate 110.

[0240] As described above, the silicon oxide layer 180 is formed so as to improve the surface passivation effect at the front surface and the back surface of the substrate 110 and to reduce the problem resulting from the natural oxide layer. Therefore, the silicon oxide layer 180 is not required to be thick and may have a thickness of about 2 nm to 3 nm.

[0241] The embodiment of the invention was described based on a bifacial solar cell, in which light is incident on both the front surface and the back surface of the sub-

strate 110. The embodiment of the invention may be applied to other kinds of solar cells, for example, other kinds of solar cells using n-type single crystal silicon.

[0242] Although embodiments have been described with reference to a number of illustrative embodiments thereof, it should be understood that numerous other modifications and embodiments can be devised by those skilled in the art that will fall within the scope of the principles of this disclosure. More particularly, various variations and modifications are possible in the component parts and/or arrangements of the subject combination arrangement within the scope of the disclosure, the drawings and the appended claims. In addition to variations and modifications in the component parts and/or arrangements, alternative uses will also be apparent to those skilled in the art.

Claims

1. A solar cell comprising:

a substrate formed of an n-type crystalline semiconductor;
 an emitter region of a p-type positioned at a first surface of the substrate;
 a first dielectric layer positioned on a second surface opposite the first surface of the substrate;
 second dielectric layers respectively positioned on the emitter region and the first dielectric layer;
 a third dielectric layer positioned on the second dielectric layer that is positioned on the emitter region;
 a first electrode which is positioned on the first surface of the substrate and is connected to the emitter region; and
 a second electrode which is positioned on the second surface of the substrate and is connected to the substrate,
 wherein the emitter region has a first textured surface including a plurality of first protrusions each having a protruding height and a maximum diameter which are within a range of about 5 μm to 10 μm , and
 wherein each of the plurality of first protrusions has a second textured surface including a plurality of second protrusions each having a protruding height and a maximum diameter which are within a range of about 300 nm to 600 nm.

2. The solar cell of claim 1, wherein the first dielectric layer and the third dielectric layer are formed of hydrogenated silicon nitride.

3. The solar cell of claim 1, wherein the second dielectric layer is formed of aluminum oxide.

4. The solar cell of claim 3, wherein the second dielec-

tric layer has a thickness of about 5 nm to 15 nm.

5. The solar cell of claim 4, wherein each of the first dielectric layer and the third dielectric layer has a thickness of about 70 nm to 100 nm.

6. The solar cell of claim 3, further comprising a hydrogenated silicon oxide layer positioned between the first dielectric layer and the second dielectric layer that is positioned on the first dielectric layer.

7. The solar cell of claim 6, wherein the hydrogenated silicon oxide layer has a thickness of about 50 nm to 100 nm.

8. The solar cell of claim 1, further comprising a silicon oxide layer positioned between the second surface of the substrate and the first dielectric layer.

9. The solar cell of claim 8, wherein the silicon oxide layer has a thickness of about 2 nm to 3 nm.

10. The solar cell of claim 1, wherein the first surface and the second surface of the substrate are incident surfaces on which light is incident.

11. The solar cell of claim 1, further comprising a hydrogenated silicon oxide layer positioned on the third dielectric layer.

12. The solar cell of claim 11, wherein the hydrogenated silicon oxide layer has a thickness of about 50 nm to 100 nm.

13. The solar cell of claim 11, further comprising a silicon oxide layer positioned between the emitter region and the second dielectric layer.

14. The solar cell of claim 13, wherein the silicon oxide layer has a thickness of about 2 nm to 3 nm.

15. The solar cell of claim 1, wherein acicular ends of the plurality of second protrusions point in a parallel direction as vertices of the plurality of first protrusions.

FIG. 1

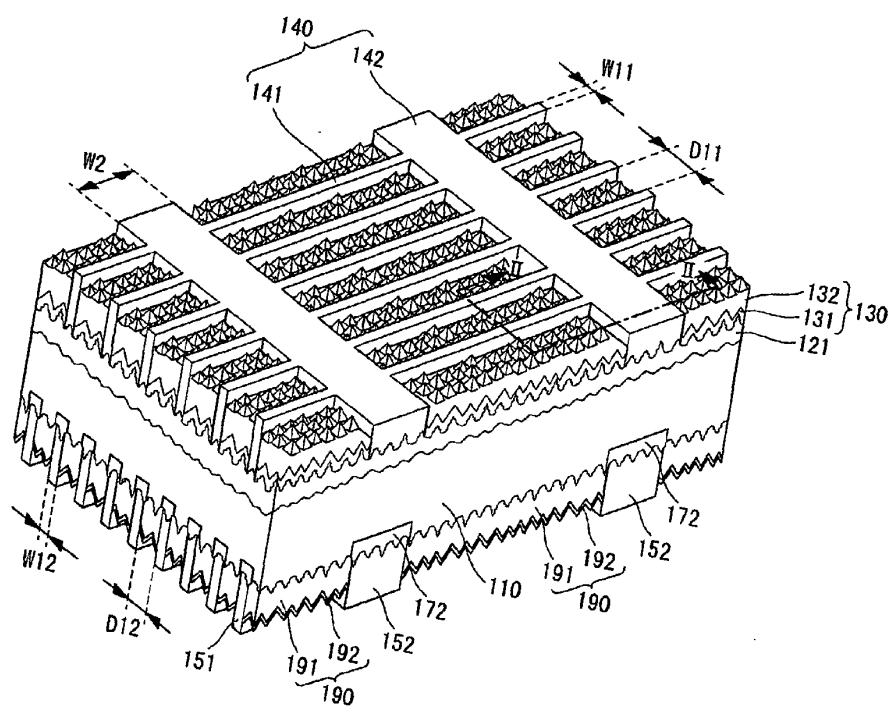


FIG. 2

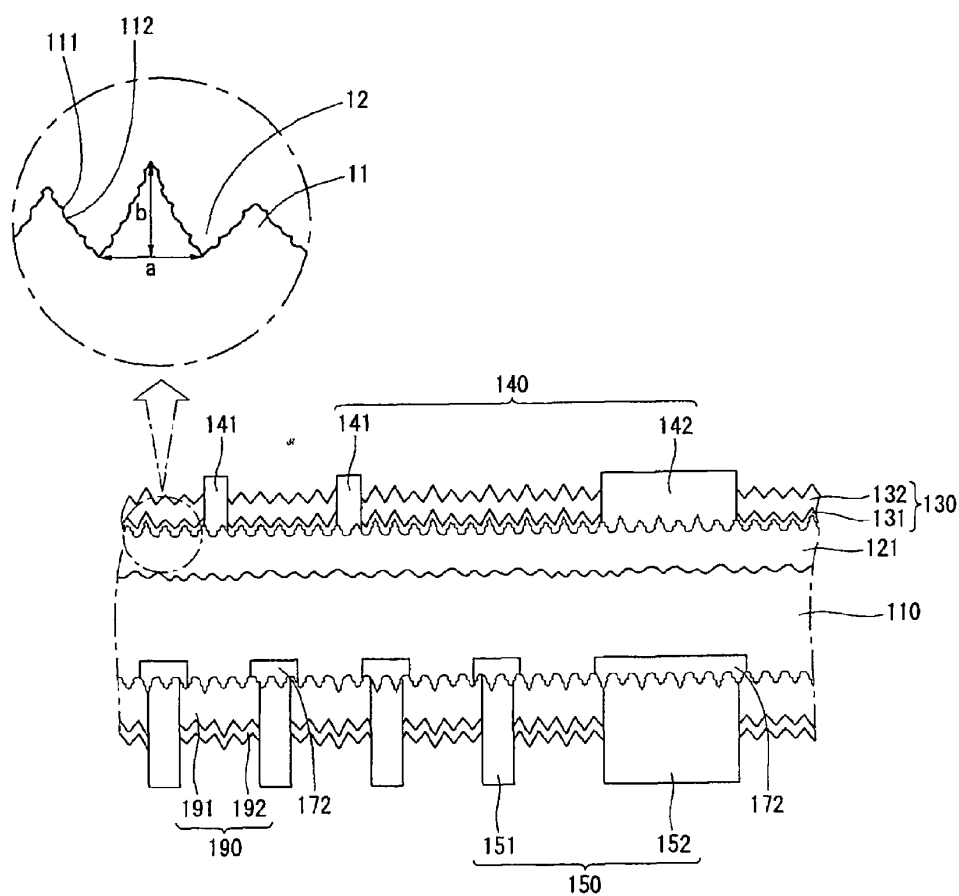


FIG. 3

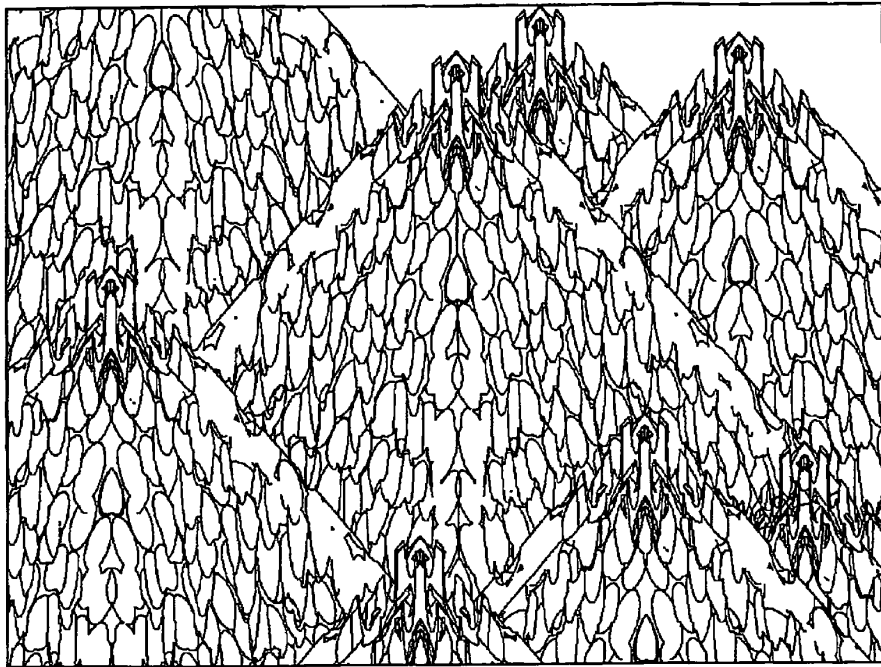


FIG. 4A

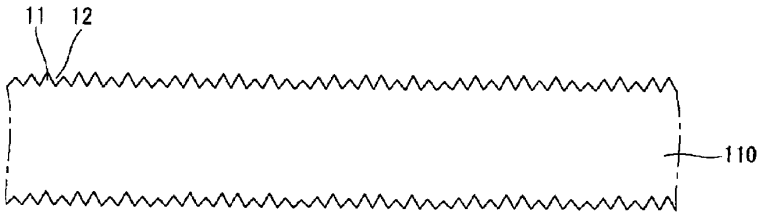


FIG. 4B

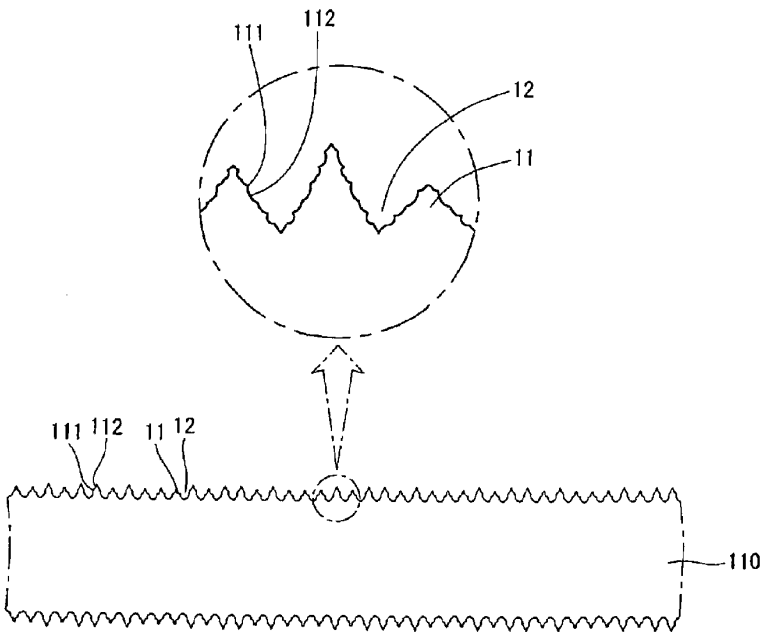


FIG. 4C

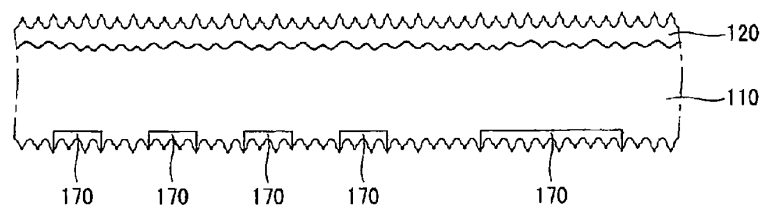


FIG. 4D

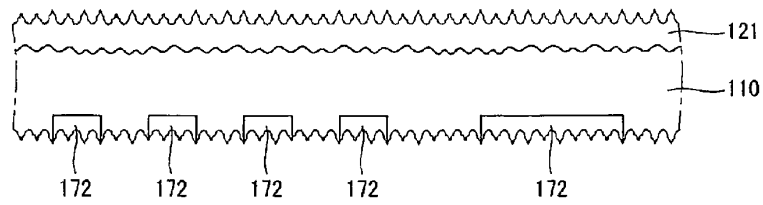


FIG. 4E

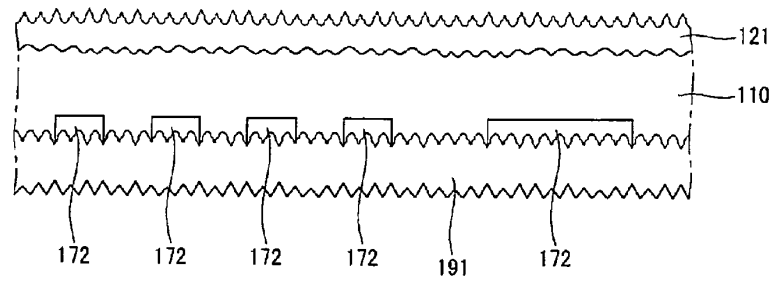


FIG. 4F

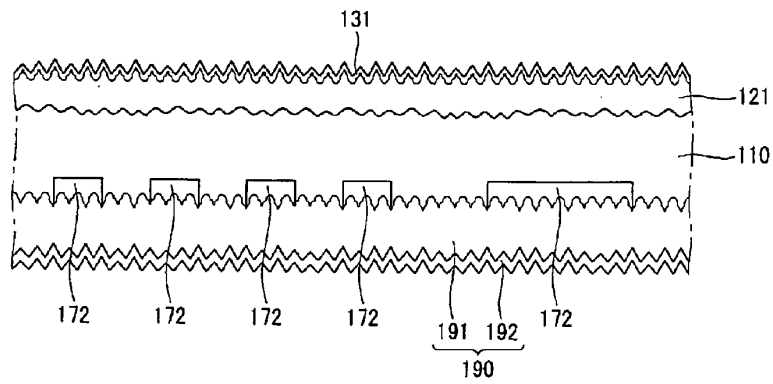


FIG. 4G

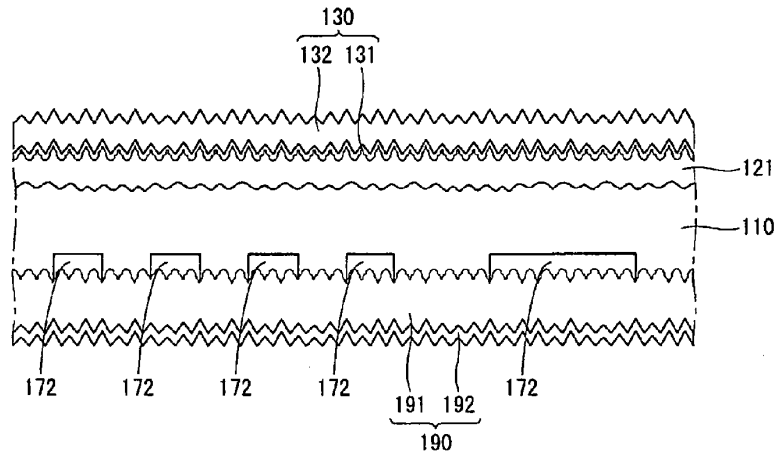


FIG. 4H

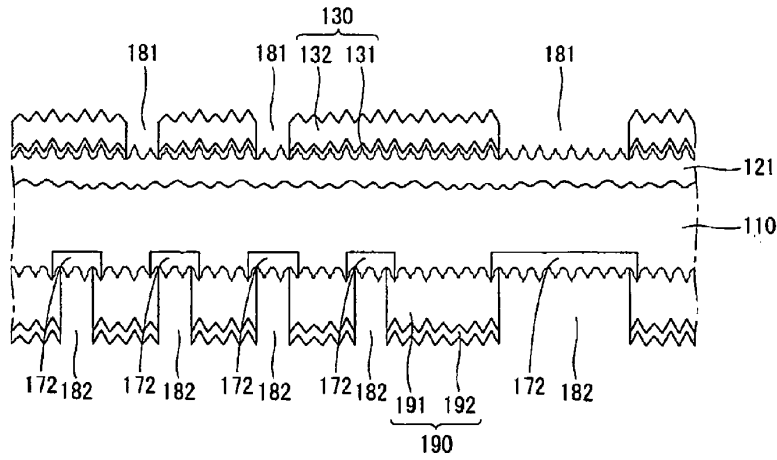


FIG. 5

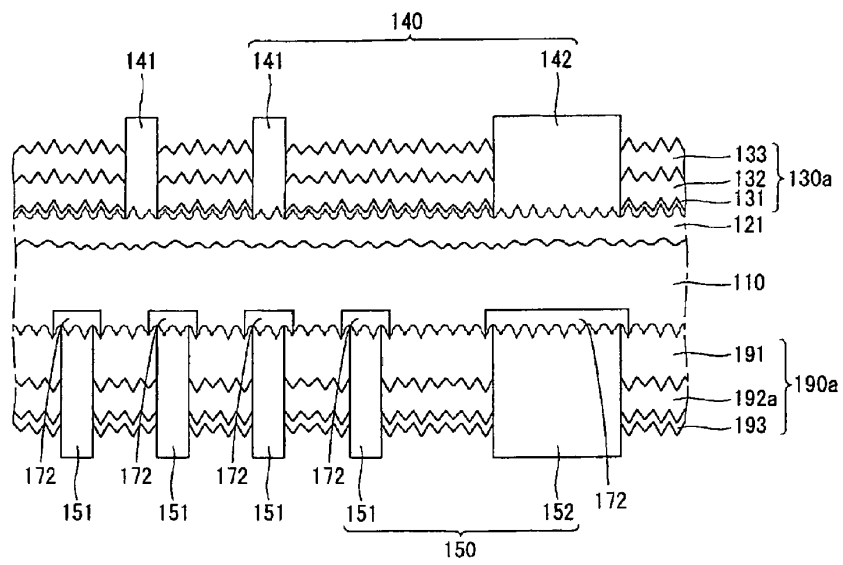


FIG. 6

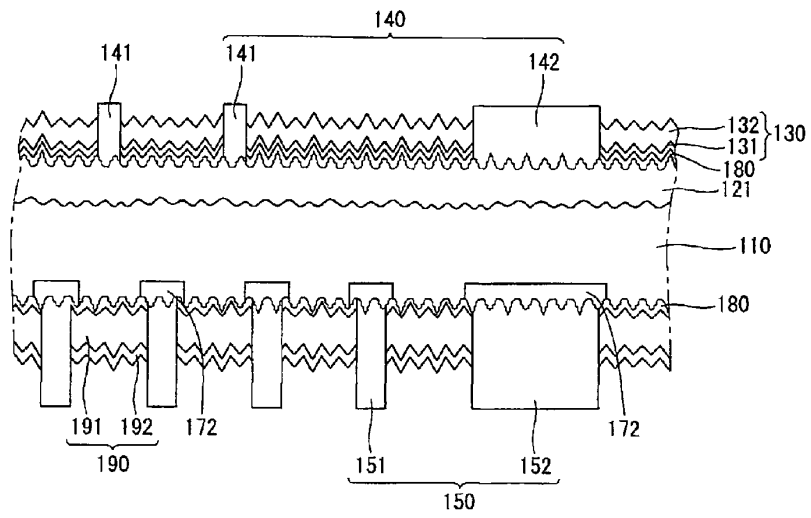
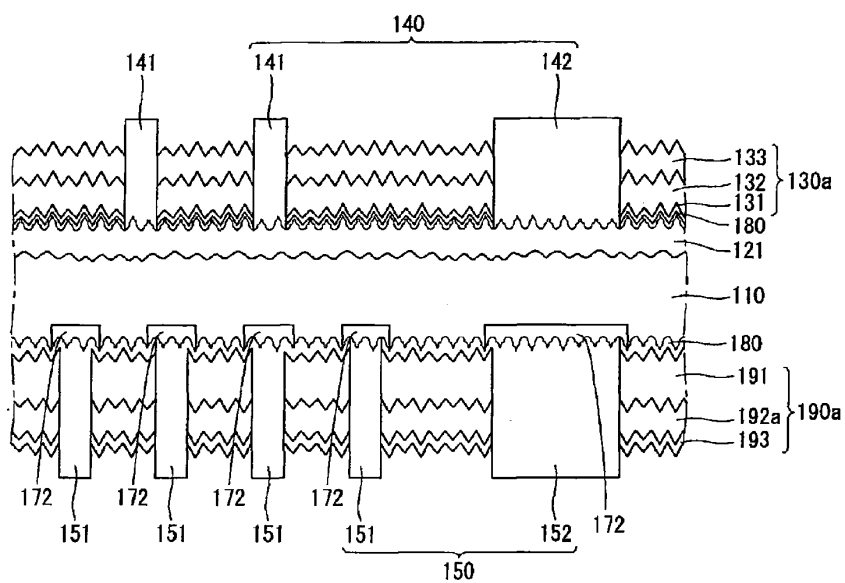


FIG. 7





EUROPEAN SEARCH REPORT

 Application Number
EP 12 00 6262

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (IPC)
X	EP 2 149 915 A2 (SAMSUNG ELECTRONICS CO LTD [KR] SAMSUNG ELECTRONICS CO LTD [KR]; SAMSU) 3 February 2010 (2010-02-03) * the whole document *	1-15	INV. H01L31/0236 H01L31/0216 H01L31/068
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A	US 2011/140226 A1 (JIN YOONSIL [KR] ET AL) 16 June 2011 (2011-06-16) * the whole document *	1-15	
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The present search report has been drawn up for all claims			
Place of search Berlin		Date of completion of the search 14 June 2013	Examiner Le Meur, M
CATEGORY OF CITED DOCUMENTS X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document		T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document	

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EPO FORM 1508 (08/02) (P04001)

**ANNEX TO THE EUROPEAN SEARCH REPORT
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EP 12 00 6262

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14-06-2013

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For more details about this annex : see Official Journal of the European Patent Office, No. 12/82



Espacenet

Bibliographic data: WO2015122257 (A1) — 2015-08-20

PHOTOELECTRIC CONVERSION ELEMENT

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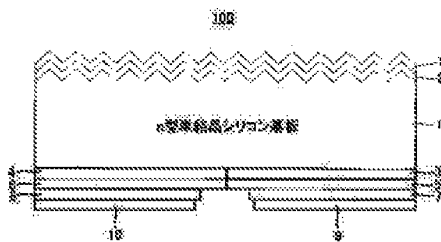
Classification: - international: H01L31/0248; H01L31/0747
- cooperative: H01L31/022441 (EP); H01L31/02366 (EP); H01L31/068 (EP);
H01L31/0747 (EP); H01L31/1804 (EP); Y02E10/547 (EP); Y02P70/50
(EP)

Application number: WO2015JP51790 20150123 Global Dossier

Priority number(s): JP20140025843 20140213

Abstract of WO2015122257 (A1)

A photoelectric conversion element (100) is provided with an n-type single-crystal silicon substrate (1). The n-type single-crystal silicon substrate (1) has a light-receiving surface on which a textured structure is formed, and a surface (back surface) opposed to the light-receiving surface and including macro-asperities having a difference in height of 0.5 μm or less and nano-asperities having an average surface roughness of 0.75 nm or less. The photoelectric conversion element (100) is provided with i-type amorphous semiconductor layers (3, 4), a p-type amorphous semiconductor layer (5), and an n-type amorphous semiconductor layer (6) on the side opposite to the light-receiving surface. The p-type amorphous semiconductor layer (5) is disposed on the i-type amorphous semiconductor layer (3), and the n-type amorphous semiconductor layer (6) is disposed on the i-type amorphous semiconductor layer (4). Consequently, a pn junction by hetero junction is formed on the back surface side of the n-type single-crystal silicon substrate (1).



1: n-type single-crystal silicon substrate

(12) 特許協力条約に基づいて公開された国際出願

(19) 世界知的所有権機関
国際事務局

(43) 国際公開日
2015 年 8 月 20 日(20.08.2015)



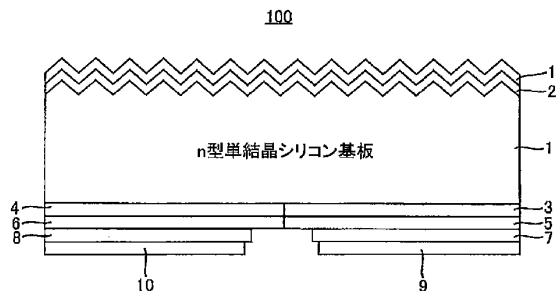
(10) 国際公開番号

WO 2015/122257 A1

- (51) 国際特許分類:
H01L 31/0248 (2006.01) H01L 31/0747 (2012.01)
- (21) 国際出願番号: PCT/JP2015/051790
- (22) 国際出願日: 2015 年 1 月 23 日(23.01.2015)
- (25) 国際出願の言語: 日本語
- (26) 国際公開の言語: 日本語
- (30) 優先権データ:
特願 2014-025843 2014 年 2 月 13 日(13.02.2014) JP
- (71) 出願人: シャープ株式会社(SHARP KABUSHIKI KAISHA) [JP/JP]; 〒5458522 大阪府大阪市阿倍野区長池町 2 番 2 号 Osaka (JP).
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- (81) 指定国 (表示のない限り、全ての種類の国内保護が可能): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.
- (84) 指定国 (表示のない限り、全ての種類の広域保護が可能): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), ユーロシア (AM, AZ, BY, KG, KZ, RU, TJ, TM), ヨーロッパ (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).
- 添付公開書類:
— 国際調査報告 (条約第 21 条(3))

(54) Title: PHOTOELECTRIC CONVERSION ELEMENT

(54) 発明の名称: 光電変換素子



1 n-type single-crystal silicon substrate

(57) Abstract: A photoelectric conversion element (100) is provided with an n-type single-crystal silicon substrate (1). The n-type single-crystal silicon substrate (1) has a light-receiving surface on which a textured structure is formed, and a surface (back surface) opposed to the light-receiving surface and including macro-asperities having a difference in height of 0.6 μm or less and nano-asperities having an average surface roughness of 0.75 nm or less. The photoelectric conversion element (100) is provided with i-type amorphous semiconductor layers (3, 4), a p-type amorphous semiconductor layer (5), and an n-type amorphous semiconductor layer (6) on the side opposite to the light-receiving surface. The p-type amorphous semiconductor layer (5) is disposed on the i-type amorphous semiconductor layer (3), and the n-type amorphous semiconductor layer (6) is disposed on the i-type amorphous semiconductor layer (4). Consequently, a pn junction by hetero junction is formed on the back surface side of the n-type single-crystal silicon substrate (1).

(57) 要約:

[続葉有]



光電変換素子（１００）は、 n 型単結晶シリコン基板（１）を備える。 n 型単結晶シリコン基板（１）は、テクスチャ構造が形成された受光面と、受光面に対して、高低差が $0.6\text{ }\mu\text{m}$ 以下であるマクロ凹凸と平均面粗さが 0.75 nm 以下であるナノ凹凸を含む表面（裏面）を有する。そして、光電変換素子（１００）は、 i 型非晶質半導体層（３、４）と、 p 型非晶質半導体層（５）と、 n 型非晶質半導体層（６）とを受光面と反対側に備える。 p 型非晶質半導体層（５）は、 i 型非晶質半導体層（３）上に配置され、 n 型非晶質半導体層（６）は、 i 型非晶質半導体層（４）上に配置される。これにより、ヘテロ接合による p - n 接合が n 型単結晶シリコン基板（１）の裏面側に形成される。

明 細 書

発明の名称：光電変換素子

技術分野

[0001] この発明は、光電変換素子に関するものである。

背景技術

[0002] 従来、単結晶シリコン基板を用いた光起電力装置では、(100)面を有するシリコン基板の表面をアルカリ溶液を用いて異方性エッチングすることにより、(111)面に起因したピラミッド状の凹凸形状を形成した光閉じ込め構造を用いることが知られている。

[0003] このような光閉じ込め構造は、ピラミッド状の凹凸形状により、シリコン基板の表面の反射率が低減されるので、短絡電流を増加させることができる。

[0004] 一方、n型単結晶シリコン基板とp型非晶質シリコン層との間に真性(i型)の非晶質シリコンを介在させて、その界面での欠陥を低減し、ヘテロ接合界面の特性を改善させたHIT(Heterojunction with Intrinsic Thin layer)構造の光起電力装置が知られている。

特許文献1：特開2011-77240号公報

発明の開示

[0005] 入射する太陽光がシリコン基板の表面で反射しないように、シリコン基板の表面にピラミッド状の凹凸形状を形成することで、シリコン基板の表面の反射率を下げる。

[0006] シリコン結晶系太陽電池では、一般に、シリコンの表面のダングリングバンドにより少数キャリアのライフタイムが低下する。このため、p型非晶質シリコン層とシリコン基板との間に真性(i型)の非晶質シリコンを成膜して高いパッシベーション効果を得ている。これにより、シリコン結晶の表面でのキャリアの消滅を抑制する。

[0007] しかし、ピラミッド構造が形成されたシリコン基板の表面に均一に非晶質

シリコンを成膜しても、均一に高いパッシベーション特性が得られるわけではない。そして、シリコン表面において均一に効果的なパッシベーション特性が得られない場合、太陽電池の変換効率が低下するという問題がある。

[0008] そこで、この発明の実施の形態によれば、テクスチャ構造によるパッシベーション特性の低下を抑制して変換効率を向上可能な光電変換素子を提供する。

[0009] この発明の実施の形態によれば、光電変換素子は、シリコン基板を備える光電変換素子であって、シリコン基板は、第1および第2の表面を有する。第1の表面は、テクスチャ構造が形成される。第2の表面は、第1の表面に対向するとともに、テクスチャ構造が形成されておらず、第1の凹凸および第2の凹凸を含む。第1の凹凸の高低差は、 $6\mu\text{m}$ 以下であり、第2の凹凸の平均面粗さは、 0.75nm よりも小さい。

[0010] 高低差が $0.6\mu\text{m}$ 以下である第1の凹凸と、平均面粗さが 0.75nm 以下である第2の凹凸とを含む第2の表面を有するシリコン基板を用いることにより、開放電圧が大きくなる。

[0011] 従って、テクスチャ構造によるパッシベーション特性の低下を抑制して変換効率を向上できる。

[0012] 好ましくは、第1の凹凸の高低差は、 $2\mu\text{m}$ 以下である。

[0013] 第1の凹凸の高低差が $2\mu\text{m}$ 以下であれば、第2の凹凸の平均面粗さが小さくなるに従って開放電圧が飛躍的に大きくできる。

[0014] 好ましくは、光電変換素子は、第1および第2の非晶質半導体層を更に備える。第1の非晶質半導体層は、第2の表面に接して配置され、実質的に*i*型の導電性を有する。第2の非晶質半導体層は、第1の非晶質半導体層に接して配置され、シリコン基板の導電型と反対の導電性を有する。

[0015] シリコン基板の受光面と反対側にヘテロ接合によるpn接合を設けた光電変換素子において、テクスチャ構造によるパッシベーション特性の低下を抑制して変換効率を向上できる。

[0016] 好ましくは、第2の凹凸の平均面粗さは、 0.40nm 以下である。

- [0017] 第1の凹凸の高低差が小さくなるに従って、開放電圧を飛躍的に大きくできる。
- [0018] 好ましくは、光電変換素子は、第3および第4の非晶質半導体層を更に備える。第3の非晶質半導体層は、第1の表面に接して配置され、実質的にi型の導電性を有する。第4の非晶質半導体層は、第3の非晶質半導体層に接して配置され、シリコン基板の導電型と同じ導電性を有する。
- [0019] シリコン基板の受光面が第3の非晶質半導体層によってパッシベートされ、光励起された少数キャリアの受光面側での再結合が抑制される。その結果、短絡電流が大きくなる。
- [0020] 従って、変換効率を向上できる。
- [0021] 好ましくは、光電変換素子が、第1から第5の非晶質半導体層を更に備える。第1の非晶質半導体層は、第1の表面に接して配置される。第2の非晶質半導体層は、第2の表面に接して配置され、実質的にi型の導電性を有する。第3の非晶質半導体層は、第2の表面に接して配置されるとともにシリコン基板の面内方向において第2の非晶質半導体層に隣接して配置され、実質的にi型の導電性を有する。第4の非晶質半導体層は、第2の非晶質半導体層に接して配置され、シリコン基板の導電型と反対の導電性を有する。第5の非晶質半導体層は、第3の非晶質半導体層に接して配置され、シリコン基板の導電型と同じ導電性を有する。
- [0022] ヘテロ接合によるpn接合が受光面と反対側に配置された光電変換素子において、シリコン基板の受光面側におけるキャリアの再結合を抑制して短絡電流が大きくなるとともに、開放電圧が大きくなる。
- [0023] 従って、シリコン基板の受光面と反対側にヘテロ接合によるpn接合を設けた光電変換素子において、テクスチャ構造によるパッシベーション特性の低下を更に抑制して変換効率を向上できる。
- [0024] また、シリコン基板は、実質的にi型の非晶質半導体層によって挟み込まれるので、光電変換素子の製造工程においてシリコン基板の熱歪を抑制してキャリアのライフタイムの低下を抑制できる。

- [0025] 好ましくは、第1の非晶質半導体層は、第6および第7の非晶質半導体層を含む。第6の非晶質半導体層は、シリコン基板の受光面に接して配置され、実質的にi型の導電型を有する。第7の非晶質半導体層は、第6の非晶質半導体層に接して配置され、シリコン基板の導電型と同じ導電型を有する。
- [0026] シリコン基板の受光面側におけるキャリアの再結合が更に抑制される。
- [0027] 従って、短絡電流を大きくして変換効率を更に向上できる。
- [0028] 高低差が0.6 μm 以下である第1の凹凸と、平均面粗さが0.75 nm以下である第2の凹凸とを含む第2の表面を有するシリコン基板を用いることにより、開放電圧が大きくなる。
- [0029] 従って、テクスチャ構造によるパッシベーション特性の低下を抑制して変換効率を向上できる。

図面の簡単な説明

- [0030] [図1]この発明の実施の形態1による光電変換素子の構成を示す断面図である。
- [図2]図1に示す光電変換素子の裏面側の電極の平面図である。
- [図3]n型単結晶シリコン基板の(100)面の顕微鏡写真を示す図である。
- [図4]フラット基板面のSEM写真を示す図である。
- [図5]AFM像を示す図である。
- [図6]平均面粗さと開放電圧との関係を示す図である。
- [図7]図1に示す光電変換素子の製造方法を示す第1の工程図である。
- [図8]図1に示す光電変換素子の製造方法を示す第2の工程図である。
- [図9]図1に示す光電変換素子の製造方法を示す第3の工程図である。
- [図10]実施の形態2による光電変換素子の構成を示す断面図である。
- [図11]図10に示す光電変換素子の製造方法を示す第1の工程図である。
- [図12]図10に示す光電変換素子の製造方法を示す第2の工程図である。
- [図13]n型単結晶シリコン基板の(100)面の顕微鏡写真を示す図である。
- [図14]実施の形態4による光電変換素子の構成を示す断面図である。

- [図15]図14に示す光電変換素子の製造方法を示す第1の工程図である。
- [図16]図14に示す光電変換素子の製造方法を示す第2の工程図である。
- [図17]図14に示す光電変換素子の製造方法を示す第3の工程図である。
- [図18]実施の形態5による光電変換素子の構成を示す断面図である。
- [図19]図18に示す光電変換素子の製造方法を示す第1の工程図である。
- [図20]図18に示す光電変換素子の製造方法を示す第2の工程図である。
- [図21]図18に示す光電変換素子の製造方法を示す第3の工程図である。
- [図22]この実施の形態による光電変換素子を備える光電変換モジュールの構成を示す概略図である。
- [図23]この実施の形態による光電変換素子を備える太陽光発電システムの構成を示す概略図である。
- [図24]図23に示す光電変換モジュールアレイの構成を示す概略図である。
- [図25]この実施の形態による光電変換素子を備える太陽光発電システムの構成を示す概略図である。

発明を実施するための最良の形態

- [0031] 本発明の実施の形態について図面を参照しながら詳細に説明する。なお、図中同一または相当部分には同一符号を付してその説明は繰返さない。
- [0032] この明細書において、アモルファスシリコンを「a-Si」と表記するが、この表記は、実際には、水素(H)原子が含まれていることを意味する。アモルファスシリコンカーバイド(a-SiC)、アモルファスシリコンオキサイド(a-SiO)、アモルファスシリコンナイトライド(a-SiN)、アモルファスシリコンオキサイドナイトライド(a-SiON)、アモルファスシリコンゲルマニウム(a-SiGe)およびアモルファスゲルマニウム(a-Ge)についても、同様に、H原子が含まれていることを意味する。更に、非晶質半導体層とは、完全に非晶質な半導体層、および微結晶半導体層を含むものとする。そして、微結晶半導体層とは、非晶質半導体層中に析出している半導体結晶の平均粒子径が1~50nmである半導体と言う。

[0033] [実施の形態 1]

図 1 は、実施の形態 1 による光電変換素子の構成を示す断面図である。図 1 を参照して、実施の形態 1 による光電変換素子 100 は、n 型単結晶シリコン基板 1 と、非晶質半導体層 2 と、i 型非晶質半導体層 3, 4 と、p 型非晶質半導体層 5 と、n 型非晶質半導体層 6 と、透明導電膜 7, 8 と、電極 9, 10 と、絶縁層 11 とを備える。

[0034] n 型単結晶シリコン基板 1 は、例えば、(100) の面方位および 0.1 ~ 10 $\Omega \cdot \text{cm}$ の比抵抗を有する。また、n 型単結晶シリコン基板 1 は、受光面がテクスチャ化されている。そして、n 型単結晶シリコン基板 1 の厚みは、例えば、100 ~ 150 μm である。

[0035] 非晶質半導体層 2 は、n 型単結晶シリコン基板 1 の受光面に接して n 型単結晶シリコン基板 1 上に配置される。

[0036] i 型非晶質半導体層 3, 4 は、n 型単結晶シリコン基板 1 の裏面（テクスチャ構造が形成された表面と反対側の表面）に接して n 型単結晶シリコン基板 1 上に配置される。

[0037] p 型非晶質半導体層 5 は、i 型非晶質半導体層 3 に接して i 型非晶質半導体層 3 上に配置される。

[0038] n 型非晶質半導体層 6 は、i 型非晶質半導体層 4 に接して i 型非晶質半導体層 4 上に配置される。

[0039] 透明導電膜 7 は、p 型非晶質半導体層 5 に接して p 型非晶質半導体層 5 上に配置される。

[0040] 透明導電膜 8 は、n 型非晶質半導体層 6 に接して n 型非晶質半導体層 6 上に配置される。

[0041] 電極 9 は、透明導電膜 7 に接して透明導電膜 7 上に配置される。

[0042] 電極 10 は、透明導電膜 8 に接して透明導電膜 8 上に配置される。

[0043] 絶縁層 11 は、非晶質半導体層 2 に接して非晶質半導体層 2 上に配置される。

[0044] 非晶質半導体層 2 は、i 型非晶質半導体層 / n 型非晶質半導体層、または

n型非晶質半導体層からなる。非晶質半導体層2がi型非晶質半導体層／n型非晶質半導体層からなる場合、i型非晶質半導体層がn型単結晶シリコン基板1に接して配置され、n型非晶質半導体層がi型非晶質半導体層に接して配置される。

[0045] i型非晶質半導体層は、i型a-Siからなる。そして、i型非晶質半導体層は、1～10nmの厚みを有し、例えば、3nmの厚みを有する。

[0046] n型非晶質半導体層は、n型a-Siからなる。そして、n型非晶質半導体層は、2～50nmの厚みを有し、例えば、12nmの厚みを有する。

[0047] なお、非晶質半導体層2がn型非晶質半導体層のみからなる場合、n型非晶質半導体層は、3～60nmの厚みを有し、例えば、15nmの厚みを有する。

[0048] このように、非晶質半導体層2は、n型単結晶シリコン基板1と同じ導電型のn型非晶質半導体層を少なくとも含む。その結果、非晶質半導体層2は、n型単結晶シリコン基板1中で生成された少数キャリア（正孔）が絶縁層11へ到達するのを抑制し、短絡電流を向上できる。

[0049] i型非晶質半導体層3、4の各々は、i型a-Siからなる。そして、i型非晶質半導体層3は、1～10nmの厚みを有し、例えば、2nmの厚みを有する。また、i型非晶質半導体層4は、1～10nmの厚みを有し、例えば、3nmの厚みを有する。このように、i型非晶質半導体層4の厚みは、i型非晶質半導体層3の厚みと異なる。なお、i型非晶質半導体層4の厚みは、i型非晶質半導体層3の厚みと同じであってもよい。

[0050] p型非晶質半導体層5は、p型a-Siからなる。p型非晶質半導体層5は、2～50nmの厚みを有し、例えば、25nmの厚みを有する。そして、p型非晶質半導体層5は、例えば、ボロン（B）をp型不純物として含み、B濃度は、例えば、 $1 \times 10^{19} \text{ cm}^{-3} \sim 1 \times 10^{20} \text{ cm}^{-3}$ である。

[0051] n型非晶質半導体層6は、n型a-Siからなる。n型非晶質半導体層6は、2～50nmの厚みを有し、例えば、15nmの厚みを有する。そして、n型非晶質半導体層6は、例えば、リン（P）をn型不純物として含み、

P濃度は、例えば、 $1 \times 10^{19} \text{ cm}^{-3} \sim 1 \times 10^{20} \text{ cm}^{-3}$ である。

[0052] 透明導電膜 7, 8 の各々は、ITO、 SnO_2 および ZnO 等からなる。そして、透明導電膜 7, 8 の各々は、70～100 nmの厚みを有する。

[0053] 電極 9, 10 の各々は、Ag, Cu, Sn, Pt, Au等の金属、それらの金属のうちの1種以上を含む合金等の導電性材料からなる。また、電極 9, 10 の各々は、上述した金属の単膜であってもよいし、透明導電膜と上記金属との多層膜であってもよい。

[0054] 絶縁層 11 は、反射防止膜としての機能と保護膜としての機能とを有する。絶縁層 11 は、シリコンまたはアルミニウムの窒化物、酸窒化物および酸化物、チタニウム、ジルコニウム、ニオブウム、イットリウムおよびタンタルウム等の酸化物等からなり、一般的には、可視光領域に大きな吸収を持たない誘電体からなる。また、絶縁層 11 は、上記の単体の膜であってもよく、好ましく、上記から選択された材料の多層膜からなる。そして、絶縁層 11 は、80～300 nmの厚みを有する。これにより、n型単結晶シリコン基板 1 の表面における反射率を低下させることができ、短絡電流を増加させることができる。また、非晶質半導体層 2 の表面のパッシベーションを考慮すると、絶縁層 11 を窒化シリコンまたは酸窒化シリコンによって構成することが好ましい。

[0055] 図 2 は、図 1 に示す光電変換素子 100 の裏面側の電極 9, 10 の平面図である。図 2 を参照して、電極 9, 10 の各々は、楕形を有する。そして、電極 9 の楕形は、電極 10 の楕形と噛み合うように配置される。

[0056] 図 3 は、n型単結晶シリコン基板 1 の(100)面の顕微鏡写真を示す図である。光電変換素子に用いられるシリコン基板は、低コストの観点から、通常、CMP (Chemical Mechanical Polishing) 等のミラー化処理を行っていない。そして、CMPのように機械的な研磨工程を用いずに、化学的なエッチングでシリコン基板を平坦化させている。この発明の実施の形態においては、このような基板面をフラット基板面と呼ぶ。このため、フラット基板面は、図 3 の(a)に示すように、凹凸を有する基板表面になっているが、

一般的なテクスチャ構造と異なる。

- [0057] フラット基板の作製工程としては、バルクのシリコンからワイヤーソウにより、バルクシリコンをスライスし、ウェハー状に加工する。厚みは、 $100 \sim 300 \mu\text{m}$ 程度である。スライスされたシリコン基板の表面には、スライス時のダメージ層が数 μm から数十 μm 程度の深さで存在し、表面の凹凸も、同様の深さである。このため、表面のダメージ層および凹凸を除去し、平坦化させるために、エッチングを行う。ここでは、このエッチングをダメージ層除去エッチング工程と呼ぶ。ダメージ層除去エッチング工程においては、工程の安定化のために、一般的に、水酸化ナトリウム (NaOH) 等のアルカリ溶液が用いられる。
- [0058] アルカリ溶液（例えば、 NaOH エッチング液：10%、 H_2O 希釈、80℃で2分程度）を用いると、図3の（a）に示すように、四角形の凹凸が重なるように形成される。これは、アルカリ溶液でシリコン基板をエッチングすると、異方性エッチングにより、ピラミッド状のテクスチャ構造が、一部、形成されるからである。
- [0059] 即ち、エッチング温度および濃度を調整することで、完全なピラミッド形状を発生させることなく、エッチングすることができる。しかし、完全にピラミッド形状の発生を抑制することが困難であるため、図3の（a）に示すように、四角形の凹凸形状が形成されることになる。
- [0060] この四角形の凹凸形状を、この発明の実施の形態においては、「マクロ凹凸」と呼ぶ。このマクロ凹凸は、1辺の長さが $10 \sim 50 \mu\text{m}$ 程度の四角形であり、レーザ顕微鏡等で深さを測定すると、浅いもので500nm程度から数 μm 程度のものまで、幅広い範囲で存在している（図3の（b））。
- [0061] また、斜面の角度は、10度から30度くらいで、多くは、20度程度である。ここでの斜面の角度は、図3の（b）に示すように、基板表面（（100）面）と四角形の形状の斜面部とのなす角度である。
- [0062] 更に、シリコンの光吸収係数等から、太陽光を効率よく吸収する適正な基板厚にするために、フッ硝酸等の酸系のエッチングを用いて、基板厚を10

0～150 μm 程度に薄くエッチングする。この場合、酸系エッチングは、等方性エッチングであるため、先に形成されたマクロ凹凸の形状は、維持される。

[0063] このようにしてシリコン基板を作製した後、シリコン基板の裏面に保護膜 (SiO_2 , SiN 等) を形成する。保護膜の厚みは、1～2 μm 程度である。保護膜は、スパッタリング法、電子ビーム蒸着およびTEOS法等の方法によって形成される。保護膜が形成されているシリコン基板の表面は、アルカリ系エッチャントでは、エッチングされないため、テクスチャ構造が形成されない。

[0064] 従って、テクスチャ構造が片面だけに形成され、他の面がフラット面となるシリコン基板を作製できる。そして、フラット面が形成された面は、裏面側になる。その後、保護膜をフッ酸等でエッチングすることによって除去する。

[0065] このようにして、テクスチャ構造が片面だけに形成されたn型単結晶シリコン基板1を作製できる。

[0066] 上述したように、マクロ凹凸が基板全面に形成され、テクスチャ構造が形成されていないフラット基板面には、 μm オーダーの凹凸が形成される。

[0067] 図4は、フラット基板面のSEM (Scanning Electron Microscope) 写真を示す図である。

[0068] 図4を参照して、 μm オーダーの凹凸が形成されているが、段差は、四角形の周辺のためのため、テクスチャ構造のように、反射率を低減する効果は、非常に小さい。そのため、フラット基板面は、テクスチャ構造が形成された表面とは、大きく役割が異なる。

[0069] また、テクスチャ構造の場合には、頂点領域および底部領域がピラミッド形状には必ず存在しており、フラット面には、このような頂点領域および底部領域が存在しない。この頂点部および底部は、少数キャリアのライフタイムの低下を引き起こすキャリア再結合中心になることは、よく知られているが、フラット基板面には、ほぼ存在しないため、この種のロス、起こり難

く、テクスチャ構造が形成された面よりも、良好なパッシベーションを行うことができる。

- [0070] しかし、フラット基板面には、別の問題が存在する。上述したとおり、マクロ凹凸の斜面部は、 $10 \sim 30$ 度程度の角度を持っている。ピラミッド状のテクスチャ構造では、異方性エッチングによって、 (111) 面が現れるため、 (100) 面との角度が 54.7 度になる、エッチング条件によっては、完全に 54.7 度に一致させることは困難であるため、少し傾きが緩くなるが、それでも、 50 度程度となる。
- [0071] 上記のように、テクスチャ構造と、フラット基板面に形成されるマクロ凹凸とは、シリコンの面方位が大きく異なる。このため、CVD法によってアモルファスシリコンを堆積した時に、パッシベーションのメカニズムが大きく異なる。
- [0072] また、フラット基板面がテクスチャ構造を有する面と異なることは、フラット基板面は、非常に微細なnmオーダーのナノ凹凸を有することである。
- [0073] 図3に示したマクロ凹凸の底部領域Aにおいて、 $2 \mu\text{m}$ 角の範囲で凹凸形状をAFM (Atomic Force Microscope) を用いて測定した。その結果を図5に示す。図5は、AFM像を示す図である。図5の(a)は、高さ分布を示すAFM像であり、図5の(b)は、高さ分布の微分像である。
- [0074] 図5から解るように、数十nmから 100 nm 程度の微細な凹凸が形成されている。上述したマクロ凹凸と比べても、大きさが桁で大きく異なり、全く異なる。高さも、数nm程度の高さを有しており、数nm程度の高さが基板の全面に形成されている。
- [0075] このように、化学エッチングのみで基板の平坦化を行った場合には、非常に複雑な大きささまざまな大きさまたは形状の凹凸が形成されており、テクスチャ構造が形成された面とは、全く異なる形状の表面になる。
- [0076] この発明の実施の形態においては、この凹凸を「ナノ凹凸」と呼び、大きさが $1 \mu\text{m}$ よりも小さく、高さが 100 nm よりも小さいnmオーダーの凹凸をナノ凹凸と定義する。また、大きさが $10 \mu\text{m}$ 以上であり、高低差が1

00nm以上である凹凸をマクロ凹凸と定義する。

[0077] このように、この発明の実施の形態においては、マクロ凹凸およびナノ凹凸を上記のように定義しているが、「マクロ凹凸が2μm以下の基板」と記載しても、基板の全ての領域で完全に2μm以下に形成されているわけではなく、異常個所が一部形成されている場合がある。この場合においても、その異常個所が、面積的に非常に小さいため、この発明の実施の形態に記載された効果が影響を受けるわけではない。そのため、マクロ凹凸が2μm以下、若しくは、ナノ凹凸が0.75nm以下と記載している場合であっても、シリコン基板の全面積の90%以上の面積が、記載の範囲に入っていれば問題ないものとする。

[0078] このように、この発明の実施の形態においては、n型単結晶シリコン基板1は、受光面（テクスチャ構造が形成された表面）と反対側の表面に、マクロ凹凸およびナノ凹凸を有することを特徴とする。

[0079] （表面凹凸とセル特性との相関）

ナノ凹凸の凹凸を制御することができるかを調べた結果、フッ酸および硝酸濃度を変えたフッ硝酸溶液にシリコン基板を浸すことにより、ナノ凹凸の大きさを変化させることが可能であることが解った。

[0080] ナノ凹凸の大きさを、AFMで測定された平均面粗さRaによって定義することにする。

[0081] 平均面粗さRaとは、AFMで測定した面の凹凸量を定量化する指標であって、次の式によって定義される。

[0082] [数1]

$$Ra = \frac{1}{n} \sum_{i=1}^n |Z(i) - Ze| \quad \cdots (1)$$

[0083] 式(1)において、Zeは、面の高さの平均値であり、nは、測定点の数である。

[0084] ここで、フッ硝酸溶液は、以下の2種類の溶液を使用した。

[0085] 溶液(A) HF : HNO₃ : H₂O = 8.3重量% : 50.0重量% : 4

1. 7 重量%

溶液 (B) $\text{HF} : \text{HNO}_3 : \text{H}_2\text{O} = 4.5 \text{ 重量\%} : 54.5 \text{ 重量\%} : 4$

1. 0 重量%

これらの溶液 (A), (B) に浸す前の平均面粗さ R_a は、 $R_a = 0.75 \text{ nm}$ であったが、溶液 (A) によって、 $R_a = 0.26 \text{ nm}$ になり、溶液 (B) によって、 $R_a = 0.34 \text{ nm}$ になった。

[0086] フッ酸濃度が高い溶液 (A) で処理する方が平均面粗さ R_a が小さくなった。フッ酸濃度が高い溶液ほど、平均面粗さ R_a が小さくなり、凹凸の高さが低く平坦に近い状態になることが解った。

[0087] なお、この場合、シリコン基板の厚みは、溶液 (A), (B) で処理を行った後の厚みが同じになるように揃えた。

[0088] フッ酸濃度および硝酸濃度は、上記に限らず、適宜設定することができる。

[0089] これらの基板を用いて図 1 に示す構造の光電変換素子を作製した。光電変換素子の大きさは、 2 cm 角であり、シリコン基板 (125 mm 角) 内に 4 行 $\times$ 4 列に等間隔に光電変換素子を作製した。

[0090] 図 6 は、平均面粗さと開放電圧との関係を示す図である。図 6 において、縦軸は、開放電圧を表わし、横軸は、平均面粗さを表わす。また、開放電圧は、マクロ凹凸の高低差が $6 \mu\text{m}$ であり、平均面粗さ R_a が 1.15 nm であるときの開放電圧で規格化されている。

[0091] 図 6 を参照して、開放電圧 V_{oc} は、マクロ凹凸の各高低差に対して、平均面粗さ R_a が小さくなるに従って大きくなる。

[0092] また、平均面粗さ R_a が 0.75 nm よりも大きい領域では、開放電圧 V_{oc} は、マクロ凹凸の高低差が小さくなっても、殆ど変化しない。しかし、平均面粗さ R_a が 0.75 nm 以下の領域においては、マクロ凹凸の高低差が $6 \mu\text{m}$ 以下であれば、開放電圧 V_{oc} が改善される。また、マクロ凹凸の高低差が $6 \mu\text{m}$ 以下の範囲において小さくなるに従って、開放電圧 V_{oc} の改善率が高くなる。

- [0093] ナノ凹凸が大きい場合は、マクロ凹凸の高低差を小さくして平坦化しても、開放電圧 V_{oc} の大きな改善は得られないが、ナノ凹凸が 0.75 nm 以下である場合には、マクロ凹凸の高低差を小さくすることが開放電圧 V_{oc} の改善に有効であることが解った。
- [0094] マクロ凹凸の高低差が $2\text{ }\mu\text{m}$ 以下であることが好ましい。また、マクロ凹凸の高低差が $1\text{ }\mu\text{m}$ 以下であり、ナノ凹凸の平均面粗さが 0.4 nm 以下であることが更に好ましい。 0.4 nm 以下では、平坦性が向上することで、電極を形成したときの密着性に関して均一になるため、電極剥がれが抑制される効果が得られた。
- [0095] このように、開放電圧 V_{oc} がマクロ凹凸およびナノ凹凸と相関を持つことに関しては、次のように考えられる。
- [0096] (100) 面上のマクロ凹凸は、上述したように、 (100) 面から主として 20 度程度の角度を持ち、テクスチャ構造の (111) 面とは異なる結晶面を露出する。この斜面部に平均面粗さ R_a が大きいナノ凹凸が形成されると、キャリアの再結合中心が大きくなるものと考えられる。斜面部の領域の面積が大きくなると、開放電圧 V_{oc} が、より低くなると考えられ、マクロ凹凸の高低差を小さくすることで、斜面部の面積が減少するものと考えられる。
- [0097] 上述したように、開放電圧 V_{oc} は、平均面粗さ R_a が小さくなるに従って大きくなる。光電変換素子 100 の構造では、 pn 接合は、 n 型単結晶シリコン基板 1 と、 n 型単結晶シリコン基板 1 上に堆積された p 型非晶質半導体層 5 との間で形成されるため、 pn 接合の界面の形状が開放電圧 V_{oc} に影響を及ぼす。即ち、平均面粗さ R_a が小さく、平坦な界面で形成された pn 接合ほど、高い開放電圧 V_{oc} が得られることが解った。
- [0098] ナノ凹凸は、フッ硝酸の濃度（フッ酸と硝酸の混合比）で平均面粗さ R_a が決定される。エッチング時間によらず、濃度で凹凸を制御できることが解った。
- [0099] それに対して、エッチング時間を調整することで、マクロ凹凸は、形状が

変化していくことが解った。マクロ凹凸に見られる四角形の凹部は、エッチング時間が長くなることで徐々にエッチングが進み、四角形の形状の深さ（周りとの高低差）が小さくなっていく。また、四角形の形状の傾斜部の角度も、20度程度から徐々に小さくなっていく。

[0100] 光電変換素子の特性を決定する開放電圧 V_{oc} は、シリコン基板の表面ラフネスと強い相関があることが解った。表面ラフネスとは、マクロ凹凸およびナノ凹凸の両方に依存しており、更に、お互いのラフネスが相互に影響していることが解った。

[0101] 上述したように、マクロ凹凸の高低差が $6\ \mu\text{m}$ 以下であり、ナノ凹凸の平均面粗さが $0.75\ \text{nm}$ 以下であれば、開放電圧 V_{oc} が改善されるので、 n 型単結晶シリコン基板 1 は、テクスチャ構造が形成された表面に対向し、マクロ凹凸が $0.6\ \mu\text{m}$ 以下であり、かつ、ナノ凹凸の平均面粗さが $0.75\ \text{nm}$ 以下である表面（裏面）を有する。

[0102] 図 7 から図 9 は、それぞれ、図 1 に示す光電変換素子 100 の製造方法を示す第 1 から第 3 の工程図である。

[0103] 光電変換素子 100 の製造方法について説明する。光電変換素子 100 は、プラズマ装置を主に用いてプラズマ CVD（Chemical Vapour Deposition）法によって製造される。

[0104] プラズマ装置は、例えば、 $13.56\ \text{MHz}$ の RF 電力を整合器を介して平行平板電極に印加する電源を備える。

[0105] 光電変換素子 100 の製造が開始されると、シリコンのインゴットからスライスされたシリコン基板を上述した溶液（A）でエッチングしてマクロ凹凸およびナノ凹凸を有する n 型単結晶シリコン基板 1 を作製する（図 7 の工程（a）参照）。

[0106] その後、 n 型単結晶シリコン基板 1 の一方の表面に $100\sim300\ \text{nm}$ 程度の厚みを有する酸化シリコン（ SiO_2 ）をスパッタリング法によって形成し、1重量%～5重量%の水酸化カリウム（ KOH ）および1重量%～10重量%のイソプロピルアルコール（IPA）を用いて $80^\circ\text{C}\sim90^\circ\text{C}$ の温

度で、30分間、n型単結晶シリコン基板1の表面を化学的に異方性エッチングし、n型単結晶シリコン基板1の他方の表面をテクスチャ化する（図7の工程（b）参照）。この場合、形成されたピラミッド形状の傾斜角度は、50度と60度との間である。

[0107] その後、n型単結晶シリコン基板1をフッ酸中に浸漬してn型単結晶シリコン基板1の表面に形成された自然酸化膜を除去するとともに、n型単結晶シリコン基板1の表面を水素で終端する。

[0108] n型単結晶シリコン基板1の洗浄が終了すると、n型単結晶シリコン基板1をプラズマ装置の反応室に入れる。

[0109] そして、非晶質半導体層2をn型単結晶シリコン基板1の受光面（テクスチャ構造が形成された表面）にプラズマCVD法によって形成する（図7の工程（c）参照）。非晶質半導体層2がi型非晶質半導体層／n型非晶質半導体層からなる場合、i型非晶質半導体層は、例えば、40 s c c mのシラン（ SiH_4 ）ガスと、0 s c c m～100 s c mの水素（ H_2 ）ガスとを反応室に流し、圧力を40 P a（40～120 P a）に設定し、基板温度を170℃（130～180℃）に設定し、8.33 mW／c m²（5～15 mW／c m²）のパワー密度を有するRFパワーを整合器を介して平行平板電極に印加することによって形成される。なお、 SiH_4 ガスの H_2 ガスによる希釈率は、5倍以下である。

[0110] また、n型非晶質半導体層は、例えば、40 s c c mの SiH_4 ガスと、0 s c c m～100 s c mの H_2 ガスと、水素希釈された40 s c c mのフォスフィン（ PH_3 ）ガスとを反応室に流し、圧力を40 P a（40～120 P a）に設定し、基板温度を170℃（130～180℃）に設定し、8.33 mW／c m²（5～15 mW／c m²）のパワー密度を有するRFを整合器を介して平行平板電極に印加することによって形成される。なお、水素希釈された PH_3 ガスの濃度は、例えば、1％である。

[0111] 非晶質半導体層2がn型非晶質半導体層のみからなる場合、n型非晶質半導体層は、上記の形成条件を用いて形成される。

- [0112] 工程(c)の後、上述したi型非晶質半導体層と同じ形成条件を用いて、i型非晶質半導体層20をプラズマCVD法によってn型単結晶シリコン基板1の裏面(テクスチャ構造が形成された表面と反対側の表面)に形成する(図7の工程(d)参照)。
- [0113] そして、40sccmのSiH₄ガスと、0sccm~100sccmのH₂ガスと、水素希釈された40sccmのジボラン(B₂H₆)ガスとを反応室に流し、圧力を40Pa(40~120Pa)に設定し、基板温度を170℃(130~180℃)に設定し、5~15mW/cm²のパワー密度を有するRFパワーを整合器を介して平行平板電極に印加する。これによって、p型非晶質半導体層30がi型非晶質半導体層20上に形成される(図7の工程(e)参照)。
- [0114] その後、p型非晶質半導体層30の全面にレジストを塗布し、その塗布したレジストをフォトリソグラフィによってパターンニングしてレジストパターン40を形成する(図8の工程(f)参照)。
- [0115] そして、レジストパターン40をマスクとしてi型非晶質半導体層20およびp型非晶質半導体層30の一部をエッチングし、i型非晶質半導体層3およびp型非晶質半導体層5を形成する(図8の工程(g)参照)。
- [0116] 引き続いて、上述したi型非晶質半導体層と同じ形成条件を用いてi型非晶質半導体層50をn型単結晶シリコン基板1およびレジストパターン40上に堆積し、その後、n型非晶質半導体層と同じ形成条件を用いてn型非晶質半導体層60をi型非晶質半導体層50上にプラズマCVD法によって形成する(図8の工程(h)参照)。
- [0117] そして、アルカリ溶液(KOH, NaOH)を用いてレジストパターン40を除去する。これによって、レジストパターン40上に形成されたi型非晶質半導体層/n型非晶質半導体層がリフトオフにより除去され、i型非晶質半導体層4およびn型非晶質半導体層6が形成される(図8の工程(i)参照)。
- [0118] その後、例えば、窒化シリコンからなる絶縁層11を非晶質半導体層2上

にスパッタリング法によって形成する（図9の工程（j）参照）。

[0119] そして、p型非晶質半導体層5およびn型非晶質半導体層6の全面に透明導電膜（ITO）をスパッタリング法によって形成し、引き続いて、電子ビーム蒸着法によってAgを形成する。そして、透明導電膜（ITO）およびAgをエッチングし、透明導電膜7、8および電極9、10を形成する（図9の工程（k）参照）。これによって、光電変換素子100が完成する。

[0120] なお、上記においては、i型非晶質半導体層3／p型非晶質半導体層5を形成した後にi型非晶質半導体層4／n型非晶質半導体層6を形成すると説明したが、実施の形態1においては、これに限らず、i型非晶質半導体層4／n型非晶質半導体層6を形成した後にi型非晶質半導体層3／p型非晶質半導体層5を形成してもよい。

[0121] 光電変換素子100のn型単結晶シリコン基板1は、マクロ凹凸の高低差が0.6μm以下であり、かつ、ナノ凹凸の平均面粗さが0.75nm以下である表面をテクスチャ構造が形成された表面（受光面）に対向して有するので、光電変換素子100の開放電圧が大きくなる。従って、テクスチャ構造によるパッシベーション特性の低下を抑制して変換効率を向上できる。

[0122] また、光電変換素子100においては、p型非晶質半導体層5と電極9との間に透明導電膜7が配置され、n型非晶質半導体層6と電極10との間に透明導電膜8が配置されるため、p型非晶質半導体層5と電極9との界面、およびn型非晶質半導体層6と電極10との界面におけるキャリアの再結合を抑制できる。

[0123] 更に、n型単結晶シリコン基板1を透過した光を透明導電膜7と電極9との界面および透明導電膜8と電極10との界面で反射して短絡電流を増加できる。

[0124] なお、光電変換素子100は、透明導電膜8を備えていなくてもよい。透明導電膜8は、多数キャリア（電子）を収集するn型非晶質半導体層6と電極10との間に配置されるため、キャリアの再結合が問題にならないからである。従って、光電変換素子100においては、少なくとも、少数キャリア

(正孔)を収集するp型非晶質半導体層5と電極9との間に透明導電膜が配置されていればよい。

[0125] 更に、光電変換素子100は、i型非晶質半導体層3, 4を備えていなくてもよい。i型非晶質半導体層3, 4が無くても、n型単結晶シリコン基板1の裏面でpn接合(n型単結晶シリコン基板1/p型非晶質半導体層5)を形成することができるからである。

[0126] 上記においては、i型非晶質半導体層3, 4は、i型a-Siからなると説明したが、実施の形態1においては、これに限らず、i型非晶質半導体層3, 4は、i型a-SiC, i型a-SiN, i型a-SiO, i型a-SiON, i型a-SiGe, i型a-Geのいずれかからなってもよい。

[0127] また、i型非晶質半導体層3, 4は、 $1 \times 10^{16} \text{ cm}^{-3}$ 以下のPまたはBを含んでいてもよい。1つの反応室で光電変換素子100を作製する場合、反応室の壁にPおよびB等のドーパント不純物が付着しており、ドーパント不純物がi型非晶質半導体層3, 4の成膜時に混入するからである。そして、 $1 \times 10^{16} \text{ cm}^{-3}$ 以下の濃度であるドーパント不純物が混入しても、 $1 \times 10^{16} \text{ cm}^{-3}$ 以下の濃度のドーパント不純物を含むアモルファスシリコン膜等は、実質的にi型の導電型を有する。従って、i型非晶質半導体層3, 4は、実質的にi型の導電型を有していればよい。

[0128] n型非晶質半導体層3は、n型a-Siからなると説明したが、実施の形態1においては、これに限らず、n型非晶質半導体層3は、n型a-SiC, n型a-SiN, n型a-SiO, n型a-SiON, n型a-SiGe, n型a-Geのいずれかからなってもよい。

[0129] p型非晶質半導体層5は、p型a-Siからなると説明したが、実施の形態1においては、これに限らず、p型非晶質半導体層5は、p型a-SiC, p型a-SiN, p型a-SiO, p型a-SiON, p型a-SiGe, p型a-Geのいずれかからなってもよい。

[0130] この場合、i型a-SiCは、SiH₄ガス、H₂ガスおよびメタン(CH₄

）ガスを材料ガスとして、上述したプラズマCVD法によって形成される。

i 型 a-SiN は、SiH₄ ガス、H₂ ガスおよびアンモニア (NH₃) ガスを材料ガスとして、上述したプラズマCVD法によって形成される。i 型 a-SiO は、SiH₄ ガス、H₂ ガスおよびO₂ ガスを材料ガスとして、上述したプラズマCVD法によって形成される。i 型 a-SiON は、SiH₄ ガス、H₂ ガス、O₂ ガスおよびNH₃ ガスを材料ガスとして、上述したプラズマCVD法によって形成される。i 型 a-SiGe は、SiH₄ ガス、H₂ ガスおよびゲルマン (GeH₄) ガスを材料ガスとして、上述したプラズマCVD法によって形成される。i 型 a-Ge は、H₂ ガスおよびGeH₄ ガスを材料ガスとして、上述したプラズマCVD法によって形成される。

[0131] n 型 a-SiC は、SiH₄ ガス、H₂ ガス、CH₄ ガスおよびPH₃ ガスを材料ガスとして、上述したプラズマCVD法によって形成される。n 型 a-SiN は、SiH₄ ガス、H₂ ガス、NH₃ ガスおよびPH₃ ガスを材料ガスとして、上述したプラズマCVD法によって形成される。n 型 a-SiO は、SiH₄ ガス、H₂ ガス、O₂ ガスおよびPH₃ ガスを材料ガスとして、上述したプラズマCVD法によって形成される。n 型 a-SiON は、SiH₄ ガス、H₂ ガス、O₂ ガスを、NH₃ ガスおよびPH₃ ガスを材料ガスとして、上述したプラズマCVD法によって形成される。n 型 a-SiGe は、SiH₄ ガス、H₂ ガス、GeH₄ ガスおよびPH₃ ガスを材料ガスとして、上述したプラズマCVD法によって形成される。n 型 a-Ge は、H₂ ガス、GeH₄ ガスおよびPH₃ ガスを材料ガスとして、上述したプラズマCVD法によって形成される。

[0132] p 型 a-SiC は、SiH₄ ガス、H₂ ガス、CH₄ ガスおよびB₂H₆ ガスを材料ガスとして、上述したプラズマCVD法によって形成される。p 型 a-SiN は、SiH₄ ガス、H₂ ガス、NH₃ ガスおよびB₂H₆ ガスを材料ガスとして、上述したプラズマCVD法によって形成される。p 型 a-SiO は、SiH₄ ガス、H₂ ガス、O₂ ガスおよびB₂H₆ ガスを材料ガスとして、上述したプラズマCVD法によって形成される。p 型 a-SiON は、SiH₄ ガス

、 H_2 ガス、 O_2 ガスを、 NH_3 ガスおよび B_2H_6 ガスを材料ガスとして、上述したプラズマCVD法によって形成される。p型a-SiGeは、 SiH_4 ガス、 H_2 ガス、 GeH_4 ガスおよび B_2H_6 ガスを材料ガスとして、上述したプラズマCVD法によって形成される。p型a-Geは、 H_2 ガス、 GeH_4 ガスおよび B_2H_6 ガスを材料ガスとして、上述したプラズマCVD法によって形成される。

[0133] また、光電変換素子100は、n型単結晶シリコン基板1に代えて、p型単結晶シリコン基板、n型多結晶シリコン基板およびp型多結晶シリコン基板のいずれかを備えていてもよい。

[0134] この場合、p型単結晶シリコン基板、n型多結晶シリコン基板およびp型多結晶シリコン基板の各々は、上述した方法によってエッチングされ、高低差が $6\mu m$ 以下であるマクロ凹凸と、平均面粗さが $0.75nm$ 以下であるナノ凹凸とを含む表面（裏面）を有する。

[0135] また、p型単結晶シリコン基板の一方面（＝受光面）には、上述した方法によってテクスチャ構造が形成され、n型多結晶シリコン基板またはp型多結晶シリコン基板の一方面（受光面）には、ドライエッチングによってテクスチャ構造が形成される。

[0136] このように、光電変換素子100は、一般的には、シリコン基板を備えていればよい。

[0137] そして、光電変換素子100においては、pn接合は、テクスチャ構造が形成される受光面側ではなく、高低差が $6\mu m$ 以下であるマクロ凹凸と、平均面粗さが $0.75nm$ 以下であるナノ凹凸とを有する表面側に配置される。マクロ凹凸の高低差が 6μ 以下であり、ナノ凹凸の平均面粗さが $0.75nm$ 以下であれば、開放電圧が改善されるからである。

[0138] [実施の形態2]

図10は、実施の形態2による光電変換素子の構成を示す断面図である。

図10を参照して、実施の形態2による光電変換素子200は、n型単結晶シリコン基板1と、i型非晶質半導体層201、203と、n型非晶質半導

体層 202 と、p 型非晶質半導体層 204 と、透明導電膜 205 と、導電層 206 と、電極 207, 208 とを備える。

- [0139] i 型非晶質半導体層 201 は、真性な非晶質半導体からなる。i 型非晶質半導体層 201 は、n 型単結晶シリコン基板 1 の受光面（テクスチャ構造が形成された表面）に接して n 型単結晶シリコン基板 1 上に配置される。i 型非晶質半導体層 201 の厚みは、例えば、0.5 nm～25 nm である。そして、i 型非晶質半導体層 201 は、i 型 a-SiC, i 型 a-SiO, i 型 a-SiON, i 型 a-SiN, i 型 a-Si, i 型 a-SiGe, i 型 a-Ge のいずれかからなる。
- [0140] n 型非晶質半導体層 202 は、n 型の不純物がドーピングされた非晶質半導体からなる。n 型の不純物は、例えば、P である。n 型非晶質半導体層 202 は、i 型非晶質半導体層 201 に接して i 型非晶質半導体層 201 上に配置される。n 型非晶質半導体層 202 の厚みは、例えば、約 2 nm～約 50 nm である。n 型非晶質半導体層 202 における P 濃度は、例えば、 $1 \times 10^{19} \text{ cm}^{-3} \sim 1 \times 10^{20} \text{ cm}^{-3}$ である。そして、n 型非晶質半導体層 202 は、n 型 a-SiC, n 型 a-SiO, n 型 a-SiON, n 型 a-SiN, n 型 a-Si, n 型 a-SiGe, n 型 a-Ge のいずれかからなる。
- [0141] i 型非晶質半導体層 203 は、n 型単結晶シリコン基板 1 の受光面と反対側の表面に接して n 型単結晶シリコン基板 1 上に配置される。i 型非晶質半導体層 203 の厚みは、i 型非晶質半導体層 201 の厚みと同じである。そして、i 型非晶質半導体層 203 は、i 型 a-SiC, i 型 a-SiO, i 型 a-SiON, i 型 a-SiN, i 型 a-Si, i 型 a-SiGe, i 型 a-Ge のいずれかからなる。
- [0142] p 型非晶質半導体層 204 は、p 型の不純物がドーピングされた非晶質半導体からなる。p 型の不純物は、例えば、B である。p 型非晶質半導体層 204 は、i 型非晶質半導体層 203 に接して i 型非晶質半導体層 203 上に配置される。p 型非晶質半導体層 204 の厚みは、例えば、約 2 nm～約 50 nm である。そして、p 型非晶質半導体層 204 は、p 型 a-SiC, p 型 a

-SiO, p型a-SiON, p型a-SiN, p型a-Si, p型a-SiGe, p型a-Geのいずれかからなる。そして、p型非晶質半導体層204におけるB濃度は、例えば、 $1 \times 10^{19} \text{ cm}^{-3} \sim 1 \times 10^{20} \text{ cm}^{-3}$ である。

[0143] 透明導電膜205は、n型非晶質半導体層202に接してn型非晶質半導体層202上に配置される。透明導電膜205は、例えば、ITO、SnO₂およびZnO等からなる。

[0144] 導電層206は、p型非晶質半導体層204に接してp型非晶質半導体層204上に配置される。導電層206は、透明導電膜、Ag, Cu, Sn, Pt, Au, Ti, Ta, Ni, Co, Al等の金属、およびそれらの金属のうちの一種以上を含む合金等の導電性材料からなる。導電層206の厚みは、例えば、約70nm～約100nmである。

[0145] 電極207は、透明導電膜205の一部に接して透明導電膜205上に配置される。電極207は、例えば、Agからなる。

[0146] 電極208は、導電層206に接して導電層206上に配置される。電極208は、例えば、Agからなる。

[0147] 図11および図12は、それぞれ、図10に示す光電変換素子200の製造方法を示す第1および第2の工程図である。

[0148] 光電変換素子200の製造が開始されると、図7の工程(a), (b)と同じ工程を実行してn型単結晶シリコン基板1を作製する(図11の工程(a), (b)参照)。

[0149] その後、n型単結晶シリコン基板1をフッ酸中に浸漬してn型単結晶シリコン基板1の表面に形成された自然酸化膜を除去するとともに、n型単結晶シリコン基板1の表面を水素で終端する。

[0150] n型単結晶シリコン基板1の洗浄が終了すると、n型単結晶シリコン基板1をプラズマ装置の反応室に入れる。

[0151] そして、上述したi型非晶質半導体層3, 4の形成条件と同じ形成条件を用いてi型非晶質半導体層201をn型単結晶シリコン基板1の受光面(テ

クスチャ構造が形成された表面)上に形成する(図11の工程(c)参照)

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[0152] その後、上述したn型非晶質半導体層306の形成条件と同じ形成条件を用いてn型非晶質半導体層202をi型非晶質半導体層201上に形成する(図11の工程(d)参照)。

[0153] 次に、i型非晶質半導体層3、4の形成条件と同じ形成条件を用いてi型非晶質半導体層203をn型単結晶シリコン基板1の受光面と反対側の表面上に形成する(図11の工程(e)参照)。

[0154] そして、上述したp型非晶質半導体層5の形成条件と同じ形成条件を用いてp型非晶質半導体層204をi型非晶質半導体層203上に形成する(図12の工程(f)参照)。

[0155] その後、n型単結晶シリコン基板1の温度が180℃になるようにn型単結晶シリコン基板1を加熱し、200～800sccmのアルゴン(Ar)ガスと、0～30sccmの酸素(O₂)ガスとの混合ガスを流してチャンバ内の圧力を0.4～1.3Paに保ちながら0.2～2kWの電力を投入して放電させる。これによって、透明導電膜205(=ITO)がn型非晶質半導体層202上に形成される(図12の工程(g)参照)。

[0156] 次に、導電層206(ITO)を透明導電膜205(=ITO)と同じ形成条件によってp型非晶質半導体層204上に形成する(図12の工程(h)参照)。

[0157] なお、透明導電膜205および導電層206は、スパッタリング法の他に、CVD法および蒸着法等の薄膜形成方法、またはめっき法、またはそれらの組合せによって形成されてもよい。

[0158] そして、エポキシ樹脂にAgの微粉末を練り込んだAgペーストをスクリーン印刷によって、高さを約10～30μm、幅を100～500μmに形成した後、200℃で80分、焼成硬化することによって櫛形の電極207、208を形成する(図12の工程(i)参照)。これによって、光電変換素子200が完成する。

[0159] 光電変換素子200は、光電変換素子100と同じようにn型単結晶シリコン基板1を備え、受光面と反対側にヘテロ接合によるpn接合（n型単結晶シリコン基板1／p型非晶質半導体層204）が存在する。従って、テクスチャ構造によるパッシベーション特性の低下を抑制して変換効率を向上できる。

[0160] また、光電変換素子200においては、p型非晶質半導体層204と電極208との間に導電層206が配置されているため、p型非晶質半導体層204と電極208との界面におけるキャリアの再結合を抑制できる。また、導電層206が透明導電膜からなり、電極208がAgからなる場合、n型単結晶シリコン基板1を透過した光は、導電層206（透明導電膜）／電極208（Ag）界面で反射され、n型単結晶シリコン基板1で吸収される。従って、光電変換素子200の短絡電流を増加できる。

[0161] なお、光電変換素子200において、i型非晶質半導体層203／p型非晶質半導体層204を受光面側に形成し、i型非晶質半導体層201／n型非晶質半導体層202を受光面と反対側に形成してもよい。このようにしても、マクロ凹凸の高低差が6μm以下になり、かつ、ナノ凹凸の平均面粗さが0.75nm以下になると、開放電圧が向上した。従って、テクスチャ構造によるパッシベーション特性の低下を抑制して変換効率を向上できる。

[0162] 実施の形態2におけるその他の説明は、実施の形態1についての説明と同じである。

[0163] [実施の形態3]

実施の形態1においては、NaOHエッチング液：10%、H₂O希釈、80℃で2分程度の条件を用いてシリコン基板をエッチングしたが、実施の形態3においては、NaOHエッチング液：10%、H₂O希釈、100℃で3分程度の条件を用いてシリコン基板をエッチングした。

[0164] 図13は、n型単結晶シリコン基板の（100）面の顕微鏡写真を示す図である。上記条件でシリコン基板をエッチングした場合、スプーンカット状のマクロ凹凸が形成される（図13の（a）参照）。

[0165] このスプーンカット状のマクロ凹凸が発生する場合には、若干、四角形のマクロ凹凸に比べ、高低差が小さくなるので（図13の（b）参照）、好ましい。この場合、高低差とは、スプーンカット部のボトムから隣り合うスプーンカット部との境界の一番高い領域までの高低差を言う。

[0166] 図13に示すマクロ凹凸を有するn型単結晶シリコン基板を用いた光電変換素子においても、実施の形態1と同じように、マクロ凹凸の高低差が $6\mu\text{m}$ 以下であり、かつ、ナノ凹凸の平均面粗さが 0.75nm 以下である場合、開放電圧が向上する。

[0167] 従って、テクスチャ構造によるパッシベーション特性の低下を抑制して変換効率を向上できる。

[0168] なお、実施の形態3における光電変換素子の構成は、上述した光電変換素子100、200であってもよいし、後述する実施の形態4、5による光電変換素子であってもよい。

[0169] [実施の形態4]

図14は、実施の形態4による光電変換素子の構成を示す断面図である。

図14を参照して、実施の形態4による光電変換素子400は、n型単結晶シリコン基板401と、反射防止膜402と、第1パッシベーション膜403と、第2パッシベーション膜404と、電極405、406とを備える。

[0170] n型単結晶シリコン基板401は、p型拡散層4011とn型拡散層4012とを受光面と反対側の表面に接して含む。この場合、p型拡散層4011およびn型拡散層4012は、n型単結晶シリコン基板401の面内方向に交互に配置される。p型拡散層4011は、例えば、 $1\times 10^{18}\text{cm}^{-3}\sim 1\times 10^{19}\text{cm}^{-3}$ のB濃度を有する。また、p型拡散層4011は、例えば、 $100\sim 200\text{nm}$ の厚みを有する。n型拡散層4012は、例えば、 $1\times 10^{18}\text{cm}^{-3}\sim 1\times 10^{19}\text{cm}^{-3}$ のP濃度を有する。また、n型拡散層4012は、例えば、 $100\sim 200\text{nm}$ の厚みを有する。

[0171] n型単結晶シリコン基板401についてのその他の説明は、n型単結晶シリコン基板1についての説明と同じである。

- [0172] 反射防止膜402は、n型単結晶シリコン基板401の受光面（テクスチャ構造が形成された表面）に接してn型単結晶シリコン基板401上に配置される。反射防止膜402は、例えば、窒化シリコンからなり、例えば、80～300nmの厚みを有する。
- [0173] 第1パッシベーション膜403は、n型単結晶シリコン基板401のp型拡散層4011に接して配置される。第1パッシベーション膜403は、例えば、SiO₂からなり、例えば、100～200nmの厚みを有する。
- [0174] 第2パッシベーション膜404は、n型単結晶シリコン基板401のp型拡散層4011以外の部分に接して配置される。第2パッシベーション膜404は、例えば、窒化シリコンからなり、例えば、100～200nmの厚みを有する。
- [0175] 電極405は、第1パッシベーション膜403を貫通してp型拡散層4011に接して配置される。そして、電極405は、例えば、Agからなる。
- [0176] 電極406は、第2パッシベーション膜404を貫通してn型拡散層4012に接して配置される。そして、電極406は、例えば、Agからなる。
- [0177] 図15から図17は、それぞれ、図14に示す光電変換素子400の製造方法を示す第1から第3の工程図である。
- [0178] 光電変換素子400の製造が開始されると、図7の工程（a）、（b）と同じ工程を実行してn型単結晶シリコン基板1を作製する（図15の工程（a）、（b）参照）。
- [0179] そして、n型単結晶シリコン基板401の受光面および裏面の全面に酸化シリコンからなる第1拡散マスク410を形成する。次に、n型単結晶シリコン基板401の裏面に形成された第1拡散マスク410に第1エッチングペーストをスクリーン印刷法によって所望のパターンに印刷する。続いて、第1エッチングペーストが印刷されたn型単結晶シリコン基板401を加熱処理する。これにより、n型単結晶シリコン基板401の裏面に形成された第1拡散マスク410のうち、第1エッチングペーストが印刷された部分のみがエッチングによって除去される。その後、n型単結晶シリコン基板401

を水中に浸漬し、超音波を印加して超音波洗浄を行う。これにより、第1エッチングペーストが除去され、n型単結晶シリコン基板401の裏面に窓412が形成される（図15の工程（c）参照）。

[0180] そうすると、p型不純物であるBを窓412を介してn型単結晶シリコン基板401へ気相拡散させる。そして、第1拡散マスク410と、Bが拡散してn型単結晶シリコン基板401に形成されたBSG（ボロンシリケートガラス）とをフッ化水素水溶液等を用いて除去する。これによって、p型拡散層4011が形成される（図15の工程（d）参照）。

[0181] その後、n型単結晶シリコン基板401の受光面および裏面の全面に、酸化シリコンからなる第2拡散マスク411を形成する。次に、n型単結晶シリコン基板401の裏面に形成された第2拡散マスク411上に第2エッチングペーストをスクリーン印刷法によって所望のパターンに印刷する。続いて、第2エッチングペーストが印刷されたn型単結晶シリコン基板401を加熱処理する。これにより、n型単結晶シリコン基板401の裏面に形成された第2拡散マスク411のうち、第2エッチングペーストが印刷された部分のみがエッチングによって除去される。その後、n型単結晶シリコン基板401を水中に浸漬し、超音波を印加して超音波洗浄を行う。これにより、第2エッチングペーストが除去され、n型単結晶シリコン基板401の裏面に窓414が形成される（図15の工程（e）参照）。

[0182] そうすると、n型不純物であるPを窓414を介してn型単結晶シリコン基板401へ気相拡散させる。そして、第2拡散マスク411と、Pが拡散してn型単結晶シリコン基板401に形成されたPSG（リンシリケートガラス）とをフッ化水素水溶液等を用いて除去する。これによって、n型拡散層4012が形成される（図16の工程（f）参照）。

[0183] 次に、n型単結晶シリコン基板401に対して熱酸化を行う。これにより、n型単結晶シリコン基板401の受光面に酸化シリコン膜413が形成され、n型単結晶シリコン基板401の裏面に酸化シリコンからなるパッシベーション膜415が形成される（図16の工程（g）参照）。

- [0184] その後、パッシベーション膜415のうち、p型拡散層4011上に形成された部分以外の部分にエッチングペーストをスクリーン印刷法によって印刷し、n型単結晶シリコン基板401を加熱処理する。これにより、パッシベーション膜415のうち、p型拡散層4011上に形成された部分以外の部分が除去され、p型拡散層4011上に第1パッシベーション膜403が形成される（図16の工程（h）参照）。
- [0185] 次に、プラズマCVD法によって窒化シリコンからなる第2パッシベーション膜404をn型単結晶シリコン基板401の裏面に形成する（図16の工程（i）参照）。
- [0186] 引き続き、n型単結晶シリコン基板401の受光面に形成された酸化シリコン膜413をフッ化水素水溶液等を用いて除去し、窒化シリコンからなる反射防止膜402をn型単結晶シリコン基板401の受光面に形成する（図17の工程（j）参照）。
- [0187] そして、第1パッシベーション膜403の一部と、第2パッシベーション膜404のうち、n型拡散層4012上に位置する部分とにエッチングペーストをスクリーン印刷法によって印刷し、n型単結晶シリコン基板401を加熱処理する。これにより、第1パッシベーション膜403の一部と、第2パッシベーション膜404の一部とが除去され、コンタクトホール416、417が形成される（図17の工程（k）参照）。
- [0188] その後、コンタクトホール416、417にAgペーストを印刷し、その印刷したAgペーストを焼成する。これにより、電極405、406が形成され、光電変換素子400が完成する（図17の工程（l）参照）。
- [0189] 光電変換素子400は、光電変換素子100のn型単結晶シリコン基板1と同じように、テクスチャ構造が形成された受光面に対向して、マクロ凹凸の高低差が0.6 μm 以下であり、ナノ凹凸の平均面粗さが0.75 nm以下である表面（裏面）を有するn型単結晶シリコン基板401を備えるので、開放電圧 V_{oc} が向上する。従って、テクスチャ構造によるパッシベーション特性の低下を抑制して変換効率を向上できる。

[0190] 実施の形態4におけるその他の説明は、実施の形態1における説明と同じである。

[0191] [実施の形態5]

図18は、実施の形態5による光電変換素子の構成を示す断面図である。

図18を参照して、実施の形態5による光電変換素子500は、n型単結晶シリコン基板501と、反射防止膜502と、絶縁層504と、電極503、505とを備える。

[0192] n型単結晶シリコン基板501は、n型拡散層5011と、p型拡散層5012とを含む。n型拡散層5011は、n型単結晶シリコン基板501の受光面に接してn型単結晶シリコン基板501中に配置される。n型拡散層5011は、例えば、 $1 \times 10^{18} \text{ cm}^{-3} \sim 1 \times 10^{19} \text{ cm}^{-3}$ のP濃度を有する。また、n型拡散層5011は、例えば、100～200nmの厚みを有する。

[0193] p型拡散層5012は、n型単結晶シリコン基板501の受光面と反対側の表面に接してn型単結晶シリコン基板501中に配置される。p型拡散層5012は、例えば、 $1 \times 10^{18} \text{ cm}^{-3} \sim 1 \times 10^{19} \text{ cm}^{-3}$ のB濃度を有する。また、p型拡散層5012は、例えば、100～200nmの厚みを有する。

[0194] n型単結晶シリコン基板501についてのその他の説明は、n型単結晶シリコン基板1についての説明と同じである。

[0195] 反射防止膜502は、n型単結晶シリコン基板501の受光面に接してn型単結晶シリコン基板501上に配置される。反射防止膜502は、酸化シリコン、窒化シリコンおよび酸窒化シリコンのいずれかからなる。反射防止膜502は、入射光の反射を防止する機能を考慮すると、80～300nmの厚みを有する。

[0196] 電極503は、反射防止膜502を貫通してn型単結晶シリコン基板501のn型拡散層5011に接して配置される。電極503は、例えば、Agからなる。

- [0197] 絶縁層 504 は、n 型単結晶シリコン基板 501 の裏面（＝受光面と反対側の表面）に接して n 型単結晶シリコン基板 501 上に配置される。絶縁層 504 は、反射防止膜 502 と同じ材料からなり、100～200 nm の厚みを有する。
- [0198] 電極 505 は、絶縁層 504 を貫通して n 型単結晶シリコン基板 501 の p 型拡散層 5012 に接して配置される。電極 505 は、例えば、Ag になる。
- [0199] このように、光電変換素子 500 は、テクスチャ構造が形成される受光面と反対側に pn 接合（n 型単結晶シリコン基板 501 のバルク領域／p 型拡散層 5012）を備える。
- [0200] 図 19 から図 21 は、それぞれ、図 18 に示す光電変換素子 500 の製造方法を示す第 1 から第 3 の工程図である。
- [0201] 光電変換素子 500 の製造が開始されると、図 7 の工程（a），（b）と同じ工程を実行して n 型単結晶シリコン基板 501 を作成する（図 19 の工程（a），（b）参照）。
- [0202] その後、P 原子を n 型単結晶シリコン基板 501 の受光面から n 型単結晶シリコン基板 501 中へ気相拡散し、n 型拡散層 5011 を形成する（図 19 の工程（c）参照）。
- [0203] そして、B 原子を n 型単結晶シリコン基板 501 の裏面から n 型単結晶シリコン基板 501 中へ気相拡散し、p 型拡散層 5012 を形成する（図 19 の工程（d）参照）。
- [0204] 引き続いて、反射防止膜 502 をスパッタリング法によって n 型単結晶シリコン基板 501 の受光面上に形成する（図 19 の工程（e）参照）。
- [0205] そして、絶縁層 504 をスパッタリング法によって n 型単結晶シリコン基板 501 の裏面上に形成する（図 20 の工程（f）参照）。
- [0206] その後、レジストを反射防止膜 502 の全面に塗布し、その塗布したレジストをフォトリソグラフィによってパターンニングしてレジストパターン 510 を形成する（図 20 の工程（g）参照）。

- [0207] そうすると、レジストパターン510をマスクとして反射防止膜502の一部をエッチングする（図20の工程（h）参照）。
- [0208] そして、Agペーストをスクリーン印刷によって印刷し、その印刷したAgペーストを焼成して電極503を形成する（図20の工程（i）参照）。
- [0209] 引き続いて、レジストを絶縁層504の全面に塗布し、その塗布したレジストをフォトリソグラフィによってパターンニングしてレジストパターン520を形成する（図21の工程（j）参照）。
- [0210] そして、レジストパターン520をマスクとして絶縁層504の一部をエッチングする（図21の工程（k）参照）。
- [0211] その後、絶縁層504を覆うようにAgを電子ビーム蒸着して電極505を形成する（図21の工程（l）参照）。これによって、光電変換素子500が完成する。
- [0212] 光電変換素子500は、光電変換素子100のn型単結晶シリコン基板1と同じように、テクスチャ構造が形成された受光面に対して、マクロ凹凸の高低差が0.6 μm 以下であり、かつ、ナノ凹凸の平均面粗さが0.75 nm以下である表面（裏面）を有するn型単結晶シリコン基板501を備えるので、開放電圧 V_{oc} が向上する。従って、テクスチャ構造によるパッシベーション特性の低下を抑制して変換効率を向上できる。
- [0213] なお、光電変換素子500のn型単結晶シリコン基板501は、受光面に接してp型拡散層を含み、受光面と反対側の裏面に接してn型拡散層を含んでいてもよい。
- [0214] 実施の形態5におけるその他の説明は、実施の形態1における説明と同じである。
- [0215] [実施の形態6]
- 図22は、この実施の形態による光電変換素子を備える光電変換モジュールの構成を示す概略図である。図22を参照して、光電変換モジュール1000は、複数の光電変換素子1001と、カバー1002と、出力端子1003, 1004とを備える。

- [0216] 複数の光電変換素子 1001 は、アレイ状に配置され、直列に接続される。なお、複数の光電変換素子 1001 は、直列に接続される代わりに、並列に接続されてもよく、直列と並列を組み合わせで接続されてもよい。
- [0217] そして、複数の光電変換素子 1001 の各々は、光電変換素子 100, 200, 400, 500 のいずれかからなる。
- [0218] カバー 1002 は、耐候性のカバーからなり、複数の光電変換素子 1001 を覆う。
- [0219] 出力端子 1003 は、直列に接続された複数の光電変換素子 1001 の一端に配置される光電変換素子 1001 に接続される。
- [0220] 出力端子 1004 は、直列に接続された複数の光電変換素子 1001 の他端に配置される光電変換素子 1001 に接続される。
- [0221] 上述したように、光電変換素子 100, 200, 400, 500 は、高い変換効率を有する。
- [0222] 従って、光電変換モジュール 1000 の変換効率を向上できる。
- [0223] なお、実施の形態 6 による光電変換モジュールは、図 22 に示す構成に限らず、光電変換素子 100, 200, 300, 400, 500 のいずれかを用いる限り、どのような構成であってもよい。
- [0224] [実施の形態 7]
- 図 23 は、この実施の形態による光電変換素子を備える太陽光発電システムの構成を示す概略図である。
- [0225] 図 23 を参照して、太陽光発電システム 1100 は、光電変換モジュールアレイ 1101 と、接続箱 1102 と、パワーコンディショナー 1103 と、分電盤 1104 と、電力メーター 1105 とを備える。
- [0226] 接続箱 1102 は、光電変換モジュールアレイ 1101 に接続される。パワーコンディショナー 1103 は、接続箱 1102 に接続される。分電盤 1104 は、パワーコンディショナー 1103 および電気機器 1110 に接続される。電力メーター 1105 は、分電盤 1104 および系統連系に接続される。

- [0227] 光電変換モジュールアレイ 1101 は、太陽光を電気に変換して直流電力を発電し、その発電した直流電力を接続箱 1102 に供給する。
- [0228] 接続箱 1102 は、光電変換モジュールアレイ 1101 が発電した直流電力を受け、その受けた直流電力をパワーコンディショナー 1103 へ供給する。
- [0229] パワーコンディショナー 1103 は、接続箱 1102 から受けた直流電力を交流電力に変換し、その変換した交流電力を分電盤 1104 に供給する。また、パワーコンディショナー 1103 は、接続箱 1102 から受けた直流電力の一部を交流電力に変換せずに、直流電力のまま分電盤 1104 に供給してもよい。
- [0230] 分電盤 1104 は、パワーコンディショナー 1103 から受けた交流電力および／または電力メーター 1105 を介して受けた商用電力を電気機器 1110 へ供給する。また、分電盤 1104 は、パワーコンディショナー 1103 から受けた交流電力が電気機器 1110 の消費電力よりも多いとき、余った交流電力を電力メーター 1105 を介して系統連系へ供給する。
- [0231] 電力メーター 1105 は、系統連系から分電盤 1104 へ向かう方向の電力を計測するとともに、分電盤 1104 から系統連系へ向かう方向の電力を計測する。
- [0232] 図 24 は、図 23 に示す光電変換モジュールアレイ 1101 の構成を示す概略図である。
- [0233] 図 24 を参照して、光電変換モジュールアレイ 1101 は、複数の光電変換モジュール 1120 と、出力端子 1121, 1122 とを含む。
- [0234] 複数の光電変換モジュール 1120 は、アレイ状に配列され、直列に接続される。なお、複数の光電変換モジュール 1120 は、直列に接続される代わりに、並列に接続されてもよく、直列と並列を組み合わせで接続されてもよい。そして、複数の光電変換モジュール 1120 の各々は、図 22 に示す光電変換モジュール 1000 からなる。
- [0235] 出力端子 1121 は、直列に接続された複数の光電変換モジュール 112

0の一方端に位置する光電変換モジュール1120に接続される。

[0236] 出力端子1122は、直列に接続された複数の光電変換モジュール1120の他方端に位置する光電変換モジュール1120に接続される。

[0237] 太陽光発電システム1100における動作を説明する。光電変換モジュールアレイ1101は、太陽光を電気に変換して直流電力を発電し、その発電した直流電力を接続箱1102を介してパワーコンディショナー1103へ供給する。

[0238] パワーコンディショナー1103は、光電変換モジュールアレイ1101から受けた直流電力を交流電力に変換し、その変換した交流電力を分電盤1104へ供給する。

[0239] 分電盤1104は、パワーコンディショナー1103から受けた交流電力が電気機器1110の消費電力以上であるとき、パワーコンディショナー1103から受けた交流電力を電気機器1110に供給する。そして、分電盤1104は、余った交流電力を電力メーター1105を介して系統連系へ供給する。

[0240] また、分電盤1104は、パワーコンディショナー1103から受けた交流電力が電気機器1110の消費電力よりも少ないとき、系統連系から受けた交流電力およびパワーコンディショナー1103から受けた交流電力を電気機器1110へ供給する。

[0241] 太陽光発電システム1100は、上述したように、高い変換効率を有する光電変換素子100、200、400、500のいずれかを備えている。

[0242] 従って、太陽光発電システム1100の変換効率を向上できる。

[0243] なお、実施の形態7による太陽光発電システムは、図23、24に示す構成に限らず、光電変換素子100、200、400、500のいずれかを用いる限り、どのような構成であってもよい。

[0244] [実施の形態8]

図25は、この実施の形態による光電変換素子を備える太陽光発電システムの構成を示す概略図である。

- [0245] 図25を参照して、太陽光発電システム1200は、サブシステム1201～120n（nは2以上の整数）と、パワーコンディショナー1211～121nと、変圧器1221とを備える。太陽光発電システム1200は、図23に示す太陽光発電システム1100よりも規模が大きい太陽光発電システムである。
- [0246] パワーコンディショナー1211～121nは、それぞれ、サブシステム1201～120nに接続される。
- [0247] 変圧器1221は、パワーコンディショナー1211～121nおよび系統連系に接続される。
- [0248] サブシステム1201～120nの各々は、モジュールシステム1231～123j（jは2以上の整数）からなる。
- [0249] モジュールシステム1231～123jの各々は、光電変換モジュールアレイ1301～130i（iは2以上の整数）と、接続箱1311～131iと、集電箱1321とを含む。
- [0250] 光電変換モジュールアレイ1301～130iの各々は、図23に示す光電変換モジュールアレイ1101と同じ構成からなる。
- [0251] 接続箱1311～131iは、それぞれ、光電変換モジュールアレイ1301～130iに接続される。
- [0252] 集電箱1321は、接続箱1311～131iに接続される。また、サブシステム1201のj個の集電箱1321は、パワーコンディショナー1211に接続される。サブシステム1202のj個の集電箱1321は、パワーコンディショナー1212に接続される。以下、同様にして、サブシステム120nのj個の集電箱1321は、パワーコンディショナー121nに接続される。
- [0253] モジュールシステム1231のi個の光電変換モジュールアレイ1301～130iは、太陽光を電気に変換して直流電力を発電し、その発電した直流電力をそれぞれ接続箱1311～131iを介して集電箱1321へ供給する。モジュールシステム1232のi個の光電変換モジュールアレイ13

01～130iは、太陽光を電気に変換して直流電力を発電し、その発電した直流電力をそれぞれ接続箱1311～131iを介して集電箱1321へ供給する。以下、同様にして、モジュールシステム123jのi個の光電変換モジュールアレイ1301～130iは、太陽光を電気に変換して直流電力を発電し、その発電した直流電力をそれぞれ接続箱1311～131iを介して集電箱1321へ供給する。

[0254] そして、サブシステム1201のj個の集電箱1321は、直流電力をパワーコンディショナー1211へ供給する。

[0255] サブシステム1202のj個の集電箱1321は、同様にして直流電力をパワーコンディショナー1212へ供給する。

[0256] 以下、同様にして、サブシステム120nのj個の集電箱1321は、直流電力をパワーコンディショナー121nへ供給する。

[0257] パワーコンディショナー1211～121nは、それぞれ、サブシステム1201～120nから受けた直流電力を交流電力に変換し、その変換した交流電力を変圧器1221へ供給する。

[0258] 変圧器1221は、パワーコンディショナー1211～121nから交流電力を受け、その受けた交流電力の電圧レベルを変換して系統連系へ供給する。

[0259] 太陽光発電システム1200は、上述したように、高い変換効率を有する光電変換素子100, 200, 300, 400, 500のいずれかを備えている。

[0260] 従って、太陽光発電システム1200の変換効率を向上できる。

[0261] なお、実施の形態8による太陽光発電システムは、図25に示す構成に限らず、光電変換素子100, 200, 400, 500のいずれかを用いる限り、どのような構成であってもよい。

[0262] 上述した実施の形態1においては、受光面と反対側にヘテロ接合によるpn接合を設けた光電変換素子100において、マクロ凹凸の高低差が0.6μm以下であり、かつ、ナノ凹凸の平均面粗さが0.75nm以下である表

面（裏面）を有するn型単結晶シリコン基板1を用いることにより、開放電圧を高くして、テクスチャ構造によるパッシベーション特性の低下を抑制して変換効率を高くできることについて説明した。

[0263] また、実施の形態2においては、受光面側または受光面と反対側にヘテロ接合によるpn接合を設けた光電変換素子200において、マクロ凹凸の高低差が $0.6\mu\text{m}$ 以下であり、かつ、ナノ凹凸の平均面粗さが 0.75nm 以下である表面（裏面）を有するn型単結晶シリコン基板1を用いることにより、開放電圧を高くして、テクスチャ構造によるパッシベーション特性の低下を抑制して変換効率を高くできることについて説明した。

[0264] 更に、実施の形態4においては、受光面と反対側にホモ接合によるpn接合を設けた光電変換素子400において、マクロ凹凸の高低差が $0.6\mu\text{m}$ 以下であり、かつ、ナノ凹凸の平均面粗さが 0.75nm 以下である表面（裏面）を有するn型単結晶シリコン基板401を用いることにより、開放電圧を高くして、テクスチャ構造によるパッシベーション特性の低下を抑制して変換効率を高くできることについて説明した。

[0265] 更に、実施の形態5においては、受光面側にホモ接合によるpn接合を設けた光電変換素子500において、マクロ凹凸の高低差が $0.6\mu\text{m}$ 以下であり、かつ、ナノ凹凸の平均面粗さが 0.75nm 以下である表面（裏面）を有するn型単結晶シリコン基板501を用いることにより、開放電圧を高くして、テクスチャ構造によるパッシベーション特性の低下を抑制して変換効率を高くできることについて説明した。

[0266] 従って、この発明の実施の形態による光電変換素子は、pn接合は、ヘテロ接合およびホモ接合のいずれからなってもよく、pn接合の配置位置は、シリコン基板の受光面側であってもよく、受光面と反対側であってもよい。その結果、この発明の実施の形態による光電変換素子は、シリコン基板を備える光電変換素子であって、シリコン基板は、テクスチャ構造が形成された第1の表面と、第1の表面に対向するとともに、テクスチャ構造が形成されておらず、第1の凹凸および第2の凹凸を含む第2の表面とを有し、第

1の凹凸の高低差は、 $6\mu\text{m}$ 以下であり、第2の凹凸の平均面粗さは、 0.75nm よりも小さければよい。

[0267] 第1の凹凸の高低差が $6\mu\text{m}$ 以下であり、第2の凹凸の平均面粗さが 0.75nm よりも小さければ、開放電圧が向上し、テクスチャ構造によるパッシベーション特性の低下を抑制して変換効率を向上できるからである。

[0268] ヘテロ接合によるpn接合を受光面と反対側に設けた光電変換素子100においては、シリコン基板との間でヘテロ接合によるpn接合を構成することが重要である。従って、の発明の実施の形態による光電変換素子は、好ましくは、高低差が $0.6\mu\text{m}$ 以下である第1の凹凸と、平均面粗さが 0.75nm 以下である第2の凹凸とを含む第2の表面を有するシリコン基板に加えて、第2の表面に接して配置され、実質的にi型の導電型を有する第1の非晶質半導体層と、第1の非晶質半導体層に接して配置され、シリコン基板の導電型と反対の導電型を有する第2の非晶質半導体層とを更に備えていればよい。

[0269] 今回開示された実施の形態はすべての点で例示であって制限的なものではないと考えられるべきである。本発明の範囲は、上記した実施の形態の説明ではなくて特許請求の範囲によって示され、特許請求の範囲と均等の意味および範囲内でのすべての変更が含まれることが意図される。

産業上の利用可能性

[0270] この発明は、光電変換素子に適用される。

請求の範囲

- [請求項1] シリコン基板を備える光電変換素子であって、
前記シリコン基板は、
テクスチャ構造が形成された第1の表面と、
前記第1の表面に対向するとともに、前記テクスチャ構造が形成されておらず、第1の凹凸および第2の凹凸を含む第2の表面とを有し、
前記第1の凹凸の高低差は、 $6\ \mu\text{m}$ 以下であり、
前記第2の凹凸の平均面粗さは、 $0.75\ \text{nm}$ よりも小さい、光電変換素子。
- [請求項2] 前記第2の表面に接して配置され、実質的にi型の導電型を有する第1の非晶質半導体層と、
前記第1の非晶質半導体層に接して配置され、前記シリコン基板の導電型と反対の導電型を有する第2の非晶質半導体層とを更に備える、請求項1に記載の光電変換素子。
- [請求項3] 前記第1の表面に接して配置され、実質的にi型の導電型を有する第3の非晶質半導体層と、
前記第3の非晶質半導体層に接して配置され、前記シリコン基板の導電型と同じ導電型を有する第4の非晶質半導体層とを更に備える、請求項1または請求項2に記載の光電変換素子。
- [請求項4] 前記第1の表面に接して配置された第1の非晶質半導体層と、
前記第2の表面に接して配置され、実質的にi型の導電型を有する第2の非晶質半導体層と、
前記第2の表面に接して配置されるとともに前記シリコン基板の面内方向において前記第2の非晶質半導体層に隣接して配置され、実質的にi型の導電型を有する第3の非晶質半導体層と、
前記第2の非晶質半導体層に接して配置され、前記シリコン基板の導電型と反対の導電型を有する第4の非晶質半導体層と、

前記第3の非晶質半導体層に接して配置され、前記シリコン基板の導電型と同じ導電型を有する第5の非晶質半導体層とを更に備える、請求項1に記載の光電変換素子。

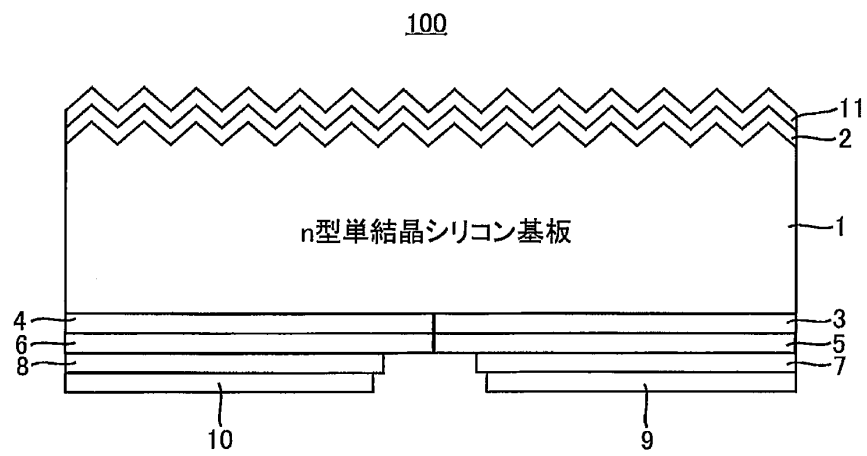
[請求項5]

前記第1の非晶質半導体層は、

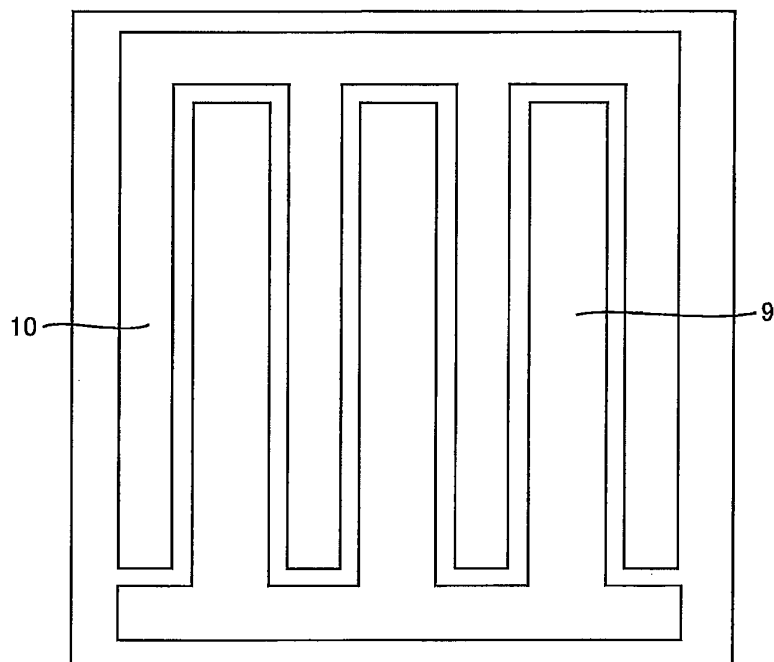
前記シリコン基板の受光面に接して配置され、実質的にi型の導電型を有する第6の非晶質半導体層と、

前記第6の非晶質半導体層に接して配置され、前記シリコン基板の導電型と同じ導電型を有する第7の非晶質半導体層とを含む、請求項4に記載の光電変換素子。

【図1】

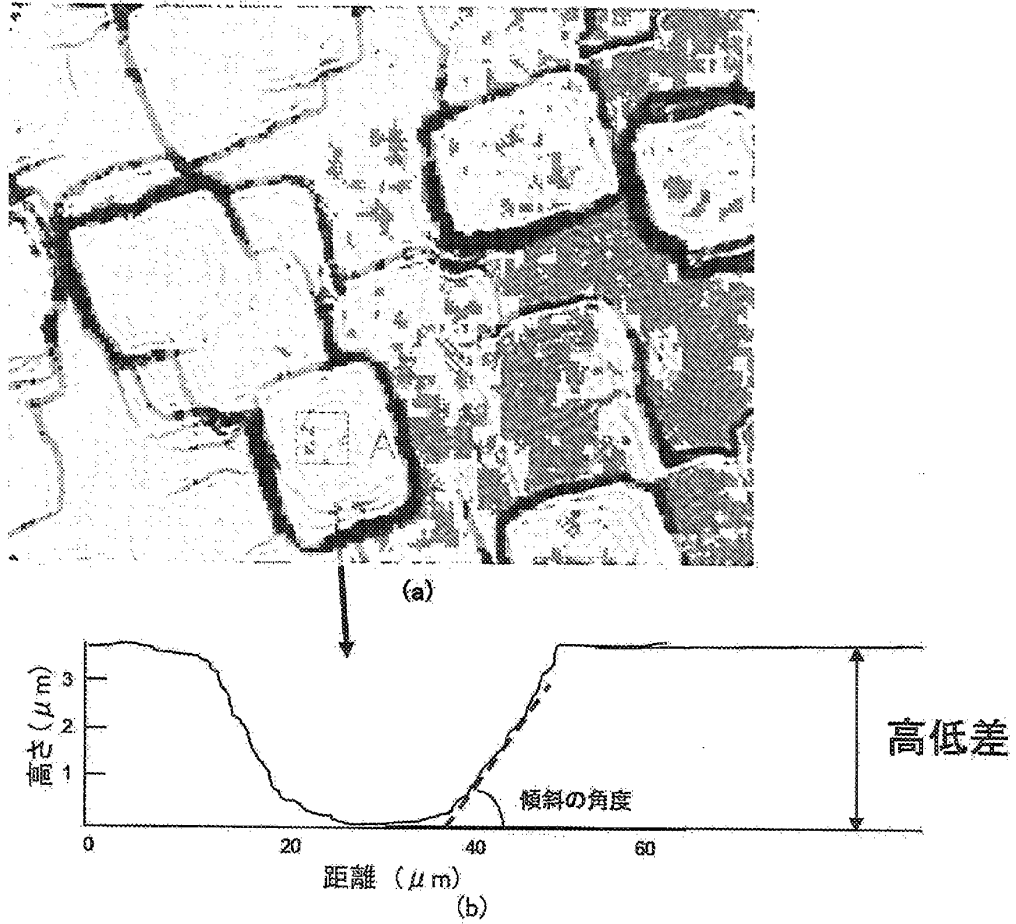


【図2】

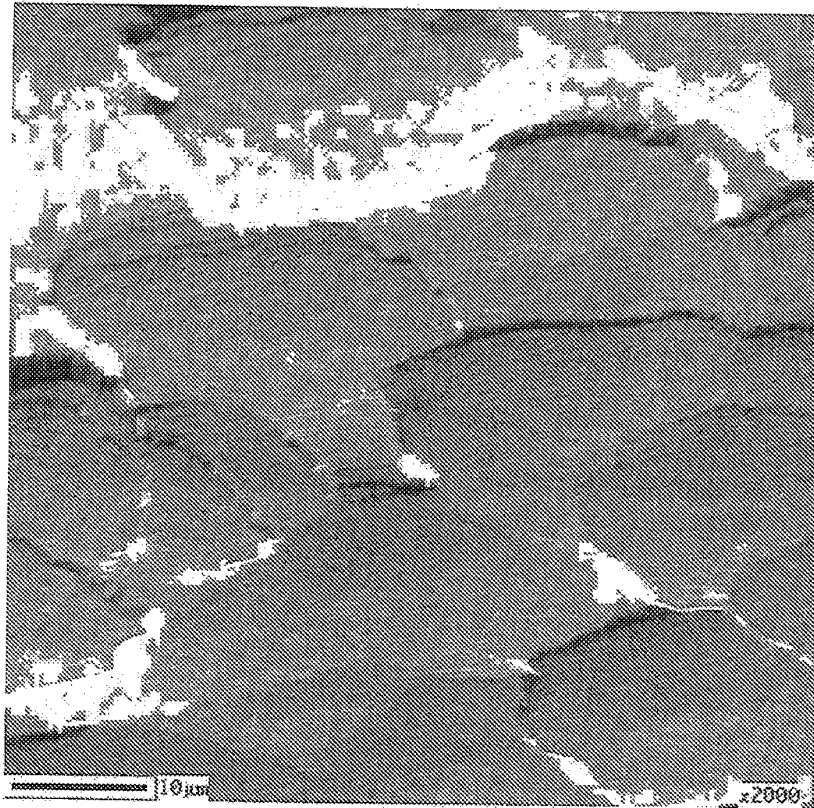


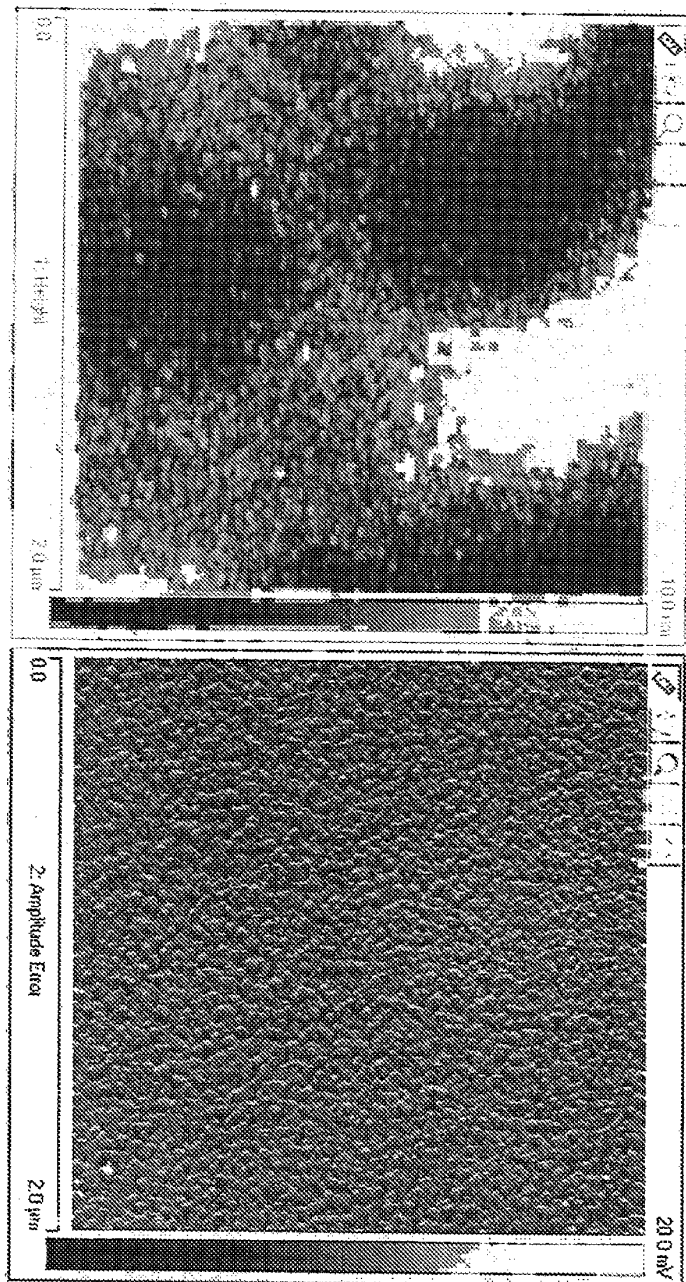
[図3]

Si(100)面の表面形状



[図4]



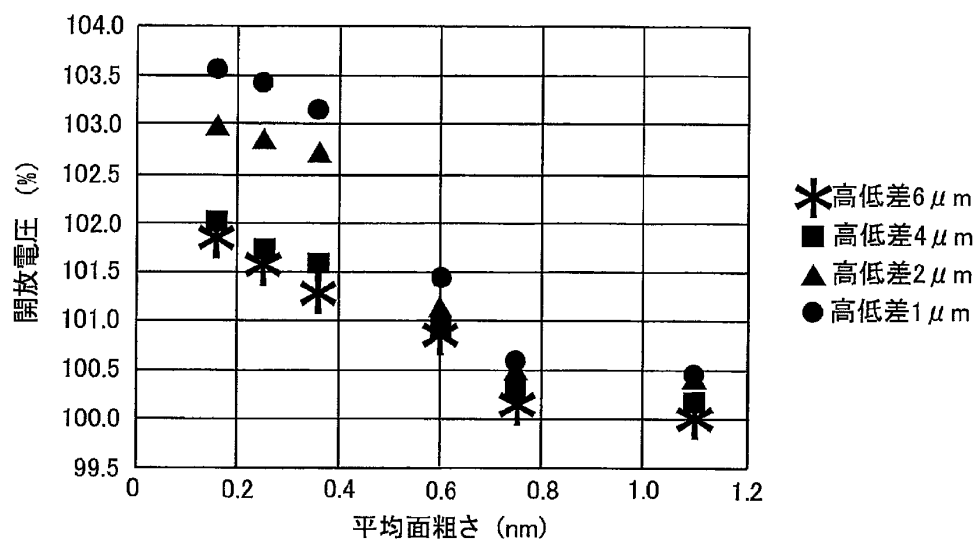


[5]

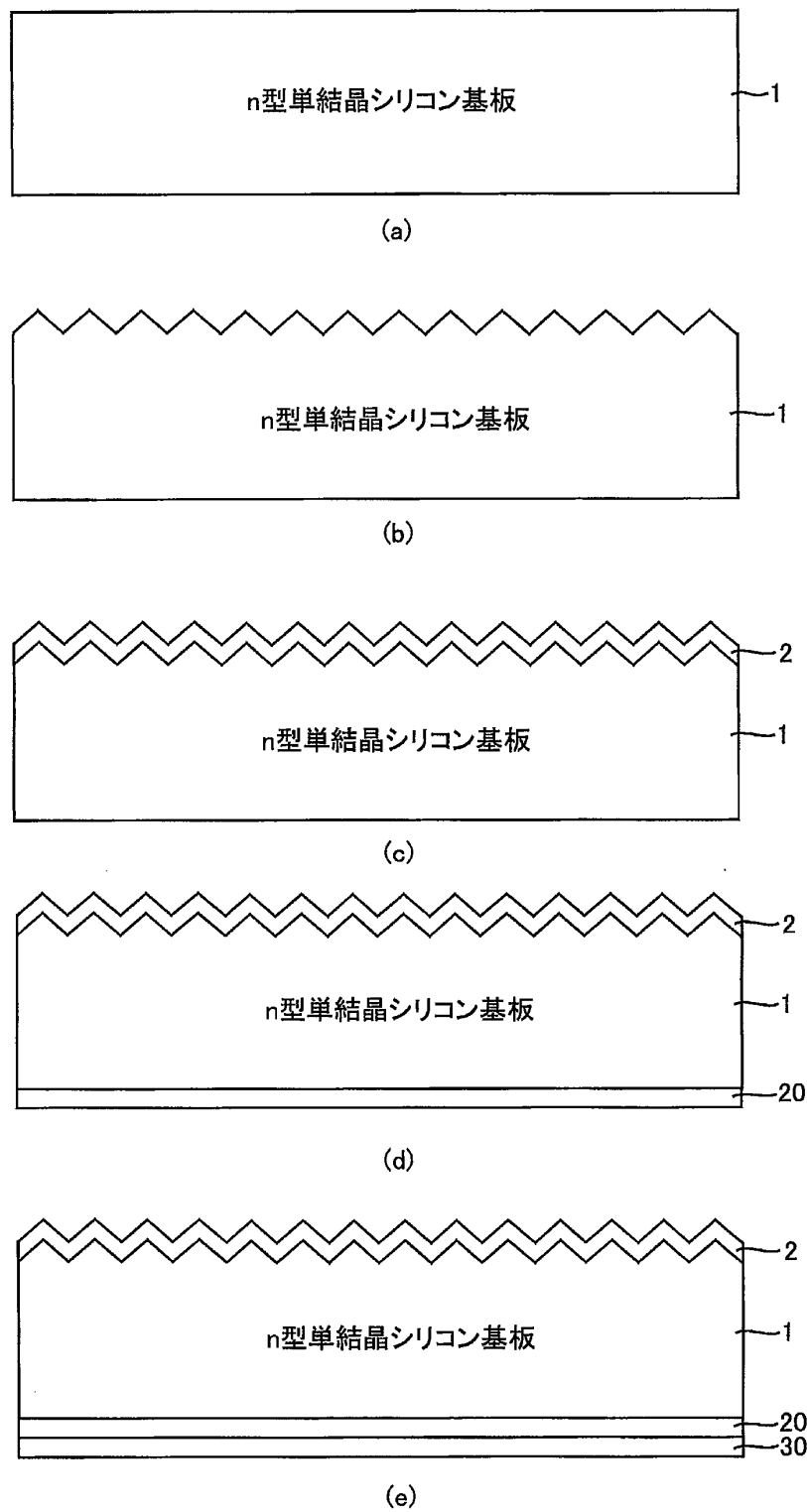
WO 2015/122257

PCT/JP2015/051790

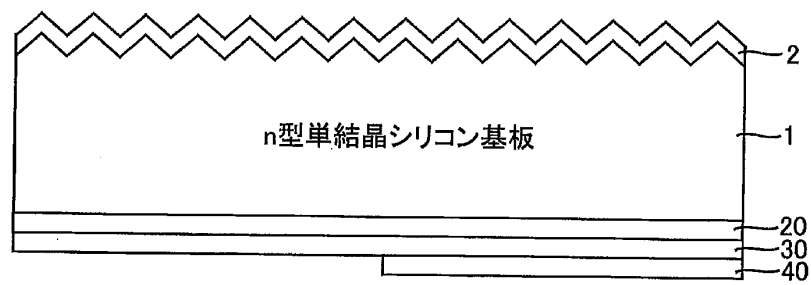
[図6]



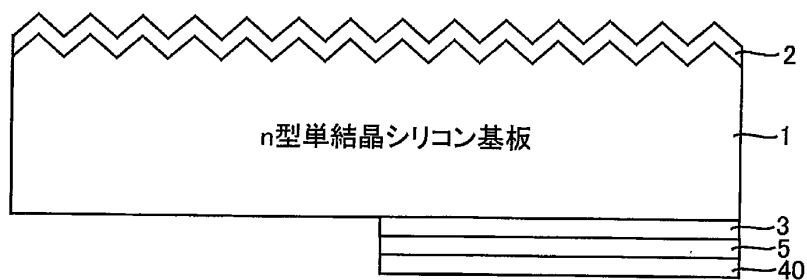
[図7]



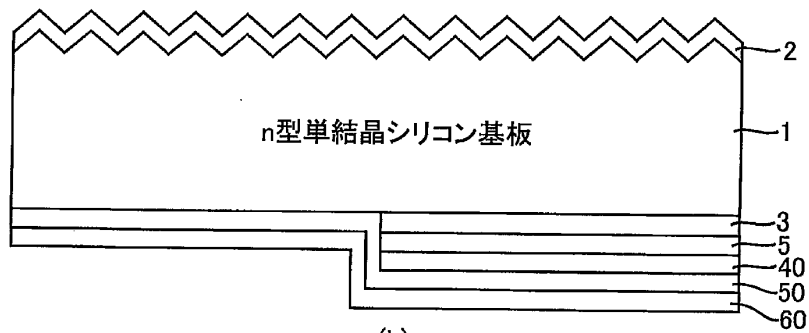
[図8]



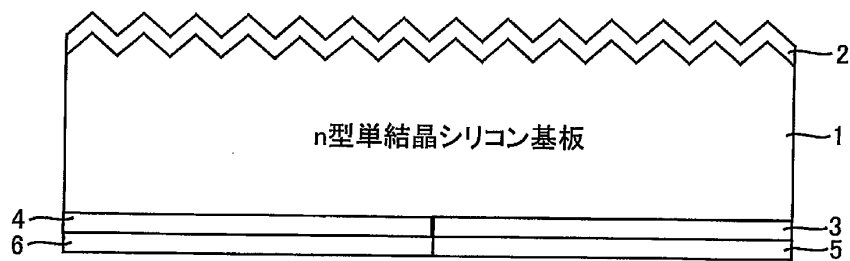
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(g)

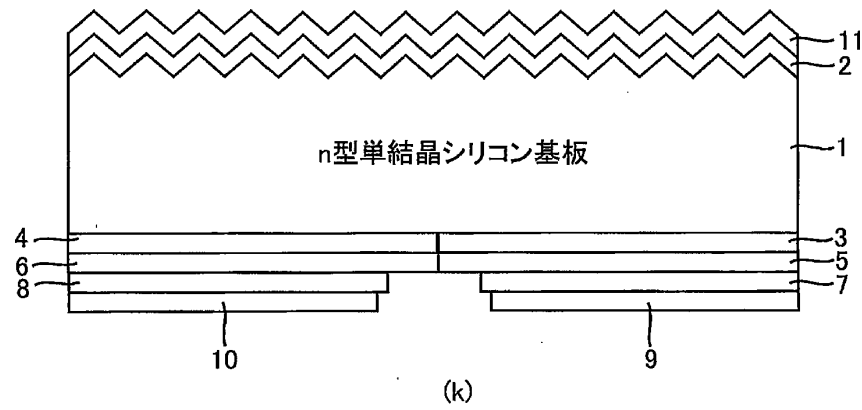
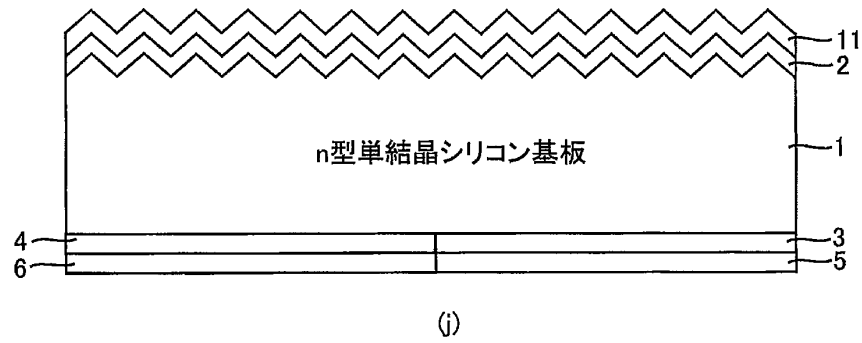


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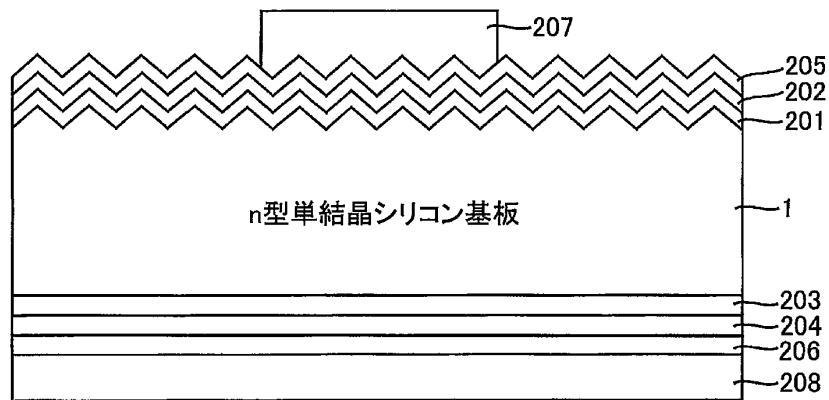
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【図9】

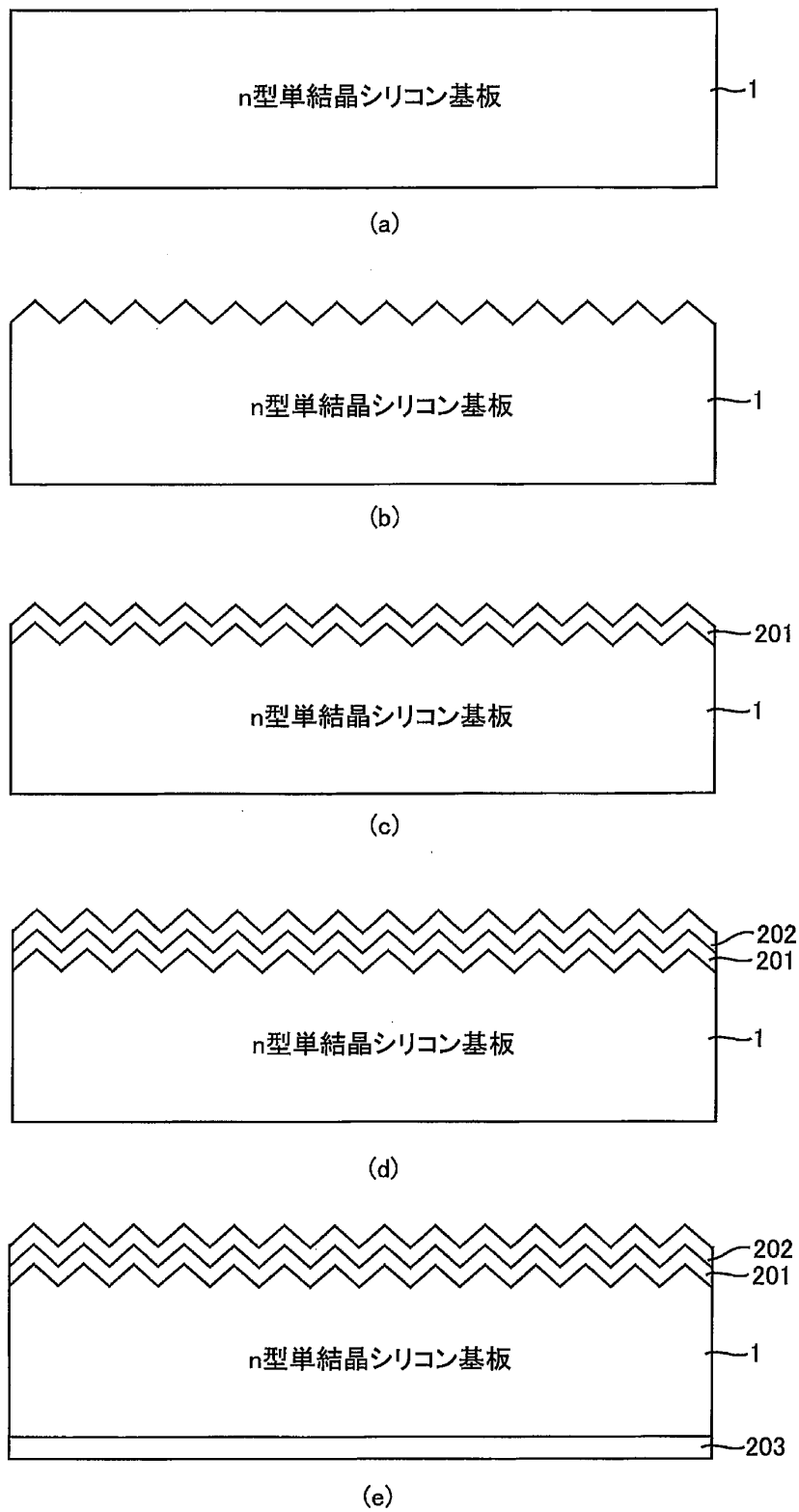


【図10】

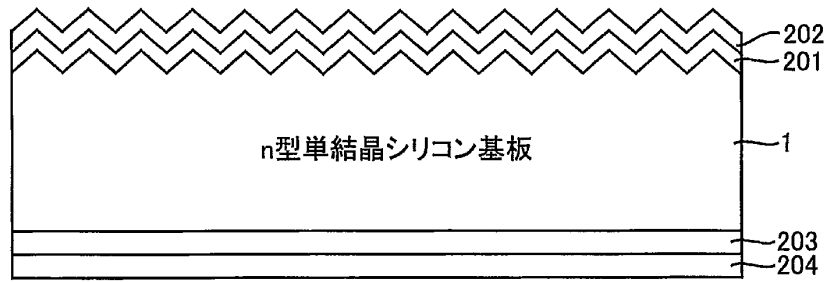
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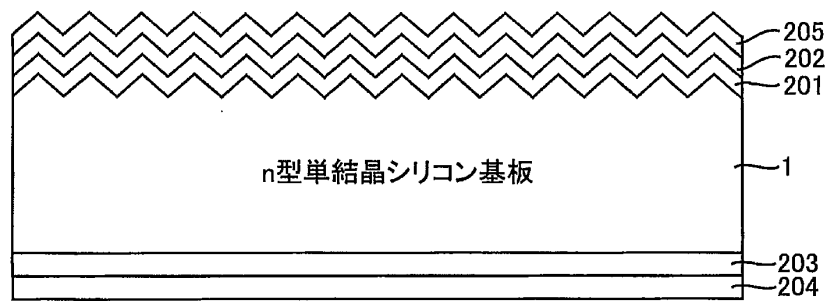
[図11]



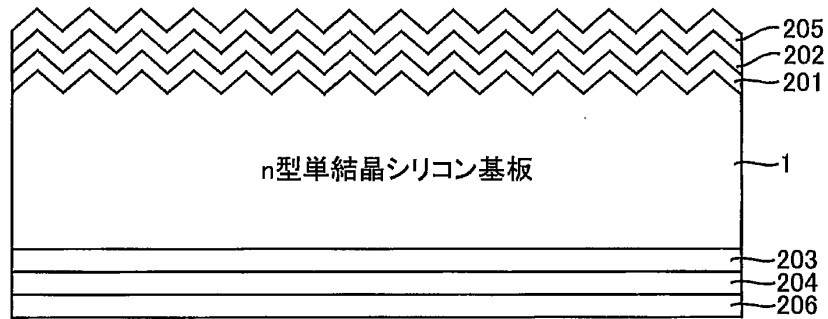
[図12]



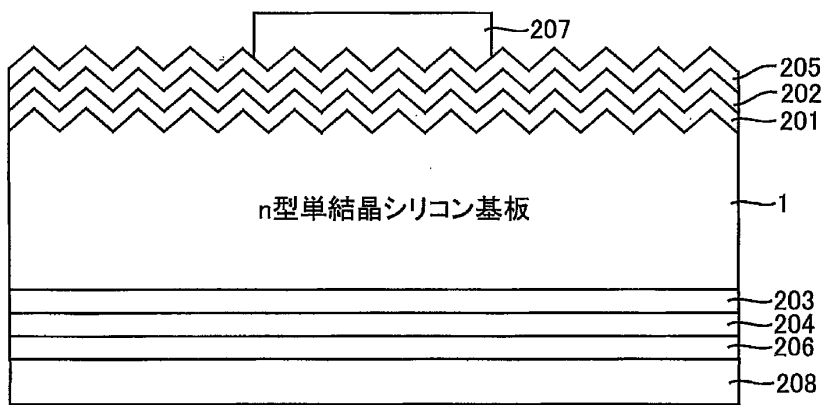
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(g)

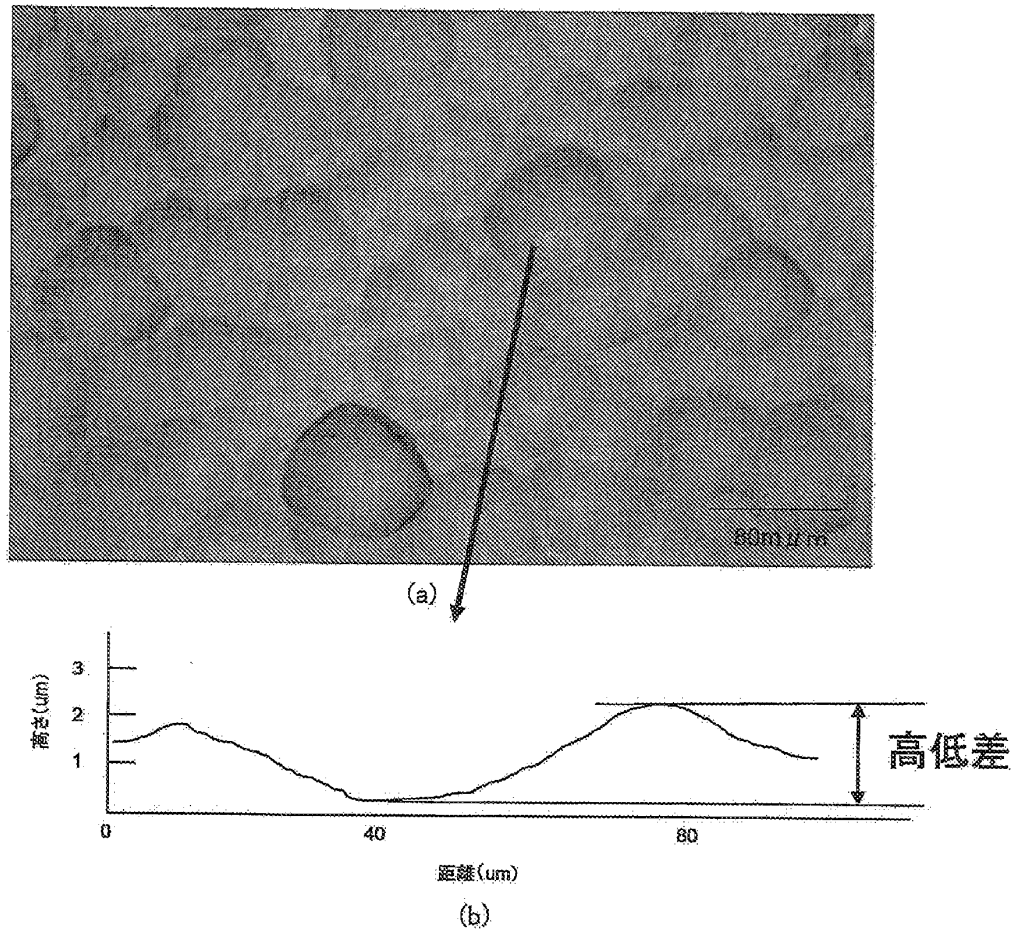


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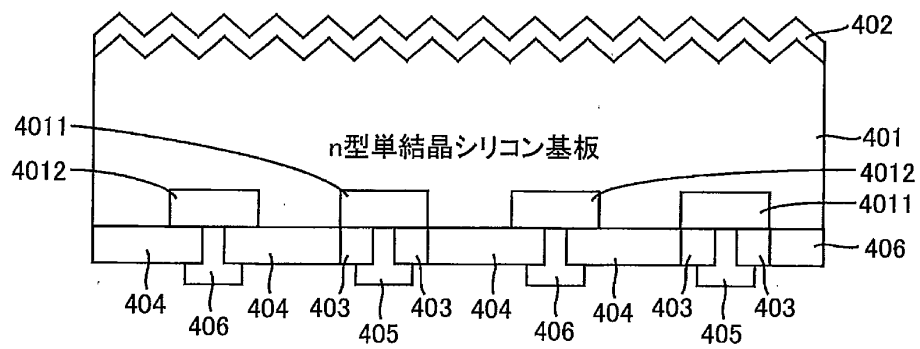
(i)

[図13]

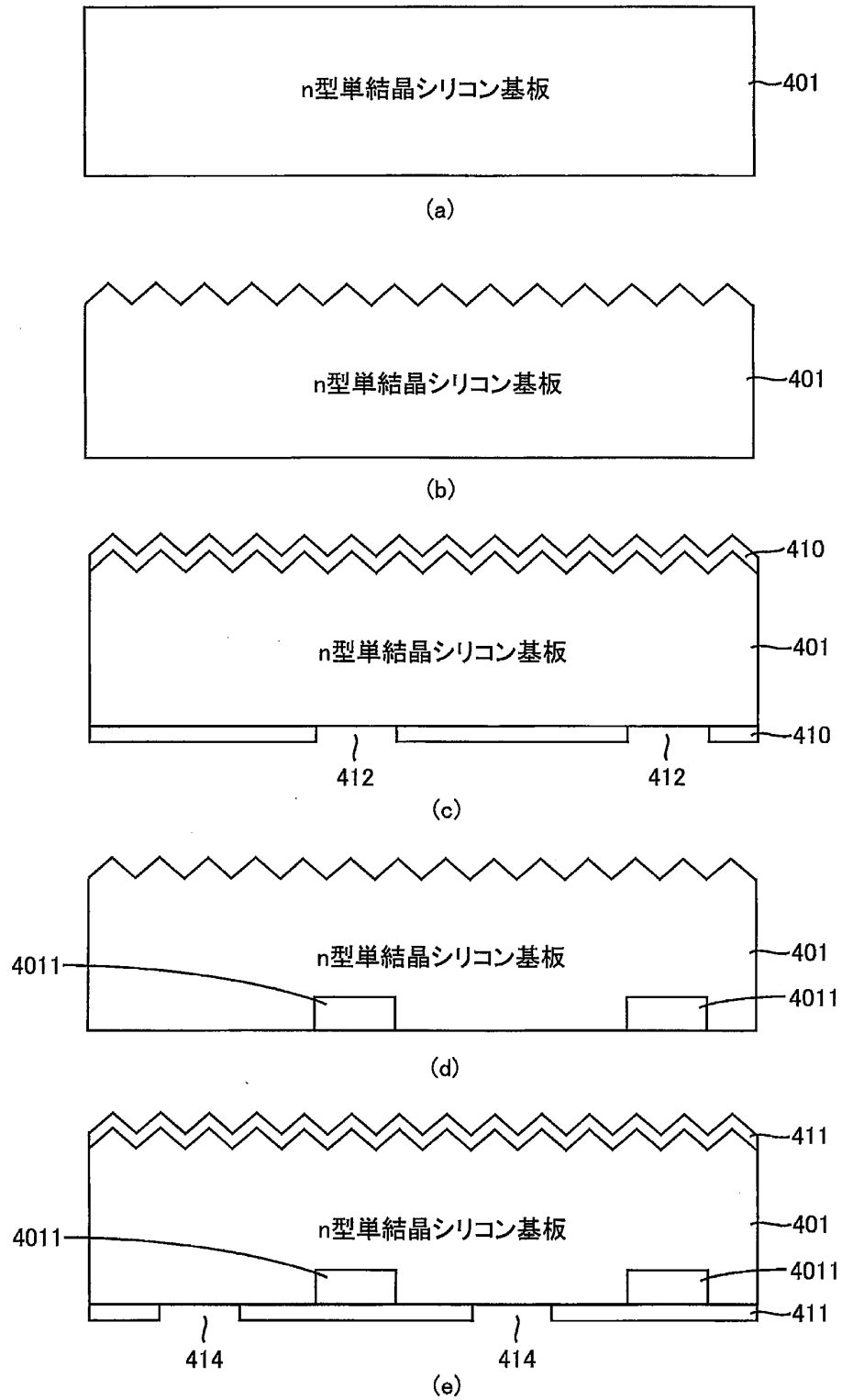


[図14]

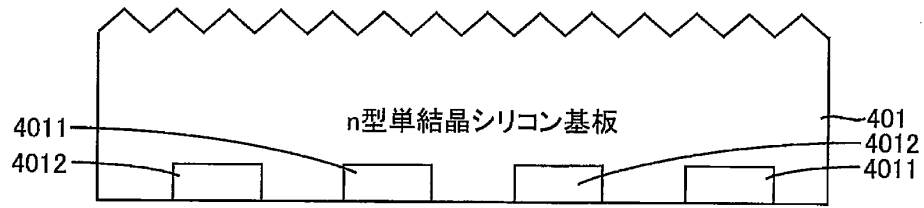
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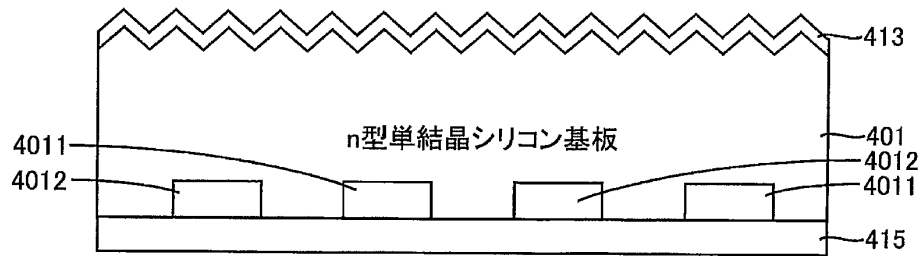
[図15]



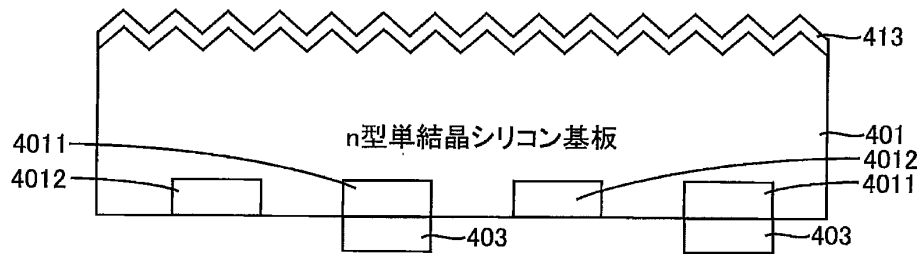
[図16]



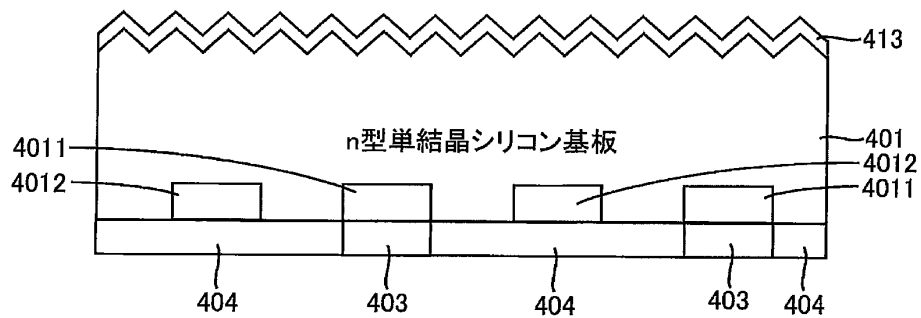
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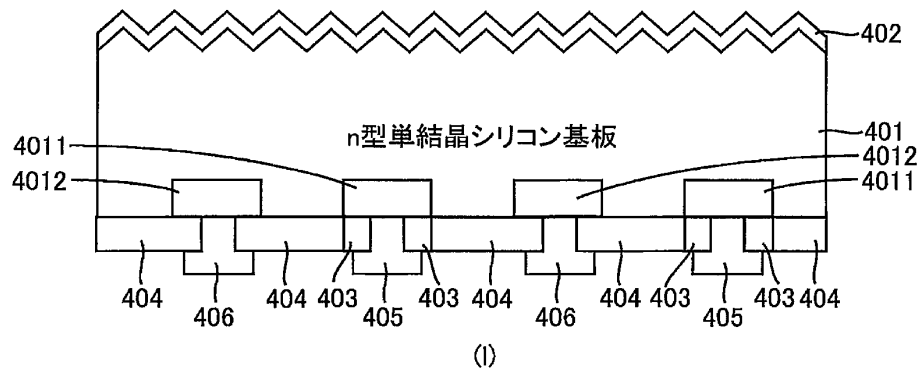
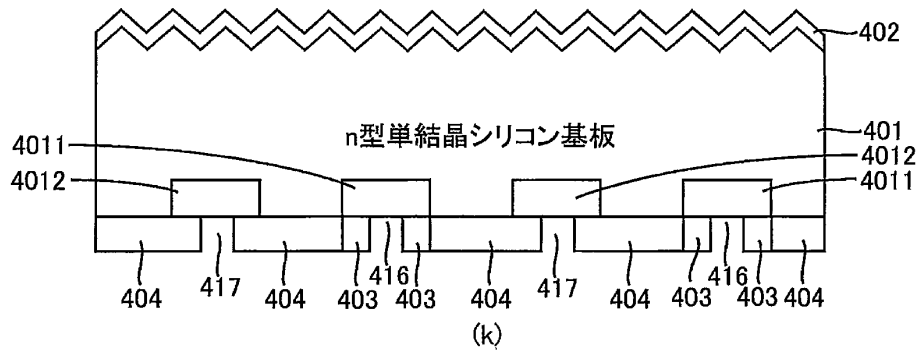
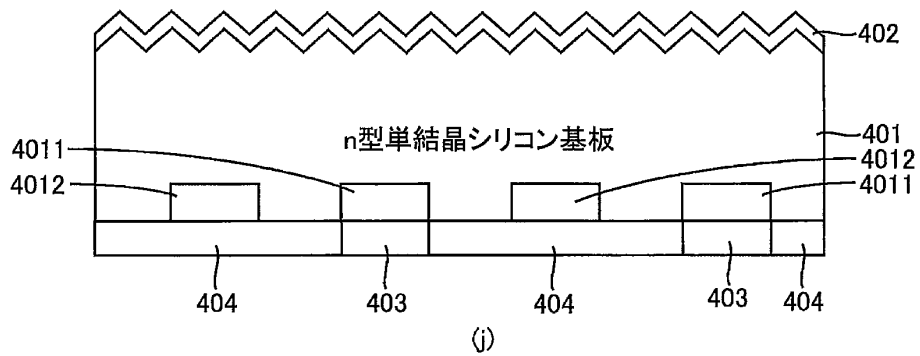


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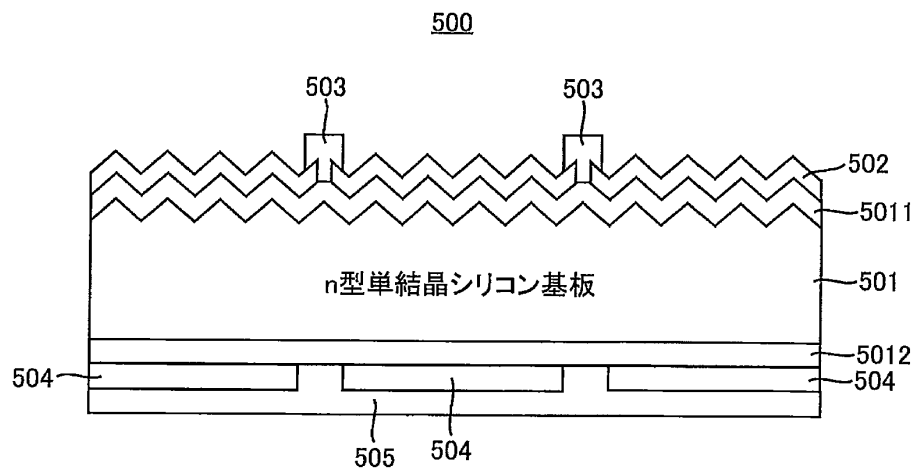


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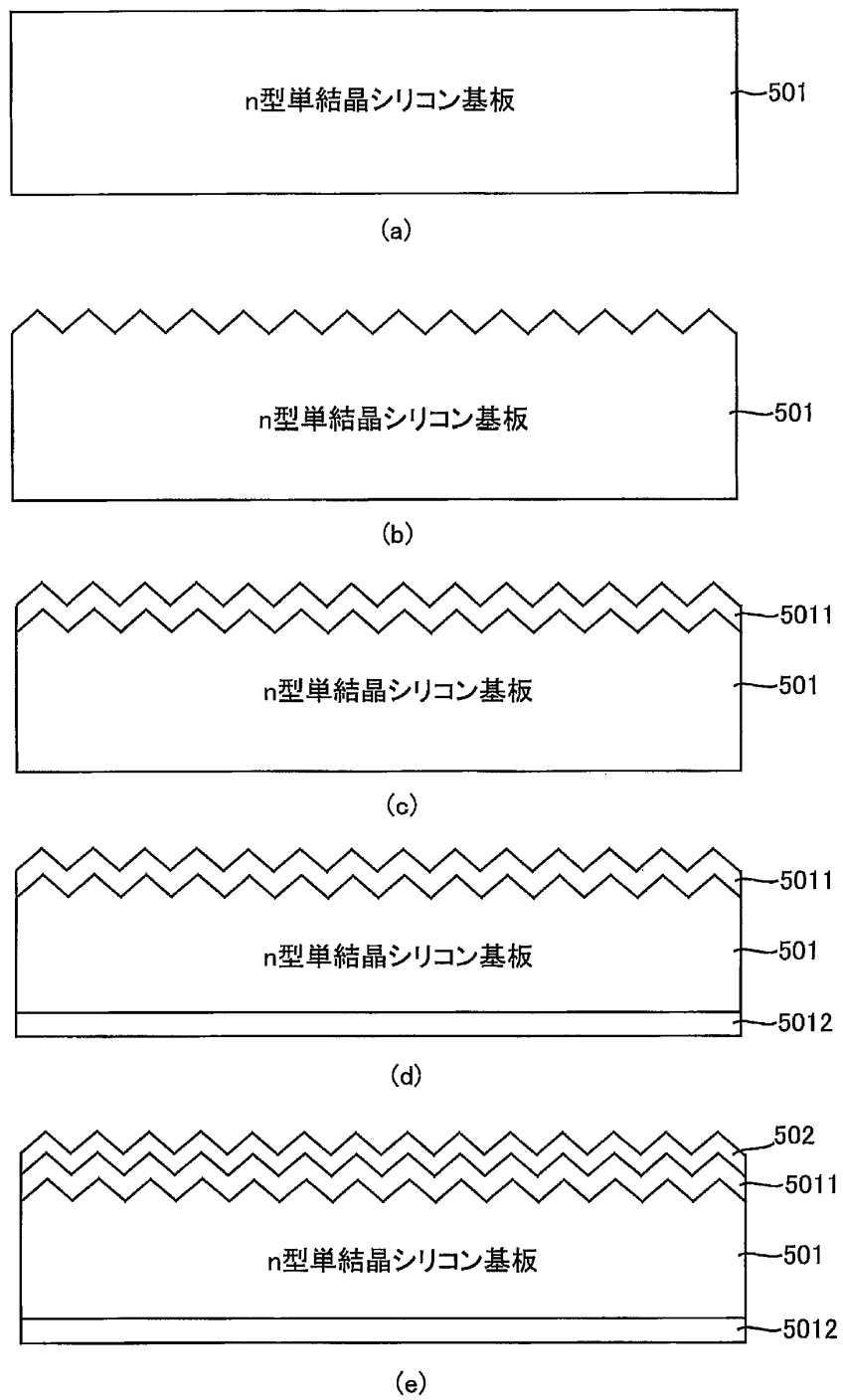
[図17]



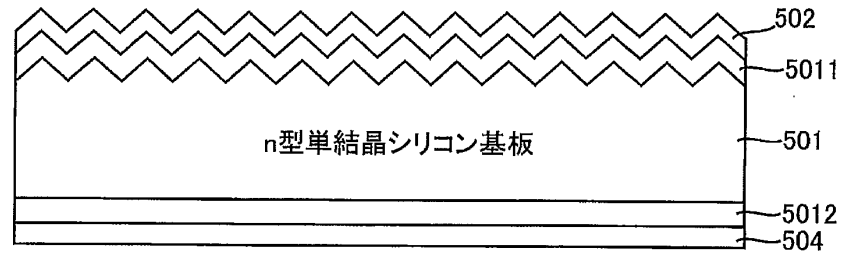
[図18]



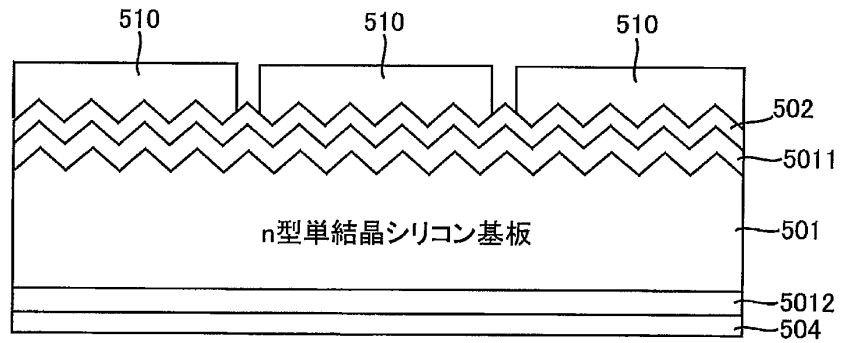
[図19]



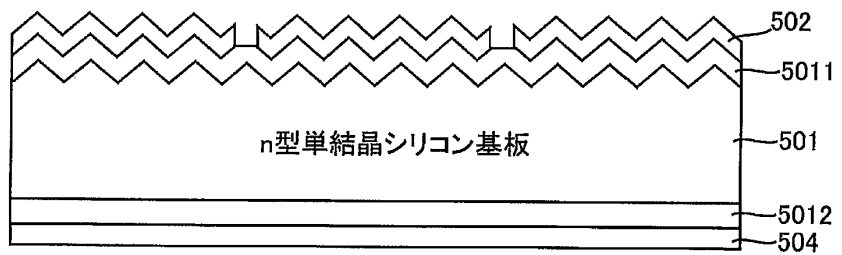
[図20]



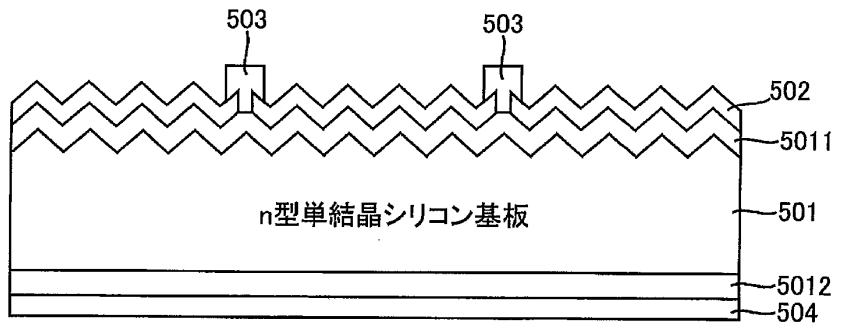
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(g)

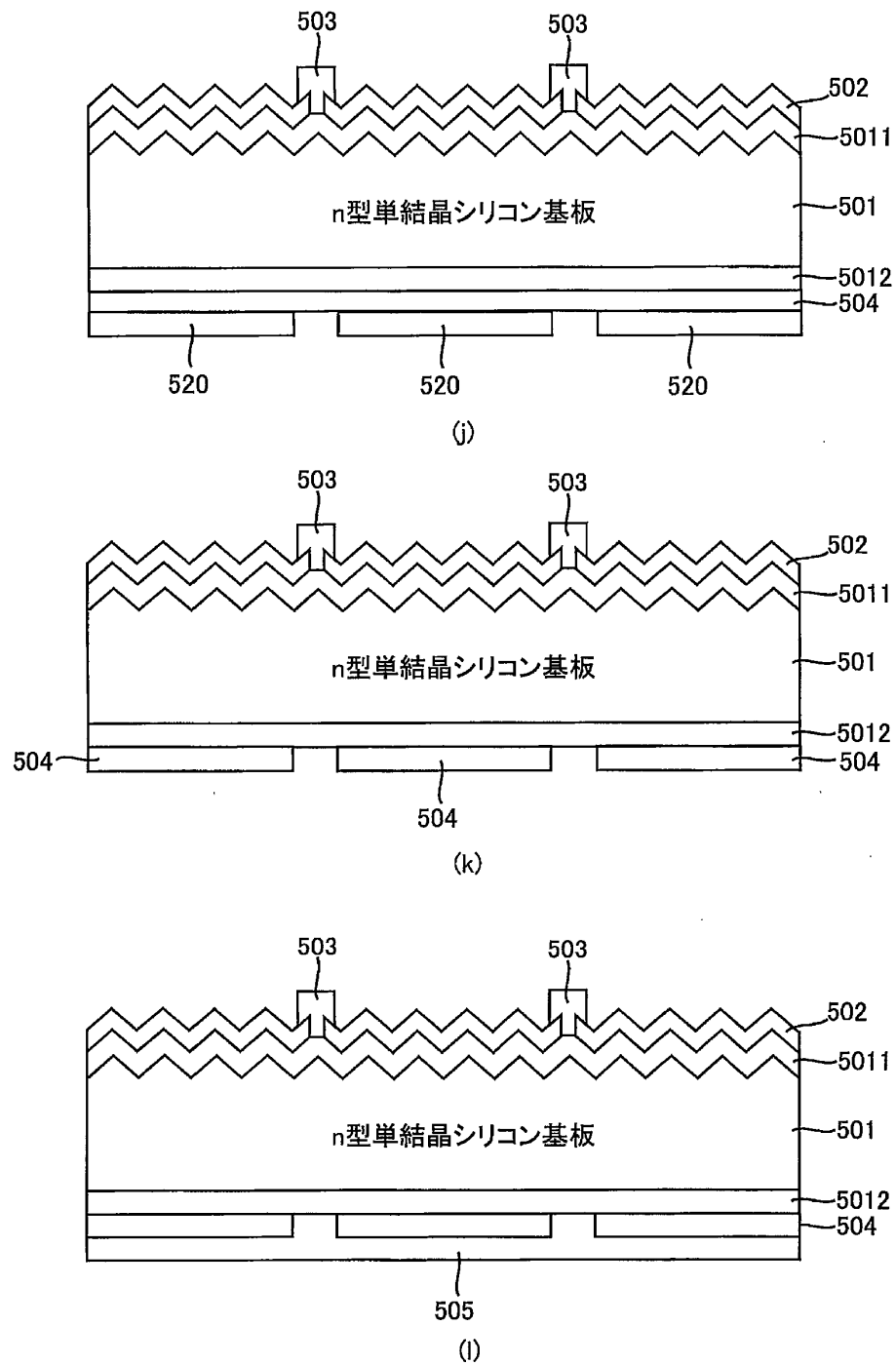


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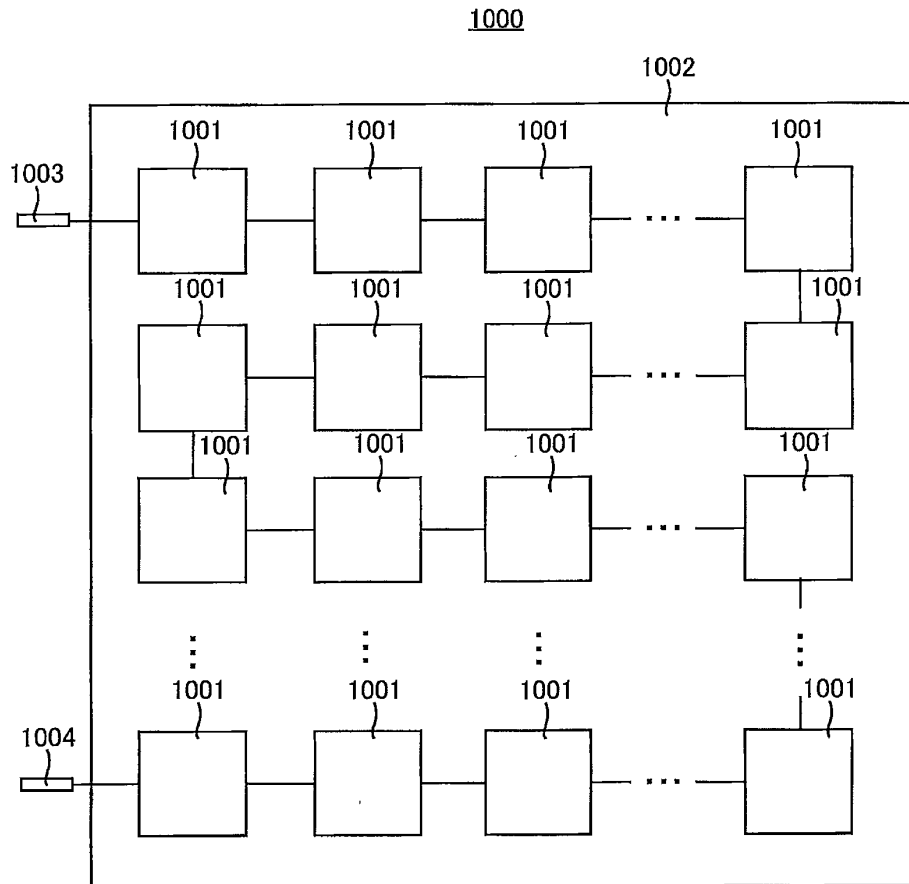


(i)

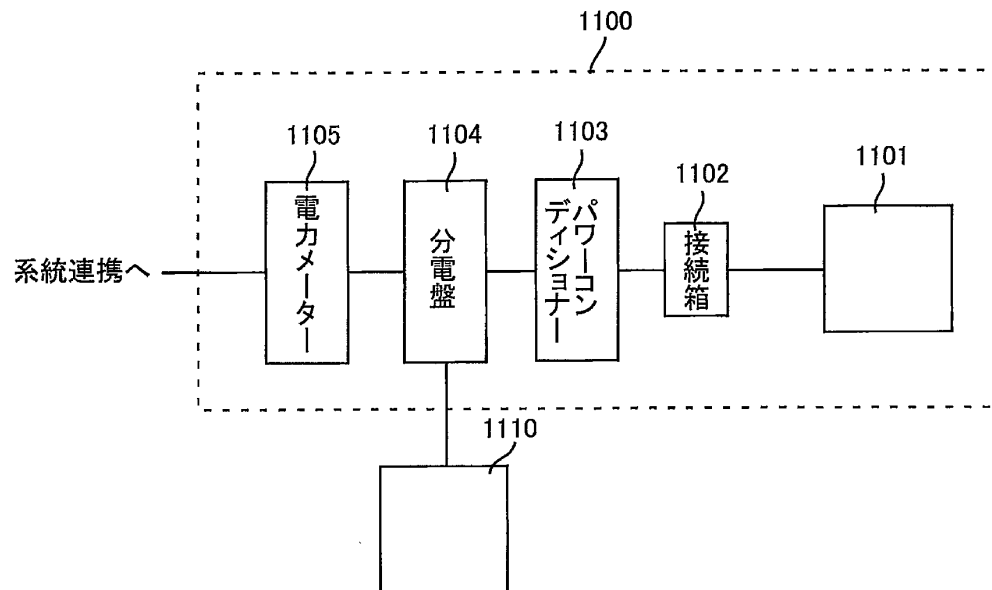
[図21]



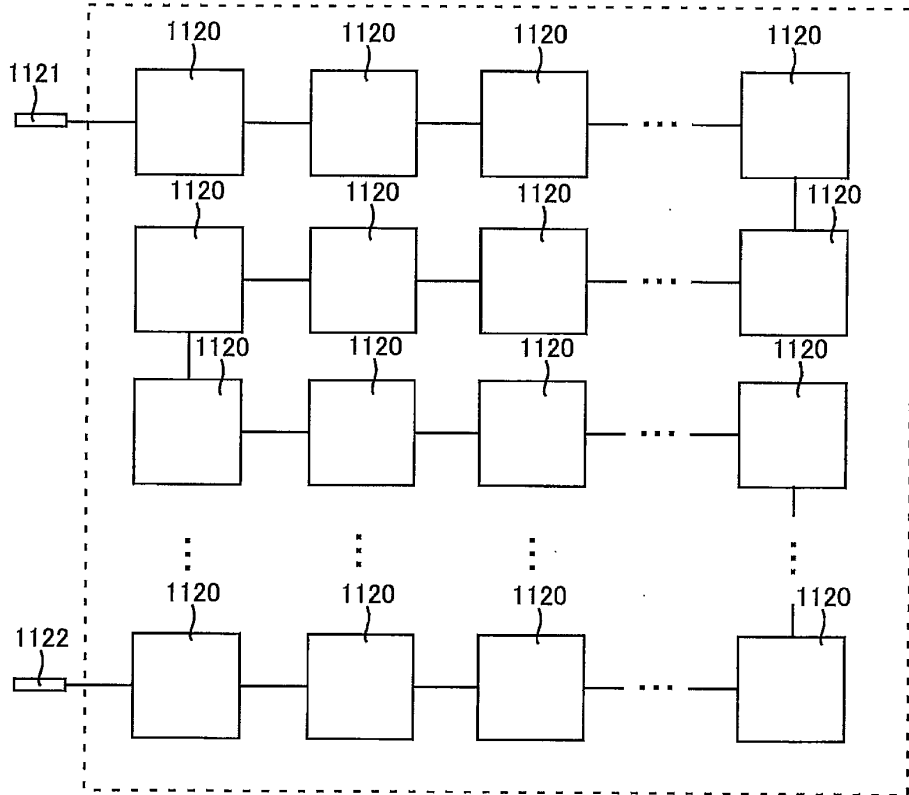
[図22]



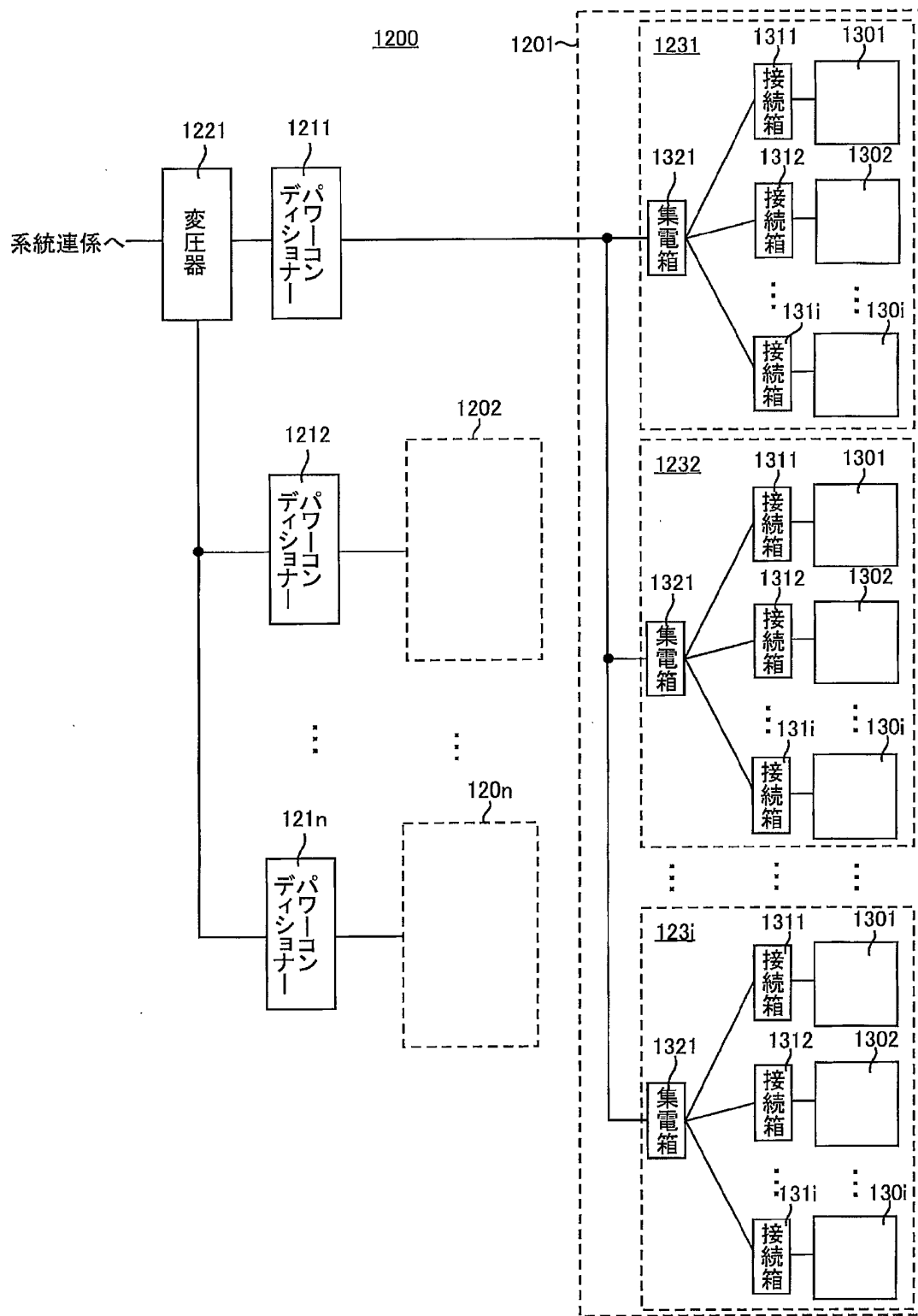
[図23]



[図24]

1101

[図25]



INTERNATIONAL SEARCH REPORT

International application No.

PCT/JP2015/051790

A. CLASSIFICATION OF SUBJECT MATTER

H01L31/0248(2006.01)i, H01L31/0747(2012.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L31/0248, H01L31/0747

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Jitsuyo Shinan Koho 1922-1996 Jitsuyo Shinan Toroku Koho 1996-2015
Kokai Jitsuyo Shinan Koho 1971-2015 Toroku Jitsuyo Shinan Koho 1994-2015

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	EP 2421057 A2 (LG ELECTRONICS INC.), 22 February 2012 (22.02.2012), paragraphs [0036] to [0106]; fig. 1 to 3 & US 2012/0042945 A1	1-5
Y	JP 2011-77240 A (Sanyo Electric Co., Ltd.), 14 April 2011 (14.04.2011), paragraphs [0009] to [0011], [0014] to [0040]; fig. 1 to 2 (Family: none)	1-5
Y	JP 2012-216788 A (Panasonic Corp.), 08 November 2012 (08.11.2012), paragraph [0020]; fig. 1-1, 5 (Family: none)	1-5

☒ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search
27 March 2015 (27.03.15)

Date of mailing of the international search report
07 April 2015 (07.04.15)

Name and mailing address of the ISA/
Japan Patent Office
3-4-3, Kasumigaseki, Chiyoda-ku,
Tokyo 100-8915, Japan

Authorized officer

Telephone No.

Form PCT/ISA/210 (second sheet) (July 2009)

BNSDOCID: -WO_2015122257A1_1_>

INTERNATIONAL SEARCH REPORT

International application No.

PCT/JP2015/051790

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	JP 2012-222300 A (Panasonic Corp.), 12 November 2012 (12.11.2012), entire text; all drawings (Family: none)	1-5
A	JP 11-191632 A (Sharp Corp.), 13 July 1999 (13.07.1999), entire text; all drawings (Family: none)	1-5
A	WO 2008/037658 A2 (COMMISSARIAT A L'ENERGIE ATOMIQUE), 03 April 2008 (03.04.2008), entire text; all drawings & JP 2010-504636 A & US 2010/0087031 A1	1-5
P,A	WO 2014/042114 A1 (Sharp Corp.), 20 March 2014 (20.03.2014), entire text; all drawings & JP 2014-56918 A	1-5
P,A	JP 2014-170775 A (Panasonic Corp.), 18 September 2014 (18.09.2014), entire text; all drawings & US 2014/0246092 A1	1-5

A. 発明の属する分野の分類 (国際特許分類 (IPC)) Int.Cl. H01L31/0248(2006.01)i, H01L31/0747(2012.01)i		
B. 調査を行った分野 調査を行った最小限資料 (国際特許分類 (IPC)) Int.Cl. H01L31/0248, H01L31/0747		
最小限資料以外の資料で調査を行った分野に含まれるもの 日本国実用新案公報 1922-1996年 日本国公開実用新案公報 1971-2015年 日本国実用新案登録公報 1996-2015年 日本国登録実用新案公報 1994-2015年		
国際調査で使用した電子データベース (データベースの名称、調査に使用した用語)		
C. 関連すると認められる文献		
引用文献の カテゴリー*	引用文献名 及び一部の箇所が関連するときは、その関連する箇所の表示	関連する 請求項の番号
Y	EP 2421057 A2 (LG ELECTRONICS INC.) 2012.02.22, [0036]ー[0106], 図 1-3 & US 2012/0042945 A1	1-5
Y	JP 2011-77240 A (三洋電機株式会社) 2011.04.14, [0009]ー[0011], [0014]ー[0040], 図 1-2 (ファミリーなし)	1-5
Y	JP 2012-216788 A (パナソニック株式会社) 2012.11.08, [0020], 図 1-1, 5 (ファミリーなし)	1-5
☒ C欄の続きにも文献が列挙されている。 ☐ パテントファミリーに関する別紙を参照。		
* 引用文献のカテゴリー 「A」 特に関連のある文献ではなく、一般的技術水準を示すもの 「E」 国際出願日前の出願または特許であるが、国際出願日後に公表されたもの 「L」 優先権主張に疑義を提起する文献又は他の文献の発行日若しくは他の特別な理由を確立するために引用する文献 (理由を付す) 「O」 口頭による開示、使用、展示等に言及する文献 「P」 国際出願日前で、かつ優先権の主張の基礎となる出願日の後に公表された文献 「T」 国際出願日又は優先日後に公表された文献であって出願と矛盾するものではなく、発明の原理又は理論の理解のために引用するもの 「X」 特に関連のある文献であって、当該文献のみで発明の新規性又は進歩性がないと考えられるもの 「Y」 特に関連のある文献であって、当該文献と他の1以上の文献との、当業者にとって自明である組合せによって進歩性がないと考えられるもの 「&」 同一パテントファミリー文献		
国際調査を完了した日 27.03.2015	国際調査報告の発送日 07.04.2015	
国際調査機関の名称及びあて先 日本国特許庁 (ISA/J P) 郵便番号 100-8915 東京都千代田区霞が関三丁目4番3号	特許庁審査官 (権限のある職員) 堀部 修平 電話番号 03-3581-1101 内線 3255	2K 9215

様式 PCT/ISA/210 (第2ページ) (2009年7月)

C (続き) . 関連すると認められる文献		
引用文献の カテゴリー*	引用文献名 及び一部の箇所が関連するときは、その関連する箇所の表示	関連する 請求項の番号
A	JP 2012-222300 A (パナソニック株式会社) 2012. 11. 12, 全文, 全図 (ファミリーなし)	1-5
A	JP 11-191632 A (シャープ株式会社) 1999. 07. 13, 全文, 全図 (ファミリーなし)	1-5
A	WO 2008/037658 A2 (COMMISSARIAT A L'ENERGIE ATOMIQUE) 2008. 04. 03, 全文, 全図 & JP 2010-504636 A & US 2010/0087031 A1	1-5
P, A	WO 2014/042114 A1 (シャープ株式会社) 2014. 03. 20, 全文, 全図 & JP 2014-56918 A	1-5
P, A	JP 2014-170775 A (パナソニック株式会社) 2014. 09. 18, 全文, 全図 & US 2014/0246092 A1	1-5

様式 PCT/ISA/210 (第2ページの続き) (2009年7月)

Electronic Acknowledgement Receipt	
EFS ID:	44641874
Application Number:	17459689
International Application Number:	
Confirmation Number:	8617
Title of Invention:	SOLAR CELL, MANUFACTURING METHOD THEREOF, AND PHOTOVOLTAIC MODULE
First Named Inventor/Applicant Name:	Kun YU
Customer Number:	22204
Filer:	Jeffrey Costellia/Donald Sias
Filer Authorized By:	Jeffrey Costellia
Attorney Docket Number:	084546-000033
Receipt Date:	30-DEC-2021
Filing Date:	27-AUG-2021
Time Stamp:	14:04:13
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal Letter	084546_000033_IDS_Transmittal.pdf	102603 084aaa59e4d444dd6263d2f82a905bab4521446	no	2

Warnings:

Information:					
2	Information Disclosure Statement (IDS) Form (SB08)	084546_33_PTO_1449.pdf	116740	no	1
			9328a47ee4ce7a8321b977733dfac842b2cdff1d3		
Warnings:					
Information:					
This is not an USPTO supplied IDS fillable form					
3	Foreign Reference	CN111628049.pdf	1529127	no	19
			3f7c4506a578d1e6ee4a23a9daa726a8634cdff14		
Warnings:					
Information:					
4	Foreign Reference	CN212750903.pdf	1060505	no	9
			559d368af5fb22c097120450ff4093798a76bcb9		
Warnings:					
Information:					
5	Foreign Reference	EP2149915.pdf	1232482	no	18
			52c46337d09a57d7291d1d346b0fecf2cfaa72b2		
Warnings:					
Information:					
6	Foreign Reference	EP2645421.pdf	2720762	no	28
			cc3982cfd1b808be4e0283eb17df4136c72aa169		
Warnings:					
Information:					
7	Non Patent Literature	European_Search_Report.pdf	384556	no	7
			ac91b025c0a449d1cfb5367f4ed565830e2762f6		
Warnings:					
Information:					
8	Foreign Reference	WO2015122257.pdf	5274239	no	69
			0b7922f77dbe89db0d6dc2ade87636fc1c500d6c		
Warnings:					
Information:					

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application	)	
Kun YU et al.	)	Art Unit: Not Yet Assigned
Application No.: 17/459,689	)	Examiner: Not Yet Assigned
Filed: August 27, 2021	)	Confirmation No.: 8617
For: SOLAR CELL, MANUFACTURING	)	
METHOD THEREOF, AND	)	
PHOTOVOLTAIC MODULE	)	

INFORMATION DISCLOSURE STATEMENT

Mail Stop Amendment – Via EFS

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In accordance with the duty of disclosure as set forth in 37 C.F.R. § 1.56, Applicant hereby submits the following information in conformance with 37 C.F.R. §§ 1.97 and 1.98. In accordance with the policies of the U.S. Patent and Trademark Office, only copies of newly cited foreign patents and non-patent literature are being submitted.

Foreign Communication – European Search Report

Applicant notes that the *Foreign Patent Documents*: CN-111628049; CN-212750903; EP-2 149 915; EP-2 645 421 and WO-2015/122257 listed in the attached Form PTO-1449 were previously cited by European Patent Office in an Extended European Search Report mailed **December 2, 2021** (copy enclosed) issued in a counterpart European Patent Application No. 21194044.0.

The undersigned certifies that each item of information contained in this information disclosure statement was first cited in any communication from a foreign patent office in connection with a counterpart foreign application not more than three (3) months prior to the filing of this statement.

It is requested that the accompanying Form PTO-1449 be considered and made of record in the above-identified application and that an Examiner-initialed copy of this form be returned to the undersigned.

The present Information Disclosure Statement is filed within three months of filing, or before the mailing of a first Office action on the merits, whichever is later; therefore, no fee is believed to be necessary at this time.

4868-3937-1528.1

However, if a fee becomes necessary, the Commissioner is hereby authorized by this paper to charge any additional fees, except the issue fee, during the entire pendency of this application including fees due under 37 C.F.R. §§ 1.16 and 1.17 which may be required, including any required extension of time fees, or credit any overpayment to Deposit Account No. 19-2380.

Respectfully submitted,

/Jeffrey L. Costellia, Reg. No. 35,483/
Jeffrey L. Costellia
Registration No. 35,483

NIXON PEABODY LLP
CUSTOMER NO.: 22204
799 9th Street, N.W., Suite 500
Washington, DC 20001-4501
Tel: 202-585-8000



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
17/459,689	08/27/2021	Kun YU	084546-000033

CONFIRMATION NO. 8617

POA ACCEPTANCE LETTER



22204
NIXON PEABODY, LLP
799 Ninth Street, NW
SUITE 500
WASHINGTON, DC 20001

Date Mailed: 10/06/2021

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 10/01/2021.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at (571) 272-4000 or (571) 272-4200 or 1-888-786-0101.

/qtran/

Electronic Acknowledgement Receipt	
EFS ID:	43922687
Application Number:	17459689
International Application Number:	
Confirmation Number:	8617
Title of Invention:	SOLAR CELL, MANUFACTURING METHOD THEREOF, AND PHOTOVOLTAIC MODULE
First Named Inventor/Applicant Name:	Kun YU
Customer Number:	22204
Filer:	Jeffrey Costellia/Donald Sias
Filer Authorized By:	Jeffrey Costellia
Attorney Docket Number:	084546-000033
Receipt Date:	01-OCT-2021
Filing Date:	27-AUG-2021
Time Stamp:	13:21:34
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no				
File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Power of Attorney	084546_000033_Power_of_Attorney_Statement_Recordation.pdf	16865933 6b3e77aca7bf0e3c623f6d29b5194161fe75b0df	no	13
Warnings:					

Information:	
Total Files Size (in bytes):	16865933
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.	

Under the Paperwork Reduction Act of 1995, no person is required to respond to a collection of information unless it displays a valid OMB control number

POWER OF ATTORNEY TO PROSECUTE APPLICATIONS BEFORE THE USPTO

I hereby revoke all previous powers of attorney given in the application identified in the attached statement under 37 CFR 3.73(c).

I hereby appoint:



Practitioners associated with Customer Number:

22204

OR



Practitioner(s) named below (if more than ten patent practitioners are to be named, then a customer number must be used):

Name	Registration Number

Name	Registration Number

As attorney(s) or agent(s) to represent the undersigned before the United States Patent and Trademark Office (USPTO) in connection with any and all patent applications assigned only to the undersigned according to the USPTO assignment records or assignment documents attached to this form in accordance with 37 CFR 3.73(c).

Please change the correspondence address for the application identified in the attached statement under 37 CFR 3.73(c) to:



The address associated with Customer Number:

22204

OR



Firm or individual name

Address

City

State

Zip

Country

Telephone

Email

Assignee name and address: SHANGHAI JINKO GREEN ENERGY ENTERPRISE MANAGEMENT CO., LTD.
5/F, No. 277 Huqingping Road, Minhang District, Shanghai, China

A copy of this form, together with a statement under 37 CFR 3.73(c) (Form PTO/AIA/96 or equivalent) is required to be filed in each application in which this form is used. The statement under 37 CFR 3.73(c) may be completed by one of the practitioners appointed in this form, and must identify the application in which this Power of Attorney is to be filed.

SIGNATURE of Assignee of Record

The individual whose signature and title is supplied below is authorized to act on behalf of the assignee.

Signature

Shaofa LAN

Date 2021-09-02

Name Shaofa LAN

Telephone

Title Intellectual Property Director

This collection of information is required by 37 CFR 1.31, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public, which is to update (and by the USPTO to process) the file of a patent or reexamination proceeding. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 18 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

STATEMENT UNDER 37 CFR 3.73(c)

Applicant/Patent Owner: SHANGHAI JINKO GREEN ENERGY ENTERPRISE MANAGEMENT CO., LTD.

Application No./Patent No.: 17/459,689 Filed/Issue Date: August 27, 2021

Titled: SOLAR CELL, MANUFACTURING METHOD THEREOF, AND PHOTOVOLTAIC MODULE

SHANGHAI JINKO GREEN ENERGY ENTERPRISE MANAGEMENT CO., LTD., a corporation

(Name of Assignee)

(Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that, for the patent application/patent identified above, it is (choose **one** of options 1, 2, 3 or 4 below):

1. ☒ The assignee of the entire right, title, and interest.

2. ☐ An assignee of less than the entire right, title, and interest (check applicable box):

☐ The extent (by percentage) of its ownership interest is ____%. Additional Statement(s) by the owners holding the balance of the interest must be submitted to account for 100% of the ownership interest.

☐ There are unspecified percentages of ownership. The other parties, including inventors, who together own the entire right, title and interest are:

Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

3. ☐ The assignee of an undivided interest in the entirety (a complete assignment from one of the joint inventors was made). The other parties, including inventors, who together own the entire right, title, and interest are:

Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

4. ☐ The recipient, via a court proceeding or the like (e.g., bankruptcy, probate), of an undivided interest in the entirety (a complete transfer of ownership interest was made). The certified document(s) showing the transfer is attached.

The interest identified in option 1, 2 or 3 above (not option 4) is evidenced by either (choose **one** of options A or B below):

A. ☒ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel 057314, Frame 0980, or for which a copy thereof is attached.

B. ☐ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

2. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

[Page 1 of 2]

This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

STATEMENT UNDER 37 CFR 3.73(c)

3. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

4. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

5. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

6. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

☐ Additional documents in the chain of title are listed on a supplemental sheet(s).

☒ As required by 37 CFR 3.73(c)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

/Jeffrey L. Costellia, Reg. No. 35,483/

October 1, 2021

Signature

Date

Jeffrey L. Costellia, Attorney of Record

35,483

Printed or Typed Name

Title or Registration Number

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

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POWER OF ATTORNEY TO PROSECUTE APPLICATIONS BEFORE THE USPTO

I hereby revoke all previous powers of attorney given in the application identified in the attached statement under 37 CFR 3.73(c).

I hereby appoint:

☒

Practitioners associated with Customer Number:

22204

OR

☐

Practitioner(s) named below (if more than ten patent practitioners are to be named, then a customer number must be used):

Name	Registration Number

Name	Registration Number

As attorney(s) or agent(s) to represent the undersigned before the United States Patent and Trademark Office (USPTO) in connection with any and all patent applications assigned only to the undersigned according to the USPTO assignment records or assignment documents attached to this form in accordance with 37 CFR 3.73(c).

Please change the correspondence address for the application identified in the attached statement under 37 CFR 3.73(c) to:

☒

The address associated with Customer Number: 22204

OR

☐

Firm or individual name

Address

City

State

Zip

Country

Telephone

Email

Assignee name and address: ZHEJIANG JINKO SOLAR CO., LTD.
No. 58, Yuan Xi Road, Yuan Hua Town, Haining,
Zhejiang, China

A copy of this form, together with a statement under 37 CFR 3.73(c) (Form PTO/AIA/96 or equivalent) is required to be filed in each application in which this form is used. The statement under 37 CFR 3.73(c) may be completed by one of the practitioners appointed in this form, and must identify the application in which this Power of Attorney is to be filed.

SIGNATURE of Assignee of Record

The individual whose signature and title is supplied below is authorized to act on behalf of the assignee.

Signature

Shaofa LAN

Date 2021-09-02

Name Shaofa LAN

Telephone

Title Intellectual Property Director

This collection of information is required by 37 CFR 1.31, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public, which is to update (and by the USPTO to process) the file of a patent or reexamination proceeding. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.21 and 1.24. This collection is estimated to take 18 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.
If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

STATEMENT UNDER 37 CFR 3.73(c)

Applicant/Patent Owner: ZHEJIANG JINKO SOLAR CO., LTD.

Application No./Patent No.: 17/459,689 Filed/Issue Date: August 27, 2021

Titled: SOLAR CELL, MANUFACTURING METHOD THEREOF, AND PHOTOVOLTAIC MODULE
ZHEJIANG JINKO SOLAR CO., LTD., a corporation

(Name of Assignee)

(Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that, for the patent application/patent identified above, it is (choose **one** of options 1, 2, 3 or 4 below):

1. ☒ The assignee of the entire right, title, and interest.
2. ☐ An assignee of less than the entire right, title, and interest (check applicable box):
- ☐ The extent (by percentage) of its ownership interest is ____%. Additional Statement(s) by the owners holding the balance of the interest must be submitted to account for 100% of the ownership interest.
- ☐ There are unspecified percentages of ownership. The other parties, including inventors, who together own the entire right, title and interest are:

Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

3. ☐ The assignee of an undivided interest in the entirety (a complete assignment from one of the joint inventors was made). The other parties, including inventors, who together own the entire right, title, and interest are:

Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

4. ☐ The recipient, via a court proceeding or the like (e.g., bankruptcy, probate), of an undivided interest in the entirety (a complete transfer of ownership interest was made). The certified document(s) showing the transfer is attached.

The interest identified in option 1, 2 or 3 above (not option 4) is evidenced by either (choose **one** of options A or B below):

- A. ☒ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel 057314, Frame 0980, or for which a copy thereof is attached.

- B. ☐ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

2. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

[Page 1 of 2]

This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

STATEMENT UNDER 37 CFR 3.73(c)

3. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

4. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

5. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

6. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

☐ Additional documents in the chain of title are listed on a supplemental sheet(s).

☒ As required by 37 CFR 3.73(c)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

/Jeffrey L. Costellia, Reg. No. 35,483/

Signature

Jeffrey L. Costellia, Attorney of Record

Printed or Typed Name

October 1, 2021

Date

35,483

Title or Registration Number

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.



UNITED STATES PATENT AND TRADEMARK OFFICE

UNDER SECRETARY OF COMMERCE FOR INTELLECTUAL PROPERTY AND
DIRECTOR OF THE UNITED STATES PATENT AND TRADEMARK OFFICE

AUGUST 30, 2021

PTAS

NIXON PEABODY LLP
799 9TH STREET NW
SUITE 500
WASHINGTON, DC 20001

506841821

UNITED STATES PATENT AND TRADEMARK OFFICE NOTICE OF RECORDATION OF ASSIGNMENT DOCUMENT

THE ENCLOSED DOCUMENT HAS BEEN RECORDED BY THE ASSIGNMENT RECORDATION BRANCH OF THE U.S. PATENT AND TRADEMARK OFFICE. A COMPLETE COPY IS AVAILABLE AT THE ASSIGNMENT SEARCH ROOM ON THE REEL AND FRAME NUMBER REFERENCED BELOW.

PLEASE REVIEW ALL INFORMATION CONTAINED ON THIS NOTICE. THE INFORMATION CONTAINED ON THIS RECORDATION NOTICE REFLECTS THE DATA PRESENT IN THE PATENT AND TRADEMARK ASSIGNMENT SYSTEM. IF YOU SHOULD FIND ANY ERRORS OR HAVE QUESTIONS CONCERNING THIS NOTICE, YOU MAY CONTACT THE ASSIGNMENT RECORDATION BRANCH AT 571-272-3350. PLEASE SEND REQUEST FOR CORRECTION TO: U.S. PATENT AND TRADEMARK OFFICE, MAIL STOP: ASSIGNMENT RECORDATION BRANCH, P.O. BOX 1450, ALEXANDRIA, VA 22313.

RECORDATION DATE: 08/27/2021

REEL/FRAME: 057314/0980
NUMBER OF PAGES: 4

BRIEF: ASSIGNMENT OF ASSIGNORS INTEREST (SEE DOCUMENT FOR DETAILS).

DOCKET NUMBER: 084546-000033

ASSIGNOR:
YU, KUN

DOC DATE: 08/17/2021

ASSIGNOR:
LIU, CHANGMING

DOC DATE: 08/17/2021

ASSIGNOR:
ZHANG, XINYU

DOC DATE: 08/17/2021

ASSIGNEE:
SHANGHAI JINKO GREEN ENERGY
ENTERPRISE MANAGEMENT CO., LTD.
5/F, NO. 277 HUQINGPING ROAD
MINHANG DISTRICT, SHANGHAI, CHINA

ASSIGNEE:
ZHEJIANG JINKO SOLAR CO., LTD.
58, YUANG XI ROAD, YUAN HUA TOWN
HAINING, ZHEJIANG, CHINA

APPLICATION NUMBER: 17459689	FILING DATE:
PATENT NUMBER:	ISSUE DATE:
TITLE: SOLAR CELL, MANUFACTURING METHOD THEREOF, AND PHOTOVOLTAIC MODULE	

ASSIGNMENT RECORDATION BRANCH
PUBLIC RECORDS DIVISION

PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1
 Stylesheet Version v1.2

EPAS ID: PAT6888642

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT
CONVEYING PARTY DATA	
Name	Execution Date
KUN YU	08/17/2021
CHANGMING LIU	08/17/2021
XINYU ZHANG	08/17/2021
RECEIVING PARTY DATA	
Name:	SHANGHAI JINKO GREEN ENERGY ENTERPRISE MANAGEMENT CO., LTD.
Street Address:	5/F, NO. 277 HUQINGPING ROAD
City:	MINHANG DISTRICT, SHANGHAI
State/Country:	CHINA
Name:	ZHEJIANG JINKO SOLAR CO., LTD.
Street Address:	58, YUANG XI ROAD, YUAN HUA TOWN
City:	HAINING, ZHEJIANG
State/Country:	CHINA
PROPERTY NUMBERS Total: 1	
Property Type	Number
Application Number:	17459689
CORRESPONDENCE DATA	
Fax Number:	(202)585-8080
<i>Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.</i>	
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ATTORNEY DOCKET NUMBER:	084546-000033
NAME OF SUBMITTER:	JEFFREY L. COSTELLIA
SIGNATURE:	/Jeffery L. Costellia, Reg. No. 35,483/
DATE SIGNED:	08/27/2021

ASSIGNMENT

WHEREAS, we, YU, Kun of China, Zhejiang Province, LIU, Changming of China, Zhejiang Province, ZHANG, Xinyu of China, Zhejiang Province ("Assignor"), are the inventors of an invention entitled "SOLAR CELL, MANUFACTURING METHOD THEREOF, AND PHOTOVOLTAIC MODULE" that is the subject matter of: (check all that apply)

- [X] a U.S. application for Letters Patent which claims the priority of the Chinese Patent Application No. 202110895225.8 filed on August 4, 2021;
- [] an application made under the Patent Cooperation Treaty which is identifiable at WIPO by Application No. PCT/___ filed on ___;
- [] an application for Letters Patent which is identifiable in the Patent Office of ___ the U.S. by Application No. _____ filed on _____;

WHEREAS, SHANGHAI JINKO GREEN ENERGY ENTERPRISE MANAGEMENT CO., LTD. located 5/F, No.277 Huggingping Road, Minhang District, Shanghai, China and ZHEJIANG JINKO SOLAR CO., LTD. located NO. 58, YUAN XI ROAD, YUAN HUA TOWN, HAINING, ZHEJIANG, CHINA hereinafter referred to as "Assignee", are desirous of acquiring the entire right, title and interest in and to the invention, the applications, and any and all Letters Patent or similar foreign or domestic legal protection;

- [x] in the United States
- [] in all other countries or jurisdictions;

"NOW THEREFORE, for good and valuable consideration, the receipt and adequacy of which is hereby acknowledged,

- a) we agree to transfer, and
- b) we do hereby transfer,

to Assignee, its successors and assigns, effective as of August 4, 2021 *nunc pro tunc*, our entire right, title and interest in the above named countries and jurisdictions in and to the following including the right to sue for past infringement: the invention, the above-identified applications, all applications from which any of the above-identified applications claim priority, corresponding U.S. and non-U.S. applications, any continuation, division, renewal, or substitute for the applications, all Letters Patent, any reissue, re-examination, or similar legal protection issuing related to the Letters Patent, and all rights and benefits under any applicable treaty or convention, and I/we authorize the Director of the United States Patent and Trademark Office or foreign equivalent to issue the Letters Patent or similar legal protection to the Assignee."

We authorize the U.S. Attorneys handling this matter in the U.S. and the Assignee, its successors and assigns, to insert in this instrument the filing date(s) and application numbers when ascertained. We further authorize the Assignee, its successors and assigns, or anyone it may properly designate, to apply for Letters Patent or similar legal protection, in its own name if desired, in the above named countries and jurisdictions and appoint Assignee the common representative in the above-identified international application and any international application for the invention.

We represent to the Assignee, its successors and assigns, that we shall not execute any writing or do any act whatsoever conflicting with this Assignment. We, our executors or administrators, will at any time upon request, without additional consideration, but at the expense of the Assignee, its successors and assigns, execute and deliver to Assignee or its legal representatives such additional writings and do such additional acts as the Assignee, its successors and assigns, may deem desirable to perfect its enjoyment of this grant, and render all assistance in making application for and obtaining, maintaining, and enforcing the Letters Patent or similar legal protection on the invention in any and all countries and jurisdictions, including without limitation providing testimony in any related interference, litigation or proceeding. To the extent that we, our executors or administrators are unable or unavailable to execute and deliver to Assignee or its legal representatives such additional writings and do such additional acts as Assignee, its successors and assigns may deem desirable to perfect its enjoyment of this grant, and render all assistance in making application for and obtaining, maintaining, and enforcing the Letters Patent or similar legal protection on the invention in any and all countries and jurisdictions, we, our executors or administrators hereby authorize Assignee, its successors and assigns to act on our behalf.

01/11/2019

validity of the invention procedure, will not be affected by such holding, and the patent held under enablement in conflict with the law of such procedure will remain in effect for other jurisdictions until held unenforceable to it.

YU, Binyu
YU, Binyu
(Inventor / Assignor)

2021.8.17
Date

LIU, Changmeng
LIU, Changmeng
(Inventor / Assignor)

2021.8.17
Date

ZHANG, Xinyu
ZHANG, Xinyu
(Inventor / Assignor)

2021.8.17
Date

CERTIFICATE OF AVAILABILITY OF A CERTIFIED PATENT DOCUMENT IN A DIGITAL LIBRARY

The International Bureau certifies that a copy of the patent application indicated below has been available to the WIPO Digital Access Service since the date of availability indicated, and that the patent application has been available to the indicated Office(s) as of the date specified following the relevant Office code:

Document details: Country/Office: CN

Filing date: 04 Aug 2021 (04.08.2021)

Application number: 2021108952258

Date of availability of document: 11 Aug 2021 (11.08.2021)

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Date of issue of this certificate: 17 Sep 2021 (17.09.2021)

国家知识产权局

NATIONAL INTELLECTUAL PROPERTY ADMINISTRATION, PRC



证 明

本证明之附件是向本局提交的下列专利申请文件副本。

申 请 号：202110895225.8

申 请 类 型：发明专利

发 明 创 造 名 称：太阳能电池及其制备方法、光伏组件

申 请 日：2021 年 08 月 04 日

申 请 人：上海晶科绿能企业管理有限公司、浙江晶科能源有
限公司

发明人或设计人：于琨、刘长明、张昕宇

局长

申长雨

2021 年 08 月 11 日

20210804

2021108952258

DD212023I

权利要求书

1、一种太阳能电池，其特征在于，所述太阳能电池包括：
半导体衬底，所述半导体衬底的后表面具有第一纹理结构，所述第一纹理结构包括至少部分堆叠的两个或多个第一子结构，对于所述至少部分堆叠的两个或多个第一子结构，在远离所述后表面且垂直于所述后表面的方向上，最外侧第一子结构的顶部表面及其相邻的第一子结构的顶部表面之间的距离小于等于 $2\mu\text{m}$ ，所述最外侧第一子结构的顶部表面的一维尺寸小于等于 $45\mu\text{m}$ ；
位于所述半导体衬底的前表面的第一钝化层；
位于所述半导体衬底的后表面的第一纹理结构上的隧穿氧化层；
位于所述隧穿氧化层表面的掺杂导电层，所述掺杂导电层与所述半导体衬底具有相同导电类型的掺杂元素；以及
位于所述掺杂导电层表面的第二钝化层。

2、根据权利要求1所述的太阳能电池，其特征在于，所述半导体衬底的前表面具有第二纹理结构，所述第二纹理结构包括金字塔状微结构，所述金字塔状微结构包括远离所述半导体衬底前表面的顶部及靠近所述半导体衬底前表面的底部，在远离所述前表面且垂直于所述前表面的方向上，所述金字塔状微结构的顶部与底部的距离小于等于 $5\mu\text{m}$ 。

3、根据权利要求1所述的太阳能电池，其特征在于，对于所述至少部分堆叠的两个或多个第一子结构，在远离所述后表面且垂直于所述后表面的方向上，最外侧第一子结构的顶部表面及其相邻的第一子结构的顶部表面的距离在 $0.3\mu\text{m}\sim 1.2\mu\text{m}$ 内。

4、根据权利要求1所述的太阳能电池，其特征在于，所述最外侧第一子结构的顶部表面的平均一维尺寸在 $10\mu\text{m}\sim 15\mu\text{m}$ 内。

5、根据权利要求1所述的太阳能电池，其特征在于，所述最外侧第一子结构的顶部表面上的隧穿氧化层厚度小于所述最外侧第一子结构侧面表面上的隧穿氧化层厚度。

6、根据权利要求1所述的太阳能电池，其特征在于，所述最外侧第一子结构的顶部表面上的隧穿氧化层与所述最外侧第一子结构的侧面表面上的隧穿氧化层之间的厚度差小于等于 0.15nm 。

7、根据权利要求1所述的太阳能电池，其特征在于，所述第一纹理

结构还包括邻接非堆叠排布的两个或多个第二子结构，远离所述后表面的所述第二子结构的顶部表面的一维尺寸小于等于 $45\text{ }\mu\text{m}$ 。

8、根据权利要求 7 所述的太阳能电池，其特征在于，所述第一子结构和/或所述第二子结构的顶部表面为多边形平面。

9、根据权利要求 8 所述的太阳能电池，其特征在于，所述多边形平面的形状包括菱形、方形、梯形、近似菱形、近似方形、近似梯形中的至少一种。

10、根据权利要求 1 所述的太阳能电池，其特征在于，所述隧穿氧化层包括氧化硅层、氧化铝层、氮氧化硅层、氧化钼层及氧化镱层中的至少一种，所述隧穿氧化层的厚度为 $0.8\text{nm}\sim 2\text{nm}$ 。

11、根据权利要求 1 所述的太阳能电池，其特征在于，第二钝化层包括氮化硅层、氧化硅层、氮氧化硅层中的至少一种，所述第二钝化层的厚度为 $70\text{nm}\sim 120\text{nm}$ 。

12、根据权利要求 1 所述的太阳能电池，其特征在于，所述第一钝化层包括氧化硅层、氮化硅层、氧化铝层、氮氧化硅层中的至少一种。

13、根据权利要求 1~12 中任意一项所述的太阳能电池，其特征在于，所述半导体衬底为 N 型单晶硅衬底，所述掺杂导电层为 N 型掺杂多晶硅层、N 型掺杂微晶硅层或 N 型掺杂非晶硅层，所述掺杂导电层的厚度为 $60\text{nm}\sim 200\text{nm}$ 。

14、一种光伏组件，其特征在于，所述光伏组件包括多个太阳能电池串，所述太阳能电池串包括权利要求 1~13 任一项所述的太阳能电池。

15、一种太阳能电池的制备方法，其特征在于，包括以下步骤：

对半导体衬底进行制绒处理，所述半导体衬底的前表面形成第二纹理结构，所述第二纹理结构包括金字塔状微结构；

对制绒后的半导体衬底的前表面进行掺杂处理，形成掺杂层；

采用碱溶液对半导体衬底的后表面进行抛光处理，使得在所述半导体衬底后表面形成第一纹理结构，其中，所述第一纹理结构包括至少部分堆叠的两个或多个第一子结构，其中，对于所述至少部分堆叠的两个或多个第一子结构，在远离所述后表面且垂直于所述后表面的方向上，最外侧第一子结构的顶部表面及与其相邻的第一子结构的顶部表面的距离小于等于 $2\text{ }\mu\text{m}$ ，所述最外侧第一子结构的顶部表面的一维尺寸小于等于 $45\text{ }\mu\text{m}$ ；

在所述半导体衬底的后表面的第一纹理结构上形成隧穿氧化层；

在所述隧穿氧化层表面沉积形成多晶硅层，并对所述多晶硅层进行掺杂处理，形成掺杂导电层，所述掺杂导电层与所述半导体衬底具有相同导电类型的掺杂元素；

在所述半导体衬底的前表面形成第一钝化层；以及
在所述掺杂导电层表面形成第二钝化层。

16、根据权利要求 15 所述的制备方法，其特征在于，所述采用碱溶液对半导体衬底的后表面进行抛光处理，包括：

采用质量分数为 5%~15%碱溶液清洗所述半导体衬底的后表面，去除多孔硅；

采用喷淋方式将所述碱溶液的微液滴滴至所述半导体衬底的后表面进行粗糙化处理，再用质量分数为 5%~10%的氢氟酸进行预清洗；

采用抛光液对所述半导体衬底的后表面进行抛光，抛光温度为 70℃~80℃，抛光时间<260s，其中，所述抛光液包括质量分数为 1%~15%的 NaOH、质量分数为 1%~15%的 KOH 及质量分数为 0.5%~2.5%的添加剂；

采用质量分数为 5%~15%的氢氧化钾与质量分数为 15%~40%的双氧水的混合液对所述抛光液中的有机成分进行去除；

对抛光后的半导体衬底进行水洗、烘干处理。

17、根据权利要求 15 所述的制备方法，其特征在于，所述形成隧穿氧化层的步骤满足以下特征中的至少一种：

(1) 采用变温式工艺以及化学气相沉积法在所述半导体衬底的后表面的第一纹理结构上沉积形成所述隧穿氧化层；

(2) 在沉积形成所述隧穿氧化层过程中，控制升温速率为 0.5℃/min~3℃/min，沉积温度为 560℃~620℃，沉积时间为 3min~10min；

(3) 所述隧穿氧化层的沉积温度低于所述多晶硅层的沉积温度；

(4) 所述隧穿氧化层包括氧化硅层、氧化铝层、氮氧化硅层、氧化钼层及氧化钨层中的至少一种；

(5) 所述隧穿氧化层的厚度为 0.8nm~2nm。

说明书

太阳能电池及其制备方法、光伏组件

技术领域

本申请涉及光伏电池技术领域，具体地讲，涉及太阳能电池及其制备方法、光伏组件。

背景技术

N 型 TOPCon (Tunnel Oxide Passivated Contact, 隧穿氧化层钝化接触) 电池依靠“隧穿效应”实现后表面钝化接触。在制备 TOPCon 电池时，在硅片表面硼扩散后会形成硼硅玻璃，其清洗去除难度较常规 PERC 电池的磷硅玻璃更难；一般 N 型电池后表面的硼硅玻璃采用具有氧化性的混合酸溶液进行去除；表面清洗干净干燥后，进行槽式或者链式的酸性添加剂辅助后表面抛光。抛光之后的硅片后表面具有平整的结构，但抛光之后的后表面结构将会直接影响隧穿氧化层以及多晶硅层的制备，进而影响电池的钝化性能和电池的转化效率。

发明内容

鉴于此，本申请提出一种太阳能电池及其制备方法、光伏组件，通过电池衬底表面纹理结构的匹配，能够提高太阳能电池的开路电压，降低金属电极接触电阻，提升电池转化效率。

第一方面，本申请提供一种太阳能电池，所述太阳能电池包括：

半导体衬底，所述半导体衬底的后表面具有第一纹理结构，所述第一纹理结构包括至少部分堆叠的两个或多个第一子结构，对于所述至少部分堆叠的两个或多个第一子结构，在远离所述后表面且垂直于所述后表面的方向上，最外侧第一子结构的顶部表面及与其相邻的第一子结构的顶部表面的距离小于等于 $2\mu\text{m}$ ，所述最外侧第一子结构的顶部表面的一维尺寸小于等于 $45\mu\text{m}$ ；

位于所述半导体衬底的前表面的第一钝化层；

位于所述半导体衬底的后表面的第一纹理结构上的隧穿氧化层；

位于所述隧穿氧化层表面的掺杂导电层，所述掺杂导电层与所述半导体衬底具有相同导电类型的掺杂元素；以及

位于所述掺杂导电层表面的第二钝化层。

在一种可行的实施方式中，所述半导体衬底的前表面具有第二纹理结构，所述第二纹理结构包括金字塔状微结构，所述金字塔状微结构包括远离所述半导体衬底前表面的顶部及靠近所述半导体衬底前表面的底部，在远离所述前表面且垂直于所述前表面的方向上，所述金字塔状微结构的顶部与底部的距离小于等于 $5\mu\text{m}$ 。

在一种可行的实施方式中，对于所述至少部分堆叠的两个或多个第一子结构，在远离所述后表面且垂直于所述后表面的方向上，最外侧第一子结构的顶部表面及与其相邻的第一子结构的顶部表面的距离在 $0.3\mu\text{m}\sim 1.2\mu\text{m}$ 内。

在一种可行的实施方式中，所述最外侧第一子结构的顶部表面的平均一维尺寸在 $10\mu\text{m}\sim 15\mu\text{m}$ 内。

在一种可行的实施方式中，所述最外侧第一子结构的顶部表面上的隧穿氧化层厚度小于所述最外侧第一子结构侧部表面上的隧穿氧化层厚度。

在一种可行的实施方式中，所述最外侧第一子结构的顶部表面上的隧穿氧化层与所述最外侧第一子结构的侧部表面上的隧穿氧化层之间的厚度差小于等于 0.15nm 。

在一种可行的实施方式中，所述第一纹理结构还包括邻接非堆叠排布的两个或多个第二子结构，远离所述后表面的所述第二子结构的顶部表面的一维尺寸小于等于 $45\mu\text{m}$ 。

在一种可行的实施方式中，所述第一子结构和/或所述第二子结构的顶部表面为多边形平面。

在一种可行的实施方式中，所述多边形平面的形状包括菱形、方形、梯形、近似菱形、近似方形、近似梯形中的至少一种。

在一种可行的实施方式中，所述隧穿氧化层包括氧化硅层、氧化铝层、氮氧化硅层、氧化钼层及氧化钨层中的至少一种，所述隧穿氧化层的厚度为 $0.8\text{nm}\sim 2\text{nm}$ 。

在一种可行的实施方式中，第二钝化层包括氮化硅层、氧化硅层、氮氧化硅层中的至少一种，所述第二钝化层的厚度为 $70\text{nm}\sim 120\text{nm}$ 。

在一种可行的实施方式中，所述第一钝化层包括氧化硅层、氮化硅层、氧化铝层、氮氧化硅层中的至少一种。

在一种可行的实施方式中，所述半导体衬底为 N 型单晶硅衬底，所述



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掺杂导电层为 N 型掺杂多晶硅层、N 型掺杂微晶硅层或 N 型掺杂非晶硅层，所述掺杂导电层的厚度为 60nm-200nm。

第二方面，本申请提供一种光伏组件，所述光伏组件包括多个太阳能电池串，所述太阳能电池串包括上述第一方面所述的太阳能电池。

第三方面，本申请提供一种太阳能电池的制备方法，包括以下步骤：

对半导体衬底进行制绒处理，所述半导体衬底的前表面形成第二纹理结构，所述第二纹理结构包括金字塔状微结构；

对制绒后的半导体衬底的前表面进行掺杂处理，形成掺杂层；

采用碱溶液对半导体衬底的后表面进行抛光处理，使得在所述半导体衬底后表面形成第一纹理结构，其中，所述第一纹理结构包括至少部分堆叠的两个或多个第一子结构，其中，对于所述至少部分堆叠的两个或多个第一子结构，在远离所述后表面且垂直于所述后表面的方向上，最外侧第一子结构的顶部表面及与其相邻的第一子结构的顶部表面的距离小于等于 $2\mu\text{m}$ ，所述最外侧第一子结构的顶部表面的一维尺寸小于等于 $45\mu\text{m}$ ；

在所述半导体衬底的后表面的第一纹理结构上形成隧穿氧化层；

在所述隧穿氧化层表面沉积形成多晶硅层，并对所述多晶硅层进行掺杂处理，形成掺杂导电层，所述掺杂导电层与所述半导体衬底具有相同导电类型的掺杂元素；

在所述半导体衬底的前表面形成第一钝化层；以及

在所述掺杂导电层表面形成第二钝化层。

在一种可行的实施方式中，所述采用碱溶液对半导体衬底的后表面进行抛光处理，包括：

采用质量分数为 5%~15%碱溶液清洗所述半导体衬底的后表面，去除多孔硅；

采用喷淋方式将所述碱溶液的微液滴滴至所述半导体衬底的后表面进行粗糙化处理，再用质量分数为 5%~10%的氢氟酸进行预清洗；

采用抛光液对所述半导体衬底的后表面进行抛光，抛光温度为 70°C ~ 80°C ，抛光时间 $<260\text{s}$ ，其中，所述抛光液包括质量分数为 1%~15%的 NaOH、质量分数为 1%~15%的 KOH 及质量分数为 0.5%~2.5%的添加剂；

采用质量分数为 5%~15%的氢氧化钾与质量分数为 15%~40%的双氧水的混合液对所述抛光液中的有机成分进行去除；

对抛光后的半导体衬底进行水洗、烘干处理。

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在一种可行的实施方式中，所述形成隧穿氧化层的步骤满足以下特征中的至少一种：

(1) 采用变温式工艺以及化学气相沉积法在所述半导体衬底的后表面的第一纹理结构上沉积形成所述隧穿氧化层；

(2) 在沉积形成所述隧穿氧化层过程中，控制升温速率为 $0.5^{\circ}\text{C}/\text{min}\sim 3^{\circ}\text{C}/\text{min}$ ，沉积温度为 $560^{\circ}\text{C}\sim 620^{\circ}\text{C}$ ，沉积时间为 $3\text{min}\sim 10\text{min}$ ；

(3) 所述隧穿氧化层的沉积温度低于所述多晶硅层的沉积温度；

(4) 所述隧穿氧化层包括氧化硅层、氧化铝层、氮氧化硅层、氧化钼层及氧化钨层中的至少一种；

(5) 所述隧穿氧化层的厚度为 $0.8\text{nm}\sim 2\text{nm}$ 。

本申请的技术方案至少具有以下有益的效果：

通过将半导体衬底后表面的第一纹理结构中的子结构的距离控制在理想范围内，可以保障半导体衬底后表面的粗糙度在合适的范围，有利于提高形成于第一纹理结构上的隧穿氧化层的均匀性，形成的隧穿氧化层性能更好，并进一步抑制掺杂导电层的局部掺杂浓度偏高，降低接触电阻率，提高太阳能电池的开路电压，提升填充因子及光电转换效率。

附图说明

为了更清楚的说明本申请实施例或现有技术的技术方案，下面将对实施例或现有技术描述中所需要使用的附图作简单的介绍，显而易见地，下面描述中的附图仅仅是本申请的一些实施例，对于本领域普通技术人员来讲，在不付出创造性劳动的前提下，还可以根据这些附图获得其他的附图。

图1为本申请实施例提供的太阳能电池制备方法的结构示意图。

图2为本申请实施例提供的太阳能电池的半导体衬底前表面的第二纹理结构的电镜示意图。

图3为本申请实施例提供的太阳能电池的半导体衬底后表面的第一纹理结构的电镜示意图。

图4a为本申请实施例提供的太阳能电池的半导体衬底后表面的第一纹理结构中第一子结构的结构示意图。

图4b为本申请实施例提供的太阳能电池的半导体衬底后表面的第一纹理结构中另一种第一子结构的结构示意图。

图 5 为本申请实施例提供的太阳能电池的半导体衬底后表面的第一纹理结构中子结构的结构示意图。

图 6 为本申请实施例提供的太阳能电池的半导体衬底后表面的第一纹理结构上的隧穿氧化层的结构示意图。

图 7a 为本申请实施例提供的光伏组件的结构示意图。

图 7b 为本申请实施例提供的光伏组件的俯视图。

图 8 为本申请实施例提供的太阳能电池的制备方法的流程示意图。

具体实施方式

为了更好的理解本申请的技术方案，下面结合附图对本申请实施例进行详细描述。

应当明确，所描述的实施例仅仅是本申请一部分实施例，而不是全部的实施例。基于本申请中的实施例，本领域普通技术人员在没有作出创造性劳动前提下所获得的所有其它实施例，都属于本申请保护的范围。

在本申请实施例中使用的术语是仅仅出于描述特定实施例的目的，而非旨在限制本申请。在本申请实施例和所附权利要求书中所使用的单数形式的“一种”、“所述”和“该”也旨在包括多数形式，除非上下文清楚地表示其它含义。

应当理解，本文中使用的术语“和/或”仅仅是一种描述关联对象的相关关系，表示可以存在三种关系，例如，A 和/或 B，可以表示：单独存在 A，同时存在 A 和 B，单独存在 B 这三种情况。另外，本文中字符“/”，一般表示前后关联对象是一种“或”的关系。

TOPCon 电池依靠“隧穿效应”实现后表面钝化，现有的 TOPCon 电池后表面结构从内向外依次为半导体衬底，隧穿氧化层，掺杂导电层，后表面钝化层。N 型 TOPCon(接触钝化电池)在硼扩散形成 BSG 硼硅玻璃，硼硅玻璃清洗去除难度相比于磷硅玻璃更难；一般采用具有氧化性的混合酸溶液进行去除；表面清洗干净干燥后，进行后表面抛光。目前，半导体衬底后表面的抛光后的状态对纳米级厚度超薄隧穿氧化层有一定影响，容易造成隧穿氧化层与半导体衬底之间的接触电阻率提高，进行容易导致太阳能电池的填充因子的波动，影响电池的光电转换效率。

基于此，第一方面，本申请提供一种太阳能电池，如图 1 所示，太阳能电池包括：

半导体衬底 10，半导体衬底 10 的后表面具有第一纹理结构 12，第一纹理结构 12 包括至少部分堆叠的两个或多个第一子结构，其中，对于所述至少部分堆叠的两个或多个第一子结构，在远离所述后表面且垂直于所述后表面的方向上，最外侧第一子结构的顶部表面及与其相邻的第一子结构的顶部表面的距离小于等于 $2\mu\text{m}$ ，所述最外侧第一子结构的顶部表面的一维尺寸小于等于 $45\mu\text{m}$ ；半导体衬底 10 的前表面具有第二纹理结构 11，第二纹理结构 11 可以包括金字塔状微结构；

位于半导体衬底 10 的前表面的第一钝化层 20；

位于半导体衬底 10 的后表面的第一纹理结构上的隧穿氧化层 30；

位于隧穿氧化层 30 表面的掺杂导电层 40，所述掺杂导电层与所述半导体衬底具有相同导电类型的掺杂元素；

以及位于掺杂导电层 40 表面的第二钝化层 50。

半导体衬底 10 的前表面可以指受光面，即接收太阳光线照射的表面（受光面），半导体衬底 10 的后表面是指与所述前表面相对的表面。在一些实施例中，所述形成的太阳能电池为单面电池，所述前表面可以是指受光面，后表面可以是指背光面。在一些实施例中，所述形成的太阳能电池为双面电池，所述前表面和后表面均可以是受光面。

作为本申请可选的技术方案，半导体衬底 10 为 N 型晶体硅衬底（或硅片），可以采用高温扩散、浆料掺杂或者离子注入中的任意一种或多种工艺，在半导体衬底的前表面形成 P 型掺杂层，以便在所述半导体衬底 10 中形成 PN 结。在一些实施例中，所述半导体衬底 10 可以为单晶硅衬底、多晶硅衬底、微晶硅衬底或碳化硅衬底中的一种。

在一些实施例中，所述 P 型掺杂层为掺硼扩散层。掺硼扩散层是利用硼源通过扩散工艺使硼原子扩散到前表面一定深度而形成的 P 型掺杂层（即，P⁺层）。例如，硼源可以是液态三溴化硼。

在一些实施例中，如图 2 所示，半导体衬底 10 的前表面具有第二纹理结构 11，第二纹理结构 11 包括金字塔状微结构 111。金字塔状微结构 111 可以是四面体、近似四面体、五面体、近似五面体等结构。金字塔状微结构 111 可以通过对半导体衬底进行制绒工艺来形成。制绒工艺的方式可以是化学刻蚀、激光刻蚀、机械法、等离子刻蚀等。所述金字塔状微结构使在丝网印刷金属浆料形成电极时可以更好地填充于所述微结构中，获

得更优异的电极接触，能够有效降低电池串联电阻，提高填充因子。

在一些实施例中，所述金字塔状微结构 111 包括远离半导体衬底前表面的顶部及靠近半导体衬底前表面的底部，在远离前表面且垂直于所述前表面的方向上，所述金字塔状微结构的顶部与底部的距离（或高度）小于等于 $5\mu\text{m}$ ，优选地，所述距离的范围为 $2\mu\text{m}$ - $5\mu\text{m}$ 。具体可以是 $2\mu\text{m}$ 、 $2.5\mu\text{m}$ 、 $2.8\mu\text{m}$ 、 $3\mu\text{m}$ 、 $3.5\mu\text{m}$ 、 $3.8\mu\text{m}$ 、 $4\mu\text{m}$ 、 $4.2\mu\text{m}$ 、 $4.5\mu\text{m}$ 、 $4.8\mu\text{m}$ 或 $5\mu\text{m}$ 等。当金字塔状微结构 111 的距离范围控制在 $5\mu\text{m}$ 以内，比如， $2\mu\text{m}$ - $5\mu\text{m}$ ，所述金字塔状微结构 111 具有低反射、低复合、易填充的特性，使得电池的光电转换效率得以提升。

可以理解的是，由于前表面硅晶体的晶向的各向异性，在前表面形成的金字塔状微结构数量不可能穷尽，这里所指的金字塔状微结构 111 的距离可以是在特定区域内随机选取的金字塔状微结构 111 的凸出的顶部最高点与凹陷的最低点之间的距离。例如，金字塔状微结构 111 的距离可以通过使用原子力显微镜 (AFM) 测定半导体衬底的表面形状来确定。例如，在前表面选取 $40\mu\text{m}\times 40\mu\text{m}$ 左右的扫描范围，通过原子力显微镜在选取的范围内扫描半导体衬底的前表面，测定前表面的金字塔微结构的形貌尺寸，计算得到高度值 h 。具体地，从测得的形貌尺寸中 (AFM 图像) 选择金字塔状微结构的凸出的顶部最高点 h_a ，与顶部对应的底部的最低点为 h_b ，得到 $h=h_a-h_b$ 。在其他实施方式中，随机采集第二纹理结构中的多个金字塔状微结构的高度，并计算平均值，将平均值定义为金字塔状微结构的高度。例如，随机选取 4 个金字塔状微结构 111，其高度分别为 h_1 、 h_2 、 h_3 及 h_4 ，那么金字塔状微结构 111 的高度值为 $(h_1+h_2+h_3+h_4)/4$ 。也就是说，多个金字塔状微结构 111 的平均距离可以视为前表面的金字塔状微结构的距离，用来表征前表面的纹理特征。

作为本申请可选的技术方案，第一钝化层 20 包括氧化硅层、氮化硅层、氧化铝层、氮氧化硅层中的至少一种或多种的层叠结构。

在一些实施例中，所述第一钝化层 20 的厚度范围为 10nm - 120nm ，具体可以是 10nm 、 20nm 、 30nm 、 40nm 、 50nm 、 60nm 、 70nm 、 80nm 、 90nm 、 100nm 或 120nm 等，当然也可以是上述范围内的其他值，在此不做限定。

可选地，所述第一钝化层 20 为氧化铝层和氮化硅层的叠层钝化结构。所述氧化铝层设置在半导体衬底 10 前表面上，所述氮化硅层设置在氧化

铝层表面上。在一些实施例中，氧化铝层的厚度为 2nm~10nm，氧化铝层的折射率为 1.5-1.8；所述氮化硅层的厚度为 50nm-110nm，氮化硅层的折射率为 1.65-2.25。所述第一钝化层 20 的整体折射率为 1.9-2.0。在一些实施例中，所述氧化铝层或氮化硅层可以包括多个子层，例如氮化硅层由 2~5 个氮化硅子层组成。

可选地，所述第一钝化层为依次层叠设置的氧化铝层、氮化硅层和氮氧化硅的叠层钝化结构，其中，氧化铝层的厚度范围为 2nm~10nm，氧化铝层的折射率范围为 1.5-1.8，所述氮化硅层的厚度范围为 40nm-80nm，氮化硅层的折射率范围为 1.9-2.3，氮氧化硅层的厚度范围为 10nm-60nm，氮氧化硅层的折射率范围为 1.5-1.75。

进一步地，半导体衬底 10 的后表面具有第一纹理结构 12。具体地，第一纹理结构 12 可以经过碱抛光处理形成。

作为本申请可选的技术方案，图 3 为本申请实施例提供的半导体衬底的后表面的第一纹理结构 12 的电镜示意图，如图 3 所示，第一纹理结构 12 包括至少部分堆叠的两个或多个第一子结构 121。所述第一纹理结构 12 呈现出非金字塔状微结构形貌。例如，所述第一纹理结构可以呈现出近似“台阶”状的形貌，第一子结构 121 可以被视为“台阶”的阶梯。

图 4a 为示例的部分堆叠的三层第一子结构的示意图，图 4b 为示例的部分堆叠的两层第一子结构的示意图。

对于所述至少部分堆叠的两个或多个第一子结构 121，在远离所述后表面且垂直于所述后表面的方向上（也可以理解为在堆叠方向上），最外侧第一子结构的顶部表面 121a 及与其相邻的第一子结构的顶部表面 121b 的距离 H 小于等于 $2\mu\text{m}$ ，具体可以是 $2\mu\text{m}$ 、 $1.8\mu\text{m}$ 、 $1.5\mu\text{m}$ 、 $1.2\mu\text{m}$ 、 $1.1\mu\text{m}$ 、 $1.0\mu\text{m}$ 、 $0.8\mu\text{m}$ 、 $0.5\mu\text{m}$ 、 $0.3\mu\text{m}$ 、 $0.2\mu\text{m}$ 或 $0.1\mu\text{m}$ 等。当距离 H 超过 $2\mu\text{m}$ ，第一纹理结构的粗糙度过大，形成于第一纹理结构上的隧穿氧化层 30 的厚度越大，则不利于形成高致密度和高均匀性的隧穿氧化层，进而影响隧穿氧化层 30 的隧穿和钝化效果；第一纹理结构的粗糙度过小，形成于第一纹理结构上的隧穿氧化层的厚度越小，则不利于与电极浆料的接触。优选地，在远离所述后表面且垂直于所述后表面的方向上，最外侧第一子结构的顶部表面 121a 及与其相邻的第一子结构的顶部表面 121b 的距离 H 在 $0.3\mu\text{m}$ ~ $1.2\mu\text{m}$ 内。

需要说明的是，当层叠设置的三层第一子结构时，任意一层第一子结构的顶部表面 121a 与相邻一层的第一子结构的顶部表面 121b 的距离 H 小于等于 $2\mu\text{m}$ 。

可以理解地，控制最外侧第一子结构的顶部表面 121a 及与其相邻的第一子结构的顶部表面 121b 的距离小于等于 $2\mu\text{m}$ ，可以使得第一纹理结构的粗糙度控制在所需范围内，有利于提高形成于第一纹理结构上的隧穿氧化层的均匀性，形成的隧穿氧化层性能更好，并进一步抑制磷扩散导致的局部磷浓度偏高，降低接触电阻率，提高太阳能电池的开路电压，提升填充因子及光电转换效率。

所述最外侧第一子结构的顶部表面 121a 的一维尺寸 L 小于等于 $45\mu\text{m}$ ，即， $0 < L \leq 45\mu\text{m}$ ，可选地，所述一维尺寸 L 在 $2\mu\text{m} \sim 45\mu\text{m}$ 内。这里，所述顶部表面的一维尺寸 L 具体可以是表面的长、宽、对角线长度、圆形的直径等，在此不做限定。在一些实施例中，所述一维尺寸可以是指衬底后表面的预设范围区域内，多个最外侧第一子结构的顶部表面的一维尺寸的平均值。最外侧第一子结构的顶部表面的平均一维尺寸具体可以是 $2\mu\text{m}$ 、 $5\mu\text{m}$ 、 $8\mu\text{m}$ 、 $12\mu\text{m}$ 、 $15\mu\text{m}$ 、 $18\mu\text{m}$ 、 $20\mu\text{m}$ 、 $25\mu\text{m}$ 、 $28\mu\text{m}$ 、 $30\mu\text{m}$ 、 $35\mu\text{m}$ 、 $40\mu\text{m}$ 、 $42\mu\text{m}$ 、 $40\mu\text{m}$ 或 $45\mu\text{m}$ 等。优选地，最外侧第一子结构的顶部表面的平均一维尺寸在 $10\mu\text{m} \sim 15\mu\text{m}$ 内。

在具体实施例中，如图 3 所示，所述第一纹理结构还包括邻接非堆叠排布的两个或多个第二子结构 122，远离所述后表面的所述第二子结构 122 的顶部表面的一维尺寸 L 小于等于 $45\mu\text{m}$ ，即， $0 < L \leq 45\mu\text{m}$ 。可选地，所述第二子结构 122 的一维尺寸 L 在 $2\mu\text{m} \sim 45\mu\text{m}$ 内，具体可以是 $2\mu\text{m}$ 、 $5\mu\text{m}$ 、 $8\mu\text{m}$ 、 $12\mu\text{m}$ 、 $15\mu\text{m}$ 、 $18\mu\text{m}$ 、 $20\mu\text{m}$ 、 $25\mu\text{m}$ 、 $28\mu\text{m}$ 、 $30\mu\text{m}$ 、 $32\mu\text{m}$ 、 $35\mu\text{m}$ 或 $45\mu\text{m}$ 等。

区别于前表面的金字塔状微结构，后表面的所述第一子结构和/或所述第二子结构的顶部表面为多边形平面，所述多边形平面的形状包括菱形、方形、梯形、近似菱形、近似方形、近似梯形中的至少一种。可以理解的是，在实际的制造过程中，所述第一子结构或第二子结构的顶部表面形貌呈现不规则的多边形平面，但总体呈现出近似于菱形、方形、梯形的形貌特征。

在一些实例中，由于后续钝化膜层的制备，比如第一钝化层 20、隧穿

氧化层 30、掺杂导电层 40 等，可能会对第二纹理结构和第一纹理结构的初始结构产生一定的破坏，例如，在量产的太阳能电池中，所述第二纹理结构中可能还包括少量的非金字塔状的微结构，所述非金字塔状的微结构是由于金字塔状微结构的塔尖被破坏而形成。

在一些实例中，在测量表征所述太阳能电池的第二纹理结构或第一纹理结构的纹理尺寸特征时，比如第一子结构顶部表面的一维尺寸、相邻第一子结构的表面之间的距离，可以通过测试仪器（光学显微镜、原子力显微镜、扫描电子显微镜、透射电子显微镜等）直接测量膜层表面标定。在一种情况下，由于膜层厚度为纳米级别，可以直接利用对应于第二纹理结构或第一纹理结构的膜层测量数据获得，所述膜层测量数据为膜层厚度和纹理尺寸的总和。在另一种情况下，也可以利用前述膜层测量数据减去膜层厚度数据获得。以上测量手段仅作参考，本申请对此不加以限定。

如图 1 及图 6 所示，位于半导体衬底 10 的后表面的第一纹理结构 12 上的隧穿氧化层 30，隧穿氧化层 30 可以是氧化硅层、氧化铝层、氮氧化硅层、氧化钼层、氧化钨层中的一种或多种层叠结构。在其他实施例中，隧穿氧化层 30 也可以是含氧氮化硅层、含氧碳化硅层等。隧穿氧化层 30 的厚度为 0.8nm~2nm。具体地，隧穿氧化层 30 的厚度为 0.8nm、0.9nm、1.0nm、1.2nm、1.4nm、1.6nm、1.8nm 或 2nm 等。隧穿氧化层 30 的厚度是指隧穿氧化层相对于形成面上的厚度。在第一纹理结构上形成的隧穿氧化层 30 的厚度可以通过将子结构的斜面的法线方向作为厚度方向，进行截面观察并计算得到。隧穿氧化层 30 的厚度过大，不利于降低隧穿氧化层的接触电阻。通过控制隧穿氧化层的厚度，可以抑制接触电阻引起的填充因子的降低。

具体地，隧穿氧化层 30 的带隙宽度 $>3.0\text{eV}$ ，载流子通过热发射一般难以传输通过隧穿氧化层 30，但是由于隧穿氧化层 30 很薄，载流子可以通过隧穿效应穿过隧穿氧化层 30，因此厚度在 0.8nm~2nm 内的隧穿氧化层对多数载流子的传输没有阻碍。随着隧穿氧化层的厚度逐渐增大时，多数载流子的隧穿效应受到影响，载流子难以传输通过隧穿氧化层 30，电池的光电转换效率会逐渐下降。隧穿氧化层的厚度过小时，无法起到钝化作用。优选地，隧穿氧化层 30 为氧化硅层，隧穿氧化层 30 的厚度为 0.8nm~1.5nm。

作为本申请可选的技术方案，如图 6 所示，所述最外侧第一子结构的

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顶部表面上的隧穿氧化层厚度 D1 小于所述最外侧第一子结构侧部表面上形成的隧穿氧化层厚度 D2。具体地，所述最外侧第一子结构的顶部表面上的隧穿氧化层与所述最外侧子结构的侧部表面上形成的隧穿氧化层之间的厚度差(D2-D1)小于等于 0.15nm。厚度差具体可以是 0.14nm、0.13nm、0.12nm、0.11nm、0.10nm、0.09nm、0.08nm、0.07nm、0.06nm、0.05nm、0.04nm 等。当最外侧第一子结构的顶部表面上的隧穿氧化层与最外侧子结构的侧部表面上形成的隧穿氧化层过大时，隧穿氧化层的厚度均匀性差，太阳能电池的电流密度容易受影响，太阳能电池的开压电路下降。

在一些实施例中，通过在半导体衬底前后表面设置不同形貌的纹理结构，在前表面形成金字塔状纹理结构以及在后表面形成非金字塔纹理结构，可以使得形成的电池具有不同层次的陷光结构，增加光的有效接触面积，而且，对于形成在后表面的第一纹理结构，使得将最外侧第一子结构的顶部表面及与其相邻的第一子结构的顶部表面的距离控制在 $2\mu\text{m}$ 以内，有利于减少隧穿氧化层中的孔洞密度 (pinhole) 进而提升隧穿氧化层的致密度和均匀性，并进一步抑制隧穿氧化层表面的掺杂导电层的局部掺杂浓度偏高，降低接触电阻率，提高太阳能电池的开路电压，提升填充因子及光电转换效率。

在一些实施例中，掺杂导电层 40 可以是掺杂多晶硅层、掺杂微晶硅层、掺杂非晶硅层，所述掺杂导电层 40 与所述半导体衬底具有相同导电类型的掺杂元素。

当半导体衬底 10 为 N 型单晶硅衬底，掺杂导电层 40 为 N 型掺杂多晶硅层、N 型掺杂微晶硅层或 N 型掺杂非晶硅层，掺杂元素可以是磷等 N 型掺杂元素。

在一些实施例中，所述掺杂导电层 40 的厚度范围为 60nm-200nm，例如，N 型掺杂多晶硅层，所述掺杂导电层 40 的折射率范围为 3.5-4.5。

作为本申请可选的技术方案，第二钝化层 50 包括氮化硅层、氧化硅层、氮氧化硅层中的至少一种。所述第二钝化层 50 的厚度为 70nm-120nm。例如，所述第二钝化层 50 为氮化硅层，所述氮化硅层具有低硅氮比，氮化硅层的折射率范围为 1.7~2.1，氮化硅层的折射率可以为 1.7、1.8、1.9、2.0 或 2.1 等，当然也可以是上述范围内的其他值，在此不做限定。通过控制氮化硅层的折射率，使得其具有低硅氮比，形成的第二钝化层 50 在金属化处理时能够降低接触电阻率，从而进一步降低太阳能电池的接触电阻

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率。

在一些实施例中，当第二钝化层 50 为层叠设置的氮化硅层与氧化硅层或层叠设置的氮化硅层与氮氧化硅层时，氮化硅层位于掺杂导电层的表面，氧化硅层或氮氧化硅层位于氮化硅层的表面。

进一步地，太阳能电池还包括第一电极 60 与第二电极 70，第一电极 60 穿过第一钝化层 20 与半导体衬底 10 的前表面的 P 型掺杂层（例如，掺硼扩散层）形成欧姆接触，第二电极 70 穿过第二钝化层 50 与掺杂导电层 40 形成欧姆接触，掺杂导电层 40 与隧穿氧化层 30 组成钝化接触结构。所述第一电极 60 以及第二电极 70 可以通过涂敷在第一钝化层以及第二钝化层表面的金属导电浆料烧结形成。在一些实施例中，所述第一电极 60 或第二电极 70 的材料包括银、铝、铜、镍等金属材料。

对于如图 1 所示形成的太阳能电池，即，在半导体衬底 10 的前表面形成金字塔状微结构的第二纹理结构，在半导体衬底的后表面形成非金字塔状的微结构的第一纹理结构，在所述第二纹理结构上形成匹配的第一钝化层 20（例如，氧化铝层和氮化硅层的叠层钝化结构），在所述第一纹理结构上形成匹配的隧穿氧化层 30、掺杂导电层 40 以及第二钝化层 50（例如，氮化硅层），所述太阳能电池结构具有较高的光电转化效率。

第二方面，本申请实施例提供了一种光伏组件，所述光伏组件包括多个太阳能电池串。

如图 7a 及图 7b 所示，光伏组件包括第一盖板 1、第一封装胶层 2、太阳能电池串 3、第二封装胶层 4 和第二盖板 5。

其中，太阳能电池串 3 包括多个太阳能电池（如图 1 所述的太阳能电池），太阳能电池之间通过导电带（图未示）连接。太阳能电池之间的连接方式可以是部分层叠，也可以是拼接。

第一盖板 1、第二盖板 5 可以为透明或不透明的盖板，例如玻璃盖板、塑料盖板。

第一封装胶层 2 的两侧分别与第一盖板 1、电池片 3 接触贴合，第二封装胶层 4 的两侧分别与第二盖板 1、电池片 3 接触贴合。其中，第一封装胶层 2、第二封装胶层 4 分别可以乙烯-乙酸乙烯共聚物（EVA）胶膜、聚乙烯辛烯共弹性体（POE）胶膜或者聚对苯二甲酸乙二醇酯（PET）胶膜。

光伏组件还可以采用侧边全包围式封装，即采用封装胶带对光伏组件的侧边完全包覆封装，以防止光伏组件在层压过程中发生层压偏移的现象。

进一步地，光伏组件（图 7b 所示的光伏组件 100）还包括封边部件 6，该封边部件 6 固定封装于光伏组件的部分边缘。如图 7b 所示，该封边部件 6 固定封装于光伏组件上的靠近拐角处的边缘。该封边部件 6 可以为耐高温胶带。该耐高温胶带具有较优异的耐高温特性，在层压过程中不会发生分解或脱落，能够保证对光伏组件的可靠封装。其中，耐高温胶带的两端分别固定于第二盖板 5 和第一盖板 1。该耐高温胶带的两端可以分别与第二盖板 5 和第一盖板 1 粘接，而其中部能够实现对光伏组件的侧边的限位，防止光伏组件在层压过程中发生层压偏移。

第三方面，本申请还提供一种太阳能电池的制备方法，用于制备上述太阳能电池，如图 8 所示，制备方法包括以下步骤：

步骤 S10，对半导体衬底进行制绒处理，半导体衬底的前表面形成第二纹理结构，第二纹理结构可以包括金字塔状微结构；

步骤 S20，对制绒后的半导体衬底的前表面进行掺杂处理，形成掺杂层；

步骤 S30，采用碱溶液对半导体衬底的后表面进行抛光处理，使得半导体衬底后表面形成第一纹理结构，其中，所述第一纹理结构包括至少部分堆叠的两个或多个第一子结构，其中，对于所述至少部分堆叠的两个或多个第一子结构，在远离所述后表面且垂直于所述后表面的方向上，最外侧第一子结构的顶部表面及与其相邻的第一子结构的顶部表面的距离小于等于 $2\text{ }\mu\text{m}$ ，所述最外侧第一子结构的顶部表面的一维尺寸小于等于 $45\text{ }\mu\text{m}$ ；

步骤 S40，在半导体衬底的后表面的第一纹理结构上形成隧穿氧化层；

步骤 S50，在隧穿氧化层表面沉积形成多晶硅层，并对多晶硅层进行掺杂处理，形成掺杂导电层，所述掺杂导电层与所述半导体衬底具有相同导电类型的掺杂元素；

步骤 S60，在半导体衬底的前表面形成第一钝化层；以及

步骤 S70，在掺杂导电层表面形成第二钝化层。

在上述方案中，采用碱溶液对半导体衬底的后表面进行抛光处理，使

得半导体衬底前后表面形成不同形貌的纹理结构，在前表面形成金字塔状纹理结构以及在后表面形成非金字塔纹理结构，可以使得形成的电池具有不同层次的陷光结构，增加光的有效接触面积，而且，对于形成在后表面的第一纹理结构，将最外侧第一子结构的顶部表面及与其相邻的第一子结构的顶部表面的距离控制在 $2\mu\text{m}$ 以内，有利于减少隧穿氧化层中的孔洞密度 (pinhole) 进而提升隧穿氧化层的致密度和均匀性，并进一步抑制隧穿氧化层表面的掺杂导电层的局部掺杂浓度偏高，降低接触电阻率，提高太阳能电池的开路电压，提升填充因子及光电转换效率。

以下具体介绍本方案：

步骤 S10，对半导体衬底进行制绒处理，半导体衬底的前表面形成第二纹理结构，第二纹理结构包括金字塔状微结构。

半导体衬底可以为晶体硅衬底（硅衬底），例如为多晶硅衬底、单晶硅衬底、微晶硅衬底或碳化硅衬底中的一种，本申请实施例对于半导体衬底的具体类型不作限定。在一些实施例中，半导体衬底为 N 型晶体硅衬底（或硅片），半导体衬底的厚度为 $60\mu\text{m}\sim 240\mu\text{m}$ ，具体可以是 $60\mu\text{m}$ 、 $80\mu\text{m}$ 、 $90\mu\text{m}$ 、 $100\mu\text{m}$ 、 $120\mu\text{m}$ 、 $150\mu\text{m}$ 、 $200\mu\text{m}$ 或 $240\mu\text{m}$ 等，在此不做限定。半导体衬底的掺杂元素可以是磷、氮等。

需要指出的是，本申请对于制绒的具体操作方式不作限定。例如，可以选用不限于湿法制绒工艺对 N 型衬底进行制绒，当 N 型半导体衬底为 N 型单晶硅衬底时，可以采用碱性溶液例如氢氧化钾溶液进行制绒，由于 NaOH 溶液的腐蚀具有各向异性，从而可以制备得到金字塔状微结构。

如图 2 所示，半导体衬底 10 的前表面具有第二纹理结构 11，第二纹理结构 11 包括金字塔状微结构 111。金字塔状微结构 111 可以是四面体、近似四面体、五面体、近似五面体等结构。金字塔状微结构 111 可以通过对半导体衬底进行制绒工艺来形成。制绒工艺的方式可以是化学刻蚀、激光刻蚀、机械法、等离子刻蚀等。所述金字塔状微结构使在丝网印刷金属浆料形成电极时可以更好地填充于所述微结构中，获得更优异的电极接触，能够有效降低电池串联电阻，提高填充因子。

步骤 S20，对制绒后的半导体衬底的前表面进行掺杂处理，形成掺杂层。

在具体实施方式中，当半导体衬底 10 为 N 型衬底时，可以采用高温

扩散、浆料掺杂或者离子注入中的任意一种或多种工艺在半导体衬底的前表面形成 P 型掺杂层，以便在所述半导体衬底 10 中形成 PN 结。

在一些实施例中，所述 P 型掺杂层为掺硼扩散层。掺硼扩散层是利用硼源通过扩散工艺使硼原子扩散到前表面一定深度而形成的 P 型掺杂层（即，P⁺层）。例如，硼源可以是液态三溴化硼。硼扩散处理的衬底的微晶硅相转变为多晶硅相。由于半导体衬底表面具有较高浓度的硼，通常会形成硼硅玻璃层（BSG）。

进一步地，在步骤 S30，采用碱溶液对半导体衬底的后表面进行抛光处理之前，方法还包括：

用配制好的混合酸去除半导体衬底的后表面的硼硅玻璃层，混合酸包括质量分数为 0.1%~10%的氢氟酸溶液、质量分数为 10%~20%的硫酸溶液与 25%~50%的硝酸溶液；

将酸洗后的半导体衬底后表面进行水洗、烘干处理。

可以理解地，在硼扩散处理时，半导体衬底的后表面会绕镀形成部分硼硅玻璃，需要去除这部分的硼硅玻璃。需要说明的是在酸洗后半半导体衬底的后表面会出现多孔结构。

具体地，酸洗时间为 10s~180s，酸洗温度为 7°C~20°C，即在常温状态下对半导体衬底后表面的硼硅玻璃进行酸洗去除，露出半导体衬底本体。

步骤 S30，采用碱溶液对半导体衬底的后表面进行抛光处理，采用碱溶液对半导体衬底的后表面进行抛光处理，使得半导体衬底后表面形成第一纹理结构。

具体地，采用质量分数为 5%~15%碱溶液清洗半导体衬底的后表面，去除多孔硅；

再采用喷淋方式将碱溶液的微液滴滴至半导体衬底的后表面进行粗糙化处理，再用质量分数为 5%~10%的氢氟酸进行预清洗；

采用抛光液对半导体衬底的后表面进行抛光，抛光温度为 70°C~80°C，抛光时间<260s，其中，抛光液包括质量分数为 1%~15%的 NaOH、质量分数为 1%~15%的 KOH 及质量分数为 0.5%~2.5%的添加剂；

采用质量分数为 5%~15%的氢氧化钾与质量分数为 15%~40%的双氧水的混合液对刻蚀液中的有机成分进行去除；

对抛光后的半导体衬底进行水洗、烘干处理。

在一些实施例中，在进行后表面抛光处理时，需要对半导体衬底前表面的硼硅玻璃层进行保护，比如通过掩模保护硼硅玻璃层。

在具体实施例中，由于半导体衬底后表面的硼浓度较低，采用碱溶液进行蚀刻，可以有效提高蚀刻效率。碱溶液中含有有机碱和/或无机碱，无机碱可以是 NaOH、KOH、 $\text{Ga}(\text{OH})_2$ 、 $\text{NH}_3\cdot\text{H}_2\text{O}$ ，有机碱可以是三乙胺、硝基苯酚、吡啶、奎宁、秋水仙素等。抛光液中的添加剂可以是由磺酸钠、马来酸酐、烷基糖苷等组成的缓冲液。

抛光温度具体可以是 70°C 、 72°C 、 74°C 、 75°C 、 78°C 、 79°C 、 80°C 等，抛光时间可以是 250s、240s、230s、220s、200s、180s、160s、140s、120s、100s、80s 等，当然也可以是上述范围内的其他值。

在一些实施例中，半导体衬底的抛光减重小于 0.3g。

通过控制抛光时间与抛光温度，可以调整抛光后的第一纹理结构中的子结构的形状，使得至少部分堆叠的两个或多个第一子结构中，在远离所述后表面且垂直于所述后表面的方向上，最外侧第一子结构的顶部表面及与其相邻的第一子结构的顶部表面的距离小于等于 $2\mu\text{m}$ ，从而增加半导体衬底后表面的粗糙度。

在一些实施例中，可以采用热风干燥半导体衬底的表面形成包括非金字塔状微结构的第一纹理结构。

作为本申请可选的技术方案，图 3 为本申请实施例提供的半导体衬底的后表面的第一纹理结构 12 的电镜示意图，如图 3 所示，第一纹理结构 12 包括至少部分堆叠的两个或多个第一子结构 121。

图 4a 为示例的部分堆叠的三层第一子结构的示意图，图 4b 为示例的部分堆叠的两层第一子结构的示意图。

对于所述至少部分堆叠的两个或多个第一子结构 121，在远离所述后表面且垂直于所述后表面的方向上，最外侧第一子结构的顶部表面 121a 及与其相邻的第一子结构的顶部表面 121b 的距离 H 小于等于 $2\mu\text{m}$ ，具体可以是 $2\mu\text{m}$ 、 $1.8\mu\text{m}$ 、 $1.5\mu\text{m}$ 、 $1.2\mu\text{m}$ 、 $1.1\mu\text{m}$ 、 $1.0\mu\text{m}$ 、 $0.8\mu\text{m}$ 、 $0.5\mu\text{m}$ 、 $0.3\mu\text{m}$ 、 $0.2\mu\text{m}$ 或 $0.1\mu\text{m}$ 等。当距离 H 超过 $2\mu\text{m}$ ，第一纹理结构的粗糙度过大，形成于第一纹理结构上的隧穿氧化层 30 的厚度越大，则不利于形成高致密度和高均匀性的隧穿氧化层，进而影响隧穿氧化层 30 的隧穿和钝化效

果；第一纹理结构的粗糙度过小，形成于第一纹理结构上的隧穿氧化层的厚度越小，则不利于与电极浆料的接触。优选地，在远离所述后表面且垂直于所述后表面的方向上，最外侧第一子结构的顶部表面 121a 及与其相邻的第一子结构的顶部表面 121b 的距离 H 在 $0.3\ \mu\text{m}$ ~ $1.2\ \mu\text{m}$ 内。

需要说明的是，当叠层设置的三层第一子结构时，任意一层第一子结构的顶部表面 121a 与相邻一层的第一子结构的顶部表面 121b 的距离 H 小于等于 $2\ \mu\text{m}$ 。

可以理解地，控制最外侧第一子结构的顶部表面 121a 及与其相邻的第一子结构的顶部表面 121b 的距离小于等于 $2\ \mu\text{m}$ ，可以使得第一纹理结构的粗糙度控制在所需范围内，有利于提高形成于第一纹理结构上的隧穿氧化层的均匀性，形成的隧穿氧化层性能更好，并进一步抑制磷扩散导致的局部磷浓度偏高，降低接触电阻率，提高太阳能电池的开路电压，提升填充因子及光电转换效率。

所述最外侧第一子结构的顶部表面 121a 的一维尺寸 L 小于等于 $45\ \mu\text{m}$ ，可选地，所述一维尺寸 L 在 $2\ \mu\text{m}$ ~ $45\ \mu\text{m}$ 内。这里，所述顶部表面的一维尺寸 L 具体可以是表面的长、宽、对角线长度、圆形的直径等，在此不做限定。在一些实施例中，所述一维尺寸可以是指衬底后表面的预设范围区域内，多个最外侧第一子结构的顶部表面的一维尺寸的平均值。最外侧第一子结构的顶部表面的平均一维尺寸具体可以是 $2\ \mu\text{m}$ 、 $5\ \mu\text{m}$ 、 $8\ \mu\text{m}$ 、 $12\ \mu\text{m}$ 、 $15\ \mu\text{m}$ 、 $18\ \mu\text{m}$ 、 $20\ \mu\text{m}$ 、 $25\ \mu\text{m}$ 、 $28\ \mu\text{m}$ 、 $30\ \mu\text{m}$ 、 $35\ \mu\text{m}$ 、 $40\ \mu\text{m}$ 、 $42\ \mu\text{m}$ 、 $40\ \mu\text{m}$ 或 $45\ \mu\text{m}$ 等。优选地，最外侧第一子结构的顶部表面的平均一维尺寸在 $10\ \mu\text{m}$ ~ $15\ \mu\text{m}$ 内。

在具体实施例中，如图 3 所示，所述第一纹理结构还包括邻接非堆叠排布的两个或多个第二子结构 122，远离所述后表面的所述第二子结构 122 的顶部表面的一维尺寸 L 小于等于 $45\ \mu\text{m}$ 。可选地，所述第一子结构 122 的一维尺寸 L 在 $2\ \mu\text{m}$ ~ $45\ \mu\text{m}$ 内，具体可以是 $2\ \mu\text{m}$ 、 $5\ \mu\text{m}$ 、 $8\ \mu\text{m}$ 、 $12\ \mu\text{m}$ 、 $15\ \mu\text{m}$ 、 $18\ \mu\text{m}$ 、 $20\ \mu\text{m}$ 、 $25\ \mu\text{m}$ 、 $28\ \mu\text{m}$ 、 $30\ \mu\text{m}$ 、 $32\ \mu\text{m}$ 、 $35\ \mu\text{m}$ 或 $45\ \mu\text{m}$ 等。

区别于前表面的典型金字塔状微结构，后表面的所述第一子结构和/或所述第二子结构的顶部表面为多边形平面，所述多边形平面的形状包括菱形、方形、梯形、近似菱形、近似方形、近似梯形中的至少一种。可以理解的是，在实际的制造过程中，所述第一子结构或第二子结构的顶部表

面形貌呈现不规则的多边形平面，但总体呈现出近似于菱形、方形、梯形的形貌特征。

步骤 S40, 在半导体衬底的后表面的第一纹理结构上形成隧穿氧化层。

在一些可行的实施方式中，可以采用臭氧氧化法、高温热氧化法、硝酸氧化法、化学气相沉积法、低压化学气相沉积法对半导体衬底进行后表面刻蚀之后进行处理，形成隧穿氧化层 30。

在一些实施例中，采用变温式工艺以及化学气相沉积法在半导体衬底的后表面沉积形成隧穿氧化层 30。在沉积过程中，控制升温速率为 $0.5^{\circ}\text{C}/\text{min}\sim 3^{\circ}\text{C}/\text{min}$ ，沉积温度为 $560^{\circ}\text{C}\sim 620^{\circ}\text{C}$ ，沉积时间为 $3\text{min}\sim 10\text{min}$ 。

具体地，在沉积过程中，沉积温度可以是 560°C 、 570°C 、 580°C 、 590°C 、 600°C 、 610°C 、 615°C 或 620°C 等，沉积时间可以是 3min 、 4min 、 5min 、 6min 、 7min 、 8min 、 9min 或 10min 等，升温速率可以为 $0.5^{\circ}\text{C}/\text{min}$ 、 $0.8^{\circ}\text{C}/\text{min}$ 、 $1.0^{\circ}\text{C}/\text{min}$ 、 $1.2^{\circ}\text{C}/\text{min}$ 、 $1.5^{\circ}\text{C}/\text{min}$ 、 $2.0^{\circ}\text{C}/\text{min}$ 、 $2.5^{\circ}\text{C}/\text{min}$ 或 $3^{\circ}\text{C}/\text{min}$ 等，当然也可以是上述范围内的其他值，在此不做限定。

优选地，采用低压化学气相沉积法在半导体衬底的后表面沉积形成隧穿氧化层 30，可以减少后续高温掺杂处理时较薄的隧穿氧化层 30 局部掺杂浓度过高的影响，降低开路电压的波动，通过变温式工艺以及低压化学气相沉积法沉积形成的隧穿氧化层 30，可以使得太阳能电池的开路电压提高 4mV 至 6mV 。

隧穿氧化层 30 可以是氧化硅层、氧化铝层、氮氧化硅层、氧化钼层、氧化钨层中的一种或多种层叠结构。在其他实施例中，隧穿氧化层 30 也可以是含氧氮化硅层、含氧碳化硅层等。隧穿氧化层 30 的厚度为 $0.8\text{nm}\sim 2\text{nm}$ 。具体地，隧穿氧化层 30 的厚度为 0.8nm 、 0.9nm 、 1.0nm 、 1.2nm 、 1.4nm 、 1.6nm 、 1.8nm 或 2nm 等。隧穿氧化层 30 的厚度是指隧穿氧化层相对于形成面上的厚度。在第一纹理结构上形成的隧穿氧化层 30 的厚度可以通过将子结构的斜面的法线方向作为厚度方向，进行截面观察并计算得到。隧穿氧化层 30 的厚度过大，不利于降低隧穿氧化层的接触电阻。通过控制隧穿氧化层的厚度，可以抑制接触电阻引起的填充因子的降低。

具体地，隧穿氧化层 30 的带隙宽度 $> 3.0\text{eV}$ ，载流子通过热发射一般难以传输通过隧穿氧化层 30，但是由于隧穿氧化层 30 很薄，载流子可以通过隧穿效应穿过隧穿氧化层 30，因此厚度在 $0.8\text{nm}\sim 2\text{nm}$ 内的隧穿氧化层对多数载流子的传输没有阻碍。随着隧穿氧化层的厚度逐渐增大时，多

数载流子的隧穿效应受到影响，载流子难以传输通过隧穿氧化层 30，电池的光电转换效率会逐渐下降。隧穿氧化层的厚度过小时，无法起到钝化作用。优选地，隧穿氧化层 30 为氧化硅层，隧穿氧化层 30 的厚度为 0.8nm~1.5nm。

作为本申请可选的技术方案，如图 6 所示，所述最外侧第一子结构的顶部表面上的隧穿氧化层厚度 D1 小于所述最外侧第一子结构侧部表面上形成的隧穿氧化层厚度 D2。具体地，所述最外侧第一子结构的顶部表面上的隧穿氧化层与所述最外侧子结构的侧部表面上形成的隧穿氧化层之间的厚度差(D2-D1)小于等于 0.15nm。厚度差具体可以是 0.14nm、0.13nm、0.12nm、0.11nm、0.10nm、0.09nm、0.08nm、0.07nm、0.06nm、0.05nm、0.04nm 等。当最外侧第一子结构的顶部表面上的隧穿氧化层与最外侧子结构的侧部表面上形成的隧穿氧化层过大时，隧穿氧化层的厚度均匀性差，太阳能电池的电流密度容易受影响，太阳能电池的开压电路下降。

步骤 S50，在隧穿氧化层表面沉积形成多晶硅层，并对多晶硅层进行掺杂处理，形成掺杂导电层，掺杂导电层的导电类型与半导体衬底的导电类型相同。

在一些可行的实施方式中，采用物理气相沉积法、化学气相沉积法、等离子体增强化学气相沉积法、原子层沉积法中的任意一种方法沉积在隧穿氧化层的表面沉积形成多晶硅层。化学气相沉积法可以是低压化学气相沉积法或常压化学气相沉积法。

在具体实施方式中，隧穿氧化层与多晶硅层的沉积以及多晶硅层的掺杂均在低压化学气相沉积设备中形成。

具体步骤包括：

首先，将碱抛光后的半导体衬底置于沉积设备中，通入 20L 至 60L 的氧源(例如可以是氧气、一氧化二氮、臭氧)，按照升温速率为 0.5°C/min~3°C/min 将沉积设备内的温度加热至 560°C~620°C，沉积时间为 3min~10min，形成隧穿氧化层 30；

通氧结束后，进行恒温阶段，然后通入适量硅烷气体，形成多晶硅层；最后，对多晶硅层进行原位掺杂，形成掺杂导电层 40。

在一些实施例中，掺杂导电层 40 可以是掺杂多晶硅层，所述掺杂导电层 40 与所述半导体衬底具有相同导电类型的掺杂元素。

在其他实施例中，也可以在隧穿氧化层 30 的表面沉积形成微晶硅层

DD212023I

或非晶硅层，并进行原位掺杂，形成掺杂微晶硅层或掺杂非晶硅层，即掺杂导电层 40。

当半导体衬底 10 为 N 型单晶硅衬底，掺杂导电层 40 为 N 型掺杂多晶硅层、N 型掺杂微晶硅层或 N 型掺杂非晶硅层，掺杂元素可以是磷等 N 型掺杂元素。

在一些实施例中，所述掺杂导电层 40 的厚度范围为 60nm-200nm，例如，N 型掺杂多晶硅层，所述掺杂导电层 40 的折射率范围为 3.5-4.5。

在步骤 S50 之后，并在步骤 S60 之前，上述方法还包括：

在沉积原位掺杂的多晶硅层之后进行了高温退火处理和清洗处理。

本申请实施例对于该高温退火处理和清洗处理的具体操作方式不作限定。示例性的，该高温退火处理所处理的是沉积的多晶硅层，能使得多晶硅层更好的结晶，退火的温度范围可以为 700℃~1000℃。

通过高温退火处理，使得扩散五价的磷原子形成掺杂多晶硅层，退火处理后，晶体硅的微晶硅相转变为多晶硅相，磷沉积在半导体衬底表面形成磷硅玻璃（PSG）。

清洗处理是为了去除在磷掺杂过程中形成的磷硅玻璃层（PSG）。可以理解地，在磷扩散时，由于半导体衬底表面具有较高浓度的磷，通常会形成磷硅玻璃层（PSG），这层磷硅玻璃层具有金属吸杂作用，会影响太阳能电池的正常工作，需要去除。

在具体实施例中，可以将半导体衬底后表面朝下置于链式酸洗设备（链式设备带速为 1.0m/min~2.0m/min，半导体衬底进入酸槽，刻蚀掉后表面磷扩散形成的磷硅玻璃层（PSG）。酸槽内设有配制好的混合酸，混合酸包括质量浓度为 2%~10% 的氢氟酸溶液与质量浓度为 2%~10% 的盐酸溶液，酸洗温度为 15℃~25℃，酸洗时间约为 30s~60s，半导体衬底前表面有水膜覆盖，且半导体衬底前表面的硼硅玻璃层（BSG）也可以作为保护层，在去磷硅玻璃层（PSG）过程中，避免半导体衬底前表面与混合酸反应。

需要说明的是，酸洗后需要进行水洗，水洗时间为 10~20s，水洗温度可以为 15℃~25℃；当然，水洗之后还可以对半导体衬底进行烘干处理。

步骤 S60，在导体衬底的前表面形成第一钝化层。

在一些实施例中，可以采用等离子体增强化学气相沉积法沉积第一钝

DD212023I

化层20,当然还可以采用其他的方法,例如有机化学气相沉积法等。本申请实施例对于第一钝化层20的具体实施方式不作限定。

第一钝化层20可以包括但不限于氮化硅层、氮氧化硅层、氧化硅层等单层或叠层结构。当然,第一钝化层还可以采用其他类型的钝化层,本申请对于第一钝化层的具体材质不作限定,例如,在其他实施例中,第一钝化层还可以为二氧化硅和氮化硅的叠层等。上述第一钝化层能够对半导体衬底产生良好的钝化效果,有助于提高电池的转换效率。

步骤S70,在掺杂导电层表面形成第二钝化层。

可以采用等离子体增强化学气相沉积法沉积第二钝化层50,当然还可以采用其他的方法,例如有机化学气相沉积法等。本申请实施例对于第二钝化层50的具体实施方式不作限定。

作为本申请可选的技术方案,第二钝化层50包括氮化硅层、氧化硅层、氮氧化硅层中的至少一种。所述第二钝化层50的厚度为70nm-120nm。例如,所述第二钝化层50为氮化硅层,所述氮化硅层具有低硅氮比,氮化硅层的折射率范围为1.7~2.1,氮化硅层的折射率可以为1.7、1.8、1.9、2.0或2.1等,当然也可以是上述范围内的其他值,在此不做限定。通过控制氮化硅层的折射率,使得其具有低硅氮比,形成的第二钝化层50在金属化处理时能够降低接触电阻率,从而进一步降低太阳能电池的接触电阻率。

在一些实施例中,当第二钝化层50为层叠设置的氮化硅层与氧化硅层或层叠设置的氮化硅层与氮氧化硅层时,氮化硅层位于掺杂导电层的表面,氧化硅层或氮氧化硅层位于氮化硅层的表面。

进一步地,在步骤S70之后,方法还包括:

对半导体衬底进行丝网印刷并烧结形成电极。

在一些实施例中,太阳能电池还包括第一电极60与第二电极70,第一电极60穿过第一钝化层20与半导体衬底10的前表面的P型掺杂层(例如,掺硼扩散层)形成欧姆接触,第二电极70穿过第二钝化层50与掺杂导电层40形成欧姆接触,掺杂导电层40与隧穿氧化层30组成钝化接触结构。所述第一电极60以及第二电极70可以通过涂敷在第一钝化层以及第二钝化层表面的金属导电浆料烧结形成。在一些实施例中,所述第一电极60或第二电极70的材料包括银、铝、铜、镍等金属材料。



下面根据上述方法制备得到太阳能电池实施例 1 至 13，以及对比例 1 至 4，具体工艺参数见表 1 所示：



DD212023I

表 1 太阳能电池的参数

样本	第二级理结构		第一级理结构		隧穿氧化层厚度 (nm)	第一钝化层	第一钝化厚度 (nm)	第一钝化层的折射率	第二钝化层的厚度 (nm)	第二钝化层的折射率
	金字塔状微结构顶部与底部之间的距离 (um)	第一子结构的顶部与底部表面之间的距离 (um)	最外侧第二子结构的顶部的尺寸 (um)	隧穿氧化层的厚度 (nm)						
实施例 1	3.0	1.9	8.6	1.2	0.12	氧化铝+氮化硅	5+50	1.92	氮化硅	70
实施例 2	3.2	1.8	8.9	1.2	0.12	氧化铝+氮化硅	5+60	1.95	氮化硅	75
实施例 3	3.1	1.7	10.2	1.15	0.11	氧化铝+氮化硅	5+65	1.94	氮化硅	78
实施例 4	4.4	1.6	11.6	1.12	0.11	氧化铝+氮化硅	5+70	1.93	氮化硅	80
实施例 5	3.8	1.8	12.4	1.1	0.11	氧化铝+氮化硅	5+75	1.95	氮化硅	82
实施例 6	3.6	1.6	13.2	1.1	0.11	氧化铝+氮化硅	5+80	1.97	氮化硅	85
实施例 7	3.5	1.7	14.5	1.1	0.10	氧化铝+氮化硅	8+85	1.98	氮化硅	88
实施例 8	3.2	1.5	12.1	1.05	0.10	氧化铝+氮化硅	10+100	1.95	氮化硅	90
实施例 9	3.0	1.6	15.6	1.02	0.10	氮化硅	100	1.98	氮化硅	95
实施例 10	3.0	1.5	18.2	1.0	0.10	氮化硅	105	1.96	氮化硅	98
实施例 11	2.8	1.9	24.8	0.95	0.12	氮化硅	110	1.92	氮化硅	100
实施例 12	2.7	1.4	26.3	0.95	0.08	氮化硅	95	2.0	氮化硅	110
实施例 13	2.8	1.5	38.4	0.9	0.08	氮化硅	90	1.95	氮化硅	120
对比例 1	3.0	2.5	5.5	1.3	0.18	氧化铝+氮化硅	5+50	1.92	氮化硅	70
对比例 2	3.0	/	/	1.4	0.18	氧化铝+氮化硅	5+50	1.92	氮化硅	70
对比例 3	3.0	1.8	8.6	1.2	0.12	氧化铝+氮化硅	5+50	1.92	氮化硅	70
对比例 4	3.0	1.8	8.6	1.2	0.12	氧化铝+氮化硅	5	1.52	氮化硅	70

表 2.太阳能电池的相关制备工艺参数

样本	氧源气体 加载温度 (°C)	氧化温度 1 (°C)	氧化温度 2 (°C)	氧化温度 3 (°C)	预沉积升 温阶段 (°C)	沉积多晶 硅层温度 (°C)	硅烷气体 加载温度 (°C)
实施例 1	590	590	595	600	620	620	590
实施例 2	590	595	590	600	620	620	590
实施例 3	590	595	600	600	620	620	590
实施例 4	590	590	595	600	625	630	590
实施例 5	590	595	590	600	625	630	590
实施例 6	590	595	600	600	625	630	590
实施例 7	600	608	610	600	620	630	600
实施例 8	600	610	610	610	625	630	600
实施例 9	600	605	610	600	625	625	600
实施例 10	610	600	615	600	620	625	610
实施例 11	615	610	610	610	625	625	615
实施例 12	615	610	605	600	620	625	615
实施例 13	615	610	605	600	620	625	615
对比例 1	590	590	590	590	610	610	605
对比例 2	610	610	610	610	620	620	615
对比例 3	630	630	630	630	650	650	645
对比例 4	590	590	590	590	610	610	605

表 3. 太阳能电池的测试结果

样本	开路电压(mV)	短路电 流 (A)	填充因子	光电转化 效率 (%)	接触电阻率 (mΩ.cm)
实施例 1	710	11.06	83.51	24.52	1.26
实施例 2	710	11.05	83.04	24.36	1.25
实施例 3	710	11.04	83.54	24.49	1.28
实施例 4	710	11.11	83.41	24.61	1.27
实施例 5	712	11.1	83.43	24.66	1.31
实施例 6	712	11.08	83.39	24.60	1.30
实施例 7	712	11.09	83.51	24.66	1.29
实施例 8	712	11.12	83.04	24.59	1.32
实施例 9	688	11.11	83.46	23.86	1.28
实施例 10	689	11.1	83.14	23.78	1.27
实施例 11	687	11.08	83.27	23.70	1.28
实施例 12	688	11.04	83.04	23.59	1.26
实施例 13	686	11.05	83.06	23.55	1.29
对比例 1	709	11.03	82.77	24.21	1.53
对比例 2	707	11.04	82.76	24.16	1.51
对比例 3	710	11.04	82.645	24.23	1.54
对比例 4	710	11.04	82.7	24.20	1.50

根据实施例 1 至实施例 13 可知, 通过将半导体衬底后表面的第一纹理结构中的子结构的距离控制在理想范围内, 可以保障半导体衬底后表面的粗糙度在合适的范围, 有利于提高形成于第一纹理结构上的隧穿氧化层的均匀性, 形成的隧穿氧化层性能更好, 并进一步抑制掺杂导电层的局部掺杂浓度偏高, 可以有效降低接触电阻率, 提高太阳能电池的开路电压,

提升填充因子及光电转换效率。

对比例 1 的太阳能电池中的第一纹理结构中，在远离所述后表面且垂直于所述后表面的方向上，最外侧第一子结构的顶部表面及与其相邻的第一子结构的顶部表面的距离大于 2 μm ，最外侧第一子结构的顶部表面的一维尺寸越小，沉积形成的隧穿氧化层越厚，隧穿氧化层的均匀性下降，导致形成于隧穿氧化层表面的掺杂导电层的局部掺杂浓度偏高，接触电阻率相较于实施例 1 有所增大，导致太阳能电池的开路电压下降，填充因子及光电转换效率也随之下降。

对比例 2 的太阳能电池在制绒后未经过碱抛光处理，后表面为金字塔状微结构，沉积在金字塔状微结构上的隧穿氧化层的均匀性下降，容易导致形成于隧穿氧化层表面的掺杂导电层的局部掺杂浓度偏高，接触电阻率相较于实施例 1 有所增大，导致太阳能电池的开路电压下降，填充因子及光电转换效率也随之下降。

对比例 3 的太阳能电池虽然通过第一纹理结构的子结构的处理，可以抑制掺杂导电层的局部掺杂浓度偏高，但是由于采用高硅氮比的氮化硅层，在金属化处理过程中，接触电阻率难以进一步下降。相比于实施例 1，采用控制半导体衬底后表面的第一纹理结构中的子结构的距离以及控制第二钝化层的折射率，两者协同作用，可以更好地降低接触电阻率，提高太阳能电池的开路电压、填充因子及光电转换效率。

对比例 4 的太阳能电池虽然通过第一纹理结构的子结构的处理，可以抑制掺杂导电层的局部掺杂浓度偏高，但是由于采用整体折射率较低的氧化铝层和氮化硅层作为第一钝化层，在金属化处理过程中，接触电阻率升高。

本申请虽然以较佳实施例公开如上，但并不是用来限定权利要求，任何本领域技术人员在不脱离本申请构思的前提下，都可以做出若干可能的变动和修改，因此本申请的保护范围应当以本申请权利要求所界定的范围为准。



说明书附图

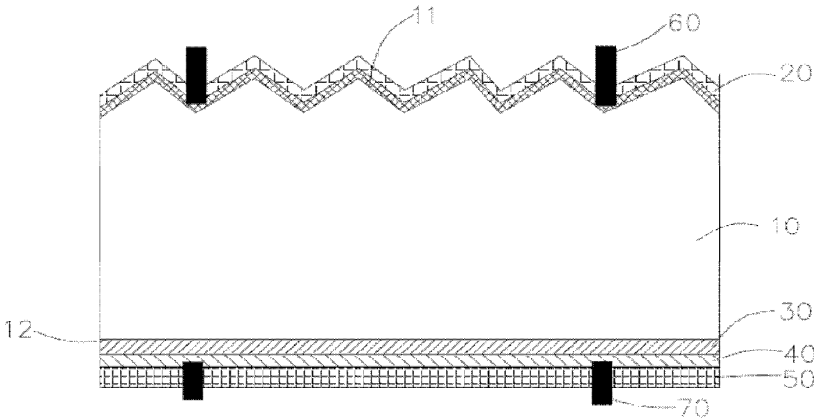


图 1

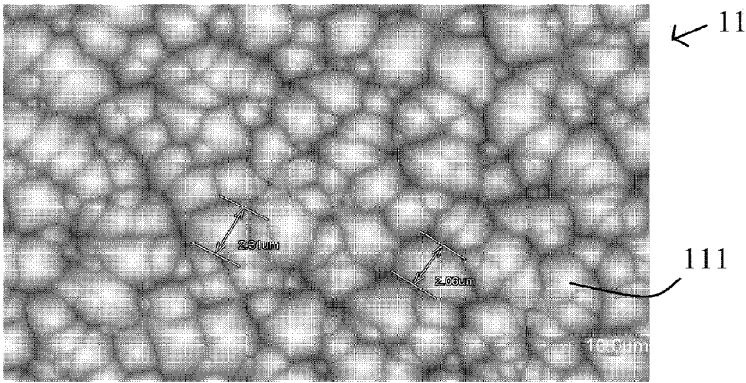


图 2

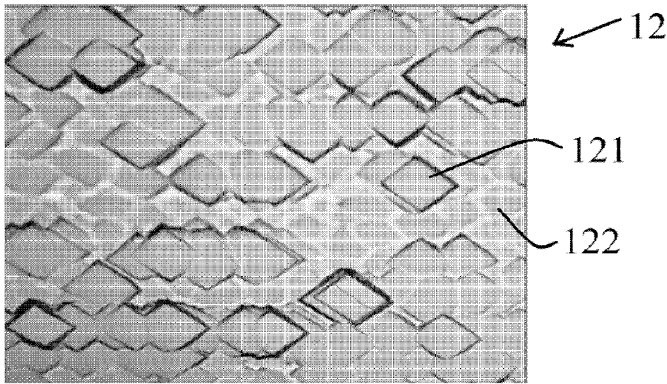


图 3



DD212023I

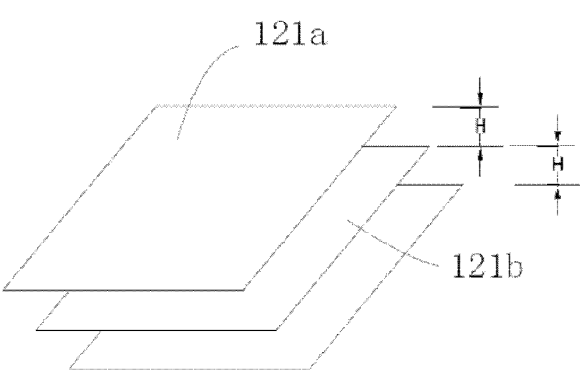


图 4a

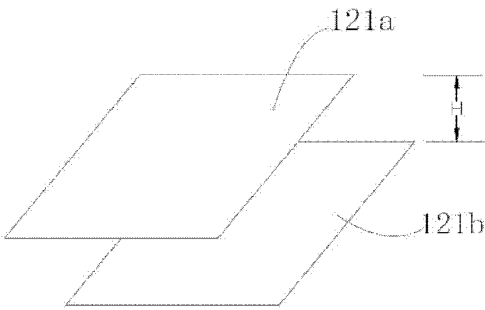


图 4b

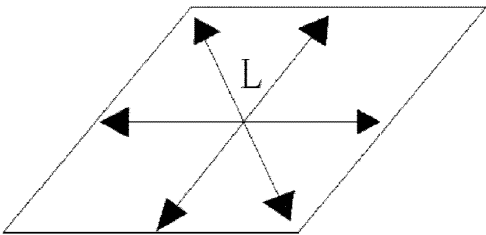


图 5

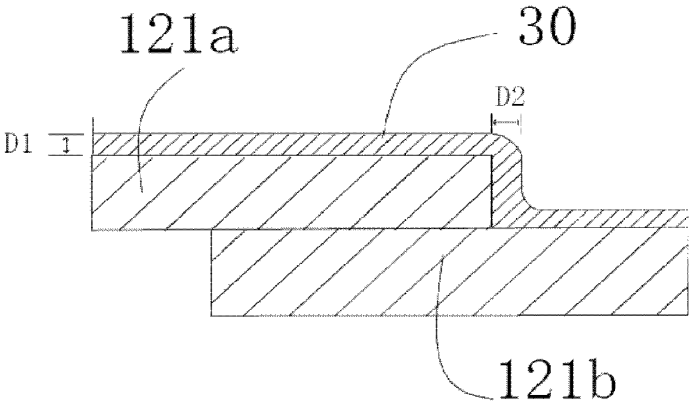


图 6



DD212023I

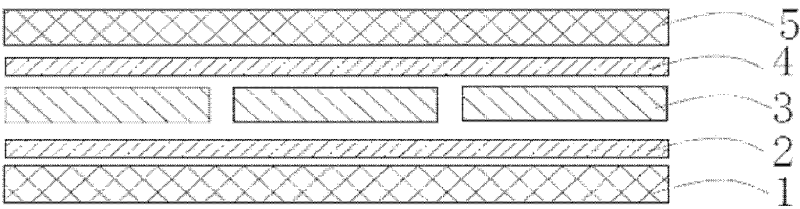


图 7a

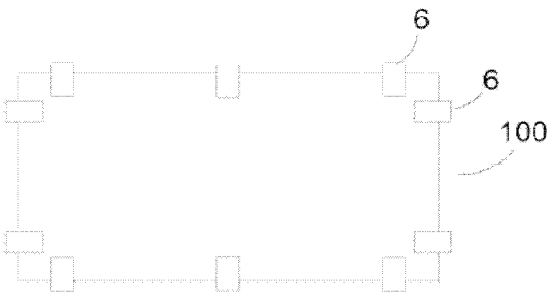


图 7b

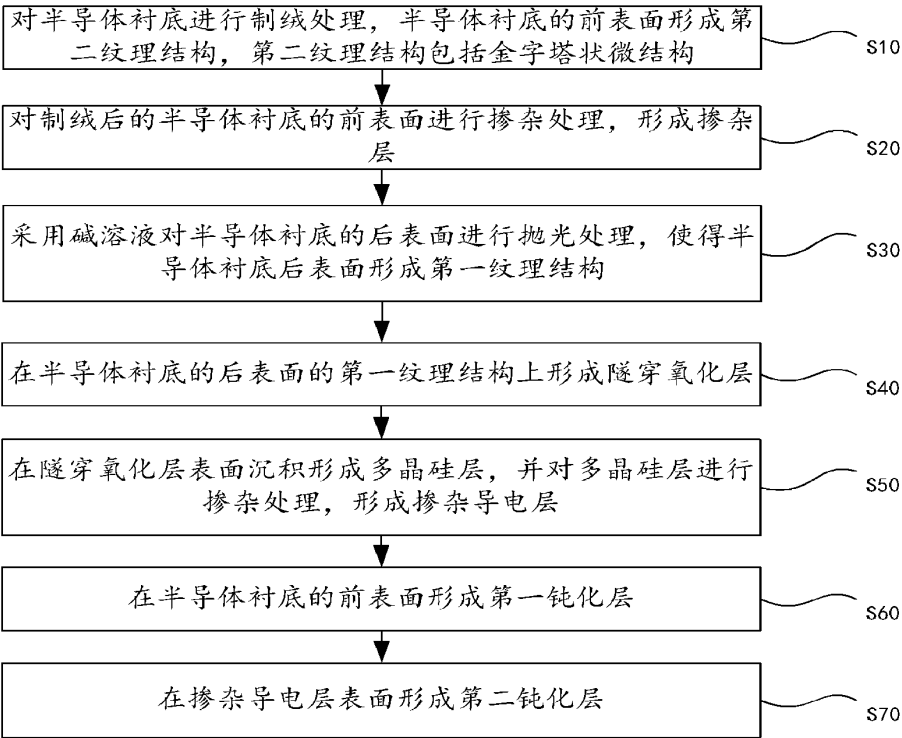


图 8



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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY DOCKET NO	TOT CLAIMS	IND CLAIMS
17/459,689	08/27/2021	1733	1820	084546-000033	20	3

CONFIRMATION NO. 8617

FILING RECEIPT



0000000128249004

22204
NIXON PEABODY, LLP
799 Ninth Street, NW
SUITE 500
WASHINGTON, DC 20001

Date Mailed: 09/09/2021

Receipt is acknowledged of this non-provisional utility patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF FIRST INVENTOR, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection.

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Inventor(s)

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Power of Attorney: The patent practitioners associated with Customer Number 22204

Domestic Applications for which benefit is claimed - None.

A proper domestic benefit claim must be provided in an Application Data Sheet in order to constitute a claim for domestic benefit. See 37 CFR 1.76 and 1.78.

Foreign Applications (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see <http://www.uspto.gov> for more information.)
CHINA 202110895225.8 08/04/2021 Access Code Provided

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If Required, Foreign Filing License Granted: 09/07/2021

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 17/459,689**

Projected Publication Date: 02/09/2023

Non-Publication Request: No

Early Publication Request: No

Title

SOLAR CELL, MANUFACTURING METHOD THEREOF, AND PHOTOVOLTAIC MODULE

Preliminary Class

148

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875						Application or Docket Number 17/459,689				
APPLICATION AS FILED - PART I										
(Column 1)		(Column 2)		SMALL ENTITY		OR OTHER THAN SMALL ENTITY				
FOR	NUMBER FILED	NUMBER EXTRA	RATE(\$)	FEE(\$)		RATE(\$)	FEE(\$)			
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	320			
SEARCH FEE (37 CFR 1.16(k), (j), or (m))	N/A	N/A	N/A			N/A	700			
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	800			
TOTAL CLAIMS (37 CFR 1.16(i))	20	minus 20 = *				x 100 =	0.00			
INDEPENDENT CLAIMS (37 CFR 1.16(h))	3	minus 3 = *				x 480 =	0.00			
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00			
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00			
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL		TOTAL	1820			
APPLICATION AS AMENDED - PART II										
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY		OR OTHER THAN SMALL ENTITY		
AMENDMENT A		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)		RATE(\$)	ADDITIONAL FEE(\$)
	Total (37 CFR 1.16(i))	*	Minus	**	=	x	=		x	=
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x	=		x	=
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))									
						TOTAL ADD'L FEE			TOTAL ADD'L FEE	
AMENDMENT B		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)		RATE(\$)	ADDITIONAL FEE(\$)
	Total (37 CFR 1.16(i))	*	Minus	**	=	x	=		x	=
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x	=		x	=
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))									
						TOTAL ADD'L FEE			TOTAL ADD'L FEE	
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.										

SOLAR CELL, MANUFACTURING METHOD THEREOF, AND PHOTOVOLTAIC MODULE

CROSS-REFERENCE TO RELATED APPLICATIONS

5 **[0001]** The present application claims priority to Chinese Patent Application No. 202110895225.8, filed on August 04, 2021, the content of which is incorporated herein by reference in its entirety.

TECHNICAL FIELD

[0001] The present disclosure relates to the field of photovoltaic cell technologies, and in particular, to a solar cell, a manufacturing method thereof, and a photovoltaic module.

10

BACKGROUND

[0002] An N-type tunnel oxide passivated contact (TOPCon) solar cell relies on a "tunnel effect" to achieve passivated contact on a rear surface of the solar cell. When manufacturing the TOPCon solar cell, borosilicate glass is formed by boron diffusion on a surface of a silicon wafer (or a substrate), which is more difficult to be removed compared with
15 phosphorosilicate glass of a conventional PERC solar cell. Generally, borosilicate glass on a rear surface of an N-type solar cell is removed by an oxidizing mixed acid solution. After the surface is cleaned and dried, the rear surface is polished with the aid of a trough or chain acid additive. The polished rear surface of the silicon wafer has a flat structure, but the structure of the polished rear surface may directly affect the manufacturing of the tunnel oxide layer and
20 the polycrystalline silicon layer, and then affect passivation performance and conversion efficiency of the solar cell.

SUMMARY

[0003] In view of the above, the present disclosure provides a solar cell, a manufacturing method thereof, and a photovoltaic module, which, through matching between texture structures on substrate surfaces of the solar cell, can improve an open-circuit voltage of the solar cell, reduce contact resistance of a metal electrode, and improve conversion efficiency of the solar cell.

[0004] In a first aspect, the present disclosure provides a solar cell, including:

a semiconductor substrate, wherein a rear surface of the semiconductor substrate has a first texture structure, the first texture structure includes two or more first substructures at least partially stacked on one another, and in a direction away from the rear surface and perpendicular to the rear surface, a distance between a top surface of an outermost first substructure and a top surface of an adjacent first substructure is less than or equal to 2 μm , and a one-dimensional size of the top surface of the outermost first substructure is less than or equal to 45 μm ;

a first passivation layer located on a front surface of the semiconductor substrate;

a tunnel oxide layer located on the first texture structure of the rear surface of the semiconductor substrate;

a doped conductive layer located on a surface of the tunnel oxide layer, a conductivity type of doping elements of the doped conductive layer being same as that of the semiconductor substrate; and

a second passivation layer located on a surface of the doped conductive layer.

[0005] In an implementation, the front surface of the semiconductor substrate has a second texture structure, the second texture structure includes a pyramid-shaped microstructure, the pyramid-shaped microstructure includes a top portion away from the front surface of the semiconductor substrate and a bottom portion close to the front surface of the semiconductor substrate, and in a direction away from the front surface and perpendicular to the front surface, a distance between the top portion and the bottom portion of the pyramid-shaped microstructure is less than or equal to 5 μm .

[0006] In an implementation, for the two or more first substructures at least partially

stacked on one another, in the direction away from the rear surface and perpendicular to the rear surface, the distance between the top surface of the outermost first substructure and the top surface of the adjacent first substructure ranges from 0.3 μm to 1.2 μm .

5 **[0007]** In an implementation, an average one-dimensional size of the top surface of the outermost first substructure ranges from 10 μm to 15 μm .

[0008] In an implementation, a thickness of the tunnel oxide layer on the top surface of the outermost first substructure is less than a thickness of the tunnel oxide layer on a side surface of the outermost first substructure.

10 **[0009]** In an implementation, a thickness difference between the tunnel oxide layer on the top surface of the outermost first substructure and the tunnel oxide layer on a side surface of the outermost first substructure is less than or equal to 0.15 nm.

[0010] In an implementation, the first texture structure further includes two or more adjacent second substructures that do not stacked on one another, and a one-dimensional size of a top surface of the second substructure away from the rear surface is less than or equal to
15 45 μm .

[0011] In an implementation, the top surface of the first substructure and/or the top surface of the second substructure is a polygonal plane.

[0012] In an implementation, a shape of the polygonal plane includes at least one of a diamond, a square, a trapezoid, a substantially diamond, a substantially square or a
20 substantially trapezoid.

[0013] In an implementation, the tunnel oxide layer includes at least one of a silicon oxide layer, an aluminum oxide layer, a silicon oxynitride layer, a molybdenum oxide layer or a hafnium oxide layer, and the tunnel oxide layer has a thickness ranging from 0.8 nm to 2 nm.

[0014] In an implementation, the second passivation layer includes at least one of a
25 silicon nitride layer, a silicon oxide layer or a silicon oxynitride layer, and the second passivation layer has a thickness ranging from 70 nm to 120 nm.

[0015] In an implementation, the first passivation layer includes at least one of a silicon oxide layer, a silicon nitride layer, an aluminum oxide layer or a silicon oxynitride layer.

[0016] In an implementation, the semiconductor substrate is an N-type monocrystalline
30 silicon substrate, the doped conductive layer is an N-type doped polycrystalline silicon layer,

an N-type doped microcrystalline silicon layer or an N-type doped amorphous silicon layer, and the doped conductive layer has a thickness ranging from 60 nm to 200 nm.

5 [0017] In a second aspect, the present disclosure provides a photovoltaic module, including a plurality of solar cell strings, each of the plurality of solar cell strings including the solar cell described in the first aspect.

[0018] In a third aspect, the present disclosure provides a method for manufacturing a solar cell, including:

10 texturing a semiconductor substrate, and forming a second texture structure on a front surface of the semiconductor substrate, wherein the second texture structure includes a pyramid-shaped microstructure;

forming a doped layer with doping elements to the front surface of the textured semiconductor substrate;

15 polishing a rear surface of the semiconductor substrate with an alkali solution, such that a first texture structure is formed on the rear surface of the semiconductor substrate, wherein the first texture structure includes two or more first substructures at least partially stacked on one another, and in a direction away from the rear surface and perpendicular to the rear surface, a distance between a top surface of an outermost first substructure and a top surface of an adjacent first substructure is less than or equal to 2 μm , and a one-dimensional size of the top surface of the outermost first substructure is less than or equal to 45 μm ;

20 forming a tunnel oxide layer on the first texture structure of the rear surface of the semiconductor substrate;

25 depositing a polycrystalline silicon layer on a surface of the tunnel oxide layer, and forming a doped conductive layer by doping the polycrystalline silicon layer, wherein the doped conductive layer and the semiconductor substrate have doping elements of a same conductivity type;

forming a first passivation layer on the front surface of the semiconductor substrate; and

forming a second passivation layer on a surface of the doped conductive layer.

30 [0019] In an implementation, the polishing a rear surface of the semiconductor substrate with an alkali solution includes: cleaning the rear surface of the semiconductor substrate with

the alkali solution having a mass fraction of 5% to 15% to remove porous silicon; dropping, by spraying, micro-liquid droplets of the alkali solution to the rear surface of the semiconductor substrate for roughening treatment, and then performing pre-cleaning with a hydrofluoric acid having a mass fraction of 5% to 10%; polishing the rear surface of the semiconductor substrate with a polishing liquid at a polishing temperature ranging from 70°C to 80°C for a polishing time less than 260 seconds, wherein the polishing liquid includes NaOH having a mass fraction of 1% to 15%, KOH having a mass fraction of 1% to 15% and an additive having a mass fraction of 0.51% to 2.5%; removing organic components in the polishing liquid by a mixture of potassium hydroxide having a mass fraction of 5% to 15% and hydrogen peroxide having a mass fraction of 15% to 40%; and washing and drying the polished semiconductor substrate.

[0020] In an implementation, the forming a tunnel oxide layer includes at least one of: (1) depositing the tunnel oxide layer on the first texture structure of the rear surface of the semiconductor substrate by a temperature change process and chemical vapor deposition; (2) during the deposition of the tunnel oxide layer, controlling a heating rate to range from 0.5°C/min to 3°C/min, a deposition temperature to range from 560°C to 620°C and a deposition time to range from 3 min to 10 min; (3) a deposition temperature of the tunnel oxide layer being lower than a deposition temperature of the polycrystalline silicon layer; (4) the tunnel oxide layer including at least one of a silicon oxide layer, an aluminum oxide layer, a silicon oxynitride layer, a molybdenum oxide layer or a hafnium oxide layer; and (5) the tunnel oxide layer having a thickness ranging from 0.8 nm to 2 nm.

BRIEF DESCRIPTION OF DRAWINGS

[0021] In order to better illustrate the technical solutions in embodiments of the present disclosure or the prior art, the accompanying drawings used in the description of the embodiments or the prior art will be briefly introduced below. It is apparent that, the accompanying drawings in the following description are only some embodiments of the present disclosure, and other drawings can be obtained by those of ordinary skill in the art from the provided drawings without creative efforts.

[0022] FIG. 1 is a schematic structural diagram of a solar cell according to an embodiment of the present disclosure.

[0023] FIG. 2 is an electron microscope picture of a second texture structure on a front surface of a semiconductor substrate of a solar cell according to an embodiment of the present disclosure.

[0024] FIG. 3 is an electron microscope picture of a first texture structure on a rear surface of the semiconductor substrate of the solar cell according to an embodiment of the present disclosure.

[0025] FIG. 4a is a schematic structural diagram of a first substructure in the first texture structure of the rear surface of the semiconductor substrate of the solar cell according to an embodiment of the present disclosure.

[0026] FIG. 4b is a schematic structural diagram of another first substructure in the first texture structure of the rear surface of the semiconductor substrate of the solar cell according to an embodiment of the present disclosure.

[0027] FIG. 5 is a schematic structural diagram of a substructure in the first texture structure of the rear surface of the semiconductor substrate of the solar cell according to an embodiment of the present disclosure.

[0028] FIG. 6 is a schematic structural diagram of a tunnel oxide layer on the first texture structure of the rear surface of the semiconductor substrate of the solar cell according to an embodiment of the present disclosure.

[0029] FIG. 7a is a schematic structural diagram of a photovoltaic module according to an embodiment of the present disclosure.

[0030] FIG. 7b is a top view of the photovoltaic module according to an embodiment of the present disclosure.

[0031] FIG. 8 is a schematic flowchart of a method for manufacturing a solar cell according to an embodiment of the present disclosure.

DESCRIPTION OF EMBODIMENTS

[0032] In order to better understand the technical solutions of the present disclosure, the

embodiments of the present disclosure are described in detail below with reference to the accompanying drawings.

[0033] It shall be made clear that the embodiments described are merely some embodiments rather than all of the embodiments of the present disclosure. All other
5 embodiments obtained by those of ordinary skill in the art without creative efforts based on the embodiments of the present disclosure shall fall within the protection scope of the present disclosure.

[0034] The terms used in the embodiments of the present disclosure are merely for the purpose of describing particular embodiments and are not intended to limit the present
10 disclosure. As used in the embodiments of the present disclosure and the appended claims, the singular forms of "a/an", "one", and "the" are also intended to include plural forms, unless otherwise clearly specified by the context.

[0035] It shall be understood that the term "and/or" used herein describes only an association relationship between associated objects and indicates that three relationships may
15 exist. For example, A and/or B may indicate the following three cases: only A exists, both A and B exist, and only B exists. In addition, the character "/" generally indicates an "or" relationship between the associated objects.

[0036] The TOPCon solar cell relies on a "tunnel effect" to passivate the rear surface. An existing TOPCon solar cell rear surface structure sequentially includes a semiconductor
20 substrate, a tunnel oxide layer, a doped conductive layer and a passivation layer on the rear surface from the inside out. Borosilicate glass (BSG) can be formed by inboron diffusion for an N-type TOPCon solar cell, which is more difficult to be removed than phosphorosilicate glass (PSG). Generally, the borosilicate glass is removed by an oxidizing mixed acid solution. The rear surface is polished after the surface is cleaned and dried. Currently, a state of the rear
25 surface of the semiconductor substrate after polishing has a certain effect on an ultra-thin tunnel oxide layer with a nanometer thickness, which easily leads to an increase in contact resistivity between the tunnel oxide layer and the semiconductor substrate, which in turn leads to the fluctuation of a fill factor of the solar cell, and finally affects the photoelectric conversion efficiency of the solar cell.

[0037] In a first aspect, the present disclosure provides a solar cell. As shown in FIG. 1,

the solar cell includes: a semiconductor substrate 10, a first passivation layer 20 located on a front surface of the semiconductor substrate 10, a tunnel oxide layer 30 located on the first texture structure of a rear surface of the semiconductor substrate 10, a doped conductive layer 40 located on a surface of the tunnel oxide layer 30, and a second passivation layer 50 located on a surface of the doped conductive layer 40. The rear surface of the semiconductor substrate 10 has a first texture structure 12, and the first texture structure 12 includes two or more first substructures that are at least partially stacked on one another. In a direction away from the rear surface and perpendicular to the rear surface, a distance between a top surface of the outermost first substructure and a top surface of the first substructure adjacent thereto is less than or equal to 2 μm . A one-dimensional size of the top surface of the outermost first substructure is less than or equal to 45 μm , a front surface of the semiconductor substrate 10 has a second texture structure 11, and the second texture structure 11 may include a pyramid-shaped microstructure. The doped conductive layer and the semiconductor substrate have doping elements of a same conductivity type.

[0038] The front surface of the semiconductor substrate 10 may refer to a light receiving surface, that is, a surface receiving solar rays. The rear surface of the semiconductor substrate 10 refers to a surface opposite the front surface. In some embodiments, the solar cell formed is a single-sided solar cell. The front surface may refer to a light receiving surface, and the rear surface may refer to a backlight surface. In some embodiments, the solar cell formed is a double-sided solar cell. The front surface and the rear surface may both be light receiving surfaces.

[0039] As an optional technical solution of the present disclosure, the semiconductor substrate 10 is an N-type crystalline silicon substrate (or silicon wafer). A P-type doped layer may be formed on the front surface of the semiconductor substrate by one or more of the processes of high temperature diffusion, slurry doping, and ion implantation, so as to form a PN junction in the semiconductor substrate 10. In some embodiments, the semiconductor substrate 10 may be one of a monocrystalline silicon substrate, a polycrystalline silicon substrate, a microcrystalline silicon substrate and a silicon carbide substrate.

[0040] In some embodiments, the P-type doped layer is a boron-doped diffusion layer. The boron-doped diffusion layer is a P-type doped layer (i.e., P⁺ layer) formed by using a

boron source to diffuse boron atoms to a certain depth on the front surface through a diffusion process. For example, the boron source may be liquid boron tribromide.

[0041] In some embodiments, as shown in FIG. 2, the front surface of the semiconductor substrate 10 has a second texture structure 11, and the second texture structure 11 includes a pyramid-shaped microstructure 111. The pyramid-shaped microstructure 111 may have a structure of a tetrahedron, a substantially tetrahedron, a pentahedron, a substantially pentahedron, or the like. The pyramid-shaped microstructure 111 may be formed by texturing the semiconductor substrate. The texturing process may be chemical etching, laser etching, a mechanical process, plasma etching, or the like. The pyramid-shaped microstructure enables a metal paste to better fill the microstructure when the metal paste forms an electrode by screen printing, which obtains better electrode contact, can effectively reduce series resistance of the solar cell, and improves the fill factor.

[0042] In some embodiments, the pyramid-shaped microstructure 111 includes a top away from the front surface of the semiconductor substrate and a bottom close to the front surface of the semiconductor substrate, and in a direction away from the front surface and perpendicular to the front surface, a distance (or height) between the top and the bottom of the pyramid-shaped microstructure is less than or equal to 5 μm . For example, the distance ranges from 2 μm to 5 μm . The distance may be 2 μm , 2.5 μm , 2.8 μm , 3 μm , 3.5 μm , 3.8 μm , 4 μm , 4.2 μm , 4.5 μm , 4.8 μm , 5 μm or the like. When the distance range of the pyramid-shaped microstructure 111 is controlled within 5 μm , for example, 2 μm to 5 μm , the pyramid-shaped microstructure 111 has the characteristics of low reflection, low recombination and easy filling, so that the photoelectric conversion efficiency of the solar cell can be improved.

[0043] It may be understood that a number of the pyramid-shaped microstructure formed on the front surface cannot be exhausted due to anisotropy of crystal orientation of silicon crystal on the front surface. The distance of the pyramid-shaped microstructure 111 referred to herein may be a distance between a convex highest point of the top and a concave lowest point of the pyramid-shaped microstructure 111 randomly selected in a specific region. For example, the distance of the pyramid-shaped microstructure 111 may be determined by measuring a surface shape of the semiconductor substrate by using an atomic force microscope (AFM). For example, a scanning range of 40 μm ×40 μm is selected from the front

surface, the front surface of the semiconductor substrate is scanned within the selected range by using the atomic force microscope, a profile size of the pyramid-shaped microstructure on the front surface is measured, and a height value h is calculated. The convex highest point h_a of the top of the pyramid-shaped microstructure is selected from the measured profile size (an AFM image), the lowest point of the bottom corresponding to the top is h_b , and $h=h_a-h_b$ is obtained. In other implementations, heights of a plurality of pyramid-shaped microstructures in the second texture structure are randomly collected, and an average value is calculated. The average value is defined as the height of the pyramid-shaped microstructure. For example, 4 pyramid-shaped microstructures 111 are randomly selected, with heights of h_1 , h_2 , h_3 and h_4 respectively, and then a height value of the pyramid-shaped microstructure 111 is $(h_1+h_2+h_3+h_4)/4$. That is, an average distance of a plurality of pyramid-shaped microstructures 111 can be regarded as a distance of the pyramid-shaped microstructure on the front surface, which is configured to represent a texture feature of the front surface.

[0044] As an optional technical solution of the present disclosure, the first passivation layer 20 has a stacking structure of at least one or more of a silicon oxide layer, a silicon nitride layer, an aluminum oxide layer and a silicon oxynitride layer.

[0045] In some embodiments, the first passivation layer 20 has a thickness ranging from 10 nm to 120 nm, which may be 10 nm, 20 nm, 30 nm, 40 nm, 50 nm, 60 nm, 70 nm, 80 nm, 90 nm, 100 nm, 120 nm or the like, and may also be other values in the range, which is not limited herein.

[0046] In an embodiment, the first passivation layer 20 has a stacked passivation structure of an aluminum oxide layer and a silicon nitride layer. The aluminum oxide layer is arranged on the front surface of the semiconductor substrate 10. The silicon nitride layer is arranged on a surface of the aluminum oxide layer. For example, the aluminum oxide layer has a thickness ranging from 2 nm to 10 nm, and the aluminum oxide layer has a refractive index ranging from 1.5 to 1.8. The silicon nitride layer has a thickness ranging from 50 nm to 110 nm, and the silicon nitride layer has a refractive index ranging from 1.65 to 2.25. The first passivation layer 20 has an overall refractive index ranging from 1.9 to 2.0. The aluminum oxide layer or silicon nitride layer may include a plurality of sublayers. For example, the silicon nitride layer is composed of 2 to 5 silicon nitride sublayers.

[0047] In an embodiment, the first passivation layer has a stacked passivation structure of an aluminum oxide layer, a silicon nitride layer and a silicon oxynitride layer sequentially stacked. The aluminum oxide layer has a thickness ranging from 2 nm to 10 nm, the aluminum oxide layer has a refractive index ranging from 1.5 to 1.8, the silicon nitride layer has a thickness ranging from 40 nm to 80 nm, the silicon nitride layer has a refractive index ranging from 1.9 to 2.3, the silicon oxynitride layer has a thickness ranging from 10 nm to 60 nm, and the silicon oxynitride layer has a refractive index ranging from 1.5 to 1.75.

[0048] Further, the rear surface of the semiconductor substrate 10 has a first texture structure 12. The first texture structure 12 may be formed by alkali polishing.

[0049] As an optional technical solution of the present disclosure, FIG. 3 is an electron microscope picture of the first texture structure 12 on the rear surface of the semiconductor substrate of the solar cell according to an embodiment of the present disclosure. As shown in FIG. 3, the first texture structure 12 includes two or more first substructures 121 at least partially stacked on one another. The first texture structure 12 presents a non-pyramid-shaped microstructure profile. For example, the first texture structure may present a substantially "step" profile, and the first substructure 121 may be regarded as a stair of the "step".

[0050] FIG. 4a is a schematic diagram of three layers of first substructures partially stacked, and FIG. 4b is a schematic diagram of two layers of first substructures partially stacked. Reference sign 121a denotes the outermost first substructure in the first texture structure away from the rear surface, and 121b denotes an adjacent first substructure.

[0051] For the two or more first substructures 121 at least partially stacked on one another, in a direction away from the rear surface and perpendicular to the rear surface (which may also be understood as "in a stacking direction"), a distance H between a top surface of the outermost first substructure 121a and a top surface of the first substructure 121b adjacent thereto is less than or equal to 2 μm , which may be 2 μm , 1.8 μm , 1.5 μm , 1.2 μm , 1.1 μm , 1.0 μm , 0.8 μm , 0.5 μm , 0.3 μm , 0.2 μm , 0.1 μm or the like. When the distance H is more than 2 μm , the roughness of the first texture structure is excessively large, and the thickness of the tunnel oxide layer 30 formed on the first texture structure is larger, which bring adverse effects to the formation of the tunnel oxide layer with high density and high uniformity, thereby affecting tunneling and passivation effects of the tunnel oxide layer 30. If the

roughness of the first texture structure is excessively small, the thickness of the tunnel oxide layer formed on the first texture structure is smaller, which brings adverse effects to the contact with an electrode paste. In an embodiment, in the direction away from the rear surface and perpendicular to the rear surface, the distance between the top surface of the outermost first substructure 121a and the top surface of the first substructure 121b adjacent thereto ranges from 0.3 μm to 1.2 μm .

[0052] It should be noted that, when the three layers of first substructures are stacked, a distance H between a top surface of the first substructure 121a in any layer and a top surface of the first substructure 121b in an adjacent layer is less than or equal to 2 μm .

[0053] It is appreciated that, the distance between the top surface of the outermost first substructure 121a and the top surface of the first substructure 121b adjacent thereto is controlled to be less than or equal to 2 μm , so that the roughness of the first texture structure is controlled within a desired range, which helps to improve the uniformity of the tunnel oxide layer formed on the first texture structure, ensure better performance of the tunnel oxide layer formed, further inhibit a high local phosphorus concentration caused by phosphorous diffusion, reduce contact resistivity, improve the open-circuit voltage of the solar cell, and improve the fill factor and photoelectric conversion efficiency.

[0054] A one-dimensional size L of the top surface of the outermost first substructure 121a is less than or equal to 45 μm , that is, $0 < L \leq 45 \mu\text{m}$. In an embodiment, the one-dimensional size L is within a range of 2 μm to 45 μm . Here, the one-dimensional size L of the top surface may be a length, width, diagonal length or circular diameter of the surface, which is not limited herein. In some embodiments, the one-dimensional size may be an average value of one-dimensional sizes of top surfaces of a plurality of outermost first substructures within a preset range region of the rear surface of the substrate. An average one-dimensional size of the top surface of the outermost first substructure may be 2 μm , 5 μm , 8 μm , 12 μm , 15 μm , 18 μm , 20 μm , 25 μm , 28 μm , 30 μm , 35 μm , 40 μm , 42 μm , 40 μm , 45 μm or the like. For example, an average one-dimensional size of the top surface of the outermost first substructure ranges from 10 μm to 15 μm .

[0055] In an embodiment, as shown in FIG. 3, the first texture structure further includes two or more adjacent second substructures 122 that are not stacked, and a one-dimensional

size L of a top surface of the second substructure 122 away from the rear surface is less than or equal to 45 μm , that is, $0 < L \leq 45 \mu\text{m}$. In an embodiment, the one-dimensional size L of the second substructure 122 is within a range of 2 μm to 45 μm , which may be 2 μm , 5 μm , 8 μm , 12 μm , 15 μm , 18 μm , 20 μm , 25 μm , 28 μm , 30 μm , 32 μm , 35 μm , 45 μm or the like.

5 **[0056]** Different from the pyramid-shaped microstructure of the front surface, the top surface of the first substructure and/or the top surface of the second substructure of the rear surface is a polygonal plane. The polygonal plane is in a shape of at least one of a diamond, a square, a trapezoid, a substantially diamond, a substantially square and a substantially trapezoid. It shall be understood that, during actual manufacturing process, the top surface of
10 the first substructure or second substructure presents a profile of an irregular polygon plane, and wholly presents a profile of a substantially diamond, a square and a trapezoid.

[0057] In some examples, the manufacturing of subsequent passivation film layers, such as the first passivation layer 20, the tunnel oxide layer 30 and the doped conductive layer 40, may damage original structures of the second texture structure and the first texture structure to
15 some extent. For example, in a mass-produced solar cell, the second texture structure may also include a small number of non-pyramid-shaped microstructures formed due to the damages to the spires of the pyramid-shaped microstructures.

[0058] In some examples, when a texture size representing the second texture structure or the first texture structure of the solar cell is measured, such as the one-dimensional size of the
20 top surface of the first substructure and the distance between the surfaces of adjacent first substructures, surfaces of the film layers are directly measured for calibration through a test instrument (an optical microscope, an atomic force microscope, a scanning electron microscope, a transmission electron microscope, or the like). In one case, since the thickness of the film layer is in nanoscale, it can be obtained directly using film layer measurement data
25 corresponding to the second texture structure or the first texture structure, and the film layer measurement data is a sum of the thickness of the film layer and a texture size. In another case, it can also be obtained by subtracting film layer thickness data from the film layer measurement data. The above measurement means are only examples and are not limited in the present disclosure.

30 **[0059]** As shown in FIG. 1 and FIG. 6, the tunnel oxide layer 30 located on the first

texture structure 12 of the rear surface of the semiconductor substrate 10 may have a stacking structure of one or more of a silicon oxide layer, an aluminum oxide layer, a silicon oxynitride layer, a molybdenum oxide layer and a hafnium oxide layer. In other embodiments, the tunnel oxide layer 30 may also be an oxygen-containing silicon nitride layer, an oxygen-containing silicon carbide layer or the like. The tunnel oxide layer 30 has a thickness ranging from 0.8 nm to 2 nm. For example, the thickness of the tunnel oxide layer 30 is 0.8 nm, 0.9 nm, 1.0 nm, 1.2 nm, 1.4 nm, 1.6 nm, 1.8 nm, 2 nm or the like. The thickness of the tunnel oxide layer 30 refers to a thickness of the tunnel oxide layer relative to a formation surface. The thickness of the tunnel oxide layer 30 formed on the first texture structure can be calculated by taking a normal direction of an inclined surface of the substructure as a thickness direction and observing a cross section thereof. When the thickness of the tunnel oxide layer 30 is excessively large, it may bring adverse effects to reducing the contact resistance of the tunnel oxide layer. A decrease in the fill factor caused by the contact resistance can be inhibited by controlling the thickness of the tunnel oxide layer.

[0060] In an embodiment, a band gap width of the tunnel oxide layer 30 is greater than 3.0 eV, and it is generally difficult to transport carriers through the tunnel oxide layer 30 by thermal emission. However, the tunnel oxide layer 30 is very thin and carriers can pass through the tunnel oxide layer 30 through a tunnel effect, so the tunnel oxide layer having a thickness within a range of 0.8 nm to 2nm does not block the transport of most carriers. As the thickness of the tunnel oxide layer gradually increases, the tunnel effect of most carriers is affected, and it is difficult to transport the carriers through the tunnel oxide layer 30, and the photoelectric conversion efficiency of the solar cell may gradually decrease. When the thickness of the tunnel oxide layer is excessively small, the tunnel oxide layer cannot perform the passivation effect. As a result, in an embodiment, the tunnel oxide layer 30 is a silicon oxide layer, and the tunnel oxide layer 30 has a thickness ranging from 0.8 nm to 1.5 nm.

[0061] As an optional technical solution of the present disclosure, as shown in FIG. 6, a thickness D1 of the tunnel oxide layer on the top surface of the outermost first substructure is less than a thickness D2 of the tunnel oxide layer on a side surface of the outermost first substructure. For example, a thickness difference (D2-D1) between the tunnel oxide layer on the top surface of the outermost first substructure and the tunnel oxide layer on a side surface

of the outermost substructure is less than or equal to 0.15 nm. The thickness difference may be 0.14 nm, 0.13 nm, 0.12 nm, 0.11 nm, 0.10 nm, 0.09 nm, 0.08 nm, 0.07 nm, 0.06 nm, 0.05 nm, 0.04 nm or the like. When the tunnel oxide layer on the top surface of the outermost first substructure and the tunnel oxide layer on the side surface of the outermost substructure are
5 excessively large, the thickness of the tunnel oxide layer has poor uniformity, a current density of the solar cell is easily affected, and the open-circuit voltage of the solar cell decreases.

[0062] In some embodiments, texture structures with different profiles are arranged on the front and rear surfaces of the semiconductor substrate, a pyramidal texture structure is formed
10 on the front surface, and a non-pyramidal texture structure is formed on the rear surface, so that the solar cell formed has a light trap structure at different levels, which increases an effective contact area of light. Moreover, for the first texture structure formed on the rear surface, the distance between the top surface of the outermost first substructure and the top surface of the first substructure adjacent thereto is controlled within 2 μm , which helps to
15 reduce a pinhole in the tunnel oxide layer and then improves the density and uniformity of the tunnel oxide layer, further inhibit a high local doping concentration of the doped conductive layer on the surface of the tunnel oxide layer, reduce contact resistivity, improve the open-circuit voltage of the solar cell, and improve the fill factor and photoelectric conversion efficiency.

[0063] In some embodiments, the doped conductive layer 40 may be a doped polycrystalline silicon layer, a doped microcrystalline silicon layer or a doped amorphous silicon layer. The doped conductive layer 40 and the semiconductor substrate have doping elements of a same conductivity type.
20

[0064] When the semiconductor substrate 10 is an N-type monocrystalline silicon, the doped conductive layer 40 is an N-type doped polycrystalline silicon layer, an N-type doped microcrystalline silicon layer or an N-type doped amorphous silicon layer, and the doping element may be an N-type doping element such as phosphorus.
25

[0065] In some embodiments, the doped conductive layer 40 has a thickness ranging from 60 nm to 200 nm. For example, as an N-type doped polycrystalline silicon layer, the doped
30 conductive layer 40 may have a refractive index ranging from 3.5 to 4.5.

[0066] As an optional technical solution of the present disclosure, the second passivation layer 50 includes at least one of a silicon nitride layer, a silicon oxide layer and a silicon oxynitride layer. The second passivation layer 50 has a thickness ranging from 70 nm to 120 nm. For example, the second passivation layer 50 is a silicon nitride layer. The silicon nitride layer has a low silicon to nitrogen ratio, and the silicon nitride layer has a refractive index ranging from 1.7 to 2.1, which may be 1.7, 1.8, 1.9, 2.0, 2.1 or the like, and may also be other values in the above range, and is not limited herein. The refractive index of the silicon nitride layer is controlled to enable the silicon nitride layer to have low silicon to nitrogen ratio, so that contact resistivity can be reduced during metallization of the second passivation layer 50 formed, so as to further reduce the contact resistivity of the solar cell.

[0067] In some embodiments, when the second passivation layer 50 has a stacking structure of a silicon nitride layer and a silicon oxide layer or a stacking structure of a silicon nitride layer and a silicon oxynitride layer, the silicon nitride layer is located on a surface of the doped conductive layer, and the silicon oxide layer or the silicon oxynitride layer is located on a surface of the silicon nitride layer.

[0068] Further, the solar cell further includes a first electrode 60 and a second electrode 70. The first electrode 60 passes through the first passivation layer 20 to form ohmic contact with the P-type doped layer (for example, the boron-doped diffusion layer) on the front surface of the semiconductor substrate 10. The second electrode 70 passes through the second passivation layer 50 to form ohmic contact with the doped conductive layer 40. The doped conductive layer 40 and the tunnel oxide layer 30 form a passivated contact structure. The first electrode 60 and the second electrode 70 may be formed by sintering a metal conductive paste coated on surfaces of the first passivation layer and the second passivation layer. In some embodiments, the first electrode 60 or the second electrode 70 is made of a metal material such as silver, aluminum, copper or nickel.

[0069] For the solar cell formed as shown in FIG. 1, that is, the second texture structure of the pyramid-shaped microstructure formed on the front surface of the semiconductor substrate 10, the first texture structure of the non-pyramid-shaped microstructure formed on the rear surface of the semiconductor substrate, the first passivation layer 20 (for example, a stacked passivation structure of an aluminum oxide layer and a silicon nitride layer) formed on the

second texture structure, and the tunnel oxide layer 30, the doped conductive layer 40 and the second passivation layer 50 (for example, a silicon nitride layer) matching one another formed on the first texture structure. The solar cell structure formed as above has higher photoelectric conversion efficiency.

5 **[0070]** In a second aspect, an embodiment of the present disclosure provides a photovoltaic module including a plurality of solar cell strings.

[0071] As shown in FIG. 7a and FIG. 7b, the photovoltaic module includes a first cover plate 1, a first packaging adhesive layer 2, a solar cell string 3, a second packaging layer 4 and a second cover plate 5.

10 **[0072]** The solar cell string 3 includes a plurality of solar cells (the solar cell as shown in FIG. 1) that are connected through a conductive band (not shown). The solar cells may be connected by partial stacking or by splicing.

[0073] The first cover plate 1 and the second cover plate 5 are transparent or opaque cover plates, such as glass cover plates or plastic cover plates.

15 **[0074]** Two sides of the first packaging adhesive layer 2 contact and are bonded to the first cover plate 1 and the solar cells 3, respectively, and two sides of the second packaging layer 2 are contact and are bonded to the second cover plate 1 and the solar cells 3, respectively. The first packaging adhesive layer 2 and the second packaging layer 4 may be ethylene-vinyl acetate copolymer (EVA) film, a polyolefin elastomer (POE) film or a
20 polyethylene terephthalate (PET) film, respectively.

[0075] Side edges of the photovoltaic module may also be completely packaged, that is, the side edges of the photovoltaic module are fully packaged with a packaging adhesive tape to prevent a stacking deviation during the stacking of the photovoltaic module.

[0076] Further, the photovoltaic module (the photovoltaic module 100 shown in FIG. 7b)
25 further includes an edge sealing member 6 fixedly packaged to a partial edge of the photovoltaic module. As shown in FIG. 7b, the edge sealing member 6 is fixedly packaged to an edge of the photovoltaic module near a corner. The edge sealing member 6 may be a high-temperature resistant tape. The high-temperature resistant tape has excellent high-temperature resistance and may not decompose or fall off during the stacking, which can
30 ensure the reliable packaging of the photovoltaic module. Two ends of the high-temperature

resistant tape are fixed to the second cover plate 5 and the first cover plate 1, respectively. The two ends of the high-temperature resistant tape may be bonded to the second cover 5 and the first cover 1, respectively, and the middle thereof can limit a side edge of the photovoltaic module to prevent a stacking deviation of the photovoltaic module during the stacking.

5 **[0077]** In a third aspect, the present disclosure further provides a method for manufacturing a solar cell for manufacturing the solar cell described above. As shown in FIG. 8, the method includes the following steps.

10 **[0078]** In S10, a semiconductor substrate is textured, and a second texture structure is formed on a front surface of the semiconductor substrate, the second texture structure includes a pyramid-shaped microstructure.

15 **[0079]** In S20, the front surface of the textured semiconductor substrate is doped to form a doped layer.

20 **[0080]** In S30, a rear surface of the semiconductor substrate is polished with an alkali solution, so that a first texture structure is formed on the rear surface of the semiconductor substrate, the first texture structure includes two or more first substructures at least partially stacked, for the two or more first substructures at least partially stacked, in a direction away from the rear surface and perpendicular to the rear surface, a distance between a top surface of the outermost first substructure and a top surface of the first substructure adjacent thereto is less than or equal to 2 μm , and a one-dimensional size of the top surface of the outermost first substructure is less than or equal to 45 μm .

25 **[0081]** In S40, a tunnel oxide layer is formed on the first texture structure of the rear surface of the semiconductor substrate.

30 **[0082]** In S50, a polycrystalline silicon layer is formed on a surface of the tunnel oxide layer, and the polycrystalline silicon layer is doped to form a doped conductive layer, the doped conductive layer and the semiconductor substrate having doping elements of a same conductivity type.

35 **[0083]** In S60, a first passivation layer is formed on the front surface of the semiconductor substrate.

40 **[0084]** In S70, a second passivation layer is formed on a surface of the doped conductive layer.

[0085] In the above solution, the rear surface of the semiconductor substrate is polished with an alkali solution, so that texture structures with different profiles are formed on the front and rear surfaces of the semiconductor substrate. A pyramidal texture structure is formed on the front surface, and a non-pyramidal texture structure is formed on the rear surface, so that
5 the solar cell formed has a light trap structure at different levels, which increases an effective contact area of light. Moreover, for the first texture structure formed on the rear surface, the distance between the top surface of the outermost first substructure and the top surface of the first substructure adjacent thereto is controlled within 2 μm , which helps to reduce a pinhole in the tunnel oxide layer and then improve the density and uniformity of the tunnel oxide layer,
10 further inhibit a high local doping concentration of the doped conductive layer on the surface of the tunnel oxide layer, reduce contact resistivity, improve the open-circuit voltage of the solar cell, and improve the fill factor and photoelectric conversion efficiency.

[0086] The solution is described in detail as follows.

[0087] In S10, a semiconductor substrate is textured, and a second texture structure is
15 formed on a front surface of the semiconductor substrate, the second texture structure includes a pyramid-shaped microstructure.

[0088] The semiconductor substrate may be a crystalline silicon substrate, which is, for example, one of a polycrystalline silicon substrate, a monocrystalline silicon substrate, a microcrystalline silicon substrate and a silicon carbide substrate. A specific type of the
20 semiconductor substrate is not limited in the embodiments of the present disclosure. In some embodiments, the semiconductor substrate is an N-type crystalline silicon substrate (or silicon wafer). The semiconductor substrate has a thickness ranging from 60 μm to 240 μm , which may be 60 μm , 80 μm , 90 μm , 100 μm , 120 μm , 150 μm , 200 μm , 240 μm or the like. The doping elements of the semiconductor substrate may be phosphorus, nitrogen and the like.

[0089] It shall be noted that the present disclosure does not limit how the texturing is performed. For example, an N-type substrate may be textured using, but not limited to, a wet texturing process. When the N-type semiconductor substrate is an N-type crystalline silicon substrate, the texturing may be performed using an alkaline solution such as a potassium hydroxide solution. Since the corrosion of the NaOH solution is anisotropic, a
30 pyramid-shaped microstructure can be manufactured.

[0090] As shown in FIG. 2, the front surface of the semiconductor substrate 10 has a second texture structure 11, and the second texture structure 11 includes a pyramid-shaped microstructure 111. The pyramid-shaped microstructure 111 may have a structure of a tetrahedron, a substantially tetrahedron, a pentahedron, a substantially pentahedron, or the like.

5 The pyramid-shaped microstructure 111 may be formed by texturing the semiconductor substrate. The texturing may be chemical etching, laser etching, a mechanical process, plasma etching, or the like. The pyramid-shaped microstructure enables a metal paste to better fill the microstructure when the metal paste forms an electrode by screen printing, to obtain better electrode contact, which can effectively reduce series resistance of the solar cell, and improve
10 the fill factor.

[0091] In S20, the front surface of the textured semiconductor substrate is doped to form a doped layer.

[0092] In an embodiment, when the semiconductor substrate 10 is an N-type substrate, a P-type doped layer may be formed on the front surface of the semiconductor substrate by one
15 or more of the processes of high temperature diffusion, slurry doping, and ion implantation, so as to form a PN junction in the semiconductor substrate 10.

[0093] In some embodiments, the P-type doped layer is a boron-doped diffusion layer. The boron-doped diffusion layer is a P-type doped layer (i.e., P⁺ layer) formed by using a boron source to diffuse boron atoms to a certain depth on the front surface through a diffusion
20 process. For example, the boron source may be liquid boron tribromide. A microcrystalline silicon phase of the substrate after boron diffusion treatment is transformed into a polycrystalline silicon phase. Since the surface of the semiconductor substrate has a high concentration of boron, a borosilicate glass (BSG) layer is generally formed.

[0094] Further, in S30, prior to the step of polishing a rear surface of the semiconductor substrate with an alkali solution, the method further includes: removing the borosilicate glass
25 layer from the rear surface of the semiconductor substrate with a prepared mixed acid, the mixed acid includes hydrogen fluoride having a mass fraction of 0.1% to 10%, sulfuric acid having a mass fraction of 10% to 20% and nitric acid having a mass fraction of 25% to 50%; and washing and drying the rear surface of the semiconductor substrate after pickling.

30 **[0095]** During the boron diffusion treatment, the rear surface of the semiconductor

substrate is coated to form part of the borosilicate glass, which shall be removed. It shall be noted that a porous structure may appear on the rear surface of the semiconductor substrate after pickling.

5 **[0096]** In an embodiment, a pickling time ranges from 10 seconds to 180 seconds, and a pickling temperature ranges from 7°C to 20°C, that is, the borosilicate glass on the rear surface of the semiconductor substrate is removed by pickling at room temperature to expose a body of the semiconductor substrate.

10 **[0097]** In S30, the rear surface of the semiconductor substrate is polished with the alkali solution, so that a first texture structure is formed on the rear surface of the semiconductor substrate.

[0098] In an embodiment, the rear surface of the semiconductor substrate is cleaned with the alkali solution having a mass fraction of 5% to 15% to remove porous silicon.

15 **[0099]** Micro-liquid droplets of the alkali solution are dropped by spraying to the rear surface of the semiconductor substrate for roughening treatment, and then pre-cleaning is performed with a hydrofluoric acid having a mass fraction of 5% to 10%.

[00100] The rear surface of the semiconductor substrate is polished with a polishing liquid at a polishing temperature ranging from 70°C to 80°C for a polishing time less than 260 seconds. The polishing liquid includes NaOH having a mass fraction of 1% to 15%, KOH having a mass fraction of 1% to 15% and an additive having a mass fraction of 0.5% to 2.5%.
20 Here, the polishing liquid may be designated as the etching solution.

[00101] Organic components in the etching solution are removed by a mixture of potassium hydroxide having a mass fraction of 5% to 15% and hydrogen peroxide having a mass fraction of 15% to 40%.

[00102] The polished semiconductor substrate is washed and dried.

25 **[00103]** In some embodiments, when the rear surface is polished, the borosilicate glass layer on the front surface of the semiconductor substrate shall be protected, for example, by a mask.

[00104] In an embodiment, due to the low boron concentration on the rear surface of the semiconductor substrate, the etching efficiency can be improved effectively by using the
30 alkali solution. The alkali solutions contain organic bases and/or inorganic bases. The

inorganic bases may be NaOH, KOH, Ga(OH)₂, NH₃·H₂O, and the organic bases may be triethylamine, nitrophenol, pyridine, quinine, colchicine, and the like. The additive in the polishing liquid may be a buffer solution composed of sodium sulfonate, maleic anhydride, alkyl glycoside, and the like.

5 **[00105]** The polishing temperature may be 70°C, 72°C, 74°C, 75°C, 78°C, 79°C, 80°C or the like, and the polishing time may be 250 seconds, 240 seconds, 230 seconds, 220 seconds, 200 seconds, 180 seconds, 160 seconds, 140 seconds, 120 seconds, 100 seconds, 80 seconds or the like, which may also be other values in the above ranges.

10 **[00106]** In some embodiments, a polishing weight loss of the semiconductor substrate is less than 0.3 g.

15 **[00107]** A shape of the substructure in the first texture structure after polishing may be adjusted by controlling the polishing time and the polishing temperature, so that in the two or more first substructures at least partially stacked a distance between a top surface of the outermost first substructure and a top surface of the first substructure adjacent thereto is less than or equal to 2 μm in a direction away from the rear surface and perpendicular to the rear surface, so as to increase the roughness of the rear surface of the semiconductor substrate.

15 **[00108]** In some embodiments, the first texture structure including a non-pyramid-shaped microstructure may be formed by hot-air drying the surface of the semiconductor substrate.

20 **[00109]** As an optional technical solution of the present disclosure, FIG. 3 is an electron microscope picture of the first texture structure 12 on the rear surface of the semiconductor substrate of the solar cell according to an embodiment of the present disclosure. As shown in FIG. 3, the first texture structure 12 includes two or more first substructures 121 at least partially stacked.

25 **[00110]** FIG. 4a is a schematic diagram of three layers of first substructures partially stacked, and FIG. 4b is a schematic diagram of two layers of first substructures partially stacked. Reference sign 121a denotes the outermost first substructure in the first texture structure away from the rear surface, and 121b denotes the innermost first substructure in the first texture structure close to the rear surface.

30 **[00111]** For the two or more first substructures 121 at least partially stacked, in the direction away from the rear surface and perpendicular to the rear surface, a distance H

between a top surface of the outermost first substructure 121a and a top surface of the first substructure 121b adjacent thereto is less than or equal to 2 μm , which may be 2 μm , 1.8 μm , 1.5 μm , 1.2 μm , 1.1 μm , 1.0 μm , 0.8 μm , 0.5 μm , 0.3 μm , 0.2 μm , 0.1 μm or the like. When the distance H is more than 2 μm , the roughness of the first texture structure is excessively large, and the thickness of the tunnel oxide layer 30 formed on the first texture structure is larger, which brings adverse effects to the formation of the tunnel oxide layer with high density and high uniformity, thereby affecting tunneling and passivation effects of the tunnel oxide layer 30. If the roughness of the first texture structure is excessively small, the thickness of the tunnel oxide layer formed on the first texture structure is smaller, which brings adverse effects to the contact with an electrode paste. As a result, in an embodiment, in the direction away from the rear surface and perpendicular to the rear surface, the distance between the top surface of the outermost first substructure 121a and the top surface of the first substructure 121b adjacent thereto ranges from 0.3 μm to 1.2 μm .

[00112] It shall be noted that, when the three layers of first substructures are stacked, a distance H between a top surface of the first substructure 121a in any layer and a top surface of the first substructure 121b in an adjacent layer is less than or equal to 2 μm .

[00113] The distance between the top surface of the outermost first substructure 121a and the top surface of the first substructure 121b adjacent thereto is controlled to be less than or equal to 2 μm , so that the roughness of the first texture structure is controlled within a desired range, which helps to improve the uniformity of the tunnel oxide layer formed on the first texture structure, ensure better performance of the tunnel oxide layer formed, further inhibit a high local phosphorus concentration caused by phosphorous diffusion, reduce contact resistivity, improve the open-circuit voltage of the solar cell, and improve the fill factor and photoelectric conversion efficiency.

[00114] A one-dimensional size L of the top surface of the outermost first substructure 121a is less than or equal to 45 μm . In an embodiment, the one-dimensional size L is within a range of 2 μm to 45 μm . Here, the one-dimensional size L of the top surface may be a length, width, diagonal length or circular diameter of the surface, which is not limited herein. In some embodiments, the one-dimensional size may be an average value of one-dimensional sizes of top surfaces of a plurality of outermost first substructures within a preset range region of the

rear surface of the substrate. An average one-dimensional size of the top surface of the outermost first substructure may be 2 μm , 5 μm , 8 μm , 12 μm , 15 μm , 18 μm , 20 μm , 25 μm , 28 μm , 30 μm , 35 μm , 40 μm , 42 μm , 40 μm , 45 μm or the like. For example, an average one-dimensional size of the top surface of the outermost first substructure ranges from 10 μm to 15 μm .

[00115] In an embodiment, as shown in FIG. 3, the first texture structure further includes two or more adjacent second substructures 122 not stacked, and a one-dimensional size L of a top surface of the second substructure 122 away from the rear surface is less than or equal to 45 μm . In an embodiment, the one-dimensional size L of the first substructure 122 is within a range of 2 μm to 45 μm , which may be 2 μm , 5 μm , 8 μm , 12 μm , 15 μm , 18 μm , 20 μm , 25 μm , 28 μm , 30 μm , 32 μm , 35 μm , 45 μm or the like.

[00116] Different from the typical pyramid-shaped microstructure of the front surface, the top surface of the first substructure and/or the top surface of the second substructure of the rear surface is a polygonal plane. The polygonal plane is in a shape of at least one of a diamond, a square, a trapezoid, a substantially diamond, a substantially square and a substantially trapezoid. It shall be understood that, during actual manufacturing, the top surface of the first substructure or second substructure presents a profile of an irregular polygon plane, and presents in entirety a profile of a substantially diamond, a square and a trapezoid.

[00117] In S40, a tunnel oxide layer is formed on the first texture structure of the rear surface of the semiconductor substrate.

[00118] In some embodiments, the rear surface of the semiconductor substrate may be etched and then treated by ozone oxidation, high temperature thermal oxidation, nitric acid oxidation, chemical vapor deposition and low-pressure chemical vapor deposition to form the tunnel oxide layer 30.

[00119] In some embodiments, the tunnel oxide layer 30 is deposited on the rear surface of the semiconductor substrate by a temperature change process and chemical vapor deposition. During the deposition, a heating rate is controlled to range from 0.5°C/min to 3°C/min, a deposition temperature is controlled to range from 560°C to 620°C and a deposition time is controlled to range from 3 min to 10 min.

[00120] For example, during the deposition, the deposition temperature may be 560°C, 570°C, 580°C, 590°C, 600°C, 610°C, 615°C, 620°C or the like, the deposition time may be 3 min, 4 min, 5 min, 6 min, 7 min, 8 min, 9 min, 10 min or the like, and the heating rate may be 0.5 °C/min, 0.8 °C/min, 1.0 °C/min, 1.2 °C/min, 1.5 °C/min, 2.0 °C/min, 2.5 °C/min, 3 °C/min or the like, which may also be other values in the above ranges and are not limited herein.

[00121] The tunnel oxide layer 30 is deposited on the rear surface of the semiconductor substrate by low-pressure chemical vapor deposition, which can reduce the influence of a high local doping concentration of the thinner tunnel oxide layer 30 in subsequent high temperature doping treatment and reduce the fluctuation of the open-circuit voltage. The tunnel oxide layer 30 formed by the temperature change process and low-pressure chemical vapor deposition can increase the open-circuit voltage of the solar cell by 4 mV to 6 mV.

[00122] The tunnel oxide layer 30 may have a stacking structure of one or more of a silicon oxide layer, an aluminum oxide layer, a silicon oxynitride layer, a molybdenum oxide layer and a hafnium oxide layer. In other embodiments, the tunnel oxide layer 30 may also be an oxygen-containing silicon nitride layer, an oxygen-containing silicon carbide layer or the like. The tunnel oxide layer 30 has a thickness ranging from 0.8 nm to 2 nm. For example, the thickness of the tunnel oxide layer 30 is 0.8 nm, 0.9 nm, 1.0 nm, 1.2 nm, 1.4 nm, 1.6 nm, 1.8 nm, 2 nm or the like. The thickness of the tunnel oxide layer 30 refers to a thickness of the tunnel oxide layer relative to a formation surface. The thickness of the tunnel oxide layer 30 formed on the first texture structure can be calculated by taking a normal direction of an inclined surface of the substructure as a thickness direction and observing a cross section thereof. When the thickness of the tunnel oxide layer 30 is excessively large, it brings adverse effects to reducing the contact resistance of the tunnel oxide layer. A decrease in the fill factor caused by the contact resistance can be inhibited by controlling the thickness of the tunnel oxide layer.

[00123] A band gap width of the tunnel oxide layer 30 is greater than 3.0 eV, and it is generally difficult to transport carriers through the tunnel oxide layer 30 by thermal emission. However, the tunnel oxide layer 30 is very thin and carriers can pass through the tunnel oxide layer 30 through a tunnel effect, so the tunnel oxide layer having a thickness within a range of 0.8 nm to 2nm does not block the transport of most carriers. As the thickness of the tunnel

oxide layer gradually increases, the tunnel effect of most carriers is affected, and it is difficult to transport the carriers through the tunnel oxide layer 30, and the photoelectric conversion efficiency of the solar cell may gradually decrease. When the thickness of the tunnel oxide layer is excessively small, the tunnel oxide layer cannot have a passivation effect. As a result, in an embodiment, the tunnel oxide layer 30 is a silicon oxide layer, and the tunnel oxide layer 30 has a thickness ranging from 0.8 nm to 1.5 nm.

[00124] As an optional technical solution of the present disclosure, as shown in FIG. 6, a thickness D1 of the tunnel oxide layer on the top surface of the outermost first substructure is less than a thickness D2 of the tunnel oxide layer on a side surface of the outermost first substructure. A thickness difference (D2-D1) between the tunnel oxide layer on the top surface of the outermost first substructure and the tunnel oxide layer on a side surface of the outermost substructure is less than or equal to 0.15 nm. The thickness difference may be 0.14 nm, 0.13 nm, 0.12 nm, 0.11 nm, 0.10 nm, 0.09 nm, 0.08 nm, 0.07 nm, 0.06 nm, 0.05 nm, 0.04 nm or the like. When the tunnel oxide layer on the top surface of the outermost first substructure and the tunnel oxide layer on the side surface of the outermost substructure are excessively large, the thickness of the tunnel oxide layer has poor uniformity, a current density of the solar cell may be affected, and the open-circuit voltage of the solar cell decreases.

[00125] In S50, a polycrystalline silicon layer is formed on a surface of the tunnel oxide layer, and the polycrystalline silicon layer is doped to form a doped conductive layer, a conductivity type of the doped conductive layer is the same as that of the semiconductor substrate.

[00126] In some embodiments, the polycrystalline silicon layer is deposited on the surface of the tunnel oxide layer by any one of physical vapor deposition, chemical vapor deposition, plasma enhanced chemical vapor deposition and atomic layer deposition. The chemical vapor deposition may be low-pressure chemical vapor deposition or atmospheric chemical vapor deposition.

[00127] In an embodiment, the deposition of the tunnel oxide layer and the polycrystalline silicon layer and the doping of the polycrystalline silicon layer are all performed in a low-pressure chemical vapor deposition device.

[00128] Firstly, the alkali-polished semiconductor substrate is placed in a deposition device, an oxygen source (e.g. oxygen, nitrous oxide, or ozone) of 20 L to 60 L is introduced, and the deposition device is heated to 560°C to 620°C according to a heating rate ranging from 0.5 °C/min to 3 °C/min for a deposition time ranging from 3 min to 10 min to form the tunnel oxide layer 30.

[00129] After the introduction of the oxygen, a constant temperature phase is reached, and then an appropriate amount of silane is introduced to form a polycrystalline silicon layer.

[00130] Finally, the polycrystalline silicon layer is doped in situ to form the doped conductive layer 40.

[00131] In some embodiments, the doped conductive layer 40 may be a doped polycrystalline silicon layer. The doped conductive layer 40 and the semiconductor substrate have doping elements of a same conductivity type.

[00132] In other embodiments, a microcrystalline silicon layer or an amorphous silicon layer may also be deposited on the surface of the tunnel oxide layer 30 and doped in situ to form a doped microcrystalline silicon layer or doped amorphous silicon layer, that is, the doped conductive layer 40.

[00133] When the semiconductor substrate 10 is an N-type monocrystalline silicon, the doped conductive layer 40 is an N-type doped polycrystalline silicon layer, an N-type doped microcrystalline silicon layer or an N-type doped amorphous silicon layer, and the doping element may be an N-type doping element such as phosphorus.

[00134] In some embodiments, the doped conductive layer 40 has a thickness ranging from 60 nm to 200 nm. For example, as an N-type doped polycrystalline silicon layer, the doped conductive layer 40 has a refractive index ranging from 3.5 to 4.5.

[00135] Subsequent to S50 and prior to S60, the method further includes: performing high-temperature annealing treatment and cleaning treatment after the doped polycrystalline silicon layer is deposited in situ.

[00136] Embodiments of the present disclosure does not limit how the high-temperature annealing treatment and the cleaning treatment are performed. Illustratively, the high-temperature annealing treatment deals with the deposited polycrystalline silicon layer, which enables the polycrystalline silicon layer to better crystalize. An annealing temperature

ranges from 700°C to 1000°C.

[00137] Through the high-temperature annealing treatment, diffused pentavalent phosphorus atoms form the doped polycrystalline silicon layer. After the annealing treatment, a microcrystalline silicon phase of the crystalline silicon is transformed into a polycrystalline silicon phase, and phosphorus is deposited on the surface of the semiconductor substrate to form phosphorosilicate glass (PSG).

[00138] The cleaning treatment is intended to remove a phosphorosilicate glass (PSG) layer formed during the phosphorus doping. Due to the high concentration of phosphorus on the surface of the semiconductor substrate, a phosphorosilicate glass (PSG) layer is generally formed during phosphorus diffusion. This phosphorosilicate glass layer has a metal impurity absorption effect, may adversely affect the normal operation of the solar cell, and shall be removed.

[00139] In an embodiment, the rear surface of the semiconductor substrate may be placed downward in a chain pickling device (the chain device is at a tape speed of 1.0 /min to 2.0 m/min). The semiconductor substrate enters an acid tank to etch away the phosphorosilicate glass (PSG) layer formed on the rear surface by phosphorus diffusion. The acid tank is provided with a prepared mixed acid. The mixed acid includes hydrogen fluoride with a mass concentration of 2% to 10% and hydrogen chloride with a mass concentration of 2% to 10%. A pickling temperature ranges from 15°C to 25°C, and a pickling time ranges from about 30 seconds to 60 seconds. The front surface of the semiconductor substrate is covered with a water film, and the borosilicate glass (BSG) layer on the front surface of the semiconductor substrate may also be used as a protective layer. During the removal of the phosphorosilicate glass (PSG) layer, reaction of the front surface of the semiconductor substrate with the mixed acid is prevented.

[00140] It shall be noted that a washing process is needed after the pickling. A washing time ranges from 10 seconds to 20 seconds, and a washing temperature may range from 15°C to 25°C. In an embodiment, the semiconductor substrate may also be dried after washing.

[00141] In S60, a first passivation layer is formed on the front surface of the semiconductor substrate.

[00142] In some embodiments, the first passivation layer may be deposited by plasma

enhanced chemical vapor deposition. It is appreciated that, other methods such as organic chemical vapor deposition may also be used. Embodiments of the present disclosure does not limit implementations of the first passivation layer 20.

5 **[00143]** The first passivation layer 20 may have, but is not limited to, a monolayer or laminated structure of a silicon nitride layer, a silicon oxynitride layer, a silicon oxide layer and the like. It is appreciated that, the first passivation layer may also be other types of passivation layers. The present disclosure does not limit a specific material of the first passivation layer. For example, in other embodiments, the first passivation layer may also have a stacked structure of silicon dioxide and silicon nitride. The first passivation layer can
10 have a good passivation effect on the semiconductor substrate, which helps to improve the conversion efficiency of the solar cell.

[00144] In S70, a second passivation layer is formed on a surface of the doped conductive layer.

[00145] The second passivation layer 50 may be deposited by plasma enhanced chemical vapor deposition. It is appreciated that, other methods such as organic chemical vapor
15 deposition may also be used. Embodiments of the present disclosure does not limit implementations of the second passivation layer 50.

[00146] As an optional technical solution of the present disclosure, the second passivation layer 50 includes at least one of a silicon nitride layer, a silicon oxide layer and a silicon
20 oxynitride layer. The second passivation layer 50 has a thickness ranging from 70 nm to 120 nm. For example, the second passivation layer 50 is a silicon nitride layer. The silicon nitride layer has a low silicon to nitrogen ratio, and the silicon nitride layer has a refractive index ranging from 1.7 to 2.1, which may be 1.7, 1.8, 1.9, 2.0, 2.1 or the like, and may also be other values in the above range, which is not limited herein. The refractive index of the silicon
25 nitride layer is controlled to enable the silicon nitride layer to possess low silicon to nitrogen ratio, so that contact resistivity can be reduced during metallization of the second passivation layer 50 formed, so as to further reduce the contact resistivity of the solar cell.

[00147] In some embodiments, when the second passivation layer 50 has a stacking structure of a silicon nitride layer and a silicon oxide layer or a stacking structure of a silicon
30 nitride layer and a silicon oxynitride layer, the silicon nitride layer is located on a surface of

the doped conductive layer, and the silicon oxide layer or the silicon oxynitride layer is located on a surface of the silicon nitride layer.

[00148] Further, subsequent to S70, the method further includes: screen-printing and sintering the semiconductor substrate to form an electrode.

5 **[00149]** In some embodiments, the solar cell further includes a first electrode 60 and a second electrode 70. The first electrode 60 passes through the first passivation layer 20 to form ohmic contact with the P-type doped layer (for example, the boron-doped diffusion layer) on the front surface of the semiconductor substrate 10. The second electrode 70 passes through the second passivation layer 50 to form ohmic contact with the doped conductive layer 40. The doped conductive layer 40 and the tunnel oxide layer 30 form a passivated contact structure. The first electrode 60 and the second electrode 70 may be formed by sintering a metal conductive paste coated on surfaces of the first passivation layer and the second passivation layer. In some embodiments, the first electrode 60 or the second electrode 70 is made of a metal material such as silver, aluminum, copper or nickel.

15 **[00150]** Embodiments 1 to 13 and Comparative Examples 1 to 4 of the solar cell manufactured according to the above method are illustrated as below. Parameters are shown in Table 1.

[00151] Table 1 Parameters of the solar cell

Sample	Second texture structure	First texture structure		Thickness of the tunnel oxide layer (nm)	Thickness difference between tunnel oxide layers (nm)	First passivation layer	Thickness of the first passivation layer (nm)	Refractive index of the first passivation layer	Second passivation layer	Thickness of the second passivation layer (nm)	Refractive index of the second passivation layer
	Distance between a top and a bottom of a pyramid-shaped microstructure (μm)	Distance between a top surface and a bottom surface of a first substructure (μm)	One-dimensional size of the top surface of the outermost first substructure (μm)								
Embodiment 1	3.0	1.9	8.6	1.2	0.12	Aluminum oxide + silicon nitride	5+50	1.92	Silicon nitride	70	1.95
Embodiment 2	3.2	1.8	8.9	1.2	0.12	Aluminum oxide + silicon nitride	5+60	1.95	Silicon nitride	75	2.1
Embodiment 3	3.1	1.7	10.2	1.15	0.11	Aluminum oxide + silicon nitride	5+65	1.94	Silicon nitride	78	1.9
Embodiment 4	4.4	1.6	11.6	1.12	0.11	Aluminum oxide + silicon nitride	5+70	1.93	Silicon nitride	80	2
Embodiment 5	3.8	1.8	12.4	1.1	0.11	Aluminum oxide + silicon nitride	5+75	1.95	Silicon nitride	82	2.02
Embodiment 6	3.6	1.6	13.2	1.1	0.11	Aluminum oxide +	5+80	1.97	Silicon nitride	85	2.03

						silicon nitride					
Embodiment 7	3.5	1.7	14.5	1.1	0.10	Aluminum oxide + silicon nitride	8+85	1.98	Silicon nitride	88	1.98
Embodiment 8	3.2	1.5	12.1	1.05	0.10	Aluminum oxide + silicon nitride	10+100	1.95	Silicon nitride	90	1.96
Embodiment 9	3.0	1.6	15.6	1.02	0.10	Silicon nitride	100	1.98	Silicon nitride	95	1.97
Embodiment 10	3.0	1.5	18.2	1.0	0.10	Silicon nitride	105	1.96	Silicon nitride	98	2.07
Embodiment 11	2.8	1.9	24.8	0.95	0.12	Silicon nitride	110	1.92	Silicon nitride	100	1.95
Embodiment 12	2.7	1.4	26.3	0.95	0.08	Silicon nitride	95	2.0	Silicon nitride	110	1.96
Embodiment 13	2.8	1.5	38.4	0.9	0.08	Silicon nitride	90	1.95	Silicon nitride	120	1.97
Comparative Example 1	3.0	2.5	5.5	1.3	0.18	Aluminum oxide + silicon nitride	5+50	1.92	Silicon nitride	70	1.95
Comparative Example 2	3.0	/	/	1.4	0.18	Aluminum oxide + silicon nitride	5+50	1.92	Silicon nitride	70	1.95
Comparative Example 3	3.0	1.8	8.6	1.2	0.12	Aluminum oxide + silicon nitride	5+50	1.92	Silicon nitride	70	2.15
Comparative Example 4	3.0	1.8	8.6	1.2	0.12	Aluminum oxide + silicon nitride	5	1.52	Silicon nitride	70	1.95

* i.e., thickness difference between a tunnel oxide layer on a top surface of the outermost first substructure and a tunnel oxide layer on a side surface of the of the outermost first substructure

[00152] Table 2 shows parameters used in a deposition process of a tunnel oxide layer and a polycrystalline silicon layer thereon of the solar cell in each embodiment and in each comparative example. In the process, the silicon substrate is installed in a low-pressure chemical vapor deposition (LPCVD) device, the device is vacuumed and the temperature is raised, oxide gas (e.g., oxygen) having a loading temperature is added, and a three-stage oxidation process is conducted, in which a first oxidation period of 1.2 minutes is performed in the first stage, a second oxidation period of 1.3 minutes is performed in the second stage, and a third oxidation period of 1.5 minutes is performed in the third stage, so as to form the tunnel oxide layer on the silicon substrate. Then, the oxide gas is exhausted and nitrogen is added to form an atmosphere in the interior of the device, the temperature of the device is raised to a pre-deposition temperature, a silane gas having a loading temperature is added to the tunnel oxide layer of the silicon substrate for deposition, so as to form the polycrystalline silicon layer.

[00153] Table 2 Deposition parameters of the solar cell

Sample	Oxygen source gas loading temperature (°C)	Oxidation temperature 1 (°C)	Oxidation temperature 2 (°C)	Oxidation temperature 3 (°C)	Pre-deposition temperature (°C)	Deposition temperature for the polycrystalline silicon layer (°C)	Silane gas loading temperature (°C)
Embodiment 1	590	590	595	600	620	620	590
Embodiment 2	590	595	590	600	620	620	590
Embodiment 3	590	595	600	600	620	620	590
Embodiment 4	590	590	595	600	625	630	590
Embodiment 5	590	595	590	600	625	630	590
Embodiment 6	590	595	600	600	625	630	590

Embodiment 7	600	608	610	600	620	630	600
Embodiment 8	600	610	610	610	625	630	600
Embodiment 9	600	605	610	600	625	625	600
Embodiment 10	610	600	615	600	620	625	610
Embodiment 11	615	610	610	610	625	625	615
Embodiment 12	615	610	605	600	620	625	615
Embodiment 13	615	610	605	600	620	625	615
Comparative Example 1	590	590	590	590	610	610	605
Comparative Example 2	610	610	610	610	620	620	615
Comparative Example 3	630	630	630	630	650	650	645
Comparative Example 4	590	590	590	590	610	610	605

[00154] Table 3 Test results of the solar cell

Sample	Open-circuit voltage (mV)	Short-circuit current (A)	Fill factor	Photoelectric conversion efficiency (%)	Contact resistivity (mΩ.cm)
Embodiment 1	710	11.06	83.51	24.52	1.26
Embodiment 2	710	11.05	83.04	24.36	1.25
Embodiment 3	710	11.04	83.54	24.49	1.28
Embodiment 4	710	11.11	83.41	24.61	1.27
Embodiment 5	712	11.1	83.43	24.66	1.31
Embodiment 6	712	11.08	83.39	24.60	1.30
Embodiment 7	712	11.09	83.51	24.66	1.29
Embodiment 8	712	11.12	83.04	24.59	1.32
Embodiment 9	688	11.11	83.46	23.86	1.28
Embodiment 10	689	11.1	83.14	23.78	1.27
Embodiment 11	687	11.08	83.27	23.70	1.28
Embodiment 12	688	11.04	83.04	23.59	1.26
Embodiment 13	686	11.05	83.06	23.55	1.29
Comparative Example 1	709	11.03	82.77	24.21	1.53
Comparative Example 2	707	11.04	82.76	24.16	1.51
Comparative Example 3	710	11.04	82.645	24.23	1.54
Comparative Example 4	710	11.04	82.7	24.20	1.50

[00155] It can be seen from Embodiment 1 to Embodiment 3 that a distance between the substructures in the first texture structure of the rear surface of the semiconductor substrate is controlled within an ideal range, which can ensure that the roughness of the rear surface of the semiconductor substrate is within an appropriate range, helps to improve the uniformity of the tunnel oxide layer formed on the first texture structure, ensure better performance of the tunnel oxide layer formed, further inhibit a high local doping concentration of the doped conductive layer, reduce contact resistivity, improve the open-circuit voltage of the solar cell, and improve a fill factor and photoelectric conversion efficiency.

[00156] In the first texture structure of the solar cell according to Comparative Example 1,

in the direction away from the rear surface and perpendicular to the rear surface, a distance between a top surface of the outermost first substructure and a top surface of the first substructure adjacent thereto is less than or equal to 2 μm . The smaller the one-dimensional size of the top surface of the outermost first substructure, the thicker the tunnel oxide layer formed by deposition. The uniformity of the tunnel oxide layer decreases, resulting in a high local doping concentration of the doped conductive layer formed on the surface of the tunnel oxide layer. The contact resistivity is increased compared with that in Embodiment 1, which leads to the reduction of the open-circuit voltage of the solar cell, as well as the reduction of the fill factor and the photoelectric conversion efficiency.

10 **[00157]** The solar cell according to Comparative Example 2 is not subjected to an alkali-polishing process after texturing, the rear surface has a pyramid-shaped microstructure, and the uniformity of the tunnel oxide layer deposited on the pyramid-shaped microstructure decreases, which easily leads to a high local doping concentration of the doped conductive layer formed on the surface of the tunnel oxide layer. The contact resistivity is increased compared with that in Embodiment 1, which leads to the reduction of the open-circuit voltage of the solar cell, as well as the reduction of the fill factor and the photoelectric conversion efficiency.

20 **[00158]** Although the solar cell according to Comparative Example 3, through the treatment of the substructure of the first texture structure, inhibits a high local doping concentration of the doped conductive layer, the contact resistivity is difficult to further decrease during the metallization due to the use of a silicon nitride layer with a high silicon to nitrogen ratio. Compared with Embodiment 1, the distance between the substructures in the first texture structure of the rear surface of the semiconductor substrate and the refractive index of the second passivation layer are controlled, and a synergistic effect of the two can better reduce the contact resistivity and improve the open-circuit voltage, the fill factor and the photoelectric conversion efficiency of the solar cell.

25 **[00159]** Although the solar cell according to Comparative Example 4, through the treatment of the substructure of the first texture structure, inhibits a high local doping concentration of the doped conductive layer, the contact resistivity increases during the metallization due to the use of an aluminum oxide layer and a silicon nitride layer with a

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lower overall refractive index as the first passivation layer.

[00160] The present disclosure has been disclosed as above with preferred embodiments, the present disclosure should not be limited by those embodiments. Any person skilled in the art may make several possible changes and modifications without departing from the
5 conception of the present disclosure. Therefore, the protection scope of the present disclosure should be subject to the scope defined by the claims of the present disclosure.

CLAIMS

What is claimed is:

1. A solar cell, comprising:

5 a semiconductor substrate, wherein a rear surface of the semiconductor substrate has a first texture structure, the first texture structure includes two or more first substructures at least partially stacked on one another, and in a direction away from the rear surface and perpendicular to the rear surface, a distance between a top surface of an outermost first substructure and a top surface of an adjacent first substructure is less than or equal to 2 μm , and a one-dimensional size of the top surface of the outermost first substructure is less than or
10 equal to 45 μm ;

a first passivation layer located on a front surface of the semiconductor substrate;

a tunnel oxide layer located on the first texture structure of the rear surface of the semiconductor substrate;

a doped conductive layer located on a surface of the tunnel oxide layer, a conductivity
15 type of doping elements of the doped conductive layer being same as that of the semiconductor substrate; and

a second passivation layer located on a surface of the doped conductive layer.

2. The solar cell according to claim 1, wherein the front surface of the semiconductor substrate has a second texture structure, the second texture structure includes a
20 pyramid-shaped microstructure, the pyramid-shaped microstructure includes a top portion away from the front surface of the semiconductor substrate and a bottom portion close to the front surface of the semiconductor substrate, and in a direction away from the front surface and perpendicular to the front surface, a distance between the top portion and the bottom portion of the pyramid-shaped microstructure is less than or equal to 5 μm .

25 3. The solar cell according to claim 1, wherein for the two or more first substructures at least partially stacked on one another, in the direction away from the rear surface and perpendicular to the rear surface, the distance between the top surface of the outermost first substructure and the top surface of the adjacent first substructure ranges from 0.3 μm to 1.2

μm.

4. The solar cell according to claim 1, wherein an average one-dimensional size of the top surface of the outermost first substructure ranges from 10 μm to 15 μm.

5. The solar cell according to claim 1, wherein a thickness of the tunnel oxide layer on the top surface of the outermost first substructure is less than a thickness of the tunnel oxide layer on a side surface of the outermost first substructure.

6. The solar cell according to claim 1, wherein a thickness difference between the tunnel oxide layer on the top surface of the outermost first substructure and the tunnel oxide layer on a side surface of the outermost first substructure is less than or equal to 0.15 nm.

7. The solar cell according to claim 1, wherein the first texture structure further includes two or more adjacent second substructures that do not stacked on one another, and a one-dimensional size of a top surface of the second substructure away from the rear surface is less than or equal to 45 μm.

8. The solar cell according to claim 7, wherein the top surface of the first substructure and/or the top surface of the second substructure is a polygonal plane.

9. The solar cell according to claim 8, wherein a shape of the polygonal plane includes at least one of a diamond, a square, a trapezoid, a substantially diamond, a substantially square or a substantially trapezoid.

10. The solar cell according to claim 1, wherein the tunnel oxide layer includes at least one of a silicon oxide layer, an aluminum oxide layer, a silicon oxynitride layer, a molybdenum oxide layer or a hafnium oxide layer, and the tunnel oxide layer has a thickness ranging from 0.8 nm to 2 nm.

11. The solar cell according to claim 1, wherein the second passivation layer includes at least one of a silicon nitride layer, a silicon oxide layer or a silicon oxynitride layer, and the second passivation layer has a thickness ranging from 70 nm to 120 nm.

12. The solar cell according to claim 1, wherein the first passivation layer includes at least one of a silicon oxide layer, a silicon nitride layer, an aluminum oxide layer or a silicon oxynitride layer.

13. The solar cell according to claim 1, wherein the semiconductor substrate is an N-type monocrystalline silicon substrate, the doped conductive layer is an N-type doped

polycrystalline silicon layer, an N-type doped microcrystalline silicon layer or an N-type doped amorphous silicon layer, and the doped conductive layer has a thickness ranging from 60 nm to 200 nm.

14. A photovoltaic module, comprising a plurality of solar cell strings, wherein each of the plurality of solar cell strings comprises a plurality of solar cells, and each of the plurality of cells comprises:

a semiconductor substrate, wherein a rear surface of the semiconductor substrate has a first texture structure, the first texture structure includes two or more first substructures at least partially stacked on one another, and in a direction away from the rear surface and perpendicular to the rear surface, a distance between a top surface of an outermost first substructure and a top surface of an adjacent first substructure is less than or equal to 2 μm , and a one-dimensional size of the top surface of the outermost first substructure is less than or equal to 45 μm ;

a first passivation layer located on a front surface of the semiconductor substrate;

a tunnel oxide layer located on the first texture structure of the rear surface of the semiconductor substrate;

a doped conductive layer located on a surface of the tunnel oxide layer, a conductivity type of doping elements of the doped conductive layer being same as that of the semiconductor substrate; and

a second passivation layer located on a surface of the doped conductive layer.

15. The photovoltaic module according to claim 14, wherein the front surface of the semiconductor substrate has a second texture structure, the second texture structure includes a pyramid-shaped microstructure, the pyramid-shaped microstructure includes a top portion away from the front surface of the semiconductor substrate and a bottom portion close to the front surface of the semiconductor substrate, and in a direction away from the front surface and perpendicular to the front surface, a distance between the top portion and the bottom portion of the pyramid-shaped microstructure is less than or equal to 5 μm .

16. The solar cell according to claim 14, wherein for the two or more first substructures at least partially stacked on one another, in the direction away from the rear surface and perpendicular to the rear surface, the distance between the top surface of the outermost first

substructure and the top surface of the adjacent first substructure ranges from 0.3 μm to 1.2 μm .

17. The solar cell according to claim 14, wherein an average one-dimensional size of the top surface of the outermost first substructure ranges from 10 μm to 15 μm .

5 18. A method for manufacturing a solar cell, comprising:

texturing a semiconductor substrate, and forming a second texture structure on a front surface of the semiconductor substrate, wherein the second texture structure includes a pyramid-shaped microstructure;

10 forming a doped layer with doping elements to the front surface of the textured semiconductor substrate;

polishing a rear surface of the semiconductor substrate with an alkali solution such that a first texture structure is formed on the rear surface of the semiconductor substrate, wherein the first texture structure includes two or more first substructures at least partially stacked on one another, and in a direction away from the rear surface and perpendicular to the rear surface, a distance between a top surface of an outermost first substructure and a top surface of an adjacent first substructure is less than or equal to 2 μm , and a one-dimensional size of the top surface of the outermost first substructure is less than or equal to 45 μm ;

forming a tunnel oxide layer on the first texture structure of the rear surface of the semiconductor substrate;

20 depositing a polycrystalline silicon layer on a surface of the tunnel oxide layer, and forming a doped conductive layer by doping the polycrystalline silicon layer, wherein the doped conductive layer and the semiconductor substrate have doping elements of a same conductivity type;

forming a first passivation layer on the front surface of the semiconductor substrate; and

25 forming a second passivation layer on a surface of the doped conductive layer.

19. The method according to claim 18, wherein the polishing a rear surface of the semiconductor substrate with an alkali solution includes:

cleaning the rear surface of the semiconductor substrate with the alkali solution having a mass fraction of 5% to 15% to remove porous silicon;

30 dropping, by spraying, micro-liquid droplets of the alkali solution to the rear surface of

the semiconductor substrate for roughening treatment, and then performing pre-cleaning with a hydrofluoric acid having a mass fraction of 5% to 10%;

polishing the rear surface of the semiconductor substrate with a polishing liquid at a polishing temperature ranging from 70°C to 80°C for a polishing time less than 260 seconds, wherein the polishing liquid includes NaOH having a mass fraction of 1% to 15%, KOH having a mass fraction of 1% to 15% and an additive having a mass fraction of 0.51% to 2.5%;

removing organic components in the polishing liquid by a mixture of potassium hydroxide having a mass fraction of 5% to 15% and hydrogen peroxide having a mass fraction of 15% to 40%; and

washing and drying the polished semiconductor substrate.

20. The method according to claim 18, wherein the forming a tunnel oxide layer includes at least one of:

1) depositing the tunnel oxide layer on the first texture structure of the rear surface of the semiconductor substrate by a temperature change process and chemical vapor deposition;

2) during the deposition of the tunnel oxide layer, controlling a heating rate to range from 0.5°C/min to 3°C/min, a deposition temperature to range from 560°C to 620°C and a deposition time to range from 3 min to 10 min;

3) a deposition temperature of the tunnel oxide layer being lower than a deposition temperature of the polycrystalline silicon layer;

4) the tunnel oxide layer comprising at least one of a silicon oxide layer, an aluminum oxide layer, a silicon oxynitride layer, a molybdenum oxide layer or a hafnium oxide layer; and

5) the tunnel oxide layer having a thickness ranging from 0.8 nm to 2 nm.

ABSTRACT

Provided are a solar cell, a manufacturing method thereof, and a photovoltaic module. The solar cell includes: a semiconductor substrate, in which a rear surface of the semiconductor substrate having a first texture structure, the first texture structure includes two
5 or more first substructures at least partially stacked on one another, and in a direction away from the rear surface and perpendicular to the rear surface, a distance between a top surface of an outermost first substructure and a top surface of an adjacent first substructure being less than or equal to 2 μm ; a first passivation layer located on a front surface of the semiconductor substrate; a tunnel oxide layer located on the first texture structure; a doped conductive layer
10 located on a surface of the tunnel oxide layer; and a second passivation layer located on a surface of the doped conductive layer.

(Fig. 1)

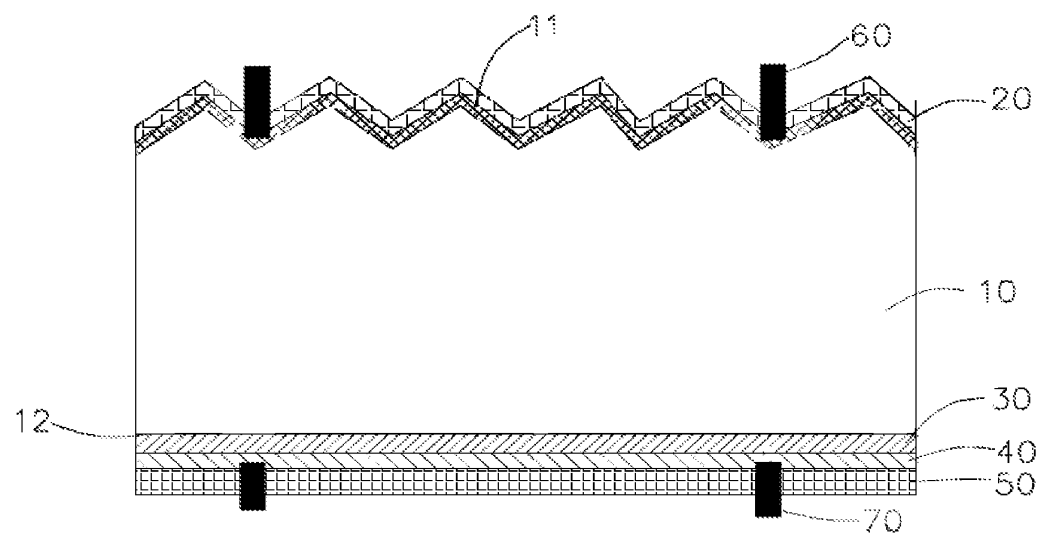


FIG. 1

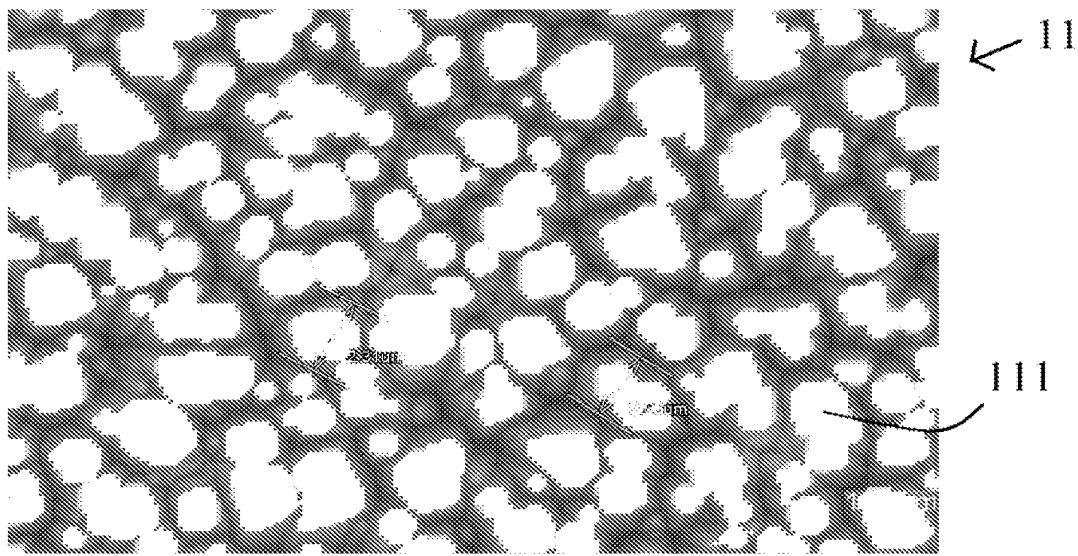


FIG. 2

2/5

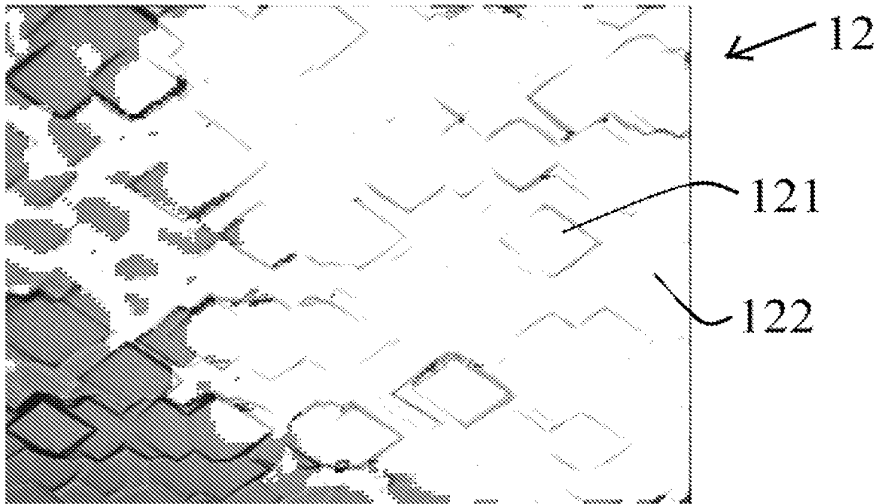


FIG. 3

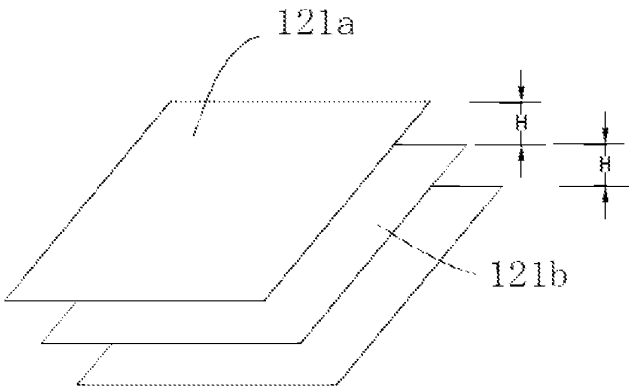


FIG. 4a

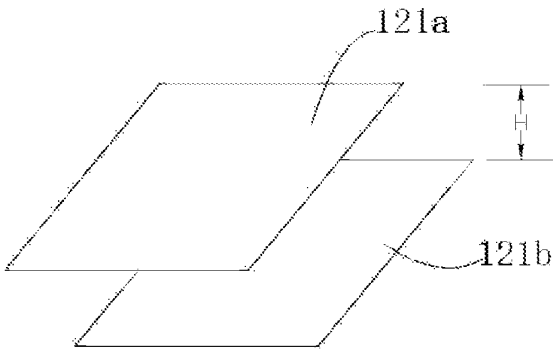


FIG. 4b

3/5

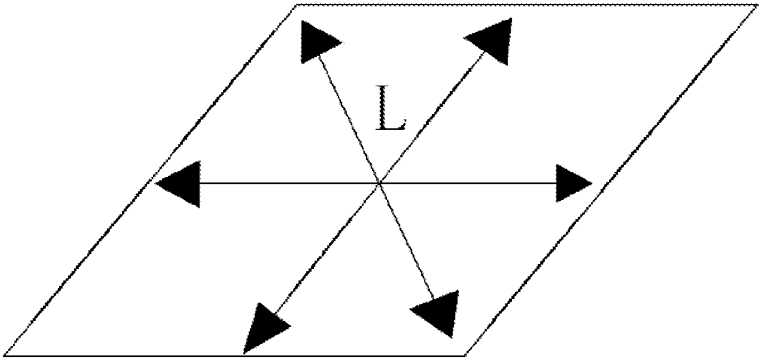


FIG. 5

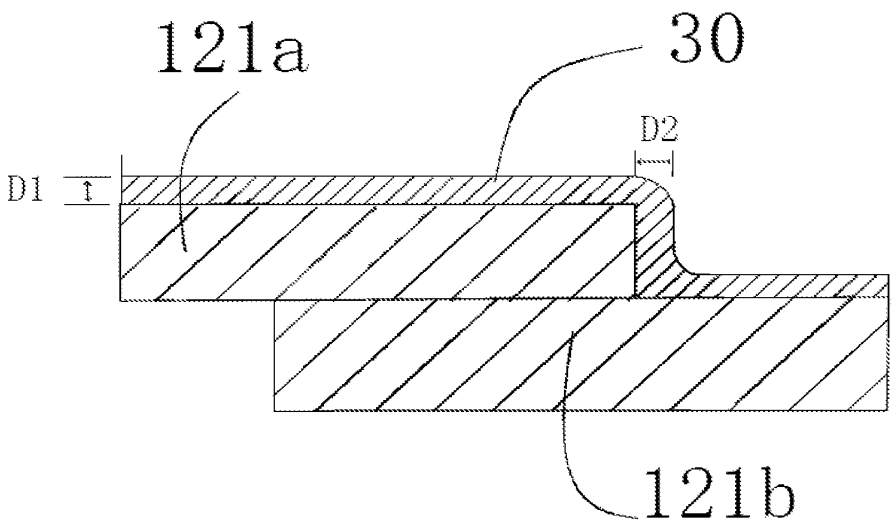


FIG. 6

4/5

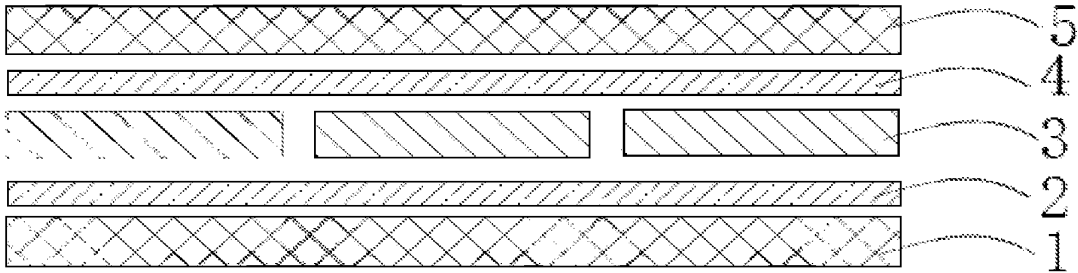


FIG. 7a

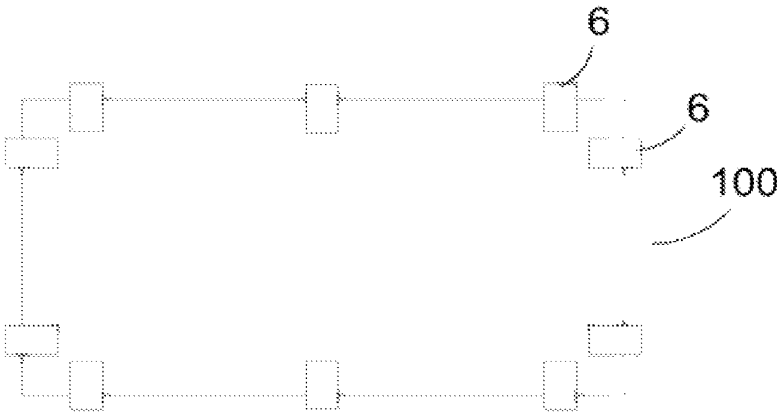


FIG. 7b

5/5

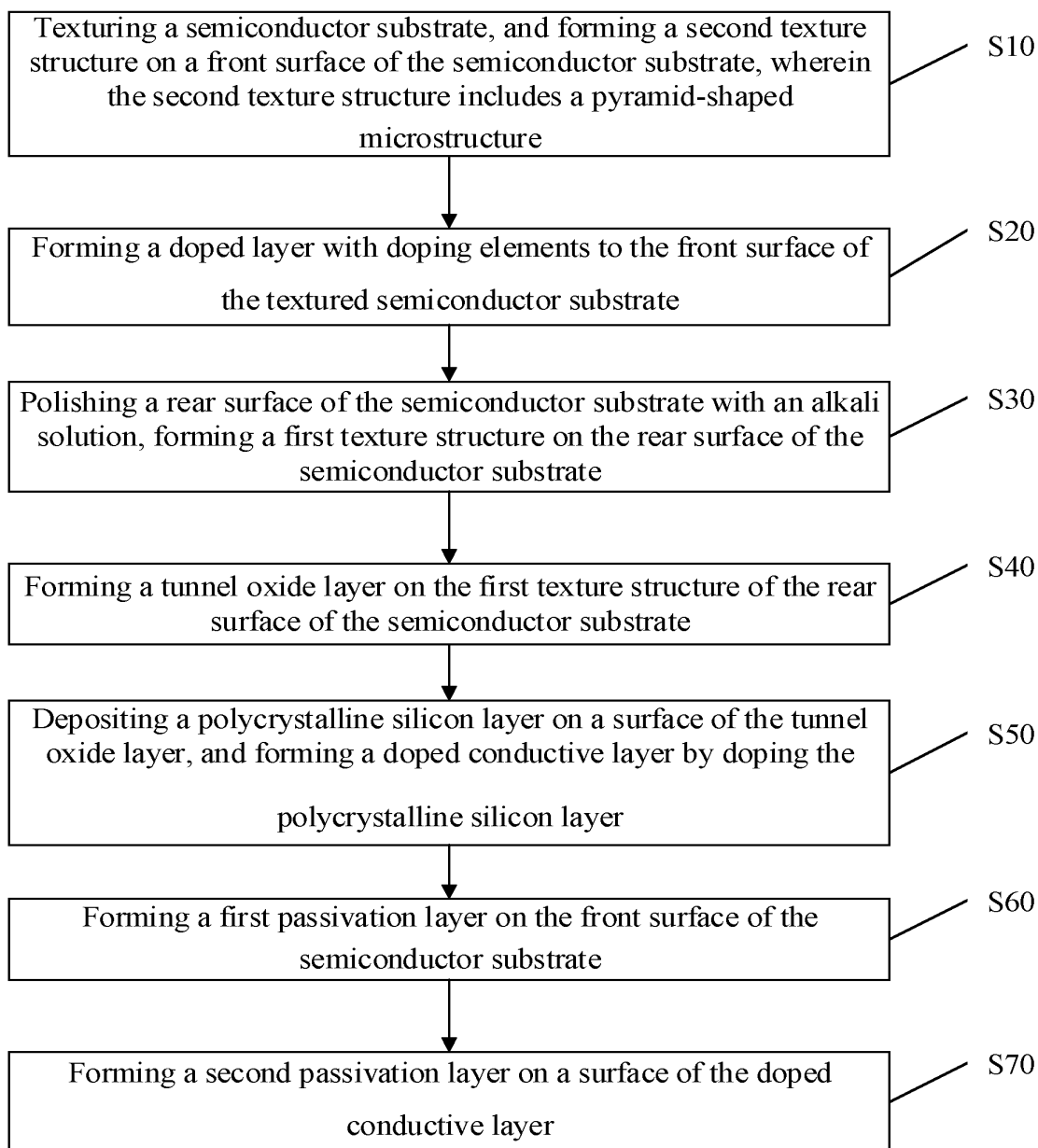


FIG. 8

DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of
Invention

**SOLAR CELL, MANUFACTURING METHOD THEREOF, AND
PHOTOVOLTAIC MODULE**

As the below named inventor, I hereby declare that

This declaration
is directed to:



The attached application, or



United States application or PCT International application number _____
filed on _____

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001
by fine or imprisonment of not more than five (5) years, or both.

WARNING:

Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available.

LEGAL NAME OF INVENTOR

Inventor: YU, Kun

Date (Optional): 2021.8.17

Signature: YU, Kun

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form or must have been previously filed. Use an additional PTO/AIA/01 form for each additional inventor.

This collection of information is required by 35 U.S.C. 115 and 37 CFR 1.63. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 1 minute to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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 PTO/AIA/US 16-423

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DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of Invention: **SOLAR CELL, MANUFACTURING METHOD THEREOF, AND PHOTOVOLTAIC MODULE**

As the below named inventor, I hereby declare that:

The declaration is checked to: ☒ The attached application, or

☐ United States application or PCT international application number _____

filed on _____

The above identified application was made or authorized to be made by me

I believe that I am the original inventor of an original joint inventor of a claimed invention in the application

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

WARNING:

Settlor/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2036 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, persons/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application, (unless a non-publication request in compliance with 37 CFR 1.273(a) is made in the application), or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is reentered in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2036 submitted for payment purposes are not retained in the application file and therefore are not publicly available.

LEGAL NAME OF INVENTOR

Inventor: **ZHANG Xinyu**

Date (optional): **2021-8-17**

Signature: **ZHANG Xinyu**

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the sole or inventive entity, must accompany this form or must have been previously filed. Use an additional PTO/AIA/US form for each additional inventor.

The collection of information is required by 35 U.S.C. 115 and 37 CFR 1.63. The information is required to obtain or retain a benefit by the USPTO which is to the land by the USPTO to process an application. Confidentiality is guaranteed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is allocated to take 1 minute to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing the burden should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22303-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22303-1450.

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Application Data Sheet 37 CFR 1.76		Attorney Docket Number	084546-000033
		Application Number	
Title of Invention	SOLAR CELL, MANUFACTURING METHOD THEREOF, AND PHOTOVOLTAIC MODULE		
The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76. This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.			

Secrecy Order 37 CFR 5.2:

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor	1				Remove
Legal Name					
Prefix	Given Name	Middle Name	Family Name	Suffix	
	Kun		YU		
Residence Information (Select One) US Residency ☒ Non US Residency Active US Military Service					
City	Haining, Zhejiang		Country of Residence ⁱ	CN	
Mailing Address of Inventor:					
Address 1	No. 58, Yuan Xi Road, Yuan Hua Town				
Address 2					
City	Haining, Zhejiang		State/Province		
Postal Code		Country ⁱ	CN		
Inventor	2				Remove
Legal Name					
Prefix	Given Name	Middle Name	Family Name	Suffix	
	Changming		LIU		
Residence Information (Select One) US Residency ☒ Non US Residency Active US Military Service					
City	Haining, Zhejiang		Country of Residence ⁱ	CN	
Mailing Address of Inventor:					
Address 1	No. 58, Yuan Xi Road, Yuan Hua Town				
Address 2					
City	Haining, Zhejiang		State/Province		
Postal Code		Country ⁱ	CN		
Inventor	3				Remove
Legal Name					

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Application Data Sheet 37 CFR 1.76		Attorney Docket Number	084546-000033
		Application Number	
Title of Invention	SOLAR CELL, MANUFACTURING METHOD THEREOF, AND PHOTOVOLTAIC MODULE		

Prefix	Given Name	Middle Name	Family Name	Suffix
	Xinyu		ZHANG	
Residence Information (Select One) US Residency ☒ Non US Residency Active US Military Service				
City	Haining, Zhejiang		Country of Residence ⁱ	CN
Mailing Address of Inventor:				
Address 1	No. 58, Yuan Xi Road, Yuan Hua Town			
Address 2				
City	Haining, Zhejiang	State/Province		
Postal Code		Country ⁱ	CN	
All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the Add button. Add				

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below. For further information see 37 CFR 1.33(a).	
☐ An Address is being provided for the correspondence Information of this application.	
Customer Number	22204
Email Address	Add Email Remove Email

Application Information:

Title of the Invention	SOLAR CELL, MANUFACTURING METHOD THEREOF, AND PHOTOVOLTAIC MODULE		
Attorney Docket Number	084546-000033	Small Entity Status Claimed	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)		Suggested Figure for Publication (if any)	

Filing By Reference:

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country ⁱ

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	084546-000033
		Application Number	
Title of Invention	SOLAR CELL, MANUFACTURING METHOD THEREOF, AND PHOTOVOLTAIC MODULE		

Publication Information:

☐	Request Early Publication (Fee required at time of Request 37 CFR 1.219)
☐	Request Not to Publish. I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application has not and will not be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32). Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.											
<table border="1"> <tr> <td>Please Select One:</td> <td>☒ Customer Number</td> <td>US Patent Practitioner</td> <td>☐ Limited Recognition (37 CFR 11.9)</td> </tr> <tr> <td>Customer Number</td> <td colspan="3">22204</td> </tr> </table>				Please Select One:	☒ Customer Number	US Patent Practitioner	☐ Limited Recognition (37 CFR 11.9)	Customer Number	22204		
Please Select One:	☒ Customer Number	US Patent Practitioner	☐ Limited Recognition (37 CFR 11.9)								
Customer Number	22204										

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, 365(c), or 386(c) or indicate National Stage entry from a PCT application. Providing benefit claim information in the Application Data Sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.

When referring to the current application, please leave the "Application Number" field blank.

Prior Application Status		Remove
Application Number	Continuity Type	Prior Application Number
Filing or 371(c) Date (YYYY-MM-DD)		
Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the Add button.		
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Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55. When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX)¹ the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(i)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

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Application Data Sheet 37 CFR 1.76		Attorney Docket Number	084546-000033
		Application Number	
Title of Invention	SOLAR CELL, MANUFACTURING METHOD THEREOF, AND PHOTOVOLTAIC MODULE		

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Application Number	Country ⁱ	Filing Date (YYYY-MM-DD)	Access Code ^j (if applicable)
202110895225.8	CN	2021-08-04	5E05
Additional Foreign Priority Data may be generated within this form by selecting the Add button.			Add

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013. NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	084546-000033
		Application Number	
Title of Invention	SOLAR CELL, MANUFACTURING METHOD THEREOF, AND PHOTOVOLTAIC MODULE		

Authorization or Opt-Out of Authorization to Permit Access:

When this Application Data Sheet is properly signed and filed with the application, applicant has provided written authority to permit a participating foreign intellectual property (IP) office access to the instant application-as-filed (see paragraph A in subsection 1 below) and the European Patent Office (EPO) access to any search results from the instant application (see paragraph B in subsection 1 below).

Should applicant choose not to provide an authorization identified in subsection 1 below, applicant **must opt-out** of the authorization by checking the corresponding box A or B or both in subsection 2 below.

NOTE: This section of the Application Data Sheet is **ONLY** reviewed and processed with the **INITIAL** filing of an application. After the initial filing of an application, an Application Data Sheet cannot be used to provide or rescind authorization for access by a foreign IP office(s). Instead, Form PTO/SB/39 or PTO/SB/69 must be used as appropriate.

1. Authorization to Permit Access by a Foreign Intellectual Property Office(s)

A. Priority Document Exchange (PDX) - Unless box A in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the State Intellectual Property Office of the People's Republic of China (SIPO), the World Intellectual Property Organization (WIPO), and any other foreign intellectual property office participating with the USPTO in a bilateral or multilateral priority document exchange agreement in which a foreign application claiming priority to the instant patent application is filed, access to: (1) the instant patent application-as-filed and its related bibliographic data, (2) any foreign or domestic application to which priority or benefit is claimed by the instant application and its related bibliographic data, and (3) the date of filing of this Authorization. See 37 CFR 1.14(h)(1).

B. Search Results from U.S. Application to EPO - Unless box B in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the EPO access to the bibliographic data and search results from the instant patent application when a European patent application claiming priority to the instant patent application is filed. See 37 CFR 1.14(h)(2).

The applicant is reminded that the EPO's Rule 141(1) EPC (European Patent Convention) requires applicants to submit a copy of search results from the instant application without delay in a European patent application that claims priority to the instant application.

2. Opt-Out of Authorizations to Permit Access by a Foreign Intellectual Property Office(s)

☐ A. Applicant **DOES NOT** authorize the USPTO to permit a participating foreign IP office access to the instant application-as-filed. If this box is checked, the USPTO will not be providing a participating foreign IP office with any documents and information identified in subsection 1A above.

☐ B. Applicant **DOES NOT** authorize the USPTO to transmit to the EPO any search results from the instant patent application. If this box is checked, the USPTO will not be providing the EPO with search results from the instant application.

NOTE: Once the application has published or is otherwise publicly available, the USPTO may provide access to the application in accordance with 37 CFR 1.14.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	084546-000033
		Application Number	
Title of Invention	SOLAR CELL, MANUFACTURING METHOD THEREOF, AND PHOTOVOLTAIC MODULE		

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.			
Applicant 1		Remove	
If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.			
		Clear	
☐ Assignee	Legal Representative under 35 U.S.C. 117		Joint Inventor
Person to whom the inventor is obligated to assign.		Person who shows sufficient proprietary interest	
If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:			
Name of the Deceased or Legally Incapacitated Inventor:			
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Organization Name	SHANGHAI JINKO GREEN ENERGY ENTERPRISE MANAGEMENT CO., LTD.		
Mailing Address Information For Applicant:			
Address 1	5/F, No. 277 Huqingping Road		
Address 2			
City	Minhang District, Shanghai	State/Province	
Country	CN	Postal Code	
Phone Number		Fax Number	
Email Address			
Additional Applicant Data may be generated within this form by selecting the Add button. Add			

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	084546-000033
		Application Number	
Title of Invention	SOLAR CELL, MANUFACTURING METHOD THEREOF, AND PHOTOVOLTAIC MODULE		

Applicant	2 Remove		
If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section. Clear			
☒ Assignee	Legal Representative under 35 U.S.C. 117	Joint Inventor	
Person to whom the inventor is obligated to assign.		Person who shows sufficient proprietary interest	
If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:			
Name of the Deceased or Legally Incapacitated Inventor:			
If the Applicant is an Organization check here. ☒			
Organization Name	ZHEJIANG JINKO SOLAR CO., LTD.		
Mailing Address Information For Applicant:			
Address 1	No. 58, Yuan Xi Road, Yuan Hua Town		
Address 2			
City	Haining, Zhejiang	State/Province	
Country	CN	Postal Code	
Phone Number		Fax Number	
Email Address			
Additional Applicant Data may be generated within this form by selecting the Add button. Add			

Assignee Information including Non-Applicant Assignee Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Assignee	1 Remove
Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication. An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.	
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Application Data Sheet 37 CFR 1.76		Attorney Docket Number	084546-000033
		Application Number	
Title of Invention	SOLAR CELL, MANUFACTURING METHOD THEREOF, AND PHOTOVOLTAIC MODULE		

Prefix	Given Name	Middle Name	Family Name	Suffix

Mailing Address Information For Assignee including Non-Applicant Assignee:

Address 1			
Address 2			
City		State/Province	
Country i		Postal Code	
Phone Number		Fax Number	
Email Address			

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Signature:

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NOTE: This Application Data Sheet must be signed in accordance with 37 CFR 1.33(b). However, if this Application Data Sheet is submitted with the INITIAL filing of the application and either box A or B is not checked in subsection 2 of the "Authorization or Opt-Out of Authorization to Permit Access" section, then this form must also be signed in accordance with 37 CFR 1.14(c).

This Application Data Sheet must be signed by a patent practitioner if one or more of the applicants is a juristic entity (e.g., corporation or association). If the applicant is two or more joint inventors, this form must be signed by a patent practitioner, all joint inventors who are the applicant, or one or more joint inventor-applicants who have been given power of attorney (e.g., see USPTO Form PTO/AIA/81) on behalf of all joint inventor-applicants.

See 37 CFR 1.4(d) for the manner of making signatures and certifications.

Signature	/Jeffrey L. Costellia, Reg. No. 35,483/		Date (YYYY-MM-DD)	2021-08-27	
First Name	Jeffrey L.	Last Name	Costellia	Registration Number	35,483

Additional Signature may be generated within this form by selecting the Add button.

Add

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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The information provided by you in this form will be subject to the following routine uses:

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7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
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Electronic Patent Application Fee Transmittal				
Application Number:				
Filing Date:				
Title of Invention:		SOLAR CELL, MANUFACTURING METHOD THEREOF, AND PHOTOVOLTAIC MODULE		
First Named Inventor/Applicant Name:		Kun YU		
Filer:		Jeffrey Costellia/Donald Sias		
Attorney Docket Number:		084546-000033		
Filed as Large Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
UTILITY APPLICATION FILING	1011	1	320	320
UTILITY SEARCH FEE	1111	1	700	700
UTILITY EXAMINATION FEE	1311	1	800	800
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				1820

Electronic Acknowledgement Receipt	
EFS ID:	43621768
Application Number:	17459689
International Application Number:	
Confirmation Number:	8617
Title of Invention:	SOLAR CELL, MANUFACTURING METHOD THEREOF, AND PHOTOVOLTAIC MODULE
First Named Inventor/Applicant Name:	Kun YU
Customer Number:	22204
Filer:	Jeffrey Costellia/Donald Sias
Filer Authorized By:	Jeffrey Costellia
Attorney Docket Number:	084546-000033
Receipt Date:	27-AUG-2021
Filing Date:	
Time Stamp:	17:07:06
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	\$1820
RAM confirmation Number	E20218QH07192184
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The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

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Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		084546_000033_Specification_ and_Drawings.pdf	744999	yes	48
			9fa4aa4c3990e855229f6b28068ee867d2d90aef		
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Specification		1	37	
	Claims		38	42	
	Abstract		43	43	
	Drawings-other than black and white line drawings		44	48	
Warnings:					
Information:					
2	Oath or Declaration filed	084546_000033_Declaration. pdf	2279481	no	3
			2e7f28007a7ee98f12a3115a2ea3600c25eb016c		
Warnings:					
Information:					
3	Application Data Sheet	084546_000033_Application_D ata_Sheet.pdf	1276214	no	9
			cae8ab8861ce0ba69fb626a8df06c5cb4fdff4401		
Warnings:					
Information:					
4	Fee Worksheet (SB06)	fee-info.pdf	43982	no	2
			f2996a2407469d877e2bdcefb89f576bd9dc0c076		
Warnings:					
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Total Files Size (in bytes):			4344676		

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If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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Application Number: 17459689

Document Date: 08/27/2021

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